Hybrid EMI Filter for Common Mode Noise Reduction at VSI output

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***Abstract*—A hybrid EMI filter has been designed to show their effectiveness at improving inverter common mode output noise. The filter has been constructed using the TI TPSF12C1 active EMI filter and the minimal size and amount of passive filter components. Performance tests with and without the active filter enabled show that there is a significant increase in filter performance in the range from 150 kHz to 1 MHz. Additional limit tests of the active filter show that the TPSF12C1 can also effectively be used outside of the manufacturer's recommended parameters. The active filter is still effective when its output is clipping slightly and when a 400 Hz main frequency is used.**

***Index Terms*—Common mode, VSI, Hybrid EMI filter, AEF, TPSF12C1**

I. Introduction

The number of electronic converters used in households and vehicles is steadily increasing. Some examples of this are the rise in electric vehicles and the switch to LED lighting. Common converters used in such devices are a switched mode power supply (SMPS) for AC/DC conversion and Voltage Source Inverters (VSI) in motor drives. These devices share a similar noise source of transistor switching using square wave signals to obtain the desired output signal. These signals can produce a lot of harmonic distortion, as seen by applying a Fourier transform [1]. The relatively high frequencies used in some converters require a signal with a high slew rate, which increases the harmonic distortion of the converter. The increasing use of GaN and SiC transistors, which usually have much shorter rise and fall times than Si transistors, increases electromagnetic interference (EMI) emission [2].

At an inverter's output, this noise current can lead to multiple problems. Some general problems with this noise are that it can radiate and/or shorten the life of devices connected to it. There are, however, also problems specifically related to common mode (CM) current, consisting of bearing current in motors and ground voltage [3][4]. Even without these known issues, this noise may not exceed electromagnetic compatibility (EMC) limits, such as the DO-160 limits [5] for airborne devices.

One commonly used method for the reduction of EMI is using a passive EMI filter (PEF) [4]. These are low-pass filters consisting of inductors, capacitors and chokes. In practical applications, the common mode choke (CMC) is often the most bulky/heavy component of the filter [6]. One reason for their large size is that the capacitance to ground is limited due to leakage current to the ground, such as described in for example the CISPR 32 standard [7]. This means that the CM filter performance is usually increased by increasing the size of the CMC.

Another form of EMI mitigation can be achieved with a active EMI filter (AEF). These filters all follow the same basic principle consisting of three parts. First, the noise is measured, then a counter signal is generated which is then injected back into the powerline. To reduce possible issues with delays and phase matching, a simple circuit is preferred. Sensing and injecting can be done with either a voltage or current. The signal generation can be straightforward in the form of an amplifier with negative gain. More complex signal processing can however also be done to target only the switching frequency of the electronic converter and its harmonics.[1]

Both of these filters are however limited in their bandwidth and insertion loss. Namely, the bandwidth of a PEF is limited since the components become excessively large and heavy. On the other hand, a AEF is only effective at lower frequencies due to the limited gain-bandwidth product of their amplifiers. Therefore, combining both filters in a hybrid EMI filter (HEF) can be very effective at EMI mitigation.[1]

A HEF also enables a size reduction of the passive components. Since the active part of the filter improves mostly the low-frequency insertion loss, the passive components can be downsized while still having an insertion loss greater than or equal to only using a PEF.[8] Active and hybrid filtering is, however, not very common for filtering VSI output noise [2].

The main goal of this paper is to design a HEF using Commercial Off-the-shelf (COTS) components. The focus of the filter design is to minimize the size and number of the passive components while retaining filter performance. The goal is reached by using the following sections: Section II dives deeper into inverter and EMI filter theory, Section III covers the construction of the measurement setup in simulation and practice together with the filter design, then Section IV consists of results from measurements and simulations, after which conclusions are drawn in Section V.

II. Theoretical Analysis

This section first covers inverter theory, with a focus on the control scheme and noise generation. The following section contains the main principles behind passive filtering, including

component parasitics. The last subsection consists of AEF theory and the chosen COTS part.

A. Inverters

Inverters are power converters that deliver AC power from a DC source. The most common types are switched-mode inverters with either 2 or 4 transistors. These are called half-bridge and full-bridge inverters respectively. An AC signal is created by using these transistors as switches and alternating which switch is turned on. The control signal to the transistors determines the output signal and its noise signature. The useful output power of an inverter consists purely of the differential mode (DM) signal. The CM current at the output of the inverter thus only consists of unwanted noise.[9]

An example of this is sinusoidal Pulse Width Modulation (SPWM), where the on-and-off time of the transistors changes according to the amplitude of a reference sine wave. This effect can be achieved by comparing the reference sine wave to a triangular waveform and setting the output high when it is greater than the triangular wave, as seen in Fig. 1. The output of the inverter can be tuned by changing the characteristic variables of this control signal. Three main variables of this control signal are the sine (F1) and triangle frequencies (Fs) and the modulation amplitude (ma). Both frequencies determine where peak amplitudes are in the frequency spectrum. The modulation amplitude is a factor of the sine wave amplitude compared to the triangular wave amplitude, which linearly determines the output frequency in the range from 0 to 1. In Fig. 1, F1, Fs and ma are 50 Hz, 500 Hz and 0.8 respectively.

Lastly, a delay between the control signals of an inverter's top and bottom transistor, known as dead time, is given in practical applications to ensure that the transistors cannot be active simultaneously, thus creating a short between the supply lines. The minimum required dead time is determined by the control signal's rise and fall time and the transistors' threshold voltage.[9]

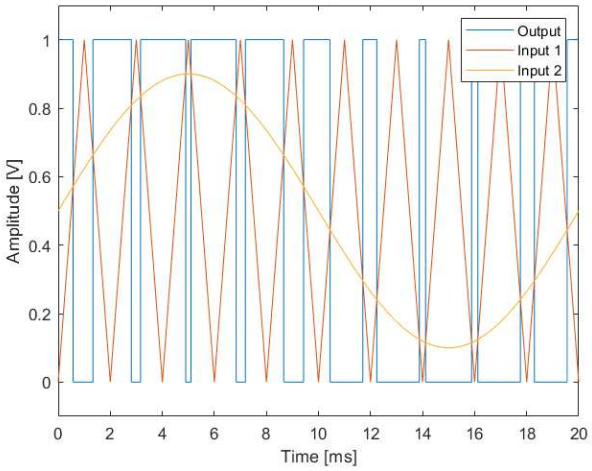


Figure 1. SPWM control signal generation (F1 = 50 Hz, Fs = 500 Hz, ma = 0.8)

The noise generated from SPWM switching has a distinct shape, as seen in Fig. 2. It consists of peaks at odd harmonics of the switching/triangular wave frequency with side peaks at multiples of Fs±F1. The envelope of these harmonics decreases with 20 dB/decade up till the frequency corresponding to the rise/fall time of the PWM signal, after which the envelope decreases with 40 dB/decade [9] [10].

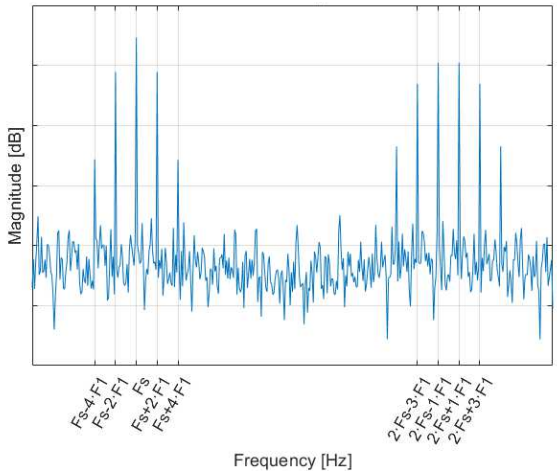


Figure 2. Noise at the output of a SPWM inverter

B. Passive Filters

A PEF is made to attenuate two specific noise types, namely CM and DM noise. These noise currents and an example filter can be seen in Fig. 3. In CM, a current of the same phase and magnitude flows in the phase and neutral conductor. The earth line is then the return for both currents. In practical circuits, this return current can however be different from the sum of the line and neutral currents due to radiated noise. DM currents, on the other hand, flow from line to neutral [11]. In practice, these noise currents are present at the same time, which is also called normal mode (NM).

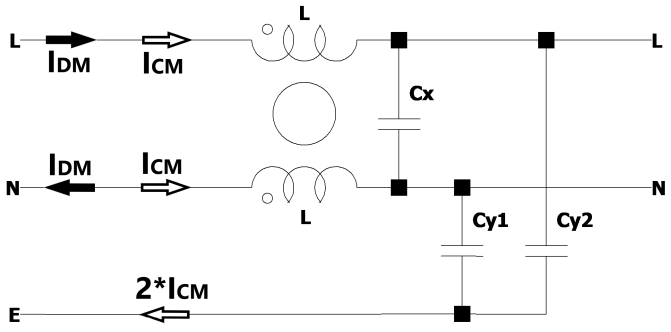


Figure 3. Simple EMI filter with ideal currents

As mentioned in the introduction, a PEF usually only consists of inductors, capacitors and chokes for CM and DM noise rejection [11]. A CMC and y-capacitors between line and neutral to ground are used for common mode noise. Differential mode noise is filtered by an x-capacitor between

line and neutral with the possible addition of inductors or a differential mode choke (DMC). The naming for the capacitors in EMI filters is related to their rating in the IEC 60384-14 standard [12].

EMI filters all consist of the same basic filtering circuits: L, C, LC, CL, π and T. π and T refer to CLC and LCL filters respectively [13]. These filters can be seen in Fig. 4, where the filters are either from line to neutral or from line and neutral to ground to represent DM and CM noise filters respectively. The effectiveness of the filters is indicated by their attenuation above the cut-off frequency in dB/decade. It should also be mentioned that all filters have two additional impedances in the form of source and load impedance.

The choice between these different circuit topologies depends on the required insertion loss (IL), source impedance, and load impedance. According to [13], the inductors should be coupled with low impedances and capacitors should be coupled with high impedances for highest IL. This can be seen when calculating the insertion loss of the basic filter topologies, as is also done in [14] and [15]. These basic topologies can be combined or multiplied when even higher IL is required. For example, a CLC-LC filter can theoretically reach an attenuation slope of -100 dB/decade.

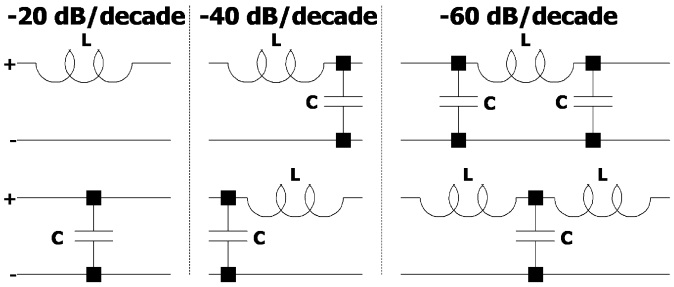


Figure 4. Basic EMI filter topologies

The bandwidth for the low pass filter is limited since all components contain parasitic elements, as seen in Fig. 5. In the case of a capacitor, the main parasitics are the series inductance and resistance. For an inductor, these are a series resistance and parallel capacitance. A parallel resistor can also be added to represent that the conduction at resonance is finite. Another effect that can limit the performance of an inductor is saturation. It occurs when the current through the inductor, and thus also the magnetic field according to Ampere's law, is sufficiently large that the core approaches a maximum magnetic field. When this happens, the permeability of the core material reduces significantly and thus also the inductance [11].

Since the parasitic components are significantly smaller than the main wanted characteristic, these components only start having an effect at high frequencies (except for the inductor's series resistance, which limits DC current). The effect of the parasitic of a capacitor can be seen in Fig. 6. Three x-rated capacitors with the same pitch but different capacitance values are displayed. It can be seen that the largest capacitor reaches

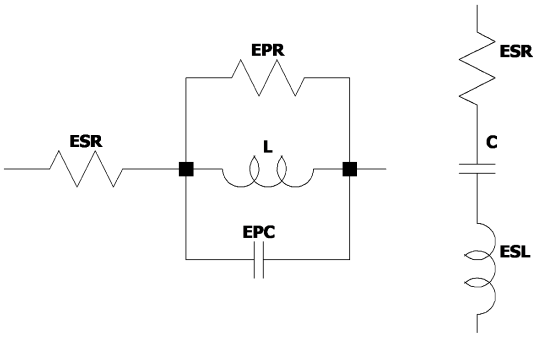


Figure 5. Parasitic equivalent circuits of an inductor and capacitor

the highest insertion loss, but also has a slightly higher series inductance from its physical size increase. Next to these, there is also a capacitor with a smaller pitch. This smaller pitch gives a smaller series inductance.

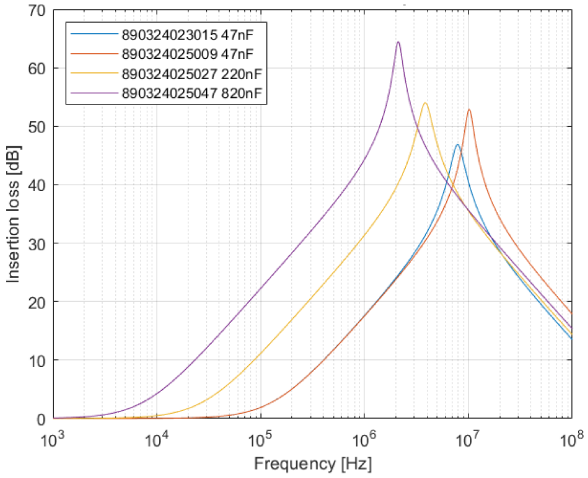


Figure 6. Insertion loss of realistic x-capacitors [16]

The chokes in these filters are components that ideally should only affect the current of a single mode while leaving the current in the other mode unaffected. This is achieved by winding two inductors around the same toroidal core material, which is comparable to a transformer structure. If the coils are connected such that the current flows in the opposite direction, as seen in Fig. 3, only CM currents will be rejected. This can be explained by looking at the magnetic field induced by both windings. Namely, when CM currents are applied, the magnetic fields of both coils will have a similar direction and thus constructively interfere. This causes the inductance of the coils to ideally be twice as high due to the mutual inductance incurred by this interference ($L + M = 2 \cdot L$). DM currents induce destructively interfering fields, ideally resulting in no inductance ($L - M = 0$). Using this knowledge, the circuit in Fig. 3 can simplified to equivalent models for both modes. The CM equivalent consists of two LC filters and the DM equivalent consists of only the x-capacitor, without considering non-idealities.

For CMCs it is possible to use the same core size for a range of different inductance values. The additional windings in some higher inductance chokes do, however, need to be more closely spaced to fit on the same core, which increases the parasitic capacitance of the CMC. This can be seen for the 15 mH choke in Fig. 7, where the insertion loss of nanocrystalline chokes with the same core size is compared. The other chokes have a similar parasitic capacitance, which is indicated by their roughly overlapping curves above 30 MHz.

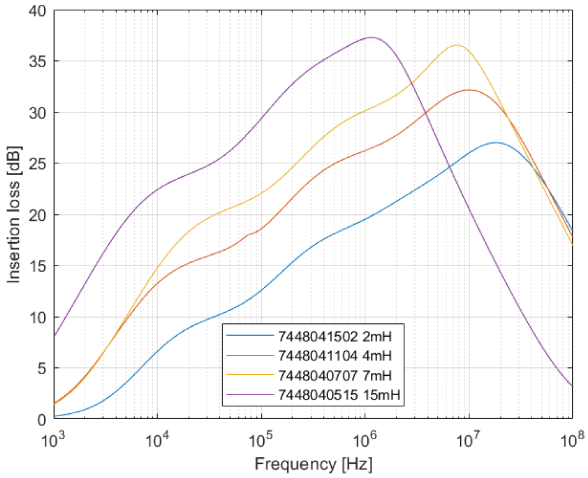


Figure 7. Insertion loss of realistic nanocrystalline CMCs with the same core size[16]

The core material is also of critical importance to the CMC performance, as can be seen in Fig. 8. The most common core material, MnZn, is most effective at lower frequencies, while nanocrystalline cores have a more broadband attenuation [16]. The choice for core material becomes especially important when including the AEF since it can significantly influence loop stability.

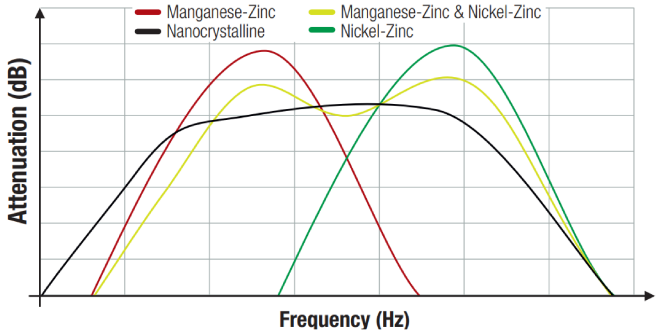


Figure 8. Attenuation of CMCs with different core materials[17]

C. Active filtering

Active filtering consists of three main parts: Sensing, Amplifying, and Injecting. Sensing and Injecting are relatively similar since they need to interface with the main power lines in such a fashion that preferably isolates the active filter from the relatively high voltages. The amplifier can be used in either a feedback or feed-forward topology [18]. In a feedback AEF, the noise is measured at the EMI victim. The amplifier then creates a signal that counters the noise signal, such that adding them in the injecting stage causes destructive interference between the noise and the synthesized anti-noise. A feed-forward topology measures noise at the source and injects the anti-noise at the victim with unity gain.

Sensing and Injection can mainly be done by adding an extra winding to a CMC or using a capacitor. For sensing, the capacitor gives a voltage, while the CMC winding gives a current. The opposite is true for injecting, where a capacitor is used for current injection and an extra winding for voltage. The effect of different sensing methods and feed-forward or feedback on the insertion loss of the AEF can be seen in Table I.

Table I
INSERTION LOSS OF DIFFERENT AEF TOPOLOGIES[6]

AEF Topology		Control (FB/FF)	Sensing (VS/CS)	Injection (VI/CI)	Insertion Loss (IL)
a	FB-CSVI	Feedback	Current	Voltage	$\left\|1+\frac{G}{Z_S+Z_L}\right\|$
b	FB-CSCI	Feedback	Current	Current	$\left\|1+\frac{Z_S}{Z_S+Z_L}\cdot G\right\|$
c	FB-VSVI	Feedback	Voltage	Voltage	$\left\|1+\frac{Z_L}{Z_S+Z_L}\cdot G\right\|$
d	FB-VSCI	Feedback	Voltage	Current	$\left\|1+\frac{G}{Y_S+Y_L}\right\|$
e	FF-VSVI	Feedforward	Voltage	Voltage	$\left\|\frac{1}{1-G}\cdot\left(1-\frac{Z_S}{Z_S+Z_L}\cdot G\right)\right\|$
f	FF-CSCI	Feedforward	Current	Current	$\left\|\frac{1}{1-G}\cdot\left(1-\frac{Z_L}{Z_S+Z_L}\cdot G\right)\right\|$

In March of 2023, Texas Instruments released the first stand-alone AEF IC, namely the TPSF12C1 [8]. This active filter's application is EMI reduction from mains-powered AC/DC converters. This filter improvement is then used to reduce the inductance of CMCs. The active filter is especially effective for this purpose since it operates from 100 kHz to 3 MHz [19]. As mentioned in the introduction, this enables a reduction in CMC inductance and can lead to an increase in filter bandwidth and reduction of filter size. The goal of reducing magnetic component size also explains the choice for a VSCI topology, since there do not need to be extra windings around the CMC core. [6][18]

Since the active filter injects and senses using capacitors, it can be compared to a y-capacitor. The contribution of the AEF can then also be rewritten to an effective capacitance. By simplifying the IC to an inverting amplifier and using the fact that the output voltage is looped back to the input through the inject capacitor, the effective capacitance is derived to get Eq. 1[6]. There is however no equation available for the loop gain. It also cannot be completely derived since the exact layout and signal path of the IC are not public. An example of this is the feedback network between the COMP1 and COMP2 pins, which is important for the loop gain, but whose connection to the amplifier is not documented.

$$V_{Cinj} = [1 - G_{AEF}(F)]V_{sens}$$
$$I_{Cinj} = C_{INJ}\frac{dV_{Cinj}}{dt} = [1 - G_{sens}(F)]C_{INJ}\frac{dV_{AEF}}{dt}$$
$$C_{INJ,eff}(f) = |1 - G_{AEF}|C_{INJ} \quad (1)$$

TI recommends a passive filter setup consisting of at least 2 CMCs, in between which the filter IC senses and injects its signal. An x-capacitor between the chokes effectively acts as a short between the power lines at the frequencies of interest for the AEF. This means that only 1 inject y-capacitor is required. The high impedance given by the CMCs serves two purposes; giving high insertion loss as seen in Fig. I and reducing the sensitivity of the loop gain to changes in source and load impedances. An evaluation model, shown in Fig. 9, and design tips are available in [20]. The passive filter is rated for a maximum of 265 Vrms and 10 A. It has a CLC-LC structure for both CM and DM noise, with the DM inductance being the "leakage" inductance of the CMCs. The middle y-capacitors have been replaced by a single inject capacitor and 2 sensing capacitors.

The AEF has a feedback loop through the passive filter. This does however require a compensation network, which trades amplifier gain for loop stability. This network consists of the components to the right of the TPSF12C1, which makes the effective AEF impedance from neutral to the ground of Eq. 2 [6]. The 3 distinct branches, labeled D1, D2, and D3, are given capacitances and resistances which provide specific current paths depending on frequency [19]. At low frequencies, the LC resonance of the CMCs and the inject capacitor requires damping. The equivalent circuit that achieves this and loop stability consists of R_{D1}, C_{D2}, and R_{D3}. When frequency increases above roughly 10 kHz, C_{D1} becomes more dominant in its branch. This provides lower series impedance with the inject capacitor and thus increases the AEF attenuation. Increasing the frequency further will make C_{D3} and R_{D2} more dominant in their respective branches, which results in lowering the impedance of branch D3 and a high pass filter consisting of C_{D1} and R_{D2}. These changes both serve to maximize the Filter attenuation. Lastly, above 100 kHz, R_{D1A} starts to dampen the AEF output for increased stability at high frequencies.

$$Z_{AEF}(s) \approx \frac{Z_{INJ}(s) + Z_{D3}(s) + (Z_{D1}(s)||Z_{D2}(s))}{1 - G_{AEF}(s)\frac{Z_{D2}(s)}{Z_{D1}(s)+Z_{D2}(s)}} \quad (2)$$

where:

$$Z_{D1}(s) = (Z_{Rd1a} + Z_{Cd1}(s))||Z_{Rd1}$$
$$Z_{D2}(s) = Z_{Rd2} + Z_{Cd2}(s)$$
$$Z_{D3}(s) = Z_{Rd3}||Z_{Cd3}(s)$$

The equation for the AEF impedance again shows a dependence on the loop gain of the AEF. From the IC simplification to an inverting amplifier, the ideal gain range is 0 to -∞. When the AEF is disabled, and thus the gain is zero, the denominator

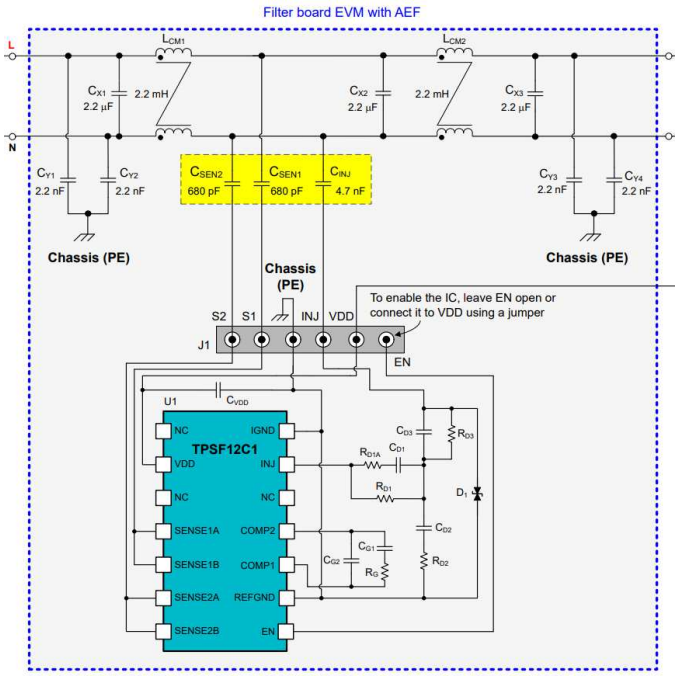


Figure 9. TPSF12C1 Evaluation filter board [19]

becomes 1, which leaves only the numerator. This shows that the compensation network becomes a y-capacitor with increased series impedance. Going to the other side of the gain range shows that the effective impedance of the AEF decreases with increasing gain, which is comparable to using larger y-capacitance in passive filters. Instead of trying to calculate the impedance, TI recommends design flow in [20] instead. This consists of using their "quickstart calculator" spreadsheet and simulation models to design a filter using the TPSF12C1.

III. Methodology

To test and validate filter designs, a PSpice simulation is created. However, as mentioned in the analysis, it is important to consider parasitic components. The devices used in the practical setup must be known to identify these accurately. In Fig. 10, the test setup adapted from [21] and [2] can be seen. The equipment used in the practical setup from left to right is: a Tenma 72-2720 DC power supply, 2 Tekbox TBOH01 Line Impedance Stabilization Networks (LISNs), a GaN Systems GS66516T-EVBDB2 dual GaN transistor evaluation board, the filter designs from this paper and a TE2000B8R2J power resistor. A Teledyne LeCroy T3AFG120 arbitrary waveform generator supplies the SPWM signal required for inverter operation. A sample frequency of 150 kHz is used for all tests since most of the noise generated by the inverter then falls within the range of the AEF and the DO-160 standard. Since the TPSF12C1 has an internal line reject filter made for line frequencies [19], a main frequency of 50 Hz is used for most measurements.

In the following subsections, the PSpice model will be further elaborated. Then there is a section about the measurement

setup used in conjunction with the test setup mentioned above. Lastly, the filter design considerations are given.

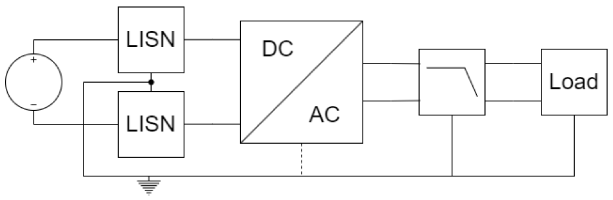


Figure 10. Simplified test setup layout

A. Simulation

According to [21], the most important parts of the setup that should be accurately modeled consist of the LISNs, DC Link capacitor, transistor model, and load model. Fortunately, the model for the LISNs can be obtained from its datasheet [22]. The parasitics for the DC link capacitor on the GaN evaluation board, [23], can similarly be obtained from its datasheet [24]. The GaN transistors can be modeled using their PSpice library [25]. Lastly, a load model needs to be constructed since the RLC equivalent circuit parameters are not readily available. The implementation of these parts is described in the sections below. The complete circuit can be seen in Appendix A.

1) Control signal generation: The complete control circuit can be seen in Fig. 11. SPWM signal generation is performed as described in the analysis, meaning that a triangular and sine wave are compared in a behavioral voltage source. The signal is then split into two branches with an inverted signal. Next, the dead time is added by combining the signal with a time-shifted version of itself with an AND gate. This effectively delays the rising edge of the SPWM signal. Since ideal PSpice control components are used, the signal has extremely steep slopes. As stated in the analysis, this influences the SPWM noise spectrum. Therefore, the slew rate is limited using an RC circuit. To match the datasheet and measured signals, the dead time is set to 100 ns and the RC time to 20 ns.

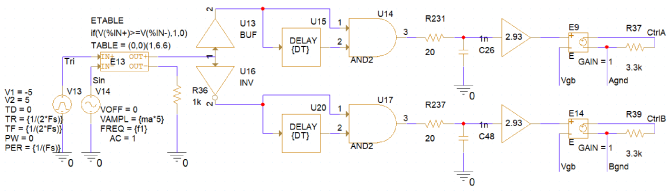


Figure 11. SPWM generation and gate-driving circuit

The last part of the control signal generator is the gate-driving circuit. The gain and Voltage Controlled Voltage Source (VCVS) change the logic levels from 0 and 3.3 V to -4 and 6 V respectively [23]. For the transistors to switch, however, these voltages need to be the gate-source voltage, which is done by setting the ground level of the VCVS equal to the source voltage of the transistor. This last step should be repeated for each transistor to make this control circuit work for a full bridge inverter.

2) Inverter: The inverter can be made in either a half or full-bridge configuration. There is however a large difference in CM noise current at the output of the inverter. The main difference is that the noise cancels when there is a perfectly symmetric load for a full-bridge inverter, which does not happen when using a half-bridge inverter. This effect can be seen when comparing the simulation of symmetrically distributed common mode capacitance non-symmetrical situations, as seen in Fig. 12. The line for symmetrical capacitance is well below 0 dBμA, thus it is not visible in the graph. An additional trace with mismatched capacitors has been added to see the effect of using two equal capacitors within 10% capacitance tolerance. It shows the importance of considering the manufacturers' tolerance when simulating since it can greatly impact noise current. The shape of the noise spectrum results from the noise spectrum combined with the capacitive current path. Namely, the increasing conductance of the current path and decreasing noise magnitude over frequency cancel to leave a roughly flat noise spectrum. At higher frequencies, the parasitic inductance determines the slope of the noise spectrum.

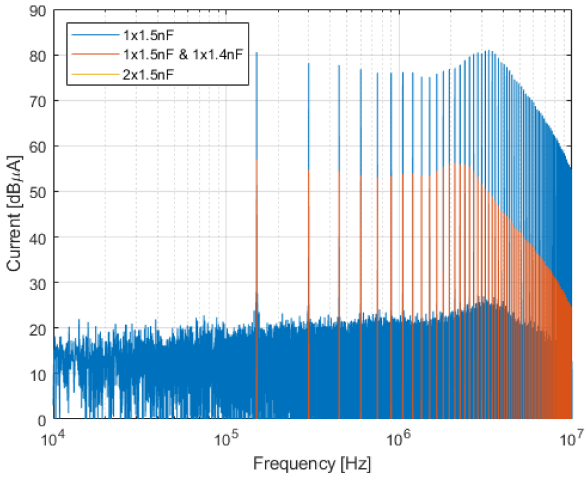


Figure 12. CM current Simulations of different load capacitance distributions using a full bridge inverter (the yellow line is below 0 dBμA and therefore not visible)

A likely cause for this noise caused by asymmetry is mode conversion [2]. This is a phenomenon where DM noise is converted into CM noise. If mode conversion is the cause of the CM current, a DM filter should attenuate the CM noise significantly. Simulations show that this filter removes almost all of the CM noise, confirming that it is only caused by mode conversion.

3) Power resistor: To determine the power resistor's series inductance and parallel capacitance, the power resistor can be connected in series with a 2-port VNA. The CM parasitic capacitance to the ground can be measured by connecting both terminals of the power resistor to the transmitter and connecting the receiver to the ground plane. For these measurements, the Rohde&Schwarz ESPI EMI test receiver is used with its optional Tracking Generator (TG). This setup can be used

instead of a Vector Network Analyzer (VNA) since only the S21 magnitude is of interest. The equivalent circuit parameters can then be extracted by fitting the RLC model to corner frequencies in the measurements.

For the DM measurement, this is more specifically the low-frequency resistive attenuation, the transition into inductive behavior, and the resonance between the parasitic inductance and capacitance. As seen from Fig. 13, there is some constant attenuation in the region from 10 to 100 kHz. Using this attenuation and the fact that the source and receiver have 5 Ω impedance, the resistance is calculated to be 8.3 Ω. The parasitic inductance gives a 3-dB cut-off frequency of around 1.5 MHz, which resonates with the capacitance at 18 MHz. Considering these transitions, the equivalent model has 10 μH inductance and 8 pF capacitance.

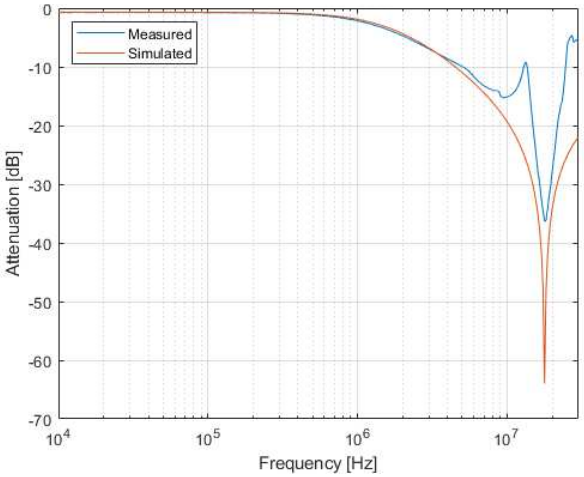


Figure 13. DM measurement of the power resistor with the output of the simulated DM equivalent circuit

The CM measurement, as seen in Fig. 14, shows a slope of +20 dB/decade, meaning there is only capacitive behavior in this frequency span. Adding this parasitic capacitance to the simulation and fitting it to this line gives a CM capacitance of roughly 80 pF. The clear distinction between DM and CM conduction path indicates that the CM noise current is independent from the DM current. This means that the CM current only depends on the voltage and switching scheme.

B. Practical setup

The test setup using the devices mentioned before can be seen in Fig. 15. For safety reasons, the main supply voltage is to the relatively low voltage of 20 V. A second power supply, EA-PS 3080-20, is added to supply the AEF with nominally 12 V. An oscilloscope with two probes measures the AEF performance and voltage across the load. The active filter output is evaluated at its measure point after the compensation network but before the injection capacitor. The voltage across the power resistor is measured using a differential voltage probe. The R&S ESPI is used with an FCC F-33-2 Current probe to measure the common mode noise current after the EMI filter. It has a frequency-dependent transfer impedance,

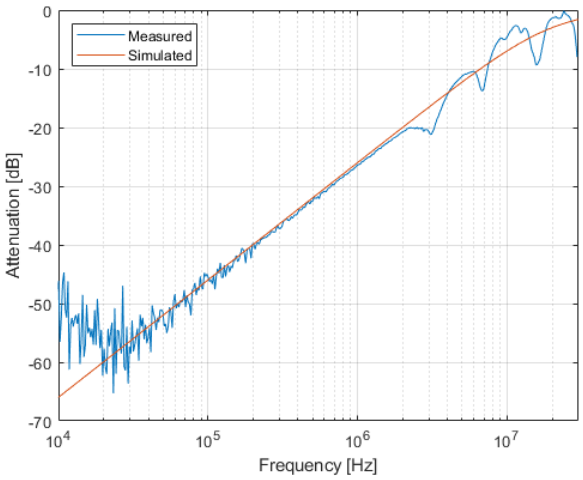


Figure 14. CM measurement of the power resistor with the output of the simulated CM equivalent circuit

which is added to the calibration of the ESPI [26]. The scan settings for the ESPI in Table II have been adapted from the DO-160 conducted EMI standard. Deviations from the standard are mainly put in place to make the results of the measurements more comparable to simulations. This means that a measurement with a flat noise floor, resulting from a constant resolution bandwidth is preferred over switching it dependent on the frequency band. The final setup also has the inverter and power resistor floating above the ground plane to limit the test setup to one dominant CM path.

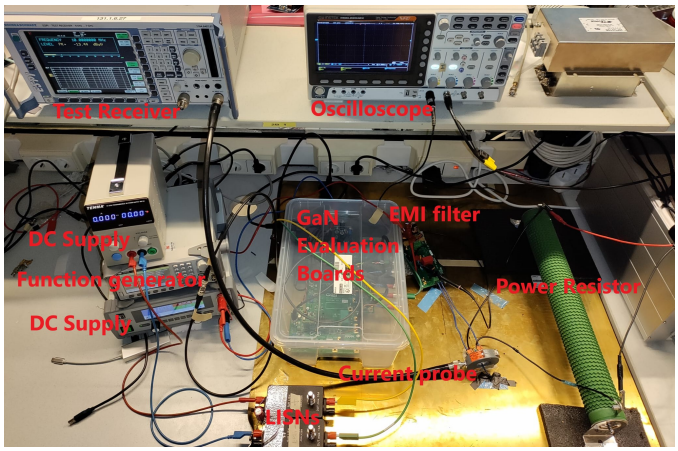


Figure 15. Practical measurement setup with filter

The placement of the current probe has proven to be vital for measurement accuracy. For this paper, three probing locations have been evaluated. The first measurement point is the wires leading to the load. Using the same principle as given for the CMC in the analysis, putting both wires leading in the same direction through the current clamp should cancel the DM magnetic fields. This perfect cancellation, however, only works in simulations.

In practice, the noise cancellation is not perfect. Since the DM noise output of the inverter is several orders of magnitude

Table II
R&S ESPI SCAN TABLE SETTINGS

Setting	Value
Start Frequency	100 kHz
Stop Frequency	10 MHz
Step Size (Linear)	500 Hz
(3 dB) Resolution Bandwidth	1 kHz
Measurement Time	40 ms
Auto Ranging	OFF
RF Attenuation	0 dB
Preamplifier	OFF

higher than the CM noise, the resulting measured noise signal largely consists of the DM noise. The DM noise is identified by its slope, which ideally should be -40 dB/decade due to the noise spectrum and inductive load. As mentioned before, the expected CM noise spectrum should, however, be flat.

The CM should therefore be measured at one of the ground connections in Fig. 10. Since the load current through the load is of interest, it should ideally be measured at its parasitic connection to the ground plane. To do this, 2 additional 1.5 nF y-capacitors are added to the load. Next to the measurement point, the increased load capacitance also increases the CM current. This allows measurements to be performed at lower main supply voltages. Similar to Fig. 12, the CM current using the additional load capacitors is shown in Fig. 16. As mentioned before, the resonance peaks in the MHz range are caused by the parasitic inductance of the ground path. However, one major difference between the figures is that using a symmetric distribution does not result in complete CM current cancellation in the practical setup. The symmetric distribution instead results in a noise spectrum similar to using mismatched capacitors in PSpice. Therefore, the CM current is likely caused by the ±20% capacitance tolerance on the Vishay AY2 capacitors [27] used in the practical setup.

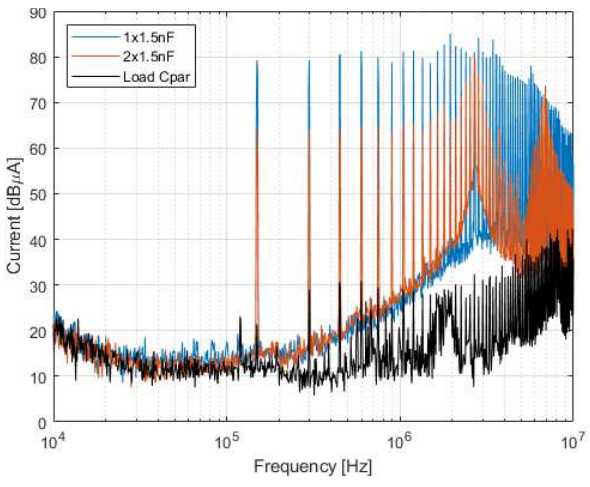


Figure 16. CM current measurements of different load capacitances with a full bridge inverter

C. Filter design

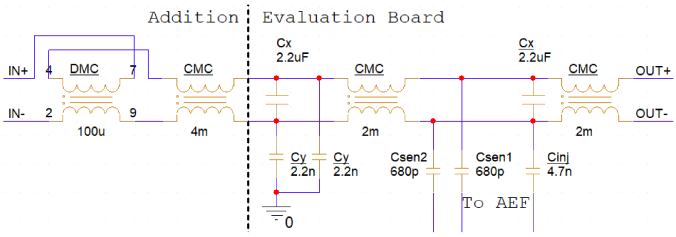
For accurate simulation of the filter, its components should include parasitics. For many components, there are PSpice libraries available, which contain parts performing similarly to their measured performance [16]. Since the AEF impedance cannot be calculated due to the missing loop gain, the simulations play a crucial role in determining proper operating conditions for the AEF.

The evaluation board filter is used as the starting point of the filter design since it is a known good and stable filter. It can however not be implemented directly, since the first DM component is an x-capacitor. This capacitor effectively creates a short between the output lines, which also shorts the supply DC supply lines through the GaN HEMTs. Therefore the first component of the filter should be an inductor or differential mode choke (DMC). The required inductance is calculated using the conventional approach from [28], which uses the required attenuation set by the noise magnitude and the attenuation of the filter topology to determine the required cut-off frequency. This has been done in [29] with an inverter using relatively similar frequencies to get a cut-off frequency of roughly 10 kHz. This cut-off is also high enough to not interfere with the main output frequency of the inverter. Since the x-capacitors on the evaluation board are 2.2 μF, the inductance should be roughly 100 μH. Inductors with this value and a current rating close to 10 A are, however, not readily available. Instead, a WE-ExB 100 μH CMC is repurposed as a DMC by switching the connections from 1 of its coils.

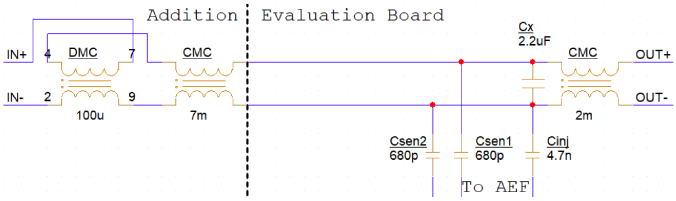
From the characterization of the load, it can be seen that it has a low impedance. This means that the capacitors at the output side of the filter have a relatively low impact on the filter performance. Therefore the x-capacitor and the 2 y-capacitors are removed from the filter.

The minimum required inductance for the CMCs is limited by the AEF maximum voltage swing. TI recommends that the voltage swing at the output of the filter IC should be between 2.5 V and (V_s – 2) V for linear operation [20], with the output being biased around 6 V. It can be determined from simulations that the relatively low 2 mH inductance of the CMCs on the evaluation board does not provide enough noise attenuation for the AEF. The voltage swing of the AEF output far exceeds the recommended range, to the point that the amplifier is clipping. The addition of a 4 mH CMC in front of the evaluation board relieves this problem, making the output swing roughly equal to the maximum recommended swing. The resulting HEF can be seen as layout 1 in Fig. 17. The last choke off the filter is not strictly required for attenuation, but more importantly for isolating the active filter from the load. The high attenuation of the CMC ensures that the load has minimal impact on loop gain and stability.

The filter is however still not very practical due to the large number of components. Simulations show that the 2 chokes and 2 y-capacitors before the active filter can be substituted by a single, sufficiently large, CMC. This second compact filter



(a) Layout 1



(b) Layout 2

Figure 17. Hybrid EMI filter layouts, where the "DMC" components are CMCs wired to attenuate DM signals

layout can be seen as layout 2 in Fig. 17. A 7 mH choke lets the AEF operate with roughly the recommended output swing, while a single 4 mH choke also works without clipping the AEF output.

Since the main supply voltage of 20 V is likely higher in realistic applications, the filter is also evaluated using an increased voltage. As mentioned before, one purpose of using an active filter is to reduce the size of the CMCs. Therefore, three methods have been evaluated to allow the HEF to operate with an increased supply voltage without increasing the CMC size.

The first method is increasing the supply voltage of the AEF from 12 V to 16 V, which is the absolute maximum given in the datasheet [6]. This should ideally increase the voltage headroom at the output of the inverter, keeping it from clipping.

The second method consists of using multiple TPFS12C1s. While such usage of the IC is not described in its documentation, it would lower the required current of each chip. The filter evaluation board conveniently has a socket where a secondary evaluation module can be plugged in. By using the module instead of only an extra IC, there is, however, also an extra compensation network. Since this lowers the impedance to ground at the output of the ICs, the attenuation provided by the active filters is decreased.

Lastly, the third method is to adjust the AEF gain. Using the information from the analysis and PSpice modeling, the components with the largest influence on the INJ pin voltage are identified to be R_g, C_{D1}, R_{D1a} and the series resistance of the sense capacitors. Since the TPSF12C1 acts as a current source, changing the impedance directly at its output, D1, has a significant effect on the output INJ pin voltage. Changing the impedance of sub-circuits D2 and D3 can also yield improvement. Tuning the components of these sub-circuits and the series resistance of the inject capacitor can however quickly lead to instability due to under-damped resonance with the CMCs when the total impedance to ground increases. Additional damping is then required by either lowering the impedance of the other sub-circuit or by adding additional damping directly from line/neutral to ground. For example, INJ pin voltage can be lowered by increasing the impedance of D3 or C_{inj} combined with a decrease of D2 impedance.

IV. Results

The layouts from Fig. 17 are created by adding a prototyping board to the front of the filter for the DMC and CMC, and removing the unwanted components from the evaluation board. The extra choke is mounted using a connector instead of soldering it directly to the board to be able to change between chokes for the second filter layout. The realization of the first layout can be seen in Fig. 18. The second layout is created by removing all passive components from the first up to and including the middle CMC.

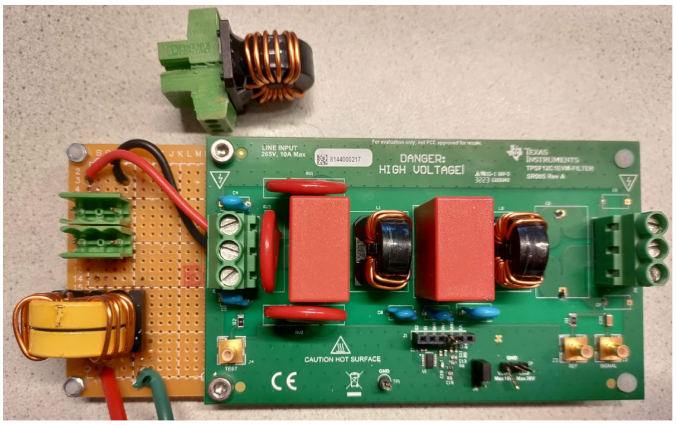


Figure 18. Realization of filter layout 1

The filter performance will be evaluated using the setup from the power filter characterization or the setup from Fig. 15. These measurements are described in the 2 following subsections. After this, limit tests are performed with the solutions described in the methodology.

A. Tracking Generator measurements

For measurements using the TG, the EMI filter needs to be connected such that only the CM attenuation is measured. As described in [30], this can be done by shorting the line and neutral connections of the filter. The TG and receiver are then connected to the shorted input and output, after calibrating their transfer losses in the ESPI.

The measurement of the first filter layout can be seen in Fig. 19, and the second layout results are in Fig. 20. One common factor in all these figures is that the simulated trace seems to be shifted to the right. This could likely be caused by a (parasitic) capacitance present on the evaluation board which was not taken into account and/or by component tolerances. For the measurements with the active filter turned off, the main slope starting from 100 kHz shows a different rate between simulations and reality. When the filter is enabled, however, the slopes match quite accurately.

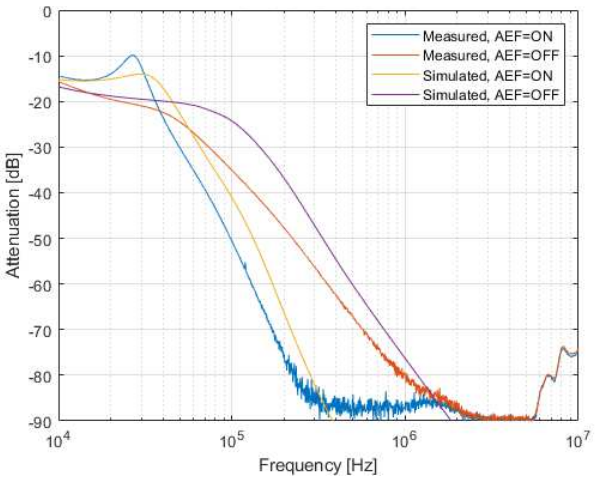
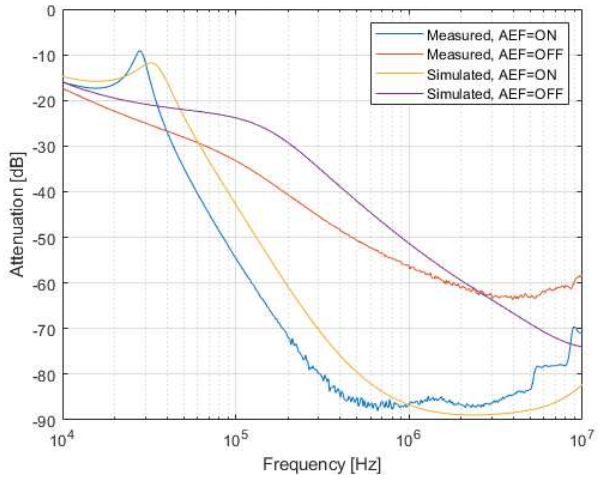
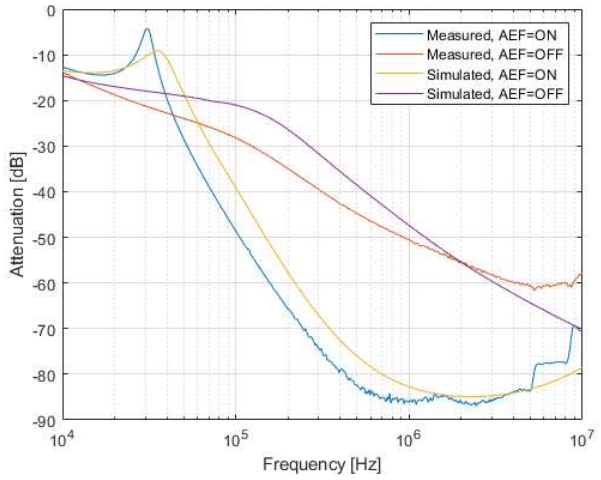


Figure 19. TG measurement of filter layout 1



(a) 7 mH CMC

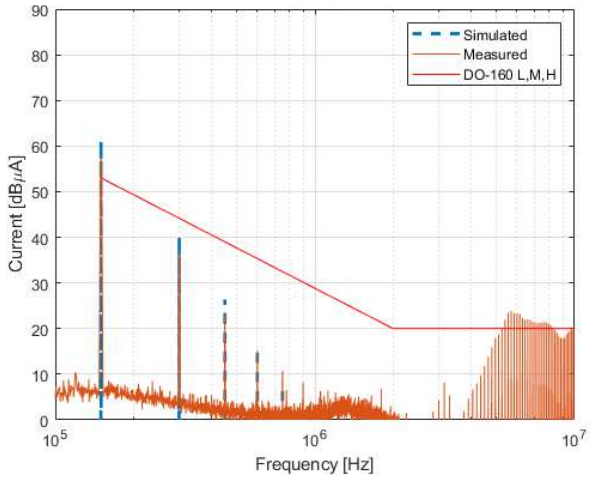


(b) 4 mH CMC

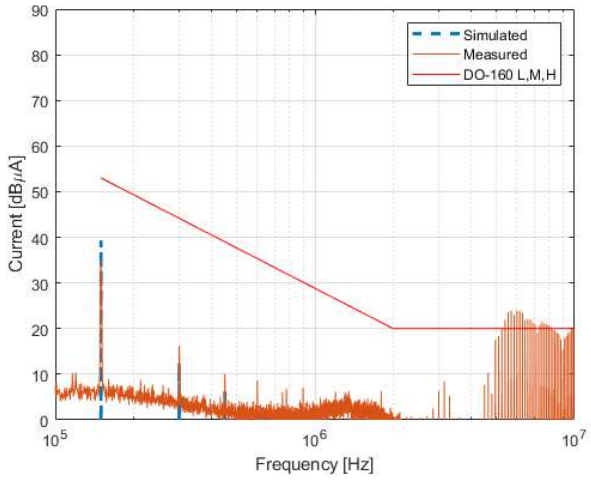
Figure 20. TG measurement of filter layout 2 with different CMCs

The traces also show a resonance between 10 and 100 kHz for all curves with the AEF on. This is an expected instability from the compensation network used with the active filter [19] and the CMCs. Since the noise floor of the ESPI is around -85 dB, the average detector of the ESPI is used to reduce the magnitude of the resulting noise peaks. Since this is not a limitation in simulations, the simulated trace continues below -90 dB in Fig. 19.

B. EMI measurements



(a) AEF off



(b) AEF on

Figure 21. Simulated and measured CM current of filter layout 1

The EMI measurements are performed as described in the practical setup subsection of the methodology, using the half bridge inverter. For each filter, 2 figures compare the measured to the simulated CM noise current, with the filter on and off. Next to this, a DO-160 limit line has been added for comparison between figures [5]. It should however be noted that there are significant deviations from the standard. The line should therefore only be used for the comparison mentioned above and not for determining whether the EMI filter is compliant.

Fig. 21 shows the CM measurement of the first filter layout, with the AEF off and on. The main observations are that the simulated emissions peaks are higher than the measured noise peaks, which follows the trend of the TG measurements. With

the active filter disabled, the slope of the peaks is relatively similar. Enabling the filter makes the slope of the simulation much steeper. Lastly, there is relatively high noise above 4 MHz, which is present in both figures. However, the AEF is expected to have little to no effect above 3 MHz [19]. This high-frequency noise also roughly coincides with the noise peaks from Fig. 16, where the resonance peaks of the load capacitors with the parasitic inductance occur.

The output of the active filter can be seen in Fig. 22. Since the measurement point for the INJ voltage is after the compensation network before C_{inj}, the voltage swing is roughly a quarter of the AEF pin voltage. This means that the linearity limits given by TI are roughly at a peak-to-peak voltage of 2 V. It can be seen that the measured swing is lower than the simulated swing. This lower AEF output is also present in the TG measurement of Fig. 20, where the resulting attenuation is lower in simulation with the AEF enabled. The measured signal also has an additional 500 Hz "hum", resulting from the relatively high power supply noise and low power supply rejection ratio of the TPSF12C1 [19].

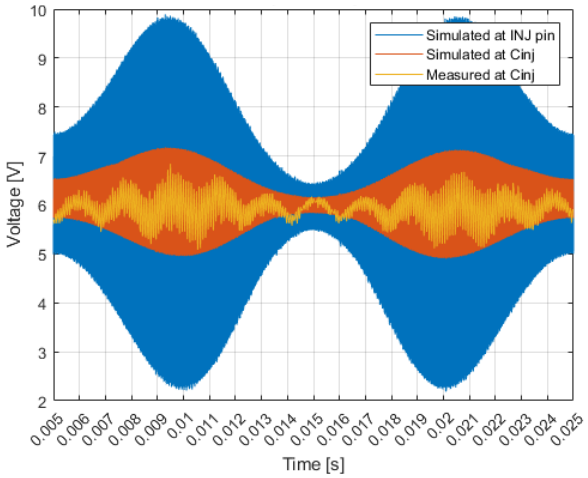
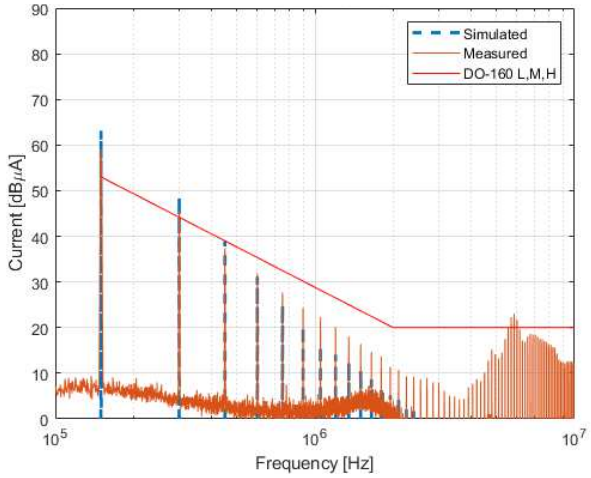


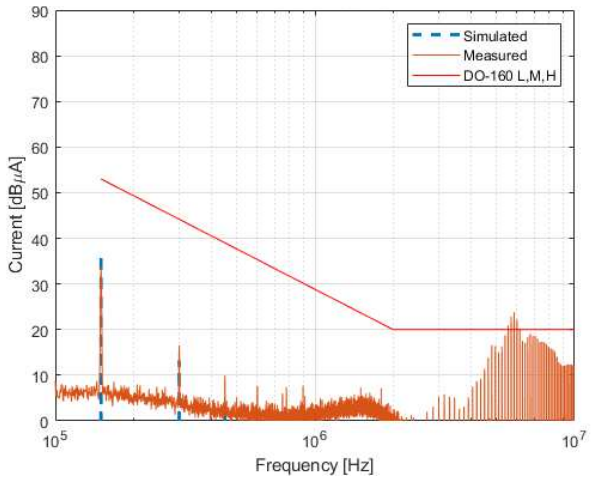
Figure 22. Simulated and Measured Inject voltage of filter layout 1

Filter layout 2 with a 7 mH choke, the filter output is resonating at roughly 10 kHz. Using the 4 mH moves its resonance with the feedback network to a higher frequency and relieves this issue. This issue can only be recreated in simulations by reducing the damping of this resonance peak. To still be able to test the filter with a 7 mH choke, an additional C_{inj} is placed to make the current injection symmetric. The reasoning for this is that the x-capacitor cannot be seen as short at the relatively low resonance frequencies of the filter. Then an additional 13 kΩ resistor is placed between neutral and ground to remove the resonance.

The resulting CM emission measurement of this altered layout can be seen in Fig. 23. Due to the reduction in passive filtering, there is significantly more CM. The observations made for the first layout hold for these measurements. Without these extra resonance countermeasures, the resonance can still be seen. Fig. 24 shows that the active filter can still attenuate the CM noise well under these conditions. The additional



(a) AEF off



(b) AEF on

Figure 23. Simulated and measured CM current of layout 2 with a 7 mH CMC and resonance suppression using an additional C_{inj} and 13 kΩ resistor

current peaks are roughly spaced at multiples of the resonance frequency.

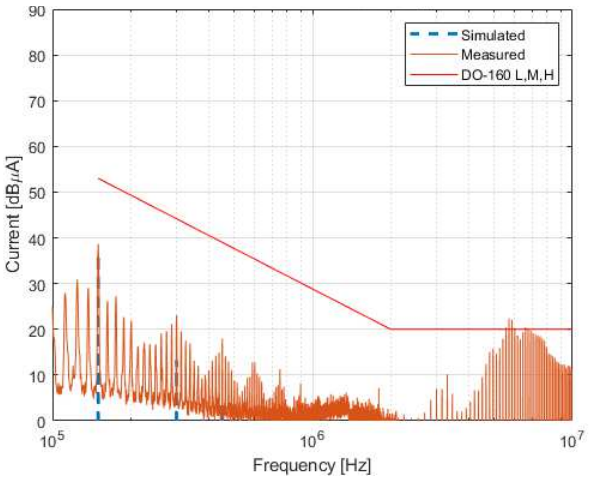
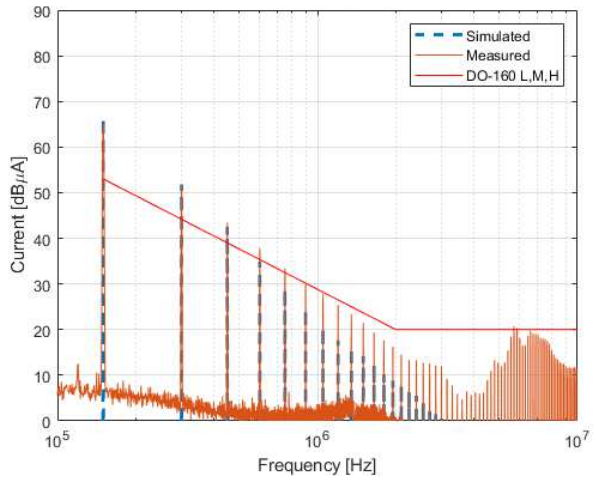
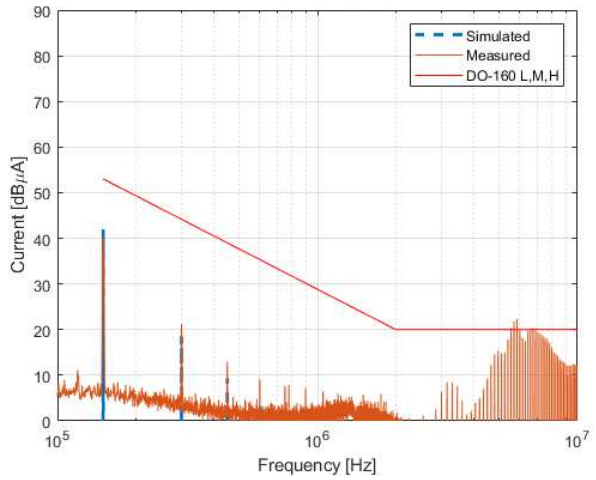


Figure 24. CM current of filter layout 2 with 7m choke with resonances



(a) AEF off



(b) AEF on

Figure 25. Simulated and measured CM current of filter layout 2 with a 4 mH CMC

The filter measurements with a 4 mH choke are closest to the simulations, as seen in Fig. 25. This filter does not require the additional components used in the previous filter to achieve stability.

C. Limitation tests

In all the previous tests, the filter IC can operate nominally. As stated in the filter design section, the AEF works even though the manufacturer's recommended parameters are already exceeded. To find the actual limitations of the active filter, the voltage is increased to 35 V. This gives roughly the maximum power out of the power supply without the voltage sagging. Clipping starts to be visible at the inject capacitor from 30 V. The second filter layout with the 4 mH choke is used since it tasks most of the AEF compared to the other filters. From Fig. 26 it can be seen that the active filter is overloaded since the CM noise is barely attenuated. The inject voltage changes from a symmetric waveform to a skewed output.

The first method to operate at the higher supply voltage, without increasing the CMC size, is to increase the AEF

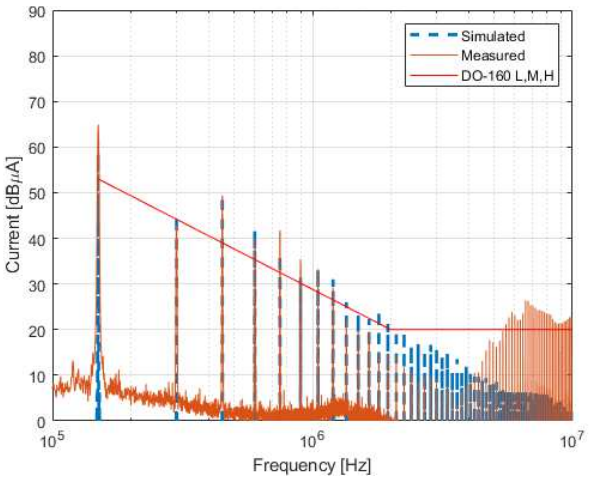


Figure 26. CM current of filter layout 2 with 4 mH choke at 35 V main supply voltage

supply voltage. The active filter acts as expected and increases its bias voltage always to half of the supply voltage. The extra headroom allows the active filter to cancel the additional CM current and give an EMI measurement similar to Fig. 27. The measurements have also shown that the 35 V main supply voltage is the maximum the AEF can handle with a 16 V supply. Since the simulations show slightly higher output voltages, this maximum appears at a main supply voltage of 30 V. At this voltage there is already some clipping at the output of the TPSF12C1, but this does not affect the CM noise reduction significantly.

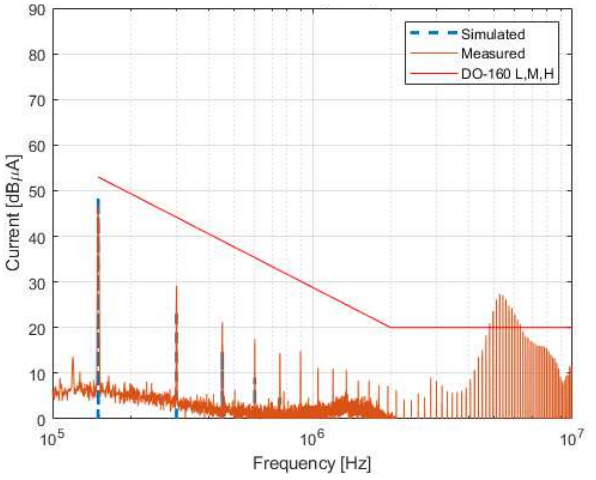


Figure 27. CM output current of filter layout 2 with 4 mH choke at 35 V main supply voltage with 2 AEFs

The second method of adding an extra AEF with compensation network initially results in a roughly 3 dB increase in peak CM noise current. Similarly to increasing the voltage, this setup allows the active filters to cancel the increased CM noise current, as seen in Fig. 27. There is also a longer startup time that must be considered when simulating. During this startup, the measuring point at C_{inj} is fixed to Vsupply.

The last method of using an adjusted compensation network in the CM current of Fig. 28. The filter performance is close to the results observed in Fig. 25, even with an increased main supply voltage. To resolve the clipping of the AEF, resistor R_g and C_{D1} have been increased to 3 kΩ and 47 nF respectively. Further voltage increase is also possible when decreasing the series resistance of the D1 subcircuit.

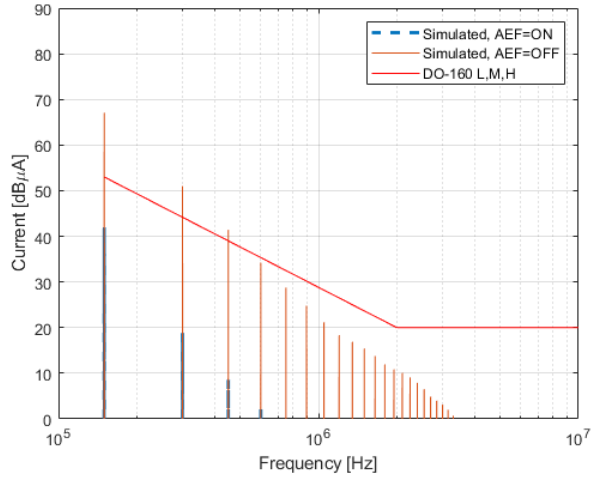


Figure 28. CM current simulations of filter layout 2 with 4 mH choke, adjusted compensation network and 30 V main supply voltage

Since the DO-160 is an aircraft standard, where the line frequency is commonly 400 Hz, the HEF is also tested at this frequency. It can, however, be seen from Fig. 29 that this results in the output of the AEF containing a significant 400 Hz component. Another supply without the 500 Hz noise is used to see the 400 Hz component more clearly. Testing at 20 V supply voltage shows that the filter can operate properly at this frequency. The unwanted frequency component can however cause the active filter to start clipping at lower CM noise currents, since its swings cause the AEF output to be closer to its supply voltage.

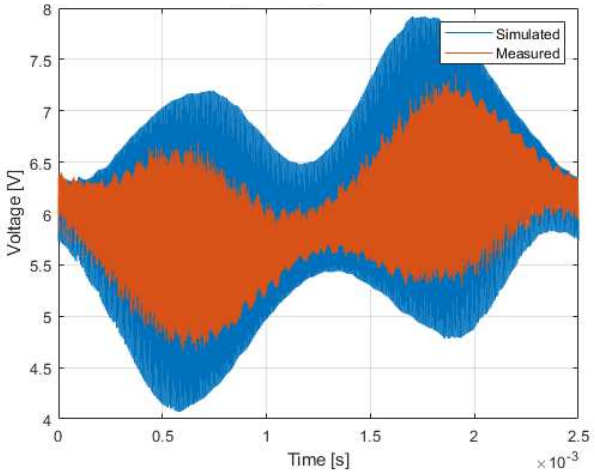


Figure 29. Vinj voltages of filter layout 2 with 4 mH choke and a 400 Hz main frequency

During all of these tests, the temperature of the filter was closely monitored. A figure at the end of a few 35V tests can be seen in Fig. 30. The two hottest components of the filter were the active filter IC and the DMC, with them being roughly 10 degrees Celsius above ambient temperature. The highest measured temperature of the filter IC was slightly higher at 15 degrees Celsius above ambient temperature.

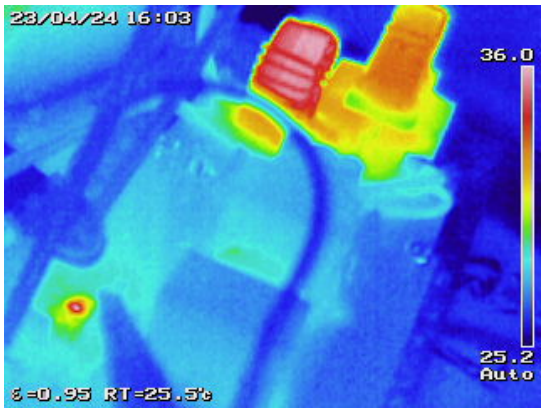


Figure 30. Heat figure of the Filter components

V. Conclusion

Three hybrid EMI filters have been designed to reduce the number and size of passive components. This has been done by creating a PSpice model and a validation setup. The relatively accurate model is then used to design and test different filter layouts. The Filter performance is evaluated by using a tracking generator and by measuring the current through the CM capacitance of the load. When comparing the results of these measurements, with and without an active filter, it can be concluded that the active filter can increase filter attenuation up to 30 dB, and can thus also be used to reduce the CMC size.

To test the filter within its operating range, a switching frequency of 150 kHz is used. A large CM load capacitance is created using two 1.5 nF y-capacitors, which are also used for current probe placement. This capacitance allows the measurements to be performed at low voltages while retaining CM current.

The PSpice model also shows the effectiveness of using a full bridge inverter to cancel CM current. The associated requirement of a highly symmetric load is also accurately depicted, as seen by the mode conversion of a non-symmetric load.

Limitation tests have been performed with increasing main output frequency and voltage. At 400 Hz the AEF is effective with a lowered maximum CM canceling capacity. Increasing the main supply voltage introduces AEF clipping. Increasing the AEF supply voltage, adjusting the compensation network and adding a parallel AEF with extra compensation network have shown to be effective in dealing with higher CM noise.

Acknowledgements

I want to thank Professor Niek Moonen for supervising this thesis and for providing his guidance in regular meetings. Next to this, I would also like to show gratitude to the staff and members of the PE group for their willingness to help with issues around the lab.

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APPENDIX A
PSPICE MODEL

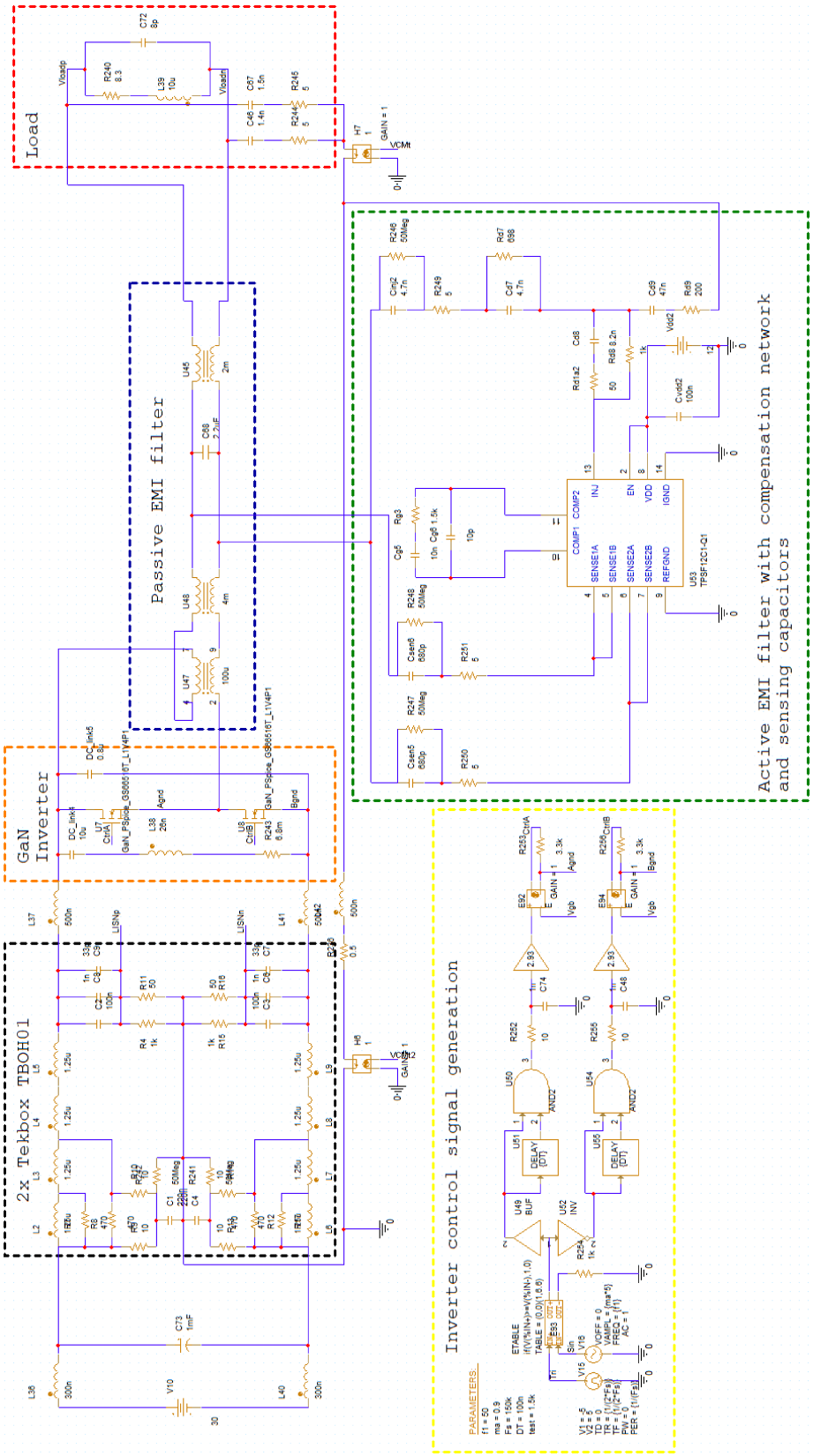

Figure 31. Complete PSpice model of the inverter with EMI filter and load