Optimizing EMI Filter Performance Through Capacitor Placement and Orientation

Csongor Buzogany

***Abstract*—This paper investigates methods to enhance the performance of EMI filters without significant modifications to their design, focusing specifically on the placement and orientation of the capacitors. A simplified Shunt Capacitor (SC) filter with two capacitors was used to determine the best capacitor placement, reducing the need for complex simulations of full EMI filters. Key couplings within different layouts of the SC filter were identified, analytically calculated, and input into an LTspice simulation model to assess the performance of the different layouts. These simulations were validated against actual measurements, and the resulting filter performances were evaluated based on their high-frequency attenuations. It was found that replacing a single capacitor with two parallel capacitors improves performance, but placing capacitors in an antiparallel configuration yields the best results, achieving an 11 dB increase in attenuation above 50 MHz. This antiparallel layout offers the highest performance with minimal space requirements, making it an optimal solution for larger EMI filters. Attempts to apply these findings to a more complex Common Mode (CM) filter, consisting of two capacitors and a common mode choke, revealed limitations due to the lack of an accurate analytical model for the choke. Consequently, simulation results did not align with measurements, indicating the need for more precise modelling, possibly through 3D simulation software.**

I. Introduction

Electrical devices emit radiation that can interfere with other devices. This issue is particularly concerning for high-power devices, as their emitted radiation is significantly stronger. To mitigate this problem, Electromagnetic Interference (EMI) filters are used, which are often composed of passive components, typically inductors and capacitors. Using these components, a low-pass filter is created, filtering out the high-frequency noise from a signal, thus reducing the emitted radiation.

In an ideal scenario, the filter's attenuation would continuously increase with frequency, however, in reality, this only holds up to a certain point. Beyond this point, the impedance of the parasitic inductances within the circuit become dominant, resulting in a worse attenuation. The PCB's traces together with the capacitor's leads and body, all result in some small parasitic inductances, which can affect the filter's performance greatly at higher frequencies. The Equivalent Series Inductance (ESL) of a capacitor is mainly dependent on the size and the type, with smaller capacitors often having a smaller inductance.

The parasitic effects inside a filter extend beyond the impacts within individual components. Another, often overlooked effect is the mutual coupling between the components, which arise due to the proximity of the components to each other. Even though these values are small, they do affect the filter's high-frequency response. To be able to accurately determine the filter's performance, a way to calculate these mutual parasitic effects is needed [2, 3, 10, 19]. In addition to parasitic inductances, the circuit will also have parasitic capacitances, but as their impact is significantly smaller, they will be disregarded.

This paper aims to show the importance of the often neglected effect of the placement of the capacitors on an EMI filter. This is achieved, by comparing various capacitor layouts and evaluating their effects on the filter.

II. Theory

A. EMI filters

EMI filters are used to reduce the noise emitted by a device so that it does not disrupt other devices in its vicinity. A commonly used EMI filter topology can be seen in figure 1.

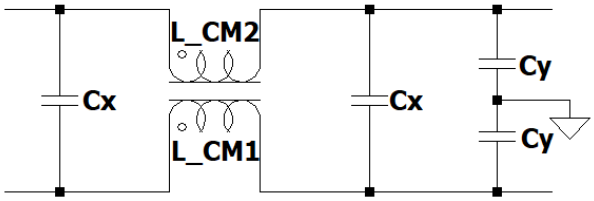


Fig. 1: A typical example of a single-phase EMI filter.

To be able to properly filter out the noise, it is important to differentiate between two different types of signals, as both of these need a different type of filtering. Common Mode (CM) signals occur when currents in both conductors flow in the same direction and return via a different route (like the grounding), while Differential Mode (DM) signals have the return current flowing through the opposite wire. In a typical EMI filter, as shown in figure 1 both CM and DM filtering parts are present. The X-type capacitors filter out the differential mode noise, while the Common Mode Choke (CMC) with the Y-type capacitors, filters out the common mode signals. By choosing the proper values for the capacitors and the choke, the filter can be used to filter out the high-frequency noise, while keeping the signal intact.

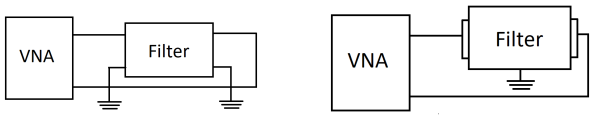
To analyse this filter properly, it will be split up into two parts. The first part, which will function as a DM filter, is a Shunt Capacitor (SC) filter, consisting of two capacitors and is shown in figure 2a. The second filter will be a CM filter that uses a common mode choke with two Y-type capacitors, as seen in figure 2b.

(a) Shunt capacitor, DM filter using two X-type capacitors.

(b) CM filter using two Y-type capacitors and a common mode choke.

Fig. 2: The two filters used for testing.

To be able to measure the effects of the different placements, a Vector Network Analyser (VNA) will be used. As the DM filter will need a differential mode and the CM filter a common mode signal, both filters need to be connected differently. The proposed setup is shown in figure 3.



(a) Measurement of the DM filter

(b) Measurement of the CM filter

Fig. 3: The measurement setup.

B. Self-inductance of the capacitors

As mentioned before, the parasitic inductance of the components worsens the filter's high-frequency attenuation, meaning that more EMI will be let through. This parasitic inductance is largely caused by the ESL of the capacitor. Putting two identical capacitors in parallel should result in a 6 dB increase, as putting two inductors in parallel halves the total inductance. This is, however, not the case in reality, as the adjacent parallel capacitors result in a mutual coupling, which increases the effective inductance. [7].

Starting the analysis of the SC filter from figure 2a, the first step is to calculate the capacitor's self-inductance. The capacitor body, along with the capacitor's leads and the ground plane, form a loop through which the current flows. The self-inductance is determined by the size of this loop. As the internal structure of the capacitor is very complex, calculating the self-inductance is nearly impossible without an extensive simulation model. To simplify the problem, some assumptions are made about the internal structure of the capacitor and the current flowing through it. As the current is flowing in a known closed loop, the self-inductance can be calculated using the partial inductances of the different sections of the loop. Calculating the partial self-inductance of the leads can be done using equation A.1.

Calculating the current distribution through the body of the capacitor is not as simple. Because the internal structure of the capacitor, consisting of a metal foil together with some kind of dielectric, can result in a non-uniform current distribution, some simplifications will be made. The assumption is made that the presence of the ground plane causes the currents in the capacitor to flow very closely to the bottom of the capacitor. The current will be distributed in a thin strip at the bottom of the capacitor, approximated as a flat wire with the same width and length as the internal foil winding. [7, 18] The high-frequency current is approximated to flow at the bottom of the foil winding, at a height $l + \delta$ above the ground plane. Using equation A.2, the partial inductance of this strip can be determined [7].

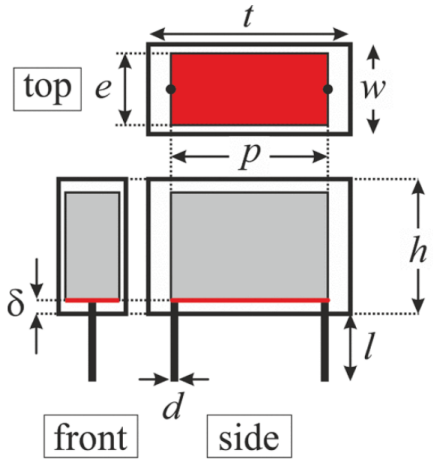


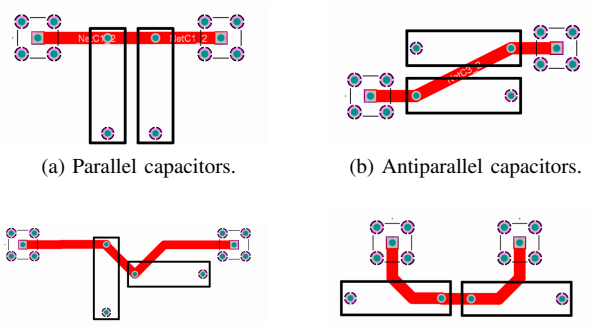
Fig. 4: *"Top, front, and side views of a thin-film capacitor. Gray surfaces indicate the foil winding inside the capacitor. The area where currents are expected to flow at high frequencies is highlighted in red."* [7]

As previously mentioned, the loop inductance can be calculated using partial inductances however, simply summing the partial inductances from all sides of the loop does not provide the complete loop inductance. To obtain the total inductance, mutual partial inductances must also be considered. Since the capacitor leads are parallel and carry opposing currents, their mutual partial inductance will be negative. The exact value can be calculated using equation A.1. Similarly, the mutual partial inductance between the ground plane and the capacitor body can be considered. Because the capacitor leads are orthogonal to the currents in the capacitor body and the ground plane, their mutual partial inductance will be zero. By summing the partial inductances with the mutual partial inductances, the total loop inductance can be determined.

C. Mutual inductances of different layouts

To increase the high-frequency performance of the filter, some methods are needed to minimise the circuit's inductance. This can be done by using some kind of parasitic cancellation technique, using PCB trace loops to cancel out the parasitic inductances using a negative coupling [4, 15, 13]. This paper, however, will only focus on the component placement and its effect on the filter's response. Specifically, the capacitor placement on a DM (figure 5) and CM (figure 8) filter will be looked at.

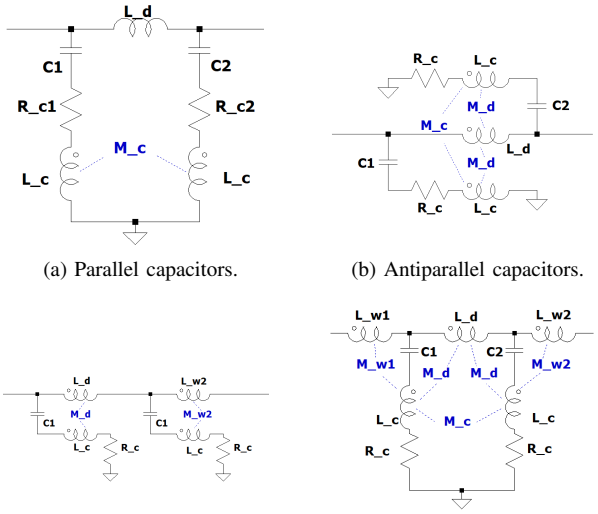
Starting with the DM filter, the first case is the parallel configuration shown in figure 5a, with the corresponding



(a) Parallel capacitors. (b) Antiparallel capacitors.

(c) Perpendicular capacitors. (d) Side by side capacitors.

Fig. 5: Different configurations of the 2 capacitor SC filter.



(a) Parallel capacitors. (b) Antiparallel capacitors.

(c) Perpendicular capacitors. (d) Side by side capacitors.

Fig. 6: The equivalent circuits which correspond to the layouts from figure 5.

equivalent circuit depicted in 6a. These equivalent circuits include the parasitic inductance and resistance of the capacitors, which are assumed to be identical for both capacitors. L_d represents a small inductance, caused by the trace connecting the capacitors. Although the traces connecting the filter to the input and output connectors also have some inductance, their effect on the filter's response is negligible, so they are omitted from the equivalent circuit. The most significant coupling in the parallel layout is between the two capacitors. Other inductive couplings, such as those between the traces or between a trace and a capacitor, are ignored due to their negligible effect. Capacitive couplings are also completely disregarded. The coupling between the two capacitors, denoted by M_c is caused by the two current loops, formed by the body and leads of the capacitors, being parallel to each other. The magnetic fields created by one capacitor will induce a current in the other. The exact magnitude of the mutual inductance can be calculated using mutual partial inductances. For simplification, the current inside the capacitors is approximated by a thin wire running through the centre of the capacitor, at the bottom of the foil winding. Assuming b is the distance between the outsides of the capacitors, the distance between the two loops will be $b+w$, where w is the width of the capacitor as shown in figure 4. By summing all the mutual partial inductances from both current loops, calculated using equation A.1, the total mutual inductance between the capacitors can be determined. Since the currents in both capacitors flow in the same direction, the mutual coupling will be positive.

Considering the antiparallel layout, from figure 5b, with its corresponding equivalent circuit from figure 6b, the situation is similar to the parallel case, but with a few important differences. As the currents through the capacitors flow in opposite directions, the coupling becomes negative. Additionally, the current distribution inside the capacitors is concentrated near the inner sides of the capacitors, causing the distance between the current loops to decrease. It is assumed that the currents flow close, but not completely at the edge of the capacitors, with the distance between the current loops being approximated by $b + 0.1w$ [7]. Placing the capacitors in an antiparallel arrangement will also increase the length of the trace L_d, which will also run mostly parallel to the capacitors. This results in the mutual coupling between the trace and the capacitors, as denoted by M_d in figure 6b. Although the trace is not completely parallel to the capacitors, for simplification, it is assumed to be, and positioned on the centre line between the two capacitors. The mutual partial inductances can be calculated in the same way as in the capacitor's case.

When the capacitors are placed perpendicularly to each other, as shown in figure 5c, the current loops formed by the capacitors will have little to no effect on each other, resulting in no coupling between the capacitors. This arrangement does, however, lead to some coupling between the traces and the capacitors. As seen in figure 5c, the trace connecting the capacitors runs somewhat parallel to the left capacitor resulting in the coupling denoted as M_{w1}. Additionally, the right capacitor will couple in the trace above it, resulting in M_{w2}.

In the fourth case, where the capacitors are arranged side by side (figure 5d), the coupling between the capacitors, M_c does exist, but is very small. The couplings between the wires are also taken into account and are calculated in a similar way as the previous cases.

In addition to these four cases, the performance of a single capacitor and a double capacitor filter without coupling between the capacitors will also be tested. Both configurations will be tested using the setup from figure 5a. For the single capacitor test, only one of the capacitors will be placed, while for the uncoupled case, one of the capacitors will be positioned on the bottom, ensuring no coupling between the capacitors.

To be able to compare the different configurations more easily, the magnitude of the high-frequency attenuation will be used. The results from all aforementioned tests will be compared to the single capacitor case, to be able to determine the extent of improvement. Additionally, each layout's effective inductance will be evaluated, representing the equivalent inductance if only one capacitor was present. These can be

analytically calculated as mentioned in [5].

To more easily express the coupling between the components, the coupling factor, as shown in equation 1 can also be used. These coupling factors will also be used to simulate the mutual couplings between the inductors in LTspice.

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{1}$$

D. CM filter

After the SC filters are analysed, the next step is to examine the CM filter from figure 2b. Since the Common Mode Choke (CMC) is a relatively complex component with no clearly defined equations for its couplings, the filter will not be solved analytically, instead, relevant findings from other papers will be applied.

According to several studies utilising 3D simulation software, an optimal orientation and placement of the capacitor relative to the CMC was identified [1, 8, 17]. This layout is depicted in figure 7.

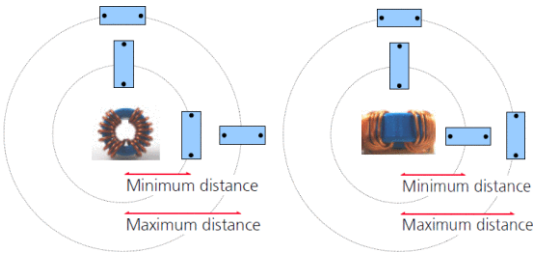
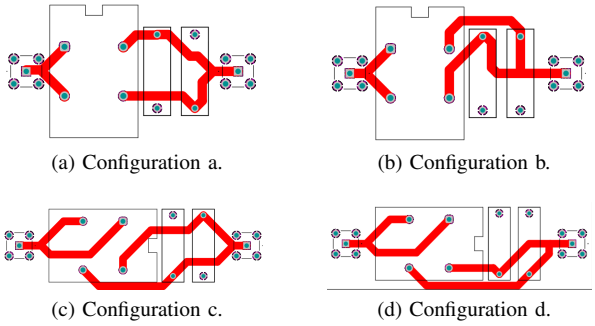


Fig. 7: The placement of capacitors next to a CMC [8].

To determine whether this placement also applies when using two parallel capacitors, the different layouts from figure 8 were tested. The capacitors have been placed in the place of the least and the most coupling (from figure 7). In both cases, the capacitors have been placed in both a parallel and an antiparallel configuration, as these layouts were the most space-efficient. Given the complexity and difficulty of calculating mutual inductances between all traces and components without proper 3D simulation software, only the self-inductances of the wires will be considered and calculated like the previous filter analysis. The couplings between the capacitors will be calculated similarly to the SC filter.

For the CM filter, all circuits from figure 8 are assumed to have the same equivalent circuit, which is shown in figure 9. The differences between the simulated circuits are mainly caused by the different self-inductances of the traces connecting the components, denoted by L_{t1} and L_{t2} and the couplings between the capacitors to each other and the CMC. The CMC is modelled as an ideal inductor with some series and parallel resistance. M_{ch} is the coupling between the CMC and the capacitors and will be approximated based on the findings of other papers. Most of the mutual couplings between the capacitors and traces have been ignored for simplicity.



(a) Configuration a. (b) Configuration b.

(c) Configuration c. (d) Configuration d.

Fig. 8: Different layouts for the CM filter.

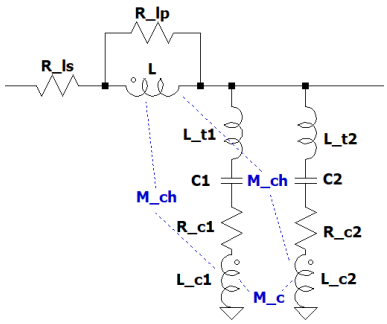


Fig. 9: The equivalent circuit which corresponds to the layouts from figure 8.

.

E. Scattering parameters

To compare the boards with each other, Scattering parameters (S-parameters) will be used, which are commonly used to describe the behaviour of a multi-port circuit.

For a two-port circuit, four different S parameters show the correlation between the waves at the ports as seen from equation 2. The parameters S_{11} and S_{22} represent the reflected waves at the in and output of the device. The S_{12} and S_{21} parameters, which are the reverse and forward voltage gains respectively, can also be used to determine the filter's frequency response.

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{2}$$

In equation 2, V_1^+ and V_2^+ represent the incident voltage waves, while V_1^- and V_2^- are the reflected waves from the source and the load side respectively. The voltages and currents can be calculated at both ports using these waves.

These S-parameters can be measured using a VNA, with figure 10 showing the equivalent circuit used for the circuit measurement. The VNA functions as a variable voltage source, which measures the responses to a specific excitation from both ports, yielding the S-parameters. R_0 on the left corresponds to the series resistance of the voltage source, and R_0 on the right is the termination resistor over which the voltage is

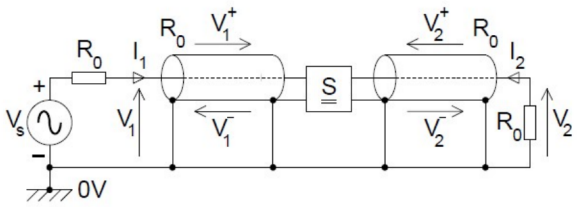


Fig. 10: The equivalent circuit of the VNA [12].

measured. These are both internal components of the VNA and must thus be considered when measuring the filter. The filter is connected to the VNA using a coax cable, whose characteristic impedance is matched to the output and the load impedances which are all 50Ω. Since the output and load impedance are both 50Ω, forming a voltage divider, the measured voltage by the VNA will only be half the actual voltage over the filter. This relation between the S_{21} parameter and the input/output voltages is shown in equation 3 [12]. For this paper, only the S_{21} (or S_{12}) is of interest, as this represents the filter's transfer function.

$$S_{21} = \frac{2V_2}{V_s} \tag{3}$$

III. Calculations

A. PCB design

To confirm the theory, two, two-layer Printed Circuit Boards (PCBs) were designed using Altium Designer, as shown in figure 11. The capacitors used, are Kemet P295 capacitors [9], with outer dimensions 7.5 mm · 14.5 mm · 18 mm (w · h · t, following the convention of figure 4), with their values ranging from 2.5 nF to 3.3 nF. For the CM filter, the CMC used was Wurth Elektronik's 7448060535 CMC [6], with an inductance of 35mH. For testing with the VNA, SubMiniature version B (SMB) connectors were used for both the input and output connections of the circuits. SMB connectors were chosen for their compact size, ease of use, and reliable connection, which are crucial for accurate high-frequency measurements.

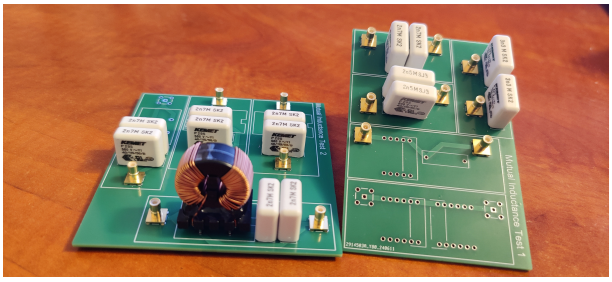


Fig. 11: The PCB's used to measure the filter's performance.

.

The different layouts for the capacitors were all put on the same PCB however, only one circuit was tested at a time, ensuring the circuits do not influence each other.

Configuration	L_d	M_c	M_d	M_{w1}	M_{w1}
Parallel	1.94 nH	0.94 nH	-	-	-
Antiparallel	4.70 nH	3.32 nH	1.72 nH	-	-
Perpendicular	3.23 nH	-	-	0.16 nH	78 pH
Side by side	1.88 nH	0.25 nH	2.77 nH	2.6 nH	2.6 nH

TABLE I: Calculated inductances.

B. The self-inductance of a capacitor

To simulate the circuits shown in figures 6 and 9, the capacitor's self- and mutual inductances were required. These inductances were calculated using the method described in the theory section. Based on the capacitor's outer dimensions (7.5 mm · 14.5 mm · 18 mm) and inner foil dimensions (6 mm · 15 mm), together with the distance from the bottom of the capacitor to the internal foil (δ) being 3 mm, the self-inductance was determined to be 10.8nH.

C. The mutual inductance of the capacitor layouts

The mutual inductances from figure 6 were calculated as described in the theory section. The values for all four cases can be seen in table I. The predicted effective inductances for the full circuits can be seen in table III.

The values from table I, were used to subsequently run a simulation, whose results can be seen in figure 13. In addition to the four layouts from figure 5, two extra simulations have been added. One of these simulations used a single capacitor, while the other involved two capacitors, placed on different sides of the PCB, to avoid any mutual coupling.

Simulations have also been run for the CM filter from figure 2b, resulting in figure 14. These measurements, however, are not as trustworthy as the DM filter, as many mutual couplings have been neglected. Also, instead of analytically deriving the couplings between the CMC and the capacitors, some approximations were made based on other papers which have either run a 3D simulation or used some other method to determine the coupling. [1, 8, 16, 17]. The CMC was also assumed to be an ideal inductor, which is also inaccurate. When looking at the attenuation graph from the CMC's datasheet in figure A.3, oscillations in the attenuation can be seen as the frequency is increased. This will likely result in the actual measurement of the filter also having these oscillations. Due to the above-mentioned approximations, the model likely will not match the measured results very closely.

IV. Results

To confirm whether the approximation of the self-inductance is accurate enough, the simulation results have been compared to the measurements of the real circuit. To ensure the assumption that only the physical size and distance of the capacitors affect the self-inductance, capacitors with three different rated capacitances were tested: 2.5 nF, 2.7 nF, and 3.3 nF. The capacitances of these capacitors have been measured with an LCR meter and compared to their rated values in table II. The measured values were then used to get figure 12. The parasitic resistance was determined by testing various values

Rated capacitance	Measured capacitance
2.5 nF	2.7 nF
2.7 nF	2.8 nF
3.3 nF	3.1 nF

TABLE II: Rated vs measured capacitances of the used capacitors.

and selecting the one that most closely matched the measured transfer function, ultimately resulting in a value of 0.25 Ω.

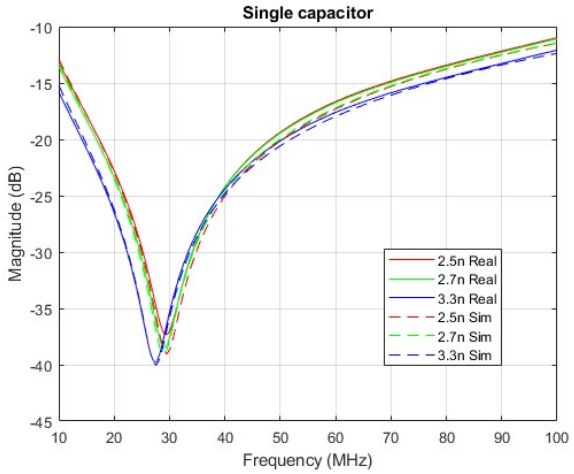


Fig. 12: Comparing the single capacitor circuits from the simulation and the actual measurements.

When comparing the simulation results with the measurements, only minor deviations are observed. This indicates that the approximations used to calculate the self-inductance of the capacitors are sufficiently accurate. Additionally, the variations in capacitor values do not cause significant deviations in the capacitor's self-inductance.

The next step is to compare the different layouts with each other. Figure 13 shows both the simulations and the measurements of the six different layouts for the 3.3 nF capacitor. The results for the other capacitor values can be found in the appendix (figures A.1 and A.2).

As can be seen from figure 13, most of the simulations match the real measurements closely. When comparing the different layouts, the single capacitor variant performs the worst. The relatively high self-inductance causes the filter response to deteriorate at higher frequencies. This also results in the highest effective inductance out of all the different layouts.

The next best layout is the parallel configuration, where the two parallel capacitors decrease the circuit's inductance. The effective inductance is nearly halved, however, because of the mutual couplings between the capacitors, it is not quite the case. The resulting performance increase is 5.4 dB at 70 MHz, as shown in table III.

The third-best configuration is a tie between the perpendicular and side-by-side placements. Both configurations experience some coupling between the capacitors and/or traces, however, as this coupling is less than the parallel case, the

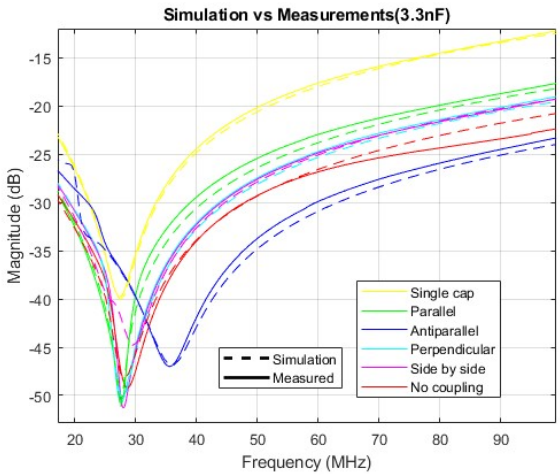


Fig. 13: Comparing the simulation of all layouts with the measured S-parameters for the 3.3 nF capacitors.

Configuration	Predicted		Measured	
	Att	L_{eff}	Att	L_{eff}
Single capacitor(reference)	0 dB	10.8 nH	0 dB	11.0nH
Parallel	5.7 dB	5.5 nH	5.4 dB	5.8nH
Perpendicular	6.9 dB	4.9 nH	6.8 dB	5.0 nH
Side by side	7.3 dB	4.7 nH	7.1 dB	4.9 nH
No coupling	8.5 dB	4.2 nH	9.5 dB	3.9 nH
Antiparallel	12.5 dB	2.9 nH	11.6 dB	3.2 nH

TABLE III: The improvements in filter performance at 70 MHz (compared to single capacitor circuit).

filter's performance is better. The exact values can be seen in figure 13 and table III.

The second-best performing configuration is the no-coupling layout. In this case, there is a significant deviation between the simulated and measured values at the higher end of the frequency spectrum. This likely results from some unexpected couplings in the filter, which have caused the filter's attenuation to be better in reality than the simulation would suggest.

The best-performing configuration was the antiparallel one, as in this case, the capacitors' mutual inductances cause a negative coupling, which decreases the filter's effective inductance and thus also increases the high-frequency attenuation. This configuration would also be the easiest, and most space-efficient to implement after the parallel layout, as only some traces would need to be redrawn, in a slightly more complicated shape. As shown in table III, the increase in the filter's performance is more than 11 dB at 70 MHz.

The CM filter's simulations have also been compared to the measurements. The resulting S_{21} parameter plots can be seen in figure 14. The simulation does not match the measurements very closely, which is likely due to the improper calculation and simplification of the filter's parasitics. The real circuit performs better than the simulation would suggest, which can mean that in reality, there are many couplings present on the circuit which cancel out the traces' and other components' inductances, increasing the filter's attenuation.

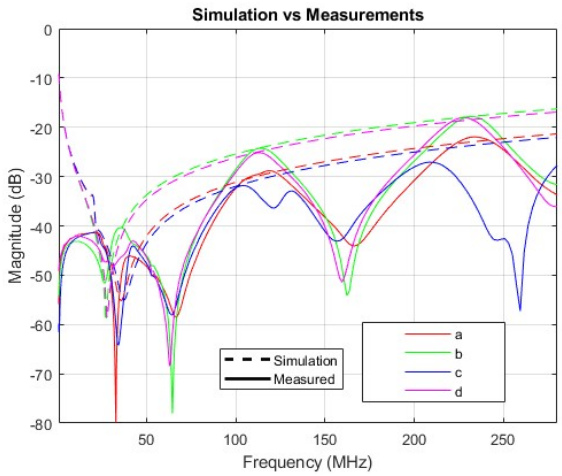


Fig. 14: Comparing the simulation of the CM filter to the measurements.

While the simulation does not overlap with the reality, there is a correlation. Both in simulation and reality, circuits b and d, which use the parallel capacitor configuration perform the worst out of the four layouts. This is likely due to increased inductance caused by coupling between the capacitors, which worsens the filter's response. Additionally, it is possible that the coupling from the CMC to the capacitors is higher, as the fields from the capacitors are less contained.

All four measurements show a heavily frequency-dependent change in the attenuation, which seems to oscillate, with the increase of the frequency. This can be caused by the CMC not functioning as an ideal inductor, as was already mentioned in the earlier section and be seen from the datasheet figure in the appendix (figure A.3). To model this circuit properly, 3D simulation software or a more in-depth simulation model, which would include most of the neglected effects should have been used.

V. Conclusion

In conclusion, this paper's goal was to improve an EMI filter's performance without any major modifications to the filter. This was mainly done by looking at the effects of the capacitor's placement on the filter's high-frequency attenuation. As a full EMI filter would have been more complex to simulate, a simplified Shunt Capacitor (SC) filter was used to determine the optimal placement of the capacitors. To achieve the best placement, the most important couplings were identified and simulated for a two-capacitor SC filter. By first analytically calculating the inductances and couplings between the components, a simplified simulation could be run to determine the effects of the different layouts. After confirming the accuracy of the method by comparing them to some actual measurements, the performance of the filters was compared, by looking at the high-frequency attenuation of the resulting filters. To achieve better high-frequency attenuation, a single capacitor can be replaced by two capacitors in parallel. Although this would increase the performance somewhat, a much better layout would be to place the capacitors in an antiparallel setting, which can result in an increase of more than 11 dB above 50MHz. This antiparallel layout gives the best performance while needing the least amount of space thus being also the most optimal option to implement on a bigger-size filter.

These findings were also tried to be implemented on a more complex CM filter, using two capacitors and a common mode choke, however, the lack of availability of an analytical model for the CMC, resulted in the simulation not matching the measurements. This meant that the approximations were not accurate enough, resulting in an inaccurate simulation model.

References

[1] Mohammad Ali, Jens Friebe, and Axel Mertens. "Design and Optimization of Input and Output EMI Filters under the Influence of Parasitic Couplings". In: *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*. 2021, pp. 1–10. DOI: 10.23919/EPE21ECCEEurope50061.2021.9570483.

[2] G. Asmanis et al. "Mutual couplings between EMI filter components". In: *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*. 2015, pp. 908–913. DOI: 10.1109/ISEMC.2015.7256286.

[3] Gundars Asmanis, Aivis Asmanis, and Denis Stepins. "Mutual couplings in three phase T-type EMI filters". In: *International Symposium on Electromagnetic Compatibility - EMC EUROPE*. 2012, pp. 1–6. DOI: 10.1109/EMCEurope.2012.6396838.

[4] J. Bernal, M. Freire, and S. Ramiro. "Simple and cost-effective method for improving the high frequency performance of surface-mount shunt capacitors filters". In: *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*. 2015, pp. 372–377. DOI: 10.1109/ISEMC.2015.7256189.

[5] Joaquín Bernal, Manuel J. Freire, and Sebastian Ramiro. "Use of Mutual Coupling to Decrease Parasitic Inductance of Shunt Capacitor Filters". In: *IEEE Transactions on Electromagnetic Compatibility* 57.6 (2015), pp. 1408–1415. DOI: 10.1109/TEMC.2015.2478058.

[6] *Datasheet WE-CMBNC Common Mode Power Line Choke Nanocrystalline*. 7448060535. Rev. 2.0. Wurth Elektronik. Jan. 2024.

[7] Pablo González-Vizuete et al. "Calculation of Parasitic Self- and Mutual-Inductances of Thin-Film Capacitors for Power Line Filters". In: *IEEE Transactions on Power Electronics* 34.1 (2019), pp. 236–246. DOI: 10.1109/TPEL.2018.2824658.

[8] E. Hoene, A. Lissner, and S. Guttowski. "Prediction of EMI behaviour in terms of passive component placement". In: *2007 18th International Zurich Symposium on Electromagnetic Compatibility*. 2007, pp. 49–52. DOI: 10.1109/EMCZUR.2007.4388193.

[9] *KEM_F3088_P295_Y1_500*. 3316927. KEMET. Aug. 2023.

[10] Niek Moonen, Frits Buesink, and Frank Leferink. "Optimizing capacitor placement in EMI-filter using back annotation of 3D field coupling parameters in circuit models". In: *2016 International Symposium on Electromagnetic Compatibility - EMC EUROPE*. 2016, pp. 576–580. DOI: 10.1109/EMCEurope.2016.7739225.

[11] Clayton R. Paul. *Inductance. Loop and Partial*. 2011.

[12] *Printed Circuit Board Demokit Electromagnetic Compatibility Lab-manual*. Oct. 2021.

[13] Yasuhiro Shiraki et al. "High performance broadband noise filter using inductance cancellation technique and various capacitors". In: *2016 International Symposium on Electromagnetic Compatibility - EMC EUROPE*. 2016, pp. 570–575. DOI: 10.1109/EMCEurope.2016.7739162.

[14] Charles S Walker. *Capacitance, inductance, and crosstalk analysis*. 1990.

[15] Pinhe Wang et al. "Utilizing Mutual Coupling to Eliminate Parasitic Inductance in EMI Filter Capacitors for Noise Reduction". In: *IEEE Transactions on Industry Applications* (2024), pp. 1–10. DOI: 10.1109/TIA.2024.3405929.

[16] Shuo Wang, F.C. Lee, and W.G. Odendaal. "Characterization and parasitic extraction of EMI filters using scattering parameters". In: *IEEE Transactions on Power Electronics* 20.2 (2005), pp. 502–510. DOI: 10.1109/TPEL.2004.842949.

[17] Shuo Wang et al. "Effects of parasitic parameters on EMI filter performance". In: *IEEE Transactions on Power Electronics* 19.3 (2004), pp. 869–877. DOI: 10.1109/TPEL.2004.826527.

[18] S.-P. Weber et al. "On coupling with EMI capacitors". In: *2004 International Symposium on Electromagnetic Compatibility (IEEE Cat. No.04CH37559)*. Vol. 1. 2004, 336–341 vol.1. DOI: 10.1109/ISEMC.2004.1350052.

[19] S.-P. Weber et al. "Predicting parasitics and inductive coupling in EMI-filters". In: *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.* 2006. DOI: 10.1109/APEC.2006.1620684.

APPENDIX

APPENDIX A

The mutual partial inductance between two parallel wires of the same length l, can be calculated using equation A.1. This assumes both wires to have a radius of r_w at a distance d from each other. The partial self-inductance of the wires can be calculated with this same equation by setting d to zero. [11].

$$M_p = \frac{\mu_0}{2\pi} l[sinh^{-1}\frac{l}{r_w+d} - \sqrt{1+(\frac{r_w+d}{l})^2} + \frac{r_w+d}{l}] \tag{A.1}$$

The partial inductance of a flat strip above the ground plane can be calculated with equation A.2. The width has a width w at a height h above the ground place. [14].

$$L_p = \begin{cases} \frac{\mu_0 l}{\frac{w}{h}+2.42-0.44\frac{h}{w}+(1-\frac{h}{w})^6}, & \text{with } w > h. \\ 60\ln(\frac{8h}{w}+\frac{w}{4h}, & \text{with } w \leq h. \end{cases} \tag{A.2}$$

The circuit has been tested with three different capacitor values. The results from the 2.5 nF and the 2.7 nF configurations can be seen in figures A.1 and A.2.

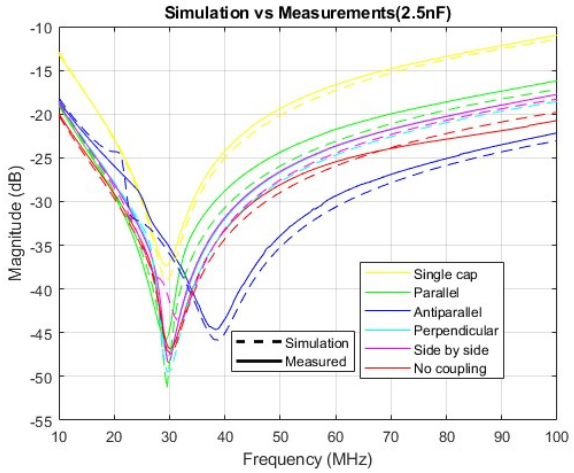


Fig. A.1: Comparing the simulation of all layouts with the measured S-parameters for the 2.5 nF capacitors.

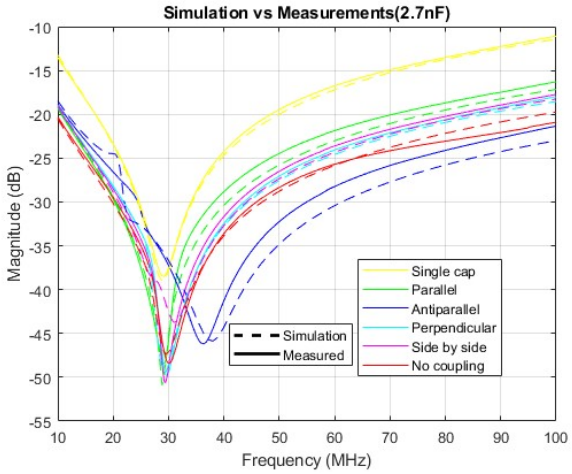


Fig. A.2: Comparing the simulation of all layouts with the measured S-parameters for the 2.7 nF capacitors.

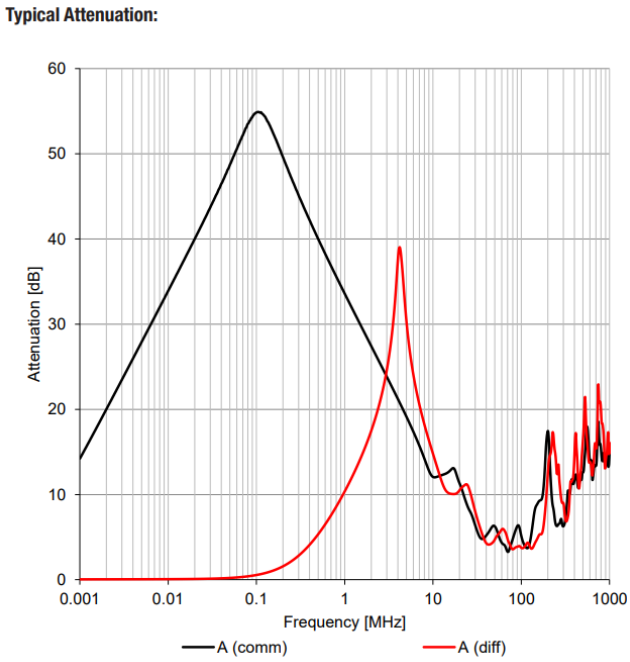


Fig. A.3: The attenuation of the Wurth 7448060535 CMC used in this paper [6].