Integrating Power Electronics Stages and Dynamic Load Balancing in Level 2 EV Charging

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Abstract – This paper investigates the possibility of designing power electronics and conversion stages and implementing them within residential level 2 Electric Vehicle (EV) chargers. Moreover, it investigates the validity of applying a Dynamic Load Balancing (DLB) mechanism by controlling these power electronics stages, making the EV charger a controllable load. Currently, the main function of residential EV chargers is to directly connect the On-Board Charger (OBC) to the grid, while providing it with safety and communication protocols. However, some EVs face communication issues with some brands of EV chargers due to incompatibility. This causes the charging performance to be limited, as well as restricting the application of DLB. Moreover, existing DLB systems can only control the output power of the level 2 chargers in discrete steps, thus, limiting the controllability of the load of the charger. The proposed power electronics stages consisted of an input LC filter, an interleaved boost PFC converter, a DC-AC inverter, an output filter, and a load impedance that resembles the input stage of the OBC. The proposed DLB system has a fluctuating input voltage from the grid (which fluctuates according to the load), and accordingly adjusts the power output to reduce these fluctuations. This is done using a feed-forward controller that directly controls the power output of the charger. A major advantage introduced is that the power output of the overall system can be continuously and dynamically controlled, bringing benefits for better EV grid integration and support. However, the idealised proposed system portrayed 7% lower efficiency than commercial level 2 chargers and introduced higher costs of manufacturing. The compatibility issues will not be solved with this system since it does not bypass the control pilot.

I. Introduction

There is an increasing demand in having EV chargers, also known as Electric Vehicle Supply Equipment (EVSE), available everywhere. Thus, several types of EVSEs are developed, each adapted to certain uses while following fixed regulations. One of the more common ones in Europe is the residential AC charger that charges EVs at the users' home. These EVSEs directly connect the EV to house's power grid, with the usual option of manually changing the current output to adapt it to the EV's requirements. These are commonly known as level 2 EVSEs. With the rising problems of power grids being overloaded, the development of Energy Management Systems (EMS) has started. These systems monitor the power usage of the house, and accordingly control the power used by certain devices. Alongside this, Dynamic Load Balance (DLB) kits are applied with the EVSEs to make them controllable loads. The overall charging process, whether dynamic or not, is dependant on the communication protocol between the off-board and on-board chargers. This process has introduced unanticipated communication problems between certain EVs and EVSEs. An example is an EV only charging with a certain amount of power, despite the capability of the charger and the grid to control and provide a different value. This issue becomes more significant when considering the application of previously mentioned EMS and DLB kits. If there is no control of the power output of the EVSE, then the DLB mechanism loses its functionality.

Currently, the main focus of EVSE manufacturers and distributors is to make level 2 chargers as compact, affordable and accessible as possible in both the residential and commercial aspects. There is also a larger focus on developing DLB mechanisms integrated within the charger to help reduce the load on the power grids. As for the development of level 1 and 3 chargers, research is mainly focused on finding the correct power electronics topology to increase charging performance and efficiency. However, there is a lack of research when it comes to attempting to apply power electronics stages within level 2 charging. Thus, this paper investigates the possibility of applying power electronics into residential level 2 EVSEs, while maintaining the requirements to keep it within fixed regulations. The choice of the system explored is mainly influenced by the topology of stages in DC chargers. These topologies are also challenged to see how charging performance and efficiency can be further improved. Finally, DLB is applied to the suggested system and its overall performance and feasibility is compared to the existing solutions to conclude if the system is a valid option.

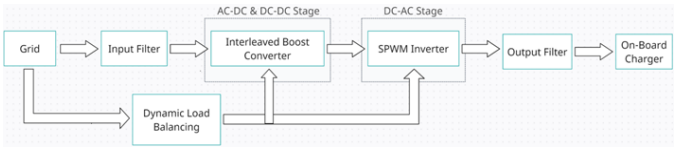

Figure 1: Overview of overall system

Therefore, the research is driven by the following three research questions: is it possible to apply power electronics stages in these EVSEs? If so, what are the advantages and disadvantages of such application? And finally, does applying power electronics stages in a level 2 EV charger improve the charging performance and application of DLB?

The paper will start by providing a preview and understanding of EV charging modes, regulations and requirements. This is followed by proposing an integration of power electronics stages in level 2 EVSEs and testing it by simulation. Finally, the DLB control system mechanism is discussed and tested.

II. Understanding EV Charging

The first step of introducing a new system into level 2 EVSE and seeking improvements on existing DC charger's topologies is to understand their functioning mechanism. Van den Bossche [1] has defined 4 charging modes, each with different requirements. The relevant ones for this research are Mode 3 and 4 since they are widely applied in EVSEs.

A. Charging Mode 1 and 2

Mode 1 and 2 charging are very similar with simple traits. They both imply a direct connection between the EV and the AC supply from the grid through a wire. The main difference is that mode 2 charging involves having a control box within the charging wire. This control box allows for additional safety considerations and applying a control pilot. Van den Bossche [1] emphasises a disadvantage in mode 2 charging, which is 'the control box protects the downstream cable and the vehicle, but not the plug itself, whereas the plug is one of the components more liable to be damaged in use.' Mode 1 and 2 are less available in the EU region due to the restrictions of their use in several countries in the EU. These restrictions, however, focus more on the larger vehicles, leaving space for mode 1 charging to be used for smaller vehicles like electric bikes and scooters [2].

B. Charging Mode 3

Moving onto mode 3 charging, there are no restrictions on their use due to its effective functionality, thus making it the most popular option for level 2 charging. This mode is similar to mode 2 where a control box is required between the AC supply and the EV; however, the control box is now required to be in an EVSE. This rids of the disadvantage of mode 2. The control box provides lightening, surge and current leakage protection and an emergency stop using varistors, circuit breakers, Residual Current Devices (RCDs), ground fault circuit interrupters and thermal sensors [3]. Van den Bossche [1] also mentions the presence of a control pilot conductor in the EVSE, or a control pilot alternative of it. This control pilot's main functions are [1]:

- 'Verification that the vehicle is properly connected'
- 'Continuous verification of the protective earth conductor integrity'
- 'Energization and deenergization of the system'
- 'Selection of the charging rate'

The control pilot is the main aspect of the communication protocol between the EVSE and the EV. Thus, any problems in this area have a direct effect on the charging performance of the charger. Lopez [4] discusses the importance of communication protocol in EV charging and how it is not prioritised when developing EVSEs. Although he implicitly says that there is no direct ratio highlighting how many EVSE malfunctions root from communication problems; he suggests that it could be a major factor in casuing these problems.

C. Charging Mode 4

The final charging mode explained by Van den Bossche [1] is mode 4. Unlike the previously discussed charging modes, this one does not have a direct link between the AC supply and the EV. Rather, off-board chargers are the mediator between them providing the EV with DC power. This allows the process to bypass the OBC and directly communicate with and charge the battery. The requirements of the control box remain in this charging mode to maintain the safety precautions. However, the control pilot works differently as the 'communication link is necessary to allow the charger to be informed about the type and state of charge of the battery, so as to provide it with the right voltage and current' [1]. This charging mode is found in level 1 and 3 charging where, respectively, low and high power DC output is provided from the off-board charger.

III. Level 2 Charger Design

A. Overall System Design

The first step of designing this system is deciding on the simulation platform that will hold it. The proposed system is divided into several subsystems and stages, and also considers the integration of DLB control, Simulink is used to design and simulate the system.

The next step is to decide on the overall system's structure. It is important to set the requirements and standards of the power electronics integrated level 2 charger to be designed. The charger needs to be single phase, have a AC input and AC output, have a controllable power output with a maximum output of $3680\ W$ and unidirectional. The reasoning behind choosing it to be single phase, up to $3680\ W$ power output and unidirectional is to keep the research limited to be on a simple residential example where the power grid is only single-phase and can provide 230 Vac with $16\ A$ of current, as shown in Equation 1.

$$P = VI = 230\ V * 16\ A = 3680\ W \tag{1}$$

With a large influence from DC charger circuit topologies that are discussed by Yilmaz and Krein [5], as well as the solid state transformer discussed by Moradewicz [6], the system in Figure 1 was chosen.

B. AC-DC and DC-DC Stage

1) Circuit Topology: As previously discussed, the design of the suggested power electronics integrated level 2 charger is highly influenced by the level 1 and 3 DC chargers. Thus, this stage was deduced by researching existing literature and models of DC chargers. Several resources discuss the same circuit topologies for this stage when considering the previously mentioned requirements. Musavi et al. [7] discuss three converter topologies that match the requirements of the power electronics integrated level 2 charger under design in this system: conventional boost converter, phase shifted bridgeless Power Factor Correction (PFC) boost converter and interleaved boost converter. The conventional boost converter was discarded due to its low efficiency at power levels higher than $1000\ W$, as well as the high ripple effects leaving the output capacitor with high ripple current.

The phase shifted bridgeless PFC and interleaved boost boost converters are better suited for power levels higher than $1000\ W$ and up to $3500\ W$. They both have parallel semiconductors operating $180\ ^\circ$ out of phase. This allows for the ripple effect to be reduced due to the cancellation of the ripples, which 'reduces stress on output capacitors' [5]. Comparing the efficiency and performance of these two topologies, Musavi et al. [7] provide plots of the efficiency of the converters at output power up to $3500\ W$. Within the standard range of input voltages in Europe (220-240 V), the interleaved converter had a slightly lower efficiency than the phase shifted bridgeless one (less than 1% difference in efficiency) at lower power loads.

However, there are tradeoffs when choosing either of them. An interleaved boost converter would lead to the need for better heat management due to the presence of a rectifier. On the other hand, using a phase shifted bridgeless converter would lead to higher ripple effects on both the input and output capacitors. Another main aspect to take into consideration is the sinusoidal input current of the interleaved boost converter while functioning in Discontinuous Conduction Mode (DCM). This is because the input current automatically follows the sinusoidal signal of the input voltage, which eliminates the need for control mechanisms [8]. Moreover, upon testing both topologies on Simulink, the phase shifted bridgeless converter had higher input reactive power than input active power, leading to overall low output active power no matter the efficiency. Thus, the interleaved boost converter was chosen.

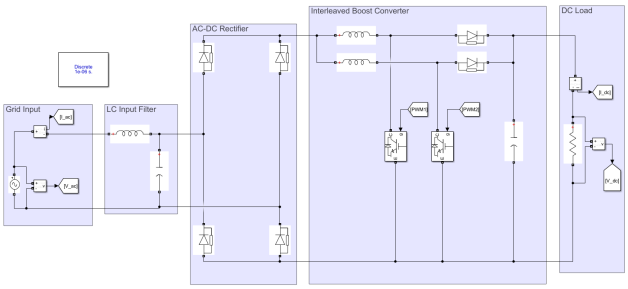

Figure 2: AC-DC and DC-DC stage overview

2) Input Filter: The first part of this stage is the input LC filter, which was added before the interleaved boost converter. The main reason for adding this filter is that it heavily reduces distortion. Distortion adds reactive power to the system, and without a stage to reduce them, the input current will have large peaks. Large peak currents will cause a negative impact on the grid. A major disadvantage about this stage is the fact that it introduces extra losses due to the series resistance of the inductor.

The values of the parameters in the LC filter are determined by tuning them towards the best balance between a good efficiency, standardised and non-distorted input current, and attainable components according to their inductance/capacitance value and power rating. The power rating was determined by taking the current measurement of the inductor and the voltage measurement of the capacitor. The input current directly flows through the inductor, thus the inductor should be able to handle a current of $16 * \sqrt{2} \approx 22.6\ A$. As for the capacitor, the voltage across it was measured and shown in Figure 3. Thus, the chosen values were a $30\ mH$ inductor rated at $25\ A$ and a $5\ nF$ capacitor rated at $300\ V$. For the capacitor real life use, several ones can be put in parallel, such as having a $3.5\ nF$ and $1.5\ nF$ capacitor in parallel, costing a total of around $1\,€$ or $2\,€$. As for the inductor, several ones can be placed in series to achieve such a high inductance. Due to the redundancy of inductors at such value and power rating, an option of inductance is two $12\ mH$ inductors [9] and one $6.3\ mH$ inductor [10], costing a total of $58.13\,€$.

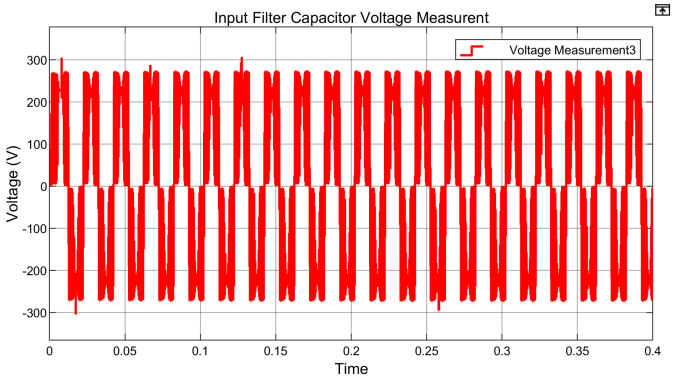

Figure 3: Voltage measurement the capacitor in the input filter

3) Interleaved Boost PFC Converter (PWM Signal): The interleaved boost converter has the Field Effect Transistors (FETs) or Insulated-Gate Bipolar Transistors (IGBTs) operating $180\ ^\circ$ out of phase. Thus, two Pulse Width Modulation (PWM) signals with this characteristic are generated. PWM signals can be a tool to control of the output power of the system without the need to change the grid input. This is done by changing the duty cycle of the signal. The higher the duty cycle, the more power is fed into to the system, allowing for larger power output. The $180\ ^\circ$ phase shift between the two signals is achieved as follows: a constant source is inputted to two PWM Generators, each followed by a Discrete Variable

Time Delay block, where the delay that causes the phase shift is inputted through another constant source block. The operating frequency of the PWM was chosen to be 10 kHz as it seems to be a common choice in models like those created by Shanmugam et al. [11] and Sanjeev et al. [12]. The PWM signals with a duty cycle of 30% can be seen in Figure 17 in section V and the 180 ° is also clearly visible. Each signal is inputted to an IGBT which is the switching device of choice over MOSFETs. The reason is that IGBTs are more typically used in high power applications, being better suited for high voltage and current. Moreover, the high switching speeds of the MOSFET are not necessary since the frequency is relatively low and unchanged [13].

4) Interleaved Boost PFC Converter (Component Parameters): Finally, the parameters of the components in the circuit are deduced. This is done by looking at the values of pre-existing models, as well as trial and error with the system, until a system with well balanced trade-off between the PF and quality of the output was achieved. Initially, Table II in [7] was used as the source for determining the values of the components. These values were later tuned to get a pleasing result while still maintaining feasible and attainable components in terms of price, size and availability. The inductors value was determined to be 500 μH each, the capacitor to be 2200 μF and the resistor to be 80 Ω as suggested by [14]. The required power ratings were obtained by measuring the current through one of the inductors and the voltage across the capacitor. Figure 4 shows the results attained from these measurements with the AC Voltage Source block set at 230 V Root Mean Square (RMS) with a PWM duty cycle of 50% and 16 A RMS input current drawn.

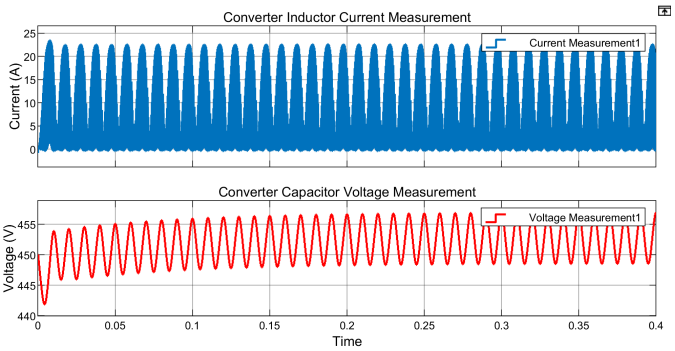

Figure 4: Current and voltage measurements of one of the inductors and the capacitor in the interleaved boost converter after setting initial capacitor voltage at 450V

Although the chosen capacitance is large and is required to have high power rating, capacitors with a power rating of 450 V can be placed in parallel to achieve the capacitance value determined. There are different options to get that, however, for simplicity in this research, a 2200 μF capacitor rated for 450 V found on AliExpress was chosen. Its price is 23 € and its dimensions are 100 × ⌀50 mm. As for the inductors, [10] includes a choke with an inductance of 0.48 mH at 10 kHz rated for 25 A. This is a convenient choice with a price of 12.31 € and dimensions of ⌀62.1 × 37.1 mm.

5) AC-DC & DC-DC Stage Results: The duty cycle of the PWM signal is set at 50%. This duty cycle allows for the normalised ripple RMS at both input and output capacitors in this circuit to be completely cancelled as suggested by [15]. The input and output readings are presented in the following figures.

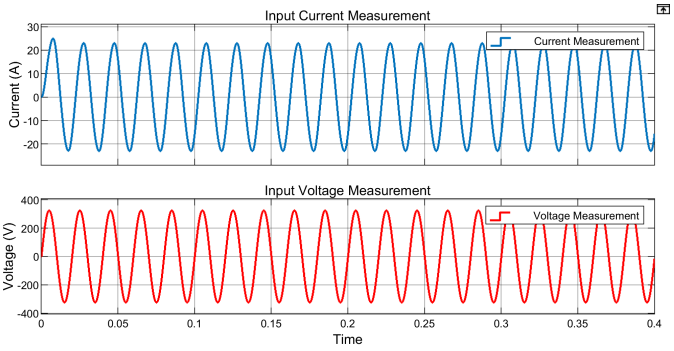

Figure 5: Input Current and Voltage Measurements with PWM Duty Cycle 50%

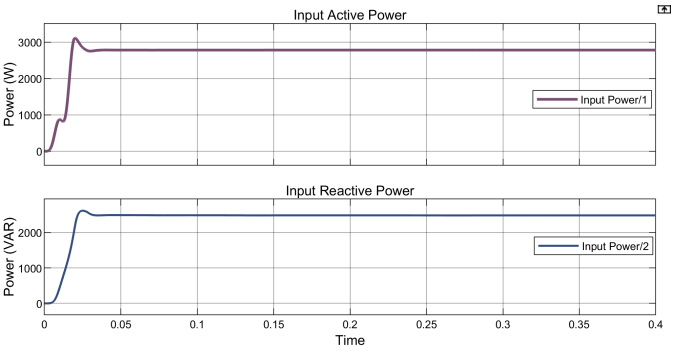

Figure 6: Input Active and Reactive Power with PWM Duty Cycle 50%

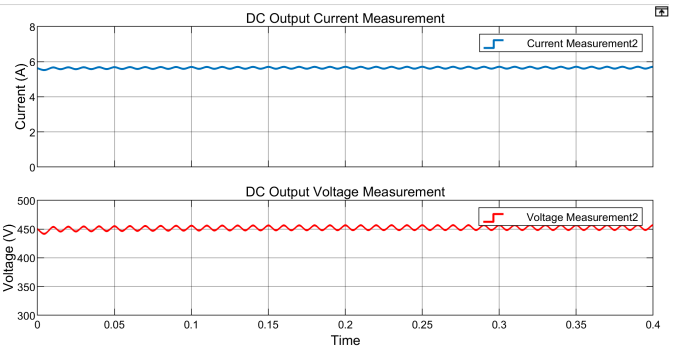

Figure 7: DC Output Voltage and Current Measurements on the Load Resistance with PWM Duty Cycle 50%

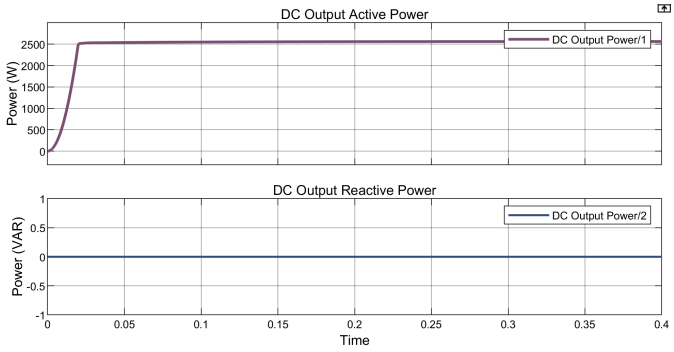

Figure 8: DC Output Active and Reactive Power on the Load Resistance with PWM Duty Cycle 50%

As can be seen, the input current is sinusoidal with an RMS value of approximately $16\ A$, maintaining a requested current input with the usual standards of residential power grids. The input active power is approximately $2780\ W$, and the DC output active power is approximately $2560\ W$. Thus, the efficiency can be calculated to be:

$$eff = \frac{P_{out}}{P_{in}} \times 100 = \frac{2560}{2780} \times 100 \approx 92\% \tag{2}$$

It can also be realised that the input active power is less than the intended total input power of $3680\ W$. This is due to the large amount of input reactive power (approximately 2400 VAR).

C. DC-AC Stage

In order to resemble the AC power output supplied by residential EVSEs, the DC output of the Interleaved Boost Converter is inverted to an AC signal. It seems counter-intuitive to add such a stage after the power has been provided in DC (which can be directly supplied to the battery). However, the purpose of the research is to compare the commercial and standard EVSEs that depend on communication protocol and control pilot with a system that includes power electronics. Power losses are inevitable in a system with such passive and active components functioning together. However, in scenarios where communication fails to make the charging experience live up to its expectations, this research investigates whether power electronics stages can be a valid substitute.

1) Inverter Topology: With the research purpose reassuring the purpose of the DC-AC inverter, the design process goes as follows. The inverter starts with an H-bridge with four switching devices. In the case of the proposed system, IGBTs were chosen again as previously discussed. This is followed by an LC filter which is used to filter out the high frequency components in the output voltage. Finally, the AC power is loaded on a resistive load. The resistive load was chosen according to the input impedance of the EV's OBC, which is connected to the EVSE with a type two cable that is designed to have negligible resistance as current is drawn through it, to the EV. The overall system, including the interleaved boost converter and the DC-AC inverter are depicted in Figure 9.

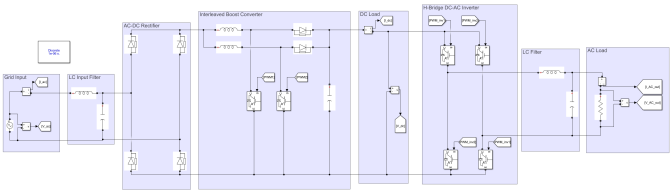

Figure 9: Overview of the Power Electronics Stages of the Suggested AC Residential Charger

2) SPWM Signal: The switching of the IGBTs is controlled via a Sinusoidal PWM (SPWM). Thus, the proposed inverter is a SPWM inverter, which, unlike a PWM inverter, generates an AC signal that has a sinusoidal shape. In order to get the initial SPWM that is fed into a pair of diagonally opposite IGBTs in a standard H-bridge, a sine wave and a repeating sequence are inputted to a relational operator ($\geq$). This means that as long as the sine wave is greater than the repeating sequence, the signal turns on. The width of the pulse varies across one period. The frequency of the sine wave block is set to be the desired frequency of the AC signal, which in the case of the inverter is $50\ Hz$. As for the repeating sequence, the carrier frequency will be kept at $10\ kHz$ just like the boost converter. The output of the relational operator gives us the switching signal for one pair of diagonally opposite IGBTs. In order to get the switching signal of the other pair, a 'NOT' logical operator is added to the output. The amplitude of the sinusoidal source block (V_{ref}) and carrier signal amplitude (V_c) directly impact the modulation index M [16], which is used to control $V_{out,RMS}$ [17].

$$V_{out,RMS} = M * \frac{V_{dc,in}}{\sqrt{2}} = V_{ref} * \frac{V_c * V_{dc,in}}{\sqrt{2}} \tag{3}$$

It might seem intuitive to just choose the highest value for V_{ref} in order to achieve high power output, or to choose its value according to the desired $V_{out,RMS}$. However, it is not that simple. Figure 7 shows the DC output voltage to be around $450\ V$ when a fixed load resistance is connected. However, now that the inverter is connected to the converter, the DC voltage depends on the duty cycle of the PWM of the converter, V_{ref} and the parameters of the output LC filter. The design of the LC filter will have fixed parameters, and the choice for these parameters .

With the desire to tune the PWM duty cycle and V_{ref}, there are several tradeoffs to take into consideration. The duty cycle chosen for the converter has already been reasoned according to [15]. Attempting a duty cycle in the ranges of $10\% - 49\%$ and $51\% - 55\%$ is still acceptable; however, they come with direct impacts on the system. Choosing a duty cycle within the $10\% - 44\%$ range causes the input current from the grid to not be sinusoidal.

Thus, duty cycles in the $45\% - 55\%$ range are tested alongside different values of V_{ref}. A higher value of V_{ref} causes the DC voltage to decrease and $V_{out,RMS}$ to increase, while a lower value causes the opposite. After testing different combinations, it was decided that $V_{ref} = 0.48$ and the duty

cycle stays as has been decided earlier at 50%. The SPWM signal can be seen in Figure 18 in section V.

3) Output LC Filter: The choice of parameters for the LC filter shown in Equation 4 was decided based on [18]:

$$LC = \frac{1}{(2\pi f_{cutoff})^2} \tag{4}$$

Where f_{cutoff} is the cutoff frequency of the filter. The cutoff frequency needed to follow to main requirements: $f_{cutoff} < 0.5 f_{carrier}$ and $f_{cutoff} \geq 10 \times f_{fundamental}$, where $f_{fundamental}$ is the fundamental frequency $= 10 \times 50\ Hz = 500\ Hz$. The current on the inductor and voltage across the capacitor were measured, and the peak values were taken into consideration to see the required power ratings for the LC components. This is shown in Figure 10.

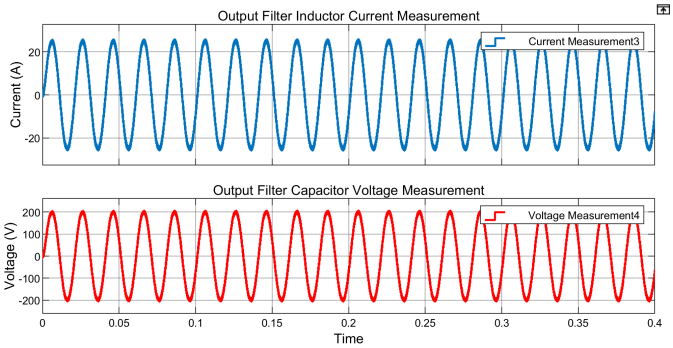

Figure 10: Current and Voltage Measurements of the Inductor and Capacitor in the LC Filter

There are several arrangements and combinations that can be done to achieve a $8.84\ mH$ inductor rated at around $25\ A$, and a $115\ nF$ capacitor rated at $200\ V$. One suggestion for the inductance is to have four $2.2\ mH$, $25\ A$ rated inductors [19] in series, reaching a cost of 109.68 €. As for the capacitance, one $100\ nF$ [20] and one $10\ nF$ [21] rated at $200\ V$, as well as the capacitors suggested for the input filter can be oriented in parallel to achieve $155\ nF$. Their total costs accumulate to 3.8 €.

4) Load Impedance: Finally, regarding the load impedance value, it was determined by calculating the input impedance of a virtual OBC found on Simulink examples [22], with Figure 19 in section V showing the model.

The voltage input was varied in order to test the limits of the OBC (minimum and maximum voltage input). Change in input voltage resulted in a linear change in current, which suggested the input impedance is resistive. The value of resistance was not the exact same for all input voltages, but was within the 10^0 order of magnitude; thus it was averaged out to be $8\ \Omega$.

5) Overall Power Electronics Integrated Charger Results: After designing the whole power electronics integrated level 2 charger, it needs to be simulated to observe its behaviour through some results.

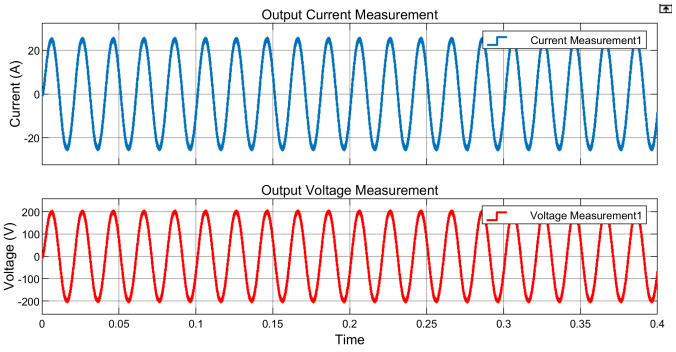

Figure 11: Voltage and Current measurements on the load resistance of the whole system

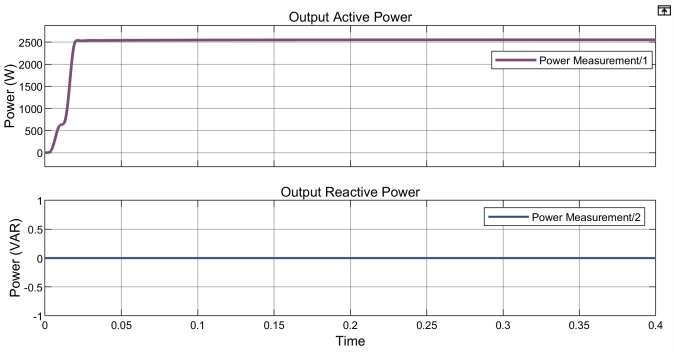

Figure 12: Load Power on the load resistance

The output power is measure to be approximately $2550 - 2560\ W$, which shows that the inverter has unity PF (or as close to unity PF as possible). This also shows that the system has a efficiency of 92%. Although the efficiency of the overall system is not too bad, the already existing EVSEs on the market usually have an efficiency higher than 99% [23]. The 92% efficiency also only represents a simulated power electronics integrated level 2 charger with idealised conditions. According to the suggested diodes and switches suggested by [7], the total power losses will not be less than $600 - 700\ W$ [24] [25]. Adding to that the standard losses in a $3600\ W$ rated inverter, which has a typical efficiency of 80% [26], the final efficiency will be around 61%. Therefore, the proposed power electronics integrated level 2 charger has added value if there is incompatibility between the EV and EVSE due to an incorrect choice of purchase from the EV user.

IV. Dynamic Load Balancing

In order to dynamically control the power output of the power electronics integrated level 2 charger, its working principle needs to be determined. The system will depend on the grid's voltage supply, which indicates if the grid is being overloaded, under-loaded or properly loaded. Ideally, the grid constantly outputs $230\ V$ RMS; however, with continuous variations on the loads used by the house, the voltage changes [27]. If the grid is supplying a larger amount of loads, the voltage decreases and vice versa. Another factor that

impacts grid voltage is the installation of photovoltaic (PV) panels, which can potentially cause over-voltage due to their intermittency [28]. Thus, the main aim of the control system is to charge the car with appropriate power levels, according to the grid's voltage measurement.

To do that, a feed-forward control system will be applied, that has the grid's voltage as its input and directly controls the duty cycle of the interleaved boost converter, which controls the power output of the power electronics integrated level 2 charger model. The voltage of the grid is assumed to have a maximum deviation of approximately $\pm 10\%$, so the control of the power electronics integrated level 2 charger will be designed to receive an input voltage ranging from $207-253\ V$. As for the control of the duty cycle, the standard one was chosen to be 50% with the fixed input voltage of $230\ V$ RMS. If the grid is supplying a lower voltage, the duty cycle needs to be decreased.

When designing the power electronics integrated level 2 charger, an optimised duty cycle took all aspects into consideration, including the output power, input current, normalised ripple RMS and EMI. Now however, the main point of concern is the input and output power. If the grid voltage is above $230\ V$, the intuitive choice would be to control the charger to charge the vehicle more by increasing the duty cycle. However, since the charger functions with an input current of $16\ A$ RMS, the power output has already been achieved by choosing these stages and parameters. Thus, an over-voltage should only be an indicator for the charger to keep charging.

As for the case where the voltage drops below $230\ V$ RMS, the power output can be decreased by decreasing the duty cycle. However, the minimum charging power for EVs is $1380\ W$ [29]. Different duty cycles were tested, and at 31% duty cycle and the maximally deviated input voltage at $207\ V$ RMS, the minimum power output is achieved as seen in Figure 13.

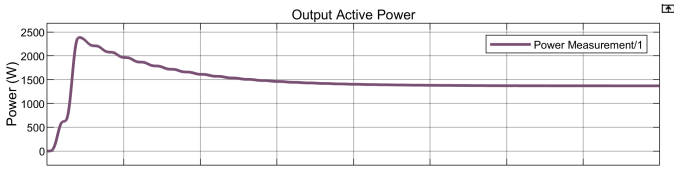

Figure 13: Power output of off-board charger at $207\ V$ RMS input voltage and 31% duty cycle

Moreover, it is wise to test if the OBC still functions properly if its input voltage is lower than the standard. This was done by simulating the OBC model shown in Figure 19 with low input voltages. At 31% duty cycle and $207\ V$ RMS input voltage, the output voltage of the power electronics integrated level 2 charger is $105\ V$ RMS. So, voltages $\geq 105\ V$ RMS were tested on the OBC model. The OBC still functions well at these input voltages, thus, the range to control the power electronics integrated level 2 charger during a grid voltage drop below $230\ V$ RMS is 31% up to 49%. Equation 5 controls the duty cycle (D) according to the input voltage (V_{in}):

$$D = 0.31 + \frac{0.5 - 0.31}{230\sqrt{2} - 207\sqrt{2}}(V_{in}\sqrt{2} - 207\sqrt{2}) \quad (5)$$

The control system will depend on conditional logic to apply the appropriate output. The input of the system is the input AC voltage $V_{in,AC}$ and the outputs are the duty cycle and V_{ref}. The last condition that needs to be discussed is when V_{in} is less than $207\ V$ RMS. If such scenario occurs, this suggests that the grid is too overloaded and the voltage has reached the minimum deviation, which poses danger to devices that do not have a tolerance to voltage deviations as big as this. Thus, charging completely stops, which requires both the duty cycle and V_{ref} to be zero. Figure 14 shows how the control system is integrated with the proposed power electronics integrated level 2 charger.

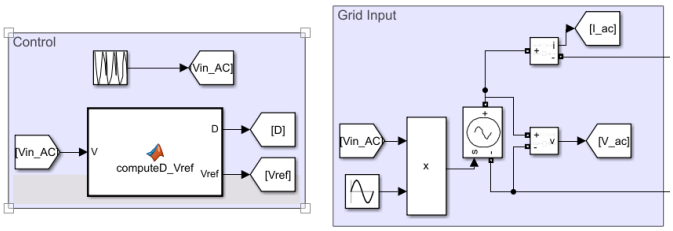

Figure 14: Control system integrated with the proposed power electronics integrated level 2 charger

A repeating sequence is fed into the input voltage. This repeating sequence includes arbitrary values of voltages within the $230 \pm 10\%\ V$ RMS range. These values represent readings taken from the grid at a frequency of 1 reading per 5 minutes. Thus, the control system updates the input voltage of the power electronics integrated level 2 charger at this rate, and it adjusts the power output accordingly. The power output adjustment is controlled through the MATLAB compute block, which controls the values of the duty cycle and V_{ref}. The code of the compute block can be seen in section V.

In order to test the control system, the simulation is scaled down to have the repeating sequence updates the value of the input voltage every 0.5 seconds for 6 seconds (12 intervals). This is a scale down of the actual control system which takes reading every 5 minutes and has 12 intervals in 1 hour. The arbitrary set of input voltages that follows this trend is [354.99, 327.75, 309.97, 326.34, 321.47, 309.58, 323.72, 334.61, 354.29, 347.58, 337.26, 312.76] V_{peak}. The input and output power of the simulation was measured and is shown in Figure 15 and Figure 16 respectively.

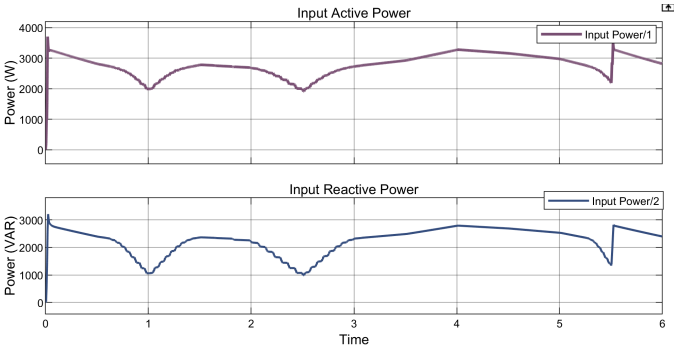

Figure 15: Input power measurements of fluctuating grid

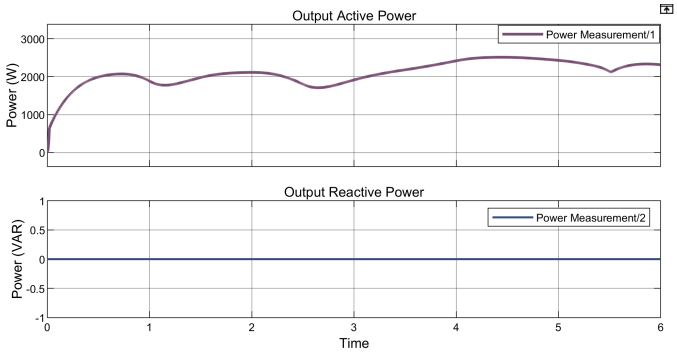

Figure 16: Output power on system's load with fluctuating input voltage

The added value of the power electronics stages and the control system is mainly presented here. Although the overall system experiences losses, it provides an advantage over EVSEs and DLB kits on the market. Existing solutions have the problem of only providing discrete output power values, according to the limited control of the input current [30]. Assuming the current provided by the grid is 16 A RMS, and the EVSE directly connects the OBC to the grid, requiring a minimum of 6 A to charge. The usual case is that the current provided to the OBC through the EVSE can be manually or automatically controlled by intervals of 1 A. This leads to the DLB kits only being able to output discrete values of power. However, the proposed system enables continuous DLB as can be seen in Figure 16. This allows EV charging to have better grid integration, since the output power is not limited to discretised values set by the communication protocols and regulations. Moreover, many smart charging and DLB algorithms assume that the power is continuously controllable, cause the system to be less effective than expected when actually applied in real life [31]. Thus, the proposed system helps overcome this problem.

V. Conclusion

This research paper investigated the integration of power electronics in level 2 EV charging, and the impact of such an integration on the charging performance and application of DLB. Designing power electronics stages to transfer power from the grid to the EV caused two major disadvantages. The first of which is the power losses along the electric component which lead to an efficiency of 92% compared to commercial EVSEs' 99%. The second major disadvantage is the high cost of the components required to achieve the proposed power electronics integrated level 2 charger. The price of only the passive components accumulates to around 200 € - 250 €. On the other hand, when applying the control system on the proposed charger, load balancing become continuously dynamic, whereas in commercial EVSEs, the load power has discretised values. Moreover, charging using power electronics and a dedicated DLB system achieves faster response than DLB using commercial EVSEs.

One of the main motives to attempt the power electronics integrated level 2 charger was the rare incompatibility between certain EVs and EVSEs. Thus, the proposed system can be used as an alternative to solve this issue. However, implementing this idea in real life would still require the presence of a control pilot. OBCs do not have the capability of alternating reception between a system that directly connects it to the grid, and one that indirectly connects it to the grid. Moreover, the OBC does not receive power unless the communication protocol of the control pilot commands it to. This aspect makes the proposed system inapplicable to level 2, mode 3 charging.

When considering mode 4 charging in level 1 and 3 DC chargers that already include power electronics, many aspects can be taken from this research. The first aspect is the topology of the converter and the filters in the system. For low power level 1 chargers, the interleaved boost converter functions really well and does not require control mechanisms or digital processing. Considering level 3 charging, the stages of the proposed power electronics integrated charger are not applicable in high power charging. However, the proposed control system would be a more robust way of dynamically controlling the power output (also in level 1 charging).

In conclusion, the proposed power electronics integrated level 2 charger is not an effective enough to be an applicable device competing in the market of EVSEs. The main focus required to solve the incompatibility problems between EVs and EVSEs should be in improving the control pilot. The advantages seen in the design of this system are much more useful when looking at EV system integration, smart charging and grid support.

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APPENDIX I

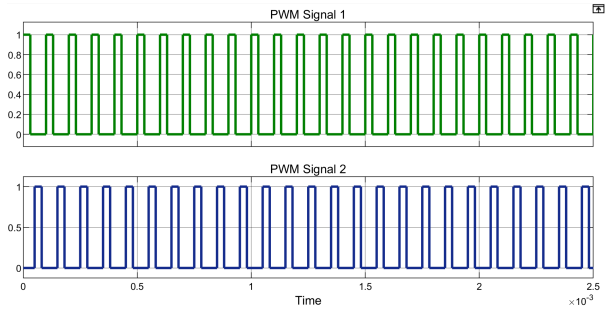

Figure 17: PWM signals inputted to the IGBTs of the interleaved converter with duty cycle 30%

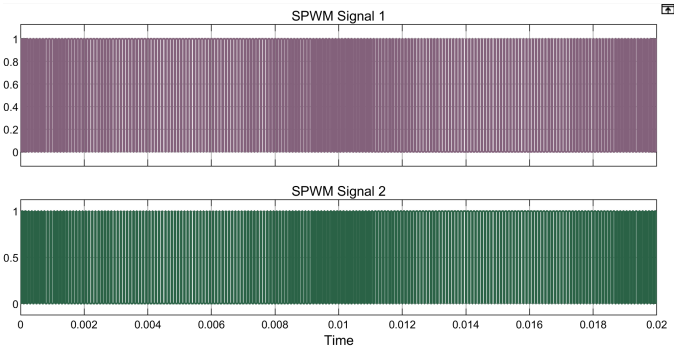

Figure 18: SPWM inputted to IGBTs in the inverter with $V_{ref} = 0.48$

APPENDIX II

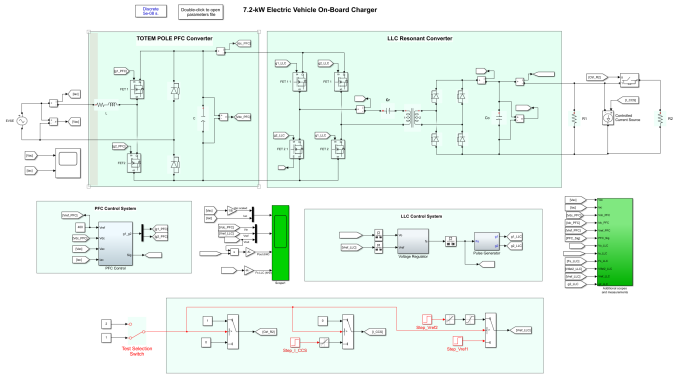

Figure 19: Virtual Model of OBC [22]

APPENDIX III

```
function [D, Vref] = computeD_Vref(V)
if V >= 325
    D = 0.5;
    Vref = 0.48;
elseif V >= 292.75
    D = 0.31 + ((0.5-0.31)/(325 - 292.75)
        * (V - 292.75);
    Vref = 0.48;
else
    D = 0;
    Vref = 0;
end
```