Fault-Ride-Through Capability and Interoperability of Grid-Forming Inverters in Microgrids

MASTER THESIS

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February 2024 / August 2024

Acronyms

BESSs Battery Energy Storage Systems. [7,](#page-7-0) [18,](#page-18-0) [26,](#page-26-0) [36,](#page-36-0) [54](#page-54-0)

- CMS Current Magnitude Saturation. [5,](#page-5-0) [47,](#page-47-0) [48,](#page-48-0) [52,](#page-52-0) [53,](#page-53-0) [58,](#page-58-0) [59,](#page-59-0) [61,](#page-61-0) [62,](#page-62-0) [65,](#page-65-0) [66,](#page-66-0) [68,](#page-68-0) [72,](#page-72-0) [81–](#page-81-0)[84,](#page-84-0) [87,](#page-87-0) [89,](#page-89-0) [90,](#page-90-0) [92,](#page-92-0) [98,](#page-98-0) [100](#page-100-0)[–103,](#page-103-0) [105–](#page-105-0)[110](#page-110-0)
- DNOs Distribution Network Operators. [9,](#page-9-0) [16,](#page-16-0) [50,](#page-50-0) [106,](#page-106-0) [107,](#page-107-0) [109,](#page-109-0) [111](#page-111-0)
- FRT Fault-Ride-Through. [4,](#page-4-0) [5,](#page-5-0) [7,](#page-7-0) [8,](#page-8-0) [14,](#page-14-0) [16–](#page-16-0)[20,](#page-20-0) [24,](#page-24-0) [47,](#page-47-0) [49,](#page-49-0) [56–](#page-56-0)[58,](#page-58-0) [61,](#page-61-0) [62,](#page-62-0) [64,](#page-64-0) [65,](#page-65-0) [68,](#page-68-0) [72,](#page-72-0) [79–](#page-79-0)[81,](#page-81-0) [83,](#page-83-0) [85–](#page-85-0)[87,](#page-87-0) [90,](#page-90-0) [92,](#page-92-0) [93,](#page-93-0) [96,](#page-96-0) [98–](#page-98-0)[103,](#page-103-0) [105,](#page-105-0) [106,](#page-106-0) [108–](#page-108-0)[111](#page-111-0)
- G-C Grid-Connected. [5,](#page-5-0) [7,](#page-7-0) [8,](#page-8-0) [15,](#page-15-0) [19,](#page-19-0) [20,](#page-20-0) [40–](#page-40-0)[42,](#page-42-0) [44,](#page-44-0) [54,](#page-54-0) [55,](#page-55-0) [76,](#page-76-0) [78–](#page-78-0)[82,](#page-82-0) [84,](#page-84-0) [85,](#page-85-0) [87,](#page-87-0) [89,](#page-89-0) [90,](#page-90-0) [92,](#page-92-0) [93,](#page-93-0) [96–](#page-96-0)[100,](#page-100-0) [103–](#page-103-0)[105,](#page-105-0) [107–](#page-107-0)[110](#page-110-0)
- GC Grid Codes. [8,](#page-8-0) [17,](#page-17-0) [20,](#page-20-0) [25,](#page-25-0) [41,](#page-41-0) [42,](#page-42-0) [56,](#page-56-0) [57,](#page-57-0) [59,](#page-59-0) [62,](#page-62-0) [65,](#page-65-0) [69,](#page-69-0) [75,](#page-75-0) [79,](#page-79-0) [82,](#page-82-0) [85,](#page-85-0) [89,](#page-89-0) [104–](#page-104-0)[106,](#page-106-0) [109–](#page-109-0)[111](#page-111-0)
- GFL Grid-Following Inverter. [4,](#page-4-0) [7,](#page-7-0) [8,](#page-8-0) [10–](#page-10-0)[14,](#page-14-0) [19,](#page-19-0) [39,](#page-39-0) [44,](#page-44-0) [46,](#page-46-0) [47,](#page-47-0) [54–](#page-54-0)[56,](#page-56-0) [64,](#page-64-0) [78,](#page-78-0) [79,](#page-79-0) [97,](#page-97-0) [98,](#page-98-0) [104](#page-104-0)
- GFM Grid-Forming Inverter. [4,](#page-4-0) [5,](#page-5-0) [7,](#page-7-0) [8,](#page-8-0) [12–](#page-12-0)[20,](#page-20-0) [23,](#page-23-0) [29,](#page-29-0) [35,](#page-35-0) [39,](#page-39-0) [40,](#page-40-0) [42,](#page-42-0) [44,](#page-44-0) [47,](#page-47-0) [54–](#page-54-0)[58,](#page-58-0) [61,](#page-61-0) [64–](#page-64-0)[66,](#page-66-0) [69,](#page-69-0) [72,](#page-72-0) [78–](#page-78-0)[81,](#page-81-0) [83,](#page-83-0) [85](#page-85-0)[–87,](#page-87-0) [89,](#page-89-0) [90,](#page-90-0) [92,](#page-92-0) [96–](#page-96-0)[111](#page-111-0)
- HIL Hardware-in-the-loop. [19](#page-19-0)
- IBRs Inverter Based Resources. [7–](#page-7-0)[12,](#page-12-0) [14–](#page-14-0)[20,](#page-20-0) [25,](#page-25-0) [28,](#page-28-0) [36,](#page-36-0) [39,](#page-39-0) [42,](#page-42-0) [45,](#page-45-0) [47,](#page-47-0) [49,](#page-49-0) [54–](#page-54-0)[56,](#page-56-0) [64,](#page-64-0) [69,](#page-69-0) [79,](#page-79-0) [105,](#page-105-0) [109](#page-109-0)
- LPF Low-Pass Filter. [12,](#page-12-0) [42](#page-42-0)
- PCC Point of Common Coupling. [10,](#page-10-0) [11,](#page-11-0) [13,](#page-13-0) [16,](#page-16-0) [17,](#page-17-0) [19,](#page-19-0) [23,](#page-23-0) [37,](#page-37-0) [39,](#page-39-0) [42,](#page-42-0) [44,](#page-44-0) [54,](#page-54-0) [59,](#page-59-0) [82,](#page-82-0) [105](#page-105-0)
- PLL Phase-Locked-Loop. [4,](#page-4-0) [7,](#page-7-0) [10–](#page-10-0)[14,](#page-14-0) [41,](#page-41-0) [44](#page-44-0)[–46,](#page-46-0) [55,](#page-55-0) [56](#page-56-0)
- PP Phase-to-Phase. [64,](#page-64-0) [65,](#page-65-0) [68](#page-68-0)[–72,](#page-72-0) [74–](#page-74-0)[76,](#page-76-0) [85,](#page-85-0) [86,](#page-86-0) [90–](#page-90-0)[93,](#page-93-0) [95](#page-95-0)[–97](#page-97-0)
- PVs Photovoltaic Panels. [7,](#page-7-0) [13,](#page-13-0) [26,](#page-26-0) [54,](#page-54-0) [109](#page-109-0)
- RESs Renewable Energy Sources. [6,](#page-6-0) [7](#page-7-0)
- RoCoF Rate of Change of Frequency. [13,](#page-13-0) [39,](#page-39-0) [40,](#page-40-0) [58,](#page-58-0) [105,](#page-105-0) [106,](#page-106-0) [109,](#page-109-0) [111](#page-111-0)
- SCR Short-Circuit Ratio. [7,](#page-7-0) [13,](#page-13-0) [55,](#page-55-0) [80,](#page-80-0) [105,](#page-105-0) [111](#page-111-0)

SGs Synchronous Generators. [7,](#page-7-0) [12,](#page-12-0) [14,](#page-14-0) [36,](#page-36-0) [39,](#page-39-0) [40,](#page-40-0) [104](#page-104-0)

SPG Single-Phase-to-Ground. [64–](#page-64-0)[69,](#page-69-0) [72,](#page-72-0) [73,](#page-73-0) [75,](#page-75-0) [76,](#page-76-0) [85,](#page-85-0) [87–](#page-87-0)[89,](#page-89-0) [92–](#page-92-0)[94,](#page-94-0) [96,](#page-96-0) [97](#page-97-0)

SPWM Sinusoidal Pulse Width Modulation. [21,](#page-21-0) [22,](#page-22-0) [36,](#page-36-0) [46,](#page-46-0) [65](#page-65-0)

- VI Virtual Impedance. [5,](#page-5-0) [18](#page-18-0)[–20,](#page-20-0) [47–](#page-47-0)[49,](#page-49-0) [52,](#page-52-0) [53,](#page-53-0) [61,](#page-61-0) [62,](#page-62-0) [65,](#page-65-0) [68,](#page-68-0) [69,](#page-69-0) [72,](#page-72-0) [83,](#page-83-0) [84,](#page-84-0) [90,](#page-90-0) [92,](#page-92-0) [99,](#page-99-0) [101–](#page-101-0)[103,](#page-103-0) [105,](#page-105-0) [106,](#page-106-0) [108](#page-108-0)[–110](#page-110-0)
- VSG Virtual Synchronous Generator. [5,](#page-5-0) [16,](#page-16-0) [19,](#page-19-0) [20,](#page-20-0) [29,](#page-29-0) [31,](#page-31-0) [39–](#page-39-0)[42,](#page-42-0) [55](#page-55-0)[–59,](#page-59-0) [61,](#page-61-0) [62,](#page-62-0) [65–](#page-65-0)[70,](#page-70-0) [72–](#page-72-0)[75,](#page-75-0) [78,](#page-78-0) [80,](#page-80-0) [82,](#page-82-0) [84,](#page-84-0) [85,](#page-85-0) [87–](#page-87-0)[97,](#page-97-0) [99,](#page-99-0) [100,](#page-100-0) [103](#page-103-0)[–111](#page-111-0)

WTs Wind Turbines. [7,](#page-7-0) [13,](#page-13-0) [19,](#page-19-0) [26,](#page-26-0) [109](#page-109-0)

Acknowledgements

Firstly, I am deeply grateful to my sponsor, the Ministry of National Education of the Republic of Türkiye, for providing me with all kinds of support and enabling me to pursue my education abroad. Throughout this thesis, I extend my endless thanks to my supervisors, Mr. Thiago Batista, Nataly, and Rutger, who have always been by my side at every stage and with every problem, providing me with unwavering any kind of support. Finally, I owe a debt of gratitude to my family, my fiance Bahriye, and to my esteemed friends both in Türkiye and the Netherlands, who have always stood by me throughout this process.

Contents

Chapter 1 Introduction

In the last few decades, the rapid advancement of technology and the extensive policies pursued by certain international organizations, such as the European Commission's zero-emission target by 2030 [\[1\]](#page-112-1) and the United Nations' Sustainable Development Goals $(11, 12, 13)[2]$ $(11, 12, 13)[2]$, have led the way for more environmentally conscious societies regarding climate change and carbon footprint issues. As a result, efforts towards sustainability and efficiency in energy have sharply increased. With these efforts, one of the new terms "Smart Grids" entered the literature around the mid-2000s and its popularity has been steadily increasing. Smart grids are simply a modern electrical distribution and management system that offers greater reliability, security, and efficiency compared to traditional electrical grids. Key features of these grids include data collection and communication, automation, renewable energy integration, consumer participation, capacity management, and security [\[3\]](#page-112-3).

Considering the developments mentioned above, it is not difficult to predict the rapid proliferation of [Renewable Energy Sources \(RESs\)](#page-1-6) worldwide. According to the report published by the European Energy Commission in 2021, the total energy produced in Europe consists of petroleum products (34%), natural gas (23%), renewable energy (17%), nuclear energy (13%) , and solid fossil fuels (12%) [\[4\]](#page-112-4). Taking into account that the share of [RESs](#page-1-6) in this ratio is not even 5% in the year 2000, the rate of increase is quite remarkable. For better clarity, the trend of the rise of [RESs](#page-1-6) for worldwide electricity generation is depicted in Figure [1.1.](#page-6-2)

Figure 1.1: RESs share $(\%)$ worldwide [\[5\]](#page-112-5)

The integration of [RESs,](#page-1-6) a phenomenon evident to date and poised to intensify even further in forthcoming years, is increasingly imperative for the modernization and resilience of existing power grids. In conventional power grids, the system predominantly relies on [Synchronous Generators \(SGs\)](#page-2-2) for power generation. These immense energy suppliers confer various benefits. With their colossal mechanical rotors, [SGs](#page-2-2) inherently contribute to the equilibrium of system frequency amidst load fluctuations or faults by harnessing their stored kinetic energy. Voltage and frequency regulation can be readily achieved through straightforward excitation and governor control mechanisms applied to [SGs.](#page-2-2) Furthermore, their low output impedance and nearly automatic adjustment of terminal voltage and frequency render them nearly impeccable voltage sources. Additionally, their robust resistance to fault currents (6-7 p.u.) naturally contributes to upholding grid stability in fault scenarios [\[6\]](#page-112-6). When aggregating all these attributes, the characteristics of [SGs](#page-2-2) play a pivotal role in ensuring system stability and the resilience of a robust grid. However, their leisurely response to faults, dependence on environmentally harmful sources such as natural gas, petroleum derivatives, and coal for fuel, and facilitation of unidirectional energy flow represent notable drawbacks [\[7\]](#page-112-7).

The rapid integration of [RESs](#page-1-6) into [SGs-](#page-2-2)based grids brings forth certain challenges. Except for hydroelectric power plants, [RESs](#page-1-6) such as [Wind Turbines \(WTs\),](#page-2-3) [Photovoltaic](#page-1-7) [Panels \(PVs\),](#page-1-7) [Battery Energy Storage Systems \(BESSs\),](#page-1-8) and super-capacitors are primarily [Inverter Based Resources \(IBRs\).](#page-1-9) Hence, power electronics-based circuits and their control methods are utilized to connect these sources to the grid. As [IBRs](#page-1-9) become dominant in grids, the absence of moving mechanical parts will significantly reduce system inertia. This will result in much faster responses to changes in system dynamics, requiring control methods to match this speed. Therefore, the most significant challenge in such electrical grids is achieving consistent and reliable voltage and frequency regulation [\[7\]](#page-112-7), [\[8\]](#page-112-8). Presently, almost 99% of these [IBRs](#page-1-9) are incorporated into the system using a method called [Grid-Following Inverter \(GFL\)](#page-1-0) [\[9\]](#page-112-9). As the name suggests, such control methods typically track the grid voltage and frequency through a [Phase-Locked-Loop](#page-1-1) [\(PLL\)](#page-1-1) and provide active and reactive power to the grid based on its instantaneous condition. However, in weak grids (e.g., those with a low [Short-Circuit Ratio \(SCR\),](#page-1-10) located far from the main power plant, predominantly or entirely based on [IBRs\)](#page-1-9), [IBRs](#page-1-9) cannot contribute to voltage and frequency regulation, leading to stability issues. These problems can sometimes escalate into significant issues or even large-scale system collapses in both [Grid-Connected \(G-C\)](#page-1-4) and Islanded modes in microgrids.

In recent years, a new inverter control method has been introduced to address such contingencies: [Grid-Forming Inverter \(GFM\).](#page-1-2) These inverters hold great promise in solving the issues encountered with [GFLs](#page-1-0). They have the capability to regulate terminal voltages based on predefined references without relying on grid voltage and frequency [\[10\]](#page-112-10). However, [GFMs](#page-1-2) are vulnerable to overcurrents in the event of a fault and may become permanently disabled if not properly controlled. To prevent this, research on [Fault-Ride-](#page-1-3)[Through \(FRT\)](#page-1-3) capabilities should be conducted thoroughly, and control methods should be optimized accordingly. Consequently, efforts to enhance [IBRs](#page-1-9) control methods and [FRT](#page-1-3) capabilities have inspired numerous studies in the literature.

1.1 Motivation

Given the aforementioned zero-emission targets for the future, it is undeniable that in the near future, electricity grids will be predominantly occupied by [IBRs.](#page-1-9) As discussed above, the ongoing transition will undoubtedly have adverse effects on our existing power systems. Investigating these effects and ensuring optimal integration of [IBRs](#page-1-9) into microgrids are among the focal points of contemporary engineers and mathematicians. Moreover, the interoperability of multiple connected [IBRs](#page-1-9) in the same microgrid is still open to investigation [\[11\]](#page-112-11).

There are numerous studies in the literature aimed at addressing these issues(lack of system inertia, vulnerability against over currents, etc.). Research on transitioning from [GFLs](#page-1-0) to [GFMs](#page-1-2) is progressing rapidly. However, due to the significant and rapid impact of system faults on [GFMs](#page-1-2), their [FRT](#page-1-3) capabilities need to be thoroughly researched and optimized. Various approaches and methods are proposed in the literature to enhance this capability. However, most of these studies have focused on a specific control method or [FRT](#page-1-3) capability under specific fault conditions (symmetrical or asymmetrical). In this regard, there is a lack of studies focusing on multiple [IBRs](#page-1-9) interoperability, comparing different [GFM](#page-1-2) control methods, and evaluating various [FRT](#page-1-3) approaches in such a multisystem context while considering their behavior in both [G-C](#page-1-4) and islanded microgrids [\[11\]](#page-112-11). Additionally, the optimization of [FRT](#page-1-3) capabilities of [IBRs](#page-1-9) according to varying [Grid Codes \(GC\)](#page-1-11) across different countries is a hot research topic.

This thesis is organized as follows: Section 2.1 discusses the technical background related to the topic. In Section 2.2, an overview of the literature on the subject is provided and accordingly, research questions are given in Section 2.3. In Chapter 3, under the methodology section, subsection 3.1 discusses the methods used to implement this thesis, subsection 3.2 addresses the types of errors to be applied, and subsection 3.3 examines the Dutch grid code. Chapter 4 also includes a detailed modeling of the system to be simulated. Sections 4.1, 4.2, 4.3, and 4.4 present in detail the modeling of the LCL filter, [GFM,](#page-1-2) [GFL,](#page-1-0) and [FRT,](#page-1-3) respectively. Subsequently, Chapter 5 presents the results under four subheadings: section 5.1 covers the [G-C](#page-1-4) mode, section 5.2 addresses the islanded mode, section 5.3 discusses interoperability, and section 5.4 contains the discussion. Finally, Chapter 6 provides the conclusion and future work.

Chapter 2 Scientific Background & Research Questions

2.1 Technical Background

In this section, the terms mentioned in this study will be explained in detail. It is worth noting that the technical details and structures of the inverter (topology, components, losses, etc.) itself will not be discussed since it is out of the scope of this thesis.

2.1.1 Microgrids

Within the scope of smart grids, the transition from centralized energy systems to local energy systems has gained momentum. Microgrids are local small-scale networks where the functions of generating, distributing, and consuming electrical energy can be carried out. These networks have the capability to operate either connected to the main grid or in a completely islanded mode. The rapid development of distributed energy systems has paved the way for the emergence of this term. Microgrids are systems in which [Distribution Network Operators \(DNOs\)](#page-1-12) and customers play an active role, enabling bidirectional energy transfer (from the grid to the consumer, and from the prosumer to the grid) and monitoring. They represent perhaps the largest energy flow model of the future, providing opportunities for new players to participate and enhancing standards both economically and in terms of security and reliability. The ability to operate independently from the main grid can offer significant advantages in terms of regional energy security. For example, in centralized systems, there is no priority given to any particular consumer in the event of power outages. Public necessities such as hospitals and military installations, despite having backup power sources such as uninterruptible power supply (UPS) or standby generators, which are only short-term solutions, ensuring energy continuity can be vital. However, microgrids, with active involvement from [DNOs,](#page-1-12) can ensure energy continuity by controlling energy flow. Moreover, in areas where there is no connection to the main grid or where the grid is weak, the presence of microgrids will significantly improve the quality of life for inhabitants [\[12\]](#page-113-0), [\[13\]](#page-113-1). Figure [2.1](#page-10-2) provides an example diagram of a microgrid. On the other hand, the intermittent nature of [IBRs](#page-1-9) commonly used in microgrids leads to a lack of inertia and, consequently, system instabilities. When connected to the grid, they do not pose stability issues as voltage and frequency regulation is provided by the main grid, and they assume the role of providing power support to the grid. However, in islanded mode, this situation results in the system being unreliable. Even small fluctuations in the system can lead to significant imbalances in frequency or voltage. Stability in power systems comprises voltage, frequency, and small signal stability, which are the main stability components of the system following any unexpected conditions (such as various faults and the inclusion/exclusion of different types of loads from the system).

Figure 2.1: Sample microgrid diagram [\[14\]](#page-113-2)

Microgrid stability focuses primarily on control systems and power balance. Figure [2.2](#page-10-3) illustrates a detailed classification of stability for microgrids. However, these instabilities will not be discussed in detail since they are not the main subject of this work. The small size of the system, the inherent uncertainty in the characteristics of system components, the low X/R ratio (causing active and reactive coupling), the high integration of IBRs, small short-circuit current capacity, and unbalanced three-phase loading are parameters that differentiate microgrids from bulk power grids in terms of stability [\[15\]](#page-113-3), [\[16\]](#page-113-4), [\[17\]](#page-113-5).

Figure 2.2: Microgrid instability classifications [\[15\]](#page-113-3)

2.1.2 [Grid-Following Inverter \(GFL\)](#page-1-0)

The majority of [IBRs](#page-1-9) connected to main grids operate with [GFL](#page-1-0) control, accounting for about 99 %. Although there is not a precise definition in the literature, [GFLs](#page-1-0) are generally conceptualized as a parallel-connected large impedance fixed current source. Figure [2.3a](#page-11-2) depicts the simplified Thevenin circuit of [GFL,](#page-1-0) while [2.3b](#page-11-2) illustrates variations of [GFL.](#page-1-0) In Figure [2.3a,](#page-11-2) V_{PCC} and i_{PCC} represent the [Point of Common Coupling \(PCC\)](#page-1-13) parameters used in the calculation for adjusting the output of the [GFL.](#page-1-0) Z_g is the equivalent line impedance. The currents I_d^* and I_q^* (in the dq frame) are obtained by regulating the voltage using phase angle information from the [PLL.](#page-1-1) Subsequently, these currents are transformed back to the natural (abc) frame before being applied to the output. As a result, the control of active and reactive power support occurs through the manipulation

of d-q currents [\[7\]](#page-112-7), [\[18\]](#page-113-6). The abc/dq transformation process will be examined in section 3.1.

(a) Thevenin equivalent circuit of [GFL](#page-1-0)

(b) [GFL](#page-1-0) variations

Figure 2.3: [GFLs](#page-1-0) overview

In the [GFL](#page-1-0) control case, the phase angle information of the voltage at the [PCC](#page-1-13) is conveyed to the inverter through a [PLL,](#page-1-1) and based on this angle, the output voltage angle of the [GFL](#page-1-0) is locked to the output voltage at the [PCC.](#page-1-13) Meanwhile, the current is constant, and the voltage values are regulated. The reference voltage values are based on line currents. [GFLs](#page-1-0) can be divided into two categories. In Grid-Feeding (GF) mode, the inverter operates in Maximum Power Tracking (MPTT) mode, aiming to provide as much active power as possible. However, they do not provide reactive power support. In Grid-Supporting (GS) mode, both active and reactive powers are adjusted based on various control methods according to the instantaneous condition of the grid. When the number of GFs increases significantly in a microgrid, ensuring voltage and frequency stability becomes very challenging due to their inability to provide reactive power support [\[7\]](#page-112-7). Therefore, some restrictions are imposed on these inverters by grid operators. According to these limitations, GFs must provide reactive power based on the grid requirements [\[7\]](#page-112-7).

In the context of [GFLs](#page-1-0), they do not contribute any inertia to the grid. They merely synchronize their outputs to it, aligning with the values provided by the grid. This implies a lack of regulation capability over output voltage and frequency [\[19\]](#page-113-7). Consequently, in weak grids or networks predominantly composed of [IBRs,](#page-1-9) this situation can lead to significant instabilities because, in weak grids, [PCC](#page-1-13) voltages are quickly influenced by output currents, leading to continuous deviations of voltages [\[20\]](#page-113-8). While [GFLs](#page-1-0) can provide both active and reactive power support to the grid, this process introduces a delay due to voltage and current calculations and other control procedures, thereby also potentially causing stability issues [\[21\]](#page-113-9).

2.1.2.1 [Phase-Locked-Loop \(PLL\)](#page-1-1)

Currently, nearly all [GFLs](#page-1-0) employ [PLL](#page-1-1) for synchronization with the grid [\[22\]](#page-113-10). Therefore, it is deemed necessary to explain the [PLL](#page-1-1) in the context of [GFLs](#page-1-0). Figure [2.4](#page-12-2) depicts the control scheme of [PLL.](#page-1-1)

Figure 2.4: [PLL](#page-1-1) control scheme

As seen in the Figure [2.4,](#page-12-2) the [PLL](#page-1-1) structure consists of three main control stages. A Voltage Controlled Oscillator (VCO) generates voltage wave outputs at a frequency proportional to the applied voltage. The phase detector compares the phase angle information of the input signal and the feedback signal from the VCO and sends the output signal to a [Low-Pass Filter \(LPF\)](#page-1-14) to obtain a clean sample for VCO. The task of the [PLL](#page-1-1) is to ensure frequency synchronization between the inverter input and output. A feedback signal is subtracted from the input signal, and as long as the resulting error signal is non-zero, the loop repeats. When the difference is zero, it means that the input and output are synchronized. Additionally, the [PLL](#page-1-1) has minimum and maximum frequency ranges. If the frequency of the input signal is below or above these values, the [PLL](#page-1-1) cannot provide further synchronization, leading to significant discrepancies between the parameters of the main grid and the inverter output, thereby causing imbalances in the grid. Some previous research has also shown that [PLLs](#page-1-1) can induce substantial stability issues, particularly in weak grids [\[21\]](#page-113-9).

2.1.3 [Grid-Forming Inverter \(GFM\)](#page-1-2)

The problems mentioned above with [GFLs](#page-1-0), along with the increasing penetration of [IBRs](#page-1-9) in grids, have led to a rapid increase in research aimed at enhancing grid stability in the literature. As a result of simulations and limited applications so far, a promising novel control method has been proposed: [GFM.](#page-1-2) However, despite the numerous studies conducted, there is still no clear definition of [GFM](#page-1-2) even today [\[23\]](#page-113-11). Different regulatory bodies advocate for different requirements for [GFM.](#page-1-2) For instance, the European Network of Transmission System Operators for Electricity (ENTSO-E) argues that [GFM](#page-1-2) capabilities should be specifically defined in grid codes to fully meet the specific network needs/service requirements [\[24\]](#page-114-0), while the National Renewable Energy Laboratory (NREL) advocates for [GFM](#page-1-2) to be interoperable with other energy sources and capable of adjusting output voltage instantaneously without the need for [PLL](#page-1-1) [\[25\]](#page-114-1). On the other hand, the National Grid ESO asserts that [GFM](#page-1-2) should at least provide virtual [SGs](#page-2-2) characteristics and services [\[26\]](#page-114-2).

Figure 2.5: Thevenin equivalent circuit of [GFM](#page-1-2) [\[7\]](#page-112-7)

However, from a simplified general perspective, this method can be described as a voltage source with a low-impedance connected in series to it. As seen in Figure [2.5,](#page-13-1) unlike [GFL,](#page-1-0) [GFM](#page-1-2) does not require a synchronization tool such as [PLL,](#page-1-1) which could lead to the problems mentioned above. The values at the [PCC](#page-1-13) are used to detect fault conditions and provide active/reactive power support rather than synchronizing with the grid. Instead of synchronizing with the grid and following references, [GFM](#page-1-2) shapes the voltage and frequency values at the output terminal of the inverter according to preset values. Typically, sources such as [WTs,](#page-2-3) and [PVs,](#page-1-7) located in remote areas, have increasing line impedance, resulting in a decrease in the [SCR](#page-1-10) and indicating a weak grid inertia [\[10\]](#page-112-10). Inertia is defined as the sudden power response given in proportion to the [Rate of](#page-1-15) [Change of Frequency \(RoCoF\).](#page-1-15) Figure [2.6](#page-13-2) illustrates a comparison of frequency deviations occurring in the grid during an electricity generation/load imbalance situation for both strong (high inertia) and weak (low inertia) grids. Considering the deficiencies of [GFLs](#page-1-0) under such conditions mentioned above, the adoption of [GFM](#page-1-2) inverters can be considered vital.

Figure 2.6: [RoCoF](#page-1-15) comparison in strong and weak grids [\[27\]](#page-114-3)

The main difference between [GFM](#page-1-2) and [GFL](#page-1-0) lies in their methods and priorities for supplying power to the grid. The priority of [GFM](#page-1-2) is to regulate voltage and frequency, leading to continuous fluctuations in both active and reactive power. On the other hand, in [GFL,](#page-1-0) grid voltage support is secondary, and it primarily focuses on providing active power. [GFM](#page-1-2) inverters contribute to grid inertia and enhance system stability through their ability to control voltage and frequency at the output. While [GFLs](#page-1-0) may provide reactive/active power support, this process requires the calculation of current and voltage values and the provision of appropriate support conditions, leading to delays in urgent reactions. This is different for [GFM](#page-1-2) inverters. Take a grid disturbance (could be (a)symmetric fault) as

an example, the power transfer formula for [GFM](#page-1-2) is as follows [\[7\]](#page-112-7),

$$
P = \frac{V_g \cdot V_{inv}}{X} \cdot \sin(\Delta \delta)
$$
\n(2.1)

As shown in [\(2.1\)](#page-14-1): V_g represents the grid voltage, V_{inv} represents the inverter voltage, $\Delta\delta$ is the angle difference between these two voltages, and X is the coupling impedance. Since the inverter inner loop voltage is not directly affected at the beginning of the disturbance, a rapid response can be provided based on the change in phase angle difference. According to the requirements outlined in the updated IEEE1547-2018 standards [\[28\]](#page-114-4), which serve as a reference for grid codes applied to [IBRs,](#page-1-9) these sources are required to remain connected to the grid for specific short periods during a fault condition and provide a rapid response, disconnecting after a designated time. [GFMs](#page-1-2) offer a significant advantage in this regard. Furthermore, in terms of small-signal stability, in weak grids, [GFMs](#page-1-2) prevent the increasing frequency and voltage fluctuations compared to [GFLs](#page-1-0), as they do not require synchronization. In islanded mode, [GFMs](#page-1-2) adjust their output voltage without the need for any reference. Furthermore, [GFMs](#page-1-2) respond more quickly to frequency regulation compared to [SGs,](#page-2-2) which rely on stored kinetic energy, as they respond electronically [\[10\]](#page-112-10). They possess black start capability and can energize the system from scratch.

However, despite all these advantages, there are certainly some significant disadvantages. Firstly, as they are controlled as voltage sources, they naturally lack any current limiting features. Considering the sensitivity of semiconductor active circuit elements such as Mosfets and IGBTs to overcurrents, extra precautions must be taken against overcurrents. Otherwise, these circuit elements can suffer serious damage and become completely non-functional even if the current exceeds 1.2-1.5 p.u. [\[29\]](#page-114-5). Additionally, some studies indicate that [GFMs](#page-1-2) can cause stability issues in strong grids [\[30\]](#page-114-6). According to authors in [\[31\]](#page-114-7) and [\[27\]](#page-114-3), the capabilities of [GFMs](#page-1-2) can be structured as follows:

- [GFMs](#page-1-2) must operate in the form of voltage sources.
- [GFMs](#page-1-2) must have [FRT](#page-1-3) capability. This entails remaining connected to the grid and providing power support during a disturbance.
- [GFMs](#page-1-2) should contribute to system inertia.
- Control methods should prevent interactions and impacts among other energy sources.
- [GFMs](#page-1-2) should provide clean signal output and absorb harmonics in the signals.
- Generally, they should be able to absorb negative and zero sequence voltages and currents that typically occur during asymmetric faults.
- They should also have blackout capability, so there is no [PLL](#page-1-1) utilization in the main control of the inverter.

Taking into account the listed items, the fulfillment of these requirements positions [GFMs](#page-1-2) as promising tools in the development and proliferation of current and future smart grids. However, naturally, meeting all these requirements necessitates complex control methods. Besides, they are required to follow different grid codes implied by different countries. In addition to [GFMs](#page-1-2) control methods, there is also considerable research on optimizing their [FRT](#page-1-3) capacities. The mentioned control methods and [FRT](#page-1-3) optimization techniques will be discussed in the following sections.

2.1.4 [GFM](#page-1-2) Control Stages & Methods

[GFMs](#page-1-2) have numerous control methods developed for them today. These control methods are utilized to enhance inverter performance and ensure system stability. Before discussing the control methods, it would be appropriate to discuss the control stages. This section will first cover the control stages, followed by an overview of control methods found in the literature, with the most common ones selected for implementation in this thesis. Additionally, the mathematical explanations and modeling of the discussed control strategies are provided in the subsequent chapter.

2.1.4.1 Control Stages

In [G-C](#page-1-4) mode, voltage and frequency are imposed on [IBRs](#page-1-9) by the grid. However, in islanded mode, the inverter must handle this task itself. The applied control strategy is based on fulfilling this obligation. To ensure the fulfillment of these requirements, a hierarchical and tiered control strategy is employed. The control strategy can be divided into four parts: Inner loop, primary loop, secondary loop, and tertiary loop. An overview of these stages is depicted in Figure [2.7.](#page-15-3)

Figure 2.7: GFM control stages [\[32\]](#page-114-8), [\[33\]](#page-114-9)

The inner loop comprises cascaded voltage and current loops. Its task is to continuously monitor system parameters and generate output values according to references from primary control. It is the fastest loop and works at 1-5 milliseconds level. Following the inner loop, the primary control loop is the fastest to transition to the decision-making stage and operates at a timescale of 10 milliseconds. No communication medium is required in this loop; instead, reliance is placed on calculated values. The primary control's main objectives are to ensure power-sharing balance, stabilize voltage and frequency, detect islanded mode, and generate voltage and frequency reference values for the inverter terminal. The secondary control stage operates at a frequency of 100 milliseconds. It assists in minimizing minor fluctuations in voltage or frequency within a microgrid. Additionally, secondary control can contribute to optimizing the grid economically (e.g., power quality/signal quality). Lastly, in the tertiary control stage, the response time can range from seconds to minutes. This section is also referred to as Global Loop Control. Here, the [IBRs](#page-1-9) connected to the grid calculates their optimal operating range based on the production-load balance. It is beneficial to note that in this thesis tertiary control will not be implemented since it is not the scope of this research.

2.1.4.2 Primary Control Methods

Various control methods are developed for [GFMs](#page-1-2). Although the control techniques may differ, their objectives are to meet the [GFMs](#page-1-2) characteristics according to the requirements of [DNOs.](#page-1-12) Figure [2.8](#page-16-3) provides a general overview of the control methods found in the literature. Among these control methods, the most mature and widely used ones are Frequency-Based Droop Control and [Virtual Synchronous Generator \(VSG\).](#page-2-1) Other control methods such as Virtual Oscillator Based, Synchronverter, etc.(Fig. [2.8\)](#page-16-3), still in the development stage, have disadvantages or way more complex structures compared to these and, will not be included in this study. However, further information can be found in Reference [\[7\]](#page-112-7). It's worth noting that, to prevent complexity and facilitate understanding, Frequency-Based Droop Control will be simply referred to as droop control. Modeling of these two methods will be discussed in detail in the next chapter.

Figure 2.8: [GFM](#page-1-2) Control Methods Overview

2.1.5 [Fault-Ride-Through \(FRT\)](#page-1-3) Approaches

Although [GFMs](#page-1-2) provide positive outcomes in terms of system stability and operability under steady-state conditions, common grid faults encountered in daily life pose a threat to their regular operation. Specifically, as [GFMs](#page-1-2) are designed as voltage sources, any change at the [PCC](#page-1-13) easily affects the output current. While it is possible to enhance the low overcurrent capacities of inverters, it is not economically practical [\[34\]](#page-115-0). To protect inverters with maximum current capacities typically around 120% of the nominal current capacity from any harm and, more importantly, to ensure system security and reliability, it is necessary to examine their [FRT](#page-1-3) behaviors. [FRT](#page-1-3) can be summarized as controls that

enable the [IBRs](#page-1-9) to remain connected to the grid without damage and to provide support to the grid according to specific [GC](#page-1-11) during situations that cause voltage, frequency, and current fluctuations such as faults, and load shedding/acquisition. Improving the [FRT](#page-1-3) capabilities of [GFMs](#page-1-2) and optimizing their systemic behaviors in accordance with IEEE 1547-2018 standards in the event of a fault is as crucial as developing the [GFM](#page-1-2) control methods themselves [\[35\]](#page-115-1), [\[36\]](#page-115-2).

Although IEEE standards provide a framework for the performance of [GFMs](#page-1-2) during fault conditions, different [GC](#page-1-11) modify performance based on region or requirements. For example, in some countries, the [IBRs](#page-1-9) must stay connected for a typical period of 2 seconds even if the [PCC](#page-1-13) voltage drops to 0, requiring the [IBRs](#page-1-9) to support the grid, while in some other countries, the voltage drop rate is limited to around 20%. In the event of a major fault, overcurrent/overvoltage (DC link voltage) and system desynchronization may occur. Therefore, generally, [GC](#page-1-11) impose the following requirements on [GFMs](#page-1-2):

- they must remain connected to the grid for a certain period,
- they must provide reactive current injection to regulate grid voltage,
- their DC link capacitor must be protected from overvoltages,
- their semiconductor switches must be protected from overcurrents,
- and adjust system transitions(fault recovery) during normal and fault conditions.

To meet the requirements mentioned above, it is possible to categorize widely researched [FRT](#page-1-3) approaches in the literature into two main headings: control/software-based and external electronic circuit-based methods [\[37\]](#page-115-3). The diagram provided in Figure [2.9](#page-17-2) illustrates common [FRT](#page-1-3) approaches found in the literature.

Figure 2.9: Common [FRT](#page-1-3) approaches [\[38\]](#page-115-4)

2.1.5.1 Control/Software-Based Methods

Control method modification is achieved through alterations/additions to the control system of the inverter. Functions such as overcurrent protection, instantaneous current saturators, and current peak limiters are employed to address overcurrents while providing voltage support to the grid during faults. In studies falling under this category, various designs such as anti-windup methods to address the wind-up issue of PI controllers, and dual current controllers to manage negative and zero sequence components in asymmetric faults, are implemented to significantly enhance the [FRT](#page-1-3) capabilities of [IBRs.](#page-1-9) Particularly, current limiters and [Virtual Impedance \(VI\)-](#page-2-0)based approaches have yielded highly effective results. Another category, computational methods, involves implementations such as Fuzzy Logic and Particle Swarm Optimization. While some of these methods meet partial grid code requirements, others neglect certain aspects. For instance, while some studies successfully restrict overcurrent values, they may overlook reactive current injection. Additionally, studies that fulfill all [FRT](#page-1-3) requirements tend to be more complex compared to their counterparts discussed under the previous category [\[37\]](#page-115-3), [\[38\]](#page-115-4). While there are some new methods that could be added to the list, they are currently in the research stage and will not be mentioned here. In conclusion, current saturators and VI methods, which have yielded the most favorable results in the literature regarding system response, will be implemented in this thesis.

2.1.5.2 Electronic Circuit-Based Methods

In the literature, [BESSs](#page-1-8) are connected in parallel with the DC link capacitor of the [GFMs](#page-1-2), detecting and absorbing voltage increases during faults, and providing active power support to the grid after the fault. However, the installation and maintenance of this method are costly, and it does not contribute to voltage regulation in the grid, only providing active power support. In the FACTS method, the necessary requirements (such as voltage regulation, and overcurrent limitation) are met, but the cost of these devices is even higher than that of [BESSs.](#page-1-8) On the other hand, the Braking Chopper method is an effective technique for limiting overcurrents in [GFMs](#page-1-2). Essentially, it consists of a resistor and a semiconductor switch connected in parallel with the DC link capacitor. During a fault, the switch is closed based on a fault signal, and the excess energy in the DC link is absorbed through the resistor. However, this method does not provide any voltage regulation support to the grid [\[37\]](#page-115-3), [\[38\]](#page-115-4). While there are other methods that could be added under this heading, they will not be discussed here due to their effectiveness, cost, complexity, or immaturity. The most promising methods are mentioned in [\[37\]](#page-115-3) and [\[38\]](#page-115-4). However, the methods under this heading have not been implemented in this thesis due to concerns regarding feasibility and cost-performance.

2.2 Related Works

In this section, previous studies in the literature aimed at enhancing the [FRT](#page-1-3) capabilities of [GFMs](#page-1-2) and interoperability will be examined. Since the main research focus of this thesis is to compare the [FRT](#page-1-3) capabilities of [GFMs](#page-1-2) and behaviours of them when they operated together, the focal point of the literature review will be the conducted [FRT](#page-1-3) studies and interoperability of [IBRs.](#page-1-9)

In [\[29\]](#page-114-5) and [\[35\]](#page-115-1), the authors examined the behavior of a wind turbine implemented with Droop control using an adaptive [VI](#page-2-0) method, focusing solely on its performance under asymmetric faults. These studies applied different methods considering positive and negative sequence components and achieved similar results, but did not consider transient current jumps. Reference [\[34\]](#page-115-0) presented a circuit design incorporating an additional H-bridge and parallel compensation inductance to limit overcurrents. While the designed circuit successfully constrained overcurrents, it did not address reactive current support to the grid. Reference [\[39\]](#page-115-5) utilized adaptive inertia and [VI](#page-2-0) methods in the control strategy developed for [VSG-](#page-2-1)controlled [GFM](#page-1-2) systems. Although longer-term faults are simulated, specific fault types(only three and one phase faults) are applied in the simulations. Considering the different dynamic effects of various faults on the system, applying different types of faults is crucial. In reference [\[36\]](#page-115-2), the crowbar resistor method is employed to limit DC link overvoltages and [PCC](#page-1-13) overcurrents, considering newly proposed [G-Cs](#page-1-4). However, this study also focused solely on Droop control and managed to provide necessary reactive power support to the grid for some faults. Reference [\[40\]](#page-115-6) explored DC-link voltage control to enhance low-voltage [FRT](#page-1-3) capability, while reference [\[41\]](#page-115-7) utilized a DC-linked supercapacitor as an energy buffer during fault conditions. However, neither of these studies provided a solution for the 0.2 p.u.-volt voltage drop required by [G-Cs](#page-1-4). In [\[42\]](#page-115-8), effects of dynamic power flow on [IBRs](#page-1-9) and grids are investigated by utilizing real grid data, with a focus on load dynamics. In [\[43\]](#page-115-9), two different Droop methods are compared, and small signal analysis is conducted using [Hardware-in-the-loop \(HIL\)](#page-1-16) real-time simulation. Although detailed analysis is conducted in small signal analysis, the study did not address grid faults specifically. In [\[44\]](#page-115-10), a [VI](#page-2-0) based on instantaneous current values is designed and tested using [HIL](#page-1-16) simulation for fault conditions. The study focused on single-phase inverters and Droop control. Another study converted an inverter used in [GFM](#page-1-2) to [GFL](#page-1-0) to control overcurrents during faults [\[45\]](#page-115-11). However, this conversion led to the loss of inverter [GFM](#page-1-2) capabilities, making it impractical. Similarly, a method discussed in [\[46\]](#page-116-0) altered the Droop characteristic based on current values. Reference [\[47\]](#page-116-1) combined external power command control according to [G-Cs](#page-1-4) with internal current control to limit overcurrents, but this approach is more complex compared to counterparts. References [\[48\]](#page-116-2) and [\[49\]](#page-116-3) applied and simulated three different [GFM](#page-1-2) control methods for [WTs,](#page-2-3) focusing only on symmetric faults. Reference [\[50\]](#page-116-4) compared different current limitation approaches only for three-phase symmetric faults. Reference [\[51\]](#page-116-5) proposed an auxiliary voltage control based on German and Danish [G-Cs](#page-1-4), simulated only for certain percentage reductions in voltage values, but emphasized that the proposed method could be applied in different control methods. In [\[52\]](#page-116-6), the proposed fault detection algorithm method successfully simulated both symmetric and asymmetric faults using [VSG-](#page-2-1)controlled [GFM](#page-1-2) systems based on the British [G-C,](#page-1-4) using [HIL](#page-1-16) simulation. Reference [\[53\]](#page-116-7) improved [FRT](#page-1-3) capacity using a voltage prioritization method, while reference [\[54\]](#page-116-8) performed current limitations by controlling active and reactive power without examining behaviors during fault conditions. Reference [\[55\]](#page-116-9) examined the [FRT](#page-1-3) capacities of [IBRs](#page-1-9) in high-voltage DC transmission lines and proposed a gradual current-limiting technique.

To the best of our knowledge, while numerous studies like those mentioned exist in the literature, a comprehensive comparison of different [FRT](#page-1-3) approaches under both symmetric and asymmetric grid faults for the most commonly used control methods (Droop and [VSG\)](#page-2-1) and comprehensive interoperability investigation of these [GFMs](#page-1-2) has not been conducted in microgrids.

2.3 Research Questions

Based on the scientific background and developments in the literature mentioned above, the following questions will constitute the main lines of inquiry for this thesis.

• What are the behaviors of differently controlled [GFMs](#page-1-2) under different fault conditions in a microgrid system?

In this question, the aim is to compare the most common and mature control methods

in the literature, namely droop control and [VSG](#page-2-1) control, to determine the most suitable control choice under different conditions. The behaviors (such as stability during and after fault, quality of supplied active power, reactive power support and share) of these inverters under commonly occurring symmetric and asymmetric faults in microgrids will be investigated, and the behaviors of a system consisting of multiple [GFMs](#page-1-2) will be analyzed using these two control methods. In the literature review conducted, no comprehensive comparative study covering these two common [GFMs](#page-1-2) is found.

• How can the behavior of inverters be improved with different [FRT](#page-1-3) approaches?

The purpose of this question is to investigate the [FRT](#page-1-3) approaches that have yielded positive results in the literature and significantly enhanced the [FRT](#page-1-3) capabilities of [GFMs](#page-1-2). Based on the literature review, the current saturation approach and [VI](#page-2-0) approach are identified as the most promising candidates. These approaches will be applied to the inverters in the designed system, and the response of the methods mentioned above will be observed comparatively. It is aimed that during simulations, literature-based optimizations will be conducted to improve these behaviors.

• Are these control methods (droop or [VSG](#page-2-1) with mentioned [FRT](#page-1-3) approaches) appropriate designs for microgrids operating under both islanded[/G-C](#page-1-4) modes and do they comply with the Dutch [GC?](#page-1-11)

In this question, the aim is to investigate the transition from grid-connected mode to islanded mode and vice versa in a comparative manner and to examine whether the designed system of the studied [GFMs](#page-1-2) complies with the Dutch [GC.](#page-1-11)

• Can the same and different types of [GFMs](#page-1-2) be interoperated in the same microgrid? If so, is it a suitable choice for the Dutch [GC?](#page-1-11)

This research question aims to investigate the potential positive and negative interactions among multiple [GFMs](#page-1-2) operating under Droop control and [VSG](#page-2-1) control concurrently in a microgrid. Another area of research is determining which responses of [IBRs](#page-1-9) are more favorable according to the Dutch [GC](#page-1-11) when multiple same and different types of [GFMs](#page-1-2) are used.

Chapter 3 Methodology

3.1 Utilized Tools

In this section, the transformations to be used in simulations, signal modulation, and filter design will be discussed.

3.1.1 Transformations & Modulation

During the simulation, Clarke and Park transformations, as well as [Sinusoidal Pulse Width](#page-2-4) [Modulation \(SPWM\)](#page-2-4) techniques, will be used to reduce system complexity and effectively process signals. The process schematic is provided in Figure [3.1.](#page-21-4)

Figure 3.1: Transformations between frames and signal modulation [\[56\]](#page-116-10)

There are three different vector frames commonly used in electrical systems, and their utilization greatly facilitates the analysis and mitigates the complexities of AC circuits. These frames are the abc (natural) frame, the $\alpha-\beta$ frame, and the dq0 frame. Essentially, these transformations involve transitioning from the 3-phase AC system to initially a fixed 2-axis $\alpha - \beta$ frame and then to a dq frame with moving axes. This results in obtaining voltage or current values as a DC value indicated by the moving axes, which are then utilized in PI controllers. The Clarke transformation, as seen in Figure [3.1,](#page-21-4) is a mathematical technique commonly used in the analysis of complex electrical circuits, which transforms the 3-phase abc frame into the 2-phase $\alpha-\beta$ frame. In this transformation, the alpha axis is used to represent the total balanced variable parameters (voltage/current), while the beta axis represents imbalances. The Clarke transformation facilitates the understanding of imbalances in the system and thus aids in controlling the variables. On the other hand, the Park transformation is used to convert the calculated fixed-axis orthogonal frame into the moving-axis referenced orthogonal dq frame. It is worth noting that as it is not the main focus of this thesis, the mathematical explanations will not be addressed in this report.

After the control process, the obtained signals are transformed back into the abc frame and then sent to the inverter gates for controlling the inverter output. The [SPWM](#page-2-4) method is used for modulation in order to control the inverter output. Here, the comparison between the triangular carrier wave and the sinusoidal reference signal is performed to generate a sinusoidal wave at the output. When the value of the reference wave is greater than the value of the carrier wave, predefined diagonal switches in the inverter are on, otherwise, they are off and the other couple of switches are on as can be seen from Figure [3.2.](#page-22-2) This control technique enables the regulation of the output voltage period, harmonic control, and linear control of the output voltage. The output signal frequency depends on the reference frequency, and by changing the modulation index $(m_a = V_{ref}/V_c)$, the amplitude of the output signal can be adjusted. Harmonics occur at frequency points where the frequency modulation index $(m_f = f_c/f_{ref})$ is multiplied by the fundamental frequency (for example, if f_c is 15 times greater than f_{ref} , the 15th harmonic is prominent. Assuming the fundamental frequency is 50 Hz, then 50*15=750 Hz). Also preferably, instead of bipolar [SPWM,](#page-2-4) unipolar [SPWM](#page-2-4) is utilized since its first harmonic appearance will happen at $2m_f$. It means less harmonic distortion at the output [\[57\]](#page-117-0).

Figure 3.2: [SPWM](#page-2-4) Types

3.1.2 Output Filter

For compliance with international standards (IEEE 519), particular attention must be paid to the design parameters of the filters used in inverter outputs, such as their dimensions, harmonic distortion attenuation capabilities, voltage drop levels, etc. Figure [3.3](#page-22-3) illustrates three commonly found types of harmonic filter designs prevalent today [\[9\]](#page-112-9).

Figure 3.3: Harmonic Filter Configurations [\[9\]](#page-112-9)

The first model, which consists of only one inductor and represents a first-order filter, is not preferred in [GFMs](#page-1-2) due to its weak harmonic elimination and bulky structure, which increases losses. The second model, the second-order LC filter, is effective in eliminating harmonics. To minimize losses and achieve the expected performance from the inverter, in other words, to mimic an ideal source, the output impedance should be minimized as much as possible under all load conditions (linear/nonlinear). For this purpose, the inductance adjusted according to the cut-off frequency should be kept as small as possible, and the capacitance value should be kept as large as possible. However, the selected values should be kept at the most optimal point because selecting a very large capacitance value will increase the reactive current amount and, consequently, the power level required in the inverter. Below are the equations showing the calculations for the parameters of the LC filter [\[9\]](#page-112-9), [\[58\]](#page-117-1).

$$
L1 = \frac{V_{DC}}{6 \cdot f_{sw} \cdot \Delta \cdot I_{Lmax}}\tag{3.1}
$$

$$
C = K \frac{S_n}{2 \cdot \pi \cdot f_g \cdot V_f^2}
$$
\n(3.2)

where the V_{DC} is DC link voltage, ΔI_{Lmax} filter inductor current max ripple and they are calculated respectively as √

$$
V_{DC} = \frac{2 \cdot E_g \cdot \sqrt{2}}{M \cdot \sqrt{3}}\tag{3.3}
$$

and,

$$
\Delta I_{L_{max}} = \% 10 \cdot I_{max} \tag{3.4}
$$

 f_{sw} is the inverter switching frequency while the f_g and V_f are the PCC frequency and the inverter output voltage, respectively, S_n is the inverter rated apparent power, E_g is the [PCC](#page-1-13) phase-phase RMS voltage, M is the modulation index (it is taken as 0.85 in this thesis [\[59\]](#page-117-2)), I_{max} is the maximum inverter output current capacity and K is the chosen proportion (in [\[58\]](#page-117-1) K value is chosen %5 of the inverted rated power for example). In addition, the third-order LCL filter provided in the last column in Figure [3.3](#page-22-3) performs better against harmonics due to the minimization of the inductance value, but its disadvantage is the increased interaction (resonance) with the grid. In [\[9\]](#page-112-9), it is stated that the design of this filter should be determined according to many parameters such as grid voltage/frequency, switching frequency, DC link voltage, power rating, etc. The value of L1 in the LCL filter is the same as the equation used in the LC filter. However, the values of C and $L2$ are calculated as follows [\[60\]](#page-117-3):

$$
C = 0.05 \frac{S_n}{2 \cdot \pi \cdot f_g \cdot E_n^2} \tag{3.5}
$$

$$
L_2 = \frac{\sqrt{\frac{1}{K_a^2}} + 1}{(2 \cdot \pi \cdot f_g \cdot E_n)^2 \cdot C}
$$
 (3.6)

where K_a (taken as 0.2 in this thesis [\[59\]](#page-117-2)) is the aimed attenuation of harmonics and E_n is the inverter output line-to-line voltage. Also for oscillation damping at the output, it is well known to place a resistor in series with the capacitor, and the resistance value is calculated as follows:

$$
R_f = \frac{1}{3 \cdot w_{res} \cdot C} \tag{3.7}
$$

where w_{res} is

$$
w_{res} = \sqrt{\frac{L1 + L2}{L1 \cdot L2 \cdot C}} \tag{3.8}
$$

Consequently, in this thesis, LCL filter configuration with a damping resistor will be utilized during the simulations since they are more robust against fault conditions.

3.2 Types of Faults

In [\[61\]](#page-117-4), it is stated that the most probable fault to happen in a grid is the single-phase-toground fault, with an occurrence probability of approximately 70%. Following this, the second most common fault occurs with a percentage of around 15%, which is the phaseto-phase fault. Subsequently, the two-phase-to-ground fault follows with a probability of approximately 10%, and finally, the three-phase faults occur with a probability of 5%.

3.2.1 Symmetric fault

Three-phase faults are referred to as symmetric faults because phase currents and voltages are balanced. It is the most severe fault and consists only of positive sequence components. The fault diagram is provided in Figure [3.4.](#page-24-4)

Figure 3.4: $3-\phi$ Fault

3.2.2 Asymmetric Faults

Asymmetric faults can be divided into three types: single-phase-to-ground fault, twophase-to-ground fault, and phase-to-phase fault. Although the severity of these faults is lower compared to symmetric faults, their control mechanisms are more complex because they involve both positive, negative, and zero sequence (ground-connected) components. If these components are not properly eliminated, they can cause instabilities in voltage and current values. Therefore, appropriate protection and [FRT](#page-1-3) methods must be implemented. Visuals of faults are illustrated in Figure [3.5.](#page-24-5)

(a) Line-to-Line Fault (b) Line-to-Ground Fault (c) 2-Line-to-Ground Fault

Figure 3.5: Asymmetric Faults

3.3 Dutch Grid Code

Recent news reports indicate that the Dutch grid is experiencing insufficient capacity in electricity transmission due to the addition of numerous [IBRs](#page-1-9) [\[62\]](#page-117-5). Consequently, in the Netherlands, the shift towards microgrids is not just a preference but a necessity. It is of paramount importance that one of the key components of microgrids, [IBRs,](#page-1-9) comply with the Dutch [GC](#page-1-11) and fulfill the requirements in the event of a fault. Therefore, in recent years, the Netherlands has already modified its [GC](#page-1-11) to enable more [IBRs](#page-1-9) installations and reduce congestion in the grid [\[62\]](#page-117-5).

According to the latest regulation in the Dutch [GC,](#page-1-11) electric generation units are classified based on their capacities. For a source connected to the low-voltage grid with a maximum capacity below 11 kW, protection with a response time of 2 seconds within the range of 47.5 Hz to 51.5 Hz at 80% and 110% of the nominal voltage is required (Article 3.8). For sources with capacities exceeding 11 kW, in addition to the above, there should be protection at 15% of the voltage with a response time of 0.2 seconds (Article 3.14). If this time interval is exceeded, disconnection from the grid may occur. However, [IBRs](#page-1-9) must have the ability to resume service immediately (when the capacity $\langle 11 \text{ kW} \rangle$ after the disturbance (Article 3.11). For capacities exceeding 11 kW, this time should not exceed a few minutes(Article 3.14). These sources must be capable of operating continuously within the range of 49-51 Hz and intermittently within the ranges of 47.5-48.5 Hz, 48.5-49 Hz, and 51-51.5 Hz for 30 minutes each. [IBRs](#page-1-9) must automatically connect to the grid at 0.9 p.u and 1.1 p.u nominal voltages within the range of 49.9 Hz and 50.1 Hz (Article 3.13) [\[63\]](#page-117-6).

The limits set to remain connected to the grid and meet the requirements for sources at medium voltage levels and voltage levels below 110 kV are given in Figure [3.6a\(](#page-25-2)Article 3.15).In addition, the power park module must be capable of providing and absorbing reactive power. Lastly, in Figure [3.6b,](#page-25-2) voltage sags limitations are illustrated.

Figure 3.6: Low/Medium Voltage Dutch Grid Code Requirements

Chapter 4 Modelling

In this section, the modeling of controls to be used in the simulation phase will be presented. The discussed models will be demonstrated through an inverter and a filter. Figure [4.1](#page-26-3) gives the topology of the inverter and the filter.

Figure 4.1: Inverter and Filter Topology

It is worth noting that, due to the research scope of this thesis, the [PVs](#page-1-7) (or [WTs](#page-2-3) or [BESSs\)](#page-1-8) is considered solely as a DC source for the sake of simplicity and simulation speed, disregarding its dynamics. Hence, the addition of an extra buck-boost converter to the model is avoided. However, future studies incorporating the dynamics of the power source (irradiation, wind speed, SoC, etc.) will render the results even more realistic. Furthermore, a 2-level 3-phase inverter is employed for DC-AC conversion. As mentioned in the preceding section, the dynamics of the inverter have not been examined in this thesis. As depicted in Figure [4.1,](#page-26-3) the inverter is connected to the microgrid via an LCL filter. The small resistance values originating from the natural structure of the filter inductors are also illustrated separately. The filter parameters are computed based on the equations provided between [\(3.1\)](#page-23-1) and [\(3.8\)](#page-24-6), and their values are presented in the next section.

4.1 LCL Filter Modelling

In order to better observe the dynamic behavior of the LCL filter, an equivalent circuit diagram is drawn to obtain its transfer function. The values of the parameters used in the filter circuit in this thesis are provided in Table [4.1.](#page-28-1) Figure [4.2](#page-27-0) illustrates the equivalent circuit of the filter circuit.

Figure 4.2: LCL Filter Equivalent Circuit

Taking the grid voltage $V_{grid} = 0$ at 50 Hz, the transfer function of the filter will become as I_{out}/V_{inv} . By applying Kirchoff's law, the following equations can be extracted in s domain from Figure [4.2;](#page-27-0)

$$
I_{inv} = I_c + I_{out} \tag{4.1}
$$

$$
V_{out} = I_c \cdot \left(\frac{1}{sC_f} + R_f\right) \tag{4.2}
$$

and considering again $V_{grid} = 0$,

$$
V_{out} = I_{out} \cdot (sL_2 + R_2) \tag{4.3}
$$

From (4.2) and (4.3) ,

$$
I_c \cdot (\frac{1}{sC_f} + R_f) = I_{out} \cdot (sL_2 + R_2)
$$
\n(4.4)

and,

$$
I_c = I_{out} \cdot (\frac{s^2 C_f L_2 + s C_f R_2}{s C_f R_f + 1})
$$
\n(4.5)

[\(4.1\)](#page-27-3) and [\(4.5\)](#page-27-4) yields,

$$
I_{inv} = I_{out} + I_{out} \cdot (\frac{s^2 C_f L_2 + s C_f R_2}{s C_f R_f + 1})
$$
\n(4.6)

Also, from Figure [4.2,](#page-27-0)

$$
V_{inv} = V_{out} + I_{inv} \cdot (sL_1 + R_1)
$$
\n(4.7)

Then, [\(4.3\)](#page-27-2), [\(4.6\)](#page-27-5) and [\(4.7\)](#page-27-6) yield,

$$
V_{inv} = I_{out} \cdot (sL_2 + R_2) + (sL_1 + R_1) \cdot (I_{out} + I_{out} \cdot (\frac{s^2 C_f L_2 + sC_f R_2}{sC_f R_f + 1})) \tag{4.8}
$$

By rearranging [\(4.8\)](#page-27-7),

$$
V_{\text{inv}} = I_{\text{out}} \cdot \frac{s^3 L_1 L_2 C_f + s^2 C_f (L_2 R_f + L_1 R_f + L_1 R_2 + L_1 R_1) + s(L_2 + L_1 + C_f R_f R_2 + C_f R_f R_1 + C_f R_1 R_2) + R_1 + R_2}{sC_f R_f + 1}
$$
\n
$$
(4.9)
$$

From [\(4.9\)](#page-27-8), the transfer function of the designed filter is,

$$
\frac{I_{out}}{V_{inv}} = \frac{sC_fR_f + 1}{s^3L_1L_2C_f + s^2C_f(L_2R_f + L_1R_f + L_1R_2 + L_1R_1) + s(L_2 + L_1 + C_fR_fR_2 + C_fR_fR_1 + C_fR_1R_2) + R_1 + R_2}
$$
\n(4.10)

Lastly, to be able to compare the effects of damping resistor R_f , also the transfer function without R_f is obtained as follows,

$$
\frac{I_{out}}{V_{inv}} = \frac{1}{s^3 L_1 L_2 C_f + s^2 C_f (L_1 R_2 + L_1 R_1) + s(L_2 + L_1 + C_f R_1 R_2) + R_1 + R_2}
$$
(4.11)

| Parameter | Value | Value [p.u] |
|---|----------------------|-------------|
| Inverter Apparent Power Capacity (S_n) | 10 kVA | |
| Operating Frequency (f_{nom}) | 50 Hz | |
| Phase-Phase Voltage RMS value (V_{pp}) | 400 V | 1 |
| DC Bus Voltage (V_{DC}) | 780 V | |
| L_1 | 12.5 mH | 0.24 |
| R_1 | $24 \text{ m}\Omega$ | 0.0015 |
| L_2 | 679.06 μ H | 0.013 |
| R_2 | $24 \text{ m}\Omega$ | 0.0015 |
| C_f | 9.652 μ F | 0.045 |
| R_f | 2.82Ω | 0.1762 |

Table 4.1: Parameter Values for LCL Filter

Bode diagrams are plotted based on the values of the parameters provided in Table [4.1](#page-28-1) and the derived transfer functions in [\(4.10\)](#page-27-9) and [\(4.11\)](#page-28-2).

Figure 4.3: LCL filter Damping Resistor Comparison

As evident from Figure [4.3,](#page-28-3) the application of the damping resistor has effectively eliminated the spike at the resonance frequency, allowing the filter to operate without distortion at its resonance frequency. Additionally, it has shifted the phase angle at high frequencies from -270 degrees to -180 degrees. This indicates that the filter has achieved a sufficient reduction of approximately -60 dB and a phase of -180 degrees at high frequencies which can be considered as high performance. Therefore, in this thesis, [IBRs](#page-1-9) will utilize this filter and its parameters. However, it is worth noting that the filter values will vary

depending on the total capacity of the source. For instance, for double the capacity (20 kVA), the inductor and resistor values will halve, and the capacitor values will double.

4.2 [GFM](#page-1-2) Control Modelling

In this section, the whole [GFM](#page-1-2) control stages are given. The modeling of the inner control loop, primary control loop, and secondary control loop will be explained in detail sequentially. In Figure [4.4,](#page-29-3) the complete control scheme of a [GFM](#page-1-2) is shown.

Figure 4.4: Primary and Inner Control Loops Block Diagram

4.2.1 Inner Control Loops Modelling

For inner control loops cascaded voltage and current control loops are utilized.[\[64\]](#page-117-7) Some advantages of this cascaded topology are rejecting or lowering the effect of disturbances, supplying clear references for the inverter to get the desired value at the output, and protecting controllers from saturating. In this topology, the current loop is ideally 10 times faster than the voltage control loop and 50 times slower than the switching frequency of the inverter. Moreover, as mentioned in the previous chapter, the dq0 components of the output values are extracted since simplicity and PI controllers can work with zero steady-state error with DC components. The frequency and voltage values for the voltage loop are provided by the primary controllers. The primary controllers in this thesis are Droop and [VSG](#page-2-1) controllers, and their modeling will be explained in detail in subsequent sections. The circuit topology from where the dq components are extracted is given in Figure [4.5.](#page-30-0)

Figure 4.5: Illustration of abc to dq conversion

From Figure [4.5,](#page-30-0) by using Kirchhoff's Law, the system equations can be calculated as follows:

$$
\frac{di_{inA}}{dt} = -\frac{R_1}{L_1}i_{inA} + \frac{1}{L_1}(V_{Ain} - V_{Aout})
$$
\n
$$
\frac{di_{inB}}{dt} = -\frac{R_1}{L_1}i_{inB} + \frac{1}{L_1}(V_{Bin} - V_{Bout})
$$
\n
$$
\frac{di_{inc}}{dt} = -\frac{R_1}{L_1}i_{inc} + \frac{1}{L_1}(V_{Cin} - V_{Cout})
$$
\n(4.12)

And written in a matrix form:

$$
\frac{d}{dt} \begin{bmatrix} i_{inA} \\ i_{inB} \\ i_{inc} \end{bmatrix} = -\frac{R_1}{L_1} \begin{bmatrix} i_{inA} \\ i_{inB} \\ i_{inc} \end{bmatrix} + \frac{1}{L_1} \begin{bmatrix} (V_{Ain} - V_{Aout}) \\ (V_{Bin} - V_{Bout}) \\ (V_{Cin} - V_{Cout}) \end{bmatrix}
$$
(4.13)

After applying the Park Transformation to [\(4.13\)](#page-30-1), following expression is obtained:

$$
\begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = -\frac{R_1}{L_1} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \frac{1}{L_1} \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix}
$$
(4.14)

After rearranging the equation:

$$
\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{-R_1}{L_1} & \omega \\ -\omega & \frac{-R_1}{L_1} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_1} \begin{bmatrix} V_d \\ V_q \end{bmatrix}
$$
\n(4.15)

Finally, considering that the $V_{dq} = V_{indq} - V_{outdq}$:

$$
V_{ind} = L_1 \frac{di_d}{dt} + R_1 i_d + V_{outd} - \omega L_1 i_q = L_1 s i_d + R_1 i_d + V_{outd} - \omega L_1 i_q
$$

\n
$$
V_{inq} = L_1 \frac{di_q}{dt} + R_1 i_q + V_{outq} + \omega L_1 i_d = L_1 s i_q + R_1 i_q + V_{outq} + \omega L_1 i_d
$$
\n(4.16)

As can be seen from [\(4.16\)](#page-30-2), the d and q axes are coupled $(i_q$ parameter in the first equation and i_d parameter in the second equation). In the control part, they must be decoupled by subtracting/adding the same parameters. As the extracting process of other system equations given from (4.17) to (4.19) is similar to the process described in $(4.12)-(4.16)$ $(4.12)-(4.16)$ $(4.12)-(4.16)$, they are not illustrated again in the report for the sake of simplicity. The detailed system transfer functions are provided below.

$$
V_{outd} = R_2 i_{od} + L_2 s i_{od} + V_{PCC} - \omega L_2 i_{og}
$$

\n
$$
V_{outq} = R_2 i_{og} + L_2 s i_{og} + V_{PCC} + \omega L_2 i_{od}
$$
\n(4.17)

At the same time:

$$
V_{outd} = i_{cd} \frac{1}{sC_f} + i_{cd} R_f
$$

$$
i_{cd} = (sC_f + \frac{1}{R_f})V_{outd} - \omega C_f V_{outq}
$$

$$
V_{outq} = i_{cq} \frac{1}{sC_f} + i_{cq} R_f
$$

$$
i_{cq} = (sC_f + \frac{1}{R_f})V_{outq} + \omega C_f V_{outd}
$$
 (4.18)

Lastly:

$$
i_{ind} = sC_f V_{outd} + \frac{V_{outd}}{R_f} - \omega C_f V_{outq} + i_{od}
$$

\n
$$
i_{inq} = sC_f V_{outq} + \frac{V_{outq}}{R_f} + \omega C_f V_{outd} + i_{og}
$$
\n(4.19)

4.2.1.1 Voltage Loop

The voltage loop consists of feedback/feedforward blocks and PI controllers. If the PI controller in the s domain is expressed as $k_{pv} + \frac{k_{iv}}{s}$ $\frac{S_{iv}}{s}$, which are proportional and integral gains of the controller, respectively, then, the voltage loop mathematical model can be extracted as:

$$
i_d* = (k_{pv} + \frac{k_{iv}}{s})(V_d * - V_{outd}) - \omega C_f V_{outq} + i_{od}H
$$

$$
i_q* = (k_{pv} + \frac{k_{iv}}{s})(V_q * - V_{outq}) + \omega C_f V_{outd} + i_{og}H
$$
 (4.20)

According to [4.20,](#page-31-4) the block diagram of the voltage loop is given in Figure [4.6.](#page-32-0) It is worth noting that while the **d** component of the reference value of the voltage controller is calculated from the primary control (either droop or [VSG](#page-2-1) control), the q component is set to zero("0"). It means that the voltage reference is aligned to the d-axis. In Figure [4.6,](#page-32-0) ωC_f is the decoupling term, and H is the I_{odd} feedback current gain.

By considering [\(4.18\)](#page-31-5), the d-axis transfer function can be expressed as follows, and the block diagram is illustrated in Figure [4.7](#page-32-1) [\[64\]](#page-117-7):

$$
\frac{V_{outd}(s)}{i_d(s) - i_{od}(s)} = \frac{1}{sC_f} + R_f
$$
\n(4.21)

Then the voltage loop closed loop transfer function becomes:

Figure 4.6: Voltage Controller Loop Block Diagram

$$
\frac{PI(\frac{1}{sC_f} + R_f)}{1 + PI(\frac{1}{sC_f} + R_f)} = \frac{(k_{pv} + \frac{k_{iv}}{s})(\frac{1}{sC_f} + R_f)}{1 + (k_{pv} + \frac{k_{iv}}{s})(\frac{1}{sC_f} + R_f)}
$$
(4.22)

Hence:

$$
\frac{V_{outd}(s)}{V_d*(s)} = \frac{\left(\frac{k_{pv}}{C_{fs}} + R_f k_{pv} + \frac{k_{iv}}{s^2 C_f} + \frac{k_{iv} R_f}{s}\right)}{1 + \left(\frac{k_{pv}}{C_{fs}} + R_f k_{pv} + \frac{k_{iv}}{s^2 C_f} + \frac{k_{iv} R_f}{s}\right)}
$$
(4.23)

By simplifying [\(4.23\)](#page-32-2):

$$
\frac{V_{outd}(s)}{V_d*(s)} = \frac{C_f R_f k_{pv}}{C_f + C_f R_f k_{pv}} \frac{s^2 + s(\frac{k_{pv} + k_{iv}R_f}{C_f R_f k_{pv}}) + \frac{k_{iv}}{C_f R_f k_{pv}}}{s^2 + s(\frac{k_{pv} + k_{iv}R_f}{C_f + C_f R_f k_{pv}}) + \frac{k_{iv}}{C_f + C_f R_f k_{pv}}}
$$
(4.24)

Figure 4.7: Voltage Control Closed Loop Block Diagram

As can be remembered from the well-known second-order system transfer function:

$$
\frac{w_n^2}{s^2 + 2\zeta w_n + w_n^2} \tag{4.25}
$$

And matching the denominators of [\(4.24\)](#page-32-3) and [\(4.25\)](#page-33-1), k_{pv} and k_{pi} values can be obtained:

$$
k_{pv} = \frac{2\zeta w_n C_f - w_n^2 C_f^2 R_f}{1 + w_n^2 C_f^2 R_f^2 - 2\zeta w_n C_f R_f}
$$
\n
$$
k_{iv} = w_n^2 (k_{pv} C_f R_f + C_f)
$$
\n(4.26)

The natural frequency w_n is ideally chosen as 500 times lower than the switching frequency and the ζ value is chosen by trial for the best response by using MATLAB. According to the results, when ζ value is 0.707 as proposed in [\[64\]](#page-117-7), the system response has overshoot and more delay to the steady-state compared to the case when ζ is 3. Therefore, ζ is taken as 3 in this thesis. A large value for ζ (> 1) indicates that the system is overdamped, implying a slower settling time. However, in the obtained results, the system response speed is found to be adequate.

4.2.1.2 Current Loop

The current loop also consists of feedback/feedforward blocks and PI controllers [\[64\]](#page-117-7). If the PI controller in the s domain is defined as $k_{pc} + \frac{k_{ic}}{s}$ $\frac{\partial \hat{z}_c}{\partial s}$, the current loop mathematical model can be written as:

$$
e_d* = (k_{pc} + \frac{k_{ic}}{s})(i_d * - i_{ind}) - \omega L_1 i_{inq} + V_{outd}
$$

\n
$$
e_q* = (k_{pc} + \frac{k_{ic}}{s})(i_q * - i_{inq}) + \omega L_1 i_{ind} + V_{outq}
$$
\n(4.27)

The block diagram is depicted in Figure [4.8](#page-33-2) according to [\(4.27\)](#page-33-3).

Figure 4.8: Current Controller Loop Block Diagram

Based on [\(4.16\)](#page-30-2), the transfer function in d-axis can be obtained as follows [\[64\]](#page-117-7):

$$
\frac{i_d(s)}{V_{ind}(s) - V_{outd}(s)} = \frac{\frac{1}{L_1}}{s + \frac{R_1}{L_1}}
$$
(4.28)

Hence, the current loop transfer function block diagram is shown in Figure [4.9.](#page-34-0)

Figure 4.9: Current Control Closed Loop Block Diagram

From Figure [4.9,](#page-34-0) we can calculate the closed loop transfer function of the system as follows:

$$
\frac{PI(\frac{1}{s_1})}{1 + PI(\frac{1}{s + \frac{R_1}{L_1}})} = \frac{(k_{pc} + \frac{k_{ic}}{s})(\frac{1}{s + \frac{R_1}{L_1}})}{1 + (k_{pc} + \frac{k_{ic}}{s})(\frac{1}{s + \frac{R_1}{L_1}})}\tag{4.29}
$$

Therefore:

$$
\frac{i_d(s)}{i_d*(s)} = \frac{\frac{k_{pc}}{L_1} \frac{s + \frac{k_{ic}}{k_{pc}}}{s^2 + s \frac{R_1}{L_1}}}{1 + \frac{k_{pc}}{L_1} \frac{s + \frac{k_{ic}}{k_{pc}}}{s^2 + s \frac{R_1}{L_1}}}
$$
(4.30)

And by rearranging [\(4.30\)](#page-34-1):

$$
\frac{i_d(s)}{i_d*(s)} = \frac{\frac{k_{pc}}{L_1}(s + \frac{k_{ic}}{k_{pc}})}{s^2 + s\frac{R_1}{L_1} + \frac{k_{pc}}{L_1}(s + \frac{k_{ic}}{k_{pc}})}
$$
(4.31)

Finally, following equation is extracted:

$$
\frac{i_d(s)}{i_d*(s)} = \frac{k_{pc}}{L_1} \frac{(s + \frac{k_{ic}}{k_{pc}})}{s^2 + s \frac{R_1 + k_{pc}}{L_1} + \frac{k_{ic}}{L_1}}
$$
(4.32)

Again, if the denominators of (4.32) and (4.25) are matched, k_{pc} and k_{ic} values can be obtained. However, in the current loop case, the natural frequency ω_{ni} is ideally 1/50 of the switching frequency. Moreover, after observing the effects of ζ on the step response,

it is chosen as 3 for the current control loop as well instead of 0.707 as proposed in [\[64\]](#page-117-7). Therefore, the PI controller gains are as follows,

$$
k_{pc} = 2\zeta\omega_{ni}L_1 - R_1
$$

\n
$$
k_{ic} = \omega_{ni}^2 L_1
$$
\n(4.33)

Once the equations for the gains of the PI controller are derived, it can be proceed to calculate their values. However, it is worth noting that the calculated values are obtained using the real values of the circuit components. Nevertheless, all parameters used in the simulation are provided per unit (p.u.). Therefore, to ensure the p.u. compensation of the obtained values, the gain values for the voltage control loop should be multiplied by the base impedance (16 Ω in this thesis according to filter parameters), and the gain values for the current control loop should be divided by the base impedance. After these calculations, the resulting values for a [GFM](#page-1-2) with a capacity of 10 kVA are summarized in Table [4.2.](#page-35-1) After calculating the parameters, the whole inner control loop can be

| Parameter | Value |
|--|--------------------------|
| Inverter Apparent Power Capacity (S_n) | 10 kVA |
| Switching Frequency (f_{sw}) | 10 kHz |
| ω_{nv} | 125.66 rad/sec |
| ω_{nc} | 1256.6 rad/sec |
| k_{pv} | 0.22451 |
| k_{iv} | 36.978 |
| k_{pc} | 4.9084 |
| k_{ic} | 616.85 |

Table 4.2: Control Parameter Values for Inner Control

connected. The schematic of the completed inner control is illustrated in Figure [4.10.](#page-35-2)

Figure 4.10: Inner Control Completed Schematic

The output of the current loop is used as the gating signal of the inverter. First, the reference frame is shifted from dq0 to abc natural frame. For this conversion, the calculated frequency ω_t from the primary control is utilized. Additionally, for the compensation of the delay in the system, a sample time compensation term $(\omega_{nominal} * f_{sample})$ is added into ω_t . After turning the p.u. value of the gating signal to the real value by
multiplying with the base parameter, it is divided into half of the DC link voltage since the DC link voltage is divided into two by grounding in the middle. The [SPWM](#page-2-0) gating signal generation is shown in Figure [4.11.](#page-36-0)

Figure 4.11: [SPWM](#page-2-0) Signal Generation

4.2.2 Primary Control Modelling

4.2.2.1 Droop Control

The Droop control method, which emerged in the 1980s, is initially used in the control of UPS. Later on, it began to be applied in [SGs](#page-2-1) to enhance the stability of existing power grids. Implemented as a primary control, droop control is adopted for the parallel operation of many energy sources connected to the grid in microgrids. Today, the most widespread and mature inverter control method, droop control, can be divided into two segments: frequency droop control and voltage droop control, in traditional AC grids [\[65\]](#page-117-0).

Frequency droop control is associated with active power and is briefly expressed as P-f droop. In P-f droop, the changing frequency values are inversely proportional to the active power, similar to traditional [SGs.](#page-2-1) Voltage droop control, on the other hand, is related to reactive power and is briefly expressed as Q-V droop. Similar to P-f droop, there is a similar relationship based on Q values, and voltage values change inversely proportional to the reactive power.

In [SGs,](#page-2-1) these characteristics are naturally present due to the kinetic energy stored in their rotors. Only additional droop controllers are used to improve performance. However, in [IBRs,](#page-1-0) since there is no such stored inertia source, such control is essential. Otherwise, they will produce constant power regardless of grid dynamics. Furthermore, in DC grids, there is no issue of synchronizing with frequency, so the only concern is the magnitude of voltage. However, since DC grids are beyond the scope of this thesis, they will not be discussed further. As mentioned in the previous section, in droop control, there is no need for direct communication among [IBRs](#page-1-0) because they operate effectively using calculations obtained from the grid. Additionally, this control algorithm adjusts the power allocation based on the capacities of [IBRs,](#page-1-0) ensuring the safe parallel operation of [IBRs](#page-1-0) and other energy sources. However, the nature of [IBRs](#page-1-0) being affected by environmental conditions has made the implementation of [BESSs](#page-1-1) essential for microgrids. When [IBRs](#page-1-0) cannot provide the required amount of power, a [BESSs](#page-1-1) can step in and fill this gap. The power sharing in a microgrid is crucial for maintaining system stability, and when this balance is disrupted, the power drawn from certain sources is reduced. This may lead to inefficient operation of the microgrid components.

When considering an inverter connected to the [PCC](#page-1-2) via a filter, as shown in Figure [4.1,](#page-26-0) and for simplicity in analysis, ignoring the filter capacitance and resistance values, the new equivalent circuit diagram is presented in Figure [4.12](#page-37-0) [\[66\]](#page-117-1).

Figure 4.12: Simplified Equivalent Circuit

In the figure, V_q , V_{inv} , Z_L , P_{inv} and Q_{inv} are grid side voltage, inverter side voltage, the total equivalent impedance between the inverter and the grid, injected active and reactive power to the [PCC](#page-1-2) by inverter, respectively. Supplied powers can be expressed as follows:

$$
P_{inv} = \left(\frac{V_g V_{inv}}{Z_L} \cos \delta - \frac{V_g^2}{Z_L}\right) \cos \theta + \frac{V_g V_{inv}}{Z_L} \sin \delta \sin \theta
$$

$$
Q_{inv} = \left(\frac{V_g V_{inv}}{Z_L} \cos \delta - \frac{V_g^2}{Z_L}\right) \sin \theta - \frac{V_g V_{inv}}{Z_L} \sin \delta \cos \theta
$$
 (4.34)

If the impedance is inductive, meaning the inductance value is much greater than the resistance (as in our case, where $R = 0.024 \Omega$ and $X_L = 3.9 \Omega$), this impedance can be considered as purely inductive $(\theta = 90^{\circ})$. In this scenario, the total impedance value from Figure [4.1](#page-26-0) would be $\omega_n \cdot (L_1 + L_2)$. Therefore, by rewriting [\(4.34\)](#page-37-1), it can be obtained:

$$
P_{inv} = \frac{V_g V_{inv}}{Z_L} \sin \delta
$$

$$
Q_{inv} = \frac{V_g V_{inv} \cos \delta - V_g^2}{Z_L}
$$
 (4.35)

If δ is small (as it should be in normal operation mode), it can be approximated that $\sin(\delta) \approx \delta$ and $\cos(\delta) \approx 1$. Thus, [\(4.35\)](#page-37-2) can be written as:

$$
P_{inv} \approx \frac{V_g V_{inv}}{Z_L} \delta
$$
\n
$$
Q_{inv} \approx \frac{V_g}{Z_L} (V_{inv} - V_g)
$$
\n(4.36)

From [\(4.36\)](#page-37-3), it can be commented that the active power P_{inv} depends on the angle δ and as the δ increases P_{inv} decreases or vice versa. On the other hand, the same situation is also valid for the reactive power Q_{inv} and output power V_{inv} . As V_{inv} rises, Q_{inv} drops and vice versa. This relationship is illustrated in Figure [4.13.](#page-38-0)

Figure 4.13: P-f and Q-V Droop Control [\[65\]](#page-117-0)

Hence the P-f and Q-V droop control can be utilized. So, the droop control can be described as follows:

$$
f = f_{ref} - k_P(P_{ref} - P_{inv})
$$

$$
V_{inv} = V_{invref} - k_Q(Q_{ref} - Q_{inv})
$$
\n(4.37)

where P_{ref} and Q_{ref} are reference powers, f_{ref} and V_{inver} are the reference frequency and reference RMS output voltage, P_{inv} and Q_{inv} are measured active and reactive power from the inverter output, k_P and k_Q are droop coefficients (for example if it is set $k_P = 0.01$, it means that the frequency will deviate $\%1$ for the deviation 1 p.u in the active power) and f and V_{inv} are the reference values for the inner control loop. The block diagram of [\(4.37\)](#page-38-1) is depicted in Figure [4.14.](#page-38-2)

Figure 4.14: Droop Control Block Diagram

Moreover, it is important to examine the calculations of active and reactive power $(P_{\text{inv}}$ and $Q_{\text{inv}})$ in the primary control. Considering Figure [4.5,](#page-30-0) power calculations can be performed as follows [\[67\]](#page-117-2):

$$
P_{\text{inv}}* = \frac{3}{2}(V_{od}I_{ind} + V_{og}I_{inq})
$$

\n
$$
Q_{inv}* = \frac{3}{2}(V_{og}I_{ind} - V_{od}I_{inq})
$$
\n(4.38)

However, these calculated power values are not directly utilized but first applied a low-pass

filter. Therefore:

$$
P_{inv} = \frac{w_{cmeas}}{s + w_{cmeas}} P_{inv}*
$$

$$
Q_{inv} = \frac{w_{cmeas}}{s + w_{cmeas}} Q_{inv}*
$$
 (4.39)

The reason for using a low-pass filter here is to suppress harmonics and noise. The natural frequency of this low-pass filter is assumed to be around 10-20% of the nominal frequency [\[67\]](#page-117-2). The droop control parameter values are given in Table [4.3.](#page-39-0)

| Parameter | Value |
|-----------------------------------|----------------------|
| $P - f$ Droop Coefficient (K_P) | 1% |
| $Q-V$ Droop Coefficient (K_Q) | 4% |
| ω_{cmeas} | 63 rad/sec |
| P_{ref} (Islanded) | 1 p.u. |
| P_{ref} (Grid-connected) | 0.5 p.u. |
| Q_{ref} (Islanded) | 0 p.u. |
| Q_{ref} (Grid-connected) | 0 p.u. |
| V_{ref} | 1 p.u. |
| f_{ref} | 1 p.u. |

Table 4.3: Control Parameter Values for Droop Control

4.2.2.2 Virtual Synchronous Generator (VSG) Control

It is previously mentioned that there is an inertia issue in grids due to the lack of large rotating mechanical parts. Another promising control method with numerous studies in the literature is the [VSG](#page-2-2) control. [VSG](#page-2-2) is a control method in [IBRs](#page-1-0) that mimics the dynamic behavior of [SGs.](#page-2-1) The greatest advantage of [VSG](#page-2-2) is that dynamic parameter adjustments, which cannot be achieved with real physical counterparts, can be readily implemented as needed. For instance, parameters such as inertia moment, stator impedances, and damping coefficients, among others, can be easily adjusted. One of the main objectives of [VSG](#page-2-2) is to respond to frequency transients similar to [SGs.](#page-2-1) This way, system inertia and instability issues can be addressed. It's worth noting that to mimic inertia, it's necessary not only to supply power to the grid but also to absorb power from it [\[68\]](#page-117-3). In the case of [VSG](#page-2-2) control(by considering Figure [4.12\)](#page-37-0), the voltage value at the [PCC](#page-1-2) is represented as the back electromotive force. The impedance of the filter section corresponds to the stator winding impedance, while the inverter represents the electromechanical energy transfer between the stator and rotor. [IBRs](#page-1-0) represents the input torque of the prime mover [\[69\]](#page-117-4).

The [VSG](#page-2-2) can be applied in control both as a current source and as a voltage source. However, when applied as a current source, it will lack voltage and frequency support, in other words, it will operate as a [GFL.](#page-1-3) When used as a voltage source, it will provide these desired features and simply operate in [GFM.](#page-1-4) Therefore, in this thesis, only the voltage source [VSG](#page-2-2) control is addressed. Additionally, since the virtual inertia provided to the [IBRs](#page-1-0) in droop control is not sufficient, the [RoCoF](#page-1-5) may exceed the desired value. Virtual inertia with [VSG](#page-2-2) control is intended to be adequately provided. A comparison between these two control methods is discussed in the following chapter. Despite the advantages of [VSG](#page-2-2) control, such as particularly providing sufficient inertia in islanded modes, it also has disadvantages. In simple [VSG](#page-2-2) control, when high virtual inertia is applied, it causes slow settling times in [G-C](#page-1-6) modes and large overshoots in islanded modes. To correct these issues, if the inertia is reduced, it leads to a high [RoCoF](#page-1-5) rate. Moreover, the damping factor D may decrease the overshoot by increasing it but it also raises the [RoCoF](#page-1-5) [\[70\]](#page-118-0). Therefore, the values of the virtual inertia and damping factor should be chosen according to system requirements.

As shown in equations [\(4.34\)](#page-37-1)-[\(4.36\)](#page-37-3), the similar relationships between P-f and Q-V are also valid here. Besides, the [VSG](#page-2-2) control relies on the swing equations of [SGs.](#page-2-1) These equations can be summarized as follows [\[71\]](#page-118-1), [\[72\]](#page-118-2), [\[73\]](#page-118-3), [\[74\]](#page-118-4):

$$
J\frac{d\omega}{dt} = T_m - T_e - D(\omega - \omega_{ref})
$$
\n(4.40)

and

$$
\frac{d\theta}{dt} = \omega \tag{4.41}
$$

where ω and ω_{ref} are the angular frequency of the [GFM](#page-1-4) output and the nominal grid angular frequency, θ is the [GFM](#page-1-4) output angle, J is the virtual inertia and D is the damping factor of the [SGs,](#page-2-1) T_m and T_e are the mechanical output torque and electromagnetic torque. Besides, the electromagnetic torque can be expressed as [\[75\]](#page-118-5):

$$
T_e = \frac{u_a i_a + u_b i_b + u_c i_c}{\omega} = \frac{P_{inv}}{\omega}
$$
\n(4.42)

and

$$
T_m = k_p(\omega_{ref} - \omega) + \frac{P_{ref}}{\omega} \tag{4.43}
$$

where P_m and P_{inv} correspond to the mechanical power and output measured power of [SGs](#page-2-1) and k_p is the difference coefficient. Lastly, similarly to droop control, the reactive power equation can also be expressed as follows [\[76\]](#page-118-6):

$$
V = k_q(Q_{ref} - Q_{meas}) + V_{ref}
$$
\n
$$
(4.44)
$$

where k_q is the droop coefficient, Q_{ref} and Q_{meas} are the nominal and measured output power and v_{ref} is the nominal system voltage. Finally, by substituting [\(4.41\)](#page-40-0), [\(4.42\)](#page-40-1) and [\(4.43\)](#page-40-2) into [\(4.40\)](#page-40-3):

$$
J\frac{d\omega}{dt} = \frac{P_{ref}}{\omega} - \frac{P_{inv}}{\omega} + k_p(\omega_{ref} - \omega) + D(\omega - \omega_{ref})
$$
\n(4.45)

According to [\(4.45\)](#page-40-4), the block diagram of the [VSG](#page-2-2) control is shown in Figure [4.15](#page-41-0) and parameters are illustrated in Table [4.4.](#page-41-1) It is beneficial to mention that this control is used as the primary control and the parameter values are chosen according to system needs. As discussed earlier, inner and secondary controls are the same for droop and [VSG](#page-2-2) control.

Figure 4.15: [VSG](#page-2-2) Control Block Diagram

| Parameter | Value |
|---------------------------------------|------------|
| Difference Coefficient (k_f) | 50 |
| $Q-V$ Droop Coefficient (k_Q) | 4% |
| Damping Factor (D/ω_0) | 10 |
| Inertia time constant $(J\omega_0)$ | 0.25 |
| P_{ref} (Islanded) | 1 p.u. |
| P_{ref} (Grid-connected) | 0.3 p.u. |
| Q_{ref} (Islanded & Grid Connected) | 0 p.u. |
| V_{ref} | 1 p.u. |
| w_{ref} | 1 p.u. |

Table 4.4: Control Parameter Values for [VSG](#page-2-2) Control

4.2.3 Secondary Control Modelling

The implementation of secondary control systems for microgrids is critically important. Rapid re-adjustment of voltage and frequency following any disturbance is essential to ensure compliance with national [GCs](#page-1-7). Primary controllers may not be able to regulate voltage and frequency values to the desired extent if they experience severe faults and subsequently lose synchronization, potentially leading to undesirable situations. To prevent this, a secondary or microgrid controller is incorporated into the designed model. As secondary control, the transition between [G-C](#page-1-6) and islanded modes, and vice versa, involves the synchronization of the microgrid with the main grid. Additionally, it regulates oscillating voltage and frequency values, returning them to nominal levels during faults, load changes, or load-shedding events.

4.2.3.1 Voltage & Frequency Restoration

To ensure power quality and system stability, voltage and frequency must be optimally regulated and restored to their nominal values. Any deviations that occur following unexpected events can be corrected to the desired or expected values through secondary control. Additionally, secondary control utilizes the [PLL](#page-1-8) to obtain frequency information

at the microgrid bus. The applied control for frequency and voltage can be mathematically expressed as follows [\[77\]](#page-118-7):

$$
f_{ref}(s) = (k_{pf} + \frac{k_{if}}{s})(f_{nom} - (\frac{\omega_{csec}}{s + \omega_{csec}}f_{microgrid})
$$
\n(4.46)

$$
V_{ref}(s) = (k_{pV} + \frac{k_{iV}}{s})(V_{nom} - (\frac{\omega_{csec}}{s + \omega_{csec}} | V_{microgrid_{pp}}|)
$$
\n(4.47)

where f_{ref} and V_{ref} are the reference values for primary control, k_{pf} , k_{if} , k_{pV} , and k_{iV} are the PI controller gain values, f_{nom} and V_{nom} are the nominal frequency and voltage values of the grid, $\omega_{\rm csec}$ is the natural frequency of the secondary control [LPF,](#page-1-9) and $f_{\rm microgrid}$ and $V_{\text{microgrid}}$ are the frequency and voltage values obtained from the [PCC.](#page-1-2) It is beneficial to mention that the PI controller parameters are found by trial and error in secondary control. The values of the given parameters are summarized in Table [4.5.](#page-42-0)

| Parameter | Value |
|---------------------|-----------------------|
| $f_{\rm nom}$ | 50 Hz |
| V_{nom} | 400 V |
| k_{pf} | 0.03 |
| $\overline{k_{if}}$ | 2 |
| $\overline{k_{pV}}$ | 0.1 |
| $\overline{k_{iV}}$ | |
| ω_{csec} | 500 rad/sec |

Table 4.5: Control Parameter Values for Restoration Unit

Block diagrams of restoration controls are also illustrated in Figure [4.16.](#page-43-0) It should be noted that before applying the obtained reference values to the primary control, they are converted into their p.u. values. In order to see the effect of the restoration control on the microgrid parameters, system parameters are analyzed with and without restoration control. During these simulations, the droop control is used as the primary control and the microgrid is operating in islanded mode. However, the results are also the same for [VSG](#page-2-2) control and [G-C](#page-1-6) mode. Simply, when secondary control is not applied, the reference values for primary control are set to 1 p.u. The comparison of the frequency restoration control is illustrated in Figure [4.17.](#page-43-1) It is worth noting that since the effects of secondary control implementation on the behavior of [IBRs](#page-1-0) are not the scope of this thesis, these plots are depicted in this chapter.

The setup for this comparison is as follows: an initial load of 5 kW and 2 kVAr is connected to a [GFM](#page-1-4) with a capacity of 10 kVA. At seconds 1 and 4, a three-phase grid fault occurs, causing the grid voltage to drop to zero. At second 2, an additional 2 kW load is connected to the grid. As observed in Figure [4.17a,](#page-43-1) although the inverter output frequency remains relatively stable and quickly returns to its previous value after the grid fault, it is evident that the frequency stabilizes at 50.25 Hz rather than approaching exactly 50 Hz. Continuous operation at this frequency is undesirable for system health and compliance with [GCs](#page-1-7). Furthermore, after the additional load is connected, the frequency drops due to the droop control mechanism as the power demand increases, but it stabilizes at a lower value. This implies that the system will operate at different frequencies with any load change. This significantly impacts power quality and shortens the lifespan of electronic devices. In contrast, when restoration control is applied, it is observed in Figure

Figure 4.16: Voltage & Frequency Restoration Control Blocks

[4.17b](#page-43-1) that the inverter's frequency response quickly converges to 50 Hz and remains stable at exactly 50 Hz after each condition.

(b) With Restoration Control

Figure 4.17: Effects of Restoration Control

4.2.3.2 Synchronisation with the Utility Grid

As mentioned in the first chapter, [GFM](#page-1-4) has to work in either [G-C](#page-1-6) or islanded mode. Although the design of [GFMs](#page-1-4) makes them operate in both modes, transition moments are significant for the reliable and stable operation of the microgrid. The significance of these transitions stems from the lack of synchronization between the main grid and the microgrid during the transition phase. The voltage values on both sides have different frequency and phase angles. Especially during the transition from islanded to [G-C](#page-1-6) mode, the grid suddenly forces the microgrid voltage to follow its own. This abrupt change at the [PCC](#page-1-2) can cause enormous inrush currents in the [GFM](#page-1-4) filter capacitor. These currents are typically beyond what an inverter can handle and can result in the inverter being shut down or even permanently damaged.

To mitigate this issue, a synchronization section is added as part of the secondary control in this thesis to ensure proper synchronization. The applied synchronization algorithm can be mathematically expressed as follows [\[78\]](#page-118-8):

$$
V_{synch}(s) = (k_{pVsynch} + \frac{k_{iVsynch}}{s}) (V_{dgrid} \frac{w_{csyn}}{s + w_{csyn}} - V_{dPCC} \frac{w_{csyn}}{s + w_{csyn}})
$$
(4.48)

$$
f_{synch}(s) = (k_{pfsynch} + \frac{k_{ifsynch}}{s})(V_{qgrid}\frac{w_{csyn}}{s + w_{csyn}} - V_{qPCC}\frac{w_{csyn}}{s + w_{csyn}})
$$
(4.49)

Transitioning from the [G-C](#page-1-6) mode to the islanded mode does not pose any synchronization problems because the [GFM](#page-1-4) does not have to synchronize any other source; therefore, the synchronization algorithm is only activated during the transition from islanded mode to [G-C](#page-1-6) mode. The algorithm can be summarized as follows: a certain period of time is required from the receipt of the transition signal until the actual transition to the [G-C](#page-1-6) mode. In this thesis, as will be shown later, this period is applied as 2 seconds. During these 2 seconds, the switching signal is held in position to complete the synchronization. Simultaneously, according to the synchronization algorithm, when the falling or rising edge of the transition signal arrives (in this thesis, the falling edge), the algorithm becomes active, and the synchronization process begins. However, to prevent the process from continuing indefinitely after synchronization, the algorithm is reset after 2 seconds. The algorithm flow chart is depicted in Figure [4.18.](#page-45-0)

As seen from [\(4.48\)](#page-44-0) and [\(4.49\)](#page-44-1), the abc to dq0 transition is realized for both the utility grid and the microgrid with the help of [PLL.](#page-1-8) The difference between the d and q components of the grid voltage and microgrid voltage is calculated and subsequently, the error is minimized via a PI controller. The result in the d component is added to the voltage amplitude value, while the result in the q component is added to the frequency value of the primary controller. After 2 seconds, synchronization is fully achieved, and the system is ready for the transition. The synchronization block diagram is shown in Figure [4.19.](#page-45-1) Additionally, the values of the PI controllers are taken from reference [\[78\]](#page-118-8). The control parameter values are provided in Table [4.6.](#page-46-0)

4.3 [GFL](#page-1-3) Control Modelling

In this section, an inverter with a rated apparent power of 10 kVA and the same LCL filter values described in section 4.1 is considered. Since this power source is designed as a grid-following-grid-feeding system, it can be simply regarded as a current source

Figure 4.18: Synchronisation Algorithm Flow Chart

Figure 4.19: Resynchronisation Block Diagram

connected behind an impedance. Therefore, there is no voltage control loop and primary control loop. Additionally, similar to 99% of the [IBRs](#page-1-0) currently in the field, it uses a [PLL](#page-1-8) to obtain the phase angle information from the grid, which is used in the current

| Parameters | Values |
|---------------------------------------|--------------------------|
| Inverter Apparent Power Capacity (Sn) | $10\ \text{kVA}$ |
| Switching Frequency (f_{sw}) | 10 kHz |
| LPF Natural Frequency w_{csync} | 3141.6 rad/sec |
| k_{pVsync} | 0.0075 |
| k_{iVsync} | 0.015 |
| k_{pfsync} | 0.0075 |
| k_{ifsync} | 0.015 |

Table 4.6: Control Parameter Values for Synchronization Unit

control loop. The current control loop shares the same control topology as the block diagram given in the previous section (Figure [4.8\)](#page-33-0). The only difference is that the current references in the d/q components, which would come from the voltage control loop, are manually set in this case.

Since the inverter is operating in grid-feeding mode, constant and desired power outputs are targeted at the output. However, when the current references are directly set to 1 p.u. for the d component and 0 p.u. for the q component, the power outputs achieved at the output are not as expected, specifically 1 p.u. and 0 p.u. Random injections are observed, especially in the reactive power output. To prevent this situation, current references derived from the power values at the inverter's output are calculated and applied as references in the current loop. The implemented control is described below. First, [\(4.38\)](#page-38-3) can be rewritten as follows:

$$
\vec{S} = \begin{bmatrix} P_{inv} \\ Q_{inv} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} V_{od} & V_{og} \\ V_{og} & -V_{od} \end{bmatrix} \begin{bmatrix} I_{ind} \\ I_{inq} \end{bmatrix}
$$
(4.50)

To obtain the current values, we can find the inverse of the voltage matrix and use it to solve for the current values:

$$
\begin{bmatrix} P_{inv} \\ Q_{inv} \end{bmatrix} \frac{2}{3} V^{-1} = \begin{bmatrix} I_{ind} \\ I_{inq} \end{bmatrix}
$$
 (4.51)

By taking the inverse of the V matrix we get:

$$
V^{-1} = \frac{1}{-V_{od}^2 - V_{og}^2} \begin{bmatrix} -V_{od} & -V_{og} \\ -V_{og} & V_{od} \end{bmatrix} = \frac{1}{V_{od}^2 + V_{og}^2} \begin{bmatrix} V_{od} & V_{og} \\ V_{og} & -V_{od} \end{bmatrix}
$$
(4.52)

Hence,

$$
\frac{2}{3} \begin{bmatrix} P_{inv} \\ Q_{inv} \end{bmatrix} \frac{1}{V_{od}^2 + V_{og}^2} \begin{bmatrix} V_{od} & V_{og} \\ V_{og} & -V_{od} \end{bmatrix} = \begin{bmatrix} I_{ind} * \\ I_{inq} * \end{bmatrix}
$$
\n(4.53)

Then we can show the current values as follows:

$$
I_{ind}^* = \frac{2}{3} \frac{1}{V_{od}^2 + V_{og}^2} (P_{inv} V_{od} + Q_{inv} V_{og})
$$

\n
$$
I_{inq}^* = \frac{2}{3} \frac{1}{V_{od}^2 + V_{og}^2} (P_{inv} V_{og} - Q_{inv} V_{od})
$$
\n(4.54)

As a result, these obtained current reference values are applied to the current control loop. The completed block diagram of the [GFL](#page-1-3) control is shown in Figure [4.20.](#page-47-0) It is worth mentioning again that the d and q components of the voltage values are obtained using the grid angle value provided by the [PLL.](#page-1-8) Additionally, the [SPWM](#page-2-0) process following the

current control loop to generate the gating signals is the same as the block diagram given in Figure [4.11.](#page-36-0)

Figure 4.20: [GFL](#page-1-3) Control Complete Block Diagram

4.4 [Fault-Ride-Through \(FRT\)](#page-1-10) Controls Modelling

As previously discussed, the increasing number of [IBRs](#page-1-0) in power networks has made the health, reliability, and quality of the grid increasingly dependent on these devices. Although the current proportion of such resources remains relatively low, the rapid growth and expansion of renewable energy sources project that by around 2050, grids will predominantly be composed of [GFMs](#page-1-4) and [GFLs](#page-1-3). Consequently, it is crucial that the grid remains functional during common faults and disturbances, as described in Chapter 3. To achieve this, these devices must stay connected to the grid without sustaining damage and should even support grid voltage and frequency. To meet these requirements, [FRT](#page-1-10) methods are implemented to ensure that [GFMs](#page-1-4) and [GFLs](#page-1-3) operate healthily and effectively during faults, load changes, load shedding, etc. While [GFLs](#page-1-3), controlled as current sources, do not typically face overcurrent issues, the voltage source behavior of [GFMs](#page-1-4) renders them vulnerable to overcurrents. This chapter examines the [Current Magnitude Satura](#page-1-11)[tion \(CMS\)](#page-1-11) and [Virtual Impedance \(VI\)](#page-2-3) methods, which are among the most common and mature [FRT](#page-1-10) methods in the literature and employed in this thesis. Additionally, it discusses control strategies implemented to limit negative(or zero-)sequence components, which cause significant oscillations in current and voltage during asymmetric faults.

4.4.1 Current Saturators

The fundamental concept of current saturation is to clamp the output current of the inverter to its maximum allowable capacity when the demanded current exceeds this limit. Current saturation control is typically implemented in the inner loop (between the voltage and current controllers) to limit the current references generated by the voltage controller. In the literature, there are two common types of current limiters: current instantaneous limiters and current magnitude saturators. The first type, instantaneous limitation, can cause waveform distortions in sinusoidal control (such as in natural and rotational frames) because it truncates the peak points of the sinusoidal waveform according to the current constraints. The instantaneous limiter can be expressed as follows:

$$
I_{\rm ref} = \begin{cases} I_{\rm ref}, & \text{if } |I_{\rm ref}| \le I_{\rm max} \\ I_{\rm max} \cdot \text{sign}(I_{\rm ref}), & \text{if } |I_{\rm ref}| > I_{\rm max} \end{cases} \tag{4.55}
$$

On the other hand, the [CMS](#page-1-11) does not clip the sinusoidal waveform, instead, it decreases the current reference magnitude only and is expressed as:

$$
I_{\rm ref} = \begin{cases} I_{\rm ref}, & \text{if } |I_{\rm ref}| \le I_{\rm max} \\ \frac{I_{\rm max}}{I_{\rm ref}} I_{\rm ref}, & \text{if } |I_{\rm ref}| > I_{\rm max} \end{cases} \tag{4.56}
$$

Therefore, in this thesis, the [CMS](#page-1-11) approach is utilized for better performance. On top of these, since both methods cannot contribute to injecting reactive current during faulty conditions, they may require reactive current injection control by controlling reactive power reference which is given as follows [\[79\]](#page-118-9):

$$
Q_{\text{ref}} = \begin{cases} 0, & \text{if } |V_{\text{PCC}}| \ge 0.9 \text{p.u.} \\ V_{\text{inv}} I_{\text{reactive}}, & \text{if } 0.5 \text{p.u.} < |V_{\text{PCC}}| < 0.9 \text{p.u.} \\ V_{\text{inv}} I_{\text{max}}, & \text{if } |V_{\text{PCC}}| \le 0.5 \text{p.u.} \end{cases} \tag{4.57}
$$

where $I_{reactive}$ is the grid code requirement which is subject to change according to countries. To this end, the block diagram of the current magnitude limitation control is illustrated in Figure [4.21.](#page-48-0) In the figure, $1e^{-6}$ block is implemented in order to avoid zero division.

Figure 4.21: [CMS](#page-1-11) Block Diagram

4.4.2 [Virtual Impedance \(VI\)](#page-2-3)

The principle of [VI](#page-2-3) is to control and increase the impedance Z_L in the model shown in Figure [4.12](#page-37-0) using an [VI,](#page-2-3) thereby limiting the inverter current according to Kirchhoff's voltage law, $V = I \cdot Z$. The [VI](#page-2-3) is applied to the reference voltages obtained from the primary control immediately before they are fed into the voltage loop.

Initially, the fault detection is performed using the calculations provided below, followed by impedance calculations, which are subsequently incorporated into the voltage drop calculation. Virtual inductance X_{VI} and resistance R_{VI} are expressed as follows [\[80\]](#page-118-10):

$$
X_{\rm VI} = \begin{cases} 0, & \text{if } I_{inv} - I_{nom} \le 0 \\ k_{PR} \cdot \sigma_{\frac{X}{R}}, & \text{if } I_{inv} - I_{nom} > 0 \end{cases} \tag{4.58}
$$

and,

$$
R_{VI} = \frac{X_{VI}}{\sigma_{\frac{X}{R}}} \tag{4.59}
$$

where I_{inv} is the inverter output instantaneous current absolute value, I_{nom} is the nominal inverter output current (1 p.u.), k_{PR} is the [VI](#page-2-3) proportional gain, and $\sigma_{\frac{X}{n}}$ is the ratio of virtual inductance with respect to the virtual resistance. If the voltage loop is considered which is given in Figure [4.6,](#page-32-0) the effect of the [VI](#page-2-3) on the voltage references can be explained as follows:

$$
V'_d = V_d * -(R_{VI}i_d - X_{VI}i_q)
$$
\n(4.60)

$$
V'_{q} = V_{q} * - (R_{VI} i_{q} + X_{VI} i_{d})
$$
\n(4.61)

Here, i_d and i_q are the measured output currents as it is illustrated in Figure [4.4](#page-29-0) and, V'_d and V'_q are the new voltage control loop reference values. It is also stated in [\[80\]](#page-118-10) that the k_{PR} is responsible for keeping the steady-state current in an acceptable range while $\sigma_{\frac{X}{R}}$ provides a better response in a fault condition. The control block diagram of the [VI](#page-2-3) is shown in Figure [4.22.](#page-49-0) As mentioned, VI_d and VI_q are subtracted from the voltage reference values generated from the primary control.

Figure 4.22: [VI](#page-2-3) Block Diagram

4.4.3 Negative-Sequence Components Ride Through Modelling

In contrast to symmetrical faults, the occurrence of asymmetrical faults, as discussed in Section 3, leads to the formation of negative and zero sequence components within the network. These components cause significant fluctuations in voltage and current waves, resulting in excessive currents and voltages. Although asymmetrical faults are generally less severe than symmetrical faults, if not properly controlled, they can cause greater damage to the [IBRs.](#page-1-0) Therefore, the implementation of an appropriate [FRT](#page-1-10) control is vital for ensuring system reliability and integrity. It is also worth noting that in this thesis, zero sequence components are not considered because the inverter side comprises three wires without a neutral wire. The asymmetrical faults occurring on the load side are decoupled by a D1-D1 transformer between the load and the [IBRs,](#page-1-0) thereby eliminating the zero sequence components. The negative sequence control scheme adapted for this study is derived from reference [\[81\]](#page-119-0). Certain components are modified and implemented to suit the requirements of this thesis. However, first, the negative sequence components of the inverter must be obtained. To do this, an array of configurations can be implemented, namely low-pass filtering, signal delay cancellation, and cascaded notch filtering [\[82\]](#page-119-1). In this thesis, cascaded notch filtering is utilized due to its simplicity and advantages such as harmonic elimination performance and transient response speed. The block diagram of this sequence component extraction is shown in Figure [4.23.](#page-50-0) Further explanation about sequence analyzer can be found in [\[82\]](#page-119-1).

Figure 4.23: Cascaded Notch Filtering

In [\[81\]](#page-119-0), it is stated that the negative sequence current generated during the asymmetrical fault should be 90◦ ahead with respect to the same sequence voltage and must be controlled. Moreover, this current has to be a function of related voltage according to IEEE Standard 2800-2022. Also, it is mentioned that the different current control approaches and the current limits for positive and negative sequences are required to be different to comply with the [DNOs](#page-1-12) demands. Therefore, the control design will follow these requirements. It should be noted that the subscript 2 is used to remark negative sequence components ((re)active power, voltages, and currents). Based on Figures [4.4](#page-29-0) and Reference [\[81\]](#page-119-0), the current references for the negative sequence current loop at the filter output bus can be expressed as follows:

$$
I_{od_2}^{ref} = \frac{V_{outq_2}}{\sqrt{V_{outd_2}^2 + V_{outq_2}^2}} |I_{o_2}^r|
$$
\n(4.62)

$$
I_{oq_2}^{ref} = \frac{-V_{outd_2}}{\sqrt{V_{outd_2}^2 + V_{outq_2}^2}} |I_{o_2}^r|
$$
\n(4.63)

where the $|I_{o_2}^r|$ is the negative sequence current absolute value and superscript 'r' denotes the reactive current. The relation between the negative sequence current and voltage is given as follows:

$$
|I_{o_2}^r| = K \cdot \sqrt{V_{outd_2}^2 + V_{outq_2}^2}
$$
 (4.64)

where the K is defined by the system operator to fulfill the system needs. The critical point here is that the inverter current controller regulates the current at the inverter's output rather than at the filter output. Therefore, considering that the controlled current is divided across the filter capacitance, the inverter output current can be expressed as follows:

$$
I_{d_2}^{ref} = I_{od_2}^{ref} - \omega C_f V_{outq_2}
$$
\n(4.65)

$$
I_{q_2}^{ref} = I_{oq_2}^{ref} + \omega C_f V_{outd_2}
$$
\n(4.66)

After the inverter current references are obtained, these reference values are fed into the current controller, which, while dedicated to negative sequence control, utilizes the same control scheme as depicted in Figure [4.8.](#page-33-0) The block diagram of the current reference generation is given in Figure [4.24.](#page-51-0)

Figure 4.24: Negative-Sequence Current Reference Generation Block Diagram

Thus, negative sequence components can be incorporated into the control mechanism. However, if the value of K, which is the ratio of negative sequence currents to negative sequence voltages, is chosen to be large, even the negative sequence currents alone can exceed the inverter's maximum capacity. Therefore, both positive and negative sequence current controls must be maintained, ensuring their combination does not exceed the inverter's capacity (which is 1.25 p.u. in this thesis). For this purpose, an appropriate current-sharing control between positive and negative sequence currents should be implemented. This control is defined based on the following equations taken from [\[81\]](#page-119-0) , where more detailed explanations can be found.

$$
I_2^{max} = I_{th}[\lambda_{p/n}^2 + 2\lambda_{p/n} \max(cos(\Delta\delta)) + 1]^{\frac{-1}{2}}
$$
 (4.67)

and

$$
\lambda_{p/n} = \frac{I_1^{max}}{I_2^{max}} \tag{4.68}
$$

where I_1^{max} and I_2^{max} represent maximum positive and negative sequence current magnitude respectively, I_{th} denotes the maximum inverter total current magnitude and $\Delta\delta$ is the angle difference between positive and negative sequence components which is given as:

$$
\Delta \delta = \begin{bmatrix} \delta_{i_1} - \delta_{i_2} \\ \delta_{i_1} - \delta_{i_2} + \frac{2\pi}{3} \\ \delta_{i_1} - \delta_{i_2} - \frac{2\pi}{3} \end{bmatrix}
$$
 (4.69)

and

$$
\delta_{i_2} = \delta_{V_2} + \frac{\pi}{2} \tag{4.70}
$$

where $\delta_{i_1}, \delta_{i_2}, \delta_{V_2}$ are the positive sequence current angle, negative sequence current angle, and negative sequence voltage angle, respectively. From the above equations, the current division block diagram is depicted in Figure [4.25.](#page-52-0)

Figure 4.25: Negative-Sequence Current Division Block Diagram

After obtaining the maximum current values for both sequences, now the current limiting control can be applied. It is observed that applying both [CMS](#page-1-11) and [VI](#page-2-3) control at the same time during asymmetrical faults results in better system response as is detailed in the next chapter. In [VI,](#page-2-3) the current maximum values are used to readjust the I_{nom} by considering Figure [4.22,](#page-49-0) and in [CMS](#page-1-11) it is used instead of I_{th} by considering Figure [4.21.](#page-48-0) The way of the usage of these parameters is explained as follows [\[81\]](#page-119-0):

$$
I_{nom} = I_1^{th} - \Delta I \tag{4.71}
$$

and,

$$
I_{th} = I_1^{max} \tag{4.72}
$$

where ΔI is the trigger margin which means after a predefined value, the [VI](#page-2-3) will be triggered. Since the $I_{th} = 1.25$ and the demand is to trigger [VI](#page-2-3) after 1 p.u, ΔI is defined as 0.25 p.u. It is worth noting that these adaptive values should be triggered only in unbalanced conditions such as when the negative sequence voltage absolute value $(|V_2| = \sqrt{V_{d_2}^2 + V_{q_2}^2})$ is higher than 0.1 p.u. which is expressed as:

$$
UFF = \begin{cases} 1, & \text{if } |V_2| \ge 0.1p.u. \\ 0, & \text{otherwise} \end{cases}
$$
 (4.73)

Then, the adaptive values in current limiting methods can be applied when the UFF is 1. The block diagram of the implementation on [VI](#page-2-3) is given in Figure [4.26.](#page-52-1)

Figure 4.26: Adaptive [VI](#page-2-3) Block Diagram

After also obtaining the current limiting algorithm, only the implementation of the negative sequence signal to the gating signal remains. Figure [4.27](#page-53-0) illustrates this implementation and the overview of the inner control for clarity. Additionally, the adaptive [VI](#page-2-3) and [CMS](#page-1-11) strategies are applied only in the positive sequence control loop. Since the negative sequence control loop is designed to operate as a current source (with only a current control loop), a simple saturation block will suffice.

Figure 4.27: Negative Sequence Control Implementation

Chapter 5 Simulations, Results & Discussion

In this Chapter, the different control methods modeled in Chapter 4 are simulated using Matlab/Simulink, and the results are analyzed and discussed through different study scenarios. Figure [5.1](#page-54-0) depicts the microgrid used for the simulation results.

Figure 5.1: Simulated Microgrid System

As illustrated in the figure, the microgrid comprises four [IBRs.](#page-1-0) The [GFL](#page-1-3) units are considered [PVs,](#page-1-13) while the [GFM](#page-1-4) units are considered as [BESSs.](#page-1-1) Additionally, since it is not the primary focus of this thesis, the dynamics (irradiation, environmental factors, battery health, etc.) of the [PVs](#page-1-13) and [BESSs](#page-1-1) are omitted in the simulations to simplify and shorten the simulation time. Consequently, all are modeled as DC power sources. [GFM1](#page-1-4), rated at 20 kVA [\(GFM2](#page-1-4) will be connected during the interoperability simulations), and two [GFLs](#page-1-3), rated at 10 kVA, are connected to the [PCC](#page-1-2) bus via an LCL filter, a D1-D1 transformer, and a line impedance. Subsequently, the system is connected to a variable load block, which can be inductive or resistive, through another line impedance. Additionally, circuit breakers, which disconnect the [IBRs](#page-1-0) when necessary, are depicted in Figure [5.1.](#page-54-0) Furthermore, the main grid is connected to the [PCC](#page-1-2) bus through an impedance after voltage regulation by a transformer. The transition of the microgrid between islanded and [G-C](#page-1-6) modes is facilitated by the circuit breaker located adjacent to the grid bus. The load blocks can be conceptualized as any neighborhood, and the simulated grid faults occur after an impedance to these load blocks. Also, line impedances are given as $0.11/\text{km }\Omega$ resistance and $5.84 * 10^{-3}/\text{km }\text{H}$ inductance. The distances of the [IBRs](#page-1-0) from the microgrid bus are equal and set to 0.1 km, while the distance between the microgrid bus and the load blocks is set to 2.5 km. Consequently, the impedances are defined as: $Z_{1,2,3,4} = 0.1 \times (0.11 + j5.84 \times 10^{-3})$ and $Z_5 = 2.5 \times (0.11 + j5.84 \times 10^{-3})$. Also, the fault occurs 100 m away from the load which also means $Z_6 = 0.1 \times (0.11 + j5.84 \times 10^{-3})$ The grid impedance Z_7 is also set to 2.5 km line impedance.

5.1 [Grid-Connected \(G-C\)](#page-1-6) Mode

The behavior of the [GFM](#page-1-4) and the [GFLs](#page-1-3) operating in a [G-C](#page-1-6) microgrid under different scenarios e.g, load change, symmetrical and asymmetrical faults, and transition are analyzed and discussed in this section.

5.1.1 Load Change

In order to investigate the response of [GFMs](#page-1-4) and [GFLs](#page-1-3) to the load change, this simulation is conducted. Initially, a 45 kW and 5 kVAr load is connected to the microgrid. At second 2.5, a new 15 kW and 3 kVAr load istripped, and finally, at second 3.5, a 20 kW and 0 KVar load is connected. Also, for this simulation, the active and reactive power references of the [GFM](#page-1-4) are set to 0.6 and 0 p.u., respectively. These references can be chosen according to system needs. The remaining load is being supplied by the main grid.

Figure 5.2: Load Change Behaviours of [IBRs](#page-1-0)

Figure [5.2a](#page-55-0) and [5.2b](#page-55-0) illustrates the active and reactive power outputs of [GFM1](#page-1-4) (20 kVA) and [GFL1](#page-1-3) (10 kVA), respectively, under droop and [VSG](#page-2-2) control. As observed in the figure, albeit marginal, the droop control's response to load variation is superior because the power fluctuation is less pronounced under droop control compared to [VSG](#page-2-2) control. Additionally, it is worth noting as a preliminary finding that the settling time to reach a steady state of [VSG](#page-2-2) is slower than that of droop control. This is due to [VSG](#page-2-2) providing more inertia to the system. The [GFL](#page-1-3) yields consistent results independent of whether the [IBRs](#page-1-0) are operating under [VSG](#page-2-2) or droop control, tracking the grid voltage without current fluctuations. The primary reason for this is that the designed grid is strong (with an [SCR](#page-1-14) of approximately 8), hence the [PLL](#page-1-8) does not encounter significant challenges in tracking the grid frequency. Conversely, in a weak grid, this could lead to substantial issues. Furthermore, the difference in reactive power outputs of the [GFMs](#page-1-4) under different controls is noteworthy (see Figure [5.2a\)](#page-55-0). Under droop control, a negligible reactive power absorption is observed due to the filter capacitance effect (less than 0.1 p.u.), whereas the reactive power sharing issue commonly mentioned in the literature for [VSG](#page-2-2) is also evident in this simulation (around 0.4 p.u.). This effect is caused by the lack of inherent droop characteristics of [VSGs](#page-2-2). Nevertheless, in both control methods, the load change is seamlessly achieved without causing any synchronization issues. Also, [GFL2](#page-1-3) showed a similar response.

5.1.2 Symmetrical Fault

In this section, 3-phase symmetrical faults are simulated under both Droop- and [VSG](#page-2-2)controlled [GFMs](#page-1-4) while different [FRT](#page-1-10) methods are utilized. The fault resistance is chosen as 0.035 Ω which decreases the voltage sag to 0.15 p.u. on the load and is applied for 200 ms (1.4-1.6 s) as the worst case just before disconnecting the [IBRs](#page-1-0) according to the Dutch [GC.](#page-1-7) Lastly, the total load is defined as 45 kW and 5 kVAr. Moreover, since the primary research focus of this thesis is on the [FRT](#page-1-10) capabilities of [GFMs](#page-1-4), the behavior of [GFLs](#page-1-3) during fault conditions will not be examined in this section. Regarding [FRT,](#page-1-10) the expected features from a [GFM](#page-1-4) during and after a fault include maintaining synchronization with the system, limiting the overcurrents on the inverter (set to 1.25 p.u. in this thesis), keeping the frequency within the permissible range, providing voltage regulation, and reactive power support. In this context, the following subsections delve into these topics. However, to better understand the effects of the applied control methods, the load voltage in the dq frame is presented in Figure [5.3.](#page-56-0)

Figure 5.3: Load Voltages in the dq0 Frame

As observed in Figure [5.3,](#page-56-0) the load voltage decreases to 0.15 p.u. levels without the connection of [IBRs.](#page-1-0) After connecting the [GFMs](#page-1-4) without any current limitation, the voltage rises almost to 0.3 p.u.; however, in this scenario, the inverters provide currents far beyond their capacities, risking potential damage since there is no limitation on the current. On the other hand, with current limitation applied, the voltage increases to 0.18 p.u. Without current limitation, it is evident that during the post-fault period, the [GFMs](#page-1-4) lose synchronization, the voltage and current control loops reach saturation, and the voltage distorts and exceeds its nominal value (1 p.u.). Additionally, the deviations at the beginning and end of the fault in the q-frame likely result from the [PLLs](#page-1-8) used for frequency measurement losing synchronization. The reduced deviation can be attributed to the frequency support provided by the [GFMs](#page-1-4). Also, the [GFM](#page-1-4) output voltage and

Figure 5.4: [GFM](#page-1-4) Outputs Before [FRT](#page-1-10) Implementation

current waveforms (only phase A as an example) are important to investigate before any [FRT](#page-1-10) implementation, which is given in Figure [5.4](#page-57-0)

As clearly illustrated in Figure [5.4a,](#page-57-0) the voltage waveform of phase A has dropped to around 0.5 p.u., and the results are almost identical for both control methods(also for the other phases since it is a symmetrical fault) during the fault. However, it is noteworthy that the voltage waveforms are not perfectly sinusoidal and exhibit distortion. The voltage peak of [VSG](#page-2-2) is around 1.17 p.u in steady state after fault which is above the Dutch [GC](#page-1-7) limit of 1.1 p.u. while droop voltage magnitude is within the limit. This is probably caused by the reactive power-sharing error of [VSGs](#page-2-2). According to the control algorithm, reactive power is linked to voltage, and deviations in the amount of reactive power at the output lead to an increase in voltage levels. Similarly, the current outputs show nearly identical results during the fault, with current levels reaching 5-6 p.u. This far exceeds the capacity that the inverter can handle (1.25 p.u.), and in a real scenario, the inverter would sustain permanent damage. During the postfault process, the current waveforms cannot find a steady state since the synchronization with the grid is lost. Lastly, the frequency output of [GFMs](#page-1-4) is important to examine. From Figure [5.5,](#page-58-0) it is evident that the synchronization is totally lost for both controls. Nevertheless, as it is expected, the frequency peaks of [VSG](#page-2-2) control are less than droop control because of the greater inertia of [VSG.](#page-2-2)

Figure 5.5: Frequency Change of [GFMs](#page-1-4)

5.1.2.1 [FRT](#page-1-10) with [CMS](#page-1-11)

The current limiting algorithm depicted in Figure [4.21](#page-48-0) is applied to both droop and [VSG](#page-2-2)based control methods during a symmetrical fault. To better observe the distortions in voltage during the fault, Figure [5.6](#page-58-1) shows the inverter voltage outputs in the dq frame.

Figure 5.6: [GFM](#page-1-4) Output Voltages in dq0 Frame

As it can be noticed in Figure [5.6,](#page-58-1) during the fault the voltage outputs in the d and q axes are not distorted and both control behaves the same during fault duration. At the beginning of the fault, and just after the fault there is a high-frequency distortion that continues for 10 ms due to the response time of the primary control. However, this distortion can be neglected since it is immediately restored. During the postfault process, the [VSG](#page-2-2) control output voltage quickly settled down to the nominal value, while droop control shows a little bit of deviation in the d and q frame due to relatively high [RoCoF.](#page-1-5) Meanwhile, the voltage and current outputs are presented in the abc frame in Figure [5.7](#page-59-0) (only phase A is illustrated for clarity). Note that the inverter output current is

Figure 5.7: Voltage and Current Outputs of Inverters

successfully limited to 1.25 p.u. in both cases, and the current waveforms are obtained as pure sinusoids (see Figure [5.7b\)](#page-59-0). Achieving output voltages and currents without distortion is crucial for power quality. Upon the termination of the fault, the [VSG](#page-2-2) control current graph reaches its nominal value in nearly a linear manner within 0.2 seconds. In contrast, under droop control, the voltage loop experiences saturation for 0.2 seconds, followed by a minor oscillation in the current graph, and ultimately reaches its nominal value in a total of 0.5 seconds. In both control methods, the voltage magnitude hovers around 0.17 p.u. during the fault (see Figure [5.7a\)](#page-59-0). Post-fault, the [VSG](#page-2-2) control promptly returns to its nominal value, while the droop control experiences minor oscillations with small overshoots. However, these overshoots remain within acceptable limits (1.06 p.u.) according to Dutch [GC.](#page-1-7)

The active power level in both methods dropped to around 0.2 p.u. and remained there during the fault (Figure [5.8a\)](#page-60-0). However, in the post-fault period, [VSG](#page-2-2) control exhibited less overshoot and reached a steady state more quickly. The delay in droop is due to temporary saturation in the voltage control loop. Regarding reactive power referring to Figure [5.8b,](#page-60-0) both control methods provided reactive power support to the grid during the fault. The reactive power fluctuations are similar in both controls as active power. Finally, the change in microgrid frequency is shown in Figure [5.8c.](#page-60-0) As expected, the frequency deviation in [VSG](#page-2-2) is smaller due to the higher inertia provided. Even in this most severe fault, the frequency value peaked at 50.2-49.65 Hz and quickly returned to its nominal value thanks to the collaboration of primary and secondary control.

Additionally, it is worth noting that, during a 200 ms fault with the [CMS](#page-1-11) strategy, the voltage control loop in both control types experienced saturation and completely lost synchronization, causing the voltage output to cease tracking the reference value in voltage control. This situation is illustrated in Figure [5.9.](#page-61-0) To prevent this undesirable condition, the voltage control loop PI controllers should be reset at the end of the fault. The voltage drop at the [PCC](#page-1-2) can be used as a reference to detect the fault condition. For instance, a reset signal can be sent to the PI controller when the [PCC](#page-1-2) voltage recovers 0.85 p.u., enabling a swift response. Nevertheless, minor delays due to fault detection might occur, but these delays are not accounted for in this thesis.

Figure 5.8: Power and Frequency Outputs of Inverters with Fault Detection

Figure 5.9: Power Outputs Without Fault Detection

5.1.2.2 [FRT](#page-1-10) with [VI](#page-2-3)

The [VI](#page-2-3) method depicted in Figure [4.22](#page-49-0) is applied in the simulations discussed in this section. To more clearly observe the voltage qualities at the inverter outputs during and after the fault, Figure [5.10](#page-61-1) is provided initially. Similar to the previous section, aside from the high-frequency harmonics occurring for 10 ms during and immediately after the fault, both control methods maintained synchronization. In this configuration, the dominance of the [VSG](#page-2-2) control on the voltage outputs is pronounced again. Post-fault, the [VSG](#page-2-2) control brings the voltage value to a steady state within 0.015 seconds, whereas the droop control achieves this in 0.15 seconds. Nonetheless, the voltage fluctuations remain within acceptable limits. It is particularly noteworthy that the post-fault behavior, especially for the droop control, is improved in this [FRT](#page-1-10) method compared to the [CMS.](#page-1-11)

Figure 5.10: [GFM](#page-1-4) Output Voltages in dq0 Frame

On the other hand, when examining the single-phase voltage and current graphs from

Figure 5.11: Voltage and Current Outputs of Inverters

Figure [5.11,](#page-62-0) it is observed that similar to the previous [FRT](#page-1-10) method, the current is successfully stabilized around 1.24 p.u. during the fault and the sinusoidal waveform is preserved. Under [VSG](#page-2-2) control, the current again reaches a steady state with a linear decrease. However, this time, under droop control, the long-term saturation of the voltage controller and subsequent oscillations observed in [5.7b](#page-59-0) are absent, and it reaches a steady state simultaneously with the [VSG.](#page-2-2) Additionally, the small and persistent peaks in voltage waveform previously seen in droop control are not observed. The only noticeable weakness of the [VI](#page-2-3) method is the distortion in the current waveform occurring immediately after the fault and lasting for 15 ms. However, this distortion is short-lived and does not affect synchronization, thus it can be disregarded.

Finally, the inverter output powers are depicted in Figure [5.12a](#page-63-0) and [5.12b.](#page-63-0) Although the responses of both control methods are identical during the fault, post-fault behavioral differences are clearly observable. Additionally, the post-fault superiority of the [VI](#page-2-3) method over the [CMS](#page-1-11) should be noted. The reduction in active power peak from 1.3 p.u. to 1.05 p.u. is evident. While the behavior of [VSG](#page-2-2) remains relatively unchanged, the active power curve under Droop control, which previously reached a stable state in approximately 0.5 seconds, now achieves stability in 0.2 seconds. In this case, Droop responds faster than [VSG.](#page-2-2) This indicates that in the absence of inner control loop saturation, Droop control, due to its lower inertia, can respond more quickly to changes in system dynamics. In terms of reactive power curves, although [VSG](#page-2-2) remains relatively consistent, the significant 1.2 p.u. post-fault peak observed under Droop control is entirely eliminated compared to the case [CMS](#page-1-11) utilized. The voltage level remains stable under Droop control because this peak is no longer present. The frequency response, as shown in Figure [5.12c,](#page-63-0) again favors [VSG.](#page-2-2) Initially, within the first 0.05 seconds, the frequency responses are identical due to the control bandwidth, but subsequently, the more stable frequency graph of [VSG](#page-2-2) is clearly visible. Nevertheless, since the frequency gradient which is between 49.77 and 50.25 Hz in this controller is within the limits prescribed by the Dutch [GC,](#page-1-7) both controllers successfully maintain synchronization during and after the fault.

Figure 5.12: Power and Frequency Outputs of Inverters

5.1.3 Asymmetrical Faults

As discussed in the previous chapter, although asymmetric faults are less severe compared to symmetric faults, their control and the functional maintenance of [IBRs](#page-1-0) are more complex to design. This chapter will only examine the [GFMs](#page-1-4) reponses under [Single-](#page-2-4)[Phase-to-Ground \(SPG\)](#page-2-4) faults and [Phase-to-Phase \(PP\)](#page-1-15) faults. The behavior of [GFLs](#page-1-3) will not be discussed. As stated before, [PP](#page-1-15) faults are the most severe types of asymmetric faults. It is worth noting that Phase-to-Phase-to-Ground faults when simulated, produced system responses similar to those observed in [SPG](#page-2-4) faults. The same circuit schematic, loads, and line impedances used in the symmetric fault simulations are also applied here. Additionally, to simulate a relatively severe fault in the case of [SPG](#page-2-4) faults, the ground resistance is set to 0.5 m Ω . An asymmetrical fault occurs again at second 1.4 and lasts at second 1.6. Initially, the effects of asymmetric faults on the load voltage without a [GFM](#page-1-4) and in the case of a [GFM](#page-1-4) available, without a [FRT](#page-1-10) control are evaluated. Figure [5.13](#page-64-0) depicts the load voltage in the dq0 frame in the case of [PP](#page-1-15) fault and without [IBRs,](#page-1-0) with [IBRs](#page-1-0) but without [FRT,](#page-1-10) and with [IBRs](#page-1-0) and [FRT.](#page-1-10)

Figure 5.13: Load Voltage in dq-axes

As seen in the figure above, the dq axes are no longer a DC component as they are during symmetric faults. This is due to the 100 Hz negative (or zero) sequence components that arise when the current and voltage phases are unbalanced. In this thesis, a threewire system is used, allowing us to neglect zero-sequence components. Negative sequence (and zero-sequence when they exist) components are unavoidable disturbances that occur whenever there is an imbalance in the phases. As shown in Figure [5.13a,](#page-64-0) the presence of [GFM](#page-1-4) units has mitigated the voltage drop in the steady-state condition, similar to symmetric faults. The same scenario applies during fault conditions; although the [GFMs](#page-1-4) reduce the voltage support on the load when a [FRT](#page-1-10) method is utilized, they still provide better results compared to the scenario without [GFM.](#page-1-4) On the other hand, the absence of a [FRT](#page-1-10) method could result in permanent damage to the [GFMs](#page-1-4). Post-fault, it is evident that [GFMs](#page-1-4) lose synchronization when a [FRT](#page-1-10) method is not employed. When [GFMs](#page-1-4) are used with a [FRT,](#page-1-10) a high-frequency disturbance lasting 0.02 seconds is observed, but this duration is short enough to be considered negligible. Figure [5.13b](#page-64-0) shows similar conditions on the q axis, where the disturbance is more pronounced without a [FRT](#page-1-10) method postfault.

It is crucial to examine the voltage and current waveforms at the [GFM](#page-1-4) outputs before applying any [FRT](#page-1-10) methods. The output values are provided in Figure [5.14.](#page-65-0)

Figure 5.14: [GFM](#page-1-4) Outputs Before [FRT](#page-1-10) Implementation

First and foremost, it should be noted that the above graphs illustrate the inverter output solely under droop control conditions. For simplicity and to avoid graphical complexity, comparison graphs have not been provided, although the [VSG](#page-2-2) exhibits a similar output response. Furthermore, examining the voltage graph reveals that the voltage value in the healthy phase (phase C) remains approximately 1.25 p.u. throughout the fault duration. According to the Dutch [GC,](#page-1-7) this necessitates the disconnection of the [GFM.](#page-1-4) Additionally, the high-frequency disturbances caused by the negative sequence components observed across all phases have deteriorated the power quality. When analyzing the current graph, an initial peak of 3.5 p.u. is observed in the first cycle, with subsequent peak values of 2.18 and 2.22 p.u. in the faulty phases, which are significantly above the permissible limit of 1.25 p.u. Similarly, the disturbances in the healthy phase are also evident in the current graph.

In the subsequent sections, the [CMS](#page-1-11) approach will be examined for the [SPG](#page-2-4) fault, while the [VI](#page-2-3) approach will be analyzed for the [PP](#page-1-15) fault.

5.1.3.1 [FRT](#page-1-10) with [CMS](#page-1-11)

In order to further examine the distortions in the inverter output voltage, voltage graphs in dq0 frame for two different control types are presented in Figure [5.15.](#page-66-0)

As expected, the distortions caused by the 100 Hz negative sequence components during faults cannot be prevented. Additionally, when examining the peak points of the 100 Hz waves, it is evident that the [PP](#page-1-15) fault is more severe (0.7 p.u. for [PP](#page-1-15) fault and 0.4 p.u. for [SPG](#page-2-4) (compared to Figure [5.18\)](#page-69-0)). Furthermore, approximately 700 Hz [SPWM-](#page-2-0)based harmonic distortions at the beginning and end of the fault are also observed here. The superiority of [VSG](#page-2-2) control over droop control is evident in this context as well. Particularly, the oscillations in the d-axis seen in droop control are more stable under [VSG](#page-2-2) control. This will affect system stability during the fault duration. Moreover, it is noticeable that the waveforms under droop control generally exhibit 0.05 p.u. higher values compared to [VSG](#page-2-2) control.

Figure 5.15: [GFM](#page-1-4) Output Voltages in dq0 Frame

In Figure [5.16,](#page-67-0) the inverter voltage and current outputs for both control methods during a [SPG](#page-2-4) fault are presented. The outputs are similar in both control methods. The voltage peak values observed at the end of the fault, reaching approximately 1.25 p.u. and lasting for 6-7 ms, can be disregarded as they are not continuous and are of short duration. The distortions in the voltage outputs during the first 20 ms in both control methods correspond to initial distortions in Figure [5.15.](#page-66-0) However, after this period, synchronization is achieved in both control methods, and the inverter provides voltage support. The current graphs indicate that only with the [CMS](#page-1-11) approach, phase mixing occurs in the current waves, resulting in inadequate current support. The inverters are unable to provide a stable current until the fault is cleared. Additionally, for 4-5 cycles, the current value in both control methods exceeds the permissible limit of 1.25 p.u.

In Figure [5.17,](#page-68-0) the power and frequency outputs are also presented. Although 100 Hz oscillations in the active power output are expected, these oscillations did not settle into a steady state during the fault and produced chaotic output due to distortions in the current output. Furthermore, while droop control reaches a steady state faster than [VSG](#page-2-2) post-fault, [VSG](#page-2-2) is superior in terms of the power value jumps during the fault. Reactive power support is also provided to the grid. The reactive power output, which is around -0.06 p.u. before the fault, oscillated at approximately 0.5 p.u. on average. After the fault, both controllers successfully returned to a steady state. Lastly, the frequency graph showed, as expected, smaller jumps compared to symmetrical faults (50.04 - 49.9 Hz). Additionally, [VSGs](#page-2-2) superiority is evident during and after the fault. Specifically, droop control exhibits periodic oscillations of around 0.05 Hz post-fault, whereas these oscillations are weaker and gradually damped in the [VSG](#page-2-2) controller.

Figure 5.16: [SPG](#page-2-4) Fault Inverter Outputs in ABC Frame

Figure 5.17: [SPG](#page-2-4) Fault Inverter Power and Frequency Outputs

In summary, while the frequency values remain within limits due to the weak fault severity, the voltage and power support provided to the grid are not of the desired quality, and prolonged exceedance of set limits could damage the inverter. This situation worsens in the case of a [PP](#page-1-15) fault. Consequently, although the [CMS](#page-1-11) approach limits the current and provides reactive power support, it does not meet the expectations in terms of power quality.

5.1.3.2 [FRT](#page-1-10) with [VI](#page-2-3)

As mentioned, the [PP](#page-1-15) fault is observed with the [VI](#page-2-3) approach. Figure [5.18](#page-69-0) shows the voltage amplitude in the dq frame.

When using [VI,](#page-2-3) the voltage output of the [VSG](#page-2-2) during the fault is more stable and resembles a 100 Hz sine wave compared to droop control. In droop control, the voltage value on the d-axis has peak values that occasionally exceed 0.15 p.u., oscillating in contrast to [VSG.](#page-2-2) Additionally, post-fault, droop control struggles more with synchronization, exhibiting more distortions. Similar observations can be made for the q-axis. Due to the fault severity, these peak values are greater than those observed in the [SPG](#page-2-4) fault. However, in the [SPG](#page-2-4) fault, due to the ground connection, the severely distorted 100 Hz waves caused by potential zero-sequence components during the fault are almost negligible in this case. The voltage controller also takes longer to stabilize after the fault for droop

Figure 5.18: [GFM](#page-1-4) Output Voltages in dq0 Frame

control because it is a more severe fault (20 ms and 50 ms, respectively).

As seen in Figure [5.19,](#page-70-0) the voltage values during and after the fault are very similar for both primary control methods. In both graphs, the healthy phase peak voltage has exceeded the permissible 1.1 p.u. limit (approximately 1.8 - 1.9 p.u.). Under normal conditions, according to the Dutch [GC,](#page-1-7) this [IBRs](#page-1-0) should be disconnected. Furthermore, the non-sinusoidal waveforms in the faulty phases also prevent the [GFM](#page-1-4) from providing quality reactive power support to the grid. In the current graphs, peak current values reaching approximately 3 p.u. observed in the first few cycles in both controls could cause permanent damage to the [GFM.](#page-1-4) Subsequently, the [VI](#page-2-3) method has also failed to limit the current to 1.25 p.u.

In Figure [5.20,](#page-71-0) both primary control methods show nearly identical active and reactive power outputs. The onset of faults in current peak levels leads to sudden increases in power outputs. Additionally, severe distortions in the 100 Hz natural oscillations, seen in [SPG](#page-2-4) faults but absent in [PP](#page-1-15) faults due to the absence of zero-sequence components, are nearly sinusoidal. Furthermore, the 700 Hz harmonics observed at the onset and post-fault are not present here. In the frequency graph, the superiority of the [VSG](#page-2-2) observed in previous configurations is not evident here. Although the frequency responses are not identical, they exhibit similar characteristic features. The frequency variation remains within the range of 50.12 and 49.92 Hz, which is within acceptable limits according to the Dutch [GC.](#page-1-7)

Figure 5.19: [PP](#page-1-15) Fault Inverter Outputs in ABC Frame

Figure 5.20: [PP](#page-1-15) Fault Inverter Power and Frequency Outputs
5.1.3.3 [FRT](#page-1-0) Hybrid Approach

Upon finding that both [FRT](#page-1-0) approaches provide unsatisfactory results under asymmetric faults, both control methods are integrated into the system simultaneously seeking for a better result. The primary objective is to maintain the inverter's output voltage below 1.1 p.u., the current below 1.25 p.u., and to provide relatively high-quality active/reactive power support during the fault. In this section, both types of faults will be examined. Figure [5.21](#page-72-0) presents the inverter output voltage in the dq frame under the hybrid approach for both fault types.

Figure 5.21: Inverter Voltage Outputs in dq Frame for Both Faults

Upon applying the hybrid [FRT](#page-1-0) method, it is observed that the [GFM](#page-1-2) outputs for both primary control methods are identical. The 100 Hz component's distortions seen in the voltage output in dq frame during [SPG](#page-2-0) faults with [CMS,](#page-1-3) and the voltage magnitude fluctuations in dq frame during [PP](#page-1-1) faults with [VI,](#page-2-1) are not observed here. Despite both methods having unavoidable 100 Hz negative sequence components during the fault, they provide stable sinusoidal outputs. Additionally, since the saturation of the voltage control loop is prevented, both control methods returned to their nominal values within approximately 10 ms after the fault. High-frequency distortions at the fault inception are also mitigated.

In Figures [5.22](#page-73-0) and [5.23,](#page-74-0) the inverter output graphs in the ABC frame after two different asymmetric faults are presented. As shown in Figures [5.22a](#page-73-0) and [5.22c,](#page-73-0) the voltage graphs in the case of a [PP](#page-1-1) fault are purely sinusoidal, and the voltage values remain below 1.1 p.u. during and after the fault (the peak value of 1.19 p.u. at the end of the fault lasts for only 10 ms and is thus negligible). Additionally, these graphs yield identical results for both control methods. In the current graphs of the same fault (Figures [5.22b](#page-73-0) and [5.22d\)](#page-73-0), all phases exhibit sinusoidal waveforms. However, it is worth noting that in droop control, minor fluctuations during the fault in healthy phases reduce power quality. This issue is not observed in [VSG.](#page-2-2) Nonetheless, in both control methods, the current is successfully limited to below 1.25 p.u. The current spikes measured at the fault inception in one [FRT-](#page-1-0)applied configurations are not seen here. On the other hand, considering the [PP](#page-1-1) fault, the voltage graphs in Figures [5.23a](#page-74-0) and [5.23c](#page-74-0) are also sinusoidal (in steady state) and are successfully limited to below 1.1 p.u., similar for both control methods. As seen in Figures [5.23b](#page-74-0) and [5.23d,](#page-74-0) the current in both control methods is also

Figure 5.22: [SPG](#page-2-0) Fault Inverter Outputs in ABC Frame

Figure 5.23: [PP](#page-1-1) Fault Inverter Outputs in ABC Frame

successfully limited to 1.25 p.u. Furthermore, the instantaneous current spikes of 2-3 p.u. at the fault inception are prevented. The purely sinusoidal nature of the current graphs enhances power quality.

Figure 5.24: Power Outputs Under Both Faults

In Figures [5.24a](#page-75-0) and [5.24c,](#page-75-0) the active power graphs show that the peaks of the 100 Hz wave have significantly decreased compared to previous configurations. Although droop control still experiences distortions in sinusoidal waveforms during the [SPG](#page-2-0) fault, these distortions are weaker and eventually align with the [VSG.](#page-2-2) In the [PP](#page-1-1) fault, the active power outputs are almost identical. Post-fault, droop exhibits superior behavior in the [SPG](#page-2-0) fault, while this is reversed in the [PP](#page-1-1) fault. In the reactive power graphs in Figures [5.24b](#page-75-0) and [5.24d,](#page-75-0) it is evident that support is still provided to the grid. In the [PP](#page-1-1) fault, droop control shows an overshoot of 0.05 more than the [VSG.](#page-2-2) The post-fault behavior is similar to that of active power. Finally, examining the frequency response in Figures [5.25a](#page-76-0) and [5.25b,](#page-76-0) both controls provide similar responses, with frequency values ranging between 50.06 and 49.93 [\(SPG\)](#page-2-0) and 50.06 and 49.92 [\(PP\)](#page-1-1). These values comply with the Dutch [GC.](#page-1-4) However, it should be noted that [VSG](#page-2-2) control exhibits fewer oscillations in the post-fault frequency response, indicating greater inertia and stability.

Figure 5.25: Inverter Frequency Outputs for Both Faults

5.1.4 Transition Between [G-C/](#page-1-5)Islanded Mode

As discussed in Section 4.2.3.2, synchronization control should be applied as secondary control during transitions of the microgrid between [G-C](#page-1-5) and islanded modes. The block diagram in Figure [4.19](#page-45-0) is integrated at this point. Figure [5.26](#page-77-0) shows the voltage and current waveforms during the transition from [G-C](#page-1-5) to islanding mode and vice versa without the application of synchronization control. As can be clearly seen from Figure [5.26a,](#page-77-0) the transition at second 1 from [G-C](#page-1-5) to islanding mode resulted in a smooth change due to the absence of synchronization problems. There is no distortion in the voltage signal, and the current waveform exhibited only a half-period spike of approximately 0.2 p.u. However, in Figure [5.26b,](#page-77-0) at second 3.5, when the transition from islanding to [G-C](#page-1-5) mode occurred, the current value suddenly surged to 7.5 p.u. from its instantaneous value due to the reasons mentioned above. It is impossible for the inverter to tolerate this magnitude of current, and as a result, it could completely shut down. Moreover, there is significant distortion in the voltage signal corresponding to the change in the current magnitude. Another important note is that the current exceeding 7 p.u. also leads to a permanent instability at the inverter output.

In Figure [5.27,](#page-77-1) the voltage and current waveforms during the transition phases after the application of synchronization control are shown. As observed, at second 1, the transition from [G-C](#page-1-5) to islanding mode exhibits the same signal characteristics as in the unsynchronized control. However, the significant difference can be seen at second 3.5, during the transition from islanding to [G-C](#page-1-5) mode. This time, there is no distortion in the voltage signal, and the current signal does not exhibit the previously observed peak. The current value is smoothly regulated, and the system maintains stable operation.

Figure 5.26: Transitions Without Synchronisation Control

Figure 5.27: Transitions With Synchronisation Control

Finally, the waveforms illustrating the synchronization algorithm's effectiveness in

minimizing the phase difference between the utility grid and microgrid voltages are presented in Figure [5.28.](#page-78-0) As seen in Figure [5.28a,](#page-78-0) considering that the system operates in islanded mode between 1 and 3.5 seconds and in [G-C](#page-1-5) mode for the remainder, the phase difference between the two sides begins to increase at second 1. However, after the transition signal is received and the algorithm is activated, as shown in Figure [5.28b,](#page-78-0) at the moment of transition from islanded to [G-C](#page-1-5) mode (second 3.5), the phase difference between the two sides is reduced to nearly zero, making it almost impossible to distinguish between the two waveforms.

Figure 5.28: Phase Differences During Both Operating Mode

5.2 Islanded Mode

In this section, as shown in Figure [5.1,](#page-54-0) the switch connecting the main grid to the system is opened. As a result, the loads are now solely supplied by two 10 kVA [GFLs](#page-1-6) and one 20 kVA [GFM.](#page-1-2)

5.2.1 Load Change

To prevent the inverters from being overloaded, the total load is now changed to 32 kW, 5 kVAr initially. Connecting a load exceeding the installed capacity in islanded mode, without any external support, could result in excessive current draw from the inverters and cause permanent damage. In islanded mode, the [GFM](#page-1-2) needs to maintain the stability of the microgrid network and preserve grid synchronization during resistive or inductive load changes and load-shedding events. To examine the [GFM'](#page-1-2)s response to these changes, an 8 kW, 5 kVAr load is shed at second 2.5, leaving the load completely resistive. Subsequently, a 17 kW, 3 kVAr load is added at second 3.5. The results obtained for both control methods are shown in Figure [5.29.](#page-79-0)

As shown in Figure [5.29a,](#page-79-0) both control methods have smoothly and quickly tracked the loads that are shed and added. The reactive power sharing error observed in [G-C](#page-1-5) mode is not present here due to the absence of interaction with the main grid. Additionally, the delayed transition to steady state observed with [VSG](#page-2-2) in [G-C](#page-1-5) mode is not observed here, and both control methods have provided nearly identical outputs. Therefore, there is no significant superiority of one control method over the other during load changes in microgrids operating in islanded mode. On the other hand, as in [G-C](#page-1-5) mode, the [GFLs](#page-1-6) continue to provide full capacity active power support independently of the different [GFMs](#page-1-2) as illustrated in Figure [5.29b.](#page-79-0)

Figure 5.29: Load Change Behaviours of [IBRs](#page-1-7) in Islanded Mode

5.2.2 Symmetrical Fault

To observe the effects of [FRT](#page-1-0) approaches, it is important to first examine the behavior of inverter current and voltage outputs during a fault without any [FRT](#page-1-0) method applied. However, this time, as there is no external support to the microgrid, the fault resistance used in [G-C](#page-1-5) mode would almost drop the load voltage to zero in islanded mode. Therefore, in islanded mode, for the most severe fault, a three-phase fault, the fault resistance is set to 735 m Ω , which reduces the load voltage to 0.15 p.u. Additionally, to comply with the Dutch [GC](#page-1-4) requirements, faults lasting 200 ms are applied. The total load is set to 35 kW, 5 kVAr, in line with the total microgrid capacity. The behavior of [GFLs](#page-1-6) will not be examined in this section, as it is not the focus of the study.

Figure 5.30: [GFM](#page-1-2) Output Voltages in dq0 Frame

In Figure [5.30,](#page-79-1) it is observed that in a microgrid with the [FRT](#page-1-0) method applied, the load voltage drops to 0.15 p.u. Without the [FRT](#page-1-0) method, the voltage drop improves by 0.20 p.u. to 0.35 p.u. However, in the q axes, a deviation occurs for the non[-FRT](#page-1-0) situation. Different to the [G-C](#page-1-5) mode, the simulation without the [GFM](#page-1-2) is not considered

here since the microgrid lacks any voltage and frequency regulators. In this scenario, the single-phase voltage and current output graphs of the inverters (the other phases are identical with a 120-degree phase shift due to the symmetrical fault) are shown in Figure [5.31.](#page-80-0) As seen, the voltage and current graphs are identical in this case, unlike in the [G-C](#page-1-5) mode (see Figure [5.4\)](#page-57-0). The literature extensively discusses the interactions and adverse effects of different types of [GFMs](#page-1-2) with strong (high [SCR\)](#page-1-8) grids. This situation can be clearly seen here as well. The key point to note is that the peak value of the current wave is around 4 p.u., which is beyond the feasible current supply capacity of the [GFM.](#page-1-2) It is also observed that the voltage wave cannot produce a perfect sinusoidal wave at the moment of fault, experiencing distortions. Finally, the 1.24 p.u. overshoot in the voltage wave at the end of the fault exceeds the limits, but it can be disregarded as it lasts for 10 ms before returning to its nominal value.

Figure 5.31: [GFM](#page-1-2) Outputs Before [FRT](#page-1-0) Implementation

Finally, as observed in Figure [5.32,](#page-81-0) the frequency outputs indicate a clear superiority of [VSG.](#page-2-2) However, in the absence of a main grid, the system inertia is significantly lower, leading to greater frequency deviation as expected. When compared to the [G-C](#page-1-5) mode illustrated in Figure [5.5,](#page-58-0) the frequency variation band is nearly 0.5 Hz wider. Specifically, in the droop control, the frequency drops from 49.6 Hz to 49.2 Hz, highlighting the difference in inertia, especially considering the lower fault resistance. Additionally, [VSG](#page-2-2) shows an advantage over droop control by returning to the nominal value (50 Hz) more quickly due to its smaller deviation. Nonetheless, according to the Dutch [G-C,](#page-1-5) after a 200 ms fault, both control methods successfully synchronize with the system and return to the nominal value, making both methods viable for use.

Figure 5.32: Frequency Change of [GFMs](#page-1-2)

5.2.2.1 [FRT](#page-1-0) with [CMS](#page-1-3)

First, the [GFM](#page-1-2) voltage output in the dq frame is given in Figure [5.33](#page-81-1) shows the distortions.

Symmetrical Fault Voltage Output in dq Frame

Figure 5.33: [GFM](#page-1-2) Output Voltages in dq0 Frame

As seen in Figure [5.33,](#page-81-1) both control methods in the islanded mode demonstrate significantly superior characteristics compared to the [G-C](#page-1-5) mode, especially in the post-fault period. The output voltages on the d-axis for both methods are identical, except for the first 20 ms after the fault, and they reach their nominal values within approximately 200 ms without any saturation in the inner control loop. The absence of a strong grid allows the [GFM](#page-1-2) to operate more smoothly. Another interesting point is the change on the q-axis during the fault, which is not observed in the same configuration in [G-C](#page-1-5) mode. This change is due to the lack of control over the voltage reference in current magnitude saturation control and the absence of an external strong grid reference. However, considering the output voltage, both control methods perform excellently within the limits of the Dutch [GC](#page-1-4) even under the most severe fault conditions.

When examining the voltage and current for phase A in Figure [5.34,](#page-82-0) this becomes clearer. The voltage and current graphs are identical for both control methods (except for the first 5 ms during the fault), with almost no overshoot in voltage values (1.09 p.u.). The same applies to the current graph, where the current value is successfully limited to 1.25 p.u. for both control methods. Additionally, synchronization problems seen in [G-C](#page-1-5) mode immediately after the fault are not observed here, and the current value decreases linearly to its nominal value within 50 ms.

Figure 5.34: Voltage and Current Outputs of Inverters

As observed in the output power and frequency graphs in Figure [5.35,](#page-83-0) the situation remains the same. The inverter output active powers are nearly identical, with minor differences, and exhibit stable behavior during and after the fault. Both inverters provide reactive power support to the grid, and the sudden reactive power spike after the fault is due to the abrupt increase in [PCC/](#page-1-9)filter capacitor voltage. However, this condition returns to the nominal value within 25 ms. The frequency graph also shows similar behavior to the [G-C](#page-1-5) mode. Thanks to the inertia provided by the [VSG](#page-2-2) controller, the frequency output exhibits superior performance, returning to its nominal value more gradually. The frequency peak values range between 50.32 Hz and 49.7 Hz, but these variations are within the limits permitted by the Dutch [GC.](#page-1-4)

Lastly, as shown in Figure [5.36,](#page-83-1) the output powers are illustrated when the voltage controller is not reset after a fault for the [CMS](#page-1-3) approach. Similar to the [G-C](#page-1-5) mode, although control is not completely lost, the voltage control loop of both controllers experiences saturation post-fault, lasting approximately 400 ms. This saturation can be clearly seen in both active and reactive power outputs. It takes about 800 ms for the output power to reach its nominal value completely. Synchronization is achieved by the end of this period, so fault detection might not be triggered, but resetting the system provides a much better response and should be applied.

As mentioned in the [G-C](#page-1-5) mode section, the controller can be reset quickly when the [PCC](#page-1-9) voltage exceeds 0.85 p.u. While this detection can be implemented very rapidly, any minor delays it might introduce have not been considered in this simulation.

Figure 5.35: Inverter Power and Frequency Outputs

Figure 5.36: Power Outputs of Inverters without Fault Detection

5.2.2.2 [FRT](#page-1-0) with [VI](#page-2-1)

As shown in Figure [5.37a,](#page-84-0) when the [VI](#page-2-1) is applied, the voltage outputs of both controllers during and after the fault are identical. In this situation, the change observed in the q-axis with the [CMS](#page-1-3) is not present, and except for the 10 ms intervals at the beginning and end of the fault, the [GFM](#page-1-2) remains completely stable. It is clear that the performance of the [VI,](#page-2-1) which makes changes to the voltage references, yields better results than the direct current magnitude intervention applied by the [CMS.](#page-1-3) Figures [5.37b](#page-84-0) and [5.37c](#page-84-0) also show that the [GFM](#page-1-2) outputs work almost flawlessly, as seen from the voltage and current graphs. During the fault, a pure sine wave is maintained, and the high-frequency distortions observed in

the [G-C](#page-1-5) mode are not present here. The maximum voltage peak remains around 1.05 p.u., and the current is successfully limited to 1.25 p.u. It is also noteworthy that the current output reaches the nominal value within just one period after the fault.

Figure 5.37: Inverter Voltage and Current Outputs

On the other hand, from Figure [5.38a](#page-85-0) and [5.38b](#page-85-0) examining the power outputs reveals that the active and reactive power outputs are identical for both control methods. Active power is delivered to the system with high quality, without any distortion or fluctuation, and the provision of reactive power support during the fault is evident. The significant point here is that the [VI](#page-2-1) approach does not require any fault detection or inner controller reset.

In terms of frequency response, the superiority of the [VSG](#page-2-2) control, consistent with previous results, is noticeable. The inverse relationship between power and frequency after the fault is highlighted in Figure [5.38c.](#page-85-0) The frequency values range between 50.27 and 49.9 Hz, which falls within the permissible limits. While the [VSG](#page-2-2) control reaches the nominal value within 0.1 seconds after the fault, it takes approximately 0.8 seconds for the droop control. However, overall, the superiority of the [VI](#page-2-1) controller over the [CMS](#page-1-3) is also evident in this context.

Figure 5.38: Inverter Power and Frequency Outputs

5.2.3 Asymmetrical Faults

In this section, only a [SPG](#page-2-0) and [PP](#page-1-1) fault will be examined. The same microgrid configuration as in the [G-C](#page-1-5) mode will be analyzed, and to differentiate between fault intensities compared to the symmetrical fault, the fault resistance is set at $735 \text{ m}\Omega$. In the case of a ground fault, the ground resistance is set at $0.5 \text{ m}\Omega$. When no [FRT](#page-1-0) method is applied, the load voltages in the dq frame are provided in Figure [5.39.](#page-86-0) The aim here is to observe the load during a fault without an [FRT](#page-1-0) control, thus only the Droop-controlled [GFM](#page-1-2) is simulated. However, the results are similar for [VSG.](#page-2-2)

Similar to the [G-C](#page-1-5) mode, inevitable 100 Hz negative sequence component-based oscillations are observed in islanded mode. In the absence of the [FRT](#page-1-0) method, the peak value in the d-axis is approximately 0.2 p.u. higher compared to when the [FRT](#page-1-0) method is applied. This situation is problematic concerning the Dutch [GC,](#page-1-4) which stipulates a maximum voltage value of 1.1 p.u. The same difference is clearly visible in the oscillations of the q-axis. Another important point here is the stability that the [FRT](#page-1-0) method brings to the microgrid in the post-fault period. Without the [FRT](#page-1-0) method, it takes 0.13 seconds for the axes to reach their nominal values after a fault on both axes. However, with the [FRT](#page-1-0) method, this takes only 0.03 seconds, a significant improvement that is crucial for system reliability and potential future amendments to the Dutch [GC.](#page-1-4)

Examining the output voltage and current graphs of the [GFM](#page-1-2) in the ABC frame

Figure 5.39: Load Voltages in dq0 Frame

prior to the implementation of the [FRT](#page-1-0) is highly beneficial for understanding the [GFM'](#page-1-2)s behavior. As seen in Figure [5.40a,](#page-86-1) the voltage graph reveals that, from the moment the [PP](#page-1-1) fault occurs, the peak voltage value in the healthy phase rises to approximately 1.25 p.u. and remains at that level until the fault is cleared. This condition can lead to small sparks and, in the worst-case scenario, fires within the inverter due to arc formation. Furthermore, the voltage waveform deviates significantly from a sinusoidal shape, exhibiting substantial distortions that severely compromise the quality of the power supplied. As previously discussed in Figure [5.39,](#page-86-0) the voltage imbalances at the load are also evident here. The distortions and overshoots in the voltage wave persist for 1.3 seconds.

The current graph, from Figure [5.40b](#page-86-1) shows that one of the faulty phases, phase A, peaks at 3 p.u. in the first cycle and stabilizes at around 2.22 p.u. Similarly, the other faulty phase, phase B, peaks at around 1.9 p.u. Considering that the same fault resistance is used, it can be inferred from the current peak graphs that the [PP](#page-1-1) fault is less severe compared to the 3-phase fault. After the fault, the current value takes about 1.3 seconds to return to its nominal level, during which effective current support is not provided.

Figure 5.40: Voltage and Current Outputs of Inverters

5.2.3.1 [FRT](#page-1-0) with [CMS](#page-1-3)

When examining the inverter output voltage under a [SPG](#page-2-0) fault in the dq frame as shown in Figure [5.41,](#page-87-0) 100 Hz components are observed throughout the fault duration, similar to what is observed in the [G-C](#page-1-5) mode. During the first 40 ms after the fault onset, the inner control loop fails to track the provided references, and the [GFM](#page-1-2) cannot provide stable support to the microgrid. Both controllers experience similar disturbances. Subsequently, control resynchronizes, and both controllers exhibit similar behavior. The only difference between the controllers is observed in the post-fault period. Although both controllers reach their nominal value within 25 ms after the fault ends, the transition is smoother for the [VSG.](#page-2-2) Besides, it can be stated that the inverters yield much more stable results compared to the [G-C](#page-1-5) mode. The 100 Hz component disturbances observed in the [G-C](#page-1-5) mode are much more orderly in the islanded mode. Additionally, the 700 Hz harmonics that persist for 25 ms post-fault are not observed here.

Figure 5.41: GFM Output Voltages in dq0 Frame

When examining the [GFM](#page-1-2) output in the ABC frame as shown in Figure [5.42,](#page-88-0) it is evident that there are both advantages and weaknesses compared to the [G-C](#page-1-5) mode. In the voltage waveform, overshoots not observed in the [G-C](#page-1-5) mode are around 1.11 p.u. during the fault in the islanded mode. However, some distortions that occur in the initial 40 ms of the fault are much more severe in the [G-C](#page-1-5) mode. Additionally, the oscillations in the faulty phase and distortions in the healthy phase seen in the [G-C](#page-1-5) mode are not present here. The sudden voltage increase of 1.3 p.u. at the fault clearing instance also does not occur in islanded mode. In the current graph, the strength of the islanded mode is evident. Although the peak value at the fault initiation is slightly more severe compared to the [G-C](#page-1-5) mode (1.7 p.u. vs. 1.5 p.u.), the current waveforms quickly return to nominal values after the first cycle and remain stable. The distortions and imbalances seen in the [G-C](#page-1-5) mode are not observed in the islanded mode. Minor differences in current magnitudes can be seen in the current graph, but both are within acceptable limits. Overall, they exhibit similar behavior in the post-fault period.

Figure 5.42: [SPG](#page-2-0) Fault Inverter Outputs in ABC Frame

Figure 5.43: [SPG](#page-2-0) Fault Inverter Power and Frequency Outputs

As shown in Figure [5.43a](#page-89-0) and [5.43b,](#page-89-0) the power outputs in the islanded mode are far from being chaotic, unlike in the [G-C](#page-1-5) mode. After the initial 30-40 ms period observed in the voltage and current waveforms, both controllers provide similar outputs, and the power graph is sinusoidal. The only notable point is that [VSG](#page-2-2) slightly outperforms Droop in reactive power support. The steady-state achievement times are identical between the controllers and consistent between [G-C](#page-1-5) and islanded modes.

The frequency graph in Figure [5.43c](#page-89-0) reiterates the familiar pattern of [VSG'](#page-2-2)s superiority over the Droop controller. The frequency variation during and after the fault period favors [VSG](#page-2-2) due to its higher inertia. However, the absence of a strong grid, when compared to the [G-C](#page-1-5) mode, is evident in the peak frequency values. For instance, in the same configuration, the instantaneous frequency value in the islanded mode for the Droop control is 1.2 Hz higher. This highlights the critical importance of frequency regulation and support in islanded mode. Lastly, the disturbance effects of the strong grid on [GFMs](#page-1-2) are also evident in this figure. When the post-fault is examined, it is crystal clear that the [GFMs](#page-1-2) succeed in staying more stable in islanded mode and oscillations are not experienced.

Overall, it is observed that [CMS](#page-1-3) alone does not fully meet the desired requirements of Dutch [GC.](#page-1-4) Although it performs better in current limitation for both controllers in the islanded mode compared to the [G-C](#page-1-5) mode, the out-of-limit voltage overshoots render the

[CMS](#page-1-3) insufficient.

5.2.3.2 [FRT](#page-1-0) with [VI](#page-2-1)

When examining the [GFM](#page-1-2) output for a [PP](#page-1-1) fault in the dq frame (Figure [5.44\)](#page-90-0), it is observed that both controllers exhibit approximately the same behavior in the d-axis. In the q-axis, minor differences in peak values are noted, but these differences are not significant enough to impact performance.

Figure 5.44: [GFM](#page-1-2) Output Voltages in dq0 Frame

It is useful to compare the fault initiation and recovery phases of both controllers in the islanded mode with those in the [G-C](#page-1-5) mode. In the [G-C](#page-1-5) mode, the initial distortion lasts for only 10 ms, while in islanded mode, it persists for more than 40 ms. Additionally, the synchronization time after the fault is significantly longer in the islanded mode compared to the [G-C](#page-1-5) mode. In the [G-C](#page-1-5) mode, this duration is approximately 20 ms, whereas in islanded mode, it extends to 70 ms. This indicates that while grid connection provides additional inertia that can have negative effects on the [GFM,](#page-1-2) it also aids in the synchronization and steady-state achievement of [GFMs](#page-1-2) under severe fault conditions.

Figure [5.45](#page-91-0) shows that both controllers produce similar output voltage and current waveforms in islanded mode. Despite the [VI](#page-2-1) approach reducing the voltage peaks during faults, it fails to keep them below 1.1 p.u. Voltage peaks for both controllers range between 1.2 and 1.25 p.u., which exceeds permissible limits. Post-fault, the current waveforms struggle to return to nominal values, as previously discussed. Both current and voltage waveforms experience significant distortions during the fault, similar to those observed in the [G-C](#page-1-5) mode, indicating that the [GFM](#page-1-2) faces challenges throughout the fault duration.

In the power output graphs shown in Figure [5.46,](#page-92-0) the [VSG](#page-2-2) controller has a slight advantage in reactive power support, but the power waveforms' oscillations compromise power quality, making it unstable and inconsistent. The active power graphs for both controllers display similar characteristics, with the post-fault recovery being noticeably worse in islanded mode. After the fault, power output in islanded mode continues to

Figure 5.45: [PP](#page-1-1) Fault Inverter Outputs in ABC Frame

Figure 5.46: [PP](#page-1-1) Fault Inverter Power and Frequency Outputs

oscillate at 100 Hz. The frequency response also shows a slight superiority of the [VSG](#page-2-2) controller, similar to the previous section, but it should be emphasized that frequency variations are more pronounced in the islanded mode compared to the [G-C](#page-1-5) mode.

Therefore, when the [VI](#page-2-1) approach is applied alone, the [GFM](#page-1-2) ride-through capability failed for both controllers during the fault condition. Moreover, contrary to the superiority of [VI](#page-2-1) observed over the [CMS](#page-1-3) configurations from previous sections, [VI](#page-2-1) performed worse in this configuration. Therefore, as shown in the next section, a hybrid approach is necessary.

5.2.3.3 [FRT](#page-1-0) Hybrid Approach

When the hybrid approach is used, as clearly indicated in Figure [5.47,](#page-93-0) the post-fault process settles to nominal values more quickly for both fault types. This is particularly evident in the [PP](#page-1-1) fault. Although the results for the [SPG](#page-2-0) fault are approximately the same as the case that only [CMS](#page-1-3) is used, the fluctuations observed in the [PP](#page-1-1) fault are mitigated and additionally reducing the chaotic output at the beginning of the fault by half. However, when compared to the [G-C](#page-1-5) mode, the post-fault synchronization process is still longer, and the 100 Hz components are more unbalanced.

Figure 5.47: Inverter Voltage Outputs in dq Frame for Both Faults

When analyzing the voltage and current waveforms in the natural frame provided in Figure [5.48](#page-94-0) for [SPG](#page-2-0) fault, the voltage overshoots observed in the single [FRT](#page-1-0) approach are successfully reduced below 1.1 p.u. However, as seen in the dq graph, the distortion in the voltage waveform continues throughout the first two fault cycles. In the [VSG](#page-2-2) graph, both faulty and healthy phases appear as pure sine waves, while the droop control exhibits slight distortions. At the end of the fault, the [VSG](#page-2-2) voltage graph is smoother. In the current graphs, except for the first cycle, both methods successfully limit the current value. During the first cycle, the peak values of phase A in the [VSG](#page-2-2) control are approximately 0.2 p.u. higher than in the droop control, but this is negligible since it only lasts for one cycle. The current graphs for both control methods show a smooth transition to nominal values. Compared to the [G-C](#page-1-5) mode, the voltage waveform shows worse performance at the beginning of the fault in the islanded mode but better results at the end of the fault. The current peaks of 1.5-1.7 p.u. observed in islanded mode are not seen in [G-C](#page-1-5) mode. Apart from these differences, it can be stated that the current and voltage successfully rides through the [SPG](#page-2-0) fault.

The [PP](#page-1-1) fault graphs are shown in Figure [5.49.](#page-95-0) As is typical in islanded mode, the voltage and current graphs for both control methods are quite similar. The voltage in the healthy phase is limited to 1.1 p.u. and is sinusoidal. The initial severe distortion lasts only for half a cycle. At the end of the fault, there is an overshoot of around 1.16 p.u. in the voltage of phase B, lasting 5 ms, which can be considered negligible due to its short duration. On the other hand, the current graphs also show positive results. The current values are successfully limited to below 1.25 p.u., preventing damage to the inverter. Compared to the [G-C](#page-1-5) mode, the high-frequency distortion and higher peak values at the end of the fault in the voltage waveform are much smoother in islanded mode. In terms of current behavior, the results are quite similar to the [G-C](#page-1-5) mode.

For both faults, the power graphs in Figure [5.50](#page-96-0) indicate that considering the [SPG](#page-2-0) fault, the [VSG'](#page-2-2)s active and reactive power outputs are more stable compared to those of the droop control. In the [VSG,](#page-2-2) after 50 ms, the stable power output oscillates at 100 Hz and remains stable until the end of the fault. However, fluctuations are observed in the droop control. It is also evident that the [VSG](#page-2-2) has an advantage in reactive power support. In the case of the [PP](#page-1-1) fault, the power outputs of both control methods are quite similar. The fluctuations observed in the droop control during the [SPG](#page-2-0) fault are not present in the [PP](#page-1-1) fault. In both fault scenarios, the power values reached nominal values

Figure 5.48: [SPG](#page-2-0) Fault Inverter Outputs in ABC Frame

Figure 5.49: [PP](#page-1-1) Fault Inverter Outputs in ABC Frame

in approximately 40 ms. It can be said that the resynchronization process is similar for both control methods in both fault conditions. Compared to the [G-C](#page-1-5) mode, the fault recovery process in the islanded mode is smoother. The remaining parameters are quite similar to those in the [G-C](#page-1-5) mode.

Figure 5.50: Power Outputs Under Both Faults

As shown in Figure [5.51,](#page-97-0) although the frequency deviation in the [PP](#page-1-1) fault is greater due to the severity of the fault, the frequency variation in both faults remains within the permissible limits. During the first 100 ms of the fault, the [VSG](#page-2-2) exhibits more unstable behavior; however, subsequently and during the post-fault period, it demonstrates superior characteristics. When compared to the [G-C](#page-1-5) mode, it is evident that the frequency deviation is significantly higher (more than 1 Hz) in the absence of a strong grid.

As a result, it can be observed that even in the case of severe asymmetric faults, the controls applied to the [GFMs](#page-1-2) have successfully provided the necessary grid frequency and voltage support while also protecting against excessive voltage and current levels. Based on the obtained results, the performances of both control methods and [FRT](#page-1-0) approaches will be discussed in the following sections.

Figure 5.51: Inverter Frequency Outputs for Both Faults

5.3 Interoperability of [GFMs](#page-1-2)

In this section, the positive and negative impacts of [GFM](#page-1-2) controllers on each other will be examined when their primary controllers are the same or different. Figure [5.1](#page-54-0) illustrates a second inverter with a capacity of 10 kVA connected to the microgrid. This section will be analyzed under three separate configurations: both [GFMs](#page-1-2) controlled by Droop controllers, both [GFMs](#page-1-2) controlled by [VSG](#page-2-2) controllers, and one [GFM](#page-1-2) controlled by Droop while the other is controlled by [VSG.](#page-2-2) Only symmetric faults and load changes are simulated in this section. However, it should be noted that similar results are obtained for asymmetric faults as well. Additionally, both the [G-C](#page-1-5) and the islanded modes are applied in the same simulation. Figure [5.52](#page-97-1) provides the output powers of the inverters in a microgrid where two [GFMs](#page-1-2) and two [GFLs](#page-1-6) are connected, allowing the reader to comprehensively understand this section.

Figure 5.52: Microgrid Inverters Output Powers

Figure 5.53: [GFM](#page-1-2) Output Powers

As indicated in the figure, the two graphs displayed one above the other show the active power (blue line) on the top and the reactive power (red line) on the bottom. To emphasize each action in the microgrid, the graph in the top left is numbered. Accordingly, the simulation starts in the [G-C](#page-1-5) mode and a 3-phase symmetric fault occurs at point 1 (second 1.5). Then, at point 2 (second 3), the transition from the [G-C](#page-1-5) mode to the islanded mode occurs, followed by a load increase at point 3 (second 4). Finally, at point 4 (second 5), a 3-phase fault occurs in the islanded mode. It is worth noting that, as this is not the main focus of the thesis, the behavior of [GFLs](#page-1-6) will not be further examined in this section. However, since the simulation uses a strong grid when [GFMs](#page-1-2) operate stably, both [GFLs](#page-1-6) provide full capacity active power support and maintain stable operation during and after faults.

5.3.1 Droop-Droop Configuration

To keep the analysis straightforward, this section will focus solely on power outputs. During fault conditions, the inverter output currents are successfully limited to 1.25 p.u, and the voltage peak level is below 1.1 p.u. In Figure [5.53](#page-98-0) ,the output power shown is belong to the same converter, the blue line represents the output power of [GFM1](#page-1-2), while the red line also shows the output power of [GFM1](#page-1-2) when [GFM2](#page-1-2) is connected to the system.

It is worth noting that in the simulations under this section, the [CMS](#page-1-3) is applied as the [FRT](#page-1-0) approach. In the scenario with 1 [GFM](#page-1-2) (a 20 kVA [GFM](#page-1-2) and 2 units of 10 kVA [GFL\)](#page-1-6), a total load of 30 kW and 2 kVAr is initially present, with an additional load of 8 kW and 2 kVAr are added at second 4. When a second 10 kVA [GFM](#page-1-2) is connected, the system starts with 35 kW and 3 kVAr, and the load increase is 12 kW and 3 kVAr. These values are determined based on the capacities of the [GFMs](#page-1-2) to see the same output power level in the same [GFM](#page-1-2) to be able to compare two configurations. In the case of equal load sharing among [GFMs](#page-1-2) in p.u. terms, for example, for 0.5 p.u., the first [GFM](#page-1-2) would supply 10 kW, and the second [GFM](#page-1-2) 5 kW. The remaining 20 kW would be supplied by the [GFLs](#page-1-6). As suggested by the simulation's initial clue, adding an extra [GFM](#page-1-2) to the system also means adding inertia, resulting in a slightly delayed steady-state achievement. In the 3-phase fault scenario under the [G-C](#page-1-5) mode, although the effect is not as pronounced as in islanded mode, the frequency support provided by the inverter results in a smaller drop in active power level. This demonstrates the increased frequency support in the system, particularly in islanded mode. After the fault and during the transition, the system with 1 [GFM](#page-1-2) reaches steady-state more linearly, while the linearity is slightly disturbed in the 2 [GFM](#page-1-2) configuration. However, the time to reach a steady state remains the same.

In the reactive power graph, the commonly mentioned reactive power sharing error in the literature is observed. This deviation, approximately 0.03 p.u., is compensated by the other [GFM.](#page-1-2) The reactive power or voltage support during the fault is clearly in favor of the 2 [GFM](#page-1-2) configuration in this graph. This once again proves that a second [GFM](#page-1-2) in the system can effectively contribute to voltage regulation. However, the disturbances observed at the fault's end and during the transition to islanded mode are also seen in the reactive power graph.

As a result, when each inverter is controlled with droop control, the system response improves in terms of active-reactive power support when multiple inverters operate together. However, the behavior during fault conditions and transition moments is worse compared to a single [GFM](#page-1-2) scenario and is open to further improvement.

5.3.2 [VSG-VSG](#page-2-2) Configuration

Under this section, only power outputs will be examined once again. The [VI](#page-2-1) is applied as the [FRT](#page-1-0) approach, and the load amount and changes are as described in the previous section as the capacities of the [GFMs](#page-1-2) are the same. In Figure [5.54a'](#page-100-0)s active power graph, the additional inertia provided by [VSGs](#page-2-2) results in a longer time to reach steadystate at simulation start compared to droop control, and even longer with two [VSGs](#page-2-2) than with one [VSG.](#page-2-2) This increased system inertia slows down the frequency response, which in turn affects the rate of change of active power due to the inherent active powerfrequency relationship in control. The difference between one [VSG](#page-2-2) and two [VSGs](#page-2-2) is more pronounced compared to the droop control discussed earlier, further highlighting the inertia benefit of [VSGs](#page-2-2).

During fault conditions, the response differs between configurations. With one [VSG,](#page-2-2) the active power graph remains stable without oscillations, whereas with two [GFMs](#page-1-2), there is approximately a 0.05 p.u. oscillation, indicating degraded output current quality and susceptibility to high-frequency harmonics. This results in poorer power quality compared to the single [GFM](#page-1-2) configuration. Post-fault and transition periods also show that while the time to reach nominal values may be similar, the presence of sudden peaks and oscillations indicates weaker overall power performance in the two [GFM](#page-1-2) configurations.

Examining the reactive power graph in Figure [5.54b,](#page-100-0) there is more deviation in reactive power sharing in the [G-C](#page-1-5) mode compared to droop control, but this issue is absent in islanded mode. Post-fault, the two [GFM](#page-1-2) configuration also shows a delay in reaching nominal values with sudden peaks observed during this process. Contrary to the active power graph, the two [VSG](#page-2-2) configuration exhibits weaker performance in terms of reactive power support compared to the single [VSG](#page-2-2) configuration.

In conclusion, especially when compared to droop control, operating [VSGs](#page-2-2) together during fault conditions results in poorer power quality. Although they provide frequency support, the quality of provided active and reactive power is lower than that of the single [GFM](#page-1-2) configuration. Finally, their responses during post-fault and transition periods are also inferior.

Figure 5.54: [GFM](#page-1-2) Output Powers

5.3.3 Droop[-VSG](#page-2-2) Configuration

In this section, unlike the previous two sections (the same [GFM](#page-1-2) response investigation under single or multiple [GFM](#page-1-2) operation), the behavior of both [GFMs](#page-1-2) will be examined simultaneously. The load profile remains the same as in the previous sections, and both [FRT](#page-1-0) methods investigated in this thesis will be analyzed for each configuration. Figures [5.55](#page-101-0) and [5.56](#page-102-0) present the active and reactive power graphs for each [FRT](#page-1-0) configuration. In the figures, blue lines represent the droop control responses while red lines show the [VSG](#page-2-2) outputs. It is worth noting that the voltage and current values are within the accepted limit throughout all configurations under this title. Therefore, these graphs will not be illustrated.

From the active power graphs, the first notable point is that the [VSG](#page-2-2) reaches its nominal value more slowly at the beginning of the simulation compared to the droop control. This, as previously mentioned, is due to the additional inertia it provides. Another prominent point is the power-sharing of active power. In the [G-C](#page-1-5) mode, the power shares are fixed at 0.6 p.u., so regardless of the load condition, both the droop-controlled and [VSG-](#page-2-2)controlled [GFMs](#page-1-2) deliver the expected output. However, as soon as it transitions to the islanded mode, the power-sharing does not correspond to the capacities of the [GFMs](#page-1-2) but draws equal amounts of power. Considering that the droop-controlled [GFM](#page-1-2) has a capacity of 10 kVA and the [VSG-](#page-2-2)controlled [GFM](#page-1-2) has a capacity of 20 kVA, approximately 0.8 and 0.4 p.u. of active power are drawn, respectively, indicating an equal amount of power according to the [GFM](#page-1-2) capacities. If this power-sharing issue is not addressed, it may lead to decreased efficiency, differing lifetimes for the [GFMs](#page-1-2), and other complications. It is worth mentioning that the main goal of this thesis is to investigate the mutual effects of the [GFMs](#page-1-2), therefore, rectifying the power-sharing issue will remain for future work. Naturally, this power-sharing error is not influenced by the application of different [FRT](#page-1-0) approaches.

Additionally, in the [CMS-CMS](#page-1-3) configuration, during the 3-phase fault in the [G-C](#page-1-5) mode, the [GFMs](#page-1-2) produce the same results at the moment of fault, while post-fault, the droop controller returns to its nominal value very smoothly, whereas a short-term current spike is observed in the [VSG](#page-2-2) controller, causing a power surge. Later, although there is a power sharing error in the transition, both [GFMs](#page-1-2) transition softly to the islanded mode. In the case of a load increase, again, a sharing error is observed. This time, the

Figure 5.55: [GFM](#page-1-2) Output Active Powers for Different [FRT](#page-1-0) Configurations

Figure 5.56: [GFM](#page-1-2) Output Reactive Powers for Different [FRT](#page-1-0) Configurations

droop controller experiences an increase of approximately 0.05 p.u., while the [VSG](#page-2-2) sees an increase of 0.125 p.u., which is another point to be considered.

In the fault condition in islanded mode, the results are even more interesting. At the moment of fault, the power level drops for both controllers, but after the fault, in a 20 ms period, the droop controller's active power value decreases to -0.5 (indicating active power absorption or charging), while the [VSG'](#page-2-2)s active power spikes to 1.36 p.u. These sudden changes in current and voltage and, therefore, in power flow direction can shorten the lifespan of the [GFMs](#page-1-2) and lead to damage. In the [VI-VI](#page-2-1) situation, both [GFMs](#page-1-2) also exhibit disturbances in power output during the fault condition, as seen in the previous section. In the subsequent processes post-fault, the characteristics of the controllers differ from each other, although their settling times are the same.

The load increase sharing fault becomes even more pronounced here. In the droop controller, the power increase is approximately 0.07 p.u., while in the [VSG,](#page-2-2) it is 0.25 p.u. The disturbances in power outputs following the load change are another notable point. This disturbance is more pronounced in the droop controller, but it arises due to the lower current drawn, as increased capacity enhances controller robustness.

One of the key points is that in the [VI-VI](#page-2-1) configuration, the active power flow direction change is absent. This can be noted as the greatest advantage of this configuration. Power levels drop to the same level during the fault, while in the post-fault process, both controllers exhibit similar characteristics. In the [CMS-](#page-1-3)[VI](#page-2-1) configuration, during the fault, both [CMS](#page-1-3) and [VI](#page-2-1) responses are similar to their own characteristics observed so far from the previous sections. This indicates that the [FRT](#page-1-0) controllers do not influence each other at the moment of fault. However, after the fault, especially in the droop controller where [CMS](#page-1-3) is applied, the power surge increases significantly. This surge is also seen in the [VSG,](#page-2-2) and for both [GFMs](#page-1-2), the settling time increases by approximately 200 ms.

While similar results are obtained during transitions and load changes, in the postfault process in islanded mode, the droop controller again shows a change in power flow direction, although this change is not as severe as in the [CMS-CMS](#page-1-3) case. Power surges occur in opposite directions for both controllers, and settling times increase. From these results, it can be concluded that using two different [FRT](#page-1-0) approaches simultaneously is not recommended.

On the other hand, when analyzing the reactive power graphs, the power-sharing error is only observed in the [CMS-CMS](#page-1-3) case in the [G-C](#page-1-5) mode and up to the load increase in islanded mode. In all other cases, power sharing is identical for both [GFMs](#page-1-2). In the [CMS-CMS](#page-1-3) case, in the [G-C](#page-1-5) mode, the [VSG](#page-2-2) provides more reactive power support, while in islanded mode, the reactive power support is more limited. Furthermore, in post-fault situations, the droop controller yields more dramatic results. Generally, these results indicate that the droop controller is weaker in such operations. This weakness of the droop controller is also evident in the [VI-VI](#page-2-1) configuration. In the [VI-VI](#page-2-1) case, in the [G-C](#page-1-5) mode, both controllers produce the same results regarding reactive power support. In this respect, [VI](#page-2-1) appears to outperform [CMS](#page-1-3) control. However, in islanded mode, there is no reactive power support. The superiority of the [VSG](#page-2-2) controller in the post-fault process is evident here. During the load change, the disturbance in the droop controller is significantly greater compared to the [VSG.](#page-2-2) When examining the reactive power sharing, no sharing error is observed either. This indicates that when [VI](#page-2-1) is utilized in the system, this condition is achieved. In this configuration as well, the post-fault process with the applied [CMS](#page-1-3) droop controller yields more dramatic results. Notably, in the islanded mode during the post-fault process, power peaks fluctuate between 1.5 and -0.6 p.u., which, as

previously mentioned, can be detrimental to the inverter.

In conclusion, although there are fewer issues in the reactive power graphs compared to the active power outputs, it is evident that the use of [VSG-](#page-2-2)droop requires further investigation and improvement.

5.4 Dutch Grid Code Match & Discussion

In this section, it will be discussed whether the findings and results obtained in the previous sections comply and best match with the Dutch [GC](#page-1-4) standards.

First, Table [5.57](#page-104-0) provides a table summarizing the behavior under load variations for both control methods. As observed from the table, the reactive power sharing error in the droop control method is smaller compared to its predecessor [VSG.](#page-2-2) This is expected, as the droop control method takes the droop characteristics of [SGs.](#page-2-3) However, this powersharing error naturally appears in 1 [GFM](#page-1-2) configuration only operating in the [G-C](#page-1-5) mode. In Islanded mode, since the [GFM](#page-1-2) is the sole reactive power provider (with the [GFLs](#page-1-6) are designed as grid feeders with $P = 1$ p.u., $Q = 0$ p.u.), this error is not expected to be observed.

On the other hand, the [VSG](#page-2-2) control method, which is based on the swing equations of [SGs,](#page-2-3) is superior to the droop controller in providing inertia (J) and damping (D). However, it is weaker in terms of droop characteristics. It is worth noting that the control parameters for both controllers are selected to be optimal for all conditions. For example, in the droop controller, the P-f and Q-V droop values are set to 1 $\%$ and 4 $\%$, respectively, while in the [VSG](#page-2-2) controller, the $J\omega_0$ and D/ω_0 values are set to 0.25 and 10. These values are determined through trial and error. Different values might yield more optimal results under different conditions, but as indicated, these values provided the best results across all conditions.

| | Load Change | | | | | | | | |
|-----------------------|---|---|--|--|--|--|--|--|--|
| | Droop | VSG | | | | | | | |
| Grid Connected | 1) Small Reactive Power Share Error 2) Faster Response 3)Soft Transition | 1) Large Reactive Power Share Erro 2) Realtively Slow Response 3)Soft Transition | | | | | | | |
| Islanded | 1) No Reactive Power Share Error 2) Faster Response 3)Soft Transition | 1) No Reactive Power Share Error 2) Relatively Slow Response 3)Soft Transition | | | | | | | |

Figure 5.57: Load Change Comparison Table

For instance, increasing the J value and decreasing the D value in the [VSG](#page-2-2) control resulted in easier loss of angle stability post-fault, while the opposite adjustment led to quicker loss of synchronization or larger oscillations during faults. The lack of inertia in the droop controller allows for faster responses, making its step responses consistently quicker than those of the [VSG.](#page-2-2) This difference is evident during load changes as well. However, both controllers manage to maintain frequency values within the limits specified in the Dutch [GC,](#page-1-4) as shown in Figure [3.6,](#page-25-0) without exceeding these values or losing synchronization during load shedding or uptake. In summary, both controllers meet the

desired performance criteria under load variations. The choice between them can be made based on system requirements, such as the need for fast response or high inertia/low [Ro-](#page-1-10)[CoF.](#page-1-10)

In Table [5.58,](#page-106-0) a comparative summary of the two primary control methods in both [G-C](#page-1-5) and Islanded modes under symmetric and asymmetric faults, with different [FRT](#page-1-0) approaches, is presented based on the results obtained from the previous sections. The comparison criteria (KPIs) are determined according to IEEE standards and the Dutch [GC.](#page-1-4) For ease of understanding, each comparison is divided into two columns under the name of an [FRT](#page-1-0) approach, with sections for Droop and [VSG](#page-2-2) control methods. To succinctly summarize the importance of KPIs, peak voltage and current limit are crucial for the safe operation of [IBRs](#page-1-7) without causing damage. The [RoCoF](#page-1-10) and reactive power support are stipulated as essential attributes for a [GFM](#page-1-2) in the Dutch [GC](#page-1-4) and IEEE standards. These characteristics are vital for the proper functioning of individual electronic devices poared by the grid and for maintaining grid operability during islanding conditions. Additionally, the post-fault behavior of a [GFM](#page-1-2) indicates the effectiveness of its control mechanisms. Following severe faults, the [GFM](#page-1-2) should be capable of maintaining synchronization and rapidly returning to nominal values. The power quality during faults is crucial for assessing the support provided to the grid in such scenarios. Lastly, evaluating whether a [GFM](#page-1-2) requires fault detection is also important, as [GFMs](#page-1-2) that do not necessitate detection can perform their tasks more swiftly without any delays.

As seen from the figure, under symmetric faults, the voltage and current values in all configurations remain within the Dutch [GC](#page-1-4) limits and the inverter's current carrying capacity, and both controllers provide similar reactive power support. However, as previously noted, synchronization issues post-fault are more pronounced in the [G-C](#page-1-5) mode when [GFMs](#page-1-2) are connected to a strong grid, as in our thesis $(SCR = 8)$ $(SCR = 8)$. The [VSG](#page-2-2) control method shows better results in the [G-C](#page-1-5) mode compared to the droop control method. These issues do not arise in Islanded mode, and both control methods softly restore synchronization post-fault.

Regarding the [RoCoF,](#page-1-10) the [VSG](#page-2-2) method performs better in both operational modes, with the frequency range either changing within a narrower frame or remaining more stable, which can be advantageous for the system and connected loads, especially electronic devices. Besides minor differences between [FRT](#page-1-0) approaches under symmetric faults, the only notable difference is the presence of fault detection. In the [CMS,](#page-1-3) the inner voltage controller needs to be reset post-fault, requiring feedback on the fault occurrence. Although this feedback can be provided quickly (e.g., sending a reset signal to the PI controller as soon as the [PCC](#page-1-9) voltage drops below 0.85 p.u. or rises above it), minor delays can lead to transient overcurrents or voltage controller saturation. This varies with the speed of the control or the fault's severity, but in this simulation, the most severe fault allowable under the Dutch [GC](#page-1-4) without tripping the inverter (0.15 p.u. voltage level - 200 ms) is simulated without any fault detection delay. Therefore, the [VI](#page-2-1) approach's lack of detection requirements gives it an edge in symmetric faults. It is also worth mentioning that both control methods and [FRT](#page-1-0) approaches provide good results during the fault, delivering high-quality active and reactive power support to the system.

The results for asymmetric faults are generalized and provided collectively for both simulated asymmetric faults. The first notable point is that regardless of the [FRT](#page-1-0) approach used, neither approach meets the voltage peak and current limit requirements when employed individually (with the current limit being exceeded in the [CMS](#page-1-3) approach, and both voltage and current limits being exceeded in the [VI](#page-2-1) approach). Exceeding these

| | | Symmetrical | | | | Asymmetrical | | | | | |
|-----------------------|---|----------------|----------------|----------------|----------------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | KPIs | 3 Phase Fault | | | Phase-Ground & Phase-Phase | | | | | | |
| | | CMS | | VI | | CMS | | VI | | Hybrid | |
| | | Droop | VSG | Droop | VSG | Droop | VSG | Droop | VSG | Droop | VSG |
| Grid Connected | Voltage peak | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark | X | X | \checkmark | \checkmark |
| | Current Limit | \checkmark | ✓ | \checkmark | ✓ | X | x | X | X | ✓ | ✓ |
| | RoCoF | Worse | Better | Worse | Better | Worse | Better | Similar | Similar | Worse | Better |
| | Reactive Power Support | Similar | Similar | Similar | Similar | Similar | Similar | Similar | Similar | Better | Worse |
| | Post-Fault | Worse | Better | Worse | Better | Similar | Similar | Similar | Similar | Similar | Similar |
| | Harmonics & Quality* | Good | Good | Good | Good | Bad | Bad | Bad | Bad | Good | Good |
| | Fault Detection | Yes | Yes | No | No | Yes | Yes | No | No | Yes | Yes |
| Islanded | Voltage peak | \checkmark | \checkmark | \checkmark | \checkmark | X | X | X | X | ✓ | \checkmark |
| | Current Limit | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark | X | X | \checkmark | \checkmark |
| | RoCoF | Worse | Better | Worse | Better | Worse | Better | Worse | Better | Similar | Similar |
| | Reactive Power Support | Similar | Similar | Similar | Similar | Worse | Better | Worse | Better | Worse | Better |
| | Post-Fault | Similar | Similar | Similar | Similar | Worse | Better | Similar | Similar | Worse | Better |
| | Harmonics & Quality* | Good | Good | Good | Good | Bad | Bad | Bad | Bad | Good | Good |
| | Fault Detection | Yes | Yes | No | No | Yes | Yes | No | No | Yes | Yes |
| | $*$ During the Fault $\sqrt{ }$ Within the Limit. X Out of the Limit | | | | | | | | | | |

Figure 5.58: Primary Control and [FRT](#page-1-0) Comparison Table

limits necessitates the immediate disconnection of the inverter without providing any grid support, thereby failing to meet the frequency and voltage support requirements specified in the Dutch [GC.](#page-1-4)

Additionally, if only one [FRT](#page-1-0) method is used and the inverter is not disconnected, the power injected into the grid is far from being of high quality, containing high-frequency distortions and harmonics that can permanently damage sensitive devices on the load side. The [CMS](#page-1-3) method also requires fault detection in such cases. Despite the fact that the [VSG](#page-2-2) control method has an advantage in terms of [RoCoF,](#page-1-10) it is clear that the inverter cannot operate healthily under these conditions. In terms of reactive power support during the fault and behavior post-fault, both primary control methods provide similar results, with the [VSG](#page-2-2) method showing an advantage in islanded mode.

As a result, since neither [FRT](#page-1-0) method alone meets the requirements under asymmetric faults, hence, both methods are applied simultaneously in the controllers. The results obtained clearly indicate that the outcomes are promising. The voltage and current values remain within the permissible limits, and the voltage and current support provided is free from additional distortion (except 100 Hz negative sequence components). In the hybrid mode operation, the [VI](#page-2-1) approach engages when the inverter output current exceeds 1 p.u. However, if the predefined [VI](#page-2-1) value is insufficient based on the fault type or severity and the current exceeds 1.25 p.u., the [CMS](#page-1-3) method should then be incorporated into the loop. Therefore, fault detection is also necessary in this case. By doing so, the controllers do not saturate at the onset of the fault, and the voltage and current waveforms are generated healthily, allowing the inverter to successfully ride through the fault.

These results indicate that while a single [FRT](#page-1-0) approach is sufficient for symmetric faults, the desired outcomes under asymmetric faults can only be achieved by applying both [FRT](#page-1-0) approaches in the controller. Additionally, it is evident that the [VSG](#page-2-2) controller generally yields more favorable results compared to the droop controller. However, it is worth reiterating that the differences between the two methods allow either to be used as a control method based on the requirements of the [DNOs.](#page-1-11)

Lastly, the results from the interoperability of the inverters are provided in Table [5.59.](#page-107-0) As seen in the table, the table is divided into two sections: Section I and Section II. In Section I, the results compare the performance of the same inverter when another [GFM](#page-1-2) inverter is added to the system, relative to when it is operating alone. In other words, the results for the same inverter are compared to its previous performance in isolation. In Section II, the results provide a comparative analysis of Droop and [VSG-](#page-2-2)controlled [GFMs](#page-1-2) operating simultaneously under the same microgrid conditions together. For example, the comparison of a Droop [CMS-CMS](#page-1-3) configuration with a VSG [CMS-CMS](#page-1-3) configuration is summarized in the table. It is important for the reader to understand this comparison to avoid any confusion. Additionally, for the interoperability criteria, expectations and the results obtained are used to establish different comparison criteria, as depicted in the figure. These criteria are essential for evaluating the performance and interaction of different inverters under various conditions. To elaborate on the defined KPIs, the settling time indicates how quickly an inverter reaches its nominal value during a black start situation, which can be critical according to [DNOs.](#page-1-11) Additionally, the behavior of [GFMs](#page-1-2) during the [G-C-](#page-1-5)islanded transition is an important criterion for comparative analysis. Harmonics, post-fault, and reactive power support, as previously mentioned KPIs, are essential parameters in determining the superiority of [GFMs](#page-1-2) relative to one another. Moreover, analyzing power sharing among [GFMs](#page-1-2) is crucial due to their different characteristics, affecting both the quality of the power supplied and the lifespan of the [GFM](#page-1-2) (as continuous overloading can shorten its life). Finally, the Sudden Active Power Direction Change (SAPDC) is added to the KPIs based on the results obtained in this thesis and is significant for the health of [GFMs](#page-1-2).

| | | Droop-Droop | VSG-VSG | | | | Droop-VSG | | | |
|--|-------------------------------|----------------|-----------------|----------------|-----------------|-----------------|----------------|-----------------|----------------|--|
| | KPIs | Droop | VSG | Droop | | | VSG | | | |
| | | CMS-CMS | $VI - VI$ | CMS-CMS VI-VI | | CMS-VI | CMS-CMS VI-VI | | CMS-VI | |
| Grid Connected | Settling Time | Slower | Slower | Faster | Faster | Faster | Slower | Slower | Slower | |
| | Transition | Worse | Worse | Similar | Similar | Similar | Similar | Similar | Similar | |
| | Harmonics & Quality* | Similar | Worse | Similar | Similar | Better | Similar | Similar | Worse | |
| | Post-Fault | Worse | Worse | Better | Worse | Similar | Worse | Better | Similar | |
| | Reactive Power Support | Better | Worse | Worse | Smilar | Similar | Better | Smilar | Similar | |
| | Power Share Error** | Small | Large | Small | No Error | No Error | Large | No Error | No Error | |
| | SAPDC | No | No | No | No | No | No | No | No | |
| Islanded | Settling Time | Slower | Slower | Faster | Faster | Faster | Slower | Slower | Slower | |
| | Transition | Worse | Worse | Similar | Similar | Similar | Similar | Similar | Similar | |
| | Harmonics & Quality* | Similar | Worse | Similar | Similar | Better | Similar | Similar | Worse | |
| | Post-Fault | Worse | Worse | Worse | Similar | Worse | Better | Similar | Better | |
| | Reactive Power Support | Better | Similar | Similar | Similar | Similar | Similar | Similar | Similar | |
| | Power Share Error** | Small | No Error | Similar | Better | Better | Similar | Worse | Worse | |
| | SAPDC | No | No | Yes | No | Yes | No | No | No | |
| * During the Fault. **For reactive power, SAPDC: Sudden Active Power Direction Change | | | | | | | | | | |

Figure 5.59: Interoperability Comparison Table

As can be clearly understood, due to the difference in provided inertia, the settling time for [VSG](#page-2-2) control is slower in every scenario. Moreover, as the number of [GFMs](#page-1-2) in a microgrid increases, the settling time increases for both primary controls, with a more significant impact observed in [VSG.](#page-2-2) This indicates that each additional [GFM](#page-1-2) contributes to the total system inertia. When an additional droop-controlled [GFM](#page-1-2) is added to a system already having a droop-controlled [GFM,](#page-1-2) as shown in the figure, negative results are observed during transitions from [G-C](#page-1-5) mode to islanded mode and post-fault. It should be noted that only the [CMS](#page-1-3) control is applied to both droop controllers. These results are consistent with the synchronization issues between high inertia [GFMs](#page-1-2) and strong grid sides frequently mentioned in the literature. While the quality of power supplied to the grid remains unchanged, the reactive power support increases as expected. The powersharing error is minimal due to the nature of the droop controller. All these characteristics
are the same in both [G-C](#page-1-0) and islanded modes of this configuration.

In the [VSG-VSG](#page-2-0) configuration, the results differ slightly, with the droop control showing superior performance in this regard. When a second [VSG](#page-2-0) is added to a system with an existing [VSG,](#page-2-0) the quality of the power injected and the post-fault process yields worse results. Another important point is that, since the [VI](#page-2-1) approach is used in both [VSG](#page-2-0) controllers, the increasing [VI](#page-2-1) value affects the system dynamics. Therefore, for robust and reliable control, it might be important to apply adaptive [VI](#page-2-1) based on the system condition during the design phase. The only difference observed in the results between [G-C](#page-1-0) and islanded modes for this configuration is the power-sharing error. This error is significant in the [G-C](#page-1-0) mode, while there is no load-sharing error in the islanded mode.

In the Droop[-VSG](#page-2-0) configuration, all [FRT](#page-1-1) approach configurations are simulated. When the [CMS](#page-1-2) approach is applied to both [GFMs](#page-1-3), they show similar results. There are differences in the post-fault process and reactive power support, but these differences are both advantageous and disadvantageous for the [GFMs](#page-1-3), making it difficult to assert the superiority of either [GFM.](#page-1-3) However, it is noted that the droop controller exhibits more significant active power transients during the post-fault process compared to the [VSG,](#page-2-0) causing the inverter to absorb power for a brief period of 20-30 ms instead of supplying it. This is undesirable as these rapid changes in power flow direction can lead to spikes and consequently arcing in the filter capacitance. Since the droop controller has a weaker inertia characteristic than the [VSG,](#page-2-0) frequency and therefore active power changes occur more rapidly.

When the [VI](#page-2-1) is applied to both [GFMs](#page-1-3), the first notable point is the absence of the power-sharing error seen in the [CMS-CMS](#page-1-2) configuration. This indicates that applying the [VI](#page-2-1) to [GFMs](#page-1-3) can contribute to power-sharing or droop characteristics in the [G-C](#page-1-0) mode. However, in islanded mode, this situation favored the droop controller. Another important point is the deterioration in power support observed during the fault due to the changes in system dynamics brought by [VI.](#page-2-1) This situation, not seen in the [CMS-CMS](#page-1-2) setup, affects the performance of the inner control PI controllers due to the change in the total system impedance. Using adaptive [VI](#page-2-1) could potentially solve this problem.

In the case where both [FRT](#page-1-1) methods are used, the most prominent observation is the significant active power share error among the [GFMs](#page-1-3). As stated in the previous section, this problem is the most problematic case for interoperability of Droop- [VSG](#page-2-0)controlled inverters. On the other hand, sudden active power flow direction changes in the droop controller. These changes, ranging from 0.5 p.u. to -0.5 p.u., are only observed in the [CMS](#page-1-2) method. This issue should be considered during control design. On the other hand, parameters such as power quality and transitions, which had shown similar results previously, varied with different [FRT](#page-1-1) methods. However, when the [VI](#page-2-1) is used, it is again observed that there is no reactive power-sharing error in the [G-C](#page-1-0) mode, indicating that using the [VI](#page-2-1) in one of the [GFMs](#page-1-3) is sufficient to eliminate this error.

In summary, it is clear that [GFMs](#page-1-3) of the same type working together yield better results compared to when different types of [GFMs](#page-1-3) are used together. This is particularly evident in droop-controlled [GFMs](#page-1-3) due to the inherent droop characteristic. The issues observed in [VSG](#page-2-0) should be addressed and improved. When different types of inverters are connected, it especially leads to power-sharing errors and post-fault process concerns. Control systems in such operations should pay special attention to these aspects.

Chapter 6 Conclusion & Future Work

The rapid increase in renewable energy sources such as [PVs](#page-1-4) and [WTs](#page-2-2) within microgrids has significantly heightened the interest in the control of [IBRs.](#page-1-5) Efforts to enhance the performance of these devices have led to the growing popularity [GFMs](#page-1-3). However, the requirements for such devices vary from country to country, and their lack of inertia and susceptibility to overcurrent present significant challenges. Although the literature contains numerous studies aimed at improving these controls, a comprehensive study examining different types of [GFMs](#page-1-3) in both [G-C](#page-1-0) and islanded modes, under various fault conditions and employing different [FRT](#page-1-1) methods, is lacking to the best of our knowledge.

Therefore, in this thesis, the two most prevalent [GFM](#page-1-3) control methods in the current literature, namely droop control and [VSG](#page-2-0) control, are modeled in detail. They are compared in both the islanded and the [G-C](#page-1-0) modes, under symmetric and asymmetric fault conditions, using the two most common and mature [FRT](#page-1-1) methods [—CMS](#page-1-2) and [VI](#page-2-1) according to the Dutch [GC.](#page-1-6) Additionally, the interoperability of identical and different types of [GFMs](#page-1-3) operating simultaneously in the same microgrid is also examined.

The outputs obtained from the simulations are presented below in accordance with the research questions of this thesis.

1) What are the behaviors of differently controlled [GFMs](#page-1-3) under different fault conditions in a microgrid system?

Based on the results obtained, it is evident that both primary control methods (Droop and [VSG\)](#page-2-0) achieve the expected characteristics of a [GFM,](#page-1-3) such as ride-through during faults, reactive power support, and high-quality power output. However, they exhibit differences in certain aspects. For instance, the [VSG](#page-2-0) controller clearly outperforms the Droop control in terms of [RoCoF](#page-1-7) and inertia, resulting in a slower step response compared to Droop. Additionally, [VSG](#page-2-0) has demonstrated superior performance in post-fault scenarios. However, it is also evident that, in normal operation mode, the reactive power sharing error in [VSG,](#page-2-0) due to its inherent Droop characteristic, is significantly higher than that in the Droop control. Therefore, when designing a [GFM,](#page-1-3) considerations must be given to [VSG'](#page-2-0)s slower step response and reactive sharing error, while attention should be paid to the inertia deficit and post-fault behavior associated with Droop control. It is important to emphasize that although each control method has its advantages over the other, the results obtained with both are compliant with the Dutch [GC.](#page-1-6) Thus, depending on system requirements, the [DNOs](#page-1-8) can choose either method, considering the parameters mentioned above. It is also worth noting that the effectiveness of both controllers is highly dependent on the parameters used during the control process. It has been observed that parameters applied through a trial-and-error approach do not work under all conditions and may lead to a loss of control in [GFMs](#page-1-3). Therefore, during the design of the controller, system transfer functions should be derived, and parameters should be calculated accordingly.

2) How can the behavior of inverters be improved with different [FRT](#page-1-1) approaches?

It has been observed that both methods used as [FRT](#page-1-1) approaches [\(CMS](#page-1-2) and [VI](#page-2-1) have

their own distinct advantages and disadvantages. In the case of balanced faults, both methods successfully prevent overcurrents and help achieve a high-quality output signal. However, one of the most critical aspects is that the [CMS](#page-1-2) method requires fault detection in all situations, which gives the [VI](#page-2-1) method a slight advantage in this regard. Nevertheless, the [VI](#page-2-1) method's addition of impedance to the system, even if virtual, alters the system dynamics, resulting in lower output signal quality during faults (with oscillations of 0.05 p.u.) compared to what is achieved with [CMS.](#page-1-2) Therefore, an adaptive [VI](#page-2-1) impedance design may be necessary in sensitive situations. This issue was also clearly observed in interoperability simulations, where the power output distortion was higher in [GFMs](#page-1-3) using [VI](#page-2-1) during load changes. However, in cases where [CMS](#page-1-2) was used, a long-term active power flow reversal, which could lead to detrimental effects on the [GFM,](#page-1-3) was also observed. Under asymmetrical fault conditions, it was found that both [FRT](#page-1-1) approaches experienced difficulties in ensuring the [GFM'](#page-1-3)s ride-through capability (current limitation in [CMS,](#page-1-2) and both voltage and current limitations in [VI\)](#page-2-1). Consequently, both control methods were applied simultaneously under the hybrid approach, and the presence of both methods in the controller yielded positive results, successfully enabling the operation of [GFMs](#page-1-3). Hybrid approach also is one of the contribution of this thesis.

3) Are these control methods (droop or [VSG](#page-2-0) with mentioned [FRT](#page-1-1) approaches) appropriate designs for microgrids operating under both islanded[/G-](#page-1-0)[C](#page-1-0) modes and do they comply with the Dutch [GC?](#page-1-6)

As observed from the simulations, both control methods provided very similar responses in islanded mode and remained within the voltage and frequency limits specified by the Dutch [GC.](#page-1-6) Thanks to the synchronization and restoration processes applied in the secondary control, the transitions between the two modes were smooth and seamless. Although the post-fault process in [G-C](#page-1-0) mode was slightly poorer, the results still remained within acceptable limits. In conclusion, both inverters are compliant with the Dutch [GC](#page-1-6) in both modes, and their superiority relative to each other can be determined based on factors such as post-fault behavior and step response.

4) Can the same and different types of [GFMs](#page-1-3) be interoperated in the same microgrid? If so, is it a suitable choice for the Dutch [GC?](#page-1-6)

The results indicate that each [GFM](#page-1-3) added to the system contributes to the system's overall inertia, which consequently slows down the step response. Additionally, it can be stated that operating Droop controllers together presents the least problematic configuration. Besides the inertia contribution, the reactive power sharing error is minimal, and the post-fault behavior shows relatively less deterioration. Overall, the results suggest that Droop controllers can operate together within the same microgrid.When multiple ['VSGs](#page-2-0) are operated together, the post-fault outcomes are worse compared to when Droop controllers are used. Moreover, the reactive power sharing error is more significant. Nevertheless, if necessary, multiple [VSGs](#page-2-0) can still be operated together since the results obtained are compliant with the Dutch [GC,](#page-1-6) though the negative aspects discussed in this thesis should be carefully considered. On the other hand, operating different types of inverters simultaneously is problematic. The errors in active power sharing could lead to shorter inverter lifespans. Moreover, severe oscillations in power output after faults are significantly more intense compared to previous configurations, and long-term (up to 50 ms) sudden changes in active power flow direction have been observed, which could have harmful effects on the inverters. In conclusion, based on the results obtained, it is feasible to operate inverters of the same type together, while operating different types of inverters simultaneously is not recommended.

In summary, it is found that while both control methods yielded satisfactory results under symmetric faults with either [FRT](#page-1-1) method, achieving satisfactory results under asymmetric faults required the simultaneous application of both [FRT](#page-1-1) methods. Furthermore, although the [VSG](#page-2-0) controller, when used alone, showed slight advantages in terms of [RoCoF](#page-1-7) and system stability due to the inertia it provides, it also caused power-sharing errors in joint operations due to its lacking droop characteristics. However, it is evident from the simulated results that the designed [GFMs](#page-1-3), in various configurations, comply with the Dutch [GCs](#page-1-6) requirements with minor differences. Different [GFMs](#page-1-3) can be used for parameters such as step response speed or [RoCoF,](#page-1-7) which can vary according to the demands of [DNOs.](#page-1-8) Issues such as sudden power flow changes, post-fault behaviors, load sharing, and power quality in hybrid [GFM](#page-1-3) systems utilizing [VSG-](#page-2-0)Droop need further development for better performance in such joint operations.

It should be noted that this thesis did not consider the dynamics of energy sources such as irradiation, wind speed, or battery health. Considering these dynamics in future work could make simulation results more realistic. The reactive power-sharing error, which is more pronounced in VSGs, as well as the active power-sharing errors observed in the VSG-Droop configuration, are critical areas for future investigation. Additionally, further research is planned to address eliminating the 100 Hz components that arise during asymmetrical faults. Additionally, in all grid connection scenarios, the microgrid is connected to a strong grid, characterized by a [SCR](#page-1-9) of 8. However, the impact of weak grid conditions is also a subject for future research. Lastly, all simulations are conducted in the MATLAB/Simulink environment. As a next step, Hardware-in-the-Loop (HIL) tests are planned to be conducted. This would allow for the inclusion of controller dynamics and delays, leading to more realistic results.

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