A 1.35 - 8.85 GHz SiGe:C HBT Cryogenic LNA with 45 K Minimum Noise Temperature

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***Abstract*— An impedance matched low-noise 1.35 - 8.85 GHz single stage common emitter amplifier utilizing SiGe:C HBT device simulated at 18 K has achieved 10 ± 0.5 dB of gain (S_{21}) across 3 - 7.5 GHz, and reflection coefficient (S_{11}) less than -15 dB across 4 - 9.5 GHz. The circuit design utilized a SiGe:C HBT (BFP760) model from Infineon Technologies. Due to transistor and simulator limitation, noise matching has not been implemented, resulting in an average noise temperature of 49 K over 5 - 9.5 GHz. The LNA is self-biased using collector feedback biasing to increase stability. Additionally, inductive emitter degeneration has been implemented to improve RF noise performance. This LNA is designed to work as part of amplification chain for Josephson Radiation readout. As a proof of concept, the design demonstrates that it is possible to achieve a gain target of 18.6 dB in the 4 - 12 GHz range at 4 K with a cascade design.**

I. Introduction

In the field of nano-electronics, many experiments have to be conducted in a cryogenic environment, for example quantum computer readout, and cryogenic experiments which operating points are close to quantum limit [1] [2]. In these experiments, electronic signals must be brought to room temperature to be measured. However, the noise level increases as the ambient temperature rises. Therefore, the electronic signals must be amplified by low-noise amplifiers (LNAs) to maintain high Signal-to-Noise Ratio (SNR) from the cryogenic level to room temperature [3] [4].

This paper discusses the design of a single stage low-noise amplifier using common emitter (CE) configuration with Silicon Germanium Carbon (SiGe:C) [5] transistor (Fig.1) to bridge the noise gap between cryogenic-(4 K) and room-temperature(290 K) for signals with frequencies between 4 GHz and 12 GHz [6]. The single stage design serves as a proof of concept and that is the most complicated one to design. More stage can be added in the future with relative ease to increase gain and bandwidth. The motivation for this work is to obtain a higher flexibility in circuit design, as it yields an adjustable model instead of a fixed commercial model. In addition, it allows to be built in a non-industrial environment.

To find out how much amplification is needed to bridge the noise between 4 K and 290 K, the noise temperature equation can be used: [7]

$$\frac{P_n}{B}[WHz^{-1}] = k_b T_n \tag{1}$$

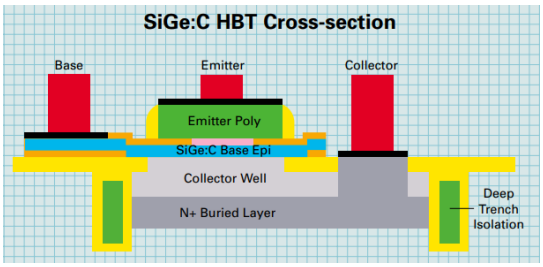

Fig. 1. Cross Section of a SiGe:C HBT; the SiGe base layer (blue) is carbon-doped; Emitter Poly represents polysilicon [5]

where,

- P_n is the noise power of the system (W),
- B is the amplifier bandwidth (Hz),
- k_b is the Boltzmann constant ($1.38 \cdot 10^{-23}$ J/K),
- T_n is the noise temperature of the system (K).

From eq.1, the equivalent noise voltage in root-mean-squared amplitude could be found: [8]

$$\frac{\bar{v}_n^2}{B}[V^2 Hz^{-1}] = 4k_b R T_n \tag{2}$$

$$v_{n,rms}[V] = \sqrt{4k_b R T_n B} \tag{3}$$

where R is the resistive part of the component's impedance. From eq.3, the noise voltage ratio between 290 K and 4 K is approximately 8.5 (or 18.6 dB).

However, there will be additional noise provided by the amplifier which can be minimized through noise matching the LNA [9]. Below are the equations of the amplifier noise factor, F [9] [10]:

$$F = F_{min} + \frac{N}{R_s R_{opt}} |Z_{opt} - Z_s|^2 \tag{4}$$

$$F = F_{min} + \frac{4R_n}{|1+\Gamma_{opt}|^2} \frac{|\Gamma_{opt} - \Gamma_s|^2}{1 - |\Gamma_s|^2} \tag{5}$$

In eq.4, $Z_s = R_s + jX_s$ is the signal-source impedance; $Z_{opt} = R_{opt} + jX_{opt}$ is the LNA's optimum signal-source impedance for minimum noise, respectively. In eq.5, R_n is the noise resistance; Γ_{opt} is the optimum reflection coefficient; Γ_s is the signal-source reflection coefficient.

Eq.4 shows that the LNA could achieve a minimum noise factor, F_{min} when Z_s = Z_{opt}, where F_{min} is the absolute lowest noise factor a device can achieve at a given operating point (supply voltage and current), frequency and temperature. For example, F_{min} decreases with decreasing frequency and temperature [11].

For the circuit design, the common emitter (CE) configuration has been chosen as it is the better choice to implement a wide band LNA with the lowest possible noise figure compared to a common base (CB) design. A common collector (CC) stage could be beneficial to work as a buffer stage with its high input impedance and low output impedance, but should not be considered to used for signal amplifying, as it has near-unit voltage gain [12]. Although a CB amplifier could achieve a higher gain than a CE amplifier, it has a higher noise resistance R_n, which increases the mismatch factor in eq.5. This leads to a larger transformation ratio from the high output to the low input impedance of the CB stage, and thus result in a narrow band characteristic [10]. So, a CE stage would be more ideal for an amplifier design. The drawback is that due to its low available gain, cascading multiple stages is required to provide a sufficient gain [10].

For the transistor, the SiGe technology has been widely used in LNA design with the target bandwidth and desired gain [13]. For example, a SiGe HBT BFU725A has been used in a LNA design for cryo-RF usage [14], illustrating the potential for this kind of transistors to be used in this field. In this experiment, a similar SiGe:C hetero-junction biploar transistor (HBT) BFP760 [15] was chosen for the LNA design. Compare to SiGe HBT, SiGe:C HBT could have higher maximum oscillating frequency, higher associated gain, and lower minimum noise figure [16]. In addition, simulating different transistors increases the flexibility of circuit design to meet different requirements for amplifiers.

The simulations were done in LTspice. The available spice model of the transistor BFP760 was limited for room temperature simulation, which means the accuracy of the transistor model simulated at cryogenic level cannot be guaranteed. Therefore, the simulation temperature is set to 18 K, which is the minimum temperature at which the transistor model remains linear (A). Besides, simulation results at 290 K are also plotted to provide room temperature performance estimates for future characterization.

To obtain more accurate simulation results, higher level model such as Most EXquisite TRAnsistor Model (MEXTRAM) should be used, as well as higher level simulator, e.g. Advanced Design System (ADS). Due to time constrain, this has been considered as future optimization options.

II. Circuit Design

As explained, the LNA uses a single stage design. The schematic of the SiGe:C LNA is shown in Fig.2. The LNA uses a common emitter (CE) (B) configuration (Q1) and a 5 V supply, with self-biasing (C) provided by R_C and R_B, to provide stability and control the LNA's sensitivity to the transistor current gain β. Additionally, inductor L_{deg} is placed

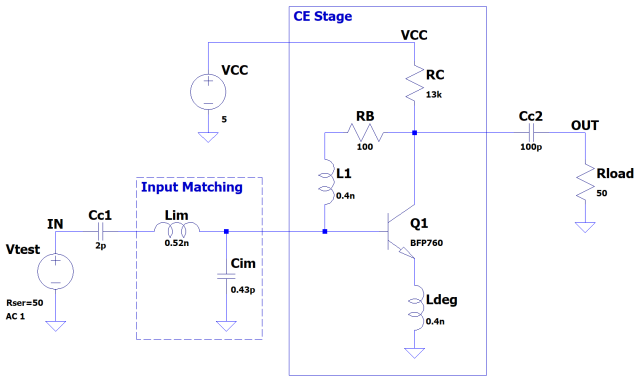

Fig. 2. Schematic of SiGe:C HBT LNA (Common Emitter) with input matching network

at the emitter, providing inductive emitter degeneration (D) to optimize the LNA high frequency noise performance. Next, an L-matching network built with shunt inductor L_{im} and series capacitor C_{im} has been implemented at the amplifier's input, to minimize signal reflection. Besides, an inductor L_1 has been used to decrease the effect of high frequency signals to LNA biasing.

With the self-biasing design, the Kirchhoff's voltage law (KVL) reads:

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0 \tag{6}$$

$$I_C[V] \approx \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}} \tag{7}$$

Eq.7 shows that I_C can be set by R_C when $R_C >> \frac{R_B}{\beta}$, and R_B only controls biasing sensitivity to β. Hence, R_B should be kept small. However, a decreasing R_B increases power consumption. After making trade-off, the value of R_C and R_B have been set (C).

Next, by adding a series inductor L_{deg} to the emitter, the impedance of the transistor increases by $j\omega L_{deg}$. This provides higher impedance at high frequency, leading to noise suppression and better noise performance. However, as the noise is suppressed with signal degeneration, the value of L_{deg} has been set after making trade-offs between gain, noise, and bandwidth (D).

For the LNA, both source and load are 50 Ω. From eq.4, to achieve minimum noise factor, the source impedance Z_s has to match the optimum signal-source impedance Z_{opt}, which is also called "noise-matched". Generally, $Z_{opt} \neq Z_{in}$, which means that just matching the source impedance and the input impedance will not lead to minimum noise. However, a mismatch between Z_s and Z_{in} will increase signal reflections. Hence, trade-offs have to be made, to keep both the noise factor F and the input reflection coefficient Γ_{in} at an acceptable level. The LNA input impedance at 18 K and 290 K before implementing the matching network is shown in Fig.3.

Due to the uncommon operating point (18 K), and limitation of the simulation software (LTspiceXVII), the noise

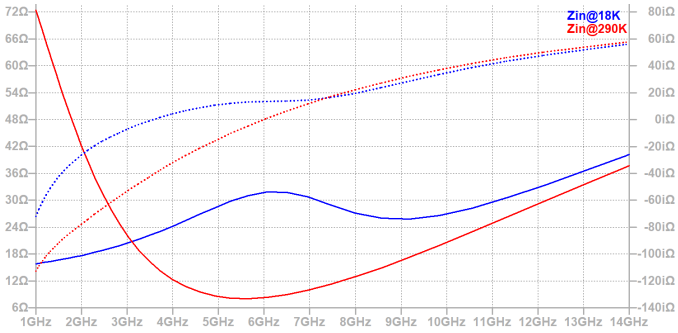

Fig. 3. LNA input impedance at 18 K (blue) and 290 K (red) before matching, solid line represents resistance, dotted line represents reactance.

parameters, i.e. minimum noise factor F_{min}, equivalent noise resistance R_n, and optimum reflection coefficient Γ_{opt} could not be determined. This mean noise matching is not feasible with this simulation setup. In this case, the goal is to achieve a noise figure NF lower than 0.4 dB (or T_n = 28 K), which is approximately the maximum noise figure of reported cryogenic-trend LNA across 1 - 10 GHz [13].

Since noise matching is not feasible in this simulation, it is aimed to achieve impedance matched to minimize input signal reflection (eq.8,9). The input impedance matching network has been designed using Smith chart shown in Fig.4. In the Smith chart tool, the characteristic impedance (Z_0 = 50 Ω), the input impedance of the amplifier, and the operating frequency have been inserted. The initial impedance was located in the upper half (inductive) of the Smith chart (DP1), and was not located on the 50 Ω constant resistance circle. Hence, a shunt capacitor is used to set it on the 50 Ω constant circle (DP2), then a series inductor to set the reactance equals zero (DP3). The matching network is shown in Fig.2.

$$\Gamma_{in} = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \tag{8}$$

$$S_{11}[dB] = 20log_{10}|\Gamma_{in}| \tag{9}$$

As the maximum available current for this transistor at 18 K remains unknown, this LNA uses low current design (B). For high current design, see (G).

III. Simulation & Results

After tuning the design, the LNA performance, especially the S-parameter and noise performance, was simulated at both 18 K and 290 K temperatures. The forward voltage gain S_{21} of the LNA is shown in Fig.5, and the input reflection coefficient S_{11} is shown in Fig.6.

Fig.5 shows that the LNA at 18 K has a relatively flat gain of 10 ± 0.5 dB across 3 - 7.5 GHz, and a 3dB bandwidth of 7.5 GHz (1.35 GHz to 8.85 GHz). At 290 K, the LNA behave as an attenuator (negative gain), indicating the biasing is not suitable for room temperature amplification. Next, from Fig.6, the LNA has input reflection lower than -15 dB across 4 - 9.5 GHz at 18 K. At 290 K, the LNA input reflection coefficient is larger than -9.65 dB (or 33%).

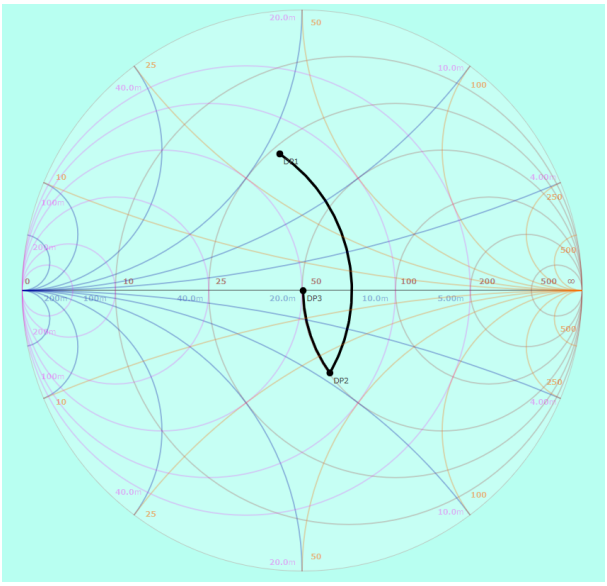

Fig. 4. Smith Chart for input impedance matching (Z_s = 50 Ω)

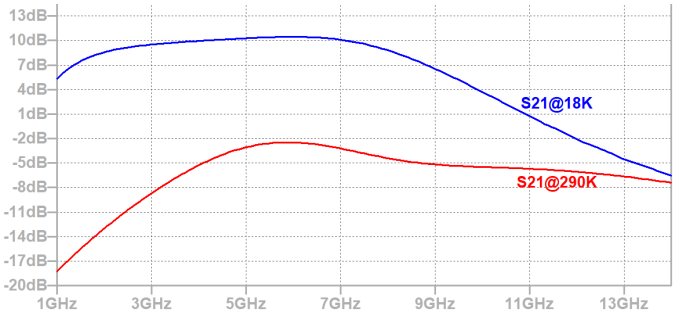

Fig. 5. S_{21} simulated at 18 K (blue) and 290 K (red) across 1 to 14 GHz

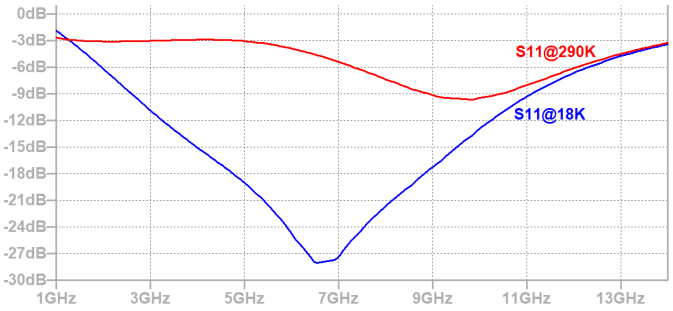

Fig. 6. S_{11} simulated at 18 K (blue) and 290 K (red) across 1 to 14GHz

Next, in Fig.7, the S-parameters (S_{21} and S_{11}) of the LNA before and after implementing matching network at 18 K are shown. From the red and blue trace (S_{21}), it could be concluded that the matching network does not increase the gain or bandwidth by much, as the gain only increased by 0.3 - 0.5 dB across the band of interest. However, the cyan and pink trace (S_{11}) clearly shows that the input matching network significantly decreased the input reflections (eq.8,9), providing at most 17 dB less reflection across the bandwidth,

and resulting in S_{11} < -15 dB across 4 - 9.5 GHz.

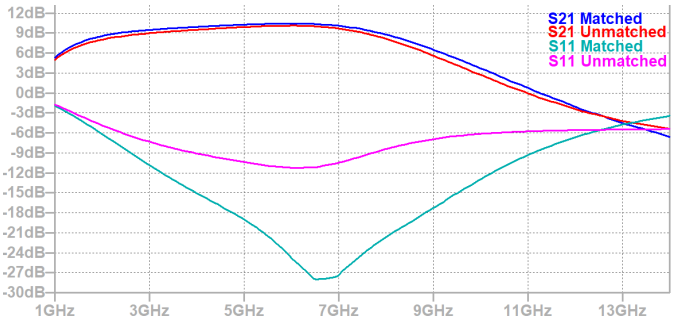

Fig. 7. S_{21} with input matching (blue); S_{21} without input matching (red); S_{11} with input matching (cyan); S_{11} without input matching (magenta)

In Fig.8, noise spectral density of the SiGe:C LNA at 18 K (blue) and 290 K (red) have been shown respectively. In LTspice, the simulation also provides the total RMS noise across the bandwidth of interest by integrating it. For the LNA at 18 K, the total RMS noise $V_{n,rms} = 44.883\ \mu V$; for the LNA at 290 K, $V_{n,rms} = 76.614\ \mu V$. The difference in noise is reasonable as from eq.1, the noise power increases with increasing temperature.

The noise spectral density of noise contributors in the LNA design at 18K are shown in Fig.9. This simulation shows that the feedback resistor R_B and the load R_{load} are main noise contributors to the total noise, while the noise contributed by collector resistor R_C is negligible compared to them. Besides, the transistor is also a main noise contributors, due to its internal resistance. However, it could not be plotted in LTspice. These resistors contribute much noise because their thermal noise (or Johnson–Nyquist noise) has been amplified by the LNA.

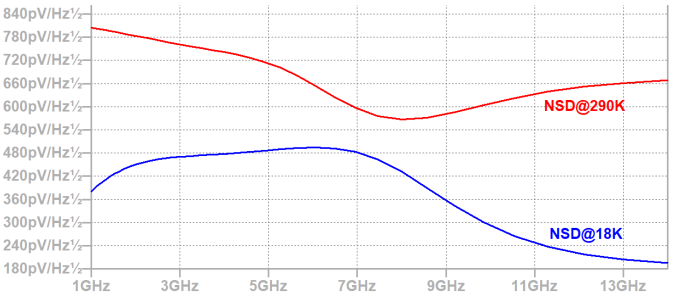

Fig. 8. Noise Spectral Density at 18 K (blue) and 290 K (red)

Fig.10 shows the noise temperature T_n(cyan), noise factor F(magenta), and noise figure NF(red), at 18 K (for 290 K, see (F)). As limited by the transistor modelling level and simulator, i.e. LTspice, the noise parameters could not be determined directly. In this simulation, the noise parameters are determined with indirect methods. First, to simulate the noise temperature, the total RMS noise at 18K ($44.883\ \mu V$) and eq.2 have been used. From eq.3:

$$T_n[K] = \frac{v_{n,rms}^2}{4k_bRB} = \frac{v_{n,rms}^2}{4k_bB}\frac{1}{Re(Z_{in})} \tag{10}$$

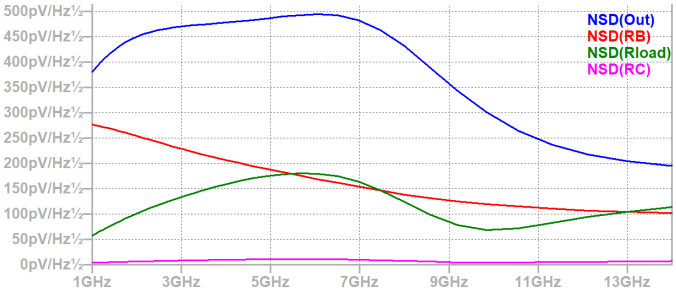

Fig. 9. Output Noise Spectral Density (blue); NSD of R_B (red); NSD of R_{load} (green); NSD of R_C (magenta), at 18 K

Then, the noise factor F and noise figure NF are simulated using equations below:

$$F = 1 + \frac{T_n}{T_0} \tag{11}$$

$$NF[dB] = 10log_{10}(F) \tag{12}$$

where T_0 is the reference temperature, typically 290 K [17]. As noise factor (F) and noise figure (NF) expect input signal is at 290 K, noise temperature (T_n) could be more useful as it shows more directly the noise performance of the LNA [17].

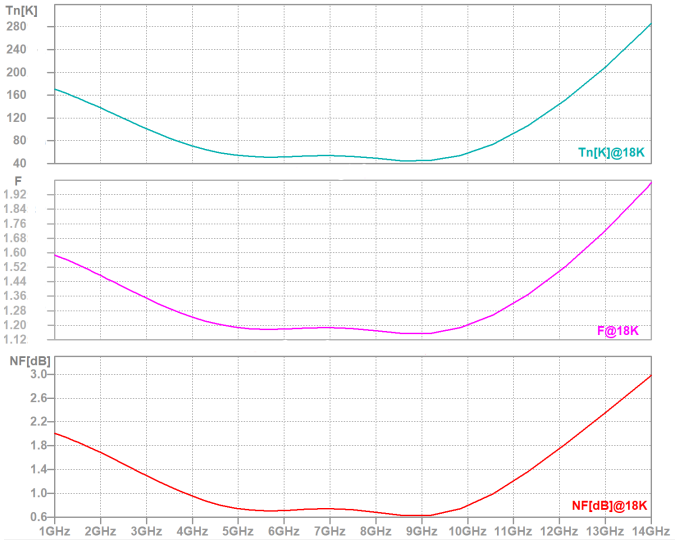

Fig. 10. (i) Noise Temperature T_n, (ii) Noise Factor F, (iii)Noise Figure NF, at 18 K

Fig.10 shows that at 18 K, the LNA achieved a minimum noise temperature of 45 K at 8.6 GHz, and average noise temperature of around 49 K across 5 - 9.5 GHz. The minimum noise figure is 0.63 dB at 8.6 GHz, and average noise figure of around 0.7 dB across 5 - 9.5 GHz. The noise performance does not achieved the goal mentioned in section II (28 K or 0.4 dB). Some reported LNAs achieved minimum noise temperature of 6 K (2 - 12 GHz, operating at 4.2 K, SiGe HBT) [6], 7.7 K (6 - 10 GHz, operating at 77 K, GaAs pHEMT) [18], 4.3 K (3 - 6 GHz, operating at 15 K, SiGe HBT) [19]. By comparison,

the LNA in this work has a worse noise performance. This is expected as noise matching has not been implemented.

IV. Conclusion & Outlook

A SiGe:C HBT common emitter cryo-LNA has been designed to work at 18 K for near-quantum limit signal readout, specifically as part of the amplification chain for Josephson Radiation Measurement [2]. The LNA is simulated in LTspice, at both 18 K and 290 K. At 18 K, the LNA achieved maximum S_{21} of 10.5 dB, 3dB bandwidth between 1.35 GHz and 8.85 GHz. Due to limitation of the transistor model and simulator, noise matching has not been implemented in the LNA. As an alternative, input impedance matching has been done, resulting in S_{11} < -15 dB across 4 - 9.5 GHz. Additionally, at 18 K, the LNA achieved total RMS noise voltage of 44.883 μV, minimum noise temperature of 45 K at 8.6 GHz, and average noise figure of around 0.7 dB across 5 - 9.5 GHz. Note that since the transistor model was made for room-temperature simulations, we tend to retain the possibility of error for simulations at 18 K.

Refering to the goal of the LNA, which was set to be S_{21} > 18.6 dB, 3dB bandwidth of 4 - 12 GHz, and a NF < 0.26 dB, the current LNA design is not sufficient. However, as currently only one transistor has been used, the LNA performance is acceptable, especially it was designed to work as the first stage with low gain, and noise matching was not availble. To achieve the desired goal, multiple methods are considerable. First, a higher level model (e.g. MEXTRAM) and simulator (ADS) could be very helpful in understanding transistor behaviour at different operating points. Next, to achieve wider band and higher gain, cascading multiple sections of the CE amplifier could be the solution [10]. By cascading stages, the gain and bandwidth of each stage add up, while the noise is mainly determined only by the first stage. Additionally, implementing a cascode configuration, which is a common emitter stage feeding into a common base stage, could also be beneficial [20]. A cascode amplifier provides a wider band by reducing the Miller Effect, resulting in higher gain, and better input-output isolation. Future work should focus on better understanding the noise performance of cryogenic SiGe LNA, and try to close the gap with noise-matched design.

After simulations, the schematic of the LNA would be converted into a PCB design using KiCAD. In PCB design, the transmission line design should be focused on, as it has to be 50 Ω, to prevent signal reflection. Additionally, each angle was set to be 45° instead of 90° to prevented reflections, and the maximum available length of the wavegudide has been calculated (E). After fabrication, the LNA would be characterized. First, the S-parameters (S_{21} and S_{11}) of the SiGe:C LNA should be checked using a Vector Spectral Analyzer (VNA). From S_{21}, the maximum gain, gain flatness, and 3-dB gain of the LNA could be known. From S_{11}, how much signal has been transmitted into the LNA can be know. Next, the noise performance of the LNA i.e. noise spectral density, T_n or NF, should also be checked. Afterwards, the thermal stability should also be checked, to study the performance of the LNA on different temperature. This determines the range of temperature which the amplifier could be useful. Last but not least, the biasing stability should also be checked, to learn how stable the operating point is with variations in temperature and supply voltage. These information are useful to keep the transistor in saturation mode, instead of linear mode or breaking down.

V. Acknowledgement

After weeks of hard work, I finally finished my bachelor's thesis project. It was not an easy work, but it was definitely a great learning experience. I have learned a lot of things new during this project, although the result was not perfect.

I encountered a variety of problems during this project. Fortunately, I had a helpful committee. I would like to introduce you to my beloved committee: Dr. Joost Ridderbos, the chair supervisor of my project, Nick Groen, my beloved daily supervisor, and Dr. Anne-Johan Annema, who really helps me to work on the right path. I would like to thank them for their helpful advice and physical and mental support, especially Nick. As a busy PhD student, he did his best to help me overcome various obstacles in my work. He is a funny, active, and responsible person, and I never felt stressed working with him. Besides, Dr. Joost Ridderbos and Dr. Anne-Johan Annema were the key in pushing me to this level. I am very grateful for their efforts and kindness. In addition, I would like to thank everyone I met during my time in the Nanoelectronics group. They are so kind, fun, and supportive. Working and playing with them was an unforgettable experience.

Lastly, during the preparation of this work, I used ChatGPT 4o, Scispace, and DeepL to find and summarize resources, generate explanations for knowledge points, do repeating calculations, sentence rephrasing/optimizing, and spelling check. After using this tool/service, I thoroughly reviewed and edited the content as needed, taking full responsibility for the final outcome.

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[21] Z. Wang, D. Hou, P. Zhou, H. Li, Z. Li, J. Chen, and W. Hong, "A ka-band switchable lna with 2.4-db nf employing a varactor-based tunable network," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 4, pp. 385–388, 2021.

APPENDIX

A. *BFP760 & Simulation Temperature*

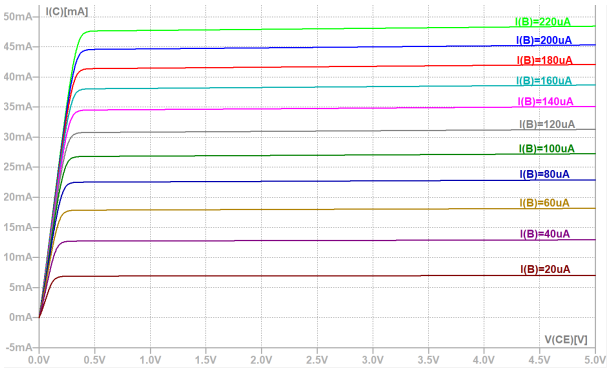

Fig. 11. BFP760 I_C-V_{CE} at room temperature (298 K)

Fig.11 shows the I_C-V_{CE} of the SiGe:C HBT BFP760 at room temperature (298 K). By comparing with BFP760 datasheet [15], it shows that the transistor model is quite match to the datasheet, showing model accuracy at room temperature.

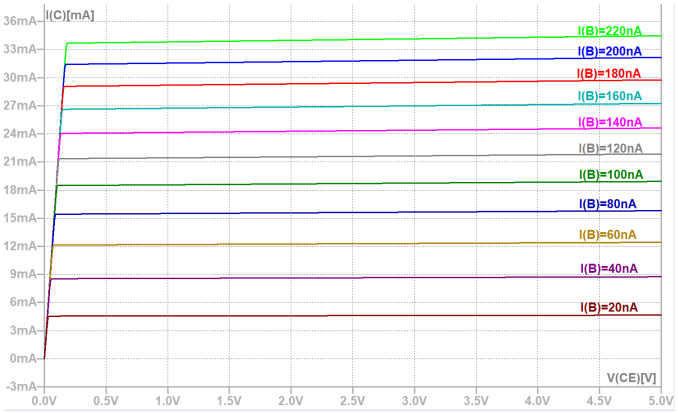

Fig. 12. BFP760 I_C-V_{CE} at 18 K

Fig. 13. BFP760 I_C-V_{CE} at 17 K

To check whether the transistor model can be used for simulation at 4 K, the transistor I_C-V_{CE} curves have been simulated while the temperature is decreasing. Fig.12 shows

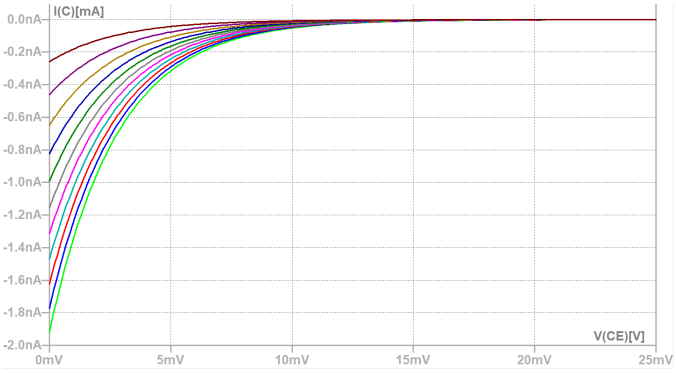

Fig. 14. BFP760 I_C-V_{CE} at 16 K

that at 18 K, the transistor model still behaves linear. However, Fig.13 and Fig.14 shows that at simulation temperature below 18 K, the transistor model is unreliable. Hence, the simulation temperature has been set to 18 K. Since this transistor model was made for room-temperature simulations, the accuracy of the results is not guaranteed.

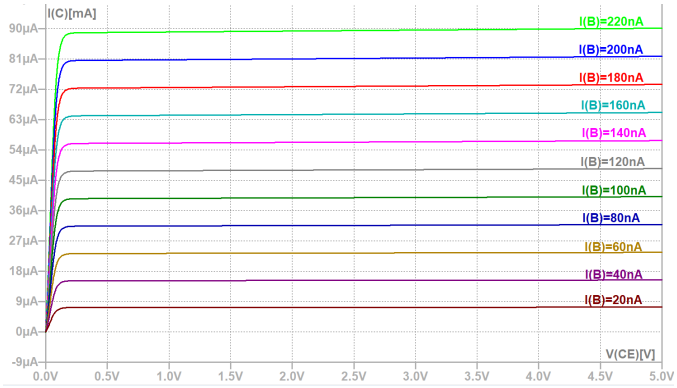

Fig. 15. BFP760 I_C-V_{CE} at 290 K

Fig.15 shows the collector current (I_C) with same array of base current (I_B) as in Fig.12, at 290 K. It shows that I_C at 18 K is much larger than 290 K. From datasheet [15], the maximum available collector current (I_C) at room temperature is around 70 mA. To prevent breaking down transistor, base current should be set sufficiently small.

B. *Common Emitter Configuration*

Common emitter (CE) configuration is a common used transistor amplifier configuration. It is an amplifier with transistor's emitter connected to ground. As a fundamental transistor amplifier design, it is very useful. A CE stage could be beneficial for a LNA, as it could achieve a lower noise than a CB stage [10]. Additionally, although its gain per stage is lower, it can be cascaded with multiple stage, leads to a high gain and wide band LNA. [10].

Fig.16 shows the parameters of transistor in a CE configuration simulated at 18 K. As a low current design, the base current is approximately 1.3 nA, the collector current is approximately 0.3 mA.

```
Name:      q:q1:1
Model:   q1:m_bfp760
Ib:        1.27e-09
Ic:        3.02e-04
Vbe:       1.08e+00
Vbc:       4.77e-07
Vce:       1.08e+00
BetaDC:    2.38e+05
Gm:        1.94e-01
Rpi:       1.25e+06
Rx:        2.90e+00
Ro:        6.88e+05
Cbe:       9.60e-13
Cbc:       6.22e-14
Cjs:       2.10e-13
BetaAC:    2.42e+05
Cbx:       2.67e-14
Ft:        2.94e+10
```

Fig. 16. Parameters of SiGe:C HBT BFP760 under specific bias at 18K

C. *Collector Feedback Biasing*

Collector feedback biasing has been implemented in the amplifier design. With this biasing method, the collector resistor R_C is use to determine the collector current I_C, while the base resistor R_B can be use to decrease the effect of DC current gain β to the amplifier biasing setup. When R_B is sufficiently small, I_C is then determined by R_C (eq.7). While it provides convenient in biasing, it also has drawback, which is the freedom of biasing is lesser (R_C determine both I_C and V_{CE}). As a common biasing method for RF LNA, it has several benefits. First, it only uses two resistor for biasing, thus results in less thermal noise (eq.3). Next, it increases the amplifier stability with the negative feedback (R_B). Besides, the feedback also improved linearity of the amplifier.

Fig.17 shows S_{21} (top), S_{11} (bottom) value when R_C increased from 11 kΩ to 15 kΩ with step of 1 kΩ. At the same time, Fig.18 shows the noise spectral density across different values of R_C.

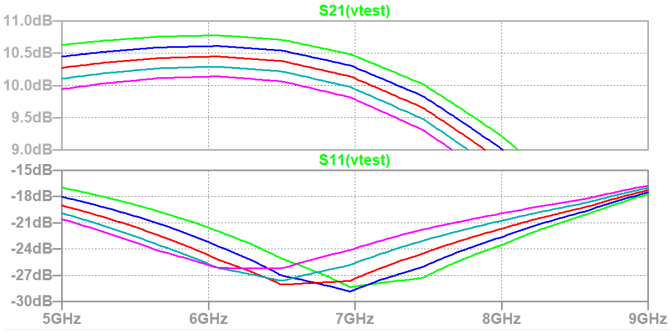

Fig. 17. S_{21}, S_{11} for R_C = 11 kΩ, 12 kΩ, 13 kΩ, 14 kΩ, 15 kΩ

Fig.19 shows S_{21} (top), S_{11} (bottom) value when R_B increased from 50 Ω to 250 Ω with step of 50 Ω. At the same time, Fig.20 shows the noise spectral density across different values of R_B.

By considering LNA's performance in each aspects, it was decided to set R_C = 13 kΩ, R_B = 100 Ω.

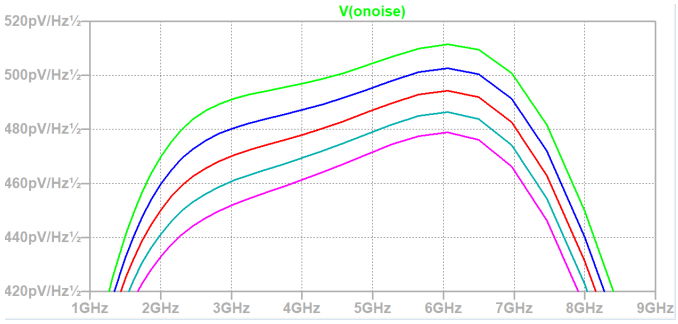

Fig. 18. NSD for R_C = 11 kΩ, 12 kΩ, 13 kΩ, 14 kΩ, 15 kΩ

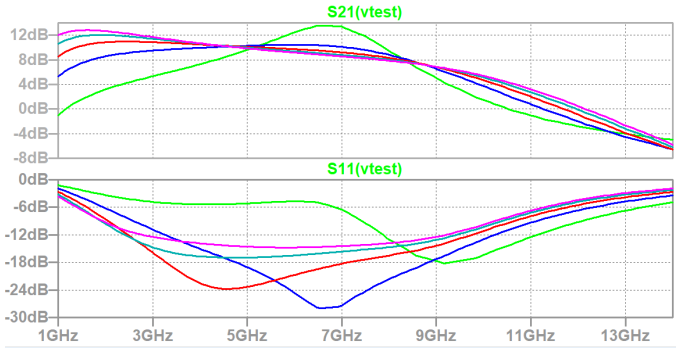

Fig. 19. S_{21}, S_{11} for R_B = 50 Ω, 100 Ω, 150 Ω, 200 Ω, 250 Ω

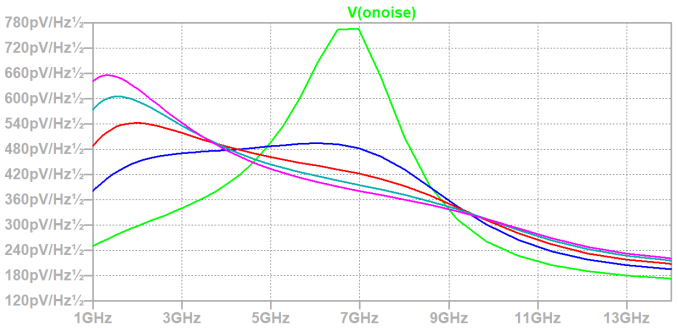

Fig. 20. NSD for R_B = 50 Ω, 100 Ω, 150 Ω, 200 Ω, 250 Ω

D. Noise Optimization

To decrease noise at high frequencies, an inductor L_{deg} is placed between emitter and the ground (Fig.2). This is called inductive emitter degeneration. The value of L_{deg} has to be choose carefully as it decreases high frequency noise by attenuating the signals. Therefore, the LNA frequency response (S_{21}, S_{11}), as well as the noise spectral density, have been plotted with respect to different values of L_{deg}, to make some trade-offs.

Fig.21 shows S_{21} (top), S_{11} (bottom) value when L_{deg} increased from 0.1 nH to 0.5 nH with step of 0.1 nH. At the same time, Fig.22 shows the noise spectral density across different values of L_{deg}. From Fig.21, it shows that the S_{21} is flattest and the S_{11} bandwidth of less than -20 dB is doubled at L_{deg} = 0.5 nH compared to L_{deg} = 0.4 nH . Additionally, the noise has also been decreased. By considering LNA's

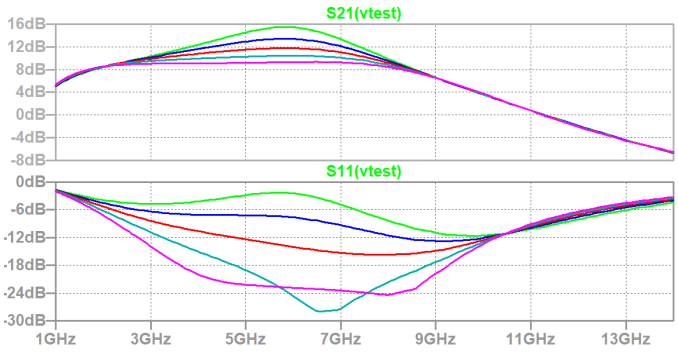

Fig. 21. S_{21}, S_{21} for L_{deg} = 0.1 nH, 0.2 nH, 0.3 nH, 0.4 nH, 0.5 nH

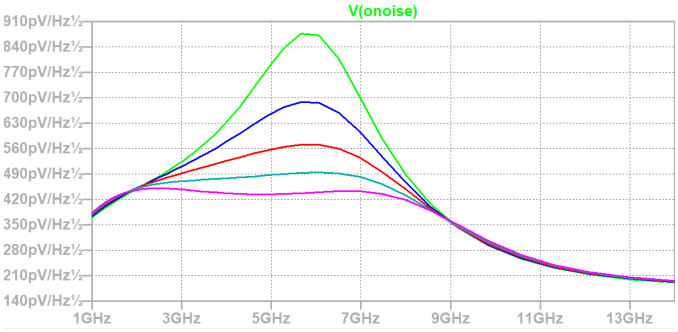

Fig. 22. NSD for L_{deg} = 0.1 nH, 0.2 nH, 0.3 nH, 0.4 nH, 0.5 nH

performance in each aspects, it was decided to set L_{deg} = 0.5 nH. (Optimal value was 0.4 nH, it becomes 0.5 nH after tuning other parts of the LNA.)

E. Transmission Line Design

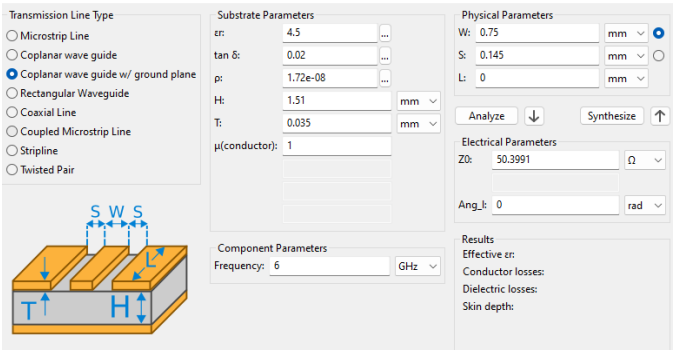

Fig. 23. Transmission line calculator from KiCAD

CPW length calculation (f = 6 GHz):

- free space wavelength, $\lambda_0 = \frac{c}{f} \approx 5$ cm (wavelength of the signal in the waveguide will be less)
- maximum quarter wave length, $\lambda_{max} = \frac{\lambda_0}{4} = 1.25$ cm

F. Noise Performance at 290 K

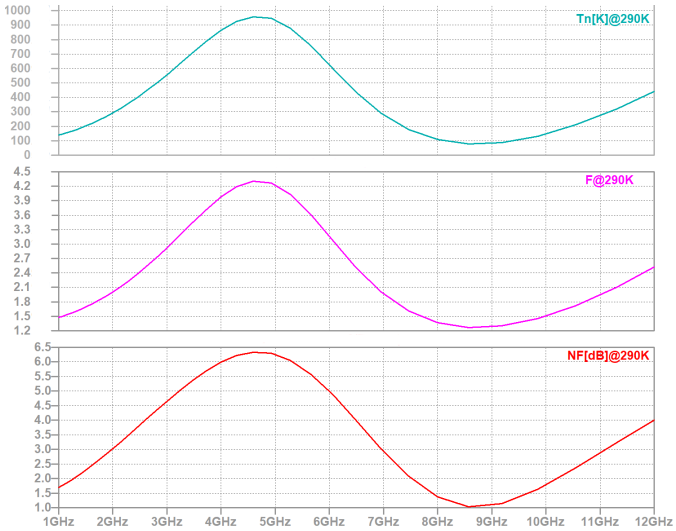

Fig. 24. (i) Noise Temperature T_n, (ii) Noise Factor F, (iii)Noise Figure NF, at 290 K

At 290 K, the LNA noise figure is varying widely across the band of interest, from 1.05 dB to 6.3 dB. This again suggests that alternative bias designs are needed to enable the amplifier to operate at 290 K. In order to enable the LNA to operate at different operating points, numerically adjustable components such as varactor diodes can be used. For example, by implementing impedance matching network with varactor diode, the LNA is able to work on different frequency range [21].

G. High Current CE

Schematic & Transistor Parameters:

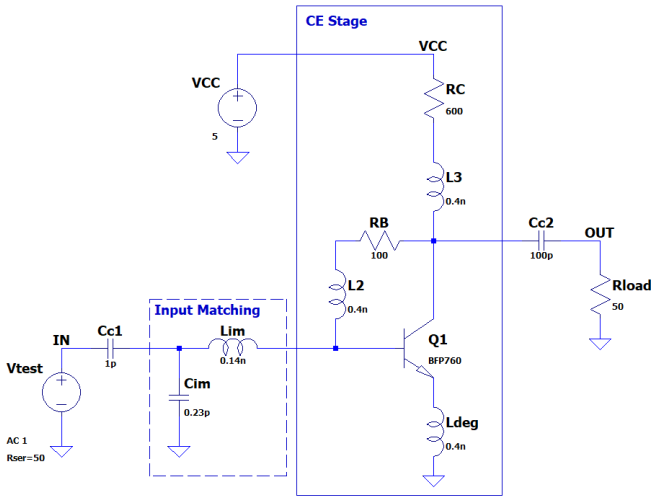

Fig. 25. Schematic of SiGe:C HBT LNA (Common Emitter) with high current design

```
Name:      q:q1:1
Model:   q1:m_bfp760
Ib:        2.94e-08
Ic:        6.52e-03
Vbe:       1.09e+00
Vbc:       1.01e-05
Vce:       1.09e+00
BetaDC:    2.22e+05
Gm:        3.80e+00
Rpi:       5.30e+04
Rx:        2.74e+00
Ro:        3.17e+04
Cbe:       8.00e-12
Cbc:       6.26e-14
Cjs:       2.11e-13
BetaAC:    2.01e+05
Cbx:       2.68e-14
Ft:        7.46e+10
```

Fig. 26. Parameters of SiGe:C HBT BFP760 with high current biasing at 18K

S-parameters (S_{21}, S_{11}):

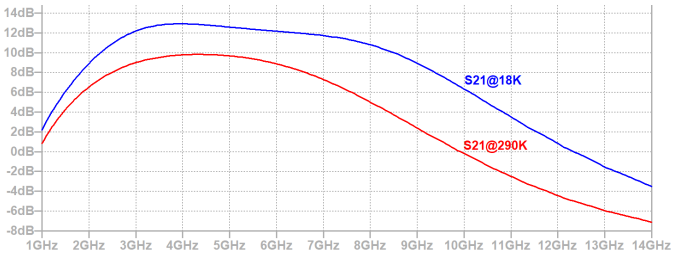

Fig. 27. S_{21} at 18 K and 290 K

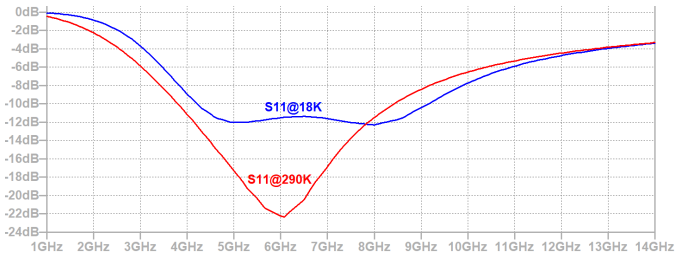

Fig. 28. S_{11} at 18 K and 290 K

R_C sweep:

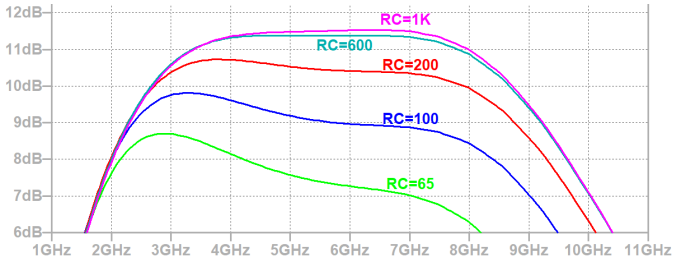

Fig. 29. S_{21} for R_C = 65 Ω, 100 Ω, 200 Ω, 600 Ω, 1 kΩ, at 18 K

L_{deg} sweep:

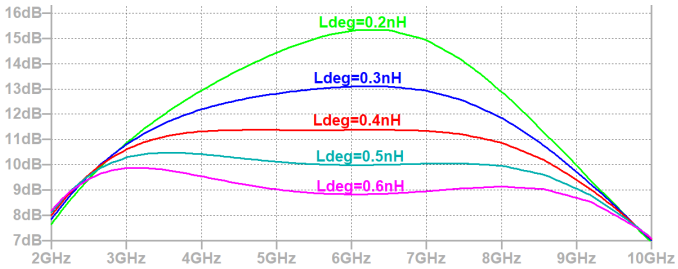

Fig. 30. S_{21} for L_{deg} = 0.2 nH, 0.3 nH, 0.4 nH, 0.5 nH, 0.6 nH, at 18 K

Smith chart & Pre-/Post Matching Comparison:

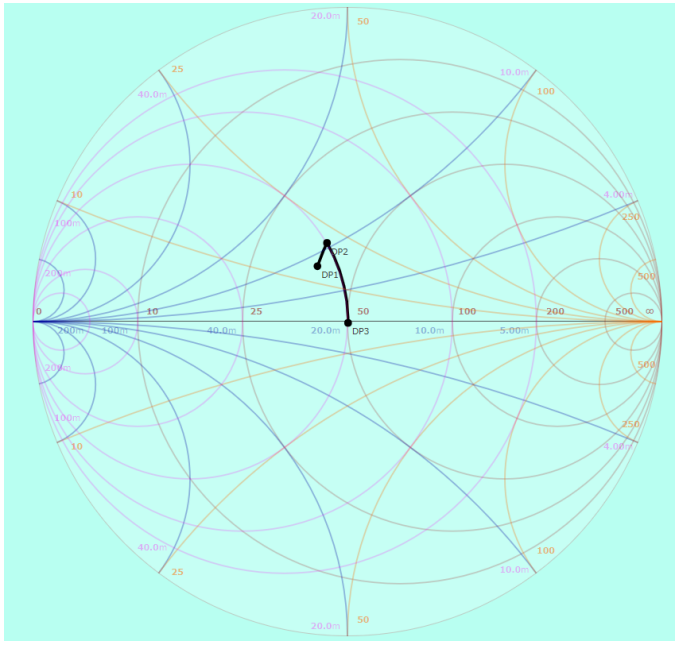

Fig. 31. Smith chart for input impedance matching (Z_s = 50 Ω)

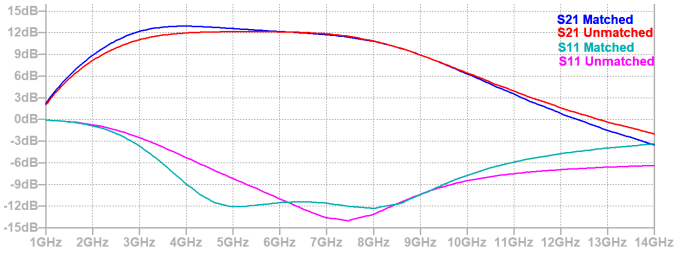

Fig. 32. S_{21} with input matching (blue); S_{21} without input matching (red); S_{11} with input matching (cyan); S_{11} without input matching (magenta)

Noise Spectral Density & Noise Contribution & Noise Performances

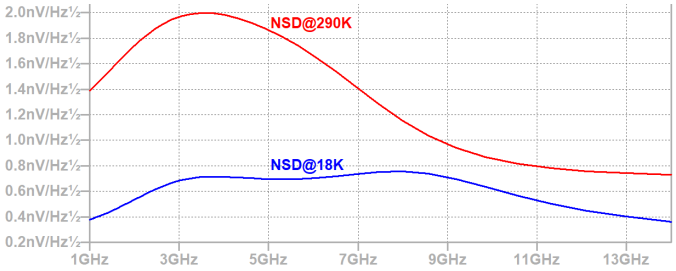

Fig. 33. Noise Spectral Density at 18 K (blue) and 290 K (red)

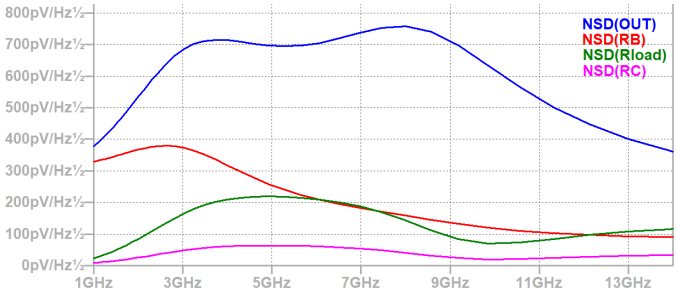

Fig. 34. Output Noise Spectral Density (blue); NSD of R_B (red); NSD of R_{load} (green); NSD of R_C (magenta), at 18 K

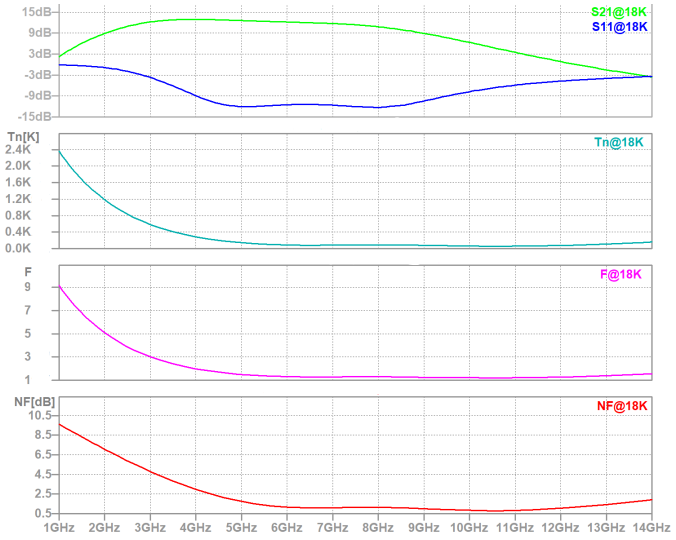

Fig. 35. i) Noise Temperature T_n, (ii) Noise Factor F, (iii)Noise Figure NF, at 18 K

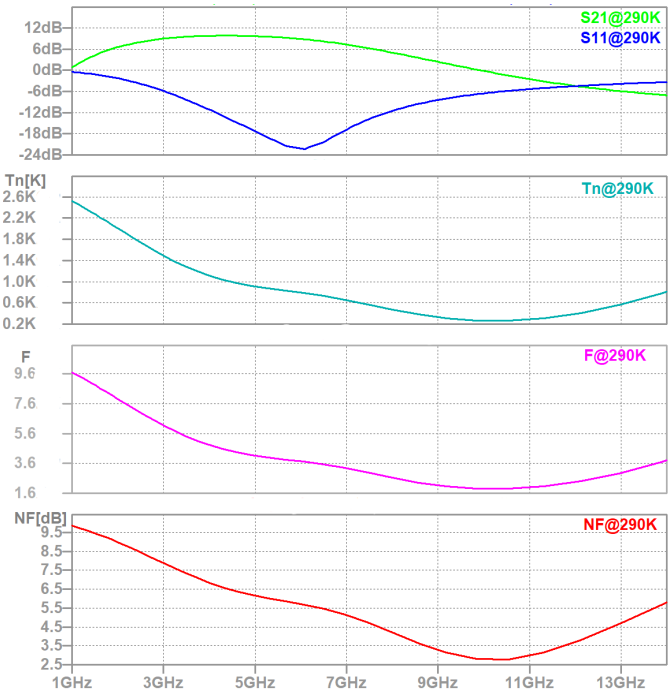

Fig. 36. i) Noise Temperature T_n, (ii) Noise Factor F, (iii)Noise Figure NF, at 290 K