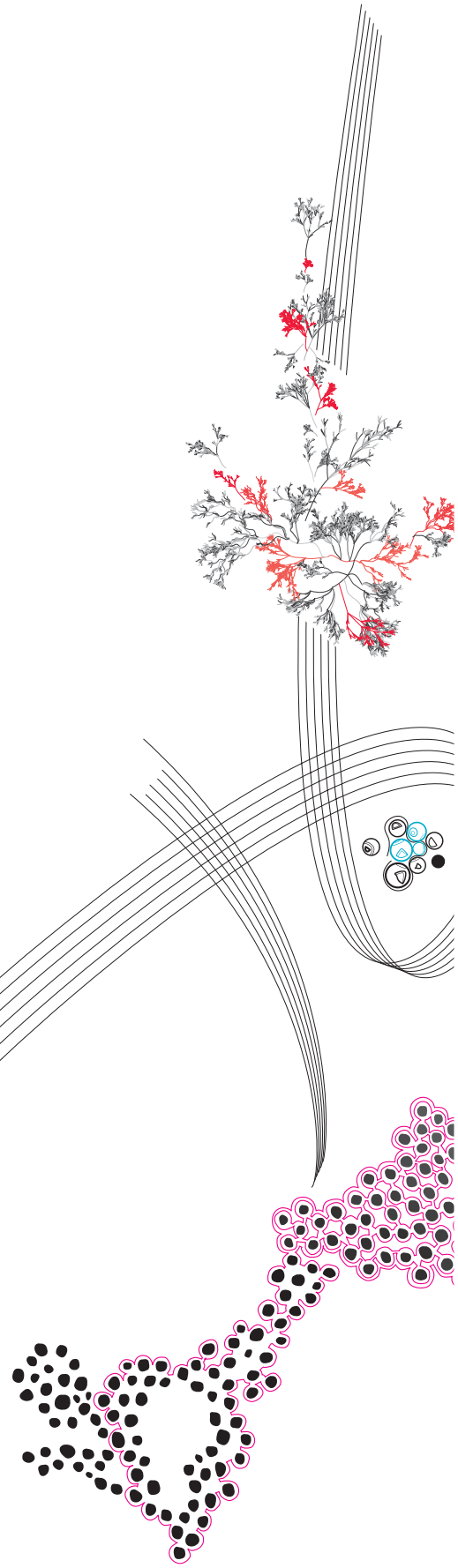

MSc Radio Systems
Final Project

RF performance optimisation by optimising distributed bond wire height over wire arrays

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UNIVERSITY OF TWENTE.

Preface

This report presents my research work in fulfilment of the graduation requirements for the Radio Systems program at the University of Twente. Furthermore, it aims to share new insights gained during this study with engineers at Ampleon Nijmegen, The Netherlands, where I conducted this research from November 2024 to June 2025.

During my student gap year, I had a remarkable experience as a propulsion systems engineer at Solar Boat Twente. Despite being told by experts that our specific foil setup was unable to make the boat foil, we successfully foiled over the waves of the Mediterranean Sea in Monaco. As the designer and producer of the boat's propeller, I had to navigate through the scepticism of stakeholders and sponsors regarding my uncontroversial design choices. Contrary to their predictions of only 65% efficiency, my first iteration achieved an impressive 78% open water efficiency, while opening a path for further improvements not previously seen in the industry.
This experience sparked a strong desire in me to innovate and challenge established claims. Ampleon provided me with a unique opportunity to do just that, allowing me to learn from experienced employees while exploring the validity of their expectations and related work.

I hope my report will inspire engineers at Ampleon to revisit and refine their designs using distribution enhancement techniques. I extend my gratitude to I. Volokhine and M. Unstel for sharing their expertise and time with me, which greatly facilitated my understanding of this project.
I would particularly like to thank Patrick Valk for his guidance, support and encouragement throughout this project. Despite the challenges that came with working with a "stubborn student," he remained committed to helping me achieve this result.

Tim Doppenberg
Achterveld, Juni 2025

Glossary

AC	Alternating Current.
ADS	Advanced Design Systems.
BWT	Bond wire Tool.
CAD	Computer-aided design.
CW	Continous Wave.
DE	Drain Efficiency.
DLP	Double Lowpass.
EM	Electro Magnetic.
GaN	Gallium Nitride.
HB	Harmonic Balance.
HEMT	High-Electron-Mobilit Transistor.
Ld	Lead drain.
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor.
Lg	Lead gate.
MOS	Metal-Oxide Semiconductor.
MXE	Maximum Efficiency point.
MXP	Maximum Power point.
PAE	Power Added Efficiency.
RF	Radio Frequency.
SiC	Silicon Carbide.

Abstract

Due to the internal coupling between bonding wires inside RF power amplifiers, the current across wire arrays becomes non-uniform, causing individual cells to operate under unequal and non-ideal conditions. Various optimisation approaches enhancing the uniformity have consistently led to improvements in device performance. The consistent performance gains across different methods suggest that a common underlying mechanism or variable may be driving observed improvements. Multiple approaches have been compared to reveal the underlying mechanism. Simulation results show that optimising the bond wire height distribution is most effective from the perspective of a voltage-controlled current source. A uniform voltage distribution over the gate results in increased maximum power output. Furthermore, the current phase of the drain should be aligned to enhance the efficiency.

Keywords: RF Power Amplifiers, Distribution effect, Scaling effect, Proximity effect, Bond wire.

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Chapter 1

Introduction

The demand for faster wireless communication has led to significant advances in high-power amplifier technology and design. High-power amplifiers are used in multiple applications like broadcasting, industrial, scientific research, medical, heating, (non-cellular) communications, aerospace and defence operations.

The basic working principle of an amplifier is to increase a weak signal to a signal with a stronger amplitude [6, 18]. Active devices such as transistors are used to achieve amplification. Radio Frequency (RF) amplifiers amplify the amplitude of signals operating at high frequencies, typically in the range of MHz to several GHz. High-power amplifiers take this principle to the next level by amplifying the signals to hundreds of watts of output power.

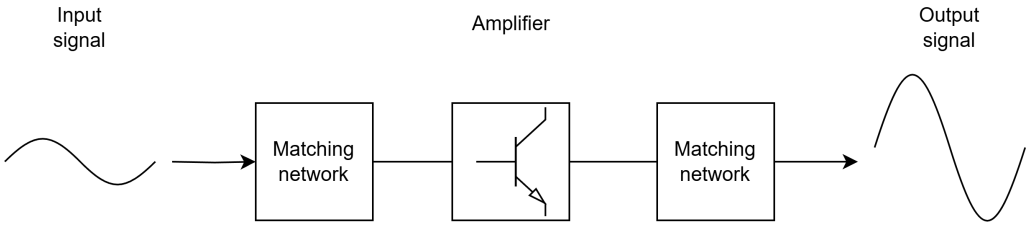


FIGURE 1.1: Basic operation of a RF amplifier.

Single transistors do not have the capabilities to achieve the power requirements in high-power applications. Therefore, designers connect multiple transistors in parallel to increase the output power constructively. The downside is that impedances decrease drastically and sometimes even approach impedances $< 1\Omega$. RF systems require well-matched networks to ensure efficient and accurate operation, which can be challenging to achieve at low impedance values [12]. Mismatching can result in excessive heat generation, ultimately damaging the amplifier or other components. Complex matching structures are therefore integrated into amplifier packaging to overcome mismatching.
Designers heavily depend on their extensive knowledge of high-power RF amplifiers when designing complex matching structures. Knowledge that is not always readily available to the end-user makes it difficult for them to extract optimal performance from the amplifier. Matching structures are therefore integrated into the amplifier package by the designer. The integration of matching structures limits the use cases of the specific amplifier. Designers, therefore, become more involved in the user application to judge it on a system level rather than a transistor level.

Based on the requirements, designers can determine the required transistors and technology. If possible, designers prefer to choose an existing transistor die model and evaluate the criteria using an CAD tool. Packaging is then determined based on the die size and the number of dies required to achieve the desired power output. Parasitics of the packaging can be simulated by EM-simulation software. Then the internal matching network is designed using package parasitics, requirements and the die impedances. Designing specific internal matching enhances the overall operation of the device, but limits its range of applications.

If the matching network is designed, the designer connects all individual parts to perform load-pull simulations. The goal of load-pull simulations is to find the optimal performance under matched conditions, and the results can be used to verify the requirements based on performance. This way, the designer can virtually simulate the device's performance before creating a prototype, resulting in shorter design cycles and fewer trial-and-error iterations. Accurate models of all components are required to provide reliable and accurate results.

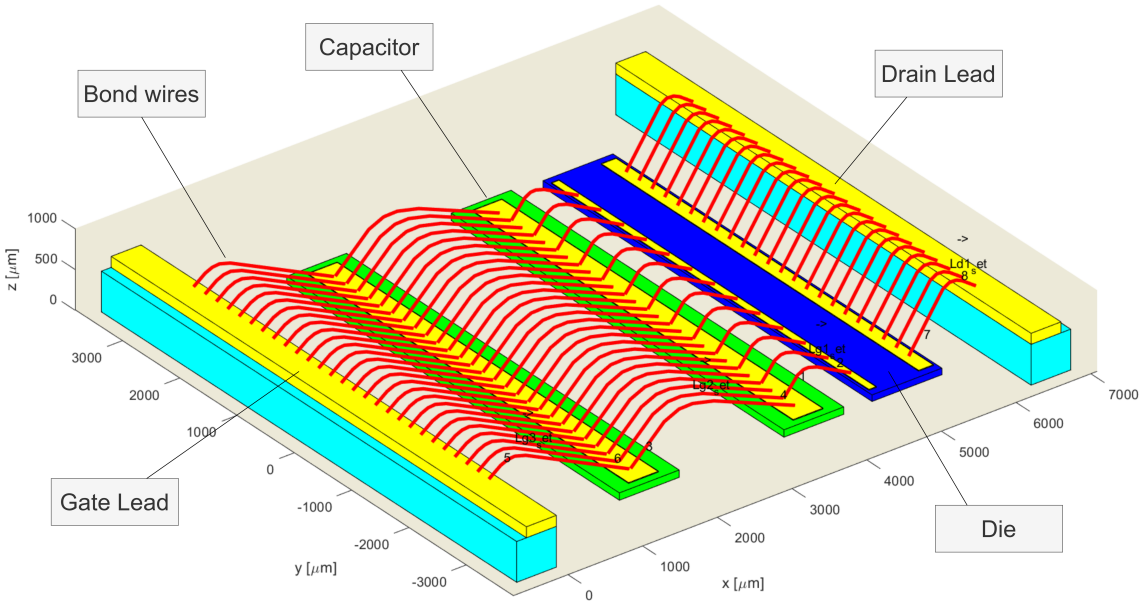


FIGURE 1.2: Internal components of a power amplifier. The transistor die (in dark blue) is connected to the matching capacitors (in green) and the package leads via bond wires (red lines). The metal bars in Yellow connect the bond wires and the transistors. The left side of the die is the gate side and gate matching structure, while the right side of the die features the drain matching structure.

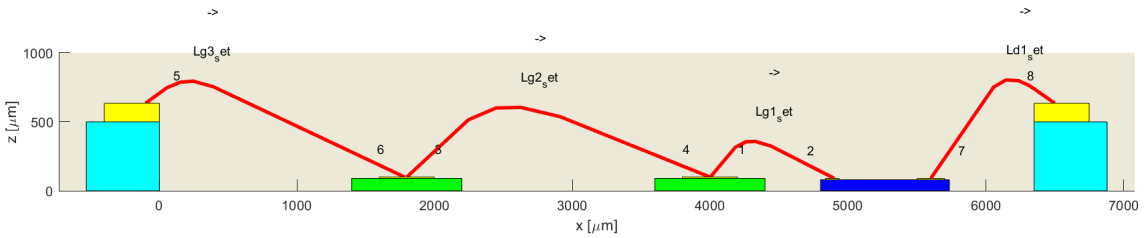


FIGURE 1.3: Internal side view of a power amplifier.

Figure 1.2 and 1.3 show the internals of a high-power RF amplifier. Typically, the device consists of four main components:

Die: The die (also referred to as power bar) contains multiple active devices (active cells) in parallel. The individual cells operate simultaneously to amplify the input signal present at the gate. Typically, the die is made using Laterally-Diffused Metal-Oxide Semiconductor (LDMOS) or Gallium Nitride (GaN) technology. Multiple dies can be placed inside the package to increase the power output further.

Capacitors: Capacitors are placed inside the packages and function as part of the matching network. Usually, the capacitors are formed using metallic contacts on top of a silicon block. A thin oxide layer between the metal and the silicon forms a Metal-Oxide Semiconductor (MOS) capacitor.

Bondwires: The primary function of the bond wires is to interconnect the devices with the package lead. In addition to connection, wires are used as inductors to match the network with capacitors. Bond wires can vary in length, height or diameter to achieve desirable inductance values. Different materials, like gold or aluminium, form the bond wires.

Packaging: The package houses the components and ensures that the amplifier can be mounted on printed circuit boards. The package also acts as the source for the transistors and is responsible for cooling. Furthermore, the package introduces package parasites such as lead capacitance and inductance.

Chapter 2

Problem discription

Ampleon specialises in designing and delivering high-quality, high-performance RF power amplifiers based on LDMOS and GaN technologies. The multimarket department targets various applications with their RF power amplifier, including broadcasting, industrial, medical, cooking, communications, aerospace, and defence.

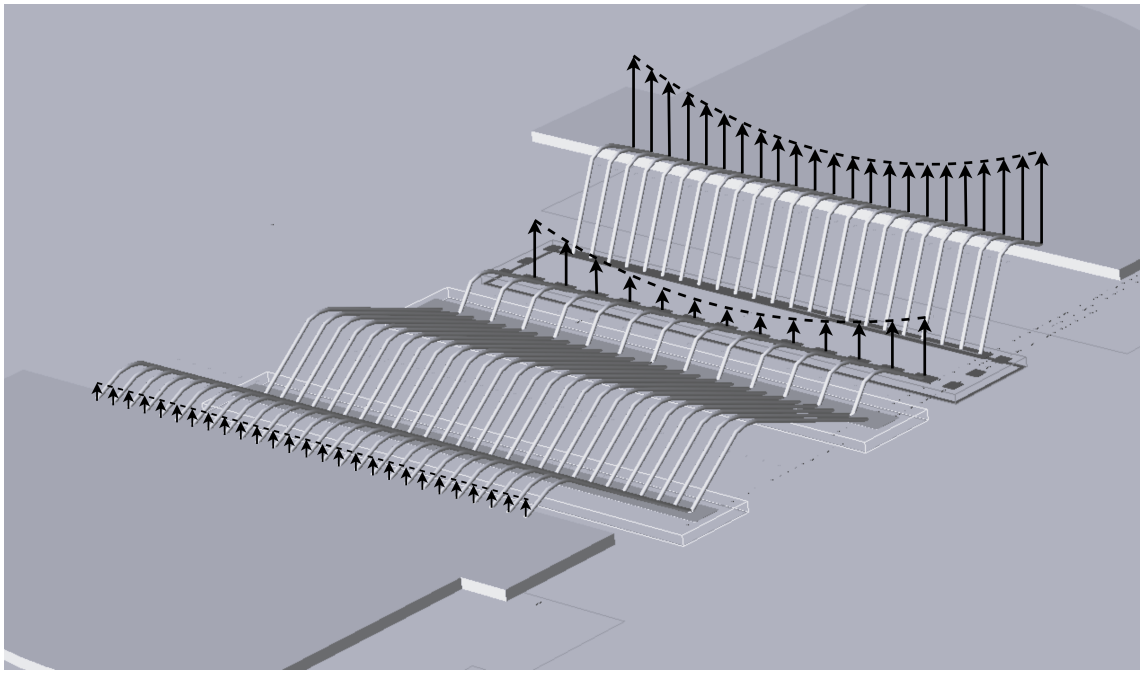


FIGURE 2.1: Current distribution over the internal bond wire arrays. The current distribution at the gate lead (bottom left) is assumed to be uniform. Due to the proximity effect, the current becomes nonlinear at the gate of the power bar. This non-uniform distribution is then amplified and delivered to the drain package lead (top right).

Figure 2.1 presents a 3D view of the internals of a power amplifier. The signal is injected into the device via the gate lead. Bond wires carry the signal from the lead via the matching capacitor to the gate of the cells in the power bar. Due to the internal coupling between the bonding wires and distributed effects inside the devices, the current across the wire array becomes non-uniform. The non-uniformity causes the individual cells in the power bar to operate under different conditions. Therefore, some cells can generate more power than their neighbours, while other cells can even start to dissipate power [2]. These effects are

highly undesirable, as they negatively impact the performance of the devices. Especially in GaN devices, since the performance heavily depends on the operation temperature. Additional heat generation can activate thermal degradation, reducing the lifespan of the devices.

RF design engineers carefully design complex matching circuits inside the packaging to ensure correct operation for their intended use of the power amplifier. Distributed effects can cause impedance mismatching, resulting in individual cells operating outside the intended operation region. Furthermore, with the advancements in GaN technology, the power density of the devices is increasing with each generation. Therefore, bond wires will carry more current, or the space between bond wires will be reduced, ultimately resulting in increased mutual coupling and non-uniform current distribution [15, 16].

Ampleon is curious if RF performance is enhanced by optimising the distributed bond wire height over the bond wire array. Due to coupling effects, not all wires inside the bonding wire arrays have the same inductance, causing the current to distribute non-uniformly. The height of individual wires can be tweaked to equalise the inductances over all wires in the bond wire array. Equal inductance should result in a more uniformly distributed current over the wire arrays. However, inductance is frequency-dependent. Bond wire height distribution could be used to optimise for the fundamental frequency, harmonics, current distribution, and more parameters. This study should therefore result in new insights into effective optimisation techniques for bond wire height to extract additional performance from high-power RF amplifiers.

Chapter 3

Related work

3.1 CAD models of bond wires

The accurate modelling is crucial for efficient design and reliable amplifiers. In 2001, the first comprehensive study was published on the modelling of high-power RF transistors using CAD tooling [13] by K. Mouthaan. Mouthaan introduced detailed models for capacitors, packages and bond wire arrays, which are implemented in Advanced Design Systems (ADS). Components are simulated individually and then cascaded using the modelling by segmentation approach to virtually estimate the performance of RF high-power amplifiers [1].
During the study, it was observed that the capacitance effects could be neglected for the bond wires at low frequencies. Consequently, Mouthaans' bond wire model is based on Neumann's inductance equation to calculate the mutual inductances [16]. Self-inductance is calculated via this equation by mirroring the wire in a perfect ground plane. Mutual coupling is calculated and added to the self-inductance to acquire the total inductance of the wire. Furthermore, DC losses (due to the finite conductivity of the wires) and AC losses (due to the skin effect) are accounted for.

For frequencies above 6GHz, discrepancies between measurements and simulations are observed [3], which highlights the limitations of the bond wire model in ADS. As frequency increases, capacitance effects and parasitics become more pronounced, rendering the bond wire model implemented in ADS incomplete. Three-dimensional EM simulation software is more accurate at higher frequencies [8, 10]. The benefit of EM simulation includes the comprehensive modelling of all effects at a higher resolution, although at the cost of increased computational requirements and increased simulation time. With fast and rapid prototyping being a priority, this increased simulation time can be undesirable. As a result, engineers often prefer simulation by lumped elements. A common workaround is to extract the S-parameters from the EM simulation and use them for further modelling purposes. Nevertheless, altering the layout or the design of the shape will influence the S-parameter, necessitating new EM simulations.

In response to these limitations, a physics-based bond wire model was proposed in 2012, accounting for the capacitance between the wires and the ground [14]. A benefit of this model is its causal nature, which allows it to be used in time-domain simulations. Additionally, there are fewer restrictions on wire shape compared to Mouthaans' model. Agilent therefore implemented this model in ADS as an improved model of Mouthaans' bond wire model. However, due to differences in shape definition and compatibility issues with developed tools and scripts, Mouthaans' bond wire model is still used in some new

designs today in sub-6GHz applications.

3.2 Distribution effects in high-power transistors

The growing interest in higher efficiency and more powerful high-power RF amplifiers has led to increased complexity in matching structures and enhanced power density. The increased power density introduced new challenges in distribution effects. To understand this consequence, Neumann formula is used [15]:

$$M = \frac{\mu_0}{4\pi} \oint \oint \frac{dI_x \cdot dI_y}{r} \tag{3.1}$$

As the power density grows, so does the current flowing over the matching structures within a smaller area. Equation 3.1 indicates that an increase in current (I) or reduction of area (r) results in increased mutual coupling between the wires. Consequently, the difference in wire inductance over the array strengthens, causing currents to concentrate more at the device's outer edges. Therefore, the differences in voltages and currents over the transistor die increase with an increase in power density. In response, operating voltages have been raised while maintaining power outputs, thereby reducing current demands. However, with the rise of GaN devices and their increased power densities, modelling distribution effects is becoming more critical.

The advancements in modelling techniques have provided the engineer with deeper insights into distribution effects, such as the proximity effect, and their impact on overall device performance. Simulations can accurately predict current and temperature distributions, allowing designers to make targeted modifications to enhance performance [11, 17]. Individual cell performance and operation conditions can be evaluated and optimised more accurately. Designers can effectively understand the impact of distribution effects on overall device performance and make informed design choices to counter these effects.

Measuring distribution effects can be challenging. Due to the small packages and high current densities, a change in the magnetic field can alter the current and disrupt the device's operation, rendering all measurement results inaccurate. The potential distribution could, however, be measured with advanced non-intrusive near-field measurements [9].
The temperature distribution is relatively easy to calculate using infrared microscopes (although not all heat is radiated from infrared radiation). From this, designers could make informed estimates about the current distribution and modify their designs accordingly [19]. Additionally, the bond wires that carry the most current are often the first to malfunction due to excessive heat caused by high current flow. When these wires melt, they physically identify where the current is concentrated. By examining which wires in the array have melted, designers can make educated guesses about which wires carried the most current. Despite this indirect method, validating the accuracy of simulation results remains challenging. Direct measurements are often not reliable enough, leaving designers to rely on advanced modelling techniques and simulation tools to predict and mitigate these effects.

3.3 Improvement techniques

Engineers often rely on their extensive knowledge and experience when designing high-power RF amplifiers. However, if critical effects are not adequately known or incorrect assumptions are made during design, discrepancies can arise between simulated results and actual measurements obtained from test samples. In such cases, engineers typically seek to develop a solution that mitigates the specific discrepancies observed. These solutions often lead to new patents and lack comprehensive scientific validation or a clear rationale for the solution [20]. The individual solutions could be generalised into the following design approaches:

- **Harmonic terminations:** When multiple active devices parallel to each other are driven with a non-uniform distribution, odd-mode oscillation caused by the harmonics can emerge. As shown in [2], individual cells in the power bar may start to dissipate power instead of contributing. A harmonically tuned filter can selectively suppress the harmonics and improve the overall device performance [4].

- **Variable Die Pitch:** Another approach to addressing non-uniform current distribution at the gate is by modifying the size of the cells in the power bar. This technique, known as variable die pitch, involves making the outer cells smaller than those in the center. By reducing the size of the outer cells, their power output decreases, resulting in a more uniform overall power output across the power bar. This method effectively mitigates the non-uniform amplification effects caused by gate current distribution, resulting in more consistent drain characteristics for the power bar. However, one major drawback of this technique is that it often results in wasted die area and decreased power density.

- **Power rail design optimisation :** The power rail connecting bond wires and gate leads can behave as transmission lines, allowing signals to propagate in unwanted directions and varying individual cell characteristics. To mitigate this effect, a simple yet effective solution is to cut the metal rails. Detailed analyses have shown that cutting the rails improves voltage distribution across the device, resulting in enhanced overall performance [7]. This optimisation technique helps to ensure that each cell operates consistently, resulting in enhanced device performance.

3.4 Improvement techniques considering bond wire length

Another possible improvement technique involves modifying the electrical length of individual electrical paths. Studies have shown that adjusting the layout of bond wires can significantly impact current distributions and heat generation [11, 17, 19, 5, 8]. In [17, 19], the layout of the drain bond wires is changed to increase the inductance of the outer shunt bond wires. Therefore, the current distribution is more uniform over the shunt bond wires. The outer bond wires generate less heat compared to the original design, which prolongs the product's life [11]. In [8], the length of the edge bond wires has increased, making them electrically longer. This makes the phase in the drain more uniform, resulting in an increased efficiency of 10-15%. In [5], the bond wire array geometry is altered to improve the power distribution over the die.

The electrical length at the drain is adjusted in the sources above to improve the distribution. In 2022, I. Vlokhine conducted an internal study at Ampleon to improve the device's performance by reducing non-uniformity over the wire array (Figure 3.1). This

study was based on an existing device model in ADS with 21 active cells in the power bar. The second-most outer bond wires at the gate have been removed, increasing the current that runs over the outer edges of the bond wire array. It has been observed that the outer edge cells operate less efficiently, while the efficiency of the centre cells in the power bar has been improved. The reason for this improvement is unknown, but the outer cells have likely been sacrificed to enable the device to operate more uniformly.

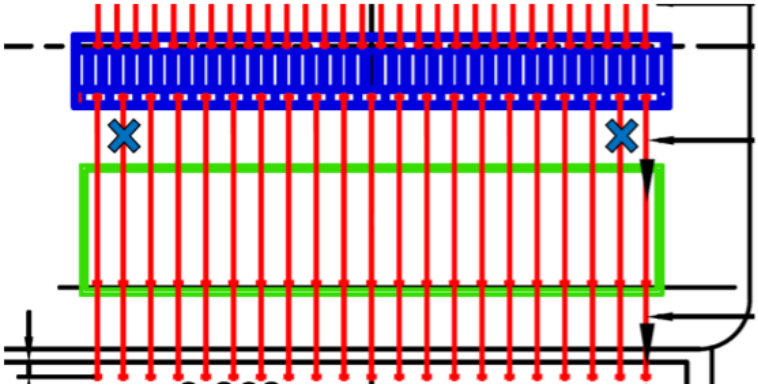


FIGURE 3.1: Second outermost bond wires are cut in I Vlokhine's work. The picture represents the matching structure at the gate of the device.

Furthermore, M, Ustunel have conducted extensive research at Ampleon in altering the gate bond wire lengths to mitigate harmonic effects at the drain, by making the voltage distribution over the gate more uniform. Furthermore, the results indicate that improvements made at the gate can impact the distribution effects at the drain.

3.5 Conclusion

Several strategies to eliminate distribution effects have been proposed and implemented. However, some solutions are patented and lack comprehensive scientific evidence supporting their effectiveness. Meanwhile, various optimisation approaches have consistently led to improvements in device performance. The consistent performance gains across different methods suggest that a common underlying mechanism or variable may be driving the observed improvements.
Some techniques have been applied to the gate, while others have been applied to the drain. Combining these may further improve the device's performance, but requires the underlying mechanism to identify effective optimisation methods.

Chapter 4

Methodology

The conclusion of section 3 indicates a research gap in the fundamental understanding of the elimination of distributed effects. In this chapter, the aim of this work is presented to fill this gap. Additionally, research questions are formulated using this methodology.

4.1 Aim

Section 3 highlights the diversity of approaches that can be employed to enhance the performance of high-power RF amplifiers. This multiplicity of methods suggests the presence of an underlying mechanism or principle that requires further investigation beyond the optimisation techniques themselves. With the growing power densities, understanding and mitigating these effects becomes increasingly crucial for resolving distribution-related issues in RF high-power amplifiers. Therefore, the purpose and contribution of this study are to uncover the underlying mechanism and propose effective optimisation strategies.

4.2 Research questions

The main question that the study focuses on is: How can bond wire height optimisation effectively be used to mitigate the distribution effects in high-power RF amplifiers to improve device performance?
To answer the question, multiple sub-questions have been formed:

- Are existing models accurate enough to model the distributed effects?
- Is optimising a specific parameter more effective at the drain or the gate side?
- Which distribution effects are encountered more effectively by the bond wire height?
- Is it possible to forecast the change in distributed effects?

These sub-questions will guide the research and analysis conducted throughout this study, ultimately contributing to a deeper understanding of the relationships between bond wire height, distribution effects, and high-power RF amplifier performance.

4.3 Methodology

Given that the primary focus of this work is not on designing high-power RF amplifiers from scratch, but rather on optimising their performance through bond wire height optimisation, it was deemed most effective to start with an existing device model that has already been fully measured and modelled. The benefits of using an existing design include:

- **Verified Design:** The design has undergone multiple iterations and modifications, resulting in a working device. This provides a reliable starting point for further optimisation and modelling;
- **Existing measurement results and models:** The device performance characteristics are already well-documented, allowing us to build upon this foundation.

With this existing design as the basis, a detailed model can be created to analyse and quantify the present distribution effects within the high-power RF amplifier. This model will serve as the foundation for further research and experimentation. Next, the bond wire heights on both the gate and drain sides will be individually altered to counteract the observed distributed effects. Different optimisation strategies will be explored on each side, enabling a comprehensive comparison of their relative effectiveness. Simulation results from these improvement strategies will then be compiled and analysed to draw overall conclusions about the impact of bond wire height optimisation on high-power RF amplifier performance. Figure 4.1 illustrates the Simulation Matrix, which will serve as a comprehensive framework for comparing and contrasting various optimisation approaches.
The simulation matrix will be populated with the results of individual approaches used to optimise for specific parameters. The parameters are on the left of the matrix. Additionally, the location of the applied technique is specified. Presenting the results in a structured matrix format will enable comparison and highlighting of any significant differences between various optimisation strategies.

	Gate	Drain	Combined
Phase			
Inductance			
Rail			

FIGURE 4.1: The simulation matrix containing multiple approaches for improvement techniques (on the left) applied at certain locations (on the top).

Chapter 5

Modelling of distributed characteristics

In this chapter, the chosen high-power RF amplifier device is rebuilt and simulated in ADS, creating a full-scale model that serves as the basis for further analysis of the distributed effects. The device's performance is evaluated to quantify distributed effects while exploring modelling choices and limitations to discuss reliability and accuracy.

5.1 CLF24HLS300P RF power amplifier

The CLF24HLS300P from Ampleon is selected as the basis for this work, an active GaN-SiC HEMT power transistor designed for Continous Wave (CW) applications in the 2400 MHz to 2500 MHz frequency range.

Key features:

* 300W RF power amplifier;
* Drain directly connected to the package lead via a single bond wire array;
* Integrated DLP internal matching network in ceramic package;
* Two dies integrated in the package, separately connected to the package leads;
* The source also acts as a heat sink, located at the bottom of the package.

For more detailed information on the device's performance, refer to the datasheet or Ampleon's website.

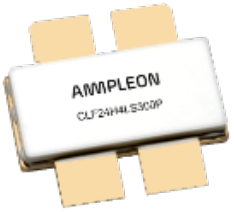


FIGURE 5.1: CLF24H4LS300P High-Electron-Mobilit Transistor (HEMT).

5.2 Ampleon Bond Wire Tool model

The performance of RF power transistors relies heavily on matching networks, with bond wires being a critical component within the matching structures. Several tools assist the design of bond wires, such as Keysight ADS or Ansys EDT. However, these tools serve multiple design purposes, making them versatile. This also leads to a repetitive and time-consuming design process for designing bond wire arrays. Additionally, extracting the impedance values is not a straightforward process since simulations are required.
To overcome the challenges, Ampleon has developed a software tool called Bond wire Tool (BWT) for designing and evaluating bond wires. The BWT provides an intuitive graphical interface which helps to visualise the shape and directly calculate wire inductance. Bond wire arrays can be created from multiple single wires, where the coupling between wires, based on frequency, is calculated directly to extract the total inductance of the array. If numerous arrays are added to a project, a complete assembly can be drawn in this tool. Based on the location of the bond wires, the tool can calculate the coupling between individual arrays and wires. To further streamline the design process, the tool can generate scripts to import bond wire designs directly into ADS and Ansys EDT.

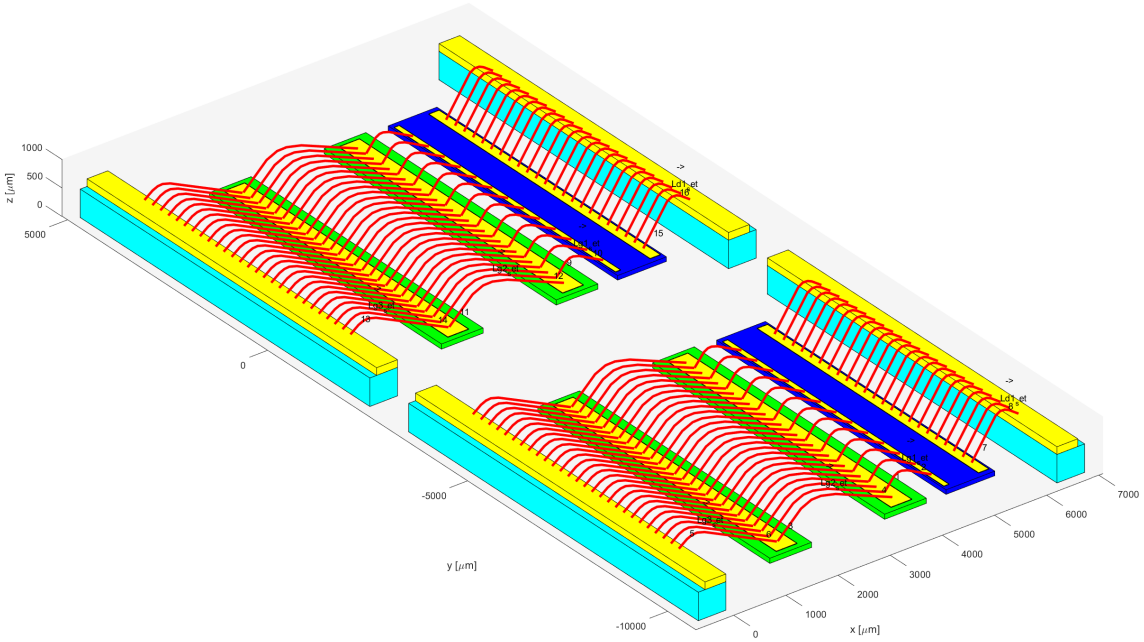


FIGURE 5.2: Assembly of the CLF24H4LS300P power amplifier graphically given by the Ampleon BWT.

The layout of the CLF24H4LS300P high power amplifier as provided by the BWT (Figure 5.2) shows two dies with identical matching structures. The bond wires are numbered from the die such that Lg1 (Lead gate (Lg)) represents the gate bond wire array connected to the die and the first capacitor. Lg2 is connected from capacitor 2 to capacitor 1, and Lg3 is the wire array connecting the package lead to the 2nd capacitor. Ld is the bond wire array connecting the drain of the die to the package lead.
From this model, the inductances of the arrays and the coupling factor between the arrays are calculated in the BWT. The results are in the table 5.1. Notably, the coupling factor found is relatively small, indicating that the placement of the second die and the matching network in the package has a negligible impact on the overall inductance values.
A further comparison (table 5.2) reveals that the presence or absence of the second half

of the device makes no difference in array inductance. Since there is no difference in bond wire inductance, further modelling is done with only one half of the device to reduce the computational time.

	Nset1 Lg1	Nset1 Lg2	Nset1 Lg3	Nset1 Ld1	Nset2 Lg1	Nset2 Lg2	Nset2 Lg3	Nset2 Ld1
Nset1 Lg1	1	0.0428	-0.0010	-0.0183	0.0007	0.0015	0.0011	-0.0017
Nset1 Lg2	0.0428	1	-0.0039	-0.0248	0.0015	0.0045	0.0008	-0.0020
Nset1 Lg3	-0.0010	-0.0039	1	-0.0811	0.0011	0.0008	0.0477	-0.0454
Nset1 Ld1	-0.0183	-0.0248	-0.0811	1	-0.0017	-0.0020	0.0455	0.0706
Nset2 Lg1	0.0007	0.0015	0.0011	-0.0017	1	0.0428	-0.0010	-0.0183
Nset2 Lg2	0.0015	0.0045	0.008	-0.0020	0.0428	1	-0.0039	-0.0248
Nset2 Lg3	0.0011	0.0008	0.0477	0.0455	-0.0010	-0.0039	1	-0.0811
Nset2 Ld1	-0.0017	-0.0020	-0.0454	0.0706	-0.0183	-0.0248	-0.0811	1

TABLE 5.1: Coupling factor k table calculated by the BWT.

	halve	full
LG1	0.059	0.059
LG2	0.168	0.168
LG3	0.174	0.174
LD1	0.114	0.114

TABLE 5.2: Inductance of the bond wire arrays in nH calculated by the BWT.

5.3 ADS simplified model

The BWT can generate a script to import the shapes and layout of the bond wires in ADS. Usually, these inserted components and definitions of the bond wires are then inserted in a simplified schematic to model the behaviour of the power amplifier. Figure 5.3 presents the simplified electric schematic of half the CLF24H4LS300P components shown in Figure 5.2.

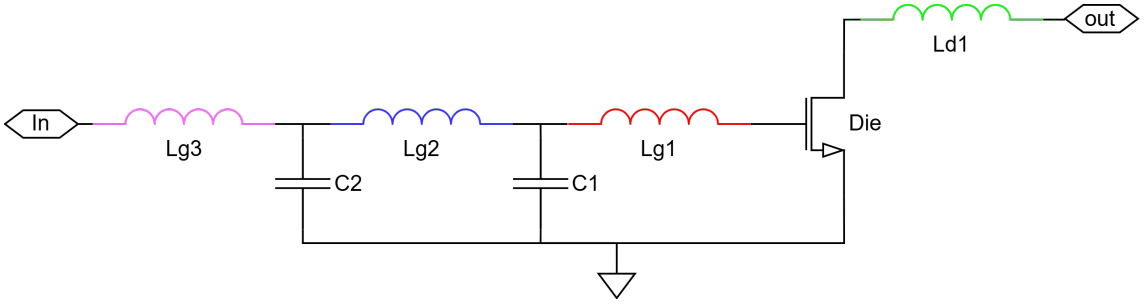


FIGURE 5.3: Simplified electrical schematic of the internal components of the CLF24H4LS300P.

The schematic in Figure 5.3 contains a DLP filter, formed by the gate bond wires and the gate capacitors, and is connected to the gate of the die. The die is a model available in the Ampleon library constructed from 13 individual cells. The drain of the power bar is then connected to the package lead via the drain bond wire (Ld1). Each inductor is equal to the equivalent inductance of the whole array. The behaviour of half of the power amplifier can therefore be described with the simplified schematic. However, the package parasitics

are not included, but have a significant impact on the device's performance due to the low operating impedances. Fortunately, these parasitics are already known and equivalent schematics already exist for this device. Figure 5.4 contains the remaining elements to complete the schematic in ADS.

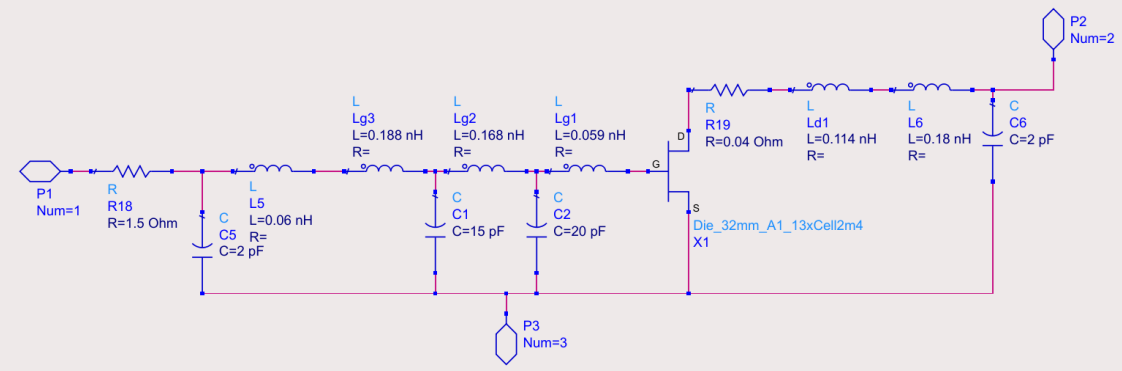


FIGURE 5.4: Simplified model of half CLF24H4LS300P internals.

Besides the inductors (bond wires), capacitors, and the package's parasitics, a resistor of 1.5Ω has been added at the gate. In reality, the package lead resistance will be significantly smaller. However, the model of the die required some additional resistance to suppress the total gain of the device and improve the stability of the simulations.

The schematic in 5.4 is used to perform HB-simulations in combination with load sweeping to determine the large signal behaviour of the device at different load points. This type of simulation is also known as a load-pull simulation and is discussed in more detail in Appendix A. Figure 5.5 contains the resulting compression contour lines from the load-pull simulation.

The compression contour lines are a useful tool, as they provide an overview of the device's performance at the 3dB compression point for a specific load. The Maximum Efficiency point (MXE) is achieved at an impedance $Z_L = 1.176 - j1.784\Omega$, reaching a drain efficiency of 79.42% with a respective output of $208W$. A load of $Z_L = 1.726 - j2.615\Omega$ reaches the Maximum Power point (MXP) with a power of $281W$. However, this shift in load impedance for a higher power output is a trade-off with efficiency, and the drain efficiency then drops to 75.15%. In both cases, the source impedance is set to 5Ω, $V_{GS} = -5V$ and $V_{DS} = 50V$.

A comparison of the simulation results and the datasheet of the CLF24H4LS300P reveals some discrepancies. First, it is important to note that the simulations only cover half the device. This results in different impedance values and power output values. It immediately becomes clear that the peak power output of the simulation model is too high. Furthermore, the drain efficiency of the simulation results is higher than the performance mentioned in the datasheet (74% compared to 79.42%). Discrepancies between the simulations and measurements are common. Engineers, therefore, measure the response of the actual device and tune their simulation model accordingly to match the measured data before making their models available for customers.

Multiple reasons can cause the discrepancies between the simulation and measured results. One reason may be the assumptions made in the models used in ADS. Another reason may be the absence of distribution effects since the schematic in Figure 5.4 assumes equal operating characteristics for each cell. Further investigation into the different operating characteristics is not possible due to the simplification of bond wire arrays to a single

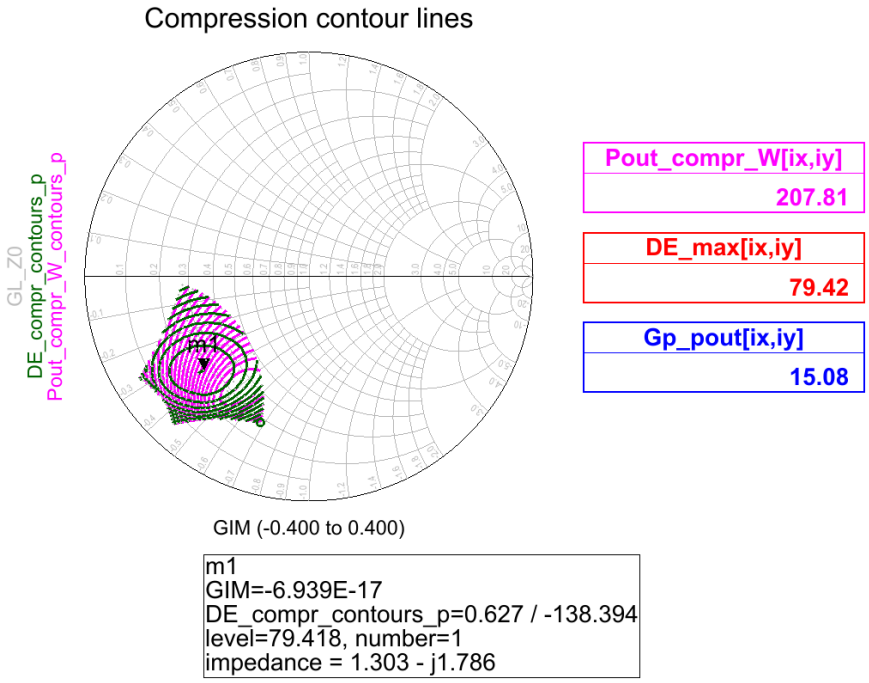


FIGURE 5.5: Load-pull compression contour lines of the schematic of Figure 5.4. The impedances are normalised to 5Ω due to the low impedance values of the device.

inductor. Therefore, in the next section, a model is designed to include all individual bond wires and rail components.

5.4 Design of the extended simulation model

To simulate the distribution of current, voltage PAE, DE, a model is required which includes all individual components. Figure 5.6 represents a block diagram for modelling the distribution effects.

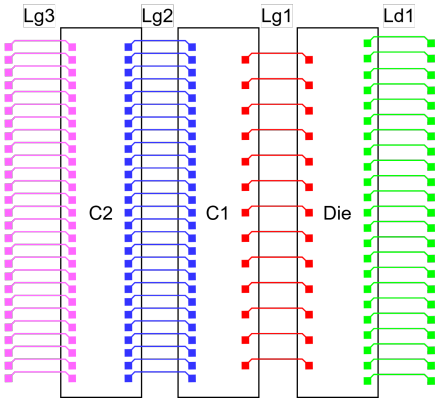


FIGURE 5.6: Block diagram of the required components to simulate the distribution effects.

In this section, the block diagram will be implemented in a schematic for simulation purposes. First, the bond wire model will be explained and discussed in detail. Then, the

capacitor rails are discussed and implemented in the schematic.

5.4.1 Bond wire model

The CLF24H4LS300P consists of 180 bond wires, 90 for each half of the device, divided over four arrays. Two models are available in ADS to model these bond wire arrays. The model based on [13] has a couple of restrictions:

- The model calculated the self- and mutual inductances of coupled bond wires using Neumann's inductance equation;
- Each bond wire is segmented into 5 straight segments;
- Bond wires are not allowed to touch or intersect;
- The model assumes a perfectly conducting ground plane;
- Capacitive coupling between bond wires and the ground is not accounted for;
- Loss due to radiation is not considered;
- A change in current distribution due to the proximity of other wires is not included;
- DC losses, due to the finite conductivity of the wires, are included;
- AC losses from the skin effect are included in a zero-order approximation.

The alternative bond wire model implemented in ADS overcomes some of these problems [14]. Capacitive effects are included, and since it is a physics-based model, the causal nature allows the model to be used in time-domain simulations. However, since the device operates at frequencies below 6GHz, the difference between the models is negligible [8, 10]. Therefore, both models are valid candidates for modelling the bond wires in the CLF24H4LS300P.
Both models allow different shape definitions in a single bond wire array. Additionally, each bond wire location could be adjusted individually. This is important for defining multiple different bond wire topologies within a single array to improve distribution across the die. Defining different bond wire topologies within a single array model ensures that the coupling between all individual wires is accounted for. Therefore, it is preferred to specify all 90 bond wires within a single bond wire array to avoid manually adjusting the coupling factor for each bond wire. The model based on [13] supports up to 50 bond wires, while the model based on [14] supports up to 100 bond wires. Since the device contains 90 bond wires, the model based on [14] is preferred.

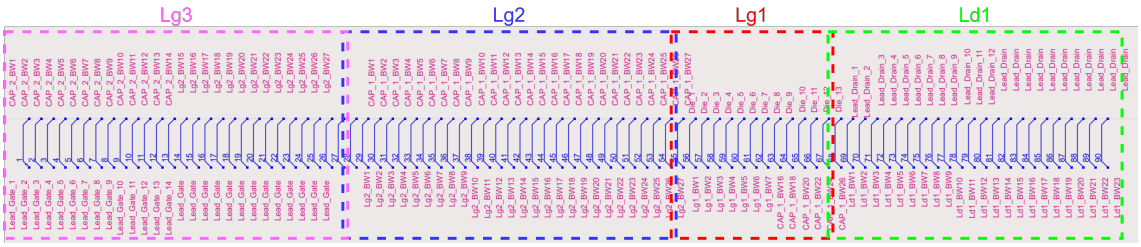


FIGURE 5.7: A single bond wire array model [14] of 90 wires in ADS. The single array is split into four arrays, indicated with the dashed lines, where the colour corresponds to Figure 5.6.

Figure 5.7 represents a single bond wire model in ADS segmented in multiple arrays where the colours correspond to the colours in Figure 5.6. The bond wire shape definitions are

generated by the BWT for each array (Lg1, Lg2, Lg3 and Ld1). Figure 5.8 and 5.9 contain screenshots of the 3D view, illustrating the location and bond wire shape for the different arrays.

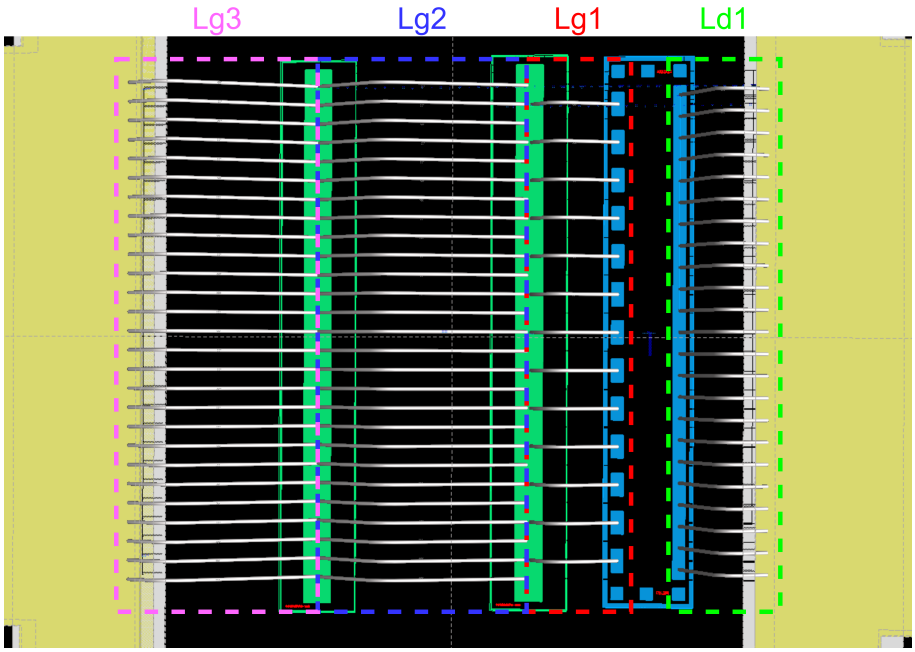


FIGURE 5.8: Top view in the layout editor in ADS. The bond wire array placement corresponds to Figure 5.6.

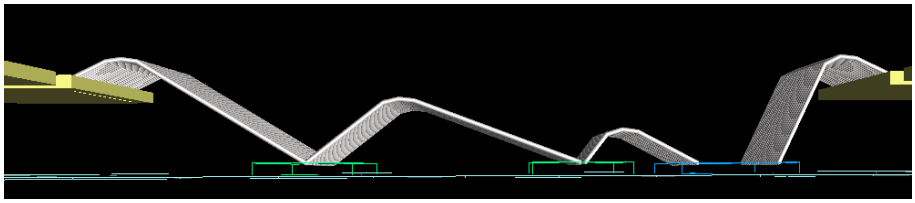


FIGURE 5.9: Side view in the layout editor. The gate lead is located on the left, and the drain is on the right side of the figure.

5.4.2 Rail modelling

The rails mainly act as a landing path for the bond wires, but also as a conductor for the signal to travel in unwanted directions, resulting in reduced performance of RF amplifiers [2, 7]. Integrating this effect while still maintaining the voltage distribution, sections of transmission line are connected between the bond wires in the schematic.
Figure 5.10 presents a small section of the capacitor metal rail constructed by transmission line. It should be noted that the capacitor is formed by the metal rails and ground plane with the dielectric substrate in between. However, the actual capacitor used typically includes additional capacitance. To account for this, additional lumped capacitors have been added to the model to match the total expected capacitance.

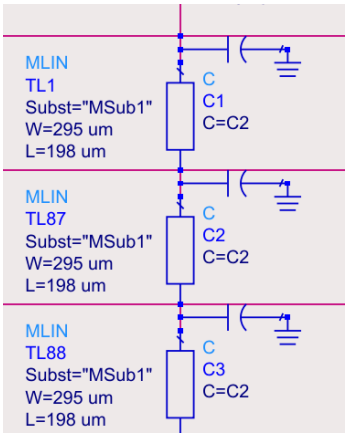


FIGURE 5.10: Capacitor moddeling.

The drain rail is modelled differently. The die contains 13 active cells, while the drain leads are connected using 23 individual bond wires. The transmission line length between each cell's output manifold and its corresponding bond wire varies depending on its position along the power bar. To accurately model the metal drain rail, transmission lines of varying lengths were added based on the positions of the Ld1 bond wires relative to the output manifolds of the active cells. Furthermore, no additional capacitance is required.

Since the metal bars consist of multiple small transmission line segments, standing waves caused by oscillations are omitted. The longest metal rail is located on the capacitors with a length of $5610\mu m$. This means that the smallest frequency that fits in the metal bar is around:

$$f = \frac{v}{\lambda} = \frac{\frac{c}{\sqrt{\epsilon_r \mu_r}}}{\lambda} = \frac{\frac{299792458}{\sqrt{12.1*1}}}{5610 * 10^{-6}} = 14.93GHz \tag{5.1}$$

This means that the first resonances can exist on half of that, which is $7.47GHz$. This is just above the 3rd harmonic of the device's operating frequency.

5.5 Reference model results and limitations

To evaluate the model's performance, two types of simulations have been conducted. First, the AC-simulation was used to validate the design by the inductance values of the bond wire arrays. Secondly, Harmonic Balance (HB) simulations, in combination with load sweeping, have been performed to evaluate the large-signal behaviour of the device. Both simulation results are included and discussed.

5.5.1 AC simulation results

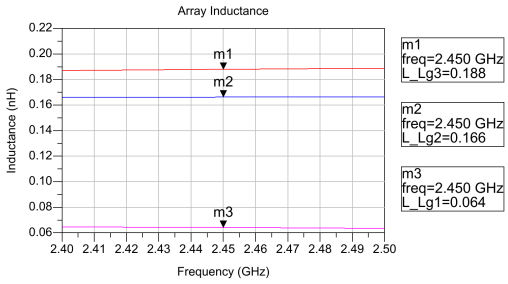
The first step is to validate the total inductance values of the arrays. It is impossible to extract the array inductance from the model directly. Therefore, AC simulations are required to measure the current and voltage drops over the bond wires of each array. Then, the individual bond wire inductance is calculated using:

$$Lg1_{BWx} = \frac{imag(Z)}{2 * \pi * freq * 10^{-9}} \tag{5.2}$$

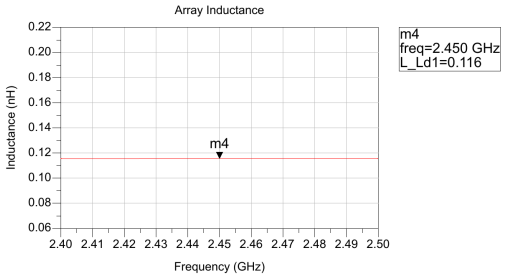
where $Z = \frac{V}{I}$. V represents the voltage drop across one bond wire. The total array inductance is then calculated by:

$$\frac{1}{Lg1} = \sum_{x=1}^{x} \frac{1}{Lg1_{BWx}} \tag{5.3}$$

where x represents the bond wire number. Results from AC-simulations are plotted in Figure 5.11. The inductance values are in close agreement with the calculated inductance value by the BWT shown in table 5.2.



(A) Gate array inductances of Lg1, Lg2 and Lg3.



(B) Drain array inductance of Ld1.

FIGURE 5.11: Bond wire array inductance of the full-scale reference model

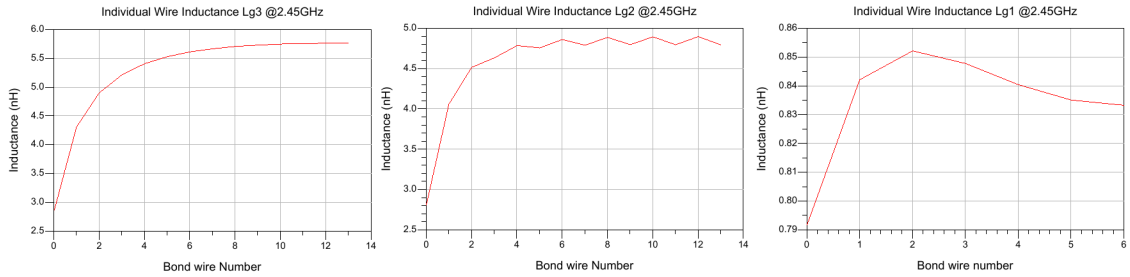


FIGURE 5.12: Individual wire inductance over the bond wires in the array. Bond wire number 0 corresponds to the outer edge bond wire of the array, 14 (or 6 in the case of Lg1) indicates the center bond wire in the array.

The bond wire inductance distribution is analyzed using equation 5.2, as shown in Figure 5.12. Notably, the outer edge bond wire (labelled as bond wire number 0) has the least inductance due to the mutual coupling included in the model [14]. The description of the bond wire model in ADS states that it assumes a uniform current distribution while calculating the wire inductance. However, Figure 5.13 shows that the majority of the current is flowing through the outer edge bond wires. The only exception is the bond wire array connecting capacitor 1 to the gate of the die. Here, the current is concentrated in the middle. This is most likely due to the discontinuity in the number of bond wires in the first array compared to the other two arrays. Either way, the distribution over the power bar is non-uniform, resulting in the cell operating under different conditions. Therefore, the model can simulate the effect of different operating conditions on the power bar.

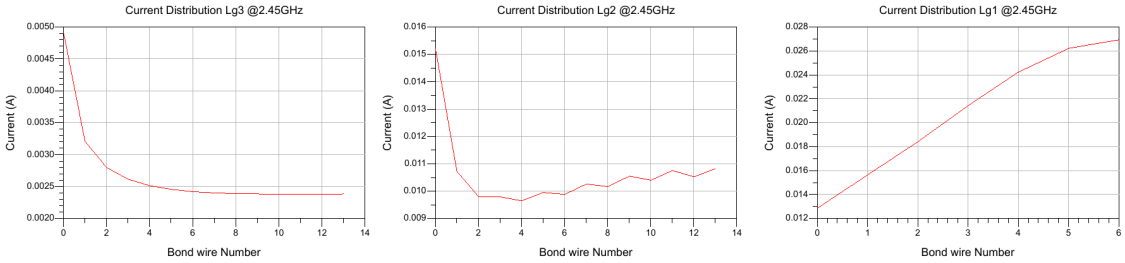


FIGURE 5.13: Current distribution over the bond wires for the gate arrays. Bond wire number 0 corresponds to the outer edge bond wire.

5.5.2 Load pull simulation results

To investigate large-signal behaviour, load-pull simulations are conducted. The gate bias is set to $V_{gs} = -5V$ to ensure class AB-operation, and the drain bias is fixed at $V_{ds} = 50V$. The load sweep region of interest is chosen to be approximately the same area as previously shown in Figure 5.5. Figure 5.14 shows the Drain Efficiency (DE) curves from the load pull simulation. The DE is expected to increase exponentially with the output power until the transistor saturates. In Figure 5.14, the graph shows significant efficiency drops along an increase in output power.

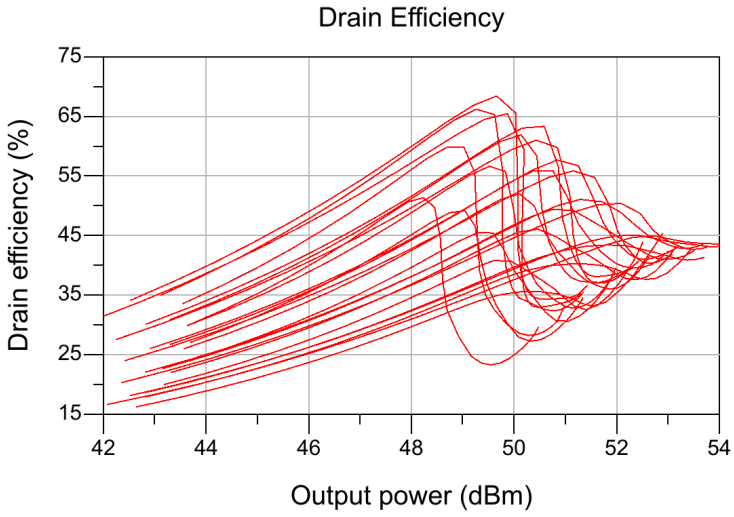


FIGURE 5.14: Drain efficiency curves unoptimised model.

A drop in DE by increased output power levels is typically caused by unwanted secondary effects. In Figure 5.15, it is seen that the complex impedances of individual cells act differently with an increase in input power. The complex impedance is a function of the current and voltage (including the phase) and therefore contains information about the operating conditions of each cell. In this case, the impedances are not closely located and do not follow the same trajectory as a function of input power. If the phase of the output signal for each cell is different, it can lead to a destructive combination of the signal, which could explain the drop in DE seen in Figure 5.14.
The datasheet states that the DE of the CLF24HLS300P power amplifier is approximatly 74%. This means that the impedance pulling should not be as significant in the real world. Therefore, there should be a cause that could explain this discrepancy.
The log file generated by the simulator reveals issues related to the model's convergence.

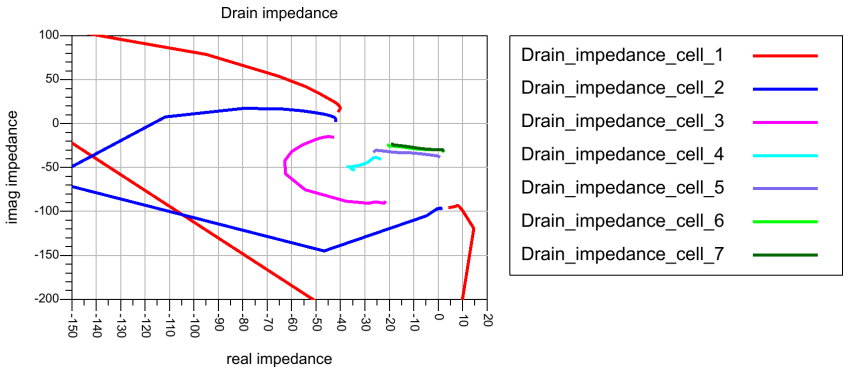


FIGURE 5.15: Complex drain impedance (fundamental frequency) as a function of the input power across the powerbar seen by each cell. Cell 1 is the outermost cell, and Cell 7 is the center cell.

Since multiple devices are connected via metal rails (transmission lines), their operating characteristics influence one another. This means that if their neighbour's characteristics change, their characteristics will change. Due to these interactions, the step-by-step calculations fail to converge on a single solution, resulting in non-converging simulations. The step-by-step approach of the simulator does not converge, which explains the discrepancy between the results and the measured data.

5.5.3 Model conclusion and limitations

The background indicated that multiple factors can significantly impact the performance of high-power RF amplifiers. These factors include impedance pulling [2], rail effects [7], and variations in impedance values of the bond wires [13]. To accurately model these complex interactions, the bond wire model in ADS was incorporated into a single schematic, alongside transmission lines to simulate the effects of metal rails.
Simulations of the model show different results compared to the measured data reported in the device's datasheet. The main reason for this discrepancy is the impedance pulling effect, which hindered the simulator from converging on a solution. In addition to this issue, the model also has further limitations, including the assumption of uniform current distribution and the absence of temperature influence. Notwithstanding these limitations, the model offers a significant advantage in uncovering optimisation techniques related to bond wire heights.

Chapter 6

Simulation and results of optimisation strategies

Using the model developed in the previous section, it is possible to adjust the height of individual bond wires to optimise various operating characteristics. The height is manually tuned to achieve a uniform distribution in the simulation result. Since the AC simulation is sufficiently fast, this process does not require a significant amount of time. Load-pull simulations are then performed with different height distributions to evaluate the device's large signal performance.

6.1 Current Phase

Multiple sources have emphasised the significance of current phase distribution in device performance, indicating that optimising phase characteristics can enhance overall performance. Increasing the electrical length of individual bond wires will slightly delay the signal. The height can, therefore, be altered to achieve a more uniform current phase distribution.

6.1.1 Gate current Phase

Figure 6.2b shows the red line representing the current phase distribution at the gate (after the signal passed the wires of Lg1). At the outer edge bond wire (bond wire number 0), the phase is ahead of the middle bond wire by approximately 50 degrees. The height of the outer bond wires has been increased to increase the electrical path, delaying the current at the edges. In the center, the wires have been slightly lowered to reduce the electrical length. The blue line in Figure 6.2b is the new current phase distribution at the gate. The height distribution of Lg1 is presented in Figure 6.2b and a 3D view in 6.2a.

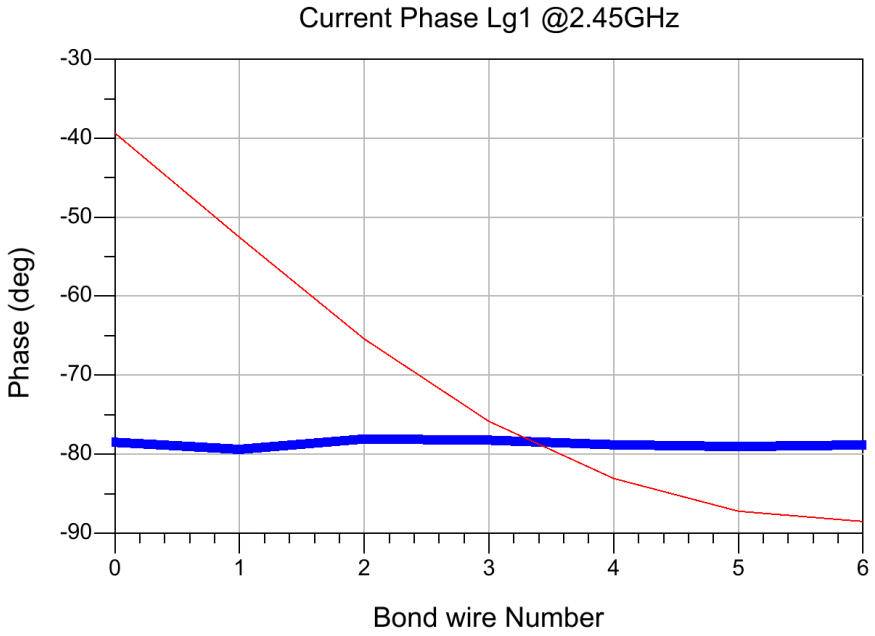
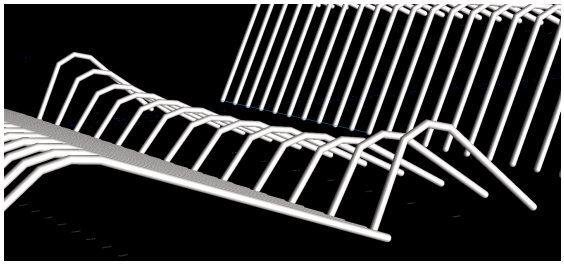
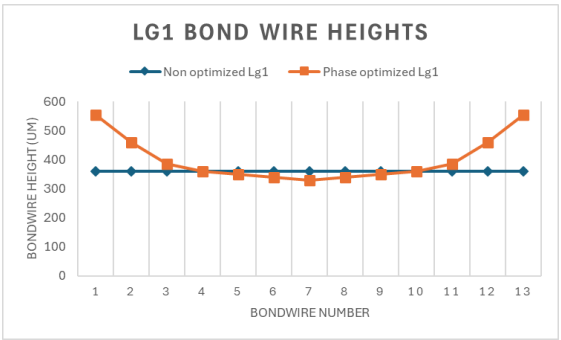


FIGURE 6.1: The original current phase (red line) where the current in the outer edge cells (on the left) is ahead of the current in the center cells. The gate bond wire height has been optimised in a way that the current phase is uniform over the gate (blue line).



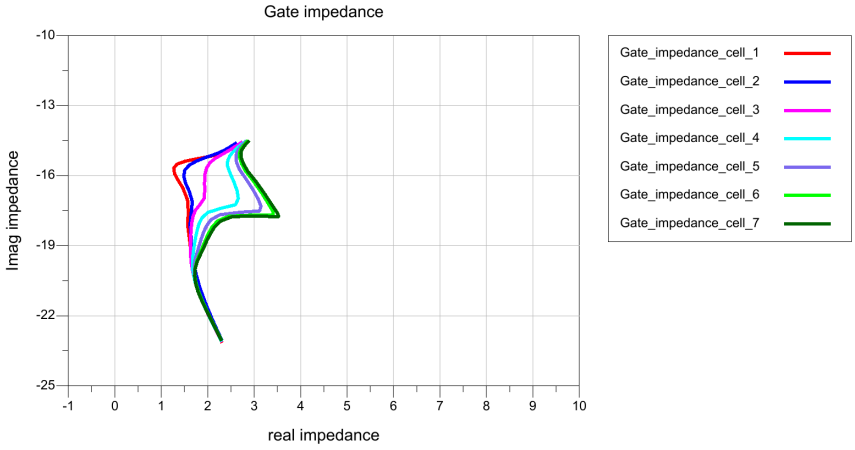
(A) 3D view of Lg1.



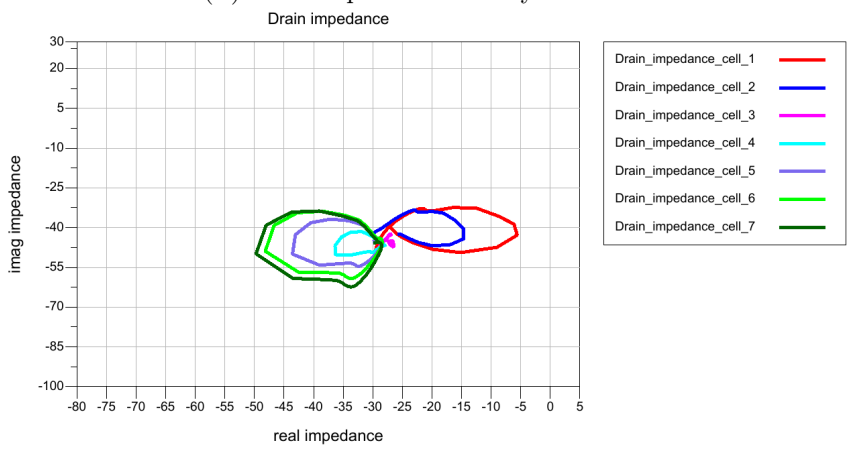
(B) Bond wire height distribution.

FIGURE 6.2: Lg1 bond wire height distribution for gate current phase optimisation.

From Figure 6.2a, it can be observed that only the bond wire height of array Lg1 has been altered. While Lg2 and Lg3 also introduce phase shifts, modifying their heights could help mitigate these effects. Nonetheless, adjusting the height of a single array to compensate for the total delay is a more straightforward approach. Given that Lg1 is directly connected to the gate of the die and shares the same current amplitude and phase, it is preferred for this optimisation technique.
Performing load pull simulation, including the current phase optimised height distribution, multiple warnings about convergence issues were reported in the log file. A closer examination of the impedances of the die itself revealed significant differences along the array as a function of the available input power (see Figure 6.3). With an available power input of 30 dBm, the gate impedance values are all closely clustered together. However, as the available input power increases, gate impedance values diverge. Despite convergence problems rendering the results unreliable, it is worth noting that the fluctuations in the fundamental drain impedances have decreased substantially compared to the drain impedance reported in Figure 5.15. This observation suggests some improvements in the uniformity of the operating characteristics, although further refinements are needed to ensure the simulator converges.



(A) Gate impedance seen by the cells.



(B) Drain impedance seen by the cells.

FIGURE 6.3: Impedance distribution over the cells in the power bar ($Z_L = 2.075 - j1.090$).

6.1.2 Drain current Phase

Figure 6.4 displays the new phase current at the drain in blue, and the original current phase in red. Notably, the original phase difference in the drain bond wire amounts to only about a couple of degrees. In contrast to the gate matching structure, which features an Double Lowpass (DLP) filter that introduces significant phase shifts along the array, the drain matching structure is relatively simple. Consequently, the improvement in uniformity of the current phase at the drain due to optimised drain bond wire heights is limited, and only small gains are realised.

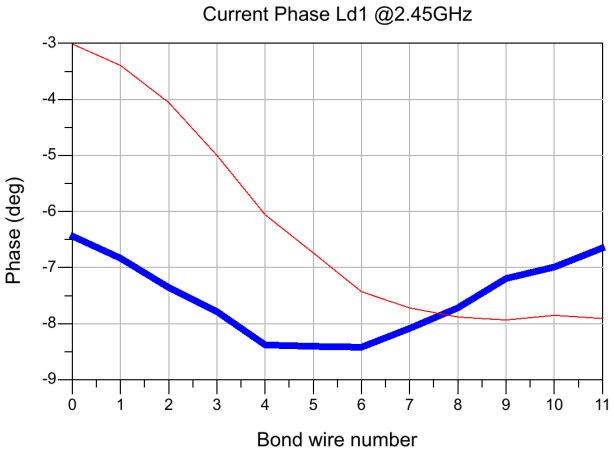
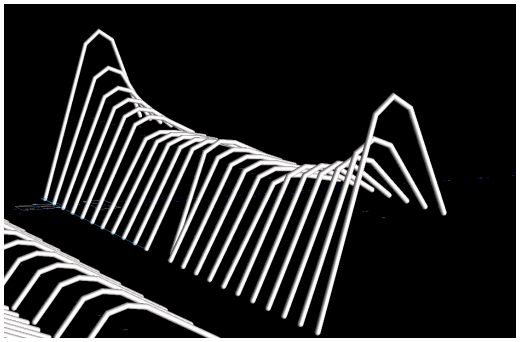
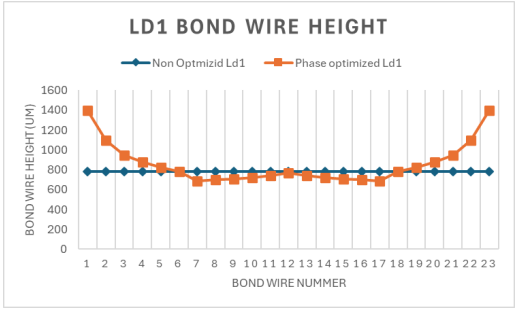


FIGURE 6.4: The original current phase (red line) where the current in the outer edge cells (on the left) is ahead of the current in the center cells. The drain bond wire height has been optimised in a way that the current phase is uniform over the gate (blue line).

Although the improvement in current phase uniformity is modest, significant increases were made to the height of the outer edge bond wires, as illustrated in Figure 6.5. Unfortunately, these increased heights render the bond wires incompatible with the package design and make them non-producible. Notwithstanding the omission of thermal feedback from the temperature increase in the bond wires, it is expected that smaller height increases would be sufficient to achieve a more uniform current phase. Simulations have therefore been conducted, despite the impracticality of implementing bond wires with such high heights.



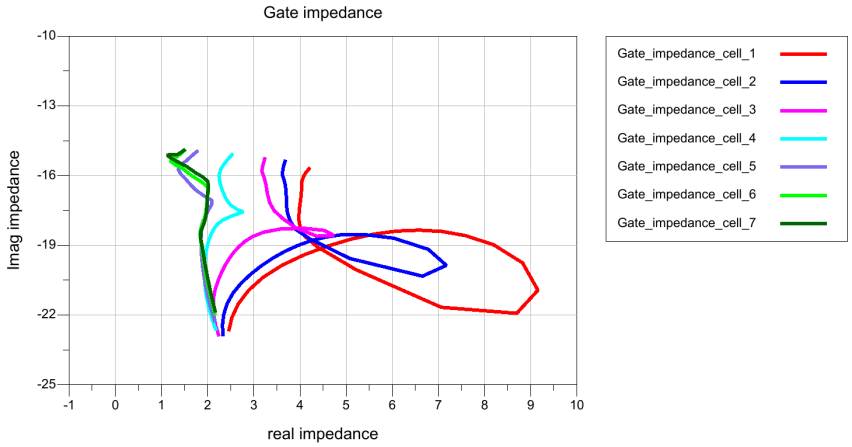
(A) 3D view of Ld1.



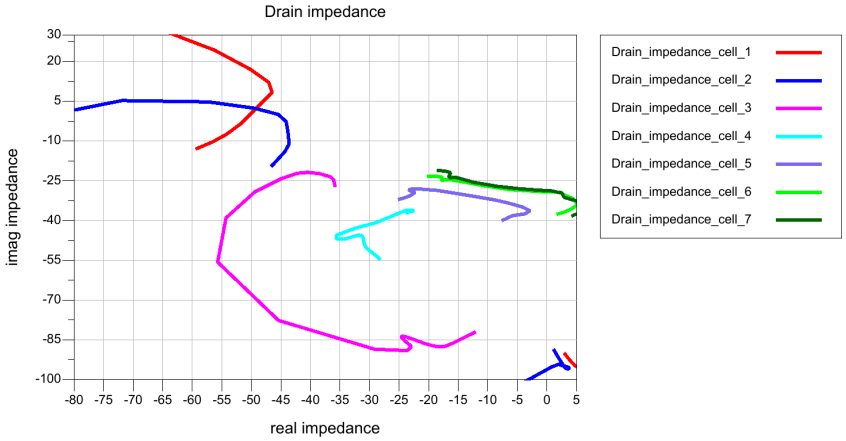
(B) Bond wire height distribution.

FIGURE 6.5: LD1 bond wire height distribution for drain current phase optimisation.

Performing load pull simulations with the new Ld1 bond wire height distribution yields convergence issues. A comparison between Figures 6.6 and 5.15 reveals that there is little to no improvement in the uniformity of operation characteristics for the power bar. This suggests that altering the bond wires at the gate has a more significant influence on the drain impedance characteristics than modifying the bond wire heights at the drain.



(A) Gate impedance seen by the cells.

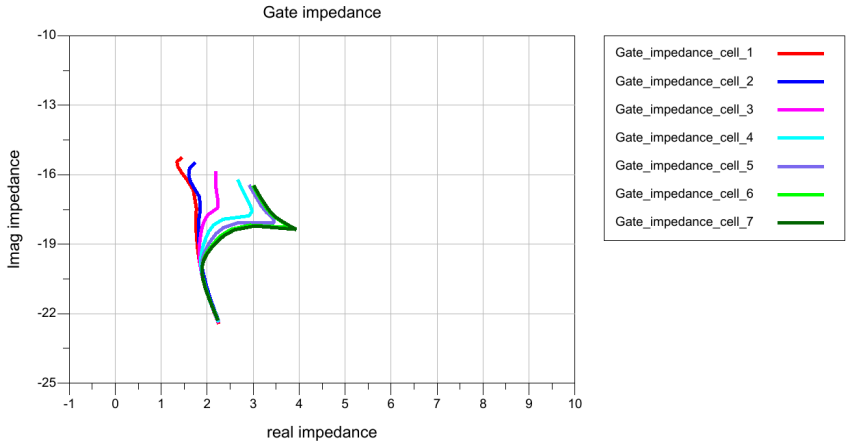


(B) Drain impedance seen by the cells.

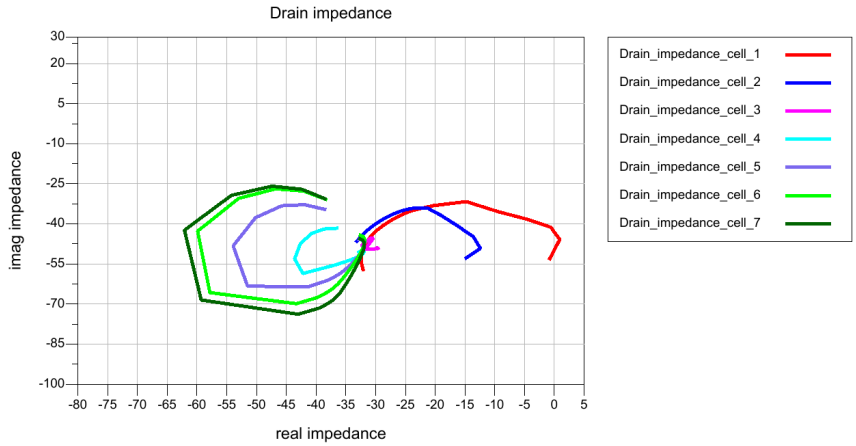
FIGURE 6.6: Impedance distribution over the cells in the power bar ($Z_L = 2.150 - j1.081$).

6.1.3 Combined current phase

With both the gate and drain bond wire arrays optimised to enhance current phase distribution uniformity, load pull simulations will be conducted on a device featuring these optimised configurations. The operating impedances, as shown in Figure 6.7, demonstrate results that are closer to those in Figure 6.2b than to those in Figure 6.6. This observation suggests that the modifications made at the gate have a more pronounced impact on the overall device performance.
Due to the persistence of convergence problems in all load-pull simulations, it is impossible to plot reliable contour lines to determine the optimal operating load value. Consequently, drawing a reliable conclusion from current and voltage distributions over the power bar is challenging.



(A) Gate impedance seen by the cells.



(B) Drain impedance seen by the cells.

FIGURE 6.7: Impedance distribution over the cells in the power bar ($Z_L = 2.196 - j1.062$).

Examination of the Drain Efficiency (DE) curves reveals that impedance oscillations are still present after optimising for the current phase (see Figure 6.8). The most effective approach to resolving convergence issues appears to be isolating the individual cells to mitigate the impedance oscillations. Therefore, the following simulations will be based on segmenting the rails to increase the isolation between all cells.

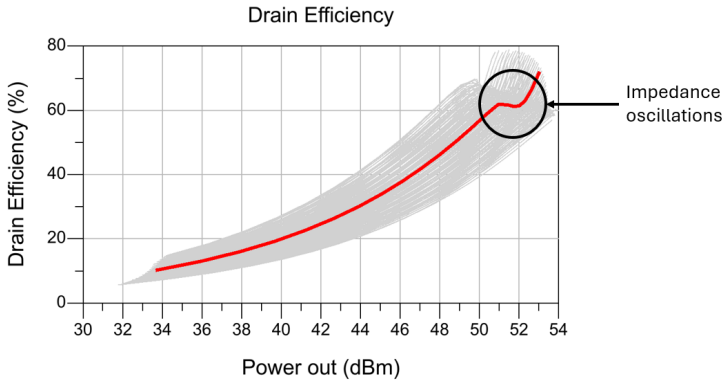


FIGURE 6.8: Drain efficiency plot indicates impedance oscillations present after improving the current phase distribution.

6.2 Rail segmentation

The metal rail is segmented into separate pieces to mitigate impedance oscillations, thereby increasing the isolation between individual cells. This modification aims to prevent the propagation of signals from one cell to another, as discussed in further detail below.

6.2.1 Drain Rail cuts

In the original device, the drains of all 13 cells are connected via a common drain rail. This shared metal structure facilitates bonding to the package lead using 23 bond wires. Since the number of cells (13) and bond wires (23) are prime numbers, it is impossible to divide the rail into equal sections. Since the oscillations are extending the simulation time, it is decided to make as many cuts as possible. There are four points in the rail where only a transmission line is between two bond wires (and no drain of a cell is connected). These transmission lines are subsequently deactivated to isolate the individual cells from each other. This modification also implies the disappearance of capacitance between these transmission lines and ground, which could potentially affect device performance. However, in simulations, the differences were not significant enough to notice and are therefore assumed to be negligible.

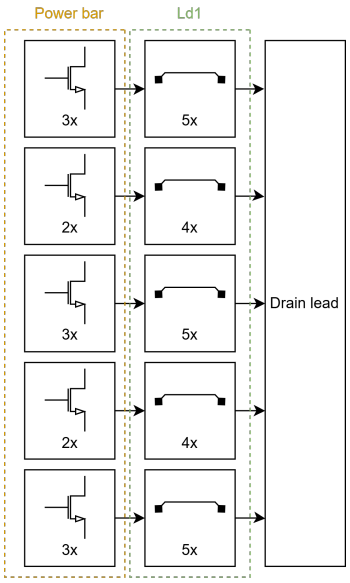


FIGURE 6.9: Block diagram of the segmentation by drain rail cuts.

The power bar configuration has been revised to a 3-2-3-2-3 arrangement, with each section connected via 5-4-5-4-5 bond wires, respectively. Since the schematic is too large to present in this report, only a block diagram is shown in Figure 6.9. In this configuration, the blocks are isolated from one another, connected solely through the bond wires and leads.

Load-pull simulations conducted on the configuration depicted in Figure 6.9 have resulted in further convergence problems. Unfortunately, these issues have prevented the simulator from finding a solution, rendering the simulation results unusable. As a result, no reliable data can be presented for this simulation.

6.2.2 Segmenting capacitor 1 rail

The gate bond wire array (Lg1) does not connect directly to a shared "gate rail" on the power bar itself. Instead, each cell features its dedicated landing pad for each bond wire, isolating all gates from one another. This configuration implies that cells can only interact with each other through the Lg1 bond wires and the capacitor rail.

As discussed in Section 6.1, it has been observed that device performance is susceptible to small changes on the gate side of the device. Given this information, further investigation into the possibility of isolating cells by cutting the rails becomes an intriguing option.

The first candidate for segmentation of the rail is the metal bar atop capacitor C1. It is essential to note that this metal bar forms an integral part of the capacitor itself, and any cuts made may potentially affect its capacitance value. For the sake of this analysis, it is assumed that the change in the capacitor's capacitance is negligible. With this consideration in mind, the metal bar on capacitor C1 has been cut at four locations, as depicted by the red dotted lines in Figure 6.10. There is slightly more flexibility in determining the optimal cut location for the capacitor's metal bar than for the drain rail. Various placements of cuts have been explored, but not all solutions have yielded convergent simulation results. Notably, isolating the outer cells has proven particularly crucial, as will be demonstrated through load-pull simulation results later on.

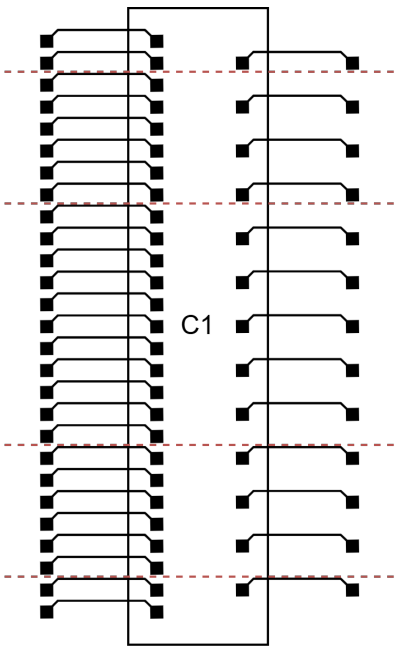
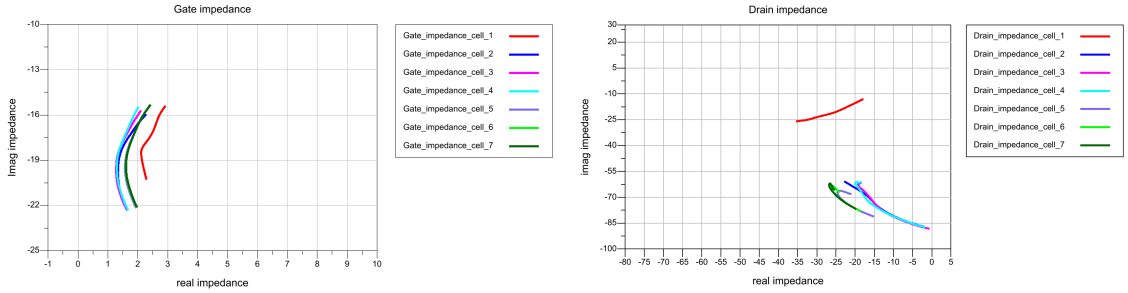


FIGURE 6.10: Cuts made on capacitor 1 rail.

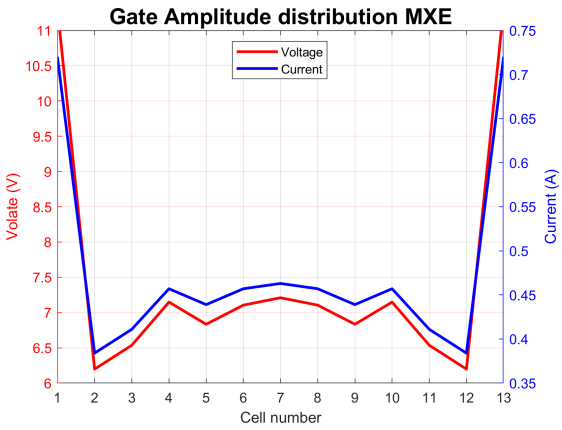
Since the result converged, the MXE and MXP could be identified in the contour lines. Consequently, the impedance of each cell could be investigated at its peak efficiency point. The impedances are presented in Figure 6.11. Inspection of this figure reveals that all cells exhibit very similar impedance characteristics across the entire available power sweep. The only notable exception is Cell 1, which shows distinct impedance behaviour. Specifically, the real impedance at the gate of Cell 1 is slightly higher than its counterparts. Conversely, the drain impedance of Cell 1 exhibits a different trend as input power increases. These



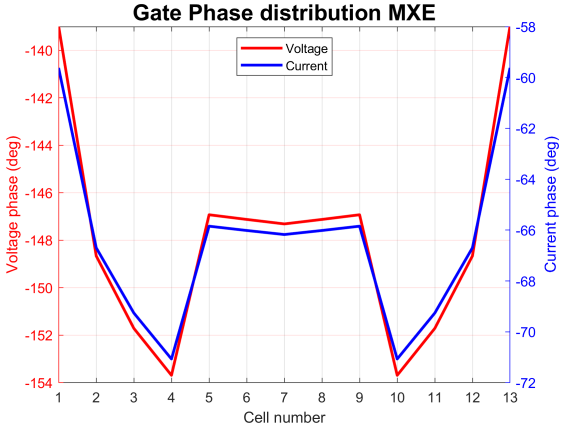
(A) Gate impedance seen by the cells.

(B) Drain impedance seen by the cells.

FIGURE 6.11: Impedance distribution over the cells in the power bar ($Z_L = 1.923 - j0.252$).



(A) Voltage and current amplitude distribution over the gate of the cells in the power bar.



(B) Voltage and current phase distribution over the gate of the cells in the power bar.

FIGURE 6.12: Voltage and current distributions over the power bar at the gate for the max efficiency point ($Z_L = 1.923 - j0.252$).

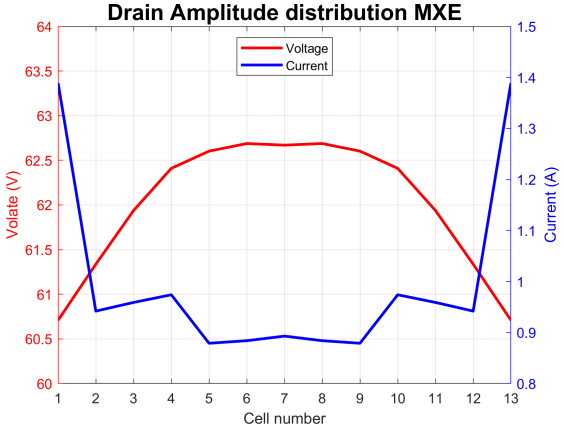
differences underscore the importance of isolating outer cells via the cuts made in Figure 6.10.

According to [7], cutting the metal rails has been shown to enhance the voltage distribution within the device, leading to improved overall performance. The complex impedance, as a function of both voltage and current, provides information about the device's operation. Figure 6.12 presents a plot of the voltage and current across the power bar, providing insights into the amplitude and phase characteristics of the device's operation, which reveals a more uniform distribution of currents and voltages. To further explore this phenomenon, Figure 6.12 presents a plot of the voltage and current across the power bar, providing insights into the amplitude and phase characteristics of the device's operation at MXE.

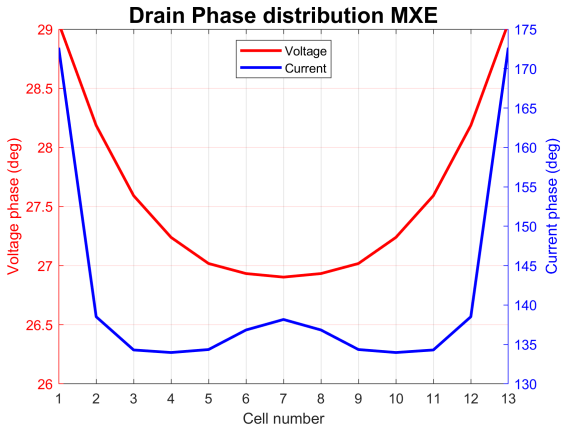
An examination of Figure 6.12 reveals that the operating conditions at the gate differ significantly between he outer cells (cell 1 and 13) and those in the middle region (cells 2-12). The isolation of outer cells via cuts exhibits a similar effect to the work of I. Volokhine. Despite convergence problems, a direct comparison of the voltage and current distribution improvements between the original and modified configurations is not feasible. However, analysing the impedance plots (which are inherently linked to both voltage and current distributions) reveals convergent results, suggesting that this phenomenon may indeed translate to a more uniform distribution within the device.

The middle cuts also contribute to the avoidance of convergence problems. Simulations conducted without these cuts resulted in convergence problems, although the effects are not immediately apparent from the amplitude plot 6.12a. However, a closer examination of Figure 6.12b reveals a significant phase difference at cells 4-5 and 9-10. As noted in [7], segmenting the rail is beneficial up to a certain amount of rail cuts before the gains diminish. This is evident from the results, as further segmentation would not lead to significantly improved distribution.

Examine Figure 6.13 reveals that the transistors continue to behave like a voltage-controlled current source since the shape of the output current amplitude is almost identical to the voltage shape in Figure 6.12a. The outer cells produce more current compared to the centre cells due to their difference in operating voltages. The amplitude of the current produced by the outer cells is significantly higher, approximately $\frac{3}{2}$ times that of the cells at the



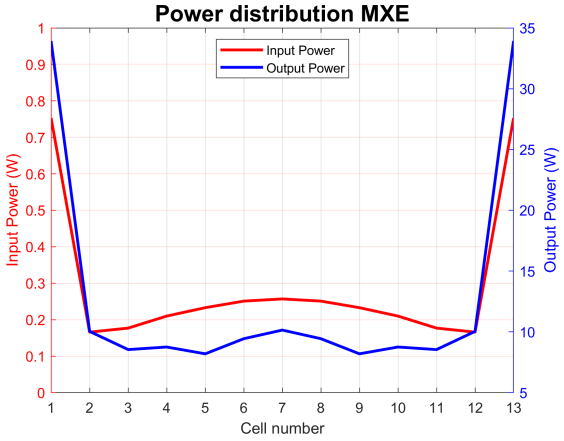
(A) Voltage and current amplitude distribution over the drain of the cells in the power bar.



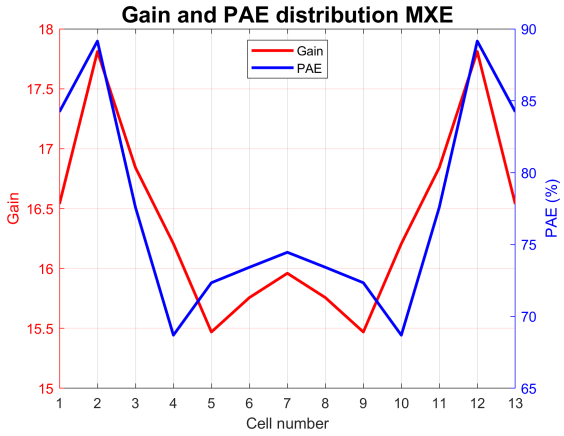
(B) Voltage and current phase distribution over the drain of the cells in the power bar.

FIGURE 6.13: Voltage and current distributions over the power bar at the drain for the max efficiency point ($Z_L = 1.923 - j0.252$).

centre. Moreover, an analysis of the phase angle (figure 6.13b) reveals a substantial phase difference between the outer and inner cells. While the centre cells exhibit only minor differences in phase, amounting to a few degrees, the former are 30 degrees off.
An examination of the voltage distribution at the drain reveals minimal differences between the outer and inner cells. The voltage is off by $1.5V$ and 2 degrees. Given this similarity in voltage behaviour, the shape of the output power is primarily determined by the current. This trend is apparent in Figure 6.14a, which plots the power distribution over the power bar at maximum efficiency.



(A) Input and output power of the cells in the power bar.



(B) Individual cell gain and PAE distribution.

FIGURE 6.14: Power, gain and Power Added Efficiency (PAE) distributions at max efficiency point ($Z_L = 1.923 - j0.252$).

The gain and PAE are provided in Figure 6.14b. It is evident from this figure that the second outermost cells (cell 2 and 12) exhibit the highest PAE, although not providing the most power. In contrast, the outer cells (cell 1 and 13) generate more power but achieve this at a slightly lower PAE. Conversely, the cells located in the center of the power bar

produce less power while operating at slightly lower PAE. Significant differences in PAE exceeding 15% imply that there is potential for further improvements in the distribution and operation of the cells.

Until now, only the distributions of the Maximum Efficiency point (MXE) has been discussed. The device also has a Maximum Power point (MXP), achieved at different load impedance, specifically $Z_L = 2.643 - j1.957$. Notably, there is minimal difference in the voltage and current distributions (and therefore output power). However, differences are observed in terms of PAE and gain, where the distribution becomes more uniform as seen in Figure 6.15. Due to the minor differences, full distributions and operating characteristics at MXP are given in Appendix B.

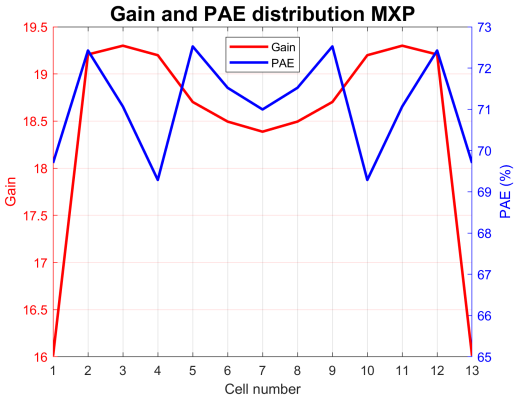


FIGURE 6.15: Gain and PAE for maximum power output point ($Z_L = 2.643 - j1.957$).

To provide an overall perspective on the performance of the device with capacitor rail cuts, Figure 6.16 presents a nose plot. This plot serves as a helpful tool for differentiating between maximum power output and maximum efficiency operating conditions. The objective of employing optimisation techniques is to minimise the distribution effects, thereby enhancing the curve to achieve higher efficiencies or power.

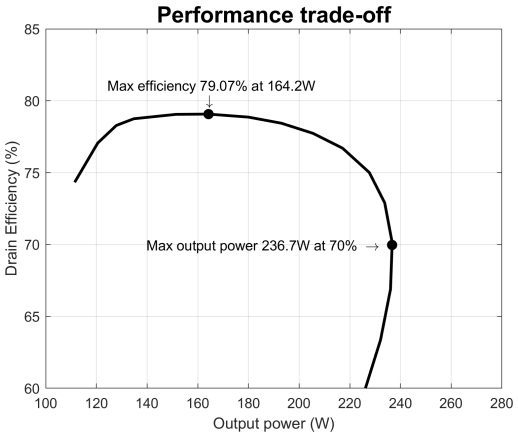
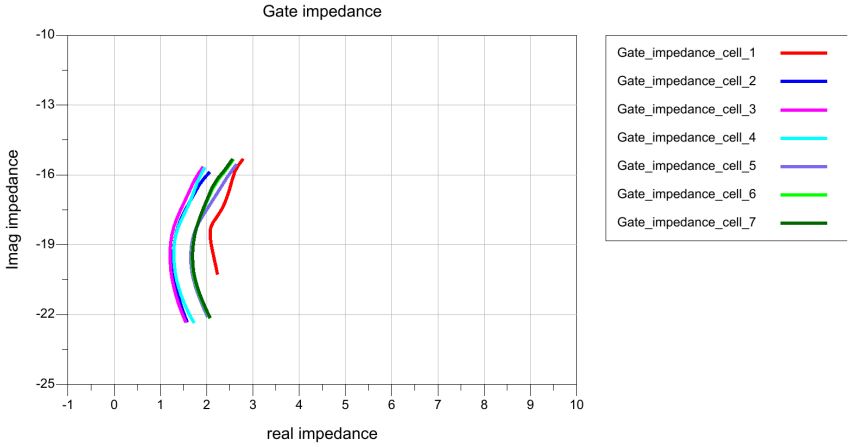


FIGURE 6.16: Performance trade-off curve of the load-pull simulation with cuts in C1.

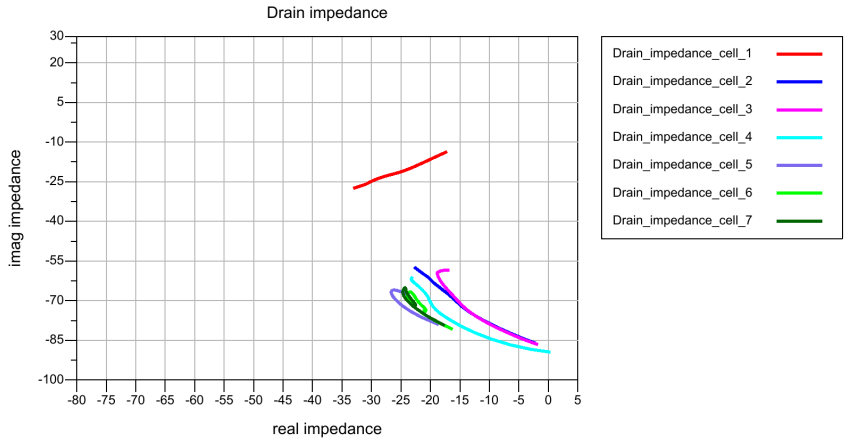
The rail cuts have resulted in the first converging simulations and results. Therefore, these results will be used as a reference when further improvement techniques are employed.

6.2.3 Combining drain rail and capacitor metal cut

Next, the rail cuts from Figure 6.9 and Figure 6.10 are combined, followed by harmonic balance simulations to analyse the changes in behaviour. Figure 6.17 presents the impedances as a function of input power for the MXE ($Z_L = 1.916 - j0.234$).



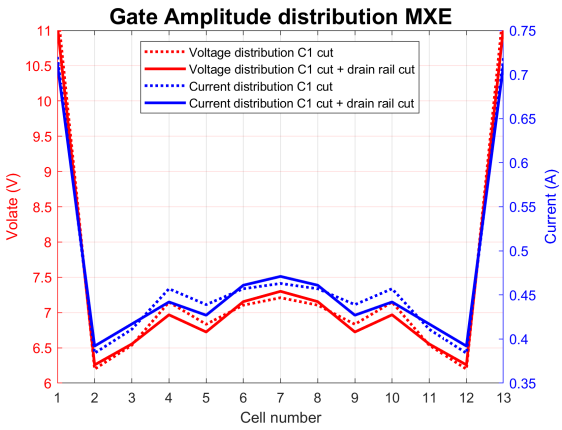
(A) Gate impedance seen by the cells.



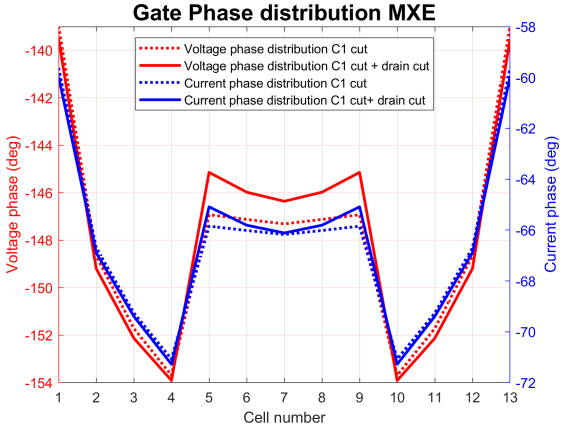
(B) Drain impedance seen by the cells.

FIGURE 6.17: Impedance distribution over the cells in the power bar ($Z_L = 1.916 - j0.234$).

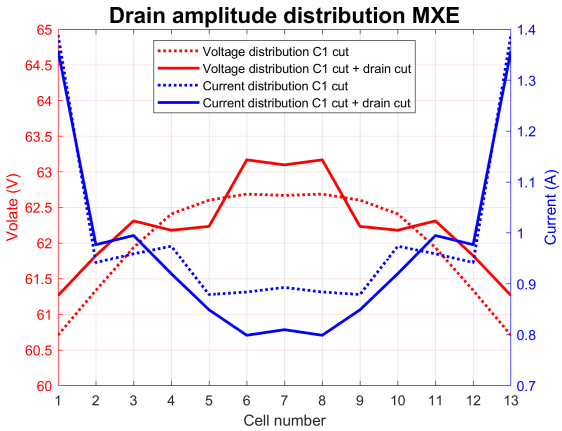
A comparison of the impedances from Figure 6.17 with that shown in Figure 6.11 reveals only minor differences. Notably, at the gate, the impedances of cells 6 and 7 exhibit a slight increase in their real impedance value. For the drain, the spread of the middle cells has become marginally broader. This subtle variation may indicate a decrease in uniformity across the device's output characteristics, which could lead to a corresponding reduction in overall performance.
Figure 6.18 presents the operating characteristics where the capacitor rail and drain rail are cut. A closer examination of Figure 6.18a and Figure 6.18b reveals that there are no significant differences in the gate operation characteristics. However, a more detailed analysis of the drain characteristics indicates some discrepancies. The implementation of rail cuts at the drain has resulted in a reduction in the uniformity of voltage distribution across the cells. This, in turn, results in a decrease in the PAE for cells 6-8 seen in Figure 6.18f.



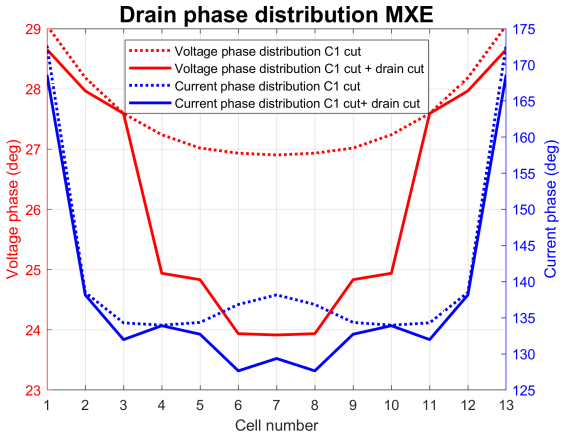
(A) Voltage and current amplitude at the gate.



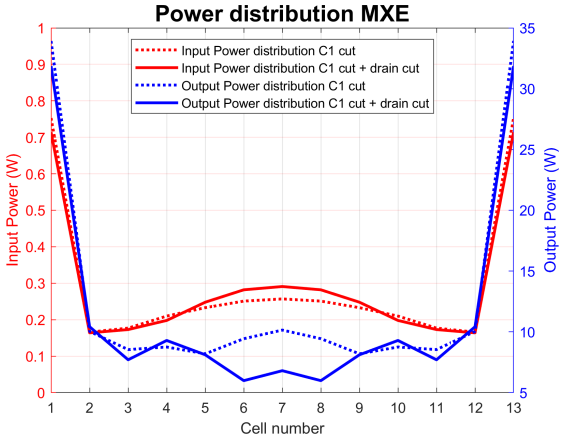
(B) Voltage and current phase at the gate.



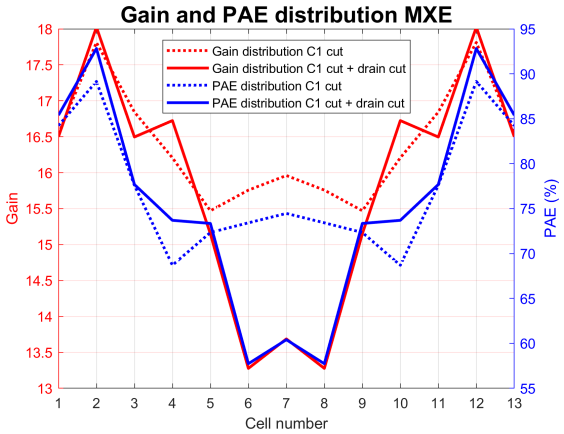
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



(E) In and output power.



(F) Gain and PAE over the powerbar.

FIGURE 6.18: Distributed characteristics and performance at maximum efficiency point ($Z_L = 1.916 - j0.234$).

Furthermore, this drop in performance is also reflected in the overall performance curve of the device. Figure 6.19 shows a slight reduction in performance along the entire curve compared to the simulation results, where only capacitor segmentation was included.

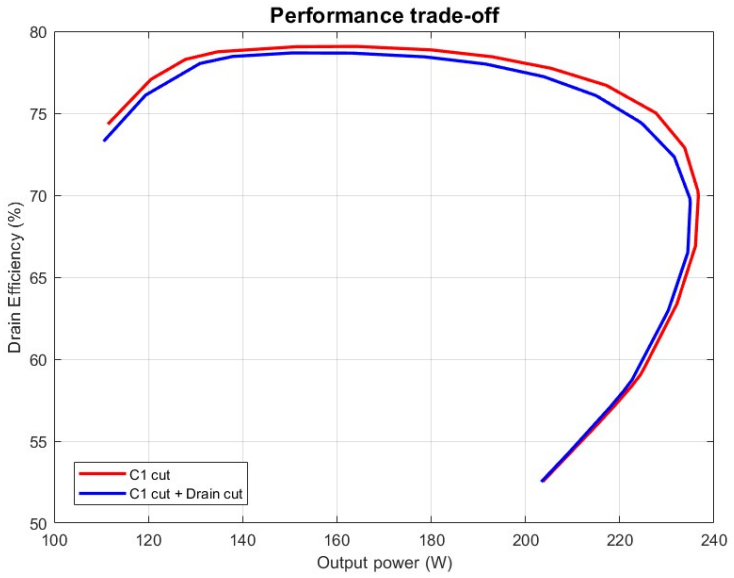


FIGURE 6.19: Performance trade-off curve of the load-pull simulation with cuts in C1 and the drain rail.

Transistors act as voltage-controlled current sources. Improving the voltage distribution over the gate will therefore translate into better overall device performance. Additional rail cuts may enhance the uniformity of the voltage distribution over the power bar, resulting in better drain impedance characteristics. This can prevent oscillations and improve the device's performance.
An attempt was made to improve the uniformity of voltage and current distributions over small sections of the drain rail by introducing additional cuts. However, this effort did not yield the desired improvement in device performance. Instead, a slight decrease in overall device performance was observed.

6.3 Gate capacitor cut combined with phase

Both solutions presented in Section 6.1, which involve modifying the bond wire height to achieve a more uniform current distribution, and those in Section 6.2, where the capacitor rail is cut to improve the voltage distribution at the gate, will be combined in this section. This combination of solutions aims to investigate further the effects of optimising the bond wire height on the overall device performance.

6.3.1 Gate phase current and capacitor rail cuts

The first configuration considered in this section combines the optimised bond wire height for a uniform phase current distribution, specifically the Lg1 height distribution from Section 6.1.1, with the cuts in the capacitor metal rail. Figure 6.20 presents the performance curve for this combination. Comparing these results directly with those shown in 6.19, it becomes evident that both the MXE and MXP have improved.

To gain a deeper understanding of why the device's MXE and MXP are increased, a further look into the operating characteristics is required. Figure 6.21 examines the operating

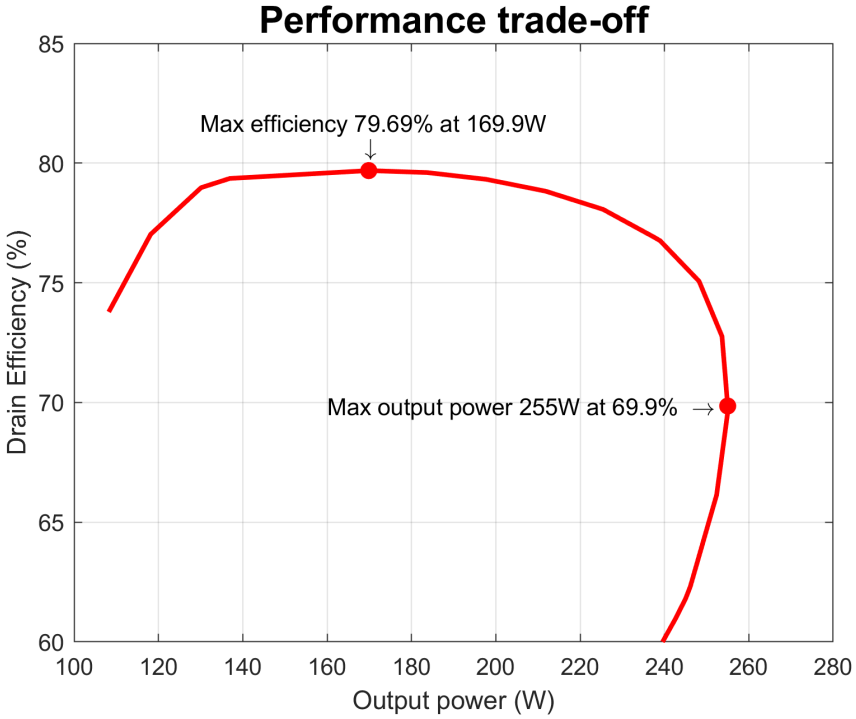
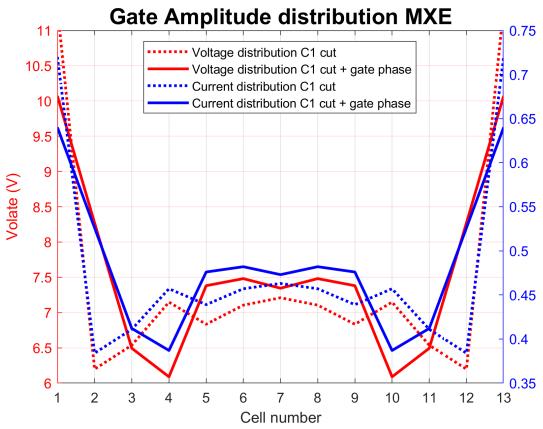


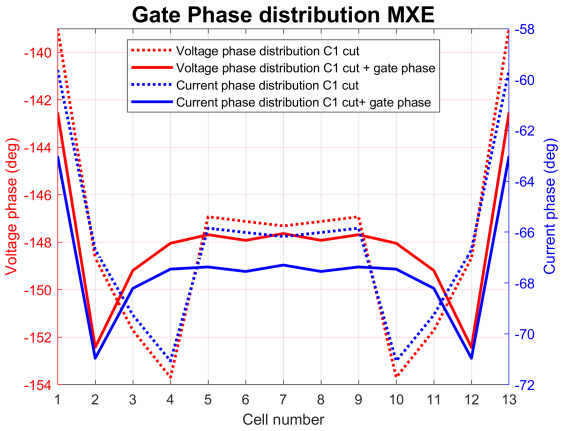
FIGURE 6.20: Nose plot of the combined solution of phase current optimisation from section 6.1.1 and cuts in C1 according to Figure 6.10.

characteristics for the MXE, specifically at $Z_L = 2.130 - j0.195$. Slight differences in the voltage and current characteristics can be observed at the gate compared to the case where only the cuts were placed on the capacitor (dotted lines). Notably, the outer edge cells (cells 1 and 13) exhibit reduced current and correspondingly lower voltages, improving overall uniformity. Conversely, the amplitude of cells 4 and 10 has decreased slightly, resulting in a slight degradation in uniformity.
Figure 6.21b reveals that the current and voltage phases are slightly less ahead at the edges. Furthermore, the increase in phase off cells 3-4 and 10-11 leads to a more uniform phase distribution over the gate.
The improvement in phase distribution at the gate results in a more uniform distribution of current at the drain. Specifically, this results in several notable changes to the current characteristics. Notably, the outermost cells produce less current (approximately $200mA$ less) while the second-most outer cells (cells 2 and 12 in Figure 6.21c) exhibit an increase in current (approximately $150mA$ more). Furthermore, there is a notable difference in the phase characteristics between the drain current and voltage in cells 5-9. This leads to an increase in output power and PAE respectively.

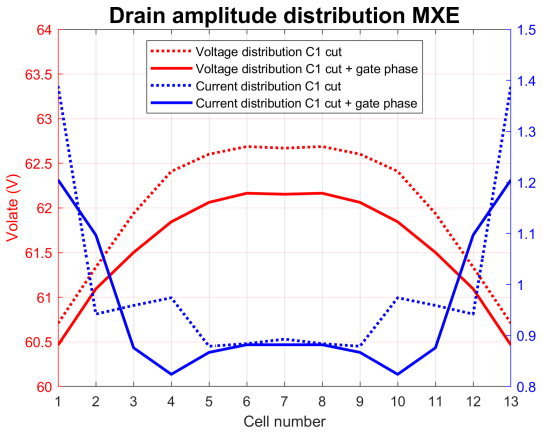
When investigating and comparing the simulation results for the maximum power point, similar trends can be observed (see Appendix B). The only difference is the drain current in the outer cells, where its amplitude remains almost unchanged. This means that the above improvements may contribute to a more cohesive construction of the output currents, ultimately leading to higher output powers. Meanwhile, the increased efficiency of the center cells plays a crucial role in enhancing the overall efficiency at the MXE.



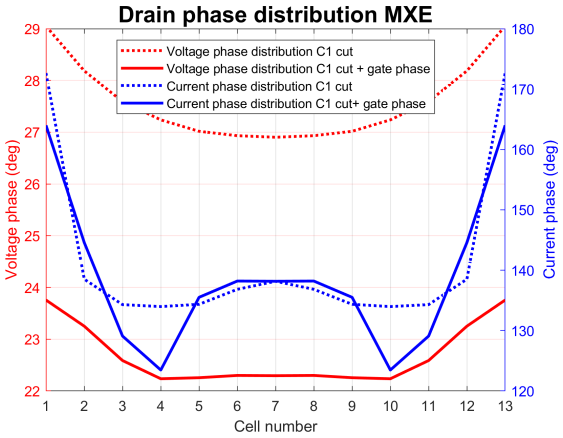
(A) Voltage and current amplitude at the gate.



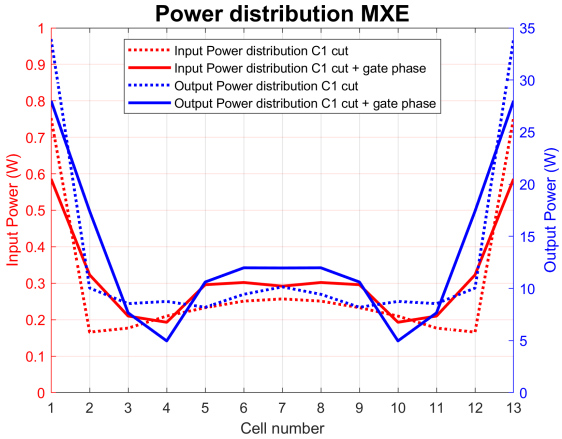
(B) Voltage and current phase at the gate.



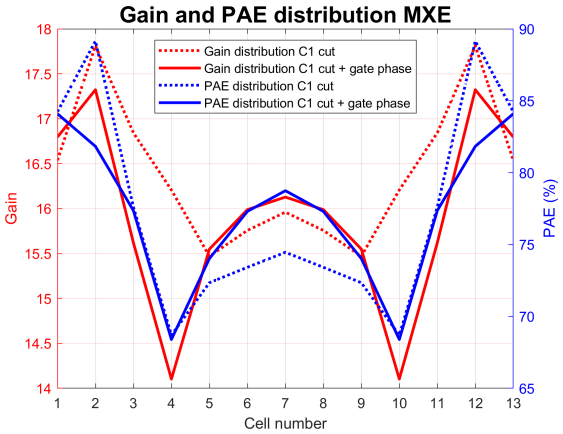
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



(E) In and output power.



(F) Gain and PAE over the powerbar.

FIGURE 6.21: Distributed characteristics and performance at maximum efficiency point ($Z_L = 2.130 - j0.195$).

6.3.2 Drain phase current and capacitor rail cuts

The performance nose plot for the device with C1 cuts and Ld1 height optimisation for the current phase (from section 6.1.2) is presented in Figure 6.22. A comparison of this plot to the nose plot to the device with only the C1 cuts (Figure 6.16) reveals that the MXP remains virtually unchanged. In contrast, the MXE has improved by approximately 0.7%. Despite the gain in DE, the output power at this point has decreased by roughly 9.6W compared to the MXE in Figure 6.20. Although it still outperforms the device with a uniform Ld1 height distribution in drain efficiency (Figure 6.16).

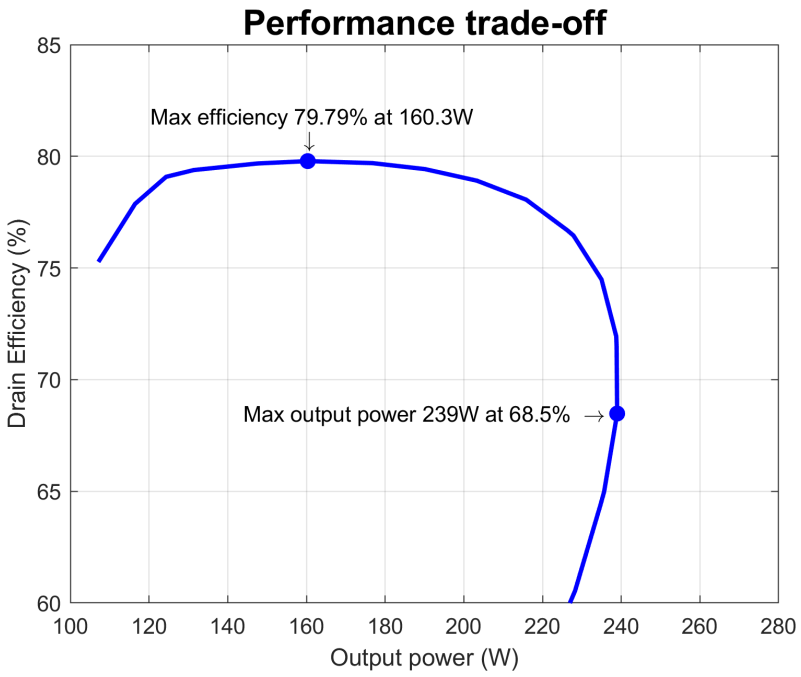
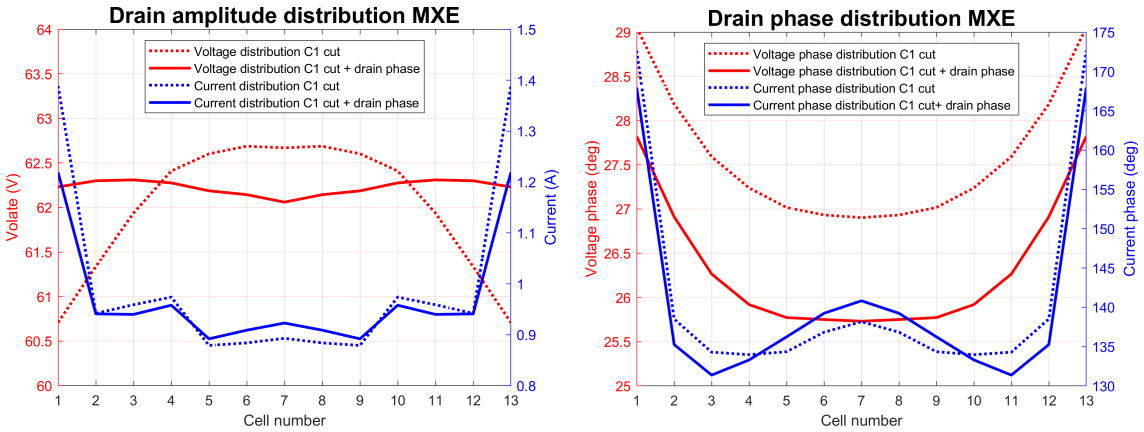


FIGURE 6.22: Nose plot of combined optimisations of the drain phase current from section 6.1.2 and cuts in C1 as in figure 6.10.



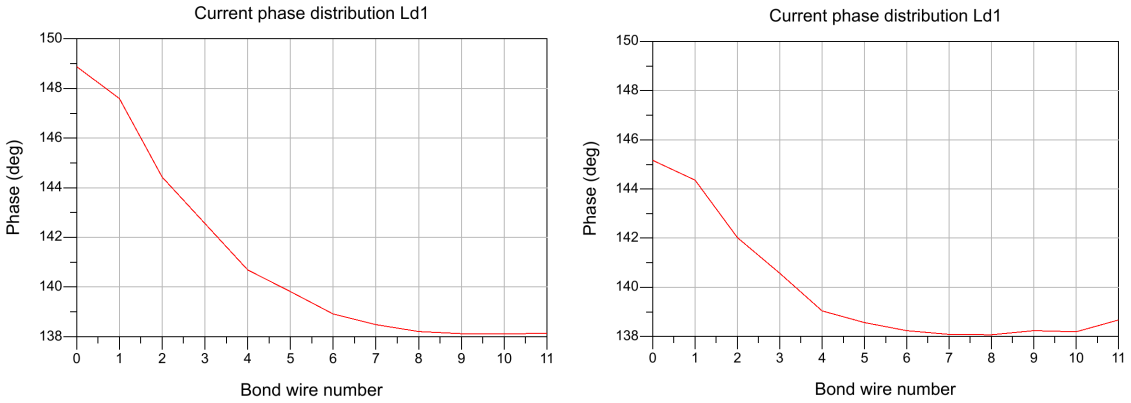
(A) Current and voltage amplitude distribution at the drain.

(B) Current and voltage phase distribution at the drain.

FIGURE 6.23: Distributed voltage and current characteristics at the drain at the maximum efficiency point ($Z_L = 1.962 - j0.228$).

As might be anticipated, the operating characteristics at the gate in this configuration are similar to those observed when all bond wire arrays have the same bond wire height across the entire array. This similarity suggests that modifying the drain bond wire heights does not significantly impact the operating characteristics at the gate. This is a valuable insight, as it indicates that the changes made to the drain bond wire heights do not have a cascading effect on the gate's operation.
On the contrary, the drain characteristics did exhibit a change. As shown in Figure 6.23, the voltage and current at the drain are compared to the results from section 6.2 (dotted lines). Notably, the voltage amplitude has become more uniformly distributed across the manifolds of the cells in the power bar. As a consequence, the current in the outer edge cells has been reduced by approximately $200mA$. In contrast to the distribution observed in Figure 6.21c, the second outermost cells maintain their lower current value, resulting in a more uniform current distribution.
The changes to the current and voltage amplitude distribution are accompanied by relatively small changes in the phase characteristics. Specifically, the voltage phase maintains its original distribution, albeit with a slight shift of only a couple of degrees. In contrast, the current retains its shape but exhibits increased phase differences in the middle region.

At first, it might seem surprising that the phase distribution at the drain is nearly identical to the case where the lead bond wires have the same height. However, this observation is not as unexpected when considering the measurement location. The signal is being measured at the drain of the power bar, which means that this is not the current phase distribution ultimately creating the package lead. Given that the drain efficiency is calculated from results obtained by combining the signals after the bond wire leads, the actual efficiency may be higher, despite the similar phase distribution observed here. Figure 6.24b provides a detailed view of the phase distribution over Ld1 at the side of the packaging lead,

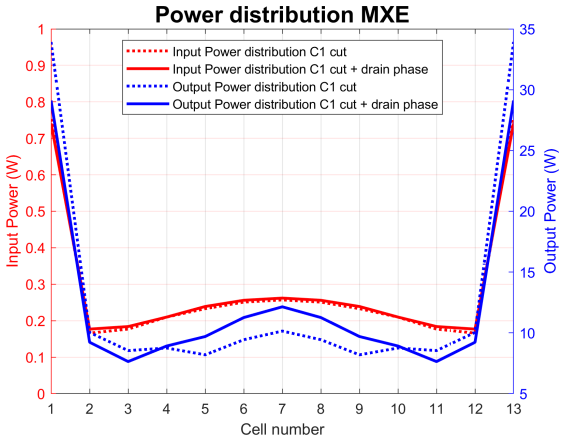


(A) Non-optimised current phase.

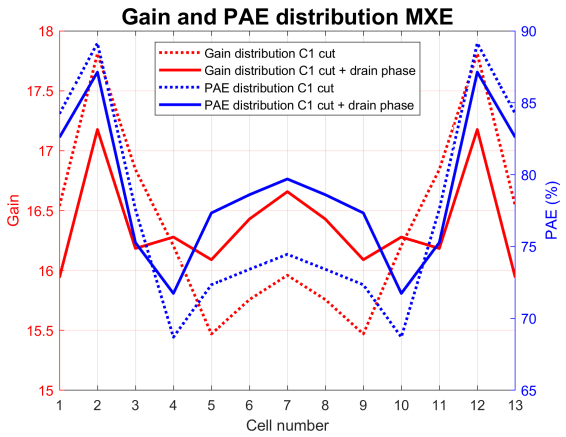
(B) Optimised current phase.

FIGURE 6.24: Non-optimised and optimised bond wire height distribution for the phase of the current where Z_L is taken for the max efficiency point.

The changes observed in Figure 6.23 result in a distinct change in the power output distribution and operating efficiencies of the device. Figure 6.25b reveals that the efficiency of the cells in the centre (cells 4-10) has increased. This observation is consistent with the findings presented in Figure 6.21f, where the optimised Lg1 height for the current phase also resulted in higher efficiency. Notably, in both cases, there is a corresponding increase in PAE in cells in the center of the power bar. The MXP did not have significant changes



(A) Input and output power of the cells in the power bar.



(B) Individual cell gain and PAE distribution.

FIGURE 6.25: Power, gain and Power Added Efficiency (PAE) distributions at max efficiency point ($Z_L = 1.962 - j0.228$).

in its operating characteristics, hence no improvements in the maximum output power are observed.

6.3.3 Current phase optimisation in combinations with C1 cuts

The simulation results will now be discussed, where both height optimisation distributions are implemented in combination with the C1 cuts. The performance nose plot is presented in Figure 6.26, from which it is evident that the performance improves without any trade-off in maximum efficiency or maximum power output.

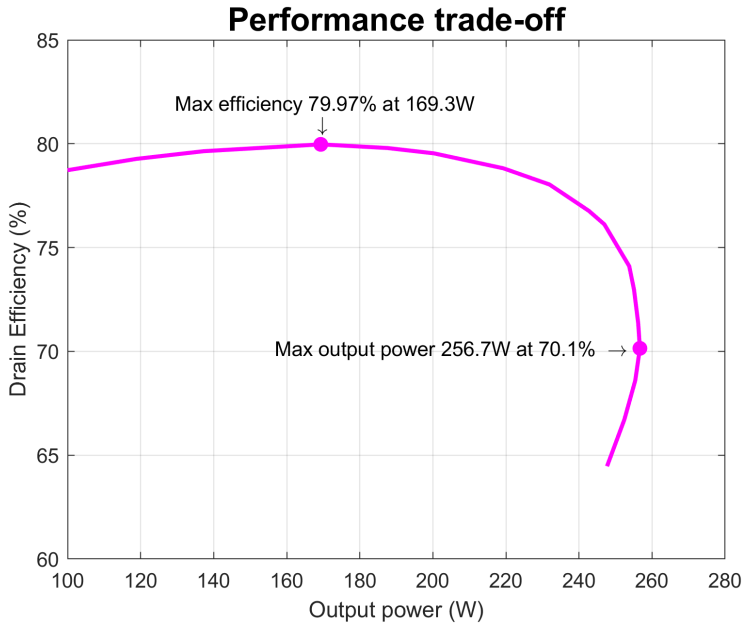
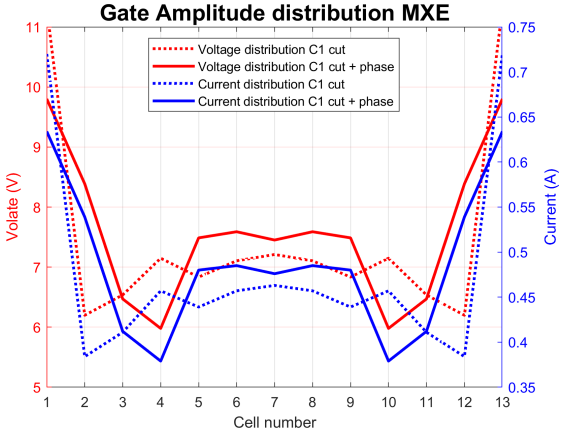
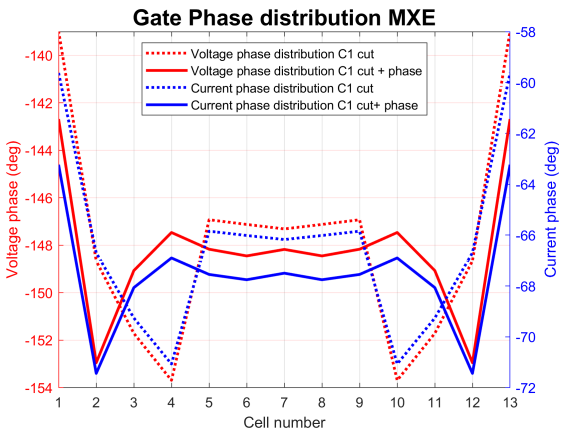


FIGURE 6.26: Nose plot of Ld1 and Lg1 height optimisation for phase current in combination with C1 cuts as seen in Figure 6.10.

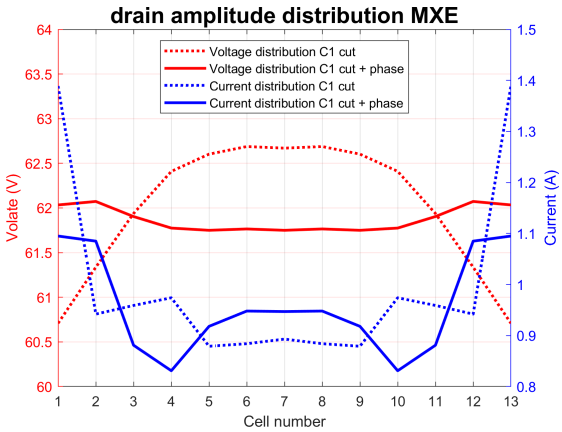
Figure 6.27 presents the distributions of the MXE, where notable differences are observed



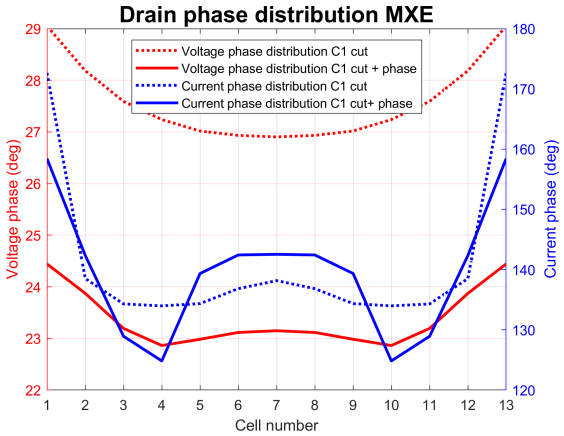
(A) Voltage and current amplitude at the gate.



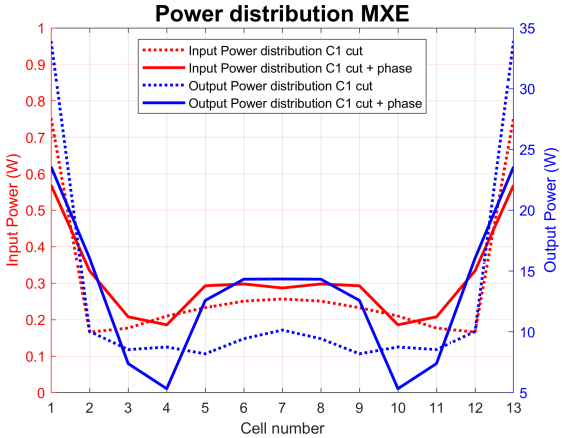
(B) Voltage and current phase at the gate.



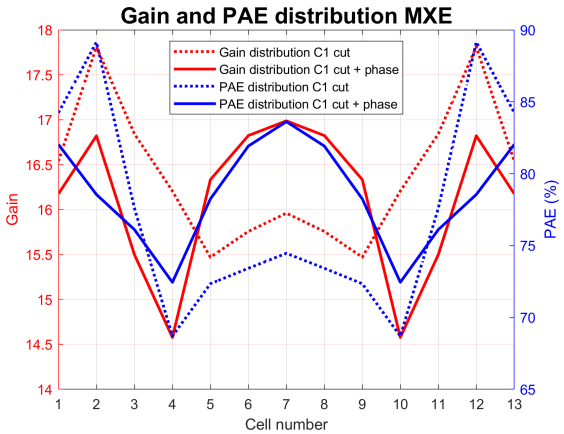
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



(E) In and output power.



(F) Gain and PAE over the powerbar.

FIGURE 6.27: Distributed characteristics and performance at maximum efficiency point.

compared to the case where only C1 is segmented in multiple sections (dotted lines). The shape of the gate distributions of the voltage and current is relatively similar to the shapes presented in Figures 6.12a and 6.12b. The similarity in the gate voltage and current distributions indicates that the changes to the voltage and current are primarily driven by

the modifications made to the Lg1 bond wire array.

Figure 6.27c reveals that the current of the outer edge cells has been reduced by approximately $300mA$, resulting in a more uniformly distributed current. As a result, the power output distribution changed as seen in Figure 6.27e. Notably, cells 5-9 contribute more significantly to the overall power output, while cells 1 and 13 (the outer edge cells) contribute substantially less. A second reason for an improved output power distribution is the reduction in phase differences between the outer edge cells and the cells in the middle of the power bar. Consequently, the PAE distribution has improved as shown in Figure 6.27f.

Considering the MXP, similar trends are observed to those discussed previously. The only significant difference is again in the current amplitude of the drain, where the outer edge cells still contribute significantly more current, as is evident from Figure 14c in Appendix B. However, due to the reduced phase differences and enhanced power output of the cells in the middle (cells 5-9), the total output power of the device also increases.

The expanded nose plot indicates that the device can operate at higher power levels while maintaining or improving efficiency. This suggests that there is no trade-off in combining Lg1 and Ld1 optimised bond wire heights for the current phase, as both modifications lead to enhanced performance without compromising the benefits of either.

6.4 Gate capacitor cuts combined with inductance-based height optimisation

In previous sections, the gate and drain impedances were used as a diagnostic tool to assess the distribution across the power bar rapidly. This approach is justified since the complex impedance is a function of both the magnitude and phase of the complex current and the voltage. Consequently, if all impedances converge and exhibit the same trajectory as a function of available input power, it suggests that the operating voltage and currents are likely to be uniformly distributed across the array. To achieve this, the height of the bond wires is tailored to ensure a uniform inductance distribution over the gate and drain of the power bar.

The proximity effect causes current accumulation at the edges of the bond wire array, resulting in lower inductance values for the outer edge bond wires compared to those in the middle of the array. Increasing the length of the bond wire also increases its inductance. To achieve a uniform distribution of inductance across the entire array, it is proposed that the outer edge bond wires be made longer than those in the middle of the array.
An additional consequence of achieving a uniform wire inductance distribution is that the current distribution becomes uniform. This is because the bond wire model used in ADS assumes a uniform current distribution when calculating the wire inductance. As a result, any differences in inductance are also reflected in the current distribution, indicating that equalising the wire inductance will inherently lead to an equal current distribution.

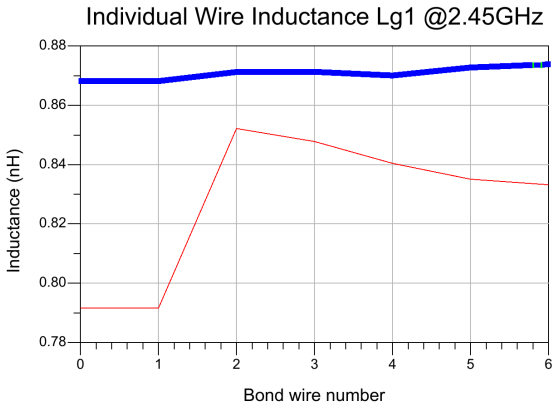
These optimisations are implemented in combination with the segmentation of the C1 rail to mitigate the convergence issues discussed in previous sections and minimise the computational time required by the simulations.

6.4.1 Gate inductance and capacitor rail cuts

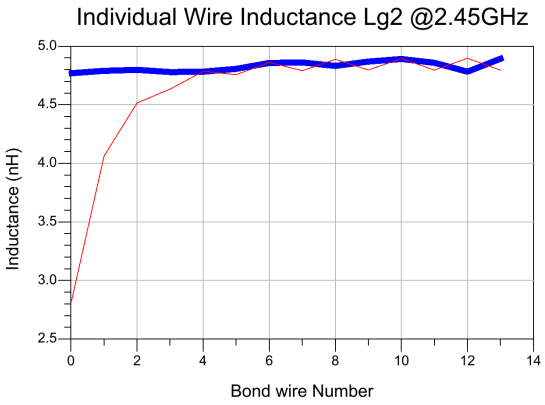
The device contains a DLP filter at the gate interface, consisting of Lg3, Lg2 and Lg1. Each array contains multiple bond wires with each different inductance as seen in Figure

6.28 in red. In contrast to section 6.1.1, where only the height of Lg3 was altered to make the phase uniform, all bond wires within each gate array will be adjusted to ensure equal inductance across each gate array.

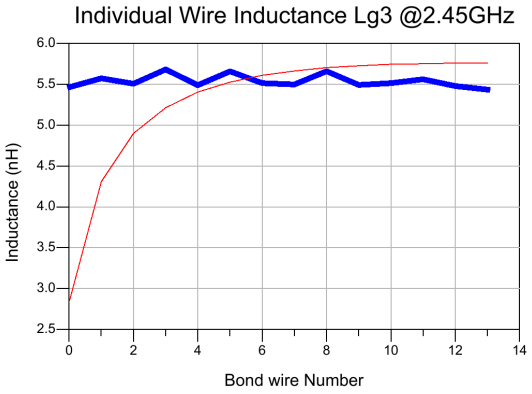
To achieve uniform inductance across the gate array, AC-simulations were employed as a rapid tuning method. The results are presented in Figure 6.28, which shows a comparison of the original inductance values (in red) and those obtained after equalising the inductance of each bond wire (in blue).



(A) Lg1 non-optimized (red) and Lg1 height optimised (blue) for equal inductance.



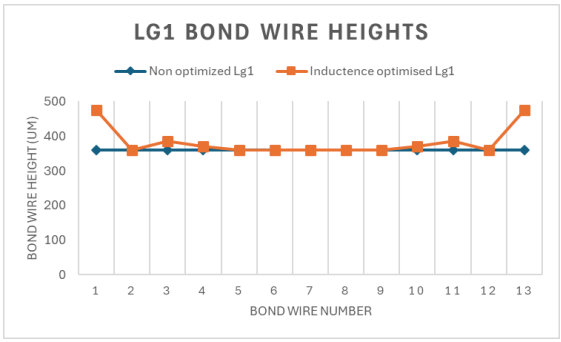
(B) Lg2 non-optimized (red) and Lg2 height optimised (blue) for equal inductance.



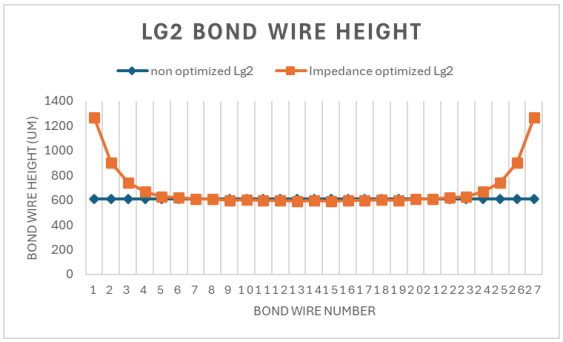
(C) Lg3 non-optimized (red) and Lg3 height optimised (blue) for equal inductance.

FIGURE 6.28: Non-optimised (red) and optimised (blue) bond wire height distribution for equal wire inductance of all three arrays at the gate.

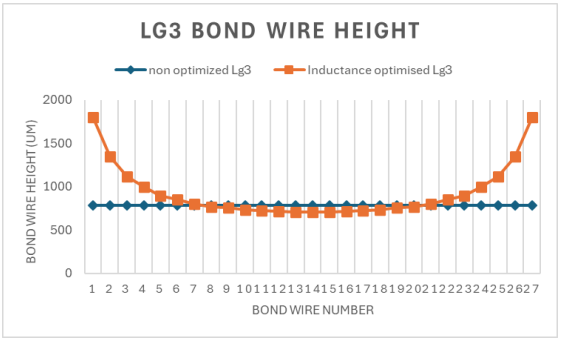
Figure 6.28 reveals that the outermost bond wire (wire 0) has undergone the most significant change in terms of inductance, as expected. This is further evident in Figure 6.29, which compares the original and new height distributions. Notably, the height of the outermost bond wires in Lg3 has been almost doubled, indicating a substantial inherent difference in inductance. A 3D view of the gate arrays is shown in Figure 6.35, demonstrating the difference in bond wire height within each array. However, it is worth noting that this design exceeds the upper height limit (approximately $1200\mu m$), making it unproducible. Despite this limitation, further analysis was performed using HB-simulation in combination with load sweeping to investigate the implications of equalising the wire inductance.



(A) Lg1 height distribution.



(B) Lg2 height distribution.



(C) Lg3 height distribution.

FIGURE 6.29: Height differences of non-optimised and optimised for equal inductance at the gate.

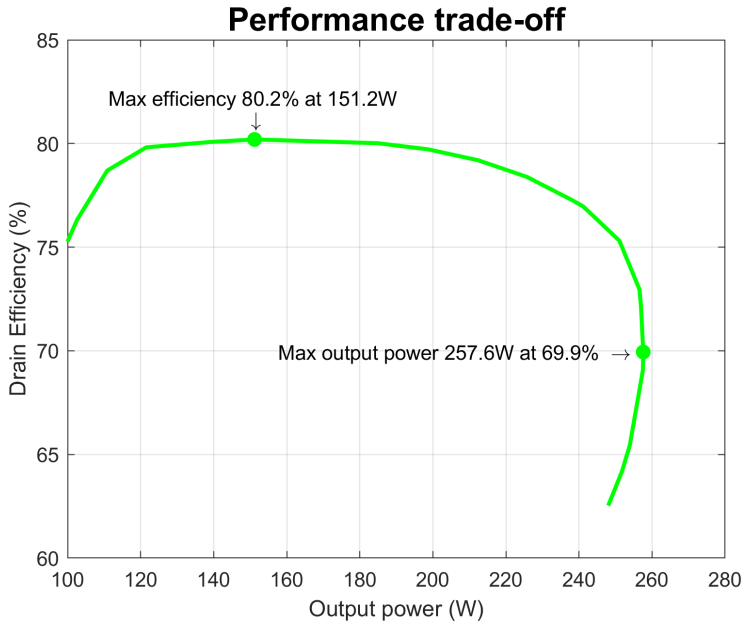
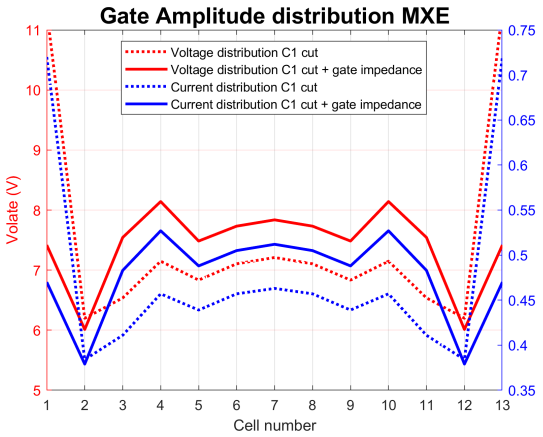


FIGURE 6.30: Nose plot of equal gate inductance in combination with C1 cuts.

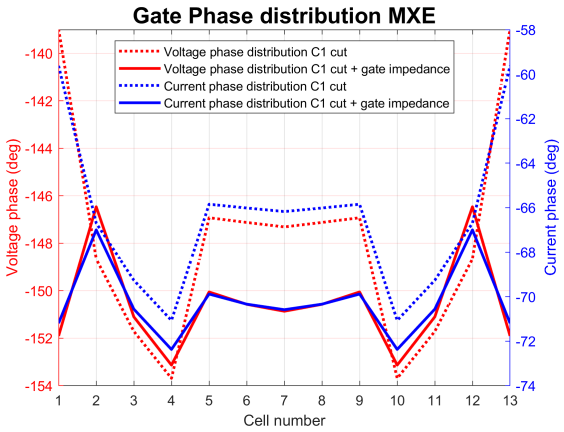
The performance trade-off curve is shown in Figure 6.30. Notably, the MXE has increased to 80.2% at an output power level of $151W$, while the MXP has also been improved to $258W$ of output power.
The performance enhancements achieved by the modifications implemented in this section

are relatively small compared to those demonstrated in section 6.3.3. However, upon examining the operational characteristics, several differences can be observed. Figure 6.31a shows that the current and voltage of cells 1 and 13 have been reduced while the voltage and current in cells 3-11 have increased. As a result, the drain current has been reduced as seen in Figure 6.31c. Furthermore, the current phase distribution has also increased in uniformity as seen in 6.31d. These modifications have yielded a notable increase in power output and operating efficiency for cells 3 through 11.

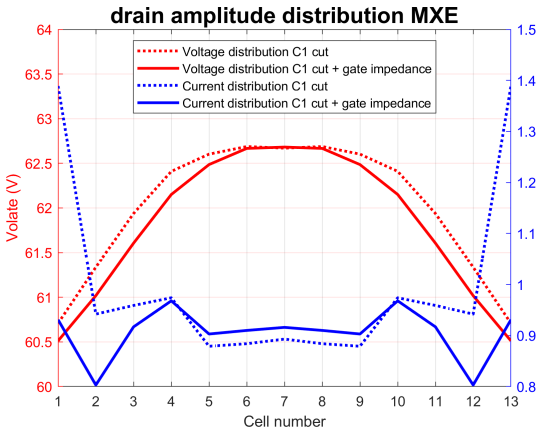
For the MXP, similar improvements are observed. In contrast to the findings discussed in section 6.3.2, the current amplitude and phase in the outer edge cells 1 and 13 have been reduced. Notably, the phase of the voltage has shown a slight increase, whereas the resulting power output has become more uniform across the device. These effects contribute to a more coherent construction of the output signal, resulting in higher peak power output.



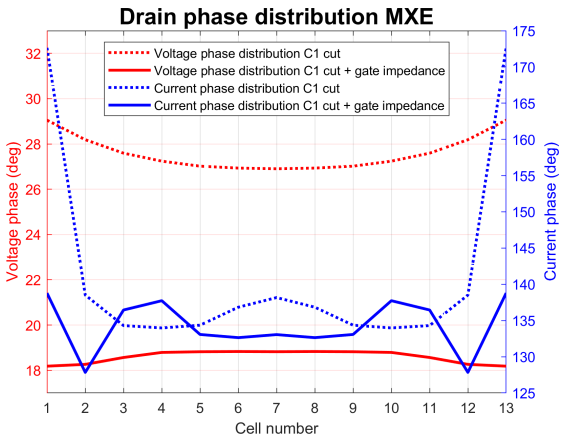
(A) Voltage and current amplitude at the gate.



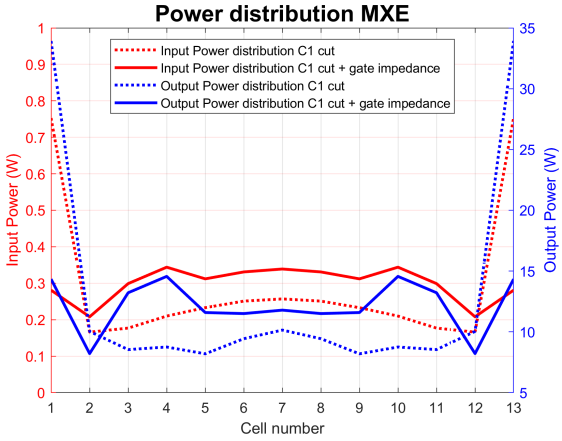
(B) Voltage and current phase at the gate.



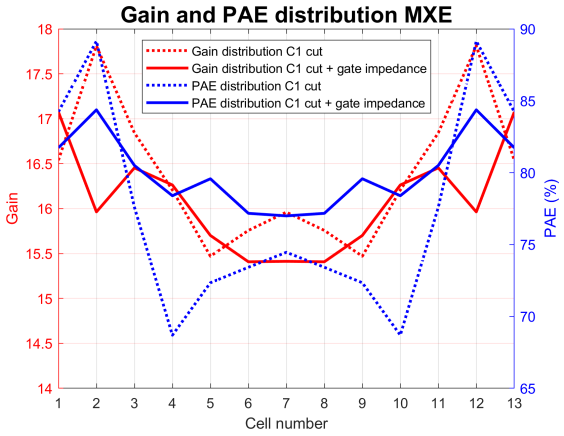
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



(E) In and output power.



(F) Gain and PAE over the powerbar.

FIGURE 6.31: Distributed characteristics and performance at maximum efficiency point.

6.4.2 Drain inductance and capacitor rail cuts

To achieve uniform inductance across the drain array (Ld1), AC-simulations were employed as a rapid tuning method. The result is presented in Figure 6.32, where the red line shows the inductance for each wire in a uniform height distributed array, and blue the inductance optimised array.

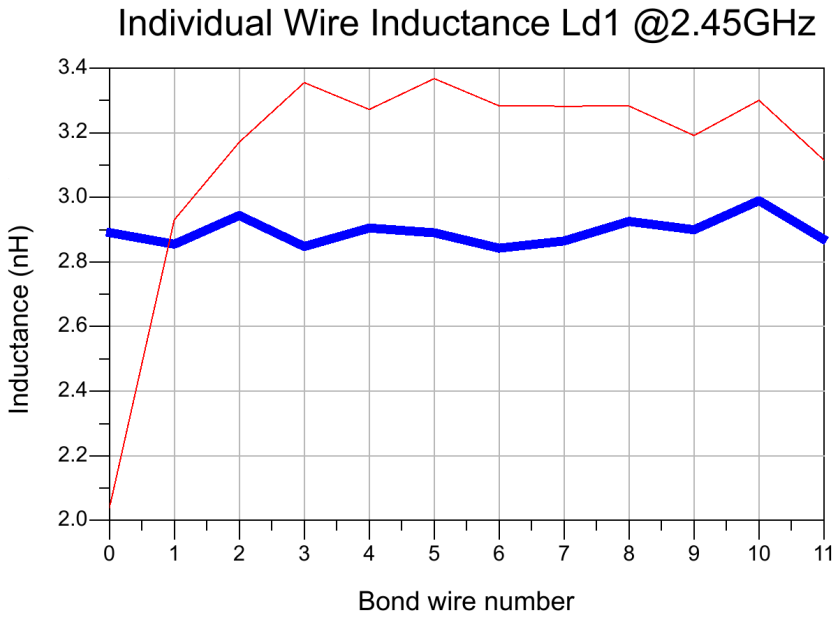


FIGURE 6.32: Non-optimised (red) and optimised (blue) bond wire height distribution for equal wire inductance of Ld1.

As shown in Figure 6.33, the height of the outermost bond wire has been increased by nearly a factor of two. This significant increase in bond wire height, as stated earlier, exceeds the upper limit that can be accommodated within the package. Nonetheless, HB-simulations are performed in conjunction with load sweeping to investigate the impact of this configuration on device performance.

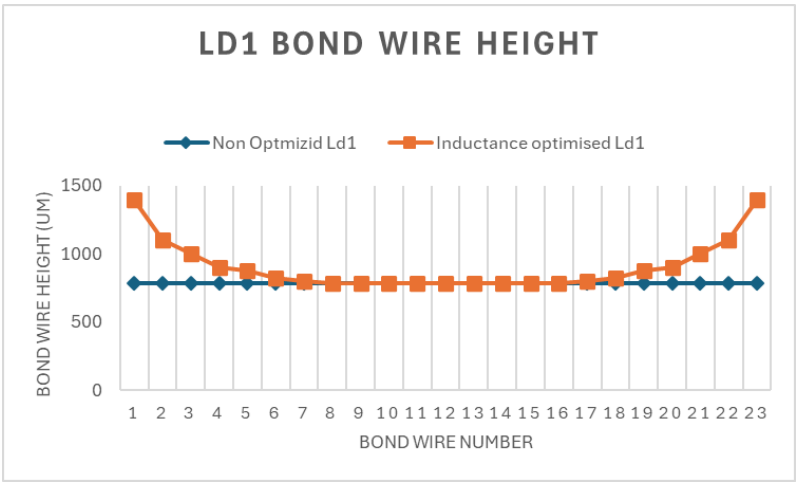


FIGURE 6.33: Height differences of non-optimised and optimised for equal inductance at the drain.

Figure 6.34 shows the performance curve of the simulation result of the device. Again, it becomes evident that the peak output power hasn't increased while the max efficiency point has increased by a small amount. This result is consistent with the outcomes obtained from previous simulations, where adjusting the drain bond wire height was found to achieve a more uniform current phase distribution, ultimately contributing to a more coherent signal construction.

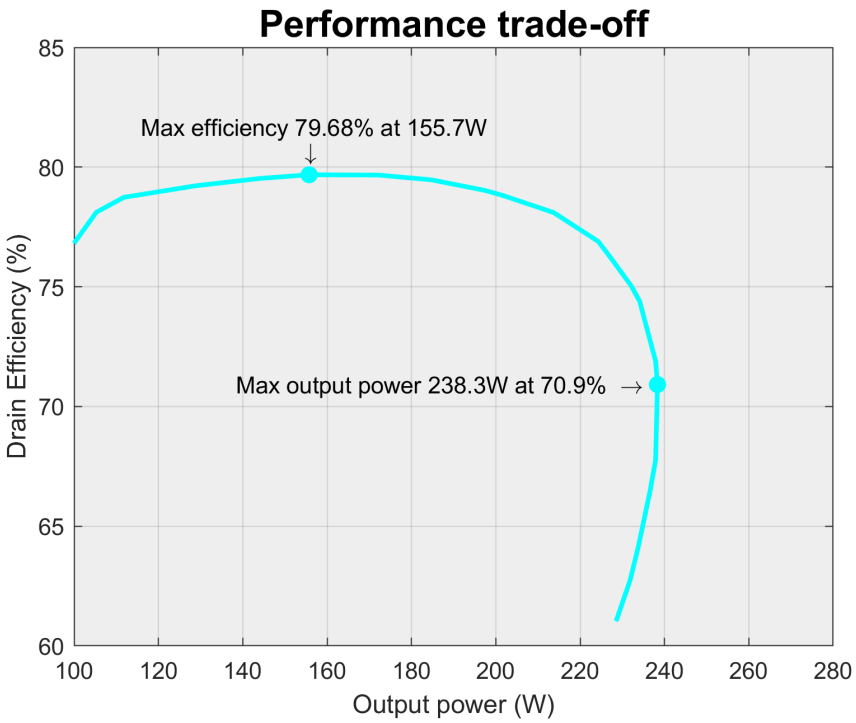


FIGURE 6.34: Nose plot of equal drain inductance in combination with C1 cuts.

Upon closer examination of the operating characteristics, it is revealed that there are no significant changes in the current and voltage at the gate of the device. However, a notable improvement is observed in the uniformity of the voltage amplitude at the drain compared to the case where only the C1 rail was cut. Furthermore, the magnitude of the current at cells 1 and 13 has decreased. As a result, the cells in the middle, cells 4-10, operate at higher efficiencies. Therefore, only the MXE has improved.

6.4.3 Inductance optimisation in combination with C1 cuts

The height distributions developed in the previous sections are integrated into one design concept. Figure 6.35 provides a 3D view of this combined design, featuring all arrays with their inductance optimised height distributions. As explained earlier, it is evident that this design will exceed the package's dimensions, resulting in a design that can not be produced. However, HB-simulations in combination with load sweeping are performed to study the effects.
Figure 6.36 presents the performance curve of the device where all the inductances in the array have been equalised. Notably, the curve contains the highest achieved MXE until now, and the MXP has also improved.

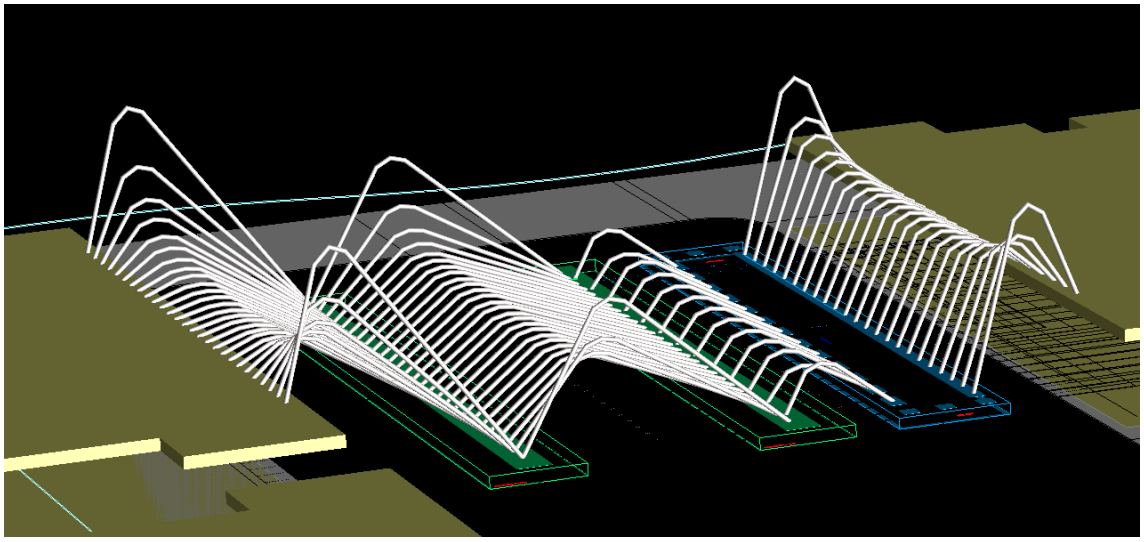


FIGURE 6.35: 3D view of the bond wire height distribution. The left-hand side is the gate. On the right is the drain of the package.

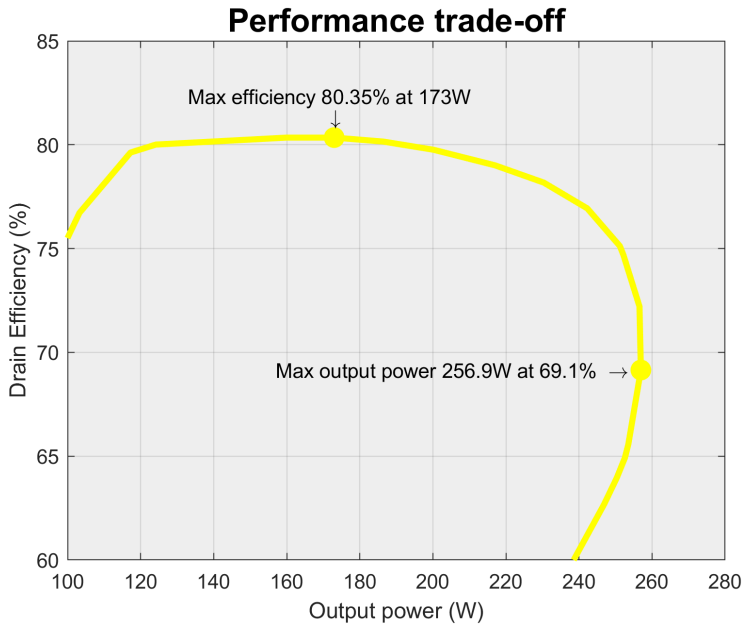


FIGURE 6.36: Nose plot of equal bond wire inductance in combination with C1 cuts.

Upon comparing the operating characteristics, it is evident that the gate optimisation has had a more pronounced impact on the device performance. The drain bond wire optimisation, while affecting the drain voltage, primarily contributes to improving the coherent construction of signals at the drain. A combination of both results in a uniform PAE and gain distribution over the power bar. While this combined approach yields the best results, the difference in outcome compared to gate optimisation alone is relatively small.

6.5 Simulation matrix results

In previous sections, various bond wire height distributions have been simulated, and their results have been briefly discussed. A logical step is to compare the overall performance of each configuration before drawing conclusions from the matrix. To facilitate this comparison, Figure 6.37 presents a single plot that combines all the nose plots obtained from the different configurations.

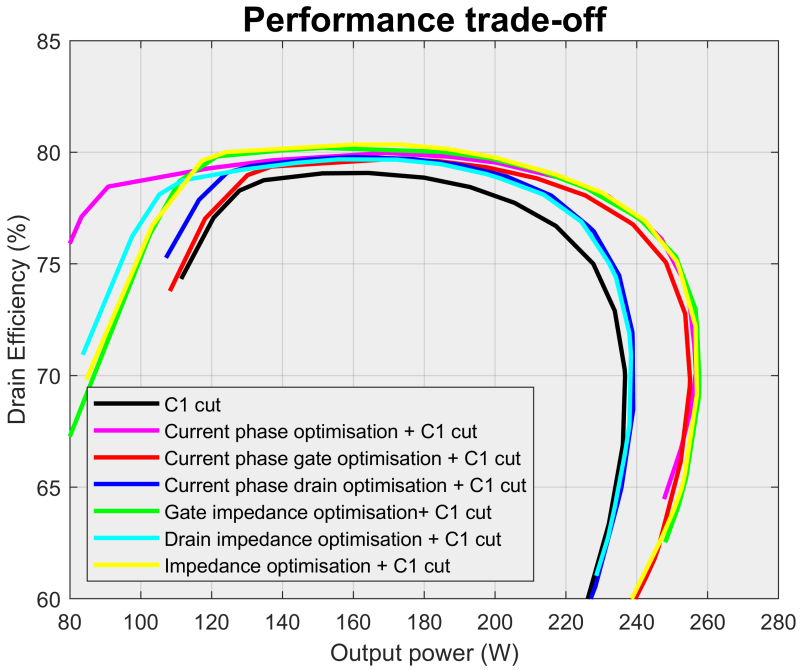


FIGURE 6.37: Performance nose plots of multiple bond wire height distributions.

Figure 6.37 reveals that the worst performing configuration is where the bond wire height distributions are equal and only C1 is segmented. This suggests that optimising the bond wire height distribution for different parameters can enhance device performance.
Notably, when the height of the drain bond wires is altered to achieve a more uniform distribution, only the MXE is improved. As discussed in the previous sections, could this be caused by the almost identical gate distributions. No enhancement in voltage at the gate will translate to the same power output, since the device acts as a voltage-controlled current source. Due to the increase in electrical length, the power will be constructed more coherently. Hence, the MXE increases while the MXP remains unchanged.
The performance curves of the gate optimised height distributions reveal improvements in both MXE and MXP. The more uniform distributions at the gate result in a slight increase in average output power per cell, which in turn leads to a higher peak power output. Additionally, the signal phase is slightly improved, enabling signals to be constructed more coherently and ultimately increasing overall efficiency.
When combining all bond wire height distributions, it is observed that there is almost no improvement in overall performance compared to the case where only the gate bond wire height distribution was optimised. The distribution characteristics at the gate remain unchanged, while the phase at the drain is slightly enhanced. The gate distribution characteristics remain unchanged, while the phase at the drain experiences a slight enhancement, leading to an insignificant increase in MXE. However, attributing this difference proves challenging, since the differences in performance curves are of such small magnitude that

they could be attributed to variations caused by the Z_L step size. Despite this uncertainty, this suggests that both solutions could be adopted without a trade-off.

to summarise the effects of the bond wire height distribution and the additional cuts in C1, the simulation matrix from Figure 4.1 is filled in.

	Gate	Drain	Combined
Phase	Non converging Although the harmonic balance simulation did not converge, it became clear that the impedance values over the drain and gate have come closer together. Therefore, some results converged, but not enough to reliably make a performance curve of this device.	Non converging The harmonic balance simulation did not converge. Furthermore, the impedance values over the individual cells did not come closer together compared to the reference. So, no improvements have been observed.	Non converging Led to a non-converging result. However, the drain efficiency vs output power can be drawn, indicating impedance oscillations. This is the root cause of the non-converging results, and further cell isolation is required.
Rail cutting	Max. Efficiency: 79.07% --> 164W Pout Max. Output Power: 236.7W --> 70% DE • Since there is no gate rail, the C1 metal has been cut. • Impedances have converged and follow the same trajectory as a function of available input power. • Outer cells produce the most power (may result in heat-related problems) • Gate voltage differences of approximately 1V between cells 2-12.	Non converging This simulation did not converge reliably for any load point. No reliable data could therefore be extracted from this simulation.	Max. Efficiency: 78.66% --> 163W Pout Max. Output Power: 235W --> 69.5% DE • Drain rail cuts improve the voltage distribution over the Drain • Lower PAE for the center cells • Small decrease in output performance.
C1 Rail cuts + Phase	Max. Efficiency: 79.69% --> 170W Pout Max. Output Power: 255W --> 69.9% DE • Increased uniform phase distribution at the gate for cells 3-11. • Less input and output power at cells 1 and 13. • Increase input and output power at cells 2 and 12 • Improved current phase distribution, especially at MXP, where cells 5-9 are less behind, and cells 1 and 13 are less in front. • Better PAE for cells 3-9	Max. Efficiency: 79.79% --> 160W Pout Max. Output Power: 239W --> 68.5% DE • Almost no changes in gate operating characteristics. • A better current phase distribution at the drain flange results in higher efficiency. • Voltage distribution at the drain has become more uniform. • 200mA less power is produced by cells 1 and 13.	Max. Efficiency: 79.97% --> 169W Pout Max. Output Power: 256.7W --> 70.1% DE • Gate characteristics are mainly influenced by Lg1 height distribution. • Cells 1 and 13 produce 300mA less of output current at MXE and are less in front in phase. • Increased PAE for cells 4-10. • Improvements observed earlier are now combined without a major trade-off.
C1 Rail cuts + Inductance	Max. Efficiency: 80.2% --> 151W Pout Max. Output Power: 258W --> 69.9% DE • Input power distribution where the difference is max 0.2W between the cells. • Lower input power for cells 1 and 13. • Uniform current distribution with max difference of 200mA between the cells. • Enhanced phase distribution at the drain with a max swing of 10 degrees. • Increased PAE for cells 4-10.	Max. Efficiency: 79.68% --> 156W Pout Max. Output Power: 238W --> 70.9% DE • Almost no change in gate operating characteristics. • Cells 1 and 13 produce 200mA less at MXE. • No significant differences at MXP, except the drain voltage distribution, which is more uniform.	Max. Efficiency: 80.35% --> 173W Pout Max. Output Power: 257W --> 69.1% DE • All improvements of the gate inductance optimisation are included. Only difference being in the drain voltage distribution, which have become more uniform in amplitude. • Uniform PAE and gain distribution.

Several key conclusions can be drawn from these findings. First, it is essential to note that the simulations only converged after the capacitor metal rail was split, as shown in Figure 6.10. Notably, the impedances converged as seen in 6.3a, indicating that the distributions within the device have become more uniform. Analysing the operating voltages, it is seen that the cells 2-12 operate at approximately the same voltages. This finding serves as

robust evidence to support the claim made in [7] that gate rail segmentation leads to an improvement in voltage distribution within the device. As a result of the improved impedance, the oscillations disappeared and the simulation converged.
Separating the drain rail into multiple sections did not make the simulation converge, nor did this prevent the impedance oscillations from occurring. Combining this approach with rail cutting techniques ultimately resulted in a slight decrease in performance compared to dividing only capacitor 1 into multiple sections. Closer examination of the operating characteristics reveals a notable drop of PAE at cells 6-8. This decline is likely due to a decrease in uniformity in drain voltage amplitude and phase, resulting in reduced power output from these cells and ultimately compromising overall performance.
Last, there is a noticeable difference between gate optimisation and drain optimisation. This disparity becomes particularly evident when the gate-optimised height distribution is combined with the drain-optimised height distribution. Gate optimisation has a significant influence on the gate characteristics, as the device operates as a voltage-controlled current source. As such, variations in gate characteristics have a significant impact on the drain characteristics as well. In contrast, drain optimisation primarily influences characteristics at the drain itself, with minimal to no effect on gate operating voltages and currents. Consequently, the drain can only control the coherent construction of signals at the drain lead. Meanwhile, the gate has a broader impact, not only improving signal construction at the drain lead but also enhancing power output distribution at the die.

Comparing the results to previous work, similarity could be observed. Notably, the results align closely with those presented in [7], where improving the voltage distribution over the gate enhanced overall device performance. The similarities with other works are less noticeable. The work of M. Ustunel at Ampleon also involved improving the voltage distribution over the gates to prevent oscillations at the output. I. Volokhine cut the second outermost bond wires to enhance distribution at the gate, thereby improving overall device performance. When examining the gate column in the simulation matrix, it is evident that improving the uniformity of the gate distributions will enhance the overall device performance.

While previous research has focused primarily on optimising device performance through modifications at the drain, our study takes a different approach by targeting gate optimisations. Upon analysing the simulation matrix, it becomes evident that our results do not align closely with those discussed in the related work section. Several factors may contribute to this discrepancy, including:

- The works mostly used non-optimised devices which were then optimised, while this study is conducted based on an optimised device that is available on the market;
- The simple output matching circuit, existing only out of a single bond wire array, only introduces small phase shifts;
- The bond wire array model assumes a uniform current distribution. Due to the high output currents, this assumption underestimates the distributed effects;
- Temperature is not taken into account, while this might be a significant factor for the drain.

Furthermore, it is worth noting that the effectiveness of bond wire height optimisation may also be influenced by the specific matching structure implemented at the gate or drain. More complex matching structures can contribute to increased non-uniformity, making bond wire height optimisation an efficient approach in these locations.

Chapter 7

Conclusion

Several enhancement techniques to address the distributed nature have been proposed and simulated. The consistent performance gains across different methods suggested that there might be a common underlying mechanism or variable driving the observed improvements. This work aims to uncover the underlying effect and reveal effective optimisation methods to address the distributed effects. To achieve this, research questions have been defined, and research has been conducted to answer them. The subsequent sections delve into the answers to the defined research questions, providing a thorough analysis and critical evaluation of the findings.

7.1 Research questions

Are existing models accurate enough to model the distributed effects?
A variety of models are available to model the bond wires. In this work, the bond wire model from [14] was chosen due to its ability to account for an array model with 90 bond wires, as well as their interactions with one another. This model incorporates certain assumptions, such as the current being uniformly distributed over the array. This simplification can compromise the accuracy of the simulation results.
Examination of the simulation results reveals some discrepancies between the gate and drain optimisation techniques. While the simulations for the gate exhibit improved performance in line with previous studies, the results for the drain distribution effects show less significant effects. The effects are still in line with expectations, and therefore, the models used are accurate enough to model the distributed effects, although they leave some room for improvement.

Is optimising a specific parameter more effective at the drain or the gate side?
Given that amplifiers act as voltage-controlled current sources, there is a noticeable difference between the gate and drain optimisation strategies. Optimising voltage distribution over the gate results in higher average cell power output, due to improved voltage uniformity across the gate. Furthermore, this leads to a more coherent signal construction at the drain lead, where the phase of the output signal is better aligned. Therefore, the gate height distribution can be adjusted to enhance the voltage distribution, thereby achieving improved efficiency and peak power output. In contrast, optimising the drain side does not yield corresponding improvements in gate distributions. However, enhancing current distribution does contribute to a more coherent signal construction at the drain lead, thereby increasing efficiency.

Which distribution effects are encountered more effectively by the bond wire height?
This work strongly suggests that improving the bond wire height at the gate to achieve a more uniform voltage distribution is effective in increasing the uniformity of the current distribution at the drain. As evident from the height optimisation of the current phase, the difference in bond wire height between the distributions of Ld1 and Lg1 is substantial. The Ld1 height distribution does not fit within the package, whereas a slight alteration in Lg1 is sufficient to improve the device's performance significantly.

Is it possible to forecast the change in distributed effects?
Simple AC-simulations have effectively shown to forecast distributed voltages and currents at low power values. This approach is advantageous as a first optimisation method, requiring less computational power and time compared to HB-simulations. Engineers can quickly alter the bond wire height and observe its effects on distribution, making it easier to identify potential design improvements. It's worth noting that this model assumes uniform current distribution over the array and neglects temperature effects. The benefit is that this model does not depend on power and therefore allows AC-simulations. Therefore, estimating the change in distributed effects for low-power purposes is possible, as other effects, such as current distribution and temperature effects, are negligible.

With these findings in mind, it becomes apparent that bond wire height can be optimised at the gate using AC-simulations of the full-scale device model. Notably, while optimising gate voltage distribution is crucial, it is also essential to optimise for complex impedance, as it encompasses both phase and amplitude information regarding current and voltage. In contrast, optimisation techniques targeting the drain have not yielded practical results.

7.2 Introduction to the broader context

Several studies have been proposed and implemented to address distribution effects, utilising various theories. However, some of these solutions lack comprehensive scientific evidence supporting their effectiveness. Meanwhile, various optimisation approaches have consistently led to improvements in device performance. The consistent performance gains across different methods suggest that a common underlying mechanism or variable may be driving the observed improvements.
This study reveals new insights into the distributed effects on device performance and how multiple optimisation strategies led to the same conclusion. Transistors act as voltage-controlled current sources, hence, a better voltage distribution will yield higher power outputs and contribute to the coherent construction of signals at the drain lead. At the fundamental level lies Ohm's law, which describes how a more uniform current distribution at the gate will lead to a more uniform voltage distribution. Therefore, examining the gate impedance, current, voltage, amplitude, or phase results in a better voltage-controlled current source, thereby enhancing its performance.

With increasing power density in RF high-power amplifiers, distributed effects are likely to become increasingly prominent. Engineers must familiarise themselves with available possibilities to mitigate these effects and optimise device performance without significant trade-offs.

Chapter 8

Summery

Due to the internal coupling between bonding wires, the current across the wire array becomes non-uniform. The non-uniform distribution causes individual cells in the power bar to operate under different conditions. These effects are highly undesirable and hurt the performance of RF high-power amplifiers.
Various strategies to eliminate distribution effects have been proposed in the literature. However, some solutions are patented and lack comprehensive scientific evidence supporting their effectiveness. Meanwhile, various optimisation approaches have consistently led to improvements in device performance. The consistent performance gains across different methods suggest that a common underlying mechanism or variable may be driving the observed improvements. Additional simulations are required to determine the underlying mechanism to propose effective distribution enhancement strategies.

To reveal the underlying mechanism, an existing RF high-power amplifier from Ampleon is chosen, and multiple enhancement methods have been implemented to study the distributions over the die. Since the distribution effects are hard to measure, a simulation model was implemented in ADS to simulate the voltages and currents within the package.
Convergence problems caused by oscillation of gate impedances hindered simulations. Segmentation of the gate rail prevents convergence problems by enhancing the uniformity of the voltage distribution over the gate side of the power bar. Using this technique, bond wire heights were altered through AC-simulation to ensure the inductance of all wires in each array was equal and the current phase was uniform. Load-pull simulations were performed on different configurations of bond wire heights.

Results show that altering the bond wire height at the drain results in enhanced efficiency at the Maximum Efficiency point (MXE). When the height at the gate is optimised, the MXE and Maximum Power point (MXP) are enhanced. A deeper dive into the distributions has shown that a more equal voltage distribution over the gate will yield higher current outputs, enhancing the peak power output. While the drain current phase is impacting the overall Drain Efficiency (DE) of the device. Therefore, applying solutions to the drain will only affect the device's efficiency. In contrast, applying the solution at the gate can enhance the peak power output of the device while improving the drain current phase, resulting in higher DE.

RF high-power amplifiers act as voltage-controlled current sources. Differences in the voltage distribution at the gate hurt the overall device performance. Cutting the capacitor rail and altering the height of the bond wires have proven to enhance the voltage distribution

at the gate. Even if the Lg array's height is altered for equal current phase distribution, the voltage distribution at the gate improves (Ohm's law). At the drain, the phase of the current should be aligned to construct the signal coherently for maximum efficiency. AC-Simulations of bond wire arrays have been proven as an effective method for tuning the height to improve the distributions accordingly.

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A: Load pull simulation

Load pulling is a technique used to determine the large-signal transistor characteristics as a function of the matching impedances. Therefore, it is a crucial part of the design process for high-power amplifiers. Whether simulated or in a measurement setup, a variable load is presented to the device under test. From these simulations, key characteristics can be determined, such as output power, efficiency, gain and the optimal operating impedances. The source can also be swept over different impedances; however, this is less effective, as it mainly influences the power gain of the device.

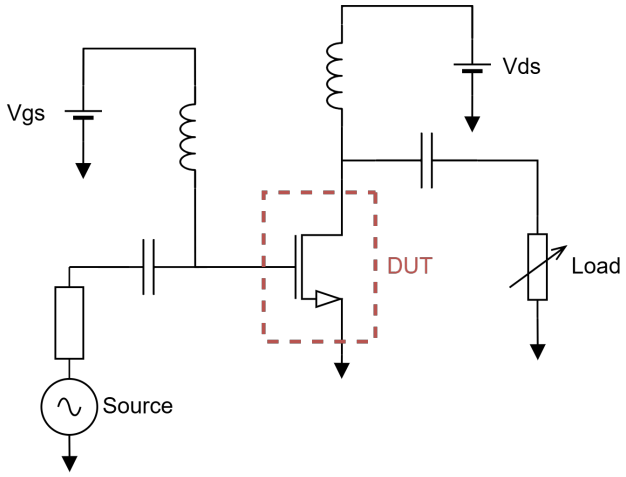


FIGURE 1: Simple load-pull simulation block diagram.

Using the setup in Figure 1, the operation currents and voltages can be detrimental under controlled load impedances. These voltages and currents can then be used to calculate the large-signal device characteristics, such as gain, Power Added Efficiency (PAE), maximum power output, Drain Efficiency (DE), and power back-off. These can be calculated for all measured or simulated load points. These results can then be visualised by contour lines on the Smith chart over the measured load impedance areas.
From the contour lines, it is not immediately clear whether the device operates in compression. Adding a power sweep will enable the possibility to plot the gain response. Since the transistor is a non-ideal device, from a certain point, the gain will no longer be linear. This is also observed in Figure 2, where the output power saturates.
In Figure 2, it becomes clear that for smaller input powers, the transistor behaves linearly. When the power output is increased significantly, the transistor deviates from the ideal linear line, and it eventually enters saturation, where adding more input power results in the same output power. The relation between the input and output power is also referred to as the gain of the device.

$$G = \frac{Pout}{Pin} \tag{1}$$

In Figure 3, the gain is given as a response to the output power. Engineers often choose a point where the decrease in linearity in the gain response is still acceptable for their application. This report assumes that the power amplifier is designed for Continous Wave (CW) applications, such as cooking, industrial, or medical applications that do not require less linearity. Therefore, a higher compression point of 3 dB is often chosen, as these points frequently correspond to higher operating efficiency.

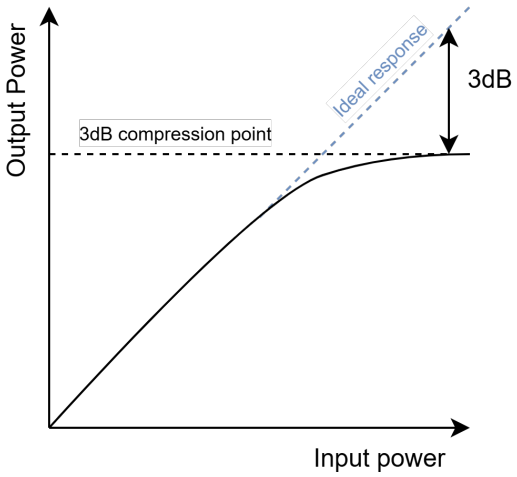


FIGURE 2: Available input power vs output power.

The drain efficiency is calculated by dividing the output power by the DC power:

$$DE = \frac{P_{out}}{P_{dc}} \tag{2}$$

where $P_{dc} = V_{dc} \cdot I_{dc}$. The input power is also dissipated in the device and, therefore, also contributes to the overall device performance. Therefore, to calculate the overall efficiency of the device, the following formula is used:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{3}$$

Equation 3 is the Power Added Efficiency (PAE) and calculate the overall efficiency of the device. The PAE must also be a function of the available input power. This means that, just as the DE, the available input power is determined by the 3dB compression point.

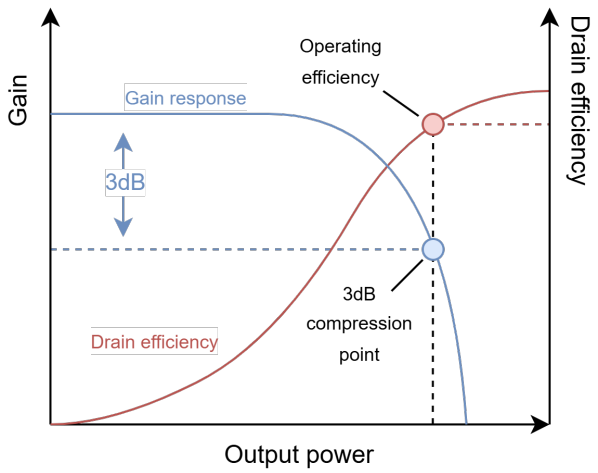


FIGURE 3: 3dB compression point on the gain curve related trough the output power to the efficiency point.

Each load point has its own DE, PAE, and gain curves, as well as corresponding compression points. From these values, the contour lines could be calculated and plotted in a Smith chart. This provides the engineer with a clear visual representation of where the optimal load should be for Maximum Efficiency point (MXE) and Maximum Power point (MXP). To show the trade-off, a so-called nose plot can be made and is shown in Figure 4. Here, the outer edge of all operating points for all loads is given, containing the maximum efficiency and power output. The engineer can then, based on these plots, choose the load that fits their application.

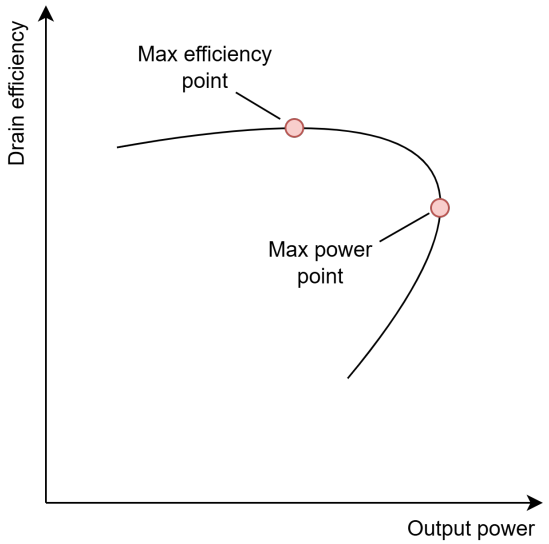
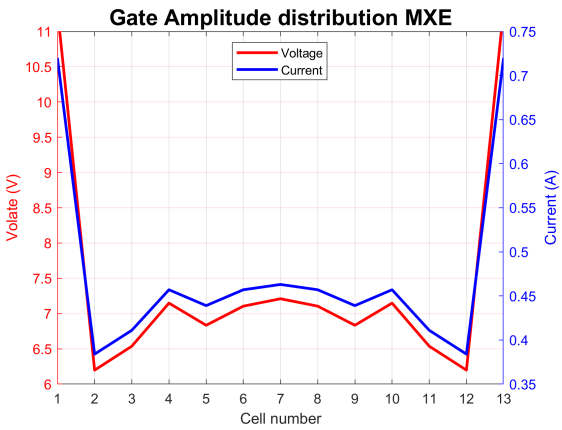


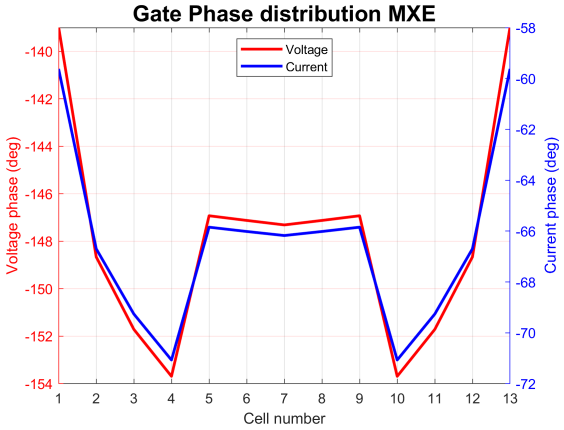
FIGURE 4: Trade off between maximum power output and efficiency.

B: Operating characteristics from simulations

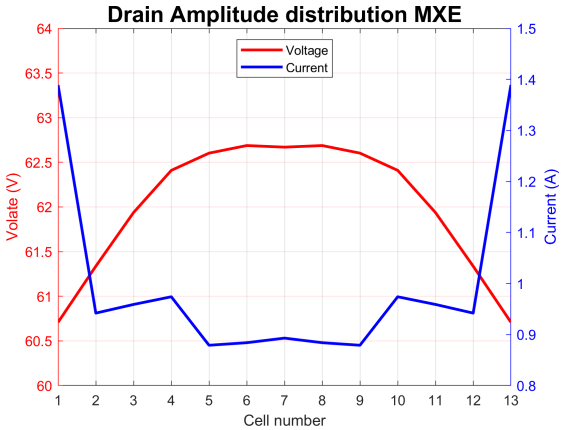
B1: C1 rail cut



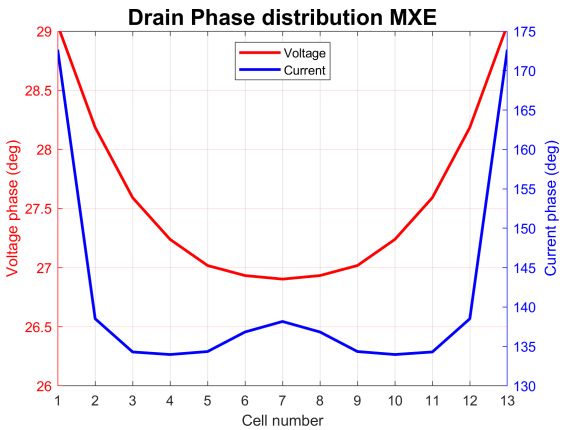
(A) Voltage and current amplitude at the gate.



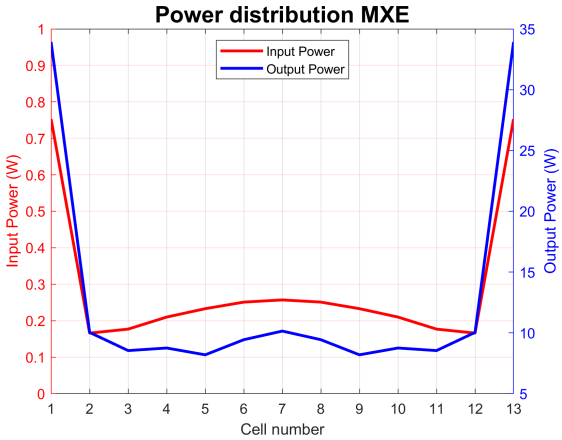
(B) Voltage and current phase at the gate.



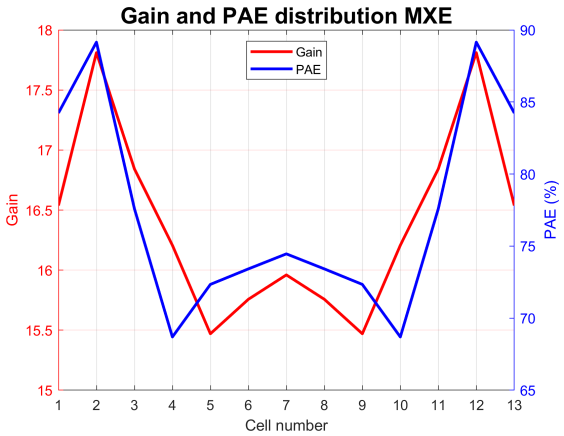
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

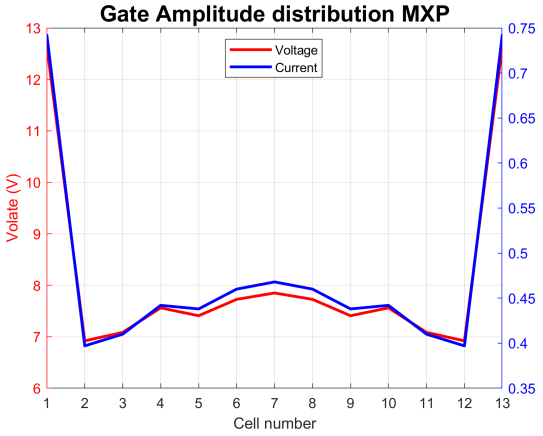


(E) In and output power.

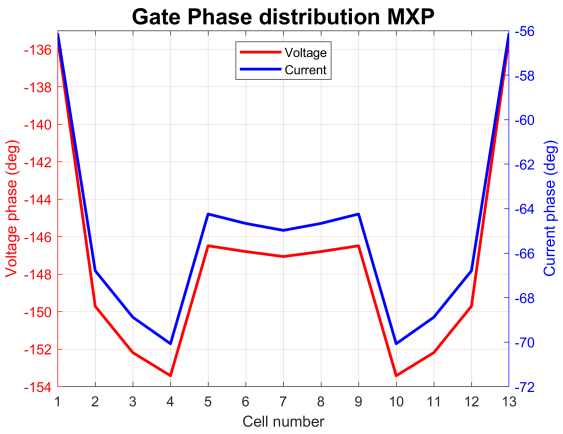


(F) Gain and PAE over the powerbar.

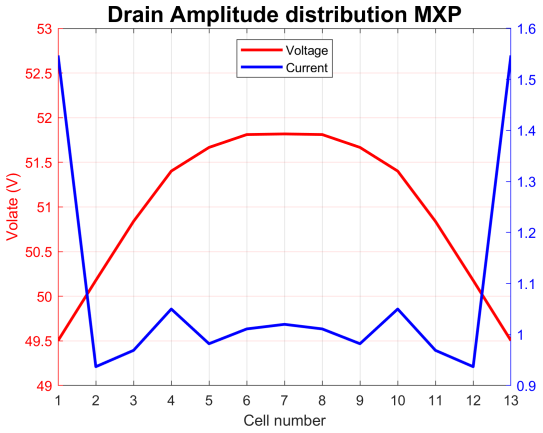
FIGURE 5: Distributed characteristics and performance at maximum efficiency point.



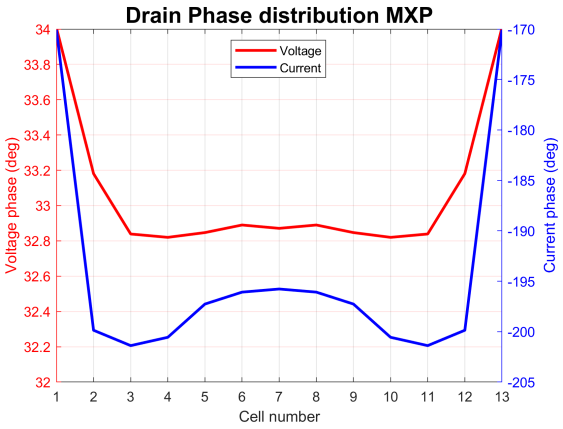
(A) Voltage and current amplitude at the gate.



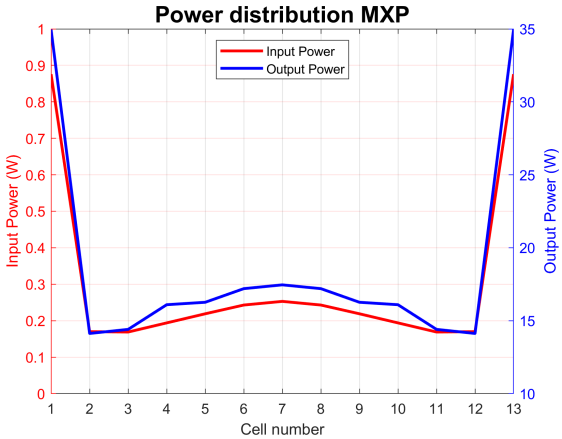
(B) Voltage and current phase at the gate.



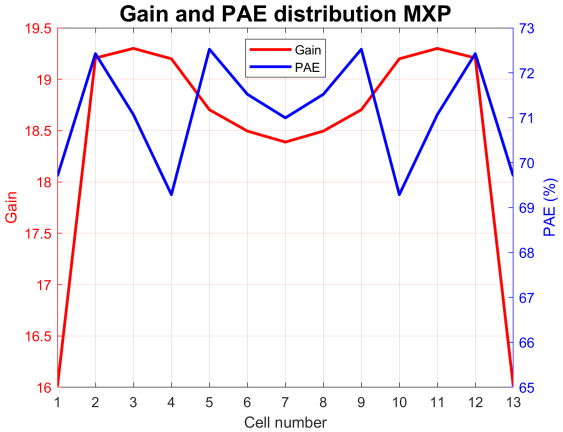
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



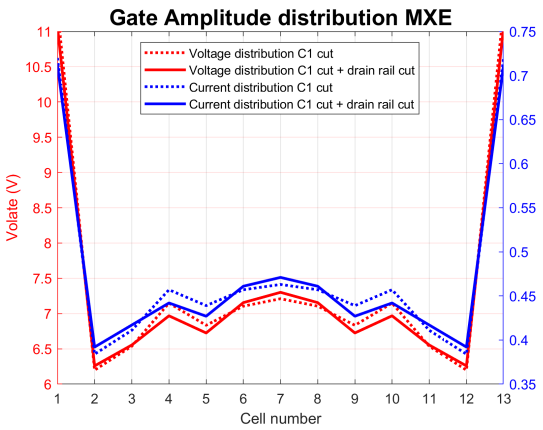
(E) In and output power.



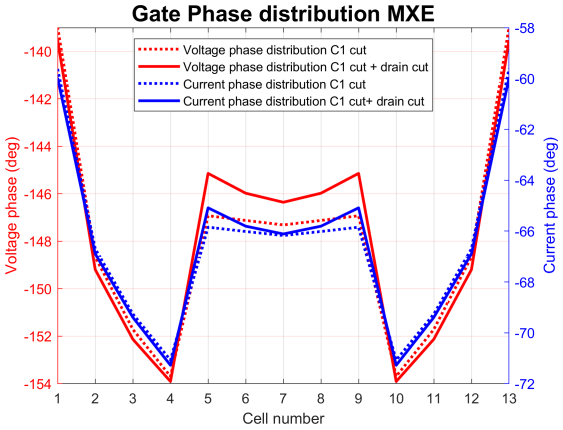
(F) Gain and PAE over the powerbar.

FIGURE 6: Distributed characteristics and performance at maximum efficiency point.

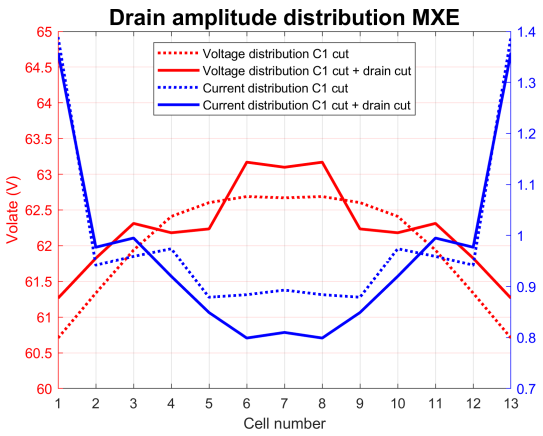
B2: C1 rail cut + Drain rail cut



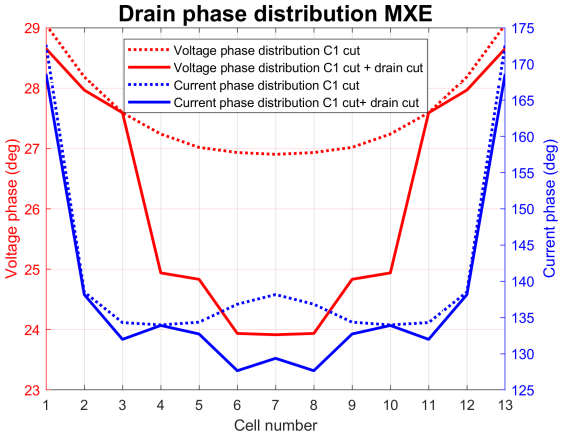
(A) Voltage and current amplitude at the gate.



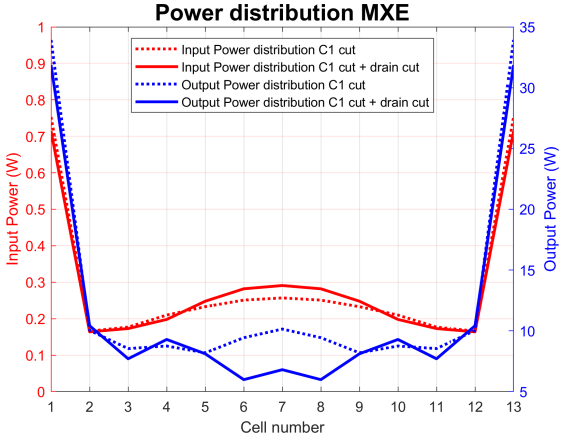
(B) Voltage and current phase at the gate.



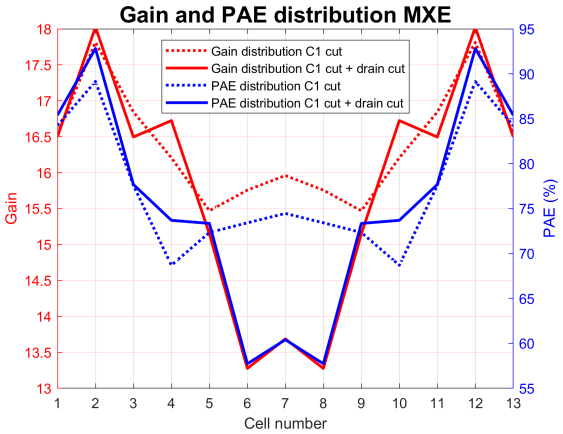
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

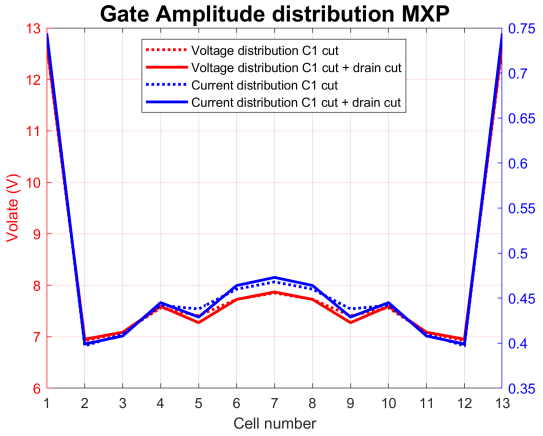


(E) In and output power.

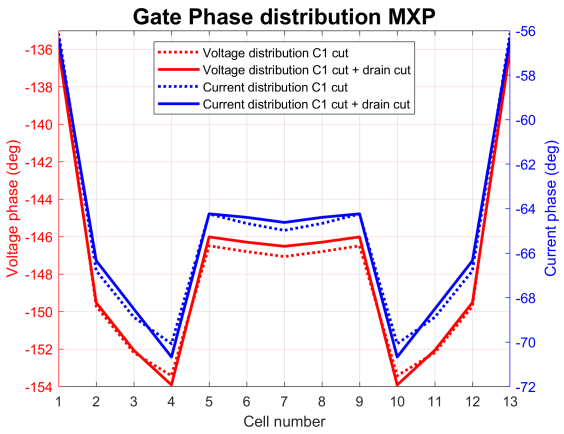


(F) Gain and PAE over the powerbar.

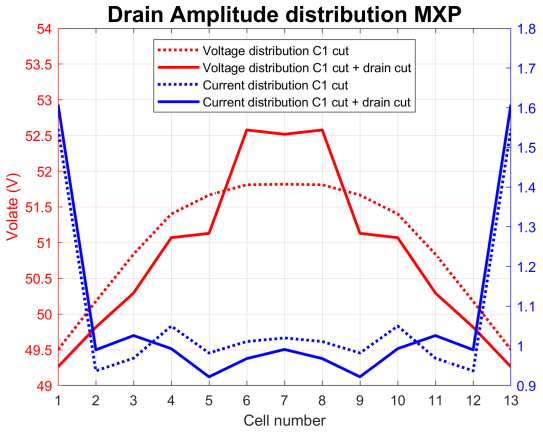
FIGURE 7: Distributed characteristics and performance at maximum efficiency point.



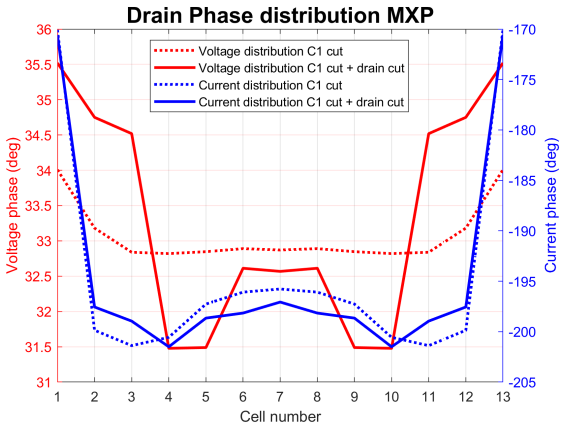
(A) Voltage and current amplitude at the gate.



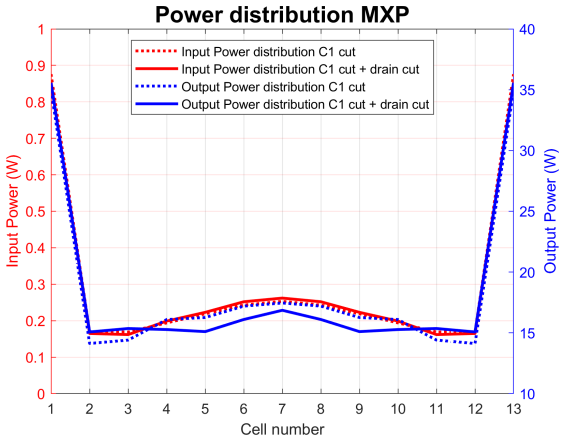
(B) Voltage and current phase at the gate.



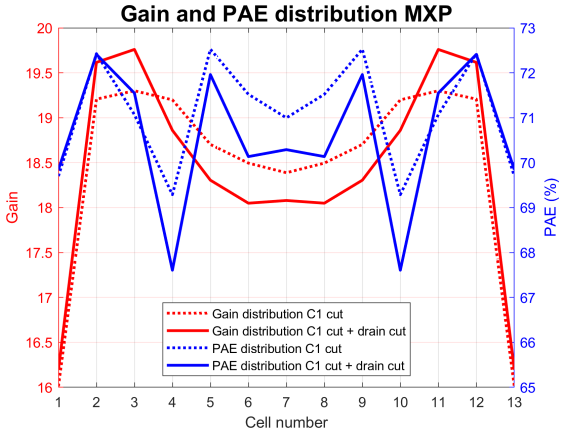
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



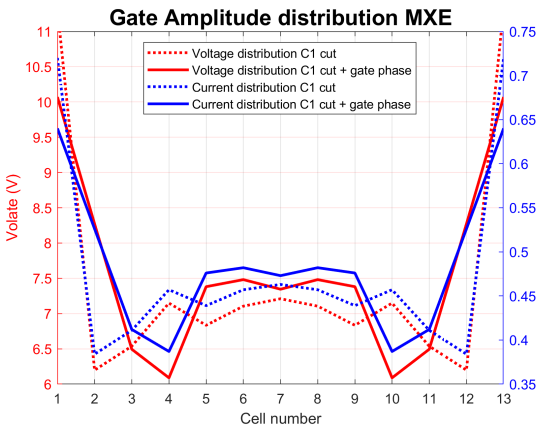
(E) In and output power.



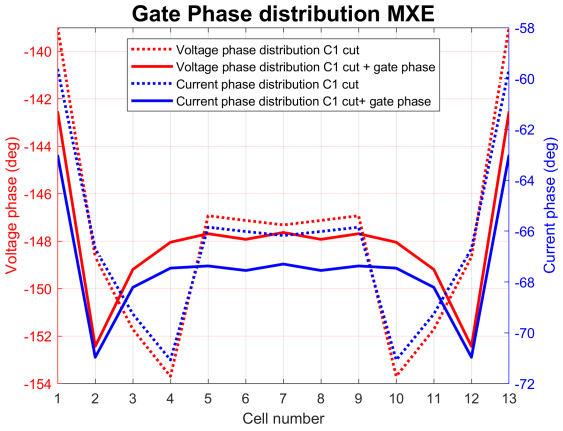
(F) Gain and PAE over the powerbar.

FIGURE 8: Distributed characteristics and performance at maximum efficiency point.

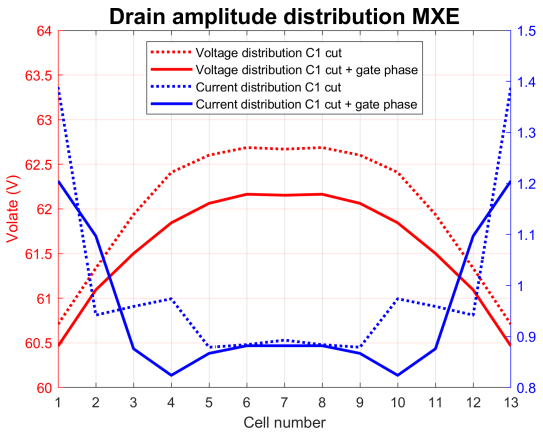
B3: Gate current phase optimisation + C1 rail cut



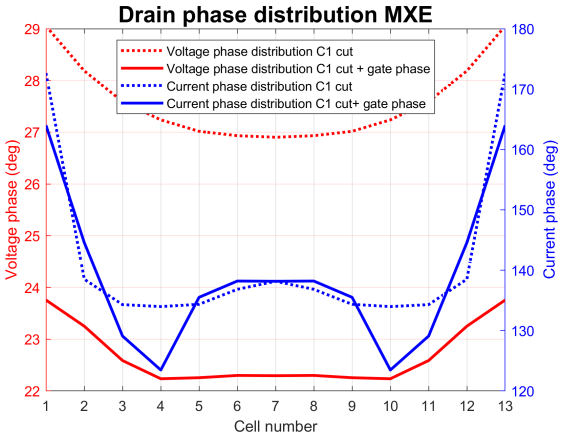
(A) Voltage and current amplitude at the gate.



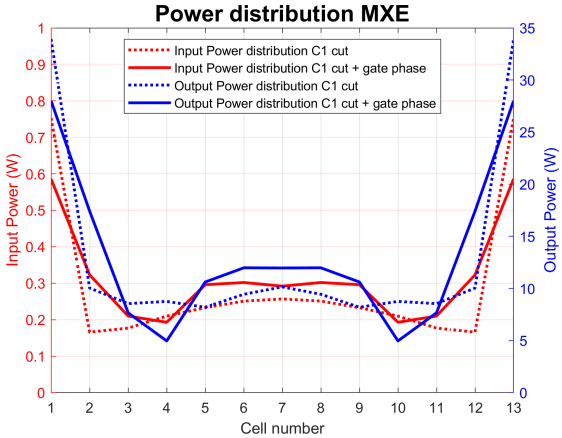
(B) Voltage and current phase at the gate.



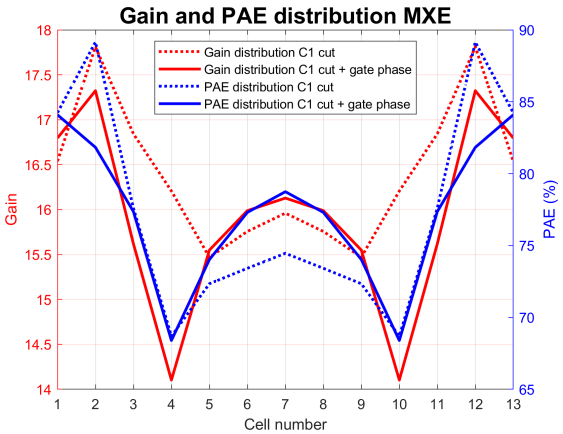
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

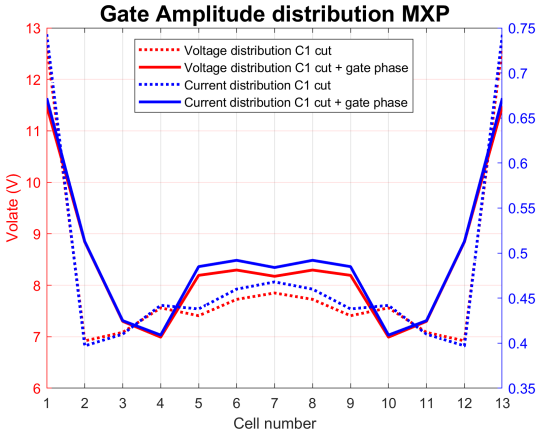


(E) In and output power.

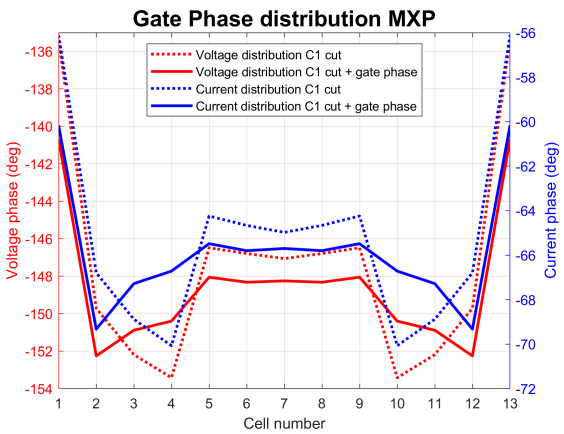


(F) Gain and PAE over the powerbar.

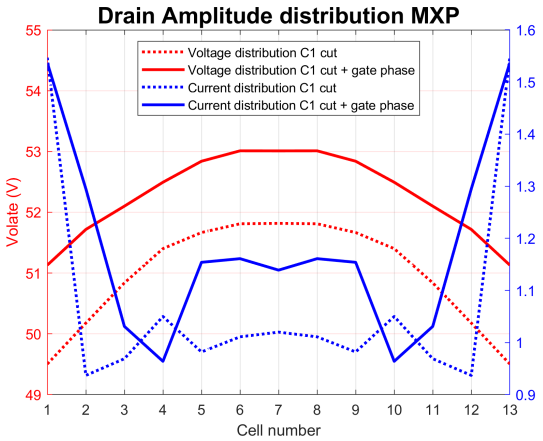
FIGURE 9: Distributed characteristics and performance at maximum efficiency point.



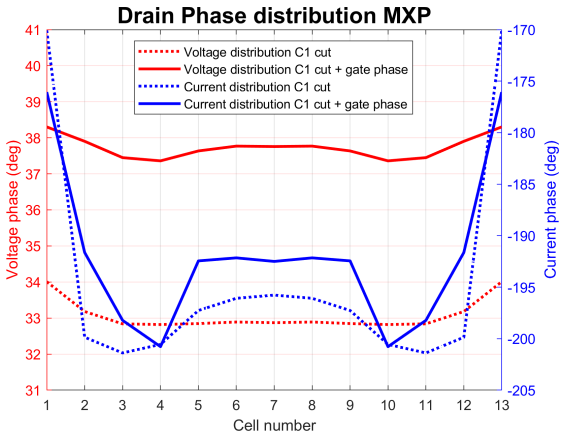
(A) Voltage and current amplitude at the gate.



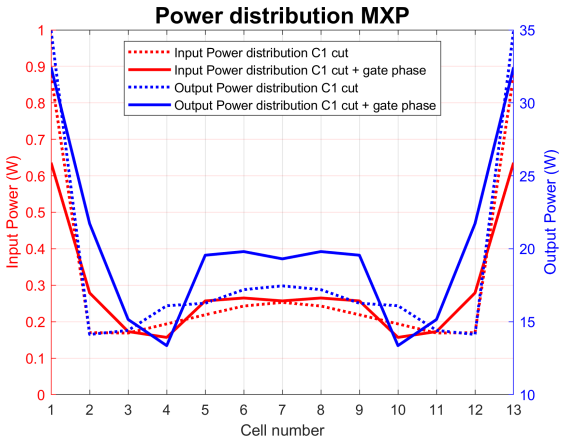
(B) Voltage and current phase at the gate.



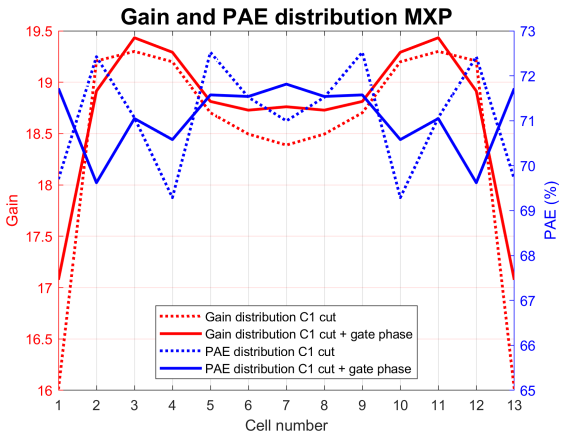
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



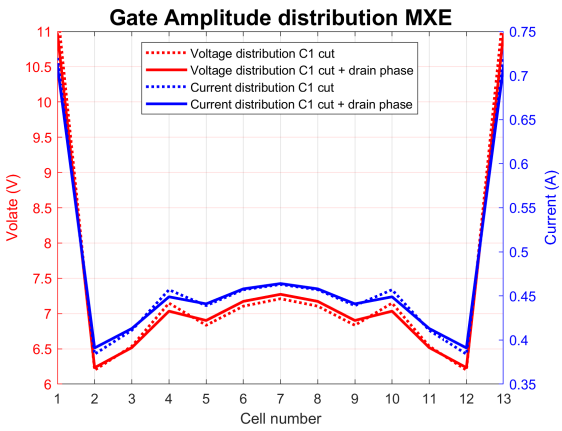
(E) In and output power.



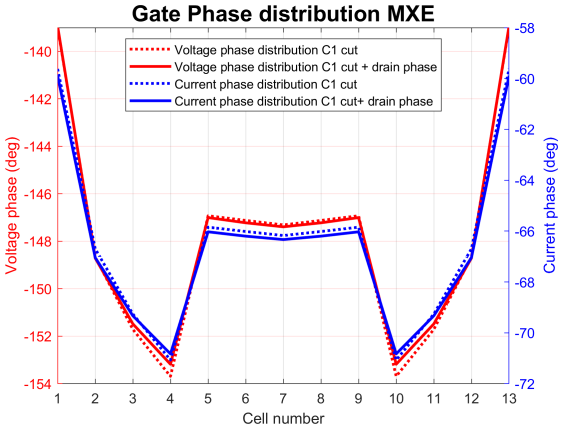
(F) Gain and PAE over the powerbar.

FIGURE 10: Distributed characteristics and performance at maximum efficiency point.

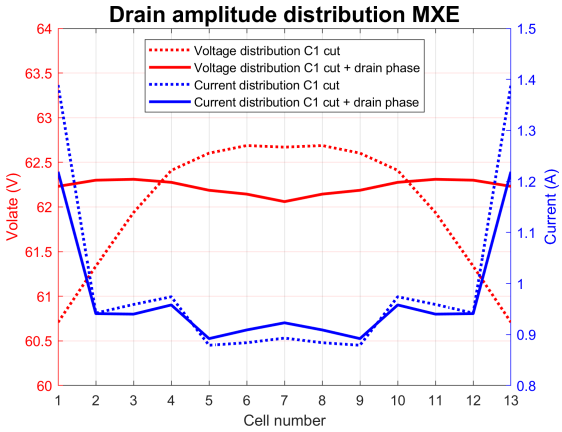
B4: Drain current phase optimisation + C1 rail cut



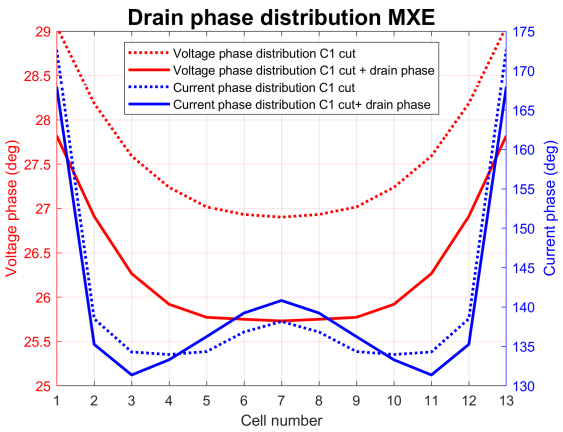
(A) Voltage and current amplitude at the gate.



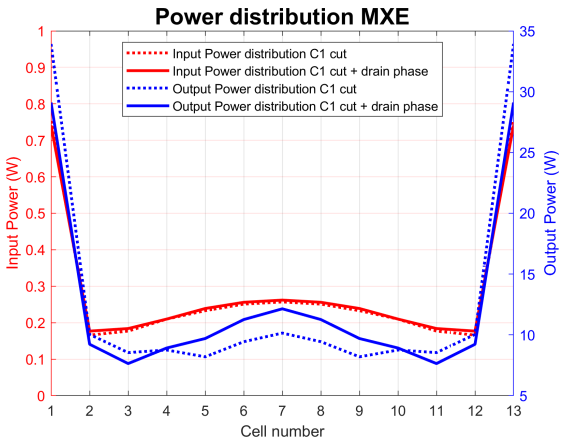
(B) Voltage and current phase at the gate.



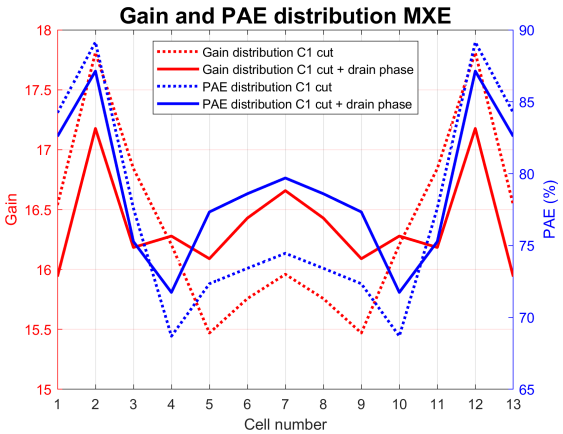
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

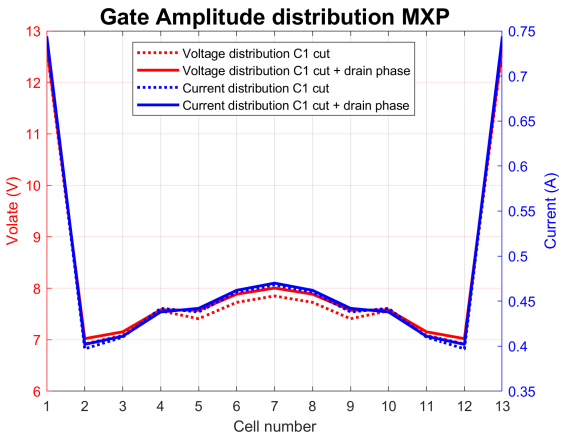


(E) In and output power.

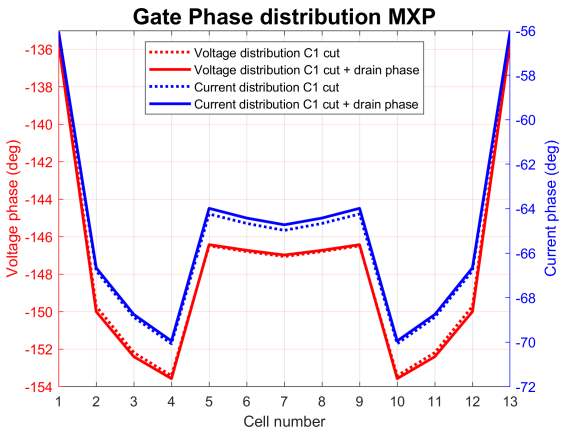


(F) Gain and PAE over the powerbar.

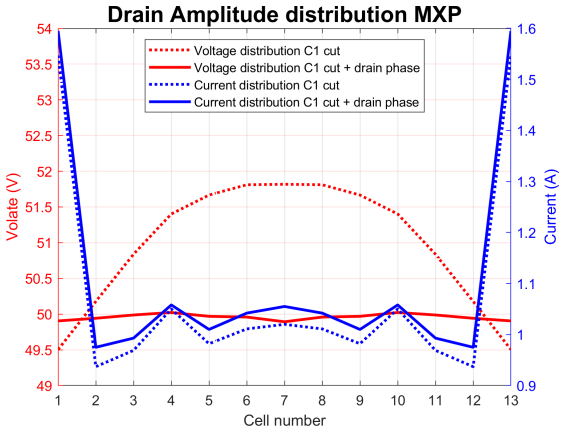
FIGURE 11: Distributed characteristics and performance at maximum efficiency point.



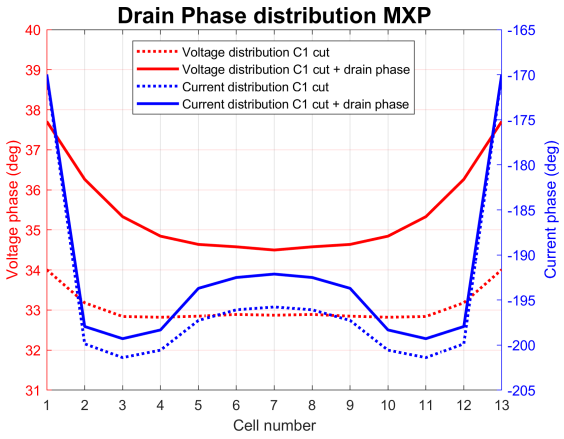
(A) Voltage and current amplitude at the gate.



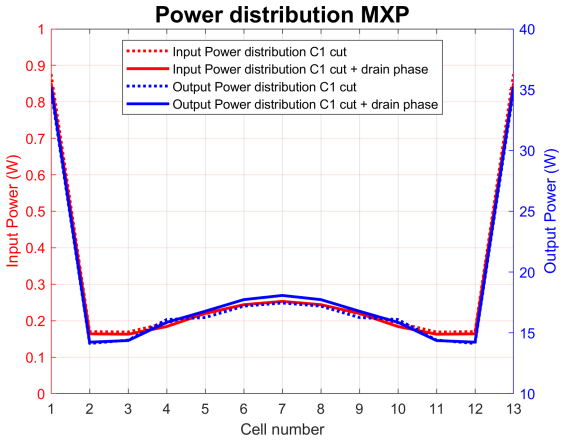
(B) Voltage and current phase at the gate.



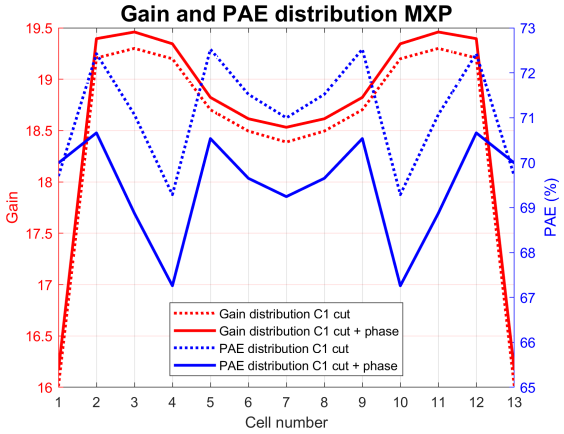
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



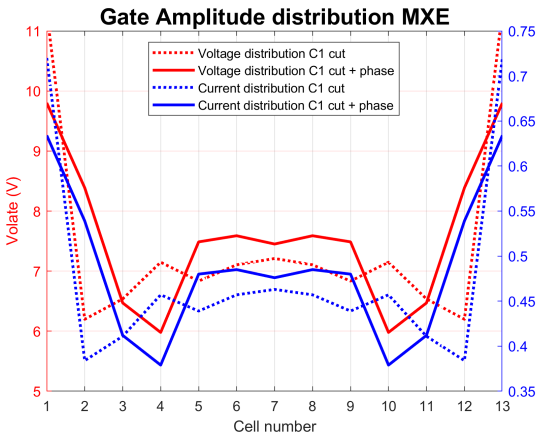
(E) In and output power.



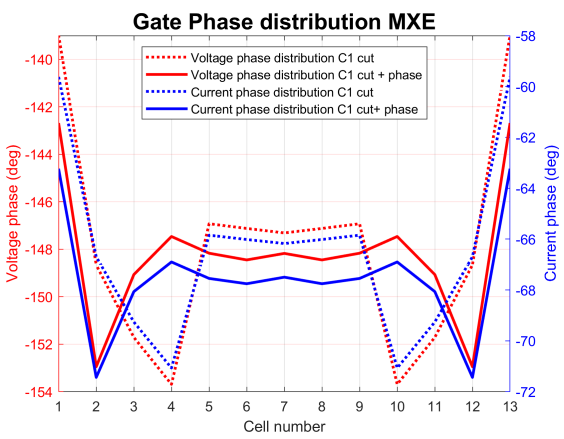
(F) Gain and PAE over the powerbar.

FIGURE 12: Distributed characteristics and performance at maximum efficiency point.

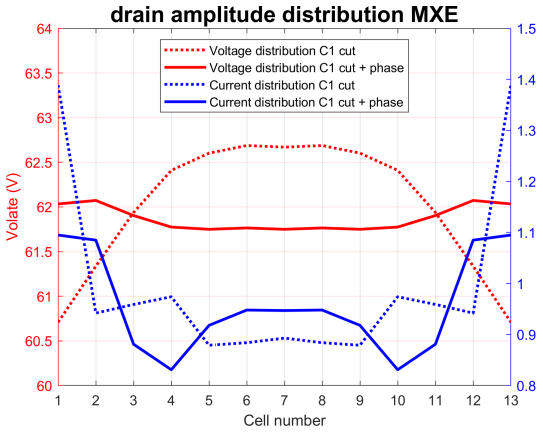
B5: Drain & gate current phase optimisation + C1 rail cut



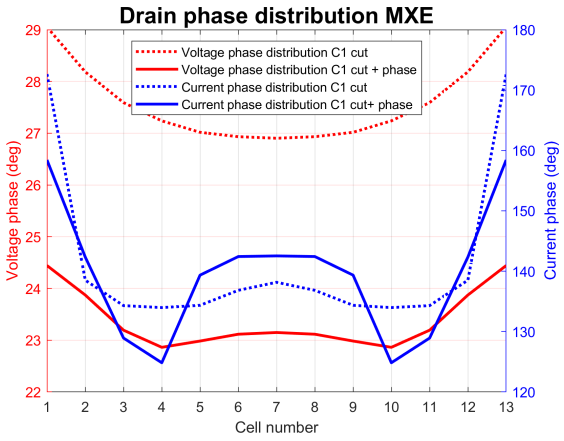
(A) Voltage and current amplitude at the gate.



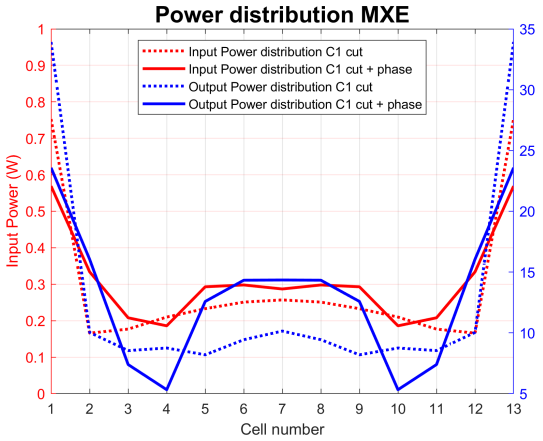
(B) Voltage and current phase at the gate.



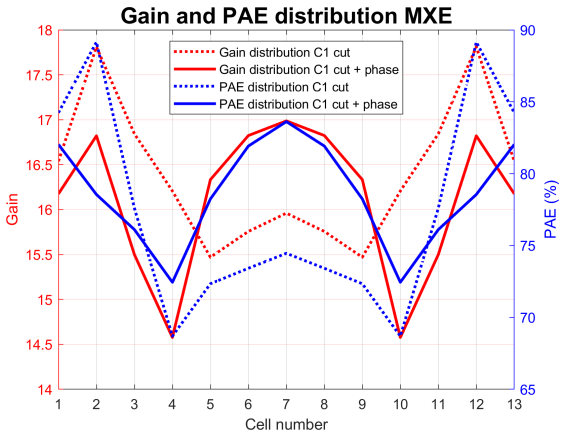
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

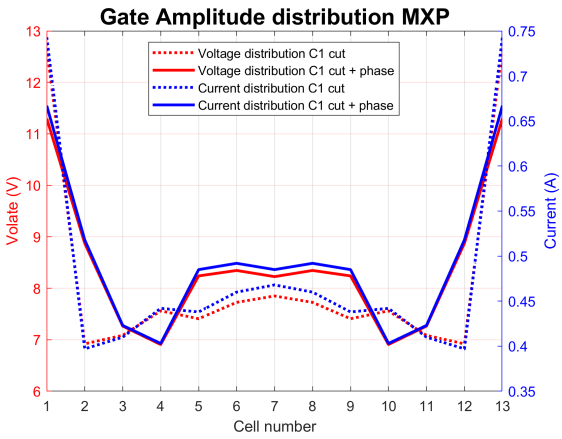


(E) In and output power.

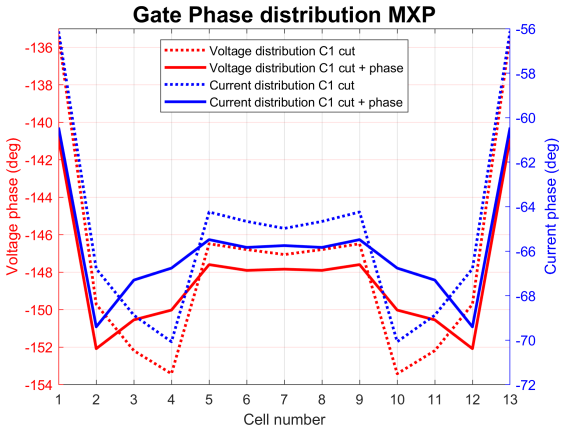


(F) Gain and PAE over the powerbar.

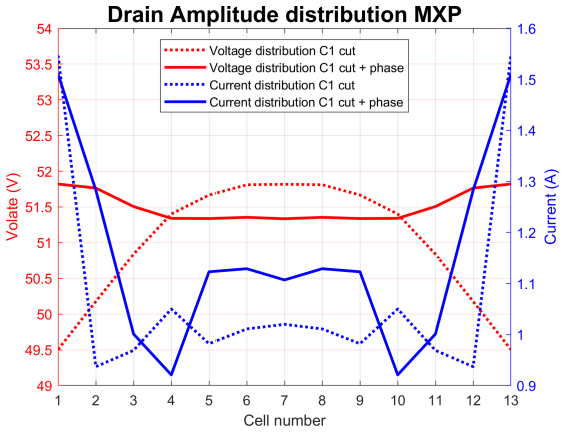
FIGURE 13: Distributed characteristics and performance at maximum efficiency point.



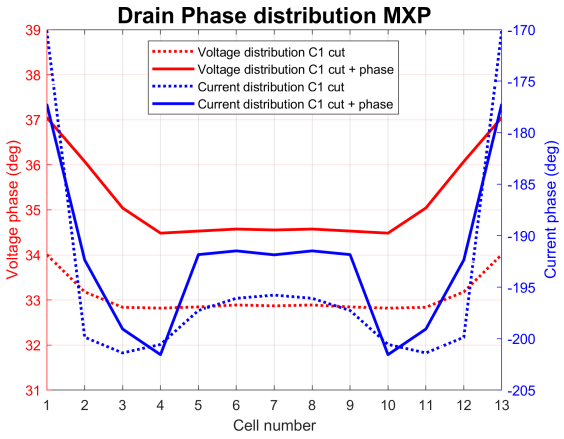
(A) Voltage and current amplitude at the gate.



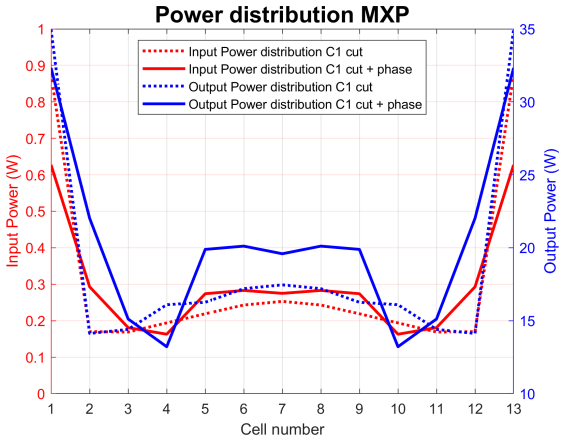
(B) Voltage and current phase at the gate.



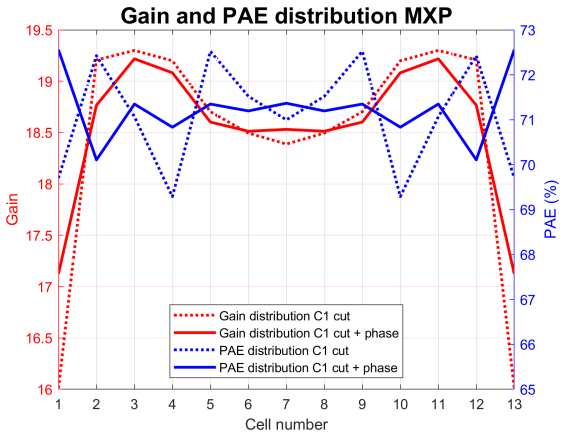
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



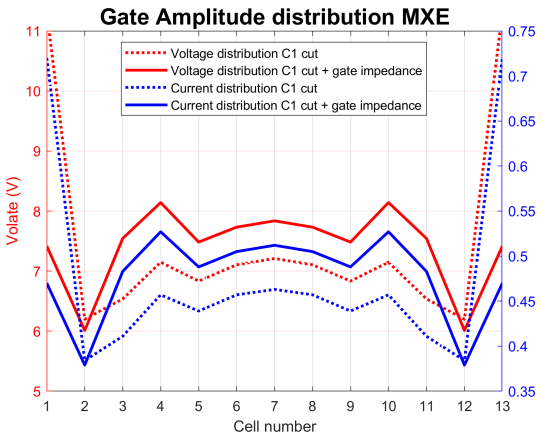
(E) In and output power.



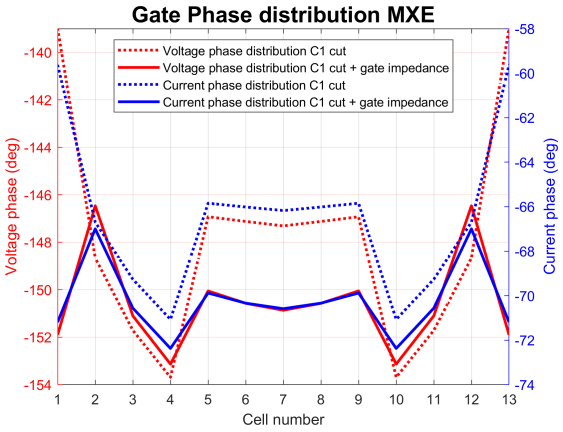
(F) Gain and PAE over the powerbar.

FIGURE 14: Distributed characteristics and performance at maximum efficiency point.

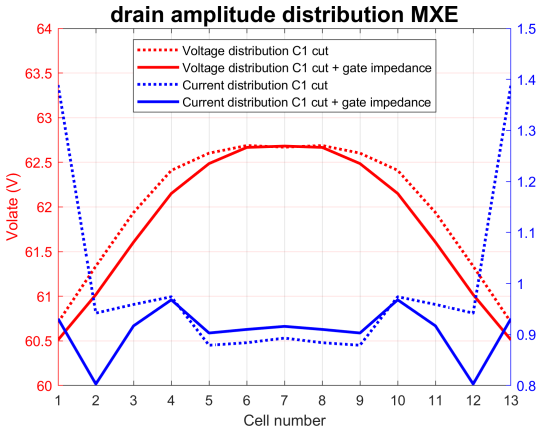
B5: Gate inductance optimisation + C1 rail cut



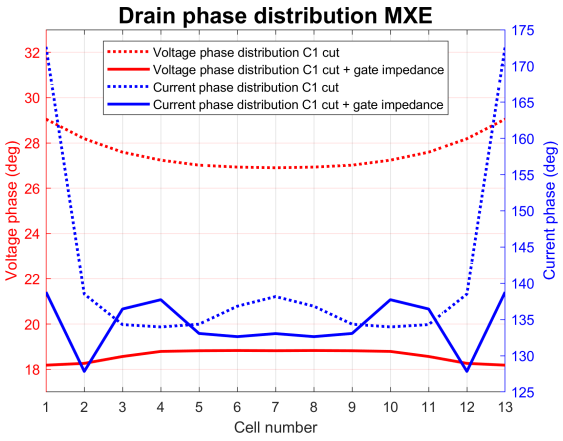
(A) Voltage and current amplitude at the gate.



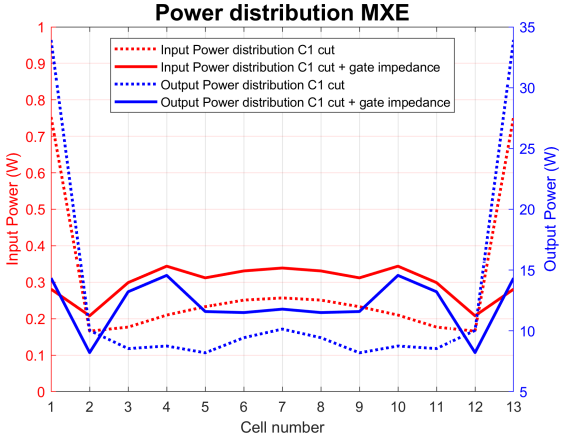
(B) Voltage and current phase at the gate.



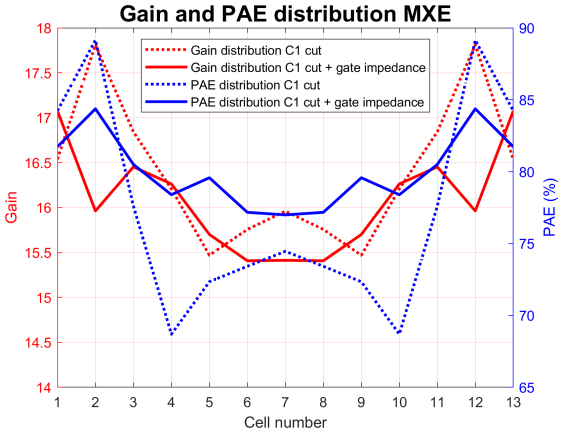
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

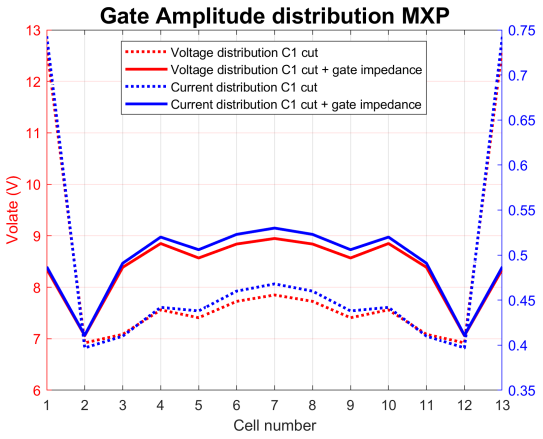


(E) In and output power.

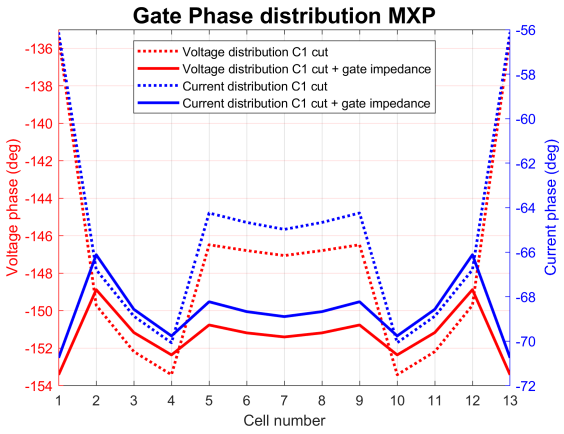


(F) Gain and PAE over the powerbar.

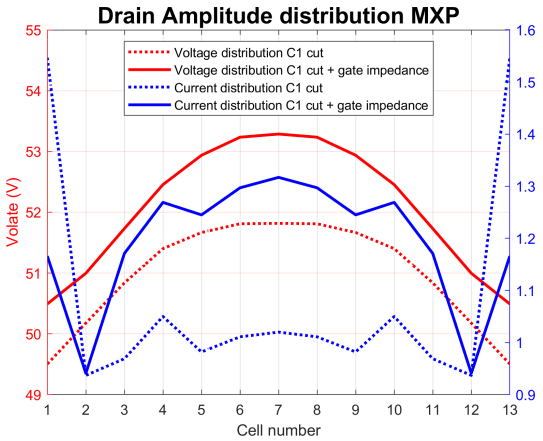
FIGURE 15: Distributed characteristics and performance at maximum efficiency point.



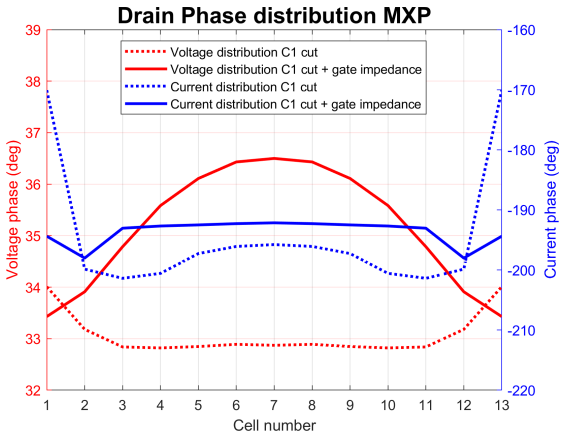
(A) Voltage and current amplitude at the gate.



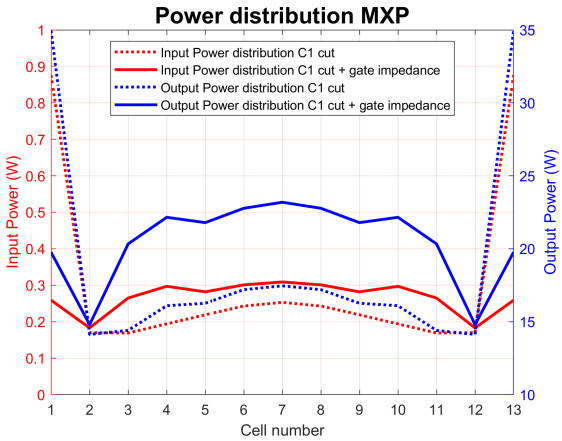
(B) Voltage and current phase at the gate.



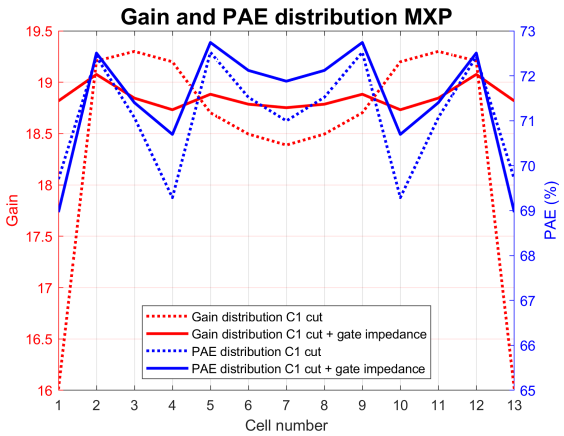
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



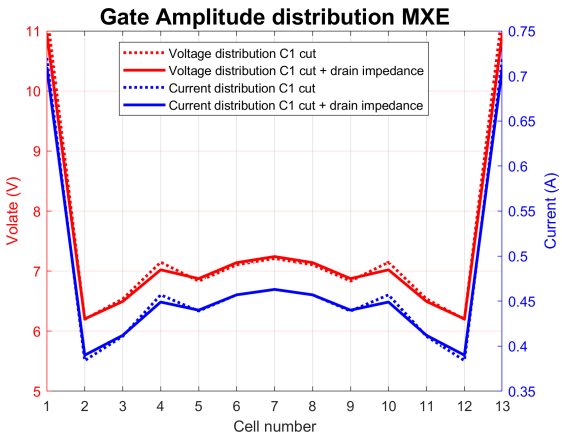
(E) In and output power.



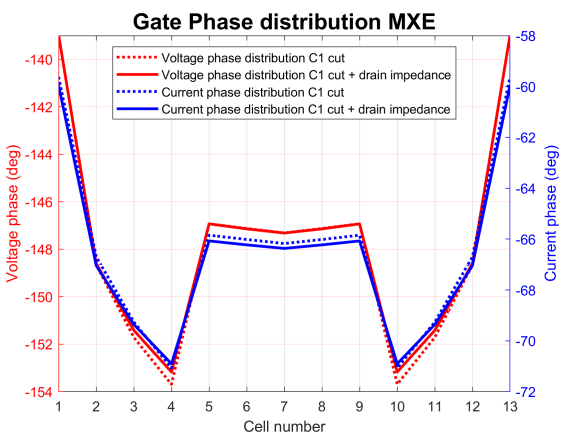
(F) Gain and PAE over the powerbar.

FIGURE 16: Distributed characteristics and performance at maximum efficiency point.

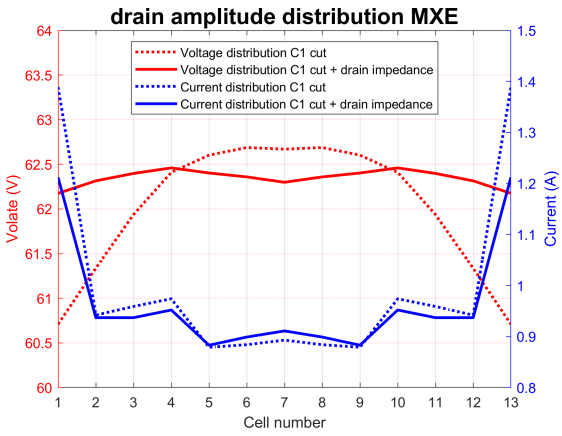
B5: Drain inductance optimisation + C1 rail cut



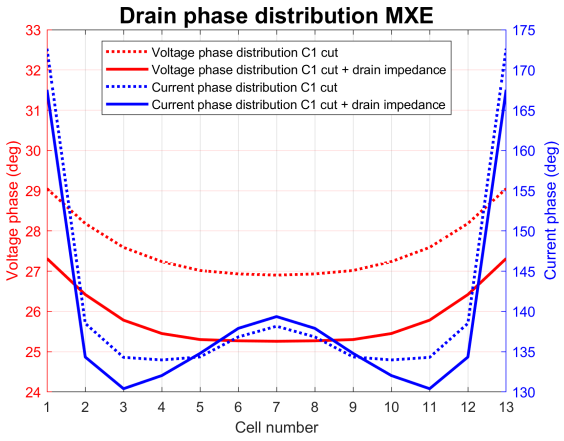
(A) Voltage and current amplitude at the gate.



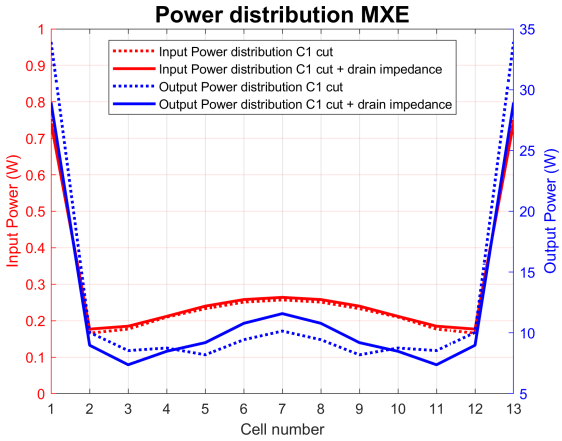
(B) Voltage and current phase at the gate.



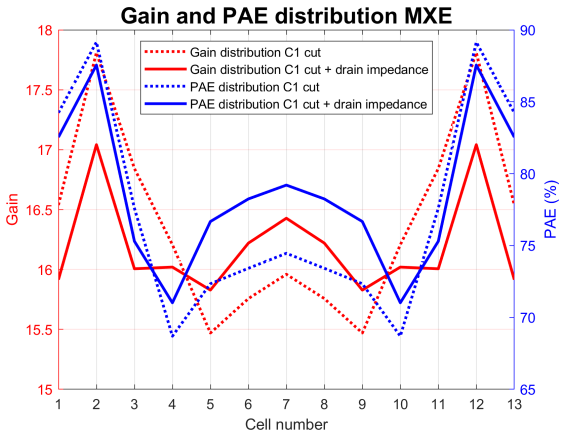
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

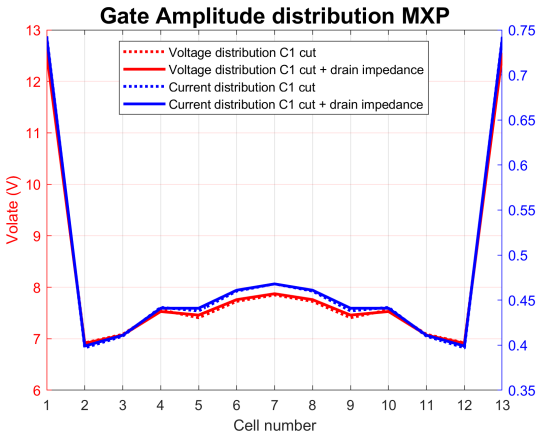


(E) In and output power.

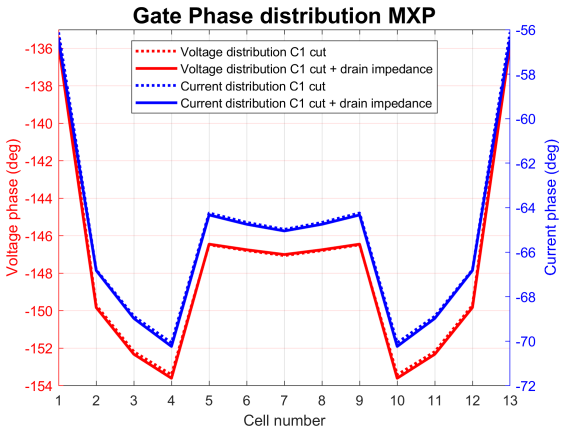


(F) Gain and PAE over the powerbar.

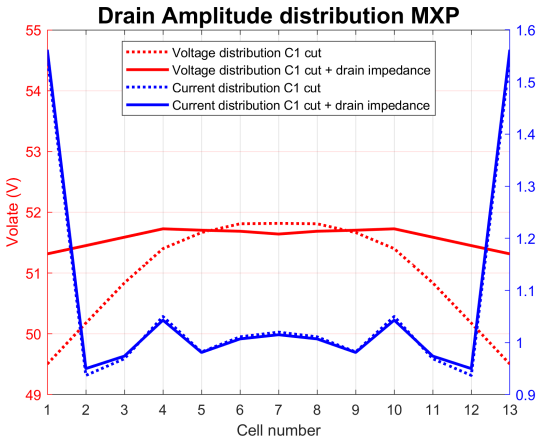
FIGURE 17: Distributed characteristics and performance at maximum efficiency point.



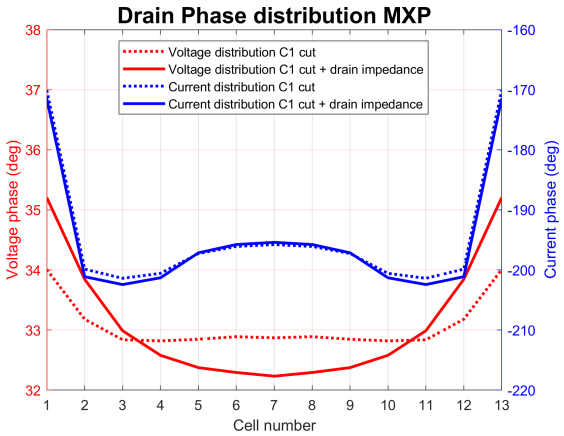
(A) Voltage and current amplitude at the gate.



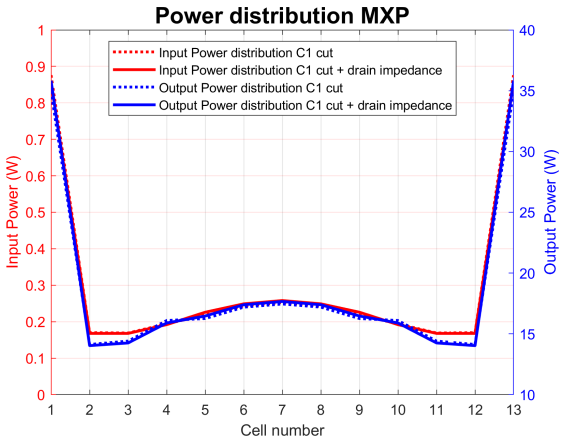
(B) Voltage and current phase at the gate.



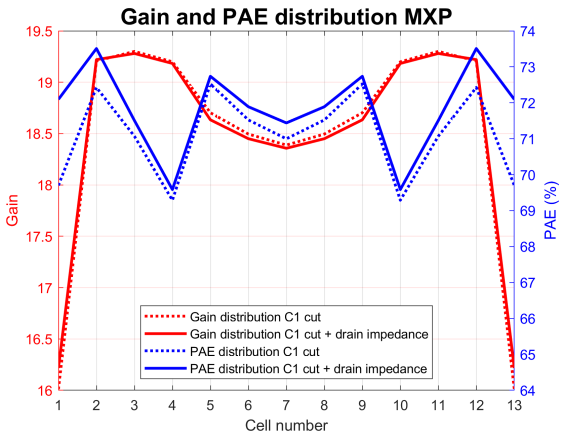
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



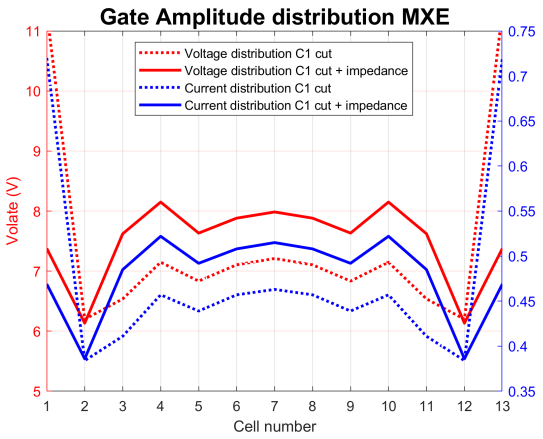
(E) In and output power.



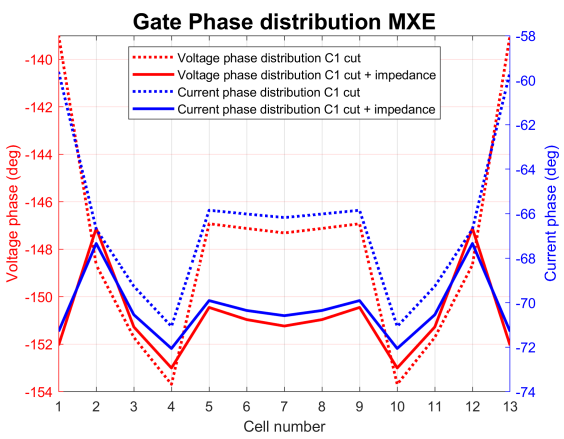
(F) Gain and PAE over the powerbar.

FIGURE 18: Distributed characteristics and performance at maximum efficiency point.

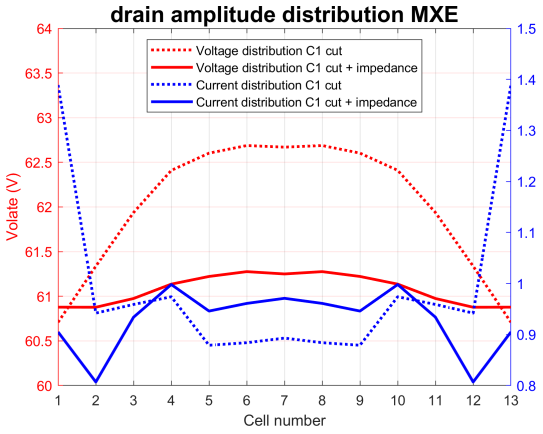
B5: Drain & gate inductance optimisation + C1 rail cut



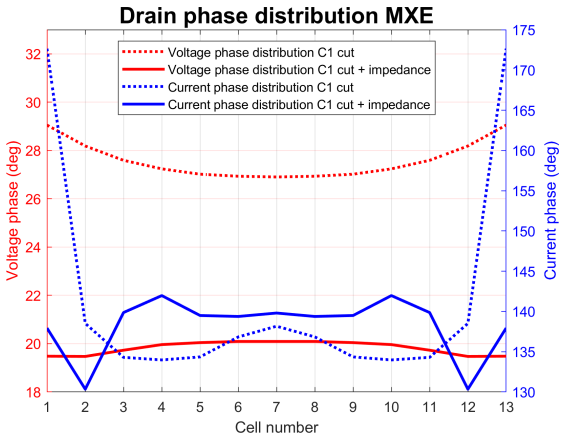
(A) Voltage and current amplitude at the gate.



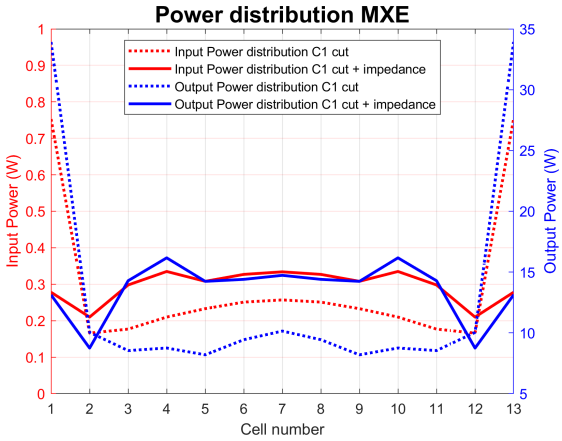
(B) Voltage and current phase at the gate.



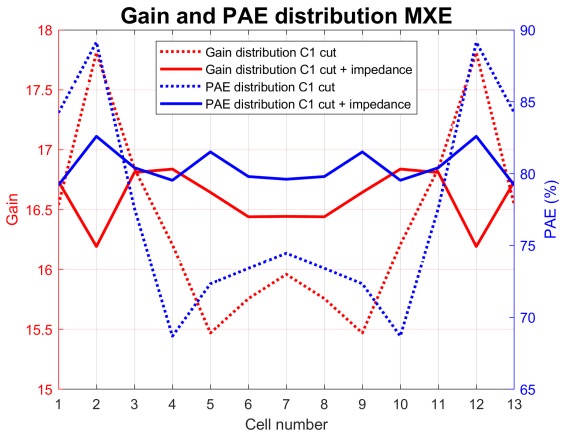
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.

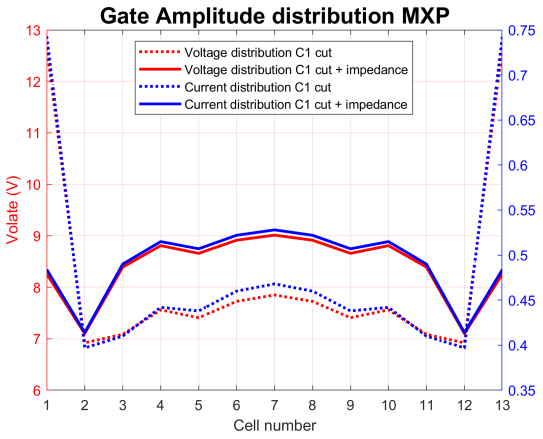


(E) In and output power.

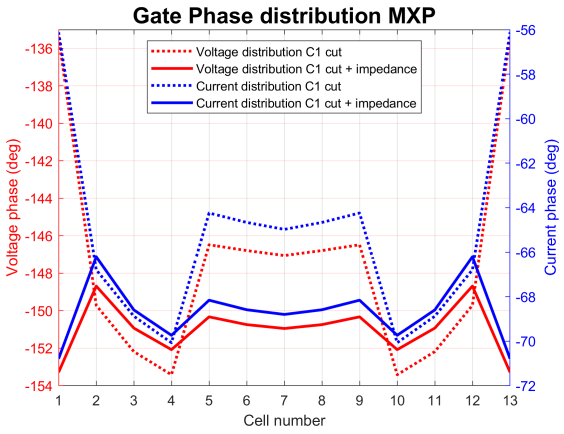


(F) Gain and PAE over the powerbar.

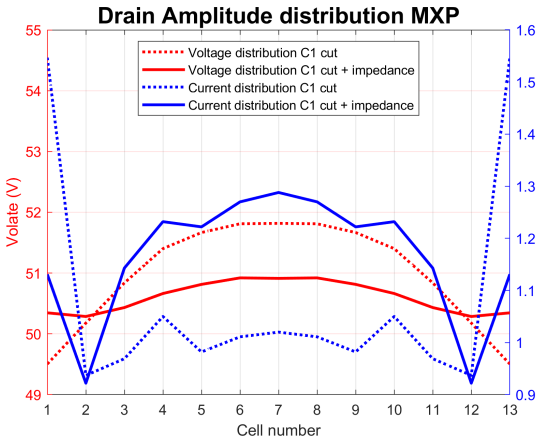
FIGURE 19: Distributed characteristics and performance at maximum efficiency point.



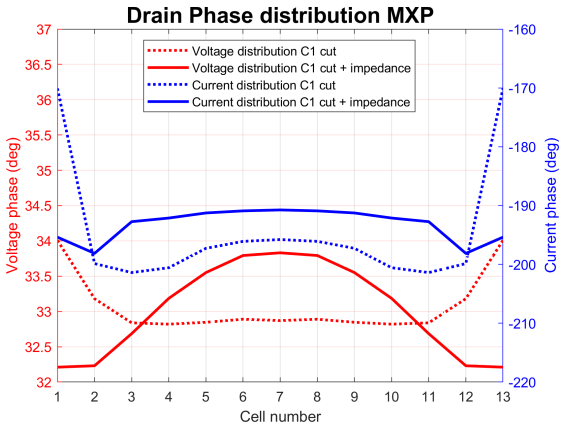
(A) Voltage and current amplitude at the gate.



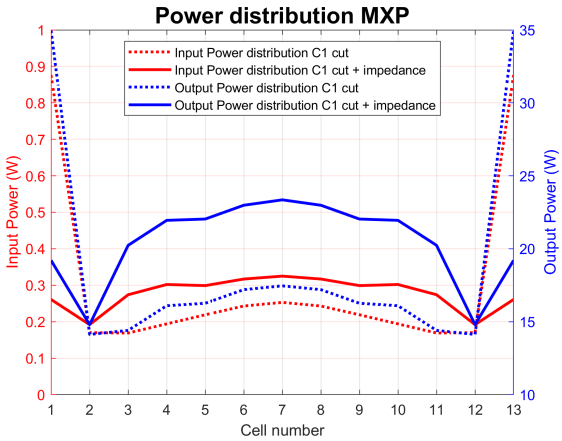
(B) Voltage and current phase at the gate.



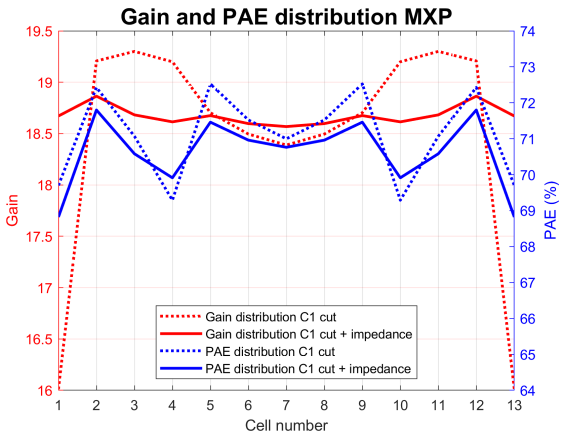
(C) Voltage and current amplitude at the Drain.



(D) Voltage and current phase at the Drain.



(E) In and output power.



(F) Gain and PAE over the powerbar.

FIGURE 20: Distributed characteristics and performance at maximum efficiency point.