Switching Loss Characterization of Wide Bandgap Semiconductor Devices

Gulin Kesapli
Faculty of Electrical Engineering, Mathematics and Computer Science
University of Twente, Enschede, NL

***Abstract*—Wide bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN), are improving modern power electronics due to their ability to operate at higher voltages, frequencies, and temperatures with significantly lower switching losses than conventional silicon devices [1]. Accurate characterization of these switching losses is crucial for optimizing power inverter performance, reducing energy usage, and guiding thermal design. This thesis presents a comprehensive investigation of the switching behavior of WBG devices through the implementation of the Double Pulse Test (DPT), a widely accepted method for dynamic characterization [2]. A complete test setup was simulated with a gate driver circuit. The variation in voltage, current, inductor value and gate resistor analyzed throughout the simulations. The switching loss and time parameters were calculated for a SiC MOSFET and two Si IGBTs and compared with the datasheet, while discussing the reasons for differences between simulations and datasheet values. In addition to simulations, measurements were carried out for the SiC MOSFET and one of the IGBTs to compare their switching losses under real operating conditions. The study concludes with an efficiency analysis using a full-bridge inverter circuit built with SiC MOSFETs and Si IGBT, demonstrating how switching behavior impacts overall power conversion efficiency with the variation in switching frequency. At lower switching frequencies, both devices show similar efficiency around 99%. However, as the frequency increases, the efficiency of the Si IGBT decreases more significantly compared to the SiC MOSFET.**

I. Introduction

Due to rising global population and increasing energy demand, annual energy consumption continues to grow. Meeting this demand with traditional silicon (Si)-based power electronics is becoming increasingly challenging. While silicon remains the most widely used semiconductor material due to its natural abundance and mature processing technology, it has reached its fundamental performance limits [3]. This has driven the search for alternative materials with superior electrical characteristics.

Wide bandgap (WBG) semiconductors, such silicon carbide (SiC) and gallium nitride (GaN), are becoming more and more popular due to the demand for energy-efficient power electronics. As shown in Figure 2, compared with traditional silicon (Si)-based semiconductors devices, WBG materials provide higher energy gap which results in higher breakdown electric fields. They further provide lower switching losses, and faster switching speeds. WBG semiconductors are suitable for more compact, highly efficient power converters to be used in a variety of applications, such as electric vehicles

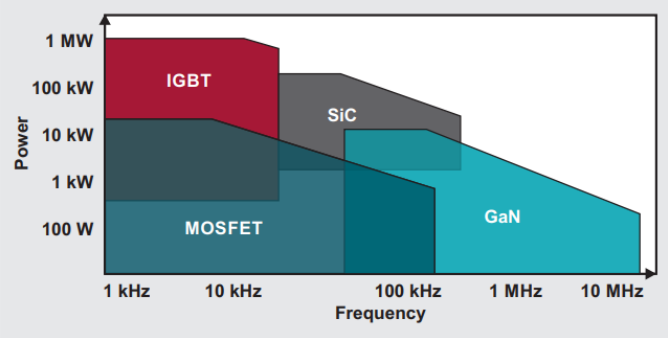

Fig. 1: Characteristics of Power Devices [4]

and renewable energy systems [1]. Based on Figure 1 SiC devices are more suitable for high power applications, whereas GaN devices are more suitable for higher frequency applications. Furthermore, MOSFETs are more suitable for higher frequency applications compared with IGBTs.

Despite their advantages, accurately measuring the switching loss of WBG devices is a challenge due to their high-speed transitions and sensitivity to parasitic elements in the circuit. One commonly used technique for dynamically characterizing semiconductor devices is the Double Pulse Test (DPT) [2].

This thesis investigates how to accurately characterize switching losses of WBG semiconductor devices using DPT. It explores the influence of parameters such as gate resistance, inductor, voltage and current on loss characterization. The primary research questions are : ***How to accurately characterize the switching losses of WBG semiconductor devices and what are the implications of the measurement results on the design of power inverters?*** A combination of simulation, experimental measurement, and inverter-level simulation is used to evaluate SiC MOSFET and Si IGBTs under different operating conditions.

II. Methodology

Wide bandgap semiconductor devices are more efficient than conventional semiconductor devices. The wide bandgap offers a higher breakdown electric field, lower switching losses, and faster switching times [1]. Characterizing these semiconductors are crucial to accurate usage in the power inverters. Double Pulse Test is a wide known circuit setup

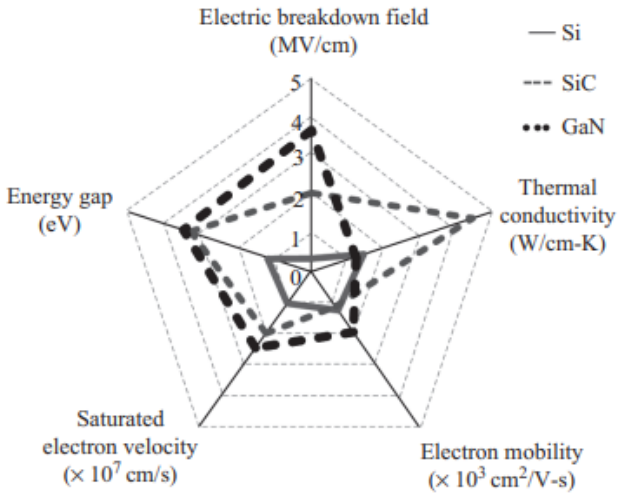

Fig. 2: Material Properties of Semiconductors [1]

for dynamic characterization of WBG semiconductor devices. It involves applying 2 consecutive pulses to turn on and turn off the power semiconductor devices such as MOSFETs or IGBTs to analyze their behaviours during turn on and turn off events. The circuit consists of an inductor, voltage source, semiconductor devices and additional gate driver circuit. Figure 3 illustrates the Double Pulse Test (DPT) setup used to characterize the switching behavior of wide bandgap (WBG) semiconductor devices. The system consists of a control side and a power side. On the control side, a PC programs a microcontroller that generates pulses for the device under test on the DPT board. An oscilloscope captures the resulting switching waveforms for post-processing. On the power side, a DC power supply provides the high-voltage input, a load inductor sets the switching current, and an auxiliary power supply powers the gate drivers. The following events occur[1]:

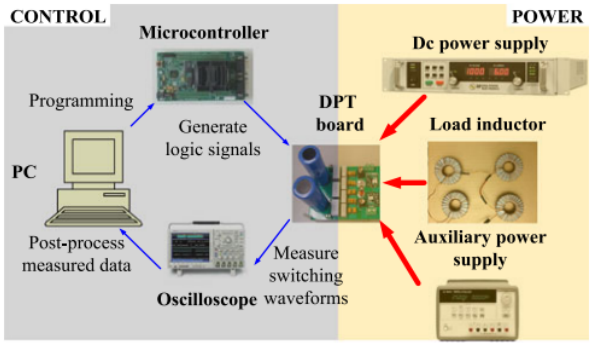

Fig. 3: Double Pulse Test Setup [2]

1) The first pulse is sent by a microcontroller to turn on the device under test(DUT) and to establish desired current level in the inductive load.
2) The first pulse ends when the current reaches to desired value and DUT is turned off. The turn off switching performance of DUT can be captured.
3) The second pulse is sent to turn on the device again and turn on switching behaviour can be obtained.
4) This completes the double pulse test.

The visual standard representation of the DPT circuit can be seen in Figure 4. The device under test is the bottom(low side) switch.

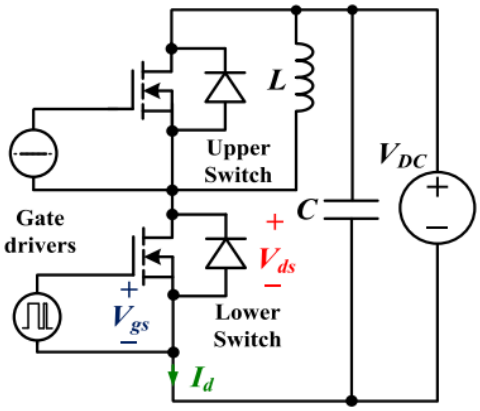

Fig. 4: Double Pulse Test Circuit [2]

1) Design of DPT: Each component in the DPT setup has certain limitations to not to violate the datasheet and ensure safe testing[1].

- *Load Inductor* is used to establish the current to the desired value during the first pulse and keep it constant during turn on and turn off events.

$$L_{min} \geq \frac{V_{DC}}{\Delta I_L} t_{sw} = \frac{V_{DC}}{k_{\Delta i} \times I_L} t_{sw} \tag{1}$$

V_{DC} is the bus voltage which supplies the voltage to the circuit. $k_{\Delta i}$ represents the current variation percentage during switching transitions, usually selected around 1-5%. I_L is the load current and t_{sw} is the time to complete a switching event and it is assumed to be written in the datasheet of each power device. The worst condition for load inductance is at maximum operating voltage and minimum operating current[2].

- *DC Voltage Source* is used to establish DC bus voltage. The rated voltage for the device should be higher than the DC voltage source to ensure safe operation.
- *Charge Pulse Time* is the duration of the first pulse applied to the DUT. It is set to enable load current to reach the desired value with the following equation[1]:

$$t_{charge} = L \frac{I_L}{V_{DC}} \tag{2}$$

- *Off Pulse Time* is the interval between the end of the first pulse and the start of the second pulse. It is set to ensure the turn-off transients are completed before the second

pulse and it should be longer than the turn-off time of the device[1].

- *Switching Time (t_{sw})* is the sum of rise time, fall time, turn on delay and turn off delay. Each device has their own way of measuring the switching time and even though these time parameters are not the main focus for this thesis, they will be discussed further.

Some sources argue that DPT circuit requires a decoupling capacitor and a bulk capacitor to maintain voltage over the power device while pulses are not sent [5], however it wasn't used in the LTSpice simulations to not to introduce more components into circuit with maintaining simplicity[2] [6]. For this thesis, 3 semiconductor devices were simulated:

1) CoolSiC™ 1200 V SiC MOSFET:IMZC120R078M2H [7]
2) Short circuit rugged 1200 V TRENCHSTOP™ IGBT:IKW25N120CS7 [8]
3) High speed 1200 V TRENCHSTOP™ IGBT:IKW40N120CH7 [9]

After the simulations, SiC MOSFET and IGBT:IKW25N120CS7 were used for the measurements and simulations for power inverter. The Device Under Test(DUT) is the bottom MOSFET or IGBT for all of the simulations, calculations and measurements.

Gate driver circuit is a essential part of testing with power devices. It is able to efficiently and reliably control power devices under various conditions. The gate driver circuit should precisely drive the semiconductor device from turn on to turn off state or vice versa with fast speed and low switching loss [10]. The gate driver circuit in Figure 5 uses different turn-on and turn-off resistors that are controlled by diodes to create a push-pull configuration. A pair of resistors and diodes are positioned in each gate drive side (high-side and low-side) to differentiate between the switching transitions. The top diode conducts when the gate drive voltage is high, which allows current to pass through the turn-on resistor and into the power device's gate, turning it on. On the other hand, the lower diode conducts when the gate voltage is low, passing current from the gate to ground via a separate turn-off resistor, turning off the power device[11]. The same gate driver circuit was used for all 3 devices, and it can be seen in Figure 5 [6]. The effect of gate resistance on switching loss will be discussed later.

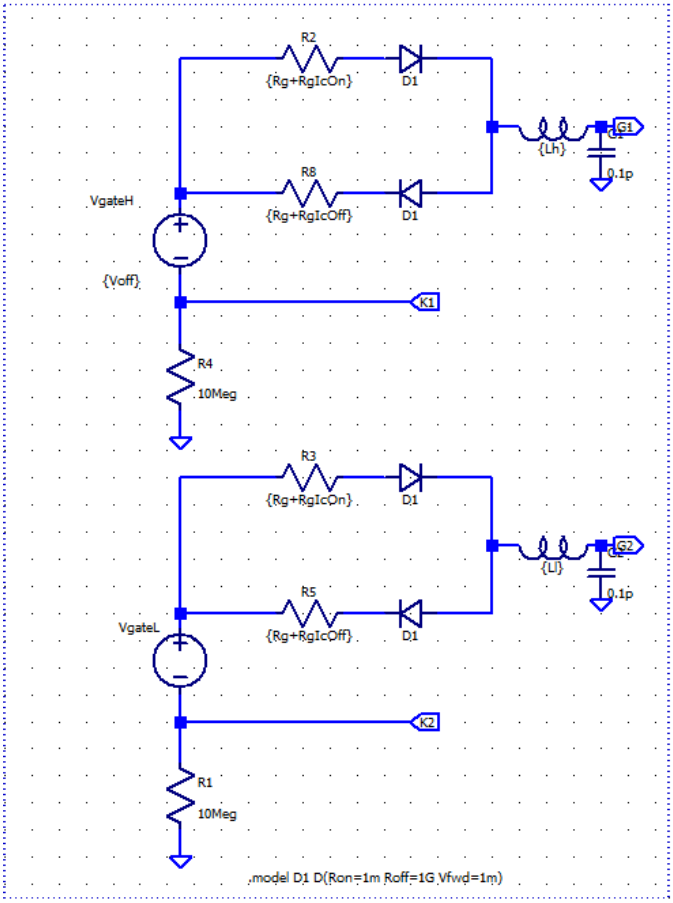

Fig. 5: Gate Driver Circuit

A. SiC MOSFET Simulations

For this thesis, the IMZC120R078M2H, a 1200 V SiC MOSFET from Infineon, was selected for simulation due to its high-speed switching capability, low on-resistance, and suitability for high-efficiency power inversion [7]. The objective of the simulation was to evaluate its dynamic behavior, particularly in a DPT setup, and to understand its switching performance under different parameters. The device was simulated using manufacturer-provided SPICE models, focusing on switching loss characterization. Power is defined as the product of drain-source voltage and drain-source current. Switching energy is calculated by integrating this power over a specific time interval. These time intervals differ for turn-on and turn-off events due to the distinct switching dynamics in each case. The turn-off and turn-on energies are defined as

$$E_{off} = \int_{t_1}^{t_2} (V_{DS} \cdot I_{DS})\, dt \tag{3}$$

$$E_{on} = \int_{t_3}^{t_4} (V_{DS} \cdot I_{DS})\, dt \tag{4}$$

t_1 is defined as the time when V_{DS} reaches 10% of the initial V_{DS} during the turn-off transition. t_2 is the time when I_{DS} falls to 10% of its maximum value during the same turn-off event, marking the end of the turn-off loss interval. t_3 is defined as the time when I_{DS} rises above 10% of its maximum value during the rising edge of the second pulse, initiating the turn-on event. t_4 is the time when V_{DS} falls to 10% of initial V_{DS} during the turn-on transition, completing the switching event[7].

In order to characterize this SiC MOSFET, LTSpice and MATLAB was used. The text file from the LTSpice's output

waveform was extracted to the MATLAB to calculate more precisely.The LTSpice model for the MOSFET was already created by the Infineon and it was succesfully added to LTSpice for testing. The initial simulation was to duplicate the operating conditions that was given in the datasheet and compare the differences between them. For dynamic characterization, the operating conditions and parameters from the datasheet and simulations can be seen in Table I.

Operating Conditions	Parameter	Value
$V_{DD} = 800\,\text{V}$, $I_D = 9\,\text{A}$	Turn-on delay time ($t_{d(on)}$)	5 ns
$V_{GS} = 0/18\,\text{V}$	Rise time (t_r)	3.2 ns
$R_{GS(on)} = R_{GS(off)} = 2.3\,\Omega$	Turn-off delay time ($t_{d(off)}$)	11.7 ns
$L_\sigma = 12\,nH$	Fall time (t_f)	4.8 ns
$T_{vj} = 25°C$	Turn-on energy (E_{on})	57 μJ
	Turn-off energy (E_{off})	22 μJ

TABLE I: Switching parameters of IMZC120R078M2H under typical operating conditions

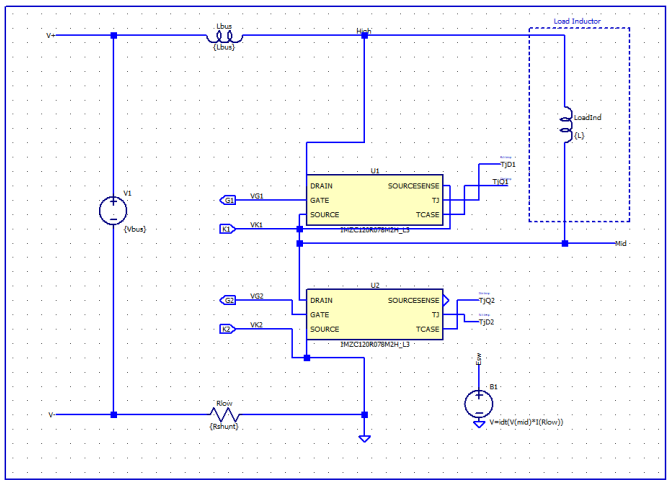

Fig. 6: SiC MOSFET DPT Simulation Schematic

Turn-on delay time $t_{d(on)}$ is defined as the time between the gate voltage V_{GS} reaching 10% of its value and the drain-source voltage V_{DS} reaching 90% of its initial value during the turn-on transition [7].

Rise time t_r is defined as the time it takes for V_{DS} to fall from 90% to 10% of its initial value during the turn-on event [7].

Turn-off delay time $t_{d(off)}$ is defined as the time between the gate voltage V_{GS} reaching 90% of its value and the drain-source voltage V_{DS} reaching 10% of its value during the turn-off transition [7].

Fall time t_f is defined as the time it takes for V_{DS} to rise from 10% to 90% of its final value during the turn-off event [7].

V_{DC} and I_L are known therefore, we can calculate the inductor value and charge pulse time based on equations 1 and 2, respectively. In these simulations, the load current corresponds to the drain-source current of the low-side MOSFET; therefore, the two terms can be used interchangeably.

$$L_{min} = \frac{V_{DC}}{k_{\Delta i} \times I_L} t_{sw} = \frac{800 \cdot 24.7 \cdot 10^{-9}}{0.03 \cdot 9} = 73.185 \mu H \quad (5)$$

$$t_{charge} = L \frac{I_L}{V_{DC}} = 0.8233 \mu s \quad (6)$$

L was chosen 80 μH for convenience and a shunt resistor of $2.5 m\Omega$ was added to the circuit to measure the drain-source current more easily.

The DPT schematic for SiC MOSFET can be seen in Figure 6 and corresponding waveform according to datasheet conditions can be seen in Figure 7. The obtained parameters can be seen in Table II.

The switching loss depends on various parameters such as DC voltage, drain-source current and gate resistance . The change in DC voltage and drain-source current causes the inductor value to change (eq 1), however charging time remains the same (eq 2). The inductor values based on

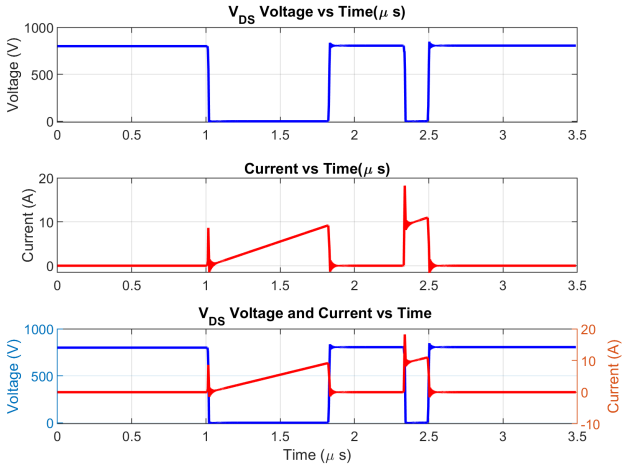

Fig. 7: Waveform of SiC MOSFET-standard conditions

Parameter	Value
Turn-on delay time ($t_{d(on)}$)	9.98 ns
Rise time (t_r)	5.14 ns
Turn-off delay time ($t_{d(off)}$)	14.791 ns
Fall time (t_f)	6.6 ns
Turn-on energy (E_{on})	55.42 μJ
Turn-off energy (E_{off})	12.96 μJ

TABLE II: Switching parameters of the simulation of IMZC120R078M2H under typical operating conditions

different DC voltages can be seen in Table III. The other parameters remained the same as the datasheet conditions, only DC voltage varies.

DC Voltage Value	Inductor Value
100V	$10\mu H$
200V	$20\mu H$
300V	$30\mu H$
400V	$40\mu H$
500V	$50\mu H$
600V	$60\mu H$
700V	$70\mu H$
800V	$80\mu H$

TABLE III: Different inductor values for different DC voltages

The same method was used to calculate inductor values for different drain-source current values and it can be seen in Table IV.

Drain-source current value	Inductor Value
2A	$350\mu H$
5A	$150\mu H$
9A	$80\mu H$
12A	$55\mu H$
15A	$45\mu H$
18A	$37\mu H$

TABLE IV: Different inductor values for different drain current

Change in gate driver parameters has no effect on the inductor value and charge pulse time, therefore the effects of gate driver circuit, specifically resistor, will be discussed in the next section.

Another way of measuring turn on and turn off energy is with using a behavioral voltage source in the LTSpice simulation [6]. Behavioral voltage source outputs the output voltage in terms of the given relation with the other parameters. To calculate turn off and turn on energy, V_{DS} and I_{DS} was multiplied, integrated over time and multiplied with 1J/1V to convert to Joules.The difference between the maximum and minimum value during the turn-off window results in the turn-off energy and vice versa. However, this is not the approach that is being used for switching loss calculations since this includes the whole range of V_{DS} and I_{DS}, not only 10% or 90% and it results in slightly higher switching loss than expected.

B. IGBT Simulation

Insulated Gate Bipolar Transistors(IGBTs) are widely used in power electronics field to be used in power inverters. It combines the advantages of MOSFETs (voltage-controlled) and bipolar junction transistors (high current capacity) to handle both high voltage and high current applications efficiently. They offer fast switching characteristic with minimal loss[12]. To compare the performance with SiC MOSFET, 2 different IGBTs were simulated : IKW25N120CS7 and IKW40N120CH7 from Infineon. They both offer fast switching characteristics and low switching losses [8] [9]. For these switches, the same DPT setup was used but parameters were adjusted for each IGBT to operate safely. The switching losses for both IGBTs are defined the same as follows:

$$E_{off} = \int_{t_1}^{t_2} (V_{CE} \cdot I_{CE})\ dt \tag{7}$$

$$E_{on} = \int_{t_3}^{t_4} (V_{CE} \cdot I_{CE})\ dt \tag{8}$$

$$\tag{9}$$

V_{CE} is the voltage between collector-emitter of the IGBT and I_{CE} is the collector-emitter current. t_1 is the time when gate-emitter voltage is 90% of its initial value during the turn off window. t_2 is the time when collector-emittor current is 2% of its initial value during the turn off window.t_3 is the time when gate-emitter voltage is at its 10% during the turn on window and t_4 is the time when the collector-emitter voltage is at 2% of its original value. First, the IGBTs' LTSpice models were successfully added to LTSpice for testing after being previously developed by Infineon. The purpose of the first simulation was to replicate the operating conditions listed in the datasheet and compare the differences. Table V and VI display the parameters and operating conditions from the datasheet of both IGBTs and simulations for dynamic characterization, respectively.

Operating Conditions	Parameter	Value
$V_{CE} = 600\,\text{V}$, $I_C = 25\,\text{A}$ $V_{GE} = 0/15\,\text{V}$ $R_{GS(on)} = R_{GS(off)} = 6\,\Omega$ $T_{vj} = 25°C$	Turn-on delay time ($t_{d(on)}$)	21 ns
	Rise time (t_r)	13 ns
	Turn-off delay time ($t_{d(off)}$)	160 ns
	Fall time (t_f)	100 ns
	Turn-on energy (E_{on})	1.20 mJ
	Turn-off energy (E_{off})	1.10 mJ

TABLE V: Switching parameters of IKW25N120CS7 under typical operating conditions

Operating Conditions	Parameter	Value
$V_{CE} = 600\,\text{V}$, $I_C = 40\,\text{A}$ $V_{GE} = 0/15\,\text{V}$ $R_{GS(on)} = R_{GS(off)} = 10\,\Omega$ $T_{vj} = 25°C$	Turn-on delay time ($t_{d(on)}$)	36 ns
	Rise time (t_r)	22 ns
	Turn-off delay time ($t_{d(off)}$)	336 ns
	Fall time (t_f)	45 ns
	Turn-on energy (E_{on})	1.69 mJ
	Turn-off energy (E_{off})	0.92 mJ

TABLE VI: Switching parameters of IKW40N120CH7 under typical operating conditions

The definitions of switching times are different than the MOSFET but they are the same for both of the IGBTs [8] [9]. Turn off delay time is the difference between when the collector-emitter current reaches 90% of its original value and when the gate-emitter voltage reaches 90% of its initial

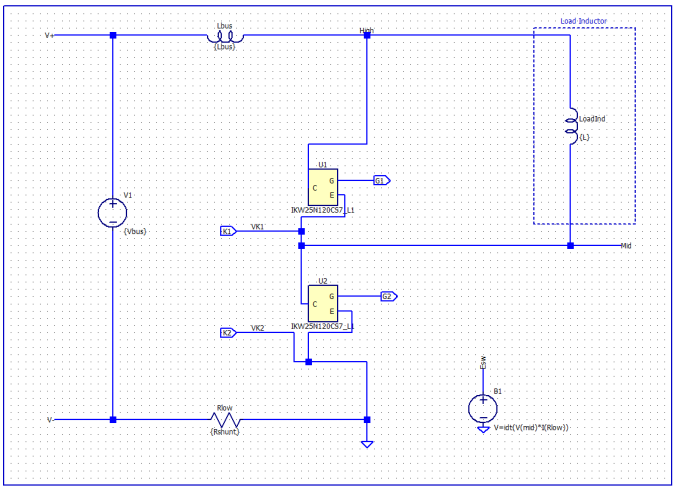

Fig. 8: IGBT:IKW25N120CS7 DPT Simulation Schematic

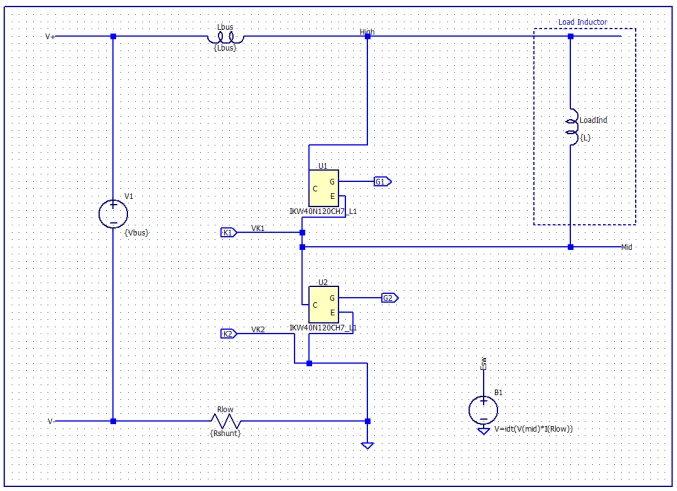

Fig. 9: IGBT: IKW40N120CH7 DPT Simulation Schematic

value. Fall time is the difference between 90% and 10% of collector-emitter current during turn off window. Turn on delay time is the difference between 10% of collector-emitter current and gate-emitter voltage during the turn on window and rise time is the difference between 90% and 10% of the collector-emitter current during turn on event.

The calculations for inductor and charge time are the same, as can be seen in the calculations below: For IKW25N120CS7:

$$L_{min} = \frac{V_{DC}}{k_{\Delta i} \times I_L} t_{sw} = \frac{600 \cdot 294 \cdot 10^{-9}}{0.02 \cdot 25} = 352.8 \mu H \quad (10)$$

$$t_{charge} = L \frac{I_L}{V_{DC}} = 14.7 \mu s \quad (11)$$

For IKW40N120CH7:

$$L_{min} = \frac{V_{DC}}{k_{\Delta i} \times I_L} t_{sw} = \frac{600 \cdot 439 \cdot 10^{-9}}{0.02 \cdot 40} = 329.25 \mu H \quad (12)$$

$$t_{charge} = L \frac{I_L}{V_{DC}} = 21.95 \mu s \quad (13)$$

For convenience, the inductor value and charge pulse time for IKW25N120CS7 were rounded up to $400 \mu H$ and 15 μs. Similarly, the values were rounded up to 350 μH and 22 μs for IKW40N120CH7. The switching parameters for both IGBTs under typical operating conditions can be seen in Table VII.

The DPT schematic for IKW25N120CS7 can be seen in Figure 8 and the corresponding waveform according to datasheet conditions can be seen in Figure 10. Similarly, DPT schematic for IKW40N120CH7 can be seen in Figure 9 and the corresponding waveform according to datasheet conditions can be seen in Figure 11.

Different V_{CE} and I_{CE} affect the turn off and turn on energies and changes in these parameters result in a variation in inductor value. The corresponding inductor value for different operating conditions can be seen in Tables VIII and VIII for IKW25N120CS7, and in Table X and XI for IKW40N120CH7.

Parameter	IKW25N120CS7	IKW40N120CH7
Turn-on delay time ($t_{d(on)}$)	20.716 ns	31.685 ns
Rise time (t_r)	40.98 ns	33.080 ns
Turn-off delay time ($t_{d(off)}$)	82.66 ns	251.724 ns
Fall time (t_f)	176.331 ns	78.174 ns
Turn-on energy (E_{on})	1.25696 mJ	1.22287 mJ
Turn-off energy (E_{off})	1.01004 mJ	850.982 μJ

TABLE VII: Switching parameters of the simulation of IGBTs under typical operating conditions

The effect of variation in gate driver circuit will be discussed in the next section as SiC MOSFET.

SiC MOSFET and IGBT IKW25N120CS7 have similar current ratings and therefore, to compare fairly, these 2

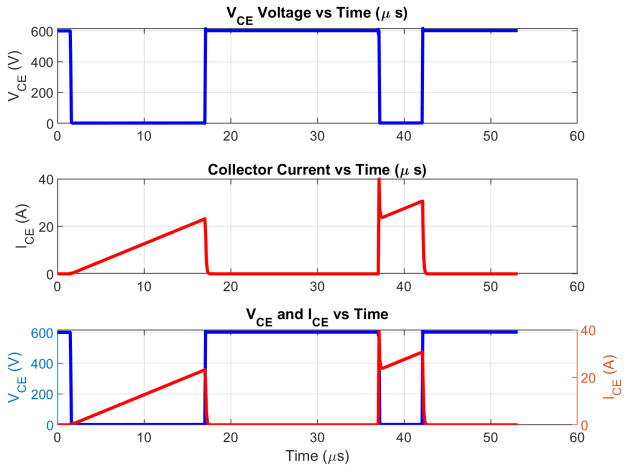

Fig. 10: Waveform of IGBT:IKW25N120CS7-standard conditions

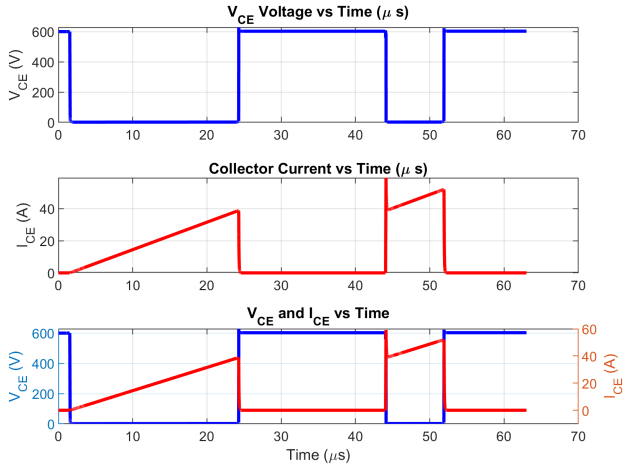

Fig. 11: Waveform of IGBT: IKW40N120CH7-standard conditions

DC Voltage Value	Inductor Value
50V	$30\mu H$
100V	$60\mu H$
200V	$120\mu H$
300V	$180\mu H$
400V	$240\mu H$
500V	$300\mu H$
600V	$400\mu H$
700V	$420\mu H$

TABLE VIII: IKW25N120CS7:Different inductor values for different DC voltages

Collector Current	Inductor Value
5A	$2mH$
10A	$1mH$
15A	$600\mu H$
20A	$450\mu H$
25A	$400\mu H$

TABLE IX: IKW25N120CS7:Different inductor values for different collector current

DC Voltage Value	Inductor Value
50V	$30\mu H$
100V	$60\mu H$
200V	$120\mu H$
300V	$180\mu H$
400V	$240\mu H$
500V	$300\mu H$
600V	$350\mu H$
700V	$400\mu H$

TABLE X: IKW40N120CH7:Different inductor values for different DC voltages

Collector Current	Inductor Value
5A	$3mH$
10A	$1.5mH$
15A	$900\mu H$
20A	$700\mu H$
30A	$500\mu H$
50A	$300\mu H$
65A	$250\mu H$

TABLE XI: IKW40N120CH7:Different inductor values for different collector current

semiconductor devices were used in the measurements and simulations for power inverter.

C. Measurements

In order to validate the chosen semiconductor devices, Double Pulse Test was conducted in the Power Electronics Lab. 2 pulses were sent by TI microcontroller through laptop and a previously designed gate driver circuit was used with 15/-5V and 8 Ω resistor. The setup can be seen in Figure 12. The voltage probe measures the drain-source voltage of the power device and current sensor measures the drain-source current for the power device. Similarly, voltage probe measures the collector-emitter of the voltage and current sensor measures the collector-emitter current for the low side IGBT and the values can be seen by the oscilloscope. Due to the availability and similar current ratings, IGBT:IKW25N120CS7 and SiC MOSFET was used for measurements. For each devices, 2 parameters were tested: V_{DS} or V_{CE} and I_{DS} or I_{CE}. The first test was done by keeping the current at 9A with the corresponding charge time(eq 2) and sweeping the voltage from 100V to 700V and the second test is done by keeping the voltage at the 400V and sweeping the current from 5A to 18A for MOSFET and 5A to 25A for IGBT. The data from the oscilloscope was saved as .csv file and data processing was done by MATLAB. The following instruments were used for the measurements:

1) Differential Probe: Micsig DP700
2) Passive Probe: 10073C
3) Current Sensor: Rogowski Coil CWT3
4) Oscilloscope
5) DC Power Supply:IT6018C-1500-40
6) TI microcontroller

D. Power Inverter Design

Power inverters are essential devices that convert DC (direct current) into AC (alternating current) power, enabling the operation of AC loads using DC sources such as batteries, photovoltaic panels, or DC power supplies. The inverter topology used in this design is a single-phase full-bridge (H-bridge) inverter, which consists of four power switches arranged in an H configuration. This topology allows the output voltage to swing both positively and negatively with respect to the load, effectively producing an AC waveform[13].

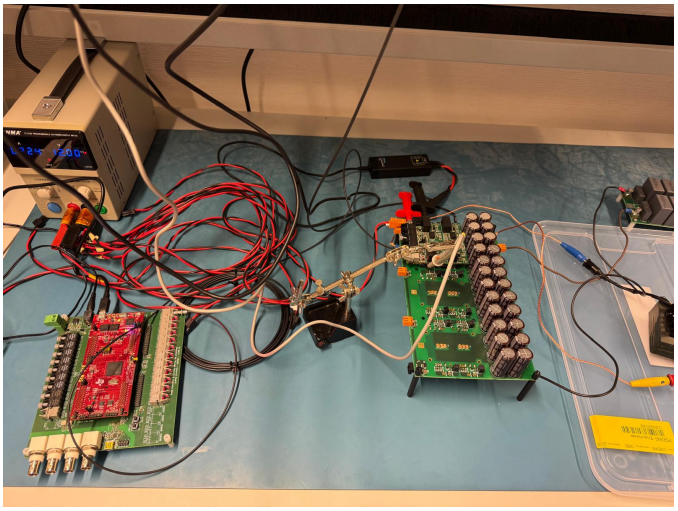

Fig. 12: Measurement Setup

The inverter is controlled using Sinusoidal Pulse Width Modulation (SPWM). A sine wave (representing the desired output frequency) is compared against a high-frequency triangular carrier wave to generate pulse-width-modulated gate signals for the MOSFETs or IGBTs [14]. The gate drive circuit shown in the simulation compares these signals using comparators and logic gates to control the switches appropriately. Two diagonal switches are turned on in a complementary way to direct current through the load alternately, creating a bipolar PWM output voltage across the load terminals. The following parameters are significant for optimizing the efficiency[14].

- **Vbus**: DC input voltage to the inverter.
- **sine_fr**: Frequency of the output sine reference.
- **PWM_fr** : Frequency of the triangular carrier for PWM.
- **DT**: Dead time to prevent shoot-through in switching legs. Dead time is the time interval between the turn-off of one switch and the turn-on of another switch in the same leg of a bridge circuit. For MOSFETs dead time is lower compared to the IGBTs. IGBTs have longer dead time due to their tail current[15].
- **M**: Modulation index; it determines the amplitude of the output voltage.
- **Rg**: Gate resistance that controls switching speed and overshoot.
- **Rload and Lload**: Resistive and inductive component of the load.
- **Von/Voff**: High and low gate voltage levels.

For a single-phase full-bridge inverter using SPWM, the RMS value of the output voltage fundamental is given by: $V_{\text{out,RMS}} = \frac{m \cdot V_{\text{DC}}}{\sqrt{2}}$ and the output power delivered to the load is:$P_{\text{out}} = \frac{V_{\text{out,RMS}}^2}{R_{\text{load}}}$.This theoretical value depends on modulation index, actual switching behavior, and filtering[14].

At the input part of the circuit, a LC low pass filter with 1.5kHz cut-off frequency was implemented to have more clear sinusoidal waveform.

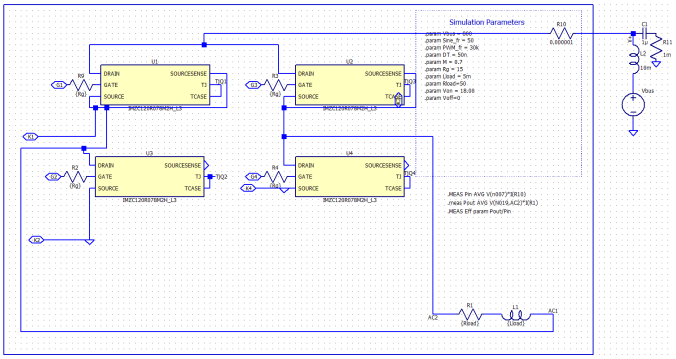

Fig. 13: Circuit Schematic of Power Inverter [16]

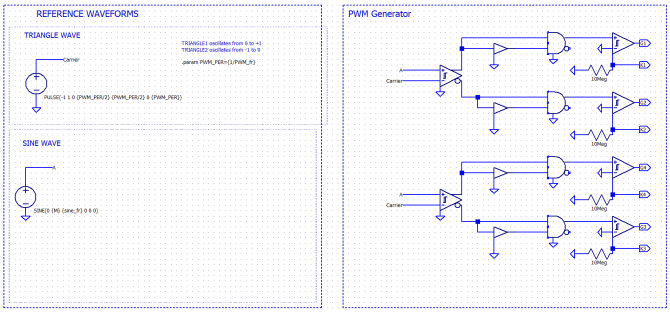

Fig. 14: Gate Driver for Power Inverter [16]

In LTspice, input and output power are measured using `.meas` commands:

```
.meas Pin AVG V(Vbus)*I(R10) FROM 10m TO 75m
.meas Pout AVG V(AC2,n019)*I(R1) FROM 10m TO 75m
.meas Eff PARAM Pout/Pin
```

The input power is the multiplication of input current and input voltage and output power is the multiplication of the current over the load resistor and voltage across the load resistor. The inverter efficiency is computed as:$\eta = \frac{P_{\text{out}}}{P_{\text{in}}}$. The expected efficiency for SiC MOSFET is $\geq 99\%$ and $\approx 97 - 98\%$ for IGBT.

III. Results and Discussion

This section presents the results of double pulse test (DPT) simulations and measurements conducted to evaluate the switching behavior of three mentioned semiconductor devices. The impact of key parameters drain-source voltage V_{DS} or V_{CE} for IGBTs, drain-source current I_{DS} or I_{CE}, gate resistance (R_G) on switching energy loss was analyzed. In order to evaluate the real life behaviour of the effects of the circuit parameters, SiC MOSFET and IGBT: IKW25N120CS7 were chosen for measurements. Based on these findings, the same 2 devices were implemented in a two-level inverter circuit to assess inverter efficiency across different switching frequencies. The device under test is the bottom device; therefore, a change in V_{DS}/V_{CE} is the same as changing the V_{DC}.

A. Simulation Results of SiC MOSFET:IMZC120R078M2

The IMZC120R078M2 SiC MOSFET was evaluated for its switching performance under varying electrical conditions. Simulations focused on how the drain-source voltage, drain-source current and gate resistance influence the turn-on and turn-off switching losses. Due to its fast switching speed and low capacitance, this device is expected to exhibit lower losses compared to IGBTs.

1) Drain-Source Voltage: Figure 15 presents the simulated switching energy as a function of drain-source voltage V_{DS} for the IMZC120R078M2H SiC MOSFET. Both E_{on} and E_{off} exhibit a increases with an increase in V_{DS}, consistent with the expectation that higher voltage levels lead to higher energy dissipation during switching transitions based on equation 4. The rise in E_{on} is significantly more than E_{off}, as the turn-on event involves a rapid increase in current with a high voltage across the device, resulting in greater overlap and thus higher energy loss. Compared to the datasheet values at 800V (indicated by stars), the simulated E_{on} aligns closely, while E_{off} is slightly underestimated. This deviation may be due to the lack of parasitic inductances and gate loop effects. Even though the main operating conditions were given in the datasheet, a slight variation in pulse duration or inductor value can affect the results.

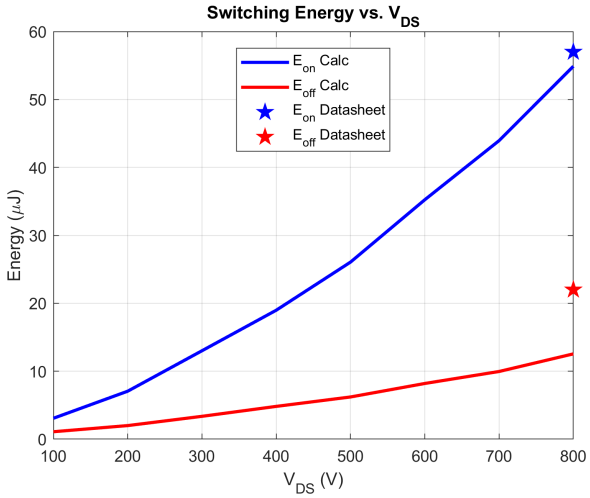

Fig. 15: Switching Loss vs Drain-Source Voltage

2) Drain-Source Current: Figure 16 illustrates the variation of turn-on and turn-off switching energies with increasing drain current. As expected, both turn on and turn off energies increase with current due to the greater charge involved during turn on and turn off event based on equation 4. The simulated results show that E_{on} rises more steeply than E_{off}, indicating higher dependence to current during turn-on transitions. When compared with datasheet values at 25°C (marked with stars), the simulation slightly underestimates both losses, which is due to the idealized switching conditions. Additionally, datasheet curves at 175°C highlight the strong temperature dependence of switching losses, especially for E_{on}. These results validate the simulated trend and emphasize the importance of thermal effects in real applications. However, the simulated component model was not dependent on temperature and therefore, the effects of temperature could not be simulated.

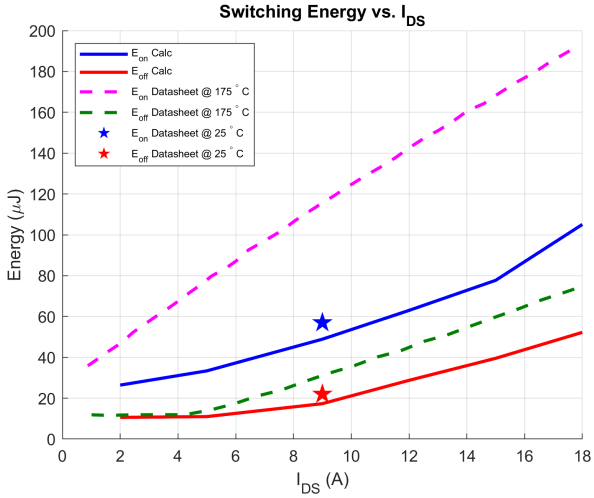

Fig. 16: Switching Loss vs Drain-Source Current

3) Gate Resistance: The Figure 17 demonstrates the voltage and current waveforms with 4 different gate resistor values and Figure 18 presents the dependence of switching energy on gate resistance R_G for the same SiC MOSFET. Both E_{on} and E_{off} increase approximately linearly with R_G, due to slower switching transitions that result in longer energy dissipation intervals. This trend is consistent with the expected trade-off between switching speed and loss. When compared to datasheet values at 25°C and 175°C, the simulated E_{on} and E_{off} follow the same general behavior but remain lower in magnitude, again due to idealized conditions that ignore parasitic inductance, device capacitance variation, and high-temperature effects. The Figure 18 demonstrates that gate resistance tuning has a direct and significant impact on switching efficiency, highlighting its importance in gate driver circuit design optimization.

B. Simulations of IGBT:IKW25N120CS7

1) Collector-Emitter Voltage: Figure 19 presents the dependency of switching energy on the applied collector-emitter voltage. Both E_{on} and E_{off} increase with V_{CE}, reflecting the higher energy processed during switching events at higher voltages. The simulated results rise steeply, especially for E_{on}, and match closely with datasheet points at $25°C$. Datasheet curves at 175°C continue to show higher energy levels across all voltages. This figure confirms that switching loss gets larger with voltage.

2) Collector-Emitter Current: Figure 20 shows how the turn-on E_{on} and E_{off} switching energies vary with collector current for the IKW25N120CS7 IGBT. As expected, both energies increase with higher current, due to greater charge flow and voltage–current overlap during switching transitions.

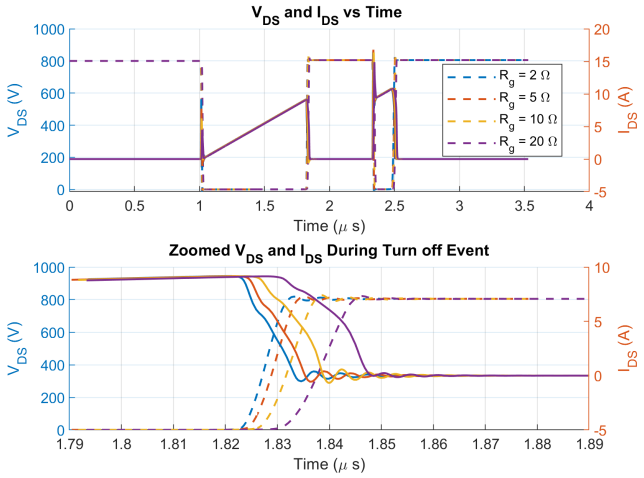

Fig. 17: SiC MOSFET with different R_G

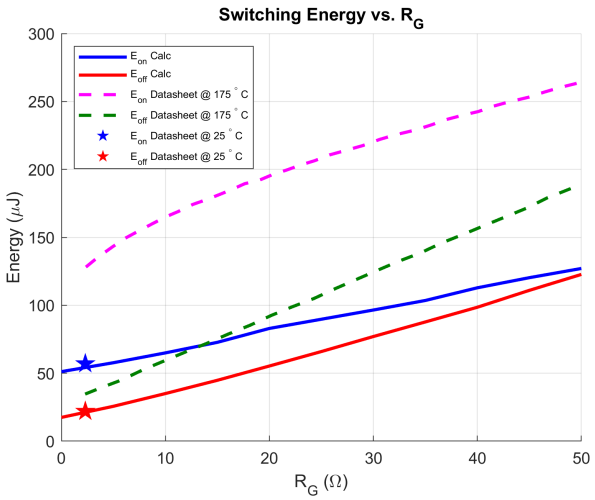

Fig. 18: Switching Loss vs Gate Resistance

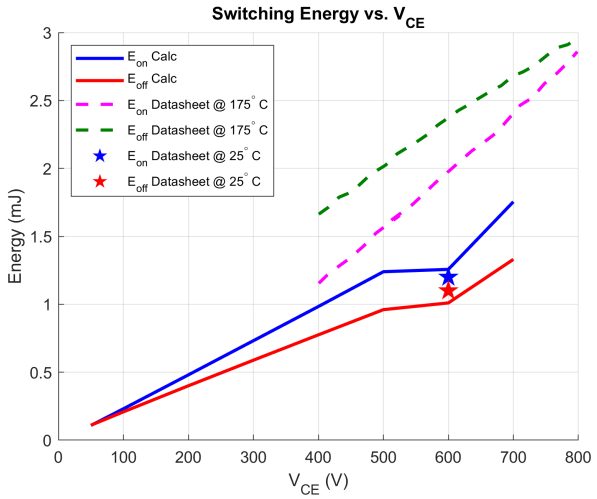

Fig. 19: Switching Loss vs Collector-Emitter Voltage

The calculated values follow a consistent increase and match well with the datasheet values at $25°C$. In contrast, the datasheet curves at $175°C$ demonstrate significantly higher switching losses, highlighting the thermal sensitivity of the IGBT.

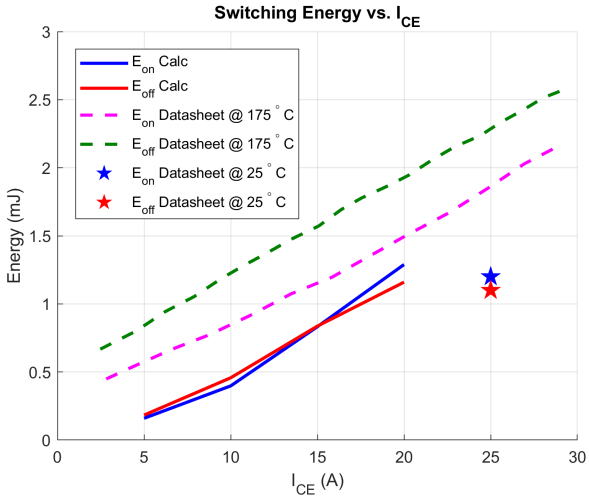

Fig. 20: Switching Loss vs Load Current

3) Gate Resistance: Figure 22 illustrates the effect of gate resistance on the switching energy and Figure 21 demonstrates the collector-emitter voltage and current with different gate resistor values. Increasing R_G slows down the gate charging and discharging process, leading to longer switching intervals and consequently higher energy loss. Both E_{on} and E_{off} exhibit nearly linear increases across the tested resistance range. The calculated results are compared to datasheet curves at $175°C$, which again show higher losses due to higher junction temperatures. This plot highlights the importance of careful gate resistance selection to balance switching speed and energy efficiency in IGBT-based converters.

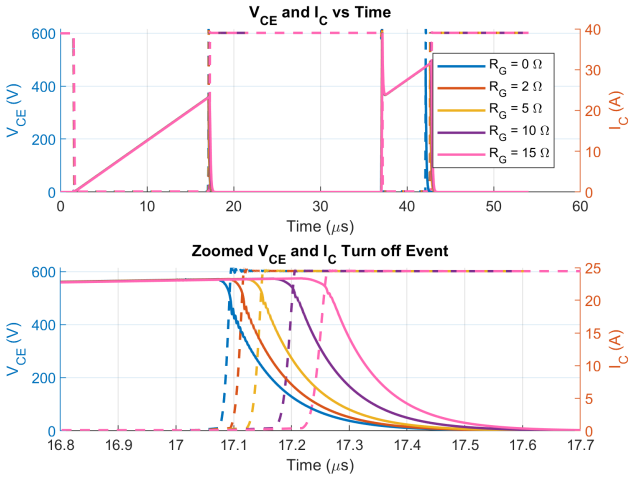

Fig. 21: IKW25N120CS7 with different R_G

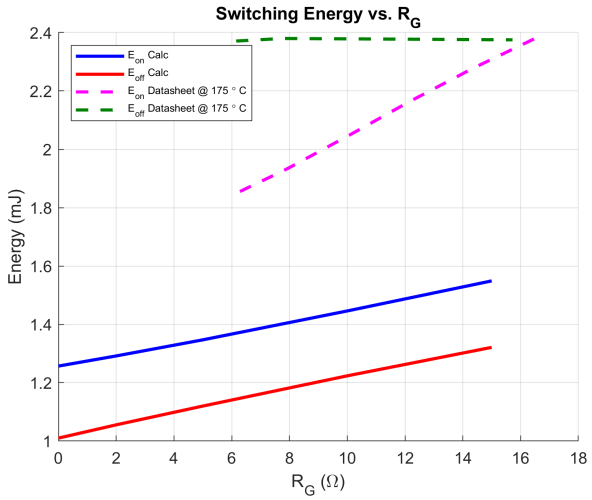

Fig. 22: Switching Loss vs Gate Resistance

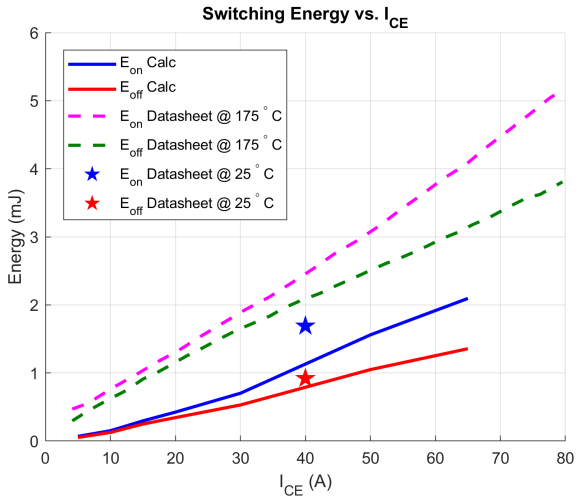

Fig. 24: Switching Loss vs Load Current

C. Simulations of IGBT:IKW40N120CH7

1) Collector-Emitter Voltage: Figure 23 presents the dependence of switching energy on the applied collector-emitter voltage. Both of the IGBTs demonstrate the similar trend based on Figure 19 and 23. However, the switching loss energy is lower for IGBT: IKW25N120CS7. Although E_{on} and E_{off} are less than the datasheet values, E_{on} and E_{off} both rise with V_{CE}.

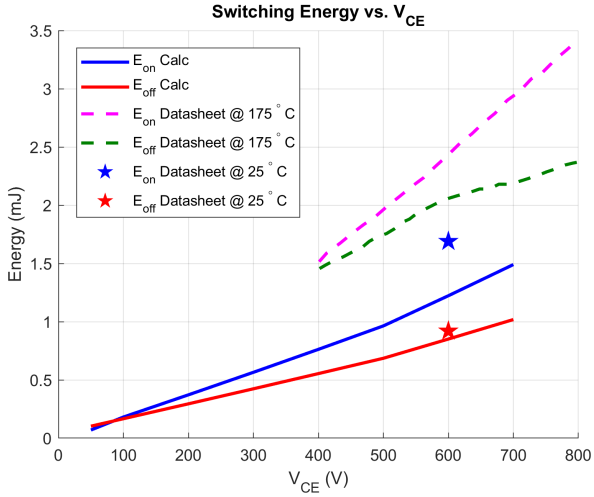

Fig. 23: Switching Loss vs Collector-Emitter Voltage

2) Collector-Emitter Current: Figure 24 shows the relationship between collector-emitter current and switching loss. As current increases, both E_{on} and E_{off} rise significantly and the difference between E_{on} and E_{off} increases. The datasheet curves at $175°C$, and markers at $25°C$, again demonstrates the dependence on the temperature.

3) Gate Resistance: The Figure 25 shows the waveform of collector-emitter voltage and current with different gate resistor values and Figure 26 illustrates how the switching energy of the IKW40N120CH7 IGBT varies with gate resistance. As R_G increases, both E_{on} and E_{off} increase linearly due to slower gate drive, which causes longer switching transitions and an increase in energy loss. The calculated results are plotted alongside datasheet curves at $175°C$, which show consistently higher values due to higher junction temperature.

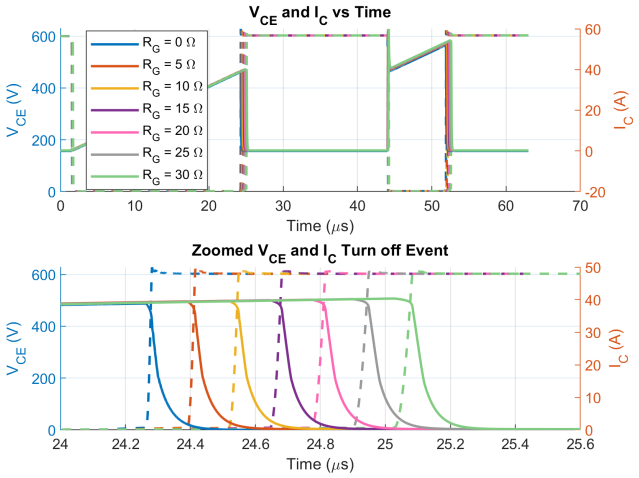

Fig. 25: IKW40N120CH7 with different R_G

D. Measurements

For the SiC MOSFET, Figure 27 demonstrates the switching energy vs drain-source voltage (V_{DS}). The data shows a nearly linear increase in energy up to 500 V, but slight non-monotonic behavior is due to the inaccuracies in the measurements.

For the SiC MOSFET, the Figure 28 shows the E_{on} and E_{off} dependence on drain-source current (I_{DS}). The increase in switching energy is less sharper compared to the IGBT, which is expected due to the faster switching capability.

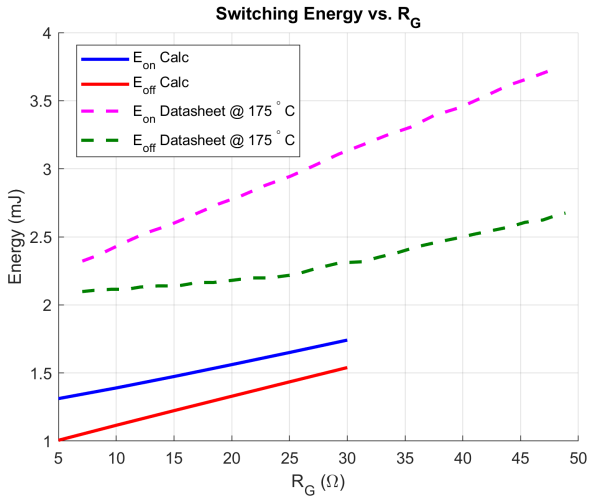

Fig. 26: Switching Loss vs Gate Resistance

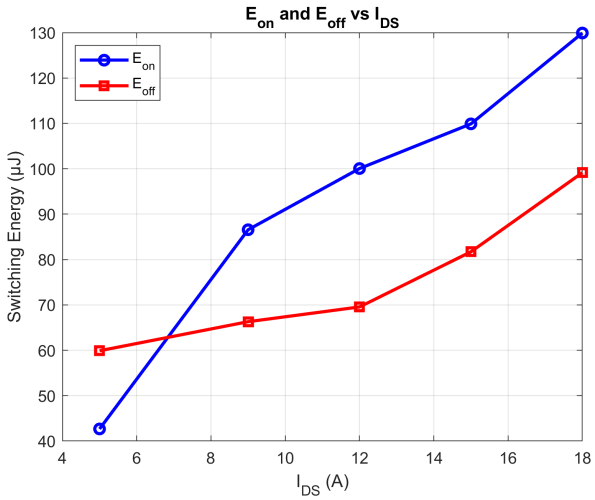

Fig. 28: Switching Loss vs Drain-Source Current(Measurements)

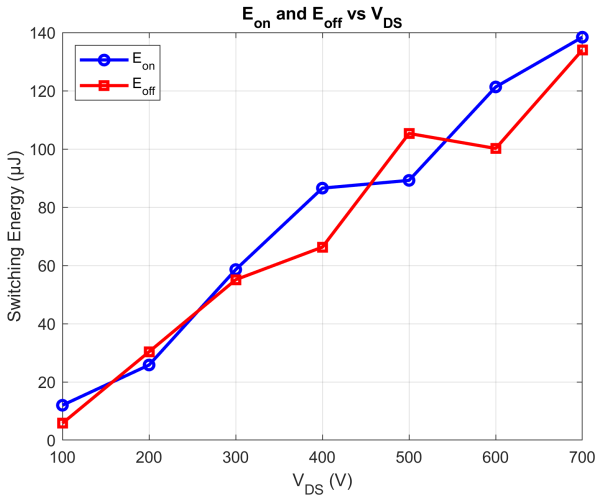

Fig. 27: Switching Loss vs Drain-Source Voltage(Measurements)

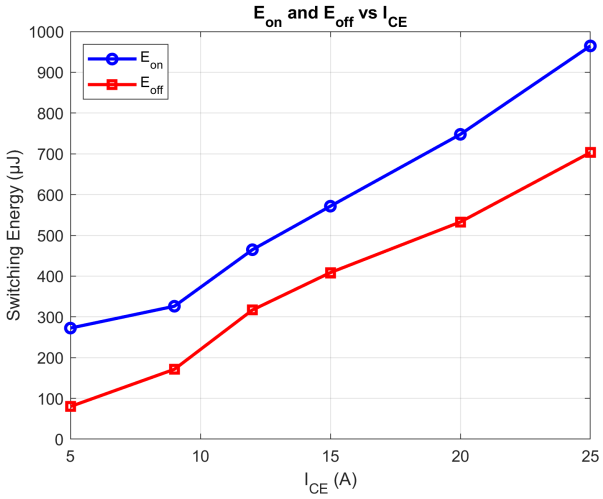

Fig. 29: Switching Loss vs Collector-Emitter Current(Measurements)

The Figure 29, shows E_{on} and E_{off} vs collector-emitter current (I_{CE}) for the IGBT, and it shows a clear linear increase in energy with current. This trend arises because higher current levels store and discharge more energy in the parasitic inductances and device capacitances during switching. E_{on} increases more than E_{off}, indicating higher sensitivity of turn-on events due to the tail current of IGBT and slower transients.

The Figure 30 demonstrates that variation in E_{on} and E_{off} according to difference in V_{CE}. E_{on} dominates and increases steeply, while E_{off} increases progressively. This voltage dependence is expected, as energy losses are proportional to both voltage and current during the switching transitions.

The Figure 31 represent the differences of switching energy between the SiC MOSFET and Si IGBT. The measurements were done with 9A current and a voltage sweep from 100V to 700V. There is a clear difference between turn on and turn off energy of the IGBT and it can be seen that as the voltage increases the gap between the E_{on} and E_{off} as the values increase. On the other hand, the same trend but in lower switching loss values than IGBT is expected with the SiC MOSFET. While the measurements result in lower switching loss for both E_{on} and E_{off} than IGBT, the gap is lower than expected. At 500V, the E_{off} is larger than E_{on} and that is contradictory to all the simulations and datasheet [7]. The ringing caused inaccuracies in the measurement of MOSFET and the ringing caused by current sensor can be seen from the Figures 34,35 and 36. The ringing is increased as the drain-source voltage increased. At 400V, E_{on} of IGBT is 7.42 times higher than SiC MOSFET and E_{off} of IGBT is 7.09 times higher than E_{off} os SiC MOSFET.

The Figure 32 shows the variations of switching energy with the change in drain-source/collector-emitter current at

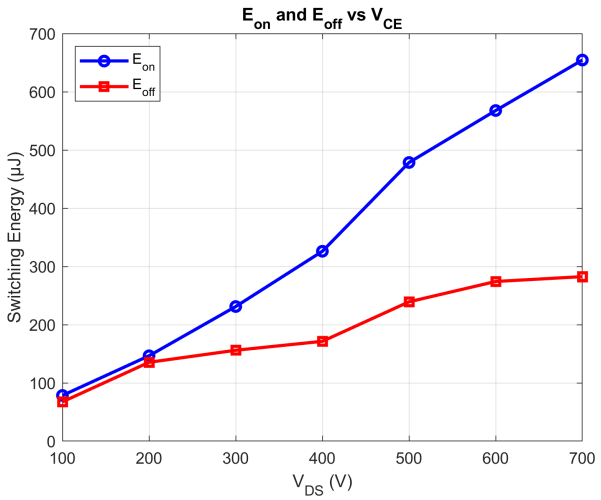

Fig. 30: Switching Loss vs Collector-Emitter Voltage(Measurements)

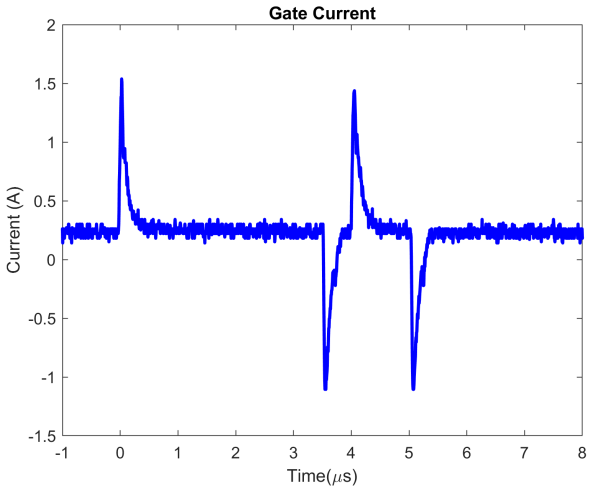

Fig. 33: Measured Gate Charge

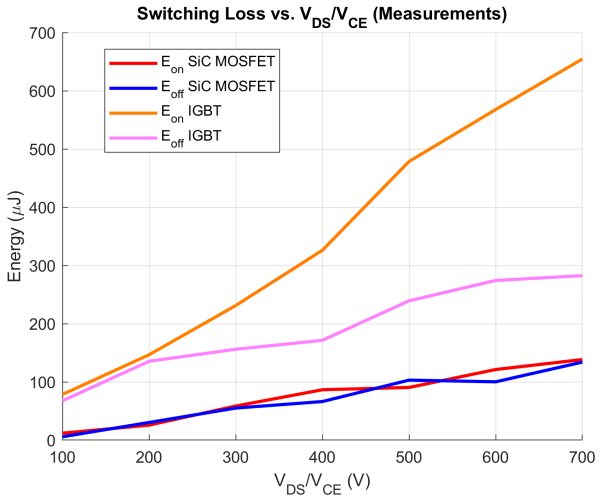

Fig. 31: Switching Loss vs V_{DS}/V_{CE}(Measurements)

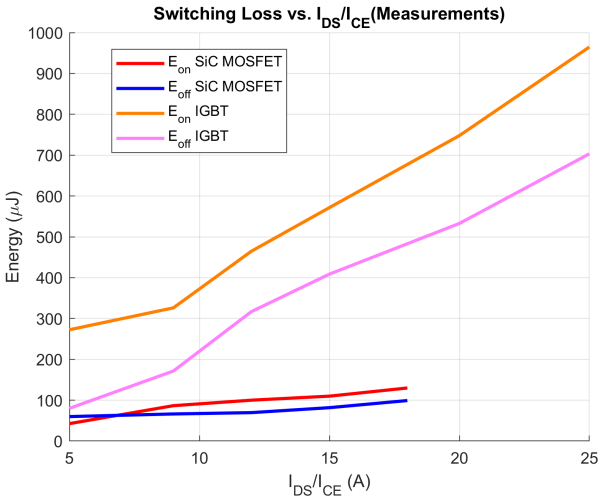

Fig. 32: Switching Loss vs I_{DS}/I_{CE}(Measurements)

400V for both of the devices. In order to operate safely, the maximum measured current for SiC MOSFET is 18A and 25A for IGBT. As the current increase, turn on and turn off energy increases for both of the devices. The switching energy of IGBT is always higher than the SiC MOSFET in this current range. At 15A, E_{on} of IGBT is 5.2 times higher than SiC MOSFET and E_{off} of IGBT is approximately 5 times higher than the SiC MOSFET.

The data processing for the measurements were based on the turn on and turn off window as a whole instead of 10% or 90% which is common in manufactured datasheet.

This measurement setup is highly sensitive to measurement instruments and parasitics. While SiC MOSFET was being measured, the current sensor started picking up the noise in the lab which eventually caused ringing before the charging started and the ringing contributed to the further values. The parasitics in the lab also have an effect on the measurements and therefore on the results. This problem was somewhat reduced with the IGBT, though, and because of slower transients and tail current, the off-charge period had to be extended. The Figures 34,35 and 36 show the waveforms from the measurements of the SiC MOSFET. Based on the figures, we can conclude that as voltage increases the ringing is increases and due to increase in the ringing, and therefore E_{on} and E_{off} calculations might result in slight inaccuracies.

Another significant limitation is the gate charge current from Figure 33. This gate charge current is approximately 1.5 A and contributes to the current during switching transients. Therefore, during switching transients, the drain-source or collector-emitter current is slightly higher than their desired values. This gate charge current is one of the reasons for the inaccuracies in the measurement setup and results.

The Figure 37,38 and 39 show the same measurement with IGBT. The ringing is significantly lower, however the switching times are visibly slower which effects the turn on and turn off energy.

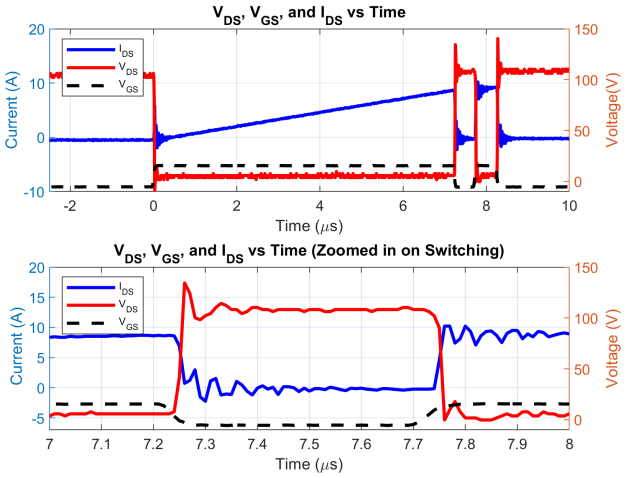

Fig. 34: Measurement of SiC MOSFET:100V-9A

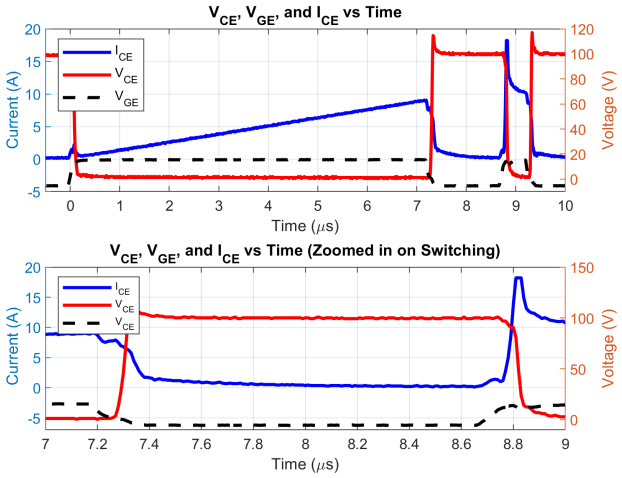

Fig. 37: Measurement of IGBT:100V-9A

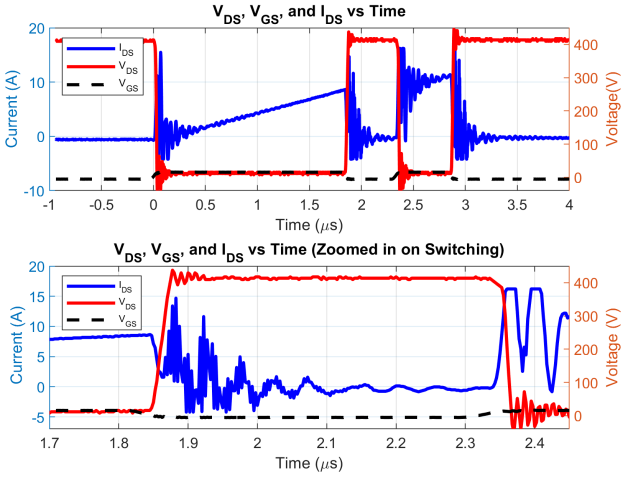

Fig. 35: Measurement of SiC MOSFET:400V-9A

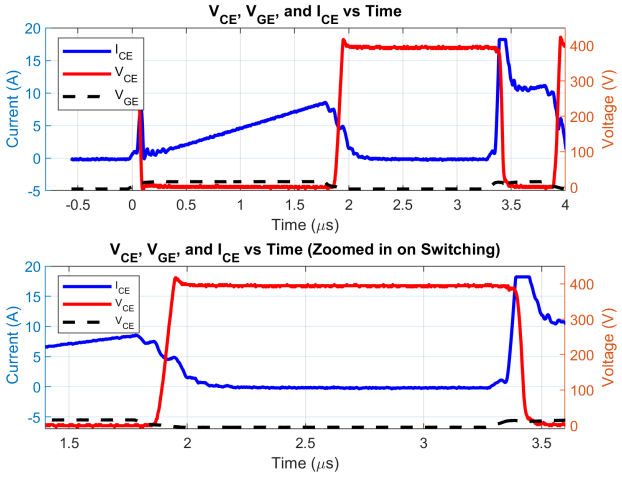

Fig. 38: Measurement of IGBT:400V-9A

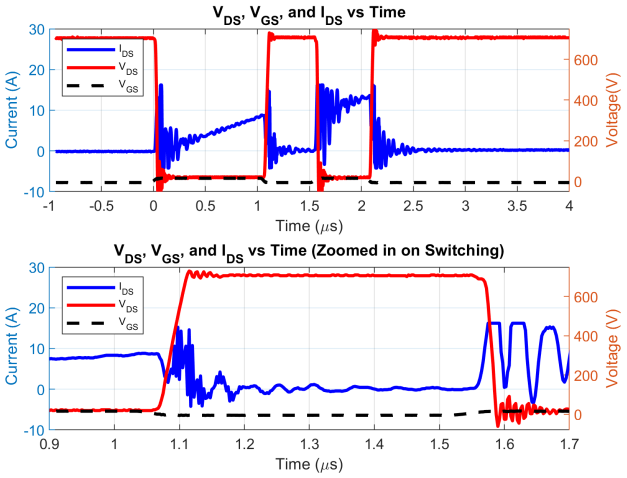

Fig. 36: Measurement of SiC MOSFET:700V-9A

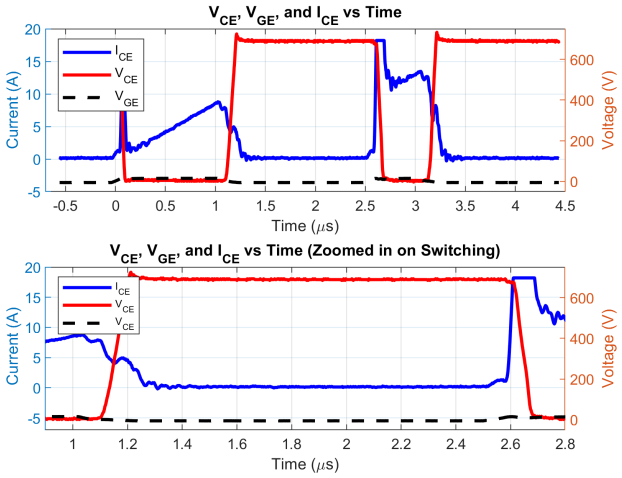

Fig. 39: Measurement of IGBT:700V-9A

E. Power Inverter Efficiency

Figure 40 presents the input and output power of the power inverter, while Figure 41 depicts the corresponding input and output voltage and current waveforms. The simulations were performed using the following parameter settings:

1) `Vbus = 800`
2) $Sine_{fr} = 50$
3) $PWM_{fr} = 30k$
4) `DT = 50n`
5) `M = 0.7`
6) `Rg = 15`
7) `Lload = 5m`
8) `Rload = 50`
9) `Von = 18.00`
10) `Voff = 0`

The selected dead time of 50ns is appropriate for SiC MOSFET operation, given their fast switching capability. For simulations involving IGBTs, all parameters were maintained identical, except for the dead time. Due to the inherently slower switching characteristics of IGBTs, the dead time was increased to $1\mu s$ to ensure safe operation and avoid cross-conduction. Figure 42 illustrates the efficiency variation of the SiC MOSFET and Si IGBT with respect to the switching frequency. As the switching frequency increases from 5 kHz to 30 kHz, the efficiency of both devices decreases; however, the rate of decline differs significantly. SiC MOSFETs maintain a consistently higher efficiency, beginning above 99.5% and dropping slightly to around 99.25%, highlighting the higher performance in high-frequency operations. In contrast, the efficiency of Si IGBT starts at approximately 99.2% and decreases more sharply, reaching around 97.3% at 30 kHz. This difference can be explained by the SiC MOSFETs' lower switching losses and faster transition capabilities compared to IGBT's higher losses and tail current characteristics. MOSFET and IGBT have very close efficiency as in lower frequencies; however, as the frequency increases efficiency of IGBT nearly decreases linearly. Consequently, SiC devices are more suitable for applications requiring high switching frequencies and maximum energy efficiency.

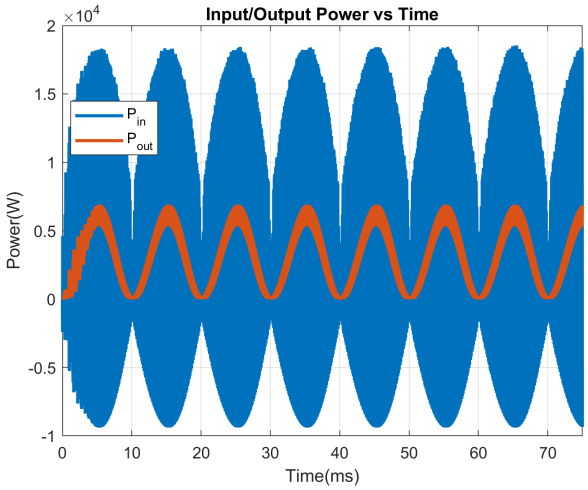

Fig. 40: Input/Output Power of the Inverter

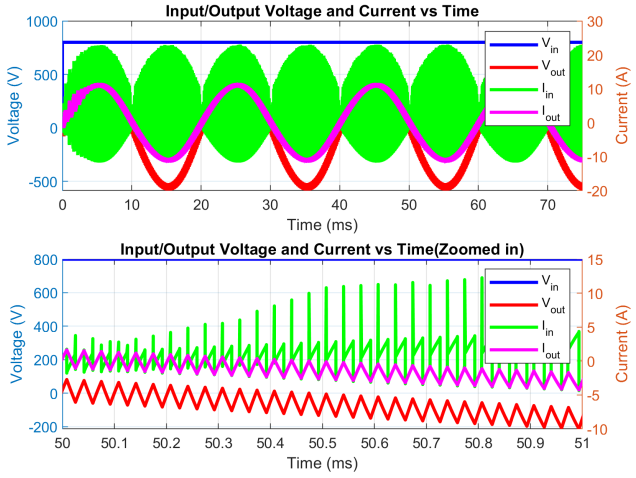

Fig. 41: Input/Output Voltage and Current of the Inverter

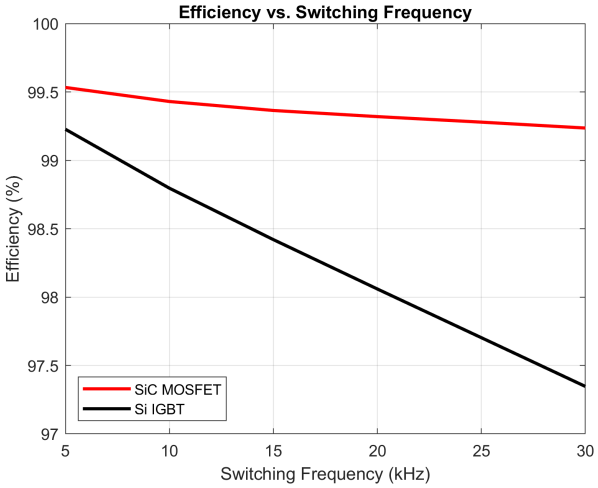

Fig. 42: SiC MOSFET vs IGBT Efficiency

IV. Conclusion

This thesis presents a comprehensive study of switching loss characterization in wide bandgap (WBG) semiconductor devices such as SiC MOSFET. Comparision was done between a SiC MOSFET(IMZC120R078M2H) and 2 Si IGBTs. Using the Double Pulse Test (DPT), dynamic behaviors were analyzed in both simulation and experimental verification to quantify the effects of drain-source/collector-emitter voltage, drain-source/collector-emitter current and gate resistance on turn-on and turn-off energies.The findings demonstrate that SiC device consistently exhibit superior performance with significantly lower switching losses compared to its Si IGBT counterparts, a trend observed consistently across both simulated and measured results. While addressing practical measurement challenges such as ringing, layout-induced

parasitics, and sensor limitations through robust MATLAB post-processing, the thesis provides valuable insights into the real-world behavior of these devices.

The thesis further extended to inverter-level analysis with sinusoidal pulse width modulation controlled H-Bridge inverter. The SiC MOSFET inverter maintained efficiencies above 99%, whereas the IGBT-based inverter exhibited a sharper decline with frequency, underlining the practical benefits of WBG technology in high-frequency operations [2], [14].

Ultimately, this research highlights that accurate characterization of switching losses is significant for device selection and the optimized design of next-generation power inverters. The insights gained contribute significantly to the ongoing development of more compact, energy-efficient, and reliable power electronics for a wide array of applications, including electric vehicles and renewable energy systems. Future work could focus on developing temperature-dependent device models, exploring advanced control strategies for inverter optimization, and investigating the long-term reliability of WBG devices under diverse operating conditions.

V. AI Statement

Artificial Intelligence (AI) tools, specifically OpenAI's ChatGPT 4o, were utilized during the preparation of this thesis to enhance the clarity, grammar, punctuation, and coherence of the written content. All technical analyses, experimental results, and conclusions presented in the thesis are the original work of the author. The MATLAB code and comments was written with the help of ChatGPT 4o as well.

References

[1] F. Wang, Z. Zhang, and E. A. Jones, *Characterization of Wide Bandgap Power Semiconductor Devices*. The Institution of Engineering and Technology, 2018, ISBN: 978-1-78561-491-0.

[2] Z. Zhang, B. Guo, F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9307–9319, 2017.

[3] A. Nobile. "Wide-bandgap (wbg) semiconductors." Accessed: June 2025. (2023), [Online]. Available: https://www.powerelectronicsnews.com/wide-bandgap-wbg-semiconductors/.

[4] M. Beheshti, "Wide-bandgap semiconductors: Performance and benefits of gan versus sic," Texas Instruments, Application Report SLYT801, 2020, Accessed: June 2025. [Online]. Available: https://www.ti.com/lit/an/slyt801/slyt801.pdf.

[5] R. bibinitperiod Schwarz, *Double pulse testing*, https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_application/application_notes/gfm347/GFM347_1e_Double_Pulse_Testing.pdf, Accessed: 2025-06-27, 2020.

[6] T. Instruments. "Tutorial: Performing double pulse test simulations for silicon carbide designs with ltspice." Accessed: 2025-06-20, Texas Instruments. (2020), [Online]. Available: https://www.youtube.com/watch?v=Gcrsmg4r2mU.

[7] Infineon Technologies AG, *Imzc120r078m2h datasheet*, https://www.infineon.com/dgdl/Infineon-IMZC120R078M2H-DataSheet-v01_10-EN.pdf, Revision 1.1, November 2021, 2021.

[8] Infineon Technologies AG, *Ikw25n120cs7 datasheet*, https://www.infineon.com/dgdl/Infineon-IKW25N120CS7-DS-v02_00-EN.pdf, Revision 2.0, November 2021, 2021.

[9] Infineon Technologies AG, *Ikw40n120ch7 datasheet*, https://www.infineon.com/dgdl/Infineon-IKW40N120CH7-DataSheet-v01_00-EN.pdf, Revision 1.0, April 2020, 2020.

[10] Texas Instruments, *Designing gate drive circuits for high-speed switching*, https://www.ti.com/lit/ml/slua618a/slua618a.pdf, Application Report SLUA618A, 2010.

[11] ROHM Semiconductor, *Gate drive circuit design guidelines for sic mosfets*, https://fscdn.rohm.com/en/products/databook/applinote/discrete/sic/mosfet/gate_drive_circuit-design_guidelines_an-e.pdf, Application Note, Document No. REH0501E, 2021.

[12] GTAKE. "What is igbt? igbt working principle." Accessed: June 2025. (2024), [Online]. Available: https://www.gtake.com/industry-news/what-is-igbt-igbt-working-principle/.

[13] G. Di Maria. "Power electronics course: Part 10 – the single-phase full-bridge inverter." Accessed: 2025-06-19. (2023), [Online]. Available: https://www.powerelectronicsnews.com/power-electronics-course-part-10-the-single-phase-full-bridge-inverter/.

[14] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 2nd. New York: John Wiley & Sons, 1995.

[15] Y. Zhang and J. Wang, *Understanding dead-time based on tps51225/275/285*, https://www.ti.com/lit/an/slua919/slua919.pdf, Application Report SLUA919, Texas Instruments, 2018.

[16] Texas Instruments, *Tutorial: Performing double pulse test simulations for silicon carbide designs with ltspice*, https://www.youtube.com/watch?v=Gcrsmg4r2mU, Accessed: 2025-06-22, 2022.

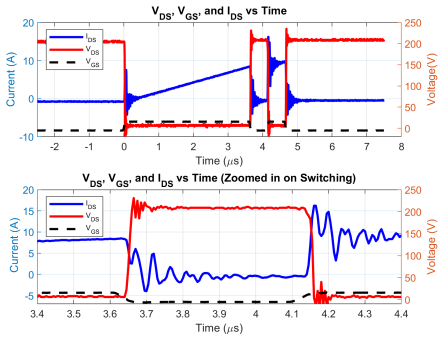

Fig. 44: Measurement of SiC MOSFET:200V-9A

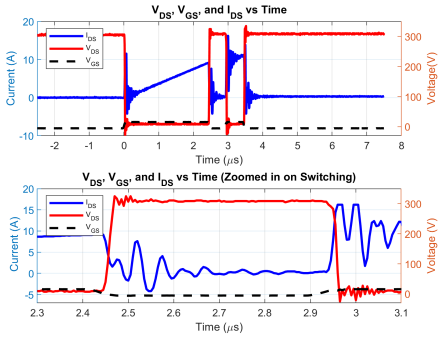

Fig. 45: Measurement of SiC MOSFET:300V-9A

VI. Appendix A

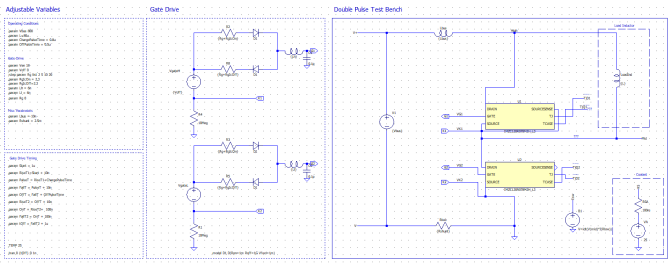

Fig. 43: Simulation Setup for SiC MOSFET

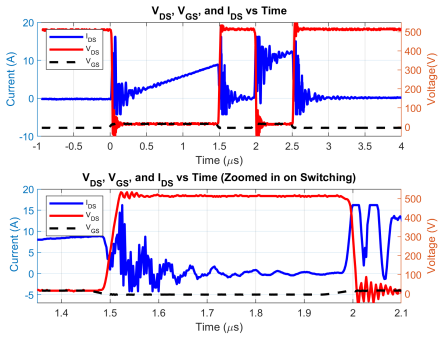

Fig. 46: Measurement of SiC MOSFET:500V-9A

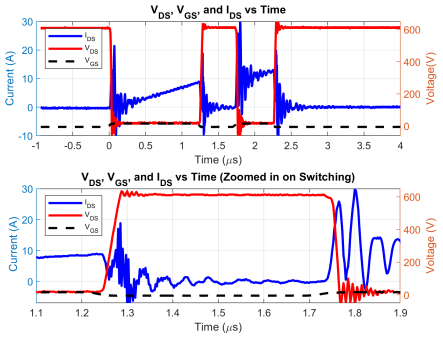

Fig. 47: Measurement of SiC MOSFET:600V-9A

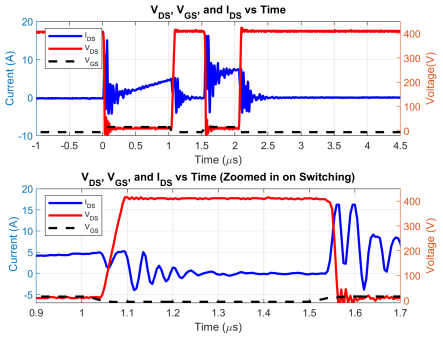

Fig. 48: Measurement of SiC MOSFET:400V-5A

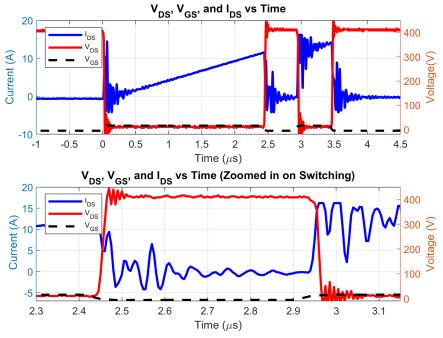

Fig. 49: Measurement of SiC MOSFET:400V-12A

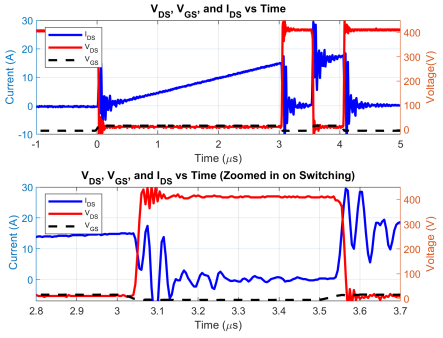

Fig. 50: Measurement of SiC MOSFET:400V-15A

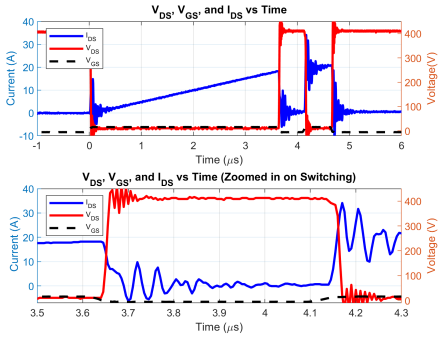

Fig. 51: Measurement of SiC MOSFET:400V-18A

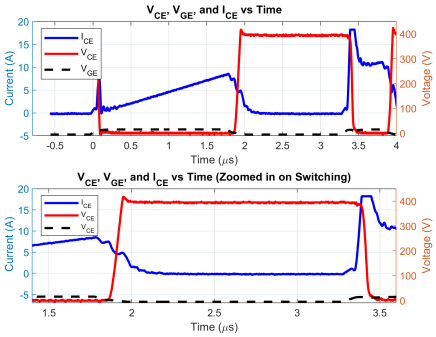

Fig. 55: Measurement of IGBT:400V-9A

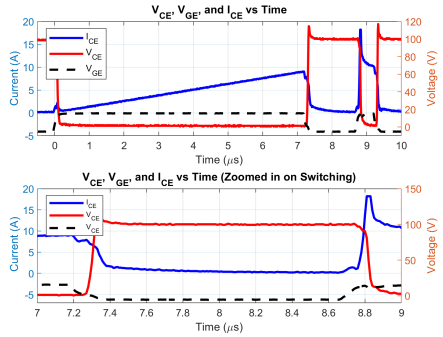

Fig. 52: Measurement of IGBT:100V-9A

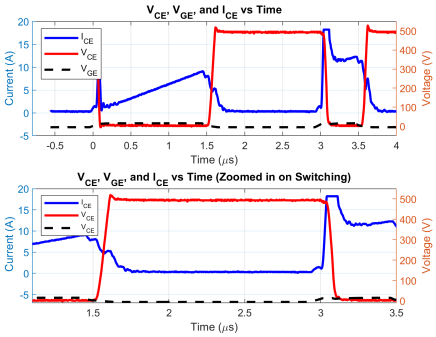

Fig. 56: Measurement of IGBT:500V-9A

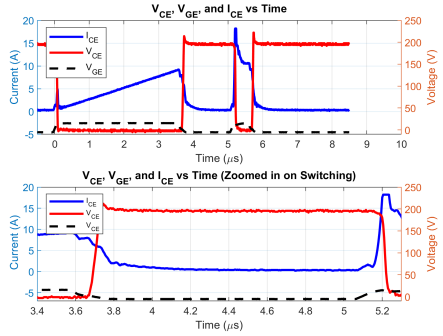

Fig. 53: Measurement of IGBT:200V-9A

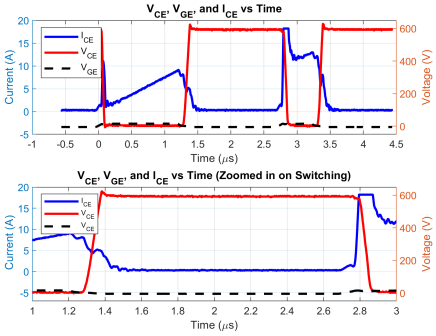

Fig. 57: Measurement of IGBT:600V-9A

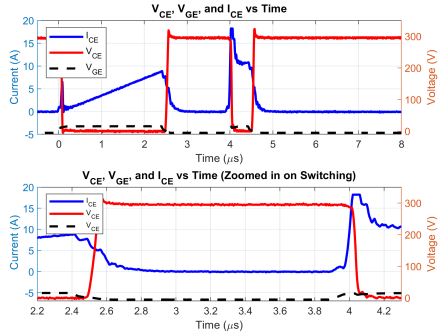

Fig. 54: Measurement of IGBT:300V-9A

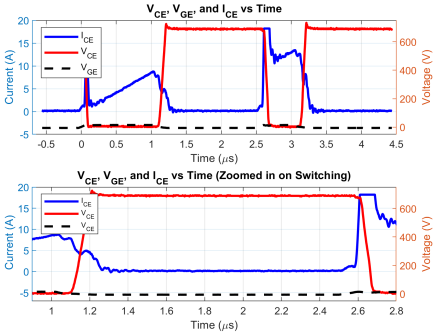

Fig. 58: Measurement of IGBT:700V-9A

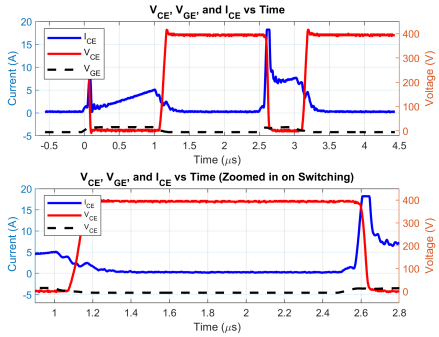

Fig. 59: Measurement of IGBT:400V-5A

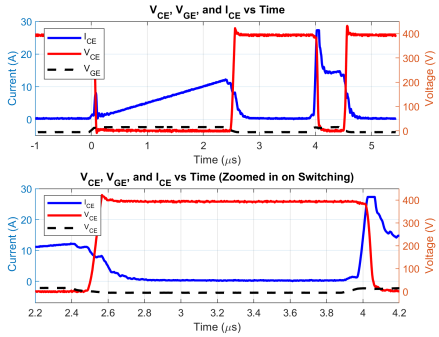

Fig. 60: Measurement of IGBT:400V-12A

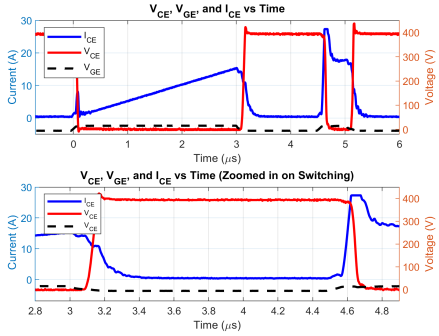

Fig. 61: Measurement of IGBT:400V-15A

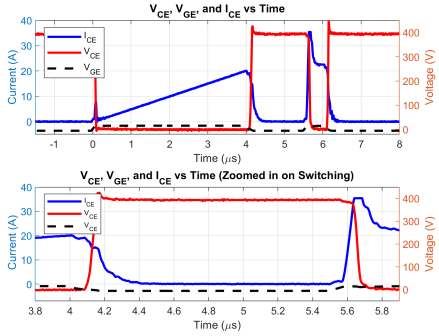

Fig. 62: Measurement of IGBT:400V-20A

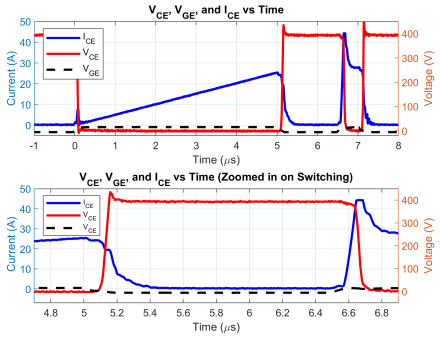

Fig. 63: Measurement of IGBT:400V-25A

VII. Appendix B

```
%Switching Loss Calculations for IKW25N120CS7 with standard operating conditions, can used for
other cases and devices with change in parameters

data = readmatrix('DPT_Test_Stand_HB_IGBT_IKW25N120CS7_600V.txt');

% Extract relevant waveforms from columns
time = data(:, 1);          %time
behavioral_vs = data(:, 2);  % Behavioral voltage signal (used for sanity check)
Vge = data(:, 3);            % Gate-emitter voltage
Vce = data(:, 4);            % Collector-emitter voltage
Ic = data(:, 5);             % Collector current

% --- SET THRESHOLD VALUES FOR DETECTION ---
V_gate = 15;
V_ce = 600;
I_collector = 25;

V_gate_10 = 0.1 * V_gate;    % 10% of gate voltage (used for turn-on detection)
V_gate_90 = 0.9 * V_gate;    % 90% of gate voltage (used for turn-off detection)
I_collector_2 = 0.02 * I_collector; % 2% of current (for detecting end of turn-off)
V_ce_2 = 0.02 * V_ce;        % 2% of Vce (for detecting end of turn-on)

% --- DEFINE ENERGY CALCULATION WINDOWS ---
t_min_energy_1st = 15.8e-6;   % Turn-off energy window start (s)
t_max_energy_1st = 18e-6;     % Turn-off energy window end

t_min_energy_2nd = 36.5e-6;   % Turn-on energy window start (s)
t_max_energy_2nd = 38e-6;     % Turn-on energy window end

% Get indices of samples inside each energy window
window_energy_1st = find(time >= t_min_energy_1st & time <= t_max_energy_1st);
window_energy_2nd = find(time >= t_min_energy_2nd & time <= t_max_energy_2nd);

% --- EXTRACT DATA FROM TURN-OFF WINDOW ---
Vge_window = Vge(window_energy_1st);
time_window = time(window_energy_1st);
Vce_window = Vce(window_energy_1st);
current_window = Ic(window_energy_1st);

% Find last index where Vge crosses 90%-used for turn-off timing
idx_Vge_90_local = find(Vge_window >= V_gate_90, 1, 'last');

if ~isempty(idx_Vge_90_local)
    idx_Vge_90_global = window_energy_1st(idx_Vge_90_local);
    time_Vge_90 = time(idx_Vge_90_global);
    Vce_at_time_Vge_90 = Vce(idx_Vge_90_global);
    fprintf('Time when VGE = 90%% of %.1f V: %.10f s\n', V_gate, time_Vge_90);
    fprintf('VCE at that time: %.10f V\n', Vce_at_time_Vge_90);
end

% Find last index where Ic reaches 2%-defines end of turn-off
idx_Id_2percent_local = find(current_window >= I_collector_2, 1, 'last');

if ~isempty(idx_Id_2percent_local)
    idx_Id_2percent_global = window_energy_1st(idx_Id_2percent_local);
    time_Id_2percent = time(idx_Id_2percent_global);
    fprintf('Time when Id = 2%% of max in window: %.10f s\n', time_Id_2percent);
end

% --- CALCULATE TURN-OFF ENERGY (Eoff) ---
if exist('idx_Vge_90_global', 'var') && exist('idx_Id_2percent_global', 'var')
    idx_start = min(idx_Vge_90_global, idx_Id_2percent_global);
    idx_end   = max(idx_Vge_90_global, idx_Id_2percent_global);
```

```
    if idx_end > idx_start && idx_end <= length(time)
        try
            t_range = time(idx_start:idx_end);
            v_range = Vce(idx_start:idx_end);
            i_range = Ic(idx_start:idx_end);
            assert(isequal(size(t_range), size(v_range), size(i_range)), 'Size mismatch!');
            E_off = trapz(t_range, v_range .* i_range);  % Numerical integration
            fprintf('Turn-off energy E_off: %.5f mJ\n', E_off * 1e3);
        catch ME
            disp('ERROR during integration:');
            disp(getReport(ME));
        end
    end
end

% --- TURN-ON ENERGY CALCULATION (Eon) ---

% Extract second window data
Vge_window_2 = Vge(window_energy_2nd);
time_window_2 = time(window_energy_2nd);
Vce_window_2 = Vce(window_energy_2nd);
Ic_window_2 = Ic(window_energy_2nd);

% Find first time when Vge exceeds 10%-start of turn-on
idx_Vge_10_local = find(Vge_window_2 >= V_gate_10, 1, 'first');

if ~isempty(idx_Vge_10_local)
    idx_Vge_10_global = window_energy_2nd(idx_Vge_10_local);
    time_Vge_10 = time(idx_Vge_10_global);
    Ic_at_time_Vge_10 = Ic(idx_Vge_10_global);
    fprintf('Time when VGE = 10%% of %.1f V: %.15f s\n', V_gate, time_Vge_10);
    fprintf('IC at that time: %.3f A\n', Ic_at_time_Vge_10);
end

% Find first time when Vce drops below 2%-end of turn-on
idx_Vce_2percent_local = find(Vce_window_2 <= V_ce_2, 1, 'first');

if ~isempty(idx_Vce_2percent_local)
    idx_Vce_2percent_global = window_energy_2nd(idx_Vce_2percent_local);
    time_Vce_2percent = time(idx_Vce_2percent_global);
    fprintf('Time when VCE = 2%% of max: %.10f s\n', time_Vce_2percent);
end

% --- COMPUTE TURN-ON ENERGY (Eon) ---
if exist('idx_Vge_10_global', 'var') && exist('idx_Vce_2percent_global', 'var')
    idx_start_on = min(idx_Vge_10_global, idx_Vce_2percent_global);
    idx_end_on   = max(idx_Vge_10_global, idx_Vce_2percent_global);

    if idx_end_on > idx_start_on && idx_end_on <= length(time)
        try
            t_range_on = time(idx_start_on:idx_end_on);
            v_range_on = Vce(idx_start_on:idx_end_on);
            i_range_on = Ic(idx_start_on:idx_end_on);
            assert(isequal(size(t_range_on), size(v_range_on), size(i_range_on)), 'Size mismatch!');
            E_on = trapz(t_range_on, v_range_on .* i_range_on);
            fprintf('Turn-on energy E_on: %.5f mJ\n', E_on * 1e3);
        catch ME
            disp('ERROR during Eon integration:');
            disp(getReport(ME));
        end
    else
        warning('Invalid index bounds for Eon integration.');
    end
end

% --- CHECK BEHAVIORAL VS DROP (SANITY CHECK) ---
```

```
% Behavioral voltage drop during turn-off window
vs_window_1 = behavioral_vs(window_energy_1st);
vs_max_1 = max(vs_window_1);
vs_min_1 = min(vs_window_1);
vs_diff_1 = vs_max_1 - vs_min_1;

fprintf('\nBehavioral VS in turn-off window:\n');
fprintf('Max: %.15f \n', vs_max_1);
fprintf('Min: %.15f \n', vs_min_1);
fprintf('Difference: %.20f mJ\n', vs_diff_1 * 1e3);

% Behavioral voltage drop during turn-on window
vs_window_2 = behavioral_vs(window_energy_2nd);
vs_max_2 = max(vs_window_2);
vs_min_2 = min(vs_window_2);
vs_diff_2 = vs_max_2 - vs_min_2;

fprintf('\nBehavioral VS in turn-on window:\n');
fprintf('Max: %.15f \n', vs_max_2);
fprintf('Min: %.15f \n', vs_min_2);
fprintf('Difference: %.20f mJ\n', vs_diff_2 * 1e3);
```