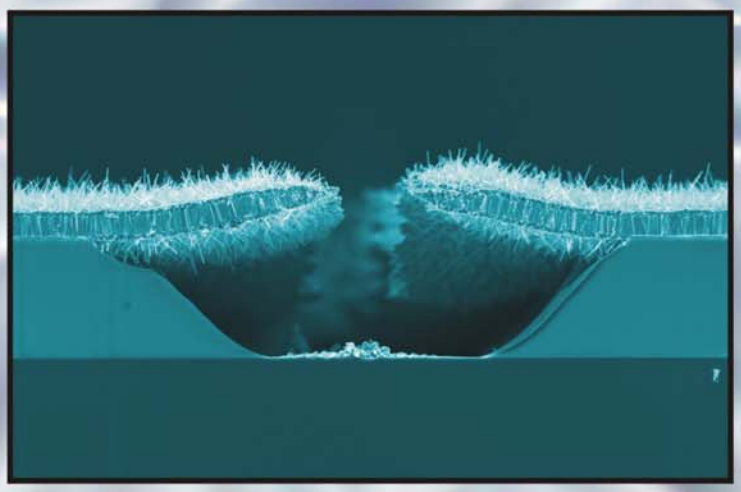
Hot tips for chemistry: development of a carbon nanotube based field emitter array for plasma chemistry on chip

M.Sc. Thesis

A.W. Groenland



Supervisors:
Prof. Dr. J.G.E. Gardeniers
A. Agiral M.Sc.
Dr. Ir. R.M. Tiggelaar

29 November 2006
(Sept. 2005 - Nov. 2006)

Fluidics
BIOS The Lab-on-a-Chip Group
MESA+ Institute for Nanotechnology
University of Twente The Netherlands

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To Femke

'Every solution breeds new problems'
Murphy's law on microtechnology

Summary

In this project, the feasibility of gated emitter array's (GFEAs) as electron source for plasma chemistry in microreactors is studied. On the basis of the existing literature, a GFEA design with carbon nanotube (CNT) emitters is selected, because of its relative high chemical stability, high electrical (σ) and thermal ($\varkappa$) conductivity, high geometric field enhancement factor (β).

A CNT based GFEA is designed and realised in which noodle shaped CNTs are grown selectively on a nickel (Ni) catalytic layer in a thermal chemical vapour deposition (CVD) process. The CNT growth process is optimized for CNT growth in the realised cups by means of the deposition temperature and time using flat silicon test samples with catalytic nickel sites only.

It was found that CNTs grow also on the TiW or TiW/W gate electrodes of GFEA samples while in that case no CNT growth occurred at the nickel catalyst.

The structural properties of these unintentionally grown CNTs are investigated by HRSEM and TEM, while their composition is verified by XFS and XPS. It was found that they are carbon nanotubes with a diameter of ca 10 nm, grown via metal catalytic particles at the end of the tube.

More research is required to further optimize the design in terms of the mechanical stability of the gate electrode during the CNT growth process, to terminate the CNT growth at the gate electrode and to initiate CNT growth at the nickel catalyst in the field emitter structures.

Preface

Here we are, at the end of November 2006, and nearly passed the finish line. Completing one's studies is quite tiring, as I've experienced. The last five years have been the most exciting years of my life, I think, and I've discovered many new things. To be able to study at a university is privilege and I enjoyed doing it very much. Now, my student life has nearly come to an end by finishing my master project. A new challenge is waiting. Before starting my PhD in the semiconductor components group of Jurriaan Schmitz, there will be one month of (delayed summer) holiday. Finally, I'm really looking forward to it!

Completing a master project is not the work of one person; it can only be achieved by the cooperation of many inspiring people. I owe them a lot and therefore I'd like to mention them here.

First of all, my supervisors Han Gardeniers and Anil Agiral; I considered it as a real privilege work with you in this project. You've given me the chance to explore myself in the cleanroom and you have been very supportive throughout the project. It is a real pleasure to realise you will be cooperating in my PhD project as well!

Of course I'd like to acknowledge my third, 'semi-official' supervisor, Roald Tiggelaar for taking place in the graduation committee, and much more important, for the numerous extensive discussions (on the strangest moments) about my project and microtechnology in general. You've been my supervisor in two previous projects, teaching me the love for microtechnology. Every time we work together I rediscover the 'red cloth on an angry bull' effect. Gathering so much new energy after our discussions is something special and I truly hope we will have the possibility to cooperate in the future!

Next I'd like to acknowledge Albert van den Berg and the rest of the BIOS, lab-on-a-chip-group, for hosting me the last year. I worked in a very nice atmosphere and I think I'll miss Jan Eijkel singing down the corridor in my new job (well, not only the corridor ☺).

The BIOS technicians have been very supportive as well: Johan Bomer for discussions and the evaporation runs in the BAK600 and Daniel Weinperle for many nice moments in the cleanroom including the dicing runs!

Apart from the BIOS group, another group has been very supportive to my project, and these are my future colleagues (still sounds strange to me ☺) of the 3rd floor: the Semiconductor Components group of Jurriaan Schmitz. I have had many nice talks with loads of useful advises and I'm really looking forward to start working with you! Jurriaan Schmitz, thanks for transferring the love for microtechnology in general and for all the smart questions that always made me explore new options. Also a special thanks to Cora Salm for relaxed coffee talks when I was not too clear in my mind, Joost Melia for TiW depositions and analysis, Arjen Boogaard for the urgent help when the Oxford PL400 crashed and finally Rob Wolters for many useful suggestions. Your experience and advice has been crucial for the TiW metal gate engineering and solving the experienced etching problems.

Starting to work in the cleanroom hasn't been easy for me and many people have helped me getting my first experience. The cleanroom staff has always been very helpful, especially Samantha Ooyman-Geerding for help with annealing experiments, Dominique

Altpeter for help regarding the lithography and Hans Mertens for his help with metal depositions.

For the growth of carbon nanotubes, I've cooperated with Jitendra Kumar Chinthaginjala, alias Kumar, of the Catalytic Processes and Materials (CMP) group in a very nice atmosphere. Without this cooperation, it would have been much more complicated to do my research and the resulting samples have been of great importance for my master project.

In order to analyse the results of cleanroom work, technicians of the Central Material Analysis Laboratory (CMAL) have been very helpful. I gratefully acknowledge Mark Smithers for making the numerous of HRSEM and TEM pictures. They are really beautiful and have become the major results of my master project. Furthermore, Gerard Kip did some XPS analysis for me and I have learned a lot from your explanations! Finally, I would like to acknowledge Louise Vrielink for the XFS measurements.

In order to test realised samples in an UHV system, I cooperated with Alexander Lefebre of the System and Materials for Information storage (SMI) group. Although we did not carry out any experiments, you offered me 'space' in your vacuum system and we had some nice discussions about the chipholder. The design and realization of chipholder became too complicated for do-it-yourself work and therefore I cooperated with Sip Jan Boorsma of the TCO. This was a very good cooperation with a very appealing result! It's a proof of the high quality work the TCO is known for.

To conclude I'd like to acknowledge some other people. Anne Hendrikse, Laurens van Oostveen and Mark Oude Alink, you made studying at Twente University to a very nice and pleasant activity. We had loads of fun, walking around and lunching at our 'centre-parks alike' campus, at the snooker table or on the racing bike.

Hans and Helma Groenland, you've always been very supportive, in many respects throughout my studies. Without this support, finishing my studies would have been much more difficult!

Jan and Marja Everlo, very pleasant people that have always been interested and very willing to organize nice activities for smaller successes in my studies. It's an art to celebrate and enjoy the smaller things in life, an art that is well understood in your house.

And finally, I think the most important person of all, Femke Everlo. Without you, I don't think I would have been where I am now and would have become who I am today. The last few months have not been easy, for the both of us, but we made it and I'm really looking forward to start living together (finally!!) in our own place. I'm fully confident you'll finish your studies in Nijmegen in style (in case the Dutch Railways keep track on their important work) and I can't wait to be in the audience for your graduation ceremonies!

Alfons Groenland

Hengelo (ov)
November 29, 2006

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1 Literature study

1.1 Introduction

The last decade a class of vacuum microelectronic devices called field emitter arrays (FEAs) have been developed by industry. The concept of field emitter arrays was introduced first by K.R. Shoulders [1][2] in 1961. These FEAs use field emission at high fields instead of thermal energy to initiate electron emission.

Among other things, these FEAs have found application in high power and high frequency amplifying devices; high temperature electronic devices; miniature mass spectrometers, e-beam lithography tools and X-ray sources. Another application of FEAs that is well documented in literature is the electron beam source for use in flat panel field emission displays (FEDs) as an alternative for liquid crystal displays (LCDs) [1][3][4][5]. FEDs use the same principle of electrons hitting a phosphor coated screen as ordinary cathode ray tubes (CRTs) as depicted in Figure 1. The difference is that CRTs contain a trio of electron guns that is scanned across the screen by deflection electrodes, whereas in FEDs millions of individual addressed field emitter tips are used as electron source [4]. The latter leads to much flatter displays panels.

In addition to these applications, it is suggested here that FEAs can also be used for other purposes, for instance as an electron source to generate high energy (hot) electrons to be used to generate reactive species in a microreactor environment. The achievable high density of tips on a surface should allow creating a significant amount of reactive species per reactor surface. Due to miniaturization, relatively small driving voltages (10-20 V) can be used [6], which allow battery powered portable devices. This is described in the following section in more detail: the M.Sc. project description.

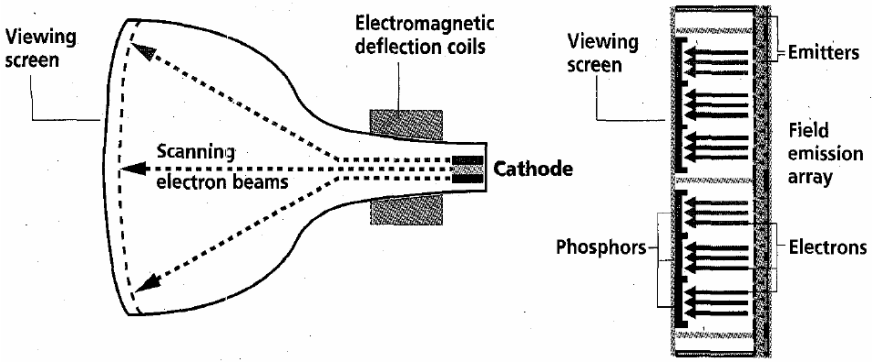


Figure 1. Field emitter displays (FEDs) and cathode-ray tubes (CRTs) are both vacuum tubes that create images by propelling electrons to phosphor-coated screens.
(a) In the CRT, electrons from a trio of hot cathodes are scanned across the screen by deflection coils.
(b) In the FED, electrons from an array of millions of microscopic field emitters are propelled directly to the screen. As no beam deflection is needed, the distance between the cathodes and the screen can be only about a millimeter. Reprinted from [4].

1.2 Assignment: M.Sc. Project: "Plasma chemistry with field emitters"

This project deals with the use of field emitter tips for the generation of reactive species in a microreactor environment. Recently high-density arrays of field emitter tips with a size of 100 nm that can be driven by low voltages (10-20 V) have been reported [6]. Figure 2 shows a typical micromachined field emitter tip [7]. Such tips have been studied mainly for the use in plasma displays. However, although this has never been demonstrated, it should be possible to use such tips also for plasma chemistry. The achievable high density of tips on a surface should allow the creation of a significant amount of reactive species per reactor surface area.

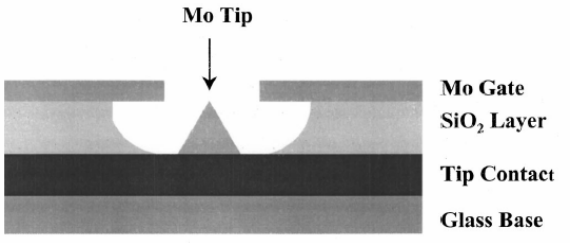


Figure 2. Field emitter tip of the Spindt type with integrated gate electrode. Reprinted from [7]

In contrast to hot filaments, field emission is a cold method that allows the generation of hot (i.e. high-kinetic-energy) electrons. Field emitter tips have been used for catalytic studies, the focus being on the study of the changes in crystalline structure of the field emitting surfaces of metal catalysts [8]. Here we intend to use the tips to create hot electrons that can excite molecules to reactive radicals, allowing chemical reactions to be studied under extreme (microplasma) conditions that are difficult to obtain otherwise. The excitation effects may be optical (via UV generation) or electrical.

Field emission tips have been used to create ions that can be transported into a (miniaturized [5]) mass spectrometer, which may become an important method to directly detect the outcome of the chemical reactions stimulated by field emission. Note that if an array of individually addressable emitter tips is used, each emitter tip may be tuned to a different energy, allowing both a chemical gas phase reaction to occur and ionisation, if required at different locations and with a certain time interval.

Field emitter tips have not been used to do chemistry, generally these devices are operated in vacuum, and non-noble gases are considered undesirable since they may cause deposits after their electron-stimulated decomposition, either on the emitter tip or elsewhere in the device. Cleaning of the tips seems however not be a big issue, what is more important is the corrosion resistance of the tip material. Generally materials that are stable up to very high temperature (diamond, carbon nanotubes, molybdenum) are chosen.

The assignment will consist of the following tasks:

a. Collect relevant literature on the topic of field emitter tips, and make an estimation of the achievable electron energies and energy densities as a function of emitter design and electrical parameters
b. Design and fabricate simple emitter structures
c. Test electrical properties of emitters
d. Perform a simple plasma reaction with emitter tips (using mass spectrometry for analysis of product formation)

1.3 Principle of operation of field emitter arrays

Field emitter arrays (FEAs) are electron sources which have the form of arrays of microfabricated sharp tips, typically with an integrated extraction electrode (gate). When the gate is biased to a large enough positive potential with respect to the tips, electron emission takes place from the tip into vacuum via electron tunnelling through the solid - vacuum potential barrier - the phenomenon known as field emission. In Figure 3 several types of microfabricated FEAs are depicted. The fabrication and choice of cathode materials are discussed in section 1.4 in more detail. The field emission effect itself has been investigated since the beginning of the 20th century but only with the advent of modern microfabrication techniques was it possible to realize microdevices based on this phenomenon [3].

As stated earlier, field emission is a quantum-mechanical phenomenon in which electrons tunnel through a potential barrier at the surface of a solid as a result of the application of a large electric field. Field emission is distinct from thermionic emission and photoemission in which electrons acquire sufficient energy via heating or energy exchange with photons, respectively, to overcome (go over) the potential barrier. In field emission external electric fields on the order of 10^7 V/cm are required for appreciable electron currents. The presence of the electric field makes the width of the potential barrier finite and therefore permeable to the electrons. This can be seen with the help of Figure 4 which presents a diagram of the electron potential energy at the surface of a metal. The dashed line in Figure 4 shows the shape of the barrier in the absence of an external electric field. The height of the barrier is equal to the work function of the metal, φ [eV], which is defined as the energy required to remove an electron from the Fermi level E_F of the metal to a rest position just outside the material (the vacuum level). The solid line in Figure 4 corresponds to the shape of the barrier in the presence of the external electric field.

As can be seen, in addition to the barrier becoming triangular in shape, the height of the barrier ($\Delta\varphi$ [eV]) in the presence of the electric field E [V/m] is smaller, with the lowering, often referred to as 'Schottky lowering", given by Eq. (1)[9]:

$$\Delta\varphi = \sqrt{\frac{eE}{4\pi\varepsilon_0}} \qquad \textbf{Eq. (1)}$$

where e is the elementary charge (1.602×10^{-19} C) and ε_0 is the permittivity of vacuum (8.8542×10^{-12} F/m).

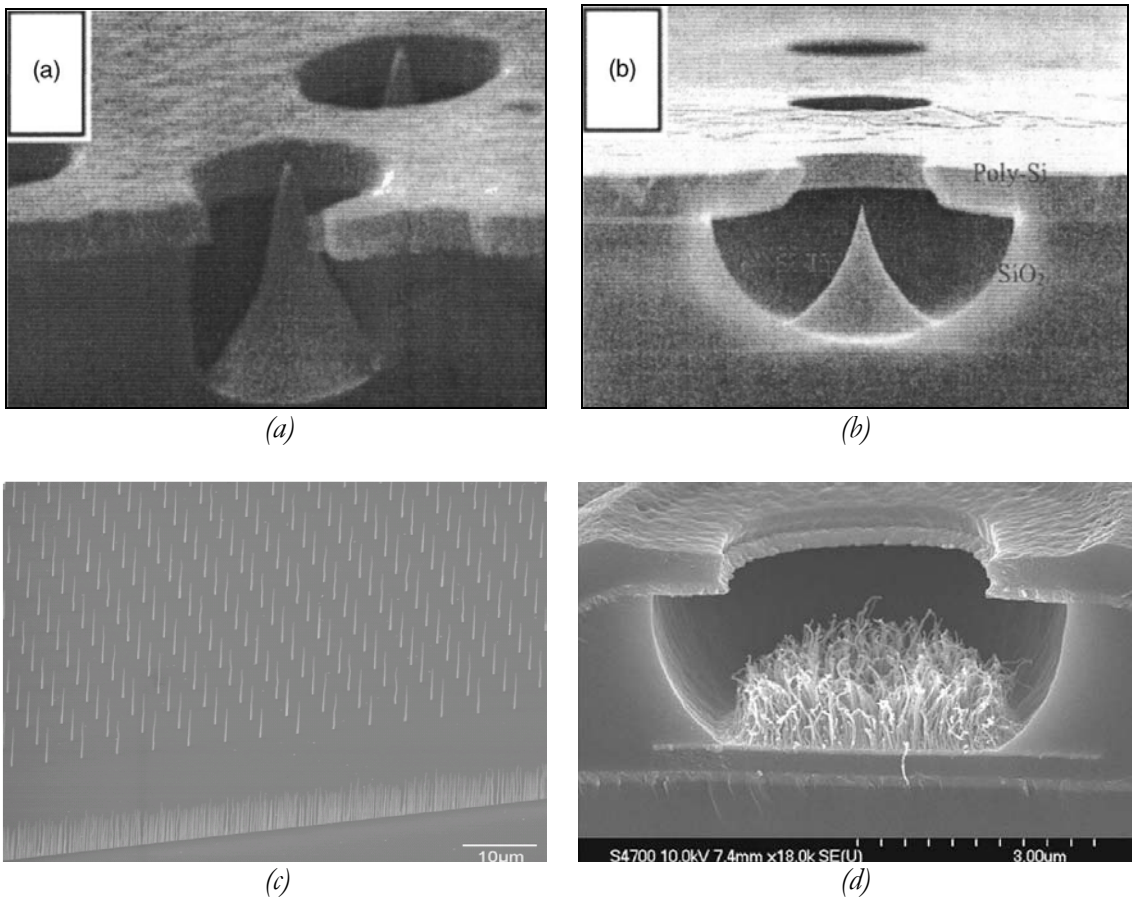


Figure 3. Scanning electron micrographs of various types of vacuum microelectronic device structures:
(a) metal Spindt-type emitter [10]. (b) silicon-post emitter [10].
(c) ungated carbon nanotube based emitters [11].
(d) gated carbon nanotube based emitters [12].

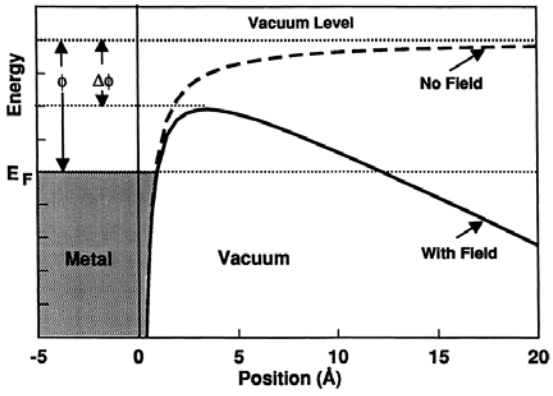


Figure 4. Diagram of the potential energy of electrons at the surface of a metal [3].

Knowing the shape of the energy barrier, one can calculate the probability of an electron with a given energy tunnelling through the barrier. Integrating the probability function multiplied by an electron supply function in the available range of electron energies leads to an expression for the tunnelling current density J [A/cm^2] as a function of the external electric field E [V/cm]. The tunnelling current density can be expressed by Eq. (2) which is often referred to as the Fowler-Nordheim equation [13][14]:

$$J = \left(\frac{e^3 E^2}{8\pi h \varphi t^2(y)} \exp\left[\frac{-8\pi (2m)^{1/2} \varphi^{3/2}}{3heE} v(y) \right] \right) \qquad \textbf{Eq. (2)}$$

where $y = \Delta\varphi/\varphi$ with $\Delta\varphi$ given by Eq. (1), h is the Planck's constant (6.6262×10^{-34} Js), m is the electron mass (9.1×10^{-31} kg), and $t(y)$ and $v(y)$ are the Nordheim elliptic functions; to the first approximation $t^2(y)=1.1$ and $v(y)=0.95 - y^2$. Substituting these approximations in Eq. (2), together with Eq. (1) for y and values for the fundamental constants, one obtains:

$$J = \left(\frac{AE^2}{\varphi t^2(y)} \exp\left[\frac{-B\varphi^{3/2}}{E} v(y) \right] \right) \qquad \textbf{Eq. (3)}$$

were the constants A and B are defined by [103]:

$$A = 1.54 \frac{A \cdot eV}{V^2} \qquad \textbf{Eq. (4)}$$

$$B = 6.87 \times 10^7 \frac{V}{cm \cdot eV^{3/2}} \qquad \textbf{Eq. (5)}$$

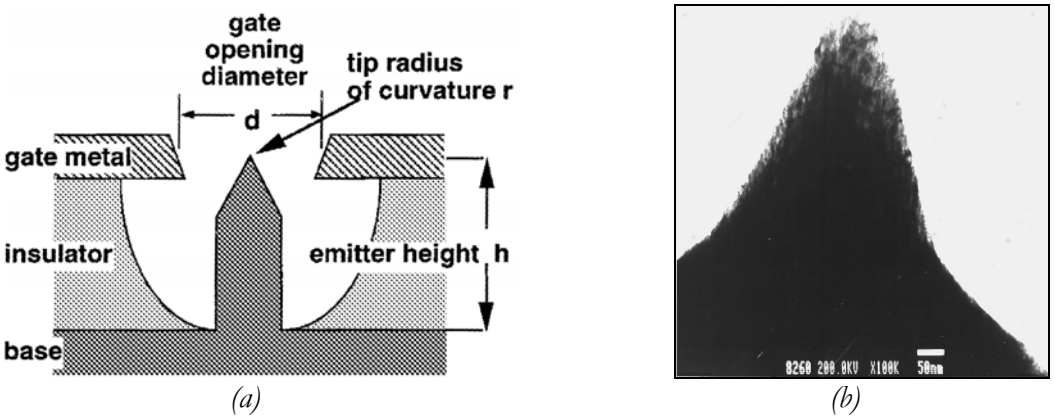


Figure 5. *(a)* Schematic diagram of a cell in a gated FEA. The emitter height is denoted by h, the gate aperture diameter by d, and the tip radius of curvature by r. The positions of the tip with respect to the centre of the gate thickness expressed in c (not shown). For this picture, $c = 0$. Reprinted from [3].
Dimensions for a typical Spindt type FEA are: $h = 2$ μm, $d = 1$ μm and $r = 50$ nm. However, recently FEAs with dimensions a factor of 10 lower ($d = 100$ nm) are reported [6][15].
(b) Transmission electron micrograph of one typical molybdenum tip removed from a microfabricated field emitter array. Reprinted from [15].

Figure 5 represents a schematic diagram of a cell in a microfabricated gated FEA. The emitter has the form of a sharp tip so that advantage can be taken of the well-known enhancement of electric field at surfaces exhibiting high curvature. The physical phenomenon causing this is that charges try to spread out as much as possible on the surface of a conductor and the tip of sharp point is as far away as possible to most of the surface. Therefore some charges of the bulk get pushed into the sharp tip. This relatively small amount of charge can still result in a large charge density due to the small surface and a high charge density results in a high field outside [16].

If the voltage V_g [V] is applied to the gate electrode, the electric field E [V/cm] at the tip is given by Eq. (6):

$$E = \frac{\beta V_g}{d} \qquad \textbf{Eq. (6)}$$

where β is the unitless proportionality constant called the field enhancement or field conversion factor and d [cm] is the gate-electrode distance. β depends on the geometry parameters as depicted in Figure 5, such as the gate opening d, the tip radius of curvature r, emitter height h and position of the tip with respect to the centre of the gate thickness.

Theoretical difficulties for the field enhancement factor are known to arise in the context of extremely sharp tips (r < 10 nm). For example, the FN analysis has built-in assumptions concerning the electron supply function and induced surface charge; assumptions that are predicated on a planar, semi-infinite medium emission surface. For the case of extremely sharp tips, either the radius of curvature or the physical dimension of the tip may violate such assumptions [17]. Other deviations from the FN-model are known, for instance the emission from multiple sites along the tip area, instead of one single emission area [18].

Nevertheless, Zuber derived an analytical relation for β for cone shaped Spindt type cathodes, using a 3D model of the cathode [17]. Although this model gives an analytical expression for β as a function of the tip coordinates (β is not constant over the tip) in the spherical coordinate system, it is still of little use since real tips differ from the modelled tip shape and differences exist between tips due to non-uniformities in the fabrication.

Others, including Spindt [19] claimed that β can be described as $1/kr$ with r the tip radius [nm] and k a unitless empirically determined fitting constant.

It has been shown that the tip radius of curvature r and the gate aperture diameter d influence β most significantly; i.e. β increases rapidly as r and d decrease. A less significant effect is produced by the tip height h and the tip position c, relative to the centre of the gate metal layer thickness. In particular, centering the tip vertically in the gate metal, corresponding to $c = 0$, produces the highest value of β [3].

In practical devices, one can expect variations in the d, r, h and c parameters from tip to tip, as well as in the value of the work function φ due to process imperfections. Even a small variation in e.g. tip radius of curvature, causes a significant variation in the field enhancement factor which leads to variation in emission current from individual tips [3]. Therefore it is difficult to predict the performance of individual tips and generally arrays of multiple tips (FEAs) are measured.

It is concluded, since fitting constants are necessary for the experimental determination of β, that no clear analytical relation exists for it and it remains subject of theoretical modelling.

The performance of FEAs can be determined by voltage/current measurements. Rewriting Eq. (2) and redefining constants leads to the following equation which forms the basis for the so-called 'Fowler-Nordheim plot':

$$\ln\left(\frac{I}{aV^2}\right) = -\frac{b}{V} \qquad \textbf{Eq. (7)}$$

with I [A] the emission current and a and b are (redefined) constants defined by:

$$a = \frac{\alpha A \beta^2}{1.1\varphi d^2} \exp\left(\frac{Bd\varphi^{3/2}(1.44\times10^{-7})}{\beta V}\right) \qquad \textbf{Eq. (8)}$$

$$b = \frac{0.95Bd\varphi^{3/2}}{\beta} \qquad \textbf{Eq. (9)}$$

where α [cm^2] is the emitting area of the FEA.

As can be observed from Eq. (7), there is a linear relation between the natural logarithm of (I/V^2) and $(1/V)$ and experimental data plotted with this relation results in a straight line when the emission mechanism obeys Fowler-Nordheim tunnelling. It has to be noted that a little difference between model and experimental data is reported for when the field emitter just begins to emit and at the high end of emission (saturation) [1].

1.4 FEAs: cathode materials and fabrication techniques

1.4.1 Cathode materials

Several different cathode materials have been used in the fabrication of FEAs. In general, a material used for sharp tips in FEAs should be usable in a microfabrication process in the first way (further referred to as 'machinability'). Many other features are important such as a low work function (φ) which helps to enhance electron emission [14], a high melting point (T_m) and high thermal conductivity ($\varkappa$) which help to withstand high temperatures caused by resistive heating, a high electrical conductivity (σ) to lower resistive heating [20][21], a high physical stiffness (Young's modulus) (Y) and/or 'sputtering threshold' to help emitters to minimize the geometric deformation from ion bombardments [22] and a high chemical inertness to make emitters immune for (residual) gases [22]. It is difficult to compare different materials on the basis of the sputtering threshold, which is defined as the energy required to remove an atom from a surface by an ion bombardment. There is no standard definition for the sputtering threshold and it depends, among other things, on the sputtering pressure, power and gas type. Inert emitter surfaces are important because field emitters typically achieve maximum current density only when their surfaces are atomically clean [23]. For large arrays of tips, high uniformity and high stability of the tip array is required to ensure proper operation [24].

Three main groups of cathode designs are distinguished (see Figure 3): metal 'Spindt' type emitters, silicon post emitters and carbon nanotube (CNT) emitters [10]. Also coated emitter tips (metal or silicon) have been reported [3]. Finally boron nitride nanotubes (BNNTs) are presented as an alternative for CNTs.

1.4.1.1 Metal cathodes

Metal cathodes have been fabricated mainly from molybdenum (Mo), since it was used in the first reported microfabricated FEAs by Spindt and co-workers in 1968 [25] in the so-called 'Spindt' process (see section 1.4.2). Molybdenum was chosen for the fabrication of the sharp tips, because of the highly reproducible emission results, even though the cathodes could not be heated to the temperatures necessary to completely remove adsorbed and dissolved gases from the region of the emitting area [19]. Because of its frequent use for this purpose, a lot of experimental data is available. Anno 2005, state of the art Spindt type FEAs are still fabricated by Spindt, Schwoebel and co-workers with molybdenum cathodes [26]. Key parameters to use molybdenum in FEAs are its strength at elevated temperatures, high melting point, high thermal conductivity and machinability [27].

Other metals for cathode fabrication than molybdenum however, have not been widely investigated in literature [28]. Titanium (Ti), niobium (Nb), zirconium (Zr) and chromium (Cr) cathodes are investigated and reported by Itoh et al, but only the structural properties (cone shape) and not their field emission properties were investigated [29]. Nagao et al [30] investigated gated field emitters with cathodes fabricated of molybdenum (molybdenum), gold (Au), nickel (Ni) and platinum (Pt). They concluded that the platinum emitters showed the best emission characteristics with the lowest operating voltage and the most stable emission among the four kinds of emitters. The platinum emitter showed the most stable emission due to its inert surface. Therefore they concluded that platinum is a promising material for Spindt-type field emitters because of its cone shape, melting point, and inert surface.

1.4.1.2 Silicon cathodes

Silicon based field emitters have been fabricated during the last decade. Silicon (Si) is an attractive material for the fabrication of field electron emitters because its conductivity could be altered through doping or applied voltages and it has a well-developed technology base. The mature silicon integrated circuit (IC) technology makes it possible to integrate silicon field emission arrays (FEAs) with metal-oxide-semiconductor field-effect transistors (MOSFETs) to form novel device structures [31][32] for instance, for FEAs applied in a neutraliser, to be used in space, silicon is chosen as it combines low mass and volume with very low power requirements and the certainty of the manufacturing chain which is crucial [33].

However, silicon FEAs suffered from shortcomings like mechanical fragility and a low electrical and/or thermal conductivity leading to overheating of the tips [34]. These problems are counteracted by applying coatings to the tips.

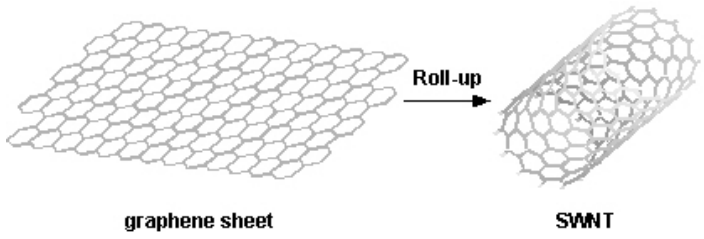
1.4.1.3 Coated metal and silicon cathodes

To improve the performance of FEAs with metal or silicon cathodes, tips have been coated with other materials. Materials used for coatings include diamond like carbon (DLC) or other wide bandgap materials (WBGMs) [34], metals, refractory metal carbides and nitrides because of their low work function and high chemical and mechanical stability [3]. For instance, the application of DCLs in silicon FEAs resulted in lowering of the effective work function (φ) and turn-on voltage [3]. The coating however, can decrease the sharpness of the tip resulting in a lower field enhancement factor β. Even though the high mechanical hardness and chemical inertness of the WBGMs are very beneficial for field emitters, concurrently a wide bandgap is still a prime obstacle that hinders large electron emission and lowers electrical conductivity unless the coating thickness is controlled with high precision [22]. The electron emission current density is a function of not only the barrier height, but also of the electron supply function which in turn depends on the electron concentration in the conduction band. Because of the wide bandgap of diamond, to obtain significant electron emission one needs to populate the conduction band by n-type doping and/or by injection of carriers from a metal contact [3][35]. Exact mechanisms of the electron injection from metal contacts, as well as of the electron transport through the diamond film still remain subjects of theoretical modelling and discussions [3].

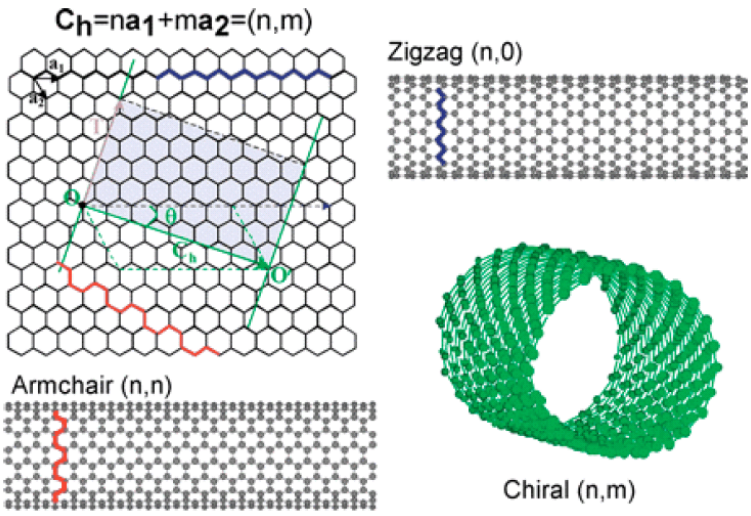
1.4.1.4 Carbon Nanotube cathodes

The last decade a lot of research focused on carbon nanotubes (CNTs) as cathodes in FEAs. CNT based emitters have emitters of long cylindrically arranged graphite sheets of carbon with diameters in the nanometer scale and were discovered by Iijiama in 1991 [36]. They are fabricated by using many different processes which are discussed in more detail in section 1.4.2.

The carbon atoms in CNTs can be arranged in different organisations, including armchair, zig-zag and chiral configurations. These all have different properties and are shown in Figure 6.



(a)

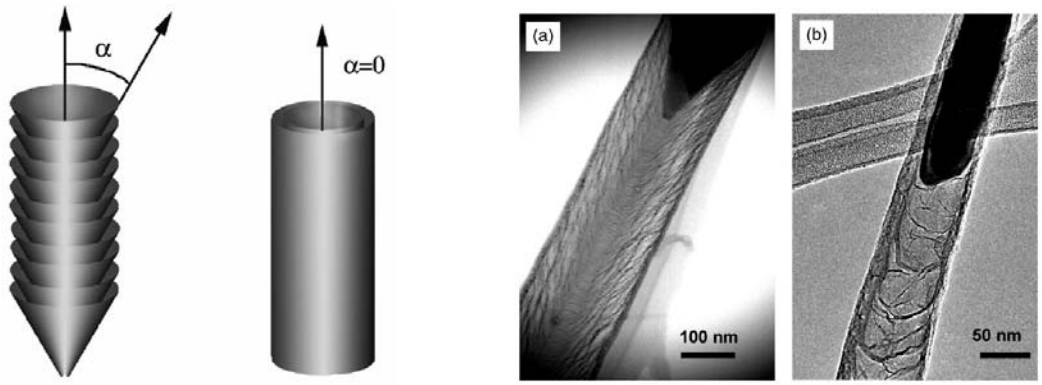


(b)

Figure 6. *(a)* Roll-up of a graphite sheet to a carbon nanotube. Reprinted from [37].
(b) Top left: 'de Heer' abacus: to realise a (*n*,*m*) tube, move *n* times a_1 and *m* times a_2 from the origin to get to point (*n*,*m*) and roll-up the sheet so that the two points coincide…
Other: Different configurations of carbon nanotubes. Reprinted from [1].

CNTs are generally divided into two groups: single walled nanotubes (SWNTs) and multi walled nanotubes (MWNTs) and the tube ends can be open or closed [38]. MWNTs consist of multiple layers of graphite sheets around each other. Furthermore differences exist in the inner structure of CNTs. Using catalytic growth techniques, often stacked cone or

herringbone nanofibres are obtained (see Figure 7). These have different properties than nanotubes. Concerning the terminology used in this work, no difference is made between 'nanotubes' and 'nanofibres'; both are referred to as 'nanotubes'.



(a) *(b)*

Figure 7. *(a)* Schematic structure of carbon nanofibres: stacked cone or herringbone (left) and nanotubes (right). Reprinted from [39].
(b) (S)TEM images of a herringbone carbon nanofibres produced by catalytic PE-CVD with nickel (Ni) as catalyst (left) and a bamboo-type carbon nanofibre grown at the same conditions with iron (Fe) as catalyst (right). Reprinted from [39].

CNTs have a number of beneficial properties that make them interesting cathodes in FEAs. These include a low work function (φ), a low bandgap (E_g) (depending on the chirality of the structure) and to a low threshold voltage (V_{th}) [1], a high geometric aspect ratio (~1000) which results in a large field enhancement factor (β) [23] (up to 18800 [101]), a high electrical (σ) and thermal ($\varkappa$) conductivity [22] and a large Young's modulus (Y) that results in a high mechanical stiffness [22]. Furthermore it is reported that CNT based FEAs have a low electron scattering [23], high stability [1] and chemical inertness [23], they are more robust against poor vacuum conditions compared to other cathode materials like metals or silicon [10], partly due to the fact that CNTs have no non-volatile surface oxide.

Different carbon nanotubes give rise to different field emission behaviour. Bonard investigated the field emission from single CNTs and found that, for his samples, closed MWNTs are the best field emitters (see Figure 8). Furthermore, Chen [40] studied the influence of the orientation (angle) of large arrays of CNTs with respect to the substrate on the field emission current and found that CNTs oriented parallel to the substrate showed the highest emission current. This indicates that electrons can emit from the body of the CNT and hence no strict perpendicular organisation of CNTs is necessary for field emission.

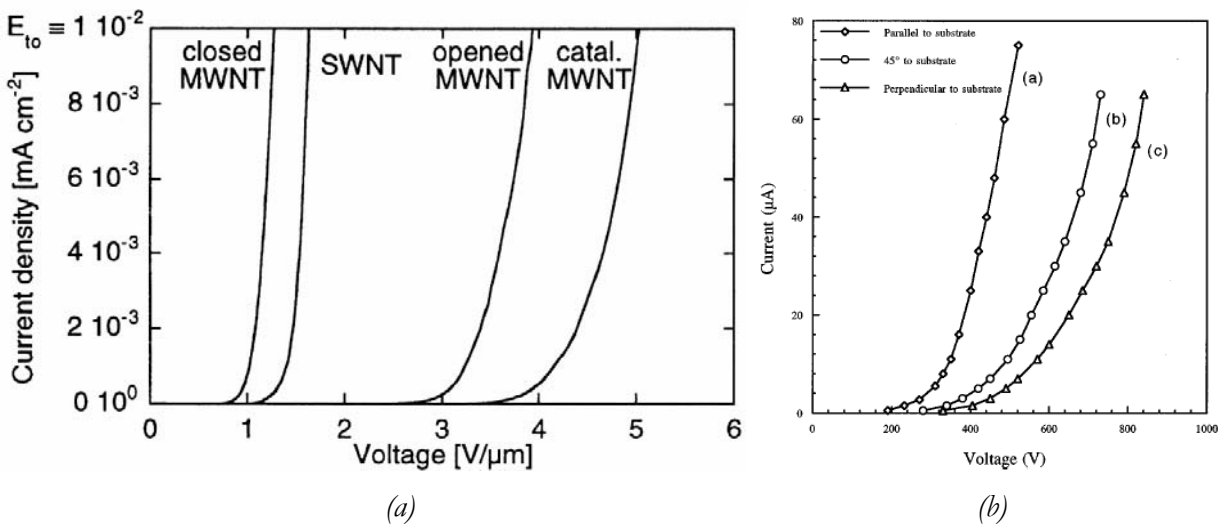


Figure 8. *(a)* Differences in field emission behaviour for different CNTs: open or close single walled (SWNTs) or multi walled nanotubes (MWNTs). Reprinted from Bonard [38].
(b) Emission current for carbon nanotube arrays with different orientations with respect to the substrate. Reprinted from Chen [40].

1.4.1.5 Boron-Nitride Nanotubes

Recently an interesting alternative for carbon nanotubes (CNTs) has been investigated: boron-nitride nanotubes (BNNTs) [41][42]. These are inorganic analogues of carbon nanotubes and possess useful physical properties. Much like carbon nanotubes, they have a high Young's modulus and are good thermal conductors. Unlike carbon nanotubes, which are metallic or semiconducting depending on their helicity, they are semiconductors with a bandgap ranging from 4.0 to 5.5 eV. Since the atomic structure of carbon- and boron-nitride nanotubes cannot be controlled at the synthesis level, this structurally independent electronic property of BNNTs is important for electronics applications.

A recent theoretical calculation predicts that the bandgap of BNNTs can be reduced and even completely eliminated by the application of transverse electric fields [42]. This so-called giant Stark effect (GSE) is analogous to the conventional Stark effect for atomic orbitals. With the GSE, mixing of electronic states in BNNTs occurs in transverse electric fields resulting in a field-induced splitting of the electronic bands. A similar effect has also been predicted for carbon nanotubes, but in BNNTs the effect is enhanced by the absence of screening afforded by the large band gap. For example, using the local density approximation (LDA) for a (22; 22) BNNT with an intrinsic band gap of 4.5 eV, a transverse electric field of 1×10^7 V/cm reduces the gap to 2.25 eV and a transverse electric field of 1.9×10^7 V/cm eliminates the band gap entirely. In principle, transverse electric fields can be used to continuously tune the electronic properties of BNNTs from nearly insulating to metallic [42].

Another advantage of BNNTs over CNTs is that they are more resistant to oxidation than carbon and therefore suited for high temperature applications in which carbon nanostructures would burn [43]. Carbon nanotubes usually have a noisy, switching

behaviour most likely associated with gas molecules adsorbed to the tips of the nanotubes. Boron nitride nanotubes, however, show stable field emission with less noise than for typical carbon nanotube samples. This may have implications for the use of BN nanotubes as stable field emission sources for lighting and flat panel displays [44].

A disadvantage of BNNTs over CNTs is that much research focuses on CNTs and therefore much more experimental data is available about CNTs.

1.4.2 Fabrication of FEAs

1.4.2.1 Metal emitters

Metal Spindt type emitters, being the first microfabricated FEAs created by Spindt and co-workers in 1976 [19], are formed by evaporating metal through a shrinking aperture [1][3][19]. The cone deposition is started after the gate hole is partially closed by an extra layer (aluminium). The cathode metal is evaporated and arrives normal to the rotating substrate. Due to the condensation of the metal, the aperture of the hole decreases gradually, leading to the formation of the cone. Considerable control of the cone height, angle and tip radius is obtained by the choice of the starting aperture size, the thickness of the oxide layer (gate spacing) and the distance of the evaporation source from the substrate [19]. An overview of the process flow is illustrated in Figure 9a. The shape (sharpness and hence the field enhancement factor β) of the cathodes depend on the exact process parameters and differ between various metals [29].

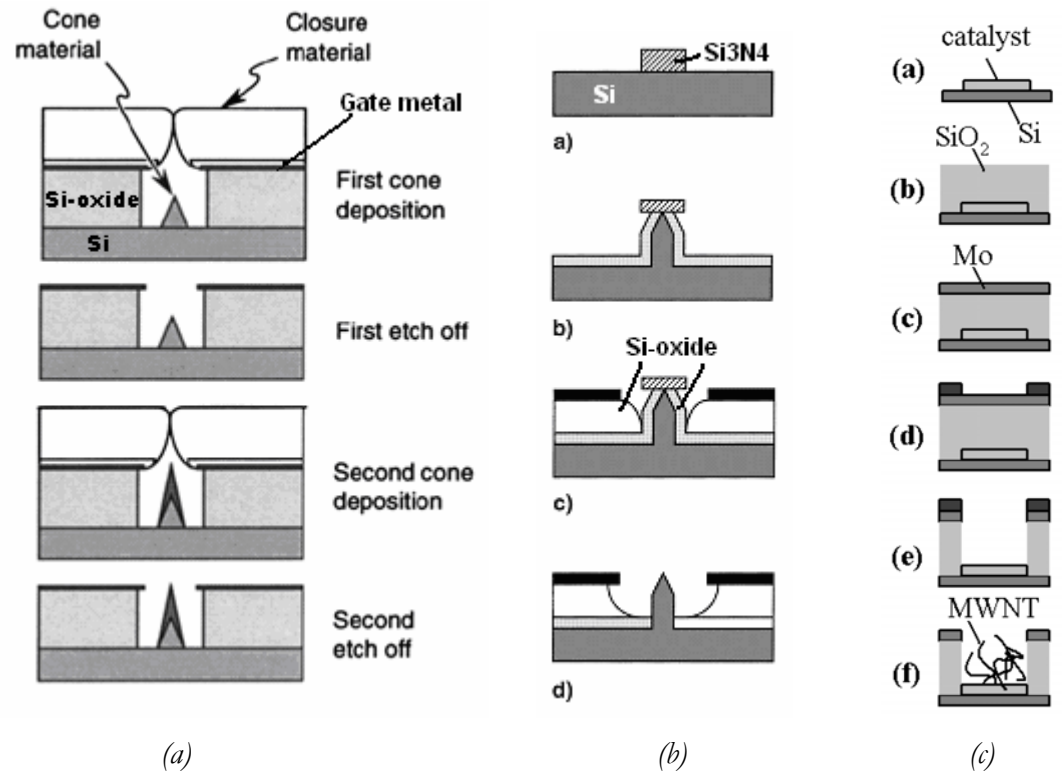


Figure 9. *(a)* State-of-the-art process flow for the fabrication of Spindt-type FEAs. High aspect ratio emitter cones are formed by a double-deposition process while rotating the substrate. Reprinted from [3][45].

(b) Diagram of the process flow for fabrication of silicon tip-on-post FEAs in which emitters are formed by etching and the gate electrode is self-aligned to the tips. Reprinted from [3][45].

(c) Process flow for the fabrication of gated CNT based FEAs.

Reprinted from [1].

1.4.2.2 Silicon emitters

Silicon post emitters are fabricated by etching posts in silicon and sharpening them afterwards in an oxidation process. An insulating layer of silicon oxide is deposited around the post on top of which the gate electrode metal is deposited. During the first etch, the width of the silicon posts is defined by a cap of silicon nitride that is removed later. An overview of the process flow is illustrated in Figure 9b [1][21][3].

1.4.2.3 Carbon nanotube based emitters

Carbon nanotube (CNT) based emitters have emitters of long cylindrically arranged graphite sheets of carbon with diameters in the nanometre scale. The first generation of CNTs was fabricated as soot by an arc discharge, sometimes in combination with laser ablation [22]. Usually, this growth method together with laser ablation is known to produce highly crystalline single-walled (SWNTs) and multiwalled nanotubes (MWNTs) [22]. MWNTs are more frequently studied than SWNTs because of the stability and the relative ease of surface modification while maintaining high conductivity [46].

However, the exact growth properties like the diameter, length and directional growth are difficult to control in an arc discharge which results in a large spread in tip parameters and hence field emission properties [22]. Also cleaning steps are necessary to remove by-products like amorphous carbon, metal and graphitic particles that have a negative effect on the field emission properties of the CNTs. Therefore CNTs are nowadays grown in a chemical vapour deposition (CVD) process on a catalytic surface that can be patterned using conventional micromechanical fabrication techniques [1]. In a CVD process the growth properties are precisely controlled and slowed down over a prolonged growth period [22] with a serious reduction in the number of purification steps. An overview of a process flow is illustrated in Figure 9c [1].

A lot of different CVD processes are used by different groups, either thermally (T-CVD) or plasma enhanced (PE-CVD), with different carbon sources like acetylene (C_2H_2), methane (CH_4), carbon monoxide (CO), ethylene (C_2H_4) and alcohol (C_2H_5OH). T-CVD grown CNTs are steel wool or noodle shaped, while PE-CVD grown CNTs are grown directionally (vertically aligned) (see Figure 10). Typical vertically aligned CNTs are grown in 20-30 minutes at temperatures ranging from 600-1000 °C and are, on average, about 10-50 μm long and 50 nm wide.

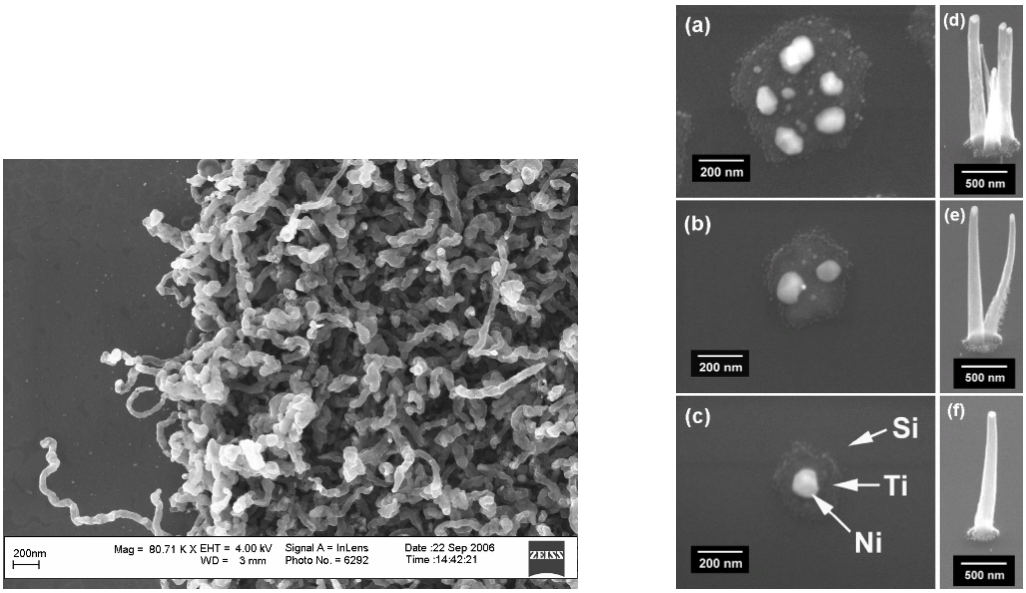


Figure 10. *(a)* Noodle shaped CNTs grown on a nickel catalyst in a T-CVD system, grown within this project for 20 min @ 700 °C in C_2H_4 + N_2.
(b) Vertically aligned CNTs grown on a nickel catalyst in a PE-CVD system (C_2H_2 and NH_3 + He) with corresponding catalytic nanoparticles. Reprinted from [47].

The catalyst used to initiate CNT growth dramatically influences the size, structure and shape of resulting CNTs [39]. In general thin films of nickel (Ni), iron (Fe), cobalt (Co) or metal alloys are used. The metal film agglomerates at high temperatures forming nanoparticles [6]. The size of these nanoparticles is related to the film thickness. On each of these active catalytic nanoparticles CNTs grow as the carbon source is switched on. In order to control the CNT growth process, the formation of these nanoparticles has to be controlled in a high manner. This is still the challenge on which current research focuses; nanoparticle formation depends, among other things, on the metal used, the thin film morphology, the substrate (metal/substrate interaction), deposition method and thin film stress [39]. Furthermore catalysts are activated and/or cleaned sometimes by means of exposure to an etchant gas (NH_3) or ion bombardment (argon) to remove pollution from the surface [39].

In general it is concluded that small nanoparticles give rise to long CNTs with a small diameter, while large nanoparticles initiate the growth of shorter and thicker CNTs [39]; the deposition of carbon per unit time is more or less constant.

1.4.2.4 Boron nitride nanotube cathodes

Boron nitride nanotubes can be produced reliably in a macroscopic amount in a non-equilibrium plasma arc discharge process. The method allows for a controllable and relatively low metal content in the growth reactants and produces almost exclusively double-walled nanotubes in high yield. The double-walled BNNTs turn in self-assembled nanotube bundles or ropes [48]. However, a non-equilibrium plasma arc discharge process is not compatible with standard microfabrication techniques which makes the integration of BNNTs in a micromechanical device more complicated.

The synthesis method employs nitrogen-free, boron-rich conducting electrodes arced in a pure nitrogen gas environment. The electrodes incorporate only a small amount of nickel and cobalt, used primarily as a catalyst. The arc discharge synthesis takes place in a conventional-design water-cooled nanotube direct-current arc synthesis chamber. The chamber is pumped down to less than 30 mTorr and then backfilled with N_2 gas with the pressure stabilized to 380 Torr. During the synthesis, the arc current is sustained nominally at 60 A (DC) with electrode voltage in the range 30 to 45 V. During the arc, a gray web-like material grows preferentially near the top of the chamber, while a thin layer of gray soot covers the side walls of the chamber. Both the web-like material and the gray soot contain an abundance of BN nanotubes, but the web-like material is significantly richer in BN nanotubes. Remains of raw material removed from the chamber are ultrasonically dispersed in isopropanol [48].

1.4.3 Materials overview table

In order to compare different cathode materials, several material properties are summarized in Table 1.

Table 1. Cathode materials properties (bulk properties)

	Workfunction	Bandgap	Electrical conductivity	Meltingpoint	Thermal conductivity	Young's modulus
	φ	E_g	σ	T_m	κ	Y
	eV	eV	10E6/cm Ω	K	W/cmK	GPa
Mo (a)	4.6		0,187	2890	1.38	329
W (b)	4.55		0,189	3680	1.74	411
Si (c)	4.52	1,1	2,52 E-12*	1683	1.48	47
Si-coated	2-4 (d,e)					
CNTs	4,3-5,7 (f,g)	< 1 (f)	1E-2 (f)	~4550	20-66(f,h)	1000-4000 (h,i,j)
BNNTs	11-13 (l)	4-5,5 (k)			6 (k)	1180 (k)

* undoped silicon: electrical conductivity of silicon is a strong function of the doping level; it varies between 10^{-3} and 10^{4} Ω^{-1} cm^{-1} for doping levels of 10^{12} and 10^{21} cm^{-3} respectively [102].
(a) [49], (b) [50], (c) [51], (d) [52], (e) [3], (f) [1], (g) [53], (h) [54], (i) [55], (j) [56], (k) [42], and (l) [44].

Such an overview gives an impression and makes it possible to compare different materials. However, the values used here are only an indication; actual values usually depend on the exact deposition and operation conditions of the tips and micromechanical properties can differ from bulk values as found in standard lookup tables.

For instance, the work function of molybdenum (Mo) is approximately 4.5 but values ranging from 4.2 - 4.7 eV are reported [57]. However, it is shown that a post sputter anneal (400 - 900 °C) alone already increases the work function by 0.7/0.8 eV which indicates that the molybdenum films are altered by the anneal [57]. Therefore it is expected that the work function will increase during operation when the tips are heated due to resistive heating.

The work function of CNTs (MWNTs) has been estimated by Chen [40] and Ago [46] to be 5.7 eV and 4.3 eV, respectively. The discrepancy (and the lack of explanation for it) indicates that it is difficult to measure the work function of carbon nanotubes accurately under present experimental conditions [1]. Moreover, according to Ago reliable work functions of carbon nanotubes have not been obtained and, hence, have been assumed to be the same as that of graphite. Work functions estimated from field-emission spectra using a Fowler-Nordheim model resulted in values that are not reliable because of uncertainty in the parameters employed and the nonlinear behaviour of the spectra. In fact a wide range of work functions from 0 to 8 eV have been reported. The work function depends on the origin of CNTs (metallic or semiconductor), chirality, and whether they are SWNTs or MWNTs [53].

Ago determined the work function of purified MWNTs using a different method (ultraviolet photoelectron spectroscopy) at 4.3 eV. However, MWNTs oxidized with different methods (air, plasma or acid) have higher work functions of (4.4, 4.8 & 5.1 eV), which indicates the MWNTs are sensitive to environmental influences [46].

It is also difficult to determine the field enhancement factor (β) of a MWNT FE device with multiple emission sites, but it is known that it will be high due to the small tip radii of the nanotubes [53].

The electrical conductivity of silicon depends strongly on the doping level and varies roughly between 10^{-3} and 10^{4} $\Omega^{-1}cm^{-1}$ for doping levels of 10^{12} and 10^{21} cm^{-3} respectively [102]. For commonly used doping levels (10^{15} cm^{-3}) the conductivity of silicon ca. 10^{-1} $\Omega^{-1}cm^{-1}$, for undoped silicon it is 2.52×10^{-6} $\Omega^{-1}cm^{-1}$.

1.4.4 Current densities achieved with various cathode materials

In order to compare the performance of field emitter arrays (FEAs) with different cathode materials, some emission characteristics are summarized in Table 2. The maximum current densities found in literature are given.

Table 2. Emission characteristics for field emitter arrays with different cathode materials.

	Current density	Current	Area	Tips	Current /tip	Voltage	Gate distance	Field	Power /area	Reference
	J	I			*I*/tip	*V*	*d*	*E*		
	A/cm^2	A	cm^2	#	nA	V	µm	MV/cm	W/cm^2	
Mo	2150.0	5.92E-02	7.45E-05	7450	8.0E+03	140			3.0E+05	[58]
Si	2250.0	3.60E+05	1.60E-07	3600	100.0	90	0.40	2.25	2.0E+05	[31]
Si-coated	2.5	1.00E-02	4.00E-03	16000	625.0	100	0.50	2.00	2.5E+02	[59]
CNTs	6.0							0.20		[60]
CNTs	0.2	1.00E-03	5.00E-03	33000	30.3	41	0.75	0.55	8.2E+00	[23]
BNNTs		6.50E-07				280	6.00	0.47		[44]

FEAs with molybdenum (Mo) cathodes have demonstrated the potential for emission currents of the order of amps and current densities in the kA/cm^2 range. However, historically their full potential has not been realized, due to insufficient emission spatial uniformity over the array. For example, current densities exceeding 2 kA/cm^2 have been reported but only over areas of approximately < 10^{-4} cm^2. For areas of 10^{-1} cm^2 or larger, current densities exceeding 10 A/cm^2 are seldom seen [26].

Silicon field emitter arrays with atomic sharp tips (< 3 nm) have been demonstrated and are able to generate 10^{-7} A/tip in a 60 × 60 array of 16 µm^2 which is equal to a current density of 2250 A/cm^2. But, the same as for molybdenum FEAs, these current densities are only achieved for very small areas [31].

Silicon field emitter coated with carbon like materials showed a lower turn-on voltage, but the maximum current density remained the same, only at lower operating voltages. This indicates that the maximum achievable current density is limited by other factors also, like anode heating or limitations in the measurement equipment [3]. Sato [59] demonstrated that his HfC coated silicon FEAs had 20 times higher maximum current density compared to uncoated silicon FEAs. Still the maximum current density of the HfC coated silicon FEAs is only 2.5 A/cm^2 of a 16000 tip array occupying 0.4 mm^2. Thus the performance of coated silicon FEAs is better than uncoated silicon FEAs, but still less than state of the art molybdenum field emitters.

Due to their structural properties, CNTs have the potential to conduct currents as large as 10^9/cm^2 [54]. This current density however belongs to CNTs used as conductive wires, not as field emitters. Bronikowski et. al. [13] demonstrated a FEA equipped with CNTs with a current density of 6 A/cm^2 with a field of 2 × 10^5 V/cm and Hsu et. al. [23] reported a maximum current density of 0.2 A/cm^2 for a 0.5 mm^2 array containing 33000 gated field emitter tips. This indicates that the current density is limited by other factors and can be reached only (a) when the emitters are well aligned and placed with their long axis perpendicular to the film substrate, and (b) when the emitters are well separated from one another. These conditions are naturally realized in (metal) Spindt tips and silicon cathode arrays, which are up-to-now the only industrially viable film field emitters. Therefore it is

concluded that carbon nanotube films will have to be realized fulfilling the conditions mentioned above to reach a maximal emitting efficiency [38].

BNNTs used in FEAs are, according to the author's best knowledge, described solely by Cumings et. al. [44]. They found a maximum current of 6.5×10^{-7} A for an operating voltage of 280 V. Since no dimensions of the test structures are given, no current density could be calculated, but it is assumed to be lower than CNT based FEAs.

1.5 Field emitter arrays in long term operation

In this project FEAs are proposed to produce chemically active species in a gaseous environment, therefore the effects of gases on the emission current of FEAs were collected from literature. As stated earlier in section 1.1, FEAs are widely applied in plasma or field emission displays (FEDs) and their performance is limited by residual gases in the displays. Because of the great commercial interest in FEDs, many groups around the world have been studying the effects of (small amounts of) gas on the emission current of FEAs.

In order to reduce the probability of electron-gas collisions in the inter-electrode spacing in FEDs, field emission devices require a high vacuum (UHV, $p < 10^{-6}$ Torr) for their operation. One large obstacle to the successful commercialization of field emission displays has been current degradation during operation over many hours [7]. This problem is related to the difficulty of sealing the display and then operating the FED while maintaining adequately high vacuum conditions. Residual gas not removed by the bake and seal cycles or gas liberated by electron beam bombardment of display components is known to interact with FEAs and result in current decay.

However, when determining the effects of ambient gases in the vacuum on a field emission device, several factors must be considered, namely: the absolute pressure and partial pressures of constituent gases, any additional sources contributing to the background pressure (and how they evolve over time), and the effects that each species, both beneficial and detrimental, may have on the emission properties of the device, which in turn depends on the materials *and* geometry that make up a particular device [10].

1.5.1 Timeframe of current degradation

The electrical behaviour of field emitter arrays (FEAs) in field emission displays (FEDs) is a function of the operating time, because current degradation occurs during operation. Although exact timeframes are difficult to determine, some general trends are observed. A parallel can be drawn with reliability engineering theory to place several current degradation mechanisms in time. In reliability engineering the lifetime devices can be described by the 'bathtub' curve which relates the failure rate in a population of devices to time. Three timeframes are defined (see Figure 11): during the first timeframe, 'infant mortality', devices with critical errors fail first, resulting in a decreasing failure rate. Next the 'useful life' starts in which devices work properly but some fail, resulting in a low, constant failure rate. In the end, 'wear-out' starts, where intrinsic failure mechanisms set in and the failure rate increases until all devices are broken [61].

Field emitters used in current degradation experiment are seldom used directly after fabrication, but before the actual current measurements, devices are operated several hours (up to 24 hours) at relatively high currents. This treatment is further referred to as 'burn-in' and afterwards stable emission characteristics are obtained [7]. This burn-in timeframe can be compared with 'infant mortality'.

The lifetime of FEAs in FEDs is limited to several 1000s of hours by wear-out mechanisms like phosphor fatigue. In between, during 'useful life' the FEAs operate with stable emission characteristics. However, this useful life can be limited to less than 1000s of hours due to several current degradation mechanisms. These current degradation mechanisms are discussed in more detail in section 1.5.4 and take place at a time scale of hours.

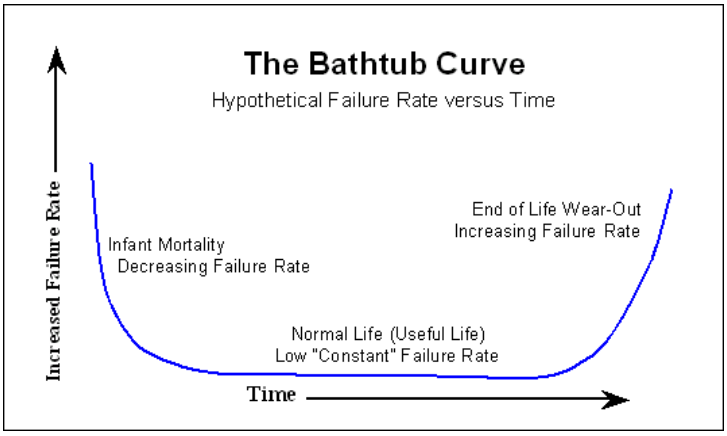


Figure 11. Bathtub curve with relates the failure rate to time [61].
For FEAs in FEDs infant mortality ends at 24 hours of operation and wear-out starts after 1000s hours of use [7].

1.5.2 Origin of gases in field emission displays

In field emission displays (FEDs), field emitter arrays (FEAs) are operated in sealed packages under UHV conditions. During operation, gas can be introduced to the sealed package. The primary species present in a sealed field emission display include hydrogen (H_2), oxygen (O_2), water (H_2O), methane (CH_4), carbon monoxide (CO), carbon dioxide (CO_2), and argon (Ar) with the sources contributing to their origin being processing conditions, outgassing, electron beam induced desorption, permeation, and leaks [10]. For instance, argon assisted sputtered molybdenum (Mo) tips are known as a source of argon [7]. A partial pressure of only 10^{-8} Torr of oxygen (O_2) gives rise to current degradation of 60% over 80 hours of use (see Figure 12) when compared to an UHV of 10^{-10} Torr [62].

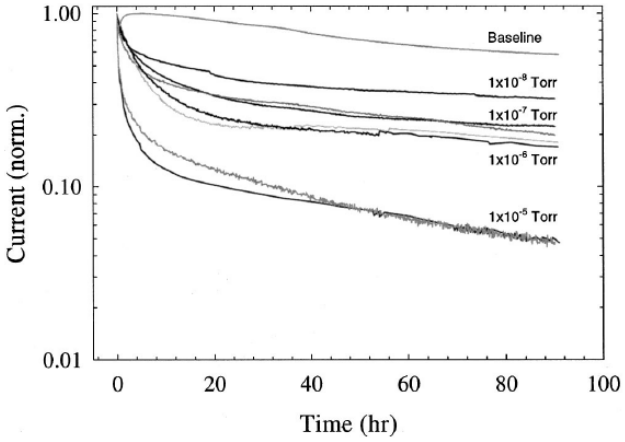


Figure 12. Emission characteristics of molybdenum field emitter arrays with stainless steel anodes in the presence of presence of O_2. The emission current is normalized to the peak value after the initial activation. Reprinted from [62].

1.5.3 Exposure time and recovery

Numerous experiments have been performed on field emission arrays (FEAs) exposed to several gases in a vacuum chamber and the emission characteristics are compared to others measured under UHV conditions ($p \sim 10^{-10}$ Torr). It is shown that emission characteristics of a FED can improve after an exposure to gas when it is operated in UHV again [7][10][63]. This indicates that degradation mechanisms are partly reversible. An example of such a recovery is given in Figure 13, where molybdenum tips are exposed to several partial pressures of argon for a limited time.

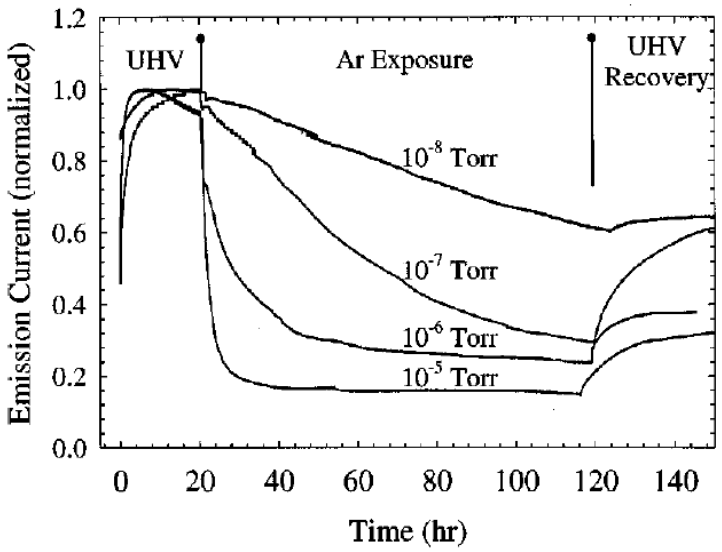


Figure 13. Normalized emission current changes in the presence of argon at various partial pressures for a total exposure time of approximately 100 h.
Reprinted from [63].

1.5.4 Current degradation models

Experiments with field emission arrays (FEAs), operated in gaseous environments, have led to a number of theories that have the potential to explain the observed current degradation. It has to be denoted that the validity of these models depends heavily on the materials used in FEAs, for instance either silicon (Si) or molybdenum (Mo) tips. Nevertheless, they give an impression of why and how the presence of gases influences the emission current characteristics of FEAs.

1.5.4.1 Oxidation induced current decay model

When molybdenum FEAs are exposed to oxygen, water or carbon dioxide, molybdenum oxides can form on the tips during useful life. Due to the presence of these oxides, the work function of the tips increases (see Eq. (2)), resulting in a lower emission current [7].

This behaviour has been thought to be evidence of oxidation induced current decay. However, the amount of degradation appears essentially identical for a given gas exposure level. Because the current degradation depends on both the gas pressure and the exposure time, the exposure is defined as the pressure multiplied by time and expressed in the units of Langmuir (L), where 1 L corresponds to 10^{-6} Torr × s [3].

This similarity in current degradation for a variety of oxygen containing species, and more importantly, for inert gases, as well as subsequent current recovery, argues against oxidation as an important factor in emitter degradation. Further, experimental measurements have shown that molybdenum oxides do not form rapidly in air under temperatures less than 200 °C. Reported effects of successful "burn-in" treatments (see section 1.5.1) of tips leading to an increase of the emission current during the first hours of operation are attributed to the removal of oxides on the tips for silicon tips.

In summary, oxidation of molybdenum as an explanation of current decay is inconsistent with the similarity in behaviour of oxygenic and inert gases, the relatively rapid current recovery after gas exposure, and the ability to remove oxide, not form it, by device operation, as occurs in the tip seasoning process. However, molybdenum oxide has been detected on emitter tips after prolonged operation, and therefore, its possible role in long-term degradation cannot be ignored [7].

1.5.4.2 Gas adsorption current decay model

While the similarity in degradation effects between inert gases and O_2 was unexpected, such behaviour might result if physical, rather than chemical interaction occurred between the gas and molybdenum emitter tip. Thus, adsorption of a monolayer of gas should increase the tunnelling barrier and decrease the emission current. Changes in emission characteristics due to the modified work function from monolayers of adsorbents are well known in the literature [7]. Based on the well-known interactions of gases and field emitters, adsorption most probably plays a role in the decay mechanisms. However, a simple adsorption process is not an adequate description. The effects of the various gases and the role that device operational parameters (like operating voltages) play in the degradation rate, argue for a mechanism much more complex than simple changes in work function because of gas adsorbed on the emitter surface [7].

1.5.4.3 Sputter damage current decay model

The ionisation of gas atoms by electrons near the sharp tips may lead to cathode sputtering: metal atoms are removed from the sharp tip due to mechanical interactions. Because of cathode sputtering, the sharpness decreases leading to a smaller field enhancement factor β in Eq. (6). However, this theory is in contradiction with the recovery of emission currents during the restored UHV after gas exposure and also in contradiction with the effects of different gases on the emission current [7].

1.5.4.4 Ion implantation model

Ambient or "local" gas is ionised by collision with the field-emitted electrons and these ions are implanted into emitter cone structures (most negatively biased) and the surrounding gate areas. Although not previously associated with changes to emission current, such an ion implant process is well known and forms the basis of ion pumps [64]. To account for the observed current degradation, it is suggested that inert gas or oxygen ions implanted into emitter tips create a region that increases the tunnelling barrier width by forming a highly resistive surface layer. This would lead to a rapid current decrease followed by saturation or slow roll-off. As more ions are implanted into the near surface region, diffusion and outgassing can compete. This establishes equilibrium between the implant and diffusion rates, leading to current saturation. Lighter atoms (deeper implant), higher pressure (higher ion flux) or increased ion energy (from higher anode voltage) produce a deeper and/or thicker resistive layer. This results in a lower emission current, and the consequent slower diffusion out of the tip material prolongs subsequent current recovery. Faster recovery is noted for lower gas pressure (fewer implanted ions) and higher atomic weight (shallow, near surface implant). As out-diffusion is relatively slow at nominal device operating temperatures, emission characteristics are dominated by implantation. Pressure measurements made on operational packaged FEDs support these arguments. During the first 100 min of operation, pressure decreases of almost two orders of magnitude have been measured. With the device off, outgassing was also detected as a pressure increase, but as expected based on the implant mechanism, it was rather slow with a rate consistent with a diffusion mechanism [7].

It is also suggested that ions, present in glass substrates may give rise to tip pollution. For instance in a study with FEAs on different glass substrates (borosilicate and sodalime glass) current degradation occurred more for sodalime substrates. This difference is attributed to the higher water content and higher porosity of sodalime substrates and also the higher mobility of sodium under high field is supposed to be of influence [7].

1.5.5 Role of hydrogen in FEDs

In contrast to most other gases, studies have shown that the presence of hydrogen can improve the emission characteristics. FEAs can be operated for several hundreds of hours in 10^{-5} Torr H_2 with no damage such as surface etching or ion erosion. An experimental graph is depicted in Figure 14. From the ion implantation model the implantation of hydrogen in molybdenum tip is suggested. While various cleaning mechanisms have been attributed to H_2, it is suggested that implantation may be the dominant effect for H_2 as well. But, because the implanted surface layer may become more conductive, current may actually increase significantly depending on the partial pressure of

H_2 and other contaminant gases. In addition, interaction of refractory metals like molybdenum with hydrogen is not a simple process. This is because the incorporation of hydrogen in metals like molybdenum is not a simple physical adsorption process alone. Hydrogen is soluble in molybdenum and forms stable hydrides. Therefore, the emission properties might depend on how the hydrogen is bonded on the surface. Methane has also been reported to improve emission characteristics. Thus, materials (H_2, hydrocarbons) that produce gas components that result in conductive materials when implanted will result in enhanced emission characteristics. The magnitude and time frame for this positive effect will vary based on the level of background contaminants that create a resistive surface layer and higher effective tunnelling barrier. Due to these beneficial properties of hydrogen, it is currently integrated in FEDs to elongate the display lifetime.

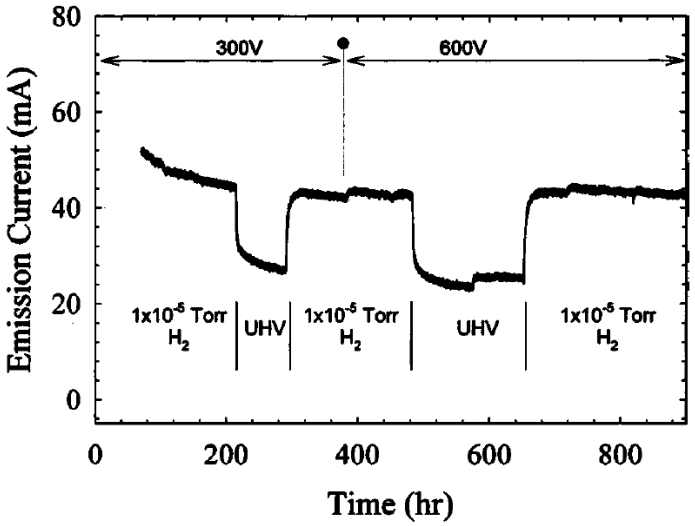


Figure 14. Operation of a molybdenum field emitter array in 10^{-5} Torr of H_2 and under UHV conditions. Experiments were done with stainless steel anodes (bias: 300 V and 600 V) placed 1 mm in front of the cathode. Reprinted from [7].

1.6 Feasibility of field emitter arrays as electron source in microreactors for plasma chemistry

In this project field emitter arrays (FEAs) are proposed as source for high energy (hot) electrons to produce chemically active species in a plasma (see section 1.2). This is not, according to the author's best knowledge, described in literature earlier or elsewhere.

Therefore, properties of FEAs described in literature used in other applications like field emitter displays (FEDs) are discussed in previous sections and related to microreactors in this section.

Several FEAs designs are discussed before, being Spindt type with metal cathode (either coated or uncoated), silicon post FEAs (either coated or uncoated) and carbon nanotube (CNT) based FEAs with boron nitride nanotubes (BNNTs) as an alternative.

The technology for Spindt type FEAs is the most mature (starting at 1968) and they can be fabricated in highly controlled manner. Silicon based field emitter are fabricated in the mature silicon technology driven by the semiconductor industry. Coated FEAs are not widely fabricated and properties differ strongly between various research groups. CNT based FEAs are rapidly evolving the last decade and more and more groups are fabricating them in a CVD process that is compatible with the microtechnology and in which the properties of the CNTs can be controlled quite well. Finally BNNTs are announced to be promising, but they are only made by a few groups around the world. Integration in a device is more complicated since they are fabricated in an arc discharge process in which the properties are controlled quite well, but which is incompatible with the regular microtechnology.

In general, the current density obtained from all FEA designs can be described by the same formula, being the Fowler-Nordheim tunnelling function. Key differences between different FEA designs occur, in principle, in values for the work function (φ) and the geometric field enhancement factor (β).

Maximum current densities in the order of kA/cm^2 are demonstrated for both molybdenum (Mo) Spindt type and silicon FEAs, but only for arrays with an area of at maximum 10^{-5} cm^2 with 1000's of tips. The maximum current (density) is limited by the uniformity of the array and the fabrication of large uniform arrays is difficult from a technological point of view. CNT based FEAs are predicted to be superior field emitters due to their high conductivity (σ) and high β but still the largest current density of only a few A/cm^2 is demonstrated due to technological difficulties including the alignment of the CNTs with respect to the gate electrode.

Since large current densities flow through the tip, tips are heated up due to ohmic heating. Therefore the electrical conductivity (σ), melting point (T_m) and the thermal conductivity ($\varkappa$) are considered. On the basis of this, CNT based FEAs are superior, since σ and $\varkappa$ are at least one order of magnitude higher and T_m a factor 2 higher with respect to molybdenum Spindt type FEAs. Silicon based FEAs are even worse compared to molybdenum Spindt type FEAs.

Field emission devices require a high vacuum (UHV, $p < 10^{-6}$ Torr $\approx 10^{-9}$ Pa) for their operation in order to reduce the probability of electron-gas collisions in the inter-electrode spacing in FEDs. Therefore all field emission properties of all FEAs designs are determined under UHV conditions. However, the effects of gas on the emission current of FEAs have been studied for maximum partial pressures of 10^{-3} Torr ($\approx 10^{-6}$ Pa) since residual gases exist in FEAs in field emission displays (FEDs) led to current degradation over many hours of use. The effects of various gases on the emission current of FEAs depend heavily

on tip material, geometry and gas type. The robustness against gases can be partly expressed in the Young's modulus (Y), since a high Y results in a high mechanical strength. CNT based FEAs are superior since its Y is a factor 10 higher compared to the other designs. Most gases have a negative effect on the emission current leading to a decrease of a factor of 10 or higher, due to the pollution of the cathode surface. Several current degradation models are proposed including tip oxidation, gas adsorption, sputtering damage and ion implantation. The models attribute the decrease in the current density to changes in the work function (φ) and/or geometric field enhancement factor (β).

Gases have different effects on different FEA designs. Within the Spindt type FEAs with metal cathodes, platinum (Pt) cathodes are found to most robust and secondly molybdenum (Mo) cathodes. However, platinum Spindt type FEAs are used only by one group, molybdenum Spindt type FEAs are widely used because of the combination the relatively high robustness and a lower work function. Compared to the other designs, CNT based FEA are found to be most robust against residual gases, since the exposure to gases has less effect on the emission currents.

Several gases including hydrogen (H_2) and methane (CH_4) are reported to have a beneficial effect of the emission current and are able to restore current degradation caused by an exposure to other gases. Also the application of the UHV after an exposure to a gas is reported to have a beneficial effect on the current density and allow partial regeneration of the initial current density for both molybdenum Spindt type and CNT based FEAs.

Given all information mentioned above, in general it is denoted that proper functioning of all FEA designs cannot be guaranteed in pressures above 10^{-5} Torr. Although some gases have a beneficial effect on the emission current, still the emission properties are not known when the FEA is applied as electron source in a microreactor. Furthermore, it is very likely the field emission properties are very poor at these pressures, especially for long term use. However, current recovery by the exposure to hydrogen of methane and/or the restoration of the UHV after operation has been demonstrated to extend the lifetime of the FEAs.

Subject to the pressure in the microreactor being in the 10^{-5} Torr range, it is concluded that CNT based FEAs are most suitable as electron source in microreactor for the generation of reactive species, because of their high robustness against gases (chemical stability), high electrical (σ) and thermal ($\varkappa$) conductivity, high geometric field enhancement factor (β) and high Young's modulus (Y). Disadvantages of CNT based FEAs include the relatively low current densities, less mature fabrication techniques and less information about the physical properties since they are relatively new. However, CNTs have currently the interest of many groups around the world and the knowledge is rapidly evolving.

2 Design and realisation of a gated field emitter array for microplasma generation

2.1 Introduction

In this project a gated field emitter array (GFEA) is designed for the generation of microplasma's on chip and realised using microfabrication techniques. The development of the process flow for making this device within the cleanroom facilities of the MESA+ institute has been the main part of this master project.

In this chapter the design of and the process flow for realising a GFEA are discussed. First the geometric design is discussed, followed by a summary of the process and finally all different steps are discussed with a high level of detail. In the detailed section all small experiments and technological issues and challenges are treated.

2.2 Process design

In order to design a new device, CNT based GFEAs published in literature are studied to base the new design on. A few examples are shown in Figure 15 and a summary of their fabrication processes is shown in Figure 16. Note that Moon (Figure 15c) did not give more process details than that the 'gated FEA templates were fabricated on glass in a photolithography process' [12].

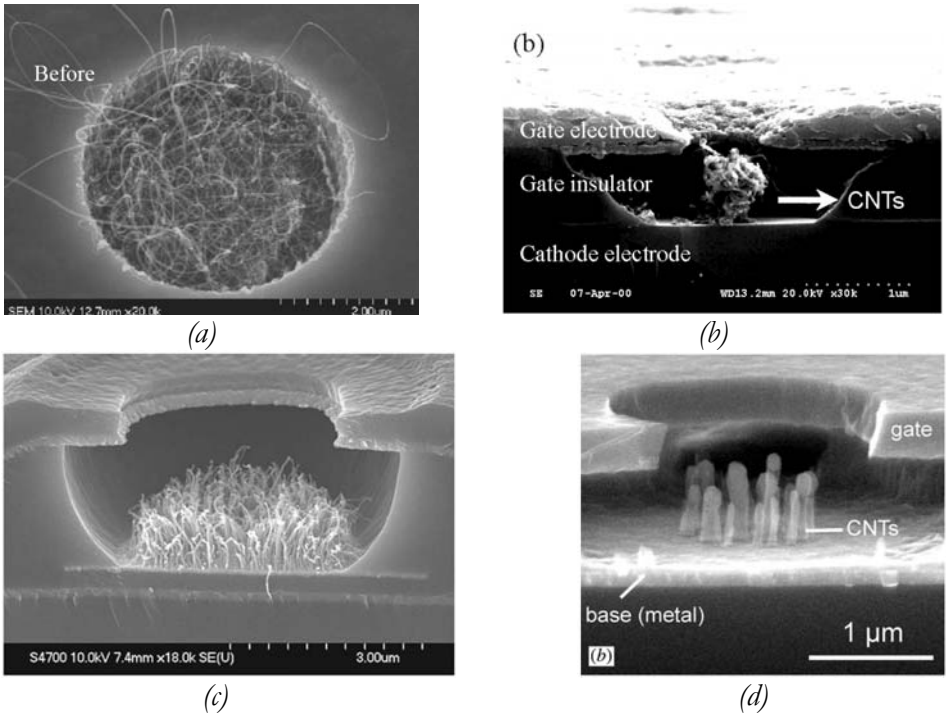


Figure 15. Overview of different carbon nanotube (CNT) based gated field emitter arrays (GFEAs), as published by:
(a) Hale [1], *(b)* Lee [65], *(c)* Moon [12] and *(d)* Pirio/Teo [66/67].

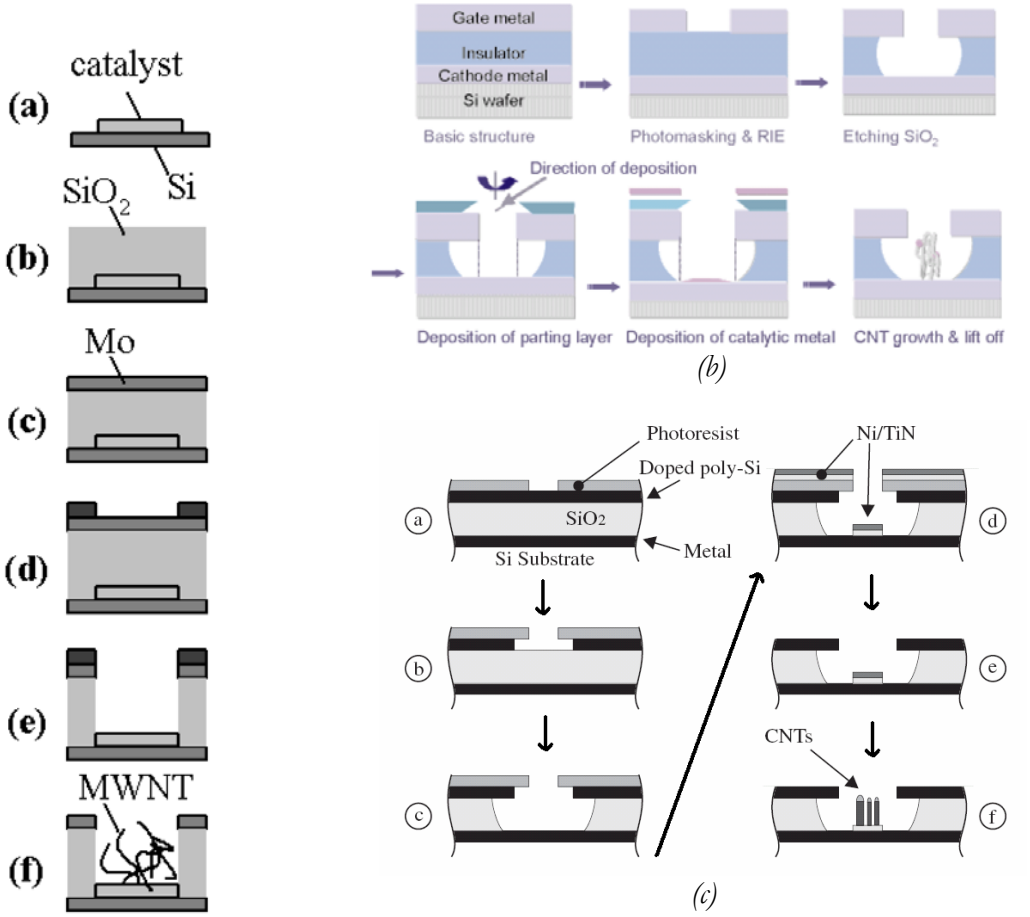


Figure 16. Overview of different processes for the fabrication of carbon nanotube (CNT) based gated field emitter arrays (GFEAs), as published by *(a)* Hale [1], *(b)* Lee [65] and *(c)* Pirio [66] and Teo [67].

Hale [1] made GFEAs by depositing the nickel (Ni) catalysts first, bury them with PECVD oxide and gate metal, and etching them free again in the end. This process requires two masks (nickel and gate hole patterning) aligned to each other. The main difficulty in this process is the controllability of the nickel properties. The deposition of the PECVD oxide, generally done at 400 °C, induces thermal stresses, and the dry etch step needs to have a very high selectivity with regards to the (10 nm thin) nickel. Etching too short leaves the nickel covered with oxide, etching too long affects the nickel thin film significantly since thinning/etching of the surface of the nickel affects its properties. As the properties of the CNTs depend very strongly on the catalyst layer (see section 2.12 and 2.13), this layer should be deposited in the best controllable manner. It is very likely that the etched nickel will behave differently than the as-deposited nickel in the CNT growth process. Furthermore, Hale did not incorporate the desired underetch in the oxide (see section below) by using a dry etch, the oxide may be wet etched in BHF, but nickel etches slowly in this etchant [68].

Lee [65], Pirio [66] and Teo [67] roughly used identical processes, in which first all layers are deposited, a single mask is used to define the gate holes, the gate and oxide are etched forming the 'cups' and the nickel is deposited directionally into the etched cups, using

the gate as an in-situ shadow mask. Excess nickel on the gate is removed by lift-off. Differences between the process used by Lee on one hand and Pirio and Teo on the other hand occur in final nickel lift-off. Lee used a special aluminium parting layer, while Pirio and Teo used photoresist. This has to do with the gate etch and is discussed in section 2.6.3.4 in more detail. The difficulties in this process is the photoresist that is used as etch mask for both gate and oxide etches, and for lift-off of the nickel in the end. Resist should be post-baked well to become hard enough to withstand both etchants, while lift-off requires 'soft' resist that does not adhere too much to the surface (i.e. non post-baked resist). Big advantage of this process is that the nickel deposition is done at the end of the process, thus that its properties can be controlled and tested separately. It is assumed that nickel evaporated through in the gate cups will not behave very different from evaporated nickel on a plain wafer, allowing CNT growth experiments on simple test substrates.

On the basis of studying the literature and iterative designs, a 'final' design, based on the work of Lee [65], Pirio [66] and Teo [67], has evolved and is shown in Figure 17. Before going into the details of the fabrication process for the CNT based GFEA, which is summarized in section 2.3, some geometrical aspects of the design are discussed in more detail first.

2.2.1 Geometric design

In order to get an impression of the dimensions of the design, some geometrical properties were obtained from similar processes published in literature, and which are summarized in Table 3. In order to discuss the geometrical properties, a device before the final nickel lift-off stage is taken as a starting point and shown in Figure 17.

Table 3. Properties of example GFEAs as shown in Figure 15.

Oxide		Gate	CNT	Reference
Thickness [µm]	Deposition method	Aperture [µm]	Growth method	
1	PECVD	4	T-CVD	[1]
1	Thermal oxidation	0,7	T-CVD	[65]
2	?	2	PECVD	[12]
0,5	?	2	PECVD	[66], [67]

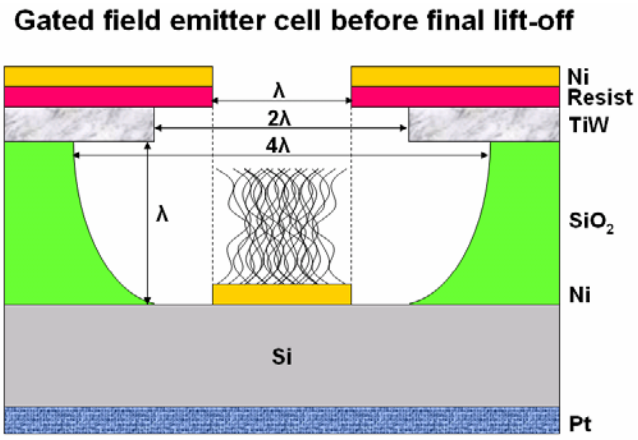


Figure 17. Overview of a gated field emitter cell before lift-off. Dimensions are given in terms of the characteristic length λ. Typical values are in the low micrometer range, in this project λ = 2 µm is used.

The different dimensions in the design are related by the characteristic dimension λ. In order to determine λ a few matters are considered, starting with the oxide thickness.

A thin oxide enables the possibility of high fields around the field emitters with low voltages. However, for thin oxides the leakage current between gate metal and substrate may become relevant and the thinner the oxide is with respect to the gate aperture, the higher the chance of bridging CNTs, shortening the gate and substrate.

The gate aperture is related to the oxide thickness: small gate holes create higher fields covering a larger area inside the etched hole (or cup), but increases the chance that CNTs connect the gate and the substrate, resulting in short circuits. Furthermore, the size of the nickel (Ni) catalytic dot deposited at the bottom of the cup using the gate and photoresist as shadow mask is determined by the same gate hole aperture. The CNTs growth

process is tuned (by the growth time) in such a way that the CNT length will have roughly the same dimensions as the nickel dot diameter. In order to decrease the chance of bridging CNTs between the gate and substrate, the gate can be underetched to a larger diameter as proposed by Teo et. al. [67]. This dimension is set at 2λ.

Finally the gate aperture is limited by the resolution of the photolithography (mask fabrication, resist development). The limit for the lithography equipment available at the MESA+ institute is 1.5 μm. However, making arrays of dots with a high uniformity near this limit is a challenge and requires high control of the photolithographic process, therefore 2.0 μm is a more practical limit.

When the oxide is etched isotropically, the underetch should be controlled in such a way that the gate metal should lean over without collapsing. This dimension is set at 4λ.

For this project, λ is chosen to be 2.0 μm. This is 0.5 μm higher than the lithographic limit. The oxide of 2.0 μm can be etched in BHF (1:7) in roughly 33 min (see section 2.7) with photoresist as mask. Higher values for λ yield a higher oxide thickness and hence require a longer etch time or stronger etchant concentration. Both are likely to give rise to photoresist adhesion instabilities (see section 2.7) which could be solved by introducing a hard mask. However, this hard mask further complicates the process as the photoresist is needed for nickel lift-off in the end.

2.3 Process flow summary

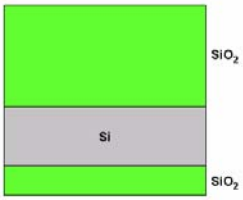
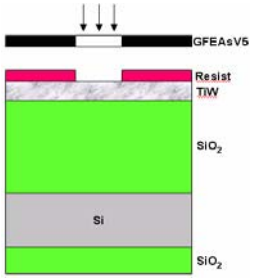
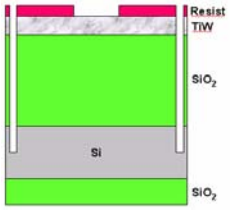
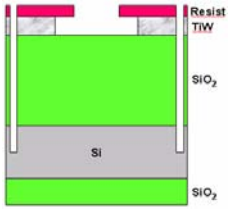
In order to create the device shown in Figure 17, a process flow is developed.
The three main challenges in this process are:

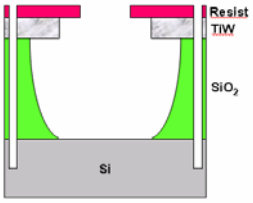
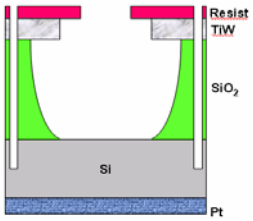
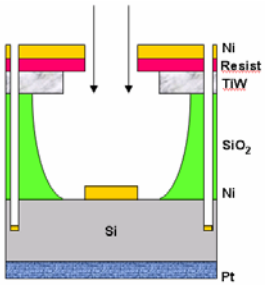
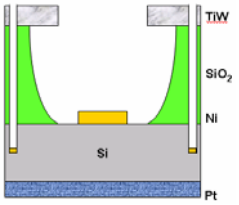
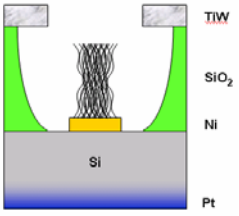
- The lithography: making a large array of holes of 2.0 μm in diameter (1000's) with acceptable uniformity requires a high level of control of the lithographic process.
- The photoresist layer: in the single mask process one layer of photoresist is used as etch mask for both gate and oxide etch steps, as well as for lift-off of the nickel. Resist should be post-baked to become hard enough to withstand both etches, while lift-off requires soft resist that does not adhere too well to the surface. A compromise has to be found to satisfy both requirements.
- Compatibility of the device with the CNT growth process: the CNTs are growth in T-CVD system at 700 °C in N_2/C_2H_4 environment. The devices should survive thermal stress related problems (e.g. adhesion, stability) and all materials used should be chemically inert in the N_2/C_2H_4 environment except for the nickel. Non inert material gives rise to the deposition of carbon based species at undesirable places, leading to deterioration of the final device performance.

Taking this into consideration, a process flow is developed and summarized in Table 4. In the following sections, all different steps are discussed separately in more detail (for instance, choices and selections are explained). In these sections all smaller experiments are discussed that were used to tune the different process steps. The detailed process flow including the exact parameters can be found in

Appendix A: Complete process flow

Table 4. Process flow summary for the realization of a carbon nanotube based gated field emitter array.

Process description	Cross-section after process
Substrate selection, marking and cleaning	
Oxide growth (Thermal oxide)	 *(note: bottom SiO_2 layer is not to scale)*
Gate deposition (TiW, sputtered)	
Lithography	
Dicing untill half the wafer depth	
Gate etch (wet etch, H_2O_2 + NH_4OH)	

Oxide etch (BHF)	
Back electrode deposition (Platinum, sputtered)	
Catalyst deposition (Nickel, evaporated)	
Nickel lift-off	
Dicing (breaking) **and** **CNT growth** (T-CVD)	

2.4 Substrate selection, marking and cleaning

For the substrate section, two choices can be made: an insulating glass or a conductive silicon substrate. As the field emitters need to have an electrical contract (cathode), a glass substrate could be used when a (metal) cathode is deposited at the base of the whole stack. However, problems (like adhesion problems or agglomeration of the metal thin film) could be expected regarding the high temperature compatibility of this concept [69]. Therefore silicon substrates were chosen.

As the charge carriers in field emitters are electrons, the doping of the silicon substrate is taken into consideration. Highly doped wafers were selected as they minimize the substrate resistance (R_s). In p-type silicon the number of electrons (minority charge carriers) is limited by thermal generation which might give rise to current saturation at high fields during field emission. By choosing for a highly doped n-type substrate, these effects are avoided. Therefore highly doped n-type (n^{++}) wafers were selected as substrates. These one side polished (OSP) 100 mm silicon wafers have arsenic (As) doping, (100)-orientation, a thickness of 525 ± 25 μm and a resistivity of 0.001-0.005 Ωcm.

New wafers were marked at the back (non-polished side) with a diamond pen while kept in hand. After marking wafers were ultrasonically cleaned in DI water for 30 minutes.

Prior to processing, wafers were cleaned in the (regular) standard cleaning, consisting of 2 × 5 minutes in fuming HNO_3 and 10 minutes in boiling HNO_3, to remove organic and non-organic species. Before oxidation, wafers were dipped in 1% HF to remove native oxide.

2.5 Oxide growth

The dielectric layer, silicon oxide (SiO_2, or 'oxide') can be manufactured in two ways: by deposition in a CVD process or via thermal oxidation. Thermal oxidation is selected as it results in a high quality oxide and can be easily performed on a large batch of wafers.

In this process ca. 2.0 μm thermal oxide is grown at 1150 °C in a wet (H_2O ambient) oxidation process for 10 hours. The oxide thickness is verified by ellipsometry using two wavelengths (632.8 and 1552 nm), and turned out to be 1945 ± 20 nm.

When a large voltage is applied at the gate electrode a leakage current may flow between the gate and substrate. In order check the oxide quality, the leakage current is measured using special test structures. Tungsten (W) dots (300 nm thick, 4 mm Ø) were sputtered on oxidized n^{++} substrates (2 μm oxide) using a shadow mask and the back of wafer was sputter coated with 200 nm platinum (Pt). Wafers were HF dipped (1%, 1 min) prior to the platinum deposition, tungsten dots were deposited after platinum sputtering. These samples were not subjected to high temperature processes.

The leakage current was measured at one spot with the back of the wafer as second electrode using an Agilent 4145 IV meter in combination with a Microtech Cascade probe station. A typical result is shown in Figure 18.

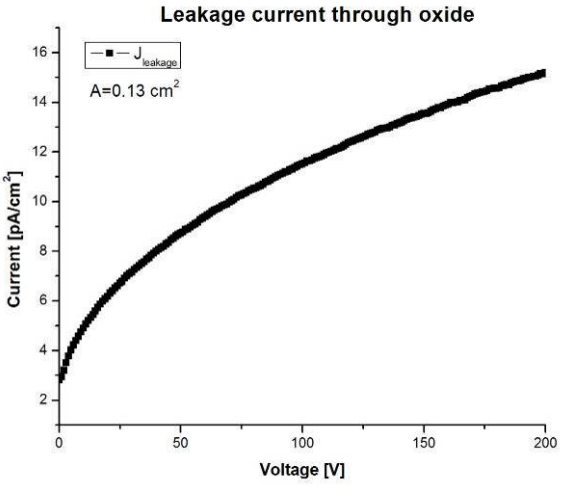


Figure 18. Leakage current (J_{GL}) through oxide (2 μm) for a typical tungsten spot (4 mm Ø).

This figure indicates that the gate leakage current (J_{GL}) is very low; in the range of pA/cm. Although no simulations were performed, the emission current is estimated in the order of mA/cm, as based on comparable designs published by Lee et. al [65]. The gate current (J_{GE}), electrons emitted from the field emitter but reaching the gate electrode and not the anode, is estimated to have the same order of magnitude. This current can be measured properly, since the gate leakage current is several orders of magnitude lower.

2.6 Gate deposition

2.6.1 Introduction

The gate electrode applies an electrical field over the field emitters for electron extractions. The engineering of this gate electrode, which appeared to be one of the most extensive jobs in this project, is discussed in this section. First the requirements on the gate metal are discussed, secondly candidate gate metals are evaluated on the basis of literature, and finally engineering experiments on two important candidates, tungsten (W) and titanium-tungsten (TiW), are discussed. These experiments focussed on adhesion related issues during high temperature processing, etching of the metals and their chemical stability during the CNT growth process.

2.6.2 Requirements on the gate metal

In order to act as an electrode in the first place, the material has to be conductive with a reasonably low resistivity to avoid voltage (IR) drops in case of a gate current. It is assumed that metal thin films with a thickness in the order of several hundreds of nm will satisfy this requirement in general.

As the FEA is be used in a gaseous environment to create reactive species in a microplasma, the cathode and gate electrode will be exposed to charged particles that might interact with them by means of adsorption, sputtering or ion implantation (see section 1.5.4). To minimize the influence of charged particles, the gate metal should be hard and mechanically strong. Furthermore, it should be mechanically stiff enough to maintain its shape after the silicon oxide is isotropically etched away (see for an example Figure 15b). Both requirements can be achieved with a thick gate electrode.

In order to fabricate the gate electrode, the material should be machinable. This means that the material should adhere properly to the layer underneath (silicon oxide) and it should be etchable afterwards to create the holes. This etch step should not stress/attack the photoresist too much, since the photoresist has to survive the oxide etch afterwards and is used in lift-off at the end of the fabrication process. This means the metal should be etchable in preferably a selective wet etchant with a reasonable etch rate in a reasonable time (few minutes). Dry etch methods are known to stress the photoresist much more and therefore less attractive. One of the reasons is that the substrate becomes heated during dry etching, as it is bombarded with plasma ions. When the etch rate is small, the gate thickness is limited by the etch time.

Finally the whole stack, - the gate metal in particular - should be compatible with the CNT growth process. This means that the metal-oxide-silicon stack (with etched structures) should survive thermal stresses induced by the high temperature during the CNT growth (see section 2.13 for detailed process information). Increasing the number of metal layers (with for instance an adhesion layer between the metal and oxide) complicates this. The typical growth temperature is 700 °C with ramp up/down speeds of 10 °C/min, starting and ending at room temperature. Apart from the temperature requirement, the metal should (largely) maintain its properties and not interact with the gases (N_2, C_2H_2 and residual gases) in the CVD reactor. Potential risks are the formation of metal-nitrides, metal-carbides, metal-oxides (residual oxygen in the system) and deposition of carbon species on the metal.

On the basis of these requirements, it is concluded that the gate thickness will be a compromise between mechanical hardness and stiffness on one hand and the (thermo-mechanical) stress at high temperatures and etch time on the other hand.

2.6.3 Comparison of different gate metal candidates

In order to get a starting point for the metal choice, different designs for CNT based GFEAs were studied in literature and summarized in Table 5. When selecting a gate material on the basis of such a table, care has to be taken, as each process is different leading to different material and fabrication choices.

Table 5. Comparison gate materials

CNTs	Gate				Oxide			Ref
Deposition method[1]	Thickness	Material	Deposition method	Etch[2]	Thickness	Etch[2]	Remarks	
	nm				nm			
T-CVD	300	W	sputtered	RIE (CF_4)	1000	BHF	Al used as hard mask	[65]
PE-CVD	150	doped poly Si		RIE (SF_6)	500	BHF	Resist as mask	[66]
T-CVD	50	Mo	evaporated	RIE	1000	RIE	Buried nickel: etched free	[1]
PE-CVD	200	Mo	evaporated	CMP	1000	HF	Self aligned process: gate after buried CNTs	[70]
MP-CVD	20	Poly Si	LPCVD	RIE	500	RIE	Resist as mask	[71]

[1] Thermal (T-CVD), Plasma Enhanced (PE-CVD) or Microwave Plasma enhanced Chemical Vapour Deposition (MW-CVD)
[2] (Buffered) Hydro Fluoric acid ((B)HF, wet), Reactive Ion Etching (RIE, dry) or Chemical Mechanical Polishing (CMP).

From this overview the following candidate gate materials are considered: molybdenum (Mo), poly silicon (poly Si), tungsten (W). Furthermore, silicon carbide (SiC) and titanium-tungsten (TiW) are investigated. Each is discussed in more detail in the following sections.

2.6.3.1 Molybdenum

Molybdenum (Mo) is a material used for Spindt type field emitters (see section 1.4.1.1) and can be deposited via sputtering or evaporation in our cleanroom. It is used by Hale [1] and Guillorn [70] as gate material for CNT based GFEAs. It was dry etched with reactive ion etching (RIE) without underetching the gate dielectric with photoresist as mask. Neither of them did lift-off afterwards: Hale deposited the catalyst sites earlier and aligned the etch mask to them to release them, Guillorn grew the vertically aligned CNTs first, covered them with oxide and metal and made gate openings by polishing back in a CMP process, making use of an increase in the topology induced by the buried CNTs.

Molybdenum can be etched in a wet etch step, molybdenum etchant (180 H_3PO_4: 11 HAc: 11 HNO_3: 150 H_2O @ 20°C) with ca. 690 nm/min (evaporated molybdenum) [68]. However, we have no experience with this etchant, neither with its selectivity with respect other materials in the device. Furthermore is the adhesion and stress of molybdenum on oxide questionable. Therefore these properties have to be tested first. Since there are other promising candidate materials as well, these are investigated first.

2.6.3.2 Silicon carbide

Silicon carbide (SiC) is generally known for being very hard and stable and for its application as high-temperature electronic material (e.g. higher frequency and power conditions than Si- or GaAs-based devices) [72]. SiC is a semiconductor with a bandgap ranging from 2.39 eV to 3.33 eV [73] and hence is has a relatively low conductivity, but this can be increased with suitable dopants [74]. SiC can be deposited using a variety of deposition methods, including chemical vapour deposition (CVD), molecular beam epitaxy (MBE) and laser ablation/pulsed laser deposition (PLD) [72].

The difficulties using SiC as gate material involve its machinability from a practical point of view. Wet etching of SiC is not feasible, as it requires molten salts (for example, NaOH-KOH at 350 °C) to be used at high temperatures, using special hard masks for patterning. The difficulty encountered in etching SiC is a result of the high bond strength, a property which makes SiC useful for high-temperature operation, but an obstacle for fabrication. For the same reason it is difficult to use sputtering or evaporation for the deposition. Nevertheless, numerous dry etch processes have been employed. Most commonly employed processes involve reactive ion etching (RIE) of SiC in fluorinated plasmas and electron cyclotron resonance (ECR) etching. Sacrificial etch masks (often composed of aluminium) are deposited and patterned using conventional photolithography to protect desired areas from being etched [75]. Because of the machinability problems, SiC is not selected as gate electrode material. Furthermore, the incorporation of a sacrificial layer further complicates the fabrication process and therefore other materials are investigated as a gate material.

2.6.3.3 Poly silicon

Poly (crystalline) silicon has been used as gate material in CMOS for many years and is used in CNT based GFEAs by Cheng [71], Pirio [66] and Teo [67]. Poly silicon is an interesting material, since it can be deposited (among other things) in a highly controlled LPCVD process. As it is part of the current CMOS process, a lot of knowledge is available about this material. As poly silicon is a semiconductor by itself, it needs to be (heavily) doped to lower the conductivity to values down to 1 mΩ-cm [76]. The doping may be incorporated during the deposition process (in situ doping) [66][68][76] but due to difficulties with this process generally, an implantation step is preferred.

Poly silicon is highly machinable and can be patterned in several ways, including isotropic silicon trilogy wet etching (126 HNO_3: 60 H_2O: 5 NH_4F @ 20 °C) [68], KOH wet etching (30% by weight @ 80 °C) [68] and numerous dry etching processes [76]. Both wet etchants are not very selective towards the underlying oxide, since they are based on HF [76]. This is not necessarily a problem, but complicates the controllability of the oxide etch afterwards as the starting conditions are not known precisely. The dry etch methods, based on reactive ion etching (RIE), allow the etching of poly silicon in both an isotropic and anisotropic way, but it is questionable whether the photoresist will be able to do lift-off afterwards. Cheng demonstrated lift-off of 7 nm iron (Fe) after an anisotropic RIE [71], etching through 20 nm poly silicon and 500 nm oxide. Pirio showed lift-off of 20 nm TiN + 3 nm nickel after dry etching through the 150 nm poly silicon gate only in an isotropical way to achieve the desired underetch [66]. He etched the oxide in BHF after the gate etch step.

The biggest disadvantages of poly silicon as gate material are its mechanical properties and its robustness against incident charged species. Although it is difficult to do a 1:1 comparison in terms of, for instance, the sputtering threshold (see section 1.4.1), the

mechanical properties of (even more robust crystalline) silicon were, apart from enhancing its electrical properties, one of the key arguments to apply coatings on silicon post emitters (section 1.4.1.3, [3]). Therefore it is concluded not to use poly silicon for the first design, but to keep it in mind as an interesting alternative.

2.6.3.4 Tungsten

Tungsten (W) is an interesting candidate as gate material because of its excellent mechanical properties. It has the highest melting point (3422 °C), lowest vapour pressure and the highest tensile strength at temperatures above 1650 ºC of all metals. Its corrosion resistance is excellent and it is only slightly attacked by most mineral acids [77]. Furthermore, it can be oxidized at temperatures above 300 °C. It forms a volatile oxide (WO_3) and the reaction is not self-limited [78]. This means that no dielectric layer will be formed on the electrode, but the tungsten thickness will decrease, leading to an increase of the gate resistance.

Tungsten dissolves very slowly in inorganic acids, but can be etched quite easily with reasonable etch rate in hydrogen peroxide (H_2O_2). This wet etch step can be accelerated by the addition of NH_4OH [78]. A typical etch mixture is 15% H_2O_2 and 1% NH_4OH in water.

Tungsten can be sputtered or evaporated with relatively low deposition rates, due to its high sputtering threshold, and it can be deposited in an LPCVD process from H_2/WF_6 chemistries [78]. When tungsten is deposited from LPCVD, there is almost no adhesion to dielectrics like silicon oxide and nitride [78]. It is known that adhesion problems are likely to occur for sputtered films and the adhesion is very sensitive to the cleaning step before the deposition [79].

Lee successfully realized CNT based GFEAs with tungsten gates after etching the gate with RIE and etching the oxide in BHF [65]. The photoresist was not used for lift-off patterning: after the oxide etch an aluminium (Al) sacrificial layer was deposited in a special evaporation run where the substrate was rotated on an axis perpendicular to the source to avoid the deposition of aluminium in the etched structures. The nickel (Ni) catalyst was deposited at normal incidence afterwards and finally the undesired nickel was dissolved together with the aluminium [65].

Disadvantages of tungsten include its adhesion to the oxide as well as the stress in the layer. It has to be denoted these disadvantages became clear during experiments described in section 2.6.4.1.

Because of its excellent mechanical properties and the relative easy wet etch step possibility, tungsten is a very promising candidate gate material in CNT based GFEAs.

2.6.3.5 Titanium-tungsten

Titanium-tungsten (TiW) as an alloy of 90% tungsten (W) and 10% titanium (Ti) (by atoms, equals 97% / 3% by weight) has frequently been used in microtechnology as a diffusion barrier between silicon and metal interconnects since 1969 [80][81]. This alloy has good adhesion and barrier properties: it combines beneficial properties of both elements: tungsten has a large mass, high bonding strength and is stable with aluminium (Al) and silicon (Si) up to 400 °C, making it a diffusion barrier, while titanium overcomes the adhesion problems with oxide [79]. The correct W/Ti ratio of 90/10 (at.%) is just above the solubility limit of titanium in tungsten, ensuring a stable alloy at higher temperatures [81]. TiW is often used as adhesion layer between tungsten and oxide, due to its excellent adhesion properties [78]. Furthermore, it has generally the same properties as pure tungsten,

including its chemical stability: the titanium is really 'confined' in the tungsten, making the alloy stable in for instance HF etching [79] (titanium etches very quickly in HF [68]). Principally speaking, it can be etched in the same etch solutions as tungsten with comparable etch rates (few microns/hour [78]), including H_2O_2 and H_2O_2 + NH_4OH mixtures [79].

No literature is found in which TiW is demonstrated successfully as a gate material. Its high temperature stability is not found in literature, but appears to be promising as it is expected to be comparable to pure tungsten.

Because of its excellent adhesion properties and the stability of tungsten, TiW is a very interesting candidate gate metal in CNT based GFEAs.

2.6.3.6 Conclusion

On the basis of this review, a gate material is selected. Molybdenum (Mo) is not chosen because the lack of knowledge about its machinability, adhesion and stress. Silicon carbide (SiC) is not chosen because of its poor electrical properties and the complicated machinability. Poly silicon is not selected because its robustness against charged species of the plasma is questionable and it needs to be etched in a dry etch step preferably. Nevertheless, poly silicon remains an interesting option.

Tungsten is selected as gate material because of its excellent mechanical properties, its machinability (etchable in a simple wet etchant), and the fact that a similar device was successfully realised in literature [65]. As the adhesion to oxide, as-deposited and after the etching and high temperature CNT growth, the etching in the proposed wet etchants, as well as its chemical stability during the CNT growth process are not fully known yet, these are all tested and discussed in section 2.6.4.

TiW appears to be the best candidate gate metal, as it appears to have mechanical and chemical properties comparable to (pure) tungsten, but to have better adhesion. Similar to tungsten, the adhesion to oxide, etching and chemical stability during the CNT growth process are not fully known yet, these are all tested and discussed in section 2.6.5.

One might wonder why TiW is not selected in the first place. The truth orders to say tungsten was selected in the first place, experiments were carried out and these results triggered the investigation of TiW as gate material. Before the experiments with tungsten, TiW was not taken into consideration; the successful fabrication of CNT based GFEAs with tungsten gates and the CNTs grown in a comparable thermal (!) CVD process with similar thermal budget. Since these experiments with tungsten yielded useful information, they are discussed in 2.6.4. Next TiW appeared to be the best gate electrode material; therefore experiments were carried out and discussed in more detail in section 2.6.5.

2.6.4 Experiments with tungsten gates

Tungsten is investigated as gate material and the adhesion to oxide, as-deposited and after the etching and high temperature CNT growth, the etching in H_2O_2, as well as its chemical stability during the CNT growth process were not fully known and are therefore all tested. The chemical stability of tungsten layer during the CNT growth process is not discussed in this section, but in section 2.13 together with the other CNT growth experiments.

2.6.4.1 Deposition

Tungsten (W) can be deposited with different equipment in our cleanroom, including sputtering in 'Sputterke' and e-beam evaporation in the 'BAK600'. Sputtering was preferred over evaporation as the deposition takes much less time (45 minutes) for a 300 nm layer on a single wafer than evaporation in the BAK600 (3 hours). However, in the BAK600 it is possible to deposit the same layer on 16 substrates simultaneously, while Sputterke can handle only one wafer at the time. This makes the BAK600 more suitable for batch processing, while Sputterke is more suitable for small volume testing. Furthermore it is suggested that the adhesion is better in a sputtering system where the metal particles arrive at the substrate with more energy. Therefore Sputterke is selected as deposition equipment for tungsten layer testing.

In general, tungsten layers were deposited under standard conditions unless mentioned differently: a sputtering power of 170 W and a chamber pressure 6.6×10^{-3} mBar (argon), taking 38 min for a 300 nm layer.

2.6.4.2 Adhesion

2.6.4.2.1 Without adhesion layer

Thin films of 300 nm thickness were deposited on oxidized (2 μm) wafers. This thickness is chosen because it is 'thick' for micromachining understandings (and 'thick' thin films are desirable to increase its robustness against incident charged species), but still shown in literature to work in realised devices [65]. Thick layers are known for their stress problems.

The wafers used in these experiments were not the same as used in the process flow described in section 2.3. The samples were stripped from oxide at the backside directly after oxidation. To protect the front side of the wafer, it was covered with 3.5 μm photoresist (Olin 907-35 spun @ 4000 RPM, no exposure) and had a 30 min post bake at 120 °C prior to the oxide etch. Oxide was etched in (the standard) BHF (1:7) for ca 33 min until the back of the wafer became hydrophobic. A bare dummy wafer was used as a reference for the end point determination. After rinsing in DI water the resist was stripped in (the standard) resist strip of 100% fuming HNO_3 for 10 minutes. No extra cleaning was performed afterwards, apart from an HF dip (1%, 1 min) just before the metal depositions. After the HF dip, the back of the wafers was sputtered with 200 nm platinum (Pt), followed by 300 nm tungsten (W) on the topside.

A batch of 8 of these wafers remained in a waferbox in the cleanroom for 3 weeks without any signs of metal degradation or adhesion problems.

After 3 weeks cracks occurred in the unpatterned wafer and these cracks were enhanced by a short bake (60 s) at 95 °C. After a short rinse in DI water, half of the tungsten layer was released. These effects were observed on more than half of the wafer batch. A typical picture showing these characteristic cracks is shown in Figure 19. The shape of the cracks upwards pushing the film suggests that the stress is compressive.

Similar effects were observed in circular shaped tungsten spots (Ø 4 mm), deposited under the same conditions on silicon oxide using a stainless steel shadow mask (Figure 20). As there was a small gap between the shadow mask and substrate, the resulting dots had a gradient in the thickness near and towards the edge. These effects occurred on half of the spots.

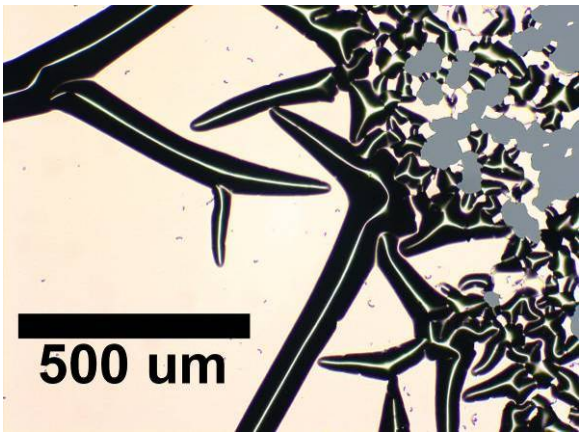


Figure 19. Cracks in a 300 nm tungsten layer deposited on oxide after 3 weeks of storage.

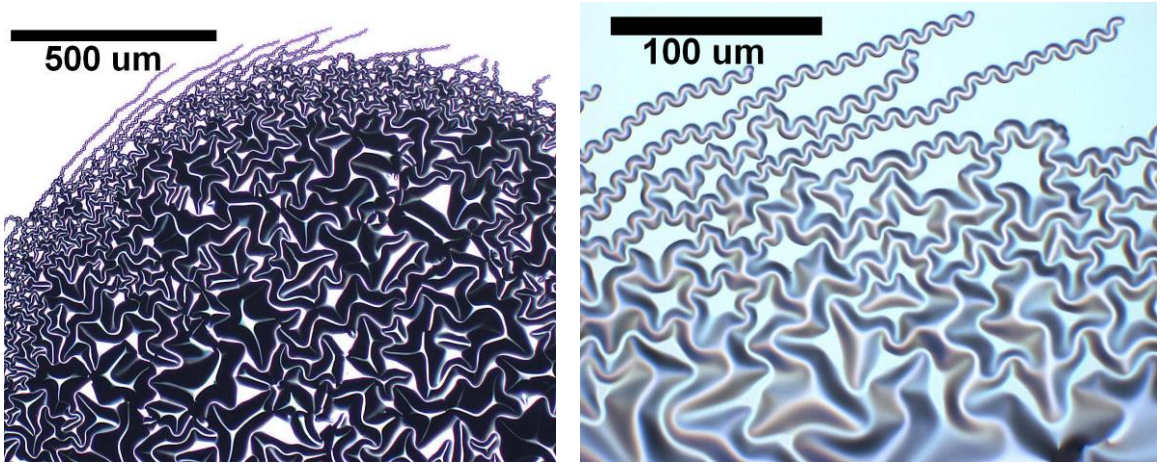


Figure 20. Cracks in a 300 nm tungsten dot (Ø 4 mm) deposited on oxide using a shadow mask.

2.6.4.2.2 With adhesion layer

The above mentioned stress problems triggered the investigation of an adhesion layer between the tungsten (W) and silicon oxide. As both the adhesion and the metal layer have to be deposited in the same vacuum chamber to avoid oxidation of the adhesion layer (in air), the choice of the adhesion layer is limited to the available materials. As this layer has to be etched later in the process, preferably a metal is to be used that is easy to etch in wet etchant. Furthermore, this adhesion layer should be stable up to 700 °C with tungsten and oxide. Several candidate metals, including chromium (Cr), titanium (Ti), tantalum (Ta) and titanium-tungsten (TiW) were considered. As TiW could not be deposited in the same sputtering system (at that time), tantalum was selected for its high temperature stability and it has proven to be a successful adhesion layer between platinum (Pt) and silicon nitride (Si_3N_4) at elevated temperatures [69].

Samples with 10 nm tantalum and 300 nm tungsten were prepared. As the stress in metal thin films is related to the film thickness, a wafer with only a thinner layer tungsten (100 nm) was made as well.

In order to test the adhesion after the stresses induced by the high temperature CNT growth process, sample were exposed to an anneal at 700 °C in N_2 ambient. As the CNT growth system was only scarcely available and it could handle two 1 × 1 cm samples only during one run (taking half a day), samples were loaded in the general purpose (tube) furnace (E1) in our cleanroom to 'mimic' the CNT growth process. In this system the samples were loaded at 400 °C, heated up to 700 °C for one hour with ramp up/down speeds of 10 °C/min. The ambient was flushing N_2 at a flow rate of 4 slm. This system is only an (but the best available) approximation of the real CNT growth process, where samples are loaded at room temperature under flushing N_2 conditions, with ramp up/down speeds of 5 °C/min (see section 2.13 for more details).

The results of both samples were dramatic. The 100 nm tungsten layer came off dramatically during the anneal, leaving a blank oxide wafer, while the 10 nm Ta / 300 nm W layer flaked after shaking the waferbox for a few seconds, leaving a greenish underlayer, (see Figure 21). This layer is most likely tantalum oxide (Ta_2O_5), which is formed in oxygen containing ambient at temperatures > 250-300 ºC [82]. This suggests oxygen or H_2O is present in the cleanroom E1 tube, which is discussed in more detail in section 2.6.5.2.

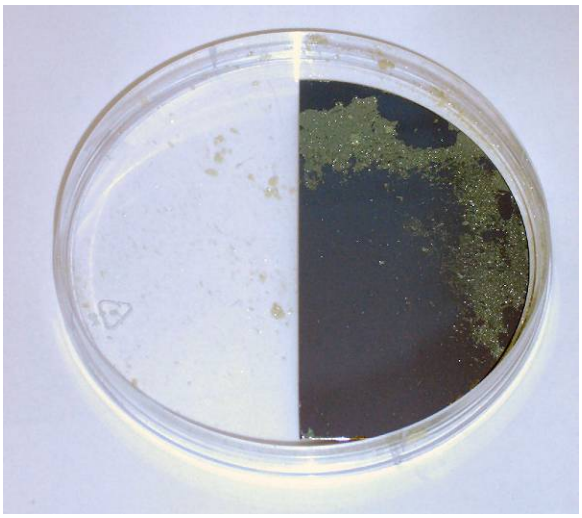


Figure 21. 10 nm tantalum + 300 nm tungsten on oxide after a 1 hour anneal at 700 °C in cleanroom furnace E1.

These experiments triggered the investigation of TiW as a gate metal. Whereas TiW was ignored as adhesion layer, because it could not be deposited in the same vacuum system as TiW without breaking the vacuum, it can be used without tungsten on top: using a 300 nm layer of only TiW as gate metal. These experiments are described in section 2.6.5.

2.6.5 Experiments with TiW gates

2.6.5.1 Deposition

Titanium-tungsten (TiW) (20/80 at.%) can be deposited in the Oxford PL400 sputtering system. Apart from TiW, this system is capable of sputtering aluminium (Al) only, both from 'big, massive' targets. Standard deposition conditions are a sputtering power of 500 W, and 10 mTorr (ca 7.5×10^{-3} mBar) base pressure (Argon), taking 6:27 min for 300 nm TiW.

As it is not trivial whether the sputtered films have the same composition as the sputtering target (different mobility of Ti and W), Rutherford backscattering (RBS) analysis was carried out, revealing a TiW composition of 14/86 at.%.

Near the end of the project a new 2" TiW target (30:70 at.%) arrived for use in sputtering system 'Sputterke', enabling the possibility of using TiW as adhesion layer between silicon oxide and tungsten (W). Standard deposition conditions are a sputtering power of 200 W and 6.6×10^{-3} mBar base pressure (Argon), taking 25 min for 250 nm TiW (10 nm/min).

The composition of TiW layer is verified by RBS, revealing a Ti:W ratio of 24:76 at.%. This is slightly less than the target composition, most likely due to the scattering of titanium (m = 48 amu) and argon (m = 40 amu) during the sputtering process [79].

As major stress problems occurred with tungsten layers and the fact that stress problems are worse with increasing layer thickness, it was decided not to use a thin (10 nm) TiW adhesion layer together with a thick (300 nm) tungsten layer, but to use a thicker (150 or 250 nm) TiW layer (which has shown its high temperature stability (see section 2.6.5.2)), covered with a thinner (50 nm) tungsten layer. These samples were incorporated in the main process and used in CNT growth experiments (see section 2.13).

2.6.5.2 Adhesion

In order to test the adhesion of TiW (Oxford PL400), as a function of the cleaning prior to the deposition, the following experiment was carried out.

Oxidized wafers (2 μm thermal oxide on both wafer sides) were used as substrates. The cleaning was varied, including 'no cleaning' (after oxidation and one day storage), the standard cleaning (see section 2.4 for details) as well as a combination of the standard cleaning with a final HF-dip+. In this HF-dip+, wafers are cleaned in a solution of 0.3% HF + isopropanol (IPA) (65:1) for 1 minute. This cleaning solution is known to promote the adhesion of CVD $W_xC_yN_{1-x-y}$ layers, a process very sensitive towards its initial cleaning [83].

Layers were deposited in two thicknesses (100 and 300 nm) to test whether thin films would have less stress and adhesion problems. All samples are summarized in Table 6.

The possibility to clean the wafers by exposing them to the argon plasma before deposition was considered, the surface is slightly sputtered by the argon plasma, increasing its roughness and removing any adsorbed species. This technique is known to be promote the adhesion of platinum on silicon nitride (Si_3N_4) [69][84], but was not carried out due to technical problems with the deposition equipment.

Table 6. Substrate cleaning and TiW deposition experiments

Wafer ID	Cleaning	TiW thickness
1)	None	300 nm
2)	None	100 nm
3)	Standard cleaning	300 nm
4)	Standard Cleaning	100 nm
5)	Standard Cleaning + HF-dip+[1]	300 nm
6)	Standard Cleaning + HF-dip+[1]	100 nm

[1] HF-dip+: 0.3 % HF: isopropanol (65:1), see text for details

After deposition, samples were exposed to a 700 °C anneal in N_2 in the cleanroom E1 tube furnace to mimic the CNT growth process, as discussed in more detail in section 2.6.4.2.2. The macroscopic adhesion of as-deposited and post anneal samples was tested using the scotch tape test [85].

All samples passed the test, showing the excellent adhesion properties of TiW on silicon oxide [78]. However, all samples showed a major colour change: from metal to all colours of the rainbow. The discolouration is related to the wafer geometry (quarter 4" wafer), indicating a correlation to the gas flow in the furnace. Typical samples are shown in Figure 22.

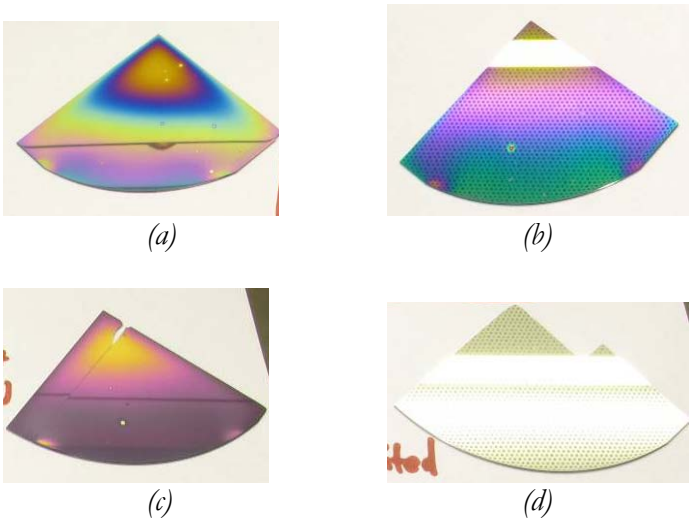


Figure 22. Discolouration of various samples after a 700°C anneal in cleanroom tube furnace E1 together with an as-deposited sample.
(a) 300 nm TiW (annealed)
(b) 100 nm TiW (annealed)
(c) 10 nm Ti + 300 nm W (annealed)
(d) 300 nm TiW (as-deposited)
Note that any 'structure' on the samples is due to reflections of the environment.

In the same experiment, extra samples of 300 or 100 nm tungsten with 10 nm titanium as adhesion layer (sputtered, on oxide) were annealed, showing the same behaviour as observed for TiW samples: proper tungsten adhesion but discolouration.

In order to get an indication of the electrical properties of the annealed TiW samples (the discolouration is not necessarily harmful if conduction is not changed dramatically), the resistivity was determined using a four probe measurement system in combination with a TTi BS 407 precision milliohm meter. The sheet resistance ($R_{\square}$ in units of ohm/square ($\Omega/\square$)) is calculated from the measured resistance (R_m) by a multiplication with a factor $\pi/\ln(2)$. The resistivity (ϱ in units of ohm cm (Ωcm)) is defined as $R_{\square}/t$ with t the layer thickness in cm. The values of ϱ for W and TiW are 27 and 60 $\mu\Omega$cm respectively [80].

The results are summarized in Table 7. Values are averages of 4 measurements across the sample. As the resistivity is related to the colour pattern, the values are an indication only.

Table 7. Sheet resistance for various TiW layers before and after a 700 °C anneal in N_2

Sample	As-deposited			Post anneal		
Standard cleaning only	R_m [Ω]	$R\square$[Ω/□]	ρ [μΩcm]	R_m [Ω]	$R\square$[Ω/□]	ρ [μΩcm]
300 nm TiW	0,246	1,12	34,0	0,49	2,20	66,0
100 nm TiW	0,739	3,35	34,0	3,83	17,3	173

It is shown that the resistivity increases significantly (by a factor 2 for 300 nm TiW and by a factor 5 for 100 nm TiW), indicating that a poor conducting species (most likely TiO_2) is formed during the discolouration process, consuming the TiW partly.

A possible explanation is the oxidation of Ti as it is very reactive and might diffuse towards the surface (both TiW and 10/300 nm Ti/W samples) at 700 °C. Although the anneal is carried out under 'flushing nitrogen conditions', oxygen might be part of the ambient as the nitrogen has a limited purity. A purity of 99.9999 still yields a partial pressure of oxygen in the 10^{-2} Torr range (10^{-5} bar) at atmospheric pressure, the working pressure for LPCVD systems [76]. This is enough to oxidize several monolayers of Ti per minute at these temperatures [79].

Furthermore, the samples were loaded in the furnace at 400 °C without an over pressure in de tube furnace, allowing oxygen from the air to diffuse into the furnace during loading of the samples. It is checked whether the discolouration was due to the loading only: samples were placed in the furnace at the loading temperature of 400 °C for a few minutes (with the end cap on) and subsequently removed: no discolouration occurred.

In order to determine the composition of the coloured species, X-ray induced photoelectron spectroscopy (XPS) was carried out on both annealed and as-deposited samples. However, from these results (not shown), no conclusions could be drawn regarding the composition of the coloured species. With this technique, only the composition of the top 5-10 nm is examined. Apparently, no difference is observed in this top layer, indicating that a more thorough examination is needed, for instance by means of an XPS depth profile, to get this information. This is not done, because time constraints and the relative unimportance of this subject.

2.7 Lithography

The lithography in this process yielded two major challenges: the resolution (making well-defined 2 µm structures) and the stability of the photoresist during the metal and oxide etch combined with the final lift-off process step. These issues are discussed in section 2.7.2 and 2.7.3 respectively. First the mask design is discussed in section 2.7.1.

2.7.1 Mask design

For this process, only a single mask is used to define the gate holes. Apart from this function, the mask contains several other structures, used for the characterisation of the devices and 'tools' used during the process, to tune for instance the lithography. In this section the mask is discussed in more detail.

2.7.1.1 Overview

A 4" wafer is divided into 45 stand-alone devices, hereafter referred to as dies. The wafers consists of 4 different types of dies, all are individually numbered and shown in Figure 23. The different dies are discussed in more detail in this section.

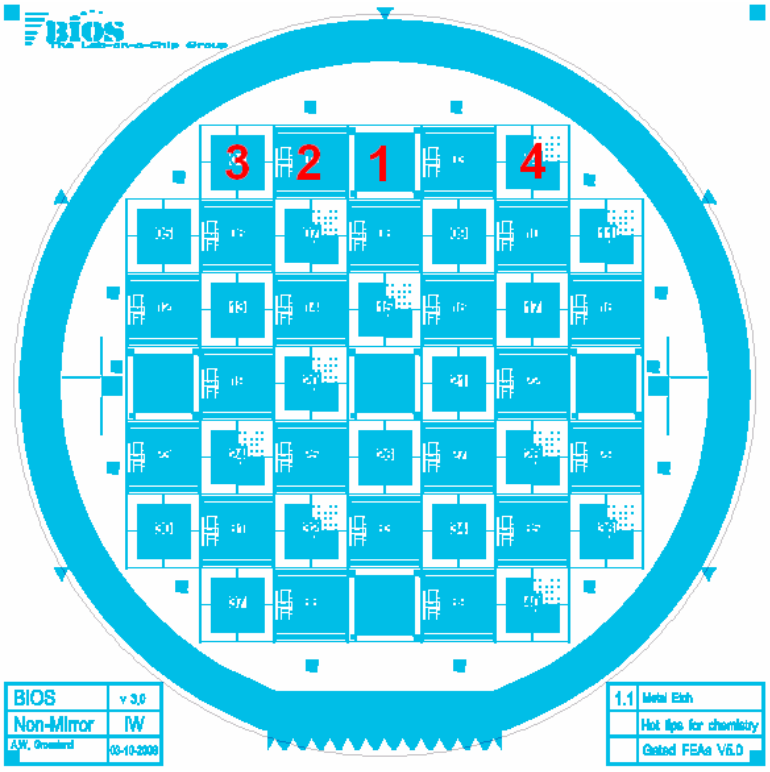


Figure 23. Overview of the mask used in this project. Four different dies are distinguished, including the 'SiO_2 underetch test die' (1), the 'cross-section test die' (2) and two versions of the 'Gated field emitter die' (3,4).

2.7.1.2 'SiO$_2$ etch underetch test die'

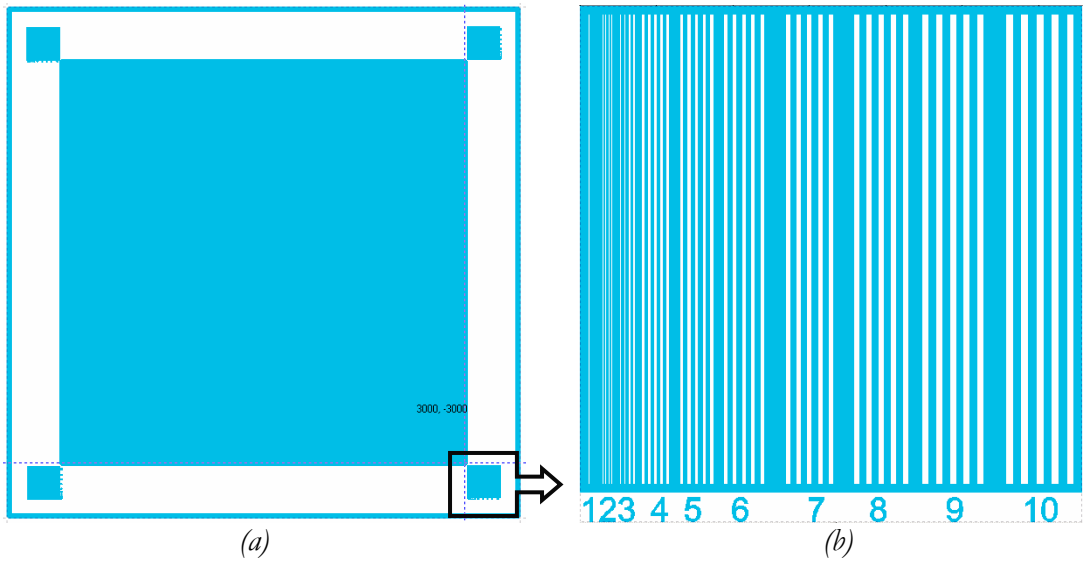


Figure 24. *(a)* The 'SiO$_2$ underetch test die', consisting of an (1:1) array of 2 μm lines spaced at 2 μm. *(b)* Extra test structure of similar composition, with line and spacing widths ranging from 1…10 μm.

The die consists of an array of 2 μm lines spaced at 2 μm (1:1 line pattern). These lines will fall off during the SiO$_2$ etch (i.e. resulting in a colour change) indicating the desired underetch of 2 μm is achieved. At the corners a group of four other test structures is placed with similar composition, line widths range from 1-10 μm. These are used to tune the lithography (exposure & development times) as well. These test structures are placed around the dies to have more of them in case a wafer is divided into smaller pieces during etch tests.

2.7.1.3 Cross-section test die

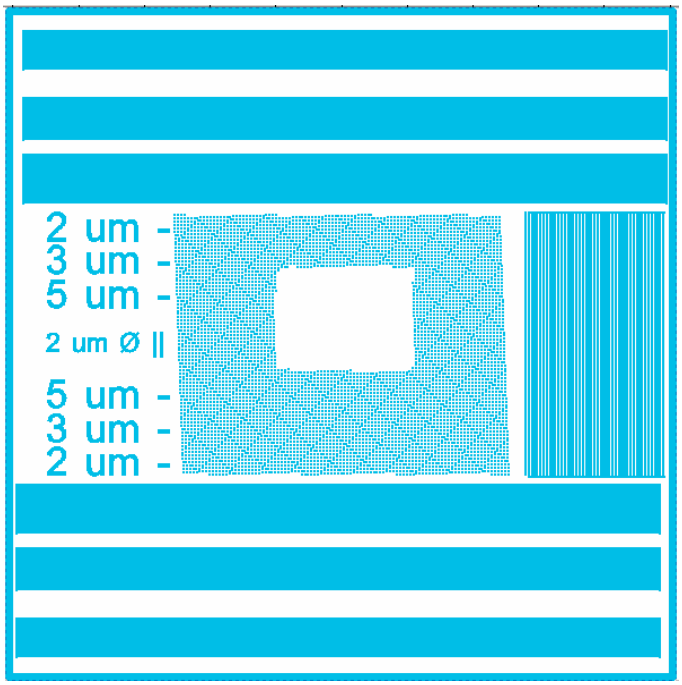


Figure 25. The 'cross-section test die', consisting of an array of 2, 3 and 5 μm lines (all spaced 10 μm) together with a large tilted array of 2 μm dots. Cuts perpendicular to the lines yield cross-sections for the inspection of etch profiles and CNT growth.

This die consists of arrays of 2, 3 and 5 μm lines (all spaced at 10 μm). When this die is cut perpendicular to the lines, the etch profiles as well as the CNT growth in the etched structures can be examined at the resulting interface. During one CNT growth run, one GFEA die is placed in the reactor, together with one cross-section die that can is used for SEM characterization afterwards. As it is difficult to cut through a single 2 μm dot, a large array of 2 μm dots is placed in the centre of the die. The array is tilted by 2 degrees with respect to the line arrays: a cut perpendicular to the lines should cleave always 2 dots. On the right and extra array of 2 μm lines is placed for cuts in the other direction.

2.7.1.4 Gated Field Emitter arrays

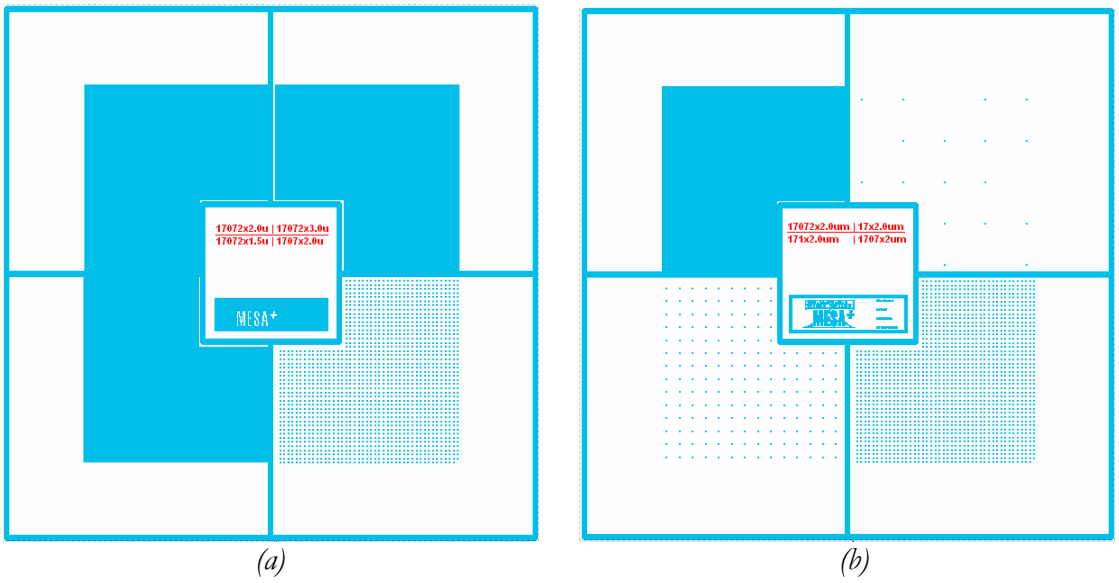


Figure 26. The gated field emitter arrays (GFEAs): the '3 hole sizes' die *(a)* and the 'four orders of magnitude' die *(b)*. The exact number of holes and their diameter is shown in the comments in the die centre.

These dies are the actual gated field emitter arrays. Both dies consist of four sections; each of them is a large area with many holes (or dots). These sections are meant to be operated individually in field emission experiments.

The '3 hole sizes' die (black centre section around MESA+ logo) consists of 17072 dots of 2.0, 3.0 and 1.5 μm diameter and 1707 dots of 2.0 μm. The section layout is depicted in the comments in the centre of the die. It is expected this die will provide information about the influence of the hole size on the CNT growth and their field emission properties.

The number of field emission devices per section was rather free to choose. As it was almost impossible to simulate the field emission behaviour of these devices with these particular CNTs (due to the lack of information about the correct simulation parameters), the number of devices per section was estimated on the basis of experimental results published by Lee [65] with GFEAs of similar composition: metal gate arrays with thermal CVD CNTs (see 2.2, Figure 15b). Lee made devices, emitting 2.5 μA with 45 V and 3600 tips, leading to an average of 0.7 nA/tip. These devices were meant to be test in an UHV system (see section 3.1) in which comparable field emission experiments were carried out on AFM tip arrays. These arrays were used to estimate suitable emission currents. The noise in these experiments was typically 40 pA with measurement currents in the order of 100-300 pA. The proposed measurement equipment was the Keithley 2425 source meter, with a measurement range of 1.05A at 21 V, and 21 mA at 1100 V. The worst case scenario was a bias voltage of 1100 V, allowing a maximum measurement current of 21 mA. Assuming 0.7 nA/tip, the maximum array size would be 30×10^6 tips in parallel (array of 5477 × 5477 tips).

As different gate hole sizes were meant to be tested, it was desirable to space the gate holes at a decent spacing, to keep the overall behaviour of the gate electrode roughly the same. Therefore, all gate holes were spaced at a 25 μm pitch in the largest arrays. As the dies need to be handled with tweezers afterwards, no device was placed closer than 2 mm from the die edge. In the area left, as many devices as possible were placed, being 17072 gate holes in total per section. On the basis of [65], emission currents in the order of μA's were expected, currents that could be measured without too many complications. This current range is an order of magnitude above the expected noise level and well within the measurement range of the proposed equipment.

The 'four orders of magnitude' die (white centre section around MESA+ logo) consists of 2.0 μm diameter holes of in arrays of 17072, 1707, 171 and 17 respectively. Section layout is depicted in the comments in the centre of the die. It is expected that this die should provide information about how the field emission properties scale with the number of devices. Furthermore it provides freedom during the measurement of the field emission current: the optimal measurement current magnitude for the measurement instruments can be chosen.

2.7.2 Resolution issues

The lithography is a complicated process influenced by many parameters and making 2 μm structures is near the limit of what is can be made in a reproducible way in our cleanroom.

In the following sections, experiments are described that were carried out to tune the photolithography. Experiments included the test of extra thin photoresist and the variation of exposure times.

2.7.2.1 Thin photoresist

In the cleanroom, 3 types of standard positive resist are available in the Olin-907 series, with thicknesses of 1.2, 1.7 and 3.5 μm (in case they are spun at 4000 RPM for 20 s). Standard, the thinnest of this series is used, being Olin 907-12. The resist can be made thinner by spinning at a higher velocity, at maximum 6000 RPM.

This is tested and samples were prepared with in a standard lithography process (see

Appendix A: Complete process flow) with Olin-907-12 spun at 4000 and 6000 RPM. A typical result is shown in Figure 27.

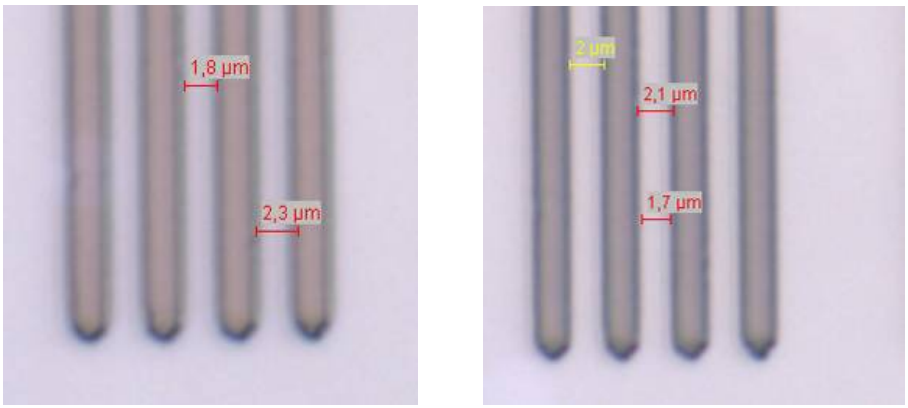


Figure 27. Resolution test with Olin 907-12 photoresist, spun at 4000 *(a)* and 6000 *(b)* RPM. Structures are 2 µm lines, with 2 µm spacing. Pictures taken with optical microscope at a magnification of 80000×.

It is observed that the 'half pipe' resist edge is less for the 6000 RPM sample and the lines are better defined. The lines of the 4000 RPM sample are smaller than the desired 2.0 µm, the lines of the 6000 RPM sample are closer to 2 µm.

The resist spun at 6000 RPM however showed instabilities during the oxide etch and came off. The 4000 RPM sample showed no adhesion problems and was used further in this project.

2.7.2.2 Various exposure times

In order to test the influence of the exposure time on the resist structures, one metallised wafer with Olin 907-12 (4000 RPM) was exposed to different exposure times on different locations of the wafer using pie-shaped tool on the Karl Süss aligner with 9 mW/cm^2 in a standard lithography process. After development, the top and bottom diameter of 2 µm lines and 2 µm (Ø) dots in the photoresist was determined using an optical microscope at a magnification of 80000× (see Figure 27) in top view. The results are summarized in Figure 28.

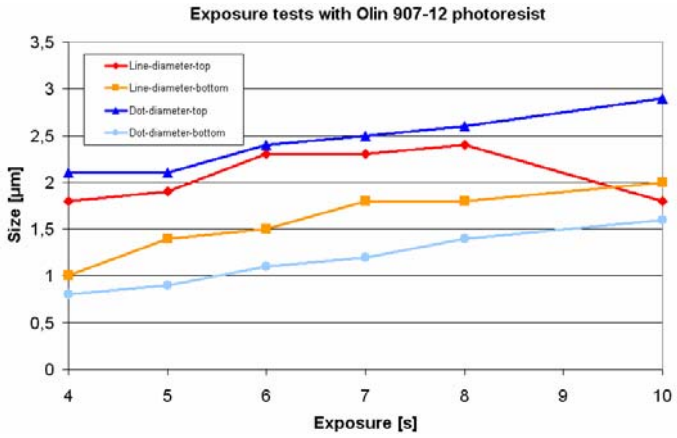


Figure 28. Exposure tests with Olin 907-12 photoresist. Note that lines are a guidance for the eye only.

On the basis of these results it appears 10 s is the optimal exposure time for lines, whereas even longer exposure times seem necessary for dots. However, the method for the determination of the diameters appeared to be rather inaccurate, as it is near the limit of the optical microscope. Ideally an examination of cross-sections with the SEM would be preferred, but this analysis is omitted because of time constraints.

Furthermore, in other experiments (not shown) a slight underetch of the metal was observed, compensating for the smaller photoresist aperture. Therefore 5.0 s was used and found to yield more or less 2 μm gate holes (see section 2.13).

2.7.3 Adhesion of the photoresist during etching

A second issue in the photolithographic process is the adhesion of the photoresist to the surface it is deposited on, especially during the subsequent etch steps. Therefore several tests were carried out.

During metal etch experiments, in which tungsten (W) was etched in 31% H_2O_2, it was found that photoresist (Olin 907-12) shows adhesion problems after ca. 30 min of etching (see section 2.9.2.1). These wafers had no special clean prior to resist spinning.

Etching the same wafers in 15% H_2O_2 and 1% NH_4OH for 6 minutes yielded no resist adhesion problems.

Although no resolution problems were observed on etched structures (only in resist), the influence of the O_3 treatment on the lithographic process was tested. Metallised wafers with Olin 907-12 (4000 RPM) were prepared in a standard lithography process, with no extra cleaning before. After the final hard bake (20 min @ 120 °C), selected samples were exposed to an O_3 treatment for 300 s with the special UV furnace in the cleanroom. All samples were etched in 31% H_2O_2 or 15% H_2O_2 and 1% NH_4OH for 6 min, and it was shown both samples with the O_3 treatment showed dramatic resist adhesion problems. Therefore it was concluded not the use the O_3 treatment (and accept possible resolution problems). Furthermore the acetone and IPA rinse prior to the lithographic process (before the dehydration bake) was introduced to gain extra cleaning.

Lift-off with photoresist is usually done in a photolithographic process without the final hard bake of 20 minutes at 120 °C. The resist remains softer, enhancing the lift-off process. As the final hard bake was necessary for the resist stability during the wet etch steps, lift-off was not guaranteed. Usually, lift-off is enhanced by placing the whole vessel with lift-off solution and sample in an ultrasonic bath.

In order to test lift-off after the final hard bake, wafers with Olin 907-12 were prepared in a standard lithography process, finished with a 20 min hard bake at 120 °C. Several metal layers (Ni, Ti+Ni, Ta+Ni) of 10-20 nm were deposited by evaporation and lift-off was done in acetone for 5 minutes, enhanced in an ultrasonic bath. A typical result of a 10 nm nickel layer is shown in Figure 29.

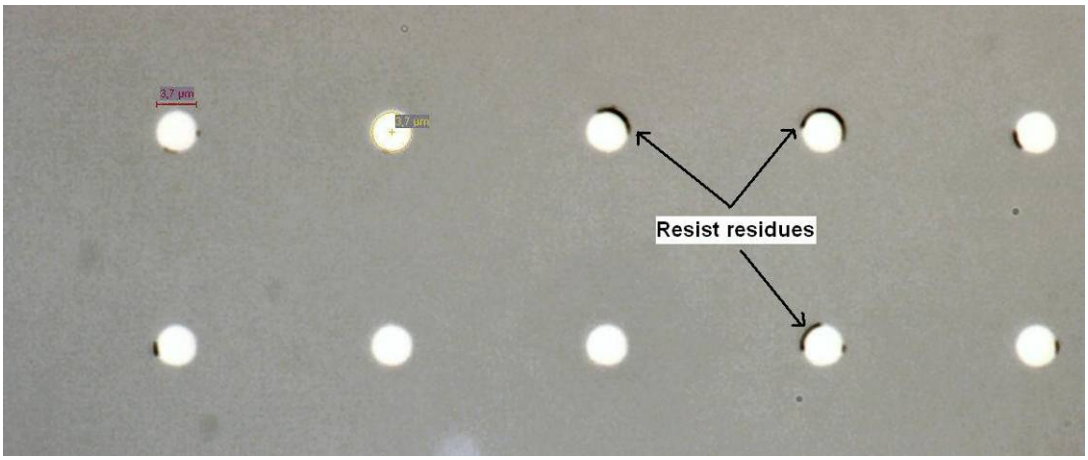


Figure 29. Nickel dots (10 nm, Ø 4 μm) deposited on silicon by evaporation using Olin-907-12 as photoresist for lift-off with the final 20 min post bake at 120 °C. Small amounts of resist residue are observed on the edge of the dots.

It was found that the photoresist showed lift-off, but small resist residues remained at the edge of the nickel dots. This is due to the tapering of the photoresist at the edge of the photoresist. These thinner parts are likely to tear off during the lift-off process and remain on the surface. This can be solved with special lift-off resists where the 'half-pipe' is reverse: upside down, so-called 'image reversal resist'. This is not done as this prompts a check of the compatibility of the new photoresist with the rest of the process including completely different exposure characteristics (and even mask redesign), consuming too much time in the limited time frame available for this project. It was chosen do lift-off for longer times, trying to remove the resist residues after all.

2.8 Dicing

Wafers are diced halfway the process for half the wafer depth. This is done before etching the cups, to avoid any silicon sawdust to be precipitated in the cups and wafers can be processed afterwards in the cleanroom without special aids. After the final lift-off, selected dies can be removed easily, by breaking the wafer along the dicing lines.

When the wafers are diced, they are thoroughly rinsed with and stored in DI water to avoid the precipitation of saw dust on the wafers. Before further processing, wafers are ultrasonically cleaned in DI water for 30 minutes to remove the sawdust.

In order to find the optimal dicing depth, several saw depths were tested, including 100, 150, 200 and 250 μm.

The wafer diced up to a depth of 250 μm was not stable enough for handling afterwards, the 200 μm wafers were used in the final process but during post processing several wafers broke spontaneously (during 'regular' wafer handling). Wafers diced at 100 μm and 150 μm were quite difficult to break, but after the experience with 200 μm wafers, 150 μm is concluded to be the optimal dicing depth.

2.9 Metal gate etch

In this section the etching of tungsten and TiW is discussed, in sections 2.9.1 and 2.9.2 respectively.

2.9.1 Etching tungsten

Before the stress problems occurred with (see section 2.6.4.2.1), some etch tests were carried out successfully on 300 nm tungsten on oxide samples. These samples had a metallization of 200 nm platinum (Pt) on the back of the wafer.

A standard lithography process based on Olin 907-12 resist was used as mask, finishing with a 20 min post bake.

Samples were etched successfully in 31% H_2O_2, directly from cleanroom cupboard storage. The end point was determined visually by a colour change: metal (grey) to oxide (green/purple). The etch rate was 85 nm/min. During the etch, a violent reaction occurred at the platinum side of the wafer, causing strong bubble formation, most likely the dissociation of H_2O_2 to H_2O and H_2. This might have heated the wafer and possibly increased the etch rate during the etching process.

2.9.2 Etching TiW

2.9.2.1 Etching in H_2O_2

In order to test the etching of TiW in H_2O_2, samples were etched for different times and examined afterwards with the high-resolution scanning electron microscope (HR-SEM). Oxidized samples with a 300 nm TiW layer on top (no platinum back electrode) were patterned in a standard lithography process based on Olin-907-12 and etched in the same solution of 31% H_2O_2 for 8/12/16/20/30/40 min (one sample taken out at the time).

After etching, samples were rinsed in DI-water and cross sections were made for examination in the HR-SEM. The results are shown in Figure 30.

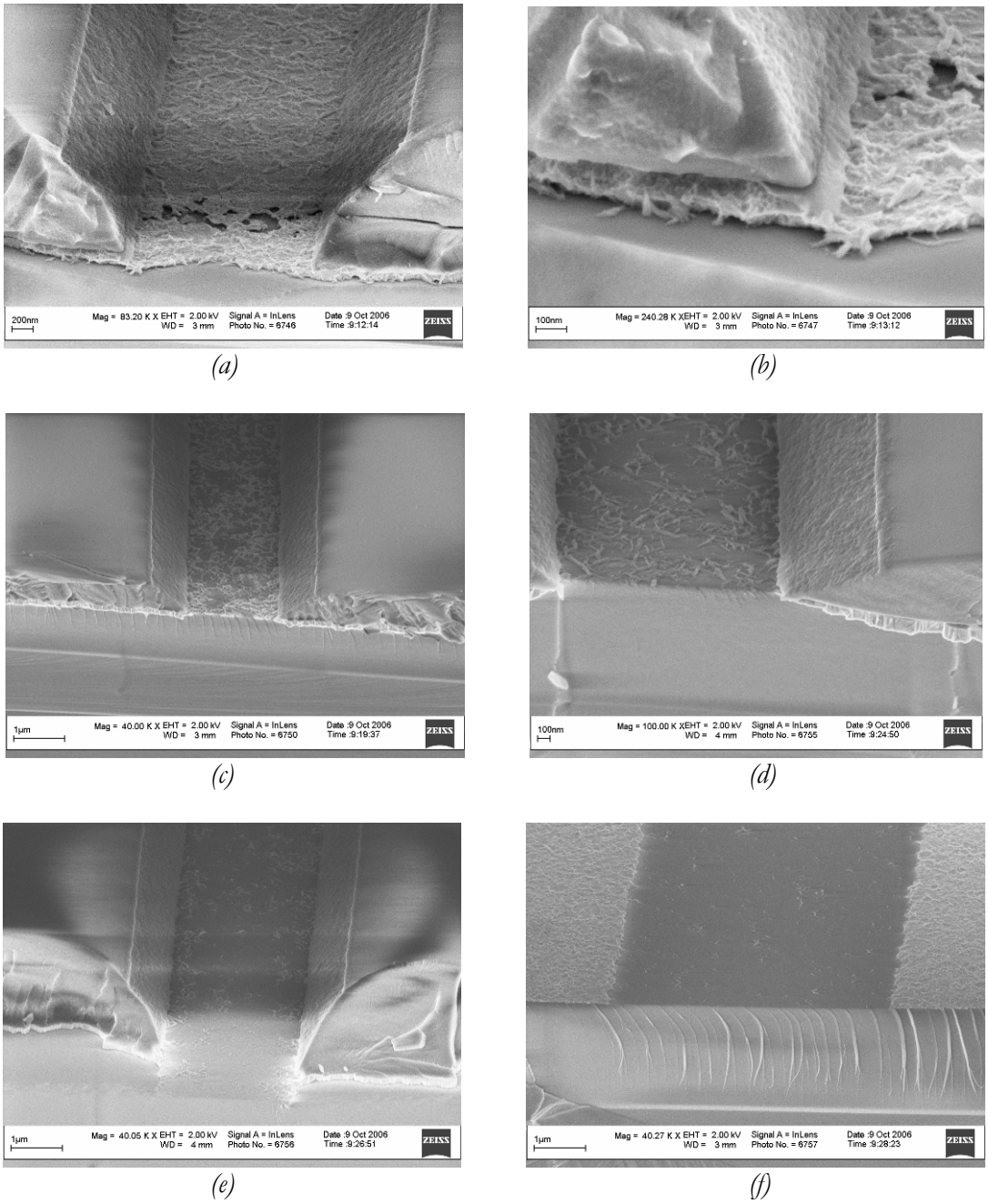


Figure 30. HR-SEM images of etching of 300 nm TiW in 31% H_2O_2 for *(a,b)* 8, *(c)* 12, *(d)* 16, *(e)* 20 and *(f)* 30 minutes. Note that the TiW is partly covered with photoresist, except for *(f)* were resist adhesion problems occurred. Pictures taken at an angle of 70 °.

After etching for 30 minutes, the photoresist showed adhesion problems during the rinse in DI water and spin drying. This is shown in Figure 30f, it was not possible to make suitable cross sections of the sample etched for 40 minutes.

It is observed that 80% of the metal layer is etched during the first 8 minutes (Figure 30b), the final 20% is etched after 16-20 minutes (Figure 30d, Figure 30e). This might indicate that different species are formed between the (bulk) TiW and the oxide layer. This is discussed in more detail in the following section (2.9.2.2).

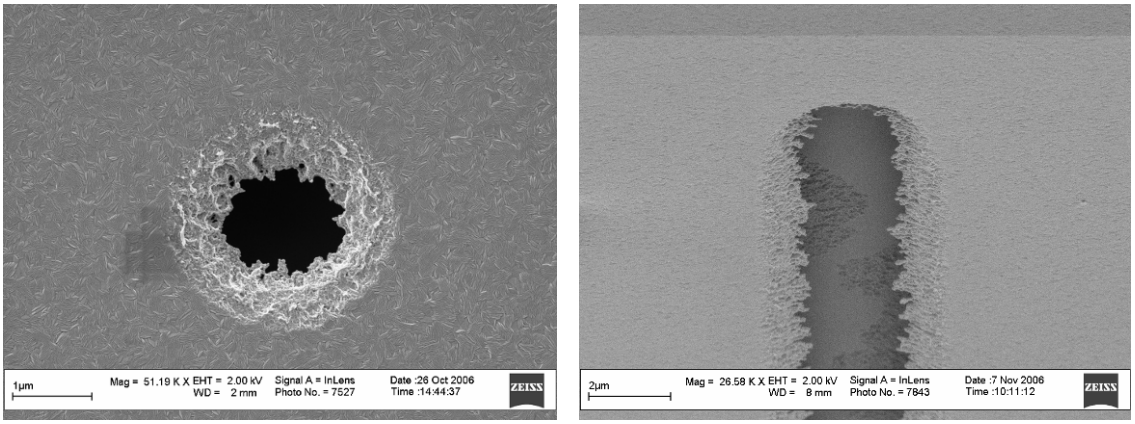
On the basis of these results it is concluded it is possible to etch 300 nm TiW in 31% H_2O_2, an etch time of 16-20 minutes is required to get an acceptable surface clearance. However, after this etch, still small particles remained on the oxide surface. As long as there are not too much, this is not problem; these will be removed in the oxide etch afterwards. Furthermore, the edge is not defined nicely, due to the grain structure of the TiW. This is not desirable, as it might lead to different fields and emission behaviour of field emitter, but not necessarily a problem when the differences between individual devices are not too large.

In order to tackle resist adhesion problems, due to the long etch time, an etch with higher etch rate is preferred and investigated in the following section.

2.9.2.2 Etching in H_2O_2 + NH_4OH

The etching of TiW in H_2O_2 can be accelerated by the addition of NH_4OH [78]. For this purpose, a mixture of 800 ml H_2O_2 (31%), 60 ml NH_4OH (25%) and 800 ml DI-water is prepared, resulting in a solution of 15 % H_2O_2 and 1% NH_4OH in water.

The same samples as described in section 2.9.2.1 were etched, with a much higher etch rate. The 300 nm TiW layer was etched in 5:30 min (endpoint determined by colour change). A picture of a device at the end of the whole process fabricated (with this etchant), after lift-off and before CNT growth is shown in Figure 31.

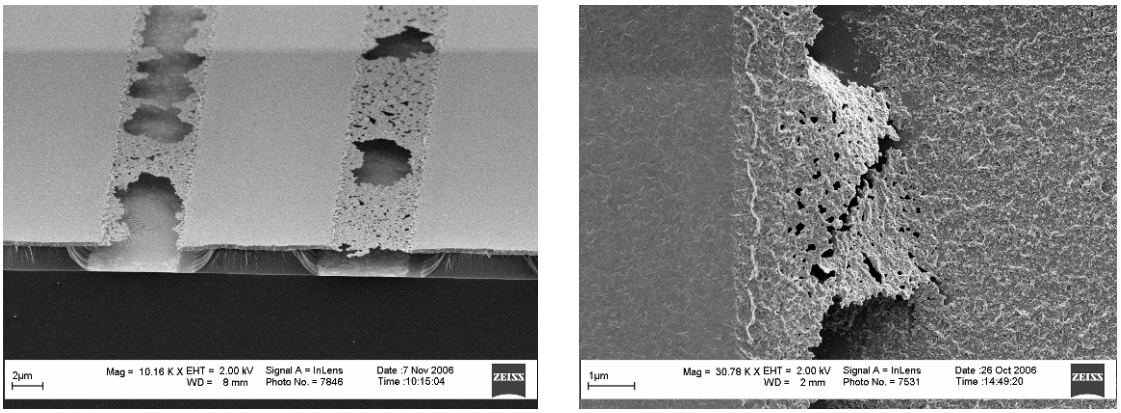


(a) *(b)*

Figure 31. HR-SEM images of etching of 300 nm TiW in 15% H_2O_2 + 1% NH_4OH for 5:30 minutes.
(a) Top view of a device at the end of the whole process (with this etchant), after lift-off and before CNT growth.
(b) Test line of 2 µm showing the edge roughness for a larger area.
Picture taken at an angle of ca. 70 °.

It is shown that 300 nm TiW can be etched for 5:30 min in this solution without resist adhesion problems.

The edge roughness is most likely caused by the same species as shown in Figure 30b. This species is most likely titanium oxide (TiO_x), formed by interaction between titanium and H_2O_2 during the etch process; H_2O_2 is a very aggressive oxidizer and can easily oxidize titanium [86]. This TiO_x is not etched in H_2O_2 or BHF (used in the oxide etch step following TiW etching) and remains in the etched structures. These artefacts are observed in structures with etched gates of 250 nm TiW + 50 nm W and shown in Figure 32.



(a) *(b)*

Figure 32. HR-SEM images of etching artefacts after etching 250 nm TiW + 50 nm W in 15% H_2O_2 + 1% NH_4OH for 5.30 min. Pictures taken of test lines at the end of the whole process, after lift-off and before CNT growth.

The TiO_x formation is most likely related to the extent of distribution of the titanium in the tungsten [79]. When the titanium is distributed homogenously to the atomic level, it will be oxidized by H_2O_2, but flushed away during the etch. However, when the titanium is not distributed homogenously, but accumulated in larger clusters (for instance at surfaces or grain boundaries), the TiO_x is formed in larger clusters as well, which precipitate at the surface.

These etch problems can be counteracted in two different ways: either by ensuring a proper distribution of titanium in tungsten and/or by etching in a modified solution with different pH to slow down the formation of large TiO_x clusters.

The distribution of titanium in tungsten is related to the sputtering process and can be enhanced by enlarging the mean free path and the kinetic energy of the metal particles during deposition. This can be achieved by increasing the sputtering power and decreasing the sputtering pressure. In this way, denser films with a higher homogeneity are obtained [79].

The etching solution can be modified by the addition of ammonium acetate (CH_3COONH_4) which leads to a change in the pH of the solution, slowing down the formation of TiO_x while etching tungsten [87].

Note that these etch artefacts are observed for 250 nm TiW + 50 nm W layers only, the 300 nm TiW layers, although being still a little rough, have much better defined edges.

This is consisted with the layer composition and sputtering conditions: 250 nm TiW layers are deposited in Sputterke with an Ti:W ratio of 24:76 at.% (measured at the substrate), whereas 300 nm TiW are sputtered in the Oxford PL400 with an T:W ratio of 14:86 at.%. Furthermore, it is difficult to estimate the layer homogeneity from the sputtering condition like sputtering power and pressure. These can be compared only properly when

key differences between the sputtering systems are taken into account, like target area, target to sample distance, sample holder with its thermodynamic behaviour etc.

2.10 Oxide etch

Directly after the metal gate etch step, the silicon oxide is etched is etched in BHF (1:7) for ca. 34 min. As oxide is etched isotropically in this solution, the desired underetch pattern is realized automatically. Apart from the front side of the wafer, the oxide on the backside is stripped simultaneously. The endpoint of the etch process is determined by checking the etched surface: when this turns hydrophobic, the (bare) silicon is reached. An extra dummy wafer is used as reference.

The typical underetch profile is shown in Figure 33.

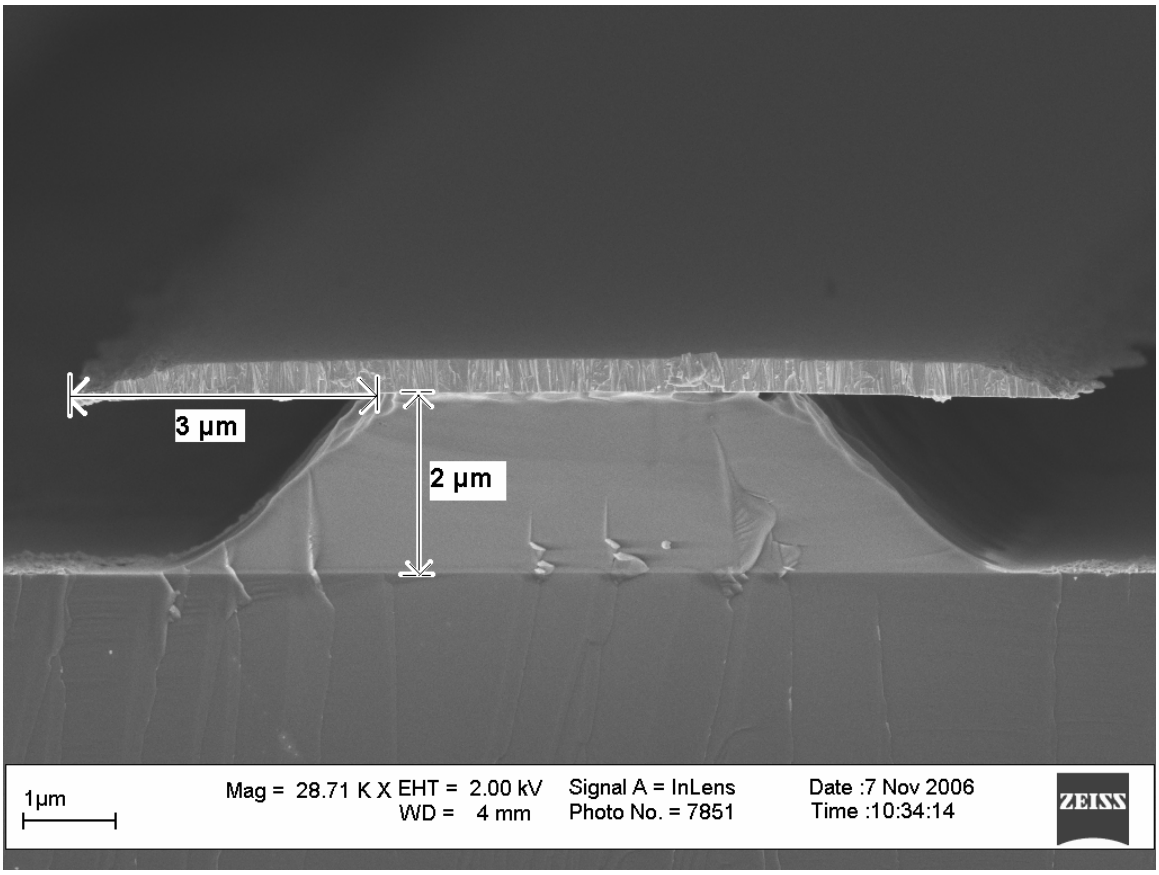


Figure 33. HR-SEM image of the etch profile of the silicon oxide, showing the characteristic underetch. Picture taken at the end of the process after lift-off and before CNT growth.

It is observed that the underetch is 3 µm which is 1 µm more than the desired 2 µm. This indicates that etching in the horizontal direction went faster as expected. This may be due to over etching (etching for too much time), stress in the tungsten layer or capillary forces between the oxide and the tungsten layer. A similar etch profile is observed in structures fabricated by Lee [65] with comparable tungsten gate electrodes on oxide (Figure 15b).

2.11 Back electrode deposition

Directly after the oxide etch, the metal on the backside of the wafer is deposited. The back of the wafer is metallised as small (10×10 mm) dies have to make a low ohmic contact when used in a test setup. This is facilitated with a metallised wafer back. The setup has no vacuum chuck as frequently used in average probe stations. By doing the deposition directly after the oxide etch, the formation of native oxide is avoided, creating a better electrical contact. Platinum (Pt) is selected for its stability and chemical inertness at high temperatures [88].

Platinum can be deposited on silicon without an adhesion layer by sputtering and evaporation. In this project 200 nm platinum is sputtered in 'Sputterke' at 200 W with 6.6 × 10^{-3} mBar in 10 min.

During the high temperature CNT growth process at 700 °C, platinum silicides (Pt_xSi_y) are likely to be formed, depending on the diffusion of platinum and Si. This diffusion is plausible on the basis of the diffusion coefficients of platinum into silicon (D_0=3.4×10^{-6} m^2/s and Q=254.5 kJ/mol) and silicon into platinum (D_0=1.54×10^{-6} m^2/s and Q=448.4 kJ/mol), together with the fact the samples are exposed to an high temperature step of 700 °C for at lease 20 minutes with relatively slow ramp up and ramp down speeds (2.13.1). As these platinum silicides enhance the electrical contact, their formation would be an advantage.

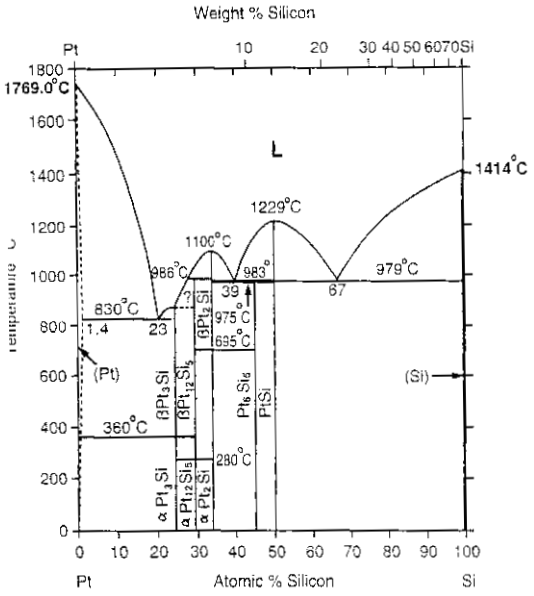


Figure 34. Phase diagram of Pt-Si showing the formation of Pt_xSi_y at low temperatures. Reprinted from [89].

Metal-silicon contacts might form Schottky contacts. The Schottky barrier depends on the work function of the metal. Although there are a lot of theories about Schottky contacts [9], in practice these theories are not valid for very large contact areas like the back of (unpolished) wafers. Therefore some electrical measurements were carried out on test samples. Both normal (p-type) and heavily doped (p^{++}) wafers were cleaned in the standard

cleaning + HF dip, and 200 nm platinum was deposited on the backside and 200 nm platinum dots (Ø 4 mm) were deposited on the front using a shadow mask.

Samples were annealed at 700 °C in N_2 for 1 hour to approximate the CNT growth process and IV characteristics were measured using an Agilent 4145 IV meter in combination with a Microtech Cascade probe station. A typical result is shown in Figure 35.

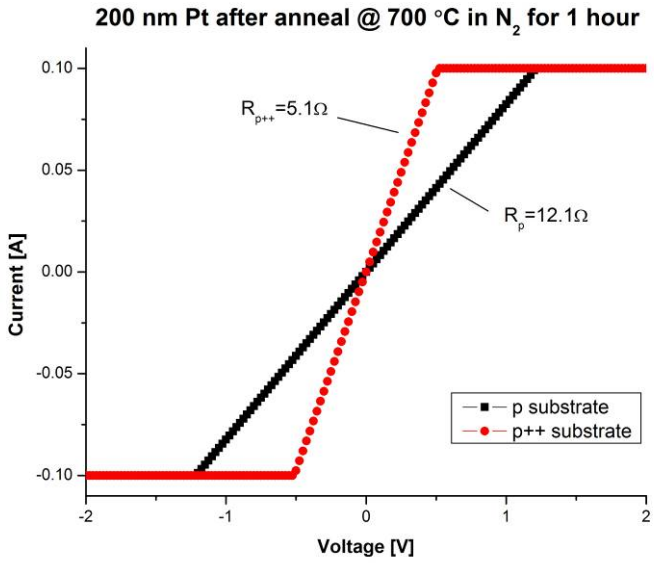


Figure 35. IV measurements on metallised samples (platinum) after an anneal at 700 °C in N_2 for 1 hour. Normal (p) and heavily doped (p^{++}) wafers were used. The current saturation at +/- 0.10 A is due to (safety) limitations in the measurement equipment (compliance).

No Schottky behaviour is observed: the current-voltage relationship is identical for positive and negative voltages. From the slope of the curves the differential resistance is derived ($R=dV/dI$). It is shown the heavily doped substrate has a lower resistance. This measured resistance is not equal to the total wafer resistance, as there are other parasitic series resistances (like probes and cables) in the measurement circuits which were not corrected for in this (2-point) measurement.

2.12 Catalyst deposition

2.12.1 Catalyst choice

As discussed earlier in section 1.4.2.3, the growth of carbon nanotubes (CNTs) is mainly controlled by the catalyst that is used in the CVD process. The catalyst, generally a metal thin film, agglomerates at high temperatures into nanoparticles from which the CNTs are grown in the CVD process. In this section the choice and deposition of the catalyst is discussed, including considerations about the incorporation of a barrier layer to avoid interaction between the catalyst and the substrate.

Many different catalysts are reported in literature for the CVD growth of CNTs including nickel (Ni), cobalt (Co), iron (Fe), palladium (Pd), platinum (Pt), ruthenium (Ru), gold (Au), silver (Ag) and several alloys of Cu-Ni, Fe-Ni and Pd-Se [39][90]. Nickel is the catalyst most frequently used in literature [39] and the only catalyst used for CNT growth in the catalytic materials and processes group (CMP) of our university [91]. In this group, the CNTs used in this project are grown (see section 2.13.1).

Nickel can be deposited with different techniques, including sputtering and evaporation. Nickel has to be deposited in a directional way in this process, to avoid the CNT growth as a result of nickel deposition on the sidewalls of the etched cups. Therefore, evaporation is chosen as deposition method, since this method is highly directional (more than sputtering in our cleanroom).

2.12.2 Barrier layers

When nickel is deposited on silicon substrates, nickel-silicides (NiSi) are formed at temperatures above 300 °C [67]. According to Melechko et. al. [39], the NiSi formation prevents the nucleation of the catalyst particles from thin films and inhibits CNT growth. However, others showed the formation of CNTs directly on top of NiSi [39]. Due to incompatibilities of substrates with catalytic materials and the growth environment, buffer layers, under layers, and adhesion layers have come into widespread use [39].

Typical barrier layers used in literature are SiO_2 [24][92][93][94], titanium (Ti) [1][47][95], titanium nitride (TiN) [66][96], and aluminium (Al) [1]. An extensive review can be found in [39].

As the CNTs act as field emitters, a conducting barrier layer is required to ensure a low ohmic contact. Therefore, SiO_2 is abandoned as possible barrier layer. TiN is a very attractive barrier layer as it is highly conductive, very stable and has a high meltingpoint (3200 °C). TiN can be deposited with reactive sputtering only in our cleanroom in the 'Nordiko'. In this sputtering process, a Ti target is sputtered with N_2 gas, leading to the formation of TiN. The system available is not capable of depositing layers of 10 nm thickness with a high accuracy and it is not possible to deposit nickel within the same vacuum. Furthermore, TiN can be deposited only in a 'high pressure' process, resulting in sputtering of the metal on the sidewalls of the cups. This may lead to electrical shorts between the gate and base electrode, but nevertheless others successfully incorporated a sputtered TiN barrier layer [66]. Because of limitations of the available deposition equipment, TiN is abandoned as a potential barrier layer.

Titanium is an interesting barrier material, as is can be deposited by evaporation and sputtering in the same vacuum as nickel. The disadvantage of titanium is its reactivity, especially with oxygen (O_2). Nickel layers in the (tens of) nm range on top of titanium are

not gas tight, leading to oxidation of titanium during exposure to air and/or high temperature processing (see section 2.6.5.2 for the stability of Ti/W layers at elevated temperatures).

2.12.3 Conclusion

As other groups successfully grew CNTs without (reporting the) barrier layer [23][65] [71], several CNT growth experiments were carried out to test the need for a barrier layer. Experiments were carried out with different nickel layers, including 10/10 nm Ti/Ni, 10/10 nm Ta/Ni and 10 nm nickel without barrier layer. These experiments are discussed in section 2.13.2.1 in more detail. On the basis of these results it is decided to use nickel deposited directly on silicon with native oxide as barrier. Although this is a 'poor mans' solution, it is preferred over the extra CNT growth tests within this project.

2.13 Carbon nanotube (CNT) growth

2.13.1 Introduction

CNTs were grown in the catalytic materials and processes group (CMP) [91][97], using a T-CVD system. The CNTs are grown in a small, vertically aligned tube furnace with a sample holder (perforated basket) capable of holding two samples of (at maximum) 10 × 10 mm simultaneously. The temperature is monitored with a single thermocouple positioned just above the samples. Gases are mixed (at atmospheric pressure), flushed through the tube furnace, collected and analysed with an online mass spectrometer (for gas composition analysis every two minutes). The whole apparatus is shown in Figure 36.

In a typical CNT growth run, samples are loaded at room temperature. Then the temperature is increased with a ramp of 6 °C/min. When the desired growth temperature is reached, the carbon (gas) source is opened while the output gas composition is monitored. No pre-treatment of the catalyst with for instance NH_3 is used, as reported by others [39]. When a hydrogen peak evolves in the spectrum of the MS, the (hydro)carbon source gas is dissociated, indicating carbon is deposited in the system. After CNT growth, ended by switching off the carbon source, the temperature is ramped down with 10 °C/min until the temperature is 400 °C. At this temperature, the heater is switched off resulting is passive cooling down. Finally, when room temperature is reached, samples are unloaded. During the whole process, including heating and cooling down, nitrogen (N_2) is flown. The carbon source used is acetylene (C_2H_4). Standard flow rates are 80 sccm for N_2 and 27 sccm for C_2H_4. In general, CNTs are grown at temperatures between 500-800 °C for tens of minutes, taking more than half a day for a single run.

(a) *(b)* *(c)* *(d)*

Figure 36. CNT growth apparatus with *(a)* the sample holder with two samples, *(b)* the mass spectrometer, *(c)* the tube furnace and *(d)* the gas supply with flow controllers and mixing board.

2.13.2 Initial CNT growth experiments

As there was no experience with CNT growth on nickel (Ni) substrates fabricated in the cleanroom MESA+, several tests were carried out.

Standard (100) p-type silicon wafers were cleaned in the standard cleaning: 2 × 5 minutes in fuming HNO_3 and 10 minutes in boiling HNO_3 to remove organic and non-organic species respectively. Wafers were patterned in a standard lithography process based on Olin 907-12, finished with a 20 min 120 °C postbake.

Different metal layers were deposited by (e-beam) evaporation: 10 nm nickel (Ni) with and without barrier layers of 10 nm titanium (Ti) or 10 nm tantalum (Ta) respectively. Excess metal was removed by lift-off in acetone, enhanced by ultrasonic agitation.

In this way, samples with regular arrays of small metal dots (Ø 4 μm) and larger areas of several 100's of μm^2 were fabricated. A typical example is previously shown in Figure 29.

2.13.2.1 CNT growth with metal layers of different composition

In the first experiment, CNTs were grown at 700 °C from 10 nm nickel layers. The carbon gas source (C_2H_4) was opened at 550 °C and 650 °C, but according to the MS results, no carbon was deposited at these temperatures. Carbon deposition was found at 700 °C and CNTs were grown for one hour.

Typical results are shown Figure 37, showing that noodle shaped CNTs are grown on small and large area of nickel. An array with decent uniformity in the shape of the nanotube balls is shown in Figure 37a.

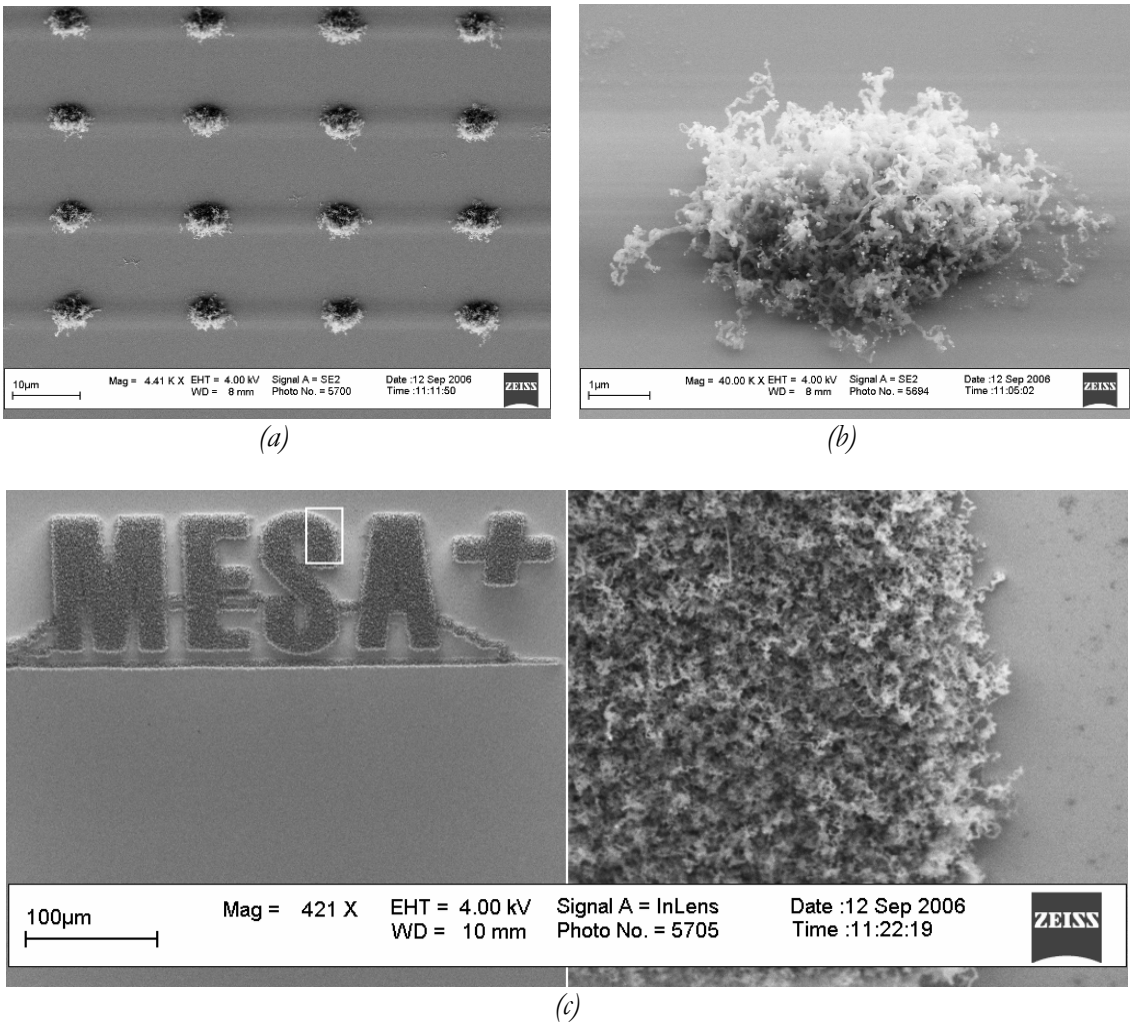


Figure 37. HR-SEM images of CNT growth experiments showing the result on *(a)* an array of 10 nm nickel dots (Ø 4 µm), *(b)* magnification of a single dot and *(c)* a large area. The 'lines' in *(a)* are measurement artefacts, most likely due to carbon redeposition as a result of the scanning electron beam of the HR-SEM.

On the basis of this, similar experiments were carried out on 10 nm nickel layers with 10 nm of titanium or tantalum as diffusion barrier layer. These results are shown in Figure 38a,b and Figure 38c,d respectively.

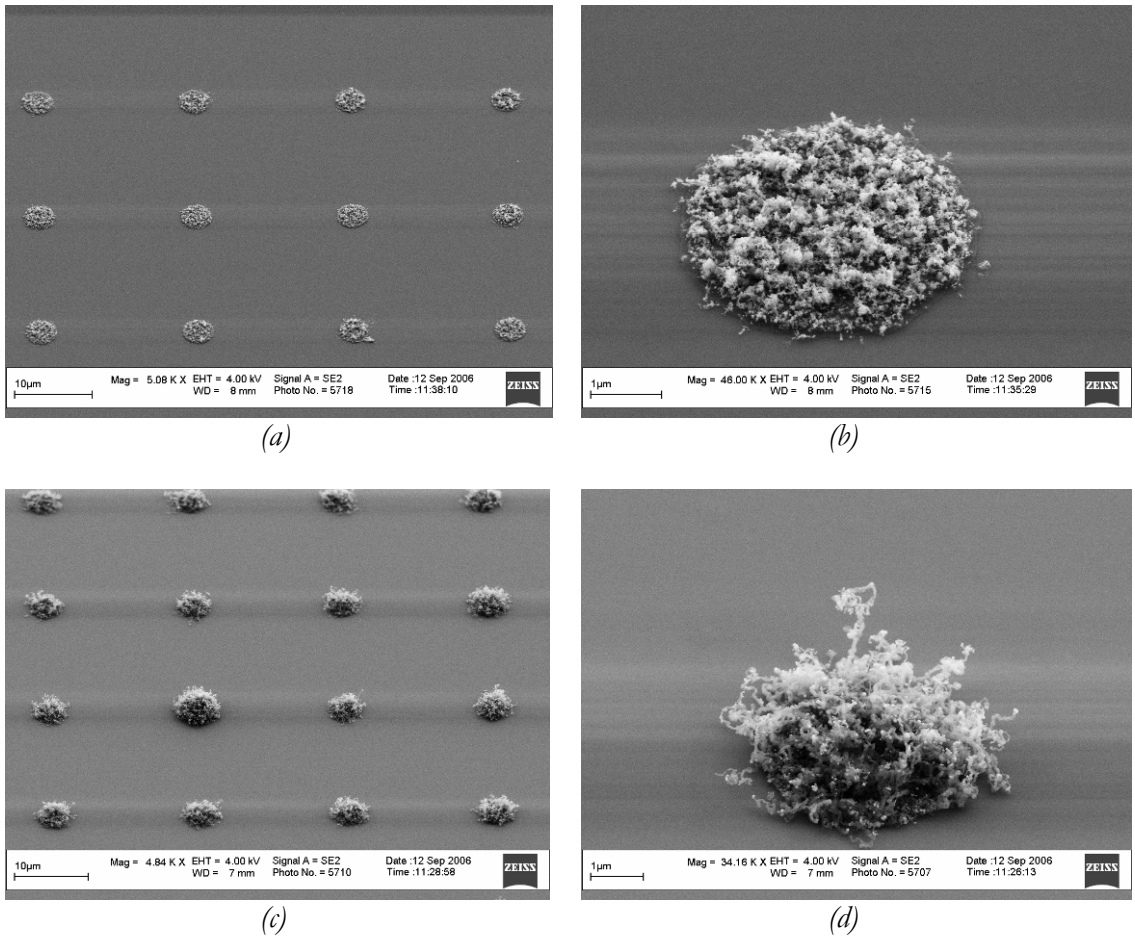
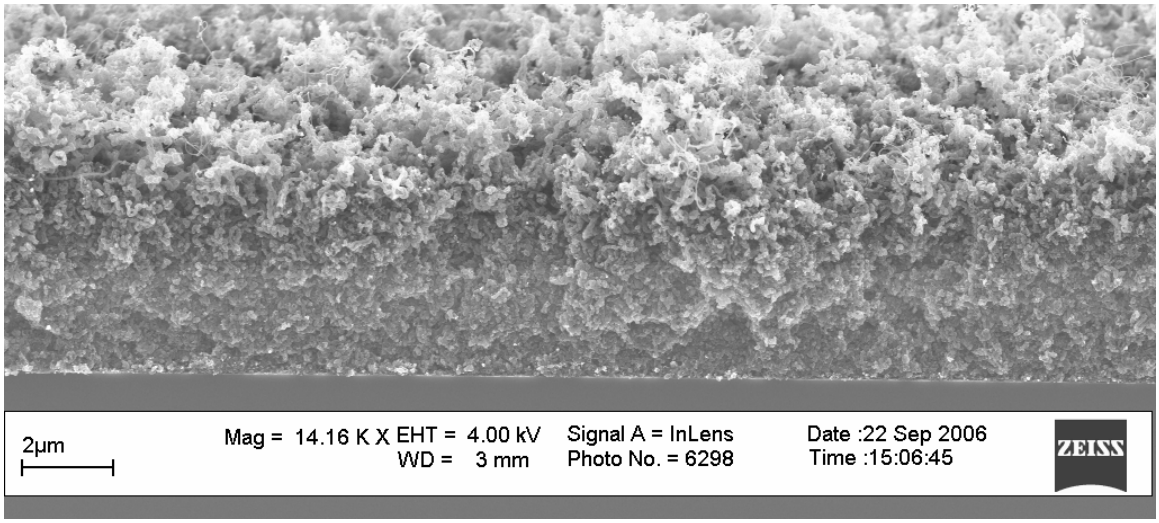


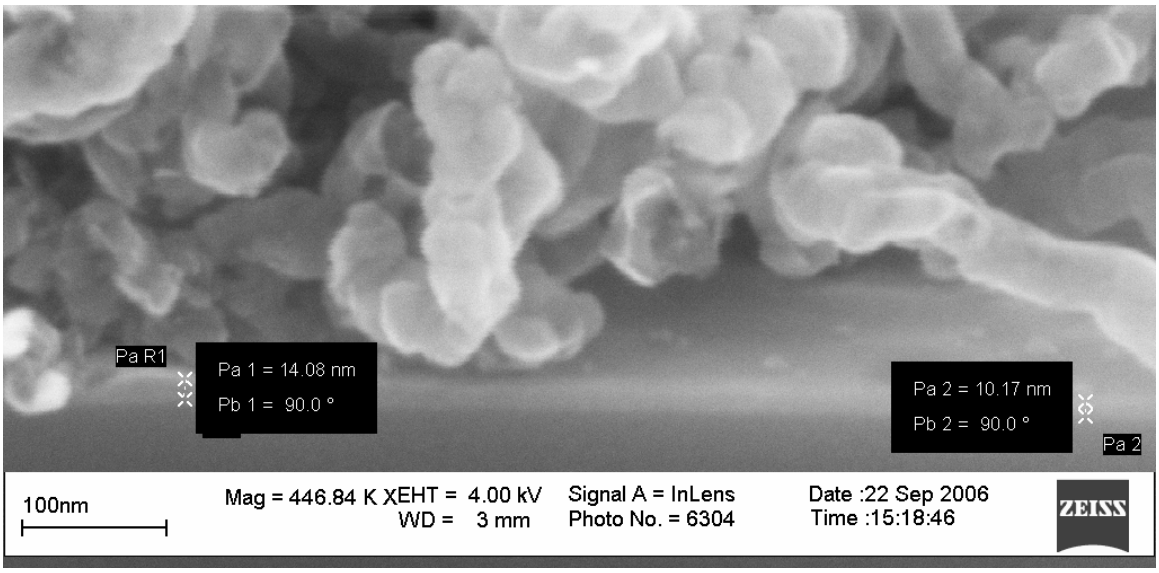
Figure 38. HR-SEM images of CNT growth experiments showing the result on *(a)* an array of 10/10 nm Ti/Ni dots (Ø 4 µm), *(b)* magnification of a single dot, *(c)* an array of 10/10 nm Ta/Ni dots (Ø 4 µm) and *(d)* magnification of a single dot.

It is observed that hardly no CNTs were grown on Ti/Ni layers, whereas Ta/Ni layers successfully acted as catalyst for CNT growth. Some carbon is deposited on Ti/Ni layers. The size of the ball of CNTs is almost equal to those grown at pure nickel layers, only slightly smaller.

This result, successful CNT growth on (pure) nickel layers and Ta/Ni layers on silicon and unsuccessful CNT growth on Ti/Ni layers is in contradiction of what would be expected on the basis of the literature [39][47]. Therefore cross-sections were made of nickel samples and examined using the HR-SEM. A typical result is shown in Figure 39.



(a)



(b)

Figure 39. HR-SEM images of CNT growth experiments on 10 nm nickel on silicon for 1 hour at 700 °C. *(a)* Cross-section of a line showing the interface at an angle of ca. 70 °. *(b)* Magnification of the silicon-CNT interface, showing an interfacial layer of ca 10-15 nm thickness.

From these cross-sections, two observations are made: the height of the CNT layer is ca. 5-6 µm and a thin interfacial layer exists between the silicon and the CNTs. This interfacial layer is observed as well on places were no CNTs were grown (results not shown), and has a thickness of ca. 5-10 nm.

This layer is most likely silicon oxide; in the cleaning process prior to the catalyst deposition, the native oxide of the silicon (with a thickness of typically several nm) was not stripped in an HF dip and the deposition was carried out half a day after the cleaning. The grey-tone colour in the SEM picture is in accordance with this as it is typical for poorly conducting layers.

Furthermore, this might explain the unsuccessful experiments with titanium as a barrier later; others grew CNTs successfully on nickel with titanium as barrier layer [1, 47, 95]. Apparently, during the high temperature step, titanium prefers interaction with silicon leaving the nickel on top active for nanotube growth (see Figure 10b how titanium remained on the silicon, while the nickel agglomerated), whereas the titanium interacts with nickel when an underlying silicon oxide layer is present, resulting in a compound that is not a proper catalyst for CNT growth.

It was concluded that a barrier layer of 5-15 nm oxide was incorporated unintentionally. Most likely this oxide layer prevented the formation NiSi and hence enhanced the CNT growth on pure nickel layers.

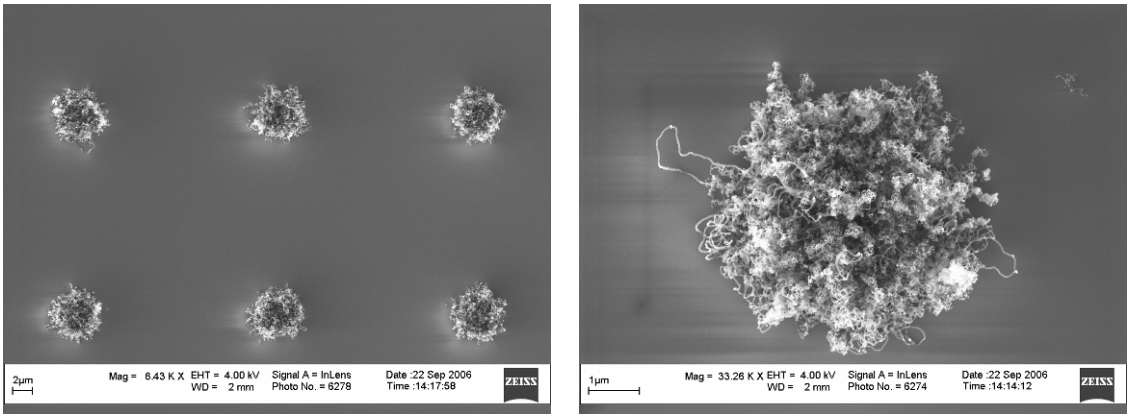
This oxide barrier layer has the large disadvantage of increasing the contact resistance, leading most likely to current saturation during field emission at high field and the 'blow out' of CNTs as a result of the local heat generation due to ohmic heating.

On the basis of this, new experiments were considered in which the native oxide was stripped before nickel deposition, followed by CNT growth experiments. In case these would have been unsuccessful, an alternative (conductive) barrier layer had to be incorporated. As discussed previously in section 2.12.2, this would not have been straight forward, thereby consuming a serious amount of time. It was decided to cancel these experiments and keep this native oxide as a 'poor mans' barrier.

Therefore the CNT growth process was fine tuned, in order to obtain the size of the CNT balls into the right proportions for use in a gated field emitter structure.

2.13.2.2 CNT growth with nickel layers for different growth times

As shown in the previous paragraph, CNTs are grown on nickel at 700 °C for 1 hour resulting in a 'cluster' with a thickness of ca. 5-6 μm. As a thickness of 2 μm is desired, different growth times are tested at the same temperature, to 'shrink' the size of the CNT ball. Tests were carried out on 10 nm nickel samples for 20 and 40 min. The results for the 20 minute run is shown in Figure 40.



(a) *(b)*

Figure 40. HR-SEM images of CNT growth experiments on 700 °C for 20 min, showing *(a)* and array and *(b)* a single dot of 4 μm.

It is observed that the 20 min run was successful and nice balls of CNTs were grown. Although the images were taken at a different angle than for instance Figure 37 it is clear the CNT balls are smaller and have nice uniformity (also on the basis of other results, not shown). The height of the CNT ball is estimated at ca 2-3 μm.

The 40 min run was not successful, hardly any CNTs were grown.

It is concluded that the result of the 20 min run is good enough to continue with, for the development of the gated field emitter structures (GFEAs) with nickel thin films as catalyst for CNT growth. These structures were fabricated according to the flowchart shown in Table 4 and CNT growth experiments were carried out and discussed in the following section.

2.13.3 CNT growth experiments in gated structures

2.13.3.1 Gated field emitter arrays with 300 nm TiW gate electrodes

Typical GFEAs structures shown in Figure 41 have a silicon substrate, 2 μm oxide, a 300 nm TiW metal gate and 10 nm nickel (Ni) at the bottom of the etched structure.

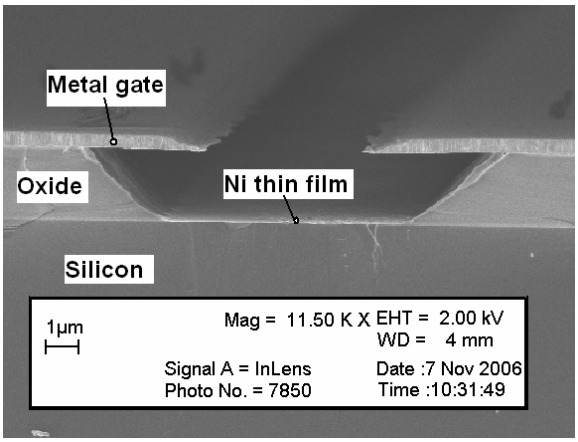
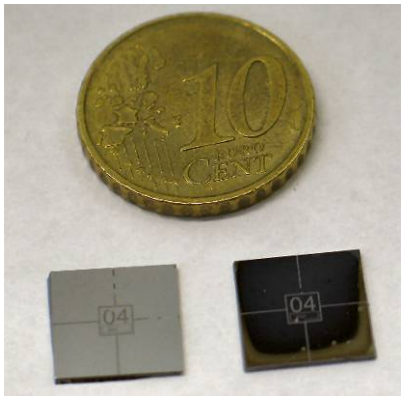
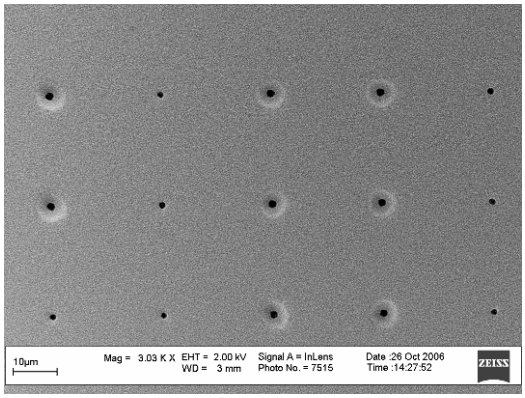


Figure 41. HR-SEM image of GFEAs as used in CNT growth experiments.

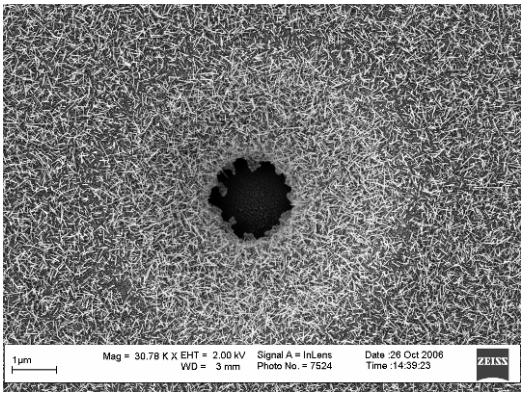
CNTs were grown on these samples for 20 min at 700 °C. The results are shown in Figure 42.



(a)



(b)



(c)

Figure 42. *(a)* Samples before (left) and after (right) the CNT growth process. *(b,c)* HR-SEM images of CNT growth experiments on GFEAs with 300 nm TiW gate electrodes and 10 nm nickel in the cups, showing the top view of *(b)* an array of 2 µm holes and *(c)* a single 2 µm device.

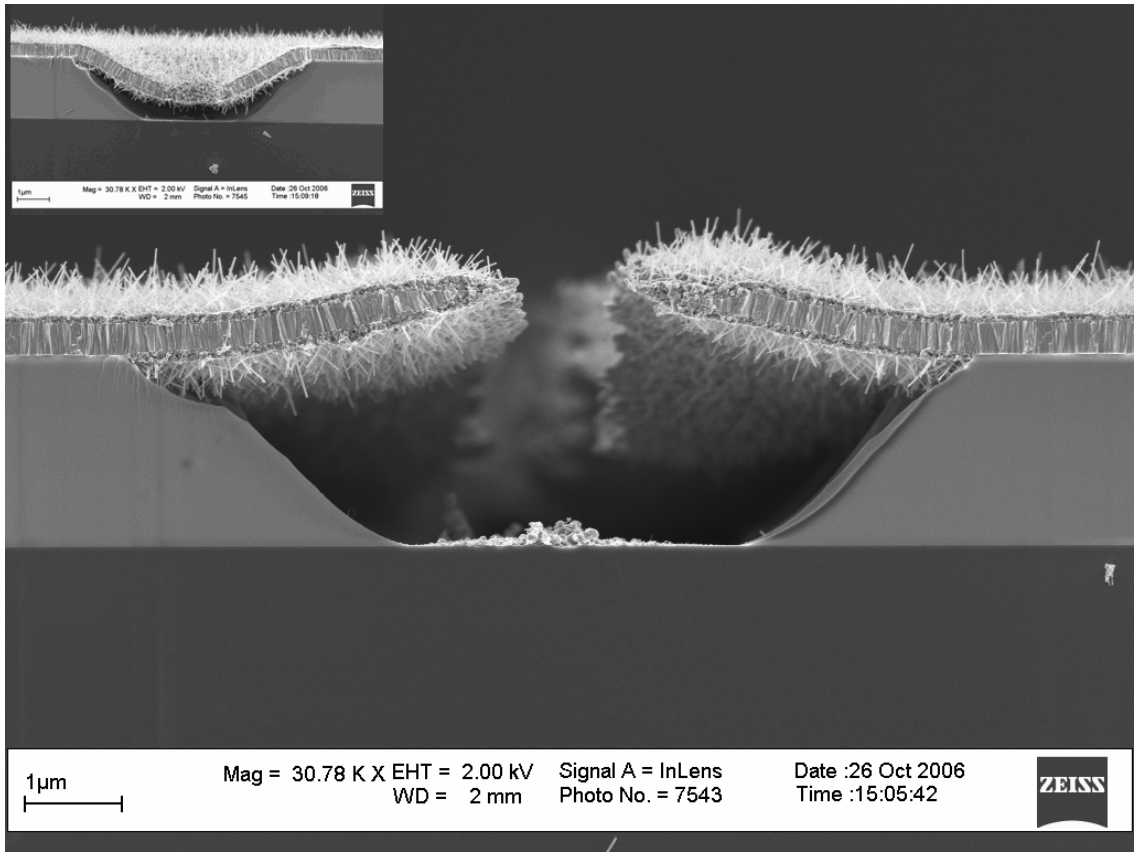
First of all, it is observed that samples, removed from the reactor, were covered with a black substance. Figure 42a shows samples before and after CNT growth. Note that the sample is not covered homogeneously with the black substance: it appears to be related to the flow pattern of the gases around the sample during CNT growth. Samples were positioned in the sample holder (Figure 36a) with the top side downwards.

Furthermore, it is observed that part of the dies collapsed (Figure 42a,b); apparently in the gate electrodes thermal stress is induced during the CNT growth process, resulting in mechanical failure. The mechanical failure appears to be related to the gate electrode hole size of the cups: gates electrodes with smaller holes (Ø 1-1.5 µm over Ø 4-5 µm cup diameters at the top) are remained in tact while the gate electrodes with larger holes Ø 1.5-2.5 µm over Ø 5-6 µm cup diameter at the top failed. This trend is confirmed by other samples (not shown) with larger holes (Ø 2-3 µm over Ø 5-8 µm cup diameters at the top) were all devices collapsed. The fact that devices with small hole do not fail appears to be related to the etching of the silicon oxide. The oxide is etched slower under a small gate hole as a result of slower diffusion of the etching solution. Apparently 1-1.5 µm is about the

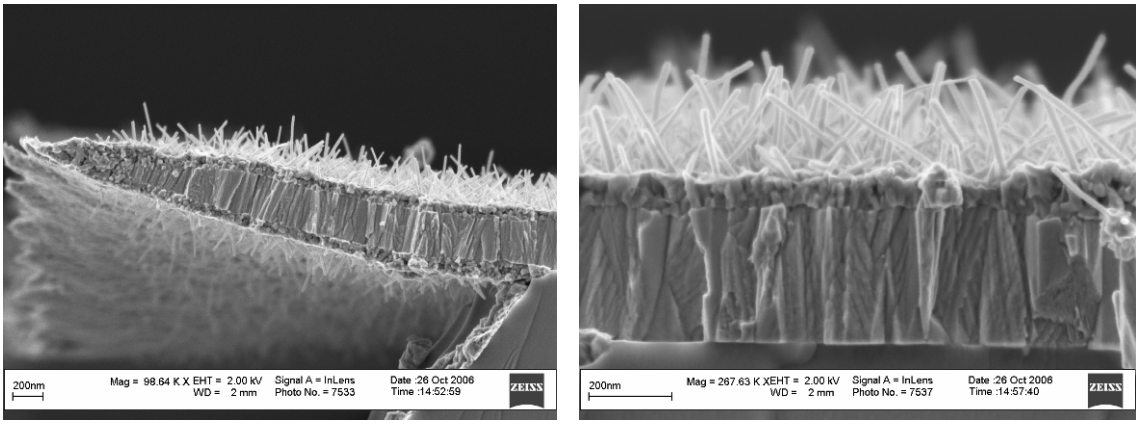
critical diameter for the gate holes (openings) for this design and combination of materials. This indicates the importance of controlling the gate hole diameter and the oxide etch in a high manner, especially for large arrays this uniformity is important.

Apart from this, it is observed that the gate electrode is covered with needle shaped nanotubes, while no nanotubes are visible in the gate hole. This TiW coverage is uniform over the whole sample.

In order to get more information on the etching and silicon oxide and the nanotube growth, cross-section were made and examined with the HR-SEM. These results are shown in Figure 43.



(a)



(b) *(c)*

Figure 43. HR-SEM images of CNT growth experiments on GFEAs with 300 nm TiW gate electrodes and 10 nm nickel in the cups, showing *(a)* the cross-section of a 2 µm test line. The inset shows the cross-section of a single cup; the gate electrode is totally covered by nanotubes, while no carbon is deposited at the nickel at the bottom of the cup.
(b), *(c)* close-up of the 2 µm line gate electrode.

Figure 43a clearly shows how the gate electrode is covered on top and a little less on the bottom side by nanotubes, while hardly no carbon nanotubes are grown at the bottom of

the structure on the nickel catalyst. However, small quantities of (most likely) amorphous carbon are deposited at the nickel. The bright grey tone indicates that metal (Ni) is still present. It appears that all carbon is 'consumed' at the gate electrode, depleting gas flow from C_2H_4 in the volume in the etched structure. In Figure 43c it is shown that some amorphous substance is formed between the nanotubes and TiW gate electrode.

2.13.3.2 Gated field emitter arrays with 250/50 nm TiW/W gate electrodes

As the gate electrode in section 2.13.2.1 is fabricated from an alloy, two elements may have given rise to the nanotube growth: titanium (Ti) and tungsten (W). Therefore samples were fabricated with exactly the same process with gate electrodes of a double layer of 250 nm TiW and 50 nm W (see section 2.9.2.2 for details). As the tungsten is known for its high stress and poor adhesion (see section 2.6.4), a thick layer of 250 nm TiW is used as an 'adhesion' layer.

CNTs were grown under similar process conditions as mentioned previously in section 2.13.3.1: 700 °C for 20 min. The results are shown in Figure 44.

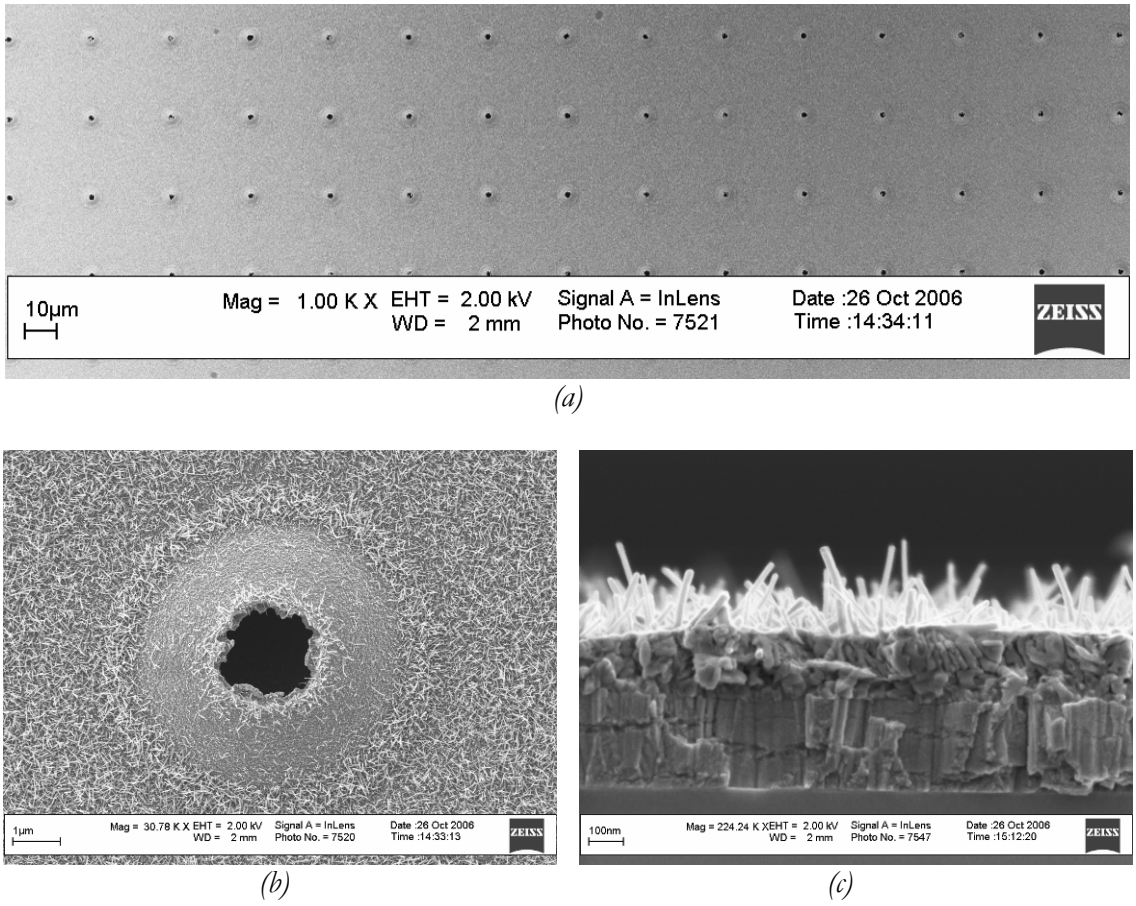


Figure 44. HR-SEM images of CNT growth experiments on GFEAs with 250/50 nm TiW/W gate electrodes, showing the top view of *(a)* an array of 2 µm holes and *(b)* a single 2 µm device and *(c)* a cross-section of the gate electrode.

First of all, considering the mechanical stability of the devices, the gates electrode were not stable but did not collapse like 300 nm TiW gates: they bended upwards (Figure 44b). This bending is most likely the result of thermally induced stress in this double layer, as a result of different thermal expansion coefficients of the TiW and W layers. This behaviour is observed for all structures and for large hole diameters as well (results not shown).

Secondly, it is observed that the gate electrode is covered with needle shaped nanotubes. This coverage shows a remarkable similarity with samples equipped with 300 nm TiW gate electrodes (see Figure 44c). However, the layer of amorphous substance on top of the metal layer appears to be thicker.

On the basis of these results it looks that the metal responsible for the nanotube growth is tungsten. However, although it seems unlikely, the diffusion of titanium along the grain boundaries towards the surface of the 50 nm tungsten layer at the high temperatures cannot be excluded and more experiments are needed to investigate this.

2.13.4 Nanotube analysis

2.13.4.1 HR-SEM analysis

In order to check whether the amorphous layer is formed during the CNT growth process or before, cross-sections are made of as-deposited (AD) samples and compared to samples after CNT growth in Figure 44.

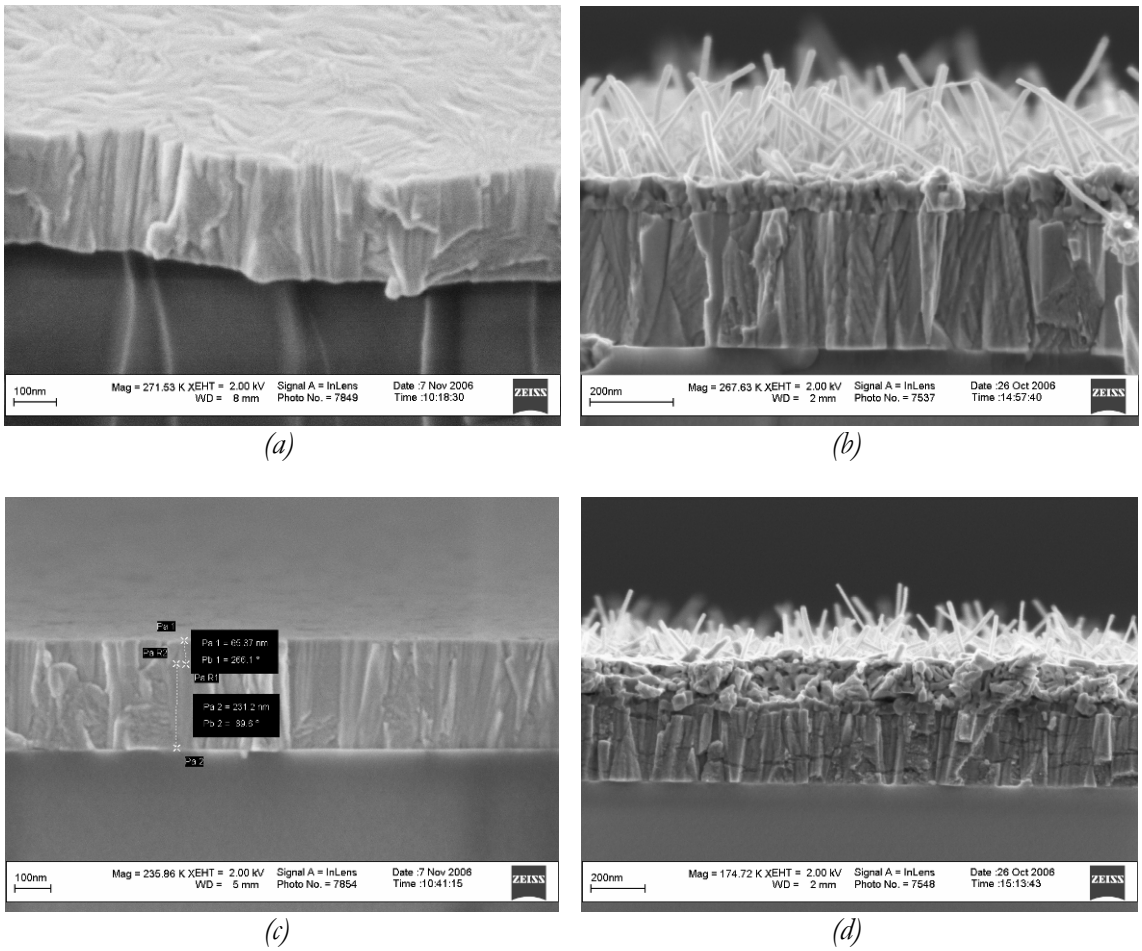
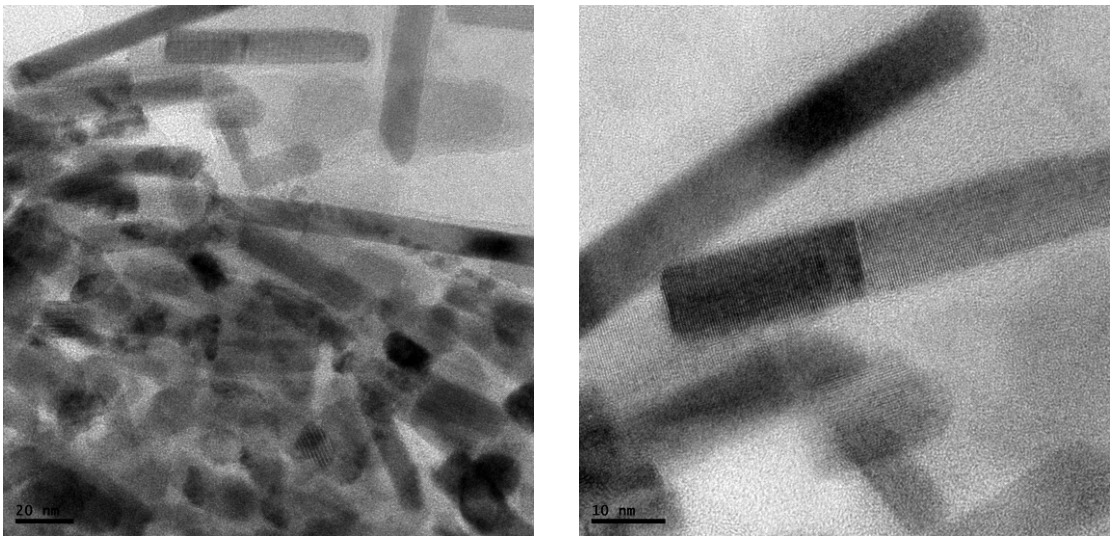


Figure 45. HR-SEM images of CNT growth experiments on GFEAs. Cross-sections of the metal gate electrode: 300 nm TiW *(a)* before and *(b)* after CNT growth, and 250/50 nm TiW/W gate electrodes *(c)* before and *(d)* after CNT growth.

It is clearly shown for both layer compositions that the amorphous layer is formed during the CNT growth process. This layer is thicker for the 250/50 TiW/W gate. Furthermore it is shown how the tungsten layer (note the slight grey tone change) has the same structure as the TiW layer (Figure 45c); the columnar grains continue in the tungsten film.

2.13.4.2 TEM analysis

In order to get more insight in the structural properties of the nanotubes, transmission electron microscopy (TEM) is carried out on 300 nm TiW samples after CNT growth. The results are shown in Figure 46.



(a) *(b)*

Figure 46. TEM images of CNT grown on 300 nm TiW gate electrodes, showing the top view of *(a)* collection of nanotubes and *(b)* a magnification of a few nanotubes, the dark 'blocks' are likely metal catalytic particles at the end of the tubes.

It is observed all nanotubes have roughly the same diameter of ca. 10 nm. Furthermore, from these results no conclusions can be drawn about the inner structure of the nanotubes (stacked cups, bamboo, compare Figure 7b, section 1.4.1.4)), due to the low contrast and resolution of the images. However, at the end of the nanotubes, rectangular objects are observed. These might be the metal catalytic particles from which the nanotubes are grown (compare Figure 7b, section 1.4.1.4). This suggests the nanotubes are grown in a catalytic growth process comparable to the nanotubes grown on nickel.

In order to determine the composition of the nanotubes, X-ray fluorescence (XRF) and X-ray induced photoelectron spectroscopy (XPS) were carried out.

2.13.4.3 XRF analysis

Samples with 300 nm TiW gate electrodes were examined by XRF before and after CNT growth; a typical result is shown in Figure 47.

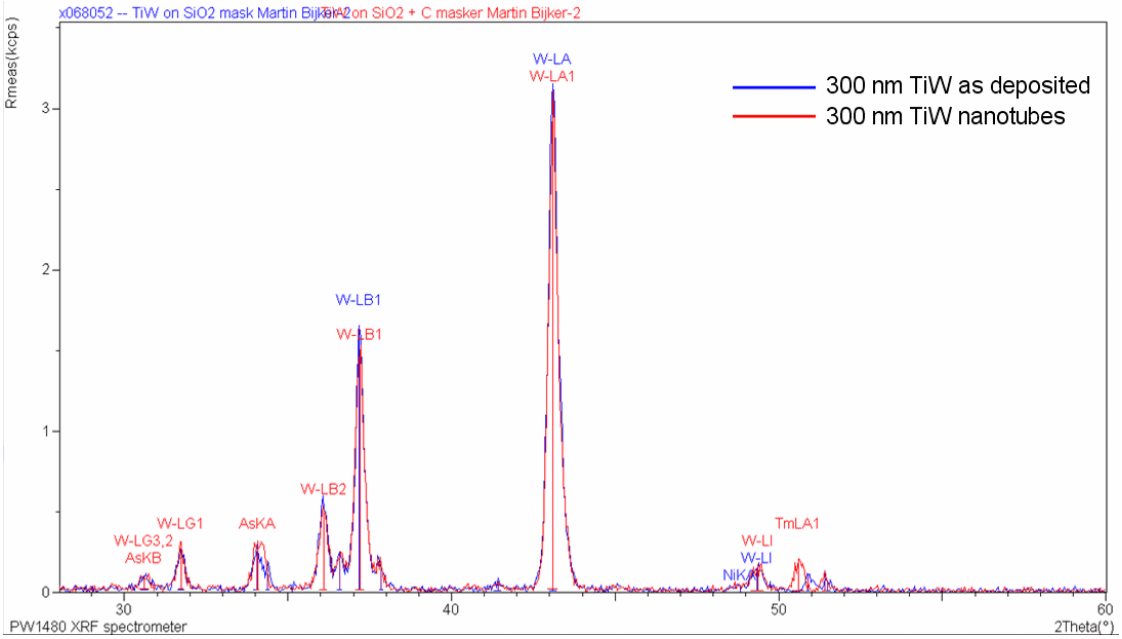


Figure 47. X-ray fluorescence (XRF) measurements on 300 nm TiW samples before and after CNT growth. Several elements are distinguished with the corresponding electrons.

It is observed that several elements are present in the sample, including tungsten (W), arsenic (As), nickel (Ni) and lanthanum (La). The first 3 elements are expected in the sample, based on the substrate doping (heavily doped with arsenic), gate electrode and catalyst. The lanthanum in the CNT sample is most likely not present in the sample and attributed to a measurement artefact. This is still under investigation.

Hardly any difference between as-deposited and CNT samples is observed. This might be due to limitations of the measurement, no carbon (C) could be detected. Furthermore, it is not clear from which depth, light and/ore X-rays are emitted and collected.

Therefore, it is concluded that XRF is not a suitable method for the determination of the elements in the nanotubes.

2.13.4.4 XPS analysis

The same 300 nm TiW and 250/50 nm TiW/W samples (pre/post CNT growth) as discussed in previous sections were examined by XPS. A typical survey spectrum for a 300 nm TiW sample after CNT growth is shown in Figure 48.

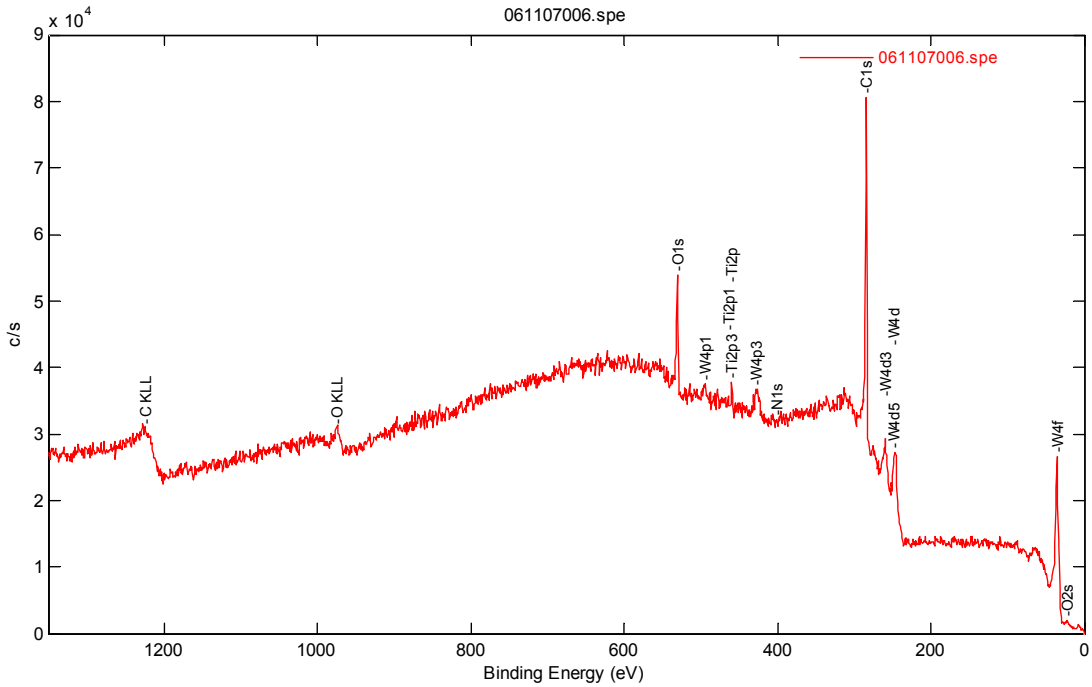
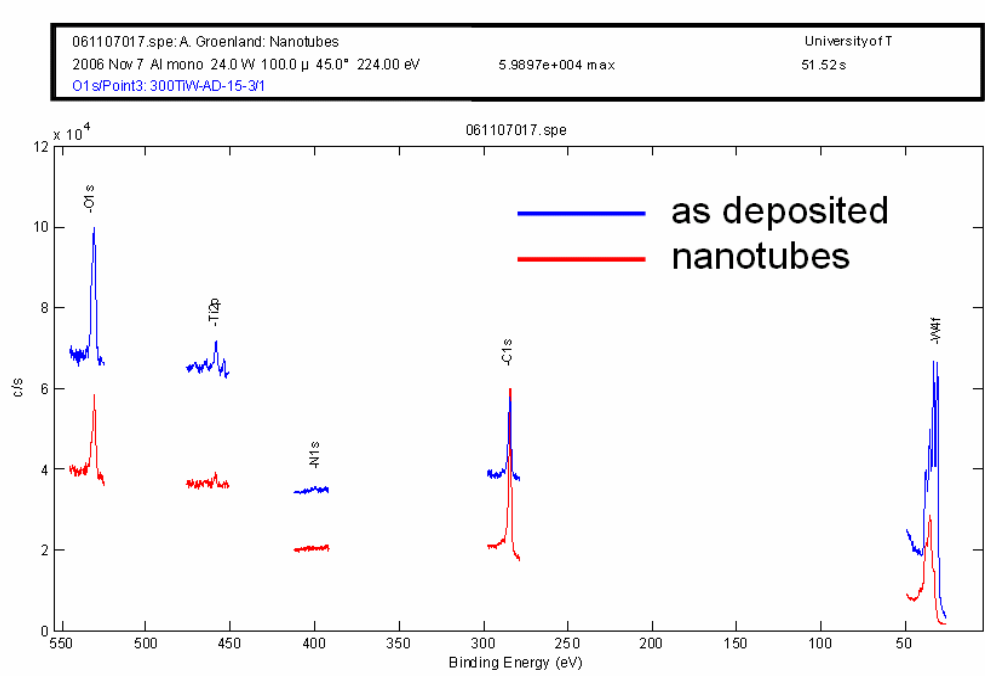


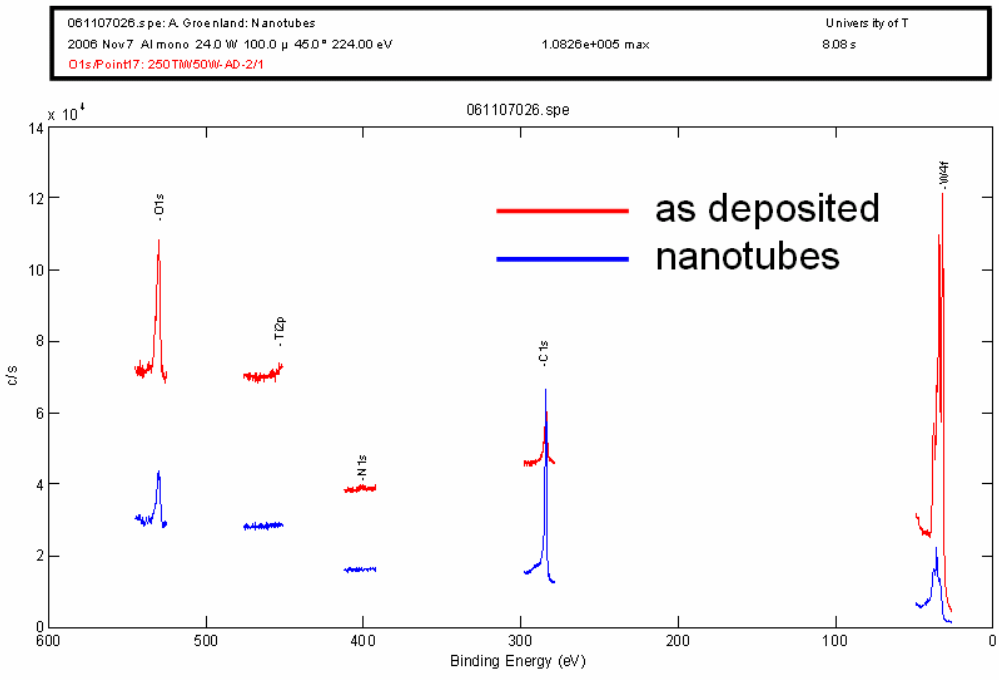
Figure 48. X-ray induced photoelectron spectroscopy (XPS) result of a 300 nm TiW sample after CNT growth: a survey spectrum from 0-1300 eV with 0.8 eV steps. Peaks indicate the response of elements with their specific electrons.

From this spectrum, titanium (Ti) and tungsten (W) peaks are observed. This is in correspondence with the layer composition. Furthermore, peaks corresponding to carbon (C), oxygen (O) and nitrogen (N) are observed. This is most likely due a surface contamination, which is normal for samples that have been kept under air ambient conditions for some time. The shape of the C1s peak is characteristic for this kind of contamination [98].

On the basis of this result (and other survey spectra for other samples, not shown), the energy bands corresponding to Ti, W, C, O and N were analyzed in more detail. These results are shown in Figure 49 for *(a)* 300 nm TiW and *(b)* 250/50 nm TiW/W samples (pre/post CNT growth).



(a)



(b)

Figure 49. X-ray induced photoelectron spectroscopy (XPS) results before and after CNT growth on *(a)* 300 nm TiW and *(b)* 250/50 nm TiW/W samples.

From these spectra, the relative density of the different elements can be estimated by carrying out a (semi) quantitative analysis. Although the peak heights are proportional to the different element concentrations, in order to compare them they have to be corrected for

the (different) relative sensitivities of the instrument for different elements. This sensitivity is expressed in the so-called 'atomic sensitivity factor' which is defined as 1 for fluor (F) [98]. By normalizing the peak heights on the atomic sensitivity factor, the relative concentration is calculated, which is shown in Table 8. Note that the different spectra in Figure 49 cannot be compared directly in a quantitative way, as the absolute electron yield (# of counts) is different for each measurement due to varying measurement circumstances.

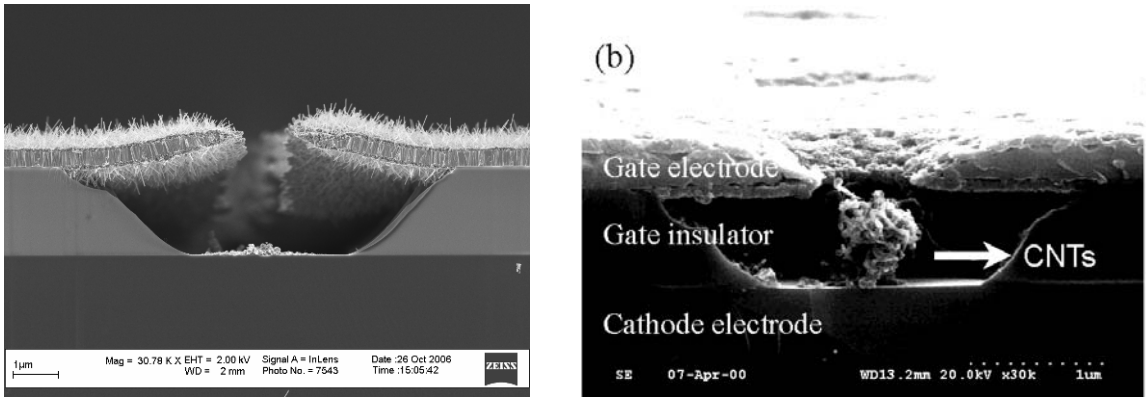
Table 8. Quantitative analysis on XPS data: relative element concentrations, data is an average of at least 4 measurements.

Element/electron	C1s	N1s	O1s	Ti2p	W4f	**C:W-ratio**
Atomic sensitivity factor	[0.314]	[0.499]	[0.733]	[2.077]	[3.863]	
300 nm TiW as-deposited	50.79	1.34	29.35	2.59	15.93	**3.2**
300 nm TiW CNTs	81.01	0.32	12.74	0.36	5.57	**14.5**
250/50 nm TiW/W as-deposited	43.08	1.72	31.26	0	23.94	**1.8**
250/50 nm TiW/W CNTs	86.82	0.55	9.73	0.07	2.83	**30.7**

It is observed that CNT samples have a much higher carbon concentration than as-deposited samples. In order to quantify this, the ratio of carbon vs. tungsten (C:W) is calculated and added in the final column. A dramatic increase in the C:W ratio is found for samples after CNT growth (factor 4,5 for TiW gate electrodes, a factor 17 for TiW/W gate electrodes).

On the basis of this result it is suggested that the nanotubes formed on the 300 nm TiW and 250/50 nm TiW/W gate electrodes during the CNT growth process are carbon nanotubes.

2.13.4.5 Comparison with literature



(a) *(b)*

Figure 50. Realised CNT based GFEAs (a) in this project and (b) by Lee et.al. [65].

The growth of CNTs on titanium-tungsten (TiW) or titanium-tungsten/tungsten (TiW/W) (gate) electrodes was unexpected. In section 2.2 different designs for CNT based GFEAs are discussed. Our design (Figure 50a) is quite similar to work published by Lee et. al. [65]. Lee used a (pure) tungsten gate on oxide (no adhesion layer was used or al least, not mentioned in the article) in combination with a nickel (Ni) catalytic layer deposited at the bottom of the cup (Figure 50b). However, no nanotubes are observed on his gate electrode. This may be due to the fact that no titanium is present in this layer (at least: not reported) and/or different conditions of CNT growth process. We grew CNT on nickel at atmospheric pressure at 700 °C in with 27/80 sccm C_2H_4/N_2 flows for 20 min (see section 2.13.1), whereas Lee used nickel in a C_2H_2/N_2 gas mixture at 10 Torr and 600-700 °C (no times or flows specified). The CNT growth process on the gate electrode is believed to be slowed down, or even terminates as a result of the difference in base pressure of more than a factor 100 (10 Torr = 7.5 mBar).

However, one might observe coverage of the gate electrode in Figure 50b by some material (not mentioned in the article), this might be amorphous carbon deposited during the CNT growth process, or some 'blocking' layer that encapsulates the gate electrode to prevent CNT growth. This is all very speculative and demonstrates the need for extra research to verify this assumption.

The literature was studied to find publications in which tungsten (or TiW) is used as catalyst for CNT growth. Extensive review articles like the one by Melechko et. al [39] do not mention tungsten as a catalyst for CNT growth processes. The only article found in literature in which tungsten is related to CNT growth found is published by (another) Lee et. al. [90] where well-aligned, high purity CNTs were synthesized using the catalytic reaction of C_2H_2 and $W(CO)_6$ mixtures. In this process $W(CO)_6$ powder is sublimated at 180 °C first, creating a $W(CO)_6$ vapour, from which, together with C_2H_2 and argon (Ar), CNT are grown at 950 °C [90]. This process differs so much from CNT growth from solid catalytic metals that it is not obvious or likely that study CNTs were grown on solid tungsten.

3 Testing field emitter devices

During the project, testing of realised field emitter arrays is considered. Although no testable devices were realized, a considerable amount of time was spent on the development of an experimental setup. In this section this work is summarized.

3.1 Setup

The realized gated field emitter arrays (GFEAs) are meant to be used in gaseous conditions. However, as previously shown in section 1.5, the emission characteristics will be affected by the gas exposure. In order to characterize the realized GFEAs properly, it is preferred to test them first in ultra high vacuum (UHV) and subsequently expose them to gases in a controlled way.

To perform this electrical characterisation, an UHV system is required. Therefore, we cooperated with the Systems and Materials for Information storage (SMI) group, where field emission experiments are carried out on arrays of STM tips [99] in an UHV system with a base pressure of ca. 10^{-9} Torr. To place the samples in the system and connect them with the measurement equipment, a dedicated chipholder with a CF flange is designed and realised and discussed in section 3.2.

In general, we are interested in the emission current (I_a) as a function of the gate voltage (V_g). The emission current is extracted from the cathode and the electrons are collected in a separate anode (stainless steel plate), placed above the array (in the chipholder), as shown in Figure 51. This anode is put at a large positive voltage with respect to the cathode to attract as many electrons as possible. Typical gate and anode voltages are estimated in the range of 100 V and 700 V, respectively, for this design [65][67].

When the gate voltage is applied, electrons can flow directly towards the gate and not to the anode, giving rise to a gate current (I_g). This current is measured as well.

Both gate en anode voltages and currents can be applied/measured simultaneously with two Keithley 2410 SourceMeter units, controlled by a computer with LabView interface.

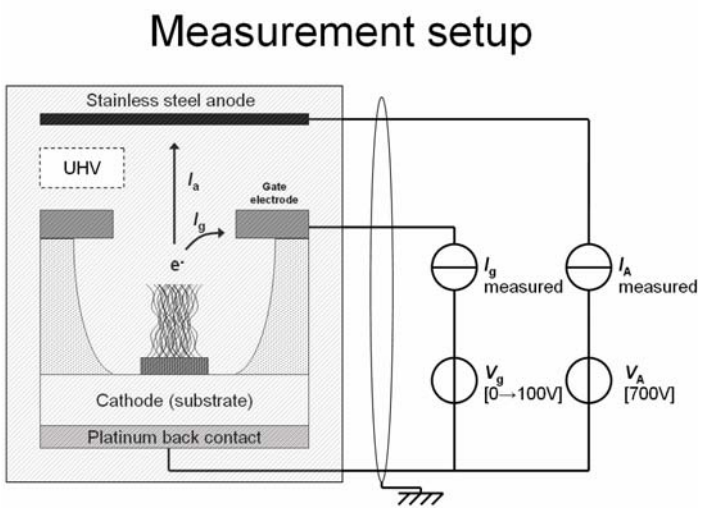


Figure 51. Overview of the measurement setup for field emitter experiments. The field emitter device is operated in ultra high vacuum (UHV) with a base pressure of approximately 10^{-9} Torr.

3.2 Chipholder

In order to get access to GFEAs, a chipholder is designed together with the mask design. The electronic connections from the chip (in UHV) to the measurement equipment were realized via a vacuum flange. The practical maximum number of electrical connections is 8, offered by the EFT0187053 flange of Kurt Lesker Co. Vacuum products [100]. The chipholder is mounted to this flange. This allows the measurement of several devices without breaking the vacuum (it takes more than a weekend to reach UHV in this particular system).

The challenge in this chipholder design was the constraint that it has to be operated in UHV of 10^{-9} Torr. This limits the materials that can be used as many materials have the tendency to release gases (outgassing) at these low pressures [64]. Furthermore, vacuum compatible solutions had to be found for for instance wire connections.

As the whole chipholder needed to fit through the flange access hole of Ø 37 mm, all parts had to be quite small and therefore the chipholder was further designed in cooperation with (and realized by) the 'Techno Centrum voor Onderwijs en Onderzoek' (TCO), a team of professional technicians.

This resulted in the chipholder shown in Figure 52.

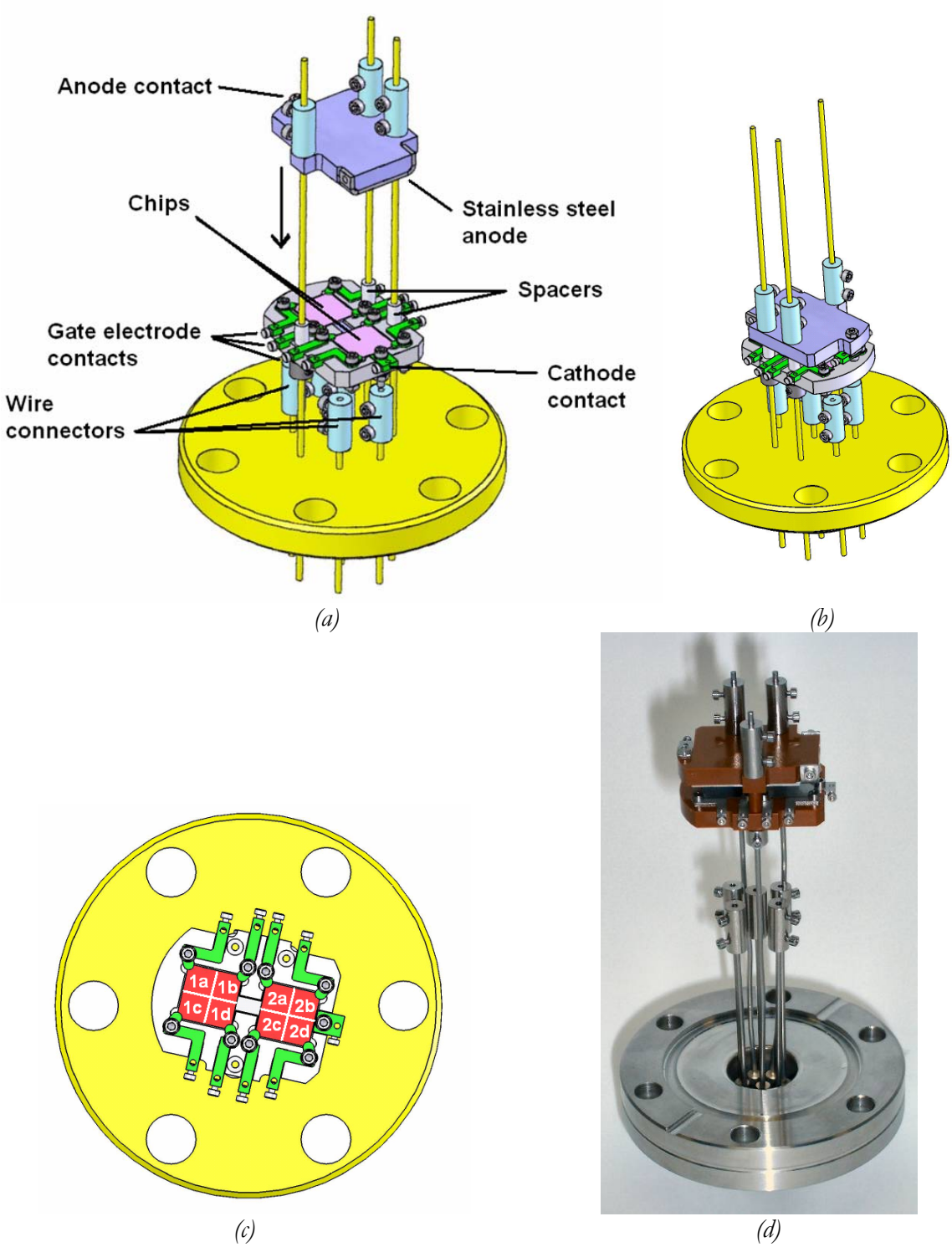


Figure 52. Overview of the chipholder design with *(a)* the anode moved up, *(b)* the anode positioned on the chip and *(c)* top view of the bottom section with chips (with subsections that are addressed individually) and contacts. Note that all electrical connections between the chipholder and the vacuum feedthrough are made with wires (not shown).
(d) Realized vacuum chipholder.

The stainless steel anode and cathode contacts are common for both chips. As there are only 8 pins available, 6 of the 8 gate electrode can be connected at the same time. The basic material of the chipholder is Meldin, a stable and insulation plastic that is compatible with UHV requirements. All other metal parts are stainless steel.

4 Summary and conclusions

The feasibility of gated field emitter field emitter arrays (GFEAs) as electron source of plasma chemistry on chip in microreactors is studied on the basis of literature. Several GFEA designs with emitter tips in the (sub) micron range are considered on the basis of their fabrication process and emission characteristics, including 'Spindt type' GFEAs with metal cathodes, silicon post emitter arrays and carbon nanotube (CNT) based GFEAs. The influence of gases on the emission characteristics is investigated, as well as the resulting emission current degradation which occurs as a result of tip oxidation, gas adsorption, tip sputtering and ion implantation in the tips. All these effects lead to a change in the emission current which is attributed to changes in the work function (φ) and geometric field enhancement factor (β) in the Fowler-Nordheim tunnelling function which is used to describe the emission current. Current recovery (partially) has been demonstrated by the exposure to hydrogen or methane and/or the restoration of the UHV after operation, leading to an extension of the FEA lifetime.

In general it is concluded that proper functioning of all GFEA designs cannot be guaranteed at pressures above 10^{-5} Torr. If the pressure in the microreactor is low enough, viz. in the 10^{-5} Torr range or lower, it is concluded that CNT based FEAs are most suitable as electron source in microreactors for the generation of reactive species, because of their relative high robustness against gases (chemical stability), high electrical (σ) and thermal ($\varkappa$) conductivities, high geometric field enhancement factor (β) and high Young's modulus (Y).

A CNT based GFEA is designed for fabrication within the cleanroom of the MESA+ research institute. The GFEA design is optimized for field emission in gaseous environments (robust). A basic GFEA is realised in which afterwards noodle shaped CNTs are to be grown selectively on a nickel (Ni) catalytic layer in a thermal chemical vapour deposition (CVD) process. This basic structure is a cup-like structure etched in a silicon oxide layer with a metal electrode of tungsten (W) and/or titanium-tungsten (TiW) on top. At the bottom of this cup, nickel is deposited as catalyst for CNT growth.

The CNT growth process is optimized for CNT growth in the realised cup by means of the temperature and time using (flat) dedicated silicon test samples with catalytic nickel sites only.

CNTs were grown on GFEA samples with TiW or TiW/W gate electrodes. After the growth process, no CNT growth was observed at the nickel catalytic sites at the bottom of the cups, but the gate electrodes were covered with large amounts of nanotubes. These nanotubes have completely different properties than CNTs grown on nickel catalysts. Their structural properties are investigated by HRSEM and TEM, while their composition is verified by XFS and XPS. It was found that they are carbon nanotubes with a diameter of ca 10 nm, grown via metal catalytic particles at the end of the tip. No conclusions could be drawn about the inner structure on the basis of the TEM results. On the basis of these results it is believed tungsten acts as a catalyst for this nanotube growth, but more research is required prove this.

Despite the design and realization of a chipholder for field emission experiments in ultra high vacuum (UHV), no experiments were carried out due a lack of successfully realized field emitter arrays with carbon nanotubes growth at the nickel catalyst at the bottom of the cups.

5 Recommendations

In this section several recommendations are made for future research. Critical design problems are summarized and solutions are suggested, which can be tested in extra research.

The recommendations are split in two parts; part one concerns the application of the current design as electron source for microreactors and the other part concerns the (deliberate) carbon nanotube (CNT) growth on (titanium)-tungsten (TiW/W) layers.

5.1 Application of the current design as electron source for plasma chemistry in microreactors

5.1.1 Tuning of the lithography

As found in section 2.7.2, the lithographic process used for the fabrication of gated field emitter arrays (GFEAs) is sub optimal in terms of resolution and uniformity, further research is required. The mask fabrication is near the limits of what is possible in standard masks fabricated at MESA+ (large arrays of uniform 2 μm holes). In case higher resolutions are needed, the mask fabrication (e-beam masks) by third parties is to be considered. Furthermore, the exposure dose can be optimized further for the positive resist, but switching to negative (image reversal) resist will enhance the lift-off and might solve resolution problems.

5.1.2 Etching of TiW

As found in section 2.9.2, the edges of TiW layers were not well defined as a result of patterning artefacts. These etching artefacts are most likely due to the formation of the (poor etchable) TiO_2. As suggested, this can be overcome by increasing the homogeneity of the TiW layer by optimizing the depositions conditions, adapting the etchant by the addition of ammonium acetate to modify the pH, as well as selecting the right target (optimal titanium/tungsten ratio). Therefore it is suggested to test the etching of TiW layers (with and without the modified etchant) that are sputtered (in the Oxford PL400) with higher power and at (perhaps) lower pressure.

5.1.3 CNT growth on nickel catalysts 'directly' on silicon

As found in section 2.12, CNT growth experiments were successful, but the nickel (Ni) and silicon (Si) were separated by 5-15 nm of (native) oxide, leading to a high ohmic contact, but this layer is prohibiting the formation of nickel silicides. This high ohmic contact is undesirable and needs to be avoided to ensure proper field emission from the CNTs.

It is suggested to test CNT growth on nickel deposited on silicon after a proper native oxide strip. In case these nanotube experiments fail, a suitable barrier layer has to be found which is compatible with the fabrication process. As this layer has to be deposited in preferably the same equipment (BAK600) as the nickel to prevent the formation of for instance TiO_2 in between the two depositions, the choice of materials is limited. Candidate materials include titanium (Ti) and tantalum (Ta). However, others, including Pirio and Teo, et. al. [66][67] deposited a barrier layer of 20 nm TiN via sputtering [66][67], followed by a nickel deposition via evaporation. It is suggested in section 2.12.2 sputtered barriers may lead

to electrical shorts between the gate electrode and the substrate, but based on the work by Pirio and Teo, it is worth trying.

5.1.4 Mechanical stability of the gate electrode during CNT growth

As found in section 2.13.3, the overlapping gate electrodes suffered from mechanical instabilities for gate holes Ø > 2 μm, most likely due to the large underetch of the gate electrode in combination with the thermal stresses induced by the CNT growth process at 700 °C for 20 minutes (plus ramp up/down). As the underetch is likely related to the stress in the metal thin film, the metal deposition process might be adapted to minimize the stress at room temperature. Furthermore, the mechanical instabilities at higher temperatures may be solved by decreasing the gate overlap by tuning the oxide etch. This can be done by means of a shorter etch time or via the incorporation of a lateral etch stop. Other solutions include increasing the (relative) gate layer thickness and/or the redesign the gate electrode on the basis of modelling of the thermal stress. Finally an alternative gate material may be selected which prompts the whole redesign of the current fabrication process.

5.1.5 Chemical stability of the gate electrode during CNT growth

As found in section 2.13.3, the TiW and TiW/W gate electrodes were found not to be chemically inert during the CNT growth process giving rise to undesirable CNT growth, thereby leading to the overgrowth of gate holes by CNTs. Solutions to this problem include changing the CNT growth parameters to terminate CNT growth on TiW/W and hopefully initiate CNT growth simultaneously on nickel. This might be achieved by lowering the pressure during deposition as suggested in section 2.13.4.5, but appears to be difficult with the current setup. It might be solved by using a completely different CNT growth process (PE-CVD), but this requires a complete new setup.

In order to terminate the CNT growth at the gate electrode, a completely different gate material might be used, like for instance poly silicon (see section 2.6.3), but it is expected that this will lead to a degradation of the robustness of the GFEA in gaseous environments. Other gate metals might be used as well, but many metals are known and used as catalyst in CNT growth process (see section 2.12.1). Molybdenum might be an interesting candidate but it needs to be investigated whether the wet etching of molybdenum is compatible with the current FEA fabrication process (viz. a single photoresist layer as etch mask for both metal and oxide etch step in combination with lift-off of the nickel afterwards).

5.2 Carbon nanotube growth on TiW/W layers

5.2.1 Verification of the element responsible for CNT growth

As found in section 2.13.4, there is still no hard proof whether the CNT growth on the TiW/W layer is due to titanium (Ti), tungsten (W) or a combination of the two (TiW).

This can be tested by exposing samples with (pure) tungsten to the CNT growth process. During this process, adhesion problems are expected, but principally speaking this experiment may be carried out with subsequent HR-SEM characterisation, and ignoring the adhesion problem.

Furthermore, TiW and TiW/W samples can be analysed by XPS (including depth profile) after a complete CNT growth run without opening the carbon source (C_2H_4) to check whether the titanium (Ti) diffuses towards the surface.

5.2.2 Analysis of the amorphous species between CNTs and the gate electrode

As found in section 2.13.3, after CNT growth an amorphous substance is observed between the CNTs and the gate electrode. This substance is of interest, for instance in case these CNT would be applied for field emission, the electrical conduction of this layer is important. This analysis can be carried out by making a depth profile using XPS (removing the CNT layer gradually via sputtering).

5.2.3 Characterisation of the growth process

In order to exploit these CNTs for intended applications, viz. field emission or catalyst support [91][97], the growth process has to be characterized in more detail, as a function of growth temperature, time and gas pressure. It is not obvious whether patterned TiW layers on different substrates will initiate the same CNT growth as it is appears to be related to the flow pattern of the gases (see section 2.13.3.1, Figure 42a).

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Appendix A: Complete process flow