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Design of an Oscillator for Satellite Reception

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Abstract

This thesis presents research on an *LC*-oscillator for Ku-band (10.7-12.7GHz) satellite reception. The zero-IF receiver architecture, proposed in the joint project involving the University of Twente and NXP Research, requires a 11.7GHz quadrature oscillator that achieves a phase noise of -85dBc/Hz@100kHz and an IRR of 30dB. Such an oscillator was designed in an NXP 65nm CMOS process.

The performance of three types of *LC*-oscillators was compared: the Colpitts topology, the cross-coupled pair topology and a new topology, the crossed-capacitor oscillator. Both single and quadrature oscillator simulations were compared. Although the cross-coupled pair topology can achieve the highest FoM and the quadrature crossed-capacitor oscillator can achieve the highest IRR, the Colpitts oscillator was selected and developed, due to its reasonable IRR performance and its ability to run at a higher supply voltage than the cross-coupled pair oscillator, allowing sufficient phase noise performance.

Development includes the design of a suitable buffer, a frequency tuning mechanism, and circuitry allowing the measurement of oscillation frequency and quadrature accuracy. Simulated performance and schematics are presented.

Contents

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Preface

At the beginning of 2007, I knew almost nothing about satellite receivers, so when Bram Nauta suggested, for the Master's thesis, work on a CMOS satellite receiver at **NXP Research** in Eindhoven, I thought it would be an interesting challenge. And it was, from the start of the project on March 15 until the end. It was a privilege to have as a daily supervisor as competent a man as Domine Leenaerts; Domine, thank you for teaching me so many things that are found in no textbook.

The final chip makes use of work from various other people. I would like to thank the people at the IRFS group of **NXP Research** for supplying the project with designs, discussions, and suggestions.

Finally, I must apologize to any potential reader that this report is so limited in both scope and content. There is much more to be said about integrated oscillators in general and the project in particular.

Frank Leong
Enschede, September 22$^{\text{nd}}$, 2007

Das rein intellektuelle Leben der Menschheit besteht in ihrer fortschreitenden Erkenntnis mittelst der Wissenschaften und in der Vervollkommnung der Künste, welche Beide, Menschenalter und Jahrhunderte hindurch, sich langsam fortsetzen, und zu denen ihren Beitrag liefernd, die einzelnen Geschlechter vorübereilen. Dieses intellektuelle Leben schwebt, wie eine ätherische Zugabe, [...] über dem weltlichen Treiben, dem eigentlich realen, vom Willen geführten Leben der Völker, und neben der Weltgeschichte geht schuldlos und nicht blutbefleckt die Geschichte der Philosophie, der Wissenschaft und der Künste.

– Arthur Schopenhauer

A science is said to be useful if its development tends to accentuate the existing inequalities in the distribution of wealth, or more directly promotes the destruction of human life.

– Godfrey Harold Hardy

Chapter 1

Introduction

Nowadays, many homes have access to television broadcasts, which are usually received using a fixed terrestrial coaxial cable. Terrestrial antenna solutions have generally been avoided, as they suffer from interference; digital standards are changing this. Another option is receiving broadcasts using a satellite dish, pointed at a satellite in space on a geosynchronous orbit in the Clarke Belt, which does not require a dedicated cable from a broadcasting node to the home and therefore gives the television viewer an additional degree of flexibility.

Although picture quality from satellite receivers is generally considered very good, the equipment is relatively expensive, as many required analog components are quite exotic. High electron-mobility transistor (HEMT) amplifier modules are required to achieve the desired noise level and dielectric resonator oscillators (DRO) are required to achieve the desired spectral purity in the downconversion stage. In addition, these components are only available as discrete building blocks, so some microwave engineering is required to minimize losses and interference in the layout of the high-frequency part. Furthermore, the Low-Noise-Block (LNB) and the decoder are generally seperated into what are known as Out-Door-Unit (ODU) and In-Door-Unit (IDU). These two parts are connected by a (lossy) cable, commonly a popular type such as RG-59/U (loss: 8.2dB/30m@1GHz) or RG-11/U (loss: 4.3dB/30m@1GHz), with (lossy) F-connectors mounted at the ends. The cable usually feeds a DC voltage of 14V or 18V to the LNB, necessitating an additional supply line in the decoder. For these reasons, a satellite receiver is far more costly to produce and install than an ordinary television tuner.

For a long time now, CMOS processes have been continuously downscaling to ever smaller (minimum) transistor lengths and thinner gate oxides, resulting in faster and more accurate ADCs. We are at a point where direct conversion of the entire Ku-band has become an option. Without intermediate IF-stages, slightly weaker oscillator performance figures can be tolerated and making the entire RF-to-baseband conversion in one reasonably-sized CMOS chip is therefore an option. With a one-chip CMOS satellite solution, production and installation costs of satellite receivers would drop significantly, flexibility due to integration potential would increase (a Wi-Fi signal could come straight from the dish) and consequently satellite receivers could become even more popular than they are today, fitting into the general trend of the wired-to-wireless shift (e.g. USB to UWB and LAN to WLAN). Imagine watching satellite TV on your PDA (see Figure 1.1) or an entire hotel with thousands of guests requiring only one satellite dish!

The focus of this report is the development of a suitable, digitally controllable, oscillator.

Figure 1.1: Satellite receiver as part of the wireless home network.

For direct conversion, a quadrature oscillator is required, which locks onto an external quartz crystal by means of a Phase-Locked Loop (PLL).

The oscillator is designed in a 65nm CMOS process. While this process provides large amounts of transconductance gain due to high gate oxide capacitance and the high W/L ratios that are possible with the nominal channel length of 60nm, reliability issues form a bottleneck; DC voltages over the gate oxide of only 1.2V are allowed. In addition, short-channel effects give the minimum-length transistors highly nonlinear output impedances and the interconnect can introduce very substantial parasitics. All these factors make it challenging to design a robust oscillator. Where normally the focus of an oscillator design is on power consumption, the main concern in this project is simply to be able to meet the performance requirements.

The report is built up as follows. First, an overview of the assignment and the satellite system is given in Chapter 2. Chapter 3 reviews basic oscillator theory and some relevant additions that have emerged in both the literature and the current work. The buffer is described in Chapter 4. Next, Chapter 5 presents the inductor model and design, followed by a description of the frequency tuning in Chapter 6. In Chapter 7 the final design, layout and simulation results are presented, which are compared with literature in Chapter 8. Chapter 9 summarizes the findings and gives some recommendations for improvements.

Chapter 2

Assignment Overview

The focus of this report is on an oscillator, which is intended to be part of a larger zero-IF receiver system. Schematically, this is shown in Figure 2.1. The LO block, including the 90 degree phase shift, is the subject of this work.

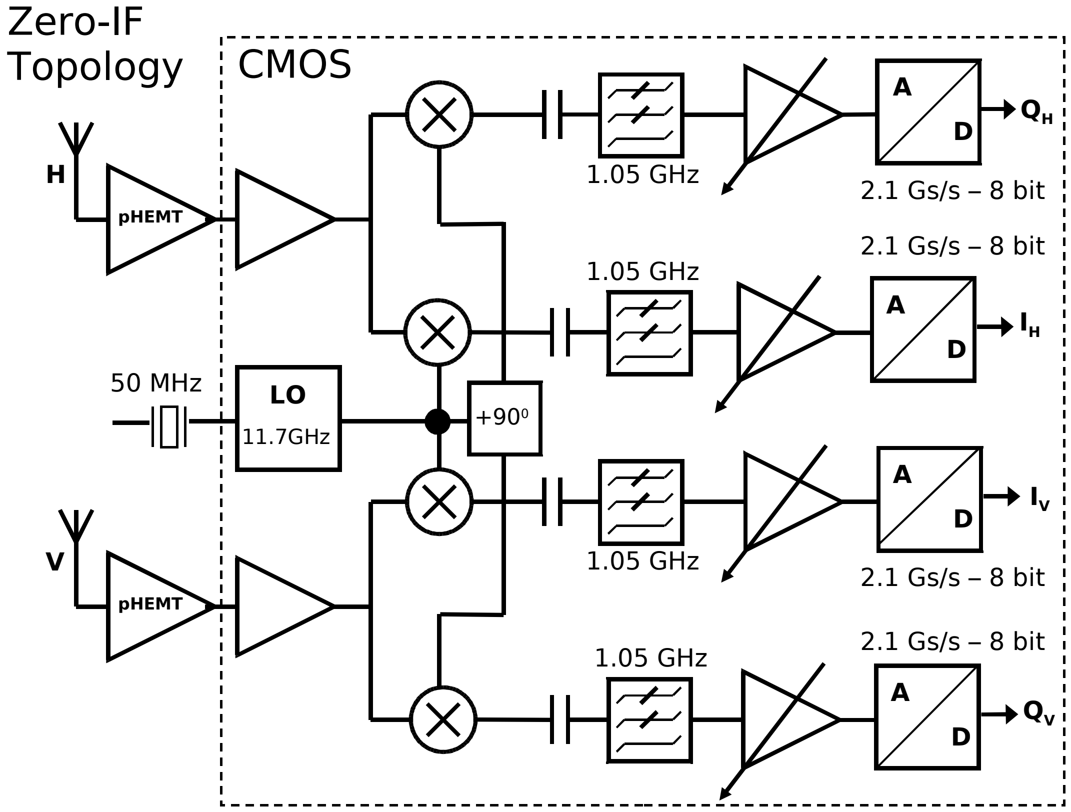
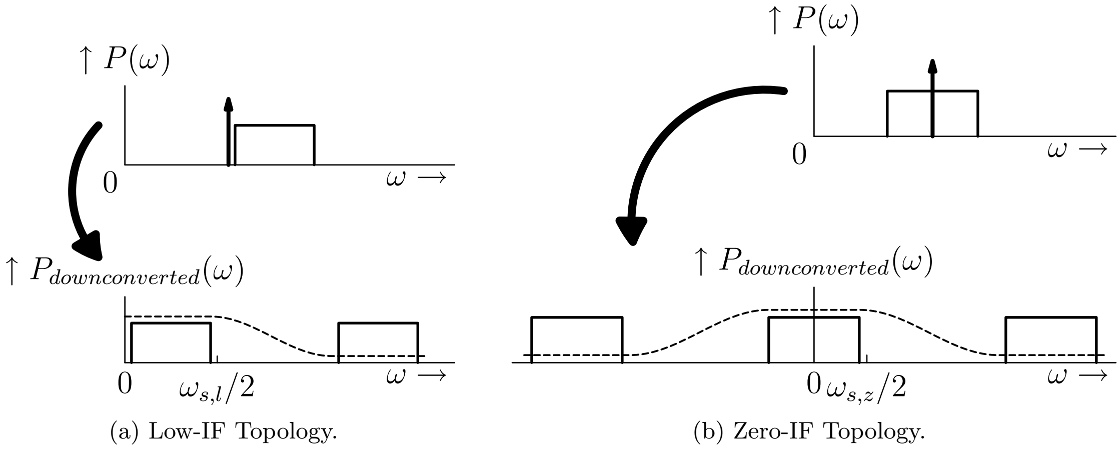


Figure 2.1: Zero-IF satellite receiver block model.

The zero-IF structure requires two ADCs per signal chain instead of one, but the required bandwidths of the ADCs are only approximately half as large as the required bandwidth of an ADC in a low-IF solution. This is depicted in Figure 2.2.

Oscillators have been part of RF receivers since Armstrong patented the superheterodyne receiver in the year 1919. Since then, the qualities of quartz-based oscillators have been appreciated and many current oscillators depend on such crystals for frequency consistency. As quartz crystals resonate only at a very limited set of frequencies, receivers are generally



(a) Low-IF Topology.

(b) Zero-IF Topology.

Figure 2.2: Spectra due to downconversion in two different schemes. The rectangular blocks represent the signal spectrum of the Ku-band, the arrows the LO frequencies, and the dotted lines the anti-aliasing filters preceding the ADCs. Clearly visible is the difference in minimum sampling rate; a lower rate also simplifies filter design.

built using a higher-frequency voltage-controlled *LC*- or ring-oscillator, connected through a frequency divider in a Phase-Locked Loop (PLL) with the crystal. This method combines the flexibility of *LC*-/ring-oscillators with the good temperature/drift properties of the quartz crystal.

For a satellite receiver, good spectral purity is required to meet specifications (from experience, a phase noise of -85dBc/Hz@100kHz or better is considered necessary for a VCO in a PLL) and therefore a common LNB uses a DRO that performs very well, but is quite costly to fabricate and calibrate in comparison with an integrated solution. The challenge in this project is to create an on-chip oscillator that can replace this component and is made in CMOS for large-scale integration.

The set of components that are available on-chip is rather limited. Fortunately, it is possible to make high-quality inductors and accurate models exist to describe them [4]. In addition, several varieties of transistors, capacitors and resistors exist. The inductors consume the most area and place the most constraints on the rest of the architecture. Therefore, the inductors are designed first, with the rest of the circuit matched to the inductor's unavoidable parasitics. As the inductor design is rather involved by itself, this step is described separately in Chapter 5. The influence on the oscillator of potential inductor parasitics is described first, in Chapter 3. That chapter is followed directly by a description of one of the most power-hungry circuit blocks, the buffer, in Chapter 4. The last circuit block to be described is the frequency tuning mechanism in Chapter 6, as it is designed last.

As can be seen in Figure 2.1, the oscillator is not directly in the signal path of the satellite receiver. Nonetheless, its properties have a huge influence on the quality of the signal that is fed into the ADC, since any impurities in either frequency, phase or amplitude (of course amplitude information is less relevant in case of a hard-switching mixer) will be transferred to the signal in the mixer stage. Especially since the system is of the zero-IF type, the oscillator is important, as the quadrature angle might limit the performance of the receiver.

The analysis of the quadrature downmixed signal outputs, for both positive and negative angular frequency offsets, makes use of the trigonometric identity

$$\cos(u)\cdot\cos(v) = \frac{1}{2}\Big[\cos(u-v) + \cos(u+v)\Big] \tag{2.1}$$

and follows below. The approximations are valid if the output signal is lowpass filtered, i.e. components around twice the oscillator frequency are removed.

$$\begin{aligned}
\cos(\omega_0\cdot t + \Delta\omega\cdot t)\cdot\cos(\omega_0\cdot t) &= \frac{1}{2}\Big[\cos(\Delta\omega\cdot t) + \cos(2\omega_0\cdot t + \Delta\omega\cdot t)\Big] \\
&\approx \frac{1}{2}\cos(\Delta\omega\cdot t). &(2.2)\\
\cos(\omega_0\cdot t + \Delta\omega\cdot t)\cdot\cos(\omega_0\cdot t + \frac{\pi}{2}) &= \frac{1}{2}\Big[\cos(\Delta\omega\cdot t - \frac{\pi}{2}) + \cos(2\omega_0\cdot t + \Delta\omega\cdot t + \frac{\pi}{2})\Big] \\
&\approx \frac{1}{2}\cos(\Delta\omega\cdot t - \frac{\pi}{2}). &(2.3)\\
\cos(\omega_0\cdot t - \Delta\omega\cdot t)\cdot\cos(\omega_0\cdot t) &= \frac{1}{2}\Big[\cos(\Delta\omega\cdot t) + \cos(2\omega_0\cdot t - \Delta\omega\cdot t)\Big] \\
&\approx \frac{1}{2}\cos(\Delta\omega\cdot t). &(2.4)\\
\cos(\omega_0\cdot t - \Delta\omega\cdot t)\cdot\cos(\omega_0\cdot t + \frac{\pi}{2}) &= \frac{1}{2}\Big[\cos(\Delta\omega\cdot t + \frac{\pi}{2}) + \cos(2\omega_0\cdot t - \Delta\omega\cdot t + \frac{\pi}{2})\Big] \\
&\approx \frac{1}{2}\cos(\Delta\omega\cdot t + \frac{\pi}{2}). &(2.5)
\end{aligned}$$

This results in the **I** and **Q** output signals, given in (2.6) and (2.7), for input signals with respectively positive and negative angular frequency offsets from the LO frequency. Note that, in principle, it makes no difference if the signal is in quadrature (difficult to achieve over a wide frequency band with the desired noise figure) or the oscillator is in quadrature.

$$+\Delta\omega: \qquad \mathbf{I}\approx\frac{1}{2}\cos(\Delta\omega\cdot t), \qquad \mathbf{Q}\approx\frac{1}{2}\cos(\Delta\omega\cdot t - \frac{\pi}{2}). \tag{2.6}$$

$$-\Delta\omega: \qquad \mathbf{I}\approx\frac{1}{2}\cos(\Delta\omega\cdot t), \qquad \mathbf{Q}\approx\frac{1}{2}\cos(\Delta\omega\cdot t + \frac{\pi}{2}). \tag{2.7}$$

Therefore it simply remains to implement a 90 degrees phase shifter to distinguish between positive and negative frequency offsets. If the **Q** signal is shifted by $+\frac{\pi}{2}$ and added to the **I** signal, the signal with positive frequency offset will be transferred and the signal with negative frequency offset will be added to its 180 degrees shifted version, resulting in zero output. The opposite happens for a $-\frac{\pi}{2}$ phase shift in the **Q** path, or, perhaps more convenient, a $+\frac{\pi}{2}$ phase shift in the **I** path. The latter solution is easily implemented by a Hilbert transformer that can be switched between the **I** and the **Q** paths. The principle is illustrated in Figure 2.3. The phase shifters are easily implemented digitally, where they can be used in parallel, such that the whole band can be received all the time.

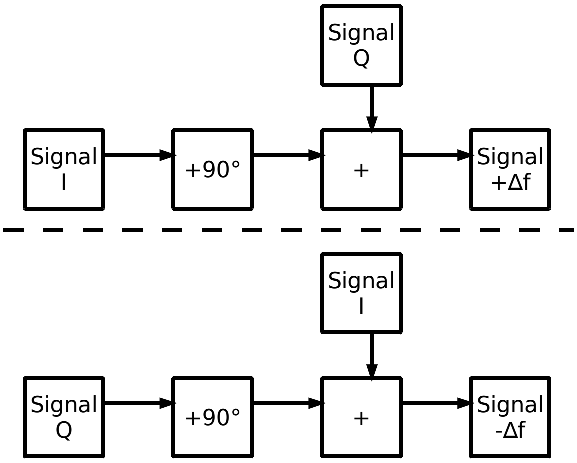


Figure 2.3: Switching of the phase shifter to receive both upper and lower band.

Of course the angle of 90 degrees between the different oscillator outputs is in reality not perfect and there will also be a certain amplitude mismatch between the different oscillator outputs. This means that a certain amount of leakage can occur from negative to positive frequency offsets and vice versa, causing distortion of the desired signal by an unwanted *image*. The quality of the quadrature angle and the amplitude mismatch determine the so-called Image-Rejection Ratio (IRR). It is defined as follows (as in, for instance, [17]), where ϵ is the relative amplitude mismatch and ϕ is the phase deviation from perfect quadrature in radians.

$$IRR = \frac{P_{sig,out}}{P_{im,out}} \times \frac{A^2_{im,in}}{A^2_{sig,in}} \approx \frac{4}{\epsilon^2 + \phi^2}. \tag{2.8}$$

In practice, the mixers are clipping, making the outputs dependent only on the zero-crossings of the inputs, eliminating amplitude mismatches and therefore making the IRR dependent solely on ϕ. From previous experience, a goal of 30dB IRR (corresponding to a quadrature accuracy better than 3.62 degrees) is set.

Although *RC* polyphase filters may be used to derive 90 degrees phase shifted outputs from a single oscillator [25] [26], these filters generally require more power due to additional buffering and suffer from relatively poor IRR due to process spread, very unfavorable in bulk CMOS, and component mismatch, consequence of the small time constants necessary in this project. Therefore this type of solution was not investigated further.

In principle, it is also possible to generate quadrature signals from a single oscillator running at twice the required output frequency. Two dividers, one triggered by the positive edges of the oscillator, and the other triggered by the negative edges of the oscillator, produce quadrature outputs. In practice, dividers with coils produce spurs on the oscillator, and dividers without coils can be considered as injection-locked RC-oscillators, with a very large power consumption for the desired frequency and noise level. In addition, this solution is very sensitive to transistor mismatch and layout parasitics, making it very difficult to achieve an accurate quadrature angle. For the above reasons, this option was not developed.

The quadrature accuracy cannot be measured properly off-chip. Because a cable length asymmetry of 1cm will already introduce approximately 50ps of propagation delay difference [18, p. 18], and the oscillator period is approximately 85ps, the equipment will measure the setup, rather than the oscillator.

By adding a mixer on-chip to downmix the quadrature to a frequency near DC, the quadrature angle will still be contained in the output signals (inspecting (2.2) and (2.3) will yield this result) and can be measured without any relevant cable delays. For this reason, two test circuits are designed in this assignment: one to measure the frequency, as shown in Figure 2.4, and one to measure quadrature accuracy, as shown in Figure 2.5. Note that the frequency of the oscillator is controlled digitally; the oscillator is therefore classified as a Quadrature Digitally Controlled Oscillator (QDCO).

To summarize, the goals of the work are as follows:

- Design a suitable ($\mathcal{L}$(100kHz) $= -85$dBc/Hz, 30dB IRR) oscillator at 11.7GHz;
- Include a frequency tuning mechanism that can be interfaced to a PLL to make the frequency accurate and stable;
- Design a suitable chip buffer to drive the PLL phase detector, mixers, and line drivers;
- Make a top-level test layout that allows the concept to be measured properly.

The oscillator is to be fabricated in a baseline 65nm CMOS process (allowing a DC voltage of 1.2V across gate oxides and a maximum RF swing exceeding this voltage by approximately 50%) with the option of a second gate-oxide process step (GO2), allowing the use of 2.5V MOST devices in the design.

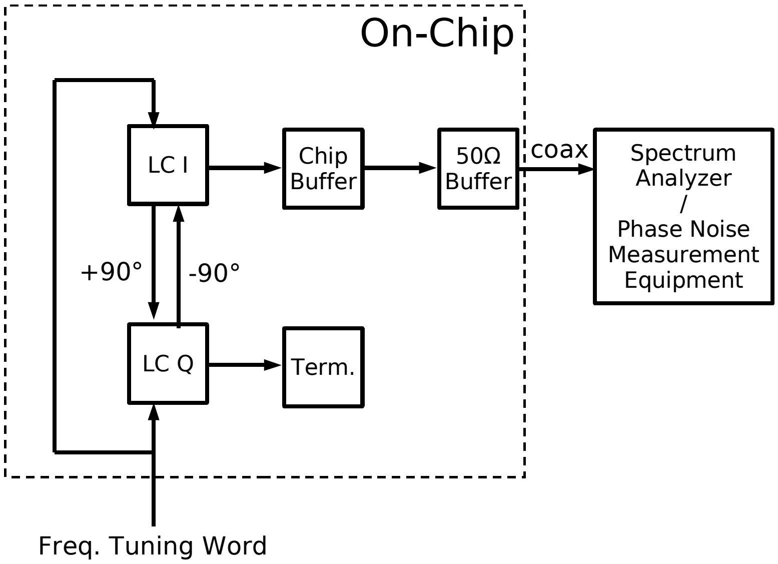


Figure 2.4: QDCO phase noise and frequency tuning measurement setup.

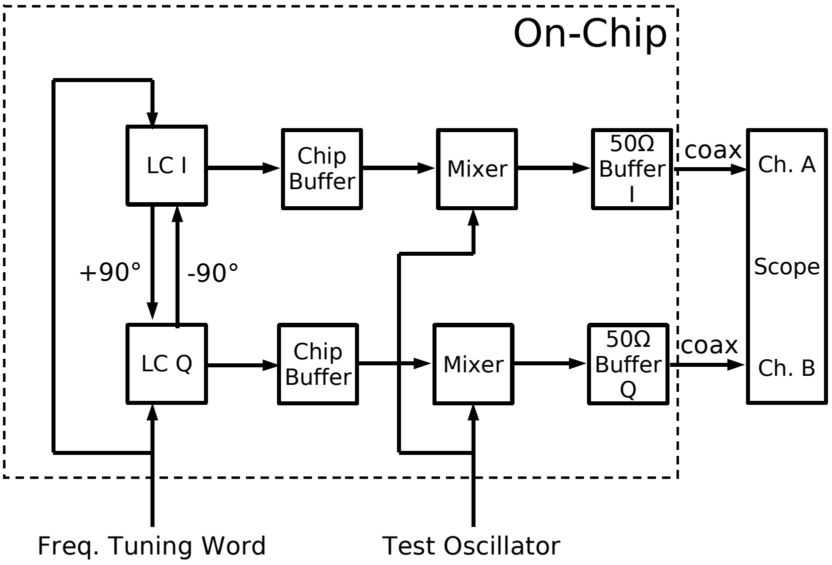


Figure 2.5: QDCO quadrature angle measurement setup.

Chapter 3

Oscillator Models

In this chapter, first abstract circuit models relevant to oscillator design are presented in Section 3.1, followed by specific implementations of single and quadrature oscillators in Sections 3.2 and 3.3, respectively.

3.1 General Aspects of Oscillators

There are basically two types of oscillator, RC-oscillators, such as ring-oscillators based on inverters, and LC-oscillators (crystals are in fact modeled as LC-resonators). Both are applied in ICs, but RC-oscillators have inferior phase-noise performance at a given power budget and are therefore not very good candidates for this project.

LC-oscillators work on a rather intriguing principle, illustrated in Figure 3.1.

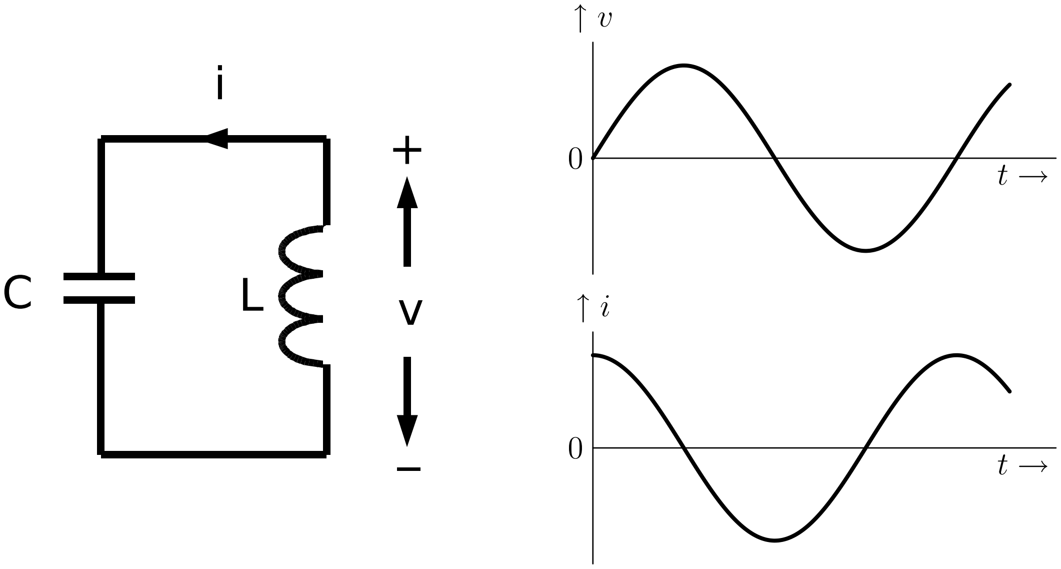


Figure 3.1: Basic LC oscillator tank with waveforms for a certain initial current.

For a certain resonance frequency, the impedance of the parallel LC-tank becomes infinite (equivalently, its series impedance becomes zero!) and when energy is stored in the tank, it circulates from voltage energy in the capacitor ($\frac{1}{2}Cv^2$) to current energy in the coil ($\frac{1}{2}Li^2$)

and vice versa, at precisely the resonance frequency $\omega_0 = 1/\sqrt{LC}$, with the voltage and current being sinusoidals in quadrature phase with respect to each other[1] and the ratio of voltage and current amplitudes being $V_0/I_0 = \sqrt{L/C}$. By copying either the current or the voltage, other circuits can be operated at a frequency that can be precisely controlled by dimensioning of the tank components.

3.1.1 Tank Losses and Impedance Transformations

In the real world, ideal reactive components do not (yet) exist and there are always losses, usually modeled as a series resistance. This series resistance causes a reactive component to have a total impedance described as $Z_{total}(\omega) = R(\omega) + jX(\omega)$ and a frequency-dependent quality factor Q defined as $Q(\omega) = |X(\omega)/R(\omega)|$.

It is very practical to unite all the losses in one resistor. With an impedance transformation [17, pp. 50–52], if only narrowband signals (such as that of an oscillator) are considered, the series resistances R_s of high-Q reactive components may be converted to parallel resistances R_p, as shown in Figure 3.2. Conveniently,

$$R_p \approx Q^2 R_s \tag{3.1}$$

in both the cases of the inductor and the capacitor. These parallel resistances are then easily combined into a total equivalent parallel resistance R_T. The impedance transformation is an indispensable tool for simplifying analysis of high-Q/low-noise oscillators at GHz frequencies, as will become clear throughout this report.

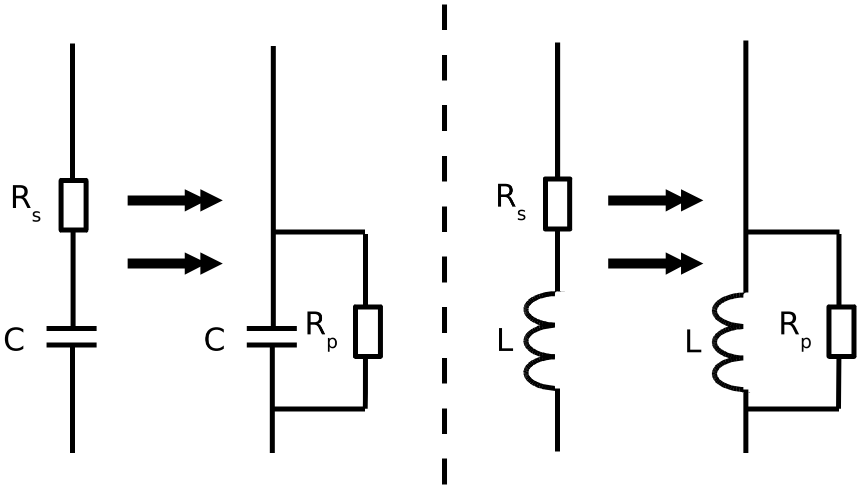


Figure 3.2: Passive impedance transformations to preferable parallel forms.

[1] This is the only solution for constant tank energy. Whether the current leads or lags the voltage depends on the reference directions. The fundamental equation of one of the components must be reversed, determining the sign of the final equation! Unfortunately, the quadrature angle between current and voltage is very difficult to copy accurately in practice.

The total resistance is compensated by a "negative resistance" to make sustained oscillations at the desired frequency. A large parallel resistance requires less compensation (less injected current) and is therefore preferable. Another way of putting this, is to say that the quality factor of the tank is higher for a larger parallel resistance, where the quality factor of the tank is defined [1, pp. 88–90] as

$$Q_{tank} = \frac{R_T}{\sqrt{L/C}}. \tag{3.2}$$

Note that the noise in the system is in principle only due to the finiteness of the tank Q, whereas in an RC-oscillator, the noisy resistor is an integral part of the operating principle.

3.1.2 Startup

It is important to be sure that an oscillator actually starts up and, if it does so, to know by which margin. For this purpose, the oscillator (especially its small-signal equivalent) can be split into an active part and a passive part, as in Figure 3.3.

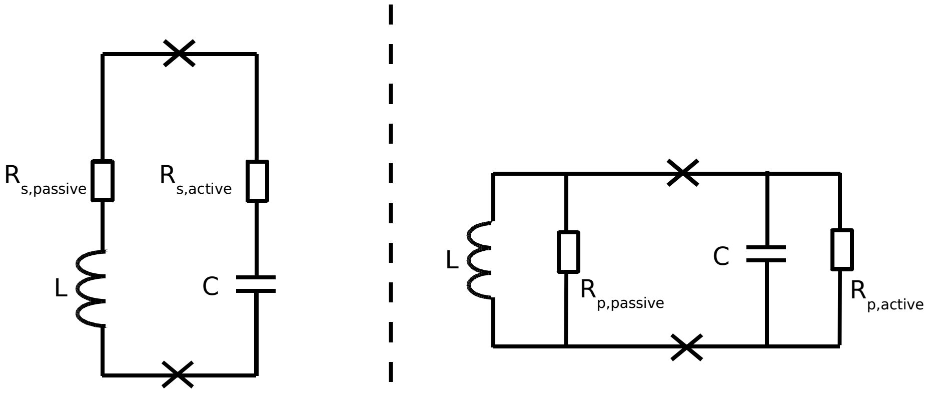


Figure 3.3: Splitting the oscillator up to determine starup ratio; crosses indicate where the circuit is cut open for small-signal analysis.

The inductor is chosen as the passive part, whereas the capacitance is considered part of the active part. This allows easy analysis of all the topologies under study. The startup ratio for the series form and the parallel form, respectively, are given below.

$$\text{Startup ratio (series)} = \frac{-R_{active}}{R_{passive}}. \tag{3.3}$$

$$\text{Startup ratio (parallel)} = \frac{-R_{passive}}{R_{active}}. \tag{3.4}$$

It is usually enough if the startup ratio exceeds 1, but for unfamiliar oscillators a safety margin is usually adopted in the design, such that the startup ratio exceeds 2.

3.1.3 Phase Noise

Both the (equivalent) parallel resistance R_T and the active device to compensate the losses generate noise. The active device usually contains also an output resistance R_{ds} which it must compensate for additionally. This situation is depicted in Figure 3.4.

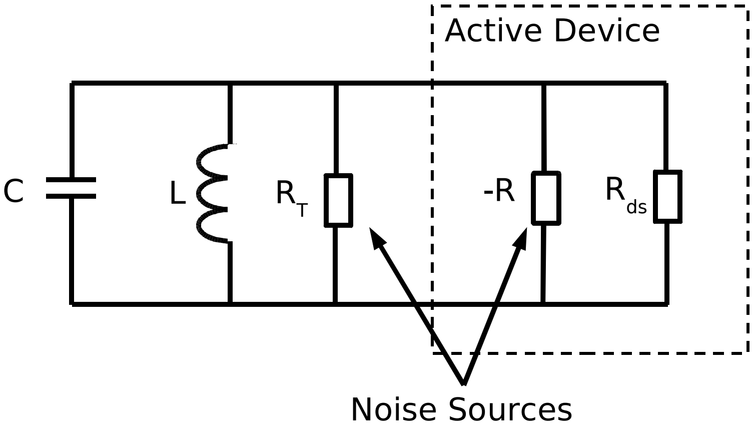


Figure 3.4: Abstract view of noise contributions in an LC-oscillator.

The resistances and the active device generate thermal noise, which is usually modeled as white noise with noise current densities $\overline{i_R^2} = \frac{4 \cdot k_B \cdot T}{R} \Delta f$ and $\overline{i_{ds}^2} = 4 \cdot k_B \cdot T \cdot \gamma \cdot g_m \cdot \Delta f$, respectively. γ varies from process to process, but can generally be assumed to be in the order of $\frac{2}{3}$ (a bit larger for short-channel devices, see for example [15]). In addition, small CMOS devices contribute significant amounts of $1/f$ noise. The noise current transfer function of an LC-oscillator contains an additional $1/f^2$ term for the sidebands [3] and the output buffers generate a flat white noise floor. This gives rise to three phase noise regions, the $1/f^3$, $1/f^2$, and *flat* regions (named after their slope), in the oscillator's frequency spectrum near the oscillation frequency, depicted in Figure 3.5 for the situation without amplitude noise. Note that the spectrum is in principle symmetrical around the oscillation frequency for small offsets (phase noise is equally likely to cause both positive and negative frequency shifts); this fact is rarely mentioned explicitly in the literature.

The proper relationship between the oscillator's Power Spectral Density (PSD) spectrum and the Single-Sideband (SSB) phase noise spectrum is given in [12] as

$$\mathcal{L}(f) = \frac{\mathbf{S_X}(f_c + f)}{P_s}, \tag{3.5}$$

where f_c is the oscillation frequency in Hz, $\mathbf{S_X}(f_c + f)$ is the oscillator's PSD in W/Hz centered around the oscillation frequency (neglecting amplitude noise), and P_s is the total power in the spectrum. In [12] it is suggested to calculate the total power as

$$P_s \approx \int_{\frac{1}{2} f_c}^{\frac{3}{2} f_c} \mathbf{S_X}(f) df. \tag{3.6}$$

This definition allows easy conversion from measured power on a spectrum analyzer (or other equipment) to SSB phase noise.

Calculating SSB phase noise spectra (properly) by hand is extraordinarily difficult. In this report, first-order approximations are used/made that reflect the method described in [3]. This method has its limitations, especially when describing injection-locking phenomena [13], where the method proposed in [11] yields more acceptable results. Even the latter method, although already extremely challenging to apply intuitively, is limited, especially for colored noise sources such as $1/f$ noise from MOSFETs [14]. Apparently, it is surprisingly difficult to understand a circuit consisting of only two passive elements and a colored noise source!

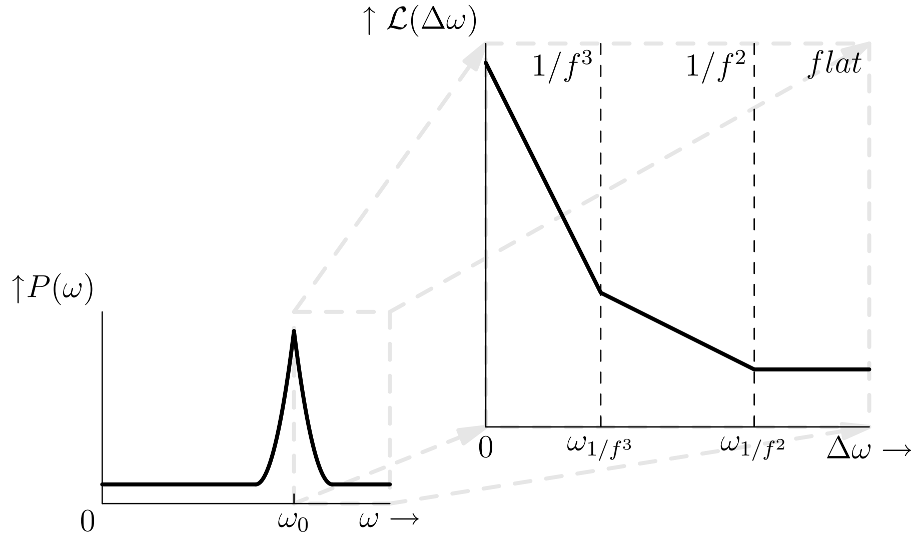


Figure 3.5: Idealised sketch of the phase noise regions generally present in most integrated oscillators, excluding amplitude noise.

The goal in this project is to achieve a phase noise of -85dBc/Hz@100kHz. Of course it is better if the oscillator consumes less power, so in literature often a reference is made to a Figure of Merit (FoM, expressed in dB – simply put, a higher FoM is better). The common FoM definition is given below, where ω_0 is the oscillation angular frequency, $\Delta\omega$ is a frequency offset somewhere in the $1/f^2$ phase noise region and P_{diss} is the amount of dissipated power.

$$\text{FoM} = -\mathcal{L}(\Delta\omega) + 20{\cdot}\log_{10}\left(\frac{\omega_0}{\Delta\omega}\right) - 10{\cdot}\log_{10}\left(\frac{P_{diss}}{1\text{mW}}\right). \tag{3.7}$$

By definition, $\Delta\omega$ is chosen in the $1/f^2$ region to allow fair comparison of performance between different oscillators. In this project, this is not an absolute measure of performance, because the $1/f^3$ region may limit the oscillator performance, which is determined by integrating the total PLL phase noise over the unwanted interferers, which are in this case the adjacent channels inside the Ku-band itself. This integral is far from straightforward to calculate, also including terms for quadrature mismatch and baseband processing inaccuracies, which is why the goal is set as a target phase noise at a specified offset. From experience it is concluded that this phase noise target yields a functional receiver system.

3.2 Specific Oscillator Types

3.2.1 Cross-Coupled Pair and Colpitts Oscillators

There are two popular ways to compensate the tank losses. One way is to cross-couple a differential pair's gates and drains to the tank. This method very closely approximates the transient properties of an ideal negative resistance. Another way to compensate the losses is by periodically injecting a burst of charge into the tank. An oscillator topology which does this very nicely is the Colpitts oscillator. Both the cross-coupled pair (XCP) oscillator and the differential Colpitts oscillator are shown in Figure 3.6.

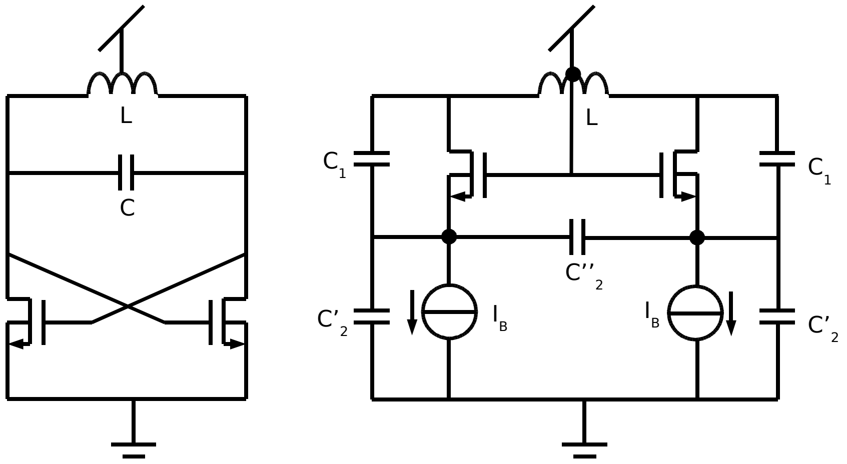


Figure 3.6: Schematics of cross-coupled pair (left) and Colpitts (right) oscillators.

A lot of research has gone into these oscillator topologies, and closed-form solutions for CMOS implementations of both oscillators have been obtained [5]. They are repeated in (3.8) and (3.9), where $\mathcal{L}_{x-pair}(\Delta\omega)$ and $\mathcal{L}_{colpitts}(\Delta\omega)$ are the phase noise densities in the $1/f^2$-region (due to thermal noise) at angular frequency offset $\Delta\omega$ for the XCP and Colpitts oscillator, respectively. k_B is Boltzmann's constant, T is absolute temperature, $N = 2$ for a differential oscillator, A_{tank} is the oscillation amplitude, C is the tank capacitance, R_T is the total equivalent resistance in parallel to the tank, I_B is the tail current (for an oscillator with tail current source), Φ is half the conduction angle of the Colpitts transistors (usually quite a small value), γ is the MOSFET noise factor described earlier, n the capacitive divider ratio, and g_{mT} the admittance of a noisy bias source. For $\gamma = \frac{2}{3}$, true for long-channel MOSTs, and in the absence of the noisy bias source, the optimum value of n can be shown to be approximately 0.3. This has been confirmed by simulation to also hold for short-channel devices in single differential Colpitts oscillators.

$$\mathcal{L}_{x-pair}(\Delta\omega) = 10\log\left[\frac{k_B{\cdot}T}{N{\cdot}A_{tank}^2{\cdot}C^2{\cdot}\Delta\omega^2{\cdot}R_T}(\gamma+1)\right]. \tag{3.8}$$

$$\mathcal{L}_{colpitts}(\Delta\omega) = 10\log\left[\frac{k_B{\cdot}T}{4{\cdot}N{\cdot}I_B^2{\cdot}R_T^3{\cdot}C^2{\cdot}(1-\Phi^2/14)^2{\cdot}\Delta\omega^2}\times \left(\frac{\gamma}{n(1-n)}+\frac{1}{(1-n)^2}+\frac{n^2{\cdot}R_t{\cdot}g_{mT}}{(1-n)^2}\right)\right]. \tag{3.9}$$

Although in [5] it is concluded that the XCP oscillator is superior to the Colpitts oscillator, this conclusion is not yet drawn in this report, as the assumption of equal oscillator swing is not correct. The Colpitts oscillator can withstand a larger swing before the gate oxides break down, since the transistors are not connected to the ground node. Also, the quadrature coupling in the two oscillators is not necessarily the same and the buffer may react differently to the different waveforms. The XCP oscillator's thermal noise has been simulated (without the noisy tail current source, which is not beneficial in this process due to low output impedance) and agrees within 1dB of the formula for the optimum nominal channel length of 120nm (A_{tank} = 1V, C = 175fF, Q = 25 yielding -100dBc/Hz@100kHz), with the Colpitts topology showing slightly inferior performance at the same supply voltage. A notable detail is that the FoM of the XCP oscillator has an optimum for a supply voltage of around 0.8V.

The advantage of using a CMOS process with smaller minimum gate length is that the same g_m can be made at a lower (parasitic) input capacitance, resulting in a wider tuning range of the oscillator. Of course the parasitic r_{ds} is more dominant (lower) for short devices, but this is apparently only harmful for the XCP topology, while the Colpitts oscillator benefits from the small half conduction angle Φ (appearing in (3.9), but not in (3.8)) resulting from the high f_T of such devices.

3.2.2 Crossed-Capacitor Oscillator

An interesting alternative has emerged during the project, which is called the Crossed-Capacitor Oscillator (CCO) in this report. In this oscillator, the negative resistance is generated by a differential common-source buffer, whose input is capacitively cross-coupled with its output, as shown in Figure 3.7, along with its small-signal model. r_{out} accounts for the total output resistance, including the drain resistor r_d and the parasitic channel resistance r_{ds} of the transistor. Note that these resistances are decoupled from the tank and the equivalent parallel resistance behaves, in a way, as an impedance transformation from a series network consisting of two output resistances and both crossed capacitors. The decoupling of these parasitic resistances explains the excellent phase noise performance of the structure[2].

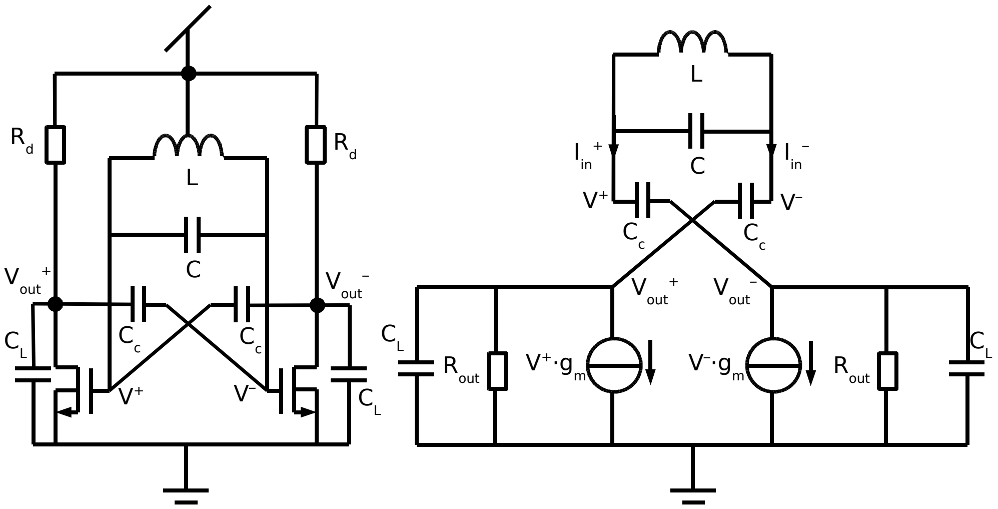


Figure 3.7: Schematic and small-signal model of the crossed-capacitor oscillator.

To simplify analysis, the output resistance is ignored at first. For this, we substitute $C'_L = C_L + \frac{1}{j\omega r_{out}}$. Next, the currents at the negative output node are related as follows, using $V^+ = \frac{V_{in}}{2}$ and $V^- = -\frac{V_{in}}{2}$.

$$\begin{aligned}
& g_m{\cdot}V^- = j\omega C'_L{\cdot}V^-_{out} + j\omega C_c(V^-_{out} - V^+) + j\omega C_g(V^-_{out} - V^-) \\
\Longleftrightarrow \quad & g_m{\cdot}\frac{V_{in}}{2} = j\omega\left(C'_L{\cdot}V^-_{out} + C_c(V^-_{out} - \frac{V_{in}}{2}) + C_g(V^-_{out} + \frac{V_{in}}{2})\right) \\
\Longleftrightarrow \quad & V^-_{out} = \frac{\frac{g_m}{j\omega} + C_c - C_g}{C'_L + C_c + C_g}{\cdot}\frac{V_{in}}{2} \\
\Longleftrightarrow \quad & \frac{V_{out}}{V_{in}} = \frac{-(\frac{g_m}{j\omega} + C_c - C_g)}{C_L + C_c + C_g + \frac{1}{j\omega r_{out}}}
\end{aligned} \tag{3.10}$$

The result is not yet very useful as such, but can be used to find the input impedance of

[2] This even gets better with process scaling; see Appendix C.

the structure, which is derived below.

$$\begin{aligned}
I_{in}^{-} &= j\omega C_g(V^{-} - V_{out}^{-}) + j\omega C_c(V^{-} - V_{out}^{+}) \\
\iff \quad I_{in}^{-} &= j\omega\left((C_c + C_g)V^{-} + (C_c - C_g)V_{out}^{-}\right) \\
\iff \quad \frac{V^{-}}{I_{in}^{-}} &= \frac{1}{j\omega\left(C_c + C_g + \frac{(C_g - C_c)(\frac{g_m}{j\omega} + C_c - C_g)}{C_L + C_c + C_g + \frac{1}{j\omega r_{out}}}\right)} \\
&= \frac{1}{j\omega(C_c + C_g)} \| \frac{C_L + C_c + C_g + \frac{1}{j\omega r_{out}}}{j\omega(C_g - C_c)(\frac{g_m}{j\omega} + C_c - C_g)} \\
\approx \frac{1}{j\omega(C_c + C_g)} &\| \frac{-(C_L + C_c + C_g)}{(C_c - C_g)\cdot g_m} \| \frac{-1}{j\omega(C_c - C_g)} \times \frac{C_L + C_c + C_g}{C_c - C_g}
\end{aligned} \tag{3.11}$$

The result implies that the cross-coupling capacitances need to be larger than the gate capacitances in order to achieve a negative input resistance (the second term). The gate capacitance is already comparatively large, because the large-signal (describing function) G_m is smaller, and therefore the negative resistance larger, than for other oscillator topologies at equal W/L. Added to the even larger crossed capacitance in the first term, this results in a large fixed capacitance. The negative input capacitance in the third term is usually negligible by comparison. The large fixed capacitance explains why this oscillator has a relatively small tuning range compared to other topologies. If the coupling capacitance is chosen dominant, the approximation of differential input impedance in (3.12) is valid.

$$Z_{in,differential} \approx \frac{-2}{g_m}. \tag{3.12}$$

This result can also be derived intuitively from the small-signal model in Figure 3.7, if the load capacitance and output resistance are ignored. No currents flow in the branches, other than those from the transconductances. Immediately it becomes clear that the negative input resistance for each branch is equal to $1/g_m$, which is doubled for differential operation. A closed-form expression for the $1/f^2$ phase noise, such as the ones in (3.8) and (3.9), was not derived.

3.3 Quadrature Oscillators

3.3.1 General Considerations Concerning Quadrature Coupling

Although many papers have been published on quadrature LC-oscillators, this class of oscillators has never been described with satisfactory clarity[3]. One of the very few design guidelines is given in [9], where it is suggested that if two tanks are properly coupled in

[3] In the author's opinion.

quadrature, the resulting phase noise is better than that of the single oscillator, because the effective tank Q is increased.

An alternative way of looking at it is given by Sander Gierkink [8]. If the quadrature coupling is basically a noiseless 90 degree phase shifter (such as a quarter-λ ideal transmission line[4]), the quadrature oscillator can in a sense be considered as two oscillators in parallel, or a single factor-2 width-scaled oscillator. The resulting oscillator produces 3dB less phase noise than the single oscillator and consumes twice the current, yielding the same FoM.

The author suggests a different, intuitive, way of looking at the quadrature coupling, since many coupling mechanisms involve a noisy coupling transistor and an exact 90 degree coupling phase shift is not always possible. The description will cover mismatch of natural tank frequencies in quadrature-coupled LC-oscillators, mismatch between the networks coupling the tanks and choice of mutual coupling strength.

To appreciate the time-varying noise contribution of the coupling transistor, it is useful to refer to the Impulse Sensitivity Function (ISF) theory due to Hajimiri and Lee [3]. Readers of this famous paper may recall that the ISF represents the instantaneous sensitivity of the oscillator phase to a unity disturbance impulse current injected into an oscillator node[5]. In the case of an LC-oscillator, this node is a tank node and the shape of the ISF is sinusoidal with a 90 degree phase shift from the tank voltage. In other words, the oscillator phase is most sensitive at zero crossings, and completely immune to disturbances at the peaks. The situation is sketched in Figure 3.8. Also visible is that a current pulse that is injected just before the voltage peak causes a phase *increase* and the same pulse causes a phase *decrease* if it is injected just after the peak.

This we can describe analytically, if we define a disturbance function Ψ. We may describe the resulting phase shift $\Delta\theta$ of an LC-tank as the integral over one period of the ISF multiplied with the disturbance function (direct convolution), provided that $\Delta\theta$ is much smaller than the oscillator period. The expression is chosen to be

$$\Delta\theta = \int_0^{2\pi} \Gamma_F(\theta)\cdot\Psi(\theta) d\theta, \tag{3.13}$$

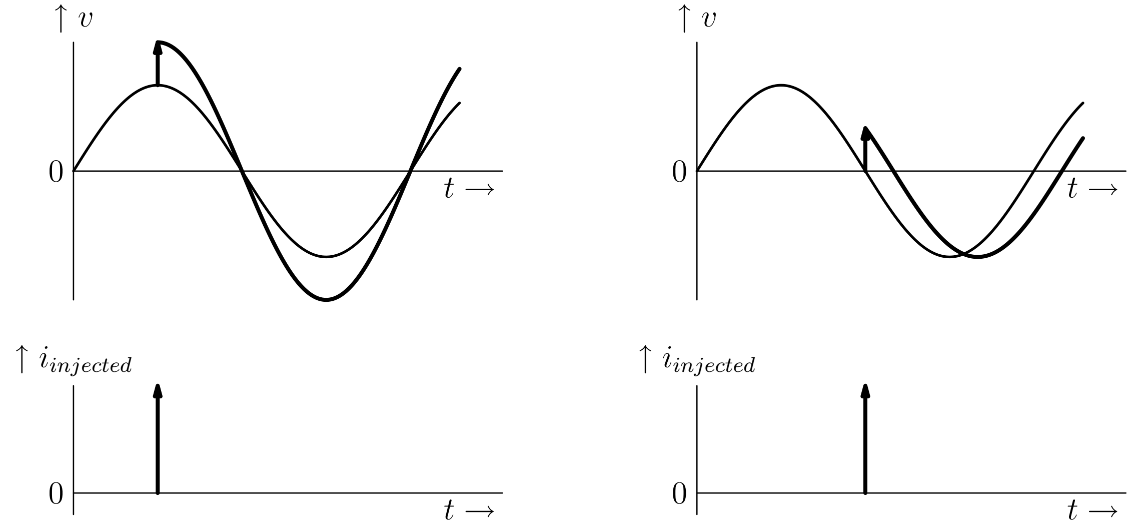
where Γ_F is a formally correct definition of the ISF[6], equal to $d\theta/dq$, also eliminating the term q_{max}, which would only increase the lengths of the equations.

Now, we will describe the single-ended coupling of one tank to another, as sketched in Figure 3.9. At the amplitude peak of the first (cosine) oscillator, an impulse should be triggered that is injected into the second (sine) oscillator with a 90 degree phase shift,

[4] Bram Nauta's way of looking at it.

[5] The usefulness of unity impulses to (intuitively) prove certain relationships seems widely underappreciated. The quadrature coupling is only one of many fine examples.

[6] The definition in [3] is actually formally incorrect, as an impulse response can only be defined for a linear system; see Appendix A.



(a) Impulse at peak.

(b) Impulse at zero-crossing.

Figure 3.8: Dependency of the phase change on the injection time of a current impulse.

such that it arrives precisely at the amplitude peak of the second oscillator. For now, it is assumed that both tanks are tuned to the exact same frequency (perfect match).

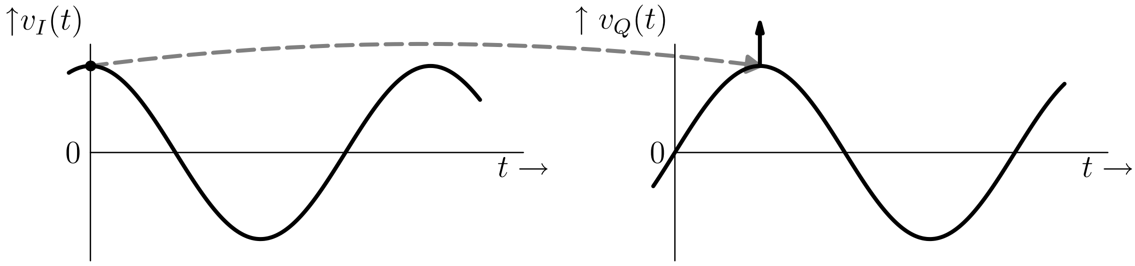


Figure 3.9: Sketch of an ideal quadrature coupling based on a single 90 degree phase shifted current impulse train derived from the input voltage peak.

For this, we define

$$\Psi(\theta) = k_\Psi \cdot \delta(\theta - \frac{\pi}{2}). \tag{3.14}$$

We know that if the second oscillator's waveform is a sine, its ISF must be a cosine[7]. Now we can solve the integral regardless of the exact magnitudes of the constants.

$$\begin{aligned} \Delta\theta &= \int_0^{2\pi} k_\Gamma \cdot \cos(\theta) \cdot k_\Psi \cdot \delta(\theta - \frac{\pi}{2}) d\theta \\ &= -\int_{\frac{-\pi}{2}}^{\frac{3\pi}{2}} k_\Gamma \cdot \sin(\theta) \cdot k_\Psi \cdot \delta(\theta) d\theta = 0. \end{aligned} \tag{3.15}$$

[7] This is derived from first principles in Appendix A.

So even for a noisy coupling transistor (a normally distributed k_Ψ), a 90 degree phase-shifted impulse coupling would introduce no additional phase noise. Let's see what happens if both oscillators have certain phase errors, $\Delta_1\theta$ and $\Delta_2\theta$, at the beginning of the integration period.

$$\begin{aligned}
\Delta_{2,new}\theta &= \Delta_2\theta + \int_0^{2\pi} k_\Gamma\cdot\cos(\theta+\Delta_2\theta)\cdot k_\Psi\cdot\delta(\theta+\Delta_1\theta-\frac{\pi}{2})d\theta \\
&= \Delta_2\theta - \int_{\frac{-\pi}{2}}^{\frac{3\pi}{2}} k_\Gamma\cdot\sin(\theta+\Delta_2\theta)\cdot k_\Psi\cdot\delta(\theta+\Delta_1\theta)d\theta \\
&= \Delta_2\theta - k_\Gamma\cdot k_\Psi\cdot\sin(\Delta_2\theta-\Delta_1\theta) \\
&\approx \Delta_2\theta(1-k_\Gamma\cdot k_\Psi) + k_\Gamma\cdot k_\Psi\cdot\Delta_1\theta. \qquad (3.16)
\end{aligned}$$

So still, as long as the coupling is a 90 degree phase-shifted impulse, no additional noise is added! For the phase jitter, this approximation leads to (3.17), where k_{inter} denotes the product of the two coupling factors k_Γ and k_Ψ. Especially for the Colpitts oscillator, as readers may recall from Section 3.2, the negative resistance of the basic oscillator may actually approximate an ideal periodic current impulse. In the ideal case, the quadrature coupling may be considered an externally injected "negative resistance current," whereas the internal transistors provide the internal current injection. For equal tank amplitude and equal power consumption, the sum of the internal impulse magnitude and the magnitude of the externally injected impulse must be constant. We may describe the internal impulse magnitude by k_{intra}, indicating its relation to the injected impulse by $k_{intra} = 1 - k_{inter}$. In practice, the sum of the two will be less than one, as the impulse magnitudes will be matched to the finite losses in the LC-tank.

$$\begin{aligned}
\sigma^2_{\theta,2,new} &= \mathrm{E}((\Delta_{2,new}\theta)^2) \\
&= k^2_{intra}\cdot\mathrm{E}((\Delta_2\theta)^2) + k^2_{inter}\cdot\mathrm{E}((\Delta_1\theta)^2) \\
&\quad +2\cdot k_{intra}\cdot k_{inter}\cdot\mathrm{E}(\Delta_1\theta\cdot\Delta_2\theta) \\
&= k^2_{intra}\cdot\sigma^2_{\theta,2} + k^2_{inter}\cdot\sigma^2_{\theta,1} \\
&\quad +2\cdot k_{intra}\cdot k_{inter}\cdot\mathrm{E}(\Delta_1\theta\cdot\Delta_2\theta). \qquad (3.17)
\end{aligned}$$

In the remainder of this analysis, $\Delta_1\theta$ and $\Delta_2\theta$ are assumed uncorrelated (quite a bold simplification), causing the last term in (3.17) to equal zero, and the tanks are considered equal, implying $\sigma^2_{\theta,1} = \sigma^2_{\theta,2}$. In that case, if k_{inter} is exactly half, the noise contributions of the two tanks are added quadratically and then divided by two. Thus, the noise in the two tanks is averaged, resulting in a 3dB phase noise reduction w.r.t. the single tank, a familiar result. The concept is illustrated in Figure 3.10.

This is the point where the ISF theory starts to be insufficient to describe the quadrature coupling, as the phase information is continuously exchanged between the two tanks. The situation is sketched in Figure 3.11. Therefore, as long as k_{inter} is neither zero nor unity,

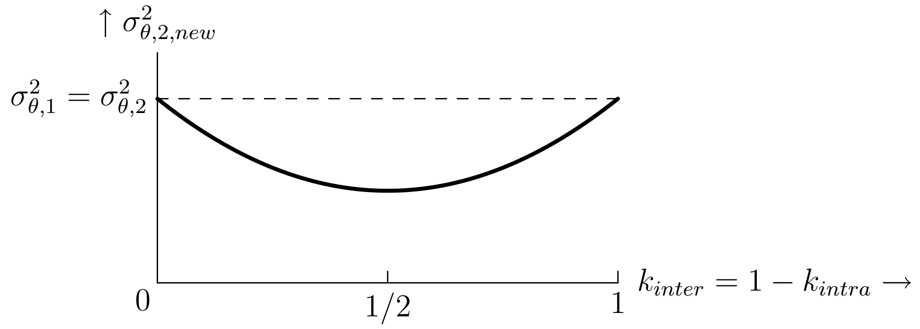


Figure 3.10: Sketch showing noise averaging as function of coupling strength.

the phase information will always be distributed among the two tanks as time goes to infinity. In case k_{inter} is zero (no coupling), the tanks can be analyzed individually, and in case k_{inter} is unity (infinitely large coupling impulses resulting from voltage peaks), the phase of one tank is always fully transferred to the other, such that no averaging of phase information occurs.

In [24] infinitely strong mutual coupling between the tanks (equivalent to $k_{inter} = 1$, if we consider $k_{inter}/k_{intra} = I_{inter}/I_{intra} = m$, where m is the common definition of mutual coupling defined as the ratio between coupling current and current due to the internal active negative resistance) results as the optimum case, a result which is in disagreement with the preceding analysis. The disagreement may be due to either the above assumption that the noise in the two tanks is uncorrelated at synchronization or the exclusion of the fact that tank losses limit the sum of k_{inter} and k_{intra}. In practice, strong coupling causes phase noise of the coupling transistors to dominate, making it difficult to reject either hypothesis based on the results from a practical circuit. In any case, both points of view yield a coupling angle of 90 degrees as the optimum, as does [9].

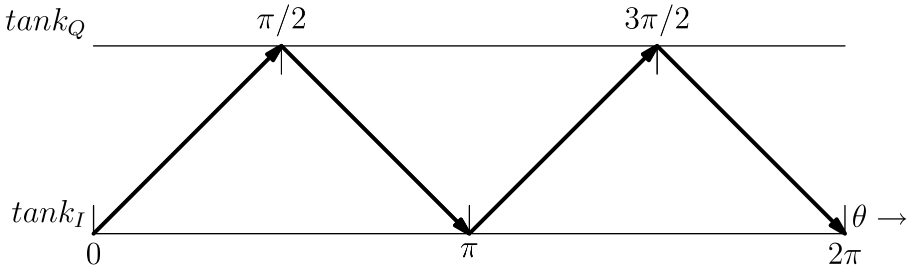


Figure 3.11: Abstract sketch of an ideal mutual quadrature coupling based on 90 degree phase shifted current impulse trains derived from the differential voltage peaks. The arrows indicate the transfer of phase information between the two tanks.

If we assume the model presented above is correct, the effect of coupling transistor noise is that the k_{inter}, once designed, deviates a little bit from 1/2. This means that the addition is not perfectly quadratic. The effect is symmetrical around 1/2, so the coupling should still not be designed any differently due to such imperfections. In short, noisy or very variable (i.e. process spread) coupling transistors set an upper limit on the quality of the noise averaging by causing random asymmetries in the quadratic noise addition due to variations away from the optimum coupling strength. Previously, the only important limiting factor was often thought to be the accuracy of the coupling angle.

In case the coupling angle is not perfectly 90 degrees, but deviates slightly from this value, it is as if the starting deviation $\Delta\theta$ has increased. This will change the quadrature angle, unless the reverse coupling has the same imperfection[8]. In that case, the total oscillator frequency will differ from the "natural" tank frequencies. Constant terms will appear in the resulting integrals, allowing coupling transistors to add phase noise. The quadrature angle might also change as a result of mismatches between the two coupling networks, which, by analogy, would also lead to more phase noise due to coupling transistors.

Similarly, one can find out what happens when the coupling is done by two impulses that are spaced symmetrically around 90 degrees at small distances D_1 and $-D_2$.

$$\begin{aligned}
\Delta_{2,new}\theta &= \Delta_2\theta + \int_0^{2\pi} k_\Gamma\cdot\cos(\theta+\Delta_2\theta)\cdot k_\Psi\cdot\Big(\delta(\theta - D_1 + \Delta_1\theta - \frac{\pi}{2}) + \\
&\quad \delta(\theta + D_2 + \Delta_1\theta - \frac{\pi}{2})\Big)d\theta \\
&= \Delta_2\theta - \int_{\frac{-\pi}{2}}^{\frac{3\pi}{2}} k_\Gamma\cdot\sin(\theta+\Delta_2\theta)\cdot k_\Psi\cdot\Big(\delta(\theta - D_1 + \Delta_1\theta) + \\
&\quad \delta(\theta + D_2 + \Delta_1\theta)\Big)d\theta \\
&= \Delta_2\theta - k_\Gamma\cdot k_\Psi\cdot\Big(\sin(D_1 + \Delta_2\theta - \Delta_1\theta) + \sin(-D_2 + \Delta_2\theta - \Delta_1\theta)\Big) \\
&\approx \Delta_2\theta(1 - 2\cdot k_\Gamma\cdot k_\Psi) + 2\cdot k_\Gamma\cdot k_\Psi\cdot\Delta_1\theta + k_\Gamma\cdot k_\Psi\cdot(D_1 - D_2). \qquad (3.18)
\end{aligned}$$

As can be seen here, as long as D_1 and D_2 are small and equal to each other, again no additional phase noise is introduced. Because there are two impulses, the optimum coupling strength has become a factor of two smaller. What this result means, is that for any shape of coupling current, as long as it is closely spaced to and symmetrical around 90 degrees, no phase noise is addded and as long as the integral of the injected current shape has the right value, the noise averaging is still nearly perfect. Of course the magnitudes of the two impulses would often differ in practice due to noisy transistors, which means that it is even more preferable to have small values of D_1 and D_2, meaning a sharper approximation of the impulse function.

In a practical oscillator, coupling is usually only done through the first harmonic[9]. For coupling currents with higher-order harmonics, a realistic transfer function with nonideal

[8] From this point of view, it is also easy to see how the quadrature angle can change as a result of poorly matched tank frequencies. Reducing mismatch by careful layout is therefore important.

[9] Superharmonic coupling [8] is currently the most important exception to this rule.

phase response will result in coupling current asymmetry around 90 degrees. It is now clear why any deviation from a 90 degrees shifted first harmonic will affect the phase noise: there will be asymmetry around 90 degrees and the coupling peak will be away from 90 degrees, allowing noise from the coupling transistor to be directly translated into phase noise.

The principle of a 90-degree phase-shifted, first harmonic quadrature coupling (although at the time described only very briefly) is exploited to good effect in [19] and seems to have been picked up again only recently in the seemingly first attempt to properly model quadrature LC-oscillators [24]. An analysis similar to the one in this section was given in [20], ignoring, however, the possibility of phase-shifting the coupling currents.

As a last remark, w.r.t. the single oscillator, phase noise improvement from quadrature coupling at 11.7GHz is in practice only realizable for two well-matched LC-tanks. The practical limit is formed by finite matching of the natural tank frequencies, for which the coupling must be able to compensate, therefore causing noise of the coupling transistors to dominate. The difference in phase noise for perfectly matched and imperfectly matched tanks in an XCP design is very large (-102 vs. -85 dBc/Hz@100kHz, respectively; for reference, a single XCP oscillator produces -100 dBc/Hz@100kHz). To achieve phase noise improvement from the quadrature coupling w.r.t. a single oscillator, the coupling current must be dimensioned very small (W/L of the coupling transistor of 0.12/1). Therefore, it may be worthwhile to look into frequency matching calibration. As individual tank calibration tremendously complicates the system and the oscillator layout, it was not investigated in this project.

Summarizing, two existing points of view [9], [24] and a newly introduced point of view suggest that the optimum coupling angle of the coupling current with respect to the voltage of the driving LC-tank is 90 degrees. An intuitive view on the noise contribution of coupling transistors was also given in this section, but without quantitative analysis. Mismatch of the natural tank frequencies, mismatch between the coupling networks and wrong choice of mutual coupling strength between the two tanks are intuitively identified as possible reasons why phase noise from the coupling network may degrade overall phase noise performance of a quadrature LC-oscillator.

3.3.2 Practical Implementations of Quadrature Coupling

There are so many variations of possible quadrature coupling methods, that only the main competitors will be discussed. For example, superharmonic coupling of XCP oscillators [8] gives a swing at the sources of the transistors, leading to a lower maximum supply voltage, leading to inferior phase noise and quadrature accuracy. This method will therefore not be discussed further.

Each of the three main oscillator topologies has a certain advantage when used in quadrature. The best coupling methods for each topology are shown in Figure 3.12 (XCP), Figure 3.13 (Colpitts), and Figure 3.14 (CCO). The phase shifter for the XCP (parallel-*RC* source degeneration of the coupling transistor) and the overvoltage protection resistor for the Colpitts (resistive source degeneration of the coupling transistor) are not shown.

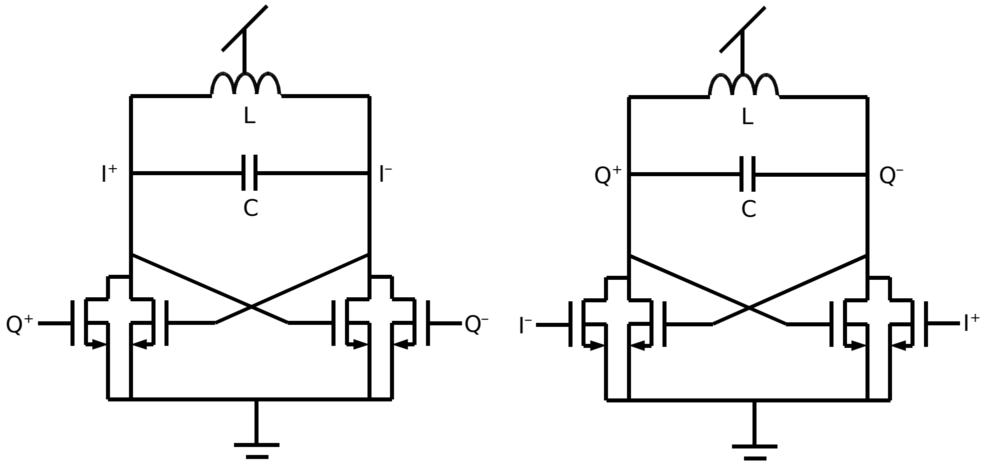


Figure 3.12: Schematic of a quadrature-coupled XCP.

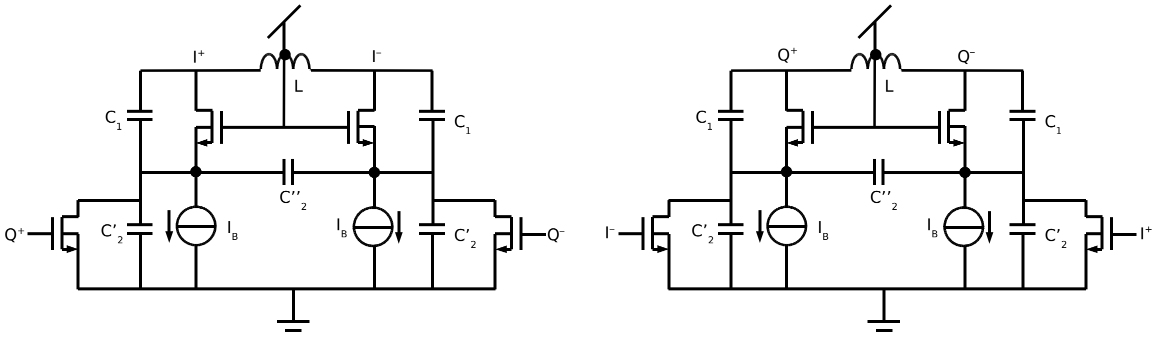


Figure 3.13: Schematic of a quadrature-coupled Colpitts oscillator.

For the XCP topology, the optimum coupling method is identical to the one in [19]. Basically, the *RC*-network shifts the phase of the coupling current closer (but nowhere near completely) to 90 degrees, resulting in better coupling at the cost of some voltage headroom for the coupling transistor. An easy way of looking at the circuit is to look at the basic oscillator first, and considering the impedance between the only two circuit nodes to be infinite (parallel *LC* at resonance, negative and positive resistance cancelling each other). This significantly simplifies small-signal analysis, as now the phase shift of the coupling current with respect to the input voltage is determined only by the circuit elements in the branch itself. The newly suggested phase-shifting method given in [24] is not very useful with the high chosen inductor *Q* and the high oscillator frequency, as the parasitic resistance from the phase shifter tends to dominate.

For the other two topologies, the coupling is done off-tank. Thus, the tank *Q* is not as

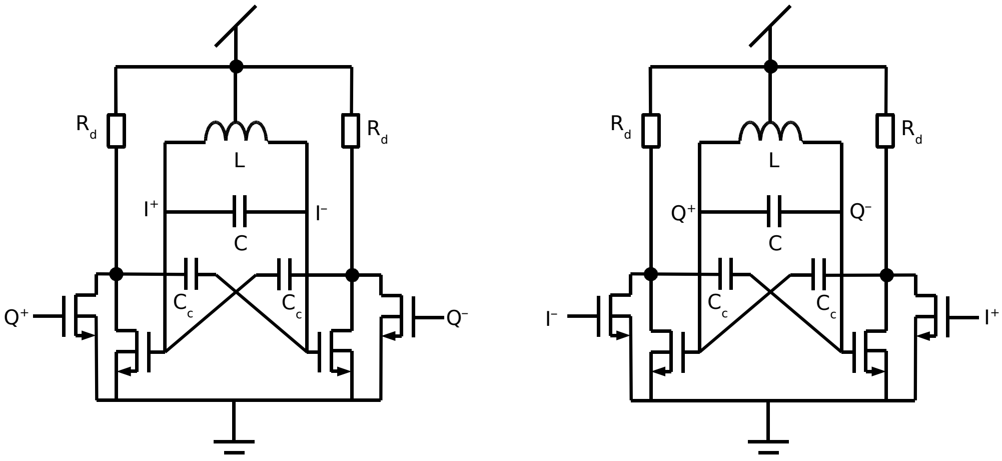


Figure 3.14: Schematic of a quadrature-coupled CCO.

severely decreased due to parasitic R_{ds}. The phase shift and matching properties of each topology are unique, so the analysis of each of the two circuits will be treated separately.

The quadrature Colpitts DCO is similar to a design by Xiaoyong Li [22, p. 97]. Although the designer does not explain the benefit of his coupling mechanism[10], it is possible to explain this in terms of the impedance as seen from the drain of the coupling transistor.

In the ideal model, ignoring the transconductances of the central transistors (assuming again that positive and negative resistance cancel exactly), the impedance as seen from the coupling transistor is infinite, just as is the case for the XCP topology. This can be seen with the help of the simplified circuit diagram in Figure 3.15. It is shown below that not only at point A, but also at point B the impedance is infinite at the resonance frequency.

In the oscillator, the resonance frequency is determined from the half-circuit, so it is easier to write L instead of $L/2$. The ideal total capacitance is then

$$C = \frac{C_1' \cdot C_2'}{C_1' + C_2'} = n \cdot C_2', \qquad \text{with} \qquad n \equiv \frac{C_1'}{C_1' + C_2'}. \tag{3.19}$$

This factor n is the same as the one in [5]. Then we have as drain impedance as seen from the coupling transistor at point B:

$$Z_d = r_{out} \| \frac{1}{j\omega C_2'} \| \left(j\omega L + \frac{1}{j\omega C_2'} \right). \tag{3.20}$$

[10] To make matters worse, his definition of the ISF is flat-out wrong (something remarkable for a Ph.D. thesis). Also, no mention is made of the quadrature accuracy of this solution (!), which fortunately turns out to be pretty good.

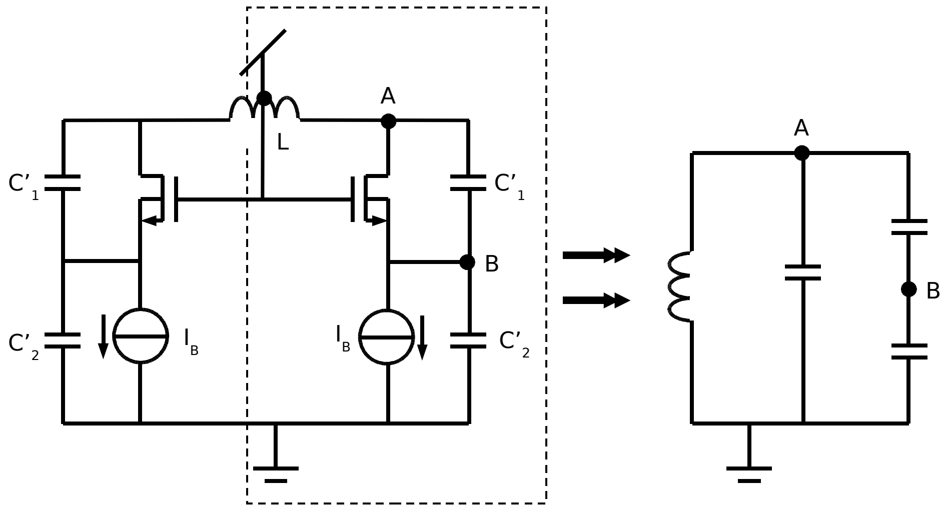


Figure 3.15: Resonator without active part showing two possible coupling nodes.

Setting $\omega = \omega_0$, this results in the following:

$$\begin{aligned} Z_d &= r_{out} \| \frac{n}{j\omega_0 C} \| j \cdot \left(\frac{\omega_0^2 LC + n - 1}{\omega_0 C} \right) \\ &= r_{out} \| \frac{n}{j\omega_0 C} \| \frac{-n}{j\omega_0 C} = r_{out}. \end{aligned} \tag{3.21}$$

Thus the ideal circuit also resonates from the perspective of the coupling transistor. However, the central transistors can be considered as cascodes to the coupling transistor, causing a phase shift of the current, which turns out to be in the order of 90 degrees. In addition, the central transistors' gate-drain capacitances are to ground instead of directly parallel to the inductor, so the spread in tank capacitances due to transistor gates is not as severe.

For the CCO topology, the coupling capacitances are in the same order of magnitude as the gate capacitances of the central oscillator transistors, reducing the spread in tank capacitance due to gate capacitance by approximately a factor of four. In addition, the coupling strength can be made large without greatly reducing resonator Q. Although not yet fully understood, the result is a very accurate quadrature angle.

In short, the Colpitts and CCO topology do not have the gate-drain capacitances of the transistors directly in parallel with the LC-tank, causing less tank mismatch. In addition, it was shown that the Colpitts oscillator does not require additional components to achieve the desired quadrature coupling phase shift. All topologies are able to meet the phase noise requirement of -85 dBc/Hz@100kHz.

Chapter 4

Buffer Design

The oscillators by themselves are relatively sensitive to parasitics. Varying load capacitances will cause changes in frequency, possibly upsetting the PLL, and low-Q loads will increase the phase noise, or, even worse, prevent the oscillator from starting up altogether. All such effects must be eliminated and therefore a buffer needs to be an integral part of the oscillator, even more so, because if no inductors are used in the buffer, its power consumption may be quite large compared to the oscillator core itself. The most common buffer approach is to connect the gate of a MOSFET to the oscillator tank, which provides a DC decoupling between the tank and the output. In this approach, the MOSFET can be connected as either a common-source amplifier with gain or a source follower with no Miller capacitance multiplication from input to output. Both configurations will be described with small-signal models in Section 4.1. Design and simulations of practical buffers will be presented in Section 4.2.

4.1 Small-Signal Buffer Models

Although in 65nm CMOS the transistors deviate strongly from ideal square-law and current-source models, classical small-signal analysis still provides valuable insights into the fundamental operation of analog circuits. At high frequencies, impedance transformations help to simplify circuit analysis even further. The analysis of both the source follower and the common-source amplifier, given below, are therefore conveniently simple.

4.1.1 Common-Source Amplifier

The circuit diagram and small-signal model for the capacitively loaded common-source amplifier are given in Figure 4.1.

In the small-signal model, the output is related to the input as follows.

$$V_{out} = -g_m \cdot V_{in} \cdot (r_{out} \| \frac{1}{j\omega C_L}). \tag{4.1}$$

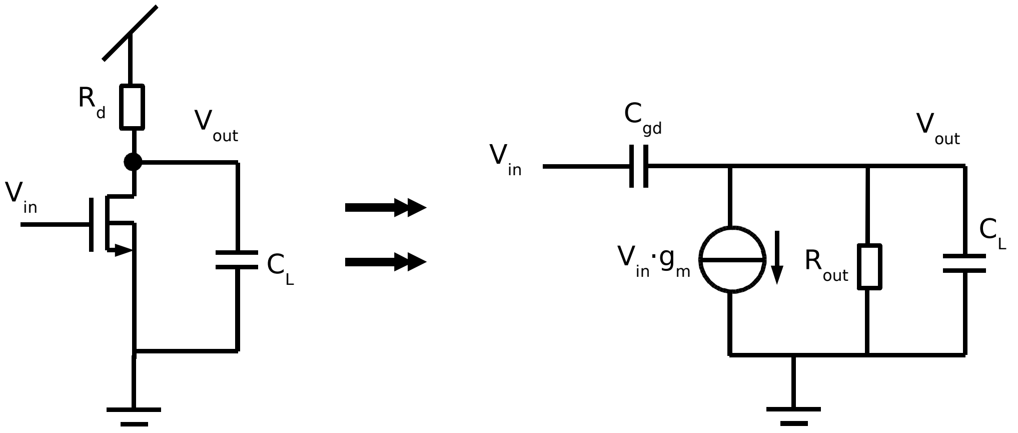


Figure 4.1: Schematic (left) and small-signal model (right) of a common-source buffer.

When worked out, this results in the following transfer function.

$$\frac{V_{out}}{V_{in}} = -g_m \cdot \frac{r_{out}}{1 + j\omega r_{out} C_L} = -g_m \cdot \frac{r_{out} - r_{out}^2 j\omega C_L}{1 + r_{out}^2 \omega^2 C_L^2}. \tag{4.2}$$

For an oscillator buffer, the phase shift is not very interesting. What is interesting, however, is that the gain decreases with increasing load capacitance. This means also that the Miller multiplication factor decreases and thus the effective input capacitance decreases with increasing load capacitance. This is indeed what happens in simulations; as the 30fF load increases by a few percent, the oscillator frequency increases by several hundreds of kHz.

Another interesting case is when $|j\omega C_L r_{out}| \gg 1$, easily achieved with large load capacitances at 10GHz. In that case, the current through the gate capacitance can be written as follows (gate capacitances to ground nodes are ignored for simplicity).

$$I_{in} = j\omega C_{gd} \cdot (V_{in} - V_{out}) = j\omega C_{gd} \cdot (V_{in}(1 + \frac{g_m}{j\omega C_L})) = V_{in} \cdot (j\omega C_{gd} + \frac{g_m \cdot C_{gd}}{C_L}). \tag{4.3}$$

For high frequencies, the transconductance and load capacitance therefore form a resistance in parallel with the input capacitance[1], whose magnitude is given by

$$\frac{V_{in}}{I_{in}} = \frac{1}{j\omega C_{gd} + \frac{g_m \cdot C_{gd}}{C_L}} = \frac{1}{j\omega C_{gd}} \| \frac{C_L}{g_m \cdot C_{gd}}, \tag{4.4}$$

[1] By cross-coupling capacitors from input to output, a negative effective gate capacitance can even be created and used to form a negative parallel input resistance that can sustain the entire oscillator. This technique was already described in Section 3.2, but was actually inspired by considering the properties of a CS buffer amplifier.

or, equivalently (in series form)

$$= \frac{\frac{g_m\cdot C_{gd}}{C_L} - j\omega C_{gd}}{\frac{g_m^2\cdot C_{gd}^2}{C_L^2} + \omega^2 C_{gd}^2} = \frac{1}{\frac{g_m\cdot C_{gd}}{C_L} + \frac{\omega^2 C_{gd} C_L}{g_m}} - \frac{j\omega}{\frac{g_m^2\cdot C_{gd}}{C_L^2} + \omega^2 C_{gd}}. \tag{4.5}$$

This directly reduces the Q of the tank and therefore the effect should be minimized. Intuitively, decreasing the load capacitance and decreasing the gate capacitance seem like logical solutions. Up to a certain point, decreasing transconductance also increases the parallel resistance. Another option is to use a coupling capacitor, which transforms the resistance to $R_{transformed} = R\cdot(1 + C_{gd,eff}/C_{coupling})^2$, but this also decreases the gain. In practice, the Miller capacitance is dominant, and –since it depends directly on the load capacitance– the oscillation frequency will depend on the load capacitance, making the buffer provide poor shielding performance.

There is a different way of implementing this amplifier, as shown in Figure 4.2. It is a three-stage inverter, with the NMOS and PMOS parts biased separately. They are biased at approximately 800mV and 400mV, respectively, so as to obtain a larger g_m without breaking the gate oxides. This solution has the advantage of smaller input capacitance (and thus resistance). This amplifier has been designed previous to the current project and its layout is known to be problem-free. An important benefit of this type of buffer is its low power consumption compared to other topologies.

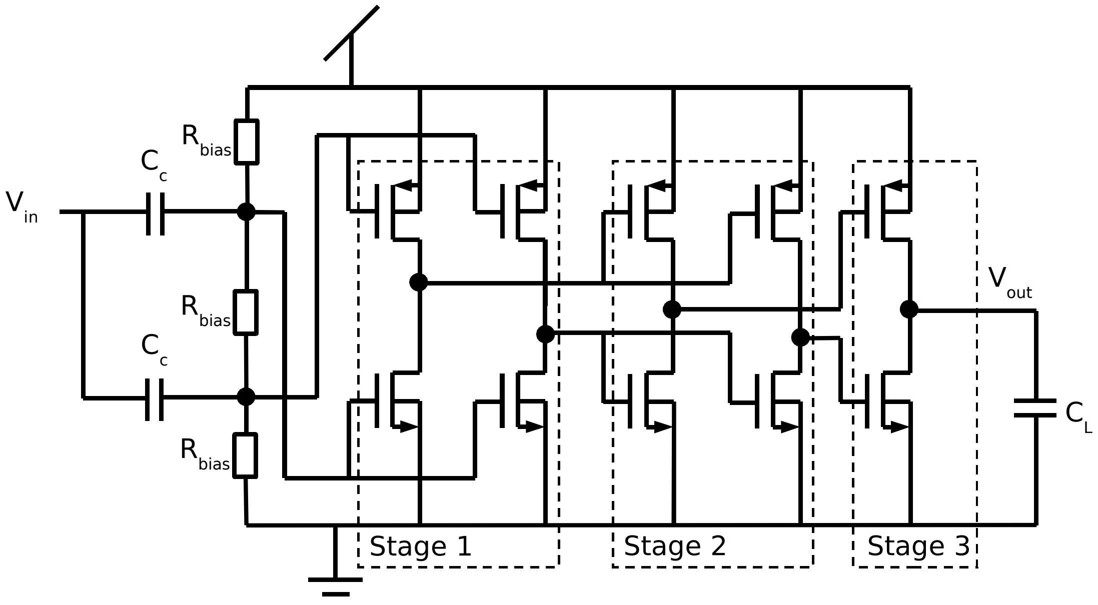


Figure 4.2: Schematic of a biased 3-stage common-source/inverter buffer.

4.1.2 Source Follower

As the oscillator swing is fairly large, even larger than the supply voltage, no gain larger than one is required, so a source follower is also a good candidate for the buffer. As the gain is also non-inverting, no Miller multiplication takes place and no “strange” input resistance is formed, other than the capacitively transformed output resistance. The circuit diagram and small-signal model for the capacitively loaded source follower are given in Figure 4.3.

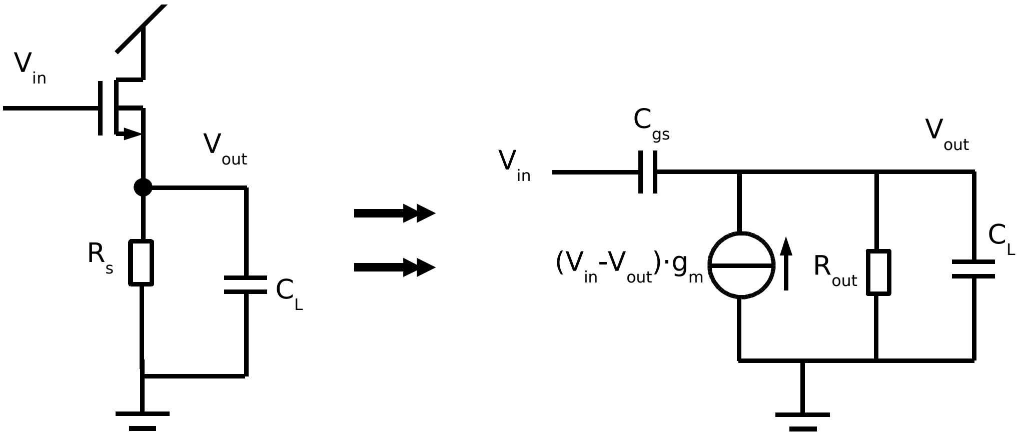


Figure 4.3: Schematic (left) and small-signal model (right) of a source follower buffer.

In the small-signal model, the output is related to the input as follows.

$$\begin{aligned} V_{out} &= -g_m \cdot (r_{out} \| \frac{1}{j\omega C_L}) \cdot (V_{in} - V_{out}) \\ \Longleftrightarrow \quad \frac{V_{out}}{V_{in}} &= \frac{g_m \cdot (r_{out} \| \frac{1}{j\omega C_L})}{1 + g_m \cdot (r_{out} \| \frac{1}{j\omega C_L})}. \end{aligned} \tag{4.6}$$

It is clear that when g_m is large enough, the gain approaches unity. In that case, also the gate-source capacitance becomes negligible, as no current flows through a capacitor between equipotential nodes. This in turn is very good for the tank Q, as the source follower's output resistance is not “felt” very strongly by the oscillator tank.

In reality, at the operating frequency of around 10GHz, g_m is not automatically large enough to avoid influence from the load on the frequency tuning. Therefore the source follower's input impedance is derived below (as for the CS stage, capacitances from the gate to ground nodes are ignored for simplicity).

$$I_{in} = j\omega C_{gs}(V_{in} - V_{out}) = j\omega C_{gs}\left(1 - \frac{g_m{\cdot}r_{out}}{1 + j\omega C_L{\cdot}r_{out} + g_m{\cdot}r_{out}}\right){\cdot}V_{in}.$$

$$\therefore \qquad Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1 + j\omega C_L{\cdot}r_{out} + g_m{\cdot}r_{out}}{j\omega C_{gs}(1 + j\omega C_L{\cdot}r_{out})}. \tag{4.7}$$

Clearly, for minimum input capacitance and minimum loading effects, r_{out} should be very small and g_m should be as large as possible.

4.2 Practical Buffers

For the oscillator running at 11.7GHz, it is possible to calculate what effect a change in buffer input capacitance will have on the oscillation frequency. As the oscillation frequency depends on the inverse square-root of the effective tank capacitance, a change in frequency corresponding to one LSB of the varactor bank, so 1MHz, would be equivalent to a change in (single-ended) tank capacitance of 7.4aF, given a tank inductance of 1nH (500pH single-ended).

If a change in load capacitance of ±20% on 30fF is to have an effect on the frequency of less than one varactor bank LSB, its impedance must be shielded by a factor of around 1000. The question is how many source follower stages are required to achieve such a shielding, with reasonable values of $g_m{\approx}0.01$S, $r_{out}{\approx}100\Omega$ and $C_{gs}{\approx}30$fF.

For this purpose, the source follower buffer's input impedance may be rewritten as a series (negative) resistance and an input capacitance. The final expressions (resulting from tedious derivation) are given below.

$$R_{in} = \frac{-g_m{\cdot}C_L{\cdot}r_{out}^2}{\omega^2 C_{gs}C_L^2 r_{out}^2 + C_{gs}}. \tag{4.8}$$

$$C_{in} = \frac{C_{gs}(1 + \omega^2 C_L^2 r_{out}^2)}{1 + g_m{\cdot}r_{out} + \omega^2 C_L^2 r_{out}^2}. \tag{4.9}$$

To drive the load, $g_m{\cdot}r_{out}$ must be approximately equal to 1. As a quick check, according to (4.9), if $g_m{\cdot}r_{out}$ would be either zero or infinity, the load capacitance would have no influence on the input capacitance (an intuitively correct result). Filling in the reasonable values for all variables yields $C_{in} = 15.22986$fF for $C_L = 24$fF and $C_{in} = 15.55075$fF for $C_L = 36$fF. As this is a difference of 320aF, the single-stage buffer provides only slightly more than the square-root of the required shielding factor. A second buffer stage could solve the problem.

However, a source follower provides no gain and the loss in amplitude, in combination with the high power consumption (typically more than 40mW for the first stage alone), makes the source follower quite unattractive. The biased three-stage inverter does not suffer from severe input resistance, provides enough shielding and typically consumes only 24mW of power in a differential quadrature configuration. Therefore, this (already available) type of buffer was selected.

In conclusion, a biased 3-stage inverter buffer offers the required shielding between the oscillator and a variable load capacitance at the lowest power consumption. Therefore, the final buffers are implemented in this way.

Chapter 5

Inductor Design

Making physically large (and heavy!) inductors for e.g. audio applications has become quite simple, as the size of the wire can generally be neglected with respect to the coil area, parasitic capacitances are minimal, and many turns are generally wound, reducing edge effects.

Making planar inductors for operating frequencies of several GHz is unfortunately not so straightforward. Parasitic capacitances can easily decrease a coil's internal resonance frequency to unacceptable values and inductance values cannot be straightforwardly calculated from the area that is enclosed by the coil, for still rather poorly understood reasons.

To help the circuit designer in choosing the appropriate inductor design, lumped models exist and, as of late, they can accurately describe how a certain planar inductor design behaves [4]. A variation of the published LSIM inductor model was used to do circuit simulations.

A constraint was placed on the area; the lateral dimensions should be in the order of 100μm. The LSIM simulation tool indicated that for an octagonal 400pH inductor, the Q and resonance frequency would be optimal in the two-turn design with a track width of 8μm and a spacing between the tracks of 10μm. In that case, $Q = 26$ at 10GHz and the resonance frequency is around 40GHz. The resonance is chosen far from the operating frequency, because the effective inductance peaks just below the resonance frequency. This can result in an uncontrollable influence on the tuning curve and other undesired effects, so it is preferable to have a more modest slope of the inductance around the operating frequency. For the chosen inductor, the plots of inductance and Q versus frequency are shown in Figure 5.1.

A smaller inductor is more sensitive to parasitics, especially interconnect resistance, but also stray inductances. A 1μm long straight interconnect wire, for example, has a parasitic inductance of approximately 1pH, as given in [2, p. 140] by

$$L \approx \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{r}\right) - 0.75\right] = (2\times10^{-7})l\left[\ln\left(\frac{2l}{r}\right) - 0.75\right], \tag{5.1}$$

where l is the wire length and r is the radius, as the wire is assumed cylindrical. In practice the expression is also useful for approximating non-cylindrical wires, as the length is the most important factor; the exact cross-sectional shape is actually not so important. In another project it has been observed that neglecting such effects can lead to a negative shift of around 1GHz in the oscillating frequency of an LC-tank [6]. A more accurate

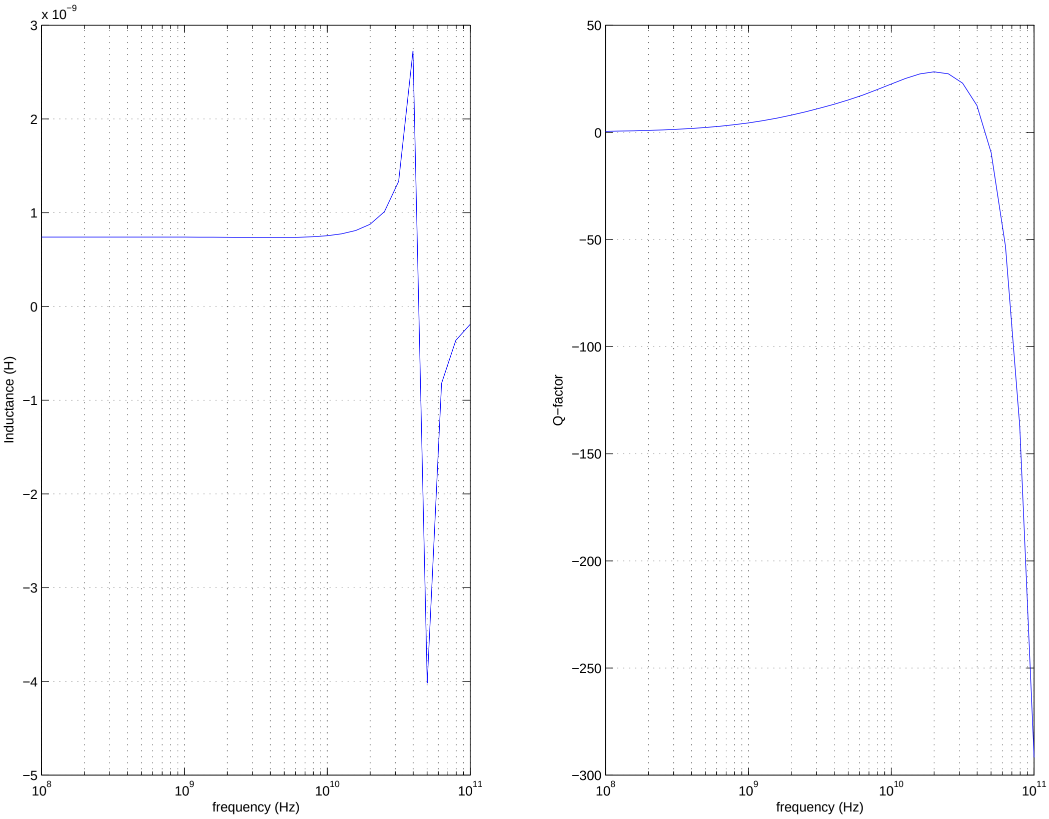


Figure 5.1: Inductance and Q versus frequency for an inductor with 100μm inner diameter.

formula (see Appendix D) reveals that the above formula is a little bit on the pessimistic side.

Even more detrimental is enclosing an area A with a wire loop, as approximated in [2, pp. 146–147] by

$$L_{loop} \approx \mu_0 \sqrt{\pi A}. \tag{5.2}$$

Apart from the self-inductance, enclosing areas with wire loops, even partially with large bends, can lead to mutual coupling to other parts of the circuit. This can be minimized by so-called "Manhattan" layout structures, where horizontal and vertical lines are drawn in different metal layers and lines with opposite phase are run along each other over their entire length, i.e. further than some of the vias. As parasitic inductances cannot be extracted from the layout, one must be very careful not to make any current loops.

Finally, the IRR can depend to some extent on the mutual magnetic coupling between the inductances of the two tanks [21], but this effect is, like the physical mechanisms determining inductance values of planar coils, poorly understood and will not be treated in this report. In [21] it is observed that the proposed theory and the measurements did not agree very well with each other.

Chapter 6

Frequency Tuning

Many process parameters have a certain tolerance, leading to differences between identically designed circuits. The most important of these differences is the resulting variation in oscillation frequency. In this project, the idea is to compensate for production differences, which are expected to cause a frequency spread of ±5%, by means of a startup calibration and to do small PLL adjustments using a finer frequency-tuning block.

The frequency adjustment is realized using digitally controlled variable capacitances (varactors) in large arrays, so-called *varactor banks.* The startup calibration is done using a coarse varactor bank and the continuous fine-tuning is done using a fine varactor bank.

In Figure 6.1 the gate capacitance versus drive voltage is plotted for an NMOST. The capacitance is quite constant around 0V and for voltages larger than 1.2V. This can be exploited by switching the drive voltage digitally between the two regions and ensuring that the AC swing is very small. In this way the capacitance is more linear and less prone to variation (for example, for non-constant supply voltage).

In principle, each varactor corresponds to a binary control bit, so subsequent varactors differ in switchable capacitance by a factor two. For the fine varactor bank, purely binary switching could cause nonmonotonicity in the frequency tuning range, so a thermometer code is used for the most significant bits, limiting the maximum switched capacitance per element to 8 LSB. In addition, the varactor capacitance does not scale linearly with area due to edge effects. This is clearly visible when comparing Figure 6.1 and Figure 6.2. For decreasing varactor size, the amount of fixed capacitance also increases with respect to the amount of variable capacitance.

For the Colpitts oscillator, the most natural way to implement the varactor is given in Figure 6.3. The capacitances C_1' and C_2' can also be split up into four capacitances, with C_3 being a variable capacitance, as shown in Figure 6.4. Note that in the actual oscillator, C_4 would actually be a differential capacitor of half the specified capacitance (thus effectively the same). The latter solution will be studied first.

The input capacitance as seen from the tank is in that case

$$C_{in} = C_1 \| (C_3 + (C_2 \| C_4)) = \frac{C_1C_2C_4 + C_1C_2C_3 + C_1C_3C_4}{C_1C_2 + C_1C_4 + C_2C_3 + C_2C_4 + C_3C_4}. \tag{6.1}$$

The capacitive division ratio n at the node between C_2 and C_4 determines the phase noise [5]. For a variable C_3, it cannot be kept constant, as follows from the expression given

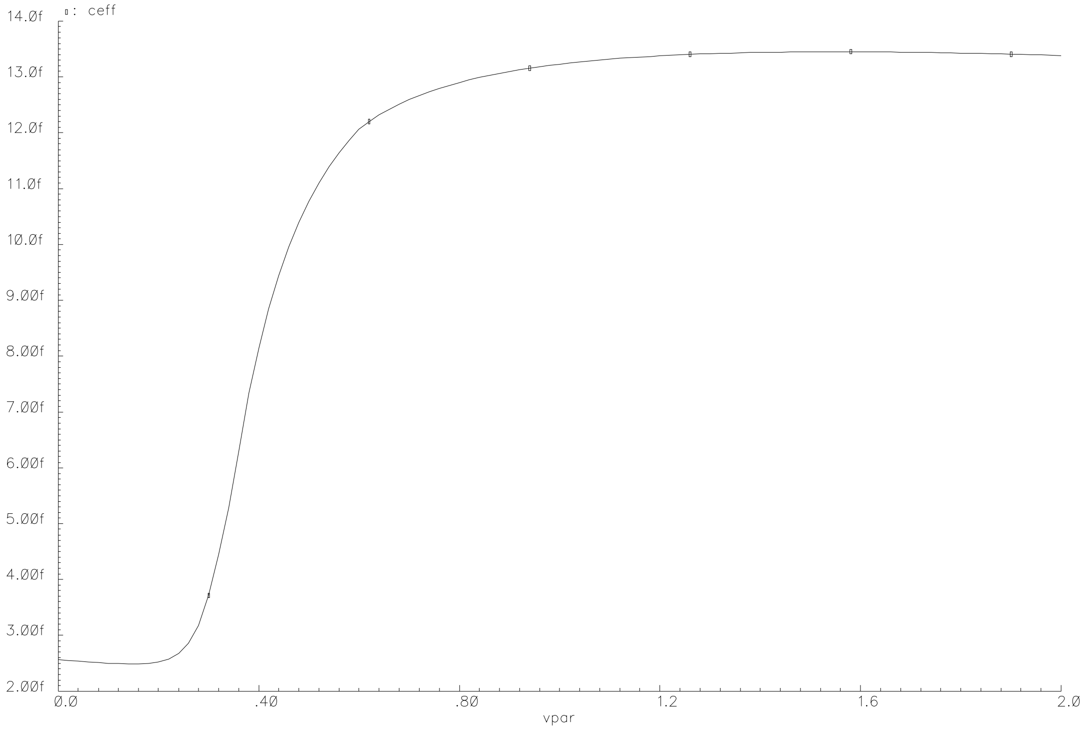


Figure 6.1: C–V curve of a $1\mu\mathrm{m}^2$ varactor.

below.

$$n = \frac{C_1'}{C_1' + C_2'} = \frac{C_1C_2}{C_1C_2 + C_1C_4 + C_2C_3 + C_2C_4 + C_3C_4}. \tag{6.2}$$

C_3 only appears in the denominator, and its influence can only be minimized by choosing C_1 very large, which means that C_4 must be large enough to obtain a division ratio of 0.3. This in turn puts a lower limit on the variability of the term in C_3C_4.

To avoid the variation in n, it is possible also to vary C_4, but this adds additional parasitics to the circuit, which would probably introduce more phase noise and IRR degradation than would result from variations in n. In addition, it has appeared in simulations that 0.3 is not always the optimum n for quadrature configurations; in fact, the optimum for n has not been properly characterized.

The differential capacitor C_4 can be to ground as well, but this will affect the symmetry of the differential oscillator waveform. For this reason, it is also not preferable to do tuning with this capacitance (as shown in Figure 6.3), as tuning capacitance is always to ground. However, as this method does not “downtransform” the negative series resistance of the oscillator to unacceptable values, it is in practice the only solution.

It is also possible to connect the tuning capacitance to the tank by means of an extra set of coupling capacitors. This makes the tuning capacitance more vulnerable to voltage

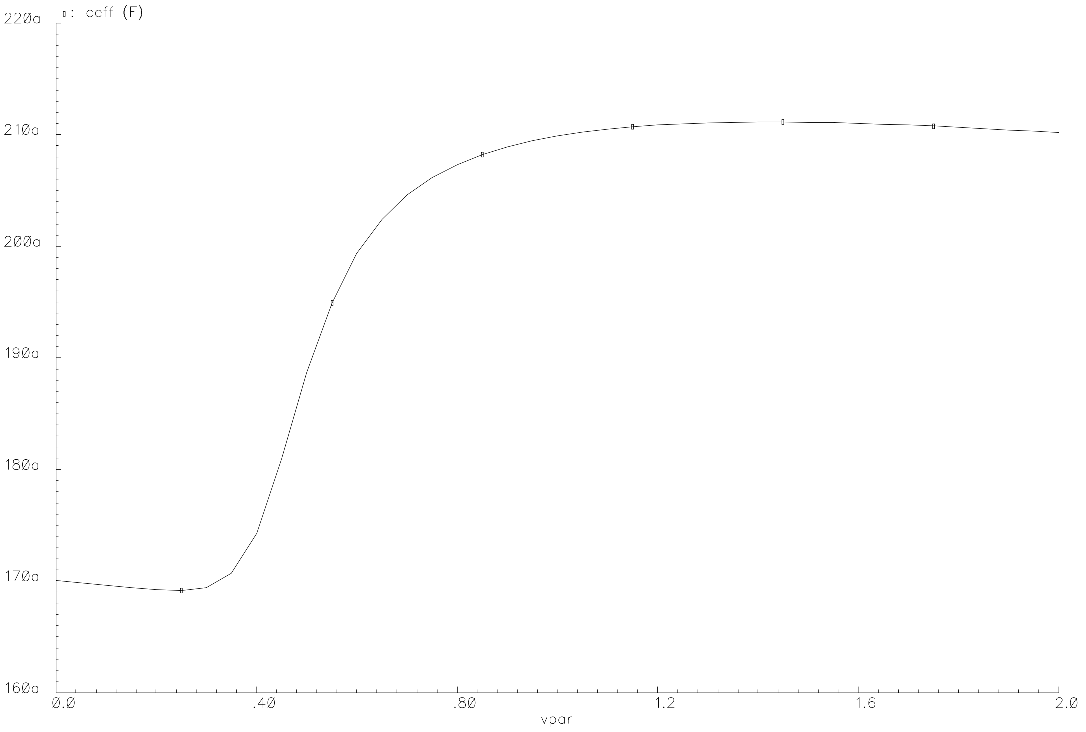


Figure 6.2: C–V curve of a minimum-size (120×60nm) varactor.

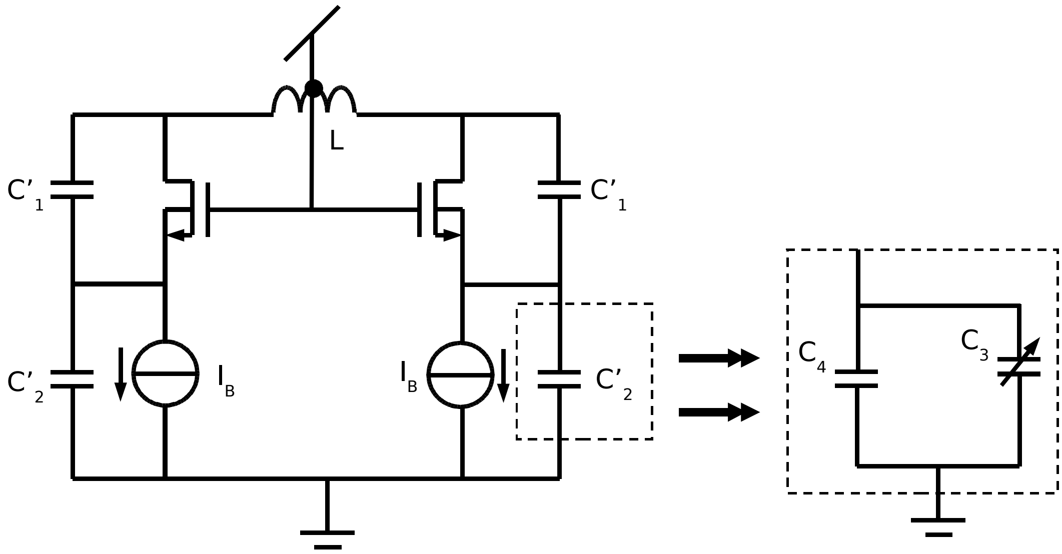


Figure 6.3: Schematic showing varactor connection.

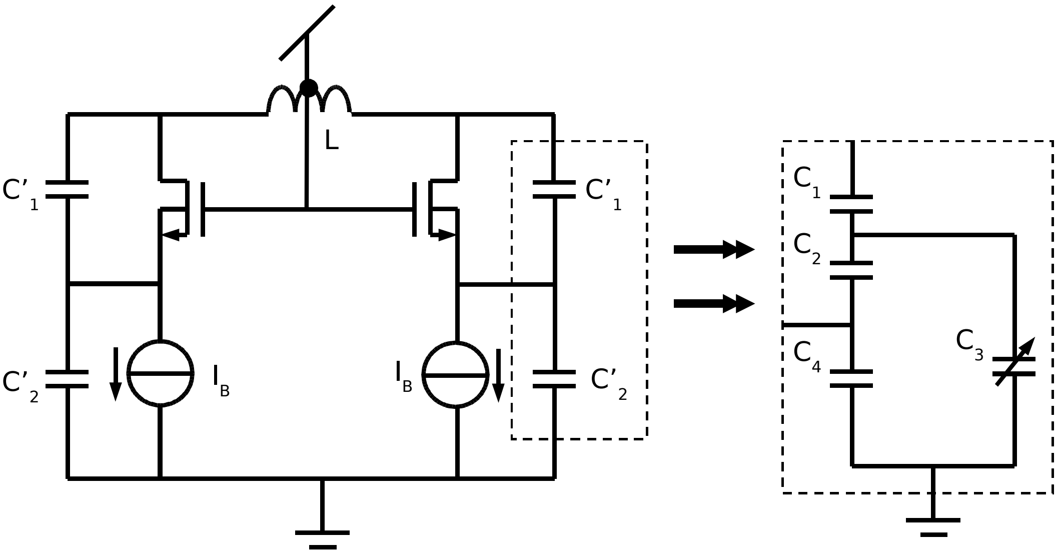


Figure 6.4: Schematic showing alternative varactor connection.

swings, as there is then no parallel capacitance to reduce the swing. This means that the coupling capacitor must be very small and the resulting varactor bank would be, compared to the chosen solution, quite enormous in chip area.

6.1 Tuning Linearity

The oscillator frequency is not linear with capacitance, but proportional to its inverse square-root (contrary to the RC-oscillator, where the time constant is directly proportional to C). For a small relative capacitance variation α, a linear approximation is valid, given as

$$\begin{aligned} f_0 = \frac{1}{2\pi\omega_0} = \frac{1}{2\pi\sqrt{L}}\cdot\frac{1}{\sqrt{C_{in}}} &= \frac{1}{2\pi\sqrt{L}}\cdot\frac{1}{\sqrt{C_0(1+\alpha)}} \\ &\approx \frac{1}{2\pi\sqrt{L}}\cdot\frac{1}{\sqrt{C_0}}\cdot(1-\frac{1}{2}\alpha). \end{aligned} \tag{6.3}$$

The tuning curve is not expected to be linear with the tuning word, but the above simplification is used to check if the tuning steps are in the correct order of magnitude. As a note, the step size should increase for higher frequencies, as the same change in capacitance α is then multiplied by a larger starting frequency. In practice this means that the tuning step size varies from 500kHz at the bottom of the tuning range upward in the direction of 1MHz, where the tuning range 11.36–12.17GHz is centered around 11.71GHz (determined using the scripts in Appendices E and F).

Chapter 7

Results

The topology choice was based on initial simulations, whose results are presented in Table 7.1. Phase noise was simulated using PSS and PNoise modes in Cadence. IRR was estimated using only a very limited number (∼10-20) of Monte Carlo runs per design. Power consumption and FoM were calculated using PSS data. The $1/f^3$ corner is in all quadrature solutions simulated to be approximately 100kHz. Note that the center tap of the coil should be biased at 750mV for the CCO to perform optimally (output resistance of this supply line has almost no influence due to the negligible current flow).

The Colpitts topology requires a higher supply voltage than the XCP topology to achieve sufficiently low phase noise; this confirms the estimation based on (3.8) and (3.9).

Topology	$\mathbf{P_{RMS}}$ **(mW)**	$\mathcal{L}$**(100kHz) (dBc/Hz)**	**FoM (dB)**	$\mathbf{V_{DD}}$ **(V)**	3σ **IRR (dB)**
Colpitts	50	-85	170	2	30
X-Coupled Pair	20	-85	180	1.2	20
Crossed-Capacitor	100	-85	165	2	40

Table 7.1: Comparison of different oscillator topologies.

Simulated negative series resistances at the DC operating point are presented in Table 7.2. The resistance of the coil is 2.35Ω; dividing the magnitude of the negative series resistance by this number gives the startup ratio. Note that in one of the cases the startup ratio is too low. This is not necessarily a problem; it is considered a simulation inaccuracy (due to inaccurate models for TSMC devices) that in the fast process corner the gain is so much lower. For the old NXP device models, the lowest startup gain was simulated to be 2.1, including parasitics. To get the startup ratio at this point, a cross-coupled pair was placed in parallel to the varactors, as described aptly in [10].

Condition	$-\mathbf{R_s}$**@11.7GHz (Ω)**	**Startup Ratio**
C_{var} at 50%, no parasitic C	13.52	5.75

Table 7.2: Negative resistance and startup ratio of the final design at 27°C across process corners and tuning range (continued on next page).

Condition		$-\mathbf{R_s}$@11.7GHz ($\boldsymbol{\Omega}$)	Startup Ratio
C_{var} at 50%	TYP corner	8.356	3.56
	slow corner	9.041	3.85
	fast corner	5.493	2.34
C_{var} at 0%	TYP corner	12.64	5.38
	slow corner	12.73	5.42
	fast corner	10.24	4.36
C_{var} at 100%	TYP corner	5.344	2.27
	slow corner	6.405	2.73
	fast corner	2.082	0.886

Table 7.2: Negative resistance and startup ratio of the final design at 27°C across process corners and tuning range.

This leads to the final schematic given with dimensions in Figure 7.1 (I part) and Figure 7.2 (Q part). The I^+, I^-, Q^+ and Q^- nodes are each buffered by a buffer, shown with dimensioning in Figure 7.3. The accompanying digital varactor implementation is not shown. The varactors are from the sources of the central transistors to ground, the coarse bank consisting of 0.76μm×0.76μm varactors and the fine bank consisting of 0.14μm×0.14μm varactors. Each bank is made up of 63 elements (equivalent to 6 bits in a binary control scheme), with 7 elements of 8LSB, 1 element of 4LSB and 3 elements of 1LSB. Thus, no elements larger than 8LSB need to be switched, in order to prevent nonmonotonicity due to mismatch.

The schematics and simulations of the mixers and the following buffers on the test chip are not presented, as these circuits were not designed by the author.

Phase noise without buffer is simulated at -83dBc/Hz@100kHz, with the oscillator amplitude at 3.8V_{pp}. This implementation typically consumes 70mW_{rms} of power from the 2V supply (working in the range of 1.6-2.0V). The buffers, connected across the coils, consume an additional 24mW_{rms} from the 1.2V supply, reducing the oscillator swing by a factor of approximately 4. The varactor is split into a fine and a coarse bank, with the minimum tuning step estimated at 500kHz. The total chip area of one quadrature oscillator including buffers is 210μm×480μm≈0.1mm^2.

Simulations with the (unfortunately inaccurate) TSMC device models are shown in Figures 7.4–7.11. High oscillator frequencies for some simulations are related to the omission of parasitic capacitances. Layouts of the oscillator and the test chip are shown in Figure 7.12 and Figure 7.13, respectively.

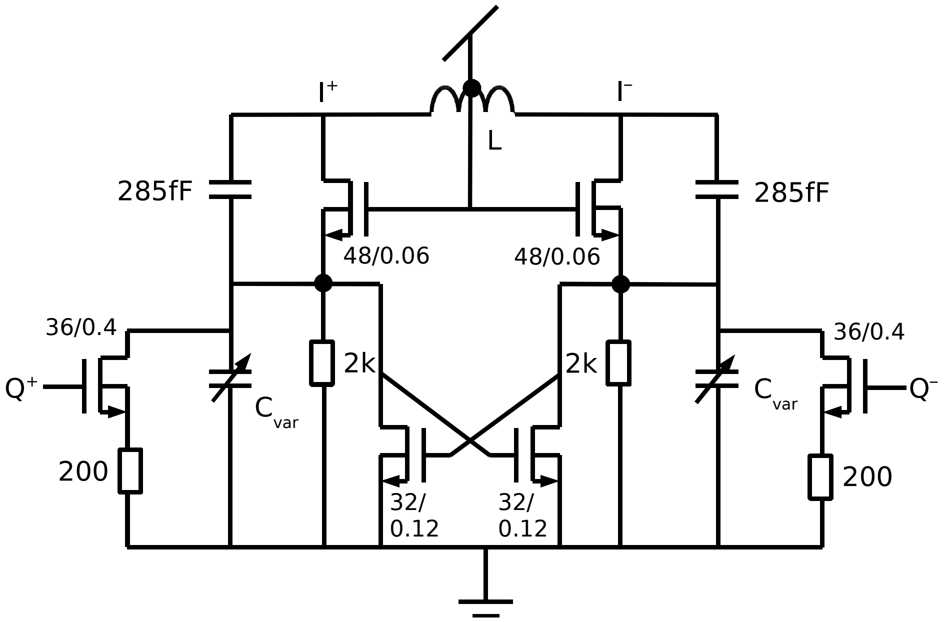


Figure 7.1: Final Colpitts schematic I part (varactors not shown).

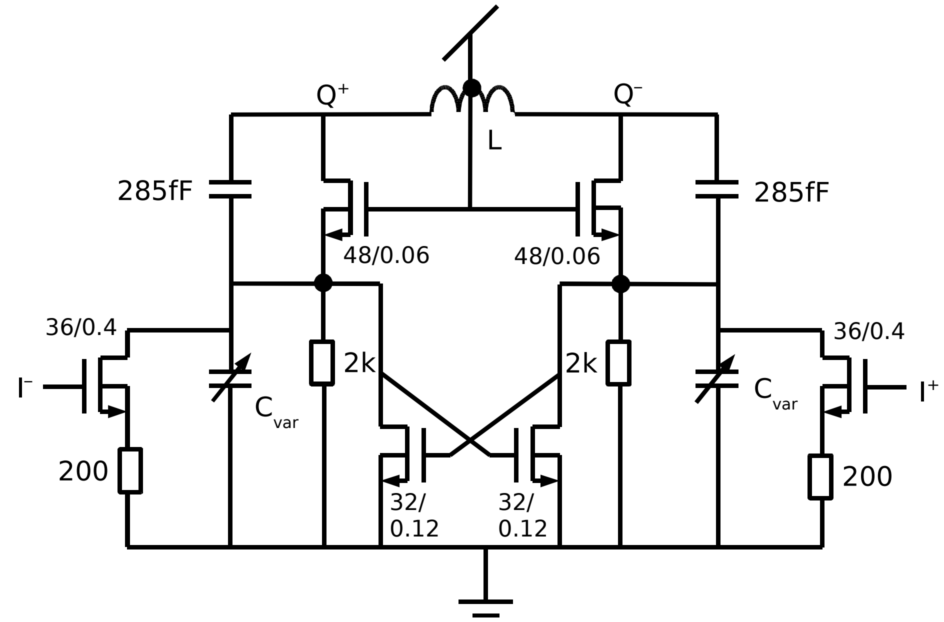


Figure 7.2: Final Colpitts schematic Q part (varactors not shown).

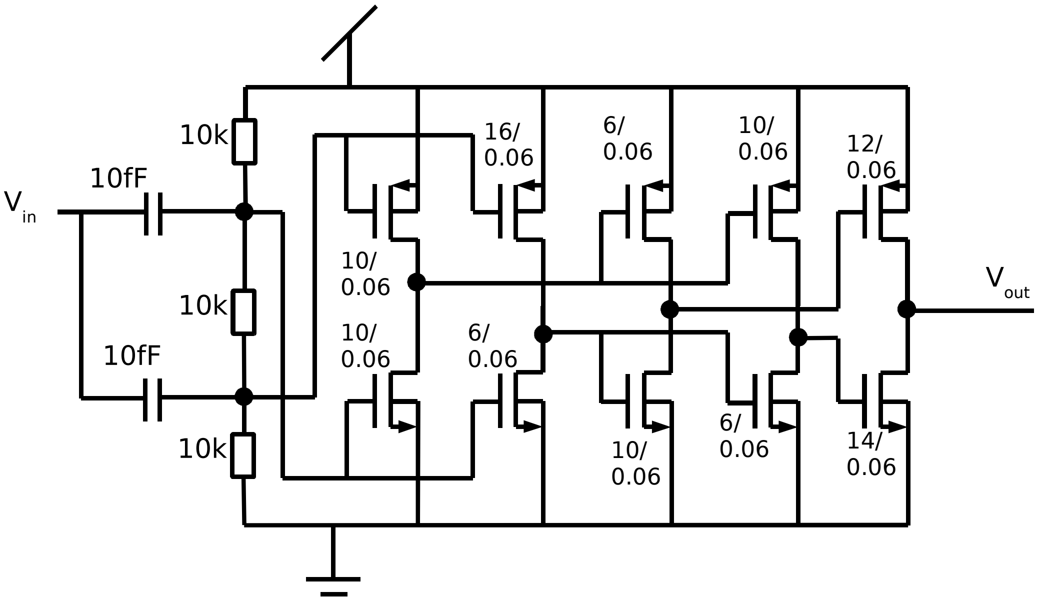


Figure 7.3: Final schematic of the biased 3-stage common-source/inverter buffer.

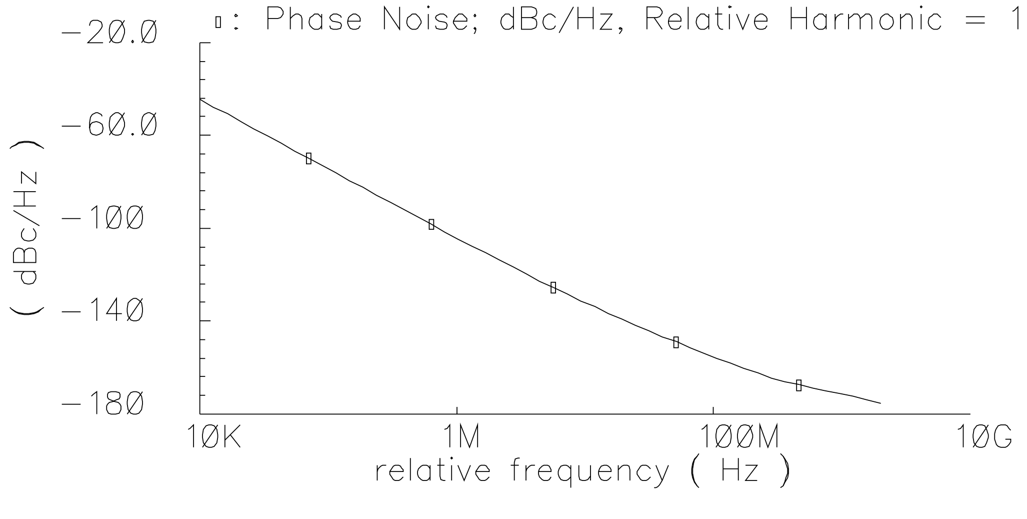


Figure 7.4: Phase noise plot generated using TSMC models and equivalent ideal capacitors instead of the varactor banks.

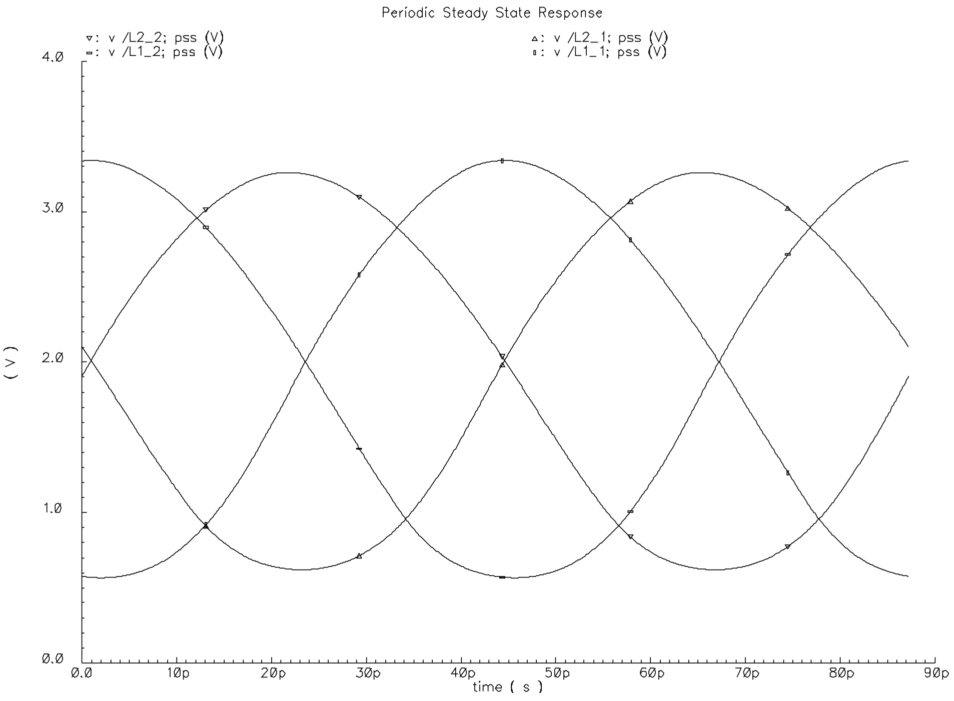


Figure 7.5: PSS waveforms of the four oscillator outputs in the presence of 2fF tank mismatch.

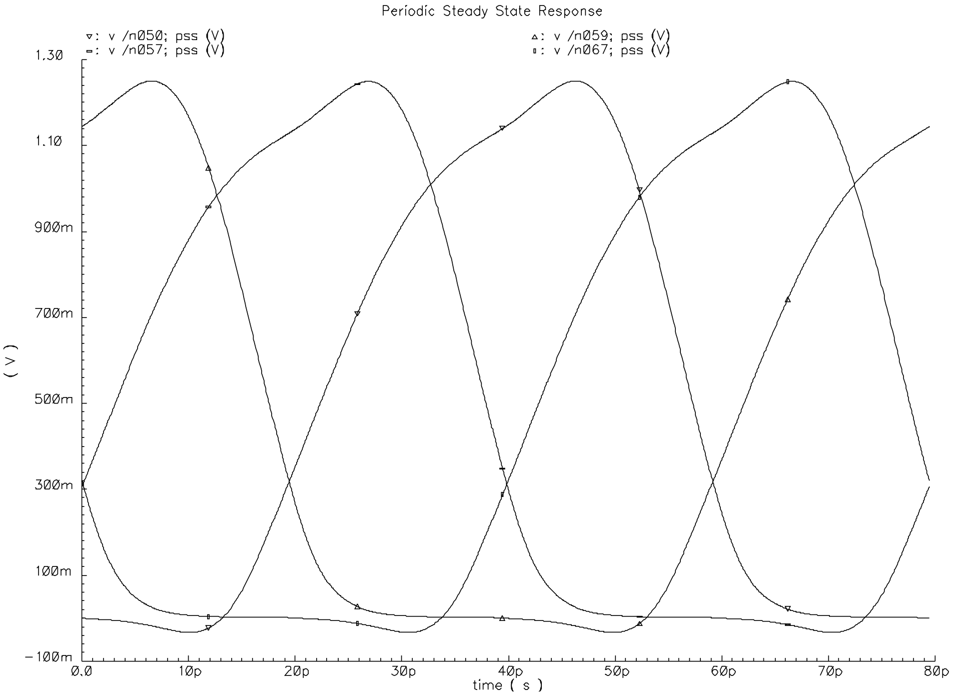


Figure 7.6: PSS waveforms of the four buffer outputs in the presence of 2fF tank mismatch.

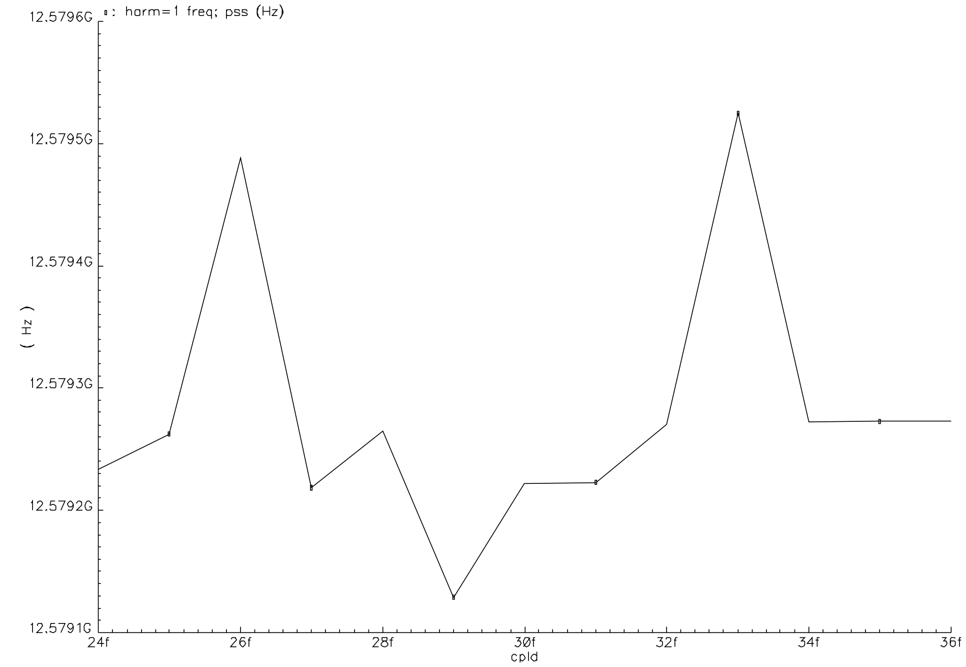


Figure 7.7: Oscillation frequency versus load capacitance at the buffer output. Simulation noise dominates over any systematic change in frequency.

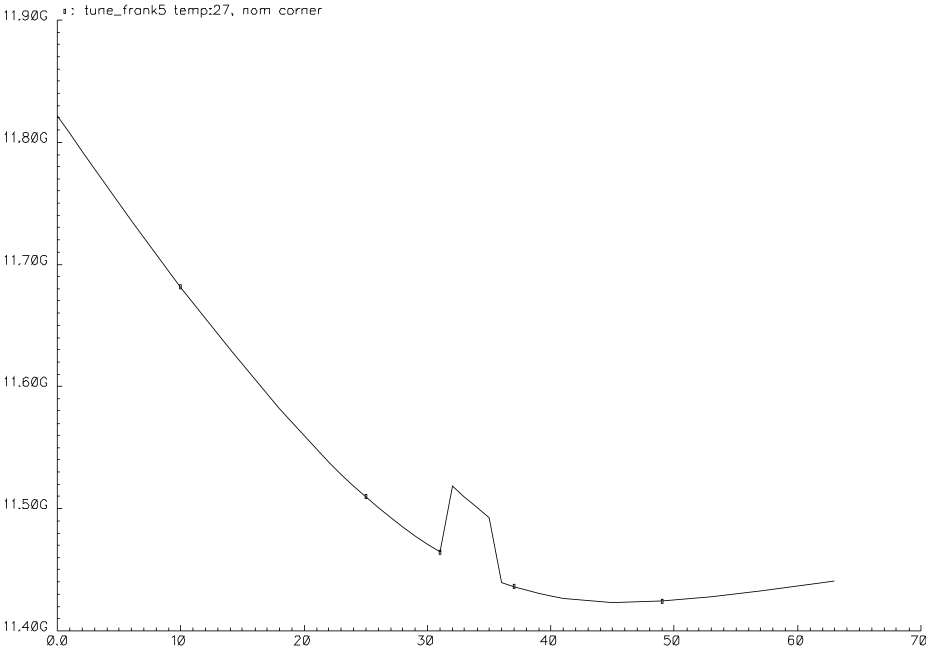


Figure 7.8: Tuning curve for the coarse varactor bank. The sudden step and the nonmonotonicity in the region of high capacitance are known to be simulation artifacts.

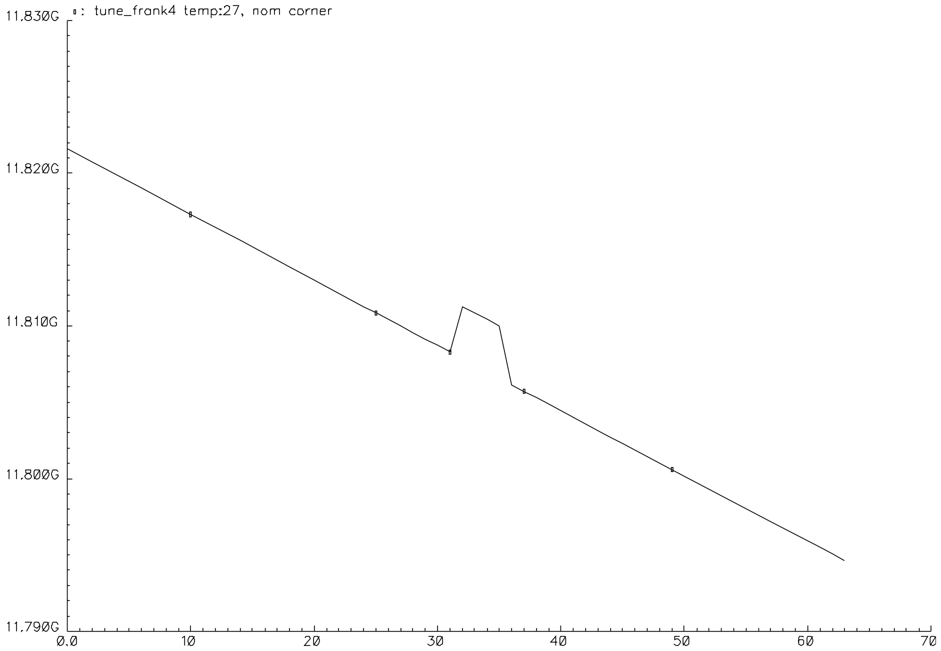


Figure 7.9: Tuning curve for the fine varactor bank. The sudden step is a known simulation artifact.

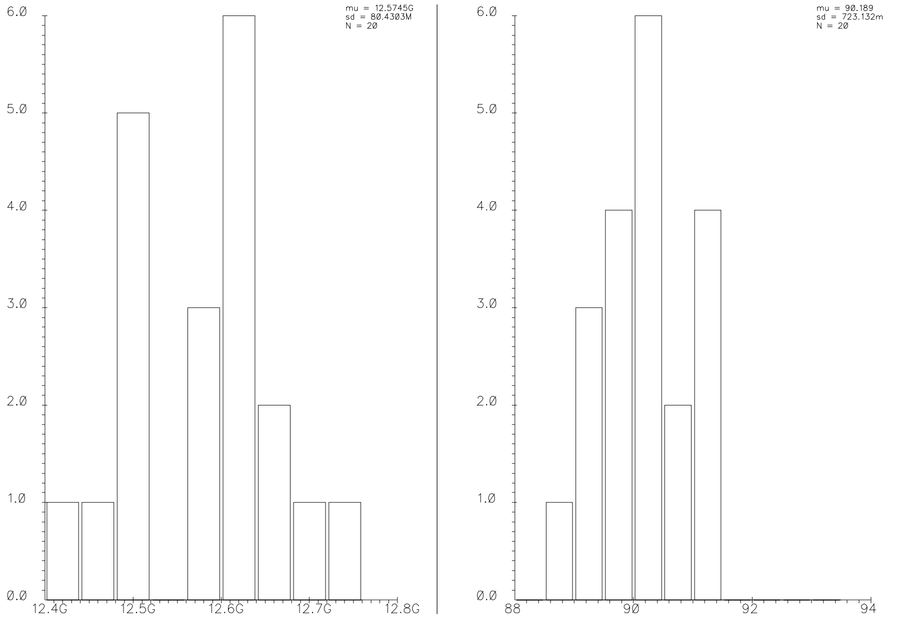


Figure 7.10: Monte Carlo histogram showing variation in oscillation frequency (left) and quadrature angle (right).

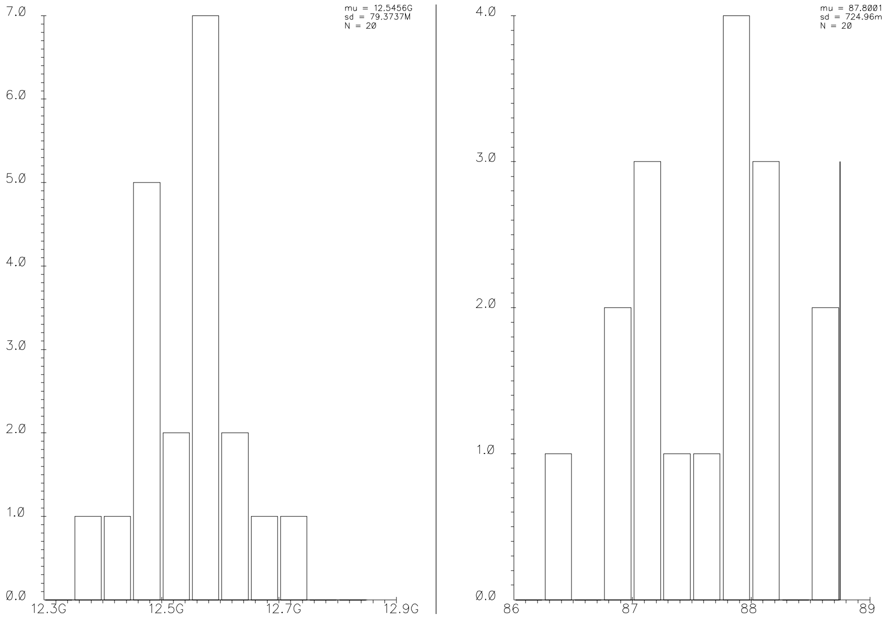


Figure 7.11: Monte Carlo histogram showing variation in oscillation frequency (left) and quadrature angle (right) in the presence of an additional 2fF tank mismatch.

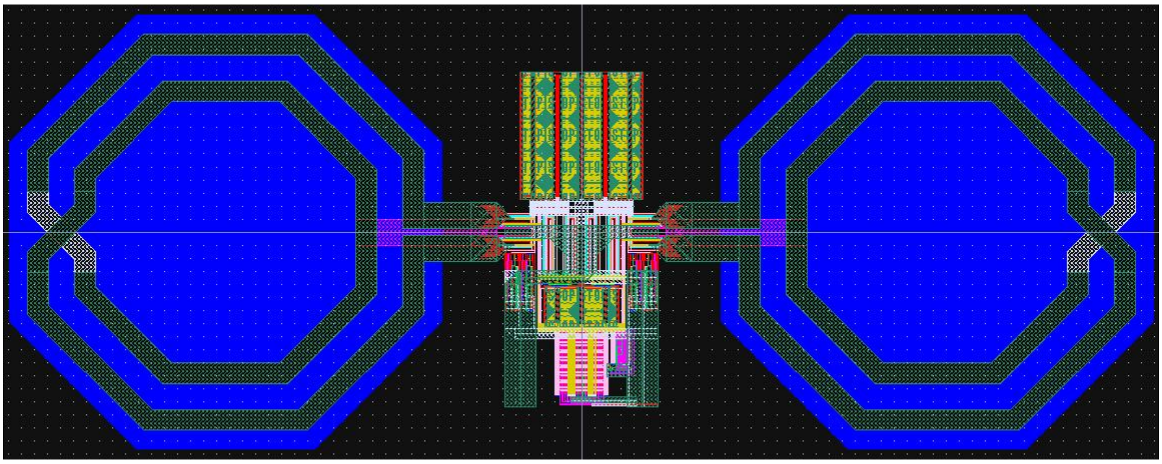


Figure 7.12: Final layout of the QDCO including buffers.

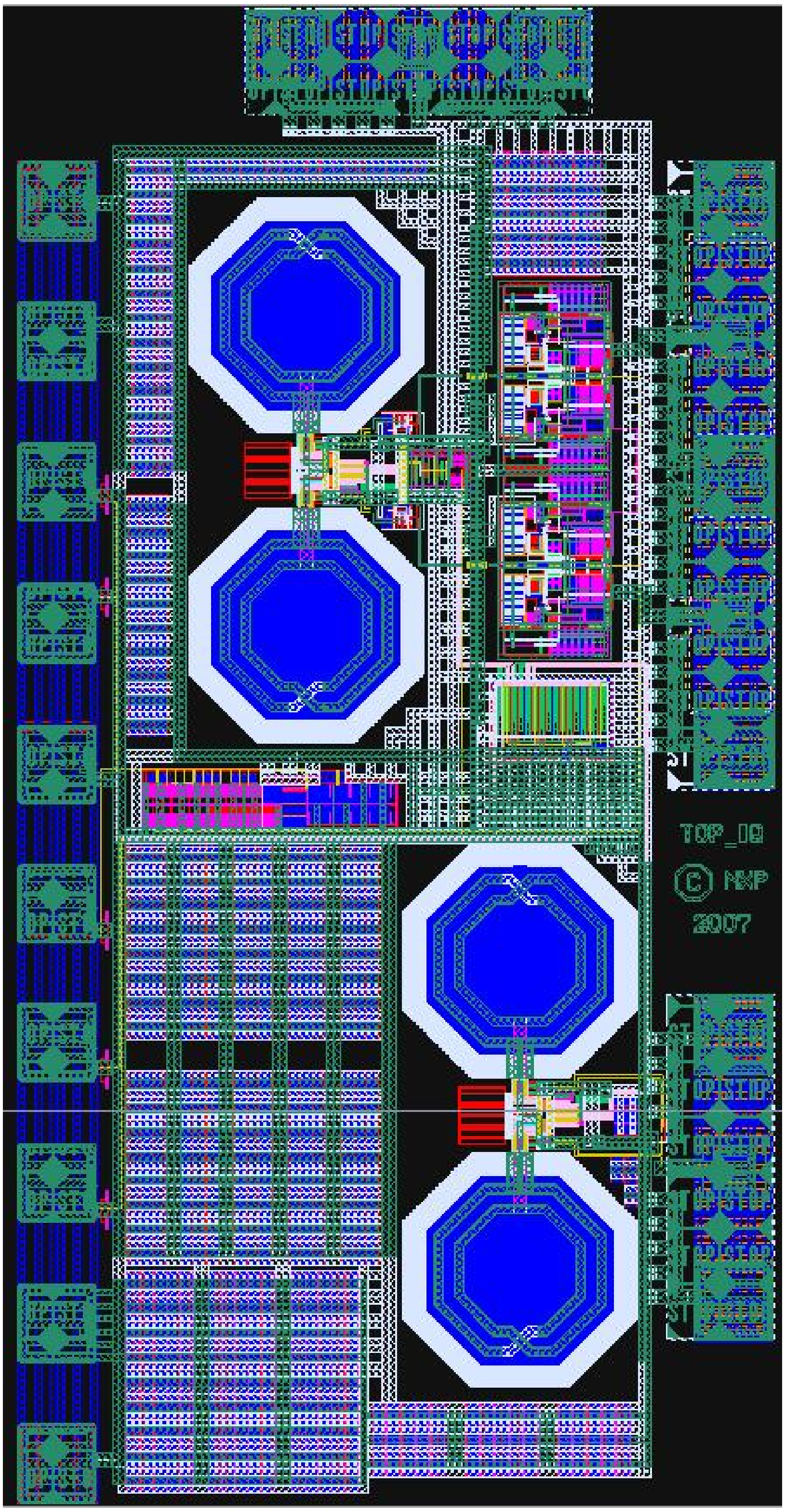


Figure 7.13: Final layout of the test chip.

Chapter 8

Benchmarking

The circuits that form the reference for this QDCO are given in [16]. In [27] a CMOS VCO of higher frequency is presented, but the quadrature accuracy, strangely, is measured on an 8.5GHz scaled VCO, and only the result for a single IRR measurement is given. The author believes that the matching problems and parasitic mutual coupling will increase at higher frequency, making the quadrature accuracy for this concept unacceptable. In [28] a 32GHz QVCO in an SiGe process is presented[1], which is actually the only chip that can match the performance of the DCO designed in this report, uses five times more power and needs a tremendous supply voltage of 5V (which is bad for integrability). Finally, a 16GHz QVCO in SiGe (running on a reasonable 2.7V supply) is presented in [23]. Its phase noise performance is excellent, but the quadrature accuracy of 6 degrees RMS (equivalent to a 3-σ spread of 18 degrees, see [29]) is vehemently insufficient. Curiously, the authors consider the matching of tail current sources to be crucial for the quadrature accuracy.

The current state-of the art in CMOS is an IRR of more than 40dB with a FoM of around 185. There are several reasons why these specifications are difficult to achieve at 11.7GHz.

First of all, injection locking is not an option at 11.7GHz with the desired phase noise, as a locking current source severely degrades phase noise performance. Also, at higher frequency the dI/dt in the coils is larger, increasing the effect of mutual coupling (which is known to have a detrimental effect on the IRR, see [21]). Because the oscillator tanks are very strongly coupled, however, this might not be as dominant a problem in the current oscillator as would appear from literature.

Finally, it is not customary to compensate so strongly for tank mismatches, as most CMOS quadrature oscillators are designed for lower frequencies (the comparison in [16] does not include oscillators above 5GHz). As the capacitor mismatch scales with $1/\sqrt{WL}$ and therefore increases with decreasing capacitance (under the condition of minimal parasitics), the achievable IRR for a certain coupling type becomes a function of frequency and it becomes more difficult to achieve a certain IRR as frequency increases.

In this context, it becomes desirable to include the relationship between IRR and operating frequency as a separate term into the FoM. The relative 3-σ mismatch error scales approximately with the inverse square-root of the capacitance, so scales linearly with frequency. Therefore the relative frequency mismatch scales with the square-root of the frequency. To a first order, the quadrature coupling strength scales with the square of

[1] It appears that in equation (1) of the article, the authors forgot to square the capacitances.

the relative frequency mismatch (Taylor expansion of the cosine around zero, or the ISF around an amplitude maximum). Therefore the quadrature error does not scale linearly with the mismatch. However, the linear approximation fits quite well empirically with QVCOs from literature, and therefore gives the following reasonable FoM expression:

$$\begin{aligned} \mathrm{FoM}_Q \; &= \; -\mathcal{L}(\Delta f) + 20\cdot\log_{10}\left(\frac{f_0}{\Delta f}\right) - 10\cdot\log_{10}\left(\frac{P_{diss}}{1\mathrm{mW}}\right) \\ & \quad +10\cdot\log_{10}(\mathrm{IRR}) + 30\cdot\log_{10}\left(\frac{f_0}{1\mathrm{THz}}\right). \end{aligned} \tag{8.1}$$

The trade-off between IRR and power is a reasonable approximation of what is observed between the different topologies studied in this project. The last term indicates that the difficulty of making a good quadrature coupling is a very strong function of the operating frequency. With this term included, the oscillators in this project are comparable to (i.e. lying on the line extrapolated from) the best ones found in literature, although the tuning ranges of the oscillators in literature are generally a bit larger. A brief comparison is shown in Table 8.1.

Reference	**f_0**	**FoM**	**IRR**	**FoM_Q**
	GHz	**dB**	**dB**	**dB**
[8]	4.89	185	33	149
[10]	1.87	176.5	41	136
[16]	1.86	185	46	149
This work (simulated)	**11.7**	**167**	**30**	**139**

Table 8.1: FoM comparison of different QVCOs with and without IRR performance included.

In short, the high oscillator frequency prohibits injection-locking, causes stronger parasitic mutual inductance between the tanks, and limits the IRR –and due to the strong coupling also the phase noise– because of the small tank capacitances.

The advantage of a quadrature solution, however, is clear. ADCs with a bandwidth equal to half the Ku-band may be employed, making it possible to convert the entire band using two ADCs. This eliminates lots of problems related to an additional IF-stage and filtering into subbands for multiple ADCs. A pair of 2Gsamples/s ADCs consumes 400mW, making the QDCO power consumption pale in comparison. If in an IF-solution the filtering and additional DCO do not make much of a difference (quite an optimistic estimate), still the ADCs must have a total bandwidth equal to the entire band, which at the same FoM comes down to the same 400mW. Splitting one ADC into multiple ADCs is almost never advantageous for power consumption and chip area, making it a safe assumption that if specifications can be met using a QDCO with low power consumption, this solution will always be better.

Chapter 9

Conclusion

After reviewing various ways of generating quadrature baseband signals in a Ku-band satellite receiver, it is concluded that a quadrature *LC*-oscillator, operating at 11.7GHz with an IRR of 30dB and a phase noise of -85dBc/Hz@100kHz, is the best means to this end. Three quadrature oscillator-topologies were studied, among which the novel CCO topology, which seems very suitable for future CMOS oscillator designs, and the more traditional XCP and Colpitts topologies.

Of the three topologies studied, both the Colpitts topology and the CCO topology meet the estimated IRR requirement of 30dB, with the Colpitts showing a better FoM and a wider tuning range, whereas the CCO topology can achieve a better quadrature accuracy. The poor IRR performance of the XCP topology is attributed to the poor matching properties of gate-drain capacitances. The Colpitts topology is able to meet phase noise specifications due to its ability to run at a high supply voltage of 2V.

After analysis, it is concluded that for phase noise performance, not only the coupling angle of first-harmonic coupling, but also the strength of the coupling have a clear optimum. It is further concluded that the optimum coupling strength w.r.t. phase noise cannot be directly achieved in the presence of realistic tank mismatches, as the quadrature coupling must then be much stronger.

A frequency tuning mechanism, designed for a digital PLL and capable of compensating for process spread, has been added to the oscillator, including three-stage-inverter buffers. The complete oscillator core is simulated to consume approximately 70mW$_{\text{rms}}$ at a supply voltage of 2V, with the buffers consuming an additional 24mW$_{\text{rms}}$. This is reasonably in line with other published quadrature oscillators.

A chip layout of the concept has been made, with two oscillators of which one has its buffer output directly connected to the bondpad, and the other is first passed through a mixer stage, such that the quadrature accuracy can be measured properly. Once some samples are produced, their phase noise spectra and quadrature accuracy still need to be measured. This allows simulation inaccuracies to be identified, such that a better oscillator may be designed.

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Appendix A

Derivation ISF of LC-Oscillator

In the 1998 paper by Hajimiri and Lee [3], the shape of the ISF of an LC-oscillator is simply given without derivation. The derivation for a lossless parallel LC-tank (a close approximation of reality) is given below, uncovering an inaccuracy in the original paper.

A.1 Definitions

For a parallel LC-tank, due to the choice of reference directions for the voltage and the current, we must reverse the sign of one of the component equations. This is done as follows. The choice of the minus sign eases the derivation significantly.

$$V = -j\omega LI = \frac{-jI}{C\omega}. \tag{A.1}$$

We will use the time domain, so it is useful to define the phase relationship between voltage and current as follows.

$$\begin{aligned} V &= V_0 \cdot \sin \omega_0 \cdot t. && \text{(A.2)} \\ I &= I_0 \cdot \cos \omega_0 \cdot t. && \text{(A.3)} \end{aligned}$$

We define, again for simplicity, the tank energy as

$$E_0 = \frac{1}{2}CV^2 + \frac{1}{2}LI^2 = \frac{1}{2}CV_0^2 \sin^2 \omega_0 \cdot t + \frac{1}{2}LI_0^2 \cos^2 \omega_0 \cdot t. \tag{A.4}$$

Note also that

$$E_0 = \frac{1}{2}CV_0^2 = \frac{1}{2}LI_0^2 \tag{A.5}$$

and

$$q_{max} = C \cdot V_0 = \frac{2E_0}{V_0}. \tag{A.6}$$

This allows us to define the ratio of the two tank amplitudes as follows.

$$\frac{V_0}{I_0} = \sqrt{\frac{L}{C}}. \tag{A.7}$$

A.2 Derivation

If we now consider only one oscillation period, we may simply substitute the phase angle θ for $\omega_0 \cdot t$. The phase angle may always be derived from the instantaneous voltage and current.

$$\begin{aligned} \frac{V}{I} = \frac{V_0 \cdot \sin\theta}{I_0 \cdot \cos\theta} &= \frac{V_0}{I_0} \cdot \tan\theta = \sqrt{\frac{L}{C}} \cdot \tan\theta \\ \iff \qquad \theta &= \arctan\left(\frac{V}{I} \cdot \sqrt{\frac{C}{L}}\right) \end{aligned} \tag{A.8}$$

Its instantaneous sensitivity, normalized to a unity voltage change[1], is simply the derivative with respect to the voltage, which is worked out below (using the fun-to-derive derivative of arctan(x) [30] [31]).

$$\begin{aligned} \frac{d\theta}{dV} = \frac{d}{dV}\left(\arctan\left(\frac{V}{I} \cdot \sqrt{\frac{C}{L}}\right)\right) &= \frac{1}{1 + \frac{V^2}{I^2} \cdot \frac{C}{L}} \cdot \frac{1}{I} \cdot \sqrt{\frac{C}{L}} \\ &= \frac{I}{LI^2 + CV^2} \cdot \sqrt{LC} = \frac{V_0 \cdot C \cdot \cos\theta}{2 \cdot E_0}. \end{aligned} \tag{A.9}$$

The ISF is the sensitivity normalized to a unity current impulse[2] or $d\theta/dq$, so we are not quite there yet. The voltage step amplitude is proportional to $1/C$ times the injected charge (interestingly, the inductor has nothing to do with the charge injection), yielding, after some substitutions for V_0, the following expression, which is not dimensionless, as the one in the Hajimiri & Lee paper, but has the unit radians per Coulomb (phase change per disturbance charge). The subscript F denotes the formal correctness; in the next section it is shown that the original definition is formally incorrect.

$$\Gamma_F(\theta) = \omega_0 \cdot \sqrt{\frac{L}{2 \cdot E_0}} \cdot \cos\theta = \frac{\cos\theta}{q_{max}}. \tag{A.10}$$

From this, it follows that the sensitivity of the phase depends on the cosine of the phase, decreases with the square-root of the tank energy (in other words, linearly with either current or voltage amplitude), and increases linearly with frequency. Once frequency and tank energy are chosen fixed, the ISF scales with the square-root of the inductance, i.e. a smaller inductance yields also a smaller ISF. Intuitively, a larger capacitor is less sensitive to noise currents, as the relative charge noise is then smaller. This intuition is now confirmed.

[1] For large changes in θ, one must actually do a path integral over $d\theta$ to obtain accurate results.

[2] Normalized, because a unity current impulse is a Coulomb of charge, which is rediculously enormous! In the paper by Hajimiri and Lee [3], the ISF is defined as the sensitivity to the actual impulse, ignoring the fact that a path integral must be done for large variations in θ. Intuitively, adding a current impulse of infinite magnitude leads to an infinite V/I ratio, or an amplitude maximum, and not simply the phase at the injection start plus the ISF at the injection start multiplied by the impulse magnitude.

A.3 Correction for Large Impulses

For large current impulses of magnitude K, applied at starting voltage V_1 and leading to voltage V_2, we have

$$V_2 - V_1 = \frac{1}{C}\cdot\int_{0^-}^{0^+} K\cdot\delta(t)dt = \frac{K}{C}. \tag{A.11}$$

Deriving the phase change involves doing a rather simple integral.

$$\begin{aligned}\theta_2 - \theta_1 &= \int_{V_1}^{V_2} \frac{d\theta}{dV}\cdot dV = \int_{\theta(V_1)}^{\theta(V_2)} d\theta \\ &= \arctan\left(\frac{V_1 + K/C}{I}\cdot\sqrt{\frac{C}{L}}\right) - \arctan\left(\frac{V_1}{I}\cdot\sqrt{\frac{C}{L}}\right).\end{aligned} \tag{A.12}$$

This correction has no practical value, because the linear approximation made by directly convolving the ISF with the noise is generally very good and much faster to compute, but it clarifies the already very difficult phase noise analysis by a small amount.

In [3] it is not clear that an approximation of the path integral is made (in fact, this can be quite confusing). Because the phase change depends nonlinearly on the impulse magnitude K, the system is nonlinear and it is formally incorrect to define an impulse response. A definition in infinitely small changes, however, such as $d\theta/dq$, does not assume linearity of the impulse response and is therefore formally correct.

Appendix B

On Constant Quadrature Currents

The fact that the total current in quadrature buffer circuits is constant, depends on their differential implementation. The reason why is clarified in this appendix.

For a quadrature buffer, the input voltages may be expressed as a sine and a cosine. Due to the transistors' square-law V-I conversion, one might assume we can simply apply $\sin^2(\omega{\cdot}t) + \cos^2(\omega{\cdot}t) = 1$ to arrive at a constant total output current. It is unfortunately not so straightforward, as the square-law model is only valid above the threshold voltage and therefore asymmetrical about the origin.

For single-ended quadrature signals, accounting for the asymmetry by adding a constant term $K \neq 0$, we therefore arrive at

$$\begin{aligned}
I_I &= (K + \cos(\omega{\cdot}t))^2 = K^2 + 2{\cdot}K{\cdot}\cos(\omega{\cdot}t) + \cos^2(\omega{\cdot}t), \\
I_Q &= (K + \sin(\omega{\cdot}t))^2 = K^2 + 2{\cdot}K{\cdot}\sin(\omega{\cdot}t) + \sin^2(\omega{\cdot}t), \\
I_{total} &= 1 + 2{\cdot}K^2 + 2{\cdot}K{\cdot}\cos(\omega{\cdot}t) + 2{\cdot}K{\cdot}\sin(\omega{\cdot}t). \qquad \text{(B.1)}
\end{aligned}$$

This is not constant! For differential signals, however, the following results.

$$\begin{aligned}
I_{I+} &= (K + \cos(\omega{\cdot}t))^2 = K^2 + 2{\cdot}K{\cdot}\cos(\omega{\cdot}t) + \cos^2(\omega{\cdot}t). \\
I_{I-} &= (K - \cos(\omega{\cdot}t))^2 = K^2 - 2{\cdot}K{\cdot}\cos(\omega{\cdot}t) + \cos^2(\omega{\cdot}t). \\
I_{Q+} &= (K + \sin(\omega{\cdot}t))^2 = K^2 + 2{\cdot}K{\cdot}\sin(\omega{\cdot}t) + \sin^2(\omega{\cdot}t). \\
I_{Q-} &= (K - \sin(\omega{\cdot}t))^2 = K^2 - 2{\cdot}K{\cdot}\sin(\omega{\cdot}t) + \sin^2(\omega{\cdot}t). \\
I_{total} &= 4{\cdot}K^2 + 2. \qquad \text{(B.2)}
\end{aligned}$$

The single sine and cosine terms disappear in the asymmetrical differential quadrature sum, leaving a constant current. If the total current is constant, elaborate regulators are not required in order to keep the supply voltage constant, simplifying circuit design.

Appendix C

CCO and Process Scaling

There are several trends in the downscaling of CMOS processes, and it is anticipated that the CCO topology is very fit to deal with these changes.

Firstly, minimum transistor length will decrease. This is good news, as the same gain can be made with a smaller gate capacitance, enlarging the currently problematic tuning range of the CCO. Also, less gate capacitance means less variation in tank capacitance due to process spread, because the fringe capacitors vary much less in capacitance than do gate capacitances.

Secondly, especially for the anticipated 32nm FinFET transistors, making low-ohmic source and drain contacts is becoming problematic. This is not such a big deal in the CCO, as the channel is completely decoupled from the LC-tank.

As frequency gets higher (60GHz CMOS projects are already underway), the CCO has an additional advantage. In (3.11) the term with the output resistance vanishes for high frequencies. This also explains why the CCO is the only topology for which the phase noise does not increase with frequency; it also means that the CCO should typically be applied at frequencies near the f_T of the process.

Finally, there is a trend that mismatch becomes worse as the device sizes continue to shrink. As the CCO in quadrature configuration shows much better IRR performance than any other topology, this indicates less sensitivity to mismatch.

In conclusion, the CCO topology and its study may be worth keeping for future reference, especially since its power-no-object phase noise performance is superior in both single and quadrature configurations. In case the structure is used in a future system, the designer may have a closer look at the start-up conditions, as simulations suggest a different optimum ratio of negative to positive resistance than for more traditional topologies, probably due to different gate biasing and different large-signal (describing function) gain.

Appendix D

Estimation of Parasitic Inductance

Below are some formulæ [7] that give first-order approximations of the behavior of straight on-chip interconnect lines:

$$
\begin{aligned}
l &= v \cdot t, && \text{(D.1)}\\
v &= \frac{c}{\sqrt{\epsilon_r}}, && \text{(D.2)}\\
t &= \sqrt{LC}, && \text{(D.3)}\\
Z_0 &= \sqrt{\frac{L}{C}}. && \text{(D.4)}
\end{aligned}
$$

These lead to the following expressions for the inductance and characteristic impedance of the line:

$$
\begin{aligned}
L &= \frac{l^2 \epsilon_r}{c^2 C}, && \text{(D.5)}\\
Z_0 &= \frac{l\sqrt{\epsilon_r}}{c \cdot C}. && \text{(D.6)}
\end{aligned}
$$

In all cases, $c \approx 3 \cdot 10^8$m/s and, for the CMOS process used in this project, $\epsilon_r \approx 4$. The expression for the parasitic inductance is known to give an accurate (within a few percent) first-order approximation [7].

The capacitance scales approximately linearly with length, leading to an almost linear dependence of the inductance on the wire length, which turns out to be approximately 60pH/100μm for a 0.4μm wide line with Metal 4 as the lowest layer. This is only a factor 0.6 compared to the formula given for bondwires in [2, p. 140].

The characteristic impedance of the line is 95Ω.

Appendix E

Fine Tuning Script Colpitts QDCO

```
;%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;%%%             Simulation of QDCO tuning curves                 %%%
;%%%                   Frank Leong, May 2007                      %%%
;%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; np_tuningCharacteristic( list( 0) list(0 4 8 31 63) list( 27 ) list( 1 ) )
; np_tuningCharacteristic( list( 0) list(0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63) list( 27 ) list( 1 ) )
; load( "./tune_frank4.ocn")


procedure( run_VCO_analysis( coarse fine tempval corner )

simulator( 'spectre )

design( "/home/nlv15336/paulg/simulation/pss_tune_colpitts2/spectre/schematic/netlist/netlist")
resultsDir( "/home/nlv15336/paulg/simulation/pss_tune_colpitts2/spectre/schematic/psf" )


  if( corner==0
  then
    modelFile( '("/home/nlv15336/Workareas4/UTC065_nlv15336/b6Ra1/include_snsp.scs" "" ) )
  )

  if( corner==1
  then
    modelFile( '("/home/nlv15336/Workareas4/UTC065_nlv15336/b6Ra1/include_nominal.scs" "" ) )
  )

  if( corner==2
  then
    modelFile( '("/home/nlv15336/Workareas4/UTC065_nlv15336/b6Ra1/include_fpfn.scs" "" ) )
  )

  ;analysis('pnoise ?relharmnum "1"  ?start "1e3"  ?stop "1e9"
  ;             ?maxsideband "5"  ?p "/n075"  ?n "/gnd!"  ?oprobe ""
  ;             ?iprobe ""  ?refsideband ""  )
  analysis('pss ?fund "8G"  ?harms "5"  ?errpreset "conservative"
                ?tstab "5n"  ?saveinit "no"  ?p "/n075"  ?n "/gnd!"
                ?maxstep "1p"  ?method "gear2only"  ?tstabmethod "gear2only"  )
  desVar(         "clsim5" 3.5371p      )
desVar(         "clsim1" 37.2286f      )
desVar(         "clsim2" 300.679f      )
desVar(         "clsim3" -10.0821f     )
desVar(         "clsim4" 5.51919f      )
desVar(         "llsim4" 80.2779p      )
desVar(         "llsim5" -129.703p     )
desVar(         "llsim2" 7.16401p      )
desVar(         "llsim6" -0.495176p    )
desVar(         "llsim8" -5.54881p     )
desVar(         "llsim3" 18.1179p      )
desVar(         "llsim1" 430.961p      )
desVar(         "llsim7" -1.25231p     )
desVar(         "rlsim2" 2.98229       )
desVar(         "rlsim4" 1.69803       )
desVar(         "rlsim1" 6.37948       )
desVar(         "rlsim3" 1.51149       )
desVar(         "rlsim5" 1.56008       )
desVar(         "rlsim6" -0.415667     )
desVar(         "rlsim8" 0.483         )
desVar(         "rlsim9" 707.547       )
desVar(         "rlsim7" 1.955         )
;desVar(        "fine" fine   )
;desVar(        "coarse" coarse        )

if( mod(fine 4)==0
then
  desVar(       "thrm1_0" 0   )
  desVar(       "thrm1_1" 0   )
  desVar(       "thrm1_2" 0   )
)
if( mod(fine 4)==1
then
  desVar(       "thrm1_0" 1.2 )
  desVar(       "thrm1_1" 0   )
  desVar(       "thrm1_2" 0   )
)
 if( mod(fine 4)==2
then
  desVar(       "thrm1_0" 1.2 )
  desVar(       "thrm1_1" 1.2 )
  desVar(       "thrm1_2" 0   )
)
 if( mod(fine 4)==3
then
  desVar(       "thrm1_0" 1.2 )
  desVar(       "thrm1_1" 1.2 )
  desVar(       "thrm1_2" 1.2 )
)
if( mod(fine 8)>=4
then
   desVar(      "thrm4" 1.2   )
else
   desVar(      "thrm4" 0     )
)
if( fine>=8
then
   desVar(      "thrm8_0" 1.2 )
else
```

```
   desVar(      "thrm8_0" 0   )
)
if( fine>=16
then
   desVar(      "thrm8_1" 1.2 )
else
   desVar(      "thrm8_1" 0   )
)
 if( fine>=24
then
   desVar(      "thrm8_2" 1.2 )
else
   desVar(      "thrm8_2" 0   )
)
if( fine>=36
then
   desVar(      "thrm8_3" 1.2 )
else
   desVar(      "thrm8_3" 0   )
)
 if( fine>=40
then
   desVar(      "thrm8_4" 1.2 )
else
   desVar(      "thrm8_4" 0   )
)
if( fine>=48
then
   desVar(      "thrm8_5" 1.2 )
else
   desVar(      "thrm8_5" 0   )
)
if( fine>=56
then
   desVar(      "thrm8_6" 1.2 )
else
   desVar(      "thrm8_6" 0   )
)


if( mod(coarse 4)==0
then
  desVar(       "cthrm1_0" 0  )
  desVar(       "cthrm1_1" 0  )
  desVar(       "cthrm1_2" 0  )
)
if( mod(coarse 4)==1
then
  desVar(       "cthrm1_0" 1.2        )
  desVar(       "cthrm1_1" 0  )
  desVar(       "cthrm1_2" 0  )
)
 if( mod(coarse 4)==2
then
  desVar(       "cthrm1_0" 1.2        )
  desVar(       "cthrm1_1" 1.2        )
  desVar(       "cthrm1_2" 0  )
)
```

```
 if( mod(coarse 4)==3
then
  desVar(       "cthrm1_0" 1.2        )
  desVar(       "cthrm1_1" 1.2        )
  desVar(       "cthrm1_2" 1.2        )
)
if( mod(coarse 8)>=4
then
   desVar(      "cthrm4" 1.2  )
else
   desVar(      "cthrm4" 0    )
)
if( coarse>=8
then
   desVar(      "cthrm8_0" 1.2        )
else
   desVar(      "cthrm8_0" 0  )
)
if( coarse>=16
then
   desVar(      "cthrm8_1" 1.2        )
else
   desVar(      "cthrm8_1" 0  )
)
 if( coarse>=24
then
   desVar(      "cthrm8_2" 1.2        )
else
   desVar(      "cthrm8_2" 0  )
)
if( coarse>=36
then
   desVar(      "cthrm8_3" 1.2        )
else
   desVar(      "cthrm8_3" 0  )
)
 if( coarse>=40
then
   desVar(      "cthrm8_4" 1.2        )
else
   desVar(      "cthrm8_4" 0  )
)
if( coarse>=48
then
   desVar(      "cthrm8_5" 1.2        )
else
   desVar(      "cthrm8_5" 0  )
)
if( coarse>=56
then
   desVar(      "cthrm8_6" 1.2        )
else
   desVar(      "cthrm8_6" 0  )
)



option(       'reltol  "1e-7" )
```

```

  ; saveOption( ?saveahdlvars "all" )
  saveOption( ?outputParamInfo nil )
  saveOption( ?elementInfo nil )
  saveOption( ?modelParamInfo nil )
  saveOption( 'save "selected" )
  ; save( 'v "/out0" "/out90" "/out180" "/out270" )
  save( 'v "/n075" "/n077" "/n45" "/n043" )
  temp( tempval )

  run()
); end run_VCO_analysis

;
; Calculate frequency-tuning characteristic of array.

procedure( np_tuningCharacteristic( coarseList fineList tempList cornerList )
  prog( (
         label xlist ylistOsc yindex ylistPN
         tempval corner
         windowID windowIsupID
         fosc1 pNoise1M
         integer numrun
        )

    xlist = nil
    ylistOsc =nil
    ;ylistPN=nil
    numrun = 0

    yindex = nil
    windowID =0

     foreach( corner cornerList
     foreach( tempval tempList
     foreach( coarse coarseList

       ycurveOsc = nil
       ;ycurvePN = nil

       ; create graphics label
       ;
       sprintf(label "tune_frank4 temp:%d, " tempval )
       if( corner==0 label = strcat( label "snsp corner" ) )
       if( corner==1 label = strcat( label "nom corner" ) )
       if( corner==2 label = strcat( label "fnfp corner" ) )

       yindex = cons(label yindex)


       ; change tune fine

       foreach( fine fineList

         printf("\n\nRunning simulation:\n")
         printf("Coarse: %f\n",float(coarse))
         println(label)
```

```

          run_VCO_analysis( coarse fine tempval corner )

          fosc1  = harmonic(xval(getData("/n075" ?result "pss_fd")) '1)
          ;pNoise10K  = value(phaseNoise(1 "pss_fd" ?result "pnoise") 10K)

          ;keep track of the number of simulations run (in case of a crash):
          filePort = outfile("./DCOcheck_frank4.tbl")
          numrun = numrun + 1
          fprintf( filePort "run %d\n" numrun)
          close(filePort)

          ycurveOsc = cons(fosc1 ycurveOsc)
          ;ycurvePN = cons(pNoise10K ycurvePN)

       ) ;endfor

       xlist =  reverse( fineList )

       ylistOsc = cons( ycurveOsc ylistOsc)
       ;ylistPN = cons( ycurvePN ylistPN)

       ; return( ylistOsc xlist yindex )

       if( windowID == 0
       then
          windowID = awvCreatePlotWindow()
          ;windowIsupID = awvAddSubwindow( windowID )
       else
          awvDeleteAllWaveforms( windowID )
       )

       awvPlotList(windowID ylistOsc xlist ?expr yindex ?subwindow 1)
       ;awvPlotList(windowID ylistPN xlist ?expr yindex ?subwindow windowIsupID)
       ;ocnPrint( ?output "./DCOcheck_frank4.txt" xlist)
  ) ; endfor
  ) ; endfor
  ) ; endfor

  printf( "Write output files...\n" )
  ;ocnPrint( ?output "./DCOdata_frank4.txt" ylistOsc ylistPN)
  ocnPrint( ?output "./DCOdata_frank4.txt" ylistOsc)

  ) ;endlet
)
```

Appendix F

Coarse Tuning Script Colpitts QDCO

```
;%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
;%%%              Simulation of QDCO tuning curves                %%%
;%%%                    Frank Leong, May 2007                     %%%
;%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
; np_tuningCharacteristic( list(0 4 8 31 63) list( 0) list( 27 ) list( 1 ) )
; np_tuningCharacteristic( list(0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63) list( 0) list( 27 ) list( 1 ) )
; load( "./tune_frank5.ocn")


procedure( run_VCO_analysis( coarse fine tempval corner )

simulator( 'spectre )

design( "/home/nlv15336/paulg/simulation/pss_tune_colpitts2/spectre/schematic/netlist/netlist")
resultsDir( "/home/nlv15336/paulg/simulation/pss_tune_colpitts2/spectre/schematic/psf" )


  if( corner==0
  then
    modelFile( '("/home/nlv15336/Workareas4/UTC065_nlv15336/b6Ra1/include_snsp.scs" "" ) )
  )

  if( corner==1
  then
    modelFile( '("/home/nlv15336/Workareas4/UTC065_nlv15336/b6Ra1/include_nominal.scs" "" ) )
  )

  if( corner==2
  then
    modelFile( '("/home/nlv15336/Workareas4/UTC065_nlv15336/b6Ra1/include_fpfn.scs" "" ) )
  )

  ;analysis('pnoise ?relharmnum "1"  ?start "1e3"  ?stop "1e9"
  ;              ?maxsideband "5"  ?p "/n075"  ?n "/gnd!"  ?oprobe ""
  ;              ?iprobe ""  ?refsideband ""  )
  analysis('pss ?fund "8G"  ?harms "5"  ?errpreset "conservative"
                ?tstab "5n"  ?saveinit "no"  ?p "/n075"  ?n "/gnd!"
                ?maxstep "1p"  ?method "gear2only"  ?tstabmethod "gear2only"  )
  desVar(         "clsim5" 3.5371p      )
  desVar(         "clsim1" 37.2286f     )
  desVar(         "clsim2" 300.679f     )
  desVar(         "clsim3" -10.0821f    )
  desVar(         "clsim4" 5.51919f     )
  desVar(         "llsim4" 80.2779p     )
  desVar(         "llsim5" -129.703p    )
  desVar(         "llsim2" 7.16401p     )
  desVar(         "llsim6" -0.495176p   )
  desVar(         "llsim8" -5.54881p    )
  desVar(         "llsim3" 18.1179p     )
  desVar(         "llsim1" 430.961p     )
  desVar(         "llsim7" -1.25231p    )
  desVar(         "rlsim2" 2.98229      )
  desVar(         "rlsim4" 1.69803      )
  desVar(         "rlsim1" 6.37948      )
  desVar(         "rlsim3" 1.51149      )
  desVar(         "rlsim5" 1.56008      )
  desVar(         "rlsim6" -0.415667    )
  desVar(         "rlsim8" 0.483        )
  desVar(         "rlsim9" 707.547      )
  desVar(         "rlsim7" 1.955        )
  ;desVar(        "fine" fine   )
  ;desVar(        "coarse" coarse       )

  if( mod(fine 4)==0
  then
    desVar(       "thrm1_0" 0   )
    desVar(       "thrm1_1" 0   )
    desVar(       "thrm1_2" 0   )
  )
  if( mod(fine 4)==1
  then
    desVar(       "thrm1_0" 1.2 )
    desVar(       "thrm1_1" 0   )
    desVar(       "thrm1_2" 0   )
  )
   if( mod(fine 4)==2
  then
    desVar(       "thrm1_0" 1.2 )
    desVar(       "thrm1_1" 1.2 )
    desVar(       "thrm1_2" 0   )
  )
   if( mod(fine 4)==3
  then
    desVar(       "thrm1_0" 1.2 )
    desVar(       "thrm1_1" 1.2 )
    desVar(       "thrm1_2" 1.2 )
  )
  if( mod(fine 8)>=4
  then
     desVar(      "thrm4" 1.2    )
  else
     desVar(      "thrm4" 0      )
  )
  if( fine>=8
  then
     desVar(      "thrm8_0" 1.2 )
  else
```

```
   desVar(      "thrm8_0" 0   )
)
if( fine>=16
then
   desVar(      "thrm8_1" 1.2 )
else
   desVar(      "thrm8_1" 0   )
)
 if( fine>=24
then
   desVar(      "thrm8_2" 1.2 )
else
   desVar(      "thrm8_2" 0   )
)
if( fine>=36
then
   desVar(      "thrm8_3" 1.2 )
else
   desVar(      "thrm8_3" 0   )
)
 if( fine>=40
then
   desVar(      "thrm8_4" 1.2 )
else
   desVar(      "thrm8_4" 0   )
)
if( fine>=48
then
   desVar(      "thrm8_5" 1.2 )
else
   desVar(      "thrm8_5" 0   )
)
if( fine>=56
then
   desVar(      "thrm8_6" 1.2 )
else
   desVar(      "thrm8_6" 0   )
)


if( mod(coarse 4)==0
then
  desVar(       "cthrm1_0" 0  )
  desVar(       "cthrm1_1" 0  )
  desVar(       "cthrm1_2" 0  )
)
if( mod(coarse 4)==1
then
  desVar(       "cthrm1_0" 1.2        )
  desVar(       "cthrm1_1" 0  )
  desVar(       "cthrm1_2" 0  )
)
 if( mod(coarse 4)==2
then
  desVar(       "cthrm1_0" 1.2        )
  desVar(       "cthrm1_1" 1.2        )
  desVar(       "cthrm1_2" 0  )
)
```

```
 if( mod(coarse 4)==3
then
  desVar(       "cthrm1_0" 1.2        )
  desVar(       "cthrm1_1" 1.2        )
  desVar(       "cthrm1_2" 1.2        )
)
if( mod(coarse 8)>=4
then
   desVar(      "cthrm4" 1.2  )
else
   desVar(      "cthrm4" 0    )
)
if( coarse>=8
then
   desVar(      "cthrm8_0" 1.2        )
else
   desVar(      "cthrm8_0" 0  )
)
if( coarse>=16
then
   desVar(      "cthrm8_1" 1.2        )
else
   desVar(      "cthrm8_1" 0  )
)
 if( coarse>=24
then
   desVar(      "cthrm8_2" 1.2        )
else
   desVar(      "cthrm8_2" 0  )
)
if( coarse>=36
then
   desVar(      "cthrm8_3" 1.2        )
else
   desVar(      "cthrm8_3" 0  )
)
 if( coarse>=40
then
   desVar(      "cthrm8_4" 1.2        )
else
   desVar(      "cthrm8_4" 0  )
)
if( coarse>=48
then
   desVar(      "cthrm8_5" 1.2        )
else
   desVar(      "cthrm8_5" 0  )
)
if( coarse>=56
then
   desVar(      "cthrm8_6" 1.2        )
else
   desVar(      "cthrm8_6" 0  )
)



option(       'reltol  "1e-7" )
```

```

  ; saveOption( ?saveahdlvars "all" )
  saveOption( ?outputParamInfo nil )
  saveOption( ?elementInfo nil )
  saveOption( ?modelParamInfo nil )
  saveOption( 'save "selected" )
  ; save( 'v "/out0" "/out90" "/out180" "/out270" )
  save( 'v "/n075" "/n077" "/n45" "/n043" )
  temp( tempval )

  run()
); end run_VCO_analysis

;
; Calculate frequency-tuning characteristic of array.

procedure( np_tuningCharacteristic( coarseList fineList tempList cornerList )
  prog( (
         label xlist ylistOsc yindex ylistPN
         tempval corner
         windowID windowIsupID
         fosc1 pNoise1M
         integer numrun
        )

    xlist = nil
    ylistOsc =nil
    ;ylistPN=nil
    numrun = 0

    yindex = nil
    windowID =0

     foreach( corner cornerList
     foreach( tempval tempList
     foreach( fine fineList

       ycurveOsc = nil
       ;ycurvePN = nil

       ; create graphics label
       ;
       sprintf(label "tune_frank5 temp:%d, " tempval )
       if( corner==0 label = strcat( label "snsp corner" ) )
       if( corner==1 label = strcat( label "nom corner" ) )
       if( corner==2 label = strcat( label "fnfp corner" ) )

       yindex = cons(label yindex)


       ; change tune coarse

       foreach( coarse coarseList

         printf("\n\nRunning simulation:\n")
         printf("Fine: %f\n",float(fine))
         println(label)
```

```

          run_VCO_analysis( coarse fine tempval corner )

          fosc1  = harmonic(xval(getData("/n075" ?result "pss_fd")) '1)
          ;pNoise10K  = value(phaseNoise(1 "pss_fd" ?result "pnoise") 10K)

          ;keep track of the number of simulations run (in case of a crash):
          filePort = outfile("./DCOcheck_frank5.tbl")
          numrun = numrun + 1
          fprintf( filePort "run %d\n" numrun)
          close(filePort)

          ycurveOsc = cons(fosc1 ycurveOsc)
          ;ycurvePN = cons(pNoise10K ycurvePN)

       ) ;endfor

       xlist =  reverse( coarseList )

       ylistOsc = cons( ycurveOsc ylistOsc)
       ;ylistPN = cons( ycurvePN ylistPN)

       ; return( ylistOsc xlist yindex )

       if( windowID == 0
       then
          windowID = awvCreatePlotWindow()
          ;windowIsupID = awvAddSubwindow( windowID )
       else
          awvDeleteAllWaveforms( windowID )
       )

       awvPlotList(windowID ylistOsc xlist ?expr yindex ?subwindow 1)
       ;awvPlotList(windowID ylistPN xlist ?expr yindex ?subwindow windowIsupID)
       ;ocnPrint( ?output "./DCOcheck_frank5.txt" xlist)
  ) ; endfor
  ) ; endfor
  ) ; endfor

  printf( "Write output files...\n" )
  ;ocnPrint( ?output "./DCOdata_frank5.txt" ylistOsc ylistPN)
  ocnPrint( ?output "./DCOdata_frank5.txt" ylistOsc)

  ) ;endlet
)
```