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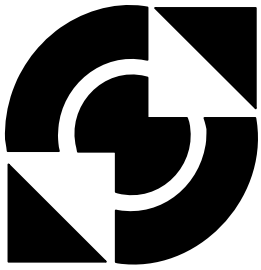

A low-power second-order sampling receiver for Bluetooth

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Abstract

The main goal of this thesis is to investigate the feasibility of a quadrature radio frequency receiver front-end using a second-order sampling topology in CMOS. Second-order sampling combines subsampling with a non-uniform sampling scheme. This non-uniform sampling scheme comprises of two uniform sampling streams with a small time delay between both streams, which allows the generation of an I and Q channel. The second goal is to determine the performance limiting mechanisms in the analog domain. The knowledge of the performance limiting mechanisms is used to implement the critical parts of a low power Bluetooth receiver in CMOS and determine the final performance of such a front-end. It is hoped that new receiver architectures offer new wireless applications, outperform traditional receivers in existing applications or offer additional features.

The performance limiting mechanisms are derived to be noise folding, clock jitter and quantisation noise. The main limiting effect is the quantisation noise, while the ADC is estimated to consume the most power. However, based on Matlab and Cadence simulations, second-order sampling turns out to be suitable for a RF receiver. A receiver with a subsampling ratio of 12 for each channel meets the requirements of the Bluetooth standard and gives the best overall performance. The implemented receiver has an IIP_3 of -12.7, noise figure $<$ 10 dB and a power consumption of 18.4 mW excluding ADC.

Preface

The master graduation project is the last project of the study electrical engineering, allowing all the knowledge attained during the study to be used. It is also the longest project during the study, which makes it altogether quite a task to finish successfully.

For someone who has never experienced this, it might be best described with an analogy to cave exploration. It start by selecting a subject/cave, which after some exploration turns out to be quite different than what you expected. Fortunately, a committee is there to guide you through the cave and give advice which path to take. However, this path often has numerous surprises to the unexperienced cave explorer. The knowledge from the study provides a lot of different tools, some of which suddenly become far more useful than previously expected. When the end of the cave is finally reached, one realises that there is still much to discover in the cave and that the chosen path was perhaps not the fastest one. However, it was definitely a worthwhile experience!

The author would like to thank my supervisors Ed, Eric and Zhiyu for their guidance and interesting discussions about the subject. I would also like to thanks my parents and brother, friends and house-mates for their support and encouragement throughout my master project.

Anne Stellinga, November 2007

Contents

Chapter 1

Introduction

This report describes the work I have done for my graduation project and the results that follow from this work. This project is the conclusion of the five year electrical engineering study. I have done this project at the integrated circuit design group of the University of Twente.

Nowadays many wireless standards exist for different applications. While these standards all use a different part of the radio frequency spectrum, the receiver implementation method into integrated circuits is quite similar. First, an analog frontend amplifies the signal from the antenna, selects a channel and converts this channel to the digital domain. In the digital domain the information is retrieved using the demodulation scheme specified by the standard. To downconvert the signal from high frequencies to baseband frequencies, mixers are used.

A trend in analog integrated circuit design is to move the analog to digital converter(ADC) closer to the antenna, which finally results in digital channel selection. However, digitizing signals in the GHz range is not possible with a conventional ADC, using the Nyquist criterium. The Nyquist criterium can be circumvented when certain conditions are met, using bandpass sampling to digitize the required frequency band with a sampling frequency that is at least two times the bandwidth.

Wireless receiver system often use I/Q modulation, which allows additional modulation options, image rejection and synchronisation. This can be realized with a 90 degree phaseshift during downconversion with mixers. These two channels(inphase and quadrature) are then digitized and digital signal processing is used to demodulate the signals, perform image rejection or solve a synchronisation problem. However, this 90 degree phaseshift can also be realised using a non-uniform sampling scheme with two sampling streams, where a small time delay is present between the first and second sampling stream. This is called second-order sampling.

1.1 Project goals and motivation

The goal of this project is to investigate the feasibility of a quadrature radio frequency receiver front-end using a second-order sampling topology and to determine the performance limiting

mechanisms in the analog domain. The knowledge of the performance limiting mechanisms is used to implement the critical parts of a low-power Bluetooth receiver in CMOS and determine the final performance of such a front-end.

The implementation of the digital signal processing is not investigated in this thesis, the first reason being the time allowed for this master thesis and secondly because the analog front-end is the bottleneck in the feasibility, not the digital part. However, some performance figures of the analog front-end can only be determined in the digital domain, so this is investigated.

The motivation to research such an architecture is to find alternatives for the traditional receiver architectures that exist today. These alternatives might offer new wireless applications, outperform traditional receivers in existing applications or offer additional features.

1.2 Thesis organization

In chapter 2 the concepts of second-order sampling, bandpass sampling and its application in a radio receiver is presented. Chapter 3 goes into a system level approach that is used to determine the implementation using general blocks such as amplifiers, filters and analog to digital converters. Furthermore, the testcase will be presented and specifications for the blocks are derived. The approach used to verify feasibility and performance, which requires a mathematical representation of the error sources, is discussed in chapter 4. Chapter 5 will go into the transistor level design of the blocks necessary for the experiments defined in chapter 4. These designs are simulated and the final specifications are determined in chapter 6. The simulation results of the experiments are also presented in chapter 6. Finally, the conclusions about the feasibility and the performance of this implementation are made in chapter 7.

Chapter 2

Introduction to second-order sampling

2.1 Introduction

In this chapter, the process of sampling is investigated using existing literature and is described mathematically. It starts with the general theory of sampling. After this short introduction some more advanced forms of sampling are introduced and the mathematical representation is given. Bandpass sampling is investigated first in section 2.2.2. After this, non-uniform sampling is described in section 2.2.3. Second-order sampling is the last form of sampling to be covered in section 2.2.4. Section 2.3 explains how sampling can be used to downconvert signals for radio transceiver applications. Finally, a quadrature receiver implementation using sampling is proposed in section 2.4. The goal for this chapter is to introduce the reader with the theoretical background required to investigate the feasibility of a second-order sampling receiver.

2.2 Sampling

2.2.1 Introduction

The Shannon sampling theorem is a well known theorem stating that the sampling frequency should be at least two times the highest frequency component to be able to completely reconstruct the original signal from it. Sampling introduces images(copies) of the original band. These image-bands can overlap with the original band if the sampling frequency is lower than two times the bandwidth of the input signal. The error caused by the overlap is then called aliasing. This is why a lowpass anti-aliasing filter is often added before an ADC[1], to attenuate high frequency signals that would cause aliasing. This form of sampling where the sampling frequency needs to be at least two times the highest frequency component of the input signal shall be referred to as *regular sampling* in this thesis. In the time domain, the process of sampling can be mathematically described[1] as a multiplication of an input signal x(t) with a pulse train P(t) which has a period of T, where the sampled signal is $x_s(t)$:

[1] when ADC is mentioned, it is referring to the combination of a sampler and Analog to digital converter

$$x_s(t) = x(t) \cdot p(t) \tag{2.1}$$

where

$$p(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) \tag{2.2}$$

In the frequency domain the pulse train can be written as:

$$P(\omega) = \frac{2\pi}{T} \sum_{n=-\infty}^{\infty} \delta(\omega - \frac{2\pi n}{T}) = \frac{2\pi}{T} \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_s) \tag{2.3}$$

A multiplication in the time domain is equivalent to a convolution(described mathematically as $*$) in the frequency domain. When equation 2.1 is Fourier transformed, the sampling operation in the frequency domain can be obtained:

$$\begin{aligned} X_s(\omega) &= \frac{1}{2\pi} X(\omega) * P(\omega) \\ &= \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\sigma) P(\omega - \sigma) d\sigma \\ &= \frac{1}{T} \sum_{n=-\infty}^{\infty} X(\omega - n\omega_s) \end{aligned} \tag{2.4}$$

To recover our original signal from the sampled signal, an ideal lowpass filter can be applied, which is mathematically[1]:

$$H(\omega) = \begin{cases} T, & |\,\omega| < \omega_b \\ 0, & \text{otherwise} \end{cases} \tag{2.5}$$

with

$$\omega_b <= \frac{\pi}{T} \tag{2.6}$$

But when the original signal had frequency components larger than ω_b, then after sampling, the closest image band overlaps with the original band. This results in an incorrect representation in the digital domain. Figure 2.1 illustrates a matlab simulation of a sampling process using a sampling frequency of 16 MHz to sample a 1 MHz sine wave. The frequency domain representation has been calculated using a 128 point FFT.

2.2.2 Bandpass sampling

Bandpass sampling, which is a specific type of subsampling, is possible when the wanted band is the only band in the spectrum. If this condition is not met, aliasing can occur, which makes reconstruction impossible. The process of bandpass sampling can be described mathematically exactly the same way as regular sampling(using equations 2.1 through 2.5). However, there are some additional demands for bandpass sampling[2]:

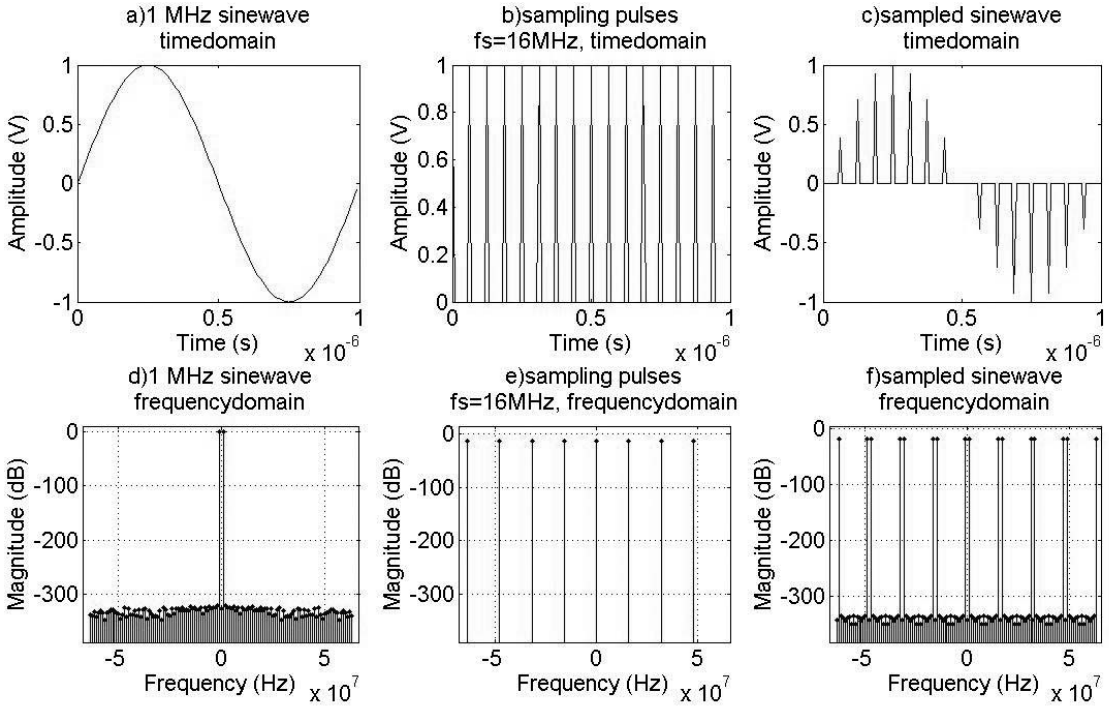


Figure 2.1: regular sampling

1. The input spectrum has to have a bandpass filtered spectrum, to prevent aliasing
2. The sampling frequency has to be at least 2 times the bandwidth(B) of the input signal
3. The sampling frequency has to be chosen in such a way that it does not alias with itself

The third item is the result of the replica's of the band with a periodicity of the sample frequency resulting from the sampling operation. If the sampling frequency is chosen wrong it is possible that these bands will overlap. This aliasing is unwanted, because the original signal cannot be fully reconstructed if aliasing occurs with a single sampler.

In figure 2.2 the results of a matlab simulation using bandpass sampling is displayed. The input signal has an input frequency of 17 MHz, while the sampling frequency is 16 MHz. The frequency band from 16 to 24 MHz is copied to baseband. The result after the convolution operation is exactly the same as with regular sampling. Instead of using a lowpass filter as an anti-aliasing filter, a bandpass filter can be used. However, a steep bandpass filter is often difficult to realize on chip, which is one of the reasons that makes bandpass sampling a less attractive option for applications. The reconstruction can be done with an ideal bandpass filter at the original frequency band location.

2.2.3 Non-uniform sampling

Another method of sampling is non-uniform sampling, where the non-uniform property is in the moment of sampling. The time interval between every two adjacent samples for regular

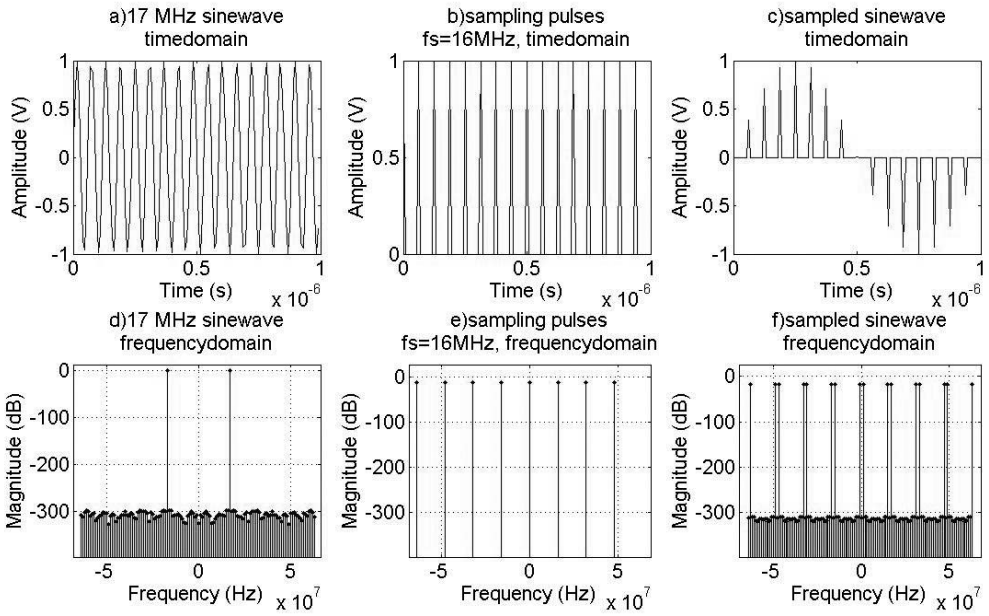


Figure 2.2: Bandpass sampling

sampling should be the same, i.e. the uniform sampling period. However, for non-uniform sampling, the time interval between adjacent sampling moments can differ. There are thus many forms of non-uniform sampling, but in this thesis, the focus is on periodic non-uniform sampling. Periodic non-uniform sampling uses multiple sampling streams with equal sampling frequency, but with a delay between streams. This delay is denoted in equations 2.7 with d_1 through d_{m-1}, where m refers to the stream number.

$$\begin{aligned} p_1(t) &= \sum_{n=-\infty}^{\infty} \delta(t - nT) \\ p_2(t) &= \sum_{n=-\infty}^{\infty} \delta(t - nT - d_1) \\ &\vdots \\ p_m(t) &= \sum_{n=-\infty}^{\infty} \delta(t - nT - d_{m-1}) \end{aligned} \tag{2.7}$$

In the next section, periodic non-uniform sampling with two streams is investigated. Due to the two streams, it is also referred to as second-order sampling.

2.2.4 Second-order sampling

Second-order sampling can be used instead of regular sampling or bandpass sampling. When using second-order sampling, an extra degree of freedom compared to the other cases is

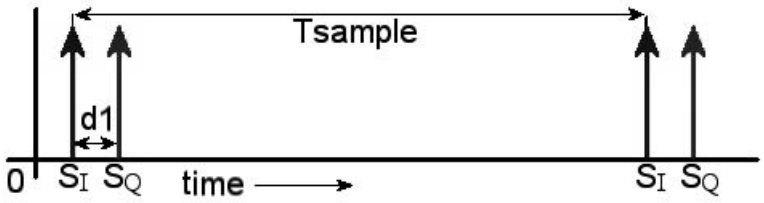


Figure 2.3: Timing diagram second-order sampling

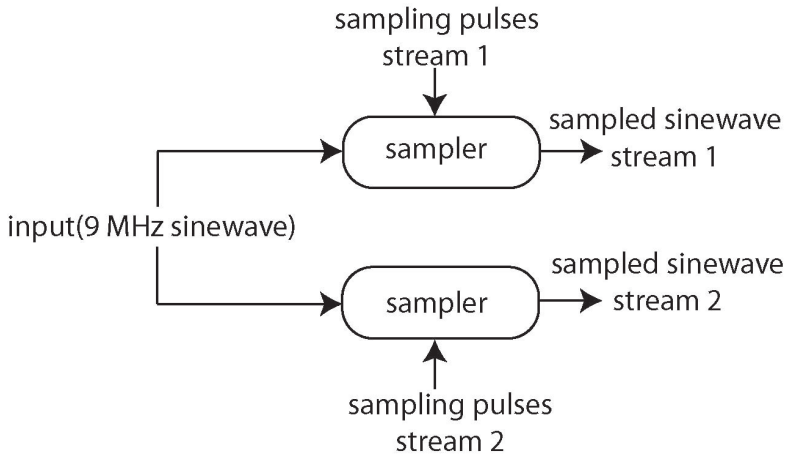


Figure 2.4: representation Matlab setup second-order sampling

available, which is the delay(d_1) between the two streams(figure 2.3). Depending on the application, this might offer an advantage in the implementation. With bandpass sampling, the position of the band of the wanted signal made it necessary to chose the sampling frequency in such a way that it did not alias with itself. This aliasing occurs when the replica's of the band generated by the sampling operation overlap, due to a poor choice of the sampling frequency. However, as proven by Kohlenberg[3], for second-order sampling, reconstruction is possible for any band position.

To illustrate the process of second-order sampling, a Matlab simulation for second-order sampling is performed, where the results are presented in figure 2.5. The used architecture is shown in figure 2.4. Two pulse streams are used, with a delay of 23.4 ns between them. The input frequency is chosen to be 9 MHz. The phase difference between the sampled data for an input frequency of 9 MHz is clearly visible. The first stream can be recognized as a sine(figure 2.5d)), while the second stream can be represented with a cosine(figure 2.5e)). This phase difference is because 23.4 ns gives around 60 degrees phaseshift for 9 MHz(90 degrees phaseshift would be ideal for image rejection, but the graphical explanation is clearer with this phaseshift choice). The frequency domain representation needs some further explanation. Because the magnitude response of the pulse streams and sampled sinewave give the same result, the phase response is also added. When the discrete Fourier transform(DFT) is performed in Matlab on a sinewave where the frequency is chosen such that there is no spectral leakage, the phase of that frequency bin is determined. However, because there is no spectral content

in the other frequency bins, the phase is determined by the limited accuracy of Matlab. To get some spectral content in these frequency bins, the phase response is calculated using a white gaussian noise source, because the phase is defined for all the frequencies. This phase distribution is then chosen as the reference, which explains the zero phase in figure 2.5g). Figure 2.5i) shows the resulting phaseshift due to the timedelay between sampling pulses stream channel 1 and 2. Unfortunately, due to limited accuracy of Matlab, the gaussian noise source still give some errors for the phase response shown in figure 2.5k), but the trend(a diagonal line from 180 to -180 degrees, which is repeated) can be recognized. This can be expected, because a time delay gives a different phase shift for each frequency. By choosing the time delay correctly, a 90 degree phaseshift can be realized for a certain frequency. This phaseshift can be used in the reconstruction of the signal.

With a single sampled stream it is quite straightforward to reconstruct the signal. But how can the original signal be reconstructed from these two streams? Kohlenberg[3] derived a reconstruction methodology and also determined the conditions that have to be met for this reconstruction to work. The reconstruction can be performed using two transfer functions(S_1 for the first stream and S_2 for the second stream), that represent ideal bandpass filters for the wanted frequency bands($[-f_u, -f_l], [f_l, f_u]$). f_u and f_l represent the frequencies at the edge of the band. S_1 and S_2 also perform an equal but opposite phase shift. Furthermore, $S_1(\omega)$=$S_2(-\omega)$. Although these transfer functions are not physically realizable(because they are non-causal), they can be well approximated, just as the reconstruction algorithm for regular sampling.

2.3 Frequency downconversion

2.3.1 Introduction

After discussing different forms of sampling, the focus will shift a bit more towards radio frequency receivers. At the antenna of the receiver a signal is present with bandwidth B at a center frequency of f_c. In a regular receiver a mixer can shift the frequency band to a much lower frequency. This downconversion greatly relaxes the requirements for the AD converter, which converts the signal to the digital domain. However, for some applications, AD converter sampling speeds have improved to a level where it is possible to remove the mixer and perform the downconversion via the sampling process. This offers the possibility to use a single receiver design to receive multiple radio standards, where the choice of the radio standard is programmable with the digital signal processing. Such a feature is often referred to as software defined radio. Downconversion using Nyquist sampling is covered in section 2.3.2. Another possibility is to use bandpass sampling for downconversion. Such a setup is discussed in section 2.3.3. However, to get more functionality compared to bandpass sampling, the second-order sampling topology is discussed in section 2.3.4.

2.3.2 Downconversion with Nyquist sampling

The principle in downconversion with Nyquist sampling is quite straightforward. The entire frequency band from 0 to $\frac{f_s}{2}$ is converted to the digital domain, where $f_c < \frac{f_s}{2}$ and $f_s \gg BW_{channel}$(channel bandwidth). With digital signal processing the wanted channel can be

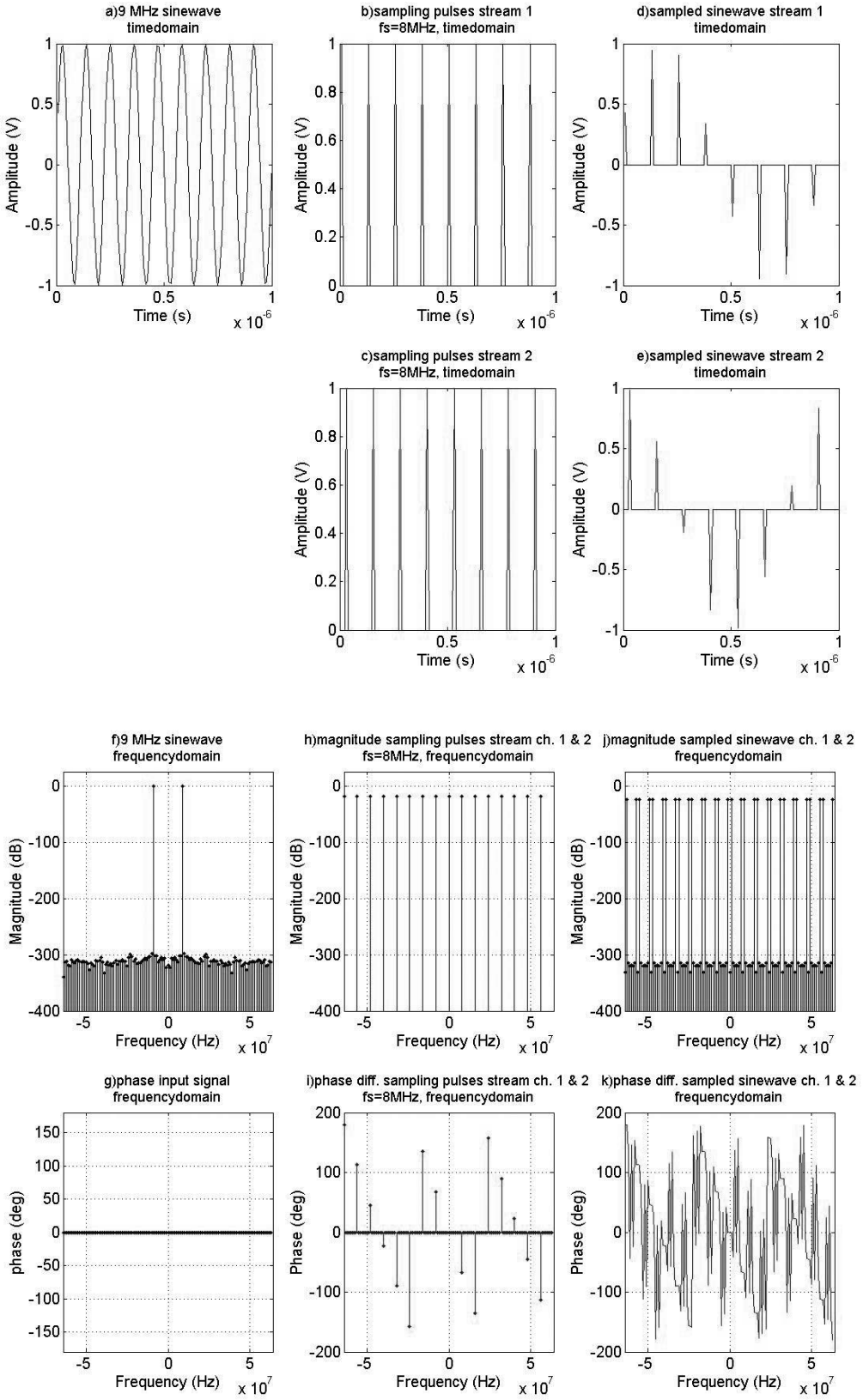


Figure 2.5: Periodic non-uniform sampling using two sampling streams, sampling frequency 8 MHz, delay=23.4 ns

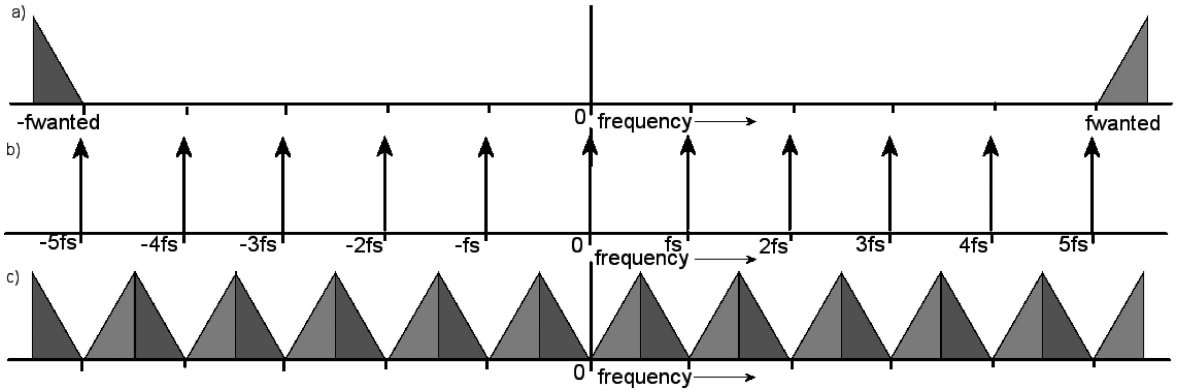


Figure 2.6: spectrum in bandpass sampling receiver showing a)input of ADC b)clock c)output of ADC

selected and demodulated digitally. However, there are quite some disadvantages to such an approach. First the power consumption of the AD converters that meet these specifications is usually quite high. Secondly a large dynamic range for the AD converter is required, because the wanted signal can be weak while interferers can be strong. The strong interferers limit the maximum gain, while the weak signals usually require multiple bits to recover the signal digitally. Finally, due to the huge amounts of samples, the digital signal processing is very computation intensive. This will again result in a high power consumption.

2.3.3 Downconversion with bandpass sampling

Downconversion with bandpass sampling results in an output spectrum consisting of copies of the original band from the positive and negative frequencies side. Copies of the original band from the positive frequency side before sampling that end up at the negative side after sampling(and vice versa), will be called image bands. For bandpass sampling, the AD converters specifications are more relaxed compared to nyquist sampling, because the sampling speed requirement of two times the bandwidth can be sufficient. This sampling speed requirement is to prevent any aliasing caused by the image bands. Because of the relaxed ADC specifications, this topology can be implemented using less power compared to regular Nyquist sampling. No mixer is needed and the amount of samples is relatively small. However, it is not straightforward to get an inphase(I) and quadrature(Q) channel, which is often used in modulation schemes nowadays. Another disadvantage is that the required bandpass filter can limit the the flexibility of the receiver. The sampling process is illustrated in figure 2.6. The input signal of the ADC(figure 2.6a)) is sampled at specific moments, illustrated using the frequency response of the clock(2.6b)). Because the signal is discrete time sampled at the output of the ADC(figure 2.6c)), the spectrum between $-\frac{1}{2f_s}$ and $\frac{1}{2f_s}$ is repeated.

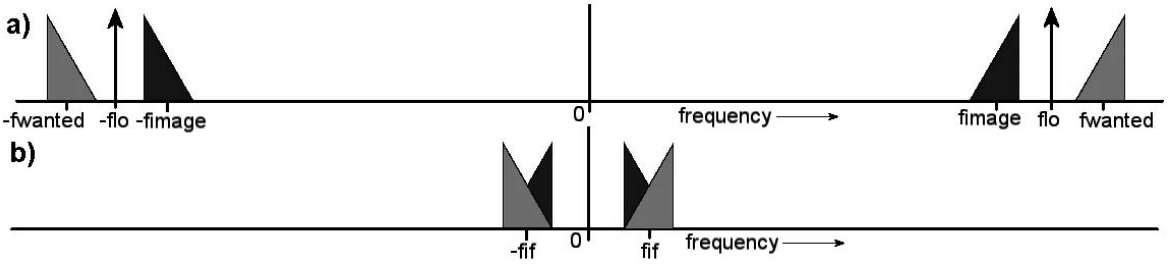


Figure 2.7: spectrum in heterodyne receiver showing a)input of mixer b)output of mixer

2.3.4 Downconversion with second-order sampling

Second-order sampling gives the designer an extra degree of freedom, which is the delay between the two sampling streams. For radio receivers this delay can be used to implement an I and Q channel, as will be discussed in section 2.4.2. The ADC specifications are similar to the bandpass sampling topology, while the I and Q channel allow for more functionality. Another advantage is that the bandposition does not impose extra conditions on the sampling frequency.

2.4 Quadrature receiver

2.4.1 Introduction

An inherent difficulty in the downconversion of radio frequency signals to baseband is the existence of one or more image bands. First the case when receivers are using mixers is considered. Mixers are used to multiply the received RF signal with a frequency(f_{LO}) that positions the band of interest to the wanted intermediate frequency(f_{IF}). However, for heterodyne receivers, there is always an image band that is mixed to the same intermediate frequency as the wanted band. This is illustrated in figure 2.7. For homodyne receivers, the f_{IF} is chosen to be zero, which moves the wanted frequency band directly to DC. Although no image band is mixed with wanted band, the left half of the frequency band is mixed with the right half of the frequency band. This effect is shown in figure 2.8. Image rejection using an I and Q channel can be used to solve these image problems for mixers. Second order sampling also has to deal with image bands present in both sampling streams. In the following section, it will be shown that for a special case of second-order sampling, the I and Q channel can also be created and similar to the mixer topologies, the image bands can be rejected.

2.4.2 Image rejection

To resolve the problems of image band(s), a form of image rejection is necessary. Heterodyne receivers can use filtering to attenuate the image. However this requires the intermediate frequency to be relatively large to get sufficient attenuation. Another often used mechanism is the use of phases to cancel out the image band while the wanted band remains unaffected. Instead of a single mixer, two mixers are used. The mixers are driven with the same LO

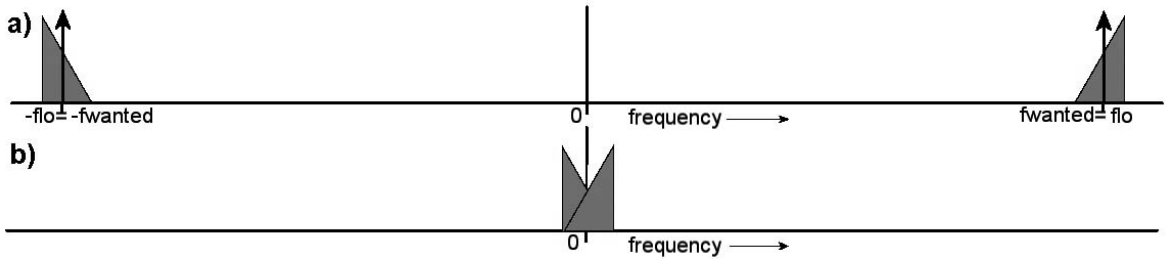


Figure 2.8: spectrum in homodyne showing a)input of mixer b)output of mixer

frequency but with a 90 degree phaseshift between each other. This results in two channels with a 90 degree phaseshift in between often referred to as the inphase(I) and quadrature(Q) channel. When another 90 degree phase shift is performed on the Q channel and after this the I channel is added, the image band is cancelled out. The second 90 degree phaseshift can be performed with additional mixers, an RC network or digital signal processing[9].

In the case of second order sampling, the first 90 degree phaseshift needs to be achieved during the sampling. Then the image rejection can be performed digitally in a similar way as with the mixer setup. But how is second-order sampling implemented in a practical sense? Using two ADC's, a time delay in the clock which controls the sampling moment can be introduced. This is equivalent to a delay in one of the branches before AD conversion. A time delay of d_1 is chosen, where d_1 is

$$d_1 = \frac{1}{4 \cdot f_c} \tag{2.8}$$

This time delay introduces exactly 90 degrees phaseshift for the carrier frequency, which gives us an I and Q channel. However, the 90 degree phaseshift introduced by mixing gives a 90 degree phaseshift for all the frequencies of the input signal. But by introducing a time delay, the phase shift of the other frequencies are now given by equation 2.9, where f is the input frequency.

$$\triangle\Phi = -2\pi f d_1 \tag{2.9}$$

If we assume an ideal analog system, the image rejection is only perfect for the the carrier frequency, while the image rejection for other frequencies are given by[4]

$$L(f_d) = \frac{\left|1 + e^{-j2\pi f d_1}\right|^2}{\left|1 - e^{-j2\pi f d_1}\right|^2} \tag{2.10}$$

where

$$f_d = f - f_c \tag{2.11}$$

However, since the error is systematic, it should be possible to improve the image rejection digitally, e.g. using the implementation proposed by Valkama[4]. Of course, the analog system

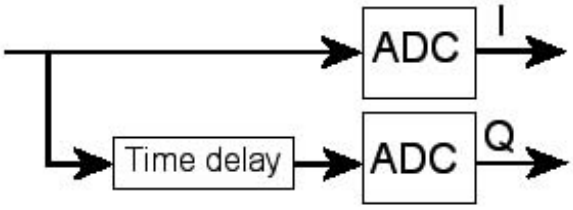


Figure 2.9: second order sampling implementation

will always have non-idealities. For a second-order sampling receiver, there could be phase and amplitude mismatches between the I and Q sampling channels. Although these errors are not systematic and can be quite challenging, we believe solutions can be found to improve this performance. However, this is out of the scope of the thesis, so we will not discuss it further.

2.5 Reconstruction of second-order sampling

2.5.1 Introduction

Second-order sampling uses two sampling streams each of which needs a sampling rate of at least B(where B is the bandwidth of the band-limited input signal). These two streams have an arbitrary delay of d_1 seconds. Combined together these two streams can have a sampling rate of at least 2B which intuitively is sufficient to reconstruct the signal. Kohlenberg[3] has shown that reconstruction of these sample streams to the original signal is indeed possible.

In this section, the focus will be on the reconstruction of second-order sampling from an implementation in hardware point of view. The input signal is band-limited, has a center frequency of f_c and bandwidth B. In section 2.4.2 an implementation for second-order sampling is proposed which uses image-rejection to perform reconstruction. Such an implementation is investigated in more detail. The implementation consists of two ADC's, where the second ADC uses a delayed signal, as illustrated in figure 2.9.

2.5.2 Reconstruction

The reconstruction methodology is described step by step and illustrated graphically in figure 2.10. The input signal is shown in figure 2.10a). When the input signal is sampled by the first ADC, the resulting spectrum is given in figure 2.10d), which is also referred to as the I channel.

The time delay is meant to phase shift the input signal 90 degrees, using equation 2.8. However for every frequency the time delay results in a different phaseshift, where the phaseshift is given by equation 2.9. Fortunately, when the input is narrowband, the phaseshift for the entire band will be approximately 90 degrees. this phaseshift/timedelay is illustrated in figure 2.10c). The output of the second ADC(Q channel) is shown in figure 2.10e).

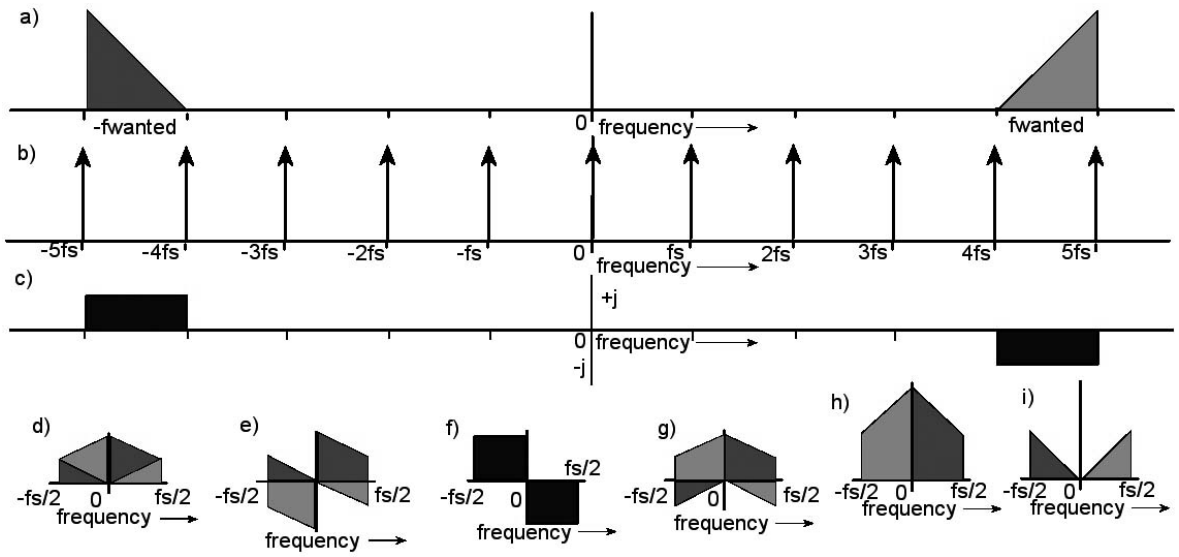


Figure 2.10: spectrum of the reconstruction of second-order sampling showing a)original input bandpass signal b)clock c)timedelay analog domain d)output ADC I channel e)output ADC Q channel f)phaseshift digital domain g)phase shifted Q channel h)addition I channel and phase shifted Q channel i)subtraction I channel and phase shifted Q channel

Because the signals of figure 2.10d) and e) are sampled, the spectrum is actually repeated to infinity. In the digital domain, another 90 degree phase shift is performed to the Q channel(output of the second ADC). This phaseshift is achieved with the Hilbert transform. The resulting phaseshift is illustrated in 2.10f). The resulting spectrum of this operation is shown in figure 2.10g).

One part of the spectrum of the original signal can be reconstructed, when adding together the I channel and the Hilbert transformed Q channel. This is shown in figure 2.10h). The two phase shift operations(one in the analog domain and one in the digital domain) are used to get image rejection. Some bands cancel out, because there is a 180 degrees phase shift between them. Other bands add up, because the total phase shift between them was 0 degrees. Due to the location of the original signal band, it has been mirrored in the process of reconstruction. The other part of the spectrum of the original signal can be reconstructed by subtracting the Hilbert transformed Q channel from the I channel illustrated in figure 2.10i).

2.6 Summary

Nyquist sampling, bandpass sampling and second-order sampling are described in this chapter. These sampling topologies can be used for downconversion in a radio receiver. Finally, a quadrature receiver using second-order sampling is investigated and the image rejection implementation is discussed.

Chapter 3

System level design

3.1 Introduction

In this chapter the system level implementation of a receiver using second-order sampling will be investigated. First the design focus for this receiver is determined. The design choices choices for this implementation are then discussed. An application is chosen that is suitable for a second-order sampling implementation. Finally, the specifications for this application are derived for the top level and each block seperately. The goal for this chapter is to investigate the second-order sampling receiver on a system-level, choose a suitable standard and derive the required block specifications for the receiver.

3.2 Topology

3.2.1 Introduction

The topology to design is a receiver based on the principle of second-order sampling. This means that the ADC performs both the digital conversion and downconversion. But what kind of advantage can such an implementation offer? The noise figure will be worse than a regular receiver, due to the noise folding effect that is discussed in chapter 4. The power consumption of a second-order sampling receiver topology is hard to predict, but could actually turn out better than regular receivers, for a number of reasons. First of all, very little analog signal processing is needed, so this might result in a low power implementation. The second reason is the amount of samples, which is much smaller than with Nyquist sampling, thus lowering the amount of samples that need to be processed digitally. An attempt will be made to save power during the design.

First, the specific blocks for a receiver with second-order sampling are discussed. The filter block can not be implemented in a straightforward way, resulting in a tradeoff. This tradeoff also has influence on the implementation of the amplification of the signal, which is discussed in section 3.2.3. After this the implementation of second-order sampling using a delay is reviewed. The clock generation is chosen to be done off-chip, which is discussed in section 3.2.5. Finally, all these choices result in a toplevel design which is presented.

3.2.2 Anti-aliasing filter

A steep bandpass filter is required to make sure the spectrum has a bandpass character. The filter has two purposes. First, any interferers outside the band are attenuated, which reduces aliasing of the interferers. The second reason is the reduction of out of band noise, which is important to reduce the effect of noise folding. A steep bandpass filter is difficult to realize on-chip, so an off-chip filter would be necessary. A possibility is a Surface Acoustic Wave(SAW) filter or the more recently developed Bulk Acoustic Wave(BAW) filter.

To maximally reduce the noise folding effect, the filter should be placed directly in front of the ADC. One possibility is to amplify the signal on-chip, go off-chip to the filter, and back on-chip to the ADC. However, there are some disadvantages to this approach. First of all, the filter needs to be terminated with a 50 Ω resistor to ensure correct operation, which would require some kind of matching network between the filter and ADC. Another problem occurs when a differential approach is chosen for the ADC, which would require the output of the matching network to be followed by a balun. To make full use of the range of the ADC, another gain stage would be necessary that could also drive the track and holds. In conclusion, a lot of noise, complexity and power consumption is added to the receiver system by going off-chip and trying to solve this.

Another possibility is to put the filter directly after the antenna, which means that all further processing can take place on-chip. This has the disadvantage that every block on-chip adds noise, which directly leads to noise folding. However, this effect can be reduced by using on-chip bandpass filters.

This trade-off is most of all a design choice, where the design focus is on low power. When low power is important, additional 50 Ω matching needs to be avoided, because half of the power is lost for wideband resistive matching. The second observation is that second-order sampling does not require much analog signal processing, which consequently limits the amount of noise that is added during analog signal processing. Finally, a trend in IC design is the wish to integrate everything on one chip. With this in mind, the choice is made to put the anti-aliasing filter directly after the antenna.

3.2.3 Gain stage

Receivers using mixers use multiple frequency shifts and subsequent filtering to select a channel. However, for second-order sampling, limited analog signal processing is required. The signal is amplified as much as possible without the range of the ADC being exceeded. The allowed input voltage range of the ADC will be chosen as large as possible in the design of the ADC. The amplification is required to reduce degredation of the signal to noise ratio(SNR) in subsequent stages. This is especially important due to the noise folding, which increases the noise floor considerably. Due to the choice of putting the steep filter directly after the antenna, a narrowband LNA is necessary. This amplifies the signal in roughly the frequency band of interest and filters outside this band.

Because of the sampling, the gain stage can be turned off when the signal is being held by the track and hold. Depending on the track and hold duty cycle and the delay required by the second-order sampling, some power can be saved here.

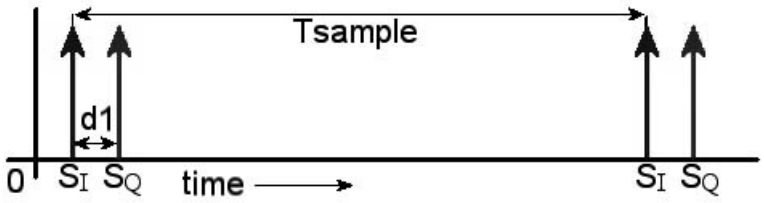


Figure 3.1: Timing diagram second-order sampling

3.2.4 Second-order sampling implementation

To implement second-order sampling, a delay needs to be introduced between the sampling moments of the two ADC's. However the sampling moment has to be well defined, because jitter can degrade the performance in several ways, which is discussed in chapter 4. It is important to realize that this delay can be orders of magnitude smaller than the period of the sampling clocks that will be interleaved(figure 3.1). The delay(d1) is given by equation 2.8 while the period of the sampling clock in relation to the carrier frequency is given by equation 3.1 where s_r is the subsampling ratio.

$$T_{sample} = \frac{s_r}{f_c} \tag{3.1}$$

The implementation of the sampling also offers a tradeoff. First, an implementation using a single track and hold and a single ADC would have to be able to convert the analog sample within the time of the delay to be ready for the next sample. Thus it needs to be orders of magnitudes faster in comparison to an implementation using two ADC's. The advantage of a single ADC would be that there is almost no difference in the transfer function between the I and Q channel, which is beneficial for the image rejection.

Another option would be to use two track and holds and a single ADC. The first track and hold sample is converted immediately, while the second track and hold holds the sample until the first sample is converted. This could be realized with a single ADC which requires a sampling period of half of equation 3.1. However, this could still introduce a difference in transfer function between the I and Q channel, because there will always be a mismatch between the capacitors of the track and holds. Some charge leakage could also cause an amplitude difference because the Q sample is held longer.

Consequently, using two interleaved ADC's and two track and holds seems to be the best choice. The sampling speed is managable and the amplitude difference can be minimized by a robust design.

3.2.5 Clock generation

On-chip clock generation has the disadvantage that a lot of power is required to get the phase noise to an acceptable level. However, when the sampling frequency is low enough(<100MHz), an off-chip crystal clock can be used, which provides a very high quality factor(Q), and thus very little phase noise. However, this resonator still needs to be driven by an on-chip amplifier

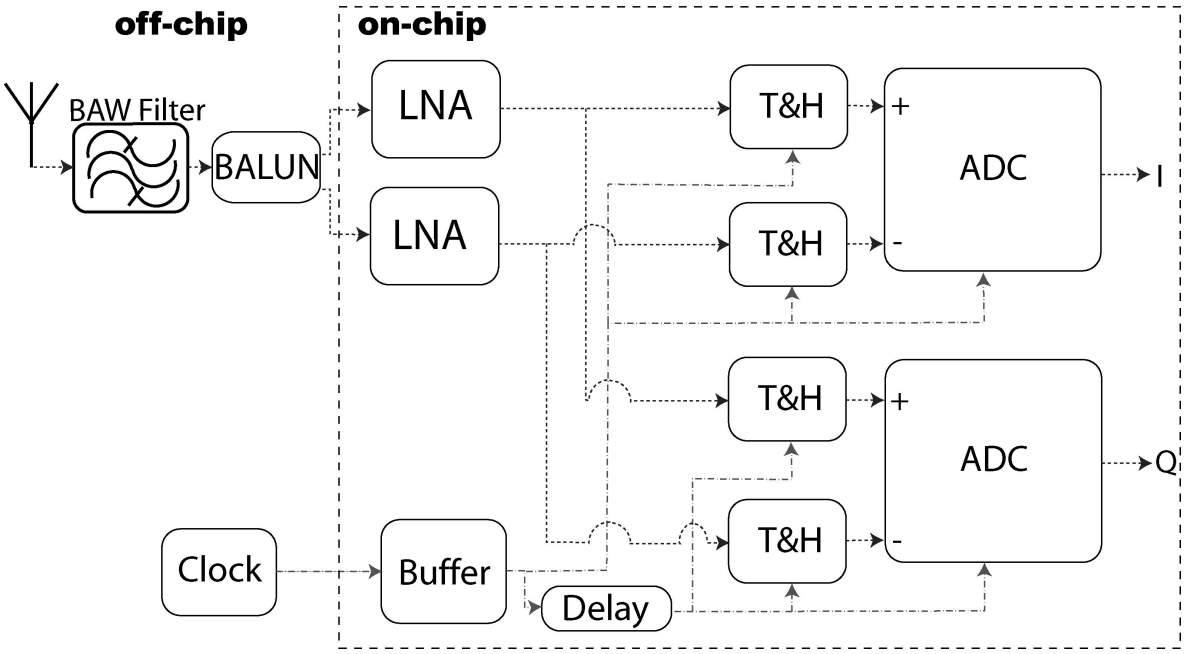


Figure 3.2: System level design second-order sampling receiver

and there will also be some losses due to the resistance of the bondpads that need to be compensated.

3.2.6 Top level design

The receiver based on second-order sampling using the considerations stated earlier, is graphically illustrated in figure 3.2. A further specification is not yet possible without further knowledge of the application. An application is chosen in section 3.3 and the specifications are derived.

3.3 Test case: Bluetooth receiver

3.3.1 Introduction

To verify the feasibility of a low power receiver using second-order sampling, the Bluetooth standard[5] is chosen. This choice is discussed in section 3.3.2. The relevant specifications of the bluetooth standard are summarised in section 3.3.3. The specifications of the receiver, which depend on the Bluetooth standard, are derived in section 3.3.4. Finally the specifications for the each block seperately are derived.

3.3.2 The choice for Bluetooth

Bluetooth is a short range low power radio frequency standard, where the transceiver can be realized at a low cost. Low cost and low power are essential, because it enables Bluetooth to be added to handheld devices. Radio frequency transceivers often use off-chip components(such as capacitors and inductors) to meet the high performance requirements. However, every off-chip component increases the cost substantially. Therefore, the Bluetooth standard has quite relaxed specifications, to minimize the amount of off-chip components, which reduces the cost. Bluetooth operates in the ISM[8] band between 2.4 and 2.5 GHz, which can be used without a license. Also, this ISM band is recognized internationally, thus enabling a Bluetooth transceiver to be used all over the world. The allowed transmission power is limited in these bands, but for a short range protocol this is not a problem. With these characteristics, Bluetooth is quite well suited for our test case. The Bluetooth standard is intended for short range communication, thus allowing a low power implementation. The specifications are quite relaxed, which allows a relatively high noise figure for the receiver.

3.3.3 Bluetooth specifications

The Bluetooth standard is specified for a basic data rate and for an enhanced data rate, where the enhanced data rate has stricter specifications. For this thesis, the basic rate specifications will be used, to keep the design simple. These specifications are simply used as a guideline to see the tradeoffs that are encountered with a second-order sampling receiver. The frequency range used by Bluetooth is from 2.4 GHz to 2.4835 GHz. The first 2 MHz and the last 3.5 MHz are used as guardbands, and the remaining spectrum is used for the 79 channels spaced 1 MHz apart. The first band is centered around 2.402 GHz and the last band is centered around 2.480 GHz. The modulation scheme used is Gaussian Frequency Shift Keying(BT=0.5, modulation index=0.32$\pm$ 1%) which requires 21 dB of signal to noise ratio to demodulate with a bit error rate(BER) of 0.1%[6].

3.3.4 Receiver specifications

Link budget

The link budget is a simplified overview of the gains and losses in the wireless link(figure 3.3). The sensitivity level($P_{rx,min}$) for a Bluetooth receiver is defined by the standard as the input power level for which a raw bit error rate of 0.1% is still met. This should be at least -70dBm, according to the specifications, where the transmitter power(P_{tx}) is 0 dBm and N is the noise floor. This -70 dBm can also be calculated using equations 3.2, 3.3 and 3.4 for the link budget[7].

$$P_{rx} = P_{tx} - L_{path} - L_{fade} \tag{3.2}$$

$$L_{path,LOS} = 27.56dB - 20log_{10}(f_c) - 20log_{10}(d) \tag{3.3}$$

$$L_{path,NLOS} = L_{path,LOS} - 10nlog_{10}(\frac{d}{d_0}) \tag{3.4}$$

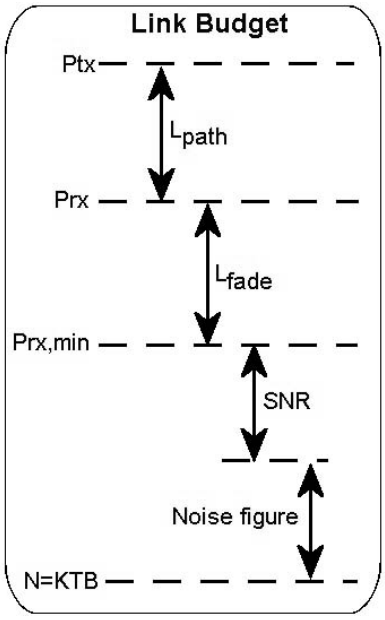


Figure 3.3: Link budget

Where L_{path} is the path loss, L_{fade} is the fading margin, $L_{path,LOS}$ is the path loss when there is line of sight, $L_{path,NLOS}$ is the path loss when there is no line of sight, f_c is the carrier frequency in MHz, d is the distance and d_0 is the reference distance for unobstructed propagation, both in meters. Finally, n is the path loss exponent. When f_c=2440 MHz, n=3, d=10m, d_0=8.5m, the resulting path loss assuming no line of sight is 62 dB. Assuming a fading margin of 8 dB and a transmitting power of 0 dBm, the minimum receivable signal power($P_{rx,min}$) becomes -70 dBm. Choosing this as the sensitivity level, the Noise Figure(NF) can be calculated:

$$P_{sensitivity} = P_{Rsource} + NF + SNR_{min} + 10log_{10}(B) \tag{3.5}$$

The noise from the source resistance($P_{Rsource}$) can be calculated(assuming input power match) with the noise voltage kT, where k is the Boltzmann constant($1.38 \cdot 10^{-23} \frac{J}{K}$) and T is the temperature in Kelvin. When the temperature is assumed to be 297 K, $P_{Rsource}$ becomes -174 dBm. Bluetooth uses a Gaussian Frequency Shift Keying(GFSK) modulation, that requires a Signal to Noise Ratio(SNR) of 21 dB. A single bluetooth channel has a bandwidth of 1 MHz, which determines the noise floor, kTB. The Noise figure is allowed to be 22.9 dB.

Gain

The maximum gain of this receiver is determined by the range of the ADC. When more than the maximum gain is applied, the ADC will not be able to convert the signal to the digital domain properly, effectively clipping the signal. Because the channel selection takes place digitally, each channel has to be digitized. Therefore, the channel with the largest signal determines the maximum gain that can be applied. According to the specifications, a Bluetooth receiver should be able to deal with a maximum signal level of -20 dBm. An

input voltage range of 2 V_{p-p} differentially should be possible with a 1.2 V supply. -20 dBm gives 63 mV_{p-p} signal, which would require a voltage gain of 31.6 or 30 dB. However, this is assuming there are no losses along the receiver chain. These losses will be calculated during the block level specifications, and need to be added to the gain to compensate.

Linearity

Non-linearities in a receiver can cause cross modulation or intermodulation, which can severely degrade the performance of the receiver. The required linearity of the entire receiver can be determined using equation 3.6[9]. The power of the third order intermodulation product(P_{im3}) should not affect the bit error rate, which requires the intermodulation product to be below the noise floor. The standard specifies a scenario where the input power level of the wanted signal is -67 dBm, while two interferers have an input power level of -40 dBm($P_{fund,in}$). The frequencies of the two interferers are chosen in such a way that the intermodulation product ends up at the same frequency as the wanted signal. In such a case, the intermodulation product should have a power level below -67dBm -21dB(SNR)=-88dBm.

$$IIP_3 = P_{fund,in} + \frac{(P_{fund,in} - P_{im3})}{2} \tag{3.6}$$

With this scenario, equation 3.6 gives an IIP_3 of -16 dBm. Because a differential circuit is used, second order intermodulation products cancel out, so the IIP_2 should be quite high. Because the noise and transfer function are probably more of a bottleneck, the IIP_2 is not investigated further.

Spurious Free Dynamic Range

There is also a specification for the relation between the noise floor of a system and the linearity. When a signal is weak, it cannot be detected. However, when it is amplified, the linearity also causes intermodulation products. The dynamic range is influenced by these products. The Spurious Free Dynamic Range(SFDR) can be defined with equation 3.7.

$$SFDR = \frac{2}{3}(IIP_3 - (P_{sensitivity} - SNR_{min})) \tag{3.7}$$

which gives a SFDR of 50 dB for a bluetooth receiver.

3.3.5 Block specifications

Introduction

The specifications from section 3.3.4 determines the performance of the receiver. A quick summary of the performance parameters is given in table 3.1. These specifications will be split up between the different blocks. First of all, the noise figure of each block needs to be calculated taking into account the noise folding effect. Combining the noise factors of each block to the total noise factor is done using equation 3.8.

Parameter	Value
f_c	2.44 GHz
NF	$<$ 22.9 dB
Gain	30 dB
IIP_3	$>$ -16 dBm
SFDR	50 dB

Table 3.1: Performance specifications receiver

$$F_{total} = 1 + (F_{stage1} - 1) + \frac{F_{stage2} - 1}{G_{a,stage1}} + \frac{F_{stage3} - 1}{G_{a,stage1} \cdot G_{a,stage2}} + \dots \tag{3.8}$$

To determine the linearity, the gain of the previous stage has to be taken into account. For this equation 3.9 is used.

$$\frac{1}{IIP_{3,total}} \approx \frac{1}{IIP_{3,stage1}} + \frac{G_{a,stage1}}{IIP^2_{3,stage2}} + \frac{G_{a,stage1} \cdot G_{a,stage2}}{IIP_{3,stage3}} + \dots \tag{3.9}$$

The required total specifications can be split up between the blocks now, as shown in table 3.2 and in figure 3.4. However, this process requires a number of iterations to end up with sensible specifications. To validate the given specifications, each block is discussed, which results in the numbers given in table 3.2.

Noise folding

The mathematics and mechanisms to calculate noise folding will be covered in more detail in chapter 4, but some estimations are necessary to derive the specifications for each block. In short, the RC network(modeling the switch as an resistance when it is on) of the track and hold can be seen as a lowpass filter which determines the bandwidth of the ADC. This bandwidth divided by the sampling frequency, determines how many frequencybands are folded on top of each other and thus determines the folding factor. The minimum sampling frequency for second-order sampling is 80 MHz per channel, which is the total bandwidth of bluetooth(79 channels of 1 MHz). An assumption is made that the half-power bandwidth of the track and hold is around 5 GHz, which results in an equivalent noise bandwidth of $\frac{\pi}{2} \cdot 5GHz$. This results in 100 bands($\frac{\pi}{2} \cdot 5GHz/80MHz$) that are folded, which is then the folding factor. This does not hold for the LNA noise contribution, which has a narrowband noise spectrum. Another assumption is made that the LNA bandpass filter decreases the noise folding by a factor 8(because the bandwidth of the LNA is approximately 8 times smaller than the bandwidth of the track and hold), which results in a folding factor of 12.5.

BAW filter

The Bulk Acoustic Wave filter is an off-chip component that approximates a 'brick wall' filter for the desired spectrum. Filters always have an insertion loss, which also adds to the noise figure. This insertion loss is assumed to be 1 dB. The filter is assumed to be very linear.

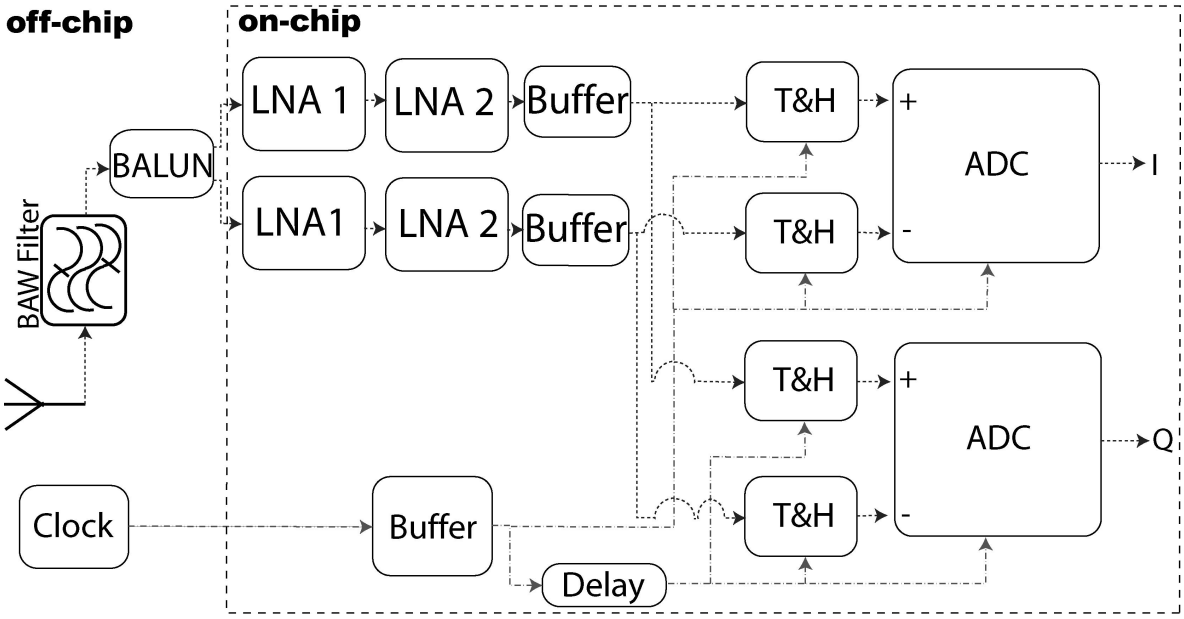


Figure 3.4: Block level design second-order sampling receiver

Parameter	Antenna	BAW	Balun	LNA1	LNA2	Buffer	T/H
Power gain(dB)		-1	0	4.9	13.9	9	0
power gain		0.8	1	3.1	24.8	7.9	1
Voltage gain,loaded(dB)		-1	0	19.1	16.1	0	0
Voltage gain,loaded		0.9	1	9.0	6.4	1.0	1.0
Zin(real,ohm)				50	100000	100000	22
Zout(real,ohm)	50			400	400	50	
NF(dB)		1	0	1	5	5	2
F		1.26	1	1.26	3.16	3.16	1.58
Folding factor				12.5	12.5	100	100
NF with folding				6.3	14.5	23.4	17.8
IIP_3(dBm)		100	100	0	0	10	15
	Antenna	BAW	Balun	LNA1	LNA2	Buffer	T/H
Σ Power gain(dB)		-1	-1	3.0	19.1	28.1	28.1
Σ Power gain		0.8	0.8	2.0	81.3	644.9	644.9
Σ Voltage gain(dB)		-1	-1	18.1	34.2	34.2	34.2
Σ Voltage gain		0.9	0.9	8.0	51.3	51.3	51.3
Σ NF(dB)		1.0	1.0	7.3	12.8	13.3	13.3
Σ F		1.3	1.3	5.4	18.9	21.5	21.6
IIP_3(dBm)		100	97.5	1.0	-4.5	-10.4	-15.0

Table 3.2: block specifications receiver

Balun

A balun is used to convert a single ended signal to a differential signal. This component will also be off-chip. The power transfer is assumed to be perfect, represented by a unity power gain. It is also assumed no noise introduced with this component and that the balun is very linear.

LNAs

Due to the relatively high gain required(30 dB), the choice has been made to cascade two LNA's, as shown in figure 3.4. The design of the two LNA's will be very similar, to save time. Because some bandpass filtering is required to reduce the noise folding, the LNAs will be inductively degenerated. This is a commonly used topology and therefore well understood. The first LNA will provide an input impedance of 50 Ω. The second LNA has a high ohmic input impedance. The LNA cannot drive a low ohmic load, because the voltage gain would degrade. This is caused by the change of the output resistance, which determines the voltage gain. The first LNA has to drive the second LNA which is high ohmic, which gives no problems. However, a buffer is needed between the second LNA and the track and holds. The noise contribution of the LNA is quite large, due to the noise folding. Although the LNA is designed to be narrowband, there will still be significant noise folding. Both LNA's have a good linearity figure.

Buffer

The buffers make it possible for the LNA to drive a low ohmic load. The noisefolding of the noise of the buffer is determined by the bandwidth of the track and hold. Due to the large voltage gain of the LNA's, this additional noise does not degrade the noise figure too much. The buffer needs to be very linear, because of the large input voltage swing.

Track and hold

The track and hold circuit converts a time continuous signal to a time discrete signal, using a switch and a capacitor. The size of the capacitor depends on the accuracy of the ADC and the type of architecture that is chosen for the ADC. Because the implementation form of the ADC is not yet known, the accuracy of the ADC is the determining factor for the size of the capacitor. The thermal noise from the switch should be smaller than the quantization noise(equation 3.10. When the ADC uses 14 bits to discretize the amplitude and the total sampling frequency is two times the bandwidth, the largest quantization error is given by equation 3.11. The least significant bit(LSB) is defined by equation 3.12, where the N is the number of bits of the ADC and V_{range} is the input range of the ADC. The thermal noise summed over the entire frequency range can be calculated with equation 3.13[10]. This results in a capacitor size given by equation 3.14, which is then calculated to be 4.3 pF.

$$V_{th,RMS} \leq v_q \tag{3.10}$$

$$v_q \leq \frac{1}{2}LSB \tag{3.11}$$

$$LSB = \frac{V_{range}}{2^N} \tag{3.12}$$

$$V_{th,RMS} = \sqrt{\frac{kT}{C}} \tag{3.13}$$

$$C \geq \frac{4^{N+1}kT}{V_{range}^2} \tag{3.14}$$

The half-power bandwidth of the track and hold is defined by the on resistance of the sampling switch and the sampling capacitor, which is given by equation 3.15 in Hz.

$$BW_{TH} = \frac{1}{2\pi}\frac{1}{RC} \tag{3.15}$$

The half-power bandwidth is chosen to be 5 GHz, which should result in a minimal loss at 2.48 GHz. From this assumption, the resulting on-resistance of the switch should be around 7 Ω. The input impedance of the track and hold can be derived using equation 3.16, which results in 22 Ω.

$$Z_{in,TH} = \frac{1}{2\pi f_c C} + R_{switch} \tag{3.16}$$

ADC's

The analog to digital converters have to digitize the entire bluetooth frequency band, which has a bandwidth of 83.5 MHz including guard bands. The Nyquist theorem states that sampling two times bandwidth is sufficient, but this provides no margin for errors such as jitter. To ensure reconstruction, guards bands have been introduced. Using the second-order sampling theory, each ADC is chosen to have a sampling frequency of 80 MHz. With this choice the subsampling ratio is 30, with f_l=2.4 GHz and f_u=2.48 GHz. The last channel at 2.48 GHz might fold back after sampling, but this can be digitally corrected if necessary. Another option would be to sample at 82.75 MHz, which would also solve the problem, but this would make calculations somewhat more difficult and less insightful. The ADC's will be implemented using a differential approach, which allows an input range of 2V. To calculate the number of bits, the receiver sensitivity is important. The receiver sensitivity was set to -70 dBm, which converts to a signal of 70,7 μV. This is amplified and the resulting voltage at the input of the track and hold is 6,3 mV_{p-p}. To get a sufficient signal to noise ratio, about 5 bits are needed for the signal, which is explained in chapter 4. This results in a 14 bits ADC.

3.4 Summary

A topology for the second-order sampling receiver is derived in this chapter. A good testcase for such receiver is Bluetooth, which is a low cost and low power standard. Because the specifications of Bluetooth are quite relaxed, the large amount of noise in each sample due to second-order sampling is acceptable. The specifications for the receiver and the blocks of the receiver are derived from the bluetooth standard, which are given in tables 3.1 and 3.2 respectively.

Chapter 4

Feasibility and performance

4.1 Introduction

Unfortunately, a master thesis is much too short to design the entire analog front-end of a receiver. To determine the feasibility the specifications need to be met. To make a good estimation of the performance, the performance figures need to be defined. These performance figures are often determined by error sources, where trade-offs are necessary between the different performance figures and specifications. To get a well designed receiver, these error sources and the impact on the different performance figures need to be well understood. First the approach used in this thesis to answer the questions on feasibility and performance is discussed. The performance figures for a second-order sampling receiver will then be defined. A large number of error sources exist in receivers, but only the noise folding, image rejection and jitter will be quantified using theory. Simulations in Matlab and Simulink are used to investigate these error sources. Finally, the experiments used to verify this theory in Cadence are specified.

4.2 Proof of concept

4.2.1 Goals

The goal of this master thesis is to determine the feasibility of a second order sampling receiver, not to make a Bluetooth receiver based on second order sampling. Thus, Bluetooth is only a test vehicle for this research. To determine the feasibility, all the performance trade offs need to be understood. With this knowledge the choice can be made whether a second-order sampling receiver topology can be used in a certain application. The goal in this chapter is to determine the performance limiting effects and derive the theoretical equations to describe these effects. Furthermore, experiments will be discussed to verify these equations and provide insight in the performance of the receiver.

4.2.2 Technology choice

The technology choice for a second-order sampling receiver can have a large impact on the feasibility of the receiver. The noise contribution from each transistor should be as low as possible, to reduce the effect of noise folding. Smaller technologies usually provide a decrease in power consumption, which would benefit our low power objective. Another choice is in the type of technology, e.g. CMOS, BJT or even BiCMOS. A big advantage of CMOS is the integration with digital logic and the relative low production cost(which is important for Bluetooth). The choice is made to go with 65 nm CMOS due to the earlier mentioned advantages and because this technology is available in Cadence to design circuits.

4.3 Performance figures

The performance figures for this receiver need to be defined, to determine how well the receiver performs. It is important to make a distinction between the specifications from chapter 3 and performance figures in this section. The specifications derived are necessary conditions for the receiver to use the Bluetooth standard(feasibility), while the performance figures determine how this receiver measures up in comparison to other receivers.

4.3.1 Signal-to-noise ratio and noise factor

The first performance figure is the signal-to-noise ratio(SNR) which is an essential figure in the design process, because it is a measure for the quality of the signal. However, to compare different receivers, the signal strength at the input of the receiver needs to be specified. Furthermore, the performance of an individual block might be difficult to determine, because it is determined by previous blocks. Therefore, a closely related performance figure is used, which is the noise factor. This performance figure specificies how much noise is added to the signal by the receiver, compared to a reference noise level. The noise generated by a 50 Ω resistor is often chosen as the reference noise level. The added noise is then given as a factor of the reference noise level, which is called noise factor. The advantage of the noise factor compared to the SNR, is that it is independent of the signal strength. Summarizing, the noise factor is a measure how much the SNR is degraded. The noise factor can be specified for individual blocks of the receiver, where the noise factor of the total receiver can be calculated with equation 3.8, which can be easily translated to the noise figure.

4.3.2 Linearity

The linearity of a receiver is another important performance characteristic of a receiver. When the output relation of a memoryless nonlinear system is approximated with a polynomial[9] of the input signal, the wanted first order harmonic is accompanied by unwanted higher order harmonics. The second and third order harmonics usually provide sufficient insight in the linearity of the system. The OIP_2 and OIP_3 relate the power of respectively the second order and third order harmonic to the first order harmonic at the output. Similarly the IIP_2 and IIP_3 relate the power of the harmonics when they are referred back to the input.

4.3.3 Power consumption

The power consumption of a receiver is becoming an increasingly important figure. However, it is not straightforward to predict the power consumption of a receiver. The power consumption of the analog front-end depends on the chosen implementation. Simulation software such as Simulink and Matlab do not take into account how the implementation is done on chip and thus cannot make a good approximation. Simulation software such as Cadence is much better suited for this purpose. The power consumption of the digital part depends on the operations that are performed digitally and the implementation on-chip. The implementation of the digital signal processing part of the receiver is outside the scope of this thesis and is not discussed here.

4.3.4 Image rejection ratio

The rejection of the image signal compared to the wanted signal gives insight in the quality of quadrature channel generation in receivers. The performance of receivers is partly determined by the image rejection that is possible with available design techniques and receiver topologies. The image rejection of the second-order sampling receiver depends on the matching quality of the I/Q channels and the effectiveness of the digital image rejection algorithm.

4.4 Performance limitations

4.4.1 Introduction

Significant performance limiting mechanisms are jitter, noise folding and quantization noise. These effects will be further investigated in this section, which will allow us to make trade-off choices in a more efficient way during the transistor level implementation.

4.4.2 Noise folding

The noise folding effect is an unwanted side-effect which occurs together with the down-conversion. During the downconversion, each band is copied to baseband, which requires a band-limited spectrum as an input. However, because the BAW filter was placed in front of the analog signal processing part, noise is added by this signal processing. The entire spectrum of noise is folded to baseband during sampling, which results in a noise power spectral density many times greater than with regular Nyquist sampling. But how much higher does the noise power spectral density become? First the number of bands that are folded is determined by the noise bandwidth and the sampling frequency of the track and hold(f_s). The noise bandwidth of a track and hold is calculated with equation 4.1[12].

$$f_b = \frac{\pi}{2} \times \frac{1}{2\pi R_{on} C_{sample}} \tag{4.1}$$

The noise power spectral density after the track and hold(S_{n2}) can be calculated, when the noise power spectral density before sampling(S_{n1}) is multiplied by the factor given in equation

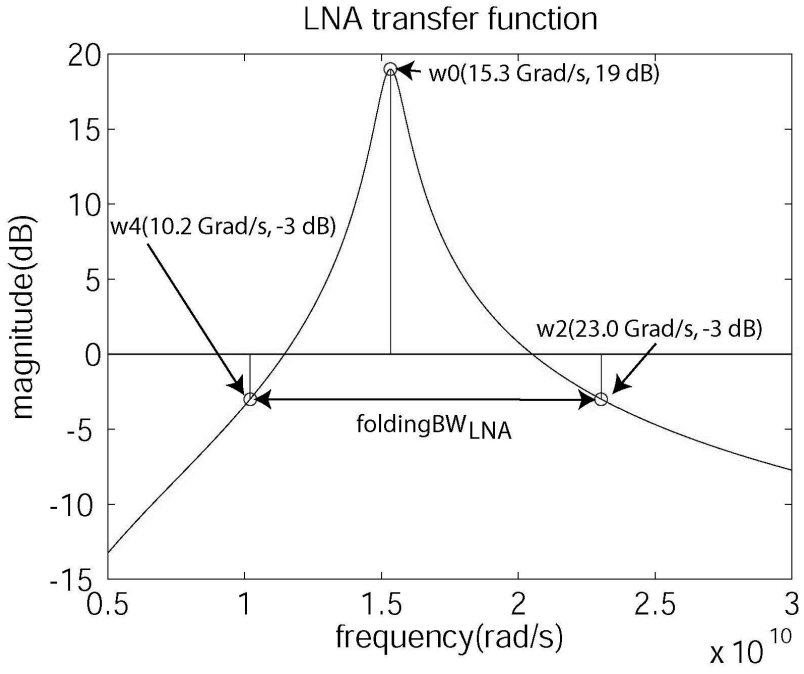


Figure 4.1: LNA transfer function

4.2.

$$S_{n2} = S_{n1} \times \frac{1}{\pi} \times (\frac{f_b}{f_s}) \tag{4.2}$$

Where the factor $\frac{1}{\pi}$ is the result of the tracking and holding of the track and hold, which reduces the conversion gain similar to a mixer.

However, equation 4.2 can only be used if no other filtering is performed between the noise source and the track and hold. This condition is true for the noise from the switch and the buffer, but is not true for the narrowband LNA. The narrowband LNA will also add noise, but the noise from the LNA is bandpass filtered, which requires a calculation of the noise bandwidth of the narrowband LNA. However, the filtering provided the LNA is quite different from a regular bandpass filter, because gain is also added. This results in a new bandwidth definition which can be used to calculate the amount of noise folding. This bandwidth will be referred to as $foldingBW_{LNA}$ and use the absolute -3 dB point, because this defines how much noise bands will contribute to the noise folding. The narrowband LNA uses the resonance of a LC-tank where the magnitude of the relative admittance(Y_{rel}) is given by equation 4.3[11], with the center frequency ω_0(in rad/s) and input frequency ω(in rad/s).

$$Y_{rel} = \frac{1}{\sqrt{1 + (Q_0)^2(\omega/\omega_0 - \omega_0/\omega)^2}} \tag{4.3}$$

where

$$Q_0 = \frac{w_0 L}{R} \tag{4.4}$$

Equation 4.3 can be modified to also include the gain of the LNA, which results in equation 4.5.

$$\alpha(\omega) = \frac{A_v}{\sqrt{1 + (Q_0)^2(\omega/\omega_0 - \omega_0/\omega)^2}} \tag{4.5}$$

With the transfer function given in equation 4.5, the frequencies where the loss is 3 dB needs to be calculated(as displayed in figure 4.1). Equation 4.5 is rewritten and using the standard solution for second order polynomials(abc formula), the frequencies given by equations 4.6 through 4.9 are derived.

$$\begin{aligned}
(\frac{A_v}{\alpha(\omega)})^2 &= 1 + (Q_0)^2(\omega/\omega_0 - \omega_0/\omega)^2 \\
\frac{(\frac{A_v}{\alpha(\omega)})^2 - 1}{(Q_0)^2} &= (\omega/\omega_0 - \omega_0/\omega)^2 \\
\swarrow & \qquad \searrow \\
\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2 - 1}{(Q_0)^2}} = \omega/\omega_0 - \omega_0/\omega & \qquad -\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2 - 1}{(Q_0)^2}} = \omega/\omega_0 - \omega_0/\omega \\
0 = \omega^2/\omega_0 - \omega\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2 - 1}{(Q_0)^2}} - \omega_0 & \qquad 0 = \omega^2/\omega_0 + \omega\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2 - 1}{(Q_0)^2}} - \omega_0
\end{aligned}$$

$$\omega_1 = \frac{\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2}} - \sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2} + 4}}{\frac{2}{\omega_0}} \tag{4.6}$$

$$\omega_2 = \frac{\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2}} + \sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2} + 4}}{\frac{2}{\omega_0}} \tag{4.7}$$

$$\omega_3 = \frac{-\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2}} - \sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2} + 4}}{\frac{2}{\omega_0}} \tag{4.8}$$

$$\omega_4 = \frac{-\sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2}} + \sqrt{\frac{(\frac{A_v}{\alpha(\omega)})^2-1}{(Q_0)^2} + 4}}{\frac{2}{\omega_0}} \tag{4.9}$$

Equation 4.8 and 4.6 can be discarded, because it gives the same result as equation 4.7 and 4.9, only the sign differs. The bandwidth(in Hz) of the LNA is calculated with equation 4.10, which has been done in figure 4.1($A_v = 19dB, Q = 15, \alpha(\omega) = -3dB, \omega_0 = 2.44GHz \times 2\pi$). The resulting noise folding can now be calculated using equation 4.11, by first converting the bandwidth of the LNA to the noise bandwidth and taking into account the switching.

$$foldingBW_{LNA} = \frac{|\omega_2 - \omega_4|}{2\pi} \tag{4.10}$$

$$S_{n2} = S_{n1} \times \frac{1}{\pi} \times \frac{foldingBW_{LNA}}{f_s} \times \frac{\pi}{2} \tag{4.11}$$

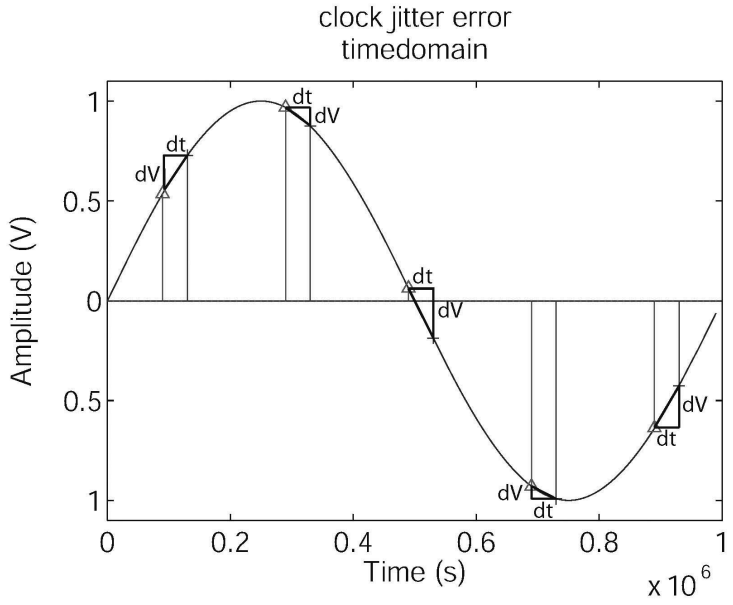


Figure 4.2: Clock jitter sampling errors

These intermediate theoretical calculations are used to derive how feasible the receiver is. Using equation 4.2 and assuming a bandwidth of 5 GHz and a sampling frequency of 80 MHz, the noise folding factor of the buffer and track and hold becomes 31, resulting in noise figures of 18.3 dB and 12.8 dB respectively. Equations 4.11 and 4.10 is used to calculate the noise folding for the two LNAs. The first LNA is calculated to have a folding bandwidth of 2 GHz, which results in a folding factor of 12.8 and a noise figure of 6.4 dB. The second LNA is calculated to have a folding bandwidth of 1.44 GHz, which results in a folding factor of 9 and a noise figure of 13.1 dB. The new calculated noise figure for the receiver becomes 12.1 dB.

4.4.3 Jitter

The influence of jitter has impact on two performance figures of this receiver which are signal-to-noise ratio and image rejection ratio. The signal-to-noise ratio in each channel is degraded by jitter because the actual sampling moment is slightly earlier or later than the intended sampling moment. When this timeshift is small compared to the period of the signal, it can be converted to an error in amplitude using the slope of the input signal, illustrated in figure 4.2. The first line(green, triangle tickmark) represents the intended sampling moment, the second line(red, cross tickmark) represent the actual sampling moment due to jitter. Note that the timeshift in this figure is equal in each case, where jitter actually causes this timeshift to vary randomly.

Using this approach, and assuming a sinusoidal input with amplitude A and frequency f(equation 4.12), the slope is easily derived using the derivative(equation 4.13). The root

mean square(RMS) value can be used to get the average slope of the derivative. The RMS value of the jitter noise($\Delta v_{j,rms}$) can now be calculated with the RMS value of the jitter time(equation 4.14)[13] assuming the jitter has a normal distribution with zero mean.

$$v(t) = Asin(2\pi ft) \tag{4.12}$$

$$\frac{dv(t)}{dt} = 2\pi fAcos(2\pi ft) \tag{4.13}$$

$$\frac{\Delta v_{j,rms}}{\Delta t_{j,rms}} = 2\pi fA\sqrt{\int_{-1/2f}^{1/2f} cos(2\pi ft)dt} = 2\pi fA\sqrt{2} \tag{4.14}$$

The RMS value of the jitter time is often derived assuming a normal distribution of the jitter, with zero mean and a variance dependent on the severity of the jitter. However, this assumption is not necessarily true[14]. It is derived in this literature, that a convolution of the clock jitter and the derivative of the input signal in the frequency domain is required to determine the resulting jitter noise. With this approach, the jitter noise can be orders of magnitude smaller than the jitter noise using the assumption of a normal distribution of jitter. Because an off-chip clock is used, the jitter frequency spectrum is assumed to have a $1/f^2$ distribution[9]. The clock jitter at a specific frequency(f_j) can be represented with a sine wave with frequency $f_s - f_j$, that frequency modulates the clock. The RMS value of the clock jitter can be calculated using the $1/f^2$ distribution and the resulting jitter noise can be determined.

The image rejection is affected by jitter, when the delay between the sampling moments of the I and Q channels differs from the chosen delay. This delay realizes a 90 degree phaseshift for one frequency, which is rejected perfectly. When the phaseshift becomes bigger or smaller(because the delay is changing), the rejection becomes less efficient overall. To get overall adequate image rejection, the delay is chosen for the frequency in the middle of the Bluetooth band, 2.44 GHz. When this delay is increased or delayed, the image rejection at the edges of the Bluetooth band will improve on one side and decrease on the other side. When this effect is increased, the image rejection might not meet the requirements specified in the standard.

Fortunately, there will probably be some correlation between the jitter of the I channel and the Q channel, because the same clock is used to generate the clocking signals. When there is full correlation between the I channnel jitter and the Q channel jitter, the delay will remain the same.

4.4.4 Quantization noise

When the conversion from the analog domain to the digital domain takes place, the accuracy of the signal in the digital domain depends on the number of bits used to quantize the amplitude. However, for every bit added to the resolution of the ADC, the power consumption is increased. When choosing the resolution of the ADC, the quantization noise should not degrade the signal-to-noise ratio. However, the ADC also shouldn't be over-specified, because the power consumption of the ADC should be as low as possible.

The Bluetooth standard assumes a worst case interferer signal power at the input of the receiver of -20 dBm. Because the band selection occurs digitally, the entire frequencyband of

Bluetooth needs to be converted to the digital domain. These two considerations have a large impact on the required resolution of the ADC. Another look at the link budget is useful to understand the resolution requirement. Assuming the wanted signal at the input has a signal power of -70 dBm and an interferer is present at -20 dBm, a dynamic range of at least 50 dB is required to accommodate both signals. To successfully demodulate the weakest signal, 21 dB of SNR is required to demodulate the signal, so another 21 dB of dynamic range is added. When the quantization noisefloor is 10 dB lower than the noisefloor from the analog front-end, the SNR is not degraded[17]. This results in a total dynamic range of 50+21+10=81 dB which requires a 14 bit ADC with a total sampling frequency(combining the I and Q channel) of at least 2 times the bandwidth using equation 4.15[13](N is the number of bits). This would satisfy the receiver sensitivity of Bluetooth standard, which is -70 dBm. To accommodate a noise figure of 11 dB, and realize a receiver sensitivity of -82 dBm, a 16 bit ADC is required.

$$SNR = 6.02N + 1.76dB \tag{4.15}$$

An often used technique for ADC's is oversampling, which decreases the quantization noise floor. Equation 4.16 shows the relation between oversampling and signal-to-noise ratio, where f_0 is the Nyquist rate.

$$SNR = 6.02N + 1.76dB + 10log_{10}(OSR) \tag{4.16}$$

where

$$OSR = \frac{f_s}{2f_0} \tag{4.17}$$

Subsampling does have impact on the determination of f_0, because it depends on the subsampling ratio where the information band will end up. If the subsampling ratio is an integer and odd, the information band ends up at the far end of the spectrum after sampling, which will give a oversampling ratio of 1(because the highest frequency component will be around $\frac{1}{2}f_s$). However, when the subsampling ratio is an integer and even, the oversampling ratio will be maximized, because the information bands ends up at the beginning of the spectrum after sampling. In other words, f_0 will be mimimized, resulting in the largest oversampling ratio. When the total sampling frequency is increased above 2 times the bandwidth, the quantization noise will decrease because it averages out. It is possible that the noise floor of the analog front-end turns out to be lower than what the standard defines, which could result in degradation of the SNR due to the quantization noisefloor. Because higher resolution means more power consumption, there is a trade-off here between power consumption and signal-to-noise ratio. Due to the focus on low power, the ADC is chosen to be 14 bit, which satisfies the sensitivity specification from the Bluetooth standard.

4.5 Performance simulations

4.5.1 Introduction

To verify some of the equations derived in the previous section, the setup is evaluated using Simulink and Matlab simulations. This has the advantage that the system can be described using a programming environment, which is much faster than making an entire design with

Cadence. The disadvantage is that the entire system is a digital approximation of the analog system. Digital system do not have to deal with noise, only finite accuracy of calculations. A digital approximation of noise is possible, but needs to be introduced by the user. First the general setup will be discussed in section 4.5.2. With this setup, the performance limiting errors in the receiver can be approximated, by introducing non-idealities.

4.5.2 Simulink/Matlab setup

Simulink and Matlab simulations have the advantage that they can provide quick insights into the performance characteristics of a system. Several setups are prepared to model the different error sources. The analog front-end is approximated with Simulink(appendix A), while the digital signal processing is performed in Matlab(Appendix B).

An error source in analog signal processing is an unwanted side-effect, which limits the final performance figures. Every topology has specific error sources that need to be minimized to get the best performance. In this overview, a number of error sources are introduced that affect the performance of the second-order sampling receiver. How the performance is influenced is shortly illustrated quantitatively using Simulink/Matlab simulations, but cannot be used to guarantee successful implementation in CMOS.

Noise folding

Noise folding is an important error mechanism in subsampling. Noise from the entire spectrum is folded to the Nyquist band after the sampling operation. The initial noise needs to be introduced manually in Simulink simulations, so a gaussian white noise generator is added to the input signal, that provides a noise floor equal to a 50 Ω resistor times a noise factor. AD converters always have a certain bandwidth that is related to the on-resistance of the switch and capacitor in the track and hold. A lowpass filter is added to the testbench to define this bandwidth, because this is essential to define the noise folding effect. Finally, a reference channel where no noise folding occurs is added, which results in the simulink model shown in figure A.1.

The noise folding effect is simulated in Simulink/Matlab and the results are presented in figure 4.3. The sampling frequency of the I and Q channel is varied, while the reference channel uses sampling frequency of 5.12 GHz. The input signal consists of a carrier sine wave with a frequency of 2.43 GHz amplitude modulated with a 1.25 MHz sine wave. The average noise level is the signal power in all the frequency bins divided by the number of frequency bins, without the frequency bins of the input signal. Simulation 1 introduces noise equivalent to a noise factor of 10, while simulation 2 uses a noise factor of 30. In this simulation the quantization noise is not introduced in the simulation, to keep this analysis clear. The reference channel has an anti-aliasing filter included, which prevents any noise folding to occur.

The results in figure 4.3 are compared to theory. Equation 4.2 can be used to calculate the relative decrease in the noise floor. The noise bandwidth is chosen to be equal for all the sampling frequencies. However, the noise bandwidth of the reference channel is different from the noise bandwidth of the subsampling channel, due to the anti-aliasing filter. Therefore, the noise levels will not be equal when the sampling frequency of the subsampling channel is

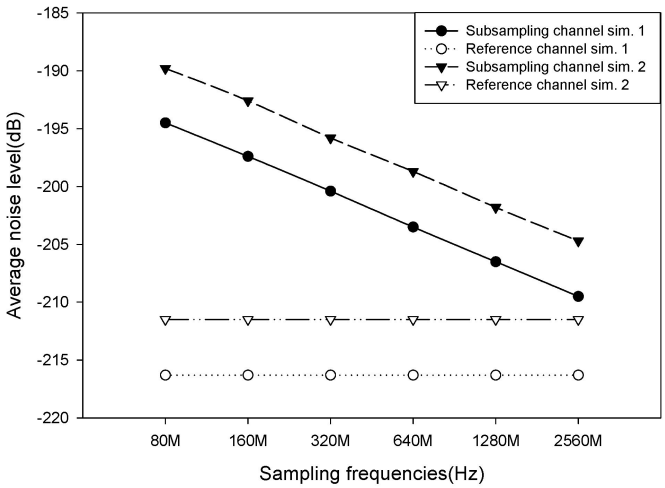


Figure 4.3: noise folding effect in Simulink/Matlab simulations sim 1) NF=10 sim 2) NF=30

equal to the sampling frequency of the reference channel. When the sampling frequency of the subsampling channel doubles, the noise should decrease by a factor 2, which is 3 dB. The added noise in simulation 2 is a factor 3 bigger than the noise in simulation 1, which is 4.8 dB. Both predictions can be verified in figure 4.3.

Mismatch

Although the I and Q channel are designed to be identical, process variations result in small differences in the channels(mismatch). A model in Simulink is derived that taken into account this mismatch(figure A.2). Variations in the transfer function can degrade the image rejection ratio. The simulations in Simulink/Matlab without mismatch, illustrated in figure 4.4 and 4.5 labeled with normal, match very well with the image rejection specified by equation 2.10. The input signal now consists of a carrier sine wave with a frequency of 2.43 GHz amplitude modulated with a 312.5 KHz sine wave, but also a carrier sine wave at the frequency specified as image frequency amplitude modulated by a 1.25 MHz sine wave. The image frequency is chosen in such a way that after sampling it is aliased to the same frequency as the other carrier wave. The sampling frequency of the I and Q channel is 80 MHz. When gain mismatch in the transfer function is introduced, the image rejection is degraded.

The effect of mismatch on the image rejection in dB is described in literature[9] with equation 4.18, where $\Delta A/A$ is the relative mismatch error in gain and θ is the phase error in radians.

$$IRR = 10log_{10}(\frac{(\Delta A/A)^2 + \theta^2}{4}) \tag{4.18}$$

For an image frequency of 2.43 GHz with no relative gain mismatch, the phase mismatch is 0.0064 rad(equation2.9), which is calculated using the delay(102.46 ps, equation 2.8 f_c=2.44

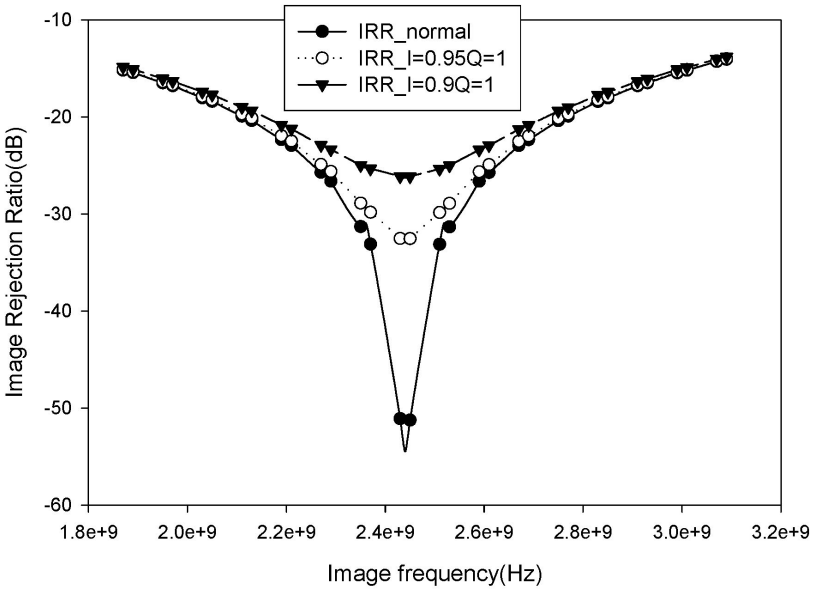


Figure 4.4: Image Rejection Ratio degradation due to variation in the transfer function in Matlab/Simulink simulations

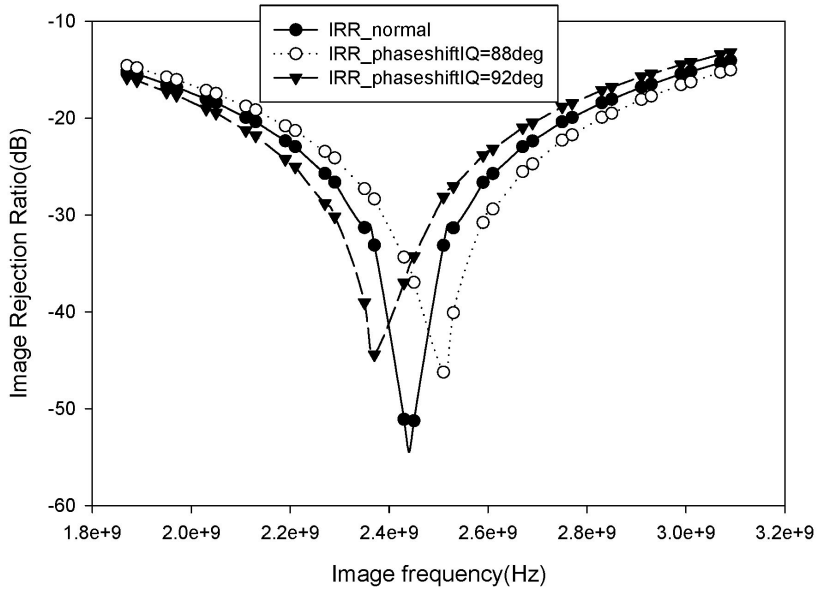


Figure 4.5: Image Rejection Ratio degradation due to phaseshift variation in Matlab/Simulink simulations

GHz). Using equation 4.18, the image rejection is calculated to be -49.8 dB. This matches well with figure 4.4, where the simulation gives an image rejection of -51.1 dB. When relative gain mismatch of 0.05 and 0.1 is introduced, the image rejection is calculated to be -32.0 and -26.0 dB respectively. Simulations match again with an image rejection of -32.5 dB and -26.1 dB.

The delay between the sampling moments of the two ADC's is implemented using a delayline. However, due to process variations or temperature, this delay can also vary slightly. The effect of these kind of variations is illustrated in figure 4.5, where the delay is 100.18 ps for the 88 degrees phaseshift and 104.7 ps degrees phaseshift for the 92 degrees phaseshift.

The image rejection is reduced by the phase mismatch only, which can be calculated with the delays. Once again, the normal rejection is calculated to be -49.8 dB for an image frequency of 2.43 GHz. With a delay of 100.18 ps, the phase mismatch is 0.0412 rad. the image rejection is calculated to be -33.7 dB, while simulations give -34.3 dB. The delay of 104.7 ps gives a calculated image rejection of -37.0 dB which matches exactly with the simulations.

Although these effects can have a significant impact on the performance, these kind of systematic errors can be improved digitally or reduced by choosing proper layout. Therefore this effect is not investigated further.

Jitter

Jitter degrades the performance on two levels, which are signal-to-noise ratio and the image rejection ratio. Clock jitter can be described as an unknown timeshift of the sampling moment, which alters the time delay between the I and the Q channel. Depending on the distribution of the clock jitter, the image rejection ratio for a specific channel can either degrade or improve. This effect is illustrated in figure 4.6. The Simulink model used is depicted in figure A.3, where the time delay is altered using a gaussian noise source. The input signal is similar to the one used in the mismatch simulations. In this simulation, the timeshift can either be -2 ps, 0 ps or +2 ps, which is dependent on the gaussian noise source.

This jitter simulation shows that jitter has impact on the image rejection. However, because the jitter is dependent on the random distribution of the gaussian noise source, it is not straightforward to predict the image rejection. This would require a statistical approximation to determine the distribution of the jitter and the correlation between the two channels.

The timeshift in the sampling moment has another effect that is visible in the signal-to-noise ratio. Because the sampling moment is affected by a random offset in time, the voltage level of the signal can be different due to this timeshift, which results in an error dependent on both the signal and the clock jitter. This error is introduced using the derivative and a random number generator, shown in the Simulink model in figure A.4. The input signal is similar to the one used for the noise folding simulations. The amount of jitter is controlled by the variance of the random number generator, which is $1 \cdot 10^{-6}$ in simulation 1 and $3 \cdot 10^{-6}$ in simulation 2, although this random number generator is attenuated before it is multiplied by the derivative. This results in a standard deviation of 100 fs for simulation 1 and 173 fs for the simulation 2.

The effect on the signal-to-noise ratio of the Q channel is illustrated in figure 4.7. Another interesting observation is the noise folding effect that occurs, because the noise floor is considerably higher than the reference channel and the -3dB decrease of the noise floor every

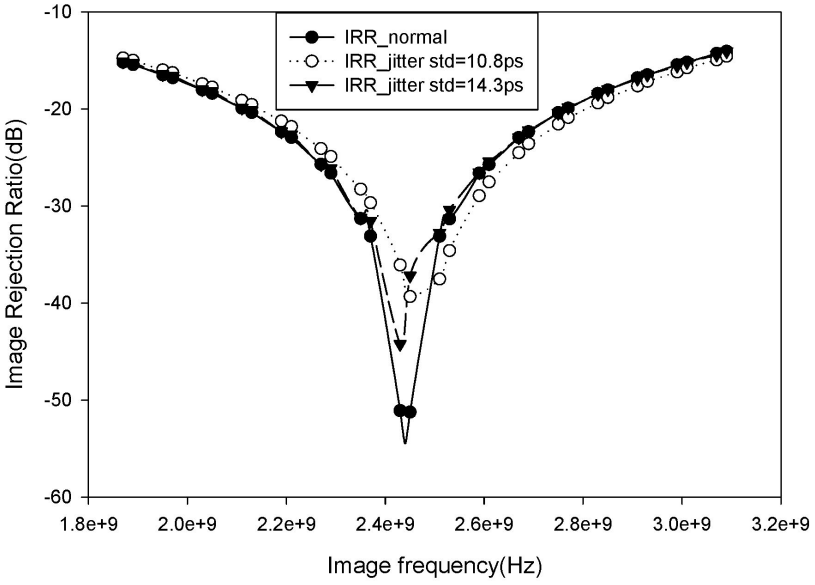


Figure 4.6: Image Rejection Ratio degradation due to jitter in Matlab/Simulink simulations

time the sampling frequency is doubled. However, this might also be due to the setup used to introduce the noise, which is an approximation of the jitter noise. The noise should actually be introduced in the zero-order hold block, with a random timeshift. When the jitter variance is three times bigger, this results in a 4.8 dB increase in noise floor, which matches with theory(equation 4.14).

Quantization noise

During the conversion from the analog domain to the digital domain, the amplitude is discretized in a limited number of quantization levels. Because of this discretization, there is always an error, where the magnitude of the error is dependent on the resolution of the analog to digital converter(ADC). This error is called quantization noise.

In this simulation, the average noise level in the Q channel is determined for different sampling frequencies and compared with a reference channel which uses a constant sampling frequency of 5.12 GHz. The same setup to illustrate the mismatch error(figure A.2) is used to illustrate the quantization noise, but no mismatch is introduced in this simulation. The first simulation uses a 10 bit quantizer, the second simulation uses a 12 bit quantizer.

When the sampling frequency is doubled for the subsampling channel, the quantization noise floor decreases with 3 dB, due to the oversampling. This matches with equation 4.16. The 12 bit quantizer lowers the noise floor with 12 dB compared to the 10 bit quantizer, because the quantization noise power is 4 times smaller. When the subsampling channel would sample at the same frequency as the reference channel, the noise floors will be equal.

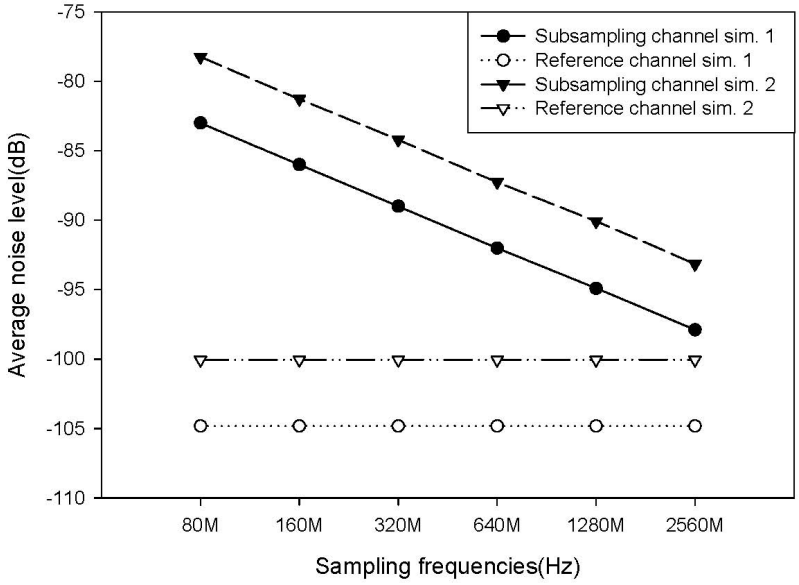


Figure 4.7: Signal-to-noise degradation due to jitter in Matlab/Simulink simulations sim 1) jitter std = 100 fs sim 2) jitter std = 173 fs

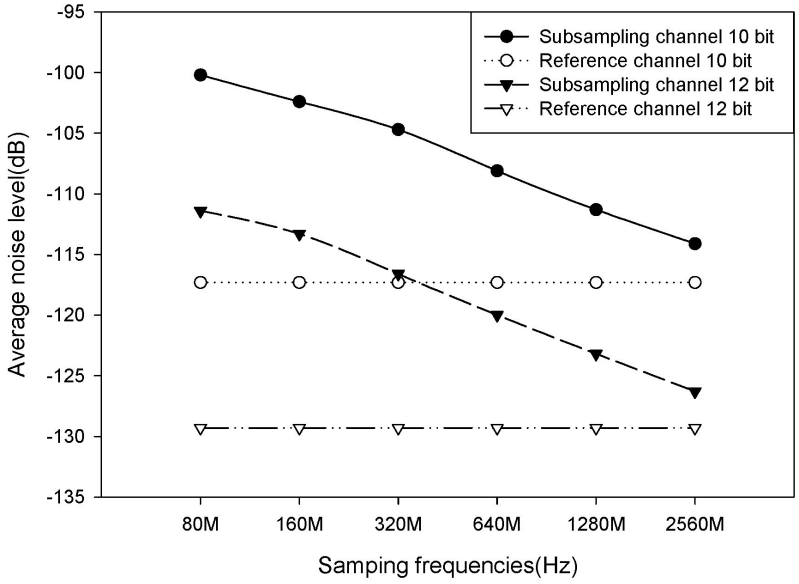


Figure 4.8: Quantization noise in Matlab/Simulink simulations

4.5.3 Conclusions

The error sources in a second-order sampling receiver can be approximated using Simulink/Matlab simulations. From this analysis, it becomes clear that noise folding, clock jitter and quantization noise are prominent limiting factors. These effects will be studied further to find out how these error sources limit the performance and which trade-offs are necessary.

4.6 Experimental setup

4.6.1 Introduction

Although simulations in Simulink/Matlab can give a first insight, simulation of an implementation is required to make a statement about the feasibility and the performance limiting factors. For this purpose, several experiments are derived to compare simulation results with the theoretical results. In chapter 6, the results of these experiments will be presented. The experiments specified here will be simulated in the Cadence environment.

4.6.2 Linearity experiment

The linearity of the receiver is determined to verify whether it meets specifications. First, individual blocks are simulated to determine their linearity. A prediction can be made how linear the total receiver should be. Then the total circuit is simulated and the linearity is derived.

4.6.3 Noise folding experiment

Using noise simulations, the noise figures for a number of components will be verified. These components include the track and hold switch, buffer and the LNA's. From these numbers, the noise figure for the total receiver is also derived, for a number of frequencies in the Bluetooth band. Furthermore, the size of the sampling capacitor and the subsampling ratio will be varied to determine the dependence on these parameters. The Q factor of the LNA LC tank will also be varied, to determine the effect of this parameter on the noise folding.

4.6.4 Quantization noise experiment

The noise that is added by quantization needs to be determined in the digital domain, to verify sufficient signal-to-noise ratio. To determine the noise floor, the DFT is used. However, the DFT adds processing gain, dependent on the number of DFT points[15]. This processing gain has to be removed to determine the RMS quantization noise floor. Finally, a -70 dBm input signal is used to determine the final signal-to-noise ratio.

4.6.5 Interferer experiment

In wireless receivers, the frequency spectrum can contain interferers that are much stronger than the wanted signal. Because the principle of subsampling is used in this receiver, interferers anywhere in the frequency spectrum can overlap with the signal of interest. Due to this reason, a bulk acoustic wave filter is added, which acts like a brickwallfilter. It is investigated how well such a configuration will reject interferers.

4.6.6 Image rejection experiment

The image rejection of the second-order sampling receiver can be predicted by equation 2.10. But how does the implementation in CMOS affect this image rejection? It is also whether the image rejection is indeed sampling frequency independent.

4.6.7 Jitter experiment

The jitter experiment will use a sine wave to control the amount of clock jitter that is present. From the relation between the RMS power of the sine wave, the power of the input signal and the resulting error in the digital domain the theory can be verified. Finally, the subsampling ratio will also be varied to investigate it's effect on the jitter noise.

4.6.8 Power consumption experiment

To determine how low-power this receiver is, the power consumption of the total circuit will be verified. Because every block of the receiver is also simulated a prediction of the total power consumption is possible.

4.7 Summary

The performance figures for a receiver are determined and the error sources in a second-order sampling receiver are described mathematically and approximated using Simulink/Matlab simulations. From this analysis, it becomes clear that noise folding, clock jitter and quantisation noise are prominent performance limiting factors. Finally a number of experiments in Cadence are specified to verify the theoretical hand calculations and derive the receiver performance.

Chapter 5

Transistor level design

5.1 Introduction

The transistor level designs of the blocks required for a second-order Bluetooth receiver are discussed in this chapter. The receiver is designed using 65 nm CMOS transistor models from NXP. The circuit is designed for different sample frequencies, but for convenience the 80 MHz configuration is used as guideline throughout this chapter. When an important circuit design parameter is changed because of this sampling speed, this is mentioned.

The track and hold design will be discussed first, which has to be very linear. A bootstrapping circuit can be used to increase the linearity of the switch. The design of the LNA's will then be discussed, where the design of the first LNA is quite similar to the design of the second LNA. The buffer that is required between the second LNA and the track and hold is examined next. Finally, the design of the clock driver circuitry is investigated. The ADC's are not designed, due to time constraints, but the figure of merit of two other designs are available and will be extrapolated for this receiver. After these blocks are designed, they can be simulated and verified in chapter 6.

5.2 General design approach

The performance limiting mechanisms all depend on the sampling speed, so varying the sampling speed is essential to making a good comparison between the theoretical models and the simulations. Therefore, the implementation of the receiver is done for a number of different sampling speeds. Another advantage is that the implementation of a receiver often reveals additional problems, so using different configurations already gives a good overview for future development.

Track and Hold	
Parameter	Value
Bandwidth	2.48 GHz
NF	$<$ 2.0 dB (80 MHz clock)
Voltage gain	0 dB
IIP_3	$>$ 15 dBm

Table 5.1: Performance specifications Track and Hold

5.3 Track and hold

5.3.1 Introduction

The track and hold circuit will be designed first, because it has impact on the design of the entire circuit. First the design goals for this block are determined, after which different topologies are presented. One topology is chosen, and hand calculations are used to determine the best choice of the design parameters of the circuit. The switch driver circuit is also discussed here, because it is part of the track and hold. Finally, the design choices of the track and hold are discussed, after which the final switch driver design is presented.

5.3.2 Design goals

The track and hold is designed to be very linear(because it is one of the last analog block) and have very little conversion gain loss, so a voltage gain of 0 dB. However, this track and hold also has to have a very large bandwidth. The track and hold also has to provide sufficient accuracy for the ADC, which is determined by the size of the sampling capacitor.

5.3.3 Topology

The track and hold topology basically consists of a switch and a capacitor, where the implementation of the switch can be chosen. Five well known topologies for the switch are shown in figure 5.1. The first two topologies(a en b) use a standard mosfet and a square wave clock is used to switch them on and off. However, because the voltage across the gate and source of the mosfet will depend on the input signal, the on-resistance of the switch will depend on the input signal. This gives non-linearities, when the input voltage range is large. This can be compensated by using mosfets with thicker gate-oxide, and driving the gate of the mosfet by a higher voltage.

Combining a nmos and pmos as shown in figure 5.1c) reduces this effect because the combination conducts well over the entire range, but introduces a new problem. When there is a small difference in timing in the clock and the inverted clock, it results in distortion of the sampled signal.

Another option to prevent the on-resistance to change, is to make sure the source-gate voltage is always fixed when the switch is on. This can be done using bootstrapping, which uses a switch driver circuit. However, this switch driver circuit needs to be designed in such a

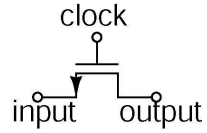
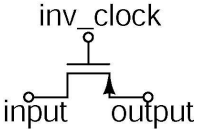
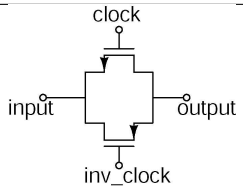
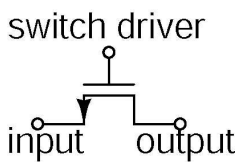
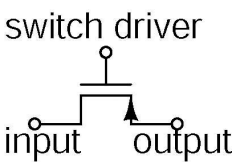
a) Nmos switch	b) Pmos switch	c) transmission gate	d) bootstrapped nmos switch	e) bootstrapped pmos switch
				

Figure 5.1: Switch topologies

way that the voltage across gate-drain and gate-source does not exceed 1.2 V. Otherwise the circuit lifetime can decrease dramatically, due to gate-oxide breakdown. This topology will be chosen, because it offers the best linearity.

5.3.4 Track and hold calculations

Capacitor size

The capacitor size is determined by the implementation of the ADC. Both speed and accuracy requirements can have impact on the capacitor size. Because the implementation of the ADC is not included in this thesis, the general equation as shown in section 3.3.5 is used. The resulting equation(3.14) is repeated for convenience(equation 5.1).

$$C_{sample} \geq \frac{4^{N+1}kT}{V_{range}^2} \tag{5.1}$$

In section 4.4.4 it was derived that a 14 bit ADC is necessary to meet the required sensitivity specification. However, a 13.5 bit accuracy for the track and hold will also meet the required sensitivity level with a sampling frequency of the track and holds of 80 MHz. Because the ADC cannot provide half bits, the ADC has to provide 14 bits.

It would require quite a lot of power to drive such a capacitor, so reducing the voltage range is a solution. However, when the voltage range is decreased, the thermal noise will have more effect, so the capacitor size needs to be increased to compensate, so no power is saved.

Switch resistance

A sampling switch can be modeled as a resistance, which has the convenient property that is has an extremely high resistance when the switch is off, and a reasonably low resistance when the switch is on. The on-resistance of the switch, in combination with the capacitor determines the bandwidth of the track and hold and thus the voltage loss across the switch. The voltage transfer(α_1) can be determined from figure 5.2 with equation 5.2.

$$\alpha_1 = \frac{Vsample}{Vin} = \frac{1}{j\omega R_{switch} C_{sample} + 1} \tag{5.2}$$

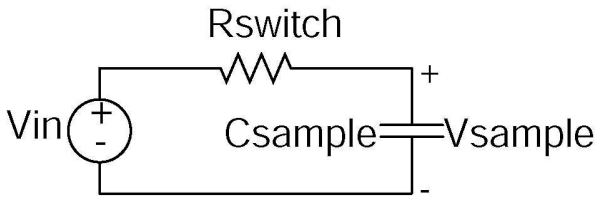


Figure 5.2: Equivalent circuit track and hold

From this equation it becomes clear that a smaller bandwidth can be chosen at the cost of additional loss in voltage transfer. A smaller bandwidth will reduce the noise folding effect. However for a smaller voltage range, the capacitor size needs to be bigger.

Input impedance

The input impedance of the track and hold for ADC's that use regular sampling is high. However, because the bandwidth of this track and hold has to be very large and the size of the sampling capacitor is big, the input impedance becomes low ohmic. This can be calculated using equation 5.3.

$$Z_{in} = \frac{1}{2\pi j\omega C_{sample}} + R_{switch} \tag{5.3}$$

This has a large impact on the buffer, especially the power consumption. When the power consumption should be low, the input impedance should be as large as possible. A relation between the input impedance and the voltage transfer in the track and hold(α_1) is derived. Equation 5.2 can be rewritten to equation 5.4 which provides the on-resistance of the switch.

$$R_{switch} \leq (\frac{1}{\alpha_1} - 1)\frac{1}{2\pi j\omega C_{sample}} = (\frac{1}{\alpha_1} - 1)\left|\frac{1}{2\pi\omega C_{sample}}\right| \tag{5.4}$$

The relation between V_{range} and α_1 is given by equation 5.5 which assumes an input signal of voltage V_{in} for each track and hold.

$$V_{range} = \alpha_1 V_{in} \tag{5.5}$$

This allows us to rewrite the capacitor size(equation 5.1) as a function of the voltage transfer(α_1) as shown in equation 5.6.

$$C_{sample} \geq \frac{4^{N+1}kT}{(\alpha_1 V_{in})^2} \tag{5.6}$$

The input impedance can now be written as a function of the voltage transfer(α_1), which is done in equation 5.7.

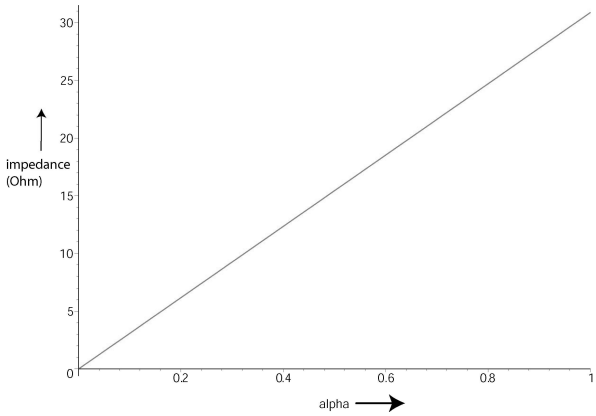


Figure 5.3: Input impedance as function of α_1

$$Z_{in} = \left| \frac{1}{2\pi\omega \frac{4^{N+1}kT}{(\alpha_1 V_{in})^2}} \right| + (\frac{1}{\alpha_1} - 1) \left| \frac{1}{2\pi\omega \frac{4^{N+1}kT}{(\alpha_1 V_{in})^2}} \right| \tag{5.7}$$

This equation is plotted in figure 5.3(N=13.5, $k = 1.38 \cdot 10^{-23}$, T=290K, $V_{in} = 1$) which shows the input impedance increases when the voltage transfer is closer to 1. This result is an important intermediate trade-off, which states that the voltage range should be as large as possible to drive the capacitor to get the lowest power consumption.

However, it does assume the input voltage is 1 volt, which can be slightly higher, for example 1.1 V. This allows α_1 to be smaller than 1 while the voltage across the capacitor is 1 V. This will result in a higher input impedance of the track and hold at the cost of some extra gain and linearity.

Power consumption

The power consumption of a single track and hold when it is tracking can be easily derived assuming a sinusoid, with amplitude(V_{in}) and the input impedance(Z_{in}). The power consumption is given by equation 5.8.

$$P_{TH} = \frac{(\frac{V_{in}}{\sqrt{2}})^2}{Z_{in}} \tag{5.8}$$

The power consumption when in hold mode is negligible.

Noise factor

The on-resistance of the switch can be used to determine the amount of thermal noise, which allows the derivation of a noise factor of the track and hold, given by equation 5.9.

$$F = 1 + \frac{4kTR_{on}}{4kTR_s} \tag{5.9}$$

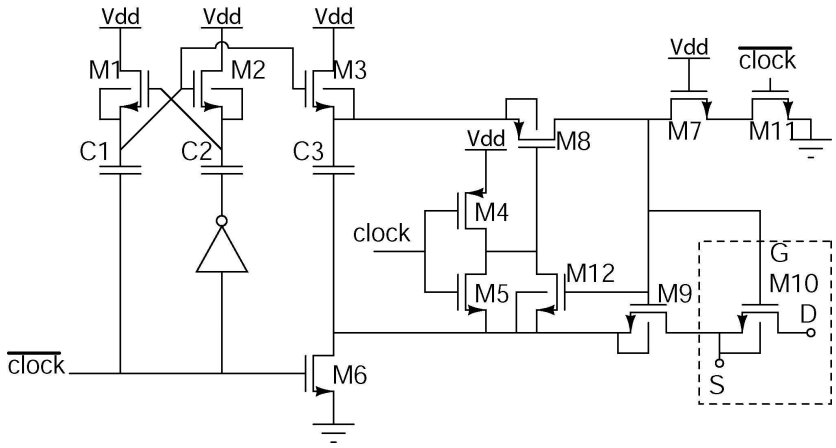


Figure 5.4: Bootstrapped switch

Frequency response

The bandwidth of the track and hold is determined by the on-resistance of the switch and the size of the sampling capacitor. This results in equation 5.10.

$$BW_{TH} = \frac{1}{2\pi R_{switch} C_{sample}} \tag{5.10}$$

5.3.5 Switch driver

The bootstrapping of a switch is performed using the circuitry shown in figure 5.4, which was derived from literature[16]. The on-resistance of switch M11 is not dependent on the input signal, because the voltage across gate-source of the transistor is always 1.2 V, when the clock is high. When the clock is low, the switch is turned off. This entire circuit is designed in such a way that the voltage across any two terminals does not exceed 1.2V. For this reason, transistors M1,M2,M3,M9,M10 and M12 have the bulk terminal tied to the source terminal.

The circuit is simplified by replacing the transistors with switches which are either on or off, which is a valid assumption, because all the transistors in the circuit are used in this way. First the situation when the clock is high is illustrated in figure 5.5a) and the startup effects are gone. The capacitors C1, C2 and C3 are charged to Vdd, and the input signal is connected to the bottom terminal of capacitor C3. The top terminal of C3 is connected to the gate of transistor M10, which now has a voltage of the input signal raised by Vdd.

When the clock becomes low, transistor M11 connects the gate of M10 to ground, closing the switch. Transistors M8 and M9 disconnect the capacitor C3 from the transistor M10. Also, transistor M3 and M6 start charging capacitor C3 to Vdd again.

5.3.6 Circuit design track and hold

The first step in the design of the track and hold is the size of the capacitor, because it has influence on different parameters of the design of the receiver. The size of the capacitor is

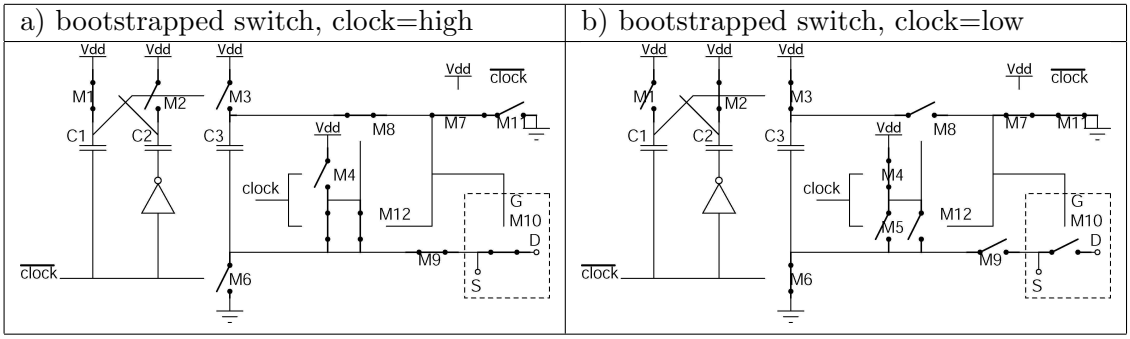


Figure 5.5: bootstrapped switch states

Track and Hold			
f_s	accuracy	C_{sample}	R_{on}
80 MHz	13.5 bits	2.17 pF	3 Ω
200 MHz	13 bits	1.09 pF	6 Ω
400 MHz	12.5 bits	543 fF	12 Ω
600 MHz	12 bits	271 fF	24 Ω
1200 MHz	11.5 bits	136 fF	48 Ω

Table 5.2: Design choices capacitor size and switch resistance

determined by the accuracy of the ADC(equation 4.16 and 5.6) and the desire to minimize the power consumption(equation 5.8). Because the quantization noise is dependent on the sampling frequency, the capacitor size is given for different sampling speeds in table 5.2. These sampling frequencies are chosen in such a way that the subsampling ratio will be even and an integer(to profit from the oversampling). The voltage loss in transfer function α is chosen to be 1 decibel, resulting in a transfer function of 1 because of the slightly higher input voltage). An important trade-off is made here, because this also determines the bandwidth of the track and hold and thus the noise folding factor. A larger on-resistance might seem a way to get less noise folding, but this would also require a larger capacitance to meet the accuracy requirement, cancelling this advantage. Once the voltage loss is determined, the on-resistance can be derived.

With these numbers, the important figures for the track and hold can be derived, which is done in table 5.3.

The estimation for the width of the transistor is shown in table 5.4 using equation 5.11 where the parameters are given in appendix C.

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L_{min}} (V_{dd} - V_{TH})} \tag{5.11}$$

5.3.7 Circuit design switch driver

The bootstrapping circuit needs to be adjusted to accommodate the 2.48 GHz input signal but is also dependent on the speed of the clocking signal. First the circuit using a sampling

Track and Hold				
f_s	Z_{in}	Power	Noise factor	Bandwidth
80 MHz	33 Ω	3.8 mW	1.06	24.4 GHz
200 MHz	67 Ω	1.9 mW	1.12	24.3 GHz
400 MHz	133 Ω	0.9 mW	1.24	24.4 GHz
800 MHz	267 Ω	0.5 mW	1.48	24.5 GHz
1200 MHz	534 Ω	0.2 mW	1.96	24.4 GHz

Table 5.3: Hand-calculated Performance figures track and hold

Track and Hold	
f_s	W
80 MHz	61.1
200 MHz	30.6
400 MHz	15.3
600 MHz	7.6
1200 MHz	3.8

Table 5.4: width estimation transistor

speed of 80 MHz is designed. Capacitor C1 and C2 are chosen to be 100 fF. The size of C3 is 500 fF which is sufficient to drive the switch M10 and all the parasitic capacitances from other transistors. This capacitor is charged during the hold phase by transistors M3 and M6, which requires some minor adjustment in the scaling. Transistors M8 and M9 have to scaled to ensure the voltage swing of the bootstrapping circuit. Transistors M7 and M11 also need to be scaled depending on the size of M10, because they determine how fast switch M10 turns off. All other transistors are minimum size switches. When the sampling speed is increased, the sampling switch will become smaller, which makes it possible to scale capacitor C3 and transistors M7 and M11 down.

5.4 LNAs

5.4.1 Introduction

The design process of the LNA will be illustrated using equations for hand calculations for important specifications. Because the LNA's in the receiver are very similar, the design process will not be repeated for each LNA. First the general design goals are stated. A topology for the LNA is chosen, based on the design goals. Finally, the performance can be calculated using the equations that are derived in section 5.4.4.

5.4.2 Design goals

For convenience, the specifications for the LNA's are repeated in tables 5.5 and 5.6. The first LNA needs to provide 50 Ω matching, but the second LNA does not. Both LNA need

LNA 1	
Parameter	Value
f_c	2.44 GHz
Bandwidth	80 MHz
NF	$<$ 1.0 dB
Voltage gain	19.1 dB
IIP_3	$>$ 0 dBm
Input impedance	50 Ω

Table 5.5: Performance specifications LNA 1

LNA 2	
Parameter	Value
f_c	2.44 GHz
NF	$<$ 5.0 dB
Voltage gain	16.1 dB
IIP_3	$>$ 0 dBm

Table 5.6: Performance specifications LNA 2

to be narrowband to limit the noise folding effect. However, the noise folding effect is not taken into account by the specified noise figure. The noise figure with noise folding can only be determined when the sampling operation is included, which requires all the system blocks(LNA, buffer and track and hold). The load of the first LNA is the second LNA, while the load of the second LNA is the buffer.

5.4.3 Topology

The topology that is chosen is the common source, with a cascode to improve the voltage gain. This topology can provide sufficient gain, can be implemented with low power and is reasonably linear. Furthermore, a LC tank can be added without much problems, which will allow the wanted bandpass frequency response. The cascoded common source topology with a LC tank is illustrated in figure 5.6. The resistor R_d represents the resistance of inductor L_d.

5.4.4 LNA calculations

Input impedance

The 50 Ω matching can be attained by using inductive source degeneration, which allows for lower noise than adding a 50 Ω resistor or getting the correct input impedance with transistor M1. The inductive degeneration is achieved by adding inductor L_s given in figure 5.6. However, L_s determines both the input impedance and the resonance frequency. This can be solved by adding inductor L_g. Finally, capacitor C_{gs} is used to control the capacitance between gate and source of transistor M1.

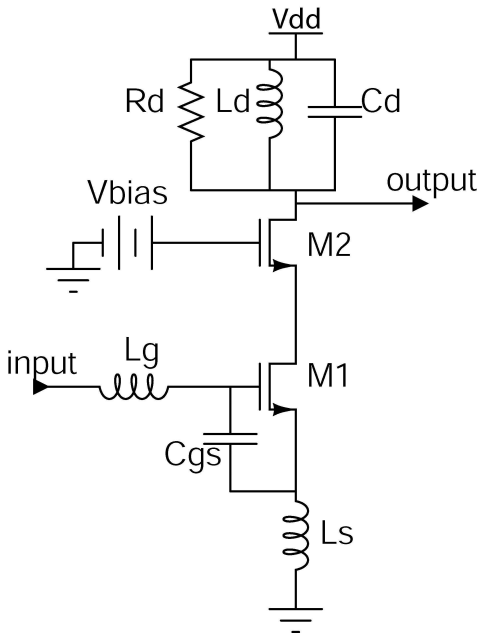


Figure 5.6: Cascoded common source LNA with LC tank

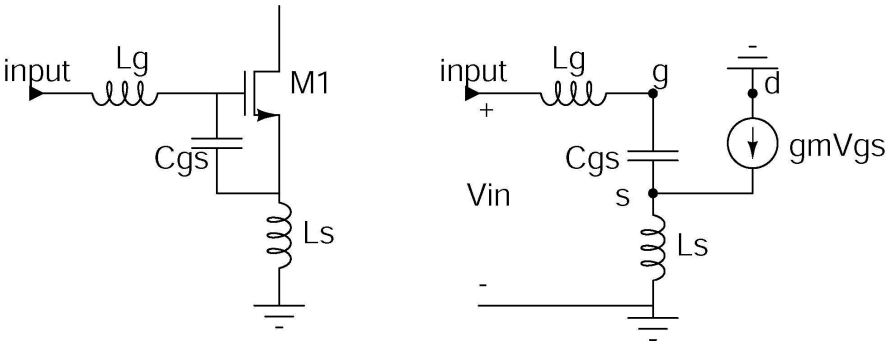


Figure 5.7: Equivalent circuit for calculation input impedance

Calculating the input impedance can be done using the equivalent circuit as shown in figure 5.7, where the relation between the input voltage and current is given by equation 5.12. When this is rewritten, the input impedance is given by equation 5.13.

$$V_{in} = \frac{I_{in}}{j\omega C_{gs}} + (g_m \frac{I_{in}}{j\omega C_{gs}}) j\omega L_s + I_{in} j\omega (L_s + L_g) \tag{5.12}$$

$$Z_{in} = \frac{1}{j\omega C_{gs}} + g_m \frac{L_s}{C_{gs}} + j\omega (L_s + L_g) \tag{5.13}$$

The input impedance can now be calculated for every input frequency, but the minimum of this function is when the resonance frequency of the LC tank at the input(equation 5.24) is chosen as the input frequency. The imaginary part of the input impedance becomes zero, which results in equation 5.14.

$$Z_{in} = g_m \frac{L_s}{C_{gs}} \tag{5.14}$$

Voltage gain

The voltage gain of the LNA depends on both the transconductance and the output impedance of the circuit. First, the transconductance is determined, taking into account the input LC tank. The quality factor(Q) is determined by the input impedance of the LNA and the source impedance(R_s), as shown in equation 5.15.

$$Q_1 = \frac{1}{\omega_0 C_{gs} R_1} \tag{5.15}$$

where

$$R_1 = R_s + z_{in} \tag{5.16}$$

When the tank is in resonance, the input voltage over the capacitance is increased by Q, due to this resonance. The total transconductance(G_m) of the tank and transistor M_1 can now be described by equation 5.17.

$$G_m = \frac{I_d}{v_{in}} = \frac{Q_1 \cdot v_{in} \cdot g_{m,M_1}}{v_{in}} = Q_1 \cdot g_{m,M1} = \frac{g_{m,M_1}}{\omega_0 C_{gs} R_1} \tag{5.17}$$

The output impedance is the second part of the voltage gain that needs to be calculated. The output impedance of the LNA can be described with equation 5.18.

$$Z_{out} = R_d // Z_{casc} \tag{5.18}$$

where

$$Z_{casc} = (1 + (g_{m,M_2} + g_{mb,M_2}) r_{0,M_2}) r_{0,M_1} + r_{0,M_2} \tag{5.19}$$

Finally, the voltage gain is given in equation 5.20.

$$A_v = G_m Z_{out} \tag{5.20}$$

Noise factor

The noise factor of the LNA can be determined by considering all the noise sources and calculating their contribution of noise back to input. This can be done for a specific frequency(spot noise) or for a frequency range(integrated noise). However, calculating the contribution of every noise source is difficult, so only the most significant error sources are taken into account. The noise from transistors M_1 and M_2 and resistor R_d seem most important. However, the contribution of the cascode transistor to both gain and noise are small, so this noise source can actually be neglected[10]. Different models exist for the noise contribution of the degenerated M_1, but based on other research at the university[19], a model from K.Shaeffer and L.Belostotski seems to be best suited for hand calculations. The resulting spot noise referred back to the input is described by equation 5.21, where k is the Boltzman constant and T is the temperature. The assumption is made that there is no gate induced noise($\delta = 0$) and that g_{d0} is equal to g_m.

$$\overline{v_{n,M_1}^2} = \frac{4kT\gamma g_{d0} R_s^2 \omega^2 C_{gs}^2}{(g_{m,M_1})^2} + \frac{4kT\delta}{5g_{d0}} \tag{5.21}$$

The contribution of noise referred to the input from the resistance R_d can be calculated using equation 5.22.

$$\overline{v_{n,R_d}^2} = \frac{4kTR_d}{(A_v/2)^2} \tag{5.22}$$

The total noise factor with the mentioned assumptions is then given by equation 5.23.

$$F = 1 + \frac{\gamma g_{m,M_1} R_s^2 \omega^2 C_{gs}^2}{(g_{m,M_1})^2 R_s} + \frac{4kTR_d}{(A_v/2)^2} \frac{1}{4kTR_s} \tag{5.23}$$

Frequency response

The narrowband character of the LNA can be described with equations for the LC tank at the input and output of the LNA. The input tank has a resonance frequency described by equation 5.24, a Q factor given by equation 5.25 and a bandwidth(in rad/s) given by equation 5.26.

$$\omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \tag{5.24}$$

$$Q_1 = \frac{1}{\omega_0 C_{gs}(50 + g_{m,M_1}\frac{L_s}{C_{gs}})} \tag{5.25}$$

$$BW_1 = \omega_0^2 C_{gs}(50 + g_{m,M_1}\frac{L_s}{C_{gs}}) \tag{5.26}$$

The output tank can be described in a similar way, given by equations 5.27 through 5.29.

$$\omega_0 = \frac{1}{\sqrt{L_d C_d}} \tag{5.27}$$

$$Q_2 = \frac{R_d}{\omega_0 L_d} \tag{5.28}$$

$$BW_2 = \frac{\omega_0^2 L_d}{R_d} \tag{5.29}$$

5.4.5 Circuit design LNA 1

Biasing is the first step in the LNA design, which is chosen to be 0.6 V for M1 and 1.2 V for M2, which puts both transistors in the saturation region. The quality factors of on-chip inductors is quite low, so a Q of 13 is assumed. With a 2.05 nH inductor and a input frequency of 2.44 GHz, equation 5.28 gives a resistance of 400 Ω. Equation 5.27 can be used to derive a capacitance of 2 pF. To get a reasonable power consumption with sufficient gain the transconductance is chosen to be 12 mS(which is achieved for a W/L value of 40/0.06). Equation 5.17 shows that for smaller C_{gs} the voltage gain is increased, but the inductor L_s need to be decreased to get 50 Ω matching. C_{gs} is chosen to be 325 fF, which results in a voltage gain of about 20 dB. To get the required 50 Ω matching, inductor L_s is chosen to be 1.4 nH. Equation 5.24 gives a value of 9.6 nH for inductor L_g. with these numbers and assuming $g_{d0} = g_m$ the noise factor can be derived with equation 5.23. This gives a noise factor of 1.4.

5.4.6 Circuit design LNA 2

The second LNA does not require input matching, which makes the design more straightforward. Once again, the transistors are biased at 0.6 V and 1.2 V. A transconductancce of 16 mS is used and with R_d of 400 Ω, this results in a gain of 16 dB. Inductor L_d is chosen to be 2.05 nH, but capacitance C_d is chosen smaller, as 1.8 pF, to compensate for the large coupling capacitor. Finally, the noise factor is once again derived using equation 5.23, but C_gs is now chosen as 25 fF, which results in a noise factor of 2.3.

5.5 Buffer

5.5.1 Introduction

The design of the buffer depends on the previous stage(LNA) and the next stage(Track and Hold). First the design goals for the buffer are repeated, after which two possible topologies are presented. To gain insight in the design parameters, some hand calculations are performed. Finally the circuit design is presented.

Buffer	
Parameter	Value
Voltage gain	0 dB
NF	< 5 dB
IIP_3	> 10 dBm

Table 5.7: Performance specifications Buffer

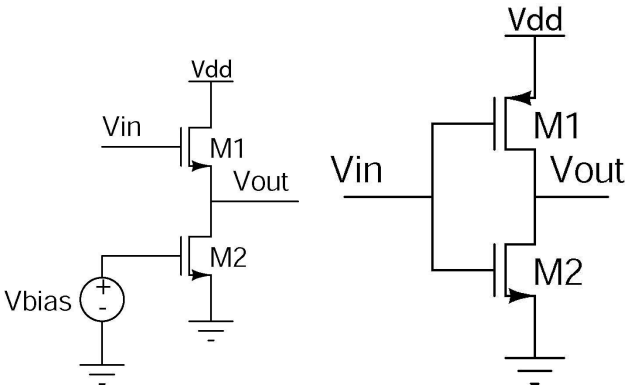


Figure 5.8: left) Source follower buffer topology right) Inverter buffer topology

5.5.2 Design goals

The buffer is used to prevent gain degredation due to the low ohmic load of the track and hold. The voltage transfer function should be close to one and the linearity should be reasonably high.

5.5.3 Topology

There are two buffer topologies that have been investigated. First, the source follower topology shown in figure 5.8. The advantage of this topology is the voltage shift that is performed, which allows the second LNA to be directly connected to the buffer. However, this topology suffers from non-linearities due to body effect, the output voltage swing is limited and the voltage gain will always be smaller than one.

Another topology is the inverter topology, which is illustrated in figure 5.8. The advantage of this circuit is that the load is driven by the nmos and pmos, which allows a very good output voltage swing. Furthermore, the voltage gain can be chosen arbitrarily, although this comes at the cost of power consumption. However, this buffer cannot be directly connected to the LNA, due to the high common mode level.

The inverter buffer topology is chosen because low power consumption and good output voltage swing are essential.

5.5.4 Buffer calculations

Output impedance

The output impedance of the buffer is defined by equation 5.30.

$$R_{out} = R_{o,M1}//R_{o,M2}//R_{load} \tag{5.30}$$

However, when a low ohmic load is added to the buffer, it will dominate the output impedance.

Voltage transfer function

The buffer will be designed in such a way that the nmos and pmos provide similar transconductance. The voltage gain of the circuit can be calculated when the buffer is loaded, which is given by equation 5.31.

$$A_v = R_{out} g_m \tag{5.31}$$

Power consumption

The power consumption is dependent on the output impedance of the buffer and the required voltage gain. When the voltage gain is chosen to be 1, the g_m has to be about $\frac{1}{R_{out}}$. From this requirement, the current can be calculated, using equation 5.32.

$$\frac{1}{R_{out}} = g_m = \frac{2I_d}{V_{gs} - V_{th}} \tag{5.32}$$

$$I_d = \frac{g_m(V_{gs} - V_{th})}{2} \tag{5.33}$$

$$P_{Buffer} = V_{dd} * I_d \tag{5.34}$$

Noise factor

The two transistors, M1 and M2, are the two dominant noise sources, which is shown in figure 5.9.

The noise contribution for M1 and M2 can be given with equation 5.35

$$\overline{v_{n,M_1}^2} = \overline{v_{n,M_2}^2} = 4kT\gamma g_m R_{out}^2 \tag{5.35}$$

This can be transformed to a noise factor with:

$$F = 1 + 2 \cdot \frac{4kT\gamma g_m R_{out}^2}{(A_v/2)^2} \frac{1}{4kTR_s} \tag{5.36}$$

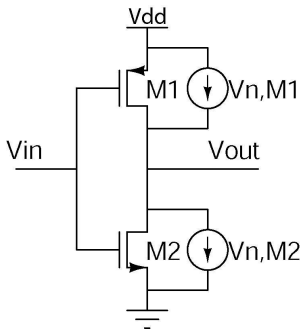


Figure 5.9: Noise sources buffer

Buffer				
f_s	R_{out}	g_m	Noise factor	Power
80 MHz	15.5 Ω	64.5 mS	1.10	10 mW
200 MHz	33 Ω	30.3 mS	1.22	4.5 mW
400 MHz	67 Ω	14.9 mS	1.46	2.2 mW
600 MHz	133 Ω	7.5 mS	1.88	1.1 mW
1200 MHz	267 Ω	3.7 mS	2.76	0.6 mW

Table 5.8: Hand-calculated performance figures Buffer

5.5.5 Circuit design buffer

The buffer is loaded by two track and holds(I and Q channel) which largely determines the output impedance of the buffer. With this in mind, the transconductance of the buffer can be derived. The power consumption and noise factor are calculated using the transconductance.

5.6 Clock driver

5.6.1 Introduction

The clock driver is a difficult block to design, because simulations cannot predict the actual performance. However, based on handcalculations, reasonable design choices are made.

5.6.2 Design goals

The clocking signal that is used for the track and hold and ADC, must be distributed over the chip, which is done using the clock driver. Because bootstrapping is used, the clock driver drives the bootstrapping circuit, while the bootstrapping circuit drives the track and hold switch.

Clock		Inverted clock	
Description	Estimated load	Description	Estimated load
2x M4	2 fF	2x M6	20 fF
2x M5	2 fF	2x M11	20 fF
		2x inverter	2 fF
wire	100 fF	wire	100 fF
Total	104 fF		144 fF

Table 5.9: Clock driver loads

5.6.3 Topology

The inverter topology is used once again, shown in figure 5.8, because a large voltage swing is important for clock signals. The steepness of the clock transitions is determined by the power consumption of the clock driver and the capacitance that has to be driven.

When designing the clock driver, it has to be taken into account that wires have parasitic capacitances. It is derived from literature that the wires with a length of 1 mm, will have a parasitic capacitance of 200 fF[20]. The assumption is made 1/2 mm wire is required from the buffer to the track and hold.

5.6.4 Clock driver calculations

Capacitances

The capacitance that has to be driven can be derived from the bootstrapping circuit. However, the bootstrapping circuit will need to be adjusted for different switch sizes(due to different sampling frequencies). This could affect the parasitic capacitance that the clock driver has to drive. Also, for higher sampling frequency, the number of clock transitions increases, which requires more current.

The load that needs to be driven is estimated for both the regular clock and the inverted clock in table 5.9.

Power consumption

The power consumption depends on the load that needs to be driven and the slopes of the clock transitions that are necessary. steeper slopes result in better resistivity against jitter effects. However, it is not straightforward to calculate the slope needed and derive the needed power consumption. This will be derived using simulation results.

Noise

Noise added by the buffer will contribute to jitter, but this is not the most contributing noise source. Mismatch between two clock buffers can have much more impact, because this will create a timing error in the differential track and hold circuit. This could be minimized with proper layout of the clock driver.

f_s	ENOB	power/conversion	Power
80M	13.5	53.3 pJ	4.26 mW
200M	13.0	37.7 pJ	7.54 mW
400M	12.5	3.47 nJ	1.39 W
600M	12.0	2.46 nJ	1.47 W
1200M	11.5	1.74 nJ	2.1 W

Table 5.10: Power consumption ADC estimation

5.7 ADC

5.7.1 Introduction

ADC's take considerable time to design, but perform a relative straightforward operation. It converts a value from the analog domain to the digital domain, with a certain accuracy and sampling frequency. An actual design of the ADC would only contribute to knowledge of the design of the receiver concerning power consumption. However, using the figure of merit of state of the art ADC's, the power consumption can be estimated. With this in mind, the ADC will not be designed to save time and effort and the figure of merit of 2 ADC's will be used to get a reasonable estimation of the power consumption.

5.7.2 Power consumption

To determine the power consumption of the ADC implementation, two possible implementations are used. One implementation is designed to be ultra low power[18], resulting in a figure of merit of 4,6 fJ/conversion-step. The second implementation is designed to have a high conversion speed and low power[21], resulting in a figure of merit of 0.6 pJ/conversion-step. Using the effective number of bits(ENOB), the power per conversion can be calculated. The sampling frequency can also be described as the number of conversions per second, resulting in power per second. The resulting numbers are calculated in table 5.10. The first implementation can only be extrapolated to about 200 MHz, because the speed will have a significant impact on the power consumption. For the higher sampling speeds, the second implementation needs to be extrapolated.

5.8 Summary

The transistor level design of the track and hold, buffer, LNA and clock buffer are discussed. An estimation is made for the power consumption of the ADC.

Chapter 6

Simulation results

6.1 Introduction

The first part of this chapter describes the simulations to verify the calculated performance for the individual blocks of the receiver. First the clock driver is verified, after which the track and hold, buffer, first LNA and second LNA are discussed. The second part goes into the verification of the performance limiting mechanisms and determining the performance of the receiver. These results are shortly discussed. Finally, a comparison is made with a similar receiver design.

Track and Hold times			
Clock frequency	time in one period	track time	hold time
80 MHz	12.5 ns	1.5625 ns	10.9375 ns
200 MHz	5 ns	1.5625 ns	3.4375 ns
400 MHz	2.5 ns	1.5625 ns	937.5 ps
600 MHz	1.667 ns	833 ps	833 ps
1200 MHz	833 ps	416 ps	416 ps

Table 6.1: Track and hold times

6.2 Receiver blocks

6.2.1 Clock driver

The clock driver needs to supply the correct clock signals for the track and hold. Because tracking will cost the most power, the track mode will be as short as possible. However, shorter track times will result in non-linearity, which limits the increase of clock frequency. It is determined from simulations, 1.5 ns is required for the circuit to be sufficiently linear that it meets Bluetooth specifications. This results in the track and hold times given in table 6.1. The clock signals are shown in figure 6.1 and 6.2 for the 80 MHz clock and the 1200 MHz clock.

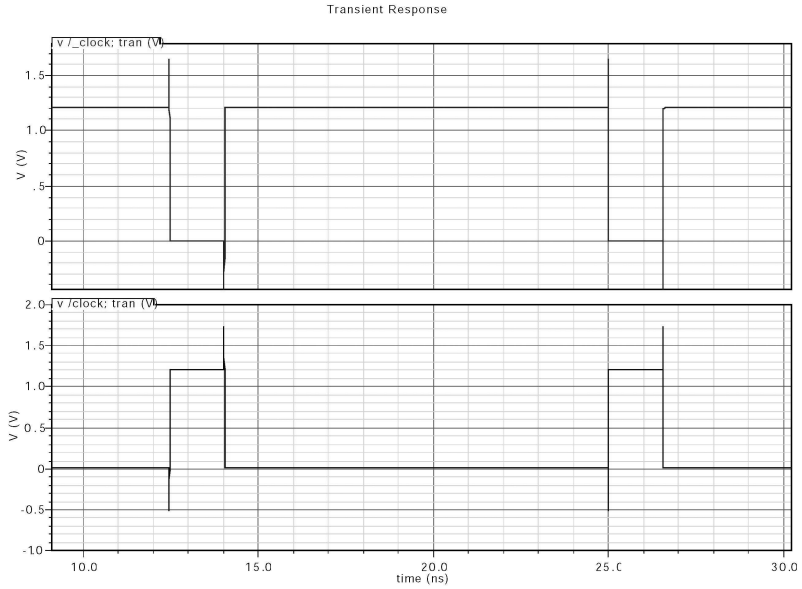


Figure 6.1: Clock driver = 80 MHz

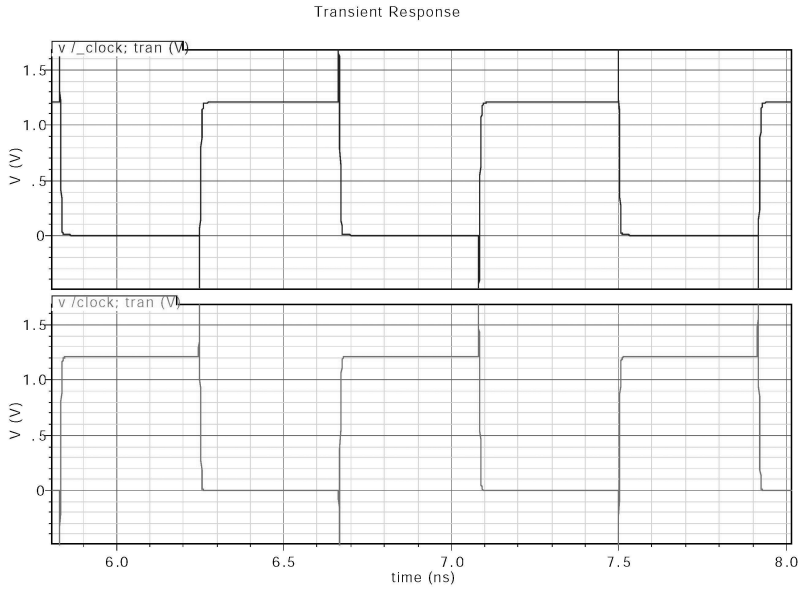


Figure 6.2: Clock driver = 1200 MHz

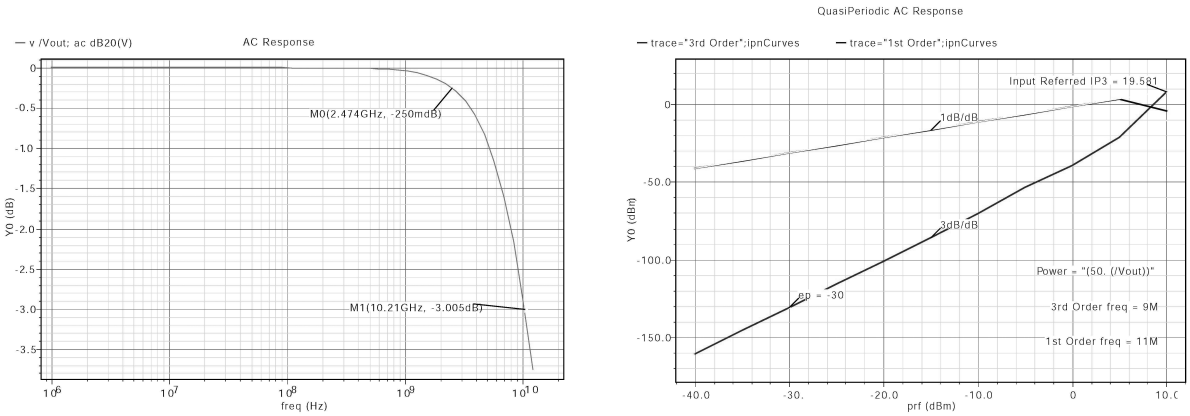


Figure 6.3: Transfer function and IIP_3 Track and Hold $f_s = 80$ MHz

6.2.2 Track and hold

The track and hold circuit is realized according to the specifications in chapter 5. However, when the circuit is simulated, there is significant feedthrough of the amplified input signal behind the switch during hold mode. This is the result of connecting the input signal to the bulk contact. This is solved by connecting the bulk to the input signal during track mode and connecting the bulk to ground during hold mode.

Simulated figures track and Hold					
Clock frequency	Transfer function	folding bandwidth	Noise figure	IIP_3	Power
80 MHz	-0.25 dB	10.2 GHz	0.48 dB	19.6	1.3 mW
200 MHz	-0.24 dB	10.3 GHz	0.90 dB	19.9	2.2 mW
400 MHz	-0.25 dB	10.0 GHz	1.70 dB	15.0	3.1 mW
600 MHz	-0.25 dB	10.0 GHz	2.89 dB	15.8	3.8 mW
1200 MHz	-0.25 dB	10.0 GHz	4.62 dB	18.5	5.4 mW

Hand-calculated figures track and Hold				
f_s	Transfer function	folding Bandwidth	Noise figure	Power
80 MHz	-1 dB	24.4 GHz	0.25 dB	3.8 mW
200 MHz	-1 dB	24.3 GHz	0.49 dB	1.9 mW
400 MHz	-1 dB	24.4 GHz	0.93 dB	0.9 mW
600 MHz	-1 dB	24.5 GHz	1.70 dB	0.5 mW
1200 MHz	-1 dB	24.4 GHz	2.92 dB	0.2 mW

Table 6.2: Performance figures track and hold

The bootstrapping circuit capacitor C3 is reduced to 400 fF for the clock frequencies 600 MHz and 1200 MHz, which is necessary due to the shorter charge times.

The circuit is now simulated, deriving the noise figure, transfer function, linearity and power consumption for different clock frequencies. Linearity and gain measurements with a clock

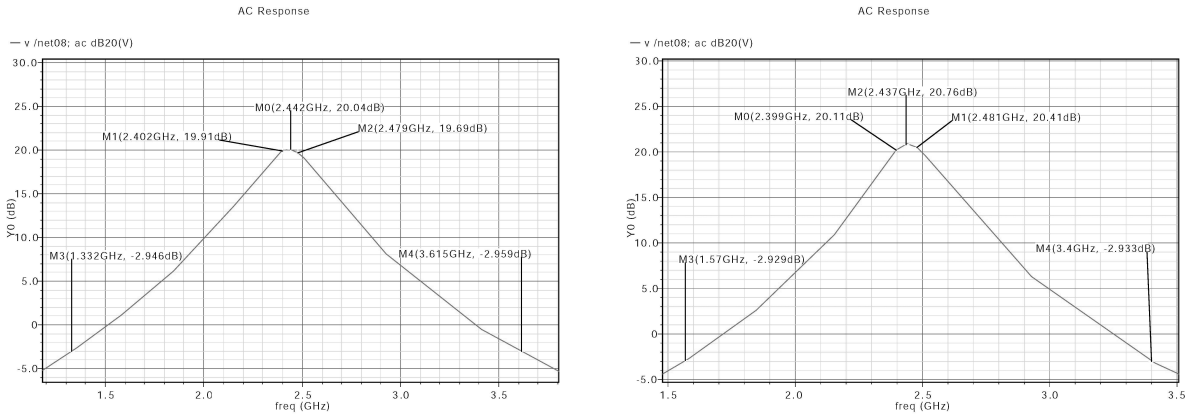


Figure 6.4: gain and bandwidth LNA1 left)Q=13 right)Q=26

frequency of 80 MHz are shown in figure 6.3, while the results for the other clock frequencies are shown in table 6.2.

The noise figures are all slightly higher than the hand calculations, which might be the result of a higher on-resistance. The bandwidth of the track and hold is shown in figure 6.3 to be 10.2 GHz, which is generally maintained over the different sampling frequencies. This bandwidth is also lower than the hand-calculated value, which confirms the higher on-resistance of the switch. The transfer function is better than expected, with only a loss of 0.25 dB of signal across the switch. Because the bandwidth is quite low, the noise folding effect will be reduced. The linearity of the track and hold stays within the specifications for all clock frequencies. The power consumption is simulated including the clock drivers circuitry. This results in the higher power consumption for higher clock frequencies, because the number of clock transitions increases, which requires more power. However, the handcalculations do not include the clock drivers, but gives a higher estimated power consumption.

6.2.3 LNA 1

Simulated figures LNA1					
Q	Gain	FoldingBW	Noise figure	Linearity(IIP_3)	Power
13	20.04	2.28 GHz	0.97 dB	6.62	1.34 mW
26	20.76	1.83 GHz	1.14 dB	4.81	0.88 mW

Hand-calculated figures LNA1				
Q	Gain	FoldingBW	Noise figure	Power
13	20.0	2.64 GHz	1.46 dB	2.2 mW
26	20.0	1.32 GHz	2.43 dB	1.4 mW

Table 6.3: Performance figures LNA1

The design of the LNA is done using two different quality factors(Q) for the inductor L_d,

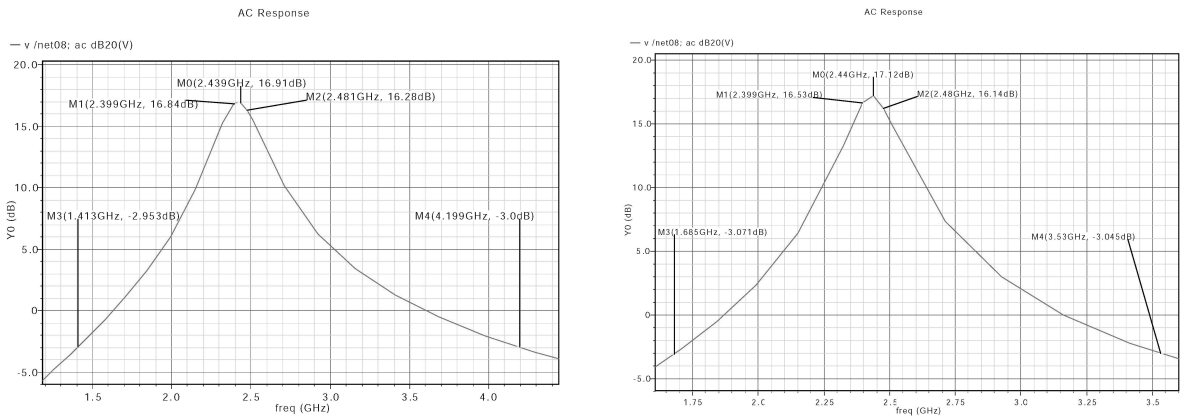


Figure 6.5: gain and bandwidth LNA2 80 MHz left)Q=13 right)Q=26

which are 13 and 26. This is done to determine how the Q of the LNA has impact on the noise figure of the receiver. A higher quality factor will decrease the amount of noise folding but will also make the resonance frequency more sensitive to mismatch and loading effects. A Q of 26 might not be possible without Q-enhancement techniques, but is purely to validate the model of the LNA for the noisefolding.

The gain of the LNA is set to approximately 20 dB, although the gain of the high-Q LNA is slightly higher. This higher gain results in a higher folding bandwidth. The hand-calculated folding Bandwidth for the low-Q is 16 % higher as the simulated folding bandwidth. However, the hand-calculated high-Q LNA folding bandwidth is about 28 % smaller as the simulated folding bandwidth. When the gain of the hand-calculated value is adjusted, this reduces to 21 %. The handcalculations give higher noises figure than the simulations. This might be improved by using a more accurate model for the LNA.

6.2.4 LNA 2

The design of the second LNA has to take into account the load of the buffer. Because this load varies for different sampling frequencies, the LNA has to be optimized for each clock frequency. The load will be higher for smaller sample frequencies, which will require additional power, to get sufficient voltage gain. The quality factor is also varied in this design.

Because the load for each configuration is different, the folding bandwidth is also altered. When the load is higher, the folding bandwidth is increased. This might be the result of the output impedance that is reduced, and thus reduces the quality factor. Higher quality factors degrade more when the LNA is loaded, which strengthens this point. Comparing the hand-calculated folding bandwidth to the simulations of the low Q 80 MHz LNA, the hand-calculated value is 40 % lower. For the high Q, this is 55 %. However, when the hand-calculated values are compared to the simulations of the low Q 600 and 1200 MHz LNA, the error in the model is much smaller, 19 %. For the high Q the error in the model is 22 %. From these results, it can be concluded that loading should be included in the modeling of the folding bandwidth.

Simulated figures LNA2						
Clock	Q	Gain	Folding BW	Noise figure	IIP_3	Power
80 MHz	13	16.9 dB	2.79 GHz	3.83 dB	3.11	1.9 mW
80 MHz	26	17.1 dB	1.84 GHz	4.88 dB	5.10	1.2 mW
200 MHz	13	17.1 dB	2.34 GHz	4.39 dB	3.00	1.56 mW
200 MHz	26	17.2 dB	1.34 GHz	6.00 dB	4.61	0.87 mW
400 MHz	13	16.9 dB	2.10 GHz	4.77 dB	3.29	1.38 mW
400 MHz	26	17.4 dB	1.18 GHz	6.46 dB	4.09	0.76 mW
600 MHz	13	17.0 dB	2.06 GHz	4.76 dB	7.00	1.38 mW
600 MHz	26	17.1 dB	1.07 GHz	6.85 dB	5.44	0.69 mW
1200 MHz	13	16.9 dB	2.06 GHz	4.76 dB	8.48	1.38 mW
1200 MHz	26	17.0 dB	1.07 GHz	6.84 dB	7.64	0.69 mW

Hand-calculated figures LNA2				
Q	Gain	Folding BW	Noise figure	Power
13	16 dB	1.66 GHz	3.6 dB	2.4 mW
26	16 dB	0.83 GHz	5.5 dB	1.9 mW

Table 6.4: Performance figures LNA2

6.2.5 Buffer

The signal from the LNA does not have the correct DC voltage, which would result in clipping. A coupling capacitor is added to remove the DC voltage and the buffer is biased at the correct DC voltage(600 mV). The buffer design is somewhat relaxed due to the higher on-resistance of the switch in the track and hold. This results in a different load for the buffer, resulting in less power consumption. The transient behavior is used to determine the correct g_m of the transistors. The buffer is then simulated and the performance figures are determined.

The buffer still needs to amplify the signal significantly to get the desired transient behavior, which can be seen for the gain in the transfer function. For higher clock frequencies this effect becomes more severe. The noise figures of the simulations is generally higher than handcalculations predicted. The noise factor is dependent on the g_m of the transistors and the output resistance and voltage gain of the buffer. However, the voltage gain of the buffer depends on the g_m and the output resistance. When this is evaluated in equation 5.36, the noise figure has an inverse linear relationship to the g_m of the transistors.

6.3 Simulation experiments

6.3.1 Introduction

In this section the total circuit will be analyzed with a number of predetermined experiments. The goal of these experiments is to determine whether different configurations of the receiver meet the specifications. Another goal is to verify the handcalculation models and determine their accuracy. The different configurations of the receiver consist of a varying sample rate

Simulated figures Buffer				
Clock frequency	Transfer function	Noise figure	IIP_3	Power
80 MHz	1.41 dB	0.75 dB	14.99	6.4 mW
200 MHz	2.26 dB	1.65 dB	14.72	3.1 mW
400 MHz	3.02 dB	1.97 dB	13.75	1.6 mW
600 MHz	3.73 dB	3.05 dB	15.00	0.9 mW
1200 MHz	6.88 dB	3.48 dB	10.81	0.7 mW

Hand-calculated figures Buffer			
Clock frequency	Transfer function	Noise figure	Power
80 MHz	0 dB	0.41 dB	10 mW
200 MHz	0 dB	0.86 dB	4.5 mW
400 MHz	0 dB	1.64 dB	2.2 mW
600 MHz	0 dB	2.74 dB	1.1 mW
1200 MHz	0 dB	4.41 dB	0.6 mW

Table 6.5: Performance figures Buffers

and a high and low quality factor for the inductors in the LNA's. First, the hand-calculated IIP_3 will be verified with simulations for various input signal powers. The second experiment will be to determine the noise figure of the circuit taking into account the noise folding. The quantization noise due to sampling will be determined next. Out of band interferers need to be rejected by the receiver, which is investigated in section 6.3.7. The image rejection realizable with second-order sampling is simulated and the effect of jitter is investigated in the last section.

6.3.2 Linearity

The linearity of the circuit is determined using QPSS simulations with varying powers for the input signal. This is done for different configurations of the receiver, which are sampling frequencies from 80 MHz to 1200 MHz and two quality factors for the inductor in the LNA's, which are 13 and 26.

The simulated IIP_3 of each block is used to calculate the IIP_3 of the total receiver, which will be referred to as hand-calculated IIP_3. After the first series of simulations, only the 80 MHz configuration matched reasonably with the hand-calculated IIP_3. When the track time of the other configurations was increased, their linearity increased. Although this solution increased the linearity, which is shown in table 6.6, the higher sample frequency configurations still do not match the hand-calculated IIP_3 and do not meet the specifications. There are many possible explanations for this problem:

1. The QPSS simulations are not accurate enough

2. The individual blocks are linear enough by themself, but together additional non-linearity might be introduced

Simulated IIP_3 total circuit - Q=13					
Clock frequency	80 MHz	200 MHz	400 MHz	600 MHz	1200 MHz
IIP_3	-9.64	-12.67	-23.02	-20.12	-23.2

Hand-calculated IIP_3 total circuit - Q=13					
Clock frequency	80 MHz	200 MHz	400 MHz	600 MHz	1200 MHz
IIP_3	-12.3	-10.4	-11.3	-8.2	-8.3

Simulated IIP_3 total circuit - Q=26					
Clock frequency	80 MHz	200 MHz	400 MHz	600 MHz	1200 MHz
IIP_3	-9.69	-13.48	-22.8	-20.9	-23.6

Hand-calculated IIP_3 total circuit - Q=26					
Clock frequency	80 MHz	200 MHz	400 MHz	600 MHz	1200 MHz
IIP_3	-13.0	-10.3	-11.3	-8.4	-8.4

Table 6.6: Linearity total circuit

3. In the transition between the unloaded and the loaded state, the buffer cannot provide enough linearity fast enough

4. In the transition between the off and the on state, the bootstrapped switch cannot provide enough linearity fast enough

Transient simulations show that the 600 MHz and 1200 MHz configurations do not work correctly, which seems to confirm the correctness of the linearity simulations. Further research will be necessary to determine the exact cause of this problem.

6.3.3 Noise folding

This experiment determines the noise performance of the entire front-end, taking into account the noise folding effect. Once again the different configurations are used, varying sampling frequency and the quality factor of the inductor. The noise figure is derived for a number of points between 0 Hz and 80 MHz, because this is where the Bluetooth band ends up after sampling. 1 dB of insertion loss is added to the noise figure for the BAW filter, because this is not included in simulations, but is included in the handcalculations. The results are displayed in figure 6.6, where some interesting observations can be made.

First of all, the front-end with Q=13 overall has similar Noise figures to the front-end with Q=26. The reason for this is that the front-end with Q=26 has better filtering and thus the folding factor is less, but the noise figure of the LNAs is worse(because the resistance of the inductor is 2 times bigger), which seems to cancel each other out.

The second observation is that higher sampling frequencies configurations generally give better noise figures, but also have frequencies where the noise figure is suddenly increased, for example the noise figure of the 600 MHz Q=13 configuration. A possible explanation for this might be that the LNA transfer function is somewhat shifted in the frequency domain due

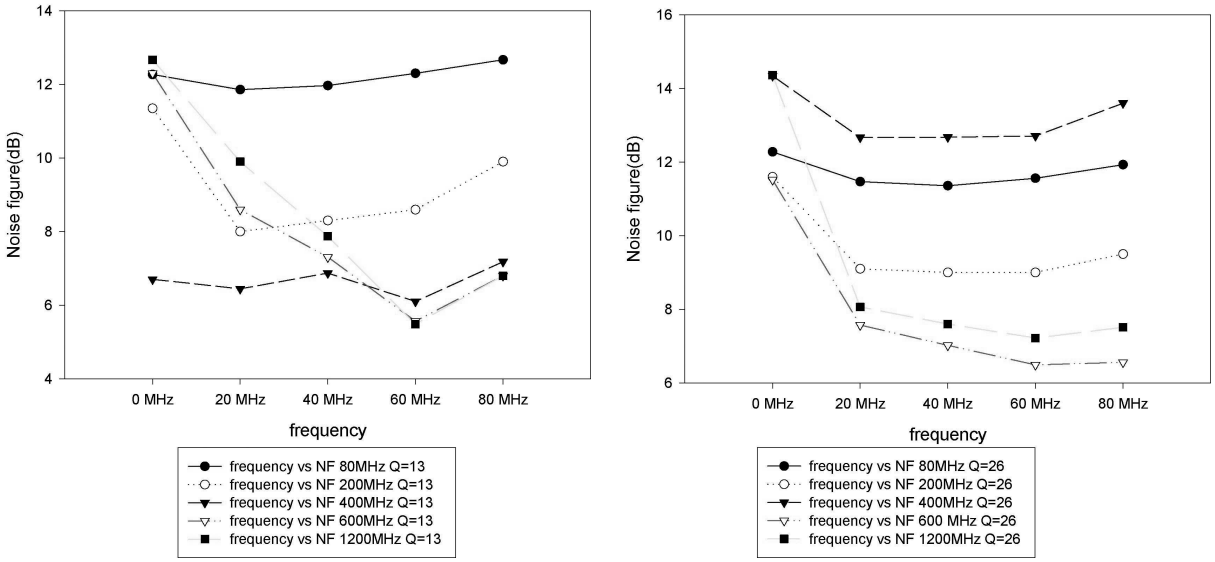


Figure 6.6: Simulated Noise figure with noisefolding total circuit left)Q=13 right)Q=26

Hand-calculated NF total circuit - Q=13					
Clock frequency	80 MHz	200 MHz	400 MHz	600 MHz	1200 MHz
Noise figure	11.3 dB	8.7 dB	6.5 dB	5.4 dB	4.1 dB

Hand-calculated NF total circuit - Q=26					
Clock frequency	80 MHz	200 MHz	400 MHz	600 MHz	1200 MHz
Noise figure	11.4 dB	8.6 dB	6.4 dB	5.5 dB	5.3 dB

Table 6.7: Hand-calculated noise figure total circuit

to loading. This would result in lower gain at one edge of the band of interest, resulting in a higher noise figure. Configurations with a high Q will be more sensitive to this effect, because the bandwidth is much more narrow. This assumption is tested and when the capacitance of the LNA is slightly adjusted/tuned, this problem can be solved.

The results of the low-Q configurations are compared to the hand-calculated values. For the 80 MHz configuration, simulations give a 1 dB higher noise figure, so more noise folding occurs than estimated by hand calculations. This mismatch cannot be explained and needs to be further investigated. The mismatch for the 200 MHz and 400 MHz configurations is 0.5 dB and 0.2 dB, respectively. The handcalculations for the 600 MHz and 1200 MHz match poorly with the simulations, with a 3 dB and 3.5 dB error respectively. This is quite a large error considering almost no noise folding occurs anymore. Because the linearity and transient simulations did not match for these configurations, it is assumed a similar problem exists in these simulations.

The high-Q configurations simulations are also compared to handcalculations. The 80 MHz and 200 MHz configurations once again match well, where once again the noise figure is too low. The 80 MHz configuration has an error of 0.3 dB, while the 200 MHz configuration has

an error of 1 dB. The 400 MHz configuration does not match handcalculations at all, where the error is about 6 dB. The cause for this is unknown, although the problem might be in the second LNA, because the 400 MHz low-Q configuration works fine. Finally the 600 MHz and 1200 MHz match poorly again, which might be the previously discussed simulation problem again.

6.3.4 A note on noise folding

In the calculation of the noise folding, a factor $\frac{1}{\pi}$ was used in the calculation of the folding factor. This factor is the result of the loss in conversion gain due to the tracking and holding, which is also seen in mixers. Periodic noise analysis of Cadence also takes this effect into account, resulting in a good matching between handcalculations and simulations. Handcalculations and simulation both approach the problem from a continuous-time point of view.

However, the track and hold is followed by an ADC, which effectively sees the track and hold as a sample and hold. Thus, from a discrete-time point of view, there will no loss in conversion gain. This will result in more noise folding than the Cadence simulations predict. Further investigation of this problem is necessary to derive a good simulation setup to derive the actual noise folding and the resulting noise figure.

6.3.5 Intermediate result

From these two experiments some conclusions about the best configuration can already be drawn. First of all, because the 600 MHZ and the 1200 MHz are not linear enough according to simulations and also do not perform correctly in transient simulations, these two configurations cannot be investigated further. The second conclusion that can be drawn is that higher quality factors for the inductor do not result in lower noise figures. Although the higher Q offers lower power consumption, the high Q would have to be realised using Q-enhancement techniques. These techniques result in additional power consumption, which is therefore not a good alternative. The high Q configuration will not be investigated further.

6.3.6 Quantization noise

Quantisation noise is added when the signal is digitised by the ADC, which is the focus in this experiment. Two ideal ADC's are used to digitise the I and Q channel. A 14 bit ADC is used for the 80 MHz configuration, while a 13 bit ADC is used for the 200 MHz and 400 MHz configuration. By oversampling the wanted band(with the 200 MHz and 400 MHz configuration) the quantisation noise floor should be reduced. To investigate the digital signals, the data is transferred from Cadence to Matlab.

The experiments uses a -70 dBm input signal as specified in the Bluetooth standard. The quantisation noise floor is approximated by calculating the average noise power as shown in figure 6.7 on the right side. Although this also includes power from higher order harmonics, the approximation seems acceptable. The noise floor on the left side of figure 6.7 is the result of higher order harmonics and numerical noise.

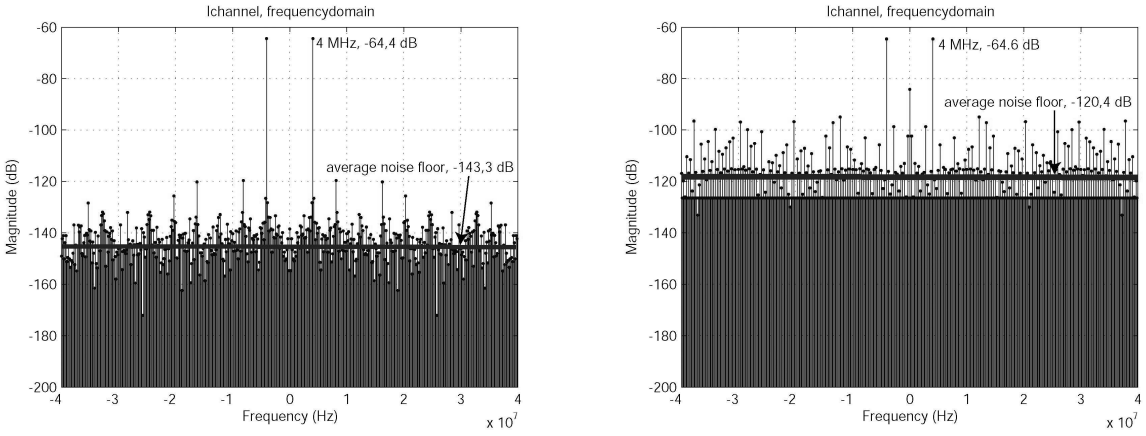


Figure 6.7: Quantisation noise simulation left)before quantisation right)after quantisation

f_s	signal power	av. noise	av. noise - fftgain	SNR
80M	-64.6 dB	-120.4 dB	-96.4 dB	31.8 dB
200M	-64.1 dB	-116.9 dB	-92.8 dB	28.7 dB
400M	-63.7 dB	-111.5 dB	-87.5 dB	23.7 dB

Table 6.8: Quantisation noisefloor

To get the actual quantisation noise floor, the FFTgain needs to be subtracted from the average quantisation noisefloor[15]. The FFT gain is specified in decibel by equation 6.1, where the FFTsize is 512.

$$FFTgain = 10log_{10}(\frac{FFTsize}{2}) \tag{6.1}$$

The resulting Signal-to-noise ratio's are given in table 6.8. The specifications are met, but especially the Signal-to-noise ratio of the 400 MHz configuration is lower than expected. From hand-calculations in section 4.4.4, the signal-to-noise ratio should be around 31 dB.

6.3.7 Interferers

This experiment investigates the effect of out of band interferers with a power of -20 dBm. The Bulk Acoustic Wave filter is approximated with ideal passive components. Inband interferers can be digitally filtered out, although interferers with a power above -20 dBm will cause the ADC input signal to clip. Out of band interferers close to the Bluetooth band are most dangerous, because they also profit from the LNA gain.

In table 6.9 the results of the experiments are shown. The 80 MHz configuration cannot reject the interferer very well. Although the BAW filter will reduce the power of the interferer, the LNA's and buffer will amplify the interferer, resulting in the high power. The 200 MHz and 400 MHz configuration work properly.

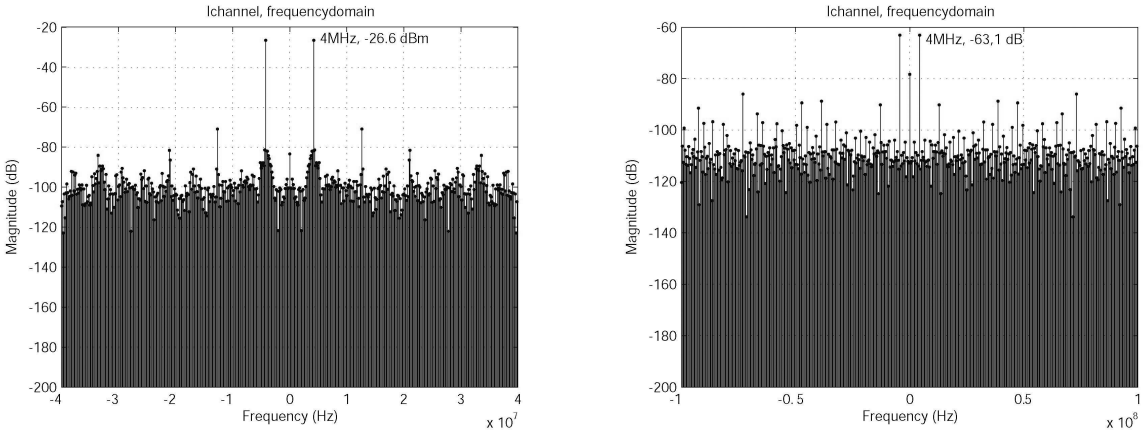


Figure 6.8: Out of band interferer left)80 MHz configuration right)200 MHz configuration

f_s	interferer freq.	power
80M	2.32421875 GHz	-26.6 dB
200M	2.204296875 GHz	-63.1 dB
400M	2.00390625 GHz	-79.6 dB

Table 6.9: Interferer simulation results

6.3.8 Image rejection

With the I and Q channel it becomes possible to perform image rejection. For the second-order sampling receiver, image rejection is also used for reconstruction. This allows us to sample with 80 MHz per channel, because the image band can be rejected.

Two input signals with different frequencies(f_1 and f_2) are put into the receiver with a power of -20 dBm. The frequencies are chosen in such a way that after the sampling operation the signals are close to each other. Matlab performs the image rejection using the Hilbert transform, shown in appendix B. The resulting image rejection is shown in figure 6.9 and table 6.10.

The hand-calculated image rejection using equation 2.10 is significantly better, which could be caused by a gain or phase mismatch. The delay implementation is very accurate, using a pulse generator. There could be a gain mismatch between the I and Q channel, because the load of the buffer changes just before the Q channel samples. This is caused by the I channel that goes from track to hold mode just before the Q channel. Simulations using ideal voltage controlled voltage sources instead of the buffers result in the correct image rejection. It is assumed that using a buffer for each track and hold will solve the problem. Another solution is to make the buffer gain independent of the load.

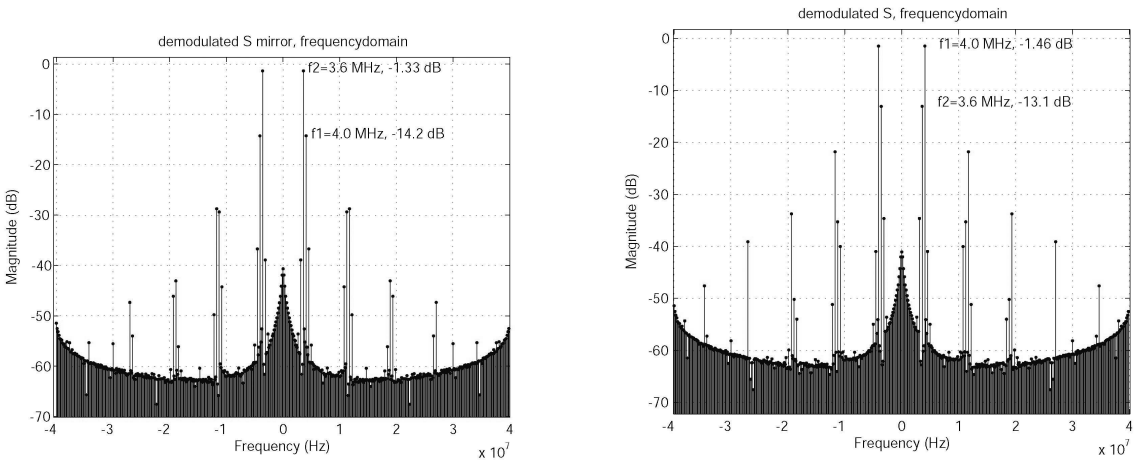


Figure 6.9: Image rejection left) rejection f_1 IIR_1 right)f_1 rejection f_2 IIR_2

Simulated IRR				
f_s	f_1	f_2	IRR_1	IRR_2
80MHz	2.4040625 GHz	2.47640625 GHz	-12.9 dB	-11.6 dB
200MHz	2.404296875 GHz	2.394921875 GHz	-12.4 dB	-11.9 dB
400MHz	2.40390625 GHz	2.39453125 GHz	-15.7 dB	-13.3 dB

Simulated IRR with ideal buffer				
f_s	f_1	f_2	IRR_1	IRR_2
80MHz	2.4040625 GHz	2.47640625 GHz	-39.1 dB	-35.3 dB

Hand-calculated IRR				
f_s	f_1	f_2	IRR_1	IRR_2
80MHz	2.4040625 GHz	2.47640625 GHz	-38.7 dB	-38.6 dB
200MHz	2.404296875 GHz	2.394921875 GHz	-38.8 dB	-36.8 dB
400MHz	2.40390625 GHz	2.39453125 GHz	-38.7 dB	-36.7 dB

Table 6.10: image rejection figures

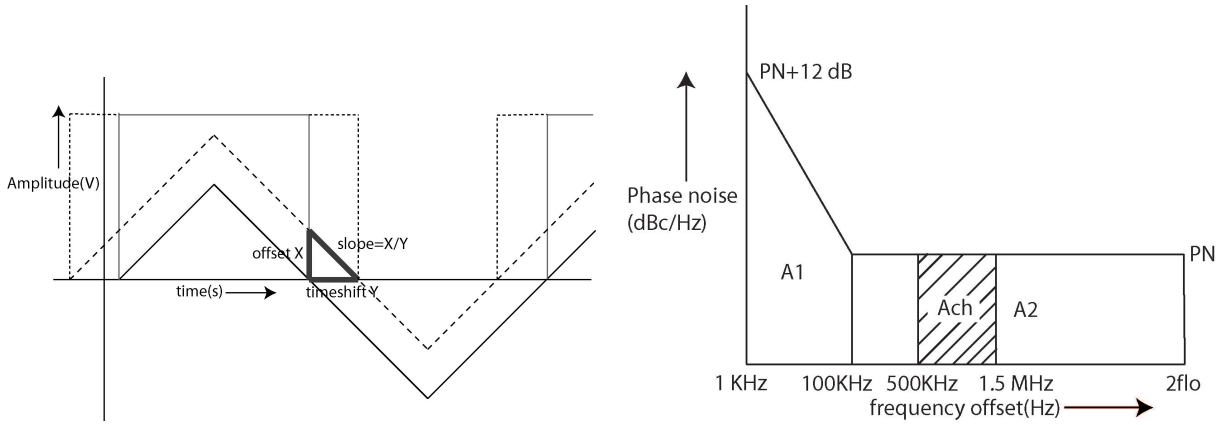


Figure 6.10: Jitter left)deterministic model right)phase noise model

f_s	f_{in}	calculated error	simulated error
80MHz	2.4040625 GHz	-40.2 dB	-39.5 dB
200MHz	2.404296875 GHz	-40.2 dB	-39.4 dB
400MHz	2.40390625 GHz	-44.6 dB	-44.1 dB

Table 6.11: Deterministic jitter error calculation and simulation

6.3.9 Jitter

Jitter is difficult to simulate in Cadence, because it is a non-deterministic error source. Therefore, jitter will be introduced in simulations in a deterministic way and the resulting error can be determined. Using this knowledge, a estimation for the allowed clock jitter can be made.

To introduce jitter in Cadence, a triangle wave is used to determine the zero crossing, where the zero crossing is then used to generate a clock pulse. By introducing a slight offset in voltage to the triangle wave, the zero crossing is shifted in time, resulting in a voltage dependent offset(X) in time. The offset is generated by a sine wave generator, which has a specific frequency, which can later be used to find and determine the error. Because the slope of the triangle wave is known, the resulting time shift(Y) can be calculated. This is illustrated in figure 6.10.

The simulations are performed using a sine wave as the offset with an amplitude of 1 mV, which results in a timeshift of 1,3 ps for the 80 MHz and the 200 MHz configuration and a timeshift of 0,781 ps for the 400 MHz(due to a different slope of the triangle wave). The jitter error in volts can now be calculated with equation 6.2 where the average value(RMS) of the f_{in} is calculated and multiplied with the RMS value of the time offset. The calculated and simulated error match very well, as shown in table 6.11.

$$jittererror = \frac{1}{\sqrt{2}} 2\pi f_{in} \cdot jitter_{RMS} \tag{6.2}$$

Now the allowed phase noise can be calculated using the same approach. The maximum error that is allowed for the different configurations is 1/2 LSB, which is calculated for the

f_s	max. error	jitter inband	A_{ch}	PN	total jitter
80MHz	-78 dB	11.8 fs	-107.5 dB	-167.5 dBc/Hz	0.15 ps
200MHz	-72 dB	23.6 fs	-93.6 dB	-153.5 dBc/Hz	0.47 ps
400MHz	-72 dB	23.6 fs	-87.5 dB	-147.5 dBc/Hz	0.47 ps

Table 6.12: phase noise calculation

different configurations in table 6.12. From this error, the maximum inband RMS jitter can be calculated, using 6.2. The RMS of the jitter can be calculated to the area(A_{ch}) of a phase noise plot in figure 6.10, using equation 6.3[15]. With this information, area A1 and A2 can be calculated, resulting in the required RMS jitter. Crystal oscillators exist that can satisfy this phase noise requirement.

$$RMSPhaseJitter(seconds) = \frac{\sqrt{2 \cdot 10^{A/10}}}{2\pi f_{lo}} \tag{6.3}$$

6.3.10 Power consumption

The power consumption is derived using a transient analysis and calculating the current from the supply voltage. The RMS value of the current is then calculated, as shown in table 6.13. The Hand-calculated power consumption is derived from simulations for individual blocks and multiplying this result by two, because of the differential implementation. This matches quite well with the simulated total power consumption.

One possibility to save power is to turn off the LNAs and buffers when the track and hold is in hold mode. The ratio between the track time and hold time is used to calculate how long the circuit can be turned off. This results in the Hand-calculated power consumption with turn off option shown in table 6.13. For reference, the estimated power consumption of the ADC is also shown in table 6.13.

6.3.11 Results

The experiments that have been performed show that a second-order sampling receiver is indeed feasible, although additional research is necessary. The linearity of the circuit is met only by the 80 MHz and 200 MHz configuration, while the other configurations do not meet the required linearity. For the 600 MHz and 1200 MHz configuration, a problem exist when transient simulations are performed. The noise figure simulations for the 80 MHz and 200 MHz configuration match within 1 dB to the predicted handcalculations, although most other configurations have too high noise figures. However, all the configurations satisfy the required specification. Quantisation noise experiments show slightly higher quantisation noise as expected, but the required Signal-to-noise ratio is met. For the 80 MHz configuration, the interferer simulation shows a serious problem. Additional filtering would be required. The 200 and 400 MHz configurations have better interferer rejection. The image rejection of all the configurations is lower as expected, the solution should be to alter the buffer configuration. Simulations have been performed with ideal buffers, which results in image rejection that

Simulated Power consumption		
f_s	RMS supply current	power consumption
80MHz	17.6 mA	21.1 mW
200MHz	14.3 mA	18.4 mW
400MHz	13.4 mA	16.1 mW

Hand-calculated power consumption	
f_s	power consumption
80MHz	21.9 mW
200MHz	16.4 mW
400MHz	14.8 mW

Hand-calculated power consumption with turn off option	
f_s	power consumption
80MHz	2.73 mW
200MHz	5.13 mW
400MHz	9.25 mW

Hand-calculated power consumption ADC	
f_s	power consumption
80MHz	8.52 mW
200MHz	15.1 mW
400MHz	2.78 W

Table 6.13: Power consumption total circuit

ref.	Noise figure	power
SDR	3.3 dB	34.8 W
this work	< 10 dB	20.23 mW

Table 6.14: comparison with SDR

matches with the handcalculations. Jitter simulations show that a crystal clock is indeed necessary, jitter requirements are reasonably high with currently available techniques. Finally the power consumption is relatively high, although power consumption could be decreased by shutting down the LNA's and buffer during hold mode.

6.4 Comparison

6.4.1 Introduction

The second-order sampling receiver needs to be compared with other receivers to get insight in the performance. Second-order sampling however, is quite different from conventional receivers, because channel selection occurs digitally and the downconversion is performed by the track and hold. One architecture that uses the same approach is the software defined radio concept, which uses an high speed high accuracy ADC to sample the entire spectrum. Such a concept was proposed by Mitola[22].

6.4.2 Comparison

The software defined radio concept is often cited[23] and in this paper an estimation of the power consumption of 500 W. However, this approach assumes a 12 GHz frequency spectrum. A design for a software designed radio similar to this design is investigated, where the ADC would have to operate 5 GHz, with around 14 bit of accuracy(assuming interferers stay below -20 dBm). It might be useful to add an anti-aliasing filter. Once again the power consumption for such an ADC is calculated, resulting in about 34.8 W of power. The power consumption that can be achieved by the subsampling receiver is 5.13 mW(front-end with turn off option) + 15.1 mW(ADC) totals to 20.23 mW. The estimated performance is compared in table 6.14. It becomes apparent that a subsampling receiver can significantly save power in comparison to a software defined radio receiver. When it is taken into account that IQ modulation is required, the comparison shows an even bigger difference. This power saving is achieved because the spectrum that needs to be digitised is significantly reduced at the cost of noise figure. Because the quantisation noise is the limiting factor, this is a good trade-off. However, the required resolution is still equal. When this resolution can also be decreased, second-order sampling can be implemented with very little power.

Chapter 7

Conclusions and recommendations

7.1 Conclusions

The main question of this thesis was whether or not a second-order sampling receiver was feasible. The concept of second-order sampling for use in a radio frequency receiver is indeed possible according to Cadence and Matlab simulations, although verification with a test-chip is still required.

Another goal was to determine the performance limiting mechanisms of such a receiver by designing a receiver for the Bluetooth standard. The specifications of individual blocks that were derived during the system level design were succesfully realised during the transistor level design. The performance limiting mechanisms were investigated using Simulink and Matlab, which identified three possible mechanisms, i.e. noise folding, clock jitter and quantisation noise. These mechanisms are not exclusive to second-order sampling, but are present in all subsampling receivers. The impact of these mechanisms was described using known theory. The individual blocks of the receiver were combined to derive the total performance of the receiver and verify the theoretical predictions. Simulations show that the predicted effect of the mechanisms match well with simulations for low sampling frequency configurations. However, simulations also show problems when the track time is reduced, which is not fully understood. Furthermore, the predicted image rejection is not realised. This is the result of gain mismatch between the I and Q channel. This mismatch can be significantly decreased when the buffer configuration is altered. Depending on how much the gain mismatch is decreased, this will result in better matching to the predicted image rejection. Another problem is the out-of-band interferer, which is not rejected sufficiently for the 80 MHz configuration. The LNAs are not narrowband enough, resulting in amplification of the interferer. Currently, the quantisation noise is the main performance limiting mechanism, especially on the receiver sensitivity level and the power consumption.

It is derived that the configuration using a 200 MHz sampling speed gives the best performance and meets all the Bluetooth specifications. The performance figures are shown in table 7.1.

Finally, the goal to design the receiver to be low power is not entirely successful. Although the power consumption of the current receiver is reasonably low, the ADC will increase the

Parameter	Value
Supply voltage	1.2 V
SNR(-70 dBm input signal)	28.7 dB
IIP_3	-12.7
NF	$<$ 10 dB
Image rejection	-11.9 dB
Sensitivity	-70 dBm
Power consumption	18.4 mW

Table 7.1: Performance second-order sampling Bluetooth receiver

power consumption substantially. However, compared to a full-rate software defined radio ADC, this architecture uses considerably less power.

7.2 Recommendations

The second-order sampling receiver has a long way to go before it becomes a viable alternative to current receivers. The quantisation noise is one of the biggest bottlenecks in the system, because the receiver sensitivity is determined by the number of bits of the ADC. The main reason for this is that inband interferers in combination with a small wanted signal requires a large number of bits to succesfully digitise the small signal. If these interferers could be rejected or filtered, the receiver front-end gain could be increased and the dynamic range requirement of the ADC could be reduced. Analog discrete-time filtering is an option to filter the interferers, e.g. in this paper[24]. However, this does require a significant amount of power.

When a low noise figure is required, a second BAW filter could be placed after the first LNA. Although this requires going off-chip which requires additional power, the first LNA would not suffer from noise folding, decreasing the contribution from the LNA to the cascade figure.

Further research is required into the relationship between the linearity of the receiver and the track time of the track and hold. Further reduction of the track time would allow an even lower power consumption. The image rejection achieved now is around 25 dB less than what is theoretically possible, which is the result of gain mismatch between the I and Q channel. This can be improved with a different buffer configuration.

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Appendix A

Simulink models

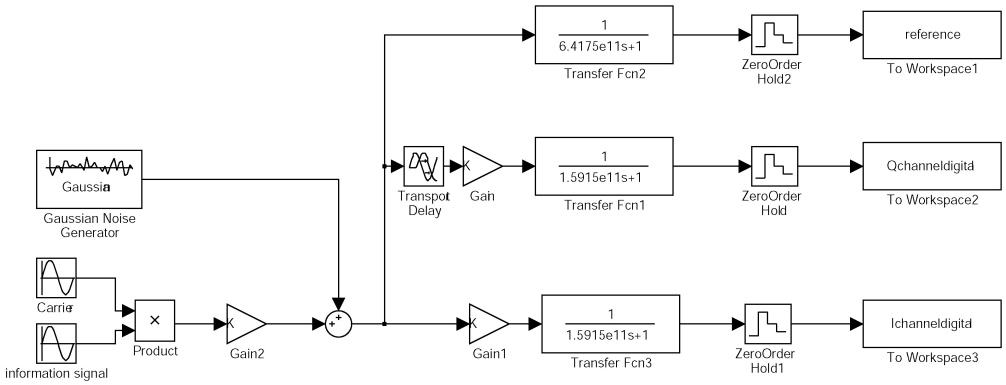

Figure A.1: Simulink model noisefolding

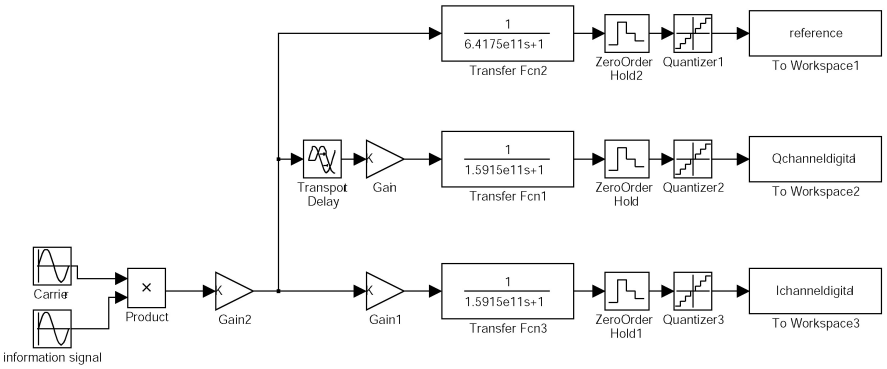

Figure A.2: Simulink model mismatch and quantization noise

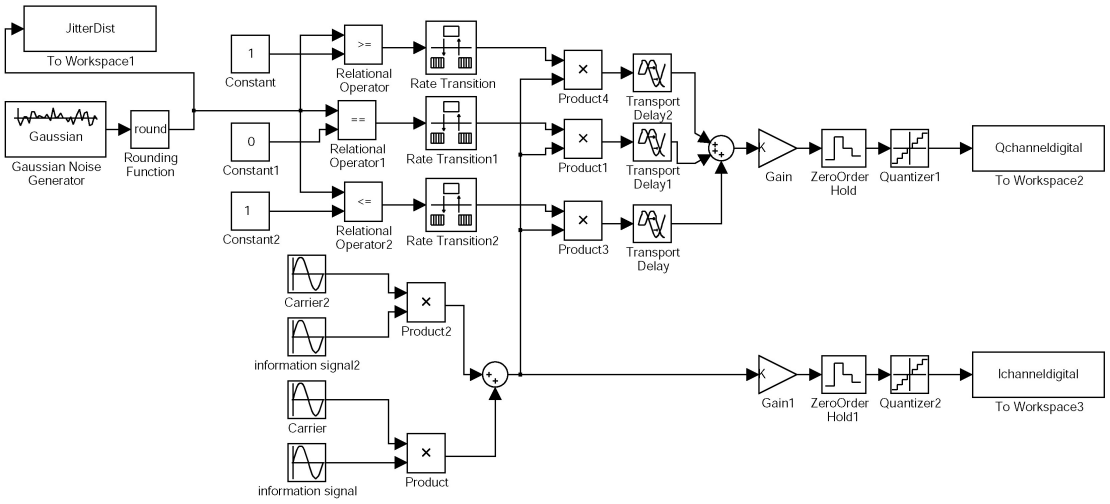

Figure A.3: Simulink model jitter IRR

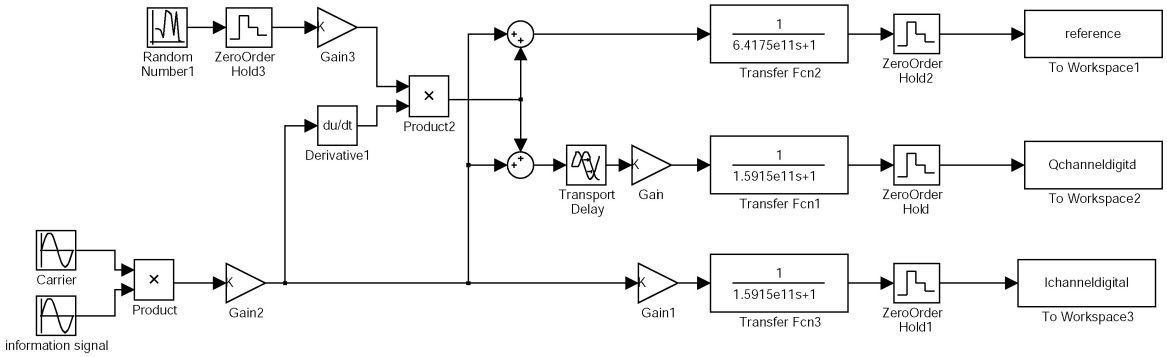

Figure A.4: Simulink model jitter SNR

Appendix B

Matlab scripts

Several Matlab simulations have been used to derive performance figures of the second-order sampling receiver. Not all the code is useful, so only the essential code is shown here.

B.1 DFT

```
fftsize=512;
Qf=fft(inputsignal(length(inputsignal)-(fftsize-1):length(inputsignal)))*2/fftsize;
Qfn=fftshift(Qf);
Qfn((fftsize/2)+1)=Qfn((fftsize/2)+1)/2;
magQfn=20*log10(abs(Qfn));
```

B.2 Image rejection

```
I2=Isamples;
Q2=imag(hilbert(real(Qsamples))) + i*imag(hilbert(imag(Qsamples)));
IQ=I2+Q2;
IQm=I2-Q2;
```

Appendix C

Process parameters

For hand calculations on transistors, process parameters that were used are included in table C.1 for reference.

Process parameter	Value
V_{dd}	1.2V
V_{TH}	0.35V
L_{min}	$0.06\mu m$
$\mu_n C_{ox}$	$385\mu A/V^2$
γ	2/3

Table C.1: process parameters