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Combined VCO/Mixer for satellite receiver in CMOS

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MSc. Thesis
January 2009

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Abstract

In this thesis research is reported studying the possibility to directly drive a switching mixer with a Voltage Controlled Oscillator without buffers in between.

The feasibility research is carried out with an LC-oscillator and a Balun/LNA I/Q mixer (BLIXER) [1] topology. At first the VCO is modeled as an LC-tank with an ideal compensation network to study the effect on the oscillation frequency when loaded with a capacitive load. Spread of capacitances in the oscillator will demand a certain tuning range of the tuneable capacitance in the oscillator to compensate for the spread and keep the oscillation frequency fixed. The required tuning range of the tuneable capacitance in the tank is studied as function of the load capacitance and spread of the load capacitance and tank capacitance.

Secondly a practical CMOS oscillator is used with an NMOS cross-coupled pair with a parallel LC-tank for simulation of the performance of the VCO when loaded with at first a fixed capacitive load and later on with the BLIXER topology.

Effects on performance of the BLIXER driven with sine wave oscillator signals have been compared to the performance of the BLIXER driven with square wave signals. The mixer will be driven with sine wave oscillator signals, which will give a small decrease in conversion gain for the mixer. Finally the effects on performance of the BLIXER have been analyzed when driven directly with the CMOS LC-oscillator without buffers in between.

Leaving the buffers between a VCO and a mixer can give benefit in power consumption but appear to give a number of difficulties when combining the VCO and mixer. It is shown that interaction between the VCO and mixer appears to give an increase in noise in both the VCO as well as the mixer. The switching transistors of the mixer appear to be part of the oscillator and since their capacitance varies in time, also the total capacitance will vary in time. Since the oscillation frequency is dependent on the total capacitance in the tank, this will give an increase in phase noise of the oscillator.

The VCO appear also become susceptible for low frequent noise sources within the mixer. The capacitances of the switching transistors will be dependent on the applied gate-source voltage and also low-frequent noise sources within the mixer can slowly vary these capacitances. Careful design of the mixer will be necessary to prevent low frequent noise contribution of the mixer to be up converted to phase noise of the VCO. Induced gate noise of the switching transistors has a dominant noise contribution in the degraded phase noise of the VCO. The noise figure of the mixer will be degraded for low IF-frequencies as a result of the degraded phase noise of the VCO.

Contents

1. Introduction

Receiving TV channels via satellites orbiting at a distance of more than 10,000 kilometers around the earth isn't a particular easy job to do. The received signal is very weak (~1pW=-90dBm) and can contain a lot of information. The frequency band used for satellite TV in Europe is the K_u-band and lies between 10.7 GHz and 12.75 GHz. The RF-signals in the K_u-band are horizontally and vertically polarized. The total available bandwidth therefore is approximately 4 GHz. This gives room for ~1000 TV-channels[1].

The current satellite receiver consists of bulky components and is a super-heterodyne RF-receiver with an Intermediate Frequency of around 0.95-2.15 GHz. Integrating a satellite receiver in CMOS requires some adaptations on system level. To make transformation to the digital domain feasible, one of the options is to use a zero-IF RF-receiver system. The satellite receiver as zero-IF receiver requires (per polarization direction) a quadrature mixer to downconvert the complete received RF-band to baseband. Furthermore for each mixer a quadrature Voltage Controlled Oscillator is required with an oscillation frequency of 11.7 GHz.

Driving a quadrature mixer with square wave oscillator signals above 7 GHz however has shown to be difficult [1]. In the BLIXER topology proposed by Stephan Blaakmeer et al creating the on-chip 25 % duty cycle square wave oscillator signals failed for frequencies above 7 GHz. The rise- and falltime of the buffers became the limiting factor in generating the high frequency square wave oscillator signals. The 25 % duty cycle square waves looked more like triangular waves as a result of the finite rise- and fall-times of the buffers. Furthermore driving buffers at a high frequency cost a lot of power and introduce a lot of noise. However the BLIXER showed promising simulation results for driving with sine wave signals and a high and flat conversion gain up to 9.5 GHz. Frank Leong showed in his master thesis [2] that a quadrature VCO with an oscillation frequency of 11.7 GHz is feasible.

The above observations have raised the question if it possible to remove the buffers between the oscillator and mixer and drive the mixer with sine wave oscillator signals. This master thesis reports a feasibility study, which is subdivided in two main research questions:

1. Can a VCO be loaded with a mixer?
2. Can a mixer be driven with sine wave oscillator signals?

It is tried to give answer to these questions and consequences on the performance of the VCO and the mixer will be studied.

[1] For Standard Definition TeleVision (SDTV) transmitted with the Digital Video Broadcasting-Satellite (DVB-S) standard.

1.1. Current satellite receiver

A typical satellite receiver (as shown in Figure 1) nowadays consists of three discrete parts, which are: a large dish, an antenna with a Low Noise Block (LNB) in the focus point of the dish and an in-house component called the Integrated Receiver Decoder. The LNB consists of some discrete components, which are necessary to receive and down convert the received RF-signal to an intermediate frequency (~0.95-2.15 GHz).

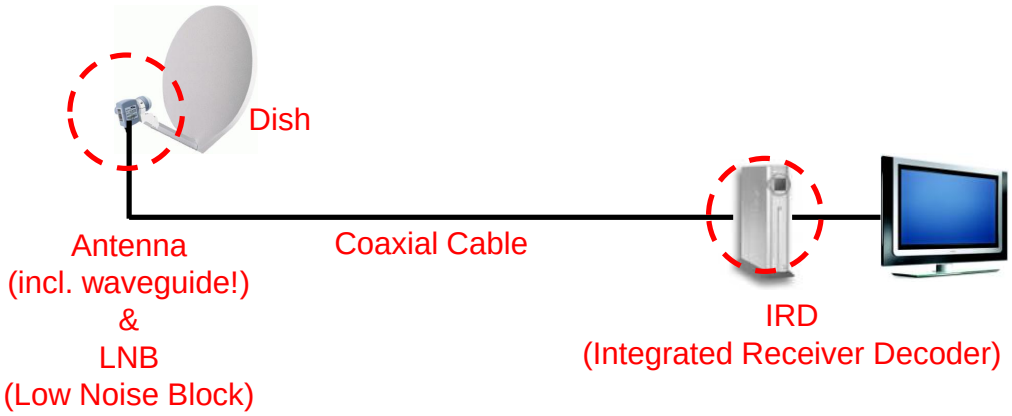

Figure 1: Current satellite receiver setup

The received RF-band is subdivided in channels with a bandwidth of 27-35 MHz each. Each channel contains multiple time multiplexed TV-channels. In the LNB one side band at a time will be downconverted to the IF-band. The IF-band is transmitted through a lossy coaxial cable (~20dB loss for standard 25m cable) to the in-house component, which is the Integrated Receiver Decoder (IRD). In the IRD the demodulation and decoding of the received signals occur.

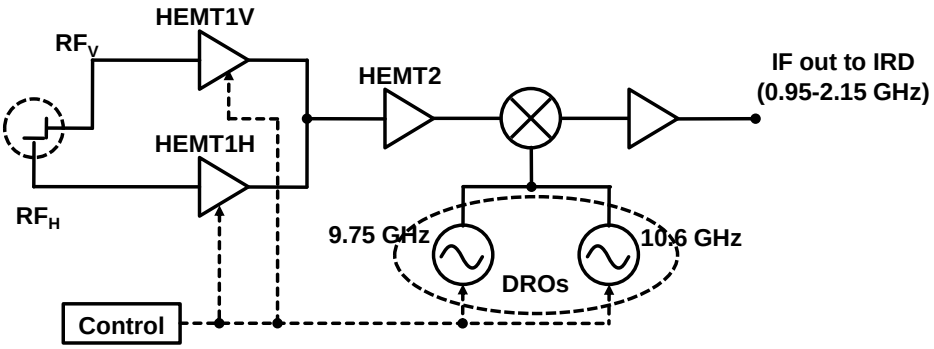

Figure 2: Low Noise Block current satellite receiver

As can be seen in Figure 2 the Low Noise Block consists of High Electron Mobility Transistors (HEMTs) for achieving a very low Noise Figure, two Dielectric Resonator Oscillators (DROs) and a mixer for down conversion to the Intermediate Frequency band. One DRO runs at 9.75 GHz and one at 10.6 GHz to down convert respectively the Lower Side Band (LSB) and Upper Side Band to an Intermediate Frequency band of 0.95 GHz to 2.15 GHz as can be seen in the frequency spectrum in Figure 3.

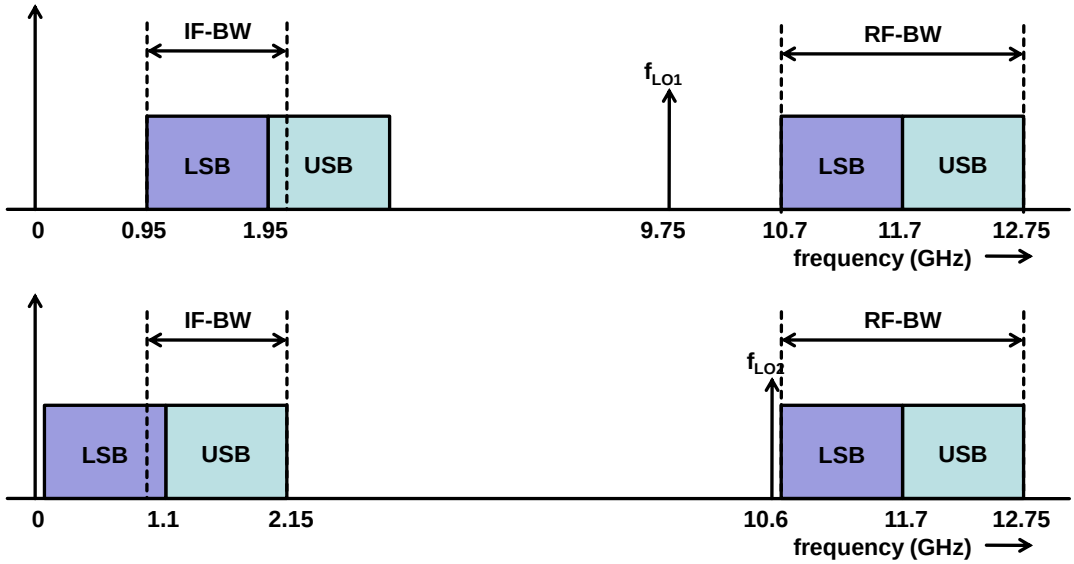

Figure 3: Downconversion in current satellite receiver

1.2. Satellite receiver in CMOS

A drawback of the current satellite receiver system is that (also as a result of the lossy cable) it isn't possible for the user to receive multiple TV-channels at the same time if they are positioned in different sidebands. Removing the coaxial cable out of the system and integrate the complete satellite receiver system in one chip gives a few opportunities and advantages.

Integrating in one chip can decreases the cost of the satellite receiver. Current discrete solutions are large and relative to one chip costly. Integrating the receiver in one chip can decrease production cost.

Integrating the receiver in a CMOS chip gives the possibility of adding all kinds of digital functionality. For example receiving all channels at the same time and take care of the channel selection in the digital domain. In that case many users can benefit from one satellite receiver system.

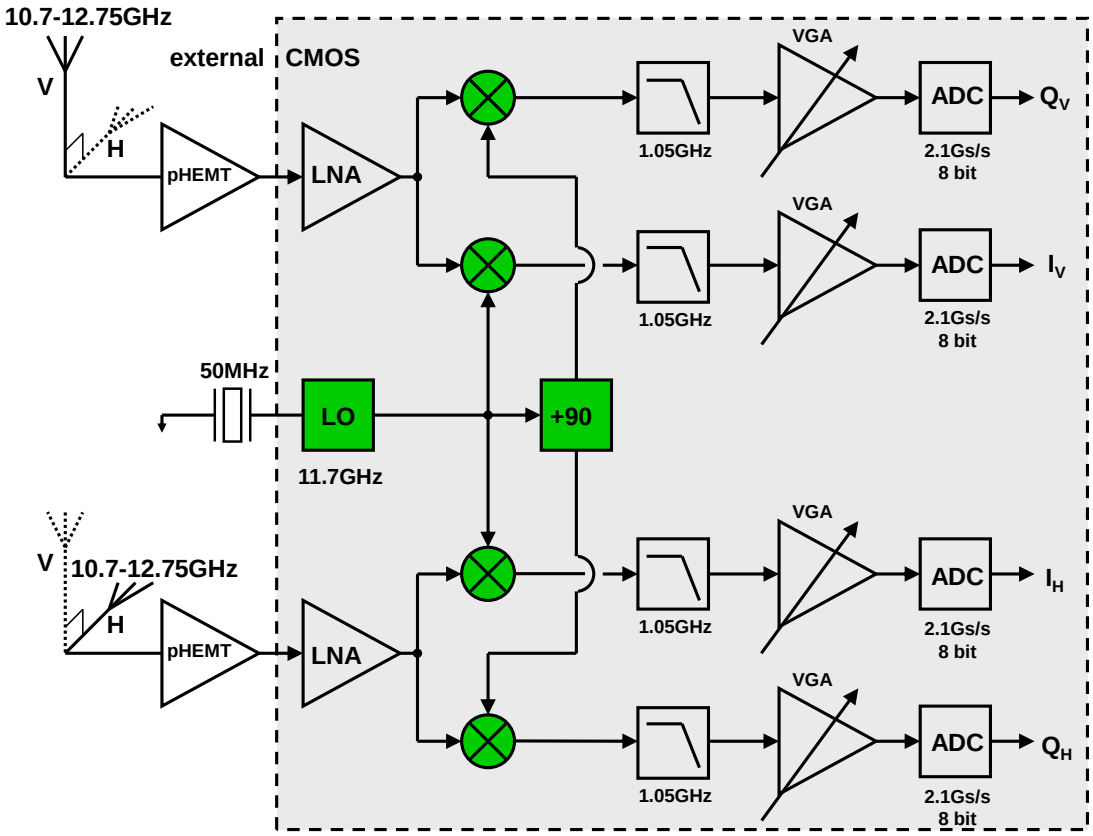

Figure 4: Zero-IF satellite receiver block model

The zero-IF satellite receiver is shown in a block model in Figure 4. The top path shows the part of the receiver for the received vertically polarized signals and the bottom part the receiver path for the received horizontally polarized signals. Only the antenna and the pHEMT (High Electron Mobility Transistor) are still external discrete parts, the rest can be integrated in CMOS. The pHEMT is needed to achieve the desired low noise level at the analog front end.

A Low Noise Amplifier is needed at the input of the chip to amplify the received RF-signal without adding a lot of noise and thereby relaxing the requirements of the next stages. The quadrature mixer then downconverts the RF-signal to baseband, which is visualized in the frequency spectrum in Figure 5. The quadrature mixer is drawn in the block model as two separate mixers, but is in reality one mixer with two outputs, i.e. In-phase and Quadrature (I and Q) outputs. The Local Oscillator provides each polarization path with two oscillator signals, which are 90º out of phase of each other.

An external quartz is used for its very high spectral purity and since it keeps during its lifetime a very accurate oscillation frequency. Since an external quartz with an oscillation frequency of 11.7 GHz doesn't exist, a more common quartz is used with an oscillation frequency of 50 MHz. The oscillator can synchronize its frequency now once every 234th period $\left(\frac{11.7GHz}{50MHz} = 234\right)$ with the external crystal of 50 MHz with the use of a Phase Locked Loop (not drawn in the block model).

Figure 5: Down converting RF in zero-IF receiver

To remove unwanted higher order frequency components introduced by mixing and a low pass anti-alias filter with an IF-BW of 1.05 GHz is needed in front of the ADC. A Variable Gain Amplifier (VGA) at amplifies the baseband signal to match the input voltage range of the ADC. Note that the order of the filter and the VGA can be interchanged, depending on design choices in the final implementation.

The focus in this thesis will be on the interaction between the oscillator and the quadrature mixer.

1.3. Previous work

Currently in literature there aren't yet Voltage Controlled Oscillators reported which drive the switching transistors of a mixer with unbuffered sine wave signals. However there are a few solutions presented, which look similar, because they integrate also oscillator and mixer design, the so-called Self-Oscillating Mixers (SOMs), or Mixer-Oscillators (MOs). Often the mixer is stacked upon the VCO for current re-use and therefore low power consumption. A solution proposed by Bos et al [3] uses mixing within a cross coupled relaxation oscillator with an oscillation frequency of 5 GHz and for a high supply voltage of 2.5 V. A resonatorless oscillator isn't often used in RF-design because they have a lot of noisy active and passive devices in the signal path.

1.4. Goal

The focus of this project is the analog part of the receiver and in particular the oscillator and the (downconverting) mixer. The objective is to combine the design of these two building blocks, which are usually designed independent of each other.

In this thesis the mixer is driven with bufferless oscillator signals, which can give an advantage in power consumption. Normally buffers are used to shield the parasitic capacitive input impedance of the mixer from the oscillator. In this case the capacitive input impedance in fact becomes part of the oscillator's tank capacitance. The tank capacitance in combination with the inductor used in the LC tank of an oscillator (mainly) determines the oscillation frequency.

The mixer in this design is driven by a sinusoidal oscillator signal. If this signal is large enough, the switches in the mixer will be fully switched, comparable with the case when a square wave oscillator signal has been used.

1.5. General assumptions

Al the designs used for testing will be made in a CMOS 65nm process with a supply voltage 1.2V. Use only necessary number of inductors (e.g. for the oscillator), because on chip inductors take up a lot of chip area and can have a lot of loss.

This work goes further on previous work of Frank Leong. So if assumptions or estimations on for instance component values have to be done, then if nothing else is known, component values of his work are used.

From now on analysis in this report will be done for only one polarization direction.

1.6. Overview

This thesis begins with the first main research question of this project: is it possible to load an oscillator with a mixer, which will be discussed in Chapter 2. In paragraph 0 the requirements of the Voltage Controlled Oscillator (VCO) for the satellite receiver will be given. Paragraph 2.2 gives an analysis of the oscillator as a simple series or parallel LC-tank in combination with some kind of compensation network. In paragraph 2.3 we will see that the input impedance of a mixer can be modeled as a fixed capacitance. The VCO will be loaded with this capacitance and its frequency behavior will be analyzed. In paragraph 2.4 the effects of what happens if a VCO is loaded with a varying capacitance will be analyzed. In Paragraph 2.5 conclusions will be drawn based on the answer on the first research question.

The third chapter of this report will focus on the second main research question: is a mixer driveable with sine waves. In the first paragraph all the relevant requirements of the mixer for the satellite receiver are given. In the second paragraph will be determined how large the amplitude and DC level of the oscillator have to be, to drive the mixer with sine wave signals without degrading the performance too much. The mixer performance with sine wave oscillator signals will be tested with the BLIXER topology, which is a Balun-LNA combined with a mixer. This performance will be compared to the performance of the BLIXER with square wave oscillator signals on all the relevant parameters. In the fourth paragraph some optimizing of the BLIXER topology will be done to make the topology suitable for the satellite receiver. In the final paragraph conclusions will be drawn and with that an answer on the research question in the beginning of the chapter will be given.

2. VCO loaded with a capacitive load

Central in this chapter will be one of the two main research questions of this feasibility research. The first main research question is: can a Voltage Controlled Oscillator (VCO) be directly loaded with a mixer without buffers in between? It is expected that the capacitive input impedance of the mixer will have influence on the oscillation frequency. But how large is this influence and will it have large consequences on the oscillator performance?

In the first paragraph the requirements of the VCO will be given, when used for the CMOS satellite receiver.

Paragraph 2.2 will begin with an analysis of a simple LC-tank with an ideal compensation network as macro model for an LC-oscillator as VCO. With the Barkhausen criteria for oscillation the requirements for oscillation for this macro model will be found. Furthermore estimation will be given for the order of magnitude of the input capacitance of a mixer. To be able to answer the research question if a VCO loaded with a mixer is feasible, it will be analyzed which on-chip inductor values are feasible. The chapter ends with a discussion of some consequences for tuning the frequency with a voltage controlled variable capacitor.

In paragraph 2.3 we'll see what happens with the oscillation frequency, if the macro model is loaded with a fixed capacitance. At this point the input impedance of a mixer is modeled as a fixed capacitance. In the case of a parallel LC-tank the oscillation frequency will change and in the case of a series LC-tank a second point in frequency will show up, where the circuit can oscillate. In the second part of the paragraph the macro model will be designed for an oscillation frequency of 11.7 GHz within the presence of a fixed capacitive load. Conditions to keep the oscillation frequency fixed will be discussed if the tank capacitance and the load capacitance exhibit spread. The paragraph will end with an implementation of an LC-oscillator in CMOS and some simulations as verification of the analytical results obtained in this paragraph.

Paragraph 2.4 will focus on the effects on performance of an LC-oscillator loaded with a varying capacitance. Since the input capacitance of a MOSt is very dependent of its applied gate-source voltage, it will be clear that the input capacitance of a mixer is also dependent on the applied voltage. Simulation of the input impedance of the switching transistors of the BLIXER will show how much the capacitive input impedance varies with the applied voltage. The performance of the VCO will be characterized for three cases: without load, loaded with a fixed capacitance and loaded with a mixer. After that we're able to say something of the relative performance of a VCO loaded with a mixer.

Paragraph 2.5 will be used to conclude if a VCO can be loaded with a mixer. Conditions in which case it is (and in which case it isn't) possible will be given. Also the consequences on the performance of the VCO will be given.

2.1 VCO Requirements

The main requirements for the Voltage Controlled Oscillator (VCO) used in the integrated satellite receiver are summarized by: the fixed frequency with high spectral purity and the relatively small tuning range needed to compensate for process variations. To be more specific, all the requirements for the VCO are:

- Fixed oscillation frequency of 11.7 GHz
- Peak to peak amplitude: 1.2 V
- Common mode level: 600 mV
- Tuning range of +/- 5% to compensate for process spread
- Phase noise: $\mathcal{L}(100kHz) = -85\ dBc/Hz$
- Low power consumption = ~ mW
- Quadrature oscillator needed for direct conversion
    - Quadrature accuracy: Image Rejection Ratio (IRR) = ~ 30 dB

The satellite receiver has to be able to receive the complete K_u-frequency band, in which the satellite TV signals are transmitted in Europe. The K_u-frequency band lies between 10.7 GHz and 12.75 GHz. To be able to digitize the received frequency band, it first has to be mixed to baseband. For a direct-conversion receiver system, the oscillator frequency normally is chosen in the middle of the RF-band. In that case the received signal band will be down converted in frequency centered around zero. For the satellite receiver this means that an oscillator frequency is needed of 11.7 GHz.

The required amplitude and common mode of the VCO for this application will depend on a number of things. At first the mixer will set demands on the ideal oscillator amplitude and common mode level, which will be determined in paragraph 3.3. Secondly the implementation of the VCO and in particular the way the tuning of the frequency is implemented will set a boundary on the maximum tank amplitude. To prevent highly nonlinear behavior of the capacitances in the varactor bank, used for tuning of the oscillation frequency, the peak to peak tank amplitude is limited to a maximum of 1.2 V. Normally for an oscillator a large amplitude is wanted, since phase noise will decrease for larger signal power [4,p.665]. Large amplitude also will be beneficial for driving the switching transistors of the mixer. Therefore the required tank amplitude for the VCO will be 1.2 V.

As will be explained more in detail in paragraph 3.3, the ideal common mode level of the oscillator signal will be around 600 mV. If the common mode voltage is larger, then the switching transistors of the mixer can't be closed well enough, which results in lower conversion gain and higher noise figure of the mixer.

Process spread in (mainly) the tank capacitance will result in spread in the oscillation frequency, since the oscillation frequency is dependent on the inverse of the square root of the tank capacitance (which will be shown in paragraph 2.2.1). Assumed is that the tank capacitance has a process spread of 10%, so the oscillation frequency has to have a tuning range of 5%:

$$f_1 = \frac{1}{2\pi\sqrt{L_0(C_0 \pm 10\%)}} \cong \frac{1}{2\pi\sqrt{L_0 C_0}} \pm 5\% = f_0 \pm 5\% \qquad (2.1)$$

With L_0 and C_0 the nominal values for respectively the inductor and the capacitance in the tank, which will give the nominal oscillation frequency f_0.

For each part of the system of the current satellite receiver there are some standards to which it normally more or less has to comply to ensure that a working system can be assembled. For instance a Low Noise Block with a Noise Figure of one dB or even smaller than one dB makes it possible that a reasonably sized dish is sufficient to receive enough signal power. For the oscillator in the satellite receiver normally a phase noise is required of 85 decibels below the carrier per hertz at an offset of 100 kHz (-85 dBc/Hz @ 100 kHz in the $1/f^2$ region) [5,p.19]. However the application of the voltage controlled oscillator in this feasibility research is for a new integrated satellite receiver system. Some tightening or loosening of some of the requirements of different system blocks therefore could be possible, since a new approach on system level has been chosen. But looser requirements for one system block often shifts the problems to another block. So therefore the original standard requirement for the phase noise of the oscillator of -85 dBc/Hz at 100 kHz offset is maintained.

The power consumption should be comparable with other high frequency VCO topologies, which is in the order of magnitude of tens of milliwatts.

The down mixed signal band theoretically will lie between -1 GHz and +1.05 GHz. Actually the positive and negative frequency bands will fold over each other and therefore for image rejection a quadrature mixer will be needed to make distinction between the positive frequency band (0..1.05GHz) and the negative (-1GHz..0). Furthermore since the received RF signal is I/Q demodulated a quadrature mixer is simply required for demodulation. To be able to drive a quadrature mixer, the oscillator has to have quadrature outputs.

To prevent interference between the down converted negative- and the positive frequency bands, the quadrature oscillator signals will have to be accurate enough in quadrature. The image rejection ratio gives an indication of how accurate the quadrature signals have to be. Assuming that the amplitude mismatch isn't a big issue for a fully switched mixer, quadrature signals must have a phase deviation of less than 3.62 degrees for an IRR of 30 dB, using the following formula [4,p.702]:

$$IRR = \frac{P_{sig,out}}{P_{im,out}} \cdot \frac{A_{im,in}^2}{A_{sig,in}^2} \approx \frac{4}{\epsilon^2 + \phi^2} \tag{2.2}$$

With ϵ the relative amplitude mismatch and ϕ the phase deviation from perfect quadrature in radians.

2.2 LC-oscillator as VCO

With the list of requirements presented in the previous chapter the most obvious choice as VCO for this application is a simple LC tank with some form of compensation network to compensate for the losses in the tank. Both series & parallel form of the LC-tank have been studied here in respectively section 2.2.1 and section 2.2.5. For analysis of the LC-oscillator a macro model is used. The macro model consists of an ideal Voltage Controlled Current Source in combination with a series- or parallel LC-tank. To be able to answer if a VCO is still feasible when loaded with a mixer, at first estimation has been made on the input capacitance of a mixer in section 2.2.2. After that rough margins will be given for feasible on-chip inductor values in section 2.2.3. A choice will be made for the value of the inductor, which will be used in the rest of this thesis. Section 2.2.4 will explain why the feasibility of loading a VCO with a mixer is also affected by restrictions of variable capacitors for tuning the frequency.

2.2.1 Parallel LC-tank

An LC-oscillator normally consists of two parts, i.e. an LC-tank which is mainly responsible for the oscillation frequency and an active part which acts as a compensation network for the losses in the tank.

An ideal LC-tank consists of 2 elements: an inductor and a capacitor. The losses of a tank can be modeled as a resistance in parallel with the tank. The model of a realistic LC-tank therefore consists of 3 elements, as can be seen in Figure 6.

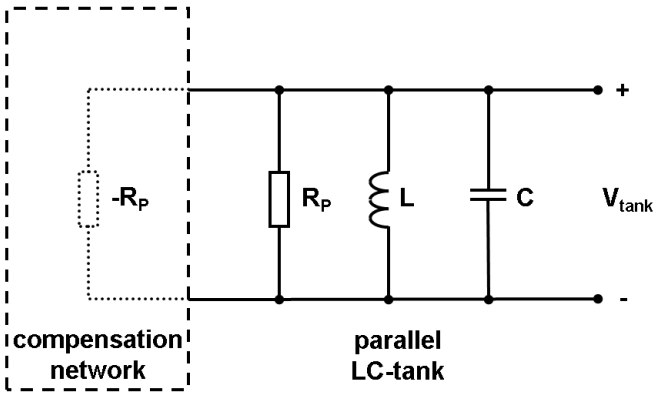

Figure 6: Parallel LC-tank

The compensation network has to compensate for the losses introduced by the tank and can be modeled as a negative resistance in parallel with the tank. A negative resistance can be modeled in two extreme cases as a Voltage Controlled Current Source (VCCS, transconductance) or a Current Controlled Voltage Source (CCVS, transresistance). Since most compensation networks have a VCCS-character (nature of MOSFET) and a transresistance isn't very straightforward to implement, the tank only will be analyzed in combination with a VCCS compensation network.

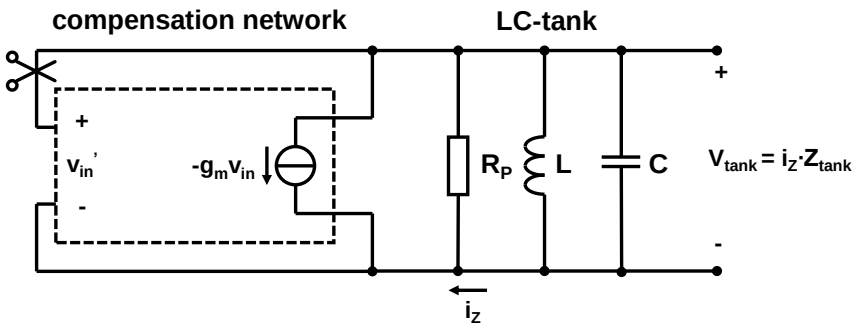

Figure 7: VCCS with parallel LC-tank

The tank will oscillate if the Barkhausen criteria for oscillation are met [6,p.206].

Barkhausen criteria:

1. Loop gain = 1
2. Phase shift of loop gain = 0°

For the parallel LC-tank with a VCCS as compensation network (as shown in Figure 7) the Barkhausen oscillation criteria will translate in:

1. $Loop\ gain = \frac{v_{in}'}{v_{in}} = \frac{-g_m v_{in} \cdot -\left|Z_{tank,par}(\omega)\right|}{v_{in}} = g_m\left|Z_{tank,par}(\omega)\right| = 1$

   $$\Longrightarrow \boldsymbol{g_m = \frac{1}{\left|Z_{tank,par}(\omega)\right|}} \tag{2.3}$$

2. $Im\left(g_m Z_{tank,par}(\omega)\right) = 0$

   $$\xrightarrow[if\ Im(g_m)=0]{} \boldsymbol{Im\left(Z_{tank,par}(\omega)\right) = 0} \tag{2.4}$$

The tank impedance can be written as:

$$Z_{tank,par}(\omega) = \frac{1}{Y_{tank,par}(\omega)} \tag{2.5}$$

$$Z_{tank,par}(\omega) = \frac{1}{\frac{1}{R_P} + \frac{1}{j\omega L} + j\omega C} \tag{2.6}$$

$$Z_{tank,par}(\omega) = \frac{1}{\frac{1}{R_P} + j\left(\frac{-1}{\omega L} + \omega C\right)} \tag{2.7}$$

It can be seen that the tank impedance will have no imaginary part, if:

$$\frac{-1}{\omega L} + \omega C = 0 \tag{2.8}$$

$$\rightarrow \omega_0 = \frac{1}{\sqrt{LC}} \tag{2.9}$$

The tank impedance for the oscillation (angular) frequency ω_0 is then:

$$Z_{tank,par}(\omega_0) = R_P \tag{2.10}$$

So, oscillation will occur for:

1. $g_m = \frac{1}{\left|Z_{tank,par}(\omega_0)\right|} = \frac{1}{R_P}$ (2.11)
2. $\omega_0 = \frac{1}{\sqrt{LC}}$ (2.12)

Note that for the oscillation to start-up, the loop gain has to be able to be larger than one (only for a small time). Furthermore parameters such as the transconductance and the parallel tank resistance always have some spread. Therefore the compensation network is usually designed such that a transconductance of 2 or 3 times higher can be achieved, than strictly necessary for steady state oscillation. This is to assure that the oscillator always will be able to start up.

2.2.2 Component values

To be able to answer the first main research question, can a VCO be loaded with a mixer, at first an estimate is made of the input capacitance of the mixer. As a rough first estimate the input capacitance of the mixer is assumed to be 200 fF per LO-port. Since these two input capacitances form in series the total input capacitance between the two LO-input ports of the mixer, the total input capacitance is assumed to be 100 fF for now.

At first will be determined if the VCO is still feasible if it is loaded with a load capacitance of 100 fF. Doesn't it give unrealistic demands on the required tank inductance and capacitance? But what can be considered as realistic values for an on-chip inductors and capacitances? Especially values of on-chip inductors are limited, which will be shown in the next section.

2.2.3 Feasible on-chip inductor values

First of all to realize a large inductor on chip will take up a lot of chip area. Furthermore it is difficult to make a large on chip inductor with a high quality factor. The quality factor is an indication of the losses in the inductor and its fundamental definition [4,p.88] is:

$$Q \equiv \omega \frac{energy\ stored}{energy\ dissipated} \tag{2.13}$$

When taking into account all the losses in an LC-tank, the quality factor of an LC-tank is a measure for the narrowness of the bandwidth of the LC-tank. For an ideal LC-tank without losses, the quality factor will be infinite and the transfer function would be a diraq pulse at the oscillation frequency.

A third difficulty of using a large on-chip inductor is the increasing parasitic capacitance of the inductor. As a result of the parasitic capacitance, the inductor will have a self-resonance frequency, which will decrease for larger inductor values. The oscillation frequency of the tank always has to be smaller than the self-resonance frequency of the inductor.

Furthermore the maximum inductor value for this application is limited for another reason. That is, for a large inductor, there won't be enough room left for the tank capacitance. For example if an inductor is used with a value of 10 nH, the corresponding tank capacitance has to be 18.5 fF for an oscillation frequency of 11.7 GHz (with the use of equation 2.12):

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$
$$\Rightarrow C = \frac{1}{L(2\pi f_{osc})^2} = \frac{1}{10 \cdot 10^{-9}(2\pi 11.7 \cdot 10^9)^2} = 18.5\, fF \quad (2.14)$$

Achieving an oscillation frequency of 11.7 GHz will be hard, because parasitic capacitances in the oscillator will be usually already larger than 18.5 fF. On the other hand the inductor can't be chosen too small either, because then parasitic inductances tend to dominate the oscillation frequency. To give an indication: a piece of straight interconnect metal of 1 µm will already have a parasitic self-inductance of roughly 1 pH [7, p. 140].

So in theory for an LC-tank with a desired oscillation frequency of 11.7 GHz on-chip inductor values between roughly 10 pH and 1 nH are feasible.

In the thesis of Frank Leong [2] a Colpitts oscillator was designed for the same satellite receiver application and therefore for the same oscillation frequency of 11.7 GHz. He used an on-chip inductor with the value of L = 400 pH. Since already practical simulation data such as quality factor, series resistance and self-resonance frequency are available, this inductor is also used for the analysis in this feasibility research.

Parameters of on-chip inductor:

- Inductance L = 400 pH
- Quality factor Q = 26 (@ 10 GHz)
- Self-resonance frequency ~ 40 GHz
- Parasitic series resistance of inductor (including all the losses in the LC-tank): $R_S = 2.35\ \Omega$
- The effective quality factor of the LC-tank becomes then at 11.7 GHz:

$$Q = \frac{\omega L}{R_s} = \frac{2\pi 11.7 \cdot 10^9 \cdot 400 \cdot 10^{-12}\ \Omega}{2.35\ \Omega} = \frac{29.4\ \Omega}{2.35\ \Omega} = 12.5 \quad (2.15)$$

2.2.4 Tuning the frequency

Tuning the frequency in an LC-oscillator is often realized with variable capacitors (for example varicaps or varactors). A varactor is in fact often a transistor with source and drain connected to ground. The gate voltage acts as control voltage for the capacitance seen between gate and drain-source.

Note that with the use of varactors always a fixed capacitance is present, even when the varactors have a zero control voltage. So there should always be room in the tank for the fixed capacitance of the varactors.

Secondly the tuning range of a varactor depends on the size of the varactor. The smaller the varactor, the smaller the fixed capacitance is compared to the variable part and therefore the tuning range for a small varactor is considerably smaller than for a larger varactor [2].

2.2.5 Series LC-tank

The LC-tank of an LC-oscillator can also be implemented with a series LC-tank (as showed in Figure 8). The losses in the tank are modeled with a series resistance. If the same inductor and capacitance are used for the tank, the series LC-tank will give the same oscillation frequency as the parallel LC-tank. This will be proven with the Barkhausen criteria later on in this section.

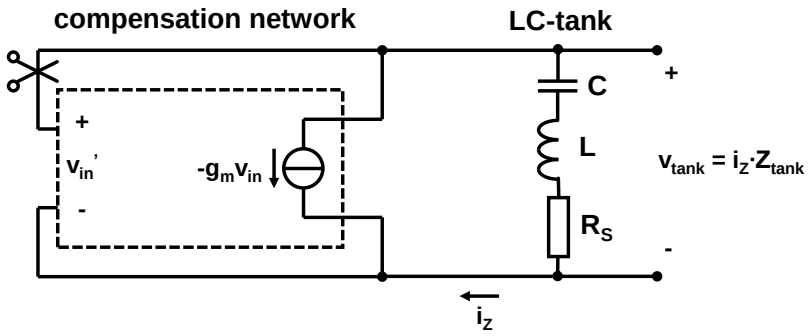

Figure 8: VCCS with series LC-tank

The main difference between a series- and parallel LC-tank is the tank impedance at the oscillation frequency. For the parallel LC-tank we've seen that the tank impedance at oscillation is equal to the parallel resistance R_P. For the series LC-tank the tank impedance at oscillation will be equal to the series resistance R_S. Normally the series resistance R_S is determined by the actual resistance of the wires of the inductor, which are in the order of magnitude of a few ohms. This is quite small and as a result of that the power consumption of the tank will be large for a given voltage ($P = \frac{V_{rms}^2}{R_S}$). Consider for example an inductor with a series resistance of 2.35 Ω, the current through the tank then will be around 170 mA for a tank amplitude of 400 mV ($I = \frac{V}{R} = \frac{400mV}{2.35\Omega} = 170mA$).

The parallel resistance R_P for the parallel LC-tank is a lot larger than the series resistance R_S in the case of a series LC-tank. If the same inductor and capacitor is used, the parallel resistance is (at oscillation) approximately Q^2 larger [4,p.95] than the series resistance. Therefore the current consumption of a parallel LC-tank will be approximately Q^2 smaller than a series LC-tank for the same tank amplitude. For example an inductor with a Q of 10 at oscillation will have a 10^2=100 times larger resistance at oscillation and therefore also a 100 times smaller current consumption.

The series LC-tank also has been analyzed with the Barkhausen criteria for oscillation.

Barkhausen criteria:

1. Loop gain = 1
2. Phase shift of loop gain = 0°

For the series LC-tank with a VCCS as compensation network (shown in Figure 8) the oscillation criteria will translate in:

1. $$Loop\ gain = \frac{v_{in}'}{v_{in}} = \frac{-g_m v_{in} \cdot -\left|Z_{tank,ser}(\omega)\right|}{v_{in}} = g_m\left|Z_{tank,ser}(\omega)\right| = 1$$
   $$\Longrightarrow \boldsymbol{g_m = \frac{1}{\left|Z_{tank,ser}(\omega)\right|}} \tag{2.16}$$
2. $$Im\left(g_m Z_{tank,ser}(\omega)\right) = 0$$
   $$\xrightarrow[if\ Im(g_m)=0]{} \boldsymbol{Im\left(Z_{tank,ser}(\omega)\right) = 0} \tag{2.17}$$

The series tank impedance can be written as:

$$Z_{tank,ser}(\omega) = R_S + \frac{1}{j\omega C} + j\omega L = R_S + j(\omega L - \frac{1}{\omega C}) \tag{2.18}$$

It can be seen that the tank impedance will have no imaginary part, if:

$$\omega L - \frac{1}{\omega C} = 0 \ \rightarrow\ \omega_0 = \frac{1}{\sqrt{LC}} \tag{2.19}$$

The tank impedance for ω_0 is then:

$$Z_{tank,ser}(\omega_0) = R_S \tag{2.20}$$

So, oscillation will occur for:

1. $$g_m = \frac{1}{\left|Z_{tank,ser}(\omega_0)\right|} = \frac{1}{R_S} \tag{2.21}$$
2. $$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.22}$$

2.3 Loading effects on VCO-frequency

In the previous paragraph the Barkhauen criteria have been used to find criteria for oscillation for the used macro-model of a series- or parallel LC-tank in combination with a voltage controlled current source. The same Barkhausen criteria will now be used to study the effects on the oscillation frequency when loading the macro-model with a fixed capacitance.

For both cases the LC-tank will consist of the already chosen inductor in section 2.2.5 of 400 pH and a capacitor of 463 fF, such that the oscillation frequency will be 11.7 GHz:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \rightarrow \tag{2.23}$$

$$C = \frac{1}{L(2\pi f_0)^2} = \frac{1}{400\ pH \cdot (2 \cdot \pi \cdot 11.7\ GHz)^2} = 463\ fF \tag{2.24}$$

In 2.3.1 the macro model will be loaded with the (already in 2.2.2 estimated) capacitive input of a mixer of 100 fF and the effects on the oscillation frequency will be given.

In section 2.3.2 the results obtained in 2.3.1 will be used to see if it's possible to choose a tank capacitance given a fixed capacitive load of 100 fF and still obtain an oscillation frequency of 11.7 GHz. This will lead to different possible ranges of capacitive load for the series- and the LC-tank. The requirement to be able to compensate for spread in the load capacitance, but also in the tank capacitance will eventually lead to an even smaller range of possible capacitive load for the series- and parallel LC-tank.

In the last section (2.3.3) of this paragraph an implementation of a VCO in CMOS will be given in the form of a cross-coupled pair. The cross-coupled pair will be designed for an oscillation frequency of 11.7 GHz. Simulations will be run to verify the analytical results found earlier in this thesis for an unloaded LC-oscillator as well as for an LC-oscillator loaded with a fixed capacitance of 100 fF.

2.3.1. Fixed capacitance model for the load

The macro model of the LC-oscillator will now be studied, if loaded with a fixed capacitance. It is expected that the oscillation frequency will change as result of capacitive loading. The input capacitance of a mixer is modeled here as a fixed capacitance. In Figure 9 this is shown for the case of a parallel LC-tank with a VCCS compensation network and a capacitive load of: $C_{load} = \frac{C_1 C_2}{C_1 + C_2} (= \frac{1}{2} C_1 \; if \; C_1 = C_2)$.

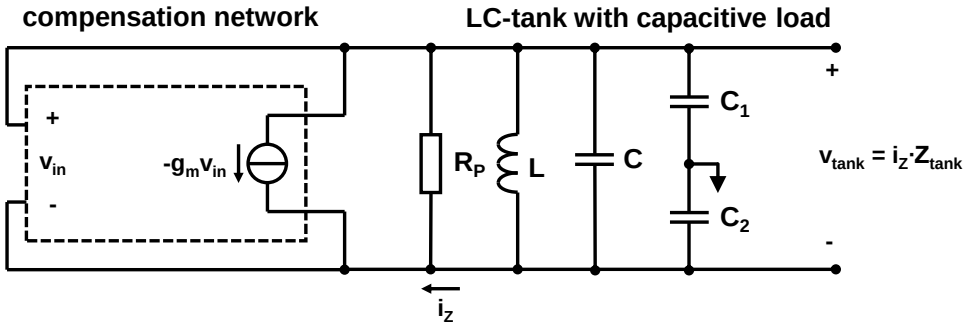

Figure 9: VCCS with parallel LC-tank and capacitive load

In this paragraph an analysis is done for both the series and parallel LC-tank in combination with an ideal VCCS compensation network. The analysis has been done with Maple, based on the Barkhausen criteria for oscillation. Plotted are the absolute value of the tank impedance and the imaginary part of the tank impedance as a function of the frequency. Recall from the previous paragraph that oscillation will occur if the loop gain is equal to one and if the total phase shift of the loop is zero. In this analysis the compensation network is assumed to be ideal, i.e. without capacitive or inductive elements. This means that for zero phase shift of the loop the imaginary part of the loaded tank impedance has to be zero.

The components values of the LC-tank are chosen such that the oscillation frequency of the *tank* is 11.7 GHz. An inductor of 400 pH and a capacitor of 463 fF are used here. With the use of equation 2.8 (and 2.18) this will give an oscillation frequency of 11.7 GHz. For the series tank, the losses in the tank are modeled by a series resistance R_S with a value of 2.35 Ω (see 2.2.3). For the parallel tank, the losses of the tank are modeled with the parallel resistance R_P, which can be approximated for frequencies near the oscillation frequency with [4,p.95]:

$$R_P \approx Q^2 R_S = (12.5)^2 \cdot 2.35\,\Omega = 368\,\Omega \qquad (2.25)$$

The tank will be loaded with the estimated capacitive input capacitance of the mixer of 100 fF.

Parallel LC-tank

At first the parallel tank will be analyzed. The impact on the oscillation frequency as a result of loading the parallel LC-tank can be seen in Figure 10 and Figure 11.

The impedance of the loaded parallel LC-tank can be written as ($with\ C_{load} = \frac{C_1 C_2}{C_1+C_2}$):

$$Z_{tank,par,loaded}(\omega) = \frac{1}{Y_{tank,par.loaded}(\omega)} \tag{2.26}$$

$$Z_{tank,par,loaded}(\omega) = \frac{1}{\frac{1}{R_P} + \frac{1}{j\omega L} + j\omega C + j\omega C_{load}} \tag{2.27}$$

$$Z_{tank,par,loaded}(\omega) = \frac{1}{\frac{1}{R_P} + j\left(\frac{-1}{\omega L} + \omega(C + C_{load})\right)} \tag{2.28}$$

The loaded tank impedance will have no imaginary part, if:

$$\frac{-1}{\omega L} + \omega(C + C_{load}) = 0 \ \rightarrow \omega_0 = \frac{1}{\sqrt{L(C + C_{load})}} \tag{2.29}$$

$$\rightarrow f_0 = \frac{1}{2\pi\sqrt{L(C + C_{load})}} = \frac{1}{2\pi\sqrt{400pH(463fF + 100fF)}} = 10.6\ GHz \tag{2.30}$$

So oscillation will occur if:

1. $\omega_0 = \frac{1}{\sqrt{L(C+C_{load})}}$ (2.31)
2. $g_m = \frac{1}{|Z_{tank,par,loaded}(\omega_0)|} = \frac{1}{R_P}$ (2.32)

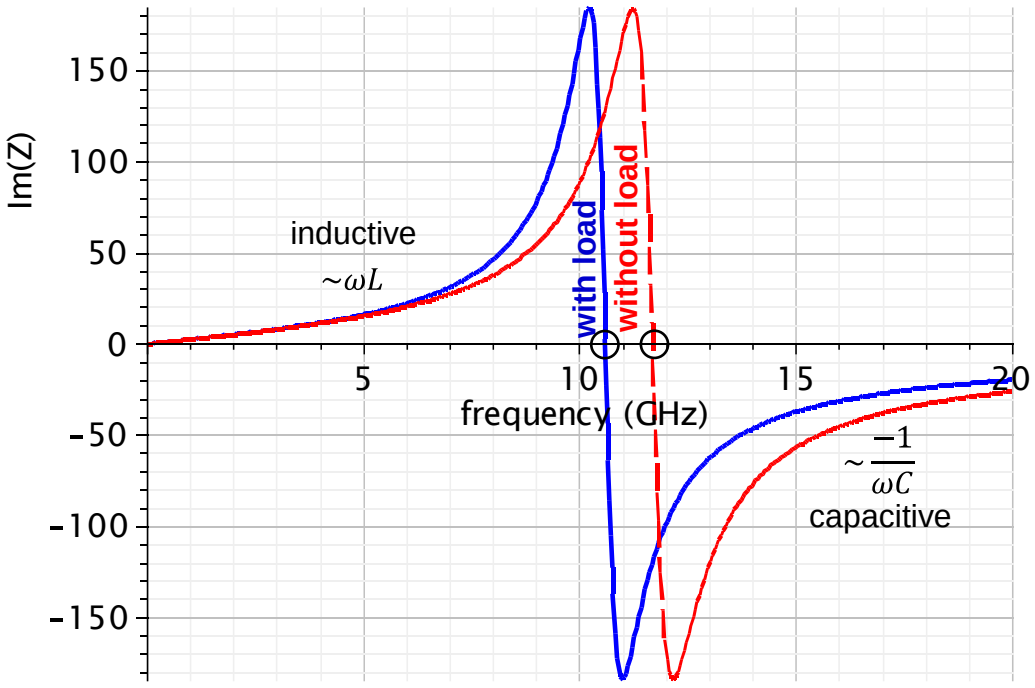

Figure 10: Imaginary part tank impedance parallel LC-tank

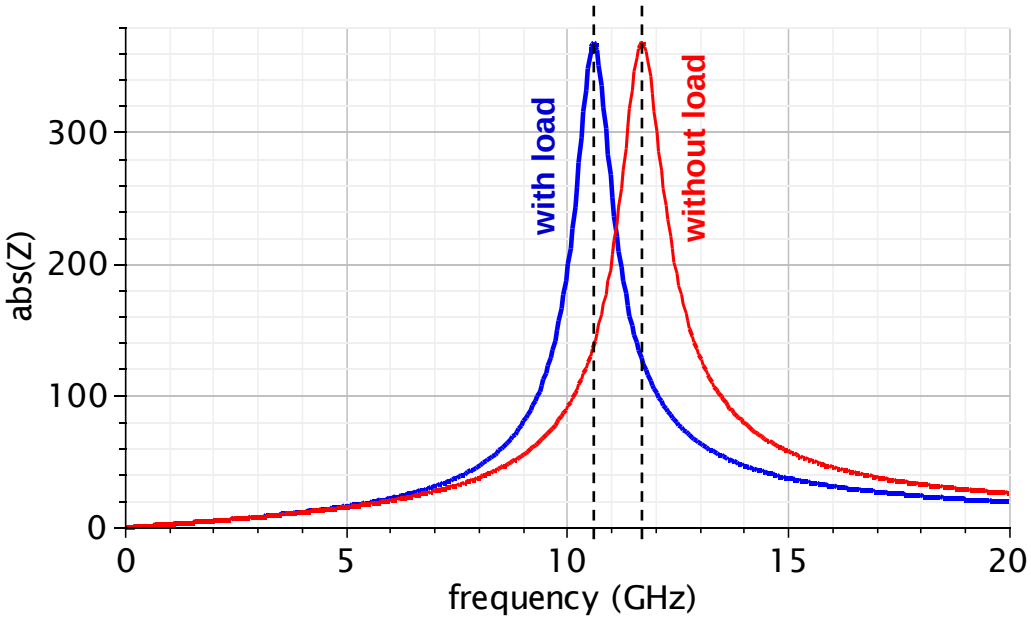

Figure 11: Absolute tank impedance parallel LC-tank

As can be seen in Figure 10 and Figure 11 the oscillation frequency is shifted down 1.1 GHz to 10.6 GHz as result of the capacitive load of 100 fF. This can be well understood, when observing the following:

As a result of the capacitive load, the total capacitance in the tank has increased with 22%:

$$\frac{\mathrm{C_{load}}}{\mathrm{C_{tank}}} \cdot 100\% = \frac{100\ \mathrm{fF}}{463\ \mathrm{fF}} \cdot 100\% = +22\ \% \tag{2.33}$$

Since the oscillation frequency is inversely dependent on the square root of the product of L and C, an increase of 22% in the capacitance will result in a decrease in oscillation frequency of -9.3 %:

$$f_1 = \frac{1}{2\pi\sqrt{L_0(C_0 + 10\%)}} = \frac{1}{2\pi\sqrt{L_0 C_0}} - 9.3\% = f_0 - 9.3\% \tag{2.34}$$

So the oscillation frequency will shift down with ~ 9.3 %:

$$-9.3\% \cdot 11.7\ GHz = -1.09\ GHz \tag{2.35}$$

to a lower oscillation frequency of:

$$11.7\ GHz - 1.09\ GHz = 10.61\ GHz \tag{2.36}$$

The obtained analytical results here will be compared later on with the simulation results of the CMOS LC-oscillator loaded with the same fixed capacitive load of 100 fF.

Series LC-tank

The same analysis with Maple has been done for the series LC-tank. The impact on the oscillation frequency as a result of loading the series LC-tank with a capacitive load of 100 fF can be seen in Figure 13 and Figure 14.

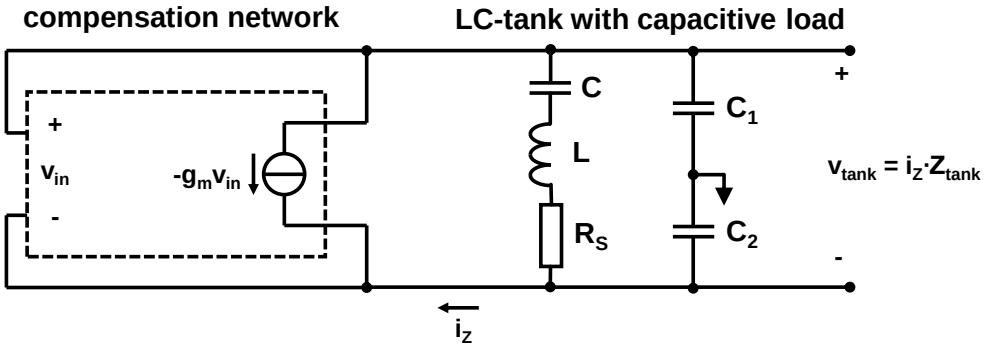

Figure 12: VCCS with series LC-tank and with capacitive load

For the series LC-tank with capacitive load there are now two points where the imaginary part of the total tank impedance is zero. The first point equals the original oscillation frequency of the tank, which is: $f_1 = \frac{1}{2\pi\sqrt{LC}} = 11.7\ GHz$. The second point is in fact the oscillation frequency determined by the inductor and the series network of the tank capacitance and the load capacitance, which is: $f_2 \approx \frac{1}{2\pi\sqrt{L\frac{CC_{load}}{C+C_{load}}}} = 27.75\ GHz$.

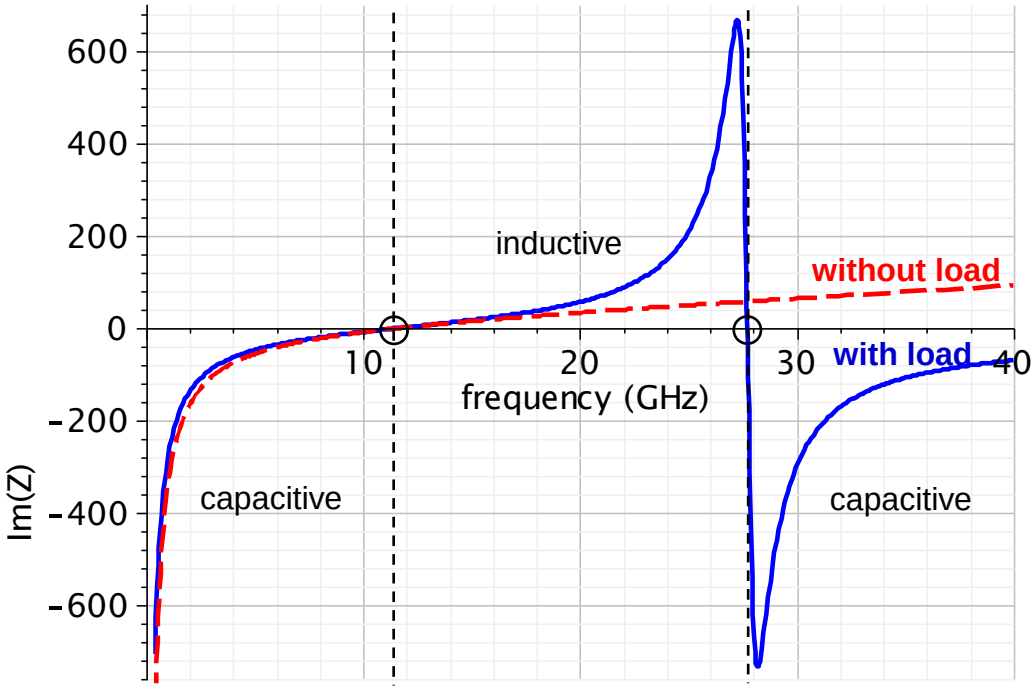

Figure 13: Imaginary part tank impedance series LC-tank

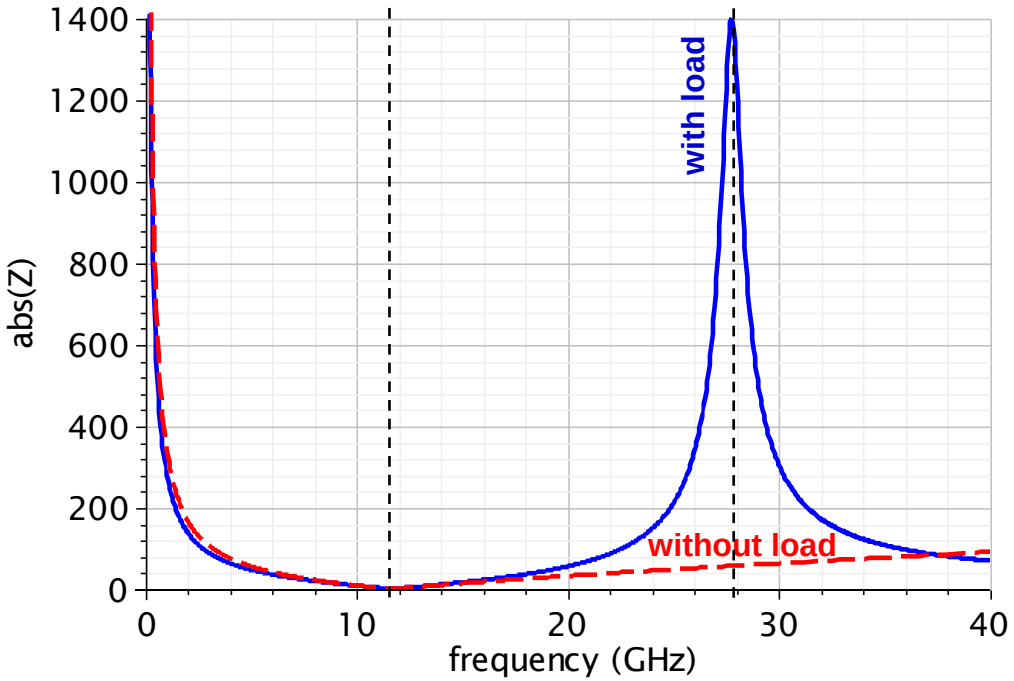

Figure 14: Absolute tank impedance series LC-tank

In the original oscillation frequency point, the required transconductance of the compensation network is very large, since the total tank impedance at that point is equal to the series resistance of the inductor R_S, which is very small (2.35 Ω).

In the second oscillation frequency point, the tank impedance is a lot larger. This means that the circuit will oscillate much easier in the second oscillation frequency point, because the transconductance needed there is a lot smaller than for the original oscillation frequency of the tank.

To confirm that now two oscillation frequencies exist, let's take a look at the expression for the unloaded tank impedance. The unloaded tank impedance also can be written in terms of the oscillation angular frequency $\omega_1 = \frac{1}{\sqrt{LC}}$ and the quality factor of the tank at the oscillation frequency, which is equal to: $Q_1 = \frac{\omega_1 L}{R_S} = \frac{1}{\omega_1 C R_S}$.

$$Z_{tank,ser}(\omega) = R_S + j\left(\omega L - \frac{1}{\omega C}\right) \tag{2.37}$$

$$Z_{tank,ser}(\omega) = R_S\left\{1 + jQ_1\left(\frac{\omega}{\omega_1} - \frac{\omega_1}{\omega}\right)\right\} \tag{2.38}$$

The loaded tank impedance now can be written as:

$$Z_{tank,ser,loaded}(\omega) = Z_{tank,ser} // Z_{load} \tag{2.39}$$

$$Z_{tank,ser,loaded}(\omega) = \frac{R_S\left\{1 + jQ_1\left(\frac{\omega}{\omega_1} - \frac{\omega_1}{\omega}\right)\right\}}{j\omega R_S C_{load}\left\{1 + jQ_1\left(\frac{\omega}{\omega_1} - \frac{\omega_1}{\omega}\right)\right\} + 1} \tag{2.40}$$

For $\omega_1 = \frac{1}{\sqrt{LC}}$ the loaded tank impedance is:

$$Z_{tank,ser,loaded}(\omega_1) = \frac{R_S}{j\omega_1 R_S C_{load} + 1} \approx R_S \ (if\ \omega_1 R_S C_{load} \ll 1) \tag{2.41}$$

This shows that for the original oscillation frequency the imaginary part of the loaded tank impedance approximately is zero ($if\ \omega_1 R_S C_{load} \ll 1$). The circuit therefore will oscillate with oscillation (angular) frequency ω_2 if the transconductance of the compensation network is approximately equal to the inverse of the series resistance R_S.

Solving the equation for the loaded tank impedance analytically shows that the second (angular) oscillation frequency can be written as:

$$\omega_2 \approx \frac{1}{\sqrt{L\frac{CC_{load}}{C + C_{load}}}} \tag{2.42}$$

The absolute value of the loaded tank impedance for the second oscillation frequency can be written as:

$$\left|Z_{tank,ser,loaded}(\omega_2)\right| \approx \frac{LC}{R_S C_{load}(C + C_{load})} (= 1.4k\Omega) \tag{2.43}$$

$$(if\ R_S^2 CC_{load} \ll LC\ \&\ if\ R_S^2 C_{load}^2 \ll LC)$$

So the series LC-tank will oscillate with (angular) frequency ω_2 if the transconductance of the compensation network is equal to the inverse of the absolute value of the loaded tank impedance.

Let's conclude this section with a resume of the oscillation criteria for both oscillation frequencies of the series LC-tank loaded with a fixed capacitance:

1. $\omega_1 = \frac{1}{\sqrt{LC}}$ (2.44)
2. $g_m \approx \frac{1}{R_S}$ (2.45)
1. $\omega_2 \approx \frac{1}{\sqrt{L\frac{CC_{load}}{C+C_{load}}}}$ (2.46)
2. $g_m \approx \frac{R_S C_{load}(C+C_{load})}{LC}$ (2.47)

2.3.2. Conditions to keep oscillation frequency fixed despite of spread

In the previous section we've seen that loading a series or parallel LC-oscillator with a fixed capacitance can shift the oscillation frequency or can give an extra oscillation frequency. The goal however is to achieve an oscillation frequency of 11.7 GHz for the LC-oscillator *within the presence of a capacitive load*. In this section therefore the goal is to find out which range of capacitive load can be used and still be able to achieve an oscillation frequency of 11.7 GHz with the loaded LC-oscillator. The tank capacitance therefore will be adapted, such that the oscillation frequency of the loaded tank will be kept equal to the desired 11.7 GHz.

Since the VCO has to be able to compensate (process) spread in the tank- and load capacitance, also will be analyzed what the required variation in tank capacitance has to compensate spread in the tank- and load capacitance. At first only spread in the load capacitance will be taken into account and later on also spread in the tank capacitance. At the end of this section both contributions will be added up and an expression for the total required tank capacitance variation will be given

Parallel LC-tank

First we analyze the parallel LC-tank. In the previous section we've seen that the total capacitance of the loaded parallel LC-tank is equal to the sum of the tank capacitance and the load capacitance:

$$C_{total} = C_{tank,par} + C_{load} \tag{2.48}$$

To achieve an oscillation frequency of 11.7 GHz this must be equal to 463 fF (see 2.20) and can be rewritten as function of the capacitive load in:

$$C_{tank,par} = C_{total} - C_{load} = 463\,fF - C_{load} \tag{2.49}$$

To visualize this dependency, the function is plotted in Figure 15. On first hand we're able to see that for a capacitive load larger than the needed total capacitance (in this case 463 fF) the tank capacitance has to be negative, which isn't feasible.

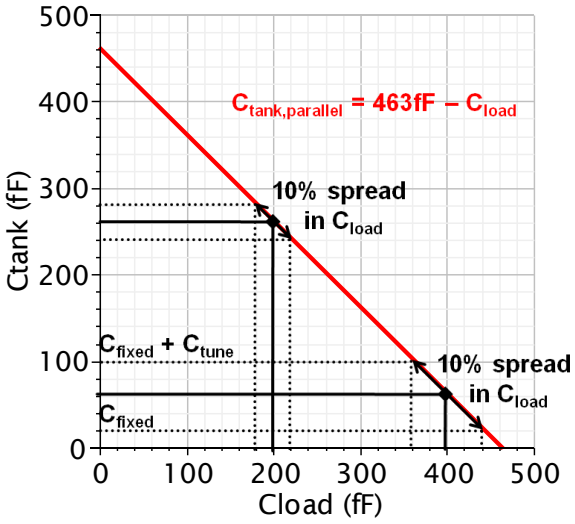

Figure 15: Tank capacitance and load capacitance parallel LC-tank for fixed oscillation frequency of 11.7 GHz

The capacitive load of the LC-oscillator won't be constant however. The capacitive load of the LC-oscillator was a model for the capacitive input of the mixer. This input capacitance is voltage dependent and since the oscillator voltage changes over time, the input capacitance of the mixer also will vary with time. Also process spread will give some variation in input capacitance of the mixer.

If the load capacitance varies, this has to be compensated by adapting the tank capacitance to keep the oscillation frequency fixed. Therefore the tank capacitance will be modeled from now on as a fixed part (C_{fixed}) and a variable part (C_{tune}) as shown in Figure 16.

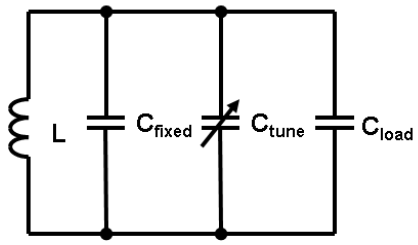

Figure 16: Parallel LC-tank with tuneable tank capacitance

How much the tank capacitance has to be able to vary depends on the capacitive load. The required tune capacitance is equal to the difference between the maximum and minimum capacitance. In the case of only spread in the load capacitance, it is proportional to the load capacitance (C_{load}) and the spread of the load capacitance (α_L):

$$C_{tune,par} = (1+\alpha_L)C_{load} - (1-\alpha_L)C_{load} = 2\alpha_L C_{load} \tag{2.50}$$

The required fixed capacitance becomes smaller for a larger load capacitance:

$$C_{fixed,par} = C_{total} - (1+\alpha_L)C_{load} \tag{2.51}$$

So the required tuning range of the tank capacitance will increase as the load capacitance increases:

$$(tuning\ range)_{par} = \frac{C_{tune,par}}{C_{fixed,par}} = \frac{2\alpha_L C_{load}}{C_{total} - (1+\alpha_L)C_{load}} \tag{2.52}$$

The required tuning range even will go to infinity if the load capacitance comes close to the required total capacitance:

$$tuning\ range \to \infty\ if\ C_{total} - (1+\alpha_L)C_{load} = 0 \tag{2.53}$$

$$\leftrightarrow C_{load,max,par} = \frac{C_{total}}{(1+\alpha_L)} \approx C_{total}(1-\alpha_L)\ (for\ \alpha_L \ll 1) \tag{2.54}$$

The expression above shows that for a parallel LC-oscillator the load capacitance must be smaller than approximately the required total capacitance in the tank minus the spread of the load capacitance.

Consider for example a spread of 10 % in the load capacitance ($\alpha_L = 0.1$). Since the total required tank capacitance is 463 fF, this results in:

$$C_{tune,par} = 0.2C_{load} \tag{2.55}$$

$$C_{fixed,par} = 463\ fF - 1.1C_{load} \tag{2.56}$$

$$(tuning\ range)_{par} = \frac{C_{tune,par}}{C_{fixed,par}} = \frac{0.2C_{load}}{463\ fF - 1.1C_{load}} \tag{2.57}$$

The required tuning range as a result of 10 % spread in the load capacitance is plotted in Figure 17.

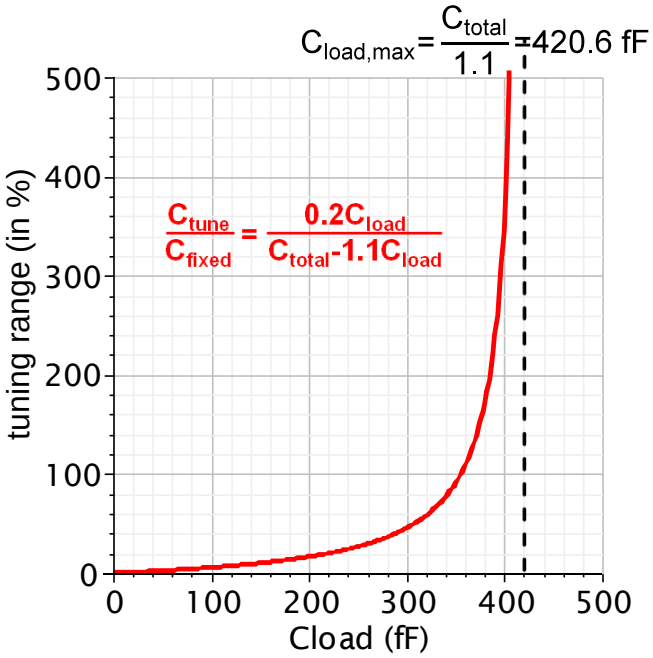

Figure 17: Required tuning range tank capacitance of parallel LC-tank for 10 % spread in load capacitance and a fixed oscillation frequency of 11.7 GHz

As expected the required tuning range will go to infinity for a capacitive load of $\frac{C_{total}}{1.1} = 420.6\ fF$. As the capacitive load approaches zero, the required tuning range as a result of spread in the load capacitance will go to zero, because the contribution of the load capacitance to the total capacitance becomes negligible.

Series LC-tank

For the series LC-tank the same analysis has been done as for the parallel LC-tank. In the previous paragraph we've seen that the series LC-tank has two possible oscillation frequencies. The first oscillation frequency of $\omega_1 = \frac{1}{\sqrt{LC}}$ depends only on the tank capacitance and therefore spread in the load capacitance won't have any effect on the oscillation frequency. The second oscillation frequency of $\omega_2 \approx \frac{1}{\sqrt{L\frac{CC_{load}}{C+C_{load}}}}$ however will be affected by spread in the load capacitance. Let's see what this means for the required tuneability of the tank capacitance.

The total capacitance of the loaded series LC-tank is equal to the series network of the load capacitance and the tank capacitance:

$$C_{total} = \frac{C_{tank,ser}C_{load}}{C_{tank,ser} + C_{load}} \tag{2.58}$$

With the used inductor of 400 pH and a required oscillation frequency of 11.7 GHz this has to be equal to 463 fF. Rewritten as a function of the capacitive load this gives for the required tank capacitance:

$$C_{tank,ser} = \frac{C_{load}C_{total}}{C_{load} - C_{total}} = \frac{C_{load} \cdot 463\ fF}{C_{load} - 463\ fF} \tag{2.59}$$

To give more insight it has been plotted in Figure 18. For a very large capacitive load, the required tank capacitance will approximate the total required capacitance. This makes sense, because in a series network of capacitances the total capacitance is dominated by the smallest capacitance. Furthermore if the capacitive load is close to the required total capacitance, then the tank capacitance has to be very large.

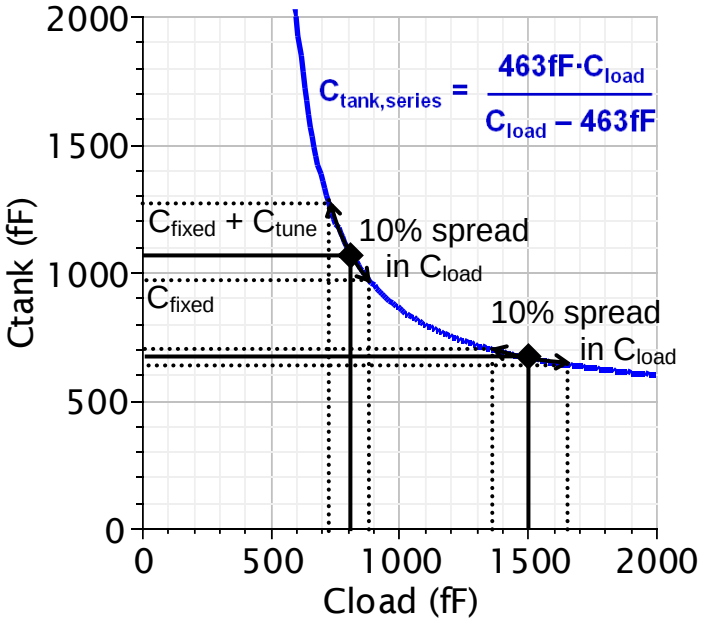

Figure 18: Tank capacitance and load capacitance series LC-tank for fixed oscillation frequency of 11.7 GHz

The tank capacitance in the series tank also has to be able to compensate for variations in the load capacitance. The model of the tank capacitance in the series LC-tank therefore is subdivided in a fixed capacitance (C_{fixed}) and a variable capacitance (C_{tune}) as can be seen in Figure 19. If for example the load capacitance is 800 fF and had 10 % spread, then it can be seen in Figure 18 that the required variation in tank capacitance will be around 300 fF. If the load capacitance is 1.5 pF, then the required variation in tank capacitance is less strict, i.e. around 70 fF. This shows that for a series LC-tank a larger load capacitance will give a more relaxed requirement on the variation in tank capacitance.

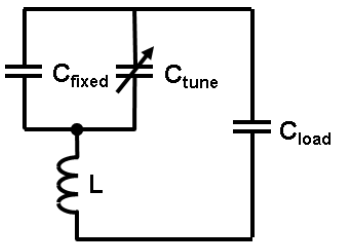

Figure 19: Series LC-tank with tuneable tank capacitance

To show the validity of this statement let's analyze a more generalized expression for the required fixed capacitance ($C_{fixed,ser}$) as function of the load capacitance (C_{load}) and the spread of the load capacitance (α_L):

$$C_{fixed,ser} = \frac{C_{load}(1+\alpha_L)C_{total}}{C_{load}(1+\alpha_L) - C_{total}} = \frac{C_{total}}{1 - \frac{C_{total}}{C_{load}(1+\alpha_L)}} \tag{2.60}$$

This expression confirms that the required fixed capacitance becomes smaller for larger load capacitance.

The required variation in tank capacitance ($C_{tune,ser}$) as a result of spread in the load capacitance (α_L) can be written as:

$$C_{tune,ser} = C_{tank,max,ser} - C_{tank,min,ser} \tag{2.61}$$

$$C_{tune,ser} = \frac{C_{load}(1-\alpha_L)C_{total}}{C_{load}(1-\alpha_L) - C_{total}} - \frac{C_{load}(1+\alpha_L)C_{total}}{C_{load}(1+\alpha_L) - C_{total}} \tag{2.62}$$

$$C_{tune,ser} = \frac{2\alpha_L C_{load} C_{total}^2}{\{C_{load}(1-\alpha_L) - C_{total}\}\{C_{load}(1+\alpha_L) - C_{total}\}} \tag{2.63}$$

$$C_{tune,ser} = \frac{\frac{2\alpha_L}{(1+\alpha_L)} C_{total}^2}{\left\{1 - \frac{C_{total}}{C_{load}(1+\alpha_L)}\right\}\left\{1 - \frac{C_{total}}{C_{load}(1+\alpha_L)}\right\}} \tag{2.64}$$

For an increasing capacitive load, the denominator becomes larger and therefore the required variation in tank capacitance ($C_{tune,ser}$) will become smaller. This confirms what we've already seen in Figure 18.

The required tuning range for the series LC-tank as a result of spread in the load capacitance can be written as the ratio of the tuneable part of the tank capacitance and the fixed tank capacitance:

$$(tuning\ range)_{ser} = \frac{C_{tune,ser}}{C_{fixed,ser}} \tag{2.65}$$

$$(tuning\ range)_{ser} = \frac{\frac{2\alpha_L C_{load} C_{total}^2}{\{C_{load}(1-\alpha_L) - C_{total}\}\{C_{load}(1+\alpha_L) - C_{total}\}}}{\frac{C_{load}(1+\alpha_L)C_{total}}{C_{load}(1+\alpha_L) - C_{total}}} \tag{2.66}$$

$$(tuning\ range)_{ser} = \frac{2\alpha_L}{1+\alpha_L} \cdot \frac{C_{total}}{C_{load}(1-\alpha_L) - C_{total}} \tag{2.67}$$

This expression shows that for a large load capacitance the required tuning range as result of spread in the load capacitance will go to zero. The tuning range will go to infinity if the numerator of the required tuning range becomes zero. This is the case if the load capacitance comes in the vicinity of the required total capacitance:

$$(tuning\ range)_{ser} \to \infty\ if\ C_{load}(1-\alpha_L) - C_{total} = 0 \tag{2.68}$$

$$\leftrightarrow C_{load,min,ser} = \frac{C_{total}}{(1-\alpha_L)} \approx C_{total}(1+\alpha_L)\ (for\ \alpha_L \ll 1) \tag{2.69}$$

The previous expression shows that the load capacitance of the series LC-tank actually has a minimum, which depends on the total required capacitance (C_{total}) and the spread in load capacitance (α_L).

A numerical example will perhaps give more insight in the obtained expressions. For the application a total capacitance is required of 463 fF. Again 10 % spread in the load capacitance is assumed, this gives the following requirements on the tuneability of the tank capacitance:

$$C_{fixed,ser} = \frac{463\ fF \cdot C_{load}}{C_{load} - 421\ fF} \tag{2.70}$$

$$C_{tune,ser} = \frac{463\ fF \cdot C_{load}}{C_{load} - 514\ fF} - \frac{463\ fF \cdot C_{load}}{C_{load} - 421\ fF} \tag{2.71}$$

$$(tuning\ range)_{ser} = \frac{2}{11} \cdot \frac{463\ fF}{0.9C_{load} - 463\ fF} = \frac{93\ fF}{C_{load} - 514\ fF} \tag{2.72}$$

To confirm the expressions above for the fixed capacitance and the tune capacitance we'll take a look again at Figure 18. For a load capacitance of 1.5 pF, from the expressions above the required fixed and tune capacitance have to be:

$$C_{fixed,ser} = \frac{463\ fF \cdot 1500\ fF}{1500\ fF - 421\ fF} = 644\ fF \tag{2.73}$$

$$C_{tune,ser} = \frac{463\ fF \cdot 1500\ fF}{1500\ fF - 514\ fF} - \frac{463\ fF \cdot 1500\ fF}{1500\ fF - 421\ fF} = 61\ fF \tag{2.74}$$

To confirm the expression (2.72) found for the required tuning range, the required tuning range for the tank capacitance in the series LC-tank is plotted in Figure 20 for 10 % spread in load capacitance. It is clear that for a capacitive load of 514 fF the required tuning range will go to infinity, since the denominator then becomes zero. For a capacitive load going to infinity, the required tuning range of the tank capacitance will go to zero, as expected.

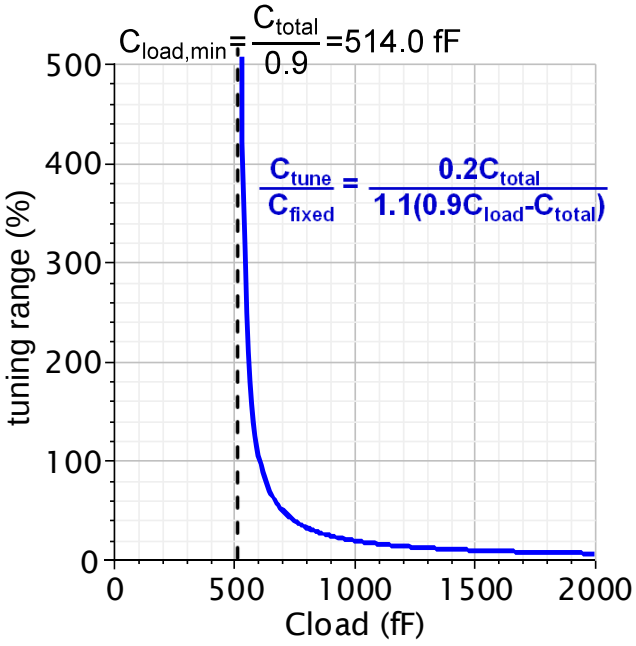

Figure 20: Required tuning range tank capacitance series LC-tank for 10 % spread in load capacitance and fixed oscillation frequency of 11.7 GHz

Spread in tank capacitance

Not only spread in load capacitance has to be compensated, but also spread in the tank capacitance has to be compensated. In the previous part of this section the requirements on the variation in tank capacitance is analyzed for spread in load capacitance. The final requirements for the tuning range of the tank capacitance will be the result of the combined effects of spread in the load- and the tank capacitance itself. The effect of spread in the tank capacitance on the required tuning range of the tank capacitance is very straightforward.

The following analysis yields for both cases of the parallel LC-tank and the series LC-tank. Consider the spread in the tank capacitance is given by α_T. The required fixed tank capacitance in this case can be written as:

$$C_{fixed} = (1 - \alpha_T)C_{lank} \tag{2.75}$$

The required variation in tank capacitance as a result of spread in tank capacitance is equal to twice the spread in the tank:

$$C_{tune} = 2\alpha_T C_{lank} \tag{2.76}$$

And the required tuning range of the tank capacitance as a result of spread in the tank capacitance can be written as the ratio between tuneable and fixed tank capacitance:

$$(tuning\ range)_{\alpha_T} = \frac{C_{tune}}{C_{fixed}} = \frac{2\alpha_T C_{lank}}{(1 - \alpha_T)C_{lank}} = \frac{2\alpha_T}{(1 - \alpha_T)} \tag{2.77}$$

So the required tuning range as a result of spread in the tank capacitance is independent of the tank capacitance and therefore constant for a given spread. If the spread in tank capacitance is 10 %, the required tuning range will be:

$$(tuning\ range)_{\alpha_T=0.1} = \frac{2}{9} \approx 22.2\ \% \tag{2.78}$$

Combining the requirements for the tuning range as a result of spread in tank- and load capacitance will result in the plot given in Figure 21. Note that both contributions of spread can be assumed independent and they therefore can be added up to each other. For both the parallel- and series LC-tank the required tuning range is plotted in Figure 21. For zero load capacitance for the parallel LC-tank now the required tuning range is at its minimum of 22.2%. For the series LC-tank the required tuning range for the series LC-tank will be at its minimum of 22.2 %, for a load capacitance which goes to infinity.

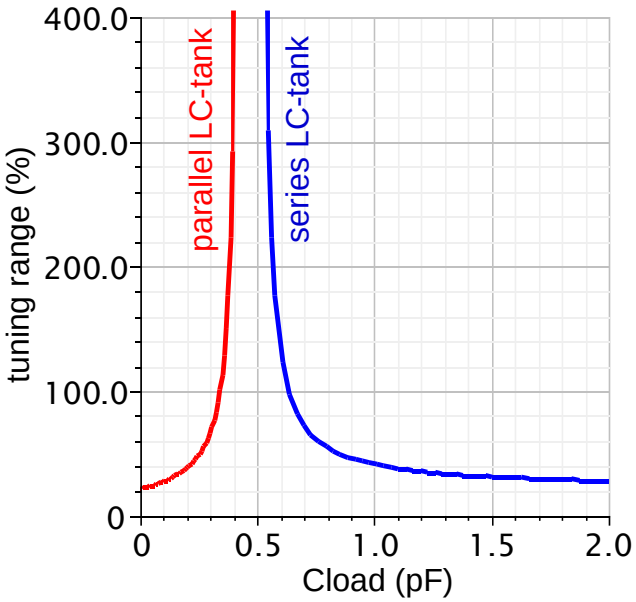

Figure 21: Required tuning range tank capacitance for 10 % spread in load- and tank capacitance and for fixed oscillation frequency of 11.7 GHz

Let's conclude this section with a resume of the requirements on the tuning range of the tank capacitance as a result of both spread in the tank- and load capacitance.

For a parallel LC-tank the required tuning range is equal to:

$$(tuning\ range)_{par} = \frac{2\alpha_L C_{load}}{C_{total} - (1+\alpha_L)C_{load}} + \frac{2\alpha_T}{(1-\alpha_T)} \tag{2.79}$$

To give a numerical example: for a total capacitance of 463 fF, 10 % spread in total and tank capacitance and a load capacitance of 200 fF this gives a required tuning range for the parallel LC-tank of almost 40 %:

$$(tuning\ range)_{par} = 22.2\ \% + 16.5\ \% = 38.7\ \% \tag{2.80}$$

For a series LC-tank required tuning range is equal to:

$$(tuning\ range)_{ser} = \frac{2\alpha_L}{1+\alpha_L} \cdot \frac{C_{total}}{C_{load}(1-\alpha_L) - C_{total}} + \frac{2\alpha_T}{(1-\alpha_T)} \tag{2.81}$$

For a total capacitance of 463 fF, 10 % spread in total and tank capacitance and a load capacitance of 2 pF this gives a required tuning range of almost 30 % for the series LC-tank.:

$$(tuning\ range)_{par} = 22.2\ \% + 6.3\ \% = 28.5\ \% \tag{2.82}$$

These numerical examples confirm the results already shown in Figure 21.

2.3.3. Loading CMOS LC-oscillator with fixed capacitance

In this last section of paragraph 2.3 the LC-oscillator is implemented in CMOS 65 nm. A choice will be made on the type of LC-tank and a topology for the compensation network. With use of the oscillation conditions found for the macro model in paragraph 2.2, component values for the CMOS oscillator are chosen such that it will give an oscillation frequency of 11.7 GHz. The CMOS LC-oscillator will be loaded with a fixed capacitive load of 100 fF and effects on the VCO-frequency will be simulated. The simulation results will be used to verify the analytical results already obtained in section 2.3.1.

Choice between parallel- and series LC-tank

Theoretically a parallel- and series LC-tank will give the same oscillation frequency, if in both cases the same component values are used. But we've seen in section 2.3.1 that this will change if the LC-tank is loaded with a fixed capacitance. In that case the oscillation frequency of the series and parallel LC-tank will differ. For the series LC-tank even two oscillation frequencies points exist. The analytical results showed that for the series LC-tank the first oscillation frequency is equal to the original tank frequency and will not be affected by capacitive loading. However the required transconductance for the series LC-tank to oscillate in that oscillation point has to be equal to the inverse of the series resistance of the tank. The series resistance of an LC-tank is normally largely determined by the series resistance of the inductor. The series resistance of an on chip inductor is normally in the order of a few ohms. That makes that the required transconductance would have to be very large. To give an example: for an inductor of 400 pH with a series resistance of 2.35 Ω, the required transconductance of the compensation network has to be equal to: $g_m = \frac{1}{2.35} = 426\,mS$ (or even momentarily larger than that to assure start-up). Such a large transconductance will give unrealistic demands on the bias current and width of the transistors. For example a transistor with a width of 600 µm (and minimum length of 65nm) and a bias current of 100mA will give a transconductance of ~450 mS. The parasitic capacitances of the transistor then will become too large (in the order of 200/300 fF)

The second oscillation frequency point of the series LC-tank will also not be feasible for this application. We've seen in 2.3.2 that oscillation at the desired 11.7 GHz isn't possible for a capacitive load smaller than the required total capacitance in the tank. With an inductor of 400 pH, this means that the series tank can't give the desired oscillation frequency for a capacitive load smaller than 463 fF. Since the input capacitance of the mixer is estimated at 100 fF, the series LC-tank will not be able to resonate at 11.7 GHz if it is loaded with the mixer. It is however possible to add extra load capacitance to increase the capacitive load above the boundary of 463 fF. This could also be a possible implementation, however for this thesis a more straightforward choice on the parallel LC-tank has been made for the implementation of the LC-oscillator in CMOS. This choice for the parallel LC-tank has also been influenced by the used topology for the CMOS oscillator used by Paul Geraedts for his satellite receiver project. If possible, the same topology would be preferable to keep this feasibility research in relevance for the application.

Chosen topology for compensation network

To keep this feasibility study in relevance to the application, the used XCP topology in this feasibility research is similar to the topology Paul Geraedts will use in the satellite receiver project. The used topology is shown in Figure 22.

The voltage room for the circuit is determined by the bias voltage (V_{B1}), connected to the center tapping of the inductor. The oscillation frequency is tuneable with a varactor bank, modeled here as one variable capacitor. The varactors in the varactor bank will be digitally driven with a voltage equal to the bias voltage V_{B1} or tied to ground. To assure the capacitances in the varactor bank won't behave very unlinear, the level of the bias voltage is chosen at 0.9 V and a maximum voltage swing of 1.2 V across the output nodes will be allowed. All the losses of the tank are modeled in the parallel resistance (R_P). The bias current I_{bias} for the cross-coupled pair is controlled by a variable resistor R_{bias}. In the current-limiting region the tank amplitude will be proportional to the bias current and the parallel resistance of the tank [8]:

$$V_{tank} \approx I_{bias} R_P \tag{2.83}$$

The tank amplitude therefore will be controllable with the variable resistor R_{bias} that controls the bias current I_{bias}. This property of amplitude control is also used for starting up of the oscillator. At start-up the bias current is increased, such that the transconductances of the cross-coupled pair can become larger than necessary for steady state oscillation.

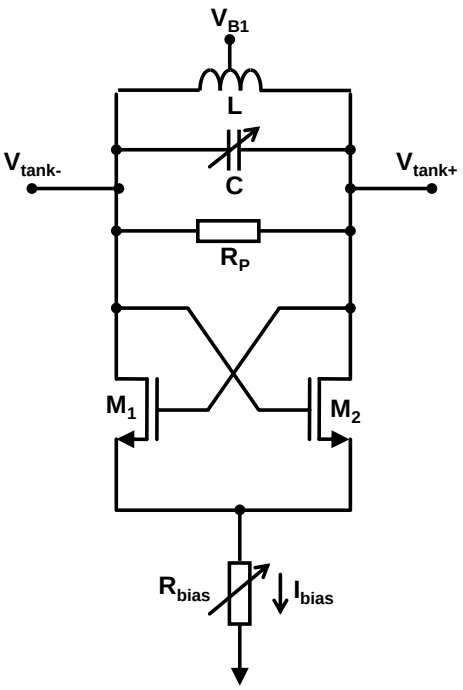

Figure 22: NMOS XCP with parallel LC-tank

Design NMOS cross-coupled pair with parallel LC-tank

To find the right component values for the design of an LC-oscillator with a NMOS XCP and a parallel LC tank, let's take a look again at the most important requirements for the oscillator and the oscillation criteria, as already discussed in 0 and 2.2.1 respectively.

Requirements oscillator:

- Fixed oscillation frequency of 11.7 GHz
- Tank amplitude: 0.6 V (1.2 V_{pp})
- Common mode level: 600 mV

Oscillation criteria parallel LC-tank with ideal compensation network:

1. $g_m = \frac{1}{|Z_{tank,par}(\omega_0)|} = \frac{1}{R_P}$ (2.84)

2. $\omega_0 = \frac{1}{\sqrt{LC}}$ (2.85)

For the LC-tank to give an oscillation frequency of 11.7 GHz, an inductor is used of 400 pH and a total capacitance of 463 fF is used. Using the formula of the second oscillation criterion, this will give the required oscillation frequency of 11.7 GHz.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{400 \cdot 10^{-12} \cdot 463 \cdot 10^{-15}}} = 11.7\ GHz \quad (2.86)$$

When neglected body-effect and output resistances, the XCP behaves as a negative resistance with the value:

$$R_{XCP} = \frac{-2}{g_m} \quad (2.87)$$

The above formula yields for the case that equal transistors are used in the cross-coupled pair. g_m represents here the transconductance of one transistor.

For steady state oscillation the absolute value of this negative resistance has to be equal to the parallel resistance of the tank. The losses in the tank modeled by R_P then will be compensated with the active XCP compensation network. This will lead to the expression for the required transconductance of the transistors of the cross-coupled pair for steady state oscillation:

$$|R_{XCP}| = R_P \rightarrow \frac{2}{g_m} = R_P \rightarrow g_m = \frac{2}{R_P} \quad (2.88)$$

This expression can also be obtained by using the formula of the first oscillation criterion (2.84).

For the simulations the same value for the parallel resistance R_P is used as for the analysis of the parallel tank in section 2.3.1. The value for R_P of 368 Ω represents an effective quality factor of the tank of Q=12.5 (see formula 2.25). The requirement for the transconductance of the transistors of the cross-coupled pair then becomes:

$$g_m = \frac{2}{R_P} = \frac{2}{368\ \Omega} = 5.4\ mS \quad (2.89)$$

Assuming the tank amplitude isn't yet voltage limited by the bias voltage of the tank, using equation 2.83 a bias current of ~1.6 mA will be needed for a tank amplitude of 0.6 V:

$$I_{bias} \approx \frac{V_{tank}}{R_P} = \frac{0.6\,V}{368\,\Omega} = 1.6\,mA \tag{2.90}$$

The length of the transistors is chosen at two times the minimum length (120nm) for a larger output resistance and for a lower 1/f noise contribution of the cross-coupled pair. A small output resistance will decrease the effective quality factor of the tank. The 1/f noise of the transistors will fold back around the oscillation frequency and will increase the ($1/f^3$ region of the) phase noise.

The voltage room for the transistors is determined by the bias voltage of the tank, the voltage swing at each output node and the voltage drop across the resistor R_{bias}. The bias voltage of the tank is 0.9 V and the voltage swing at each output node is +/- 0.3 V, this leaves 0.6 V voltage room for the transistors and the resistor R_{bias}. If this is equally divided, there will be 0.3 V voltage room for the transistors. It is prefereable to bias the transistors in saturation for a high transconductance and a high output resistance. A high W/L ratio is needed for a small overdrive voltage. For a small overdrive voltage a large W/L ratio is needed. The width however can't become too large, because the parasitic gate-source and gate-drain capacitances add up to the tank capacitance. Since only 463 fF capacitance room is available, the transistors can't become too large. The width of the transistors is therefore chosen at 120 µm. This will give a transconductance of 12 mS, if the tank amplitude is around zero and half the bias current flows through each transistor.

The required common mode level of 600 mV doesn't agree with the common mode level of the tank, which is equal to the bias voltage of the tank of 900 mV. Therefore AC-couple capacitors are added at each output to be able to control the common mode voltage independent of the bias voltage of the tank. If the tank is loaded with a capacitive load, the tank voltage will be divided between the load capacitor and the couple capacitor. To avoid a large decrease in voltage swing across the load capacitor as a result of this voltage division, the couple capacitors are chosen 20 times larger than the estimated load capacitance. This will result in: $\frac{1}{20+1} \cdot 100\,\% = 4.8\,\%$ decrease in voltage swing across the load capacitance. A large resistor of 10 kΩ is used to avoid leakage of signal current to the applied common mode bias voltage.

It has to be kept in mind that realizing capacitive coupling on-chip, already roughly 10 % of the capacitance will be present in the form of a parasitic capacitance to ground. So already as a result of on-chip parasitic capacitances to ground the AC-coupling will give a decrease in voltage swing.

The implemented LC-oscillator in CMOS with all the chosen component values and device parasitics is shown in Figure 23. Note that the bias current is somewhat larger than calculated in equation 2.90. This is caused by the output resistances of the transistors, which will lower the effective parallel resistance of the tank and therefore also the tank amplitude. A larger bias current therefore is needed to give the desired tank amplitude. Entering the voltage limited region can also be a reason of a lower tank voltage, since the tank amplitude then becomes limited by the common mode bias voltage of 900mV.

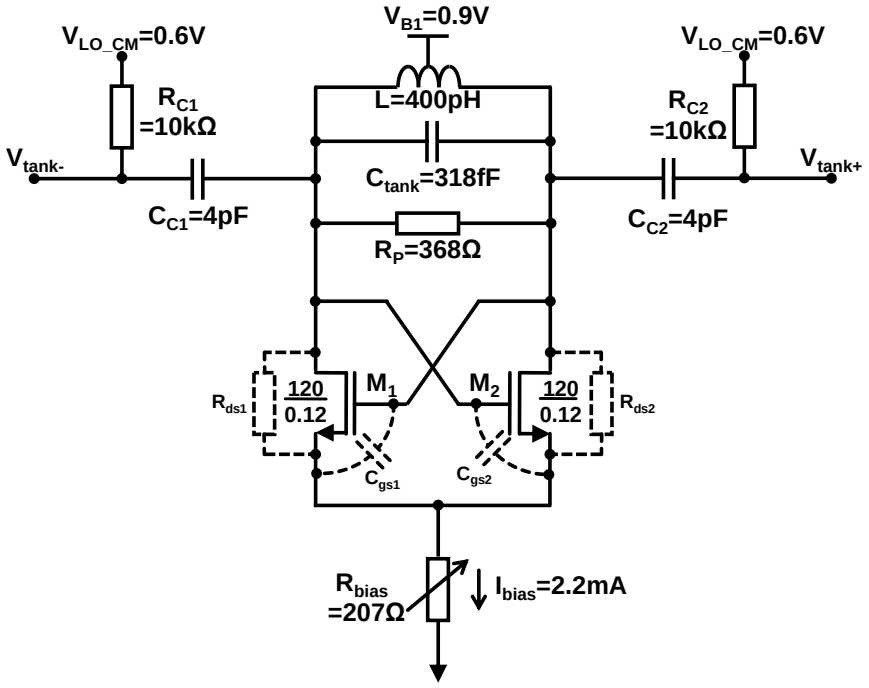

Figure 23: CMOS LC-oscillator with component values and parasitics

Note that the tank capacitance is chosen lower as a result of the parasitic capacitance of the cross-coupled pair. The total parasitic capacitance introduced by the gate-source – (and in a less extent the gate-drain capacitances) of the cross-coupled pair transistors is estimated from simulation results at around 145 fF. The tank capacitance is chosen such that the total capacitance equals the desired 463 fF.

Simulation loading effect on VCO-frequency of CMOS oscillator

At first the CMOS oscillator is simulated without load capacitance to verify the oscillation frequency and the tank amplitude. After that, the designed CMOS oscillator will be loaded with a fixed capacitance of 100 fF. and effects on the VCO-frequency will be simulated. This has been done to verify the obtained analytical results with the macro model of the loaded LC-oscillator in section 2.3.1.

1. CMOS oscillator without load

The simulation results of the start-up behavior of the designed NMOS XCP with parallel LC tank are shown in Figure 24. It can be seen that the CMOS oscillator after a start-up time of approximately 3 ns is settled to the desired oscillation frequency of 11.7 GHz. In the left top part of Figure 24 the tank voltage at both output nodes and the differential tank voltage for one oscillation period is plotted. In the left bottom part the variation in the bias current is plotted for one oscillation period. It can be seen that the shape of the waveform at both tank outputs isn't a well shaped sine wave. The differential tank at the contrary is varying as a well shaped sine wave. After settling the differential tank amplitude is equal to 600 mV (1.2 V_{pp}). The average bias current is 2.21 mA and varies with twice the oscillation frequency with amplitude ~0.29 mA. In the simulation the LC-tank is started up with a current pulse at t = 0 ns.

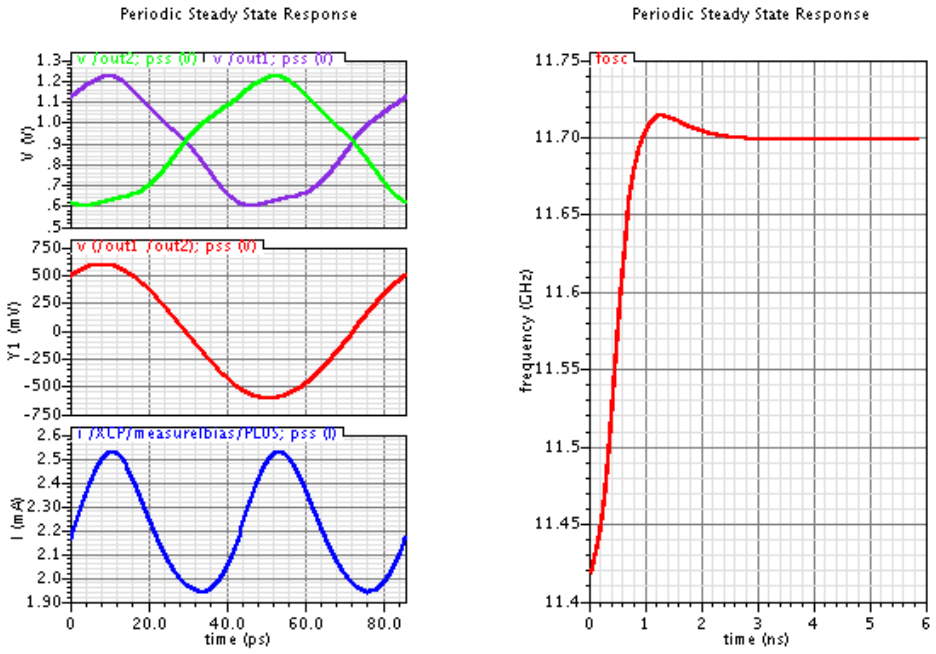

Figure 24: Simulation results designed NMOS XCP with parallel LC-tank

2. CMOS oscillator with fixed capacitive load

The CMOS oscillator is now loaded with a fixed capacitive load of 100 fF. This has been done by loading both output terminals of the oscillator with a capacitor of 200 fF as can be seen in Figure 23. The resulting capacitive load between both oscillator output terminals will be the series network of both capacitors. This will be equal to half the capacitance seen at each output terminal if both capacitances are equal. Note that the effective added capacitance to the tank includes the coupling capacitors as well. But since these capacitors are a factor of 20 larger, the added capacitance will still be dominated by the load capacitance. That is, the effective added capacitance equals the series network of the coupling capacitances and the load capacitances:

$$\frac{1}{C_{effective\ added}} = \frac{1}{C_1} + \frac{1}{C_{C1}} + \frac{1}{C_2} + \frac{1}{C_{C2}} = \frac{2}{200\ fF} + \frac{2}{4\ pF} \tag{2.91}$$

$$C_{effective\ added} = \frac{20}{21} \cdot \frac{1}{2} \cdot 200\ fF = 95.2\ fF \tag{2.92}$$

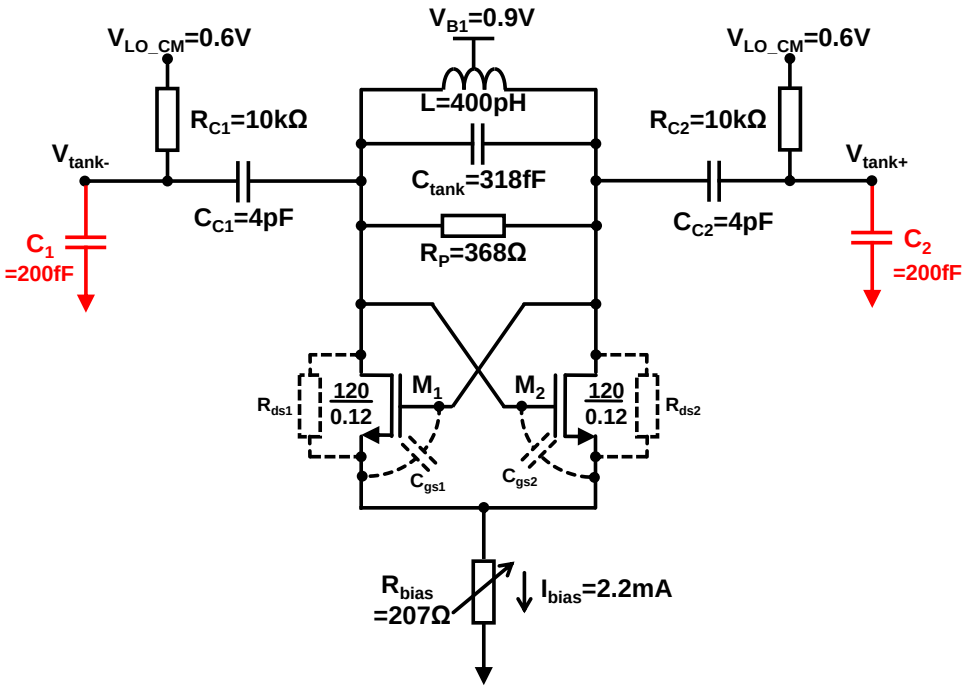

Figure 25: CMOS LC-oscillator loaded with capacitive load of 100 fF

Simulation results of the loaded CMOS oscillator are shown in Figure 26. In the right part of the figure, it can be seen that the oscillation frequency of the loaded CMOS LC-oscillator is shifted down to 10.63 GHz. This confirms the analytical results obtained earlier in section 2.3.1. In the left top part of the figure the tank amplitude is plotted. The tank amplitude is decreased with 7.6 % to 555 mV (1.11 V_{pp}). The decrease in tank amplitude is mainly caused by the voltage division between the coupling capacitance and the loading capacitance ($\frac{1}{20+1} \cdot 100\ \% = 4.8\ \%$). Also it can be seen that the bias current is slightly decreased and the shape of the varying bias current has changed, which is now not symmetrical anymore.

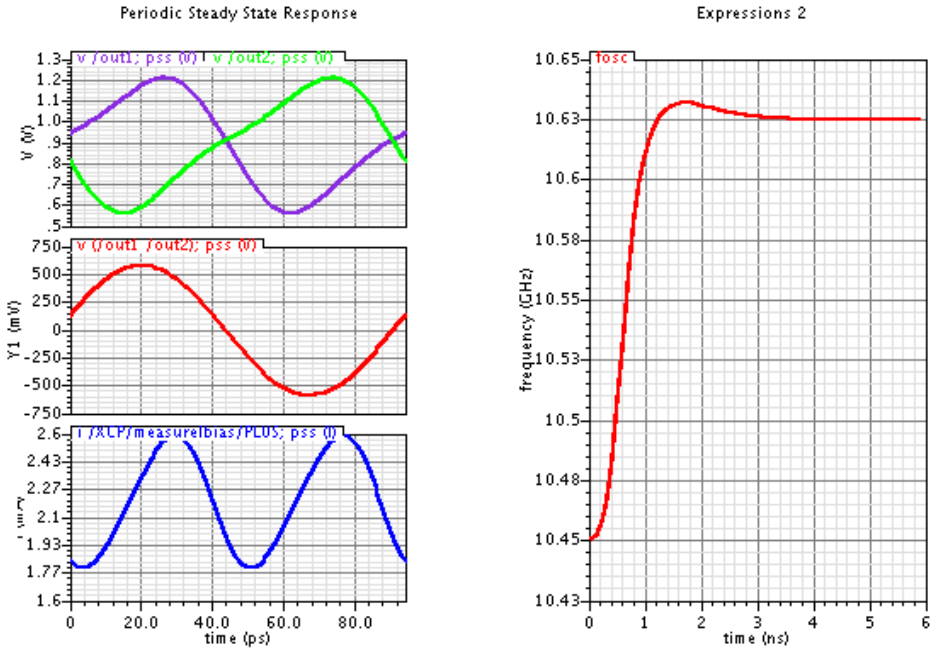

Figure 26: Simulation results CMOS LC-oscillator with capacitive load of 100 fF

2.4 LC-oscillator loaded with mixer

In the previous paragraph a CMOS parallel LC-oscillator was designed for an oscillation frequency of 11.7 GHz. The oscillation frequency shifted down to a lower frequency as a result of a capacitive load. It is however the goal to keep a fixed oscillation frequency of 11.7 GHz, even when a capacitive load is present, such as the mixer. In this paragraph therefore the CMOS LC-oscillator is designed to give the desired oscillation with taken into account the capacitive load of the mixer. The tank capacitance and the bias current will be adapted to maintain the requirements for the oscillator in the case of loading it with a mixer.

To be able to incorporate the input capacitance into the total capacitance of the LC-tank, the input capacitance of the used mixer has to be accurately determined. The used mixer is the BLIXER topology proposed by Blaakmeer et al [1]. The BLIXER topology consists of a Balun LNA and an I/Q mixer as can be seen in Figure 27. Simulations have been run to determine the exact input capacitance of the LO-ports, when driven the BLIXER with ideal quadrature sine wave oscillator signals. In section 2.4.1 we'll see that the input capacitance will be (nonlinear) varying with the voltage and therefore also will vary periodically in time.

In 2.4.2 the CMOS oscillator will be loaded with the BLIXER (and adapted to meet the requirements of the oscillator). The performance will be compared with the CMOS oscillator without load and with an ideal capacitive load equal to the effective input capacitance of the BLIXER.

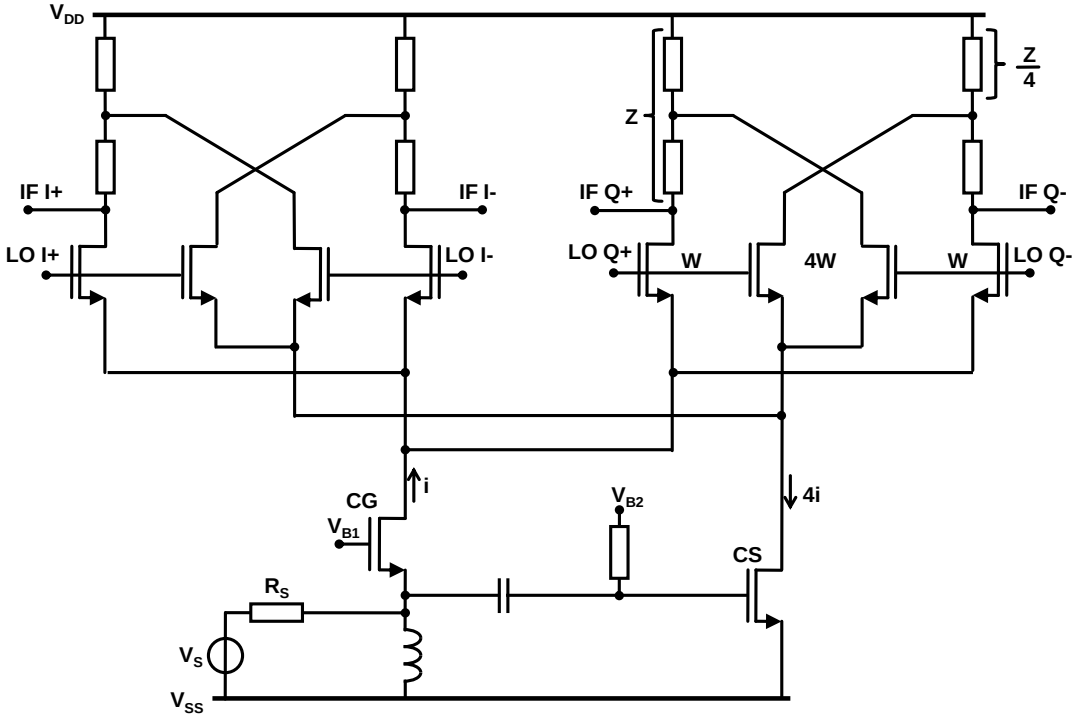

Figure 27: Basic BLIXER topology consisting of a Balun LNA and an I/Q Mixer

2.4.1 Effect varying capacitive load

Until now the LO-input capacitance of the mixer is modeled by two capacitances to ground. Earlier in this thesis the total input capacitance between the two oscillator terminals was estimated at 100 fF. We'll see in this section that it was a bit of an optimistic estimate in the case of the BLIXER.

The input capacitance of one of the LO-ports of the BLIXER will vary with the applied oscillator voltage, but will also be affected by the time-varying oscillator signals on the other LO-ports. The varying input capacitance of each of the LO-ports will therefore be estimated during normal operation of the mixer. The mixer is driven with quadrature sine wave oscillator signals with amplitude of 600 mV and a common mode level of 600 mV. The input capacitance is simulated with the use of the capacitance table output parameters of a transient analysis. The capacitances seen at each LO-input port have been plotted for one oscillation period in Figure 28.

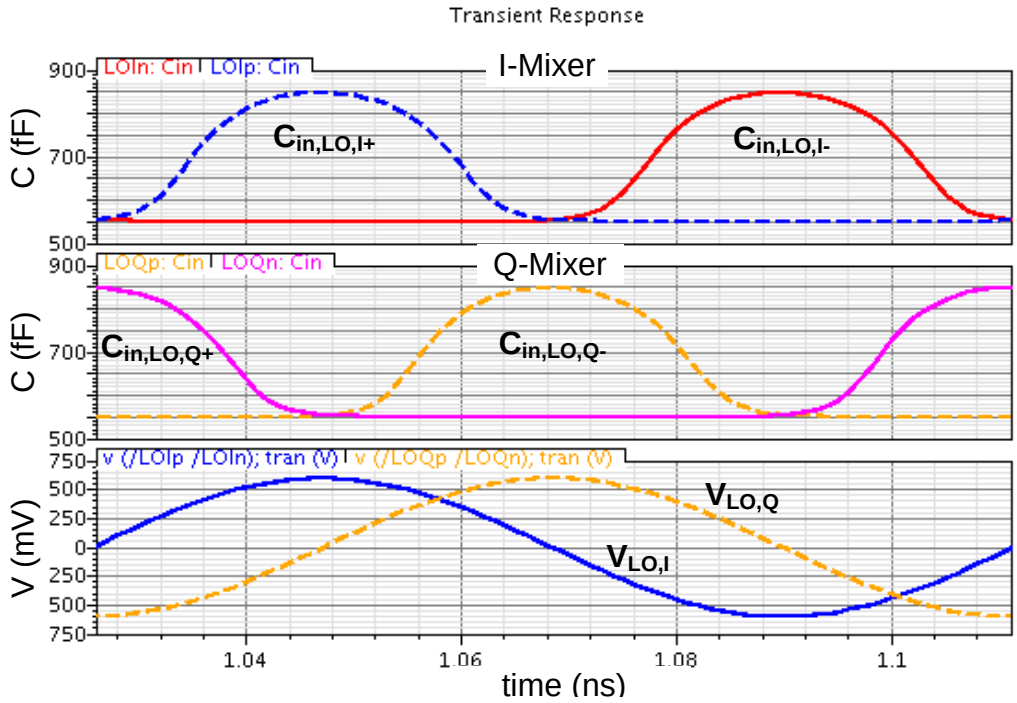

Figure 28: Variation LO-input capacitance of BLIXER for one period

It can be seen that the input capacitance varies from 550 fF to 850 fF for half a period when the applied differential oscillator voltage becomes larger than zero at the specific LO-port. The other half of the period the input capacitance remains constant at 550 fF. Qualitatively this can be well understood. If the applied voltage at the LO-port is smaller than the common mode voltage, then ideally there will be no conducting channel formed under the gate-oxide of the switching transistor. The capacitance seen at the gate of the transistor therefore will be constant and mainly determined by the overlap capacitances. If the applied voltage is larger than the common mode voltage, then a channel will be formed. The number of electrons in the channel will increase nonlinear with the applied voltage. This will result in a non-linear capacitance seen at the gate, which varies with the applied gate voltage.

The input capacitance seen between two LO-input ports of the I (or Q) mixer will be equal to the series network of the two input capacitances seen at each port. If the differential oscillator voltage is zero, the input capacitance at each port is equal to 550 fF (as can be seen in Figure 28). The total input capacitance between the two ports then is equal to:

$$C_{input,min}(V_{LO} = 0) = \frac{1}{2} \cdot 550\, fF = 275\, fF \tag{2.93}$$

The total input capacitance seen between the two LO-input ports is at its maximum if the applied oscillator voltage at one of the two LO-input ports is at its maximum and is equal to:

$$C_{input,max}(|V_{LO}| = 0.6V) = \frac{850 \cdot 550}{850 + 550}\, fF = 334\, fF \tag{2.94}$$

So the total input capacitance will vary (nonlinear) periodically with twice the oscillation frequency between 275 fF and 334 fF, which is a lot larger than the first estimation of 100 fF which has been done in the beginning of this chapter. Since the maximum input capacitance is proportional to the amplitude of the LO-voltage, the variation in input capacitance will also be proportional to the LO-voltage amplitude.

The question may arise what the origin is of this large input capacitance. In Figure 29 the dominant parasitic capacitances are shown at the LO-input ports of the I-side of the BLIXER. The dominant capacitances are the gate-source and the gate-drain capacitances of the switching transistors M_2 and M_3. These transistors are 4 times larger than M_1 and M_2 and therefore the capacitances will also be ~ 4 times larger.

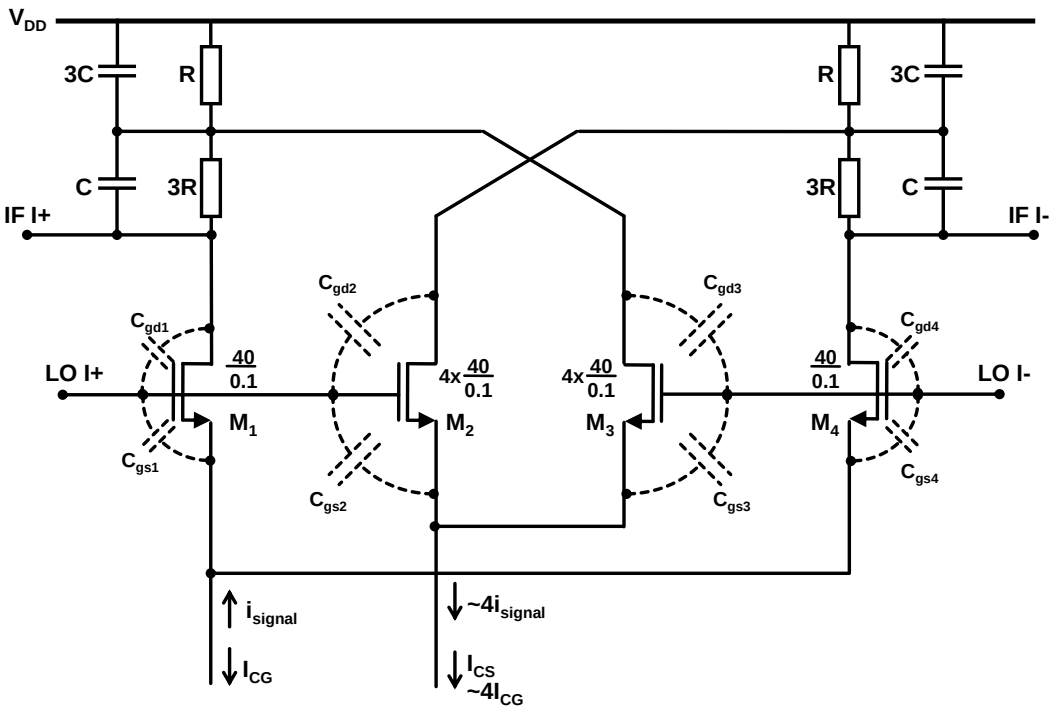

Figure 29: I-side of BLIXER including parasitic capacitances

To show the contributions of all the parasitic capacitances to the input capacitance per LO-port, they have been plotted for the LO I+ port in Figure 30. The constant gate-drain capacitance and the constant gate-source capacitance during half the period is expected to be equal to the overlap capacitance. The gate-source and gate-drain overlap capacitance of transistor M_1 is equal to 15 fF, which explains the constant part of capacitance C_{gs1} and capacitance C_{gd1}. The overlap capacitance of transistor M_2 will be ~4 times larger and is equal to 60 fF. However the fixed part of the gate-source capacitance of transistor M_2 and the gate-drain capacitance of M_2 are almost 4 times larger than the overlap capacitance of 60 fF. Apparently the fixed gate-source and gate-drain capacitances of transistor M_2 will also be affected by another capacitances in the circuit, as for example the capacitances of the IF-filter at the output of the mixer. It could also be that there is something wrong with the simulation setup, this isn't clear to the author at this moment. Further work is required to get this clear..

It is clear from Figure 30 that indeed the gate-source capacitance and the gate-drain capacitance of the largest transistor M_2 dominate the input capacitance of the LO-port. Also the gate-bulk capacitance of transistor M_2 contributes a significant part (~16%) to the input capacitance if the total capacitance is at its minimum. The gate-bulk capacitance is at its minimum, when the applied oscillator voltage is large. The bulk then will be shielded from the gate by the conducting channel. Note that the bulk is connected for all transistors to ground.

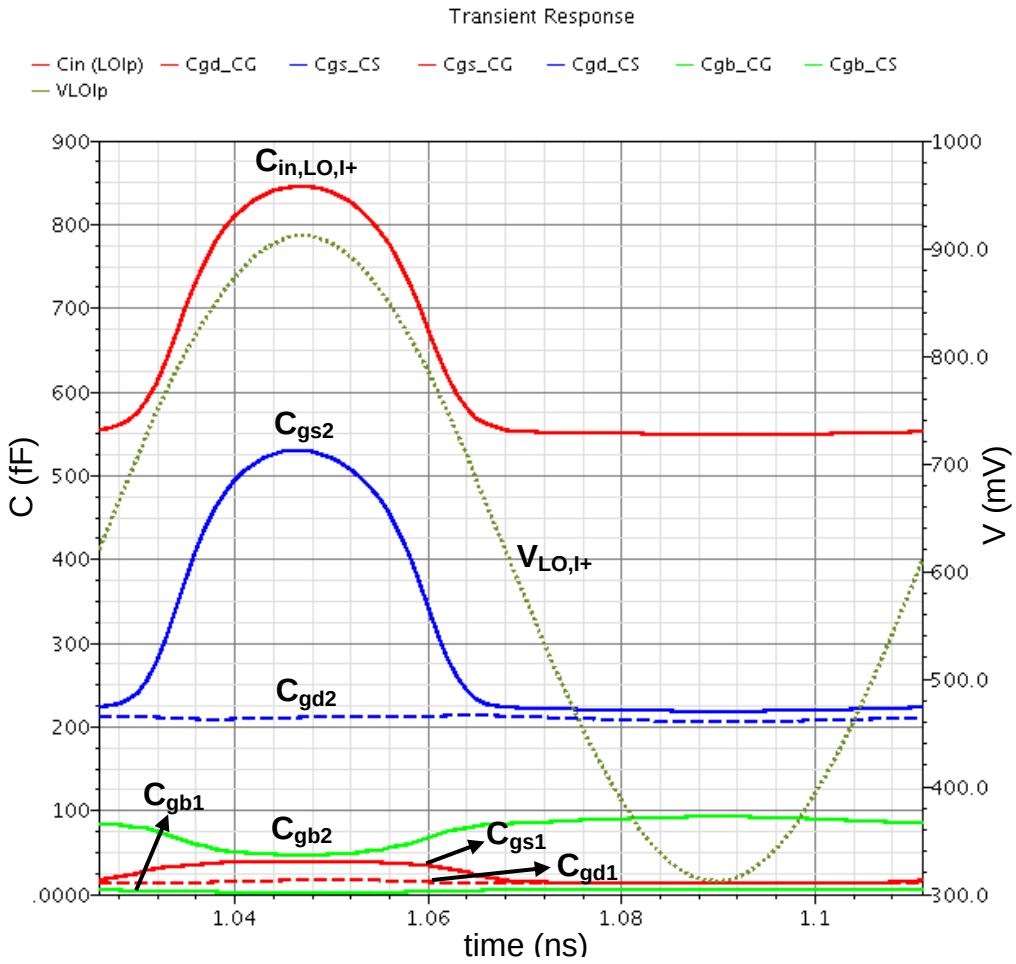

Figure 30: Parasitic capacitances at LO-input port of BLIXER

2.4.2 Simulated VCO performance loaded with mixer

In the previous section we've seen that the input capacitance of the mixer will (non-linearly) vary with the applied oscillator voltage. In this section we'll find out what the effect on the performance of the VCO is, if this non-linear varying capacitance will become part of the total impedance in the LC-tank of the oscillator. Or in words of the first research question: what will be the effects on the performance of the VCO, if the VCO is loaded with (the LO-input capacitance) of a mixer? The performance will be compared with an unloaded VCO and a VCO loaded with a fixed capacitance equal to the effective input capacitance of the mixer.

Ideal poly-phase filter for creating quadrature oscillator signals

Since the BLIXER is a quadrature mixer with an I-side and a Q-side, two quadrature oscillators would be necessary to drive the BLIXER. Therefore an ideal RC-CR poly phase filter is used to create the necessary quadrature oscillator signal to drive both the I- and Q-side of the mixer. As can be seen in Figure 31 this poly-phase filter is designed with noise-free resistors and through the use of ideal voltage controlled voltage sources, it will not load the VCO. In this case the VCO will be loaded with only one mixer (e.g. the I-mixer) and the poly-phase filter takes care that the I/Q mixer will be driven and function as it should be.

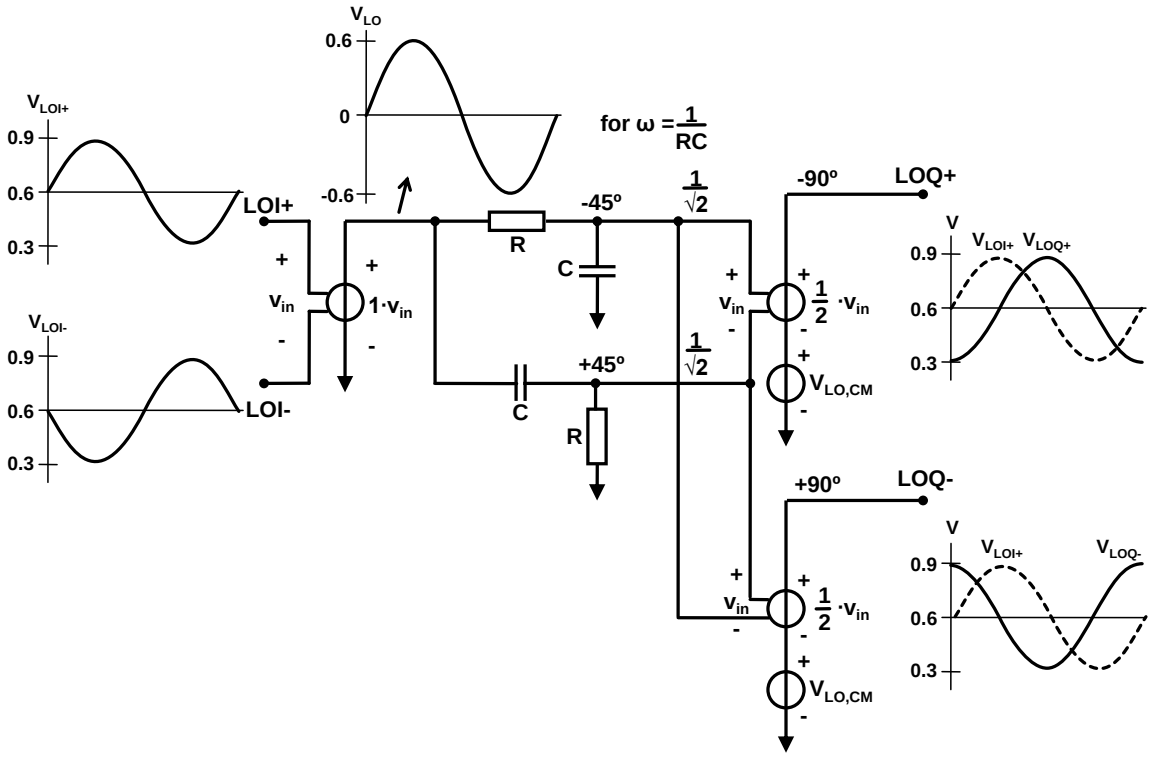

Figure 31: Ideal RC-CR poly-phase filter for creating quadrature oscillator signals

The low pass filter RC-network will give 0° phase shift at DC and -90° phase shift for frequencies going to infinity. The high pass filter CR-network gives +90° phase shift at DC and will give 0° phase shift for frequencies going to infinity. The phase difference between both networks therefore will always be 90°. The transfer however from input to output is only equal for one frequency:

$$\omega = \frac{1}{RC} \tag{2.95}$$

For R is a value chosen of 100 Ω and C a value of 136 fF, which will give equal transfer for the oscillation frequency of 11.7 GHz:

$$\omega = \frac{1}{100\,\Omega \cdot\ 136\,fF} \rightarrow f = \frac{1}{2 \cdot \pi \cdot 100\,\Omega \cdot\ 136\,fF} = 11.7\,GHz \tag{2.96}$$

The transfer for both networks for this frequency is equal to:

$$H\left(\omega = \frac{1}{RC}\right) = \frac{1}{\sqrt{2}} \tag{2.97}$$

The effective input capacitance of the mixer is determined by loading the VCO with the mixer and tuning the tank capacitance until the desired oscillation frequency of 11.7 GHz was achieved. The total capacitance needed for this oscillation frequency is known and has a fixed value. So therefore the reduction in tank capacitance must be equal to the added capacitance as a result of the load of the mixer. and also the capacitance added by the cross-coupled pair. The effective input capacitance of the mixer is found in this manner to be: 291 fF (582 fF per LO-port).

$$C_{input,effective} = 291\,fF \tag{2.98}$$

The AC-coupling capacitor has been doubled (to 8 pF), now is clear that the load capacitance is larger than at first was estimated. This has been done to reduce the loss in voltage swing as a result of voltage division between the coupling capacitor and the load capacitor of the VCO. The loss in voltage swing with an effective input capacitance of the mixer now will be equal to ~ 7 %:

$$loss\ in\ voltage\ swing = \frac{582\,fF}{582\,fF + 8\,pF} \cdot 100\% = 6.8\,\% \tag{2.99}$$

Since the maximum voltage swing of the cross-coupled pair of the VCO is limited by 1.2 as a result of the varactor bank, the maximum oscillator output voltage swing will be equal to ~ 1.12V:

$$V_{LO,out,max} = V_{XCP,max} \cdot \frac{8\,pF}{582\,fF + 8\,pF} = 1.2\,V \cdot 0.932 = 1.119\,V \tag{2.100}$$

Simulated phase noise performance of VCO loaded with BLIXER

The phase noise performance of the VCO loaded with the BLIXER will now be analyzed. The simulated phase noise performance will be compared for the following three cases:

- **VCO without load**
- **VCO loaded with fixed capacitance of 291 fF**
- **VCO loaded with mixer (I/Q BLIXER)**

To make a fair comparison, the performance is compared for the same oscillation frequency of 11.7 GHz and the same XCP-tank amplitude. The tank capacitance and the bias current therefore will be adapted for each case. The simulation results for these three cases are shown in Figure 32.

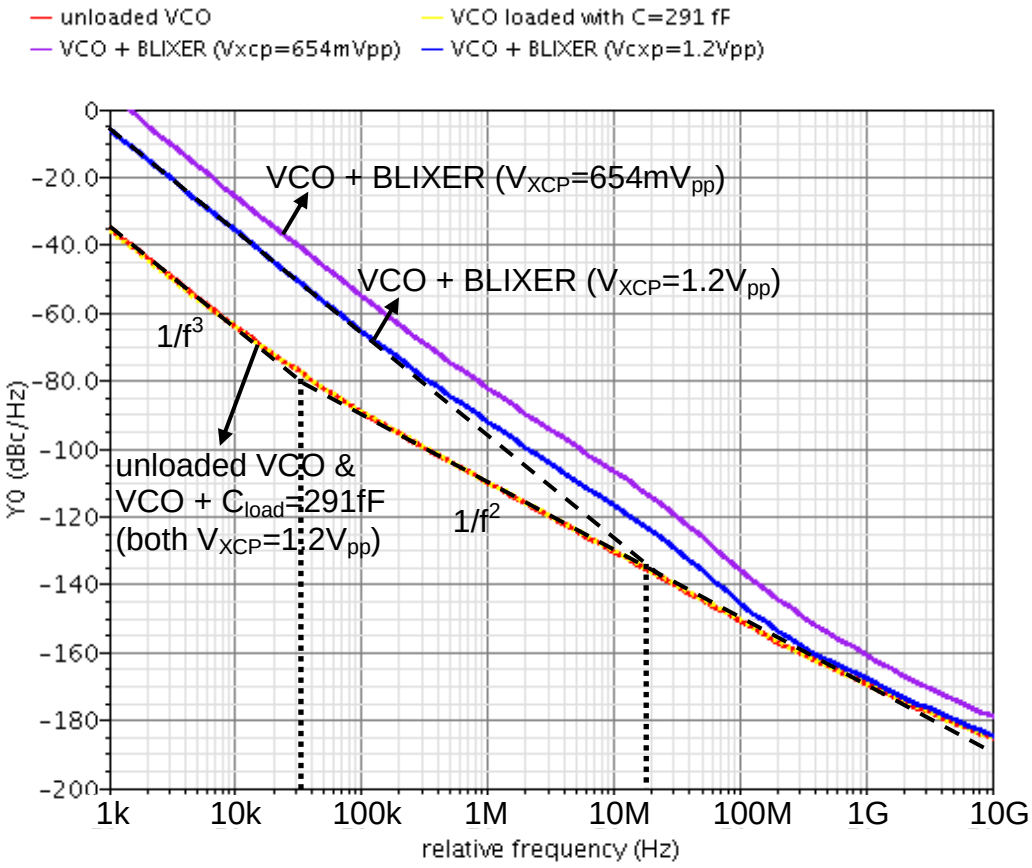

Figure 32: Relative phase noise performance VCO + mixer

Phase noise of VCO without load and VCO with fixed capacitive load

The phase noise performance of the unloaded VCO and the loaded VCO with a fixed capacitance of 291 fF is equal to each other. The phase noise at an offset of 100 kHz of the carrier is 89 decibels below the carrier per hertz. This is ~ 4 dB low the required -85 dBc/Hz at an offset of 100 kHz. Furthermore the $1/f^3$ corner frequency lies around 30 kHz.

For analysis of the dominant noise contributors to the phase noise for the VCO loaded with a fixed capacitance of 291 fF, in Appendix A all the noise summaries are presented for each decade of the offset frequency. The dominant noise contributions are extracted from the noise summaries and are presented in Table 1 for each decade of the offset frequency.

Offset frequency (Hz)	1k	10k	100k	1M	10M	100M	1G	10G
XCP 1/f	**97 %**	**77 %**	25 %	3 %	< 1 %	< 1 %	< 1 %	< 1 %
XCP thermal	1 %	10 %	33 %	42 %	44 %	**47 %**	45 %	**53 %**
Rp	1 %	11 %	**36 %**	**47 %**	**48 %**	45 %	**47 %**	37 %
XCP induced gate	< 1 %	2 %	5 %	6 %	7 %	7 %	7 %	9 %

Table 1: Dominant noise contributions for phase noise of VCO loaded with fixed capacitance

The noise summaries show that at 1 kHz offset of the carrier frequency 97 % of the noise is contributed by the 1/f noise of the cross-coupled pair transistors. At 10 kHz offset this is reduced to roughly 77 % of the total (phase) noise and at 100 kHz still 25 % is contributed by the 1/f noise of the cross-coupled pair. This confirms the $1/f^3$ behavior of the phase noise up till ~ 30 kHz.

For offset frequencies larger than ~ 100 kHz the thermal noise of the parallel resistance of the tank (R_P) together with the thermal noise of the cross-coupled pair become the dominant noise contributors to the (phase) noise. This noise is integrated as a result of the bandpass filtering of the tank and therefore is responsible for the $1/f^2$ behavior of the phase noise for offset frequencies larger than 100 kHz. Note that the contributions of the tank resistance (R_P) and cross-coupled pair are more or less the same (~ 45 % for each for an offset of 1 MHz up to 1 GHz), since the cross-coupled pair represents a 'negative resistance' which has to be equal to the parallel resistance of the tank (R_P) for steady state oscillation (and without the presence of other losses). The induced gate noise of the cross-coupled pair is a notable noise contributor with a noise contribution of ~ 7 % for offset frequencies between 1 MHz and 1 GHz. For lower offset frequencies the induced gate noise isn't a notable effect. For a larger offset frequency of 10 GHz it becomes a bit more contributing (9 % noise contribution).

Phase noise of VCO loaded with BLIXER

The phase noise performance of the VCO loaded with the mixer shows that two effects occur:

1. The tank amplitude becomes smaller as a result of extra losses
2. The phase noise increases drastically until ~ 500 MHz offset of the carrier, even when the bias current of the VCO is increased to compensate for the extra losses

The extra losses as result of loading the VCO with the BLIXER can be estimated by using the approximation that the tank amplitude can be written as the product of the bias current and the effective parallel tank resistance (see equation 2.83). Where the effective parallel tank resistance models all the losses in the tank. Since the amplitude has decreased, it is concluded that loading the VCO with the BLIXER introduces extra losses, which can be viewed as a lower effective tank resistance.

$$decrease\ in\ tank\ amplitude = \frac{1.2\ V - 0.65\ V}{1.2\ V} \cdot 100\% \cong 45\ \% \tag{2.101}$$

$$effective\ tank\ resistance = 368\ \Omega - 45\ \% \cdot 368\ \Omega = 202\ \Omega \tag{2.102}$$

$$effective\ Q\ of\ loaded\ tank\ = \frac{R_P}{\omega L} = \frac{202\ \Omega}{2\pi 11.7 \cdot 10^9 \cdot 400 \cdot 10^{-12}} = 6.9 \tag{2.103}$$

To compensate for these losses, the bias resistor in the VCO has been decreased to increase the bias current with ~45 % from 2.2 mA to 3.1 mA.

After adapting the bias current to compensate for the extra losses, the phase noise of the VCO is still drastically increased. At 100 kHz offset of the carrier, the phase noise is 65 decibels below the carrier per hertz. This is 24 dB higher compared to the VCO loaded with a constant capacitance equal to the effective input capacitance of the mixer.

Offset frequency (Hz)	1k	10k	100k	1M	10M	100M	1G	10G
Gm-bias 1/f	**95 %**	**93 %**	**79 %**	33 %	8 %	1 %	< 1 %	< 1 %
Gm-bias thermal	< 1 %	1 %	8 %	**38 %**	**79 %**	**57 %**	2 %	2 %
Switches induced gate	< 1 %	1 %	6 %	19 %	3 %	2 %	4 %	7 %
AC-coupling resistors	< 1 %	1 %	2 %	6 %	1 %	<1 %	<1 %	< 1 %
XCP thermal	< 1 %	< 1 %	< 1 %	1 %	< 1 %	17 %	**41 %**	**45 %**
Rp	< 1 %		< 1 %	1 %	2 %	12 %	35 %	28 %

Table 2: Dominant noise contributions for phase noise of VCO loaded with BLIXER

The $1/f^3$ corner frequency is shifted roughly three decades from ~ 30 kHz to ~ 20 MHz. To analyze the effects of the increased phase noise for the VCO loaded with the BLIXER in Appendix B all the noise summaries per decade offset frequency are presented. The dominant noise contributions are extracted from the noise summaries and are presented in Table 2 for each decade of the offset frequency. This shows that a lot of normally low frequent 1/f noise originating from the Gm-stage of the BLIXER is up converted to phase noise around low offset frequencies. The dominant noise contributors are the relatively small transistors responsible for biasing of the common

source - and common gate transistors within the Gm-stage of the BLIXER. The mechanism of up converting low-frequency noise contributors within the BLIXER to phase noise of the VCO will be analyzed in the next section (section 2.4.3). Also the extra losses introduced by loading the VCO with the BLIXER will be analyzed in the next section.

Without yet going into detail into the mechanism of up converting it is clear from the noise summaries that not only 1/f noise, but also resistors used in the biasing of the Gm stage of the BLIXER are the dominant noise contributors up to an offset frequency of 10 MHz. For offset frequencies above 100 MHz the effect of the up converted low frequency noise from within the BLIXER becomes smaller and the noise contributions of within the VCO become dominant. At 1 GHz offset frequency for example the thermal noise of the parallel resistance of the tank (R_P) and the thermal noise of the cross-coupled pair transistors have a noise contribution of respectively 35 % and 41 %.

It is clear that the biasing of the Gm-stage of the BLIXER contributes a lot to the increased phase noise of the BLIXER. So let's analyze what's left of this degrading of the phase noise performance if the Gm stage of the BLIXER is ideally biased. This means that all the bias voltages for the Gm-stage of the BLIXER will be applied with ideal voltage sources with an inductor in series to be able to maintain the high frequency voltage variation for example at the gate of the NMOS of the CS-stage. The simulated phase noise performance of the VCO loaded with the BLIXER with ideal biasing of the Gm-stage is shown in Figure 33.

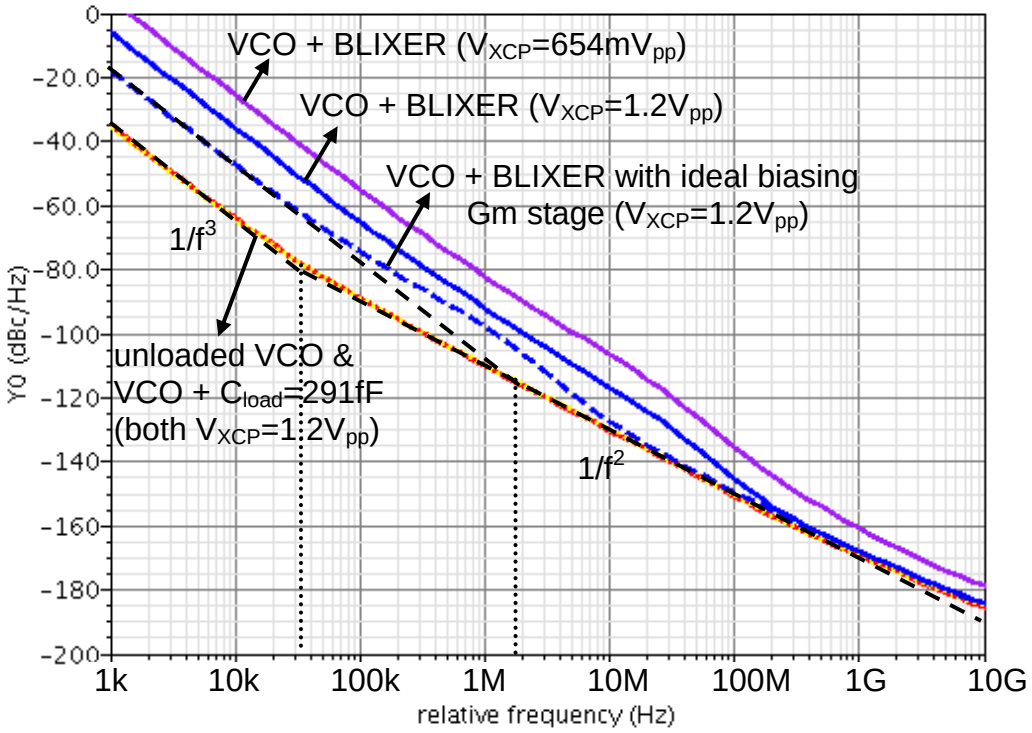

Figure 33: Phase noise improvement VCO loaded with BLIXER with ideal biasing Gm stage

Phase noise of VCO loaded with BLIXER with ideal biasing Gm stage

The simulated phase noise of the VCO loaded with ideal biasing of the Gm-stage shows that the $1/f^3$ corner frequency is shifted to an offset frequency of ~ 2 MHz. Compared to the phase noise for the unloaded VCO, the phase noise of the VCO loaded with the BLIXER with ideal biasing of the Gm stage is 15 to 20 dB higher up to an offset frequency of 1 MHz. From an offset frequency of 10 MHz the phase noise performance of the VCO loaded with the BLIXER with ideal biasing of the Gm stage becomes comparable to the phase noise of the unloaded VCO. Furthermore it is notable that between the $1/f^3$ region and $1/f^2$ region (between ~ 30 kHz and 10 MHz) it looks like the phase noise has another corner frequency at around 1 MHz. The phase noise looks to have a $1/f^3$ behavior up to ~ 30 kHz, then a sort of $1/f^2$ behavior up to ~ 1 MHz and between 1 MHz and 10 MHz it goes again down with approximately $1/f^3$. To analyze the origin of this, the noise summaries of the VCO loaded with the BLIXER with ideal biasing of the Gm-stage is presented in Appendix C. The dominant noise contributions are extracted from the noise summaries and are presented in Table 3 for each decade of the offset frequency.

Offset frequency (Hz)	1k	10k	100k	1M	10M	100M	1G	10G
Gm CS & CG 1/f	**91 %**	**78 %**	33 %	6 %	6 %	2 %	< 1 %	< 1 %
Switches induced gate	2 %	12 %	**49 %**	**70 %**	**36 %**	5 %	4 %	8 %
AC-coupling resistors	< 1 %	3 %	13 %	19 %	10 %	1 %	1 %	1 %
XCP thermal	1 %	< 1 %	1 %	2 %	22 %	**43 %**	**42 %**	**47 %**
Rp	< 1 %	< 1 %	1 %	1 %	17 %	31 %	35 %	28 %

Table 3: Dominant noise contributions for phase noise of VCO loaded with BLIXER with ideal biasing Gm stage

At an offset of 1 kHz it can be seen from the noise summary that the (up converted) 1/f noise from the NMOS CS- and CG transistors of the Gm-stage of the BLIXER are by far the dominant noise sources with 91 % noise contribution. Also at 10 kHz offset of the carrier frequency the (up converted) 1/f noise of these transistors are the dominant noise sources (78 %). The second dominant noise contributor is the induced gate noise of the switching transistors of the BLIXER (in total 12 % noise contribution). At an offset of 100 kHz the 1/f noise contribution of the CS- and CG-transistors is reduced to 33 %. The dominant noise contribution is at this point the induced gate noise of the switching transistors with 49 % noise contribution. But also the resistors of the AC-coupling have a notable noise contribution of 13%. The induced gate noise of the switching transistors and the thermal noise of the resistors of the AC-coupling both have a fall-off of $1/f^2$ between 10 kHz and 100 kHz.

At an offset frequency of 1 MHz of the carrier frequency the dominant noise contribution (90 %) is the induced gate noise of the switching transistors of the BLIXER. The second largest noise contribution (13%) is the thermal noise of the resistors of the AC-coupling. It can be noted that the fall-off of these contributors between 100 kHz and 1 MHz offset is more than $1/f^2$. Both contributors have the same fall-off in this region of a factor of ~130 ($\approx 10^{2.12}$). This suggests that both the resistors in the AC-coupling and the induced gate noise of the switching transistors are part of the same mechanism, which is responsible for the increased phase noise between 100 kHz and 1 MHz. This mechanism will be further analyzed in the next section.

At an offset frequency of 10 MHz the induced gate noise contribution of the switching transistors has decreased to 36 %. The noise contribution of the AC-coupling resistors has also become smaller and is at this point 10 %. Both absolute noise contributions have reduced by a factor of ~ 2300 ($\approx 10^{3.36}$) compared to the values at 1 MHz. This confirms the ~ $1/f^3$ decay between 1 MHz and 10 MHz. The thermal noise of the parallel tank resistance (R_P) and the thermal noise of the cross-coupled pair transistors are becoming again the dominant noise sources at this offset frequency of 10 MHz (17 % and 22 % respectively). If the spot noise of these contributors is compared to the VCO loaded with a fixed capacitance, then there are only small differences between these values. So for offset frequencies larger than 10 MHz driving the mixer with ideal biasing of the Gm-stage without buffers between the VCO and mixer doesn't degrade the phase noise performance anymore of the VCO.

At an offset frequency of 100 MHz the contribution of the induced gate noise of the switching transistors and the thermal noise of the AC-coupling resistors is further decreased to 5 % and less than 1 % respectively. The absolute noise contribution of the induced gate noise of the switching transistors is reduced by a factor of ~1400 ($\approx 10^{3.15}$) compared to the value at 10 MHz. The absolute noise contribution of the AC-coupling resistors is even decreased by a larger factor of 2500 ($\approx 10^{3.4}$) compared to the value at 10 MHz. What leaves us with the dominant (thermal) noise contributions of the VCO itself, i.e. the parallel tank resistance (31 %) and the cross-coupled pair transistors (43 %). The absolute values of these noise contributions again are not much different compared to the VCO loaded with an ideal capacitive load of 291 fF. It is notable that the thermal noise of the cross-coupled pair is ~26 % larger than for the VCO loaded with an ideal capacitive load. This can be well understood by realizing that the bias current of the VCO loaded with the mixer was increased to compensate for extra losses. The downside of this is the relatively small increase in noise contribution of the cross-coupled pair.

At an offset of 1 GHz of the carrier frequency the phase noise becomes dominated again by the noise sources within the VCO. The thermal noise of the parallel tank resistance contributes 35 % and the thermal noise of the cross-coupled pair 42 % to the total noise. The induced gate noise of the switching transistors is decreased by a factor of ~90 ($\approx 10^{1.95}$) compared to the value for an offset of 100 MHz to a total noise contribution of 4 %. Also the thermal noise of the AC-coupling resistors is decreased with a factor of ~ 90 compared tot the value for an offset of 100 MHz. This suggests that the mechanism which caused the colouring of these noise contributions isn't (notably) present anymore for high frequency offset of the carrier of larger than 100 MHz.

2.4.3 Analysis degraded phase noise performance

We've seen in the previous section that a lot of low frequency noise of within the biasing of the Gm-stage of the BLIXER converts to phase noise of the VCO when loaded with the BLIXER. With the use of an example of one of the dominant noise contributions of within the biasing of the GM-stage of the BLIXER this will be analyzed. In Figure 34 the input Gm-stage of the BLIXER can be seen with the 1/f noise of one of the transistors used for creating the bias voltage for the NMOS CS-transistor.

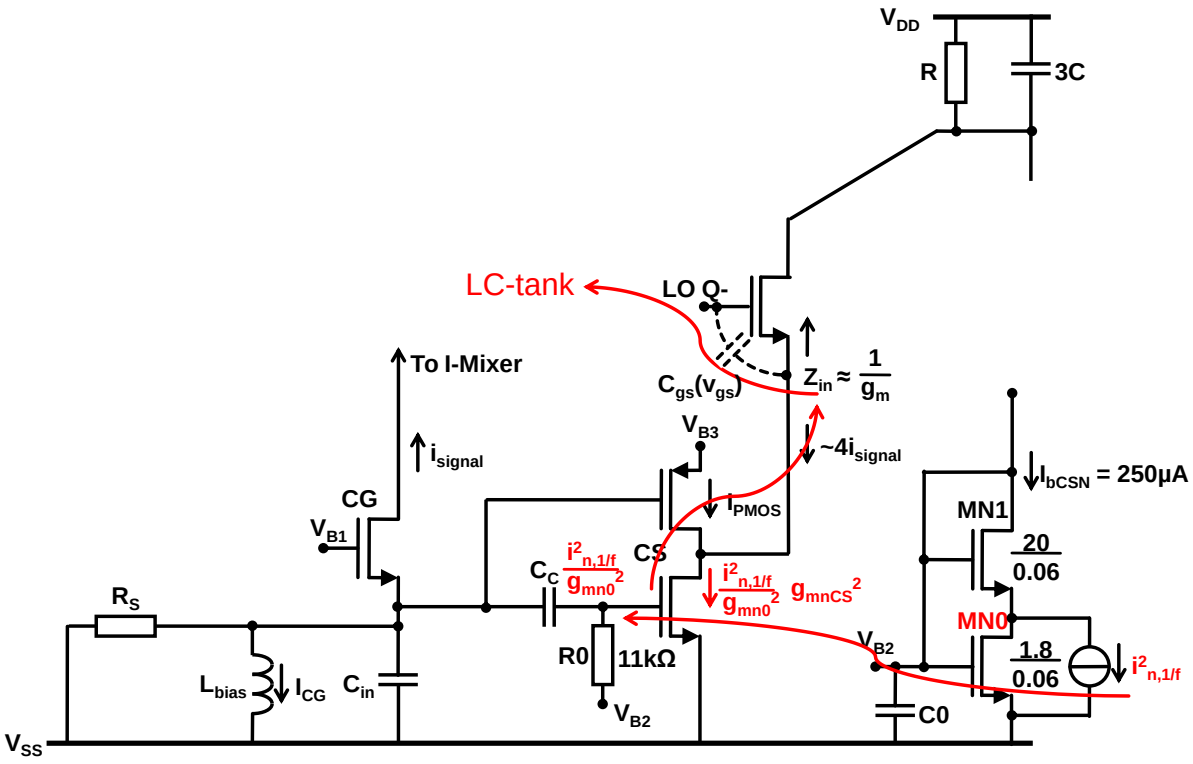

Figure 34: Example of upconverting 1/f noise of biasing of Gm-stage of BLIXER into phase noise of the VCO

The low frequency dominant 1/f noise current of transistor MN0 will be converted to a noise voltage at node V_{B2} through the transconductance g_{mn0} of the transistor:

$$\overline{v_{n,1/f}^2} = \frac{\overline{i_{n,1/f}^2}}{g_{mn0}^2} \tag{2.104}$$

For low frequencies, large part of the noise voltage will be converted to a noise current through the large transconductance of the NMOS common source transistor:

$$\overline{v_{n,1/f}^2} = \frac{g_{mnCS}^2}{g_{mn0}^2}\overline{i_{n,1/f}^2} \tag{2.105}$$

This noise current will flow through the low source input impedance and the output impedance of the switching transistors. This will result in a low frequency varying of the source voltage of the switching transistors. Since the gate source capacitance of the switching transistors is a function of the applied gate-source voltage, the variation in source voltage will result in a varying gate source

capacitance. Recall that the gate-source capacitance is part of the total tank capacitance, which determines the oscillation frequency of the tank. Influencing the gate-source voltage and therefore the gate-source capacitance will influence the oscillation frequency. If a low frequency 1/f noise source is responsible for this gate-source capacitance variation, this can be intuitively understood that this will be present as phase noise at low offset frequencies of the carrier frequency.

So to speak in more general terms: all the noise contributions which influence the gate-source voltage of the switching transistors can be seen as analog frequency modulation. This effect will translate low-frequency noise components to the region around the carrier frequency [6,p.223].

As already seen in the previous section the induced gate noise of the switching transistors is also another dominant noise contribution, especially in the frequency range between 100 kHz and 10 MHz offset of the carrier frequency. To analyze this noise contribution the VCO is shown in Figure 35 with the switching transistors modeled with the gate noise circuit model of van der Ziel [9].

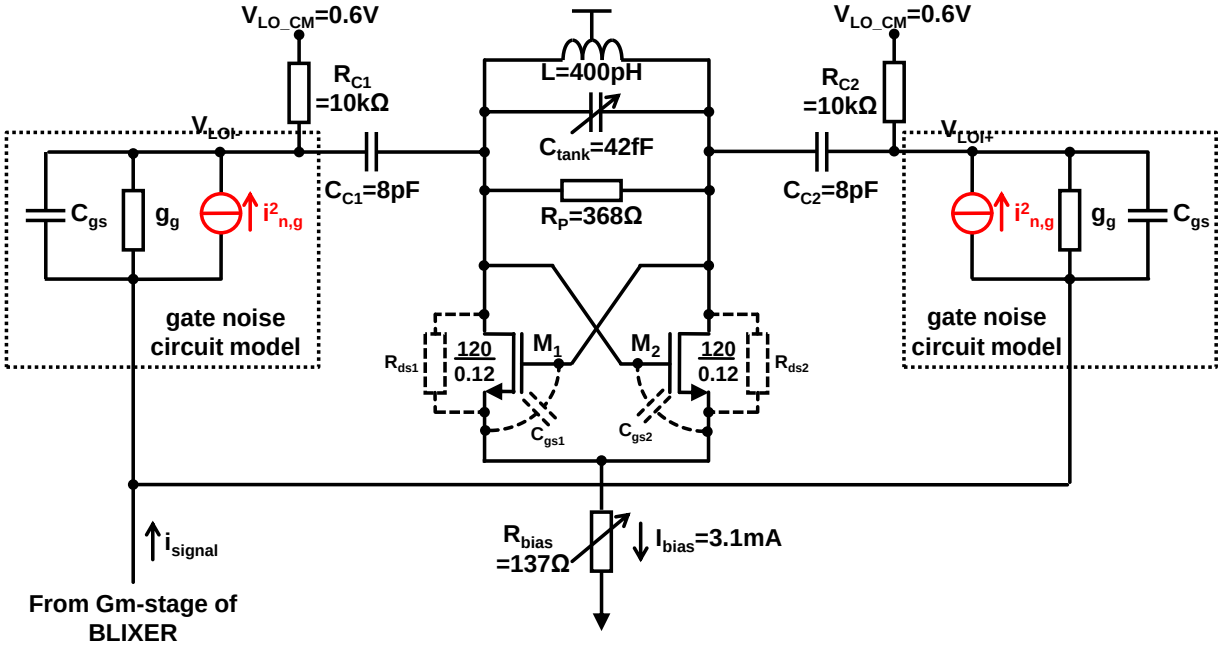

Figure 35: VCO loaded with model of gate noise of switching transistors of mixer

The induced gate noise current is expressed as [9]:

$$\overline{\imath_{n,g}^2} = 4kT\delta g_g \Delta f \tag{2.106}$$

With δ the gate noise coefficient (normally around 4/3 for long channel devices) and with the conductance g_g expressed as:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2.107}$$

This shows that the induced gate noise current has a spectral density which isn't constant and gives colored noise. It can be intuitively understood that the induced gate noise together with the filtering property of the AC-coupling (-3 dB BW = 2 MHz) is responsible for the increase in phase noise in the region between 100 kHz and 10

MHz. However it isn't quite clear yet to the author how this mechanism works and how this qualitative can be well described. Further research is therefore recommended to get full insight in this mechanism.

The extra losses introduced by loading the VCO with the BLIXER can be seen as the result of the gate conductance g_g described in equation 2.105.

2.5 Conclusions

Loading a Voltage Controlled Oscillator directly with a switching mixer will have consequences on the oscillation frequency of the VCO as a result of the capacitive input of the mixer. Furthermore the mixer can introduce extra losses in the VCO as a result of the gate resistance of the switching transistors. The phase noise of the VCO can be degraded by noise sources, which influence the gate-source voltage and therefore the gate-source capacitance of the switching transistors. This means that noise sources within the mixer can give effect to an increase in phase noise, if this affects the source voltage of the switching transistors. Induced gate noise of the switching transistors can result in an increase in phase noise.

Given the application of a CMOS satellite receiver with an LC-oscillator used as VCO and the Balun I/Q Mixer (BLIXER) [1] as a mixer and given the following boundary conditions and assumptions:

- Oscillation frequency of 11.7 GHz
- Total inductance in the tank of 400 pH
- VCO has to be able to compensate for 10 % spread in tank capacitance and load capacitance
- Feasible tuning range of tank capacitance smaller than ~ 400 %
- Compensation network of LC-oscillator doesn't add extra capacitance to the tank

The conclusion can be drawn that an LC oscillator with a parallel LC-tank can be loaded if the capacitive load is smaller than ~ 400fF and an LC oscillator with a series LC tank can be loaded if the capacitive load of the mixer is larger than ~600fF. There is a range of capacitive load where it is very difficult to load an LC oscillator with a capacitive load and still be able to adapt the tank capacitance in order to maintain the same frequency. This is the case for this project if the capacitive load of the mixer is in the range between 400 fF and 600 fF.

Simulations have shown that the effective input capacitance of the BLIXER is roughly equal to 290 fF if the applied oscillator signal has amplitude of 600 mV and a common mode level of 600 mV. The cross-coupled pair transistors add roughly 150 fF capacitance to the total tank capacitance. Therefore it has shown possible to load a parallel LC-oscillator with the BLIXER and still realize the desired oscillation frequency of 11.7 GHz. The drawbacks of directly loading the VCO with the BLIXER without buffering in between are:

- Increase in phase noise of up to 15 dB for low offset frequencies between 1 kHz and 10 MHz as result of up converted 1/f noise within the BLIXER and induced gate noise of the switching transistors together with the filtering behavior of the AC-coupling network
- Even more increase in phase noise up to 15 dB as a result of low frequency noise from within the biasing of the Gm stage of the BLIXER up converting to phase noise
- Increase in power consumption (~45 %) to compensate for extra tank losses which are thought to be as a result of the gate resistance
- Smaller tunable tank capacitance of around 50 fF which will make it harder to have enough tuning range to compensate for variation in all the capacitances in the tank.

The required tuning range for the tank capacitance can now be calculated using equation 2.79 already presented in section 2.3.2:

$$(tuning\ range)_{par} = \frac{2\alpha_L C_{load}}{C_{total} - (1+\alpha_L)C_{load}} + \frac{2\alpha_T}{(1-\alpha_T)} \quad (2.79)$$

Where α_L represents the spread in the load capacitance C_{load} and α_T represents the spread in the tank capacitance.

In section 2.3.2 however was assumed that the tank capacitance and the load capacitance together form the total capacitance in the tank. We've seen that also the cross-coupled pair transistors add capacitance to the tank. Since the cross-coupled pair capacitance and the input capacitance of the mixer can't be tuned, both capacitances now form the load capacitance (C_{load}) in equation 2.79:

$$(tuning\ range)_{par} = \frac{2\alpha_L\left(C_{XCP} + C_{in,mixer}\right)}{C_{total} - (1+\alpha_L)\left(C_{XCP} + C_{in,mixer}\right)} + \frac{2\alpha_T}{(1-\alpha_T)} \quad (2.106)$$

For simplicity it is assumed that the input capacitance of the mixer and the capacitance of the cross-coupled pair have the same spread of 10 % and also 10 % spread in the tank capacitance has to be compensated, then the required tuning range for the tank capacitance is equal to:

$$(tuning\ range)_{par} = \frac{0.2(150\ fF + 270\ fF)}{463\ fF - 0.9(150\ fF + 270\ fF)} + \frac{0.2}{0.9} = 121\ \% \quad (2.109)$$

3. Mixer directly driven with sine wave oscillator

In the previous chapter effects on performance of the VCO are analyzed, when the VCO is loaded with a capacitive load and eventually a mixer. This has been done to be able to answer the first research question of this feasibility study: is it possible to directly load an oscillator with a mixer without buffering in between.

The main focus in this chapter will be the second research question, i.e. can a mixer be driven directly with a sine wave oscillator without buffers in between? The used mixer topology for this research question is the BLIXER topology, as shown in Figure 36. The BLIXER topology consists of a Balun LNA and an I/Q mixer.

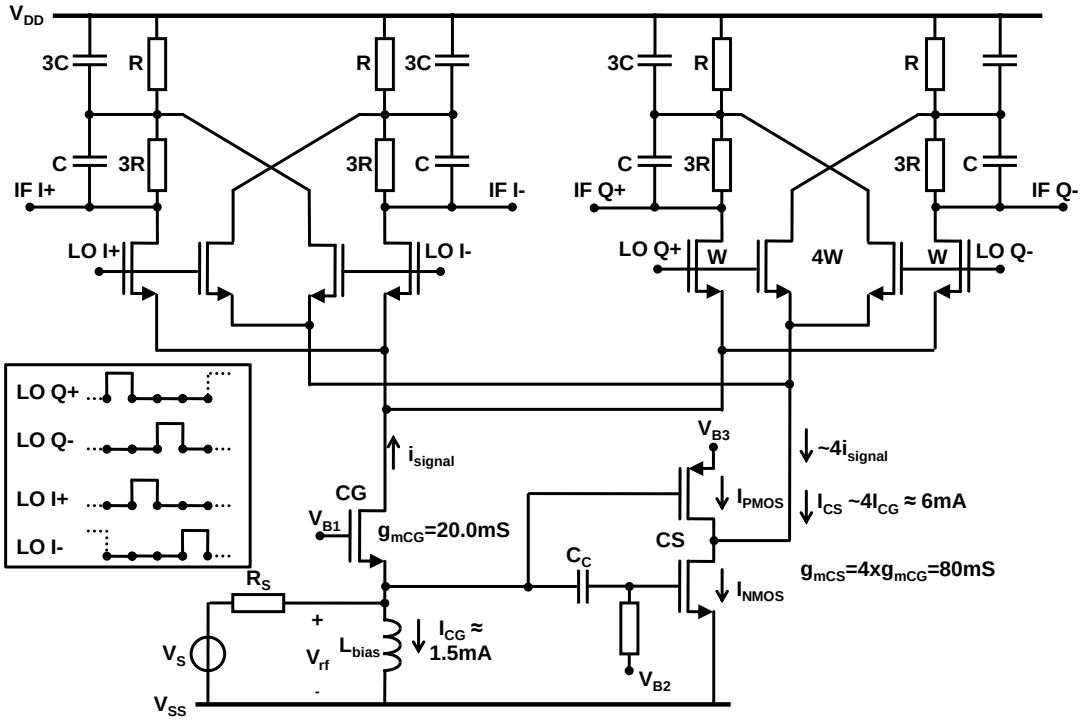

Figure 36: BLIXER topology consisting of a Balun LNA and an I/Q Mixer

The RF-input stage of the BLIXER consists of a transconductance (G_m) stage with a common gate (CG) transistor and a NMOS and PMOS common source (CS) transistor. The G_m-stage converts the input RF voltage to a differential current. With a 25% duty-cycle LO-waveform the differential signal current will be periodically switched to one of the IF-outputs. The resistive load at the IF-output will convert the signal current into a differential IF output voltage. The capacitances together with the resistances at the IF-output form the IF-filter.

The CG transistor provides 50 ohm input impedance together with a wideband input matching π-network (not shown in figure here for simplicity). The CG-stage is biased with an inductor to obtain low noise operation and save valuable voltage room. The parallel CS-CG topology (or Balun-LNA) has the nice property that the normally dominant noise of the CG-stage is cancelled because the CS-stage transfers this noise

in anti-phase to the output. To achieve a low NF, the CS-stage is scaled up 4 times. For the CS-stage a NMOS and PMOS are used to achieve a high linearity and . Both transistors are biased with a high overdrive voltage to achieve a high linearity. The NMOS is AC-coupled with the input, such that the NMOS can be biased with a high DC bias.

The BLIXER was designed for square wave oscillator signals and has shown good performance for up to oscillation frequencies of 7 GHz. For higher frequencies the circuit failed to generate the required quadrature square wave oscillator signals. At first the performance of this mixer topology when driven with sine wave oscillator signals will be analyzed. In the end of this chapter, the mixer performance will be analyzed when driven with the earlier in this thesis designed VCO without buffering in between.

To make the BLIXER suitable for the satellite receiver application and testable with the earlier in this thesis designed VCO, some modifications have to be made. The BLIXER topology was designed for UWB RF-input frequencies from 500 MHz up to 10 GHz and an IF-bandwidth of 400 MHz. The satellite receiver however has a smaller RF-input bandwidth of 2.05 GHz, but at higher frequencies, i.e. from 10.7 GHz up to 12.75 GHz. Furthermore is it necessary to increase the IF-bandwidth of the BLIXER to the required bandwidth of 1.05 GHz for the satellite receiver application. Adapting the BLIXER topology will be discussed in paragraph 3.1.

A comparison between the performance with sine wave and square wave oscillator signals driving the mixer will be given in paragraph 3.2 to study the effects on performance when driving a switching mixer with sine wave oscillator signals.

To ensure all the transistors in the BLIXER are well biased in their desired operating region when driving the BLIXER with a sine wave oscillator of 11.7 GHz, the optimal common mode level and amplitude for the sine wave will be determined in paragraph 3.3.

In paragraph 3.4 the BLIXER will be driven with the previously in this thesis presented VCO and the effects on the performance of the mixer will be analyzed. Note that this is the same simulation as has been done in section 2.4.2, only at that point the effects on the performance of the VCO were analyzed.

In the end of this chapter in paragraph 3.5 conclusions will be drawn whether it is possible to directly drive a mixer with a sine wave oscillator without buffers in between.

3.1 Adapting BLIXER for satellite receiver

The main requirements for the mixer in the CMOS satellite receiver system are a low noise figure and a high conversion gain, because of a very weak input signal of around -90 dBm. Furthermore the mixer has to be suitable for a high input RF frequency range of 10.7 GHz up to 12.75 GHz. To be more specific, all the relevant requirements for the mixer are given below:

- Quadrature mixer (I/Q-mixer) needed for direct conversion
- RF-bandwidth: 10.7 GHz - 12.75 GHz
- IF-bandwidth: 1.05 GHz
- Low noise figure
- High conversion gain

The (measured) performance of the BLIXER is given here as a reference. In this paragraph it is the objective to adapt the topology to make it useable for the satellite receiver application. The performance of the BLIXER driven with sine wave signals should be comparable with the given performance of the BLIXER driven with square wave signals, as stated below:

Measured performance square wave driven BLIXER for UWB:

- RF-(-1dB)bandwidth = 0.5 - 7 GHz
- IF-(-3dB)bandwidth = 400 MHz
- Noise Figure = 4.5 - 5.5 dB
- Conversion gain = 18 dB
- Linearity:
    - IIP3 = -3 dBm
    - IIP2 (@RF) = +20 dBm
- Power consumption = 16 mW
- Reflection coefficient: S_{11} < -10 dB

In the first section of this paragraph the original BLIXER topology will be discussed in detail and simulations will show the achievable conversion gain and the noise figure over the original RF frequency range up to 10 GHz.

In section 3.1.2 the IF-bandwidth will be increased by changing the capacitance values of the IF-filter at the output of the BLIXER to meet the requirements for the IF-bandwidth of the satellite receiver of 1.05 GHz.

In section 3.1.3 the RF-input stage of the BLIXER will be adapted to meet the requirements for the CMOS satellite receiver.

3.1.1 Simulated CG and NF performance of original BLIXER

The actual implementation of the original BLIXER topology (as shown in Figure 37) is a bit different compared to the BLIXER topology concept (shown in Figure 36) discussed earlier in this chapter. For instance the ratio between resistive loads for the CS and CG path is approximately 1:3.2 in stead of 1:4

$$280\,\Omega : (280\,\Omega + 610\,\Omega) = 280\,\Omega : 890\,\Omega \cong 1 : 3.2 \tag{3.1}$$

These little differences between the concept of the BLIXER topology and the final implementation have to do with fine-tuning of the design as a result of some non-idealities as for example finite output impedance of the switching transistors, which lower the effective load resistance.

Another difference is the wideband input matching π-network, which is shown here in Figure 37 at the input of the BLIXER. This will give well matched 50 ohm input impedance for the RF-input frequency range from 500 MHz up to 10 GHz.

The theoretical achievable voltage conversion gain of the BLIXER is given as [1]:

$$Voltage\ Conversion\ Gain = \frac{\sqrt{2}}{\pi}\left(g_{m,CG} \cdot R_{CG} + g_{m,CS} \cdot R_{CS}\right) \tag{3.2}$$

With the factor $\frac{\sqrt{2}}{\pi}$ equals the fundamental Fourier component of of a 25 % duty cycle square wave. Between brackets the voltage gain of the CG-stage and the CS-stage is added. The conversion from single-ended to differential would add a factor 2 to this equation, but falls away against the factor ½ added since for a downconversion mixer only half of the signal power is used (the upconverted signal is filtered out by the IF-filter).

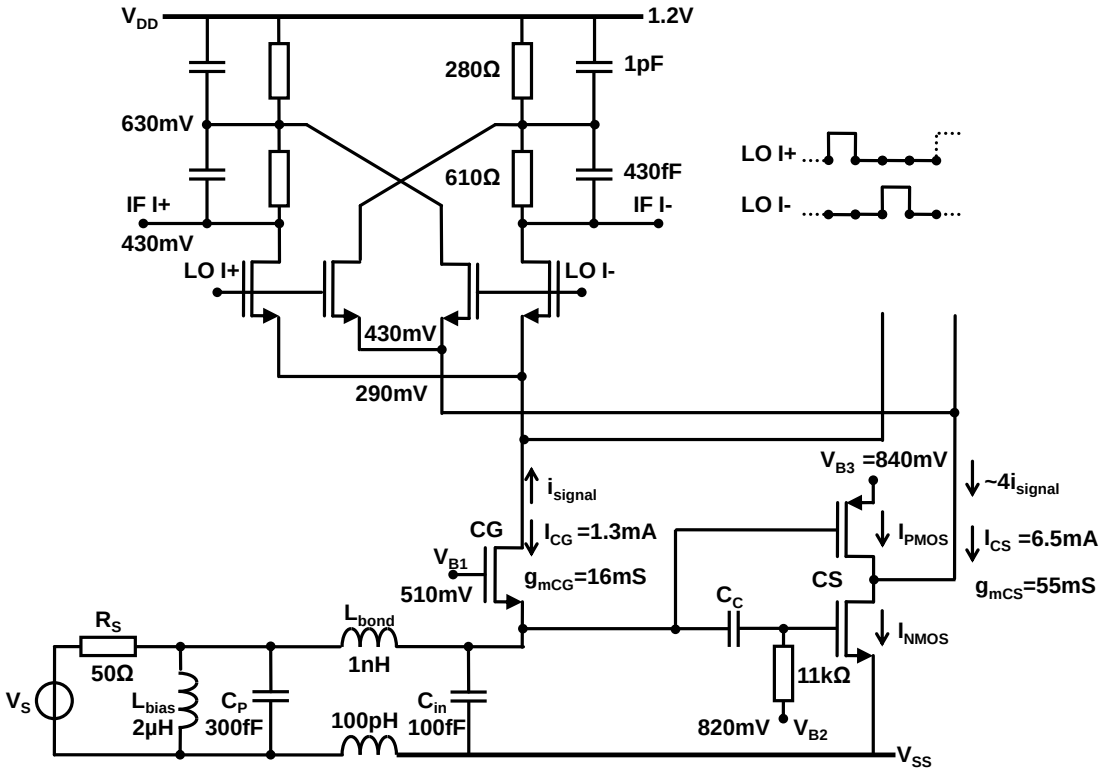

Figure 37: Original BLIXER topology with wideband input matching π-network showing DC node voltages for the I-side of the BLIXER for square wave f_{LO}=3GHz with 24 % duty cycle and 1 % rise- and fall time

For the component values shown in Figure 37 the achievable voltage conversion gain of the circuit will be:

$$Voltage\ Conversion\ Gain = \frac{\sqrt{2}}{\pi}(0.016 \cdot 890 + 0.055 \cdot 280) \tag{3.3}$$

$$Voltage\ Conversion\ Gain = \frac{\sqrt{2}}{\pi}(14.2 + 15.4) = 13.3\ (22.5\ dB) \tag{3.4}$$

The voltage conversion gain and noise figure of the BLIXER is simulated for an RF frequency range of 500 MHz up to 10 GHz at a fixed intermediate frequency of 10 MHz (shown in Figure 38). The BLIXER is driven with ideal voltage sources with a source resistance of 1 ohm. The voltage sources produced square waves from 0.1 V up to 1.0 V and had a 24 % duty cycle with 1 % rise and fall times. The source resistance of the voltage sources is chosen this low to prevent filtering out the higher order frequencies of the square wave. The high input capacitance of the BLIXER of around 550 fF (see section 2.4.1) could give a corner frequency around 6 GHz if for example the source resistance of the voltage source is 50 ohm:

$$f_{-3dB,LO-port} = \frac{1}{2\pi R_s C_{in,mixer}}$$
$$if\ R_s = 50\ \Omega\ \rightarrow\ f_{-3dB,LO-port} = \frac{1}{2 \cdot \pi \cdot 50 \cdot 550 \cdot 10^{-15}} = 5.8\ GHz \tag{3.5}$$

This would degrade the shape of the square wave severely, since already the fundamental frequency will be attenuated by more than 3 dB for oscillation frequencies above 5.8 GHz. The input bandwidth at the LO-input ports of the mixer with a source resistance of 1 ohm will be equal to 289 GHz, which is more than sufficient.

$$if\ R_s = 1\ \Omega\ \rightarrow\ f_{-3dB,LO-port} = \frac{1}{2 \cdot \pi \cdot 1 \cdot 550 \cdot 10^{-15}} = 289\ GHz \tag{3.6}$$

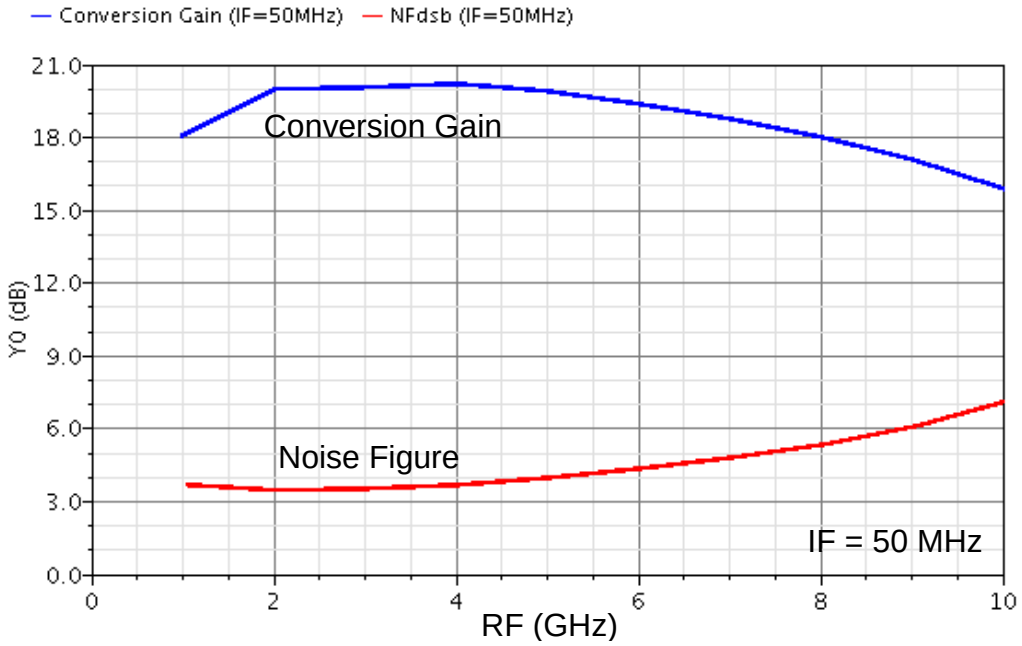

Figure 38: Conversion Gain and NF original BLIXER topology for IF=50MHz with 24 % duty cycle and 1 % rise- and fall time

Figure 38 shows a maximal voltage conversion gain of 20 dB and a minimal Noise Figure of 3.5 dB for an RF input frequency of 3 GHz. The conversion gain is ~ 2.5 dB lower than the theoretical achievable conversion gain calculated in equation 3.4. However this equation assumed no influence of the output resistances of the switching transistors and that all the signal current without losses would be switched to resistive loads at the output. The noise figure of 3.5 dB agrees with the simulation results of the BLIXER presented in the published paper [1], which was around 3 dB.

The performance of the BLIXER has also been simulated for a fixed oscillation frequency of 3 GHz and for a RF frequency range of 3.01 GHz up to 5 GHz (shown in Figure 39). It can be seen that the noise figure stays more or less flat over a large IF frequency range of 10 MHz up to 2 GHz. The IF-bandwidth determined with this simulation is around 600 MHz.

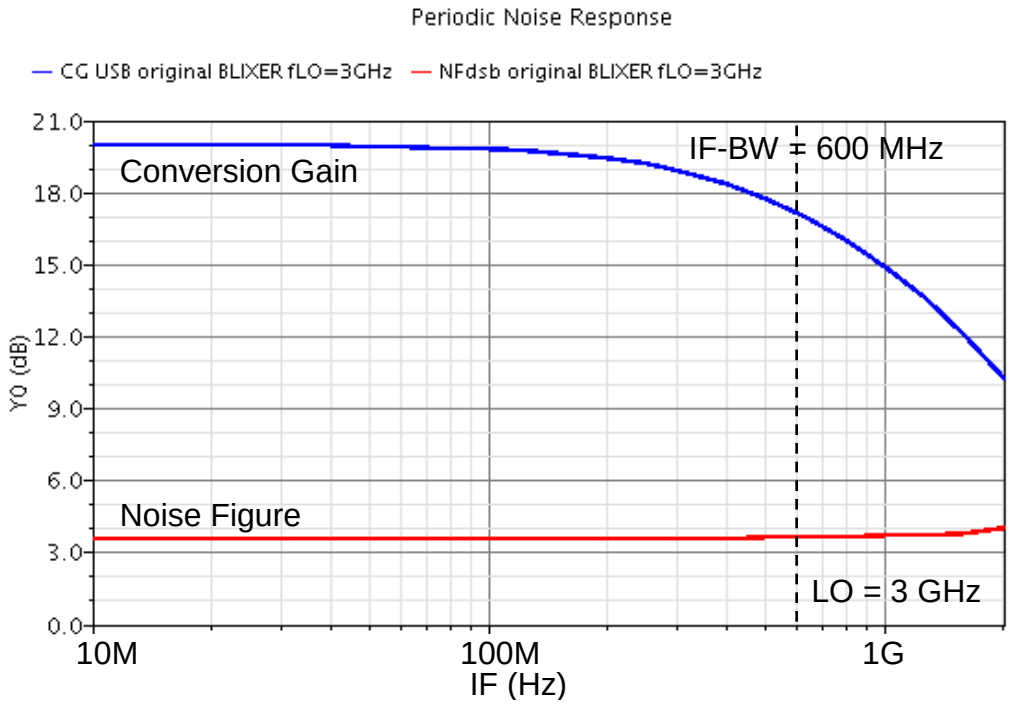

Figure 39: Conversion Gain and NF original BLIXER topology for square wave f_{LO}=3GHz with 24 % duty cycle and 1 % rise- and fall time

3.1.2 Adapting IF-filter at output of BLIXER

We saw earlier in section 3.1.1 that the simulated IF-BW of the original BLIXER is equal to ~600 MHz for an LO frequency of 3 GHz. Since the CMOS satellite receiver requires an IF-BW of 1.05 GHz, the IF-filter of the BLIXER is adapted. To increase the bandwidth approximately and keep the DC-bias settings equal, only the capacitances are decreased. The I-side of the BLIXER with adapted IF-output is shown with DC-node voltages for an oscillation frequency of 3 GHz in Figure 40.

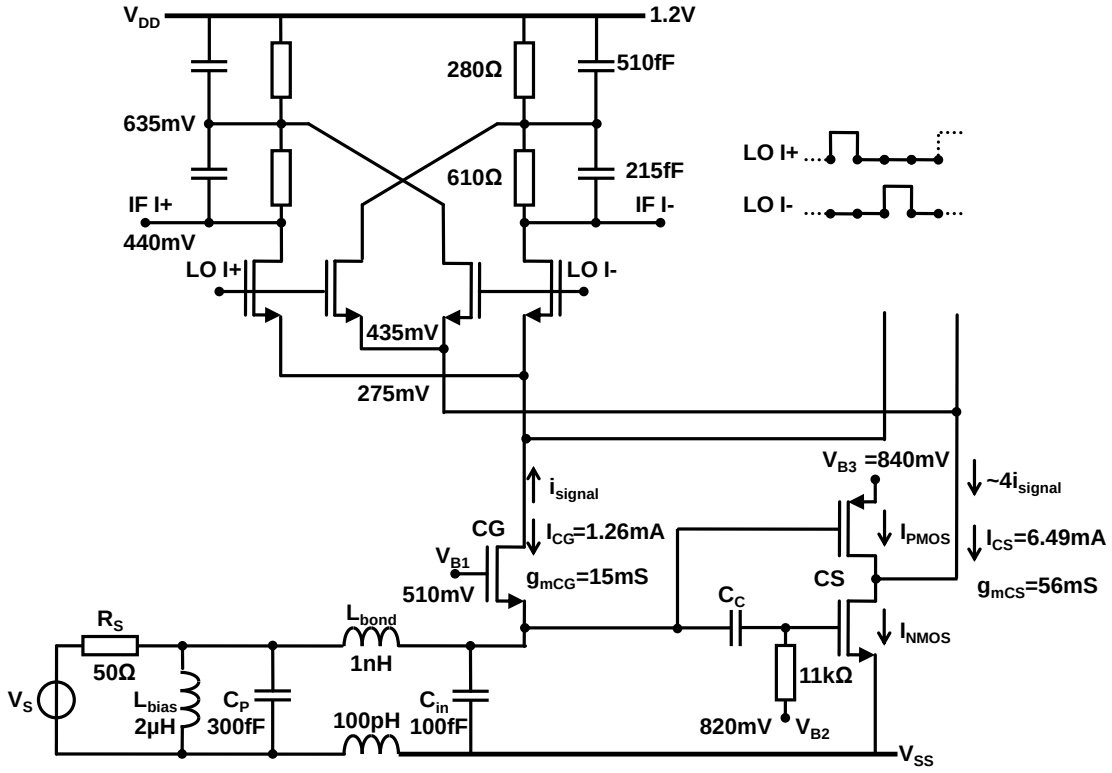

Figure 40: I-side of BLIXER with adapted IF-filter showing DC node voltages for f_{LO} = 3 GHz

Simulation results of the IF-BW of the adapted BLIXER are shown in Figure 41 for a square wave LO of 3 GHz with 24 % duty cycle and 1% rise- and falltime.

It can be seen that the IF-BW is increased to ~ 910 MHz, but is still a bit lower than the required 1.05 GHz. A side effect of increasing the IF-bandwidth is the decrease in conversion gain for low IF-frequencies. It can be seen that the conversion gain is almost 1 dB decreased. As can be seen in Figure 40 the DC-node voltages at the IF-output are slightly increased, since higher order frequency components as a result of frequency mixing are less attenuated by the IF-filter. This results in a slightly decrease in conversion gain and a little increase in noise figure.

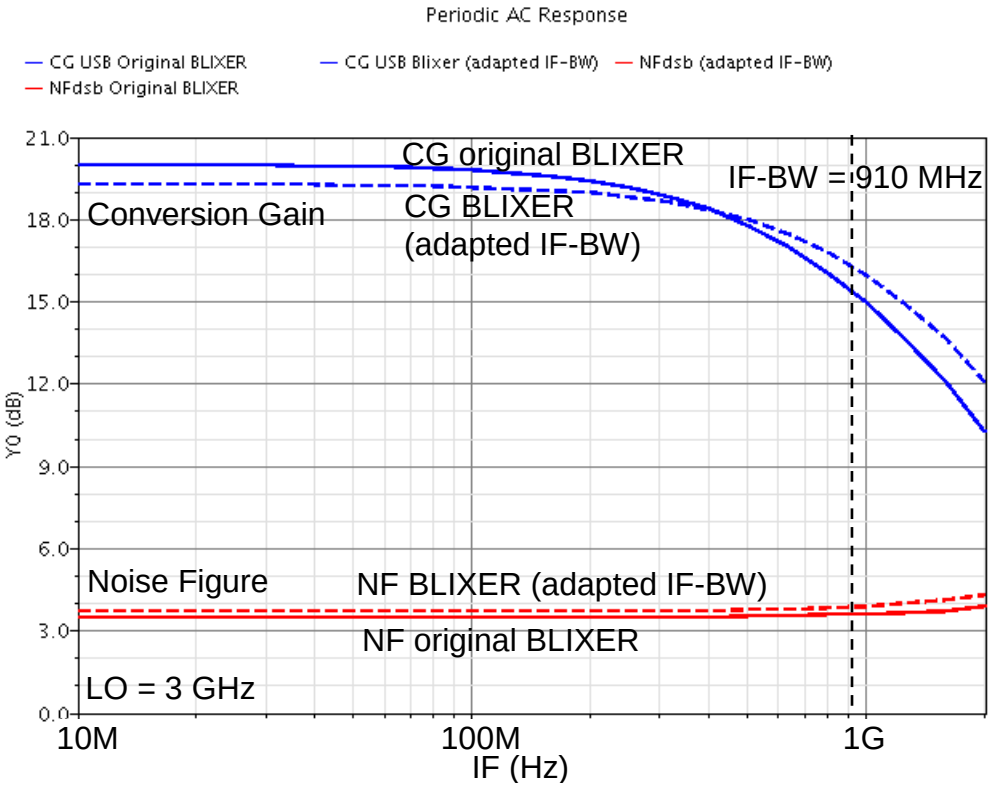

Figure 41: IF bandwidth of original and adapted BLIXER

3.1.3 Adapting RF-input bandwidth BLIXER

It is preferable to test the mixer driven with sine wave signals for the conditions of the satellite receiver. Therefore the input BW is made suitable for the satellite RF-BW of 10.7 GHz up to 12.75 GHz. The current BLIXER topology has a broadband matching π-network at the RF-input port as shown in Figure 42. The matching network takes care of matching the input impedance of the BLIXER over a large bandwidth of 500 MHz up to 10 GHz to the impedance of the external antenna to avoid reflections. The satellite receiver however requires a bandwidth of 10.7 GHz up to 12.75 GHz. The broadband matching network is therefore replaced by a bandpass filter.

The bandpass filter is formed by the input capacitance of the BLIXER and an inductor L_{bias} which also is used for biasing the common gate transistor. The value for the inductor is chosen according to the required center frequency of the pass band and with the already familiar formula:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 11.7\ GHz \rightarrow L = \frac{1}{(2\pi f_0)^2 C} \tag{3.7}$$

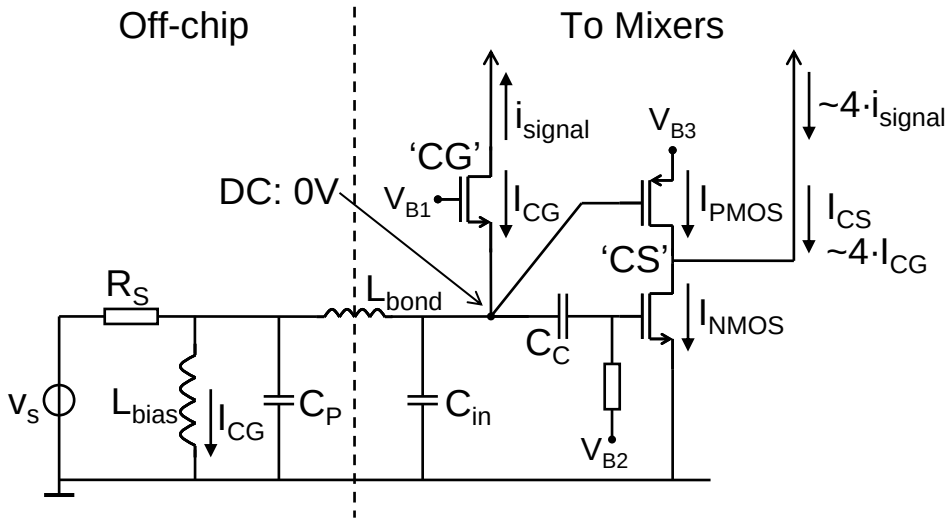

Figure 42: original RF-input stage of the BLIXER

The RF-input capacitance of the BLIXER varies according to simulation results between 400 fF and 500 fF for the RF-input frequency range of 10.7 GHz up to 12.75 GHz. The required inductor therefore should be equal to 411 pH:

$$L = \frac{1}{(2 \cdot \pi \cdot 11.7 \cdot 10^9)^2 450 \cdot 10^{-15}} = 411\ pH \tag{3.8}$$

The inductor chosen is somewhat larger (L_{bias} = 620 pH), since simulation results showed a center frequency larger than expected with an inductor of 411 pH.

The required quality factor of the inductor can be calculated since we know that the bandwidth of an LC-bandpass filter is inversely proportional to the quality factor Q [4,p.90]:

$$\frac{BW}{\omega_0} = \frac{1}{Q_0} \rightarrow \frac{2.05GHz}{11.7GHz} = \frac{1}{Q_0} \rightarrow Q_0 = \frac{11.7}{2.05} = 5.7 \tag{3.9}$$

So the required quality factor of the inductor L_{bias} is equal to 5.7. This corresponds to a series resistance of the inductor of:

$$Q_0 = \frac{\omega_0 L}{R_S} = 5.7 \rightarrow R_S = \frac{\omega_0 L}{Q_0} = \frac{2 \cdot \pi \cdot 11.7 \cdot 10^9 \cdot 620\, pH}{5.7} = 8.0\ \Omega \qquad (3.10)$$

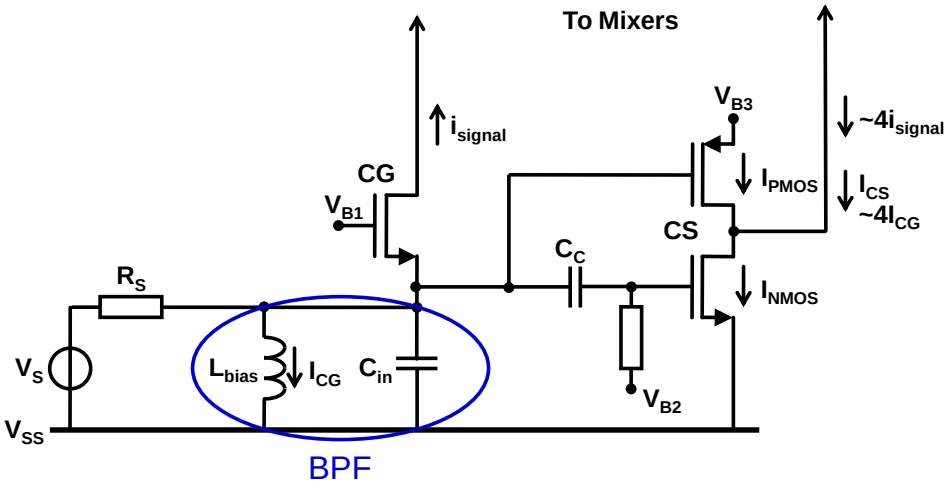

Figure 43: Adapted input stage BLIXER

The series resistance however is chosen two times smaller (R_S = 4 Ω) to create a somewhat steeper bandpass filter. The quality factor for the inductor therefore becomes: $Q_0 = 2 \cdot 5.7 = 11.4$. The adapted input stage of the BLIXER is shown in Figure 43. The transfer function of the bandpass filter is shown in Figure 44.

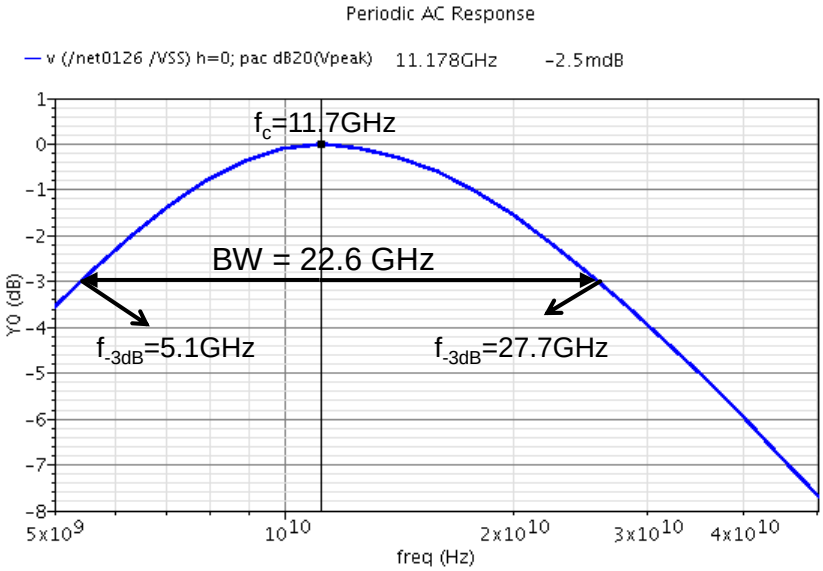

Figure 44: Transfer function bandpass filter at the RF-input of the BLIXER

3.2 Sine wave LO vs. square wave LO

Now in the previous paragraph the BLIXER topology has been adapted for the RF-input and IF-output frequency range of the satellite receiver, we're able to test the BLIXER within the appropriate conditions for the satellite receiver. That means that it now can be driven with an 11.7 GHz oscillator signal and performance can be simulated for an RF-input frequency range of 10.7 GHz up to 12.75 GHz.

To be able to answer the second research question of this thesis if a mixer can be directly driven with a sine wave oscillator without buffers in between, a comparison will be made for driving the BLIXER with ideal sine wave and ideal 25 % duty cycle square wave oscillator signals. The differences in the driving waveforms will be analyzed in the time domain, as well in the frequency domain. After that, simulation results of the conversion gain and noise figure of the BLIXER driven with ideal sine waves will be analyzed and compared with the performance of driven with ideal square waves.

3.2.1 Difference in steepness of transitions for sine wave and square wave

A sine wave and a 25 % duty cycle square wave with 1 % rise- and fall time will be compared here, when having the same oscillation frequency of 11.7 GHz. Note that actually the 25 % duty cycle square wave used in this thesis will have a somewhat effectively lower duty cycle as the result of a finite rise time. Since a rise time of 1 % is used, the duty cycle will be effectively equal to 24 %.

A major obvious difference between using a sine wave and square wave as driving signal for a mixer is the steepness of the curve at the switching moments of the mixer. For a low noise figure of the mixer it is important that the time interval of switching the current from one output to another will be as short as possible. That is if the switches of the mixer are in the balanced state, the switching transistors will act as a differential pair and amplify the noise on the LO-ports to the output. So, let's therefore analyze the steepness of the square wave compared to the sine wave.

As an example a square wave with a high value of 1.0 V and 0.1 V with rise and fall times of 1 % will be analyzed. This could be a good representation of a realistic output of an inverter-type buffer, which will have as somewhat smaller voltage swing than from ground to the supply voltage (of 1.2 V). The square wave applied with an ideal voltage source with source resistance of 1 ohm to one of the LO-inputs will look like the one plotted in Figure 45. The steepness $\frac{dv}{dt}$ of the transistion between the low and high value is simply equal to the voltage difference divided by the risetime:

$$\left(\frac{dv}{dt}\right)_{square\ wave} = \frac{high - low}{risetime} \tag{3.11}$$

So for a square wave of 11.7 GHz from 0.1 V to 1.0V with 1% rise and falltime, the steepness of transistion will be:

$$\left(\frac{dv}{dt}\right)_{square\ wave} = \frac{1\ V - 0.1\ V}{1\ \%\ of\ T = 85.5\ ps} = \frac{0.9\ V}{855\ fs} = 1.06\ V/ps \tag{3.12}$$

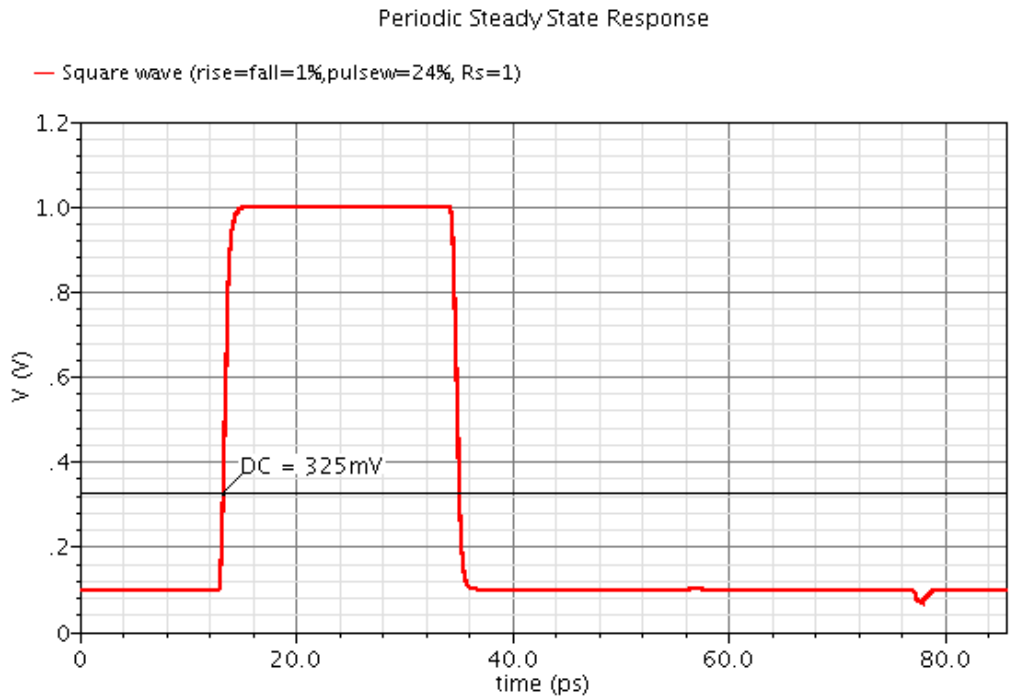

Figure 45: 11.7 GHz square wave with 24 % duty cycle and 1 % rise- and fall time driving one of the LO-ports of the BLIXER

Let's compare the just calculated steepness of the square wave to a sine wave (as shown in Figure 46) toggling between the same voltage levels. For a sine wave the steepness of transition (at the DC-level of the sine wave) is determined by the derivative of the sine wave:

$$\left(\frac{dv}{dt}\right)_{sine\ wave} = \frac{d}{dt}\left(V_{CM} + V_{AMPL}\sin\left(\frac{2\pi t}{T}\right)\right) = \frac{2\pi V_{AMPL}}{T}\cos\left(\frac{2\pi t}{T}\right) \tag{3.13}$$

Where V_{CM} represents the common mode level, V_{AMPL} the amplitude and T the period of the sine wave. The steepness at the crossings of the DC-level of the sine wave is when the derivative is at its maximum, which is equal to:

$$\left(\frac{dv}{dt}\right)_{max,sine\ wave} = \frac{2\pi V_{AMPL}}{T} \tag{3.14}$$

For an amplitude of 450 mV and a frequency of 11.7 GHz, the steepness of the sine wave at the crossings of the DC-level will be therefore equal to:

$$\left(\frac{dv}{dt}\right)_{max,sine\ wave} = \frac{2 \cdot \pi \cdot 0.45\ V}{85.5\ ps} = 33mV/ps \tag{3.15}$$

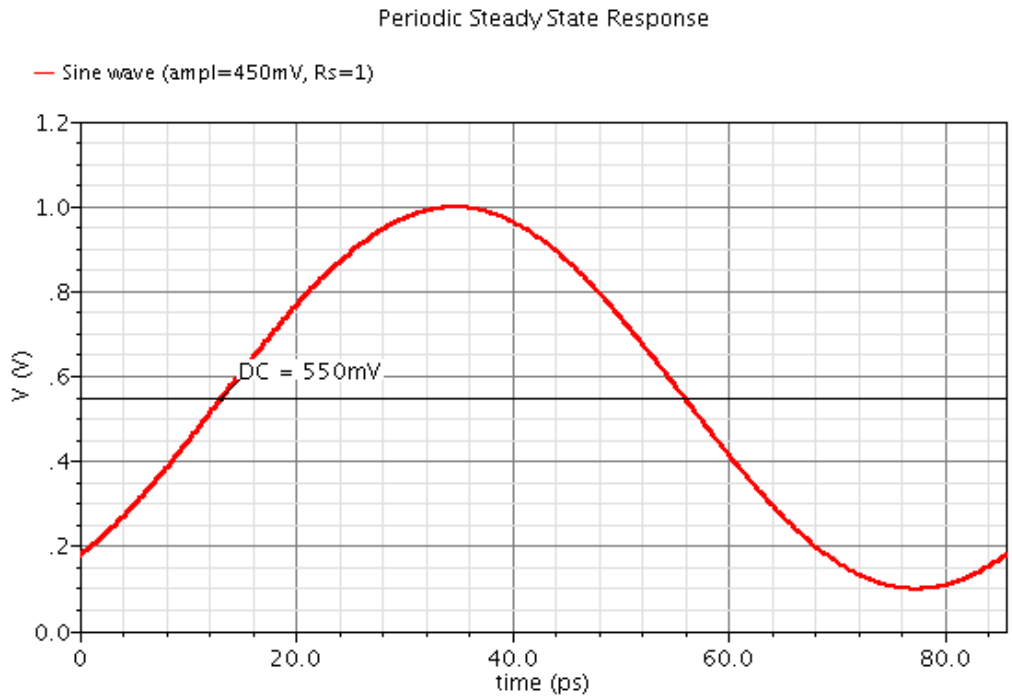

Figure 46: 11.7 GHz sine wave with amplitude of 450 mV and common mode level of 550 mV driving one of the LO-ports of the BLIXER

If we rewrite the expression for the steepness of the square wave (equation 3.11) into the following form:

$$\left(\frac{dv}{dt}\right)_{square\ wave} = \frac{high - low}{risetime} = \frac{2V_{AMPL}}{t_{rise(\%)} \cdot T} \tag{3.16}$$

With $t_{rise(\%)}$ the rise time for the square wave written in a percentage of the total period. Then we can see that the difference in steepness of transition for a sine wave compared to that of a square wave can be written as:

$$\frac{\left(\frac{dv}{dt}\right)_{max,sine\ wave}}{\left(\frac{dv}{dt}\right)_{square\ wave}} = \frac{\frac{2\pi V_{AMPL}}{T}}{\frac{2V_{AMPL}}{t_{rise(\%)} \cdot T}} = \pi \cdot t_{rise(\%)} \tag{3.17}$$

So as we can see here that for a sine wave toggling between the same voltage as the square wave, the sine wave will have a smaller steepness of π times the risetime (in %) of the square wave, when compared to the steepness of the square wave. This means that for the example here for a rise time of 1 %, the sine wave will have a transition which is ~ 32 times less steep than for the square wave:

$$\begin{aligned}\left(\frac{dv}{dt}\right)_{max,sine\ wave} &= \pi \cdot t_{rise(\%)} \cdot \left(\frac{dv}{dt}\right)_{square\ wave} = \pi \cdot 0.01 \\ &= \frac{1}{31.8}\left(\frac{dv}{dt}\right)_{square\ wave}\end{aligned} \tag{3.18}$$

3.2.2 Higher order frequency components in square wave

Compared to a sine wave, which has ideally one frequency component, a square wave will consist of a lot of higher order frequency components. To visualize this, the frequency spectrum has been plotted in Figure 47 for a square with 24 % duty cycle, toggling from 0.1 V to 1.0 V and with a rise- and fall time of 1 %.

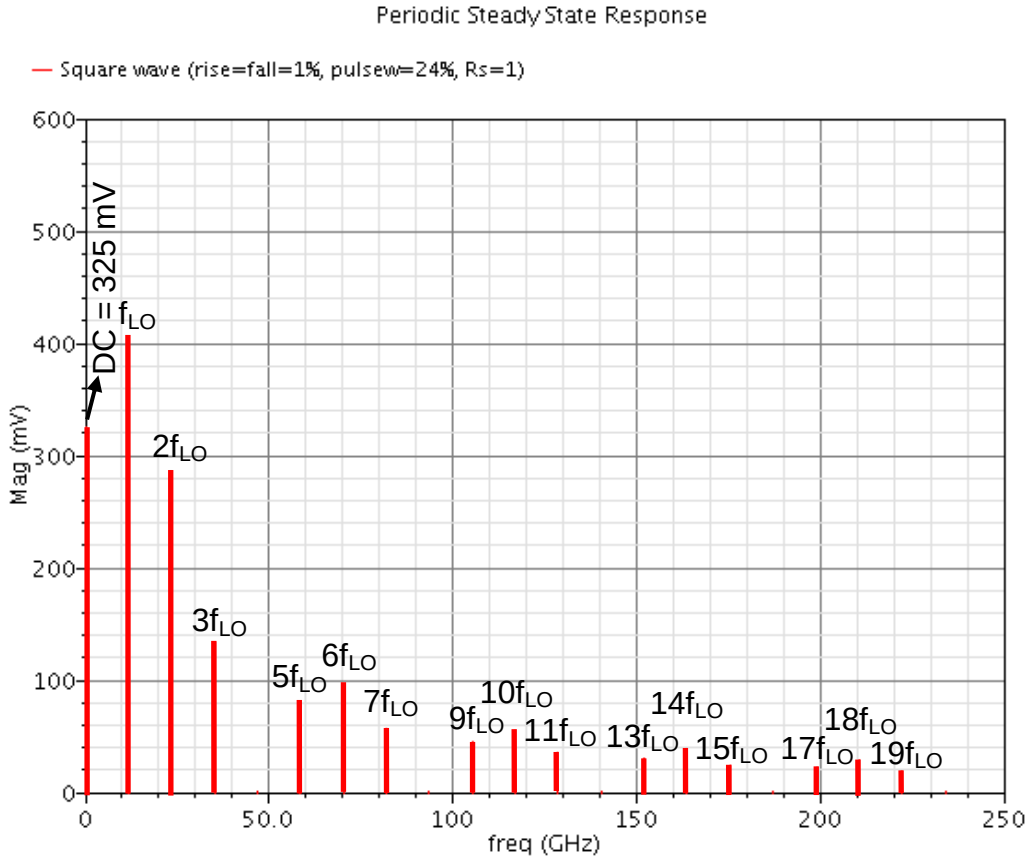

Figure 47: Frequency spectrum of an 11.7 GHz square wave with 24 % duty cycle and 1 % rise- and fall time driving one of the LO-ports of the BLIXER

As can be seen the fundamental harmonic has an amplitude of ~ 410 mV, which is a bit smaller than the amplitude of 450 mV of the sine wave seen in Figure 46. It can be seen that a lot of signal energy is present at higher harmonics. For example the 6th harmonic even has an amplitude of 100 mV, which is more or less a quarter of the amplitude of the fundamental harmonic.

However it is very likely that when driving the BLIXER with a more realistic square wave, most of the higher harmonics will be attenuated by the corner frequency at the LO-input ports as a result of the large input capacitance (~550 fF for the BLIXER) and the output resistance of the square wave oscillator.

3.2.3 Simulated BLIXER performance with sine wave and square wave LO

The BLIXER will now be driven with ideal sine wave oscillator signals of 11.7 GHz and the conversion gain and noise figure performance compared to driving with 25 % duty cycle square wave oscillator signals of 11.7 GHz. The LO-ports will therefore be driven wit an ideal voltage source with a source resistance of 1 ohm to keep enough bandwidth at the input port for the higher harmonics of the square wave (as mentioned earlier in 3.1.1). For the square wave rise- and fall times are used of 1 % and an effective duty cycle of 24 %. The minimum and maximum voltage for both the sine wave and square wave are chosen the same, i.e. 100 mV and 1.0 V respectively. The simulation results for the conversion gain and the noise figure are given in Figure 48 for an input RF-frequency range of 1.7 GHz up to 10.69 GHz (LSB).

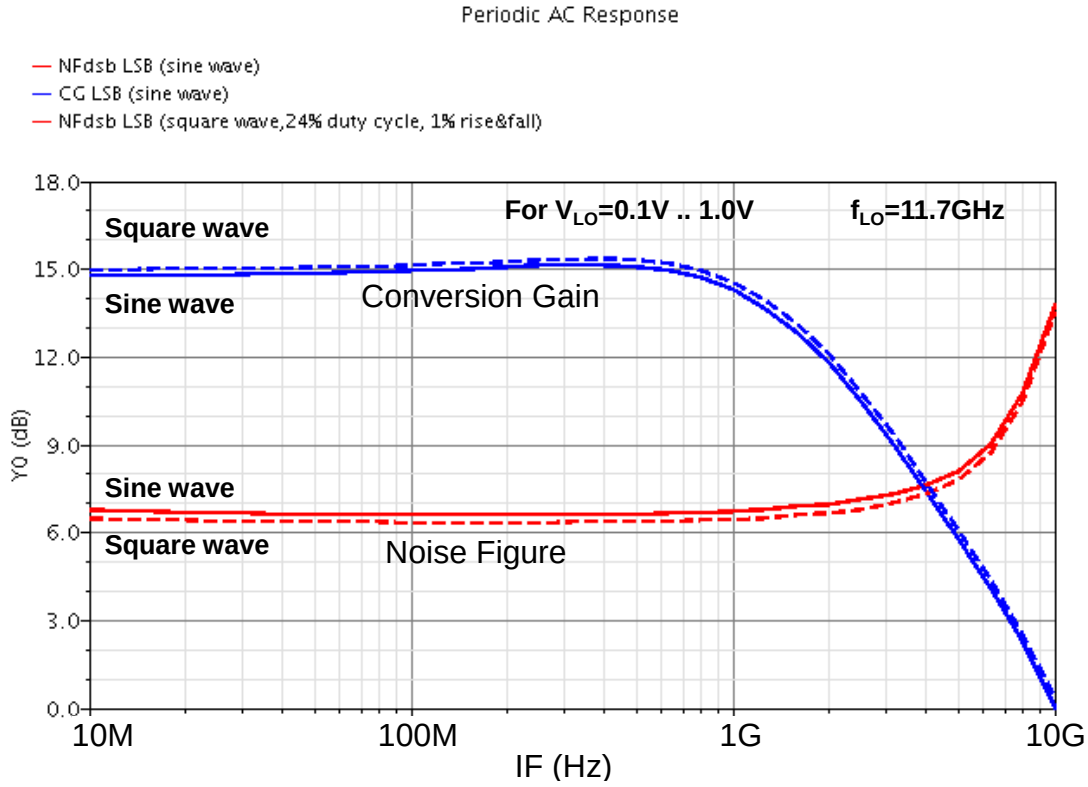

Figure 48: Conversion gain and noise figure of BLIXER for driving with sine wave and square wave LO of 11.7 GHz

As can be seen in Figure 48 for the BLIXER driven with a sine wave only little decrease in conversion gain is observed (~0.3 dB) and only little increase in noise figure is observed (also ~0.3dB) compared to driving the BLIXER with a square wave.

Compared to the performance of the original BLIXER for RF- frequencies between 500 MHz and 10 GHz as already shown in Figure 38, the high RF-frequency performance shown here does agree with each other. For instance the original BLIXER showed a conversion gain of 16 dB for an input RF-frequency of 10 GHz. The conversion gain plotted here for an IF-frequency of 700 MHz (corresponding to an RF-frequency of 11 GHz) is approximately 1 dB lower, i.e. 15 dB. Also the noise figure does agree well with what we saw earlier for the NF performance for high RF-input frequencies in Figure 38 (~7dB).

Furthermore it can be noted that the voltage conversion gain has a bit of a peak for an IF of around 400 MHz. This IF-frequency corresponds to an RF-frequency of 11.3 GHz. Simulation shows that for this input frequency the CG-stage shows a little dip in the transfer from input voltage to output current. It can be that as a result of this somewhat lower signal current, there is more drain-source voltage room for the switching transistor. This can give a higher output resistance and also a larger conversion gain.

In Figure 49 and Figure 50 the DC-node voltages are shown of the BLIXER for respectively a square wave oscillator signal and a sine wave oscillator signal.

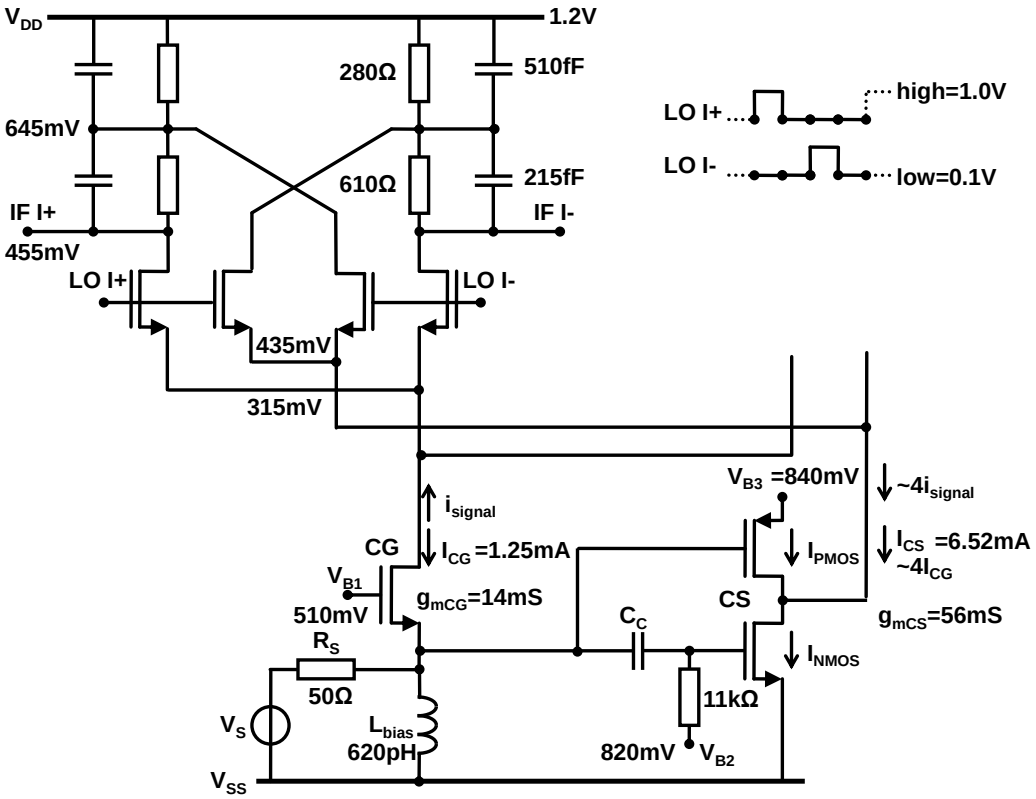

Figure 49: BLIXER showing DC-node voltages for square wave f_{LO}=11.7GHz with 24 % duty cycle and 1 % rise and fall time

It can be seen that for driving the BLIXER with sine wave oscillator signals, the DC-node voltages at the output with 25mV/30mV. However the voltage at the source node of the switching transistors in the CG-path is lower for the sine wave case. This means that more drain-source voltage room (~190 mV compared to 140 mV) is available for these switching transistors in the case when driven with sine wave oscillator signals. The drain-source voltage room for the switches in the CS-path has increased from 210 mV to 260 mV. This shows that as a result of driving the BLIXER with sine wave oscillator signals, the DC-bias setting of the BLIXER is affected. In the next paragraph therefore the ideal common mode level and amplitude for the sine wave will be determined to keep the BLIXER biased within the appropriate DC-bias settings.

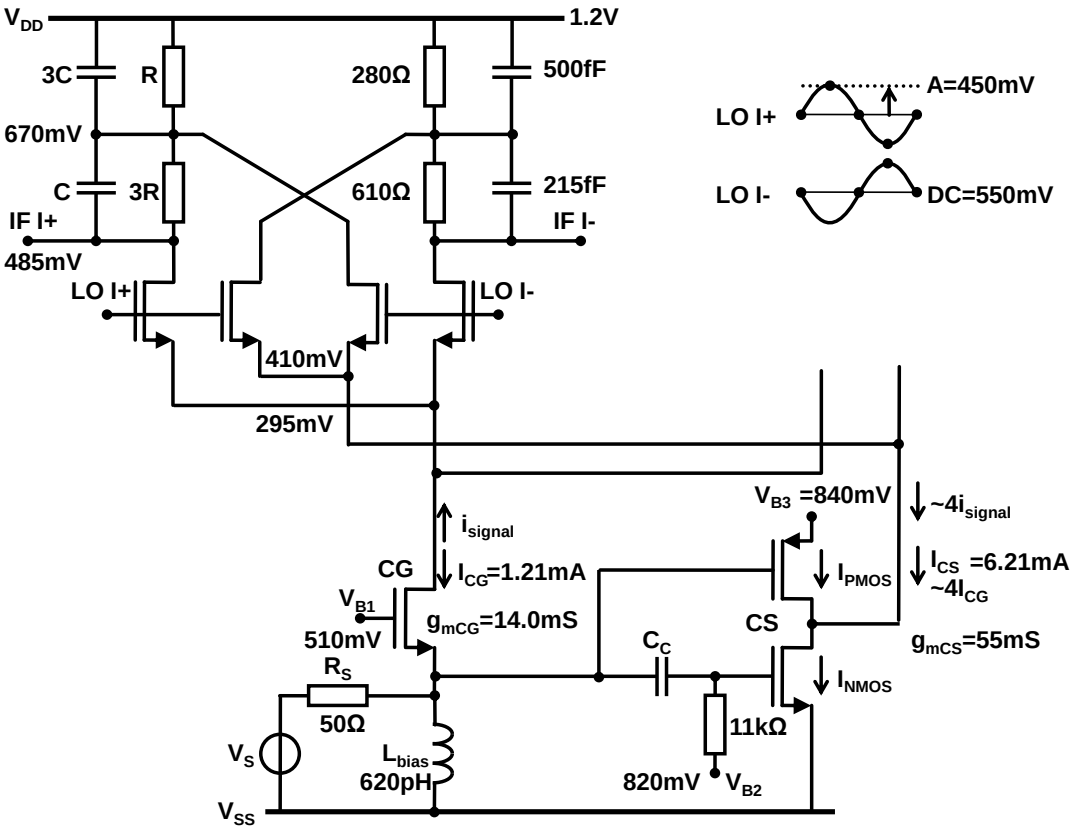

Figure 50: BLIXER showing DC-node voltages for sine wave f_{LO}=11.7GHz

3.3 Optimum CM-level & amplitude sine wave

In this paragraph the optimum common mode level and amplitude of the sine wave oscillator signal will be determined, when used for driving the BLIXER. The optimum CM-level and amplitude will be defined in terms of a maximum voltage conversion gain and a minimum noise figure for the BLIXER.

At first the optimum amplitude of the sine wave will be determined for three different common mode levels of the sine wave as can be seen in Figure 51. The conversion gain and noise figure of the BLIXER is plotted for a fixed oscillation frequency of 11.7 GHz, a fixed IF of 50 MHz and as function of the oscillator-amplitude. As can be seen each common mode level has different optimum amplitude. For example the optimum amplitude for a CM-level of 600 mV is roughly equal to 600 mV. The conversion gain is at this point 16.3 dB and the noise figure of the BLIXER is 6.8 dB. Furthermore it can be noted that for a common mode level of 900 mV the BLIXER has unacceptable performance, with a maximum conversion gain of 6 dB and a minimum noise figure of 11 dB. This confirms the fact that AC-coupling in the oscillator implementation is necessary, since the bias level of the XCP was fixed to 900 mV.

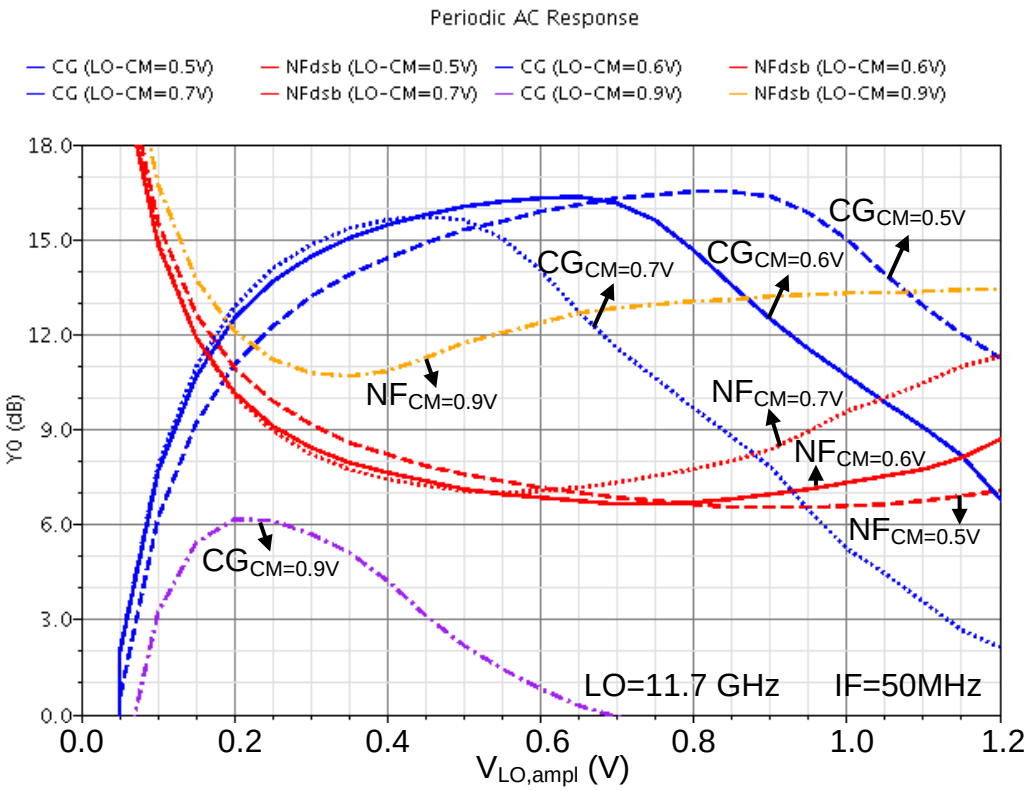

Figure 51: Conversion gain and noise figure of BLIXER for three different CM-levels for the sine wave LO (IF = 50MHz)

Note that the each optimum common mode voltage with half the corresponding optimum amplitude is roughly equal to 900 mV. The common mode voltage added with half the LO-amplitude equals the maximum gate voltage at the switching transistors. The value of the source voltages of the switching transistors will be more or less forced by the maximum gate voltage at the switching transistors minus the gate-source voltage needed for carrying the total current through one switch.

If the maximum applied gate voltage at the switching transistors becomes larger than the optimum, the voltage at the sources will also go up and will lower the drain-source voltage room of the switches and will eventually drive them out of saturation. This will lower the output resistance of the switches and the transconductance, which explains the lower conversion gain and higher noise figure if the gate voltage becomes larger than the optimum of ~ 900 mV. If the maximum applied gate voltage at the switching transistors will become smaller than the optimum, then the drain source voltage room for the NMOS CS and - CG transistors will become smaller and eventually drive them out of saturation. This will decrease the transconductance of the Gm-stage of the BLIXER, which will decrease the conversion gain and will increase the noise figure.

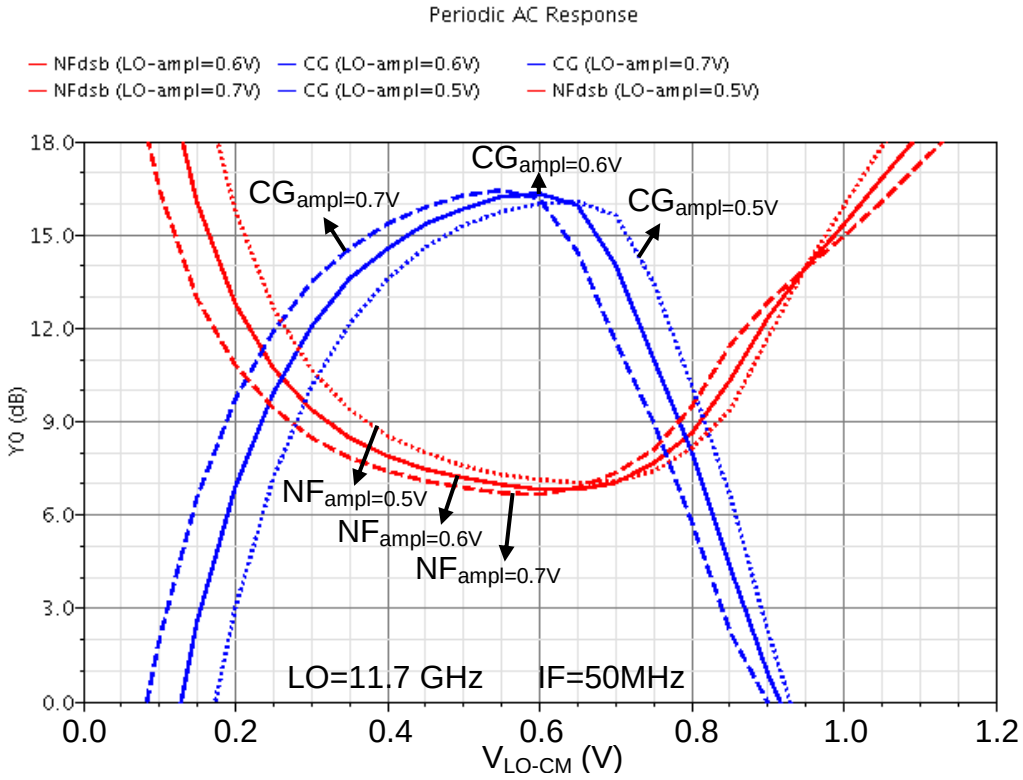

Figure 52: Conversion gain and noise figure of BLIXER for three different amplitudes for the sine wave LO (IF = 50MHz)

In Figure 52 the conversion gain and noise figure is plotted for three different amplitudes of the sine wave oscillator to determine the optimum common-mode voltage for each LO-amplitude. This more or less confirms the results obtained before from Figure 51 that the optimum common mode voltage added with half the LO-amplitude will be roughly equal to 900 mV. The conversion gain and the noise figure will be slightly better for a larger LO-amplitude than for a smaller LO-amplitude. Since the voltage swing of the used oscillator is more or less limited to 600 mV, it is chosen to use the optimum CM-level of 600 mV together with an LO-amplitude of 600 mV. The DC-bias settings of the BLIXER for an applied sine wave oscillator with a CM-level of 600 mV and amplitude of 600 mV can be seen in Figure 53. Too confirm good performance of the BLIXER for the used CM-level and amplitude of the oscillator for the entire IF-bandwidth, the corresponding conversion gain and noise figure has been plotted in Figure 54.

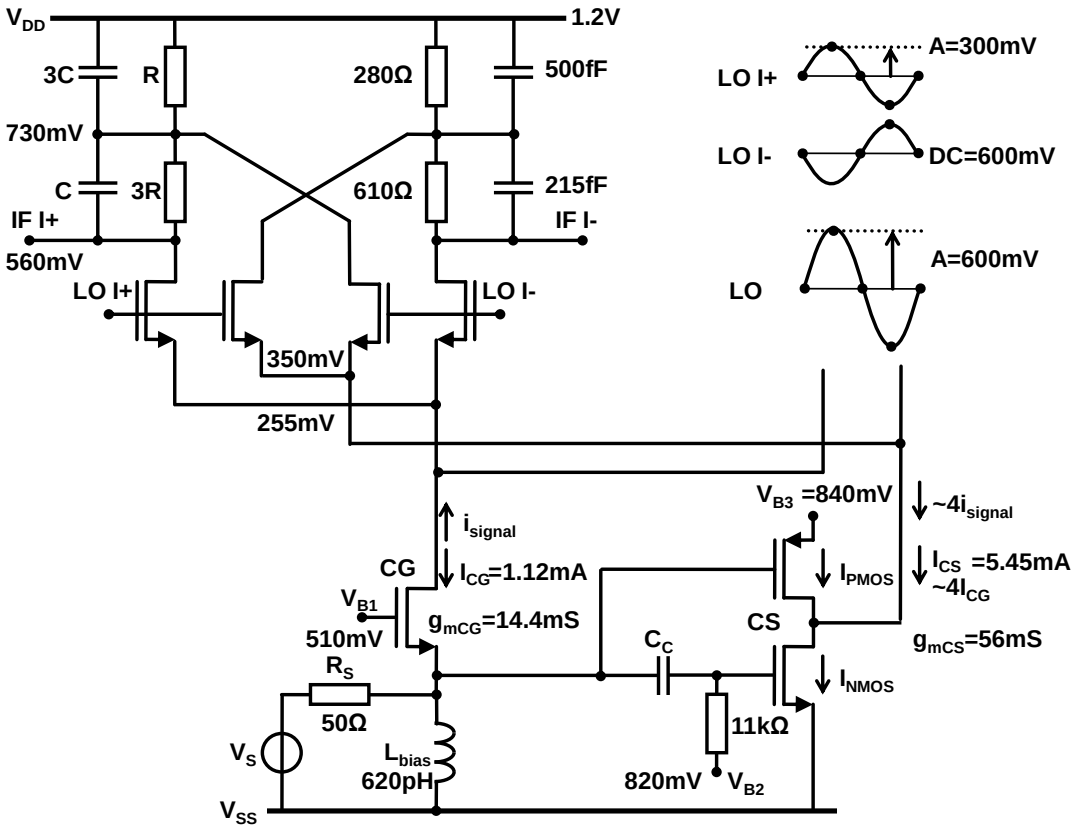

Figure 53: BLIXER showing DC-node voltages for sine wave f_{LO}=11.7GHz with optimum CM-level and amplitude

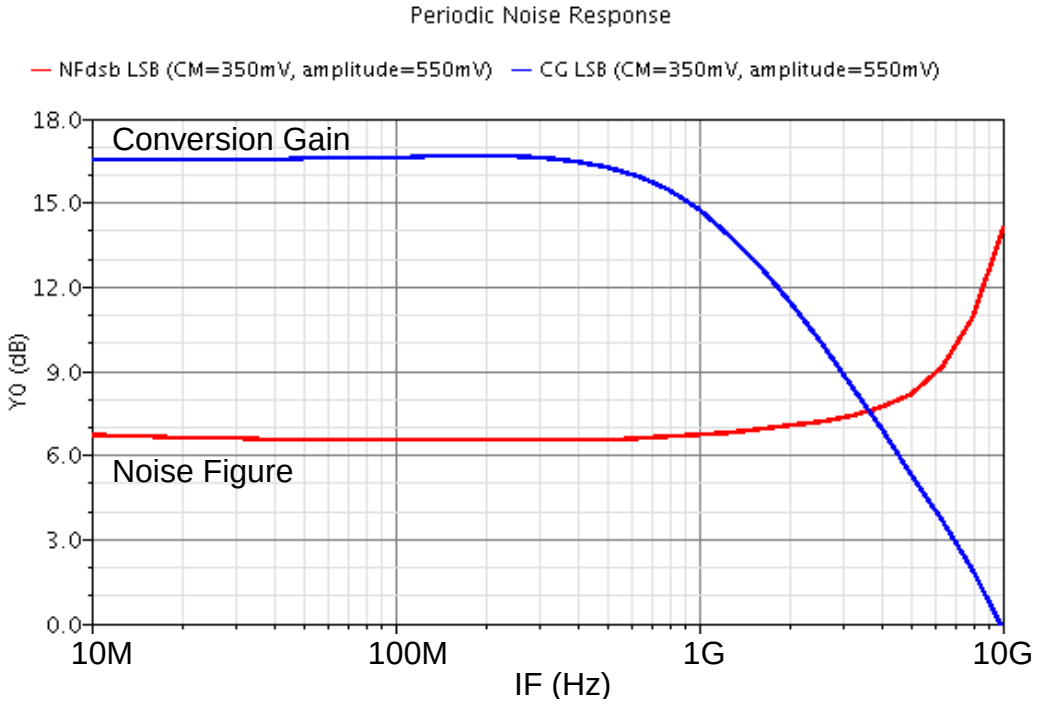

Figure 54: Conversion gain and noise figure of BLIXER for CM-level of 350 mV and amplitude of 550 mV of sine wave LO with f_{LO} = 11.7 GHz

3.4 Driving BLIXER with bufferless VCO

The BLIXER will now be driven by the VCO designed earlier in this thesis which is shown in Figure 57 and effects on the performance of the BLIXER will be analyzed. The conversion gain and the noise figure of the BLIXER will be compared for three cases: i.e.

1. BLIXER driven with ideal sine wave
2. BLIXER driven with buffered VCO
3. BLIXER driven with bufferless VCO

3.4.1 Test conditions

1. BLIXER driven with ideal sine wave

The test conditions for the simulation of the performance of the BLIXER when driving with ideal sine wave signals differs a bit from the one used in section 2.3.2 when comparing the performance of the BLIXER for square wave LO and sine wave LO. Again ideal voltage sources are used with a source resistance of 1 ohm, only now a different LO-amplitude and CM-level is used as the result of the obtained ideal LO-amplitude and CM-level in the previous paragraph. Of course for fair comparison between the three cases the same LO-amplitude and CM-level is used for all three cases.

2. BLIXER driven with buffered VCO

The BLIXER will also be driven with the designed VCO earlier in this thesis with ideal buffers in between. This has been done to analyze the effect of driving the BLIXER with a realistic VCO, but to shield the BLIXER from the LC-oscillator just for the moment. Only the I-side will be driven with the buffered VCO. The oscillator signals for the Q-side of the BLIXER will be generated by an ideal RC-CR polyphase filter, which is also connected trough ideally buffers with the VCO. This will be the same polyphase filter, earlier used in paragraph 2.4.2, when the effects on performance were analyzed when loading the VCO with the BLIXER.

Since the BLIXER is shielded from the VCO, the input capacitance of the BLIXER won't be part of the LC-tank anymore. To keep the conditions for the VCO as much as the same as possible, the VCO will be loaded with ideal capacitances, such that the same tank capacitance can be used. Only the bias current then has to be adapted, since the VCO is now loaded with lossless components instead of the BLIXER, who introduced extra tank losses. The used XCP topology with all the accompanying component values can be seen in Figure 55.

The test setup with driving the BLIXER with the buffered VCO will be useful to see the effect on mixing the RF-frequencies with the spectrum of a non-ideal oscillator signal with phase noise. The phase noise of the VCO used here is shown in Figure 56.

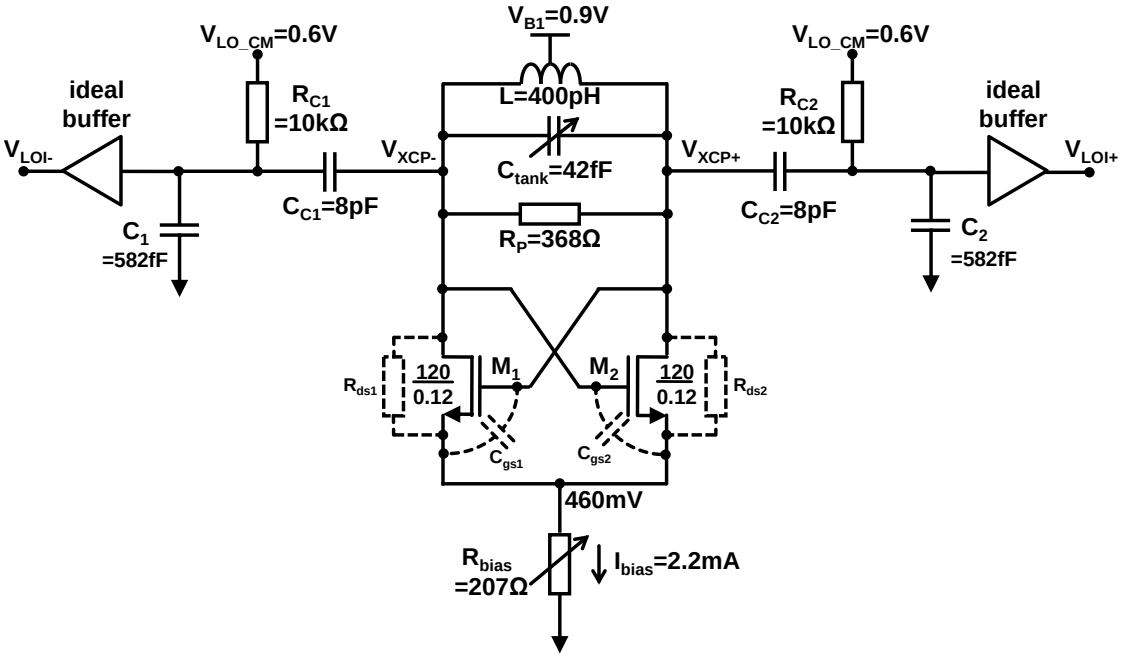

Figure 55: VCO used for driving buffered I-side of BLIXER

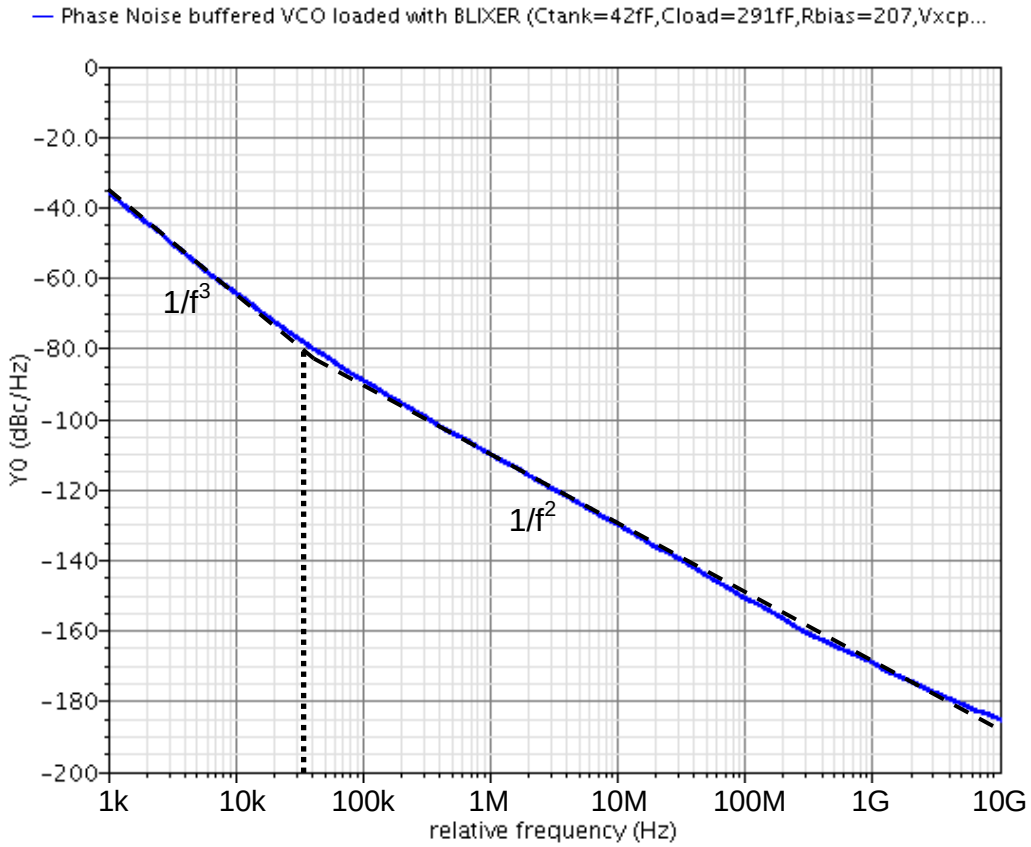

Figure 56: Phase noise of buffered VCO driving I-side of BLIXER

3. BLIXER driven with bufferless VCO

As a final test the BLIXER will be driven directly with the designed VCO. Only one mixer pair will be driven (the I-mixer in this case) and to drive the other mixer pair (Q-mixer) again the ideal RC-CR poly-phase filter will be used. The VCO and mixer now can fully interact with each other and effects on performance on the BLIXER can be analyzed. As we've seen before the mixer introduces extra losses in the XCP, which is again compensated with a larger bias current in the XCP. Furthermore the input capacitance of the mixer adds up to the total tank capacitance in the VCO, therefore the tank capacitance is decreased to compensate for that. This has resulted in the XCP topology with the accompanying component values showed in Figure 57. This VCO will give the desired oscillation frequency of 11.7 GHz and desired tank amplitude of 1.2 V_{pp} if it is loaded with the BLIXER.

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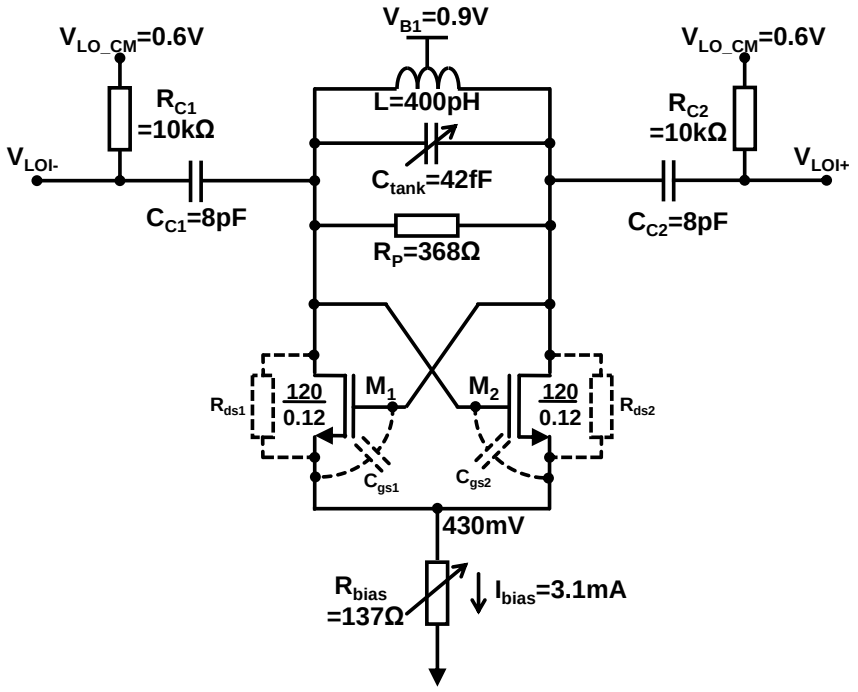

Figure 57: VCO used for driving bufferless I-side of BLIXER

Loading the VCO with the BLIXER will affect the phase noise of the XCP as we've seen already in chapter 2. The phase noise performance of the VCO presented above loaded with the BLIXER was already plotted in Figure 32 in chapter 2, but is plotted here again together with the phase noise of the unloaded VCO in Figure 58. As can be seen in Figure 58 (and already known from chapter 2) the phase noise of the VCO loaded with the BLIXER is larger for offset frequencies up to 1 GHz. It is expected that driving the BLIXER with a VCO with an increased phase noise for low offset frequencies will also increase the noise figure of the BLIXER for low intermediate frequencies.

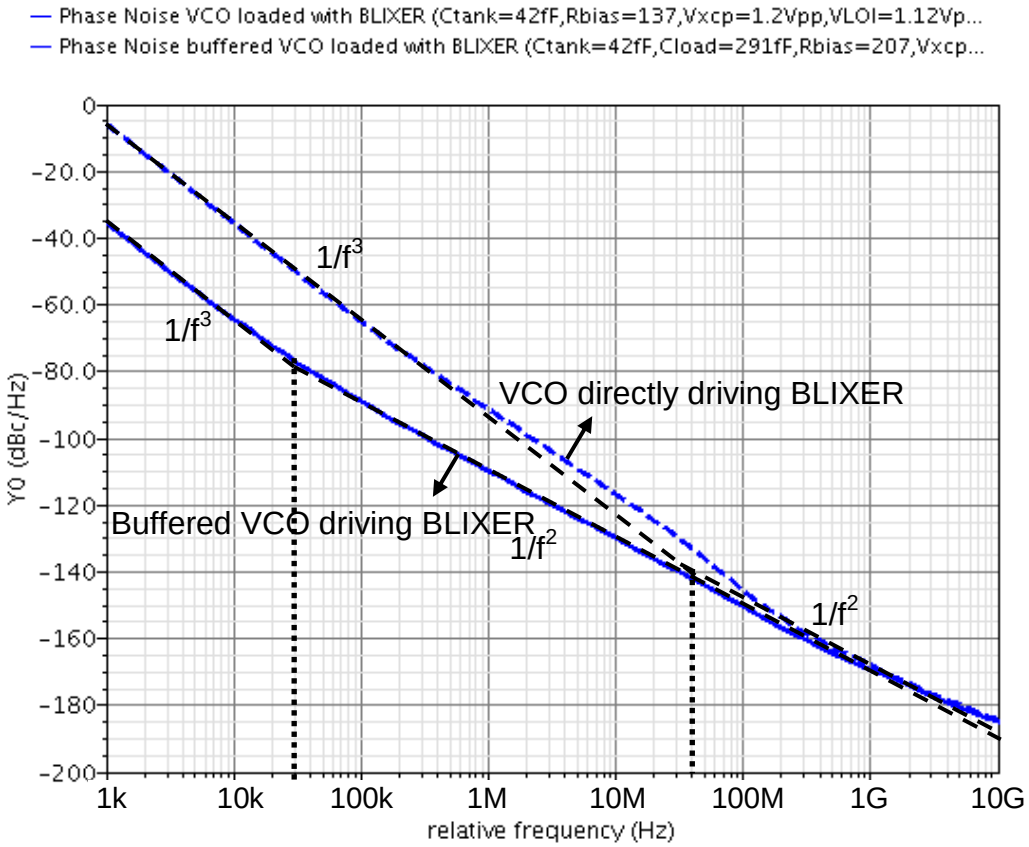

Figure 58: Phase noise of VCO used for driving bufferless I-side of BLIXER compared to phase noise of VCO driving buffered BLIXER

3.4.2 Simulation results

The simulation results for driving the BLIXER under the test conditions described in the previous section are shown in Figure 59. The conversion gain and noise figure is presented for the LSB (RF=11.69 GHz up to 9.7 GHz) for three cases:

1. BLIXER driven with ideal sine wave
2. BLIXER driven with buffered VCO
3. BLIXER driven with bufferless VCO

It can be seen that the conversion gain curves for the BLIXER driven with ideal sine waves and for the buffered and bufferless VCO fall more or less over each other. This shows that driving the BLIXER directly with a VCO without buffers in between has only a minor effect on the conversion gain compared to driving the BLIXER driven with ideal sine waves. Furthermore it can be seen that the effective -3 dB IF-bandwidth of the BLIXER is equal to 1.3 GHz.

The noise figure however has been degraded for the BLIXER driven with the ideally buffered VCO compared to the case when driven with an ideal sine wave as can be seen in Figure 59. The increase in noise figure is only visible for low IF-frequencies up to ~40MHz, for higher IF-frequencies the noise figure of the BLIXER driven with the ideally buffered VCO is comparable to the noise figure when driven with an ideal sine wave oscillator.

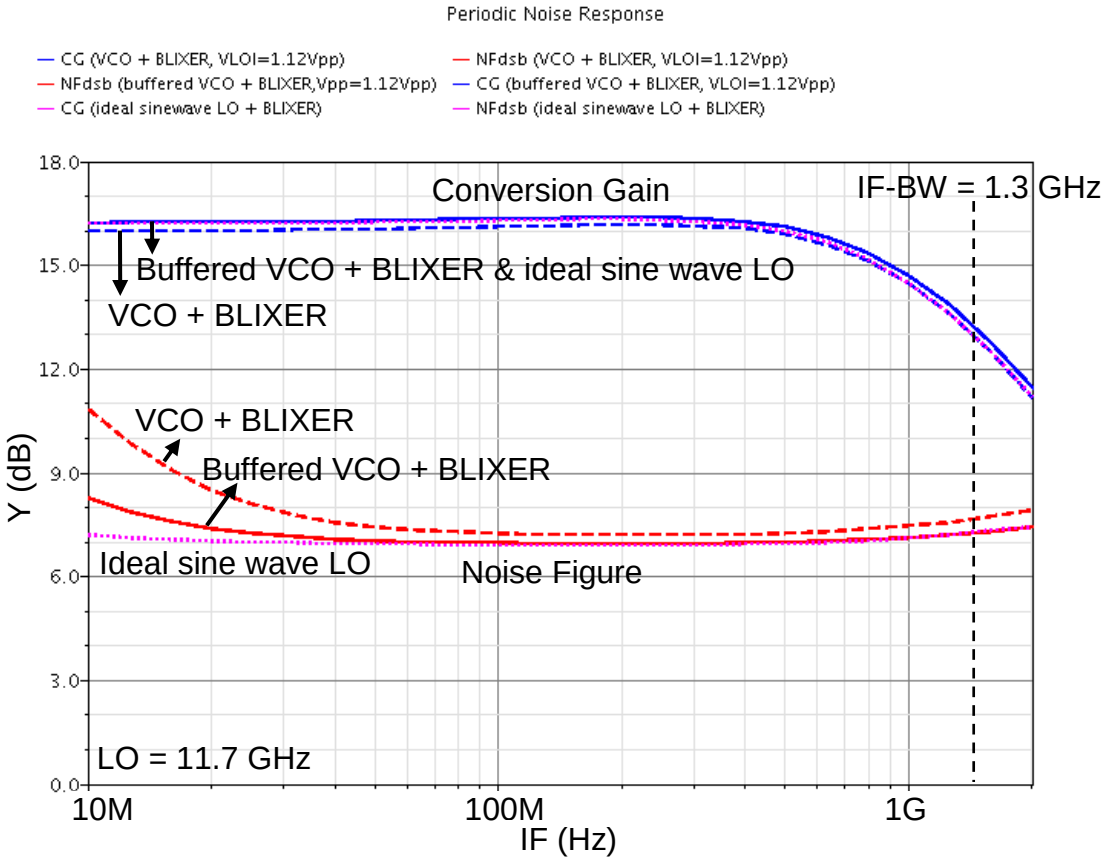

Figure 59: Conversion gain and noise figure of BLIXER driven with bufferless VCO, buffered VCO and ideal sine wave LO

The noise figure for the BLIXER directly driven with a bufferless VCO has been ~ 0.3 dB degraded compared to the case when driven with the ideally buffered VCO as can be seen in Figure 59. For low IF-frequencies the degradation is larger, for example at an IF of 10 MHz the degradation is around 3 dB compared to driving the BLIXER with the buffered VCO. To analyze the degraded noise figure performance at low IF-frequencies, the noise figures have been plotted again for the intermediate frequencies from 10 kHz up to 10 GHz in Figure 60.

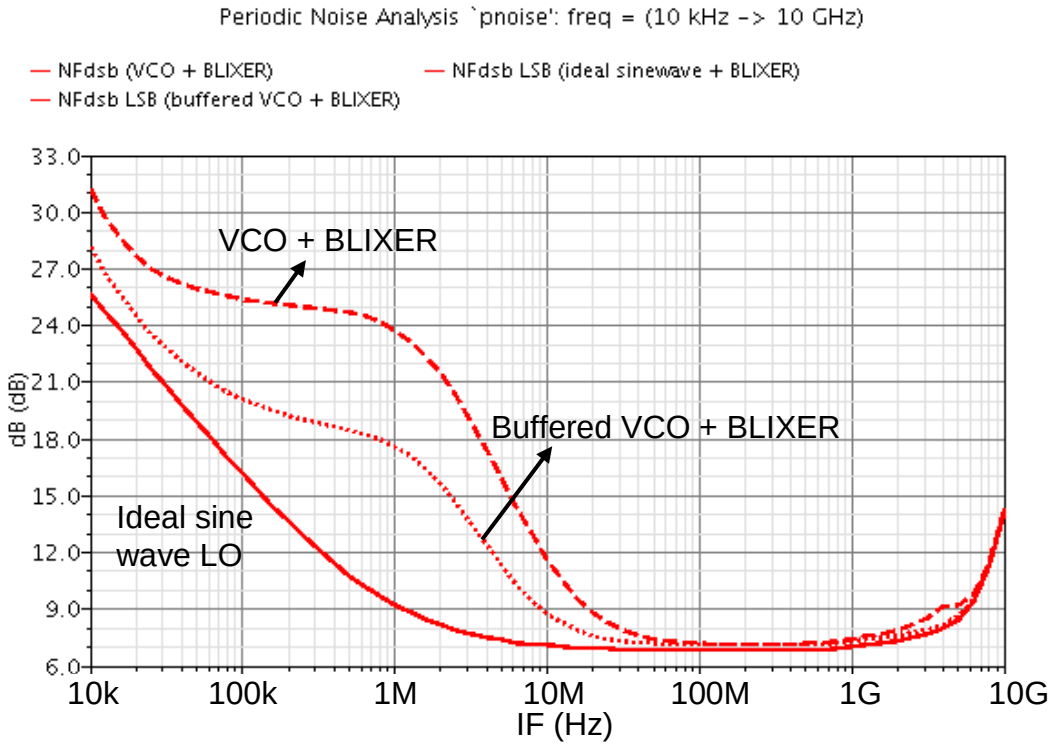

Figure 60: Noise figure of BLIXER driven with bufferless VCO, buffered VCO and ideal sine wave LO

It can be seen that for driving the BLIXER with an ideal sine wave oscillator the noise figure from an IF of 10 kHz up to ~1 MHz will be dominated by 1/f noise within the BLIXER. This is confirmed by analysis of the noise summaries, which are shown in Appendix D for each decade of the intermediate frequency. The most important noise contributions are extracted from those noise summaries and presented in Table 4. The noise figure between 10 MHz and 1 GHz of the BLIXER driven with an ideal sine wave oscillator is dominated by the thermal noise of the switching transistors.

IF (Hz)	10k	100k	1M	10M	100M	1G
Switches 1/f	**98 %**	**87 %**	**42 %**	7 %	1 %	< 1 %
Switches thermal	< 1 %	5 %	24 %	**40 %**	**43 %**	**40 %**
Load resistors	< 1 %	3 %	14 %	22 %	24 %	27 %
Input source resistance	< 1 %	2 %	12 %	20 %	21 %	20 %

Table 4: Dominant noise contributions for noise figure of BLIXER driven with ideal sine wave VCO

For noise analysis of the degraded noise figure of the BLIXER driven with the ideally buffered VCO noise summaries are presented in Appendix E for each decade of the intermediate frequency. The important noise contributions have been extracted from those summaries and presented in Table 5. This shows that the noise figure for low intermediate frequencies is dominated by 1/f noise of the cross-coupled pair transistors of the used VCO. We've already seen in paragraph 2.4 that the phase noise of an unloaded VCO is dominated with 1/f noise of the cross-coupled pair up to offset frequencies of ~10 kHz. It makes sense that this 1/f noise contribution of the cross-coupled pair is also present as an important noise contribution to the noise figure of the BLIXER for low IF. Since the 1/f noise of the cross-coupled pair has been up converted into phase noise as result of the filtering in the tank and mixed down to low IF in the BLIXER.

Between an IF of 100 kHz and 1 MHz the noise figure of the BLIXER driven with a buffered VCO is dominated by noise of the AC-coupling resistors. The shape of the noise figure in this region suggests coloring of noise with a filter with a corner frequency of 1 MHz. Since the AC-coupling has a -3 dB corner frequency this can be ascribed to the filtering of the AC-coupling. For intermediate frequencies between 10 MHz and 1 GHz the noise figure is dominated again by the thermal noise of the switching transistors, as is also the case for the BLIXER driven with an ideal sine wave oscillator.

IF (Hz)	10k	100k	1M	10M	100M	1G
Switches 1/f	16 %	30 %	7 %	5 %	< 1 %	< 1 %
Switches thermal	< 1 %	2 %	4 %	**33 %**	**47 %**	**47 %**
Load resistors	< 1 %	1 %	2 %	15 %	21 %	25 %
Input source resistance	< 1 %	1 %	2 %	13 %	19 %	19 %
XCP 1/f	**59 %**	1 %	< 1 %	< 1 %	< 1 %	< 1 %
AC-coupling resistors	3 %	**56 %**	**84 %**	28 %	< 1 %	< 1 %

Table 5: Dominant noise contributions for noise figure of BLIXER driven with buffered VCO

For noise analysis of the degraded noise figure of the BLIXER directly driven with the bufferless VCO noise summaries are presented in Appendix F for each decade of the intermediate frequency. The important noise contributions have been extracted from those summaries and presented in Table 6.

IF (Hz)	10k	100k	1M	10M	100M	1G
Switches 1/f	29 %	11 %	2 %	3 %	1 %	< 1 %
Switches thermal	< 1 %	< 1 %	1 %	17 %	**47 %**	**48 %**
Load resistors	< 1 %	< 1 %	< 1 %	7 %	21 %	24 %
Input source resistance	< 1 %	< 1 %	< 1 %	7 %	19 %	18 %
Gm-bias 1/f	**41 %**	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %
AC-coupling resistors	5 %	19 %	21 %	14 %	< 1 %	< 1 %
Switches induced gate	18 %	**68 %**	**75 %**	**49 %**	2 %	< 1 %

Table 6: Dominant noise contributions for noise figure of BLIXER driven with bufferless VCO

This shows that at an IF of 10 kHz the noise figure is dominated by 1/f noise of the biasing of the GM-stage of the BLIXER. Since this noise wasn't a dominant noise contribution when de BLIXER was driven with an ideal sine wave oscillator, it can be concluded that this noise must have been up converted to phase noise in the VCO and

then as a result of the increased phase noise of the VCO at low offset frequencies, it is converted back to low intermediate frequencies in the BLIXER. Between an IF of 100 kHz and 1 MHz the noise figure is now dominated by the induced gate noise of the switching transistors. The absolute noise contribution of the AC-coupling resistors are more or less constant in this region and also more or less the same to the case when driving the BLIXER with the buffered VCO (as can be seen in Appendix E and F). The noise summaries show that the AC-coupling resistors and induced gate noise have the same noise-coloring as a result of the filtering of the AC-coupling. At an IF of 10 MHz still the induced gate noise of the switching transistors is dominant and can therefore be held responsible for the degrade noise figure of ~ 3 dB compared to the BLIXER driven with a buffered VCO. Between an IF of 100 MHz and 1 GHz the noise figure is dominated again by the thermal noise of the switching transistors.

To conclude this paragraph, the conversion gain and noise figure performance of the BLIXER is plotted for the entire RF-input frequency range of the satellite receiver of 10.7 GHz up to 12.75 GHz in Figure 61 when driven directly with a VCO without buffers in between. It can be seen that the conversion gain for the higher side band has a fall-of for a lower IF than the conversion gain for the lower side band. This can be explained as a result of a bandwidth limitation at one of the BLIXER RF-nodes. For example at the sources of the switching transistors more signal current coming from the Gm-stage of the BLIXER will be leaking through the capacitance seen at this node for large frequencies and therefore result in a lower conversion gain. It can be seen that the noise figure for the upper side band and the lower side band are equal to each other for IF-frequencies from 10 MHz up to 2 GHz.

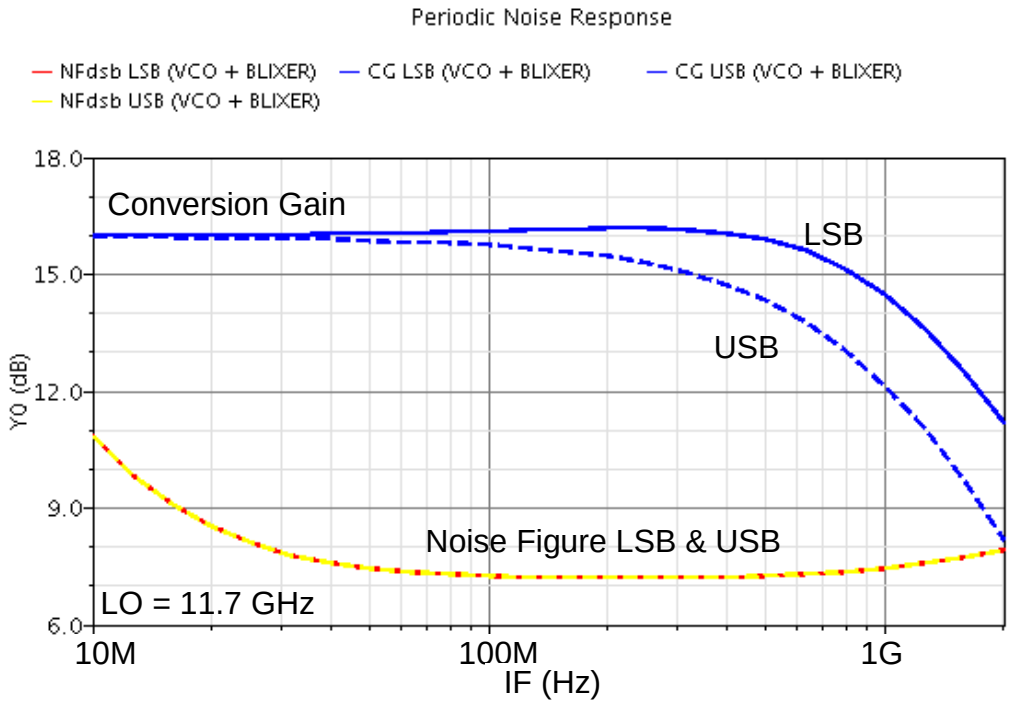

Figure 61: Conversion gain and noise figure of BLIXER driven with bufferless VCO for USB and LSB input frequencies

3.5 Conclusions

Given the Balun I/Q Mixer (BLIXER) [1] topology used as mixer, it is possible to drive this mixer with 11.7 GHz quadrature sine wave oscillator signals without buffers in between. There are however some drawbacks in decrease of performance:

- Increase in noise figure, especially at low intermediate frequencies as result of mixing with an oscillator with increased phase noise.
- Small increase in noise figure as a result of less steep transitions of switching transistors between the ‘opened’ and ‘closed’ state.
- Small decrease in conversion gain as a result of less steep transitions of switching transistors between the ‘opened’ and ‘closed’ state.

Driving one side of the BLIXER with an LC-oscillator and the other quadrature side of the mixer with an ideally RC-CR poly phase filter driven by the LC-oscillator appear to result in the following degradation in performance for an oscillation frequency of 11.7 GHz:

- Maximum increase in noise figure for IF=1 MHz of 15 dB
- For IF-frequencies between 100 MHz and 1 GHz only small increase of noise figure of less than 0.5 dB
- Decrease in conversion gain smaller than 0.5 dB for IF = 10 MHz up to 2 GHz.

Systematic simulations under various conditions indicate that the large increase in noise figure around an intermediate frequency of 1 MHz originates from the resistors of the AC-coupling between the BLIXER and the LC-oscillator. This maximum degradation of noise figure performance at this frequency is seen as a result of the corner frequency of the AC-filter.

4. Conclusions & recommendations

4.1 Conclusions

As summarized in section 2.6, the effects of capacitive loading of a VCO by a fixed capacitance and voltage dependent MOS-switch gate-capacitance have been examined. The main conclusions are:

- The *maximum* capacitance of loading a *parallel* LC-oscillator for a given fixed oscillation frequency and fixed inductor is limited by the total capacitance room in the LC-tank and the feasible tuning range for the tuneable tank capacitance
- The *minimum* capacitance of loading a *series* LC-oscillator for a given fixed oscillation frequency and fixed inductor with a fixed capacitance is limited by the total capacitance room in the LC-tank and the feasible tuning range for the tuneable tank capacitance

For the test conditions of a NMOS cross-couple pair with a parallel LC-tank loaded with the Balun I/Q Mixer the main conclusions from section 2.6 are:

- Large increase in phase noise of the VCO as a result of non-linear variation in gate-source capacitance of the switching transistors
- Increased phase noise is the result of induced gate noise of the switching transistors and the result of upconverted 1/f noise of within the mixer through the nonlinear varying capacitance of the switching transistors

As summarized in section 3.5, the BLIXER designed for UWB (500 MHz - 7GHz) [1] with adapted input match and reduced load capacitance to increase the IF-bandwidth from 400 MHz to 1GHz is directly driven with an parallel LC-oscillator without buffers in between. The main conclusions are:

- Driving with sine wave oscillator signals doesn’t degrade the performance that much (both conversion gain and noise figure only degrades slightly with 0.5 dB)
- Noise of the resistors of the AC-coupling of the VCO can give a heavily degraded noise figure performance at low intermediate frequencies around the corner frequency of the AC-coupling.

4.2 Recommendations

The induced gate noise of the switching transistors seem to be colored through the filtering of the AC-coupling and show up as a dominant noise contribution to the phase noise of the VCO at the corner frequency of the AC-coupling. This mechanism isn't quite well understood by the author and therefore recommended for further research.

The noise figure of the BLIXER is heavily degraded by the large noise contribution of the AC-coupling of the VCO, when driven with ideal buffering after the VCO with AC-coupling. However the AC-coupling doesn't degrade the phase noise performance of the VCO at the same offset-/intermediate frequency for the same test setup. Further research therefore will be recommended to study the interaction of this noise source between the phase noise of the VCO and the noise figure of the BLIXER.

Furthermore can be recommended to study the possibility of moving the ideal buffers in between the VCO and the AC-coupling to get rid of the large noise contribution of the AC-coupling to the VCO when loaded with the BLIXER. Eventually the possibility of using simple source followers as buffers could be an option to shield the noise interaction between VCO and BLIXER.

Apendices

Appendix A: Noise summaries buffered VCO loaded with 291 fF

1. Noise summary buffered VCO loaded with 291 fF at an offset of 1 kHz

Device	Param	Noise Contribution	% Of Total
XCP.MN2.m1	Sfl	2.53173e-05	48.60
XCP.MN1.m1	Sfl	2.52501e-05	48.47
/XCP/Rp	rn	7.40106e-07	1.42
XCP.MN2.m1	Sth	3.36294e-07	0.65
XCP.MN1.m1	Sth	3.36266e-07	0.65
XCP.MN1.m1	Sig	5.13383e-08	0.10
XCP.MN2.m1	Sig	5.10396e-08	0.10
/RACcouple2	rn	6.08163e-09	0.01
/RACcouple1	rn	6.08126e-09	0.01
/PORTout	rn	2.38893e-10	0.00
XCP.MN1.m1	Sigth	1.4984e-12	0.00
XCP.MN1.m1	Shotgd	1.70257e-13	0.00
XCP.MN2.m1	Shotgd	1.70257e-13	0.00
XCP.MN2.m1	Shotgs	1.4213e-13	0.00
XCP.MN1.m1	Shotgs	1.42119e-13	0.00
XCP.MN2.m1	Djnoise	8.22915e-17	0.00
XCP.MN1.m1	Djnoise	8.22888e-17	0.00
XCP.MN1.m1	Sjnoise	2.01509e-17	0.00
XCP.MN2.m1	Sjnoise	2.01509e-17	0.00
GM_0.MN0.m1	Sfl	2.36491e-30	0.00
GM_0.MNCS.m1	Sfl	1.22914e-31	0.00
GM_0.MP1.m1	Sfl	1.06946e-31	0.00
GM_0.MN3.m1	Sfl	2.12457e-32	0.00
GM_0.MN2.m1	Sfl	2.08862e-32	0.00
GM_0.MN4.m1	Sfl	1.92054e-32	0.00
GM_0.MN1.m1	Sfl	1.09632e-32	0.00
GM_0.MP2.m1	Sfl	7.43413e-33	0.00
GM_0.MNCG.m1	Sfl	6.62752e-33	0.00
MIXER_I.MNCGLOn.m1	Sfl	4.58377e-33	0.00
GM_0.MP0.m1	Sfl	3.17707e-33	0.00
GM_0.R0.r1	thermal	2.01162e-33	0.00
MIXER_I.MNCSLOp_1.m1	Sfl	1.43954e-33	0.00
MIXER_I.MNCSLOp_2.m1	Sfl	1.43954e-33	0.00
MIXER_I.MNCSLOp_3.m1	Sfl	1.43954e-33	0.00
MIXER_I.MNCSLOp_4.m1	Sfl	1.43954e-33	0.00
MIXER_I.MNCGLOp.m1	Sfl	1.36092e-33	0.00
GM_0.R3.r1	thermal	9.67896e-34	0.00
MIXER_I.MNCSLOn_2.m1	Sfl	8.92989e-34	0.00
MIXER_I.MNCSLOn_3.m1	Sfl	8.92989e-34	0.00
MIXER_I.MNCSLOn_4.m1	Sfl	8.92989e-34	0.00

Spot Noise Summary (in V^2/Hz) at 1K Hz Sorted By Noise Contributors
Total Summarized Noise = 5.20949e-05
No input referred noise available
The above noise summary info is for pnoise data

1/f noise XCP: 97 %

2. Noise summary buffered VCO loaded with 291 fF at an offset of 10 kHz

Device	Param	Noise Contribution	% Of Total
XCP.MN2.m1	Sfl	2.53186e-08	38.45
XCP.MN1.m1	Sfl	2.52514e-08	38.35
/XCP/Rp	rn	7.40092e-09	11.24
XCP.MN2.m1	Sth	3.36292e-09	5.11
XCP.MN1.m1	Sth	3.36263e-09	5.11
XCP.MN1.m1	Sig	5.1338e-10	0.78
XCP.MN2.m1	Sig	5.10393e-10	0.78
/RACcouple2	rn	6.08152e-11	0.09
/RACcouple1	rn	6.08115e-11	0.09
/PORTout	rn	2.38888e-12	0.00
XCP.MN1.m1	Sigth	1.49828e-14	0.00
XCP.MN1.m1	Shotgd	1.70252e-15	0.00
XCP.MN2.m1	Shotgd	1.70252e-15	0.00
XCP.MN2.m1	Shotgs	1.42125e-15	0.00
XCP.MN1.m1	Shotgs	1.42114e-15	0.00
XCP.MN2.m1	Djnoise	8.22899e-19	0.00
XCP.MN1.m1	Djnoise	8.22873e-19	0.00
XCP.MN1.m1	Sjnoise	2.01502e-19	0.00
XCP.MN2.m1	Sjnoise	2.01502e-19	0.00
GM_0.MN0.m1	Sfl	2.33727e-33	0.00
GM_0.MNCS.m1	Sfl	1.2788e-34	0.00
GM_0.MP1.m1	Sfl	1.07806e-34	0.00
GM_0.MN3.m1	Sfl	2.14095e-35	0.00
GM_0.MN2.m1	Sfl	2.07168e-35	0.00
GM_0.R0.r1	thermal	1.98956e-35	0.00
GM_0.MN4.m1	Sfl	1.91372e-35	0.00
GM_0.MP0.m1	Sfl	1.55862e-35	0.00
GM_0.MPCS.m1	Sfl	1.48764e-35	0.00
GM_0.MN1.m1	Sfl	1.08357e-35	0.00
GM_0.R3.r1	thermal	9.65987e-36	0.00
GM_0.MP2.m1	Sfl	7.37783e-36	0.00
GM_0.MNCG.m1	Sfl	7.21177e-36	0.00
MIXER_I.MNCGLOn.m1	Sfl	4.93195e-36	0.00
MIXER_I.MNCSLOp_1.m1	Sfl	1.56991e-36	0.00
MIXER_I.MNCSLOp_2.m1	Sfl	1.56991e-36	0.00
MIXER_I.MNCSLOp_3.m1	Sfl	1.56991e-36	0.00
MIXER_I.MNCSLOp_4.m1	Sfl	1.56991e-36	0.00
MIXER_I.MNCGLOp.m1	Sfl	1.45359e-36	0.00
GM_0.R1.r1	thermal	1.2429e-36	0.00
MIXER_I.MNCSLOn_4.m1	Sfl	9.666e-37	0.00

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Summarized Noise = 6.58443e-08
No input referred noise available
The above noise summary info is for pnoise data

1/f noise XCP: 77 %
thermal noise Rp: 11 %
thermal noise XCP: 10 %

3. Noise summary buffered VCO loaded with 291 fF at an offset of 100 kHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	7.39952e-11	36.39
XCP.MN2.m1	Sth	3.3627e-11	16.54
XCP.MN1.m1	Sth	3.36242e-11	16.54
XCP.MN2.m1	Sfl	2.53315e-11	12.46
XCP.MN1.m1	Sfl	2.52643e-11	12.43
XCP.MN1.m1	Sig	5.13349e-12	2.52
XCP.MN2.m1	Sig	5.10363e-12	2.51
/RACcouple2	rn	6.08041e-13	0.30
/RACcouple1	rn	6.08004e-13	0.30
/PORTout	rn	2.38843e-14	0.01
XCP.MN1.m1	Sigth	1.49711e-16	0.00
XCP.MN1.m1	Shotgd	1.70205e-17	0.00
XCP.MN2.m1	Shotgd	1.70205e-17	0.00
XCP.MN2.m1	Shotgs	1.42075e-17	0.00
XCP.MN1.m1	Shotgs	1.42064e-17	0.00
XCP.MN2.m1	Djnoise	8.22742e-21	0.00
XCP.MN1.m1	Djnoise	8.22716e-21	0.00
XCP.MN1.m1	Sjnoise	2.01437e-21	0.00
XCP.MN2.m1	Sjnoise	2.01437e-21	0.00
GM_0.MPCS.m1	Sfl	3.37779e-36	0.00
GM_0.MP0.m1	Sfl	3.02987e-36	0.00
GM_0.MN0.m1	Sfl	1.5931e-36	0.00
GM_0.MNCS.m1	Sfl	8.49802e-37	0.00
GM_0.MP1.m1	Sfl	2.06958e-37	0.00
GM_0.R0.r1	thermal	1.13016e-37	0.00
GM_0.MNCG.m1	Sfl	1.02228e-37	0.00
GM_0.R3.r1	thermal	7.85574e-38	0.00
MIXER_I.MNCGLOn.m1	Sfl	6.03778e-38	0.00
GM_0.MN3.m1	Sfl	4.01964e-38	0.00
GM_0.MP2.m1	Sfl	3.00288e-38	0.00
MIXER_I.MNCSLOp_1.m1	Sfl	2.28245e-38	0.00
MIXER_I.MNCSLOp_2.m1	Sfl	2.28245e-38	0.00
MIXER_I.MNCSLOp_3.m1	Sfl	2.28245e-38	0.00
MIXER_I.MNCSLOp_4.m1	Sfl	2.28245e-38	0.00
MIXER_I.MNCGLOp.m1	Sfl	1.59871e-38	0.00
GM_0.MN3.m1	Sth	1.57529e-38	0.00
GM_0.MN4.m1	Sfl	1.30378e-38	0.00
MIXER_I.MNCSLOn_2.m1	Sfl	1.28155e-38	0.00
MIXER_I.MNCSLOn_3.m1	Sfl	1.28155e-38	0.00
MIXER_I.MNCSLOn_4.m1	Sfl	1.28155e-38	0.00

Spot Noise Summary (in V^2/Hz) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 2.03319e-10
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 36 %

thermal noise XCP: 33 %

1/f noise XCP: 25 %

induced gate noise XCP: 5 %

4. <u>Noise summary buffered VCO loaded with 291 fF at an offset of 1 MHz</u>

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	7.38549e-13	46.86
XCP.MN2.m1	Sth	3.36055e-13	21.32
XCP.MN1.m1	Sth	3.36027e-13	21.32
XCP.MN1.m1	Sig	5.13044e-14	3.25
XCP.MN2.m1	Sig	5.10064e-14	3.24
XCP.MN2.m1	Sfl	2.54606e-14	1.62
XCP.MN1.m1	Sfl	2.53933e-14	1.61
/RACcouple2	rn	6.06935e-15	0.39
/RACcouple1	rn	6.06898e-15	0.39
/PORTout	rn	2.38398e-16	0.02
XCP.MN1.m1	Sigth	1.4854e-18	0.00
XCP.MN1.m1	Shotgd	1.69733e-19	0.00
XCP.MN2.m1	Shotgd	1.69733e-19	0.00
XCP.MN2.m1	Shotgs	1.41576e-19	0.00
XCP.MN1.m1	Shotgs	1.41565e-19	0.00
XCP.MN2.m1	Djnoise	8.21175e-23	0.00
XCP.MN1.m1	Djnoise	8.21149e-23	0.00
XCP.MN1.m1	Sjnoise	2.00785e-23	0.00
XCP.MN2.m1	Sjnoise	2.00785e-23	0.00
GM_0.MN0.m1	Sfl	1.6065e-35	0.00
GM_0.MPCS.m1	Sfl	1.55304e-35	0.00
GM_0.MP0.m1	Sfl	1.44641e-35	0.00
GM_0.R0.r1	thermal	1.06696e-35	0.00
GM_0.MNCS.m1	Sfl	1.87284e-36	0.00
GM_0.MN0.m1	Sth	6.34603e-37	0.00
GM_0.MNCG.m1	Sfl	3.01748e-37	0.00
GM_0.MPCS.m1	Sth	2.9506e-37	0.00
/PORTin	rn	2.54739e-37	0.00
GM_0.MP0.m1	Sth	2.29941e-37	0.00
GM_0.MP2.m1	Sfl	2.28137e-37	0.00
MIXER_I.MNCGLOn.m1	Sfl	1.70314e-37	0.00
GM_0.MNCS.m1	Sth	1.68242e-37	0.00
GM_0.MN2.m1	Sth	1.60128e-37	0.00
MIXER_I.RCSn.r1	thermal	1.40759e-37	0.00
GM_0.MP1.m1	Sfl	1.14908e-37	0.00
GM_0.MN3.m1	Sig	1.11892e-37	0.00
GM_0.MN2.m1	Sig	1.11754e-37	0.00
/R_BPF	rn	9.52525e-38	0.00
GM_0.MN3.m1	Sth	9.10457e-38	0.00
MIXER_I.MNCGLOn.m1	Sth	7.88192e-38	0.00

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.57617e-12
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 47 %

thermal noise XCP: 42 %

induced gate noise XCP: 6 %

1/f noise XCP: 3 %

5. Noise summary buffered VCO loaded with 291 fF at an offset of 10 MHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	7.24714e-15	47.94
XCP.MN2.m1	Sth	3.33946e-15	22.09
XCP.MN1.m1	Sth	3.33918e-15	22.09
XCP.MN1.m1	Sig	5.10076e-16	3.37
XCP.MN2.m1	Sig	5.07159e-16	3.35
/RACcouple2	rn	5.96032e-17	0.39
/RACcouple1	rn	5.95995e-17	0.39
XCP.MN2.m1	Sfl	2.67496e-17	0.18
XCP.MN1.m1	Sfl	2.66807e-17	0.18
/PORTout	rn	2.33999e-18	0.02
XCP.MN1.m1	Sigth	1.36693e-20	0.00
XCP.MN2.m1	Shotgd	1.65082e-21	0.00
XCP.MN1.m1	Shotgd	1.65082e-21	0.00
XCP.MN2.m1	Shotgs	1.36642e-21	0.00
XCP.MN1.m1	Shotgs	1.3663e-21	0.00
XCP.MN2.m1	Djnoise	8.05728e-25	0.00
XCP.MN1.m1	Djnoise	8.05702e-25	0.00
XCP.MN1.m1	Sjnoise	1.94326e-25	0.00
XCP.MN2.m1	Sjnoise	1.94326e-25	0.00
GM_0.R0.r1	thermal	4.00415e-35	0.00
GM_0.MN0.m1	Sfl	6.58181e-36	0.00
GM_0.MN0.m1	Sth	2.6002e-36	0.00
GM_0.MN2.m1	Sth	1.07276e-36	0.00
GM_0.MN3.m1	Sth	9.33144e-37	0.00
GM_0.R3.r1	thermal	5.38934e-37	0.00
GM_0.MPCS.m1	Sfl	3.22782e-37	0.00
GM_0.MP0.m1	Sfl	2.87616e-37	0.00
GM_0.MP1.m1	Sth	2.41872e-37	0.00
GM_0.MP2.m1	Sig	8.13762e-38	0.00
GM_0.MP1.m1	Sfl	7.47041e-38	0.00
GM_0.R1.r1	thermal	6.59864e-38	0.00
GM_0.MPCS.m1	Sth	5.68221e-38	0.00
GM_0.MP0.m1	Sth	4.77039e-38	0.00
GM_0.MNCS.m1	Sig	4.12337e-38	0.00
GM_0.MN1.m1	Sfl	2.95629e-38	0.00
GM_0.MN1.m1	Sth	2.79203e-38	0.00
GM_0.MN2.m1	Sfl	2.73353e-38	0.00
GM_0.MP2.m1	Sth	2.6084e-38	0.00
GM_0.MN3.m1	Sfl	2.41365e-38	0.00
/R_BPF	rn	1.74034e-38	0.00

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.5118e-14
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 48 %

thermal noise XCP: 44 %

induced gate noise XCP: 7 %

6. Noise summary buffered VCO loaded with 291 fF at an offset of 100 MHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	6.1292e-17	45.11
XCP.MN2.m1	Sth	3.18436e-17	23.44
XCP.MN1.m1	Sth	3.18416e-17	23.43
XCP.MN1.m1	Sig	4.90355e-18	3.61
XCP.MN2.m1	Sig	4.88077e-18	3.59
/RACcouple2	rn	5.08677e-19	0.37
/RACcouple1	rn	5.08639e-19	0.37
XCP.MN2.m1	Sfl	3.92899e-20	0.03
XCP.MN1.m1	Sfl	3.92039e-20	0.03
/PORTout	rn	1.98537e-20	0.01
XCP.MN2.m1	Shotgd	1.2822e-23	0.00
XCP.MN1.m1	Shotgd	1.28215e-23	0.00
XCP.MN1.m1	Sigth	1.23197e-23	0.00
XCP.MN2.m1	Shotgs	9.57686e-24	0.00
XCP.MN1.m1	Shotgs	9.57544e-24	0.00
XCP.MN2.m1	Djnoise	6.81679e-27	0.00
XCP.MN1.m1	Djnoise	6.8165e-27	0.00
XCP.MN1.m1	Sjnoise	1.39696e-27	0.00
XCP.MN2.m1	Sjnoise	1.39696e-27	0.00
GM_0.MN2.m1	Sth	1.65562e-35	0.00
GM_0.R0.r1	thermal	9.27872e-36	0.00
GM_0.MN3.m1	Sth	6.10125e-36	0.00
GM_0.MP0.m1	Sth	3.82606e-36	0.00
GM_0.MP0.m1	Sfl	2.35945e-36	0.00
GM_0.MN0.m1	Sth	1.78718e-36	0.00
GM_0.MPCS.m1	Sth	1.18976e-36	0.00
GM_0.R3.r1	thermal	9.20433e-37	0.00
GM_0.MN3.m1	Sig	8.28399e-37	0.00
GM_0.MN2.m1	Sig	8.2762e-37	0.00
GM_0.MP1.m1	Sth	7.83999e-37	0.00
GM_0.MPCS.m1	Sfl	6.6125e-37	0.00
GM_0.MN0.m1	Sfl	4.51197e-37	0.00
GM_0.MP2.m1	Sth	4.26471e-37	0.00
GM_0.MP2.m1	Sig	4.23773e-37	0.00
GM_0.MNCS.m1	Sth	4.02544e-37	0.00
/PORTin	rn	3.25277e-37	0.00
GM_0.MNCG.m1	Sth	2.53902e-37	0.00
/R_BPF	rn	1.52278e-37	0.00
MIXER_Q.RCSp.r1	thermal	1.44432e-37	0.00
MIXER_I.RCSp.r1	thermal	1.2629e-37	0.00

Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.35877e-16
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 45 %

thermal noise XCP: 47 %

induced gate noise XCP: 7 %

7. Noise summary buffered VCO loaded with 291 fF at an offset of 1 GHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	8.87317e-19	47.14
XCP.MN1.m1	Sth	4.2171e-19	22.41
XCP.MN2.m1	Sth	4.21691e-19	22.40
XCP.MN1.m1	Sig	6.78088e-20	3.60
XCP.MN2.m1	Sig	6.76578e-20	3.59
/RACcouple2	rn	7.67975e-21	0.41
/RACcouple1	rn	7.67941e-21	0.41
/PORTout	rn	2.9856e-22	0.02
XCP.MN2.m1	Sfl	1.4898e-22	0.01
XCP.MN1.m1	Sfl	1.48784e-22	0.01
XCP.MN2.m1	Sigth	1.64381e-24	0.00
XCP.MN1.m1	Shotgd	2.27469e-25	0.00
XCP.MN2.m1	Shotgd	2.27436e-25	0.00
XCP.MN1.m1	Shotgs	1.67443e-25	0.00
XCP.MN2.m1	Shotgs	1.67417e-25	0.00
XCP.MN2.m1	Djnoise	1.00204e-28	0.00
XCP.MN1.m1	Djnoise	1.00197e-28	0.00
XCP.MN1.m1	Sjnoise	2.21869e-29	0.00
XCP.MN2.m1	Sjnoise	2.21869e-29	0.00
GM_0.MN3.m1	Sth	7.46761e-36	0.00
GM_0.MP1.m1	Sth	2.71812e-36	0.00
GM_0.MN2.m1	Sig	2.34054e-36	0.00
GM_0.MN3.m1	Sig	2.33805e-36	0.00
GM_0.MP0.m1	Sth	1.80547e-36	0.00
GM_0.MN2.m1	Sth	1.0847e-36	0.00
GM_0.R0.r1	thermal	3.04281e-37	0.00
GM_0.MNCG.m1	Sth	2.90975e-37	0.00
MIXER_Q.RCGn.r1	thermal	2.57489e-37	0.00
MIXER_Q.RCGp.r1	thermal	2.47156e-37	0.00
GM_0.MPCS.m1	Sth	2.14309e-37	0.00
GM_0.MNCS.m1	Sth	1.91447e-37	0.00
GM_0.MP2.m1	Sig	1.84976e-37	0.00
GM_0.MP0.m1	Sfl	1.128e-37	0.00
MIXER_Q.RCSp.r1	thermal	1.03591e-37	0.00
MIXER_Q.MNCGLOp.m1	Sth	1.02435e-37	0.00
MIXER_I.MNCGLOp.m1	Sth	5.17081e-38	0.00
MIXER_I.MNCGLOn.m1	Sth	4.87731e-38	0.00
/PORTin	rn	4.39586e-38	0.00
GM_0.R3.r1	thermal	3.28965e-38	0.00
MIXER_Q.MNCSLOp_4.m1	Sth	3.21493e-38	0.00

Spot Noise Summary (in V^2/Hz) at 1G Hz Sorted By Noise Contributors
Total Summarized Noise = 1.88214e-18
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 47 %

thermal noise XCP: 45 %

induced gate noise XCP: 7 %

8. Noise summary buffered VCO loaded with 291 fF at an offset of 10 GHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	1.7961e-20	37.44
XCP.MN2.m1	Sth	1.27738e-20	26.63
XCP.MN1.m1	Sth	1.27719e-20	26.62
XCP.MN1.m1	Sig	2.04347e-21	4.26
XCP.MN2.m1	Sig	2.03822e-21	4.25
/RACcouple2	rn	1.83521e-22	0.38
/RACcouple1	rn	1.83511e-22	0.38
/PORTout	rn	6.88882e-24	0.01
XCP.MN2.m1	Sfl	3.65886e-24	0.01
XCP.MN1.m1	Sfl	3.65478e-24	0.01
XCP.MN1.m1	Sigth	1.12132e-25	0.00
XCP.MN2.m1	Shotgd	4.96769e-27	0.00
XCP.MN1.m1	Shotgd	4.96736e-27	0.00
XCP.MN2.m1	Shotgs	3.41548e-27	0.00
XCP.MN1.m1	Shotgs	3.41485e-27	0.00
XCP.MN2.m1	Djnoise	2.16068e-30	0.00
XCP.MN1.m1	Djnoise	2.16061e-30	0.00
XCP.MN1.m1	Sjnoise	6.61012e-31	0.00
XCP.MN2.m1	Sjnoise	6.61012e-31	0.00

Spot Noise Summary (in V^2/Hz) at 10G Hz Sorted By Noise Contributors
Total Summarized Noise = 4.79696e-20
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 37 %

thermal noise XCP: 53 %

induced gate noise XCP: 9 %

Appendix B: Noise summaries VCO loaded with BLIXER

1. Noise summary VCO loaded with BLIXER at an offset of 1 kHz

Device	Param	Noise Contribution	% Of Total
GM_0.MN0.m1	Sfl	0.0383046	87.76
GM_0.MNCS.m1	Sfl	0.0017914	4.10
GM_0.MP1.m1	Sfl	0.00122948	2.82
GM_0.MN4.m1	Sfl	0.000923654	2.12
GM_0.MNCG.m1	Sfl	0.000268246	0.61
GM_0.MN2.m1	Sfl	0.000261375	0.60
GM_0.MN3.m1	Sfl	0.000248435	0.57
GM_0.MP0.m1	Sfl	0.000177447	0.41
GM_0.MN1.m1	Sfl	0.000176136	0.40
GM_0.MP2.m1	Sfl	6.7938e-05	0.16
GM_0.R0.r1	thermal	3.00592e-05	0.07
XCP.MN2.m1	Sfl	1.39191e-05	0.03
XCP.MN1.m1	Sfl	1.39126e-05	0.03
MIXER_I.MN0.m1	Sig	1.21942e-05	0.03
MIXER_Q.MN0.m1	Sig	1.21942e-05	0.03
GM_0.MPCS.m1	Sfl	1.19169e-05	0.03
GM_0.R3.r1	thermal	8.75023e-06	0.02
GM_0.R1.r1	thermal	5.47023e-06	0.01
/RACcouple2	rn	4.44665e-06	0.01
/RACcouple1	rn	4.43841e-06	0.01
MIXER_I.MNCSLOn_1.m1	Sig	3.72413e-06	0.01
MIXER_I.MNCSLOn_2.m1	Sig	3.72413e-06	0.01
MIXER_I.MNCSLOn_3.m1	Sig	3.72413e-06	0.01
MIXER_I.MNCSLOn_4.m1	Sig	3.72413e-06	0.01
MIXER_I.MNCSLOp_1.m1	Sig	3.71608e-06	0.01
MIXER_I.MNCSLOp_2.m1	Sig	3.71608e-06	0.01
MIXER_I.MNCSLOp_3.m1	Sig	3.71608e-06	0.01
MIXER_I.MNCSLOp_4.m1	Sig	3.71608e-06	0.01
MIXER_Q.MNCSLOp_1.m1	Sfl	3.63567e-06	0.01
MIXER_Q.MNCSLOp_2.m1	Sfl	3.63567e-06	0.01
MIXER_Q.MNCSLOp_3.m1	Sfl	3.63567e-06	0.01
MIXER_Q.MNCSLOp_4.m1	Sfl	3.63567e-06	0.01
MIXER_Q.MNCSLOn_1.m1	Sfl	3.63376e-06	0.01
MIXER_Q.MNCSLOn_2.m1	Sfl	3.63376e-06	0.01
MIXER_Q.MNCSLOn_3.m1	Sfl	3.63376e-06	0.01
MIXER_Q.MNCSLOn_4.m1	Sfl	3.63376e-06	0.01
MIXER_Q.MNCGLOn.m1	Sfl	2.20453e-06	0.01
MIXER_Q.MNCGLOp.m1	Sfl	2.2025e-06	0.01
GM_0.MN0.m1	Sth	1.51304e-06	0.00
GM_0.MP2.m1	Sig	1.40906e-06	0.00

Spot Noise Summary (in V^2/Hz) at 1K Hz Sorted By Noise Contributors
Total Summarized Noise = 0.0436488
No input referred noise available
The above noise summary info is for pnoise data

1/f noise biasing
Gm-stage: 95 %

2. Noise summary VCO loaded with BLIXER at an offset of 10 kHz

Device	Param	Noise Contribution	% Of Total
GM_0.MN0.m1	Sfl	3.82341e-05	85.93
GM_0.MNCS.m1	Sfl	1.78818e-06	4.02
GM_0.MP1.m1	Sfl	1.22705e-06	2.76
GM_0.MN4.m1	Sfl	9.31414e-07	2.09
GM_0.R0.r1	thermal	3.0004e-07	0.67
GM_0.MNCG.m1	Sfl	2.70245e-07	0.61
GM_0.MN2.m1	Sfl	2.60859e-07	0.59
GM_0.MN3.m1	Sfl	2.47944e-07	0.56
GM_0.MP0.m1	Sfl	1.771e-07	0.40
GM_0.MN1.m1	Sfl	1.75812e-07	0.40
GM_0.R3.r1	thermal	8.73297e-08	0.20
GM_0.MP2.m1	Sfl	6.78143e-08	0.15
GM_0.R1.r1	thermal	5.51617e-08	0.12
MIXER_I.MN0.m1	Sig	5.22987e-08	0.12
MIXER_Q.MN0.m1	Sig	5.22987e-08	0.12
/RACcouple2	rn	4.44272e-08	0.10
/RACcouple1	rn	4.43449e-08	0.10
MIXER_I.MNCSL0n_1.m1	Sig	3.72062e-08	0.08
MIXER_I.MNCSL0n_2.m1	Sig	3.72062e-08	0.08
MIXER_I.MNCSL0n_3.m1	Sig	3.72062e-08	0.08
MIXER_I.MNCSL0n_4.m1	Sig	3.72062e-08	0.08
MIXER_I.MNCSL0p_1.m1	Sig	3.71258e-08	0.08
MIXER_I.MNCSL0p_2.m1	Sig	3.71258e-08	0.08
MIXER_I.MNCSL0p_3.m1	Sig	3.71258e-08	0.08
MIXER_I.MNCSL0p_4.m1	Sig	3.71258e-08	0.08
GM_0.MN0.m1	Sth	1.51026e-08	0.03
GM_0.MP2.m1	Sig	1.40627e-08	0.03
XCP.MN2.m1	Sfl	1.39436e-08	0.03
XCP.MN1.m1	Sfl	1.39371e-08	0.03
MIXER_I.MNCGL0n.m1	Sig	1.21829e-08	0.03
MIXER_I.MNCGL0p.m1	Sig	1.19644e-08	0.03
GM_0.MPCS.m1	Sfl	1.18979e-08	0.03
GM_0.MN2.m1	Sth	1.01948e-08	0.02
GM_0.MN3.m1	Sth	9.58372e-09	0.02
/XCP/Rp	rn	6.3631e-09	0.01
XCP.MN2.m1	Sth	3.98717e-09	0.01
XCP.MN1.m1	Sth	3.98635e-09	0.01
GM_0.MP1.m1	Sth	3.94969e-09	0.01
MIXER_Q.MNCSL0p_3.m1	Sfl	3.63862e-09	0.01
MIXER_Q.MNCSL0p_4.m1	Sfl	3.63862e-09	0.01

1/f noise biasing
Gm-stage: 93 %

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Summarized Noise = 4.44937e-05
No input referred noise available
The above noise summary info is for pnoise data

3. Noise summary VCO loaded with BLIXER at an offset of 100 kHz

Device	Param	Noise Contribution	% Of Total
GM_0.MN0.m1	Sfl	3.8169e-08	72.51
GM_0.R0.r1	thermal	2.99529e-09	5.69
GM_0.MNCS.m1	Sfl	1.78522e-09	3.39
GM_0.MP1.m1	Sfl	1.2246e-09	2.33
GM_0.MN4.m1	Sfl	9.36305e-10	1.78
GM_0.R3.r1	thermal	8.71562e-10	1.66
GM_0.R1.r1	thermal	5.54512e-10	1.05
/RACcouple2	rn	4.4267e-10	0.84
/RACcouple1	rn	4.4185e-10	0.84
MIXER_I.MNCSLOn_1.m1	Sig	3.70699e-10	0.70
MIXER_I.MNCSLOn_2.m1	Sig	3.70699e-10	0.70
MIXER_I.MNCSLOn_3.m1	Sig	3.70699e-10	0.70
MIXER_I.MNCSLOn_4.m1	Sig	3.70699e-10	0.70
MIXER_I.MNCSLOp_1.m1	Sig	3.69899e-10	0.70
MIXER_I.MNCSLOp_2.m1	Sig	3.69899e-10	0.70
MIXER_I.MNCSLOp_3.m1	Sig	3.69899e-10	0.70
MIXER_I.MNCSLOp_4.m1	Sig	3.69899e-10	0.70
GM_0.MNCG.m1	Sfl	2.71584e-10	0.52
GM_0.MN2.m1	Sfl	2.6034e-10	0.49
GM_0.MN3.m1	Sfl	2.47451e-10	0.47
GM_0.MP0.m1	Sfl	1.76751e-10	0.34
GM_0.MN1.m1	Sfl	1.75513e-10	0.33
GM_0.MN0.m1	Sth	1.50768e-10	0.29
GM_0.MP2.m1	Sig	1.40346e-10	0.27
MIXER_I.MNCGLOn.m1	Sig	1.21392e-10	0.23
MIXER_I.MNCGLOp.m1	Sig	1.19216e-10	0.23
GM_0.MN2.m1	Sth	1.01745e-10	0.19
GM_0.MN3.m1	Sth	9.56465e-11	0.18
GM_0.MP2.m1	Sfl	6.76985e-11	0.13
/XCP/Rp	rn	6.35793e-11	0.12
XCP.MN2.m1	Sth	3.98591e-11	0.08
XCP.MN1.m1	Sth	3.98509e-11	0.08
GM_0.MP1.m1	Sth	3.94182e-11	0.07
XCP.MN2.m1	Sfl	1.39773e-11	0.03
XCP.MN1.m1	Sfl	1.39708e-11	0.03
GM_0.MPCS.m1	Sfl	1.18881e-11	0.02
MIXER_I.MN0.m1	Sig	9.26248e-12	0.02
MIXER_Q.MN0.m1	Sig	9.26248e-12	0.02
GM_0.MN4.m1	Sth	8.27738e-12	0.02
GM_0.MNCS.m1	Sth	5.28007e-12	0.01

Spot Noise Summary (in V^2/Hz) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 5.26422e-08
No input referred noise available
The above noise summary info is for pnoise data

1/f noise biasing Gm-stage: 77 %

induced gate noise switching MOSts: 6 %

4. Noise summary VCO loaded with BLIXER at an offset of 1 MHz

Device	Param	Noise Contribution	% Of Total
GM_0.MN0.m1	Sfl	3.64294e-11	30.06
GM_0.R0.r1	thermal	2.85891e-11	23.59
GM_0.R3.r1	thermal	8.15794e-12	6.73
GM_0.R1.r1	thermal	5.17385e-12	4.27
/RACcouple2	rn	3.36032e-12	2.77
/RACcouple1	rn	3.35419e-12	2.77
MIXER_I.MNCSLOn_1.m1	Sig	2.81478e-12	2.32
MIXER_I.MNCSLOn_2.m1	Sig	2.81478e-12	2.32
MIXER_I.MNCSLOn_3.m1	Sig	2.81478e-12	2.32
MIXER_I.MNCSLOn_4.m1	Sig	2.81478e-12	2.32
MIXER_I.MNCSLOp_1.m1	Sig	2.80879e-12	2.32
MIXER_I.MNCSLOp_2.m1	Sig	2.80879e-12	2.32
MIXER_I.MNCSLOp_3.m1	Sig	2.80879e-12	2.32
MIXER_I.MNCSLOp_4.m1	Sig	2.80879e-12	2.32
GM_0.MNCS.m1	Sfl	1.70715e-12	1.41
GM_0.MN0.m1	Sth	1.43897e-12	1.19
GM_0.MP2.m1	Sig	1.31349e-12	1.08
GM_0.MP1.m1	Sfl	1.14619e-12	0.95
GM_0.MN2.m1	Sth	9.52323e-13	0.79
MIXER_I.MNCGLOn.m1	Sig	9.22061e-13	0.76
MIXER_I.MNCGLOp.m1	Sig	9.05556e-13	0.75
GM_0.MN3.m1	Sth	8.95219e-13	0.74
GM_0.MN4.m1	Sfl	8.73606e-13	0.72
/XCP/Rp	rn	6.35318e-13	0.52
XCP.MN2.m1	Sth	3.98597e-13	0.33
XCP.MN1.m1	Sth	3.98516e-13	0.33
GM_0.MP1.m1	Sth	3.68941e-13	0.30
GM_0.MNCG.m1	Sfl	2.62872e-13	0.22
GM_0.MN2.m1	Sfl	2.43676e-13	0.20
GM_0.MN3.m1	Sfl	2.31605e-13	0.19
GM_0.MN1.m1	Sfl	1.67514e-13	0.14
GM_0.MP0.m1	Sfl	1.65544e-13	0.14
GM_0.MN4.m1	Sth	7.72309e-14	0.06
GM_0.MP2.m1	Sfl	6.45076e-14	0.05
GM_0.MNCS.m1	Sth	5.06286e-14	0.04
XCP.MN2.m1	Sig	4.88947e-14	0.04
XCP.MN1.m1	Sig	4.84933e-14	0.04
GM_0.MNCS.m1	Sig	3.99112e-14	0.03
GM_0.MNCG.m1	Sth	2.46875e-14	0.02
GM_0.MP2.m1	Sth	2.07067e-14	0.02

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.21184e-10
No input referred noise available
The above noise summary info is for pnoise data

1/f noise biasing Gm-stage: 30 %

thermal noise biasing Gm-stage: 35 %

AC-coupling resistors: 6 %

induced gate noise switching MOSts: 19 %

5. Noise summary VCO loaded with BLIXER at an offset of 10 MHz

Device	Param	Noise Contribution	% Of Total
GM_0.R0.r1	thermal	2.21802e-13	64.87
GM_0.MN0.m1	Sfl	2.82525e-14	8.26
GM_0.R3.r1	thermal	2.52221e-14	7.38
GM_0.MN0.m1	Sth	1.11598e-14	3.26
GM_0.R1.r1	thermal	1.0741e-14	3.14
/XCP/Rp	rn	6.30781e-15	1.84
GM_0.MP2.m1	Sig	4.06432e-15	1.19
XCP.MN2.m1	Sth	3.98441e-15	1.17
XCP.MN1.m1	Sth	3.98362e-15	1.17
GM_0.MN2.m1	Sth	2.94476e-15	0.86
GM_0.MN3.m1	Sth	2.76814e-15	0.81
GM_0.MNCS.m1	Sfl	1.45448e-15	0.43
/RACcouple2	rn	1.41324e-15	0.41
/RACcouple1	rn	1.41105e-15	0.41
MIXER_I.MNCSLOn_1.m1	Sig	1.23156e-15	0.36
MIXER_I.MNCSLOn_2.m1	Sig	1.23156e-15	0.36
MIXER_I.MNCSLOn_3.m1	Sig	1.23156e-15	0.36
MIXER_I.MNCSLOn_4.m1	Sig	1.23156e-15	0.36
MIXER_I.MNCSLOp_1.m1	Sig	1.22941e-15	0.36
MIXER_I.MNCSLOp_2.m1	Sig	1.22941e-15	0.36
MIXER_I.MNCSLOp_3.m1	Sig	1.22941e-15	0.36
MIXER_I.MNCSLOp_4.m1	Sig	1.22941e-15	0.36
GM_0.MP1.m1	Sth	1.14074e-15	0.33
XCP.MN2.m1	Sig	4.87937e-16	0.14
XCP.MN1.m1	Sig	4.83866e-16	0.14
GM_0.MNCS.m1	Sth	4.36201e-16	0.13
MIXER_I.MNCGLOn.m1	Sig	4.12851e-16	0.12
MIXER_I.MNCGLOp.m1	Sig	4.05825e-16	0.12
GM_0.MP1.m1	Sfl	3.54394e-16	0.10
GM_0.MNCS.m1	Sig	3.09617e-16	0.09
GM_0.MNCG.m1	Sfl	2.33644e-16	0.07
GM_0.MNCG.m1	Sth	2.20023e-16	0.06
GM_0.MN4.m1	Sfl	1.8135e-16	0.05
GM_0.MN4.m1	Sth	1.60322e-16	0.05
GM_0.MP2.m1	Sth	1.5761e-16	0.05
GM_0.MN1.m1	Sfl	1.29916e-16	0.04
GM_0.MN1.m1	Sth	1.22682e-16	0.04
MIXER_I.RCSp.r1	thermal	9.97031e-17	0.03
MIXER_I.RCSn.r1	thermal	9.96989e-17	0.03
GM_0.MN2.m1	Sfl	7.53492e-17	0.02

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 3.4192e-13
No input referred noise available
The above noise summary info is for pnoise data

1/f noise biasing Gm-stage: 8 %

thermal noise biasing Gm-stage: 79 %

thermal noise Rp: 2 %

thermal noise XCP: 2 %

AC-coupling resistors: 1 %

induced gate noise switching MOSts: 3 %

6. Noise summary VCO loaded with BLIXER at an offset of 100 MHz

Device	Param	Noise Contribution	% Of Total
GM_0.R0.r1	thermal	2.64926e-16	56.85
/XCP/Rp	rn	5.7824e-17	12.41
XCP.MN2.m1	Sth	3.97147e-17	8.52
XCP.MN1.m1	Sth	3.97092e-17	8.52
GM_0.MN0.m1	Sth	1.30496e-17	2.80
GM_0.MNCS.m1	Sth	4.97582e-18	1.07
XCP.MN2.m1	Sig	4.74629e-18	1.02
XCP.MN1.m1	Sig	4.69771e-18	1.01
GM_0.R3.r1	thermal	4.30564e-18	0.92
GM_0.MN0.m1	Sfl	3.30369e-18	0.71
GM_0.MNCG.m1	Sth	2.1163e-18	0.45
GM_0.MNCS.m1	Sfl	1.65833e-18	0.36
GM_0.MP2.m1	Sth	1.58179e-18	0.34
GM_0.R1.r1	thermal	1.31005e-18	0.28
MIXER_I.MNCSLOp_1.m1	Sig	1.0276e-18	0.22
MIXER_I.MNCSLOp_2.m1	Sig	1.0276e-18	0.22
MIXER_I.MNCSLOp_3.m1	Sig	1.0276e-18	0.22
MIXER_I.MNCSLOp_4.m1	Sig	1.0276e-18	0.22
MIXER_I.MNCSLOn_1.m1	Sig	1.02675e-18	0.22
MIXER_I.MNCSLOn_2.m1	Sig	1.02675e-18	0.22
MIXER_I.MNCSLOn_3.m1	Sig	1.02675e-18	0.22
MIXER_I.MNCSLOn_4.m1	Sig	1.02675e-18	0.22
MIXER_I.RCSn.r1	thermal	8.79575e-19	0.19
MIXER_I.RCSp.r1	thermal	8.79552e-19	0.19
GM_0.MP2.m1	Sig	7.98794e-19	0.17
/RACcouple1	rn	6.42389e-19	0.14
/RACcouple2	rn	6.419e-19	0.14
GM_0.MN2.m1	Sth	5.11833e-19	0.11
GM_0.MN3.m1	Sth	4.82044e-19	0.10
GM_0.MPCS.m1	Sth	4.72603e-19	0.10
MIXER_I.MNCGLOn.m1	Sig	4.36982e-19	0.09
MIXER_I.MNCGLOp.m1	Sig	4.32338e-19	0.09
GM_0.MNCS.m1	Sig	3.73403e-19	0.08
MIXER_Q.MNCSLOp_1.m1	Sth	3.16696e-19	0.07
MIXER_Q.MNCSLOp_2.m1	Sth	3.16696e-19	0.07
MIXER_Q.MNCSLOp_3.m1	Sth	3.16696e-19	0.07
MIXER_Q.MNCSLOp_4.m1	Sth	3.16696e-19	0.07
MIXER_Q.MNCSLOn_2.m1	Sth	3.16641e-19	0.07
MIXER_Q.MNCSLOn_3.m1	Sth	3.16641e-19	0.07
MIXER_Q.MNCSLOn_4.m1	Sth	3.16641e-19	0.07

Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 4.65992e-16
No input referred noise available
The above noise summary info is for pnoise data

thermal noise biasing Gm-stage: 57 %

thermal noise Rp: 12 %

thermal noise XCP: 17 %

induced gate noise switching MOSts: 2 %

7. Noise summary VCO loaded with BLIXER at an offset of 1 GHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	8.82581e-19	34.58
XCP.MN1.m1	Sth	5.31175e-19	20.81
XCP.MN2.m1	Sth	5.31167e-19	20.81
GM_0.MNCS.m1	Sth	9.36195e-20	3.67
XCP.MN2.m1	Sig	6.35767e-20	2.49
XCP.MN1.m1	Sig	6.28456e-20	2.46
GM_0.R0.r1	thermal	5.97812e-20	2.34
GM_0.MPCS.m1	Sth	4.56396e-20	1.79
GM_0.MNCG.m1	Sth	1.98446e-20	0.78
MIXER_I.RCSn.r1	thermal	1.26148e-20	0.49
MIXER_I.RCSp.r1	thermal	1.26139e-20	0.49
MIXER_I.MNCSLOn_1.m1	Sig	1.16971e-20	0.46
MIXER_I.MNCSLOn_2.m1	Sig	1.16971e-20	0.46
MIXER_I.MNCSLOn_3.m1	Sig	1.16971e-20	0.46
MIXER_I.MNCSLOn_4.m1	Sig	1.16971e-20	0.46
MIXER_I.MNCSLOp_1.m1	Sig	1.16926e-20	0.46
MIXER_I.MNCSLOp_2.m1	Sig	1.16926e-20	0.46
MIXER_I.MNCSLOp_3.m1	Sig	1.16926e-20	0.46
MIXER_I.MNCSLOp_4.m1	Sig	1.16926e-20	0.46
/R_BPF	rn	1.03204e-20	0.40
/RACcouple2	rn	7.41511e-21	0.29
/RACcouple1	rn	7.40219e-21	0.29
/PORTin	rn	6.361e-21	0.25
MIXER_Q.MNCSLOn_1.m1	Sth	5.81932e-21	0.23
MIXER_Q.MNCSLOn_2.m1	Sth	5.81932e-21	0.23
MIXER_Q.MNCSLOn_3.m1	Sth	5.81932e-21	0.23
MIXER_Q.MNCSLOn_4.m1	Sth	5.81932e-21	0.23
MIXER_Q.MNCSLOp_1.m1	Sth	5.81929e-21	0.23
MIXER_Q.MNCSLOp_2.m1	Sth	5.81929e-21	0.23
MIXER_Q.MNCSLOp_3.m1	Sth	5.81929e-21	0.23
MIXER_Q.MNCSLOp_4.m1	Sth	5.81929e-21	0.23
MIXER_I.MNCGLOn.m1	Sig	5.03074e-21	0.20
MIXER_I.MNCGLOp.m1	Sig	4.98373e-21	0.20
GM_0.MP2.m1	Sth	4.35762e-21	0.17
MIXER_I.MNCSLOp_1.m1	Sth	3.36494e-21	0.13
MIXER_I.MNCSLOp_2.m1	Sth	3.36494e-21	0.13
MIXER_I.MNCSLOp_3.m1	Sth	3.36494e-21	0.13
MIXER_I.MNCSLOp_4.m1	Sth	3.36494e-21	0.13
MIXER_I.MNCSLOn_3.m1	Sth	3.36278e-21	0.13
MIXER_I.MNCSLOn_4.m1	Sth	3.36278e-21	0.13

Spot Noise Summary (in V^2/Hz) at 1G Hz Sorted By Noise Contributors
Total Summarized Noise = 2.55218e-18
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 35 %

thermal noise XCP: 41 %

induced gate noise XCP: 5 %

induced gate noise switching MOSts: 4 %

8. Noise summary VCO loaded with BLIXER at an offset of 10 GHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	1.65462e-20	27.86
XCP.MN1.m1	Sth	1.35741e-20	22.86
XCP.MN2.m1	Sth	1.35732e-20	22.86
XCP.MN2.m1	Sig	2.01228e-21	3.39
XCP.MN1.m1	Sig	2.00438e-21	3.38
GM_0.MNCS.m1	Sth	1.58898e-21	2.68
GM_0.MNCG.m1	Sth	1.1786e-21	1.98
/PORTin	rn	9.27119e-22	1.56
GM_0.MPCS.m1	Sth	8.90868e-22	1.50
MIXER_I.MNCSLOp_1.m1	Sig	4.94919e-22	0.83
MIXER_I.MNCSLOp_2.m1	Sig	4.94919e-22	0.83
MIXER_I.MNCSLOp_3.m1	Sig	4.94919e-22	0.83
MIXER_I.MNCSLOp_4.m1	Sig	4.94919e-22	0.83
MIXER_I.MNCSLOn_1.m1	Sig	4.94734e-22	0.83
MIXER_I.MNCSLOn_2.m1	Sig	4.94734e-22	0.83
MIXER_I.MNCSLOn_3.m1	Sig	4.94734e-22	0.83
MIXER_I.MNCSLOn_4.m1	Sig	4.94734e-22	0.83
MIXER_I.RCSn.r1	thermal	2.75161e-22	0.46
MIXER_I.RCSp.r1	thermal	2.75106e-22	0.46
MIXER_I.MNCGLOn.m1	Sig	1.893e-22	0.32
MIXER_I.MNCGLOp.m1	Sig	1.88353e-22	0.32
/RACcouple2	rn	1.59027e-22	0.27
/RACcouple1	rn	1.58991e-22	0.27
/R_BPF	rn	1.14662e-22	0.19
MIXER_I.MNCSLOp_1.m1	Sth	1.01877e-22	0.17
MIXER_I.MNCSLOp_2.m1	Sth	1.01877e-22	0.17
MIXER_I.MNCSLOp_3.m1	Sth	1.01877e-22	0.17
MIXER_I.MNCSLOp_4.m1	Sth	1.01877e-22	0.17
MIXER_I.MNCSLOn_1.m1	Sth	1.01839e-22	0.17
MIXER_I.MNCSLOn_2.m1	Sth	1.01839e-22	0.17
MIXER_I.MNCSLOn_3.m1	Sth	1.01839e-22	0.17
MIXER_I.MNCSLOn_4.m1	Sth	1.01839e-22	0.17
MIXER_I.MNCGLOn.m1	Sth	7.18414e-23	0.12
MIXER_I.MNCGLOp.m1	Sth	7.17737e-23	0.12
MIXER_I.RCGp.r1	thermal	6.08941e-23	0.10
MIXER_I.RCGn.r1	thermal	6.08612e-23	0.10
MIXER_Q.MNCSLOn_1.m1	Sth	5.33574e-23	0.09
MIXER_Q.MNCSLOn_2.m1	Sth	5.33574e-23	0.09
MIXER_Q.MNCSLOn_3.m1	Sth	5.33574e-23	0.09
MIXER_Q.MNCSLOn_4.m1	Sth	5.33574e-23	0.09

Spot Noise Summary (in V^2/Hz) at 10G Hz Sorted By Noise Contributors
Total Summarized Noise = 5.93878e-20
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 28 %

thermal noise XCP: 45 %

induced gate noise XCP: 7 %

induced gate noise switching MOSts: 7 %

Appendix C: Noise summaries VCO loaded with ideal Gm-biased BLIXER

1. **Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 1 kHz**

Device	Param	Noise Contribution	% Of Total
GM_ideal_bias.MNCS.m1	Sfl	0.00230772	77.34
GM_ideal_bias.MNCG.m1	Sfl	0.000412594	13.83
GM_ideal_bias.MP2.m1	Sfl	9.84012e-05	3.30
GM_ideal_bias.MPCS.m1	Sfl	1.72478e-05	0.58
XCP.MN1.m1	Sfl	1.50552e-05	0.50
XCP.MN2.m1	Sfl	1.50505e-05	0.50
MIXER_I.MN0.m1	Sig	1.06347e-05	0.36
MIXER_Q.MN0.m1	Sig	1.06347e-05	0.36
/RACcouple2	rn	5.49451e-06	0.18
/RACcouple1	rn	5.49049e-06	0.18
MIXER_I.MNCSLOn_1.m1	Sig	4.66336e-06	0.16
MIXER_I.MNCSLOn_2.m1	Sig	4.66336e-06	0.16
MIXER_I.MNCSLOn_3.m1	Sig	4.66336e-06	0.16
MIXER_I.MNCSLOn_4.m1	Sig	4.66336e-06	0.16
MIXER_I.MNCSLOp_1.m1	Sig	4.63926e-06	0.16
MIXER_I.MNCSLOp_2.m1	Sig	4.63926e-06	0.16
MIXER_I.MNCSLOp_3.m1	Sig	4.63926e-06	0.16
MIXER_I.MNCSLOp_4.m1	Sig	4.63926e-06	0.16
MIXER_Q.MNCSLOp_1.m1	Sfl	3.74065e-06	0.13
MIXER_Q.MNCSLOp_2.m1	Sfl	3.74065e-06	0.13
MIXER_Q.MNCSLOp_3.m1	Sfl	3.74065e-06	0.13
MIXER_Q.MNCSLOp_4.m1	Sfl	3.74065e-06	0.13
MIXER_Q.MNCSLOn_1.m1	Sfl	3.74028e-06	0.13
MIXER_Q.MNCSLOn_2.m1	Sfl	3.74028e-06	0.13
MIXER_Q.MNCSLOn_3.m1	Sfl	3.74028e-06	0.13
MIXER_Q.MNCSLOn_4.m1	Sfl	3.74028e-06	0.13
MIXER_Q.MNCGLOn.m1	Sfl	1.63025e-06	0.05
MIXER_Q.MNCGLOp.m1	Sfl	1.62995e-06	0.05
MIXER_I.MNCGLOn.m1	Sig	1.5901e-06	0.05
MIXER_I.MNCGLOp.m1	Sig	1.55829e-06	0.05
MIXER_I.MNCSLOp_1.m1	Sfl	1.06126e-06	0.04
MIXER_I.MNCSLOp_2.m1	Sfl	1.06126e-06	0.04
MIXER_I.MNCSLOp_3.m1	Sfl	1.06126e-06	0.04
MIXER_I.MNCSLOp_4.m1	Sfl	1.06126e-06	0.04
MIXER_I.MNCSLOn_1.m1	Sfl	1.06032e-06	0.04
MIXER_I.MNCSLOn_2.m1	Sfl	1.06032e-06	0.04
MIXER_I.MNCSLOn_3.m1	Sfl	1.06032e-06	0.04
MIXER_I.MNCSLOn_4.m1	Sfl	1.06032e-06	0.04
/XCP/Rp	rn	6.29636e-07	0.02
MIXER_I.RCSp.r1	flicker	5.13175e-07	0.02

Spot Noise Summary (in V^2/Hz) at 1K Hz Sorted By Noise Contributors
Total Summarized Noise = 0.00298374
No input referred noise available
The above noise summary info is for pnoise data

1/f noise CS & CG MOSt Gm-stage BLIXER: 91 %

2. Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 10 kHz

Device	Param	Noise Contribution	% Of Total
GM_ideal_bias.MNCS.m1	Sfl	2.30651e-06	66.44
GM_ideal_bias.MNCG.m1	Sfl	4.15213e-07	11.96
GM_ideal_bias.MP2.m1	Sfl	9.83497e-08	2.83
/RACcouple2	rn	5.49339e-08	1.58
/RACcouple1	rn	5.48936e-08	1.58
MIXER_I.MNCSLOn_1.m1	Sig	4.66231e-08	1.34
MIXER_I.MNCSLOn_2.m1	Sig	4.66231e-08	1.34
MIXER_I.MNCSLOn_3.m1	Sig	4.66231e-08	1.34
MIXER_I.MNCSLOn_4.m1	Sig	4.66231e-08	1.34
MIXER_I.MNCSLOp_1.m1	Sig	4.63822e-08	1.34
MIXER_I.MNCSLOp_2.m1	Sig	4.63822e-08	1.34
MIXER_I.MNCSLOp_3.m1	Sig	4.63822e-08	1.34
MIXER_I.MNCSLOp_4.m1	Sig	4.63822e-08	1.34
GM_ideal_bias.MPCS.m1	Sfl	1.7239e-08	0.50
MIXER_I.MNCGLOn.m1	Sig	1.58984e-08	0.46
MIXER_I.MNCGLOp.m1	Sig	1.55803e-08	0.45
XCP.MN1.m1	Sfl	1.50665e-08	0.43
XCP.MN2.m1	Sfl	1.50618e-08	0.43
MIXER_I.MN0.m1	Sig	1.49196e-08	0.43
MIXER_Q.MN0.m1	Sig	1.49196e-08	0.43
/XCP/Rp	rn	6.29486e-09	0.18
XCP.MN1.m1	Sth	4.00944e-09	0.12
XCP.MN2.m1	Sth	4.00849e-09	0.12
MIXER_Q.MNCSLOp_1.m1	Sfl	3.741e-09	0.11
MIXER_Q.MNCSLOp_2.m1	Sfl	3.741e-09	0.11
MIXER_Q.MNCSLOp_3.m1	Sfl	3.741e-09	0.11
MIXER_Q.MNCSLOp_4.m1	Sfl	3.741e-09	0.11
MIXER_Q.MNCSLOn_1.m1	Sfl	3.74063e-09	0.11
MIXER_Q.MNCSLOn_2.m1	Sfl	3.74063e-09	0.11
MIXER_Q.MNCSLOn_3.m1	Sfl	3.74063e-09	0.11
MIXER_Q.MNCSLOn_4.m1	Sfl	3.74063e-09	0.11
MIXER_Q.MNCGLOn.m1	Sfl	1.64182e-09	0.05
MIXER_Q.MNCGLOp.m1	Sfl	1.64152e-09	0.05
MIXER_I.MNCSLOp_1.m1	Sfl	1.06024e-09	0.03
MIXER_I.MNCSLOp_2.m1	Sfl	1.06024e-09	0.03
MIXER_I.MNCSLOp_3.m1	Sfl	1.06024e-09	0.03
MIXER_I.MNCSLOp_4.m1	Sfl	1.06024e-09	0.03
MIXER_I.MNCSLOn_2.m1	Sfl	1.0593e-09	0.03
MIXER_I.MNCSLOn_3.m1	Sfl	1.0593e-09	0.03
MIXER_I.MNCSLOn_4.m1	Sfl	1.0593e-09	0.03

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Summarized Noise = 3.47163e-06
No input referred noise available
The above noise summary info is for pnoise data

1/f noise CS & CG MOSt Gm-stage BLIXER: 78 %

AC-coupling resistors: 3 %

induced gate noise switching MOSts: 12 %

3. Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 100 kHz

Device	Param	Noise Contribution	% Of Total
GM_ideal_bias.MNCS.m1	Sfl	2.30561e-09	28.09
/RACcouple2	rn	5.47699e-10	6.67
/RACcouple1	rn	5.47297e-10	6.67
MIXER_I.MNCSLOn_1.m1	Sig	4.64833e-10	5.66
MIXER_I.MNCSLOn_2.m1	Sig	4.64833e-10	5.66
MIXER_I.MNCSLOn_3.m1	Sig	4.64833e-10	5.66
MIXER_I.MNCSLOn_4.m1	Sig	4.64833e-10	5.66
MIXER_I.MNCSLOp_1.m1	Sig	4.62431e-10	5.63
MIXER_I.MNCSLOp_2.m1	Sig	4.62431e-10	5.63
MIXER_I.MNCSLOp_3.m1	Sig	4.62431e-10	5.63
MIXER_I.MNCSLOp_4.m1	Sig	4.62431e-10	5.63
GM_ideal_bias.MNCG.m1	Sfl	4.15452e-10	5.06
MIXER_I.MNCGLOn.m1	Sig	1.58511e-10	1.93
MIXER_I.MNCGLOp.m1	Sig	1.55339e-10	1.89
GM_ideal_bias.MP2.m1	Sfl	9.83111e-11	1.20
/XCP/Rp	rn	6.29385e-11	0.77
XCP.MN1.m1	Sth	4.00935e-11	0.49
XCP.MN2.m1	Sth	4.0084e-11	0.49
GM_ideal_bias.MPCS.m1	Sfl	1.72331e-11	0.21
XCP.MN1.m1	Sfl	1.50855e-11	0.18
XCP.MN2.m1	Sfl	1.50808e-11	0.18
GM_ideal_bias.MNCS.m1	Sth	6.8721e-12	0.08
XCP.MN1.m1	Sig	4.83418e-12	0.06
XCP.MN2.m1	Sig	4.79331e-12	0.06
GM_ideal_bias.MNCG.m1	Sth	3.81013e-12	0.05
MIXER_Q.MNCSLOp_1.m1	Sfl	3.74062e-12	0.05
MIXER_Q.MNCSLOp_2.m1	Sfl	3.74062e-12	0.05
MIXER_Q.MNCSLOp_3.m1	Sfl	3.74062e-12	0.05
MIXER_Q.MNCSLOp_4.m1	Sfl	3.74062e-12	0.05
MIXER_Q.MNCSLOn_1.m1	Sfl	3.74025e-12	0.05
MIXER_Q.MNCSLOn_2.m1	Sfl	3.74025e-12	0.05
MIXER_Q.MNCSLOn_3.m1	Sfl	3.74025e-12	0.05
MIXER_Q.MNCSLOn_4.m1	Sfl	3.74025e-12	0.05
GM_ideal_bias.MP2.m1	Sth	2.88621e-12	0.04
MIXER_I.MN0.m1	Sig	1.85501e-12	0.02
MIXER_Q.MN0.m1	Sig	1.85501e-12	0.02
MIXER_Q.MNCGLOn.m1	Sfl	1.6432e-12	0.02
MIXER_Q.MNCGLOp.m1	Sfl	1.6429e-12	0.02
MIXER_I.RCSn.r1	thermal	1.12603e-12	0.01
MIXER_I.RCSp.r1	thermal	1.12589e-12	0.01

Spot Noise Summary (in V^2/Hz) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 8.2084e-09
No input referred noise available
The above noise summary info is for pnoise data

1/f noise CS MOSt Gm-stage BLIXER: 28 %

AC-coupling resistors: 13 %

induced gate noise switching MOSts: 49 %

4. Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 1 MHz

Device	Param	Noise Contribution	% Of Total
/RACcouple2	rn	4.16005e-12	9.58
/RACcouple1	rn	4.15706e-12	9.57
MIXER_I.MNCSLOn_1.m1	Sig	3.53151e-12	8.13
MIXER_I.MNCSLOn_2.m1	Sig	3.53151e-12	8.13
MIXER_I.MNCSLOn_3.m1	Sig	3.53151e-12	8.13
MIXER_I.MNCSLOn_4.m1	Sig	3.53151e-12	8.13
MIXER_I.MNCSLOp_1.m1	Sig	3.51333e-12	8.09
MIXER_I.MNCSLOp_2.m1	Sig	3.51333e-12	8.09
MIXER_I.MNCSLOp_3.m1	Sig	3.51333e-12	8.09
MIXER_I.MNCSLOp_4.m1	Sig	3.51333e-12	8.09
GM_ideal_bias.MNCS.m1	Sfl	2.21038e-12	5.09
MIXER_I.MNCGLOn.m1	Sig	1.20459e-12	2.77
MIXER_I.MNCGLOp.m1	Sig	1.18051e-12	2.72
/XCP/Rp	rn	6.28728e-13	1.45
GM_ideal_bias.MNCG.m1	Sfl	4.03283e-13	0.93
XCP.MN1.m1	Sth	4.00909e-13	0.92
XCP.MN2.m1	Sth	4.00815e-13	0.92
GM_ideal_bias.MP2.m1	Sfl	9.4235e-14	0.22
GM_ideal_bias.MNCS.m1	Sth	6.60164e-14	0.15
XCP.MN1.m1	Sig	4.83267e-14	0.11
XCP.MN2.m1	Sig	4.79181e-14	0.11
GM_ideal_bias.MNCG.m1	Sth	3.70379e-14	0.09
GM_ideal_bias.MP2.m1	Sth	2.76655e-14	0.06
GM_ideal_bias.MPCS.m1	Sfl	1.65522e-14	0.04
XCP.MN1.m1	Sfl	1.52554e-14	0.04
XCP.MN2.m1	Sfl	1.52508e-14	0.04
MIXER_I.RCSn.r1	thermal	1.10456e-14	0.03
MIXER_I.RCSp.r1	thermal	1.10442e-14	0.03
/R_BPF	rn	4.26516e-15	0.01
MIXER_I.MNCSLOp_1.m1	Sth	3.70226e-15	0.01
MIXER_I.MNCSLOp_2.m1	Sth	3.70226e-15	0.01
MIXER_I.MNCSLOp_3.m1	Sth	3.70226e-15	0.01
MIXER_I.MNCSLOp_4.m1	Sth	3.70226e-15	0.01
MIXER_I.MNCSLOn_1.m1	Sth	3.69946e-15	0.01
MIXER_I.MNCSLOn_2.m1	Sth	3.69946e-15	0.01
MIXER_I.MNCSLOn_3.m1	Sth	3.69946e-15	0.01
MIXER_I.MNCSLOn_4.m1	Sth	3.69946e-15	0.01
MIXER_Q.MNCSLOp_2.m1	Sfl	3.64603e-15	0.01
MIXER_Q.MNCSLOp_3.m1	Sfl	3.64603e-15	0.01
MIXER_Q.MNCSLOp_4.m1	Sfl	3.64603e-15	0.01

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 4.34432e-11
No input referred noise available
The above noise summary info is for pnoise data

AC-coupling resistors: 19 %

induced gate noise switching MOSts: 70 %

1/f noise CS MOSt Gm-stage BLIXER: 5 %

5. Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 10 MHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	6.2136e-15	17.00
XCP.MN1.m1	Sth	4.00465e-15	10.96
XCP.MN2.m1	Sth	4.00371e-15	10.95
GM_ideal_bias.MNCS.m1	Sfl	1.95916e-15	5.36
/RACcouple2	rn	1.73584e-15	4.75
/RACcouple1	rn	1.73475e-15	4.75
MIXER_I.MNCSLOn_1.m1	Sig	1.52513e-15	4.17
MIXER_I.MNCSLOn_2.m1	Sig	1.52513e-15	4.17
MIXER_I.MNCSLOn_3.m1	Sig	1.52513e-15	4.17
MIXER_I.MNCSLOn_4.m1	Sig	1.52513e-15	4.17
MIXER_I.MNCSLOp_1.m1	Sig	1.51782e-15	4.15
MIXER_I.MNCSLOp_2.m1	Sig	1.51782e-15	4.15
MIXER_I.MNCSLOp_3.m1	Sig	1.51782e-15	4.15
MIXER_I.MNCSLOp_4.m1	Sig	1.51782e-15	4.15
GM_ideal_bias.MNCS.m1	Sth	5.8912e-16	1.61
MIXER_I.MNCGLOn.m1	Sig	5.30106e-16	1.45
MIXER_I.MNCGLOp.m1	Sig	5.1952e-16	1.42
XCP.MN1.m1	Sig	4.81274e-16	1.32
XCP.MN2.m1	Sig	4.77213e-16	1.31
GM_ideal_bias.MNCG.m1	Sfl	3.64451e-16	1.00
GM_ideal_bias.MNCG.m1	Sth	3.36579e-16	0.92
GM_ideal_bias.MP2.m1	Sth	2.44914e-16	0.67
MIXER_I.RCSn.r1	thermal	1.02997e-16	0.28
MIXER_I.RCSp.r1	thermal	1.02983e-16	0.28
GM_ideal_bias.MP2.m1	Sfl	8.34231e-17	0.23
/R_BPF	rn	3.85957e-17	0.11
MIXER_I.MNCSLOp_1.m1	Sth	3.79631e-17	0.10
MIXER_I.MNCSLOp_2.m1	Sth	3.79631e-17	0.10
MIXER_I.MNCSLOp_3.m1	Sth	3.79631e-17	0.10
MIXER_I.MNCSLOp_4.m1	Sth	3.79631e-17	0.10
MIXER_I.MNCSLOn_1.m1	Sth	3.79355e-17	0.10
MIXER_I.MNCSLOn_2.m1	Sth	3.79355e-17	0.10
MIXER_I.MNCSLOn_3.m1	Sth	3.79355e-17	0.10
MIXER_I.MNCSLOn_4.m1	Sth	3.79355e-17	0.10
MIXER_I.RCGp.r1	thermal	2.98824e-17	0.08
MIXER_I.RCGn.r1	thermal	2.98751e-17	0.08
MIXER_Q.MNCSLOn_1.m1	Sth	2.83316e-17	0.08
MIXER_Q.MNCSLOn_2.m1	Sth	2.83316e-17	0.08
MIXER_Q.MNCSLOn_3.m1	Sth	2.83316e-17	0.08
MIXER_Q.MNCSLOn_4.m1	Sth	2.83316e-17	0.08

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 3.65474e-14
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 17 %
thermal noise XCP: 22 %
1/f noise CS MOSt Gm-stage BLIXER: 5 %
AC-coupling resistors: 10 %
induced gate noise switching MOSts: 36 %

6. Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 100 MHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	5.70662e-17	31.01
XCP.MN1.m1	Sth	4.01303e-17	21.81
XCP.MN2.m1	Sth	4.01215e-17	21.80
GM_ideal_bias.MNCS.m1	Sth	7.35934e-18	4.00
XCP.MN1.m1	Sig	4.67908e-18	2.54
XCP.MN2.m1	Sig	4.64081e-18	2.52
GM_ideal_bias.MNCG.m1	Sth	3.09092e-18	1.68
GM_ideal_bias.MP2.m1	Sth	2.87158e-18	1.56
GM_ideal_bias.MNCS.m1	Sfl	2.45529e-18	1.33
MIXER_I.MNCSLOn_1.m1	Sig	1.07522e-18	0.58
MIXER_I.MNCSLOn_2.m1	Sig	1.07522e-18	0.58
MIXER_I.MNCSLOn_3.m1	Sig	1.07522e-18	0.58
MIXER_I.MNCSLOn_4.m1	Sig	1.07522e-18	0.58
MIXER_I.MNCSLOp_1.m1	Sig	1.07294e-18	0.58
MIXER_I.MNCSLOp_2.m1	Sig	1.07294e-18	0.58
MIXER_I.MNCSLOp_3.m1	Sig	1.07294e-18	0.58
MIXER_I.MNCSLOp_4.m1	Sig	1.07294e-18	0.58
MIXER_I.RCSn.r1	thermal	9.17982e-19	0.50
MIXER_I.RCSp.r1	thermal	9.17816e-19	0.50
/RACcouple2	rn	6.77062e-19	0.37
/RACcouple1	rn	6.76319e-19	0.37
GM_ideal_bias.MPCS.m1	Sth	5.65692e-19	0.31
MIXER_I.MNCGLOn.m1	Sig	4.81415e-19	0.26
MIXER_I.MNCGLOp.m1	Sig	4.71623e-19	0.26
MIXER_Q.MNCSLOn_1.m1	Sth	3.48798e-19	0.19
MIXER_Q.MNCSLOn_2.m1	Sth	3.48798e-19	0.19
MIXER_Q.MNCSLOn_3.m1	Sth	3.48798e-19	0.19
MIXER_Q.MNCSLOn_4.m1	Sth	3.48798e-19	0.19
MIXER_Q.MNCSLOp_1.m1	Sth	3.48724e-19	0.19
MIXER_Q.MNCSLOp_2.m1	Sth	3.48724e-19	0.19
MIXER_Q.MNCSLOp_3.m1	Sth	3.48724e-19	0.19
MIXER_Q.MNCSLOp_4.m1	Sth	3.48724e-19	0.19
GM_ideal_bias.MNCG.m1	Sfl	3.30247e-19	0.18
/R_BPF	rn	3.17986e-19	0.17
MIXER_I.RCGp.r1	thermal	3.12382e-19	0.17
MIXER_I.RCGn.r1	thermal	3.12294e-19	0.17
MIXER_I.MNCSLOp_1.m1	Sth	3.08293e-19	0.17
MIXER_I.MNCSLOp_2.m1	Sth	3.08293e-19	0.17
MIXER_I.MNCSLOp_3.m1	Sth	3.08293e-19	0.17
MIXER_I.MNCSLOp_4.m1	Sth	3.08293e-19	0.17

Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.8401e-16
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 31 %
thermal noise XCP: 43 %
thermal noise CS MOSt Gm-stage BLIXER: 4 %
induced gate noise XCP: 5 %
induced gate noise switching MOSts: 5 %

7. Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 1 GHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	9.06633e-19	35.07
XCP.MN1.m1	Sth	5.43005e-19	21.00
XCP.MN2.m1	Sth	5.4289e-19	21.00
GM_ideal_bias.MNCS.m1	Sth	1.1483e-19	4.44
XCP.MN1.m1	Sig	6.38157e-20	2.47
XCP.MN2.m1	Sig	6.34249e-20	2.45
GM_ideal_bias.MPCS.m1	Sth	5.66654e-20	2.19
GM_ideal_bias.MNCG.m1	Sth	2.42922e-20	0.94
MIXER_I.RCSn.r1	thermal	1.31639e-20	0.51
MIXER_I.RCSp.r1	thermal	1.3162e-20	0.51
MIXER_I.MNCSLOn_1.m1	Sig	1.20592e-20	0.47
MIXER_I.MNCSLOn_2.m1	Sig	1.20592e-20	0.47
MIXER_I.MNCSLOn_3.m1	Sig	1.20592e-20	0.47
MIXER_I.MNCSLOn_4.m1	Sig	1.20592e-20	0.47
MIXER_I.MNCSLOp_1.m1	Sig	1.20242e-20	0.47
MIXER_I.MNCSLOp_2.m1	Sig	1.20242e-20	0.47
MIXER_I.MNCSLOp_3.m1	Sig	1.20242e-20	0.47
MIXER_I.MNCSLOp_4.m1	Sig	1.20242e-20	0.47
/RACcouple2	rn	7.63201e-21	0.30
/RACcouple1	rn	7.60902e-21	0.29
MIXER_Q.MNCSLOn_1.m1	Sth	6.37553e-21	0.25
MIXER_Q.MNCSLOn_2.m1	Sth	6.37553e-21	0.25
MIXER_Q.MNCSLOn_3.m1	Sth	6.37553e-21	0.25
MIXER_Q.MNCSLOn_4.m1	Sth	6.37553e-21	0.25
MIXER_Q.MNCSLOp_1.m1	Sth	6.3743e-21	0.25
MIXER_Q.MNCSLOp_2.m1	Sth	6.3743e-21	0.25
MIXER_Q.MNCSLOp_3.m1	Sth	6.3743e-21	0.25
MIXER_Q.MNCSLOp_4.m1	Sth	6.3743e-21	0.25
GM_ideal_bias.MP2.m1	Sth	5.84933e-21	0.23
MIXER_I.MNCGLOn.m1	Sig	5.42358e-21	0.21
MIXER_I.MNCGLOp.m1	Sig	5.33848e-21	0.21
/PORTin	rn	4.83057e-21	0.19
MIXER_I.RCGp.r1	thermal	4.34765e-21	0.17
MIXER_I.RCGn.r1	thermal	4.34648e-21	0.17
GM_ideal_bias.MNCS.m1	Sfl	3.75301e-21	0.15
GM_ideal_bias.MPCS.m1	Sfl	3.56423e-21	0.14
MIXER_I.MNCSLOp_1.m1	Sth	3.53207e-21	0.14
MIXER_I.MNCSLOp_2.m1	Sth	3.53207e-21	0.14
MIXER_I.MNCSLOp_3.m1	Sth	3.53207e-21	0.14
MIXER_I.MNCSLOp_4.m1	Sth	3.53207e-21	0.14

Spot Noise Summary (in V^2/Hz) at 10 Hz Sorted By Noise Contributors
Total Summarized Noise = 2.58553e-18
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 35 %

thermal noise XCP: 42 %

thermal noise CS MOSt Gm-stage BLIXER: 4 %

induced gate noise XCP: 5 %

induced gate noise switching MOSts: 4 %

8. Noise summary VCO loaded with ideal Gm-biased BLIXER at an offset of 10 GHz

Device	Param	Noise Contribution	% Of Total
/XCP/Rp	rn	1.66272e-20	28.30
XCP.MN1.m1	Sth	1.36629e-20	23.25
XCP.MN2.m1	Sth	1.36602e-20	23.25
XCP.MN1.m1	Sig	2.01443e-21	3.43
XCP.MN2.m1	Sig	2.00724e-21	3.42
GM_ideal_bias.MNCS.m1	Sth	1.78154e-21	3.03
GM_ideal_bias.MPCS.m1	Sth	9.883e-22	1.68
MIXER_I.MNCSLOn_1.m1	Sig	5.0488e-22	0.86
MIXER_I.MNCSLOn_2.m1	Sig	5.0488e-22	0.86
MIXER_I.MNCSLOn_3.m1	Sig	5.0488e-22	0.86
MIXER_I.MNCSLOn_4.m1	Sig	5.0488e-22	0.86
MIXER_I.MNCSLOp_1.m1	Sig	5.04618e-22	0.86
MIXER_I.MNCSLOp_2.m1	Sig	5.04618e-22	0.86
MIXER_I.MNCSLOp_3.m1	Sig	5.04618e-22	0.86
MIXER_I.MNCSLOp_4.m1	Sig	5.04618e-22	0.86
GM_ideal_bias.MNCG.m1	Sth	4.14304e-22	0.71
/PORTin	rn	3.14138e-22	0.53
MIXER_I.RCSp.r1	thermal	2.79471e-22	0.48
MIXER_I.RCSn.r1	thermal	2.79468e-22	0.48
MIXER_I.MNCGLOn.m1	Sig	2.04323e-22	0.35
MIXER_I.MNCGLOp.m1	Sig	2.02013e-22	0.34
/RACcouple2	rn	1.59978e-22	0.27
/RACcouple1	rn	1.5993e-22	0.27
MIXER_I.MNCSLOp_1.m1	Sth	1.02339e-22	0.17
MIXER_I.MNCSLOp_2.m1	Sth	1.02339e-22	0.17
MIXER_I.MNCSLOp_3.m1	Sth	1.02339e-22	0.17
MIXER_I.MNCSLOp_4.m1	Sth	1.02339e-22	0.17
MIXER_I.MNCSLOn_1.m1	Sth	1.02267e-22	0.17
MIXER_I.MNCSLOn_2.m1	Sth	1.02267e-22	0.17
MIXER_I.MNCSLOn_3.m1	Sth	1.02267e-22	0.17
MIXER_I.MNCSLOn_4.m1	Sth	1.02267e-22	0.17
MIXER_I.MNCGLOn.m1	Sth	8.80288e-23	0.15
MIXER_I.MNCGLOp.m1	Sth	8.80265e-23	0.15
MIXER_I.RCGp.r1	thermal	7.10438e-23	0.12
MIXER_I.RCGn.r1	thermal	7.10162e-23	0.12
MIXER_Q.MNCSLOn_1.m1	Sth	5.92381e-23	0.10
MIXER_Q.MNCSLOn_2.m1	Sth	5.92381e-23	0.10
MIXER_Q.MNCSLOn_3.m1	Sth	5.92381e-23	0.10
MIXER_Q.MNCSLOn_4.m1	Sth	5.92381e-23	0.10
MIXER_Q.MNCSLOp_4.m1	Sth	5.91931e-23	0.10

Spot Noise Summary (in V^2/Hz) at 10G Hz Sorted By Noise Contributors
Total Summarized Noise = 5.87622e-20
No input referred noise available
The above noise summary info is for pnoise data

thermal noise Rp: 28 %

thermal noise XCP: 47 %

induced gate noise XCP: 7 %

induced gate noise switching MOSts: 8 %

Appendix D: Noise summaries BLIXER driven with ideal sine wave VCO

1. Noise summary of mixer at IF = 10 kHz driven with ideal sine wave VCO

Device	Param	Noise Contribution	% Of Total
MIXER_I.MNCGLOp.m1	Sfl	2.01053e-15	33.73
MIXER_I.MNCGLOn.m1	Sfl	2.01037e-15	33.73
MIXER_Q.MNCGLOn.m1	Sfl	3.02151e-16	5.07
MIXER_Q.MNCGLOp.m1	Sfl	3.02128e-16	5.07
MIXER_I.MNCSLOn_1.m1	Sfl	1.42686e-16	2.39
MIXER_I.MNCSLOn_2.m1	Sfl	1.42686e-16	2.39
MIXER_I.MNCSLOn_3.m1	Sfl	1.42686e-16	2.39
MIXER_I.MNCSLOn_4.m1	Sfl	1.42686e-16	2.39
MIXER_I.MNCSLOp_1.m1	Sfl	1.42678e-16	2.39
MIXER_I.MNCSLOp_2.m1	Sfl	1.42678e-16	2.39
MIXER_I.MNCSLOp_3.m1	Sfl	1.42678e-16	2.39
MIXER_I.MNCSLOp_4.m1	Sfl	1.42678e-16	2.39
MIXER_I.RCSn.r1	flicker	2.54877e-17	0.43
MIXER_I.RCSp.r1	flicker	2.54795e-17	0.43
/PORTin	rn	1.61405e-17	0.27
MIXER_I.MNCGLOp.m1	Sth	9.0956e-18	0.15
MIXER_I.MNCGLOn.m1	Sth	9.09546e-18	0.15
MIXER_I.RCGp.r1	thermal	7.3046e-18	0.12
MIXER_I.RCGn.r1	thermal	7.30437e-18	0.12
MIXER_Q.MNCSLOp_1.m1	Sfl	6.62582e-18	0.11
MIXER_Q.MNCSLOp_2.m1	Sfl	6.62582e-18	0.11
MIXER_Q.MNCSLOp_3.m1	Sfl	6.62582e-18	0.11
MIXER_Q.MNCSLOp_4.m1	Sfl	6.62582e-18	0.11
MIXER_Q.MNCSLOn_1.m1	Sfl	6.62434e-18	0.11
MIXER_Q.MNCSLOn_2.m1	Sfl	6.62434e-18	0.11
MIXER_Q.MNCSLOn_3.m1	Sfl	6.62434e-18	0.11
MIXER_Q.MNCSLOn_4.m1	Sfl	6.62434e-18	0.11
MIXER_I.RCGp.r1	flicker	5.92733e-18	0.10
MIXER_I.RCGn.r1	flicker	5.92369e-18	0.10
GM_0.MNCS.m1	Sth	3.03845e-18	0.05
MIXER_Q.MNCGLOn.m1	Sth	1.95231e-18	0.03
MIXER_Q.MNCGLOp.m1	Sth	1.95216e-18	0.03
MIXER_I.RCSp.r1	thermal	1.88365e-18	0.03
MIXER_I.RCSn.r1	thermal	1.88351e-18	0.03
GM_0.MPCS.m1	Sth	1.70997e-18	0.03
/RBPF	rn	1.59032e-18	0.03
MIXER_I.MNCSLOn_1.m1	Sth	1.37395e-18	0.02
MIXER_I.MNCSLOn_2.m1	Sth	1.37395e-18	0.02
MIXER_I.MNCSLOn_3.m1	Sth	1.37395e-18	0.02
MIXER_I.MNCSLOn_4.m1	Sth	1.37395e-18	0.02

1/f noise CG switching MOSts: 78 %

1/f noise CS switching MOSts: 20 %

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Summarized Noise = 5.96033e-15
Total Input Referred Noise = 1.48421e-16
The above noise summary info is for pnoise data

2. Noise summary of mixer at IF = 100 kHz driven with ideal sine wave VCO

Device	Param	Noise Contribution	% Of Total
MIXER_I.MNCGLOp.m1	Sfl	2.01055e-16	30.24
MIXER_I.MNCGLOn.m1	Sfl	2.01039e-16	30.24
MIXER_Q.MNCGLOn.m1	Sfl	3.02157e-17	4.54
MIXER_Q.MNCGLOp.m1	Sfl	3.02134e-17	4.54
/PORTin	rn	1.61405e-17	2.43
MIXER_I.MNCSLOn_1.m1	Sfl	1.42688e-17	2.15
MIXER_I.MNCSLOn_2.m1	Sfl	1.42688e-17	2.15
MIXER_I.MNCSLOn_3.m1	Sfl	1.42688e-17	2.15
MIXER_I.MNCSLOn_4.m1	Sfl	1.42688e-17	2.15
MIXER_I.MNCSLOp_1.m1	Sfl	1.4268e-17	2.15
MIXER_I.MNCSLOp_2.m1	Sfl	1.4268e-17	2.15
MIXER_I.MNCSLOp_3.m1	Sfl	1.4268e-17	2.15
MIXER_I.MNCSLOp_4.m1	Sfl	1.4268e-17	2.15
MIXER_I.MNCGLOp.m1	Sth	9.0956e-18	1.37
MIXER_I.MNCGLOn.m1	Sth	9.09546e-18	1.37
MIXER_I.RCGp.r1	thermal	7.3046e-18	1.10
MIXER_I.RCGn.r1	thermal	7.30437e-18	1.10
GM_0.MNCS.m1	Sth	3.03845e-18	0.46
MIXER_I.RCSn.r1	flicker	2.54877e-18	0.38
MIXER_I.RCSp.r1	flicker	2.54795e-18	0.38
MIXER_Q.MNCGLOn.m1	Sth	1.95231e-18	0.29
MIXER_Q.MNCGLOp.m1	Sth	1.95216e-18	0.29
MIXER_I.RCSp.r1	thermal	1.88365e-18	0.28
MIXER_I.RCSn.r1	thermal	1.88351e-18	0.28
GM_0.MPCS.m1	Sth	1.70997e-18	0.26
/RBPF	rn	1.59032e-18	0.24
MIXER_I.MNCSLOn_1.m1	Sth	1.37395e-18	0.21
MIXER_I.MNCSLOn_2.m1	Sth	1.37395e-18	0.21
MIXER_I.MNCSLOn_3.m1	Sth	1.37395e-18	0.21
MIXER_I.MNCSLOn_4.m1	Sth	1.37395e-18	0.21
MIXER_I.MNCSLOp_1.m1	Sth	1.37388e-18	0.21
MIXER_I.MNCSLOp_2.m1	Sth	1.37388e-18	0.21
MIXER_I.MNCSLOp_3.m1	Sth	1.37388e-18	0.21
MIXER_I.MNCSLOp_4.m1	Sth	1.37388e-18	0.21
GM_0.MNCG.m1	Sth	1.14419e-18	0.17
MIXER_Q.MNCSLOp_1.m1	Sfl	6.62594e-19	0.10
MIXER_Q.MNCSLOp_2.m1	Sfl	6.62594e-19	0.10
MIXER_Q.MNCSLOp_3.m1	Sfl	6.62594e-19	0.10
MIXER_Q.MNCSLOp_4.m1	Sfl	6.62594e-19	0.10
MIXER_Q.MNCSLOn_4.m1	Sfl	6.62446e-19	0.10

Spot Noise Summary (in V^2/Hz) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 6.64832e-16
Total Input Referred Noise = 1.65547e-17
The above noise summary info is for pnoise data

1/f noise CG switching MOSts: 70 %

1/f noise CS switching MOSts I-mixer: 17 %

3. Noise summary of mixer at IF = 1 MHz driven with ideal sine wave VCO

Device	Param	Noise Contribution	% Of Total
MIXER_I.MNCGLOp.m1	Sfl	2.01081e-17	14.86
MIXER_I.MNCGLOn.m1	Sfl	2.01065e-17	14.86
/PORTin	rn	1.61405e-17	11.93
MIXER_I.MNCGLOp.m1	Sth	9.0956e-18	6.72
MIXER_I.MNCGLOn.m1	Sth	9.09546e-18	6.72
MIXER_I.RCGp.r1	thermal	7.30459e-18	5.40
MIXER_I.RCGn.r1	thermal	7.30437e-18	5.40
GM_0.MNCS.m1	Sth	3.03845e-18	2.25
MIXER_Q.MNCGLOn.m1	Sfl	3.02216e-18	2.23
MIXER_Q.MNCGLOp.m1	Sfl	3.02193e-18	2.23
MIXER_Q.MNCGLOn.m1	Sth	1.95231e-18	1.44
MIXER_Q.MNCGLOp.m1	Sth	1.95216e-18	1.44
MIXER_I.RCSp.r1	thermal	1.88365e-18	1.39
MIXER_I.RCSn.r1	thermal	1.88351e-18	1.39
GM_0.MPCS.m1	Sth	1.70997e-18	1.26
/RBPF	rn	1.59032e-18	1.18
MIXER_I.MNCSLOn_1.m1	Sfl	1.4271e-18	1.05
MIXER_I.MNCSLOn_2.m1	Sfl	1.4271e-18	1.05
MIXER_I.MNCSLOn_3.m1	Sfl	1.4271e-18	1.05
MIXER_I.MNCSLOn_4.m1	Sfl	1.4271e-18	1.05
MIXER_I.MNCSLOp_1.m1	Sfl	1.42702e-18	1.05
MIXER_I.MNCSLOp_2.m1	Sfl	1.42702e-18	1.05
MIXER_I.MNCSLOp_3.m1	Sfl	1.42702e-18	1.05
MIXER_I.MNCSLOp_4.m1	Sfl	1.42702e-18	1.05
MIXER_I.MNCSLOn_1.m1	Sth	1.37394e-18	1.02
MIXER_I.MNCSLOn_2.m1	Sth	1.37394e-18	1.02
MIXER_I.MNCSLOn_3.m1	Sth	1.37394e-18	1.02
MIXER_I.MNCSLOn_4.m1	Sth	1.37394e-18	1.02
MIXER_I.MNCSLOp_1.m1	Sth	1.37388e-18	1.02
MIXER_I.MNCSLOp_2.m1	Sth	1.37388e-18	1.02
MIXER_I.MNCSLOp_3.m1	Sth	1.37388e-18	1.02
MIXER_I.MNCSLOp_4.m1	Sth	1.37388e-18	1.02
GM_0.MNCG.m1	Sth	1.14419e-18	0.85
MIXER_I.RCSn.r1	flicker	2.54877e-19	0.19
MIXER_I.RCSp.r1	flicker	2.54795e-19	0.19
MIXER_Q.MNCGLOn.m1	Sig	7.7831e-20	0.06
MIXER_Q.MNCGLOp.m1	Sig	7.78264e-20	0.06
MIXER_I.MNCGLOp.m1	Sig	7.65643e-20	0.06
MIXER_I.MNCGLOn.m1	Sig	7.65643e-20	0.06
MIXER_Q.MNCSLOp_4.m1	Sth	7.29428e-20	0.05

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.35281e-16
Total Input Referred Noise = 3.36742e-18
The above noise summary info is for pnoise data

1/f noise CG switching MOSts I-Mixer: 30 %

thermal noise CG switching MOSts I-Mixer: 13 %

thermal noise CG-load resistors I-Mixer: 11 %

1/f noise CG switching MOSts Q-Mixer: 4 %

thermal noise CG switching MOSts Q-Mixer: 3 %

1/f noise CS switching MOSts I-mixer: 8 %

thermal noise CS switching MOSts I-mixer: 8 %

4. Noise summary of mixer at IF = 10 MHz driven with ideal sine wave VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	1.61393e-17	19.61
MIXER_I.MNCGLOp.m1	Sth	9.09497e-18	11.05
MIXER_I.MNCGLOn.m1	Sth	9.09482e-18	11.05
MIXER_I.RCGp.r1	thermal	7.30434e-18	8.87
MIXER_I.RCGn.r1	thermal	7.30411e-18	8.87
GM_0.MNCS.m1	Sth	3.03813e-18	3.69
MIXER_I.MNCGLOp.m1	Sfl	2.0132e-18	2.45
MIXER_I.MNCGLOn.m1	Sfl	2.01304e-18	2.45
MIXER_Q.MNCGLOn.m1	Sth	1.95227e-18	2.37
MIXER_Q.MNCGLOp.m1	Sth	1.95211e-18	2.37
MIXER_I.RCSp.r1	thermal	1.88345e-18	2.29
MIXER_I.RCSn.r1	thermal	1.88331e-18	2.29
GM_0.MPCS.m1	Sth	1.70979e-18	2.08
/RBPF	rn	1.59021e-18	1.93
MIXER_I.MNCSLOn_1.m1	Sth	1.37378e-18	1.67
MIXER_I.MNCSLOn_2.m1	Sth	1.37378e-18	1.67
MIXER_I.MNCSLOn_3.m1	Sth	1.37378e-18	1.67
MIXER_I.MNCSLOn_4.m1	Sth	1.37378e-18	1.67
MIXER_I.MNCSLOp_1.m1	Sth	1.37371e-18	1.67
MIXER_I.MNCSLOp_2.m1	Sth	1.37371e-18	1.67
MIXER_I.MNCSLOp_3.m1	Sth	1.37371e-18	1.67
MIXER_I.MNCSLOp_4.m1	Sth	1.37371e-18	1.67
GM_0.MNCG.m1	Sth	1.14421e-18	1.39
MIXER_Q.MNCGLOn.m1	Sfl	3.02802e-19	0.37
MIXER_Q.MNCGLOp.m1	Sfl	3.02779e-19	0.37
MIXER_I.MNCSLOn_1.m1	Sfl	1.42918e-19	0.17
MIXER_I.MNCSLOn_2.m1	Sfl	1.42918e-19	0.17
MIXER_I.MNCSLOn_3.m1	Sfl	1.42918e-19	0.17
MIXER_I.MNCSLOn_4.m1	Sfl	1.42918e-19	0.17
MIXER_I.MNCSLOp_1.m1	Sfl	1.4291e-19	0.17
MIXER_I.MNCSLOp_2.m1	Sfl	1.4291e-19	0.17
MIXER_I.MNCSLOp_3.m1	Sfl	1.4291e-19	0.17
MIXER_I.MNCSLOp_4.m1	Sfl	1.4291e-19	0.17
MIXER_Q.MNCGLOn.m1	Sig	7.78271e-20	0.09
MIXER_Q.MNCGLOp.m1	Sig	7.78226e-20	0.09
MIXER_I.MNCGLOp.m1	Sig	7.65592e-20	0.09
MIXER_I.MNCGLOn.m1	Sig	7.65591e-20	0.09
MIXER_Q.MNCSLOp_2.m1	Sth	7.29469e-20	0.09
MIXER_Q.MNCSLOp_3.m1	Sth	7.29469e-20	0.09
MIXER_Q.MNCSLOp_4.m1	Sth	7.29469e-20	0.09

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 8.23207e-17
Total Input Referred Noise = 2.04214e-18
The above noise summary info is for pnoise data

thermal noise CG switching MOSts I-Mixer: 22 %

thermal noise CG-load resistors I-Mixer: 18 %

1/f noise CG switching MOSts I-Mixer: 5 %

thermal noise CG switching MOSts Q-Mixer: 5 %

thermal noise CS switching MOSts I-mixer: 13 %

5. Noise summary of mixer at IF = 100 MHz driven with ideal sine wave VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	1.60146e-17	20.94
MIXER_I.MNCGLOp.m1	Sth	9.03249e-18	11.81
MIXER_I.MNCGLOn.m1	Sth	9.03234e-18	11.81
MIXER_I.RCGp.r1	thermal	7.2791e-18	9.52
MIXER_I.RCGn.r1	thermal	7.27888e-18	9.52
GM_0.MNCS.m1	Sth	3.00643e-18	3.93
MIXER_Q.MNCGLOn.m1	Sth	1.94782e-18	2.55
MIXER_Q.MNCGLOp.m1	Sth	1.94767e-18	2.55
MIXER_I.RCSp.r1	thermal	1.86386e-18	2.44
MIXER_I.RCSn.r1	thermal	1.86373e-18	2.44
GM_0.MPCS.m1	Sth	1.69202e-18	2.21
/RBPF	rn	1.57929e-18	2.06
MIXER_I.MNCSLOn_1.m1	Sth	1.3578e-18	1.78
MIXER_I.MNCSLOn_2.m1	Sth	1.3578e-18	1.78
MIXER_I.MNCSLOn_3.m1	Sth	1.3578e-18	1.78
MIXER_I.MNCSLOn_4.m1	Sth	1.3578e-18	1.78
MIXER_I.MNCSLOp_1.m1	Sth	1.35773e-18	1.78
MIXER_I.MNCSLOp_2.m1	Sth	1.35773e-18	1.78
MIXER_I.MNCSLOp_3.m1	Sth	1.35773e-18	1.78
MIXER_I.MNCSLOp_4.m1	Sth	1.35773e-18	1.78
GM_0.MNCG.m1	Sth	1.14617e-18	1.50
MIXER_I.MNCGLOp.m1	Sfl	2.02457e-19	0.26
MIXER_I.MNCGLOn.m1	Sfl	2.02441e-19	0.26
MIXER_Q.MNCGLOn.m1	Sig	7.74415e-20	0.10
MIXER_Q.MNCGLOp.m1	Sig	7.7437e-20	0.10
MIXER_I.MNCGLOp.m1	Sig	7.60494e-20	0.10
MIXER_I.MNCGLOn.m1	Sig	7.60494e-20	0.10
MIXER_Q.MNCSLOp_1.m1	Sth	7.3348e-20	0.10
MIXER_Q.MNCSLOp_2.m1	Sth	7.3348e-20	0.10
MIXER_Q.MNCSLOp_3.m1	Sth	7.3348e-20	0.10
MIXER_Q.MNCSLOp_4.m1	Sth	7.3348e-20	0.10
MIXER_Q.MNCSLOn_1.m1	Sth	7.33338e-20	0.10
MIXER_Q.MNCSLOn_2.m1	Sth	7.33338e-20	0.10
MIXER_Q.MNCSLOn_3.m1	Sth	7.33338e-20	0.10
MIXER_Q.MNCSLOn_4.m1	Sth	7.33338e-20	0.10
MIXER_Q.RCSn.r1	thermal	5.06555e-20	0.07
MIXER_Q.RCSp.r1	thermal	5.06498e-20	0.07
MIXER_Q.RCGn.r1	thermal	3.70199e-20	0.05
MIXER_Q.RCGp.r1	thermal	3.70162e-20	0.05
GM_0.R0.r1	thermal	3.50209e-20	0.05

Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 7.6483e-17
Total Input Referred Noise = 1.84831e-18
The above noise summary info is for pnoise data

thermal noise CG switching MOSts I-Mixer: 24 %

thermal noise CG-load resistors I-Mixer: 19 %

thermal noise CG switching MOSts Q-Mixer: 5 %

thermal noise CS-load resistors I-Mixer: 5 %

thermal noise CS switching MOSts I-mixer: 14 %

6. Noise summary of mixer at IF = 1 GHz driven with ideal sine wave VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	9.10937e-18	19.96
MIXER_I.MNCGLOp.m1	Sth	5.53884e-18	12.13
MIXER_I.MNCGLOn.m1	Sth	5.5388e-18	12.13
MIXER_I.RCGp.r1	thermal	5.36221e-18	11.75
MIXER_I.RCGn.r1	thermal	5.36219e-18	11.75
MIXER_Q.MNCGLOn.m1	Sth	1.47607e-18	3.23
MIXER_Q.MNCGLOp.m1	Sth	1.47599e-18	3.23
GM_0.MNCS.m1	Sth	1.41491e-18	3.10
GM_0.MNCG.m1	Sth	1.13171e-18	2.48
/RBPF	rn	9.53249e-19	2.09
MIXER_I.RCSp.r1	thermal	8.76939e-19	1.92
MIXER_I.RCSn.r1	thermal	8.76888e-19	1.92
GM_0.MPCS.m1	Sth	7.98653e-19	1.75
MIXER_I.MNCSLOn_1.m1	Sth	5.99202e-19	1.31
MIXER_I.MNCSLOn_2.m1	Sth	5.99202e-19	1.31
MIXER_I.MNCSLOn_3.m1	Sth	5.99202e-19	1.31
MIXER_I.MNCSLOn_4.m1	Sth	5.99202e-19	1.31
MIXER_I.MNCSLOp_1.m1	Sth	5.99169e-19	1.31
MIXER_I.MNCSLOp_2.m1	Sth	5.99169e-19	1.31
MIXER_I.MNCSLOp_3.m1	Sth	5.99169e-19	1.31
MIXER_I.MNCSLOp_4.m1	Sth	5.99169e-19	1.31
MIXER_Q.MNCSLOp_1.m1	Sth	6.19952e-20	0.14
MIXER_Q.MNCSLOp_2.m1	Sth	6.19952e-20	0.14
MIXER_Q.MNCSLOp_3.m1	Sth	6.19952e-20	0.14
MIXER_Q.MNCSLOp_4.m1	Sth	6.19952e-20	0.14
MIXER_Q.MNCSLOn_1.m1	Sth	6.19867e-20	0.14
MIXER_Q.MNCSLOn_2.m1	Sth	6.19867e-20	0.14
MIXER_Q.MNCSLOn_3.m1	Sth	6.19867e-20	0.14
MIXER_Q.MNCSLOn_4.m1	Sth	6.19867e-20	0.14
MIXER_Q.MNCGLOn.m1	Sig	5.21744e-20	0.11
MIXER_Q.MNCGLOp.m1	Sig	5.21722e-20	0.11
MIXER_I.MNCGLOn.m1	Sig	4.69867e-20	0.10
MIXER_I.MNCGLOp.m1	Sig	4.69862e-20	0.10
/PIF_I	rn	2.02961e-20	0.04
GM_0.R0.r1	thermal	1.9614e-20	0.04
MIXER_Q.RCGn.r1	thermal	1.76082e-20	0.04
MIXER_Q.RCGp.r1	thermal	1.76071e-20	0.04
GM_0.MPCS.m1	Sig	1.411e-20	0.03
MIXER_I.MNCGLOp.m1	Sfl	1.39715e-20	0.03
MIXER_I.MNCGLOn.m1	Sfl	1.39706e-20	0.03

Spot Noise Summary (in V^2/Hz) at 1G Hz Sorted By Noise Contributors
Total Summarized Noise = 4.56453e-17
Total Input Referred Noise = 1.63331e-18
The above noise summary info is for pnoise data

thermal noise CG switching MOSts I-Mixer: 24 %

thermal noise CG-load resistors I-Mixer: 24 %

thermal noise CG switching MOSts Q-Mixer: 6 %

thermal noise CG & CS MOSt of Gm stage: 6 %

thermal noise CS switching MOSts I-mixer: 10 %

Appendix E: Noise summaries BLIXER driven with buffered VCO

1. Noise summary of mixer at IF = 10 kHz driven with buffered VCO

Device	Param	Noise Contribution	% Of Total
XCP.MN2.m1	Sfl	7.64248e-15	29.67
XCP.MN1.m1	Sfl	7.58646e-15	29.45
/XCP/Rp	rn	2.75901e-15	10.71
MIXER_I.MNCGLOp.m1	Sfl	1.42463e-15	5.53
MIXER_I.MNCGLOn.m1	Sfl	1.42427e-15	5.53
XCP.MN2.m1	Sth	1.22662e-15	4.76
XCP.MN1.m1	Sth	1.22643e-15	4.76
/RACcouple2	rn	3.7628e-16	1.46
/RACcouple1	rn	3.76191e-16	1.46
XCP.MN1.m1	Sig	1.84615e-16	0.72
XCP.MN2.m1	Sig	1.83706e-16	0.71
MIXER_I.MNCSLOp_1.m1	Sfl	1.24792e-16	0.48
MIXER_I.MNCSLOp_2.m1	Sfl	1.24792e-16	0.48
MIXER_I.MNCSLOp_3.m1	Sfl	1.24792e-16	0.48
MIXER_I.MNCSLOp_4.m1	Sfl	1.24792e-16	0.48
MIXER_I.MNCSLOn_1.m1	Sfl	1.24792e-16	0.48
MIXER_I.MNCSLOn_2.m1	Sfl	1.24792e-16	0.48
MIXER_I.MNCSLOn_3.m1	Sfl	1.24792e-16	0.48
MIXER_I.MNCSLOn_4.m1	Sfl	1.24792e-16	0.48
MIXER_Q.MNCGLOp.m1	Sfl	9.93788e-17	0.39
MIXER_Q.MNCGLOn.m1	Sfl	9.9358e-17	0.39
MIXER_I.RCSn.r1	flicker	2.10552e-17	0.08
MIXER_I.RCSp.r1	flicker	2.10489e-17	0.08
/PORTout	rn	1.50483e-17	0.06
/PORTin	rn	1.167e-17	0.05
MIXER_I.MNCGLOn.m1	Sth	8.66789e-18	0.03
MIXER_I.MNCGLOp.m1	Sth	8.66716e-18	0.03
MIXER_I.RCGp.r1	flicker	5.27608e-18	0.02
MIXER_I.RCGn.r1	flicker	5.26888e-18	0.02
MIXER_I.RCGp.r1	thermal	5.18894e-18	0.02
MIXER_I.RCGn.r1	thermal	5.1884e-18	0.02
MIXER_Q.MNCSLOp_1.m1	Sfl	2.42867e-18	0.01
MIXER_Q.MNCSLOp_2.m1	Sfl	2.42867e-18	0.01
MIXER_Q.MNCSLOp_3.m1	Sfl	2.42867e-18	0.01
MIXER_Q.MNCSLOp_4.m1	Sfl	2.42867e-18	0.01
MIXER_Q.MNCSLOn_1.m1	Sfl	2.42806e-18	0.01
MIXER_Q.MNCSLOn_2.m1	Sfl	2.42806e-18	0.01
MIXER_Q.MNCSLOn_3.m1	Sfl	2.42806e-18	0.01
MIXER_Q.MNCSLOn_4.m1	Sfl	2.42806e-18	0.01
GM_0.MNCS.m1	Sth	2.2478e-18	0.01

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Summarized Noise = 2.57566e-14
Total Input Referred Noise = 8.86339e-16
The above noise summary info is for pnoise data

1/f noise XCP: 59 %

thermal noise Rp: 11 %

1/f noise CG switching MOSts I-Mixer: 11 %

thermal noise XCP: 10 %

AC-coupling resistors: 3 %

1/f noise CS switching MOSts I-mixer: 4 %

2. Noise summary of mixer at IF = 100 kHz driven with buffered VCO

Device	Param	Noise Contribution	% Of Total
/RACcouple2	rn	3.53443e-16	27.98
/RACcouple1	rn	3.53353e-16	27.97
MIXER_I.MNCGLOp.m1	Sfl	1.42464e-16	11.28
MIXER_I.MNCGLOn.m1	Sfl	1.42429e-16	11.27
/XCP/Rp	rn	2.76305e-17	2.19
/PORTout	rn	1.41358e-17	1.12
MIXER_I.MNCSLOp_1.m1	Sfl	1.24793e-17	0.99
MIXER_I.MNCSLOp_2.m1	Sfl	1.24793e-17	0.99
MIXER_I.MNCSLOp_3.m1	Sfl	1.24793e-17	0.99
MIXER_I.MNCSLOp_4.m1	Sfl	1.24793e-17	0.99
MIXER_I.MNCSLOn_1.m1	Sfl	1.24793e-17	0.99
MIXER_I.MNCSLOn_2.m1	Sfl	1.24793e-17	0.99
MIXER_I.MNCSLOn_3.m1	Sfl	1.24793e-17	0.99
MIXER_I.MNCSLOn_4.m1	Sfl	1.24793e-17	0.99
XCP.MN2.m1	Sth	1.23218e-17	0.98
XCP.MN1.m1	Sth	1.23198e-17	0.98
/PORTin	rn	1.167e-17	0.92
MIXER_Q.MNCGLOp.m1	Sfl	9.93813e-18	0.79
MIXER_Q.MNCGLOn.m1	Sfl	9.93604e-18	0.79
MIXER_I.MNCGLOn.m1	Sth	8.66789e-18	0.69
MIXER_I.MNCGLOp.m1	Sth	8.66716e-18	0.69
XCP.MN2.m1	Sfl	7.73385e-18	0.61
XCP.MN1.m1	Sfl	7.67818e-18	0.61
MIXER_I.RCGp.r1	thermal	5.18894e-18	0.41
MIXER_I.RCGn.r1	thermal	5.1884e-18	0.41
GM_0.MNCS.m1	Sth	2.2478e-18	0.18
MIXER_I.RCSn.r1	flicker	2.10552e-18	0.17
MIXER_I.RCSp.r1	flicker	2.10489e-18	0.17
XCP.MN1.m1	Sig	1.85059e-18	0.15
XCP.MN2.m1	Sig	1.84148e-18	0.15
GM_0.MPCS.m1	Sth	1.27715e-18	0.10
MIXER_Q.MNCGLOp.m1	Sth	1.25218e-18	0.10
MIXER_Q.MNCGLOn.m1	Sth	1.2519e-18	0.10
MIXER_I.RCSp.r1	thermal	1.19257e-18	0.09
MIXER_I.RCSn.r1	thermal	1.19233e-18	0.09
/R_BPF	rn	1.09814e-18	0.09
MIXER_I.MNCSLOn_1.m1	Sth	1.07254e-18	0.08
MIXER_I.MNCSLOn_2.m1	Sth	1.07254e-18	0.08
MIXER_I.MNCSLOn_3.m1	Sth	1.07254e-18	0.08
MIXER_I.MNCSLOn_4.m1	Sth	1.07254e-18	0.08

Spot Noise Summary (in V^2/Hz) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 1.2634e-15
Total Input Referred Noise = 4.34742e-17
The above noise summary info is for pnoise data

AC-coupling resistors: 56 %

1/f noise CG switching MOSts I-Mixer: 23 %

thermal noise Rp: 2 %

1/f noise CS switching MOSts I-mixer: 8 %

thermal noise XCP: 2 %

3. Noise summary of mixer at IF = 1 MHz driven with buffered VCO

Device	Param	Noise Contribution	% Of Total
/RACcouple2	rn	2.76844e-16	41.59
/RACcouple1	rn	2.76773e-16	41.58
MIXER_I.MNCGLOp.m1	Sfl	1.4248e-17	2.14
MIXER_I.MNCGLOn.m1	Sfl	1.42445e-17	2.14
/PORTin	rn	1.167e-17	1.75
/PORTout	rn	1.10722e-17	1.66
MIXER_I.MNCGLOn.m1	Sth	8.66789e-18	1.30
MIXER_I.MNCGLOp.m1	Sth	8.66715e-18	1.30
MIXER_I.RCGp.r1	thermal	5.18894e-18	0.78
MIXER_I.RCGn.r1	thermal	5.1884e-18	0.78
GM_0.MNCS.m1	Sth	2.2478e-18	0.34
GM_0.MPCS.m1	Sth	1.27715e-18	0.19
MIXER_Q.MNCGLOp.m1	Sth	1.25218e-18	0.19
MIXER_Q.MNCGLOn.m1	Sth	1.2519e-18	0.19
MIXER_I.MNCSLOp_1.m1	Sfl	1.24812e-18	0.19
MIXER_I.MNCSLOp_2.m1	Sfl	1.24812e-18	0.19
MIXER_I.MNCSLOp_3.m1	Sfl	1.24812e-18	0.19
MIXER_I.MNCSLOp_4.m1	Sfl	1.24812e-18	0.19
MIXER_I.MNCSLOn_1.m1	Sfl	1.24812e-18	0.19
MIXER_I.MNCSLOn_2.m1	Sfl	1.24812e-18	0.19
MIXER_I.MNCSLOn_3.m1	Sfl	1.24812e-18	0.19
MIXER_I.MNCSLOn_4.m1	Sfl	1.24812e-18	0.19
MIXER_I.RCSp.r1	thermal	1.19257e-18	0.18
MIXER_I.RCSn.r1	thermal	1.19233e-18	0.18
/R_BPF	rn	1.09814e-18	0.16
MIXER_I.MNCSLOn_1.m1	Sth	1.07253e-18	0.16
MIXER_I.MNCSLOn_2.m1	Sth	1.07253e-18	0.16
MIXER_I.MNCSLOn_3.m1	Sth	1.07253e-18	0.16
MIXER_I.MNCSLOn_4.m1	Sth	1.07253e-18	0.16
MIXER_I.MNCSLOp_1.m1	Sth	1.07247e-18	0.16
MIXER_I.MNCSLOp_2.m1	Sth	1.07247e-18	0.16
MIXER_I.MNCSLOp_3.m1	Sth	1.07247e-18	0.16
MIXER_I.MNCSLOp_4.m1	Sth	1.07247e-18	0.16
MIXER_Q.MNCGLOp.m1	Sfl	9.94062e-19	0.15
MIXER_Q.MNCGLOn.m1	Sfl	9.93853e-19	0.15
GM_0.MNCG.m1	Sth	6.45644e-19	0.10
/XCP/Rp	rn	3.16621e-19	0.05
MIXER_I.RCSn.r1	flicker	2.10552e-19	0.03
MIXER_I.RCSp.r1	flicker	2.10489e-19	0.03
XCP.MN2.m1	Sth	1.78811e-19	0.03

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 6.65665e-16
Total Input Referred Noise = 2.28956e-17
The above noise summary info is for pnoise data

AC-coupling resistors: 84 %

1/f noise CG switching MOSts I-Mixer: 4 %

thermal noise CG switching MOSts I-Mixer: 3 %

thermal noise CG-load resistors I-Mixer: 2 %

4. Noise summary of mixer at IF = 10 MHz driven with buffered VCO

Device	Param	Noise Contribution	% Of Total
/RACcouple2	rn	1.22396e-17	13.87
/RACcouple1	rn	1.22365e-17	13.86
/PORTin	rn	1.16692e-17	13.22
MIXER_I.MNCGLOn.m1	Sth	8.66738e-18	9.82
MIXER_I.MNCGLOp.m1	Sth	8.66666e-18	9.82
MIXER_I.RCGp.r1	thermal	5.18883e-18	5.88
MIXER_I.RCGn.r1	thermal	5.1883e-18	5.88
GM_0.MNCS.m1	Sth	2.24758e-18	2.55
MIXER_I.MNCGLOp.m1	Sfl	1.4263e-18	1.62
MIXER_I.MNCGLOn.m1	Sfl	1.42594e-18	1.62
GM_0.MPCS.m1	Sth	1.27703e-18	1.45
MIXER_Q.MNCGLOp.m1	Sth	1.2522e-18	1.42
MIXER_Q.MNCGLOn.m1	Sth	1.25192e-18	1.42
MIXER_I.RCSp.r1	thermal	1.19246e-18	1.35
MIXER_I.RCSn.r1	thermal	1.19222e-18	1.35
/R_BPF	rn	1.09808e-18	1.24
MIXER_I.MNCSLOn_1.m1	Sth	1.07242e-18	1.21
MIXER_I.MNCSLOn_2.m1	Sth	1.07242e-18	1.21
MIXER_I.MNCSLOn_3.m1	Sth	1.07242e-18	1.21
MIXER_I.MNCSLOn_4.m1	Sth	1.07242e-18	1.21
MIXER_I.MNCSLOp_1.m1	Sth	1.07235e-18	1.21
MIXER_I.MNCSLOp_2.m1	Sth	1.07235e-18	1.21
MIXER_I.MNCSLOp_3.m1	Sth	1.07235e-18	1.21
MIXER_I.MNCSLOp_4.m1	Sth	1.07235e-18	1.21
GM_0.MNCG.m1	Sth	6.45665e-19	0.73
/PORTout	rn	4.89366e-19	0.55
MIXER_I.MNCSLOn_1.m1	Sfl	1.24984e-19	0.14
MIXER_I.MNCSLOn_2.m1	Sfl	1.24984e-19	0.14
MIXER_I.MNCSLOn_3.m1	Sfl	1.24984e-19	0.14
MIXER_I.MNCSLOn_4.m1	Sfl	1.24984e-19	0.14
MIXER_I.MNCSLOp_1.m1	Sfl	1.24984e-19	0.14
MIXER_I.MNCSLOp_2.m1	Sfl	1.24984e-19	0.14
MIXER_I.MNCSLOp_3.m1	Sfl	1.24984e-19	0.14
MIXER_I.MNCSLOp_4.m1	Sfl	1.24984e-19	0.14
MIXER_Q.MNCGLOp.m1	Sfl	9.96598e-20	0.11
MIXER_Q.MNCGLOn.m1	Sfl	9.96379e-20	0.11
MIXER_Q.RCGn.r1	thermal	9.1196e-20	0.10
MIXER_Q.RCGp.r1	thermal	9.10642e-20	0.10
MIXER_Q.RCSn.r1	thermal	7.22111e-20	0.08
MIXER_Q.RCSp.r1	thermal	7.21188e-20	0.08

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 8.82675e-17
Total Input Referred Noise = 3.02252e-18
The above noise summary info is for pnoise data

AC-coupling resistors: 28 %

thermal noise CG switching MOSts I-Mixer: 20 %

thermal noise CG-load resistors I-Mixer: 12 %

1/f noise CG switching MOSts I-Mixer: 3 %

thermal noise CG switching MOSts Q-Mixer: 3 %

thermal noise CS-load resistors I-Mixer: 3 %

thermal noise CS switching MOSts I-mixer: 10 %

5. Noise summary of mixer at IF = 100 MHz driven with buffered VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	1.15931e-17	19.48
MIXER_I.MNCGLOn.m1	Sth	8.61746e-18	14.48
MIXER_I.MNCGLOp.m1	Sth	8.61675e-18	14.48
MIXER_I.RCGp.r1	thermal	5.17783e-18	8.70
MIXER_I.RCGn.r1	thermal	5.17731e-18	8.70
GM_0.MNCS.m1	Sth	2.22588e-18	3.74
GM_0.MPCS.m1	Sth	1.26476e-18	2.13
MIXER_Q.MNCGLOp.m1	Sth	1.25401e-18	2.11
MIXER_Q.MNCGLOn.m1	Sth	1.25372e-18	2.11
MIXER_I.RCSp.r1	thermal	1.18138e-18	1.99
MIXER_I.RCSn.r1	thermal	1.18115e-18	1.99
/R_BPF	rn	1.09206e-18	1.84
MIXER_I.MNCSLOn_1.m1	Sth	1.06069e-18	1.78
MIXER_I.MNCSLOn_2.m1	Sth	1.06069e-18	1.78
MIXER_I.MNCSLOn_3.m1	Sth	1.06069e-18	1.78
MIXER_I.MNCSLOn_4.m1	Sth	1.06069e-18	1.78
MIXER_I.MNCSLOp_1.m1	Sth	1.06062e-18	1.78
MIXER_I.MNCSLOp_2.m1	Sth	1.06062e-18	1.78
MIXER_I.MNCSLOp_3.m1	Sth	1.06062e-18	1.78
MIXER_I.MNCSLOp_4.m1	Sth	1.06062e-18	1.78
GM_0.MNCG.m1	Sth	6.47783e-19	1.09
MIXER_I.MNCGLOp.m1	Sfl	1.43395e-19	0.24
MIXER_I.MNCGLOn.m1	Sfl	1.43359e-19	0.24
/RACcouple2	rn	1.2996e-19	0.22
/RACcouple1	rn	1.29922e-19	0.22
MIXER_Q.RCGn.r1	thermal	9.06218e-20	0.15
MIXER_Q.RCGp.r1	thermal	9.04911e-20	0.15
MIXER_Q.RCSn.r1	thermal	7.08954e-20	0.12
MIXER_Q.RCSp.r1	thermal	7.08062e-20	0.12
XCP.MN2.m1	Sth	5.56747e-20	0.09
XCP.MN1.m1	Sth	5.56601e-20	0.09
MIXER_I.MNCGLOn.m1	Sig	4.99226e-20	0.08
MIXER_I.MNCGLOp.m1	Sig	4.98531e-20	0.08
MIXER_Q.MNCGLOn.m1	Sig	4.85633e-20	0.08
MIXER_Q.MNCGLOp.m1	Sig	4.84207e-20	0.08
/XCP/Rp	rn	4.03672e-20	0.07
MIXER_Q.MNCSLOp_1.m1	Sth	2.77756e-20	0.05
MIXER_Q.MNCSLOp_2.m1	Sth	2.77756e-20	0.05
MIXER_Q.MNCSLOp_3.m1	Sth	2.77756e-20	0.05
MIXER_Q.MNCSLOp_4.m1	Sth	2.77756e-20	0.05

Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 5.94999e-17
Total Input Referred Noise = 1.96336e-18
The above noise summary info is for pnoise data

thermal noise CG switching MOSts I-Mixer: 29 %

thermal noise CG-load resistors I-Mixer: 17 %

thermal noise CG & CS MOSt of Gm stage: 6 %

thermal noise CG switching MOSts Q-Mixer: 4 %

thermal noise CS-load resistors I-Mixer: 4 %

thermal noise CS switching MOSts I-mixer: 14 %

6. Noise summary of mixer at IF = 1 GHz driven with buffered VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	7.02522e-18	18.67
MIXER_I.MNCGLOn.m1	Sth	5.58133e-18	14.83
MIXER_I.MNCGLOp.m1	Sth	5.5808e-18	14.83
MIXER_I.RCGp.r1	thermal	4.0937e-18	10.88
MIXER_I.RCGn.r1	thermal	4.0936e-18	10.88
MIXER_Q.MNCGLOp.m1	Sth	1.14222e-18	3.04
MIXER_Q.MNCGLOn.m1	Sth	1.14208e-18	3.03
GM_0.MNCS.m1	Sth	1.08586e-18	2.89
GM_0.MNCG.m1	Sth	7.15122e-19	1.90
/R_BPF	rn	7.09481e-19	1.89
GM_0.MPCS.m1	Sth	6.19054e-19	1.65
MIXER_I.RCSp.r1	thermal	5.86141e-19	1.56
MIXER_I.RCSn.r1	thermal	5.86066e-19	1.56
MIXER_I.MNCSLOn_1.m1	Sth	4.82703e-19	1.28
MIXER_I.MNCSLOn_2.m1	Sth	4.82703e-19	1.28
MIXER_I.MNCSLOn_3.m1	Sth	4.82703e-19	1.28
MIXER_I.MNCSLOn_4.m1	Sth	4.82703e-19	1.28
MIXER_I.MNCSLOp_1.m1	Sth	4.82641e-19	1.28
MIXER_I.MNCSLOp_2.m1	Sth	4.82641e-19	1.28
MIXER_I.MNCSLOp_3.m1	Sth	4.82641e-19	1.28
MIXER_I.MNCSLOp_4.m1	Sth	4.82641e-19	1.28
MIXER_Q.RCGn.r1	thermal	5.05681e-20	0.13
MIXER_Q.RCGp.r1	thermal	5.04941e-20	0.13
MIXER_Q.MNCSLOp_1.m1	Sth	4.0019e-20	0.11
MIXER_Q.MNCSLOp_2.m1	Sth	4.0019e-20	0.11
MIXER_Q.MNCSLOp_3.m1	Sth	4.0019e-20	0.11
MIXER_Q.MNCSLOp_4.m1	Sth	4.0019e-20	0.11
MIXER_Q.MNCSLOn_1.m1	Sth	4.00067e-20	0.11
MIXER_Q.MNCSLOn_2.m1	Sth	4.00067e-20	0.11
MIXER_Q.MNCSLOn_3.m1	Sth	4.00067e-20	0.11
MIXER_Q.MNCSLOn_4.m1	Sth	4.00067e-20	0.11
MIXER_Q.MNCGLOn.m1	Sig	3.61232e-20	0.10
MIXER_Q.MNCGLOp.m1	Sig	3.6002e-20	0.10
MIXER_I.MNCGLOn.m1	Sig	3.2436e-20	0.09
MIXER_I.MNCGLOp.m1	Sig	3.23718e-20	0.09
XCP.MN1.m1	Sth	3.10754e-20	0.08
XCP.MN2.m1	Sth	3.10409e-20	0.08
/XCP/Rp	rn	1.98402e-20	0.05
MIXER_Q.RCSn.r1	thermal	1.96281e-20	0.05
MIXER_Q.RCSp.r1	thermal	1.96013e-20	0.05

Spot Noise Summary (in V^2/Hz) at 1G Hz Sorted By Noise Contributors
Total Summarized Noise = 3.76316e-17
Total Input Referred Noise = 1.65354e-18
The above noise summary info is for pnoise data

thermal noise CG switching MOSts I-Mixer: 30 %

thermal noise CG-load resistors I-Mixer: 22 %

thermal noise CG switching MOSts I-Mixer: 6 %

thermal noise CG & CS MOSt of Gm stage: 5 %

thermal noise CS switching MOSts I-mixer: 10 %

Appendix F: Noise summaries BLIXER driven with VCO

1. Noise summary of mixer at IF = 10kHz driven with bufferless VCO

Device	Param	Noise Contribution	% Of Total
GM_0.MN0.m1	Sfl	7.53437e-15	41.16
MIXER_I.MNCGL0p.m1	Sfl	1.98247e-15	10.83
MIXER_I.MNCGL0n.m1	Sfl	1.98229e-15	10.83
/RACcouple2	rn	4.65256e-16	2.54
/RACcouple1	rn	4.65196e-16	2.54
MIXER_I.MNCSL0n_1.m1	Sig	3.84185e-16	2.10
MIXER_I.MNCSL0n_2.m1	Sig	3.84185e-16	2.10
MIXER_I.MNCSL0n_3.m1	Sig	3.84185e-16	2.10
MIXER_I.MNCSL0n_4.m1	Sig	3.84185e-16	2.10
MIXER_I.MNCSL0p_1.m1	Sig	3.84123e-16	2.10
MIXER_I.MNCSL0p_2.m1	Sig	3.84123e-16	2.10
MIXER_I.MNCSL0p_3.m1	Sig	3.84123e-16	2.10
MIXER_I.MNCSL0p_4.m1	Sig	3.84123e-16	2.10
GM_0.MNCS.m1	Sfl	3.38813e-16	1.85
GM_0.MP1.m1	Sfl	2.72314e-16	1.49
GM_0.MN4.m1	Sfl	1.55604e-16	0.85
MIXER_I.MNCSL0n_1.m1	Sfl	1.39937e-16	0.76
MIXER_I.MNCSL0n_2.m1	Sfl	1.39937e-16	0.76
MIXER_I.MNCSL0n_3.m1	Sfl	1.39937e-16	0.76
MIXER_I.MNCSL0n_4.m1	Sfl	1.39937e-16	0.76
MIXER_I.MNCSL0p_1.m1	Sfl	1.39916e-16	0.76
MIXER_I.MNCSL0p_2.m1	Sfl	1.39916e-16	0.76
MIXER_I.MNCSL0p_3.m1	Sfl	1.39916e-16	0.76
MIXER_I.MNCSL0p_4.m1	Sfl	1.39916e-16	0.76
MIXER_I.MNCGL0n.m1	Sig	1.22087e-16	0.67
MIXER_I.MNCGL0p.m1	Sig	1.22068e-16	0.67
MIXER_Q.MNCGL0n.m1	Sfl	7.01343e-17	0.38
MIXER_Q.MNCGL0p.m1	Sfl	7.01074e-17	0.38
GM_0.R0.r1	thermal	5.90758e-17	0.32
GM_0.MN2.m1	Sfl	5.78282e-17	0.32
GM_0.MN3.m1	Sfl	5.50266e-17	0.30
GM_0.MNCG.m1	Sfl	3.89053e-17	0.21
GM_0.MP0.m1	Sfl	3.87397e-17	0.21
GM_0.MN1.m1	Sfl	3.46409e-17	0.19
MIXER_I.RCSp.r1	flicker	2.32423e-17	0.13
MIXER_I.RCSn.r1	flicker	2.32378e-17	0.13
GM_0.R3.r1	thermal	1.93391e-17	0.11
/PORTout	rn	1.81625e-17	0.10
/PORTin	rn	1.36663e-17	0.07
GM_0.MP2.m1	Sfl	1.35585e-17	0.07

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Summarized Noise = 1.83048e-14
Total Input Referred Noise = 5.3694e-16
The above noise summary info is for pnoise data

1/f noise biasing Gm-stage: 41 %

1/f noise CG switching MOSts I-Mixer: 22 %

AC-coupling resistors: 5 %

induced gate noise switching MOSts: 18 %

1/f noise CS switching MOSts I-mixer: 6 %

2. Noise summary of mixer at IF = 100 kHz driven with bufferless VCO

Device	Param	Noise Contribution	% Of Total
/RACcouple2	rn	4.52657e-16	9.51
/RACcouple1	rn	4.52596e-16	9.51
MIXER_I.MNCSLOn_1.m1	Sig	3.73604e-16	7.85
MIXER_I.MNCSLOn_2.m1	Sig	3.73604e-16	7.85
MIXER_I.MNCSLOn_3.m1	Sig	3.73604e-16	7.85
MIXER_I.MNCSLOn_4.m1	Sig	3.73604e-16	7.85
MIXER_I.MNCSLOp_1.m1	Sig	3.73542e-16	7.85
MIXER_I.MNCSLOp_2.m1	Sig	3.73542e-16	7.85
MIXER_I.MNCSLOp_3.m1	Sig	3.73542e-16	7.85
MIXER_I.MNCSLOp_4.m1	Sig	3.73542e-16	7.85
MIXER_I.MNCGLOp.m1	Sfl	1.98238e-16	4.17
MIXER_I.MNCGLOn.m1	Sfl	1.9822e-16	4.17
MIXER_I.MNCGLOn.m1	Sig	1.1872e-16	2.49
MIXER_I.MNCGLOp.m1	Sig	1.18701e-16	2.49
/PORTout	rn	1.81005e-17	0.38
MIXER_I.MNCSLOn_1.m1	Sfl	1.39681e-17	0.29
MIXER_I.MNCSLOn_2.m1	Sfl	1.39681e-17	0.29
MIXER_I.MNCSLOn_3.m1	Sfl	1.39681e-17	0.29
MIXER_I.MNCSLOn_4.m1	Sfl	1.39681e-17	0.29
MIXER_I.MNCSLOp_1.m1	Sfl	1.3966e-17	0.29
MIXER_I.MNCSLOp_2.m1	Sfl	1.3966e-17	0.29
MIXER_I.MNCSLOp_3.m1	Sfl	1.3966e-17	0.29
MIXER_I.MNCSLOp_4.m1	Sfl	1.3966e-17	0.29
/PORTin	rn	1.36594e-17	0.29
MIXER_I.MNCGLOp.m1	Sth	1.02139e-17	0.21
MIXER_I.MNCGLOn.m1	Sth	1.02135e-17	0.21
GM_0.MN0.m1	Sfl	7.53177e-18	0.16
MIXER_Q.MNCGLOn.m1	Sfl	6.96785e-18	0.15
MIXER_Q.MNCGLOp.m1	Sfl	6.96513e-18	0.15
MIXER_I.RCGp.r1	thermal	5.63011e-18	0.12
MIXER_I.RCGn.r1	thermal	5.63009e-18	0.12
GM_0.MNCS.m1	Sth	3.19393e-18	0.07
MIXER_I.RCSp.r1	flicker	2.31814e-18	0.05
MIXER_I.RCSn.r1	flicker	2.31772e-18	0.05
GM_0.MPCS.m1	Sth	1.79812e-18	0.04
MIXER_I.RCSp.r1	thermal	1.39681e-18	0.03
MIXER_I.RCSn.r1	thermal	1.39658e-18	0.03
/R_BPF	rn	1.28477e-18	0.03
MIXER_Q.MNCGLOn.m1	Sth	1.284e-18	0.03
MIXER_Q.MNCGLOp.m1	Sth	1.2839e-18	0.03

Spot Noise Summary (in V^2/Hz) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 4.75889e-15
Total Input Referred Noise = 1.39567e-16
The above noise summary info is for pnoise data

AC-coupling resistors: 19 %

induced gate noise switching MOSts: 68 %

1/f noise CG switching MOSts I-Mixer: 8 %

1/f noise CS switching MOSts I-Mixer: 2 %

3. Noise summary of mixer at IF = 1 MHz driven with bufferless VCO

Device	Param	Noise Contribution	% Of Total
/RACcouple2	rn	3.37855e-16	10.50
/RACcouple1	rn	3.3778e-16	10.50
MIXER_I.MNCSLOn_1.m1	Sig	2.78851e-16	8.67
MIXER_I.MNCSLOn_2.m1	Sig	2.78851e-16	8.67
MIXER_I.MNCSLOn_3.m1	Sig	2.78851e-16	8.67
MIXER_I.MNCSLOn_4.m1	Sig	2.78851e-16	8.67
MIXER_I.MNCSLOp_1.m1	Sig	2.78781e-16	8.66
MIXER_I.MNCSLOp_2.m1	Sig	2.78781e-16	8.66
MIXER_I.MNCSLOp_3.m1	Sig	2.78781e-16	8.66
MIXER_I.MNCSLOp_4.m1	Sig	2.78781e-16	8.66
MIXER_I.MNCGLOn.m1	Sig	8.86267e-17	2.75
MIXER_I.MNCGLOp.m1	Sig	8.86047e-17	2.75
MIXER_I.MNCGLOp.m1	Sfl	1.97439e-17	0.61
MIXER_I.MNCGLOn.m1	Sfl	1.97422e-17	0.61
/PORTout	rn	1.35126e-17	0.42
/PORTin	rn	1.34733e-17	0.42
MIXER_I.MNCGLOp.m1	Sth	1.01694e-17	0.32
MIXER_I.MNCGLOn.m1	Sth	1.01691e-17	0.32
MIXER_I.RCGp.r1	thermal	5.64775e-18	0.18
MIXER_I.RCGn.r1	thermal	5.64772e-18	0.18
GM_0.MNCS.m1	Sth	3.10712e-18	0.10
GM_0.MPCS.m1	Sth	1.75006e-18	0.05
MIXER_I.MNCSLOn_1.m1	Sfl	1.36882e-18	0.04
MIXER_I.MNCSLOn_2.m1	Sfl	1.36882e-18	0.04
MIXER_I.MNCSLOn_3.m1	Sfl	1.36882e-18	0.04
MIXER_I.MNCSLOn_4.m1	Sfl	1.36882e-18	0.04
MIXER_I.MNCSLOp_1.m1	Sfl	1.36867e-18	0.04
MIXER_I.MNCSLOp_2.m1	Sfl	1.36867e-18	0.04
MIXER_I.MNCSLOp_3.m1	Sfl	1.36867e-18	0.04
MIXER_I.MNCSLOp_4.m1	Sfl	1.36867e-18	0.04
MIXER_I.RCSp.r1	thermal	1.36469e-18	0.04
MIXER_I.RCSn.r1	thermal	1.36448e-18	0.04
MIXER_Q.MNCGLOn.m1	Sth	1.28151e-18	0.04
MIXER_Q.MNCGLOp.m1	Sth	1.28141e-18	0.04
/R_BPF	rn	1.26724e-18	0.04
MIXER_I.MNCSLOn_1.m1	Sth	1.18685e-18	0.04
MIXER_I.MNCSLOn_2.m1	Sth	1.18685e-18	0.04
MIXER_I.MNCSLOn_3.m1	Sth	1.18685e-18	0.04
MIXER_I.MNCSLOn_4.m1	Sth	1.18685e-18	0.04
MIXER_I.MNCSLOp_4.m1	Sth	1.18661e-18	0.04

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 3.21741e-15
Total Input Referred Noise = 9.53892e-17
The above noise summary info is for pnoise data

AC-coupling resistors: 21 %

Induced gate noise switching MOSts: 75 %

4. Noise summary of mixer at IF = 10 MHz driven with bufferless VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	1.29454e-17	6.86
/RACcouple2	rn	1.28259e-17	6.80
/RACcouple1	rn	1.28197e-17	6.79
MIXER_I.MNCSLOn_1.m1	Sig	1.0594e-17	5.61
MIXER_I.MNCSLOn_2.m1	Sig	1.0594e-17	5.61
MIXER_I.MNCSLOn_3.m1	Sig	1.0594e-17	5.61
MIXER_I.MNCSLOn_4.m1	Sig	1.0594e-17	5.61
MIXER_I.MNCSLOp_1.m1	Sig	1.05886e-17	5.61
MIXER_I.MNCSLOp_2.m1	Sig	1.05886e-17	5.61
MIXER_I.MNCSLOp_3.m1	Sig	1.05886e-17	5.61
MIXER_I.MNCSLOp_4.m1	Sig	1.05886e-17	5.61
MIXER_I.MNCGLOp.m1	Sth	1.0043e-17	5.32
MIXER_I.MNCGLOn.m1	Sth	1.00428e-17	5.32
MIXER_I.RCGp.r1	thermal	5.69767e-18	3.02
MIXER_I.RCGn.r1	thermal	5.69762e-18	3.02
MIXER_I.MNCGLOn.m1	Sig	3.42747e-18	1.82
MIXER_I.MNCGLOp.m1	Sig	3.42575e-18	1.82
GM_0.MNCS.m1	Sth	2.86376e-18	1.52
MIXER_I.MNCGLOp.m1	Sfl	1.95303e-18	1.03
MIXER_I.MNCGLOn.m1	Sfl	1.95291e-18	1.03
GM_0.MPCS.m1	Sth	1.61384e-18	0.86
MIXER_Q.MNCGLOn.m1	Sth	1.27457e-18	0.68
MIXER_Q.MNCGLOp.m1	Sth	1.27446e-18	0.68
MIXER_I.RCSp.r1	thermal	1.27406e-18	0.68
MIXER_I.RCSn.r1	thermal	1.27399e-18	0.68
/R_BPF	rn	1.21759e-18	0.65
MIXER_I.MNCSLOn_1.m1	Sth	1.11663e-18	0.59
MIXER_I.MNCSLOn_2.m1	Sth	1.11663e-18	0.59
MIXER_I.MNCSLOn_3.m1	Sth	1.11663e-18	0.59
MIXER_I.MNCSLOn_4.m1	Sth	1.11663e-18	0.59
MIXER_I.MNCSLOp_1.m1	Sth	1.11659e-18	0.59
MIXER_I.MNCSLOp_2.m1	Sth	1.11659e-18	0.59
MIXER_I.MNCSLOp_3.m1	Sth	1.11659e-18	0.59
MIXER_I.MNCSLOp_4.m1	Sth	1.11659e-18	0.59
GM_0.MNCG.m1	Sth	6.64494e-19	0.35
/PORTout	rn	5.12844e-19	0.27
MIXER_I.MNCSLOp_1.m1	Sfl	1.29069e-19	0.07
MIXER_I.MNCSLOp_2.m1	Sfl	1.29069e-19	0.07
MIXER_I.MNCSLOp_3.m1	Sfl	1.29069e-19	0.07
MIXER_I.MNCSLOp_4.m1	Sfl	1.29069e-19	0.07

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.88716e-16
Total Input Referred Noise = 5.80731e-18
The above noise summary info is for pnoise data

AC-coupling resistors: 14 %

Induced gate noise switching MOSts: 49 %

thermal noise CG switching MOSts I-Mixer: 11 %

thermal noise CG-load resistors I-Mixer: 22 %

5. Noise summary of mixer at IF = 100 MHz driven with bufferless VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	1.28278e-17	19.07
MIXER_I.MNCGLOp.m1	Sth	9.97707e-18	14.84
MIXER_I.MNCGLOn.m1	Sth	9.97687e-18	14.84
MIXER_I.RCGp.r1	thermal	5.68414e-18	8.45
MIXER_I.RCGn.r1	thermal	5.68409e-18	8.45
GM_0.MNCS.m1	Sth	2.82293e-18	4.20
GM_0.MPCS.m1	Sth	1.59095e-18	2.37
MIXER_Q.MNCGLOn.m1	Sth	1.27676e-18	1.90
MIXER_Q.MNCGLOp.m1	Sth	1.27665e-18	1.90
MIXER_I.RCSp.r1	thermal	1.25861e-18	1.87
MIXER_I.RCSn.r1	thermal	1.25855e-18	1.87
/R_BPF	rn	1.20777e-18	1.80
MIXER_I.MNCSLOn_1.m1	Sth	1.10145e-18	1.64
MIXER_I.MNCSLOn_2.m1	Sth	1.10145e-18	1.64
MIXER_I.MNCSLOn_3.m1	Sth	1.10145e-18	1.64
MIXER_I.MNCSLOn_4.m1	Sth	1.10145e-18	1.64
MIXER_I.MNCSLOp_1.m1	Sth	1.10142e-18	1.64
MIXER_I.MNCSLOp_2.m1	Sth	1.10142e-18	1.64
MIXER_I.MNCSLOp_3.m1	Sth	1.10142e-18	1.64
MIXER_I.MNCSLOp_4.m1	Sth	1.10142e-18	1.64
GM_0.MNCG.m1	Sth	6.71126e-19	1.00
MIXER_I.MNCGLOp.m1	Sfl	1.96016e-19	0.29
MIXER_I.MNCGLOn.m1	Sfl	1.96003e-19	0.29
/RACcouple2	rn	1.32989e-19	0.20
/RACcouple1	rn	1.32925e-19	0.20
MIXER_Q.RCGp.r1	thermal	1.19119e-19	0.18
MIXER_Q.RCGn.r1	thermal	1.19101e-19	0.18
MIXER_I.MNCSLOn_1.m1	Sig	1.18046e-19	0.18
MIXER_I.MNCSLOn_2.m1	Sig	1.18046e-19	0.18
MIXER_I.MNCSLOn_3.m1	Sig	1.18046e-19	0.18
MIXER_I.MNCSLOn_4.m1	Sig	1.18046e-19	0.18
MIXER_I.MNCSLOp_1.m1	Sig	1.1799e-19	0.18
MIXER_I.MNCSLOp_2.m1	Sig	1.1799e-19	0.18
MIXER_I.MNCSLOp_3.m1	Sig	1.1799e-19	0.18
MIXER_I.MNCSLOp_4.m1	Sig	1.1799e-19	0.18
MIXER_I.MNCGLOn.m1	Sig	9.98057e-20	0.15
MIXER_I.MNCGLOp.m1	Sig	9.97834e-20	0.15
MIXER_Q.RCSp.r1	thermal	9.54232e-20	0.14
MIXER_Q.RCSn.r1	thermal	9.54132e-20	0.14
MIXER_Q.MNCGLOp.m1	Sig	4.90178e-20	0.07

Spot Noise Summary (in V^2/Hz) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 6.72504e-17
Total Input Referred Noise = 2.00287e-18
The above noise summary info is for pnoise data

thermal noise CG switching MOSts I-Mixer: 30 %

thermal noise CG-load resistors I-Mixer: 17 %

thermal noise CG & CS MOSt of Gm stage: 6 %

thermal noise CG switching MOSts Q-Mixer: 4 %

thermal noise CS-load resistors I-Mixer: 4 %

thermal noise CS switching MOSts I-mixer: 13 %

AC-coupling resistors: 0.4 %

Induced gate noise switching MOSts: 2 %

6. Noise summary of mixer at IF = 1 GHz driven with bufferless VCO

Device	Param	Noise Contribution	% Of Total
/PORTin	rn	7.33246e-18	17.99
MIXER_I.MNCGLOp.m1	Sth	6.3152e-18	15.50
MIXER_I.MNCGLOn.m1	Sth	6.31511e-18	15.49
MIXER_I.RCGp.r1	thermal	4.34319e-18	10.66
MIXER_I.RCGn.r1	thermal	4.34316e-18	10.66
GM_0.MNCS.m1	Sth	1.26661e-18	3.11
MIXER_Q.MNCGLOn.m1	Sth	1.186e-18	2.91
MIXER_Q.MNCGLOp.m1	Sth	1.18594e-18	2.91
GM_0.MNCG.m1	Sth	8.6492e-19	2.12
/R_BPF	rn	7.41576e-19	1.82
GM_0.MPCS.m1	Sth	7.16372e-19	1.76
MIXER_I.RCSp.r1	thermal	6.24612e-19	1.53
MIXER_I.RCSn.r1	thermal	6.24598e-19	1.53
MIXER_I.MNCSLOn_1.m1	Sth	4.98465e-19	1.22
MIXER_I.MNCSLOn_2.m1	Sth	4.98465e-19	1.22
MIXER_I.MNCSLOn_3.m1	Sth	4.98465e-19	1.22
MIXER_I.MNCSLOn_4.m1	Sth	4.98465e-19	1.22
MIXER_I.MNCSLOp_1.m1	Sth	4.98455e-19	1.22
MIXER_I.MNCSLOp_2.m1	Sth	4.98455e-19	1.22
MIXER_I.MNCSLOp_3.m1	Sth	4.98455e-19	1.22
MIXER_I.MNCSLOp_4.m1	Sth	4.98455e-19	1.22
MIXER_Q.RCGp.r1	thermal	6.88439e-20	0.17
MIXER_Q.RCGn.r1	thermal	6.88307e-20	0.17
MIXER_Q.MNCSLOn_1.m1	Sth	4.83333e-20	0.12
MIXER_Q.MNCSLOn_2.m1	Sth	4.83333e-20	0.12
MIXER_Q.MNCSLOn_3.m1	Sth	4.83333e-20	0.12
MIXER_Q.MNCSLOn_4.m1	Sth	4.83333e-20	0.12
MIXER_Q.MNCSLOp_1.m1	Sth	4.83314e-20	0.12
MIXER_Q.MNCSLOp_2.m1	Sth	4.83314e-20	0.12
MIXER_Q.MNCSLOp_3.m1	Sth	4.83314e-20	0.12
MIXER_Q.MNCSLOp_4.m1	Sth	4.83314e-20	0.12
MIXER_I.MNCGLOn.m1	Sig	3.82071e-20	0.09
MIXER_I.MNCGLOp.m1	Sig	3.82044e-20	0.09
MIXER_Q.MNCGLOp.m1	Sig	3.67232e-20	0.09
MIXER_Q.MNCGLOn.m1	Sig	3.67228e-20	0.09
MIXER_Q.RCSp.r1	thermal	2.63967e-20	0.06
MIXER_Q.RCSn.r1	thermal	2.63935e-20	0.06
/XCP/Rp	rn	1.75952e-20	0.04
XCP.MN1.m1	Sth	1.69902e-20	0.04
XCP.MN2.m1	Sth	1.69891e-20	0.04

Spot Noise Summary (in V^2/Hz) at 1G Hz Sorted By Noise Contributors
Total Summarized Noise = 4.07558e-17
Total Input Referred Noise = 1.69391e-18
The above noise summary info is for pnoise data

thermal noise CG switching MOSts I-Mixer: 31 %

thermal noise CG-load resistors I-Mixer: 21 %

thermal noise CG switching MOSts I-Mixer: 6 %

thermal noise CG & CS MOSt of Gm stage: 5 %

thermal noise CS-load resistors I-Mixer: 3 %

thermal noise CS switching MOSts I-mixer: 10 %

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