# UNIVERSITEIT TWENTE.

# On the Modeling and Simulation of Novel Schottky Based Silicon Rectifiers

## Master Thesis

September 23, 2009
Report Number: 068.027/2009

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# Abstract

This report has been written in conclusion to a master's project in the Semiconductor Components group at the University of Twente. The topic is the DC (Direct Current) current voltage characteristic of both the aMSM- (asymmetric Metal Semiconductor Metal) and the CP- (Charge Plasma) diode. We will make a comparison by focusing on the modeling and simulation of both devices, after comparing those to experimental obtained from conventional vertical Schottky diodes. This report reflects the work which has been done during this project and allows the reader to understand the DC current voltage characteristics of the proposed diodes.

We present an analytical model for the IV characteristics of both diodes. This model is verified using the Synopsys device simulator. The model and the simulator show a good agreement. It was found that when one of the metal work functions is located much further away from silicon midgap then the other, then it is either the transport of holes or electrons which dominates the current. Both the on- and the off-current can be scaled independently from each other by scaling the n-metal gate and p-metal gate length.

An example is shown from which the metal work functions are extracted from experimental Schottky diode test structures. In this case proper scaling of both gate lengths can improve the on/off current ratio of the diode by a factor twenty. In another case work functions from literature were used, here the on/off current ratio couldn't be improved.

# Contents

# Chapter 1

# Introduction

The relentless scaling of the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices during the last decades has recently resulted in devices with gate lengths below 30 nm. These small dimensions have, amongst other things, resulted in serious fluctuations in the dopant concentration and location. An example of a possible variation of the threshold voltage in nano-scale MOSFET has recently been shown by Li et al. [1]. They show that a variation of few hundred $\mu$V in the threshold voltage can be expected. Also it becomes rather difficult to control the doping activation, which was shown by Ho et al. [2].

In recent years SOI (Silicon on Insulator) and FinFET (Fin Field Effect Transistor) devices have been investigated as alternative device architectures. These do not necessarily require doping. For instance Chiang et al. [3] showed that the background doping, or impurity concentration, still results in a significant variation of the device characteristics.

Alternatively Schottky based devices, such as Schottky-based MOSFETs thoroughly discussed by Larson & Snyder [4], can be used to eliminate the relevance of doping and corresponding problems altogether. However the Schottky barrier cannot be measured directly. In this case there are two metal (non-ohmic) contacts to the silicon. Conventional Schottky diodes are made with doped silicon. Depending on the type of doping either hole or electron transport dominates the current. In this case an ohmic contact can be made by one of the metals. When a very lowly doped semiconductor is used none of the contacts will be ohmic, hence an metal semiconductor metal structure is made where both interfaces influence the total current.

In 2005 Yang [5] presented a carbon nanotube Schottky diode with asymmetrical metal contacts. The word asymmetrical arises from the very different metal work functions. In 2008 an asymmetrical Schottky barrier diode on a NiGe semiconductor was presented by Ang et al. [6]. They named the device an MSM diode, hence we will use the word aMSM (asymmetrical Metal semiconductor Metal) diode to name these type of devices. Figure 1.1 (a) shows an example of the aMSM-diode.

An alternative to the Schottky based device is the charged plasma (CP) diode as presented by Rajasekharan et al. [7]. Here two separate gates are placed on top of a thin silicon body. The metallic gates are isolated from the top of the body by a dielectric. Each of the metals forms a contact at both sides of the silicon body. Figure 1.1 (b) shows the structure and band diagram for this device. Recently this diode has been investigated using device simulations by Hueting et al. [8]. They concluded that the device shows good rectifying behavior depending on the metal work functions of the gates and device dimensions.

While the current in the aMSM-diode only depends on the metal-semiconductor interface and hence it is expected that this type of diode does not allow for any scaling of the current by changing the device parameters except for the area. The current in the CP-diode is determined by the diffusion of carriers, hence it is expected that the current is dependent of both the metal-work function and the length of the gates. Therefore lithography can be used to scale the current through the device. In this report we will try to find the exact conditions under which the CP-diode is preferable.



(a) aMSM-diode                                                          (b) CP-diode
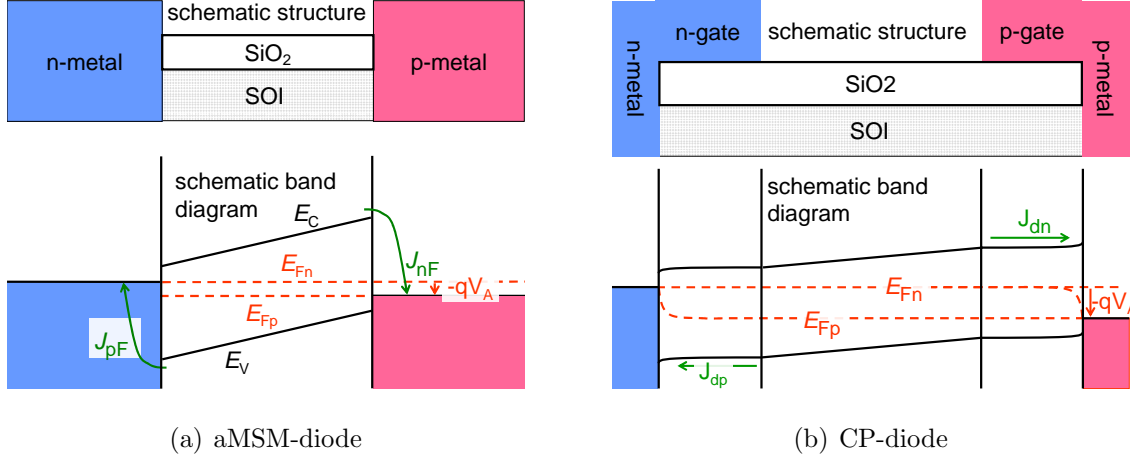
**Figure 1.1:** Schematic structure and schematic band diagram for small forward voltages for: (a) the aMSM-diode, where the current is determined by thermionic emission (their transport is indicated by $J_{nF}$ and $J_{pF}$) across the Schottky barriers and (b) the CP diode, where the current is determined by the diffusion ($J_{dn}$ and $J_{dp}$) of carriers under the gates.

## 1.1   Outline

The goal of this work is to make a good comparison of the CP- and the aMSM-diode. To do this it is necessary to derive a model for the currents in both devices to predict the scaling dependence of both devices. This model can be verified using a device simulator. If the model is accurate then the model can be used to compare the performance of a CP to an aMSM-diode. Both the CP-diode and aMSM-diode have not yet been modeled. Hence we will start this work with an experimental analysis of the DC-characteristics of a Schottky junction. Then we will show how this can be used to model the IV characteristics of an aMSM-diode. Also we will present a solution to the characteristics of a CP-diode by combining an electrostatical solution of a FinFET device and the usual diode equations. In the next section we will discuss how the electron and hole barrier heights of different metals can be extracted from measurements on Schottky diodes. These results will be used as parameter inputs for a device simulator. By comparing the measured and simulated characteristics we can verify the simulator and barrier height extraction method. Then we will discuss simulation and modeling results on both the CP- and aMSM-diode. First we will verify our models using simulations, then we will discuss how the CP-diode can be scaled and when a CP-diode is attractive compared to an aMSM-diode. Finally we

will draw conclusions from the modeling and simulation results. Also we will give a few recommendations for further work.

# Chapter 2

# Theory

In this section we will start with a discussion on the transport of carriers through Schottky junction diodes. Then we will show how this theory can be applied to derive the current equations of an aMSM diode. Finally we will present a model for the CP-diode.

## 2.1 Schottky Barriers

Since the beginning of the twentieth century metal semiconductor rectifiers have found practical applications. When a metal is brought into intimate contact with a semiconductor, this results in a potential barrier. In 1938 Schottky [9] suggested that this potential barrier could arise from stable space charges in the semiconductor. His model gave rise to the now well known thermionic emission theory. The transport processes are reviewed by Rhoderick and Williams [10] and Sze [11]. We will give a brief summary of Sze's explanation of the basic Schottky device behavior.

### 2.1.1 Energy Band Diagram

In figure 2.1 (a) a schematic band diagram of a metal and a semiconductor separated by a distance $d$ are shown. The metal Fermi level $E_{fm}$ indicates the level at which the occupancy of the states by electrons equals 0.5. Below this level the occupancy increases, and above it decreases. The distance between $E_{fm}$ and the vacuum level is given by $\phi_m$. $\phi_s$ indicates the silicon work function. The conduction band is indicated with $E_C$, the extrinsic Fermi level $E_F$, the intrinsic Fermi level $E_{FI}$ and the valence band $E_V$ are indicated in the same figure. The silicon electron affinity $\chi_{Si}$ is the distance between the vacuum level $E_{VAC}$ and the conduction band $E_C$. In figure (b) $d$ has been reduced to zero. Therefore the vacuum levels and the extrinsic Fermi levels have to align at the interface. Here a p-type metal is used, therefore all the electrons are pushed away from the metal, hence leaving positive dopant ions which are stuck to the silicon lattice. The charge is compensated by accumulated electrons in the metal layer. The positive charge of the depleted dopant atoms pulls the energy bands downward into the silicon. This continues until the Fermi level is constant. If a n-type metal was used it would be vice versa. The region depleted of electrons is usually called the depletion or space-charge region.

In this case the metal tends to attract holes to and repels electrons from the metal we will call this metal a p-metal. If a metal attracts electrons (or actually repels holes) we will call it a n-metal. Hence, when $\phi_m > \chi_{Si} + E_G/2$ we call it a p-metal. And when $\phi_m < \chi_{Si} + E_G/2$ the metal is an n-metal. Often Schottky contacts are characterized

(a) Separated
(b) Connected
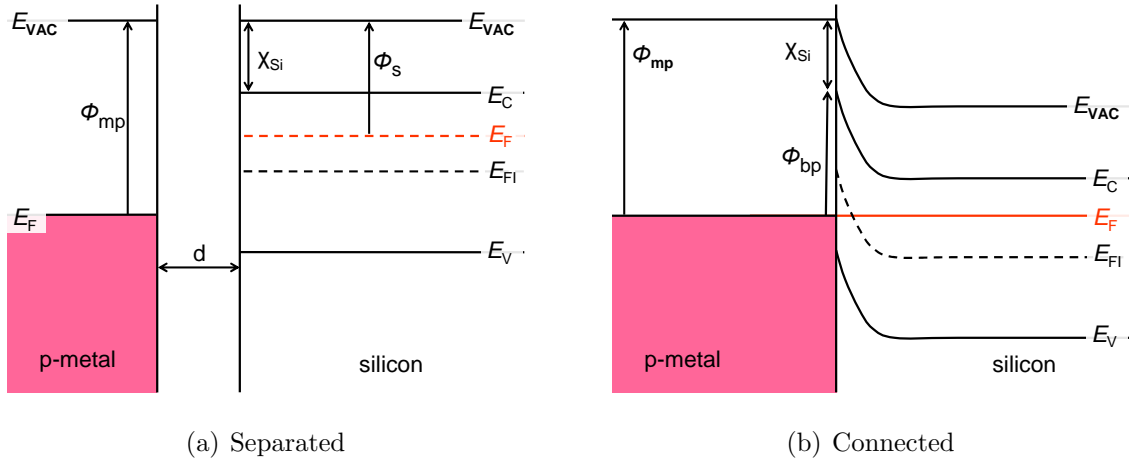
**Figure 2.1:** (a) a schematic band diagram of a metal and semiconductor. (b) When they are brought together both the extrinsic Fermi level $E_F$ en the vacuum level have to align. Also the electron affinity $\chi$ is a material constant, hence a region depleted of electrons is created adjacent to the interface at the semiconductor side

by their barrier height $\phi_{bp}$ from which the number of carriers at the interface can be calculated. In this discussion we ignored the fact that interface states or even fixed charge might by present at the interface which could change the shape of the bands, as discussed by Rhoderick and Williams [10] and Sze [11]. Because we cannot characterize the metal work function and the interface states separately with a DC measurement we will use the barrier height to characterize the contact and ignore all different possible combinations of metal work function and interface states densities/distributions which could have led to the same barrier height. Note however that an indirect way to extract interface states is possible provided that a good model has been developed by Rhoderick and Williams [10] and Sze [11]. However, this is not a part of this work. The presence of image charge in the metal close to the interface and a field at the interface effectively reduces the potential barrier by an amount, i.e. the image force barrier lowering effect as explained by Rhoderick and Williams [10],

$$\delta\phi = \sqrt{\frac{q\mathcal{E}}{4\pi\epsilon_{Si}}}, \tag{2.1}$$

where $\mathcal{E}$ is the electric field and $\epsilon_{Si}$ is the dielectric constant of silicon. This effect may be present in our measurements and is included in the extracted barrier heights. Because we use neither a high doping nor expect high barriers in our experiments, the field at the interface will be small and the image force barrier lowering effect negligible.

### 2.1.2 Thermionic Emission Current

The current transport across the interface can be characterized by the thermionic emission theory of Bethe [12]. The following assumptions have to hold (1) that the barrier height $\phi_b >> u_t$, where $u_t$ is the thermal voltage, (2) thermal equilibrium is established at the interface that determines emission and (3) the existence of a net current flow does not affect this equilibrium. Hence we can superimpose the current flux from the semiconductor into the metal and from the metal into the semiconductor. The silicon in our example

**Table 2.1:** Values for $m^*/m_0$ after Crowell [13]

| Semiconductor | Ge | Si | GaAs (low field) | GaAs (high field) |
|---|---|---|---|---|
| p-type | 0.34 | 0.66 | 0.62 | 0.62 |
| n-type $\langle 111 \rangle$ | 1.11 | 2.2 | 0.068 | 1.2 |
| n-type $\langle 100 \rangle$ | 1.19 | 2.1 | 0.068 | 1.2 |

in figure 2.1 (b) is n-type. Therefore the electron transport dominates the current, which allows to neglect the hole current. The electron current density from the semiconductor into the metal, called the forward current $J_{nF}^{th}$, depends on the concentration of electrons with energies sufficient to cross the potential barrier and which have a velocity in the direction off the metal. The current is given by,

$$J_{nF}^{th} = A_n^* T^2 e^{-\frac{\phi_{bp}}{u_t}} \cdot e^{\frac{V_A}{n u_t}}, \tag{2.2}$$

where $V_A$ is the applied voltage on the metal. $\phi_{bp}$ is the electron barrier. $A_n^*$ is the Richardson's constant, and $n$ is the ideality factor. The latter characterizes the deviation from ideality of the slope, ideally this factor is 1. If an high forward bias is applied to a Schottky contact then the series resistance of the silicon has to be taken into account, otherwise the current would increase to infinity. In section 3.1 it is shown how this can be done. The reverse current is characterized by the energy electrons in the metal need to have to travel into the conduction band. This barrier height is constantly $\phi_{bp}$ irrespective of the applied bias. Hence:

$$J_{nR}^{th} = A_n^* T^2 e^{-\frac{\phi_{bp}}{u_t}}, \tag{2.3}$$

the total electron current through the barrier is $J_{nt}^{th} = J_{nF}^{th} - J_{nR}^{th}$. The Richardson's constant characterizes the number of electrons at the interface having enough energy and the correct direction of velocity to cross the barrier. The Richardson's constant is given by:

$$A_-^* = \frac{4\pi q m^* k^2}{h^3} = 120 \cdot \frac{m^*}{m_0} \tag{2.4}$$

, where $k$ and $h$ are the Boltzmann's and Planck's constant respectively and $m^*$ is the tunneling effective mass. Where $A_-^*$ becomes $A_n^*$ for electron and $A_p^*$ for hole emission. $m^*$ depends on the type of carrier and on the semiconductor. Some values for $m^*/m_0$ are shown in table 2.1. A Schottky barrier can also be made by putting an n-metal on p-type silicon. The characteristics are similar except now holes determine the carrier transport. The hole barrier $\phi_{bn}$ is the difference between the Fermi level and the valence band. When intrinsic or lowly doped silicon is used both the hole and electron carrier transport have to be taken into account. The current for a p-type Schottky contact (n-metal p-silicon) is the forward minus the reverse current:

$$J_n^{th} = A_n^* T^2 e^{-\frac{\phi_{bp}}{u_t}} (e^{\frac{V_A}{n u_t}} - 1), \tag{2.5}$$

## 2.2    the aMSM-Diode

In the previous section the Schottky junction device characteristics has been briefly explained. In this section we will go one step further. Instead of connecting one metal to the silicon we will connect two metals with both n-type and p-type work functions to an intrinsic silicon layer. In this way we form an aMSM-diode. The current has to run through two Schottky junctions connected in series. The intrinsic or lowly doped silicon results in both metal-semiconductor interfaces to show non-ohmic behaviour. In this section we will discuss the device concept and use the Schottky theory to derive equations for the current in the device. Note that tunneling is neglected here which could become important for high electric fields, e.g. high reverse biases, high metal workfunction differences or short dimensions.

### 2.2.1    Device Structure

In figure 2.2 the device geometry of the diode is shown. The length of the intrinsic region is given by $L_i$, the thickness of the front oxide (SiO$_2$) by $t_{ox}$, thickness of the intrinsic silicon (Silicon-On-Insulator or in short SOI) by $t_{si}$, and buried oxide (BOX) thickness $t_{box}$. The n-metal and p-metal layer are indicated in blue and pink respectively.
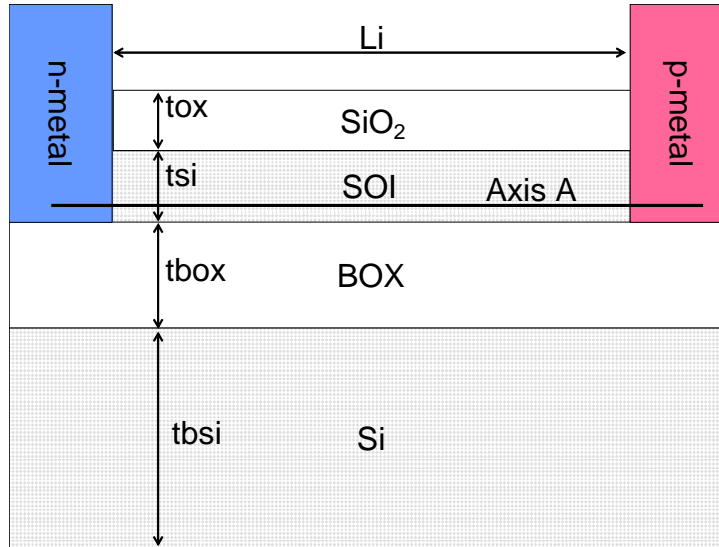


**Figure 2.2:** A schematic cross-section of the aMSM-diode. When a band diagram along axis A is made the IV relation of the p-metal and n-terminal can be derived. We assume that the band diagram is constant for various *tsi*.

The current through this device flows along Axis A. A schematic band diagram along this axis is shown in figure 2.3 (a). Here $\phi_{mn}$ is the work function of the n-metal and $\phi_{mp}$ is the work function of the p-metal. The hole barrier height at the n-metal silicon interface is given by $\phi_{bn} = \chi_{Si} + E_G - \phi_{mn}$. The electron barrier height at the p-metal interface is given by $\phi_{bp} = \phi_{mp} - \chi_{Si}$.

(a) Equilibrium  (b) Equilibrium
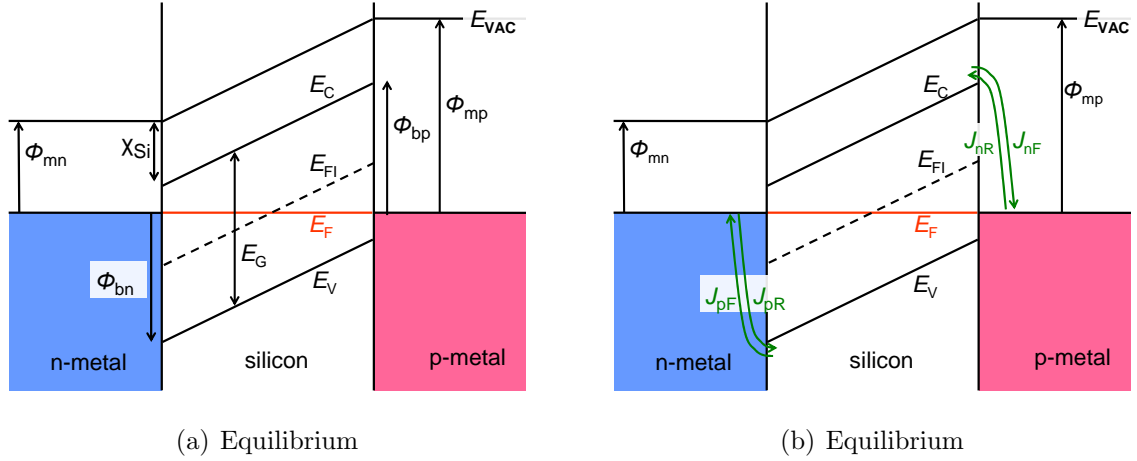
**Figure 2.3:** (a) Schematic band diagram of the proposed aMSM-diode under equilibrium conditions along axis A in figure 2.2. (b) The green arrows indicate the transport direction of carriers, their labels give the corresponding current components.

### 2.2.2 Thermionic Emission Current

When a bias is applied on the p-metal terminal both electrons and holes can flow into or out of the p-metal terminal. Hence the electron current is determined by a forward component $J_{nF}^{th}$ and reverse component $J_{nR}^{th}$. Also the hole current consists of two components, $J_{pF}^{th}$ and $J_{pR}^{th}$.

**Equilibrium**

Under equilibrium conditions the electron barrier is the highest at the p-metal interface which determines the thermal emission current. Hence the electron current at equilibrium is determined by the current across the p-metal silicon interface. The forward component is indicated by $J_{nF}^{th}$ , the reverse current by $J_{nR}^{th}$. Both are determined by thermionic emission and can be expressed as:

$$J_{nR}^{th} = A_n^* T^2 e^{\frac{-\phi_{bp}}{u_t}}. \tag{2.6}$$

For the reverse current the distance between the Fermi level and the conduction band is given by the barrier height $\phi_{bp}$. For the forward current the number of electrons in the conduction band is reduced by this same factor so the forward current becomes:

$$J_{nF}^{th} = A_n^* T^2 e^{\frac{-\phi_{bp}}{u_t}}, \tag{2.7}$$

both currents are equal but are in opposite direction, resulting in a net zero electron current. The hole current is determined by emission across the n-metal silicon interface. Analogue to the electron current both forward and reverse hole current are equal but opposite in direction, resulting in a net zero hole current. The reverse hole current is given by:

$$J_{pR}^{th} = A_p^* T^2 e^{\frac{-\phi_{bn}}{u_t}}. \tag{2.8}$$

(a) Forward
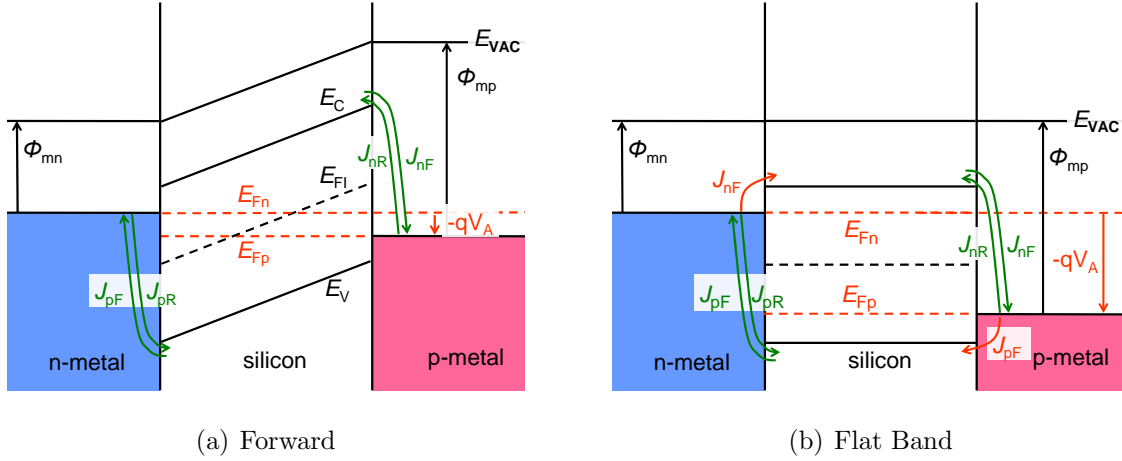
(b) Flat Band

**Figure 2.4:** Schematic band diagram of the proposed aMSM-diode. (a) When a small forward bias $V_A$ is applied on the p-metal the forward components $J_{nF}$ and $J_{pF}$ increase with a factor $exp(V_A/u_t)$. (b) In flat band condition ($V_A = \phi_{mp} - \phi_{mn}$) the forward currents components become limited by by thermionic emission from the metal into the silicon, this is indicated by the red arrows.

**Forward biasing**

When a small positive bias is applied on the p-metal terminal and the n-metal terminal is grounded, the p-metal Fermi level is slightly shifted down as indicated by $-qV_A$ in figure 2.4(a), thereby effectively reducing the barrier height. The electron quasi-Fermi level $E_{Fn}$ is determined or pinned by the Fermi level of the n-metal and the hole quasi-Fermi level $E_{Fp}$ by the p-metal Fermi level. An applied bias causes splitting between both quasi-Fermi levels. If the silicon is shorter then it's corresponding Debye length, ideally the silicon is lowly doped and hence the Debye length will be very long [1], then the splitting results in increased carrier concentrations at the metal semiconductor interfaces. The electron concentration in the silicon at the p-metal interface and the hole concentration in the silicon at the n-metal interface are both increased by a factor $exp(qV_A/kT)$, or in fact the barrier height has reduced by $V_A$. The reverse current does not depend on the applied bias. The forward current components become:

$$J_{nF}^{th} = A_n^* T^2 e^{\frac{-\phi_{bp}}{u_t}} e^{\frac{V_A}{u_t}} \tag{2.9}$$

and

$$J_{pF}^{th} = A_p^* T^2 e^{\frac{-\phi_{bn}}{u_t}} e^{\frac{V_A}{u_t}}. \tag{2.10}$$

**Far forward biasing**

When $V_A = V_{FB} = (\phi_{mp} - \phi_{mn})$ the device is in flat band condition. This is shown in figure 2.4 (b). For the flatband condition the maximum thermionic emission current from the n-metal into the conduction band is equal to the emission current from the conduction band into the p-metal (labeled $J_{nF}$ in red.). The red arrows in the figure are the currents which limit the total current. The reverse currents are still constant and

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[1]that is the length at which the charge carrier concentration (n or p) will drop by a factor 1/e

(a) Far Forward
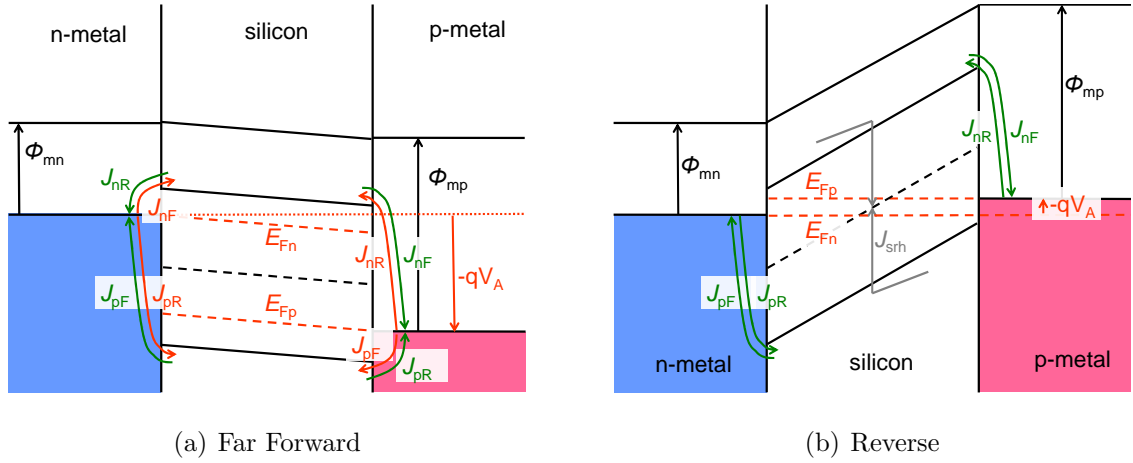
(b) Reverse

**Figure 2.5:** Schematic band diagram of the proposed aMSM-diode.(a) In far forward the red arrows indicate the current components which limit the current, this situation is comparable to flat band.(b) In reverse the forward components $J_{nF}$ and $J_{pF}$ are reduced. The SRH-current $J_{srh}$ draws electrons from the right and holes from the left metal contact. Hence this current can be modeled parallel to the emission currents.

negligible. Unfortunately a further increase in applied voltage as shown in figure 2.5 (a) will not change the barrier height between the n-metal and the semiconductor. Hence the electron current remains limited by the barrier between the n-metal and the silicon. For the hole current the same effect applies, but now the p-metal silicon interface limits the current. This current is indicated by $J_{pF}$ in red. Hence, for far forward bias holds:

$$J_{nF}^{th} = A_n^* T^2 e^{\frac{\phi_{bn} - E_G}{u_t}} \tag{2.11}$$

and

$$J_{pF}^{th} = A_p^* T^2 e^{\frac{\phi_{bp} - E_G}{u_t}}. \tag{2.12}$$

Often the currents will not reach these limits, this is caused by the resistance of the intrinsic region. If flat band conditions are reached then there will be no concentration differences in the intrinsic region any more. Hence a bias across the intrinsic region is required to generate a drift current. The electron and hole drift currents are easily described by multiplying the number of carriers in the intrinsic region, which now have become constant along axis A, charge, mobility and electric field. Now we find a hole and electron current density limited by the resistance:

$$J_{p,i}^{dr}(V_A > V_{FB}) = \frac{N_V q \mu_p (V_A - V_{FB})}{Li} e^{\frac{\phi_{bp} - E_G}{u_t}}, \tag{2.13}$$

respectively

$$J_{n,i}^{dr}(V_A > V_{FB}) = \frac{N_C q \mu_n (V_A - V_{FB})}{Li} e^{\frac{\phi_{bn} - E_G}{u_t}}. \tag{2.14}$$

### Reverse biasing

When a negative bias is applied on the p-metal terminal and the n-metal is grounded, the hole quasi-Fermi level shifts up compared to the electron quasi-Fermi level. This decreases

both carrier concentrations at the interfaces by a factor $exp(qV_A/kT)$ resulting in a lower forward current components. Finally the current equations are equal to the forward case. But now $V_A$ is negative and reduces the forward current until only the reverse current component is left.

### 2.2.3 Carrier Generation and Recombination

In practice the current in a PN-junction diode may be far in excess of that predicted by the diffusion theory especially for small forward biases. This current arises from the recombination for forward bias and generation of carriers for reverse bias through traps. Because of charge conservation, the empty places left behind by recombination have to be filled up. Eventually this results in a small current from the contacts. This is the so-called Shockley-Read-Hall [14][15] recombination/generation current, or in short SRH-current. The current will not be caused by Auger , as shown by Auger et al. [16], recombination because this requires a high number of minority carriers which are not present for small forward biases. Sah et al. [17] described the SRH-current in PN-junctions. We will use the SRH-current model in PN junctions as described by Pierret [18]. Traps at the intrinsic Fermi level have the highest probability of causing recombination, and hence affecting the SRH-current, therefore we neglect all other trap levels. Using $L_i$ for the length of the intrinsic region we get:

$$J_{srh} = \frac{qn_iLi}{\tau_n + \tau_p}(e^{\frac{V_A}{2u_t}} - 1).$$ (2.15)

Here $\tau_n$ and $\tau_p$ are the electron and hole life time respectively. Note that the slope of the recombination/generation current is given by $exp(V_A/2u_t)$. For practical semiconductor devices the carrier lifetimes are almost unknown and very strongly dependent on fabrication. However, for good quality bulk silicon the lifetimes are well defined. Still, the chance that our model is in agreement with measurement data is quite small. Fortunately the model can help us to understand the device characteristics. For reverse and small forward biases the SRH-current can be modeled parallel to the diffusion currents because it draws a current only from the regions with either high hole or high electron concentration, which are not the regions which limit the thermionic emission. Hence electrons are drawn from the n-metal contact and holes from the p-metal contact.

### 2.2.4 The proposed current model

From equations 2.6 and 2.9 we find the thermionic emission electron current;

$$J_n^{th} = J_{nF}^{th} - J_{nR}^{th} = A_n^* T^2 e^{\frac{-\phi_{bp}}{u_t}} \left(e^{\frac{qV_A}{kT}} - 1\right),$$ (2.16)

and from equations 2.8 and 2.10 the thermionic emission hole current:

$$J_p^{th} = J_{pF}^{th} - J_{pR}^{th} = A_p^* T^2 e^{\frac{-\phi_{bn}}{u_t}} \left(e^{\frac{qV_A}{kT}} - 1\right).$$ (2.17)

When biases above the flatband voltage are applied the electron current becomes limited by the sum of the reverse current 2.6, and maximum forward current, as in equation 2.11;

$$J_{n,max}^{th} = A_n^* T^2 \left(e^{\frac{\phi_{bn}-E_G}{u_t}} - e^{\frac{-\phi_{bp}}{u_t}}\right),$$ (2.18)

the hole current becomes also limited and is given derived from equation 2.8 and 2.12:

$$J_{p,max}^{th} = A_p^* T^2 \left( e^{\frac{\phi_{bp} - E_G}{u_t}} - e^{\frac{-\phi_{bn}}{u_t}} \right). \tag{2.19}$$

Let us limit the electron and hole current by the drift currents, equations 2.13 and 2.14, thermionic emission currents $J_n^{th}$ and $J_p^{th}$, and maximum thermionic emission currents $J_{n,max}^{th}$ and $J_{p,max}^{th}$:

$$J_{nt}^{th,-1} = J_n^{th,-1} + J_{n,max}^{th,-1} + J_{n,i}^{dr,-1}, \tag{2.20}$$

and

$$J_{pt}^{th,-1} = J_p^{th,-1} + J_{p,max}^{th,-1} + J_{p,i}^{dr,-1}. \tag{2.21}$$

The SRH, hole and electron current are all parallel to each other, hence we can simply add them to find the total current density:

$$J_t = J_{nt}^{th} + J_{pt}^{th} + J_{srh}^{th} \tag{2.22}$$

For the total current current we can say that:

$$I_t = Z \cdot tsi \cdot J_t, \tag{2.23}$$

where $Z$ is the width of the device.

## 2.3   The Charge Plasma Diode

As the name suggests a conventional PIN-diode consists of three regions: 1) a p-type region which is doped with acceptor-like atoms to form a region with a majority number of holes, 2) An undoped or intrinsic region, and 3) an n-type region, which is doped with donor-like atoms to form a majority of electrons. As explained in the introduction a way to fabricate an ultrathin p-i-n diode without employing an implantation process would be preferred. Such a device was proposed in 2008 by Rajasekharan et al. [7] for silicon-on-insulator (SOI) technology with a very thin oxide layer on the top. The p- and n-type regions are induced by a metal gate with a well chosen work function. These regions are not doped however we could say that a plasma of charged carriers is created in these thin regions. Hence the device is called Charge Plasma (CP) diode. At the extensions of the p- and n-type region the gates are directly contacted to the silicon layer. These metal gates form respectively the anode and cathode of the device.

At the end of 2008 a simulation study of the CP-diode was presented by Hueting et al. [8], discussing how the gate work functions and the device geometry should be chosen. It was claimed that to acquire a worthy rectifying behavior the difference in gate work functions should be at least 0.5 eV. Also the silicon thickness should be less than the Debye length, that is the length at which the charge carrier concentration (n or p) will drop by a factor $1/e$ in the direction of the gate-oxide-silicon junction. Therefore for too thick silicon layers there will be a plasma close to the gate, but there won't be a plasma close to the buried oxide. Hueting et al. also presented some simulation results, indicating that a charge plasma diode with a well chosen metal gate work function can achieve a good rectifying behavior.

## 2.3.1 Device Structure

A schematic device geometry of the CP P-N diode is shown in figure 2.6. The blue region indicates the n-metal. The metal is named like this because its work function is chosen such that it induces an electron (negative carrier or n-type) plasma in the neighbouring silicon. We will refer to this gate as the n-gate (n-type metal gate). The gate made of p-metal is colored purple and induces a hole (positive carrier or p-type) plasma in the neighbouring silicon. We will refer to this gate as p-gate (p-type metal gate). The SiO$_2$ region is the silicon oxide insulator on top of the ultrathin silicon layer. The oxide adjacent to the n- and p-gate do not necessarily have the same thickness. Hence their thicknesses are indicated by $toxn$ and $toxp$. The oxide thickness in the region which is not covered by gates is set at the the maximum of both $toxp$ and $toxn$ . SOI stands for silicon on insulator, indicating the silicon. The oxide beneath the SOI layer is called the buried oxide (BOX). Beneath the buried oxide is another silicon layer, called the silicon substrate. The lengths $Lon$ and $Lop$ denote the overlap length of the metal, which effectively increases the direct contact area between the metal and the silicon. The length of the gates are given by $Ln$ and $Lp$. The space between the gates indicates the length of the intrinsic region in the silicon and is given by $Li$.

As a start it would be useful to draw the band diagram under equilibrium conditions along axis A in figure 2.6. This will give an indication for the amount of charge carriers below the p-gate which we need for modeling the CP diode. Let us assume that this concentration in equilibrium will be constant along axis C under the p-gate. Then the band diagram of axis A will be valid all along the p-gate. A band diagram along axis B can be used to derive the carrier concentration below the n-gate. Finally these solutions can be used to construct the band diagram in equilibrium along axis C which is essential to find the current between the p- and n-metal terminals.
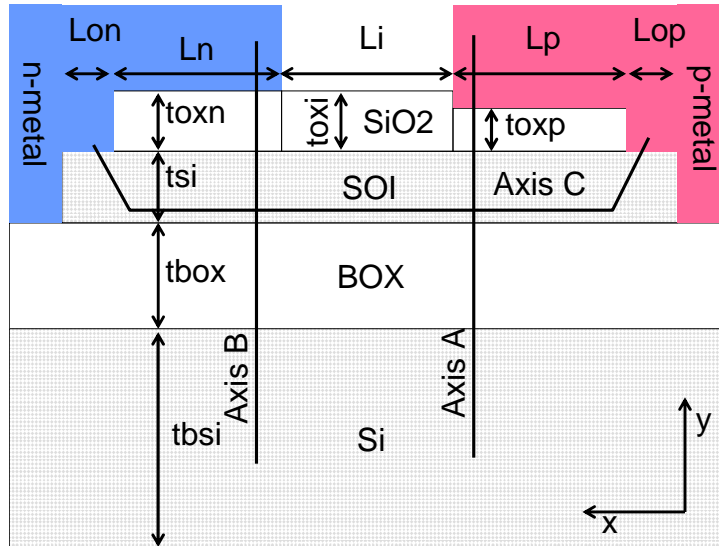


**Figure 2.6:** The schematic cross-section of the CP diode used for simulations showing all the parameters which characterize the CP P-N device geometry. We will start with a derivation of the carrier concentrations using schematic band diagrams along both axis A and B. Using their solutions we can derive the carrier concentrations along axis C.

## 2.3.2   The Charged Plasma's

In figure 2.7 (a) the band diagram along axis A of figure 2.6 is shown. When the gate induces a hole plasma under the gate then the gate is connected via a relatively low thermionic emission barrier to the holes over the length *Lop* and *tsi* to the silicon. Hence the Fermi level of the silicon adjacent to the metal and below the gate equals to the Fermi level of the gate. The p-gate work function $\phi_{mp}$ shifts the silicon bands upwards. This brings the Fermi level closer to the valence band $E_V$ which induces a hole plasma. For convenience sake, let us neglect the influence of the buried oxide and silicon substrate. Then all the charge which has to be taken into account is present in either the silicon or the metal layer, assuming no oxide charge or interface traps. If the concentration of holes in the charge plasma is higher than the doping concentration, then the presence of the dopant atoms can be neglected. The hole plasma in the silicon forms positive charge. The derivative of the potential is proportional to the charge, yielding an upward movement of the silicon bands along the $y$-axis as indicated in figure 2.7(a). The second derivative of potential is also proportional to the charge. Hence the silicon bands should become less flat along the $y$-axis. The same reasoning can be applied on figure 2.7 (b) to find a solution for the electron concentration under the n-gate.



(a) p-type metal gate          (b) n-type metal gate
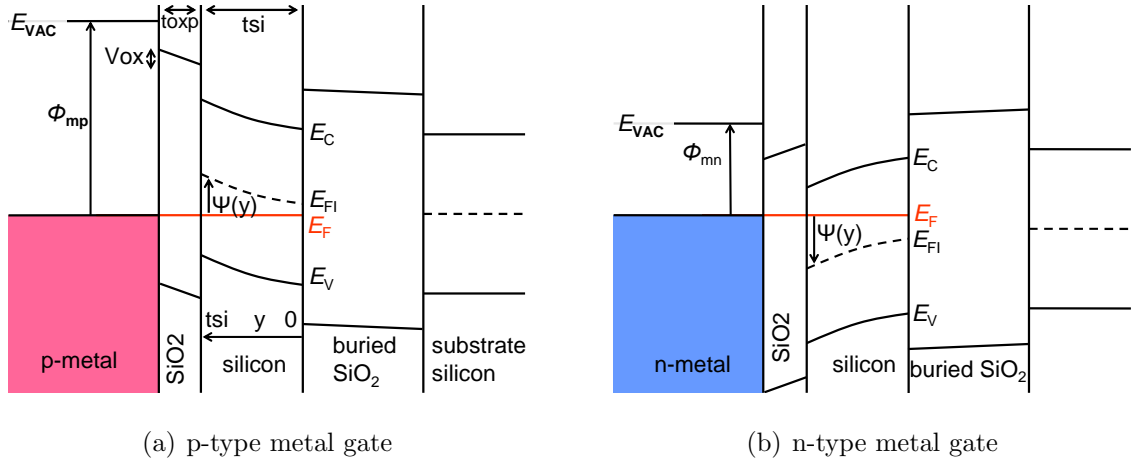
**Figure 2.7:** (a) Schematic band diagram along the axis A of figure 2.6, the metal work function causes the band of the silicon to be shifted upwards yielding a hole plasma. (b) And along axis B, where the silicon bands are shifted downwards and an electron plasma is formed.

Using the band diagram sketch in figure 2.7 (a) we can derive an exact solution for the band diagram. There are still a few unknowns to solve. For example the voltage across the front oxide $Vox$, which is related to the electric field at the silicon front-oxide interface. Also we need to find a solution for the delta potential $\Psi(y)$, which is the difference between the extrinsic and intrinsic Fermi level divided by the electron charge, in the silicon. Inside the silicon both the delta potential and charge obey the Poisson equation. For ultrathin silicon layers and low gate voltages we can neglect the doping and minority carrier charge. Then the Poisson equation is given by:

$$\frac{\delta^2 \Psi}{\delta y^2} = u_t \delta e^{\frac{\Psi(y)}{u_t}} \ , \tag{2.24}$$

where $\delta$ is a measure for the amount of carriers and their influence on the delta potential:

$$\delta = \frac{n_i}{\epsilon_{Si} u_t}, \tag{2.25}$$

here $\epsilon_{Si}$ is the dielectric constant of silicon and $u_t$ is the thermal voltage. We assumed that the intrinsic Fermi level $E_{FI}$ lays exactly at the center of the band. This holds as long as $N_V \approx N_C$, which is valid in silicon. $\Psi(y)$ is a function for the delta potential along $y$-axis in figure 2.7. All we need is a solution to this function. A similar problem shows up for the inversion charge in the subthreshold regime of a double gate MOSFET. A solution for this problem has been proposed by Taur [19] [20]. A demonstration of the validity of his solution can be found in appendix A. He proposes the following solution for the delta potential:

$$\Psi(y) = \Psi(0) - 2u_t \ln \cos(\beta y), \tag{2.26}$$

$$\beta = \sqrt{\frac{\delta}{2} e^{\frac{\Psi(0)}{2u_t}}}. \tag{2.27}$$

Here $\Psi(x)$ has a value $\Psi(0)$ at the buried oxide-silicon interface and increases for $y$. Note that $-\ln \cos(\beta y)$ is always positive. By applying the correct boundary conditions in our system we are able to derive the unknown variable $\Psi(0)$. Let us go back to figure 2.7 (a). The difference in vacuum level for the metal and the silicon is equal to the potential across the oxide $Vox$. The work function difference between the silicon and the metal is $\phi_{ms} = \phi_{mp} - \chi_{Si} - E_G/2$. The delta potential at the surface $\Psi(y = tsi)$ is equal to the work function difference minus the potential across the oxide:

$$\phi_{ms} - V_{ox} = \Psi(y = tsi). \tag{2.28}$$

If there is no charge in the front oxide silicon interface then the dipole moments on both sides of this interface are equal. Hence $\epsilon_{Si}\mathcal{E}_{Si} = \epsilon_{SiO2} \cdot \mathcal{E}_{SiO2}$ where $\mathcal{E}$ denotes the electric field. The electric field in the silicon is given by the first derivative of the delta potential $\mathcal{E}_{Si} = -\delta\Psi(y)/\delta y$. There is no charge inside the oxide, hence the electric field in the oxide is constant. The potential across the oxide now must be $V_{ox} = -tox \, \mathcal{E}_{SiO2}$ with $tox = toxn$ or $toxp$. Thus the potential across the oxide is equal to:

$$V_{ox} = tox \frac{\epsilon_{Si}}{\epsilon_{SiO2}} \frac{\delta\Psi(y)}{\delta y}\Big|_{y=tsi}. \tag{2.29}$$

Now equations 2.29 and 2.26 can be combined to one equation with one variable $\Psi(0)$ :

$$\Psi(0) = \phi_{ms} + 2u_t \ln \cos(\beta y) - tox \frac{\epsilon_{Si}}{\epsilon_{SiO2}} \frac{\delta\Psi}{\delta y}\Big|_{y=tsi}. \tag{2.30}$$

The structure in this equation is a relationship more or less according to $x = exp(x)$ and can be solved by numerical iteration. When a solution for the unknown variable $\Psi(0)$ is found the delta potential in the silicon as described by equation 2.26 can be calculated. The delta potential describes the distance between the intrinsic and extrinsic Fermi level in the silicon. Therefore the equilibrium carrier concentrations under the gate can be derived as a function of y. When $\Psi(0)$ is derived for either the p-gate or the n-gate, their majority carrier concentrations can be expressed as;

$$p_p = n_i \cdot e^{\frac{\Psi(y)}{u_t}}, \tag{2.31}$$

and:

$$n_n = n_i \cdot e^{\frac{-\Psi(y)}{u_t}}, \tag{2.32}$$

where $p_p$ is the hole concentration under the p-gate and $n_n$ is the electron concentration under the n-gate. Now the majority carrier concentrations are known the minority carrier concentrations can be calculated:

$$n_p = \frac{n_i^2}{p_p}, \tag{2.33}$$

and:

$$p_n = \frac{n_i^2}{n_n}. \tag{2.34}$$

The hole concentration under the n-gate is given by $p_n$ and the electron concentration under the p-gate by $n_p$. Hence, since the majority carriers depend exponentially on the metal workfunctions, this also holds for the minority carriers. The careful reader must have noted that $\Psi(y)$ is function of $y$. Hence the carrier concentrations depend on $y$. The highest number of minority carriers can be found at the silicon buried oxide interface. The largest concentration of minorities will dominate the diffusion current. Therefore we assume that the total current can be derived by using the carrier concentrations for $y = 0$.

### 2.3.3   Diffusion Current

In the previous section a solution has been shown for the carrier densities under the p- and n-gate in figure 2.6. When the gate work functions $\phi_{mn}$ and $\phi_{mp}$ are well chosen a positive charged plasma can be created under the p-gate and a negatively charged plasma under the n-gate. A region with the length $Li$ is not covered by a gate, hence no charged plasma is created in this junction. The shortest current path between the n- and p-gates is indicated by the Axis C in figure 2.6. Only for high forward voltages the region with the lengths $Lon$ and $Lop$ may become important. If we follow this axis we cross subsequently a n-metal, a negatively charged plasma under the gate oxide, an intrinsic region, a positively charged plasma under a gate and the p-gate. A band diagram under equilibrium conditions along this axis is shown in figure 2.8(a).

**Equilibrium**

In equilibrium no voltage is applied between the n- and p-gates. Hence the Fermi level in the band diagram of figure 2.8(a) is constant. The Fermi level in the silicon under the n-gate is close to the conduction band and indicates a strongly increased number of electrons and hence a negatively charged plasma. Under the p-gate the Fermi level is close to the valence band. In the "intrinsic" region no charge is present and when the substrate contacts are neglected the bands have to be straight lines. Also the bands in the intrinsic region have to connect to the bands in the regions under the gates. Together these requirements require band energies with a constant slope in the intrinsic region.

In reality the intrinsic region will have a low doping. As long as the length of intrinsic region is much shorter then the corresponding Debye length this will give no problems. There is Schottky barrier, as discussed in section 2.1, between the charged silicon and

(a) Equilibrium  (b) Forward
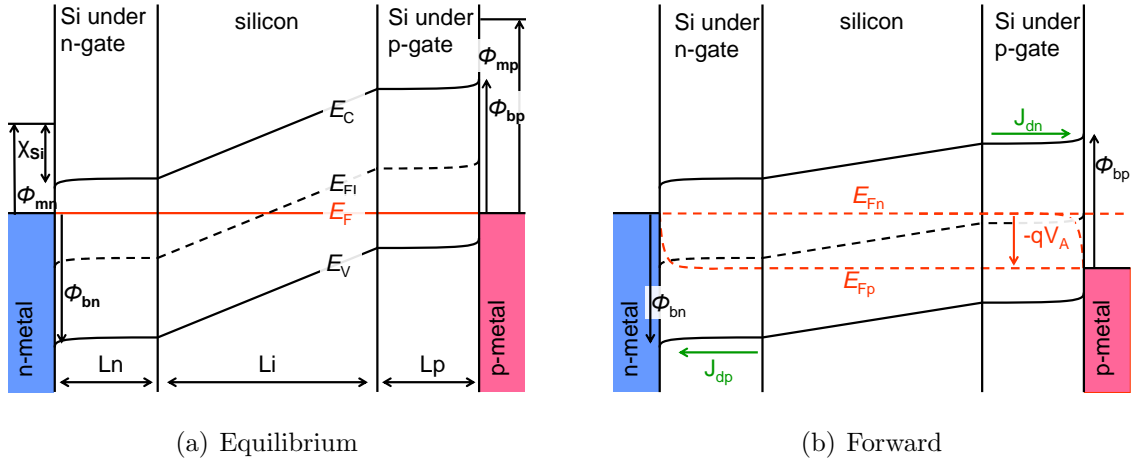
**Figure 2.8:** Schematic band diagram along axis C of figure 2.6, the green and pink area indicate the metals. The gates with a length $Ln$ respectively $Lp$ induce a charged plasma shown by the distance between the extrinsic and intrinsic Fermi level. An intrinsic region of length $Li$ exists between the charged plasma's. (a) there is no current flow in equilibrium (b) when a small forward bias $V_A$ is applied on the p-gate the diffusion

it's adjacent metal. This barrier is characterized by the barrier height. For now we will assume that this barrier doesn't limit the current. The hole barrier height at the n-metal silicon interface is given by $\phi_{bn} = -\chi_{Si} + E_G - \phi_{mn}$. The electron barrier height at the n-metal silicon interface is given by $\phi_{bp} = \phi_{mp} - \chi_{Si}$. These barrier heights induce a slightly more charged plasma compared to the regions under the gate. Under the gate the oxide has already absorbed part of the metal semiconductor work function difference which leads to a less charged plasma. This difference is also shown in the band diagram. Near the silicon metal interfaces the bands show a slight curvature, resulting in more charge. In equilibrium conditions no voltage is applied, hence there should be no current through the device.

We can also explain this by having another look at the band diagram. If no recombination or generation is present then the electron current should be constant throughout the device. The electron current will be determined by region in which it's has a very low concentration compared to the other regions. In equilibrium this is the case under the p-gate. Under this gate the electron concentration is constant and the bands are horizontal. Hence both diffusion and drift are excluded as possible current transport mechanisms and the resulting electron current will be zero. Off course a small deviation of this theory exists in the bands and concentrations close to the p-gate interface. As long as this region is much smaller then the gate length this will give no problems.

### Forward

When the p-gate is biased positively compared to the n-metal the bands under the p-gate are shifted downward compared to the bands under the n-gate. Also the Fermi level is separated in two distinct Fermi levels, also called quasi-Fermi levels. $E_{Fn}$ becomes the quasi-Fermi level for electrons and $E_{Fp}$ the quasi-Fermi level for holes. Inside the device these quasi-Fermi levels are relatively constant. This was shown for p-n junction by

Shockley [21]. We will follow Sze's conclusions [11]. The quasi-Fermi levels are constant because: (1) In the charged plasmas the semiconductor has not an equal number of holes and electrons so generation/recombination is not important here and both electron and hole current remain constant. (2) The length of the regions are much shorter than the diffusion length, typically 60 $\mu$m for holes and 190 $\mu$m for electrons, therefore the total drop of the quasi-Fermi levels cannot be significant. Under the gates the majority carriers quasi-Fermi levels are fixed by the gate semiconductor work function difference. Hence an applied voltage $V_A$ will shift both quasi-Fermi levels apart from each other:

$$qV_A = E_{Fn} - E_{Fp}. \tag{2.35}$$

This applied voltage will increase the minority carrier concentration in the regions under the gates close intrinsic region by a factor $exp(V_A/u_t)$ compared to equilibrium. The hole current is determined by the region with the lowest hole concentration. Which is the region under the n-gate. This can be observed in figure 2.8(b), under the n-gate the distance between the hole Fermi level and valence band is the largest giving the lowest number of holes. The n-gate mainly determines the potential in this region, therefore there is almost no potential drop and the current must be originate from diffusion current caused by carrier concentrations differences. The hole concentration at the n-metal silicon interface is much lower compared to the concentration at the intrinsic region interface. If we assume the hole concentration to degrade linearly the hole current is given by the derivative of the hole concentration multiplied with the diffusion constant and elementary charge:

$$J_p^d = \frac{p_n q D_p}{Ln}(e^{\frac{V_A}{u_t}} - 1), \tag{2.36}$$

where $D_p$ is the hole diffusion constant. The movement of the carriers corresponding to this hole diffusion current has been indicated in figure 2.8 (b) with a green arrow labelled $J_{dp}$. Here we assume the hole concentration at the n-gate intrinsic interface to be equal to $p_n \cdot exp(V_A/u_t)$ and the hole concentration at the n-gate silicon interface to be much lower. The latter concentration will increase with increasing current as has been showed in the user guide [22]. Since at the contacts an effective surface recombination was assumed corresponding to the thermionic emission model, the minority carrier concentration at the contacts won't reach their equilibrium values. In fact these carrier concentrations are governed by the current densities and the boundary conditions. As long the forward voltages bias is not to high the effective surface recombination can be neglected and equation 2.36 should hold. The result is comparable to the PIN-diode theory showed by Baliga [23], except that he expects the intrinsic region to be the limiting region for carrier transport. This is true when the intrinsic region becomes very long. We can apply the same theory to derive the electron current. Which will result in:

$$J_n^d = \frac{n_p q D_n}{Lp}(e^{\frac{V_A}{u_t}} - 1). \tag{2.37}$$

**Far Forward**

For increasing forward voltages the current will increase according to equations 2.36 and 2.37. However for high voltages this will not hold anymore. Some other process limits the current. In this work we will call this far forward. A band diagram of this situation has been sketched in figure 2.9 (a). The hole quasi Fermi level is closest to the valence band

in the region under the n-gate. Hence the concentration of holes under this gate is not the lowest any more. The lowest concentration of holes is found at the arrow labeled $B$.



(a) Far Forward                                (b) Reverse
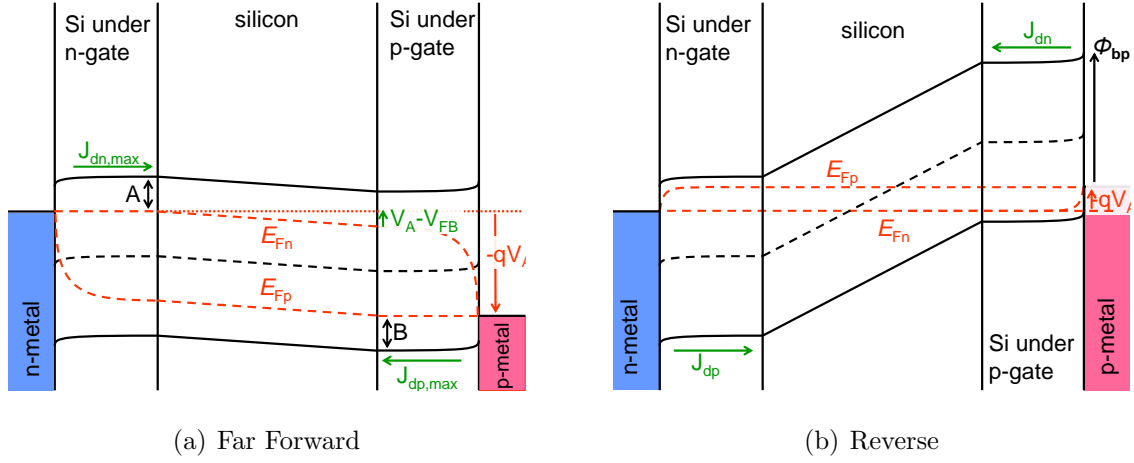
**Figure 2.9:** Schematic band diagram along axis C of the proposed CP-diode. (a) When a large positive bias ($V_A > V_{FB}$) is applied the device is in far forward. The current is determined by the diffusion of carriers from the metal to to the intrinsic region, the carrier transport directions are indicated by the green arrows. (b) When a negative bias is applied on the p-gate terminal the forward components become small and the reverse components stay.

The holes at the p-metal silicon interface have to diffuse through the silicon under the p-gate. An approximation for this current can be obtained by assuming that the hole concentration drops linearly across this region. The highest hole concentration is found at the p-metal interface. Hence the diffusion current is given by;

$$J_{p,max}^d = \frac{N_V q D_p}{Lp} e^{\frac{\phi_{bp} - E_G}{u_t}},$$
(2.38)

we can also derive the maximum electron current:

$$J_{n,max}^d = \frac{N_C q D_n}{Ln} e^{\frac{\phi_{bn} - E_G}{u_t}}.$$
(2.39)

We like to note that the expression for the carrier concentration at the n-metal interface increases for large currents. This is demanded by the boundary conditions for Schottky interfaces given in [22], as explained earlier. Therefore this diffusion current will not be constant in reality but will slightly increase for increasing forward voltage. There can also be other reasons for the current to be limited. For example the speed of the carriers in the intrinsic region cannot exceed the carrier saturation velocity. The carriers also have to cross the Schottky barriers between the metal and silicon.

### Reverse

When a negative bias is applied at the p-gate compared to the n-gate we say that the device is in reverse. A band diagram of this situation is shown in figure 2.9 (b). In this situation equation 2.35 is still valid at the boundaries of the intrinsic region. Hence the minority carrier concentrations here are known. The hole concentration reaches its minimum level

under the n-gate. Now the hole current is given by diffusion from the n-metal interface to the boundary of the intrinsic region. At the interface the hole concentration is given by 2.34. The hole concentration at the boundary is lowered by a factor $exp(V_A/u_t)$. Now the currents again are given by the same equation as the forward currents.

### 2.3.4   Carrier Generation and Recombination

Like in the PIN-device 2.2.3 a SRH-current may be important in the CP diode. Again the length of the intrinsic region is given by $Li$. Therefore we will use equation 2.15 again to define the SRH-current. For reverse and small forward biases the SRH-current can be modeled parallel to the diffusion currents because it draws a current only of the majority carriers.

### 2.3.5   The proposed current model

We showed how to derive both electron and hole current for different bias conditions. In reverse and forward the results are almost equal to the Shockley equation [11]. Although in our devices it is not the diffusion length but it is the length of the diffusion regions which determines the current. For high forward bias the currents becomes limited by diffusion of majority carriers under the gates. Also there exists Schottky contacts between the metal and the silicon, these may limit the current as well. Let us incorporate equation 2.20 and 2.21 as derived in the previous section to limit the current by thermionic emission and to account for the resistance of the intrinsic intrinsic region in forward. These don't incorporate the added contact lengths $Lon$ and $Lop$, however due to current crowding the area where the current flows will not easily become bigger then $tsi$. For the electron and hole current we find:

$$J_p^{d,-1} = J_{dp}^{d,-1} + J_{dp,max}^{d,-1} + J_{pt}^{th,-1},$$ (2.40)

and:

$$J_n^{d,-1} = J_{dn}^{d,-1} + J_{dn,max}^{d,-1} + J_{nt}^{th,-1}.$$ (2.41)

The SRH, hole and electron current are all parallel to each other, hence we can simply add them to find the total current density:

$$J_t^d = J_n^d + J_p^d + J_{srh}^d.$$ (2.42)

# Chapter 3

# Calibration

## 3.1  Barrier Height Extraction Techniques

In this section we will illustrate how the IV characteristics of an electron Schottky barrier for different temperatures can be used to derive the Schottky diode parameters as described in section 2.1. The extraction of the parameters for a hole Schottky barrier is similar. The silicon has to be either n- of p-type which allows to analyze either the hole or electron transport mechanism. The parameters which we will extract include the ideality factor $n$, which characterizes the deviation of the forward current from the ideal thermionic emission model. The series resistance in the measurement structure times unit area is denoted by $\rho_s$, the electron emission barrier height by $\phi_{bp}$ and the Richardson constant $A_n^*$. Let us include the series resistance into equation 2.2 , then the forward and reverse electron current components of a Schottky barrier are given by;

$$J_{nR}^{th} = A_n^* T^2 e^{-\frac{\phi_{bp}}{u_t}},\tag{3.1}$$

and;

$$J_{nF}^{th} = A_n^* T^2 e^{-\frac{\phi_{bp}}{u_t}} e^{\frac{(V_A - J_{nF}^{th}\rho_s)}{nu_t}},\tag{3.2}$$

where $\rho_s$ is the series resistivity [1].

### 3.1.1  Reverse

Let us start with the reverse characteristics of the Schottky diode. Ideally this current should have no slope and be constant for reverse biases greater then a few $u_t$. In reality it has, this can be caused by SRH recombination which we described in section 2.2.3. For $V_A = 0$ the SRH-current is zero. Hence if we extrapolate the current to the Y-axis crossing we can find the reverse current independent of the SRH-current. We start to fit a linear regression to the curve with the coefficients $\alpha$ (the value for $V_A = 0$) and $\beta$ (the slope). Then we recreate the reverse IV characteristic using $\alpha + \beta V = Jth_{nR,reg}$. Another advantage, besides removing the SRH-current component, of this technique is to eliminate noise. In equation 3.1 we can replace $J_{nR}^{th}$ with our current found by linear regression $J_{nR,reg}^{th}$.

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[1]since the modeling is in 1D the resistivity is expressed in $\Omega cm^2$. In real life however this is of course in $\Omega$

Let us follow Schroder [24] to extract the barrier height and Richardson constant from this equation:

$$\ln \frac{J_{nR,reg}^{th}}{T^2} = \ln A_n^* - \phi_{bp}q/kT \tag{3.3}$$

When we plot $\ln(J_{reg}^{th}/T^2)$ versus $1/T$ the graph will have a slope equal to $q/k\phi_{bp}$ and Y-axis crossing $\ln(A_n^*)$. Such a graph is usually called a Richardson plot. We illustrate this by an example, the Cobalt on n-type silicon junction, in figure 3.1(a). The plot is shown for three different reverse biases. Ideally these three should be equal. In reality they are not because of secondary effects. For zero bias the SRH-current component should be zero and hence for zero bias the Richardson plot is ought to be correct.

In figure 3.1 we show the extracted parameters. The extracted barrier height varies by a few percent. The Richardson constant is found by extrapolation of the Richardson graph. We have measurement data till $2,5$ $(1000/K)$, hence we have to extrapolate on the Y-axis from 2.5 to 0 $(1000/K)$. Therefore a small error in the slope might result in a serious error in the extracted Richardson constant. So we can conclude that although the Richardson constant can be extracted it will be very prone to error.



(a) Richardson plot    (b) Extracted parameters
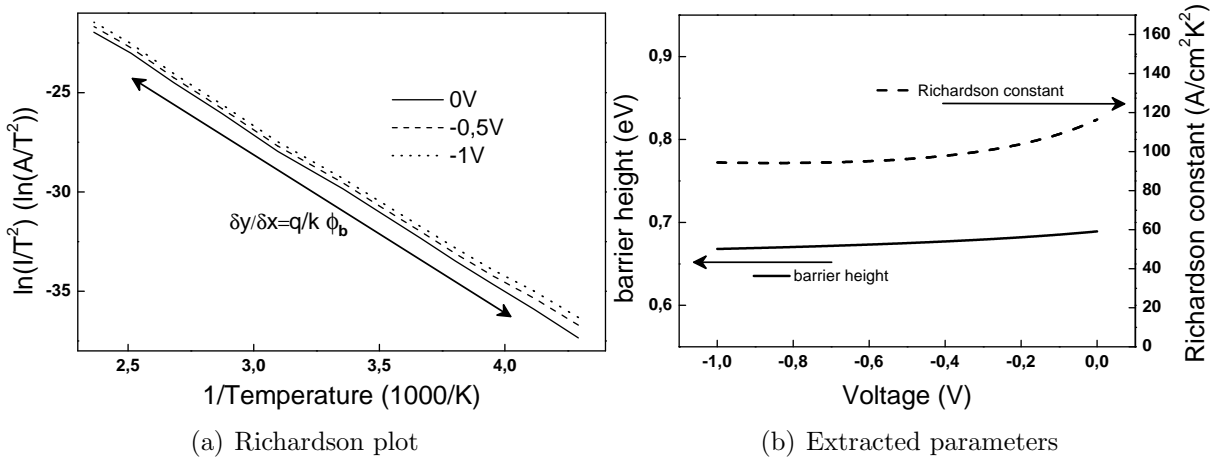
**Figure 3.1:** (a) The Richardson graph of a Cobalt on n-type Silicon Schottky barrier, the slope gives $\phi_{bp}$ and extrapolation to the y-axis $A_n^*$. (b) The extracted parameters. Their variation for different biases is caused by non-ideal behavior of the Schottky contact. For example SRH-current is a good candidate to improve our model.

### 3.1.2 Forward

For forward biases greater then a few $u_t$ the reverse current $J_{nR}^{th}$ can be neglected. To characterize the series resistance we will follow the Cheung method [25]. Let us manipulate equation 3.2 to find the relation between the applied voltage and the series resistivity.

$$V_A = n \cdot u_t \ln J_{nF}^{th} A_n^* T^2 + nq\phi_{bp} + J_{nF}^{th}\rho_s, \tag{3.4}$$

secondly we take the derivative to $\ln J_{nF}^{th}$:

$$\frac{\delta V_A}{\delta \ln J_{nF}^{th}} = nu_t + J_{nF}^{th}\rho_s. \tag{3.5}$$

In figure 3.2 (a) we show an example for different temperatures. The slope gives the resistivity. The intercept with the y-axis should give the ideality factor. Unfortunately the curves show a slight curvature close to the y-axis intercept due to non-ideal behaviour. This results in quite a lot of spread in the ideality factors and therefore we should use another method to extract the ideality factor. In figure 3.2 (b) we show the extracted series resistance for different temperatures. Note that the resistance increases with temperature indicating the semiconductor as a plausible cause.



(a) Finding $R_s$      (b) $R_s$ over temperature
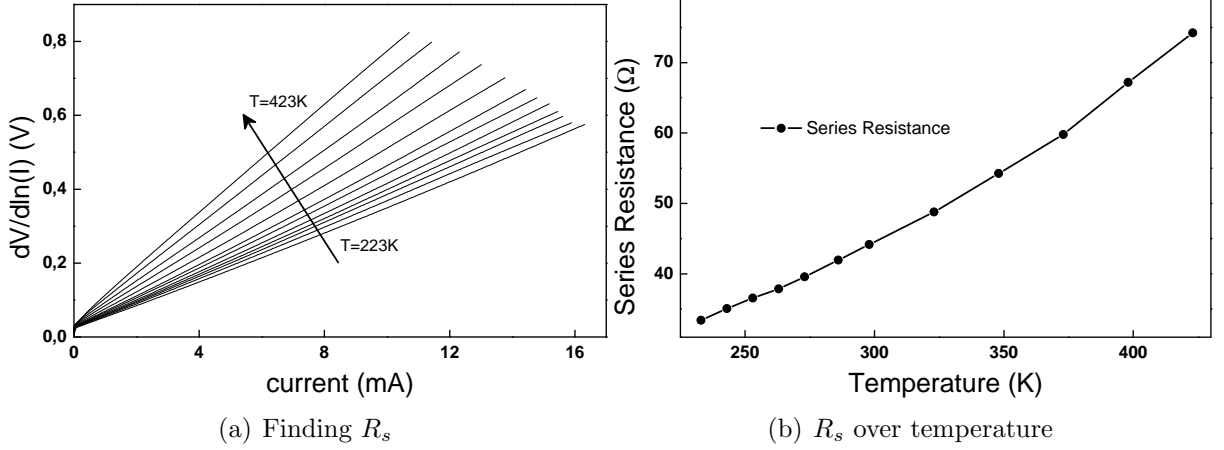
**Figure 3.2:** These graphs illustrate the extraction of the series resistance of a Cobalt on n-type silicon Schottky barrier. (a) An $\delta V/\delta \ln(I)$ versus $I$ plot as proposed by Cheung [25], the series resistance $R_s$ is extracted from the slope. (b) The extracted series resistance increases with temperature, the silicon is a plausible source of the resistance.

In figure 3.3 (a) we show the IV characteristics for different temperatures. For forward biases greater then a few $u_t$ and currents below 0.1 mA both the reverse current and the series resistance can be neglected. This is indicated by the grey area in the graph. In this region the ideality factor is given by:

$$\frac{\delta \ln(J/T^2)}{\delta V_A} = 1/(n \cdot u_t). \tag{3.6}$$

If the current in the junction is mainly determined by thermionic emission we will find an $n$ close 1. If other effects are playing a dominant role we will find a much larger $n$. In graph 3.3 we show the extracted ideality factor. For temperatures above 360 K the series resistance starts to play an important role and hence this technique becomes less accurate.

Now we have found the series resistance and the ideality factor it should be possible to find both the barrier height and the Richardson constant for forward biases. Let us manipulate equation 3.2, we find:

$$\ln(J_{nF}^{th}/T^2) + J_{nF}^{th}\rho_s/u_t = \ln A_n^* + V_A q/nkT - \phi_{bp}q/kT. \tag{3.7}$$

The result is similar to equation 3.3 except it incorporates the influence of the series resistivity and applied voltage divided by the ideality factor. Again a Richardson plot can be made and the parameters can be extracted. The method is dependent on the

(a) IV Measurements
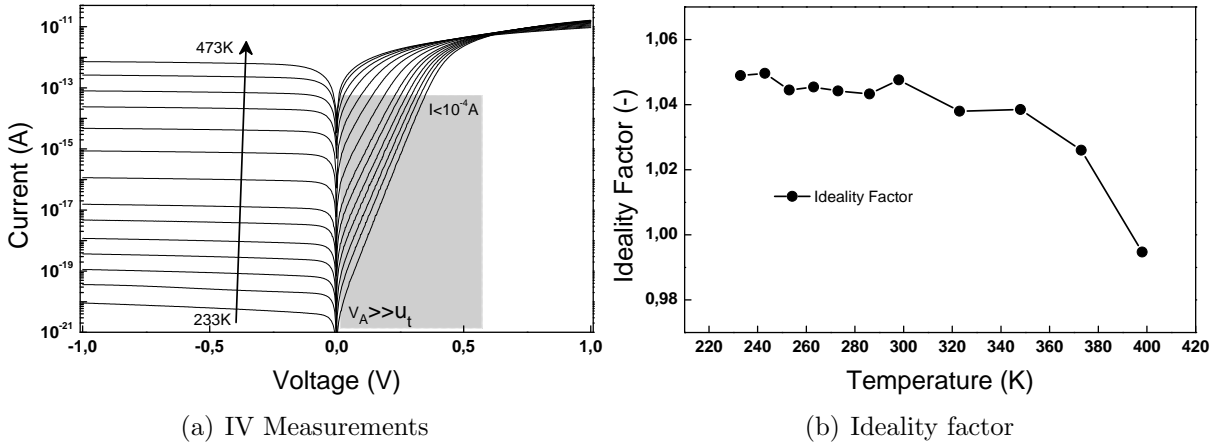
(b) Ideality factor

**Figure 3.3:** (a) the measured IV characteristics. The grey area illustrates where both series resistance and reverse current can be neglected. (b) The extracted ideality factors.

previously extracted parameters $R_s$ and $n$, therefore the extracted parameters are prone to errors.

In figure 3.4 we show the extracted parameters for both forward and reverse biasing. The barrier height shows a variation of 0.02 eV. Because the extrapolated reverse current shouldn't incorporate SRH and other non-ideal effects, we believe that the barrier height just on the negative side of zero bias is the most correct one. We find 0.69 eV for the barrier height. The Richardson constant shows a variation of 40 $Acm^{-2}K^{-2}$ and the extracted Richardson constant is 120 $Acm^{-2}K^{-2}$.
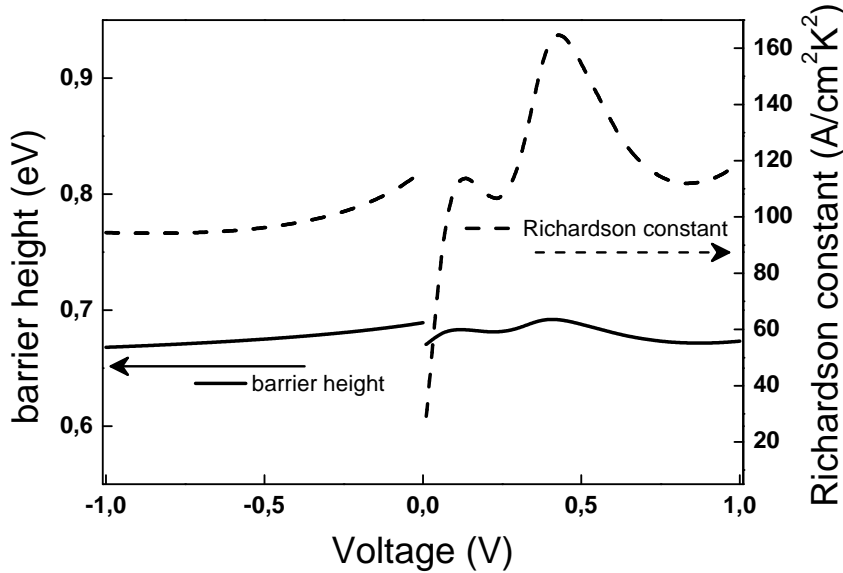


**Figure 3.4:** Extracted forward $V_A > 0$ V and reverse $V_A < 0$ V Richardson constant and Schottky barrier height. We believe that the values for very small reverse bias suffer the least from influence of secondary effects.

## 3.2   Test Devices

We studied current voltage characteristics [26] for different metal contacts on lowly doped silicon fabricated in the MESA+ cleanroom [2]. As starting material 4 inch bulk $Si(100)$ wafers were used having a specific resistance of $5\Omega$ cm for the p-type and $10\Omega$ cm for the n-type substrates. First a 100 nm thick thermal oxide layer is grown. After the definition of the contact holes the silicon contact area was cleaned using 100% $HNO_3$ to remove organic contaminants, 69% $HNO_3$ at 95 ° C to remove metal contaminants and finally they receive an 1% HF dip to remove native oxide. Following this cleaning procedure, the metal was sputtered and patterned using standard photolithography and wet chemical etching. After this the backside of the wafer was covered with the back metal to form an ohmic contact.

The mask contained a range of contact sizes form $10 \cdot 10$ $\mu$m$^2$ to $1000 \cdot 1000$ $\mu$m$^2$ to check for possible area dependency of the extracted barrier heights. All results presented here are from contact areas of $200 \cdot 200$ $\mu$m$^2$.

The following metals were chosen based on their general availability in IC processing facilities and the availability of a wet etch selective to Si and $SiO_2$ ; aluminum (Al), cobalt (Co), molybdenum (Mo), palladium (Pd), erbium (Er), titanium (Ti) and titanium tungsten (TiW, alloy contains 10% Ti). Since the adhesion of pure Pd on $SiO_2$ was very bad we have co-sputtered a small amount of titanium, resulting in a film containing 0.5 atomic % of Ti, as determined with X-ray fluorescence(XRF). This small amount of Ti is assumed not to change the electrical properties so this mixture is abbreviated as Pd in this paper. Additionally we have tried a sputter target containing 7 % titanium (form Rutherford Backscattering spectroscopy, RBS). This film is believed to have electrical characteristics in between that of Ti and Pd.

For all metals we have used available sputter recipes in our microfabrication facilities for films between 100 and 500 nm. The electrical characterisation was done using a Keithley 4200 Semiconductor Parameter Analyser, a Cascade probe station equipped with a thermochuck. The IV characteristics were recorded between $-60$ °C and $+200$ °C. After the highest temperature measurement a control measurement was done at room temperature to check the stability of the contact.

## 3.3   Characterisation Results

From the IV characteristics we derived the different Schottky barrier parameters using the techniques described in section 3.1. The results are shown in table 3.1. Each metal except Erbium was deposited both on n-type and p-type silicon. Hence all parameters have been extracted for both cases. If both barriers do not suffer from secondary effects, like image force barrier lowering, interface states, Fermi level pinning and tunneling, then $\phi_{bn} + \phi_{bp}$ should equal to the bandgap of silicon which is $E_G \approx 1.12$ eV. For both $Co$ and $Mo$ the sum of the barriers is 1.07 eV hence only 0.05 eV of the bandgap is consumed by secondary effects. Ti showed a surprisingly bad result with 0.65 eV.

Our final goal is to create a charge plasma diode. For good results we require the barrier to be as far from the center of the bandgap ($>> 0.56$ eV $<<$) as possible. To induce a plasma of electrons we will use the $Er$ barrier because it has a high $\phi_{bn}$, an high $A_n^*$ and $n$ close to 1, indicating close to ideal behavior. To create a plasma of holes we

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[2]By courtesy of B. Rajasekharan

**Table 3.1:** Measurement Results on different metal silicon Schottky barriers.

| Material | $\phi_{bp}$ (eV) | $\phi_{bn}$ (eV) | $A_n^*$ (A/cm$^2 K^2$) | $A_p^*$ (A/cm$^2 K^2$) | $n_n$ | $n_p$ |
|---|---|---|---|---|---|---|
| Ideal | $> 0.56 <$ | $> 0.56 <$ | 240 | 80 | 1 | 1 |
| Er | - | 0.72 | — | 140 | 1 | 1.17 |
| Ti | 0.23 | 0.42 | ? | 55 | $1.4 - 1.13$ | $1.16 - 1.48$ |
| TiW | 0.42 | 0.50 | 4 | 80 | 1.15 | 1.3 |
| PdTi$_{0.5\%}$ | $0.76 - 0.82$ | 0.12 | 4395 | 2 | 1.05 | 1.97 |
| PdTi$_{7\%}$ | 0.69 | 0.29 | 20 | 12 | 1.07 | 1.69 |
| Co | 0.69 | 0.38 | 115 | 12 | 1.04 | 1.5 |
| Mo | 0.69 | 0.38 | 190 | 2 | 1.04 | 2.06 |
| Al | 0.66 | 0.19 | ? | 0.32 | $1.4 - 1.0$ | 1.3 |

will use PdTi$_{7\%}$ because it shows both a low barrier to p-type silicon and $\phi_{bn} + \phi_{bp} = 0.98$ eV which is quite large compared to *Al* were we find 0.85 eV. PdTi$_{0.5\%}$ could be a better option, unfortunately it suffers from silicidation which we will discuss in section 3.4.

## 3.4 Silicidation of PdTi$_{0.5\%}$

During the first characterization of PdTi$_{0.5\%}$ the barrier height $\phi_{bp}$ showed a strong dependency on the temperature. Depending on which temperature data was used a barrier height between 0.75 eV and 0.82 eV could be extracted. During a second measurement this dependency was gone. This deviation during the first measurement can be explained by silicidation. At temperatures as low as 100 °C paladium-silicon (PdSi) is formed. Each IV recording takes at least 10 minutes time hence the sample has plenty of time to form a 50 nm thick layer silicide layer during the measurements cycles. A change in the metal resulted in a change of the barrier height.

In figure 3.5 we show a TEM recording of the PdTi$_{0.5\%}$ on n-type silicon junction. The Pd has reacted with the Si and formed a silicide. To evaluate our finding we performed a second series of measurements. The Richardson plots of the first and second series are shown in figure 3.6. Using the low temperature data only we extracted a barrier height of 0.76 eV for the first and 0.72 eV for the second series. These barrier heights were used as an input parameter for a device simulator [22]. From the output we extracted Richardson plots which are also shown in the graph. These clearly confirm the reduction of the barrier height, resulting from silicidation at temperatures above 100 °C.

## 3.5 Verification and Simulation

In the rest of this work we will show simulation results on the aMSM- and CP-diode. The extracted barrier height of Er and PdTi$_{7\%}$ will be used as an input parameter to a device simulator. For the CP-diode both the Richardson constant and ideality factor do not play an important role. Hence we will not use these as input parameters in the simulator. To verify the simulator results we can compare the measured and simulated IV characteristics of a Schottky diode.

In figure 3.7 (a) we show the IV curves for the Erbium on n-type Schottky barrier. The temperature dependence of the simulations and measurements is comparable, there-
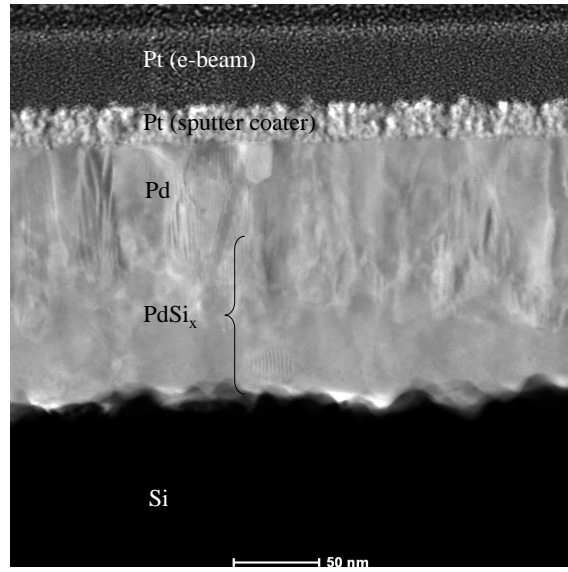
**Figure 3.5:** A TEM cross section of the PdTi on silicon junction. The lower part of the PdTi has reacted with the silicon and formed PdSi. This resulted in a reduced Schottky barrier height. (recorded by MiPlaza, Eindhoven)
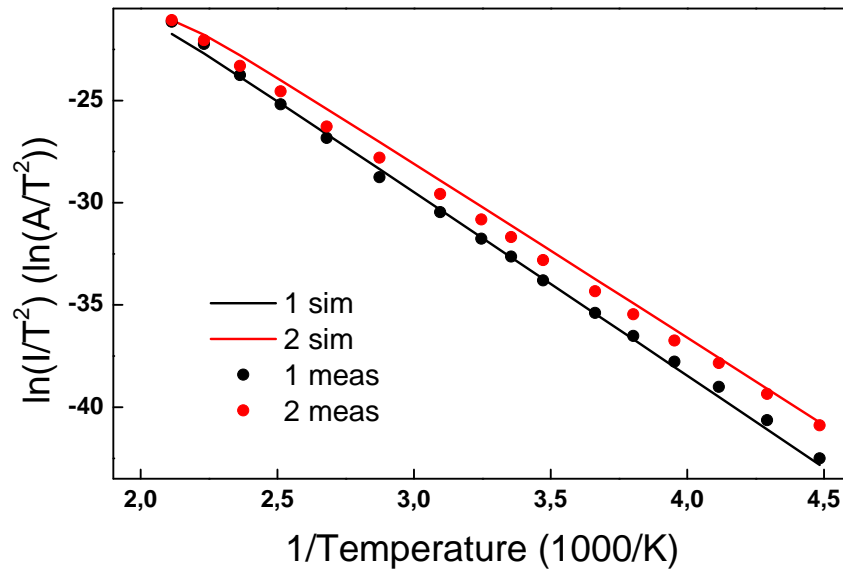


**Figure 3.6:** The Richardson plot for the PdTi$_{0.5\%}$ on n-type silicon devices. The barrier height $\phi_{bp}$ can be extracted from the slope of the graphs. The second measurement shows a lower barrier height which is caused by silicidation during the first measurement. Both extracted barrier heights have also been used as an input parameter in a device simulator. The simulated Richardson graph confirms that the change in the Richardson graph is a result of a change in the barrier height.

fore the barrier height is modeled correctly. Under reverse bias $V_A > 0V$ both show a comparable voltage dependence. Therefore the SRH-model of the simulator matches to the measurement data. Therefore we conclude that the Schottky barrier height is a valid parameter to model the characteristics of a Schottky barrier, and therefore the simulator is a valid tool to model the characteristics of the CP- and aMSM-diode.

In figure 3.7 (b) we show the measured and simulated IV characteristics for the PdTi$_{7\%}$ p-type silicon junction. Again the temperature dependence is comparable hence the barrier height is modeled correctly. The measurements show a strong voltage dependence for negative voltages. A probable reason for this is SRH generated current. The extracted $n$ of 1.69 also indicates that not only the thermionic emission current plays a role.



(a) IV

(b) $Rs$
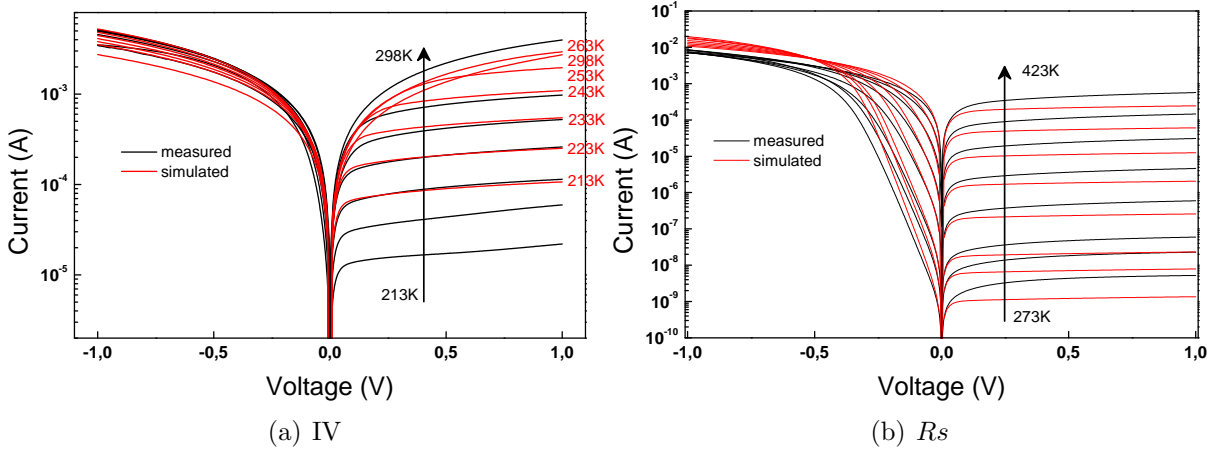
**Figure 3.7:** Simulated and measured IV curves. (a) for the Er on p-type Si barrier and (b) the PdTi$_{7\%}$ on p-type Si barrier. Both show relatively good matching temperature dependence and hence barrier height. Therefore the simulator with the barrier height as an input parameter is valid tool to model the characteristics of the CP and aMSM-diode.

# Chapter 4

# Simulation

## 4.1    The aMSM-diode

In this section we will use two-dimensional simulation results to show that the model proposed in section 2.2 gives a good estimate for the current in aMSM-diodes. More details on the exact parameters of the structure and models in the simulator can be found in section B.3. In the simulations the voltage on the p-metal gate was swept from 1 to -1 volt with the substrate and the n-gate biased at zero volt. Followed by a sweep of the n-gate from -1 to 1 Volts while both the p-gate and substrate were biased at zero Volts. In figure 4.1 we show the IV characteristics for an aMSM-diode with $Li = 0.1$ were work functions were employed extracted from our experiments or from the literature, see table B.2 for their exact values.

The modeled and simulated characteristics are very comparable. The most important deviations can be observed in the far forward regime. Here the voltage is bigger then the flatband voltage. In our theory we used either the drift or the diffusion equations to find the current. In reality both of them have to be solved simultaneously to find a good model for the current in for high forward voltages. In figure 4.1 we present the results for a diode with workfunctions according to literature, ($\phi_{mn} = 4.20$ eV, $\phi_{mp} = 5.10$ eV) as discussed in section B.2) , and varying length $Li$. The SRH-current is heavily dependent on $Li$ and shows up for reverse ($V_A > 0$) and small forward biases. For the small forward biases the SRH-current in the simulation is much lower then in our model. The discrepancy of the latter is not clear yet. In far forward the current in the intrinsic region becomes limited by drift, which scales inversely with $Li$.

The length of the intrinsic gate $Li$ is the only parameter of the aMSM-diode which can be scaled. By increasing the length both SRH-current (and off current) will increase and the far forward might decrease. Hence one would prefer a short $Li$ although there is a situation where a long $Li$ is preferable. The field across the silicon increases with reverse bias. When this field becomes high enough an avalanching current will start to flow. This field can be reduced by increasing the length $Li$ of the silicon. Hence the aMSM-diode with ideal work functions can either be optimized by scaling $Li$ for a high reverse breakdown voltage and low far forward current, long $Li$, or a low reverse current high high far forward current, short $Li$.
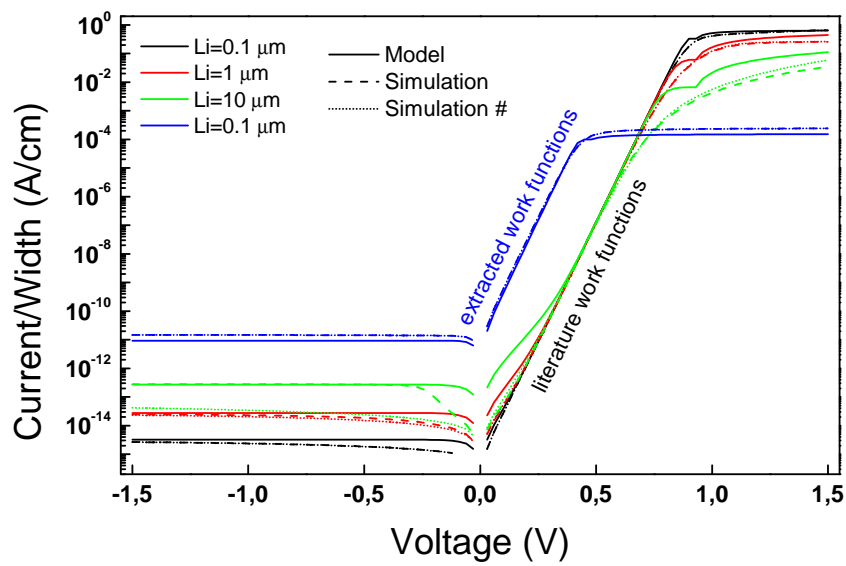
**Figure 4.1:** (a) The simulated and modeled IV characteristics of an aMSM-diode with either literature or extracted metal work functions and geometries as in appendix B.2, in the simulations we swept either the voltage on the p-gate (indicated by dashed lines), or the n-gate (dotted lines) For the literature work functions we show the current dependence on the length of the intrinsic region $Li$. In reverse the currents increases with $Li$ due an increased SRH-current. In forward the current decreases with $Li$

## 4.2    The Charge Plasma Diode

In this section we will discuss some simulation and modeling results on the CP-diode.
Here the substrate is always biased at zero Volts, unless states otherwise. Often we
will use device A2x from the tabels B.4 and B.5. The most important parameters are
$tsi = 20nm$, $Ln = Li = Lp = 2$ $\mu$m, $\phi_{mn} = 4.20$ eV, $\phi_{mp} = 5.10$ eV and $tbox = 1$ $\mu$m.

### 4.2.1    Charged Plasma

In section 2.3.2 we derived a formula in which electrostatics under the gates have been
incorporated, see equation 2.42. In figure 4.2 (a) we show the simulated and modeled
conduction band, valence band, hole and electron quasi Fermi level under small forward
bias. For a comparison both oxide conduction bands energy level at the oxide metal
interface have been used as a reference. The forward voltage results in a distance $V_A$
between both quasi Fermi levels in the silicon. In this example the work function of the
metal gate is 4.2 eV, the silicon electron affinity is 4.07 eV. Therefore the metal pulls
down the surface potential in the silicon. This results in a low field in the front oxide and
silicon.

In figure 4.2 (b) we show the electron and hole density under the same gate and bias.
The amount of electrons is given by the work function difference. The amount of holes
is increased by a factor $e^{V_A/u_t}$. The amount of electrons decreases slightly for increasing
distance from the front oxide and thus metal gate. In section D additional graphs can be
found for zero bias on the n-gate, forward and zero bias on the p-gate. Again our model
is in good agreement with simulation results.



(a) Band Diagram                          (b) Carrier Density
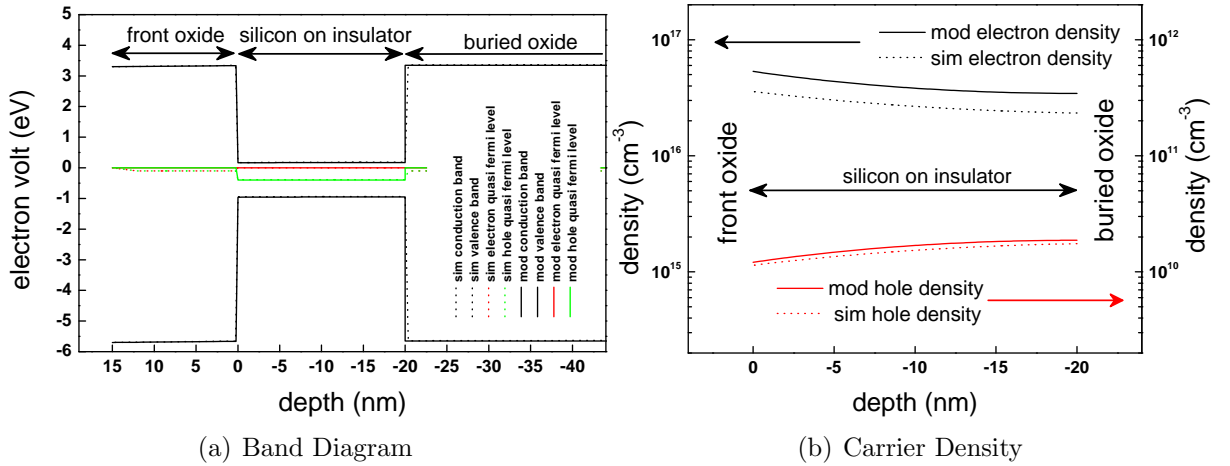
**Figure 4.2:** (a) Modeled and simulated band diagram and (b) carrier density
along axis B in figure 2.6 when a bias of 0.4 V is applied on the
p-gate.

### 4.2.2    Diffusion Current

In figure 4.3 (a) we show the simulated band diagram along axis C in figure 2.6 in forward
condition. Under the n-gate ($-2..0$ $\mu$m on the x-axis) the electron quasi Fermi level
is located close the conduction band, hence an electron plasma is formed. The distance
between the hole and electron quasi Fermi level is governed by the applied forward voltage.

This increases the number of minority carriers, (holes under n-gate, electrons under the p-gate) by a factor $exp(V_A/u_t)$.

In the intrinsic region (0..2 $\mu$m on the x-axis) the quasi Fermi levels are constant. In this region the derivative of the bands is not constant. This is caused by the influence of the substrate. It is assumed to have a boron doping concentration of $10^{15}$ cm$^{-3}$ hence it pulls the bands to a potential quite close to the region under the p-gate. Note that this effect is not included in our model for the CP-diode. In figure 4.3 (b) the carrier densities are shown as well. The slope of the electron concentration under the p-gate is constant and quite small, the electron concentration reaches its minimum (except for area $Lon$ and $Lop$, which we dont take into account) and the field in the areas under the gates ($Ln$ and $Lp$) is approximately zero. Therefore the electron current is limited by the diffusion of electrons under the p-gate. For similar reasons the hole current is limited by the diffusion of holes under the n-gate.



(a) Band Diagram

(b) Carrier Density
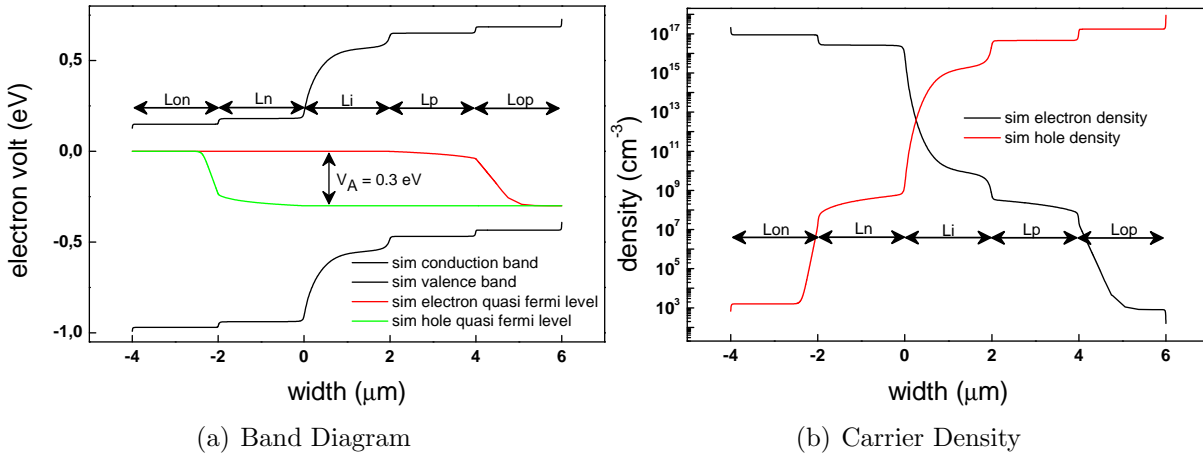
**Figure 4.3:** (a) A simulated band diagram along axis C in figure 2.6. The separation between the quasi Fermi levels is given by the forward voltage $V_A$. (b) The carrier concentrations in forward. The transport of carriers is limited by diffusion of holes under the n-gate and electrons under the p-gate.

To discuss diffusion as a possible transport mechanism in far forward we will now show some simulation results for a device with: short $Li = 0.1$ $\mu$m to get rid of the influence of the resistance of the intrinsic region, extracted work functions and with $Lon$ and $Lop = 0$ to show diffusion and not a very complicated combination of different mechanisms, although this is still a little bit the case. In figure 4.4 (a) we show a band diagram for this device in far forward. For this device the dominant current is the hole current. In the regions $Lp$ and $Ln$ the field is approximately zero, therefore the drift current in this regions is zero and the current has to depend on diffusion in the $Lp$ region.

In figure 4.5 we present the simulated and modeled IV characteristics of the CP diode with work functions according to literature and with the extracted values. The simulated curves have been made by both applying a voltage on the p-gate or applying the voltage with a minus sign on the n-gate. In all cases our model predicts the current quite well. For the literature work functions the reverse current becomes so low that the SRH-current becomes important.

The SRH-model accurately predicts the reverse current, unexpectedly however for small forward biases (0.1 V) the predicted SRH-current is too high. The reason for

(a) Band Diagram



(b) Carrier Density
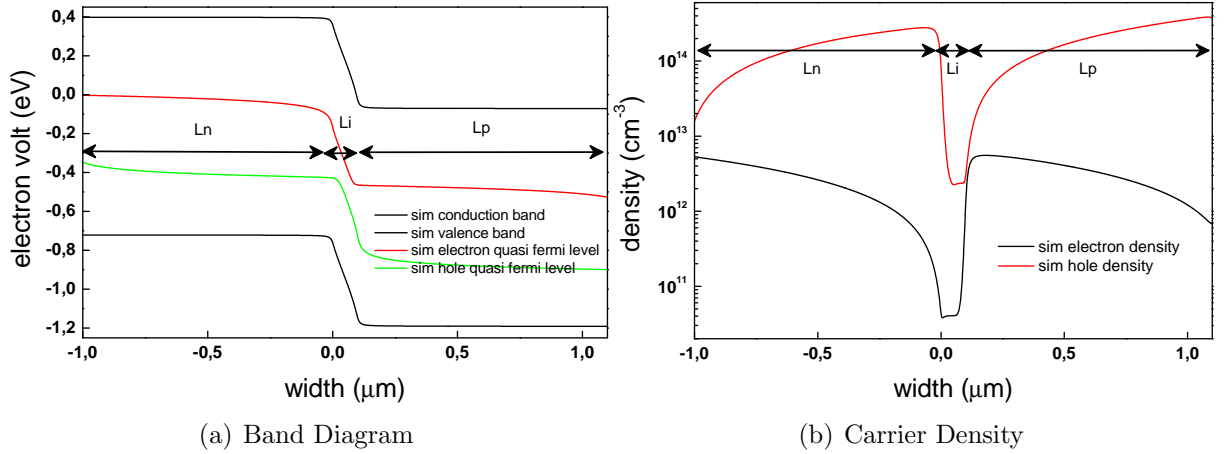
**Figure 4.4:** (a) A simulated band diagram along axis C in figure 2.6 in far forward, here 0.9 Volts . Here the extracted work functions have been used to simplify the picture. (b) The corresponding carrier concentrations. The electric field is very low in the Lp region, however the quasi Fermi level has a slope. Hence the diffusion of carriers in this region has to be taken into account to derive the total current.

the discrepancy is not clear (yet). Experiments are required to investigate this. The simulated black curve, in which the extracted work functions have been used, shows a slight difference in far forward depending on varying the potential on either the p-gate or n-gate. In far forward the current is determined by the diffusion of holes under the n-gate. A negative voltage is applied on this gate which pulls op the band diagram in the silicon body. Unforturnately the substrate, biased at zero volts, tries to pull it down an hence reduces the number of electrons in the silicon under the n-gate, resulting in a difference between applying a bias on either the n-gate or the p-gate. This effect was observed in carbon-nanotube rectifiers, however the reason for this effect was not explained [27].

We also varied the gate lengths $Ln$ and $Lp$ relative to each other. The exact dimensions can be found in section B.3 for devices F1-F5. In case of the use of the extracted work functions the current is mainly determined by the transport of holes. Hence under forward conditions the current is determined by the diffusion of holes under the n-gate. So the current should scale inversely with the length of the n-gate. In figure 4.6 (a) we show this depence for the current when $V_A = 1/2V_{FB}$. The graphs show a linear dependence on $1/Ln$. For far forward we demonstrate the same in figure 4.6 (b), these currents are dependent on the diffusion of holes under the p-gate and hence scale with $1/Lp$.

We performed the same simulations with literature work functions. Because now neither electron nor hole current can be neglected the dependence of the total current on the gate lenght will be different. In table 4.1 we present the ratio of the modelled and simulated current at forward ($V_A = 0.5 \cdot V_{FB}$) and far forward ($V_A = 1.5 \cdot V_{FB}$) biases for different gate lengths. In forward the model estimates the current a little bit too high. In far forward a little bit to low. The deviations are quite small hence the model dependence on the gate length is correct. The small discrepancies could be caused by the fact that the model is a quasi-2D model in which the influence of the substrate has not been incorporated.
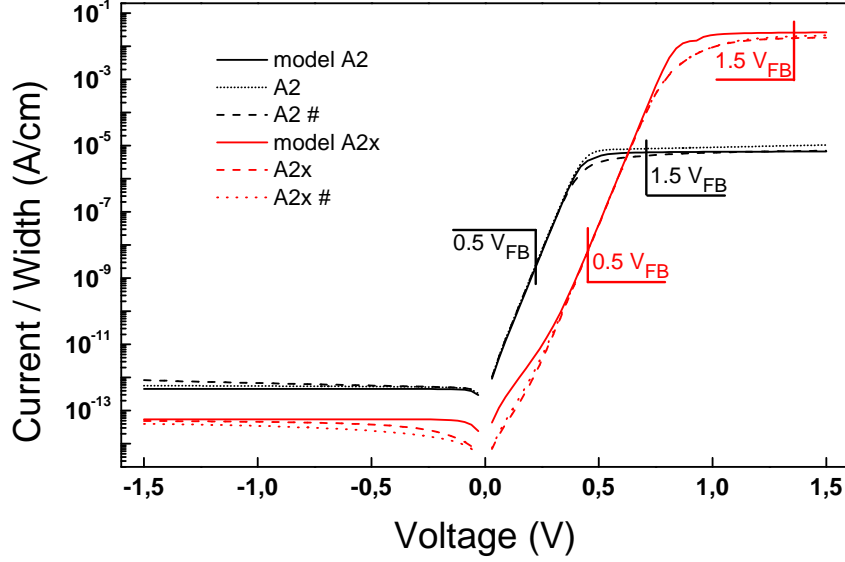
**Figure 4.5:** The modeled and simulated IV characteristics of the CP diode
with literature (red) and extracted (black) work functions. The
simulation was done by applying a bias on either the p-gate
(dashed) or the n-gate (dotted). The model predicts the IV char-
acteristics quite well.

**Table 4.1:** The ratio of the modelled and simulated current for varying gate
lengths and literature work functions. All other parameters can be
found in section B.3. The results are all close to 1 so they confirm
the accuracy of our model.

| $Ln$ ($\mu$m) | $Lp$ ($\mu$m) | $J_{mod}/J_{sim}$ $0.5V_{FB}$ | $J_{mod}/J_{sim\#}$ $0.5V_{FB}$ | $J_{mod}/J_{sim}$ $1.5V_{FB}$ | $J_{mod}/J_{sim\#}$ $1.5V_{FB}$ |
|---|---|---|---|---|---|
| $8,9$ | $0,9$ | $0,8$ | $0,78$ | $1,37$ | $1,33$ |
| $6,9$ | $2,9$ | $1,07$ | $1,04$ | $1,64$ | $1,57$ |
| $4,9$ | $4,9$ | $1,15$ | $1,13$ | $1,83$ | $1,62$ |

(a) Off Current

(b) On Current
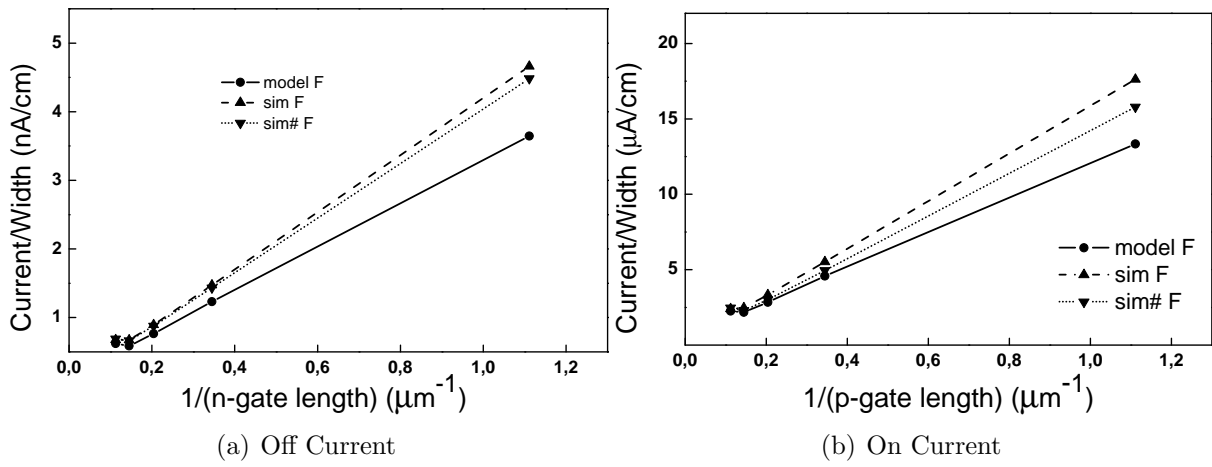
**Figure 4.6:** The current obtained through modeling and simulation (dashed and dotted lines) of CP-diodes in which the extracted wok functions were used. The current is determined mainly by the hole current. The exact geometries can be found in section B.3.(a) In forward ($V_A = 0.5V_{FB}$) conditions the current scales inversely with the n-gate length, (b) In far forward ($V_A = 1.5V_{FB}$) the current scales inversely with the p-gate length. The results confirm that the diffusion of holes, under the n-gate in forward and reverse, and under the p-gate in far forward, is the dominant transport mechanism.

## 4.3   A Comparison

In this section we discuss how the CP-diode gate lengths can be optimized. When the work functions of the metals are such that the electron density under the p-gate is much lower then the hole density under the n-gate. Then the "off" or reverse current is determined mainly by the hole diffusion under the n-gate and can be reduced by increasing $Ln$. By equating equations 2.36 and 2.37 the $Ln$ where both electron and hole reverse current are equal can be found:

$$Ln = \frac{p_n D_p}{n_p D_n} Lp,\tag{4.1}$$

where $p_n$ is the hole concentration under the n-gate, see equation 2.34, $n_p$ is the electron concentration under the p-gate, given by equation 2.33. We can enhance the far-forward hole current by decreasing $Lp$. Unfortunately this will help until the current becomes limited by thermionic emission from the metal silicon contacts. In figure 4.7 the contour plots of the on/off current ratio and maximum current of a CP-diode with varying gate lengths and extracted work functions $\phi_{mn} = 4.47$, $\phi_{mp} = 4.90$ eV are shown.

For small $Ln$ and $Lp$ the currents are limited by thermionic emission and hence the device characteristics would be approximately equal to those of an aMSM-diode. For large $Ln$ and small $Lp$ the on/off current ratio of the device is increased by a factor 10 compared to short $Ln$ and $Lp$. Hence we can conclude that when we make an aMSM-diode with work functions such that one is close to the center of the bandgap of silicon and one is further away, at least by $> 0.1$ eV, then switching to a CP-diode with a gate at the metal contact which work function is closest to silicon midgap (in our example $\phi_{mn}$) can improve the on/off current ratio.

The CP-diode might also show a better performance then an aMSM-diode when the barrier height of the Schottky contacts can be improved by adding a dielectric between the metal and the silicon. Now the gates have more ideal influence on the intrinsic silicon and a better performance might be realized.

In figure 4.8 we show contour plots of both the on/off current ratio and the on current for a CP diode with varying gate lenghs and literature work functions. In this case both work functions are seperated equally from silicon midgap. Therefore the device performance cannot be increased compared to the aMSM-diode (where both gates are zero, lowerleft in the figure).

## 4.4   Scaling the CP-diode

We showed that the model accurately predicts the simulated currents. Now we can use the model to discuss how optimal device performance can be reached.

**Intrinsic region length $Li$**

The SRH-current scales with $Li$ (see equation 2.15), the far forward intrinsic region resistance current, see equations 2.13 and 2.14, with $1/Li$, hence for far from midgap work functions, or actually the literature work functions, a short $Li$ is desireable to get a high on/off current ratio. For closer to midgap work functions, or actually the extracted work functions the reverse current is not as low, hence the SRH-current doesn't play an important role. Still the far forward current might be limited by $Li$. Another performance

(a) On/Off Current Ratio                    (b) Maximum Current Density
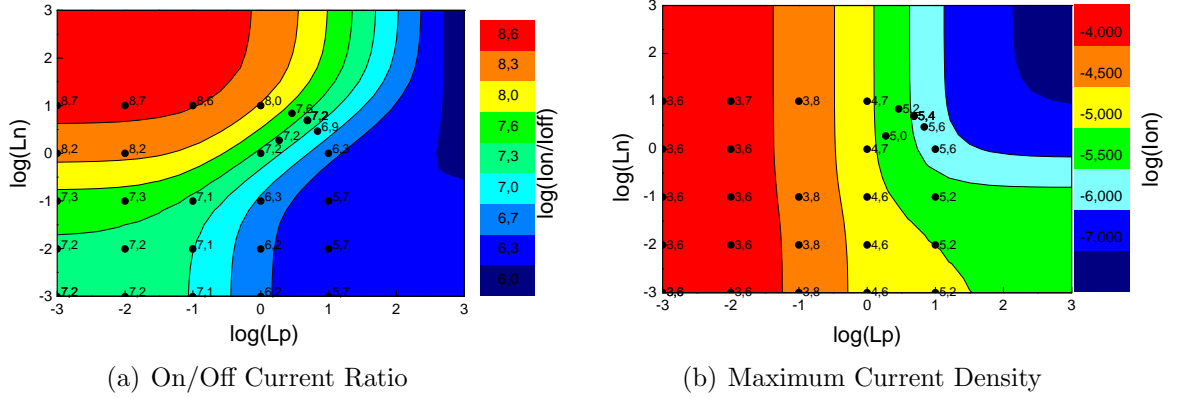
**Figure 4.7:** For a device with work functions such that the hole density under
the n-gate is much higher then the electron density under the p-
gate , then the gates can be scaled to improve the on/off current
ratio by a factor 10 compared to the aMSM-diode (where $Ln = Lp = 0$). The contour plot is made with the model. The black
dots indicate simulation data to check the validity of the model.
(a) For a relatively short $Lp$ and long $Ln$ a maximum of the on/off
current ratio is found. (b) $Lp$ can be used to scale the power of
the device.

characteristic could be the reverse breakdown voltage. This was studied by Rajasekharan
et al. [7], who showed that a long intrinsic region would be desireable. So devices which
have a high reverse breakdown voltage will automatically show a not very high on/off
current ratio.

### The gate lengths $Ln$ & $Lp$

In section 2.3.3 and 4.2.2 we showed that the diffusion of carriers under these gates
mainly determines the total current. When the metal work functions are chosen such
that both electron and hole transport are important then the reduction of $Lp$ results in
an increased far forward hole current and increased reverse electron current, see equations
2.38 respectively 2.37. If we decrease $Ln$ the far forward electron and reverse hole current
will decrease, see equations 2.38 respectively 2.36 . Hence the device will be allowed to
carry more current but the on/off ratio will not improve. Therefore we suggest to use
short gate lengths when the work functions are chosen such that both electron and hole
current are important.

When the extracted work functions are used the hole current is much higher then
the electron current. In this case we can increase $Ln$ to reduce the hole reverse current,
see equation 2.36, to reach a higher on/off current ratio and reduce $Lp$ to increase the
maximum current through the device, as shown in equation 2.38.

### The overlap gate lengths $Lon$ & $Lop$

Depending on the barrier height, resistance and bias the current might flow partly through
the overlap area. Hence it might be interesting to have a $Lon$ and $Lop$ region in which
the current flows from the silicon into the metal and vice versa. The exact relationship

(a) On/Off Current Ratio

(b) Maximum Current Density
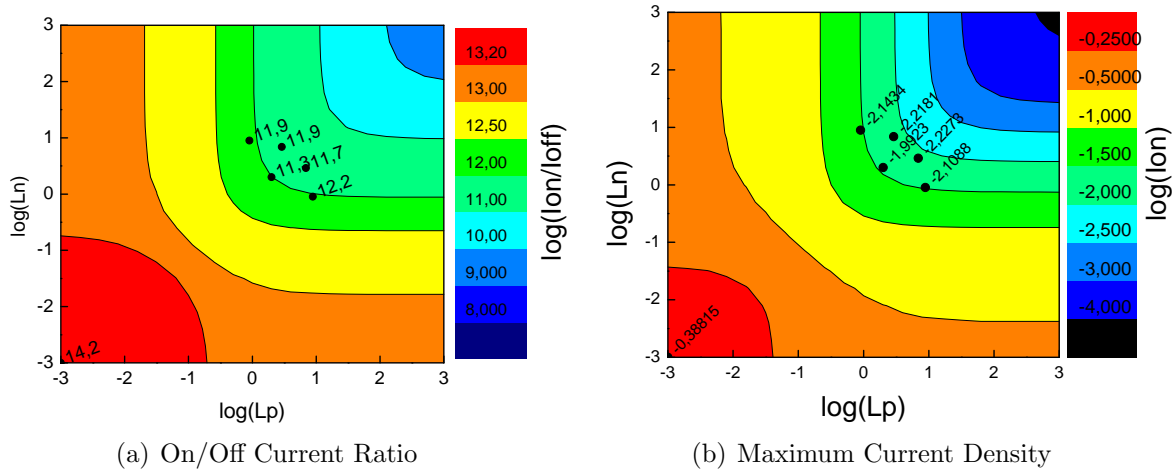
**Figure 4.8:** The on/off current ratio and on current of CP-diode diode with varying $Ln$ and $Lp$. The literature metal work functions have been used. The contours are made with the model. The black dots indicate simulation data to check the validity of the model. The literature work functions have been used. The gate lengths have been varierd. (a) The on/off current ratio can be maximized by using no or just one gate.(b) The on current can be scaled by adding two gates. But the device performance cannot be improved compared the aMSM-diode, where $(Ln = Lp \approx 1nm = 10^{-3})$

hasn't been investigated in this work. Still we can conclude that it will not decrease the device performance.

### The front oxide layer thickness $tfoxp$ and $tfoxn$

When we increase the oxide thickness in equation 2.30 the delta potential $\Psi(0)$ will decrease, which results in reduced minority carrier densities under the gates, given by equations 2.33 and 2.34. Therefore the off current, shown in equations 2.36 and 2.37 will increase. This is not desireable, therefore the oxide should be as thin as possible. On the other hand a leakage current through the oxide will result in a deviation from our model and perhaps will improve our device. Hence we should have gate dielectric which has a high dielectric constant and is thick enough to prevent tunneling. Tunneling through the dielectric might also be able to reduce the effective gate lengths and hence increase the on/off current ratio of a device where either electron or hole transport is dominating the current. This might by topic for future research.

### The silicon layer thickness $tsi$

A thicker silicon will result in a lower on/off current ratio due to large minority carrier concentration at the silicon buried oxide interface. This is illustrated in figure 2.7. An increase in $tsi$ will result in a lower $\Psi(0)$ and therefore in increased minority carrier at the silicon buried oxide interface resulting in a higher reverse current. How much exactly depends on the front oxide thickness, work functions, BOX layer thickness and substrate bias. The topic of the influence of the substrate silicon has to be investigated further to

lead us to a trade-off.

**Buried oxide (BOX) layer thickness** *tbox*

The thicker the buried oxide, the less is the influence of the substrate which tends to reduce the number of carriers under the gate and to pull on the energy bands in the intrinsic region. In fact, this depends on the ratio of the oxide capacitance of the BOX layer and the depletion capacitance of the intrinsic region as discussed by Rajasekharan [7]

# Chapter 5

# Conclusions

## 5.1 Contribution of this work

- By applying the well known Schottky theory of metal semiconductor junctions to aMSM-diodes an analytical model for the DC IV characteristics has been derived. Both holes and electrons have to cross a relatively high barrier while traveling through the diode, hence both current contributions can be equally important for the total current. This is in contrast to a standard Schottky rectifier, where the use of a relatively high doping and long channel results in a high resistance and negligible current contribution of either holes or electrons. Also a simple model for the SRH-current was implemented, which mainly depends on the length of the intrinsic region $Li$.

- The model of the aMSM-diode is verified using the Synopsys Sentaurus Device simulator. This was done by varying the length of the intrinsic region $Li$ and the work functions of the metals. The model only deviates for long $Li$ in which the resistance of the semiconductor should be taken into account.

- The on/off current ratio of the aMSM-diode is found to scale exponentially with the work function difference of the metals. Also $Li$ can be scaled to improve the performance. A long $Li$ will result in a high reverse breakdown voltage and high SRH-current, a short $Li$ will do exactly the opposite.

- The theory of FinFET's can be used to derive the carrier concentrations under the gates of the CP-diode in equilibrium. From this we can derive the diffusion of carriers from the intrinsic region interfaces to the metals in both reverse and forward conditions. This situation is very comparable to the standard PN-diode theory. When the applied forward bias is greater than the work function difference, i.e. that the device is in far forward, the diffusion current will be limited by the carriers formed by and flowing from the metal contacts to the intrinsic regions. When the gate lengths $Ln$ and $Lp$ are relatively short the current through the diode will eventually be limited by thermionic emission, which is comparable to the aMSM-diode.

- The Synopsys Sentaurus Device simulator has been used to verify the CP-diode model under DC conditions. Again for large $Li$ the series resistance of the semiconductor is neglected in the model. The model does not take the influence of the substrate into account, it is a quasi-2D model. This results in deviations especially

for thick silicon layers, high work functions differences and long $Li$. Still under reasonable conditions the model can predict the simulation results with in factor 1.5. Hence the model can help us to understand the DC IV characteristics of the CP-diode as shown in this work.

- When one of the metal work functions is much closer to silicon midgap then the other, then the current is mainly determined by the transport of either holes or electrons. Only then the gates of the CP-diode can be scaled such that the on/off current ratio of the CP-diode is superior to the aMSM-diode.

- The barrier heights of metal semiconductor junctions can be thoroughly investigated by IV measurements varying the temperature. For ideal contacts the sum of the electron and hole barrier should equal the bandgap and the ideality factor should be close to 1. From characterization results we can conclude that Erbium and an alloy of Palladium and Titanium are most suitable as a metal contact for a CP-diode fabricated in the Mesa+ cleanroom. According to the theory this diode will have on/off current ratio of $1.2 \cdot 10^7$ when both gate lengths are equal or if we make an aMSM-diode with these metals. If we make a CP-diode with $Ln \geq 10$ $\mu$m and $Lp \leq 0.1\mu$ the on/off current ratio increases to $2.4 \cdot 10^8$.

- If the addition of oxide between the metal and semiconductor leads to less interface states and oxide charge, then the performance of a CP-diode might also prove superior to that of an aMSM-diode.

- Both the CP and aMSM-diode do not require doping and both are probably compatible with FinFET technologies. Depending on the available metals, their barrier heights, the amount of fixed charge and interface states the CP-diode could be a better candidate than an aMSM-diode.

## 5.2   Recommendations for further work

- The model for the DC IV characteristics of both the aMSM and CP-diode should be verified by measurement on real devices with varying gate lengths and known semiconductor metal barrier heights.

- Before the the CP-diode can be selected as a probable candidate for future technologies the high frequency and switching behavior should be investigated using modeling, simulation and characterization. Because the CP-diode contains a larger area with charge compared to the aMSM-diode an reduced high frequency performance can be expected.

- The influence of the metal overlap lengths $Lon$ and $Lop$ on the maximum thermionic emission current should be included in our model. This will result in a slightly higher maximum thermionic emission current.

- For very thin gate oxides a tunneling current will be present. It is not known yet if this will improve or reduce the device performance.

- When $Li$ is scaled into the nanometer regime a band to band tunnel device is realized without using doping. This might be interesting.

- The reverse breakdown characteristics are heavily dependent on the field in the intrinsic region. for long $Li$ the substrate will influence this field, hence it is not granted that the reverse breakdown voltage will scale linearly with $Li$.

## 5.3 Acknowledgement

I would like to thank the following persons for their support;

**Ray Hueting** For the many fruitful discussions we had which resulted in a lot of good ideas. Also for his very thoroughly review of the first versions of my thesis.

**Jan-Laurens van der Steen** For his support on the Synopys Sentaurus simulation tools.

**Bijoy Rajasekharan** For the fabrication and measurement of metal semiconductor test structures.

**Cora Salm** For her interpretation of the metal semiconductor characterization results.

**Juriaan Schmitz** For providing me with a job as PhD. candidate at the Semiconductor Components Laboratory at the University of Twente.

**Annemiek Janssen** For her administrative support during my master studies.

# Appendix A

# A solution too the Poisson equation in a gated silicon body

In this section we demonstrate the validity of a solution for the function $\Psi(y)$ in the Poisson equation 2.25. Taur suggests [19],[20] the following function;

$$\Psi(y) = \Psi(0) - 2u_t \ln \cos(\beta y), \tag{A.1}$$

where

$$\Psi(0) = u_t \ln \frac{2\beta^2}{\delta} \tag{A.2}$$

To demonstrate the validity we have to derive the second derivative;

$$\frac{\delta \Psi(y)}{\delta y} = \frac{2u_t \beta \sin \beta y}{\cos \beta y} = 2u_t \beta \tan \beta y, \tag{A.3}$$

and hence:

$$\frac{\delta^2 \Psi(y)}{\delta y^2} = \frac{2u_t \beta^2 \cos \beta y}{\cos \beta y} + \frac{2u_t \beta^2 \sin^2 \beta y}{\cos^2 \beta y} = \frac{2u_t \beta^2}{\cos^2 \beta y} \tag{A.4}$$

Now we have found both derivatives we can check whether the function proposed by Taur, equation A.1, satisfies the Poisson equation 2.25.

$$\frac{\delta^2 \Psi(y)}{\delta y^2} = u_t \delta e^{\frac{\Psi(y)}{u_t}} = u_t \delta \frac{1}{\cos^2 \beta y} \frac{2\beta^2}{\delta} = \frac{2u_t \beta^2}{\cos^2 \beta y} \tag{A.5}$$

Hence the function proposed by Taur is a valid solution to the Poisson equation. QED.

# Appendix B

# Simulation Information

## B.1  The Device Simulator

As a device simulator we used the Synopsys Sentaurus Device simulator. Here the Schottky contacts are modeled by the model proposed by Schenk [28], according the Synopsys user guide [22] the following boundary conditions hold:

$$\phi = \phi_F - \phi_B + 2u_t \ln(\frac{N_C}{n_{i,eff}}), \tag{B.1}$$

where $\phi_F$ is the Fermi potential at the contact. The thermionic emission currents are then given by;

$$\overrightarrow{J_n} \cdot \widehat{n} = qv_n(n - n_0^B), \tag{B.2}$$

and:

$$\overrightarrow{J_p} \cdot \widehat{p} = qv_p(p - p_0^B), \tag{B.3}$$

where $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ denote the electron and hole current density vectors, $n_0^B$, $p_0^B$ are the equilibrium densities. The default values for the thermionic emission velocities $v_n$ and $v_p$ are $2.573 \cdot 10^6$ cm/s and $1.93 \cdot 10^6$ cm/s respectively, which are according to the Richardson constants given in table 2.1. The bandgap $E_G$ is modeled temperature dependent as described in [29]. The temperature dependence of the Silicon electron affinity $\chi_{Si}$ is the same as the bandgap $E_G$ but with a minus sign. The electron effective density $N_C$ of states is temperature dependent as proposed by Green [30]. The hole effective density of states $N_V$ is temperature dependent as shown by Lang [31].

To incorporate the SRH-current the following form for the recombination rate implemented:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_{i,eff}e^{(E_{trap}/kT)}) + \tau_n(p + n_{i,eff}e^{(-E_{trap}/kT)})}, \tag{B.4}$$

where $E_{trap}$ is the difference between the defect and the intrinsic Fermi level. For recombination or generation both an electron and a hole are required. With $E_{trap}$ set at 0 recombination is most likely to occur, because both the electron and hole require the same energy. The carrier lifetimes $\tau_n$ and $\tau_p$ are modeled temperature dependent as proposed by [32] respectively [33]. Because we model a lowly-doped silicon layer we neglected the doping dependence of the carrier lifetimes.

The temperature dependent mobility model of Lombardi [34] was implemented to take the temperature dependence into account. Furthermore we used the Philips unified mobility model as shown by Klaassen [35] to describe the majority and minority carrier bulk mobilities. This model also describes electron-hole scattering, screening of ionized impurities by charge carriers and clustering of impurities. To take surface scattering into account the enhanced Lombardi [34] model was used. We also tried to take the field dependent mobility into account using the Hänsch or extended Canali model as proposed by Darwish [36], unfortunately this led to convergence problems when the theoretical work functions were implemented. Hence we didn't use the Lucent mobility model to keep all the simulation data consistent.

**Table B.1:** The aMSM-diode parameters which were kept constant.

| tox | tsi | tbox | tbsi | Doping | SOI | BSI |
|------|-------|---------|---------|--------|-----------------------|-----------------------|
| 10 nm | 20 nm | 1 $\mu$m | 1 $\mu$m | Boron | 6E13 cm$^{-3}$ | 1E15 cm$^{-3}$ |

**Table B.2:** The aMSM-diode parameters which were varied.

| Label | $\phi_{mn}$ | $\phi_{mp}$ | Li |
|-------|-------------|-------------|-----------|
| Z1 | 4.47 | 4.90 | 0.1 $\mu$m |
| Z2 | 4.47 | 4.90 | 1 $\mu$m |
| Z3 | 4.47 | 4.90 | 10 $\mu$m |
| Y1 | 4.20 | 5.10 | 0.1 $\mu$m |
| Y2 | 4.20 | 5.10 | 1 $\mu$m |
| Y3 | 4.20 | 5.10 | 10 $\mu$m |

# B.2   aMSM-diode Parameters

In table B.1 and B.2 we show the parameters of the simulated aMSM-diodes. The metal work functions $\phi_{mn}$ and $\phi_{mp}$ are discussed in section B.3

**Table B.3:** Work functions of the simulated devices

|                            | $\phi_{mn}$ | $\phi_{mp}$ |
|----------------------------|-------------|-------------|
| extracted work function    | 4.47 eV     | 4.90 eV     |
| **literature work function** | 4.20 eV   | 5.10 eV     |

**Table B.4:** Constant device geometry for the simulated CP diodes

| tfoxn  | tfoxp  | tbox        | tbsi        | Lon         | Lop         |
|--------|--------|-------------|-------------|-------------|-------------|
| 15 nm  | 15 nm  | 1 $\mu$m    | 5 $\mu$m    | 2 $\mu$m    | 2 $\mu$m    |

# B.3    CP-diode Parameters

In table B.3 we summarize the different metal work functions which we used for the simulations. Note the that work function $\phi_{mn}$ and $\phi_{mp}$ originate either from the extracted barrier heights in section 3.3 for Erbium 4.47 eV and PdTi$_{7\%}$ or from literature, as shown by Michaelson [37] with Gallium 4.20 eV and Gold 5.10 eV. In table B.4 we show the parameters which have not been varied. In table B.5 we show the CP-diode parameters which have been varied en their corresponding label.

**Table B.5:** Variation in device geometry for devices A1-C4.

| tag | tsi (nm) | Li ( $\mu$m) | Ln ( $\mu$m) | Lp ( $\mu$m) |
|---|---|---|---|---|
| A1 | 10 | 2 | 2 | 2 |
| A2 | 20 | 2 | 2 | 2 |
| A3 | 30 | 2 | 2 | 2 |
| A4 | 60 | 2 | 2 | 2 |
| A5 | 100 | 2 | 2 | 2 |
| A6 | 200 | 2 | 2 | 2 |
| A7 | 300 | 2 | 2 | 2 |
| B1 | 20 | 0.25 | 4.875 | 4.875 |
| B2 | 20 | 0.50 | 4.75 | 4.75 |
| B3 | 20 | 1 | 4.5 | 4.5 |
| B4 | 20 | 2 | 4 | 4 |
| C1 | 20 | 0.25 | 4.875 | 4.875 |
| C2 | 20 | 0.25 | 2.375 | 2.375 |
| C3 | 20 | 0.25 | 1.875 | 1.875 |
| C4 | 20 | 0.25 | 0.875 | 0.875 |
| D1 | 10 | 0.2 | 4.9 | 4.9 |
| D2 | 10 | 0.2 | 2.4 | 2.4 |
| D3 | 10 | 0.2 | 1.9 | 1.9 |
| D4 | 10 | 0.2 | 0.9 | 0.9 |
| E1 | 30 | 0.2 | 4.9 | 4.9 |
| E2 | 30 | 0.2 | 2.4 | 2.4 |
| E3 | 30 | 0.2 | 1.9 | 1.9 |
| E4 | 30 | 0.2 | 0.9 | 0.9 |
| F1 | 20 | 0.2 | 8.9 | 0.9 |
| F2 | 20 | 0.2 | 6.9 | 2.9 |
| F3 | 20 | 0.2 | 4.9 | 4.9 |
| F4 | 20 | 0.2 | 2.9 | 6.9 |
| F5 | 20 | 0.2 | 0.9 | 8.9 |
| G1 | 20 | 0.1 | 1 | 1 |
| G2 | 20 | 0.1 | 10 | 1 |
| G3 | 20 | 0.2 | 10 | 0.1 |
| G4 | 20 | 0.2 | 10 | 0.01 |
| G5 | 20 | 0.2 | 10 | 0.001 |

# Appendix C

# Input files

## C.1  Structure file

```
# generic input file I(V) simulation for PIN diode
# read input filename
set infile [open "file.cur" r]
set fname [gets $infile]
close $infile
# Front metal work function
set NWFF "N$WFn"
# Back metal work function
set NWFB "P$WFp"
# set local variables
set pre   "$NWFF${NWFB}T${TEMP}_SRM_"
set mshf "_msh.tdr"
# set dopf "_msh.tdr"
set datf "_des.dat"
set pltf "_des.plt"
set logf "_des.log"
# set terminal bias value, F(ront) and B(ack)
set VS 0.10
set VFINI 1.50
set VFEND -1.50
set VZ 0.0


# initial solution
sdevice_init "
    File {
        Grid    = \"$fname$mshf\"
        Plot    = \"$fname$pre$datf\"
        Current = \"$fname$pre$pltf\"
        Output  = \"$fname$pre$logf\"
    # parameter file for Lucent mobility model
        Parameter = \"lucent.par\"
    }
    Electrode {
        { Name=\"nmetal\"   Voltage=$VZ  Schottky Workfunction=$WFn}
        { Name=\"pmetal\"   Voltage=$VS  Schottky Workfunction=$WFp}
        { Name=\"back\"   Voltage=$VZ }
    }
    Physics {
        # set temperature as defined in sim.sh
        -eQuantumPotential
        -hQuantumPotential
        Temperature=$TEMP
        EffectiveIntrinsicDensity( Slotboom )
    # Lucent mobility model  eHighFieldSaturation hHighFieldSaturation
        Mobility( PhuMob Enormal)
        Recombination(
            SRH(
                TempDependence
            )
        )
    }
    # To include barrier lowering and valence band tunneling
    # Physics(electrode = \"nmetal\") {BarrierLowering Recombination(eBarrierTunneling)}
    # Includes barrier lowering : Image force
    #Physics(electrode = \"nmetal\") { BarrierLowering }
    #Physics(electrode = \"pmetal\") { BarrierLowering }
    # quantities to be shown in 2D cross-section (Tecplot)
    Plot {
        Doping
        DonorConcentration
        AcceptorConcentration
        EffectiveBandGap
        ConductionBandEnergy
        ValenceBand
        SpaceCharge
        ElectricField
        Potential
        eDensity
        hDensity
        eMobility
        hMobility
        eCurrent
        hCurrent
        eVelocity
        hVelocity
        SRHRecombination
        eQuantumPotential
        hQuantumPotential
    }
    # plot the following quantities at coordinates (X Y) in Inspect
    CurrentPlot {
```

```
        Potential ((0.0 0.0))
        eDensity ((0.0 0.0))
        hDensity ((0.0 0.0))
    }

    # some math options. no need to change these
    Math {
    Wallclock
        RelErrControl
        Number_of_Threads=maximum
        Extrapolate
        Iterations=200
        cnormprint
        #RhsMin=1E-1
        #Digits=10

    # stop simulation if draincurrent is smaller than 1E-15 A/um
        #BreakCriteria
        #{
        #   Current (Contact = \"nmetal\" minval = 1E-15)
        #}
    }
    # nonlocal tunneling depth in cm
    #Math(Electrode=\"pmetal\"){
    #Nonlocal(Length=10e-7)
    #}
"

# solve initial conditions
sdevice_solve "
    Solve {
        Poisson
        Coupled { Poisson }
        Coupled { Poisson hQuantumPotential}
        Coupled { Poisson eQuantumPotential hQuantumpotential}
        Coupled { Poisson Hole eQuantumPotential hQuantumpotential}
        Coupled { Poisson Electron Hole eQuantumPotential hQuantumpotential}
        #Save ( FilePrefix=\"$fname${pre}VSTART\" )
    }
"

# ramp to pmetal initial conditions
    sdevice_solve "
        Solve {
            Quasistationary
            (
                InitialStep=0.01
                MaxStep=0.2
                MinStep=0.001
                Increment=1.3
                Decrement=2
                Goal { Name=\"pmetal\" Voltage=$VFINI }
            )
            {
                Coupled ( Iterations=8 ) { Poisson Electron Hole eQuantumPotential hQuantumPotential}
            }
        # Save ( FilePrefix=\"$fname${pre}INIT\" )
        }
    "
# I(V)P
    sdevice_solve "
        Solve {
                # Start V sweep
                NewCurrentPrefix=\"IVP\"
                Quasistationary
                (
                  MaxStep=0.01
                  MinStep=0.001
                  Increment=1.3
                  Decrement=2
                  Goal { Name=\"pmetal\" Voltage=$VFEND}
                )
                {
                  Coupled ( Iterations=8 ) { Poisson Electron Hole eQuantumPotential hQuantumPotential}
                  Plot
                  (
                      FilePrefix=\"${fname}${pre}_P\" NoOverwrite
                      Time=(0.0;0.05;0.1;0.15;0.2;0.25;0.3;0.35;0.4;0.45;0.5;0.55;0.6;0.65;0.7;0.75;0.8;0.85;0.9;0.95;1.0)
                  )
                }
                #Save ( FilePrefix=\"$fname${pre}PVFEND\" )
```

## C.2   Simulation File

```
# generic input file I(V) simulation for PIN diode
# read input filename
set infile [open "file.cur" r]
set fname [gets $infile]
close $infile
# Front metal work function
set NWFF "N$WFn"
# Back metal work function
set NWFB "P$WFp"
# set local variables
set pre  "$NWFF${NWFB}T${TEMP}_SRM_"
set mshf "_msh.tdr"
# set dopf "_msh.tdr"
set datf "_des.dat"
set pltf "_des.plt"
set logf "_des.log"
# set terminal bias value, F(ront) and B(ack)
set VS 0.10
set VFINI 1.50
set VFEND -1.50
set VZ 0.0

# initial solution
sdevice_init "
    File {
        Grid    = \"$fname$mshf\"
        Plot    = \"$fname$pre$datf\"
        Current = \"$fname$pre$pltf\"
        Output  = \"$fname$pre$logf\"
    # parameter file for Lucent mobility model
        Parameter = \"lucent.par\"
    }
    Electrode {
        { Name=\"nmetal\"   Voltage=$VZ   Schottky Workfunction=$WFn}
        { Name=\"pmetal\"   Voltage=$VS   Schottky Workfunction=$WFp}
        { Name=\"back\"     Voltage=$VZ }
    }
    Physics {
        # set temperature as defined in sim.sh
        -eQuantumPotential
        -hQuantumPotential
        Temperature=$TEMP
        EffectiveIntrinsicDensity( Slotboom )
    # Lucent mobility model  eHighFieldSaturation hHighFieldSaturation
        Mobility( PhuMob Enormal)
        Recombination(
            SRH(
                TempDependence
            )
        )
    }
    # To include barrier lowering and valence band tunneling
    # Physics(electrode = \"nmetal\") {BarrierLowering Recombination(eBarrierTunneling)}
    # Includes barrier lowering : Image force
    #Physics(electrode = \"nmetal\") { BarrierLowering }
    #Physics(electrode = \"pmetal\") { BarrierLowering }
    # quantities to be shown in 2D cross-section (Tecplot)
    Plot {
        Doping
        DonorConcentration
        AcceptorConcentration
        EffectiveBandGap
        ConductionBandEnergy
        ValenceBand
        SpaceCharge
        ElectricField
        Potential
        eDensity
        hDensity
        eMobility
        hMobility
        eCurrent
        hCurrent
        eVelocity
        hVelocity
        SRHRecombination
        eQuantumPotential
        hQuantumPotential
    }
    # plot the following quantities at coordinates (X Y) in Inspect
    CurrentPlot {
```

```
        Potential ((0.0 0.0))
        eDensity ((0.0 0.0))
        hDensity ((0.0 0.0))
    }

    # some math options. no need to change these
    Math {
    Wallclock
        RelErrControl
        Number_of_Threads=maximum
        Extrapolate
        Iterations=200
        cnormprint
        #RhsMin=1E-1
        #Digits=10

    # stop simulation if draincurrent is smaller than 1E-15 A/um
        #BreakCriteria
        #{
        #    Current (Contact = \"nmetal\" minval = 1E-15)
        #}
    }
     # nonlocal tunneling depth in cm
    #Math(Electrode=\"pmetal\"){
    #Nonlocal(Length=10e-7)
    #}
"

# solve initial conditions
sdevice_solve "
    Solve {
        Poisson
        Coupled { Poisson }
        Coupled { Poisson hQuantumPotential}
        Coupled { Poisson eQuantumPotential hQuantumpotential}
        Coupled { Poisson Hole eQuantumPotential hQuantumpotential}
        Coupled { Poisson Electron Hole eQuantumPotential hQuantumpotential}
        #Save ( FilePrefix=\"$fname${pre}VSTART\" )
    }
"

# ramp to pmetal initial conditions
    sdevice_solve "
        Solve {
            Quasistationary
            (
                InitialStep=0.01
                MaxStep=0.2
                MinStep=0.001
                Increment=1.3
                Decrement=2
                Goal { Name=\"pmetal\" Voltage=$VFINI }
            )
            {
                Coupled ( Iterations=8 ) { Poisson Electron Hole eQuantumPotential hQuantumPotential}
            }
          # Save ( FilePrefix=\"$fname${pre}INIT\" )
        }
    "
# I(V)P
    sdevice_solve "
        Solve {
                # Start V sweep
                NewCurrentPrefix=\"IVP\"
                Quasistationary
                (
                  MaxStep=0.01
                  MinStep=0.001
                  Increment=1.3
                  Decrement=2
                  Goal { Name=\"pmetal\" Voltage=$VFEND}
                )
                {
                  Coupled ( Iterations=8 ) { Poisson Electron Hole eQuantumPotential hQuantumPotential}
                  Plot
                  (
                      FilePrefix=\"${fname}${pre}_P\" NoOverwrite
                      Time=(0.0;0.05;0.1;0.15;0.2;0.25;0.3;0.35;0.4;0.45;0.5;0.55;0.6;0.65;0.7;0.75;0.8;0.85;0.9;0.95;1.0)
                  )
                }
            #Save ( FilePrefix=\"$fname${pre}PVFEND\" )
```

```
        }
    "
# ramp to nmetal initial conditions
    sdevice_solve "
        Solve {
            NewCurrentPrefix=\"SWITCH2\"
            Quasistationary
            (
                InitialStep=0.01
                MaxStep=0.1
                MinStep=0.0001
                Increment=1.5
                Decrement=1.9
                Goal { Name=\"nmetal\" Voltage=$VFEND }
                Goal { Name=\"pmetal\" Voltage=$VZ }
            )
            {
                Coupled ( Iterations=8 ) { Poisson Electron Hole eQuantumPotential hQuantumPotential}
            }
            Save ( FilePrefix=\"$fname${pre}INIT\" )
        }
    "
# I(V)N
    sdevice_solve "
        Solve {
                # Start VN sweep
                NewCurrentPrefix=\"IVN\"
                Quasistationary
                (
                  MaxStep=0.01
                  MinStep=0.0001
                  Increment=1.1
                  Decrement=2
                  Goal { Name=\"nmetal\" Voltage=$VFINI}
                )
                {
                  Coupled ( Iterations=8 ) { Poisson Electron Hole eQuantumPotential hQuantumPotential}
                  #Plot
                #(
                        #FilePrefix=\"${fname}${pre}_N\" NoOverwrite
                        #Time=(0.0;0.1;0.2;0.3;0.4;0.5;0.6;0.7;0.8;0.9;1.0)
                #)
            }
            #Save ( FilePrefix=\"$fname${pre}NVFEND\" )
        }
    "
# save final plot files
sdevice_finish
```

# Appendix D

# Additional Simulations Results

## D.1   Charge under the gates



(a) Band Diagram

(b) Carrier Densities
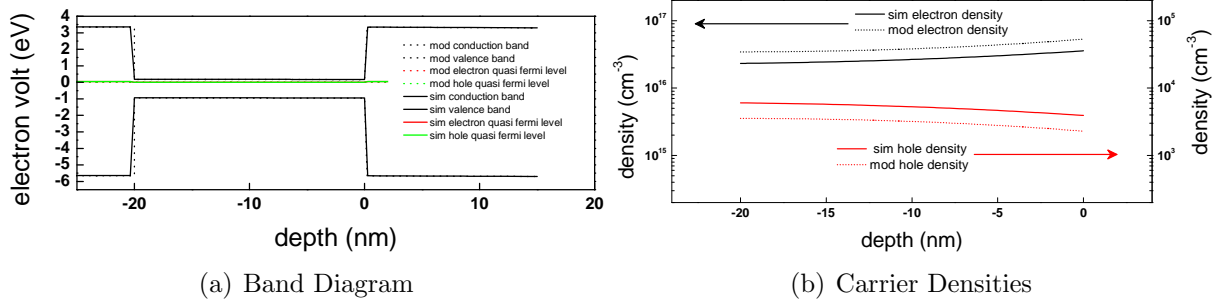
**Figure D.1:** Simulated and modeled (a) bands and (b) carrier densities along axis B in figure 2.6 (under the n-gate) in equilibrium conditions.



(a) Band Diagram

(b) Carrier Densities
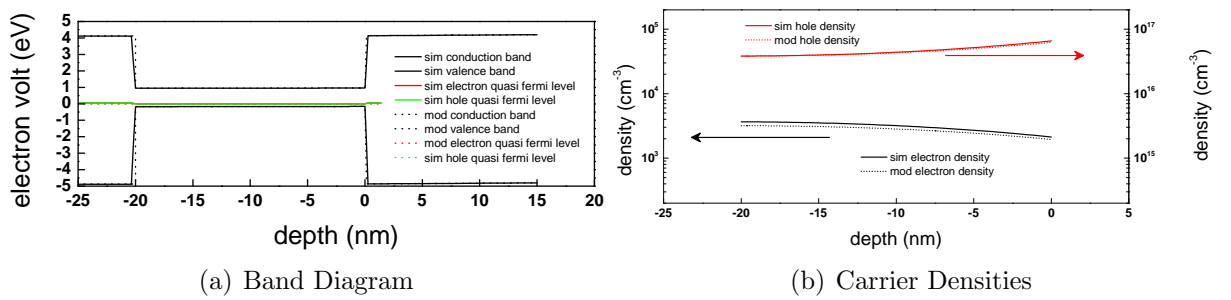
**Figure D.2:** Simulated and modeled (a) bands and (b) carrier densities along axis A in figure 2.6 (under the p-gate) in equilibrium conditions.

## D.2   Diffusion Current

(a) Band Diagram                (b) Carrier Densities

**Figure D.3:** Simulated and modeled (a) bands and (b) carrier densities along axis B in figure 2.6 (under the n-gate) in forward conditions.



(a) Band Diagram                (b) Carrier Densities
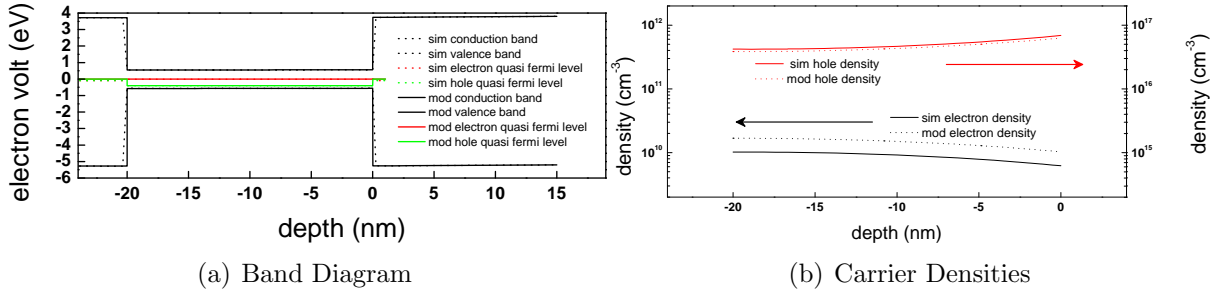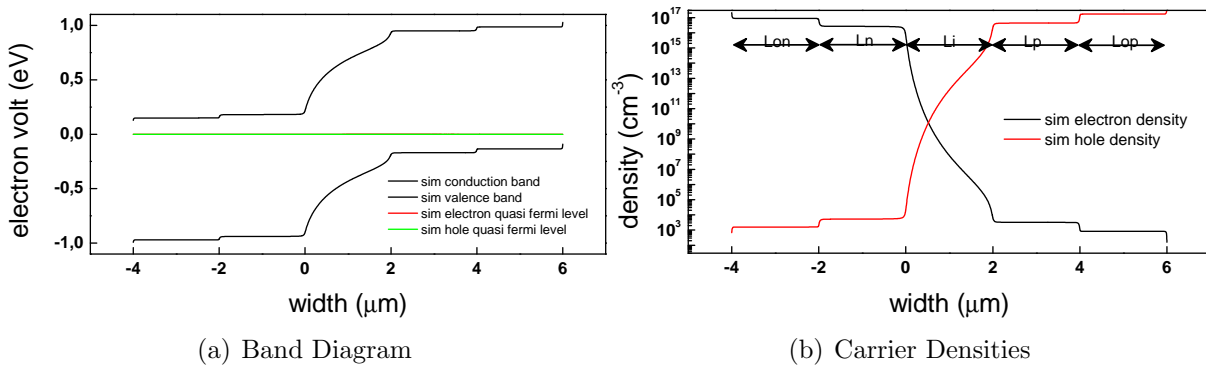
**Figure D.4:** a) A simulated band diagram along axis C in figure 2.6 in equilibrium. (b) The corresponding carrier concentrations.

# List of Symbols

| Symbol | Description | Unit |
|--------|-------------|------|
| $A$ | area of a device $= Z \cdot tsi$ | cm$^2$ |
| $A_-^*$ | Richardson constant | Acm$^{-2}K^{-2}$ |
| $A_n^*$ | Richardson constant for electron emission | Acm$^{-2}K^{-2}$ |
| $A_p^*$ | Richardson constant for hole emission | Acm$^{-2}K^{-2}$ |
| $D_n$ | electron diffusion constant | cm$^2$ s$^{-1}$ |
| $D_p$ | hole diffusion constant | cm$^2$ s$^{-1}$ |
| $\delta\phi$ | barrier lowering due to image force | eV |
| $E_C$ | conduction band energy (bottom) | eV |
| $E_F$ | extrinsic Fermi level | eV |
| $E_{FI}$ | intrinsic Fermi level | eV |
| $E_{Fn}$ | electron quasi-Fermi level | eV |
| $E_{Fp}$ | hole quasi-Fermi level | eV |
| $E_G$ | band gap of silicon | eV |
| $E_{trap}$ | difference between defect and intrinsic level | J |
| $E_V$ | valence band energy (top) | eV |
| $E_{VAC}$ | vacuum level | eV |
| $\mathcal{E}$ | electric field | Vcm$^{-1}$ |
| $\epsilon_{Si}$ | permittivity of silicon $\epsilon_{Si} = \epsilon_0 \cdot k_{Si}$ | F cm$^{-1}$ |
| $\epsilon_{SiO2}$ | permittivity of silicon-oxide $\epsilon_{SiO2} = \epsilon_0 \cdot k_{SiO2}$ | F cm$^{-1}$ |
| $\phi_B$ | Schottky barrier height multiplied by $q$ | eV |
| $\phi_{bn}$ | n-metal Schottky hole barrier height multiplied by $q$ | eV |
| $\phi_{bp}$ | p-metal Schottky electron barrier height multiplied by $q$ | eV |
| $\phi_F$ | Fermi potential at the contact | eV |
| $\phi_{mn}$ | n-metal work function multiplied by $q$ | eV |
| $\phi_{mp}$ | p-metal work function multiplied by $q$ | eV |
| $\chi_{Si}$ | silicon electron affinity | eV |
| $h$ | Planck's constant | J/s |

continued

| Symbol | Description | Unit |
|--------|-------------|------|
| $J^d$ | diffusion current density | $\text{Acm}^{-2}$ |
| $J_{n,i}^{dr}$ | electron drift current density in the i-region | $\text{Acm}^{-2}$ |
| $J_{p,i}^{dr}$ | hole drift current density in the i-region | $\text{Acm}^{-2}$ |
| $J^{th}$ | thermionic emission current density | $\text{Acm}^{-2}$ |
| $J_{nF}$ | forward electron current density | $\text{Acm}^{-2}$ |
| $J_{nR}$ | reverse electron current density | $\text{Acm}^{-2}$ |
| $J_n$ | electron current density $= J_{nF} - J_{nR}$ | $\text{Acm}^{-2}$ |
| $J_{n,max}$ | maximum electron current density | $\text{Acm}^{-2}$ |
| $J_{nt}$ | total electron current density | $\text{Acm}^{-2}$ |
| $J_{pF}$ | forward hole current density | $\text{Acm}^{-2}$ |
| $J_{pR}$ | reverse hole current density | $\text{Acm}^{-2}$ |
| $J_p$ | hole current density $= J_{nF} - J_{nR}$ | $\text{Acm}^{-2}$ |
| $J_{p,max}$ | maximum hole current density | $\text{Acm}^{-2}$ |
| $J_{pt}$ | total hole current density | $\text{Acm}^{-2}$ |
| $J_{srh}$ | Shockley-Read-Hall recombination/generation current | $\text{Acm}^{-2}$ |
| $J_t$ | total current density | $\text{Acm}^{-2}$ |
| $\overrightarrow{J_n}$ | electron current density vector | $\text{Acm}^{-2}$ |
| $\overrightarrow{J_p}$ | hole current density vector | $\text{Acm}^{-2}$ |
| $k$ | Boltzmann's constant | $\text{eVK}^{-1}$ |
| $k_{Si}$ | relative permittivity of silicon | - |
| $k_{SiO2}$ | relative permittivity of silica | - |
| $Li$ | length of the intrinsic region | $\mu\text{m}$ |
| $Ln$ | length of the n-metal gate | $\mu\text{m}$ |
| $Lp$ | length of the p-metal gate | $\mu\text{m}$ |
| $m^*$ | carrier effective mass | |
| $m_0$ | electron rest mass | $kg$ |
| $n$ | electron density | $\text{cm}^{-3}$ |
| $n_i$ | intrinsic carrier density $n_i = \sqrt{N_C N_V} e^{\frac{-E_G}{2kT}}$ | $\text{cm}^{-3}$ |
| $n_n$ | electron density under the n-metal gate | $\text{cm}^{-3}$ |
| $n_p$ | electron density under the p-metal gate | $\text{cm}^{-3}$ |
| $n_{i,eff}$ | effective intrinsic carrier concentration | $\text{cm}^{-3}$ |
| $\widehat{n}$ | normal unity vector | $-$ |
| $n_0^B$ | electron equilibrium density | $\text{cm}^{-3}$ |
| $p$ | hole density | $\text{cm}^{-3}$ |
| $p_n$ | hole density under the n-metal gate | $\text{cm}^{-3}$ |
| $p_p$ | hole density under the p-metal gate | $\text{cm}^{-3}$ |
| $p_0^B$ | hole equilibrium density | $\text{cm}^{-3}$ |
| $q$ | elementary charge | C |
| $R_s$ | series resistance | $\Omega$ |
| $R_{net}^{SRH}$ | recombination rate | $\text{s}^-1\text{cm}^3$ |
| $\rho_s$ | series resistivity $= R_s A$ | $\Omega\text{cm}^2$ |

continued

| Symbol | Description | Unit |
|--------|-------------|------|
| $T$ | temperature | K |
| $tbox$ | buried oxide layer thickness | nm |
| $tbsi$ | substrate thickness | nm |
| $tox$ | front oxide thickness | nm |
| $toxn$ | front oxide under the n-metal gate thickness | nm |
| $toxp$ | front oxide under the p-metal gate thickness | nm |
| $tsi$ | silicon on insulator thickness | nm |
| $\tau_n$ | electron lifetime | s |
| $\tau_p$ | hole lifetime | s |
| $u_t$ | thermal voltage kT/q | V |
| $V_{FB}$ | flatband voltage $= \phi_{mp} - \phi_{mn}$ | V |
| $Vox$ | voltage across an oxide | V |
| $v_n$ | electron thermionic emission velocity | cm/s |
| $v_p$ | hole thermionic emission velocity | cm/s |
| $Z$ | width of a device | $\mu$m |

| quantity | symbol | value |
|---|---|---|
| Boltzmann's constant | $k$ | $8.61738 \cdot 10^{-5}$ eV/K |
| elementary charge | $q$ | $1.60218 \cdot 10^{-19}$ C |
| electron rest mass | $m_0$ | $0.91095 \cdot 10^{-}30$ kg |
| electron volt | eV | 1 eV$= 1.60218 \cdot 10^{-19}$ J |
| permittivity | $\epsilon_0$ | $8.85418 \cdot 10^{-14}$ F/cm |
| Planck's constant | h | $6.626068 \cdot 10^{-34}$ J/s |
| relative permittivity of silicon | $k_{Si}$ | 11.9 |
| relative permittivity of silica | $k_{SiO2}$ | 3.9 |

# List of Abbreviations

| | |
|---|---|
| aMSM-diode | asymmetrical Metal Semiconductor Metal diode |
| BOX | Buried OXide |
| CMOS | Complementary Metal Oxide Semiconductor |
| CP | Charge Plasma |
| DC | Direct Current, low frequency |
| IV | Current as a function of Voltage |
| meas | measured |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| mod | modelled |
| n-gate | metal gate with a n-metal work function |
| n-metal | metal with work function $< \chi_{Si} + E_G/2$ |
| PIN-diode | P-type Intrinsic N-type silicon diode |
| PN | P region adjacent to an N region |
| p-gate | metal gate with a p-metal work function |
| p-metal | metal with work function $> \chi_{Si} + E_G/2$ |
| RBS | Rutherford Backscattering spectroscopy |
| sim | simulated |
| SiO2 | silicon dioxide |
| SOI | Silicon On Insulator |
| SRH | Shockley Read Hall |
| TEM | Transmission Electron Microscopy |
| XRF | X-ray fluorescence |

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