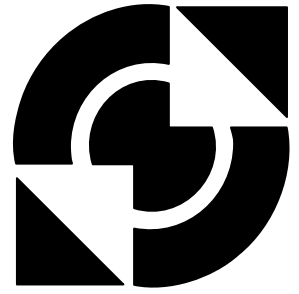


# University of Twente

Faculty of Electrical Engineering,  
Mathematics & Computer Science



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## **The design of a new power combining technique for the RF power amplifiers**

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**MSc. Thesis**  
**May 2006**

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Mathematics & Computer Science

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# The design of a new power combining technique for the RF power amplifiers

by  
Wei Cheng

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# Abstract

The wireless communication market has grown tremendously in the last decade. As a crucial block in the wireless system, the power amplifier is generally realized in dedicated and hence expensive technologies. To decrease the overall cost and size of the communication devices the power amplifier is aimed to be implemented in the mainstream digital technology: CMOS. The low breakdown voltage of the transistor in the CMOS process makes it challenging to design the power amplifier with high output power. A new power combining technique based on the parallel quarter-wavelength transmission lines has been proposed and explored to overcome this problem. By combining the output power from multiple power amplifiers the total available output power can be increased. It also has the potential for the power control application and overall reliability improvement. The simulation results of several design examples present the verification for the theoretical analysis of the proposed power combining technique.

After thorough analysis of the nonidealities of the proposed power combining technique, the practical issues regarding the microstrip implementation of the combining network are discussed. The measures to minimize the layout discontinuities of the microstrip combining network have been presented in a design example.



To my dear parents  
who give me every chance to pursue the dreams.

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# Chapter 1

## Introduction

### 1.1 Motivation

The increasing market for wireless communication systems has compelled more and more research to focus on radio-frequency integrated circuits (RFIC) design. Power amplifiers (PA) are one of the most crucial components in virtually every RF circuits. Among several different fabrication processes GaAs process technology have been used successfully to build PA block such as GaAs Metal Semiconductor Field Effect Transistors (MESFET's) and GaAs Heterojunction Bipolar Transistors (HBT's). Nevertheless, the considerable economic benefit potential of low-cost CMOS process is playing a more and more important role in RFIC area. Besides the lower cost of the process it is advantageous to put the RF front-end on the same chip as the rest of the mobile terminal. Even the less ambitious objective of implementing the mobile terminal in a set of separate chips in the same CMOS process may achieve highly economic benefits [1.1].

However, two major limitations are associated with the design of power amplifiers using sub-micron CMOS processes, namely,

1. Low transistor breakdown voltage.
2. High energy loss of on-chip impedance transformation [1.2].

Low device breakdown voltage severely constrains the design of RF power amplifiers, as the voltage on the drain of the output device in a power amplifier can swing to more than twice the supply voltage in class A and class F and even to three and half times in class E PA as shown in Fig. 1.1. A simple calculation in the following shows the constraint on the class E PA by the low breakdown voltage. The ideal output power of a class E PA is given by [1.4]

$$P_{out} = \frac{1.365 \times V_{cc}^2}{R} \quad (1.1)$$

$$V_{cc} = \frac{V_{max}}{3.65} \quad (1.2)$$

, where  $V_{cc}$  is the supply voltage,  $V_{max}$  is the drain voltage peak and  $R$  is the optimal load the transistor wants to see.

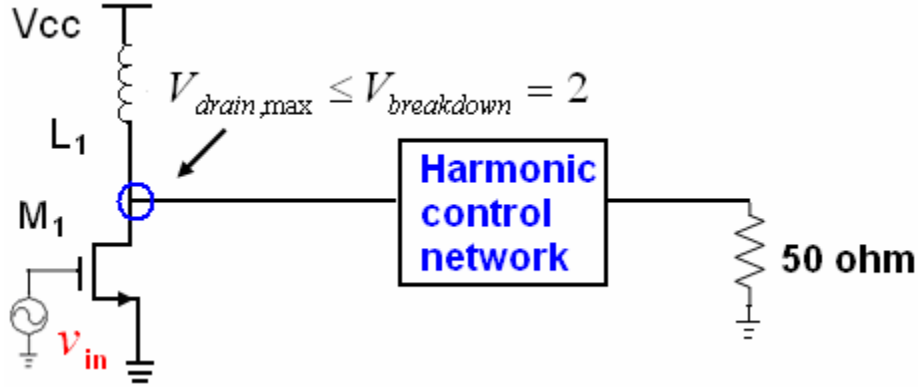


Fig. 1.1 Schematic of class E PA

$V_{max}$  is assumed to be equal to the breakdown voltage, say, 2 volt for the 0.18  $\mu\text{m}$  CMOS process. Therefore, to deliver a 100 mW power the load need to convert from 50 ohm to 4 ohm.

As can be seen, the low breakdown voltage not only limits the maximum power out of the PA but also requires larger impedance transformation, which causes higher loss in the on-chip transformation network [1.3]. Since the optimal resistance the transistor needs is small the PA is more sensitive to the on-chip parasitic impedance. Additionally the lower breakdown voltage results in reliability concerns, such as long-term performance and the response to voltage surges in case of an antenna impedance mismatch [1.3].

One way to tackle the problem of low power output in the CMOS PA is to combine the small amount of output power from several PAs through a lossless or low loss power combining structure. In the combining structure each PA shares the job with others, which decreases the burden for each of them which improve the long-term reliability. For example, the heat is not concentrated in one active device.

In this work a new power combining technique is proposed and the theory analysis is presented based on the parallel quarter-wavelength transmission line network. Theoretically the *N-device unbalanced power combining technique* is suitable for different PA classes and impedance conversion circuits. It achieves impedance

transformation and power combining simultaneously and brings the benefits for the implementation of the  $\frac{\lambda}{4}$  transmission line impedance-transformation technique.

## **1.2 Organization**

In chapter 2 two basic blocks of the power combining technique are discussed, namely, the power amplifier block and the combining network block.

In chapter 3 firstly the voltage summation structure is completely analyzed and compared with the power summation structure. As a result, the theoretical analysis of the proposed power combining technique is presented and three design examples are used for verification.

In chapter 4 the nonidealities of the proposed power combining technique are discussed, namely, phase nonidealities, amplitude nonidealities and non-resistive antenna nonidealities.

In chapter 5 the implementation of the combining network on PCB is discussed. The major issues such as the choice of the PCB substrate and layout topology, measurement of the microstrip network are discussed. At the end is given a design example of the combining network on RO4003 substrate.

In chapter 7 the conclusions of this work are given and possible future work is suggested.



## Chapter 2

### Introduction on Power Combining

#### 2.1 Introduction

The power combining structure generally consists of two parts, namely the PA block and the combining block shown in Fig. 2.1. Through the combining network the output power produced by the PA blocks is delivered to the antenna which usually is modeled as a 50 ohm resistive load. The PA block is similar to a normal single PA except the additional influence caused by the combining structure. In the following section these two blocks will be discussed respectively.

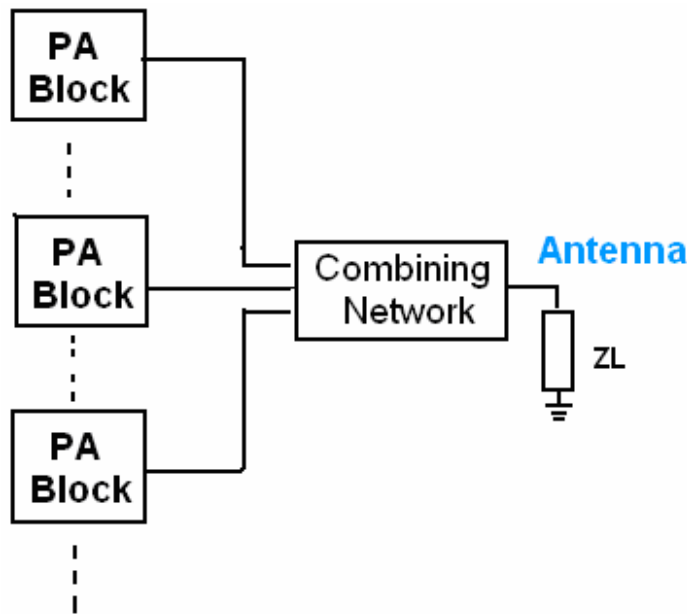


Fig. 2.1 Block diagram of the power combining circuits.

#### 2.2 Power Amplifier Block

##### 2.2.1 Introduction

The normal PA contains four major sub-blocks: input matching, active device, harmonic control and impedance conversion shown in Fig. 2.2. The input network includes every passive component used to match the transistor gate to the external input impedance. The active device comprises the transistor without its output capacitance. The harmonic

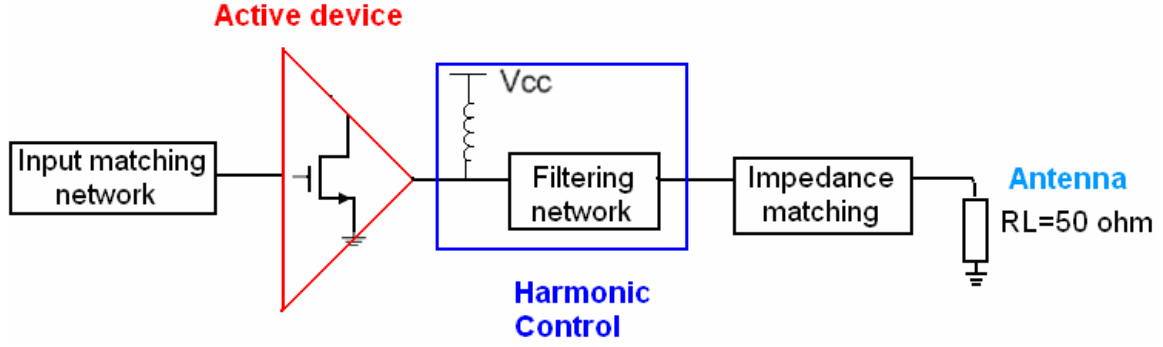


Fig. 2.2 Block diagram of the single power amplifier.

control block consists of a DC-feed inductor and a filtering network, which includes the transistor output capacitance  $C_{ds}$ . In some applications such as linear PA classes the DC-feed inductor is set to a very big value so that only DC current can pass through and the filtering network is only used to filter out the fundamental output signal. In switching PAs such as a class E PA the DC-feed inductor and the filtering network are synthesized to do the waveform shaping job. The impedance matching block is used to transfer the 50 ohm from the antenna to the optimum resistance value that the PA wants to see.

Among those four blocks the active device plays a fundamental role in the performance of the power amplifiers. Unlike in most other integrated circuits such as LNA and small-signal amplifiers, the transistors in a power amplifier do not stick on one DC point but operate in one or more of three states; namely, off (below threshold), resistive (triode region), or current source (saturation region). Depending on which of these regions are used by the transistor, the PAs fall into two categories: linear PA and nonlinear (switching) PA. In a linear PA the transistor is supposed to operate either within the saturation region or below threshold,  $v_{GS} < V_{TH}$ ; in a switching PA it is supposed to operate either within the ohmic region or below threshold.

Table 2.1 shows a summary of different classes of ideal power amplifiers to be discussed in the following sections, where the drain efficiency is defined as

$$\eta_{drain} = \frac{\text{output power}}{\text{DC power input}} \quad (2.1)$$



Table 2.1 A summary of the power characteristics of different PA modes.

Class	Modes	Conduction Angle	Output Power	Maximum Drain Efficiency	Linearity
A	linear	100%	moderate	50%	good
AB		<100% >50%	moderate	<100% >50%	moderate
B		50%	moderate	78.5%	poor
C		<50%	small	>78.5%	poor
D	switching	50%	large	100%	poor
E		50%	large	100%	poor
F		50%	large	100%	poor

Fig. 2.3 shows the ideal waveform of the drain voltage  $v_{DS}$  and drain current  $i_{DS}$  of different power amplifiers, where the Y axis for the  $v_{DS}$  is normalized to the supply voltage [2.1]. Since the power efficiency is the primary concern in this work linear PAs will not be chosen as the PA block for the combining structure. Among the switching PAs the latter discussion will indicate that class E and class F PA are suitable for this work and finally class E will be chosen.

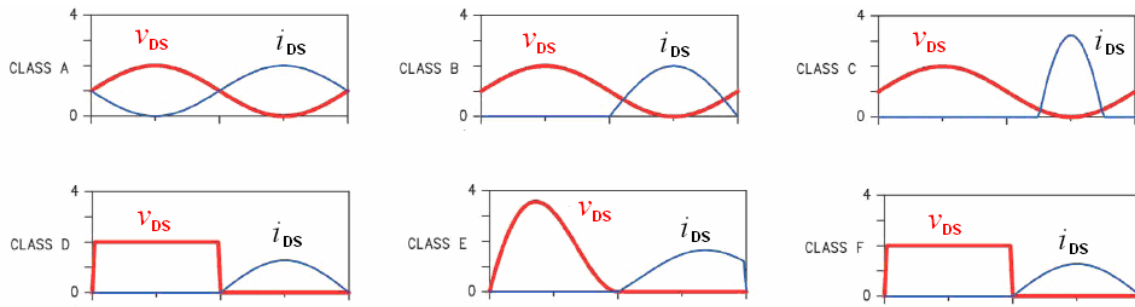


Fig. 2.3 Ideal waveforms of drain voltage and current of different classes of PAs.

## 2.2.2 Linear Power Amplifier

[2.2] and [2.5] give a classic analysis of the ideal linear PAs, which is based on three major assumptions. The ideal characteristics of the linear PAs give pretty good introductions and are reviewed briefly at first. Followed are the assumptions that the ideal

analysis is based on. In reality the assumptions may not be fully satisfied; the impact of this is discussed at the end of this sub-section.

### Ideal characteristics of linear PA

Fig. 2.4 shows the general schematic model for linear PAs, namely, class A, AB, B and C. The inductor  $L_1$  is set to a very large value assuming that only DC biasing current can go through from the supply voltage  $V_{cc}$  to the transistor  $M_1$ .  $C_1$  is a big capacitance to keep the dc voltage from the output. The resonant tank  $L_1$  and  $C_2$  together with the drain-source capacitance  $C_{ds}$  is resonant at the fundamental frequency so that the output current to the antenna is sinusoid.

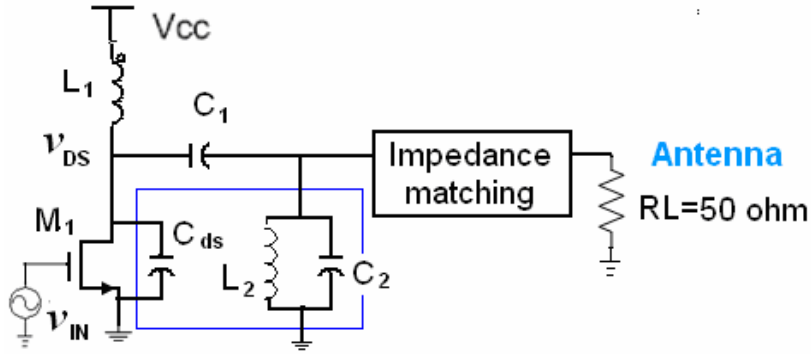


Fig. 2.4 General schematic for the linear PA.

All the common characteristics shared by the linear PA shown in Fig. 2.4 are listed as follows:

1. They are all biased in the saturation region and operate in the saturation and switch-off region.
2. They all use the similar harmonic control block consisting of  $L_1$ ,  $C_{ds}$ ,  $C_1$ ,  $L_2$ , and  $C_2$  to filter the output current.

The only difference between them is the dc bias of the input signal at the active device gate shown in Fig. 2.5. The gate bias of the class A PA is set so that during the whole swing of input signal  $v_{IN}$  the transistor stays in the saturation region and the current through the transistor  $i_{DS}$  is a complete sinusoid waveform. In the class B PA only during half swing of the  $v_{IN}$  the transistor operates in the saturation region and in the switch-off region at the other half period. Thus the conduction angle  $\theta = 180^\circ$  and  $i_{DS}$  only has half part of the sinusoid waveform. In class C the dc bias of  $v_{IN}$  is lower than that in class B

and the conduction angle is less than  $180^\circ$ . Class AB has the gate dc bias between class A and class B and its conduction angle is between  $180^\circ$  and  $360^\circ$ . Another thing that can be observed from Fig. 2.5 is that the overlap between  $i_{DS}$  and  $v_{DS}$  is decreasing as the conduction angle decreases, which mean that the class C PA has the highest drain

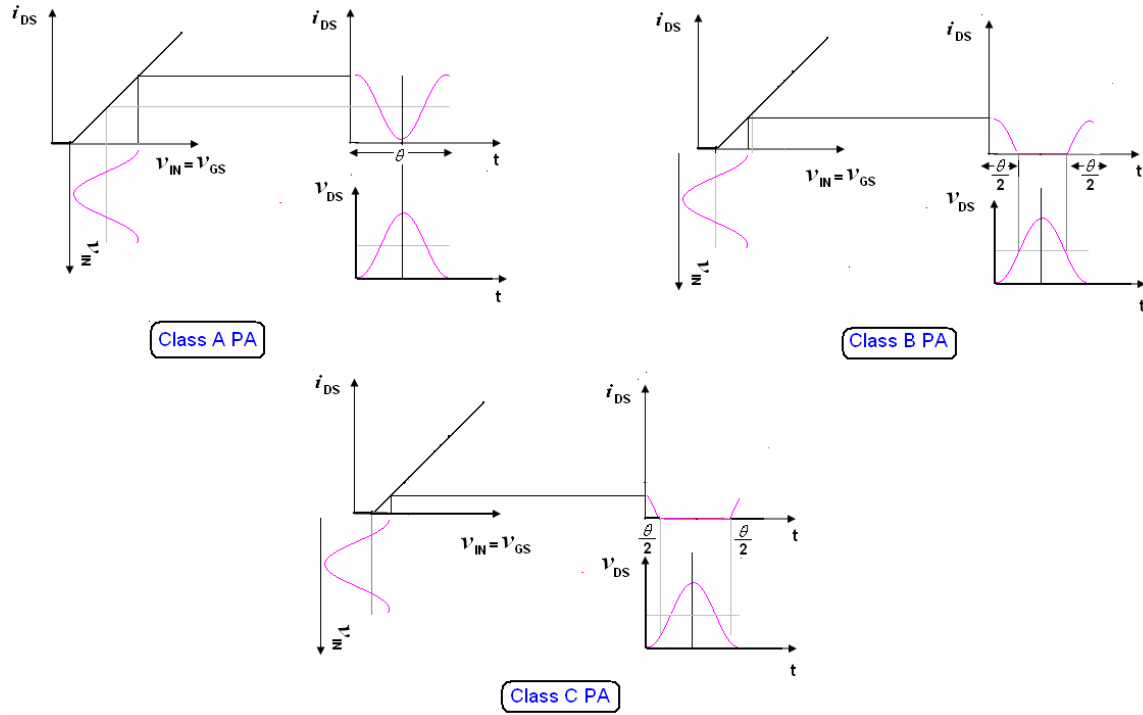


Fig. 2.5 Time-domain waveform of the transistor.

efficiency and that the class A PA has the lowest drain efficiency.

### Ideal assumptions of linear PAs

In fact the ideal characteristics of the linear PA above stated are based on three assumptions:

1. The transistor in the saturation region has a constant large-signal conductance

$G_m = \frac{i_{ds}}{v_{gs}}$ , which is shown as a straight line in the  $i_{DS} - v_{GS}$  plot shown in Fig. 2.5.

2. The knee voltage is zero so that the drain voltage  $v_{DS}$  can swing in full scale from  $2V_{cc}$  to zero and  $v_{DS}$  is always larger than  $v_{GS} - V_{TH}$  so that the transistor never enters into the triode region.

3. The phase shift between  $v_{IN}$  and  $i_{GS}$  is zero and the phase shift between  $v_{IN}$  and  $v_{DS}$  is  $\pi$ .

Following three practical cases will be discussed when these three assumptions are not satisfied

### Practical examples when ideal-linear-PA assumptions are not satisfied

#### a. non-constant $G_m$

Take a MOSFET as an example, using the simple square law equation<sup>1</sup> gives the  $G_m$  as

$$G_m = \frac{i_{ds}}{v_{gs}} = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_{TH}) = \mu_n C_{ox} \frac{W}{L} (V_{GS} + v_{gs} - V_{TH}) \quad (2.2)$$

For small-signal amplifiers the ac input  $v_{gs}$  is much smaller than  $V_{GS} - V_{TH}$  and can be neglected so that the small-signal  $G_m$  is constant for each fixed DC point. However, in the linear PAs the ac input  $v_{gs}$  is ten or a hundred times larger and the  $G_m$  is not fixed anymore. Therefore, the straight line plot between  $i_{DS}$  and  $v_{IN}$  shown in Fig. 2.5 is just a first-order approximation for linear PAs.

#### b. Mixed-mode PA

As can be seen in Fig. 2.5 when the  $v_{IN}$  approaches its peak value the  $i_{DS}$  is maximum and  $v_{DS}$  reaches its lowest value. In this region  $v_{DS}$  could be smaller than  $v_{GS} - V_{TH}$  and then the transistor enters into the triode region. This happens more often in class C mode since the input signal  $v_{IN}$  needs to be larger to produce the same amount of power as in class A, AB and B modes [2.2]. In other words it shows that  $v_{DS}$  can not swing to zero voltage and thus the maximum swing of the output voltage is  $2V_{cc} - (v_{GS} - V_{TH})$ .

To maintain the assumption for the ideal analysis of linear PA, the input signal  $v_{IN}$  has to be lower so that  $v_{DS}$  is always larger than  $v_{GS} - V_{TH}$ . However, the power output is reduced and the drain efficiency is lower. Another option is to increase the input signal  $v_{IN}$  and make the transistor operate in a mixed mode, where the saturation and triode mode are all involved. [2.24] uses the Matlab to predict the mixed mode class C PA, however, no closed-form design equations is obtained.

Fig. 2.6 could illustrate the single-mode and mixed-mode cases clearer. For a linear PA

---

<sup>1</sup> Ideally the transistor in the linear PA stays either in the saturation region or switch-off region, therefore, the square law equation is used.

mode are all involved. [2.24] uses the Matlab to predict the mixed mode class C PA, however, no closed-form design equations is obtained.

Fig. 2.6 could illustrate the single-mode and mixed-mode cases clearer. For a linear PA

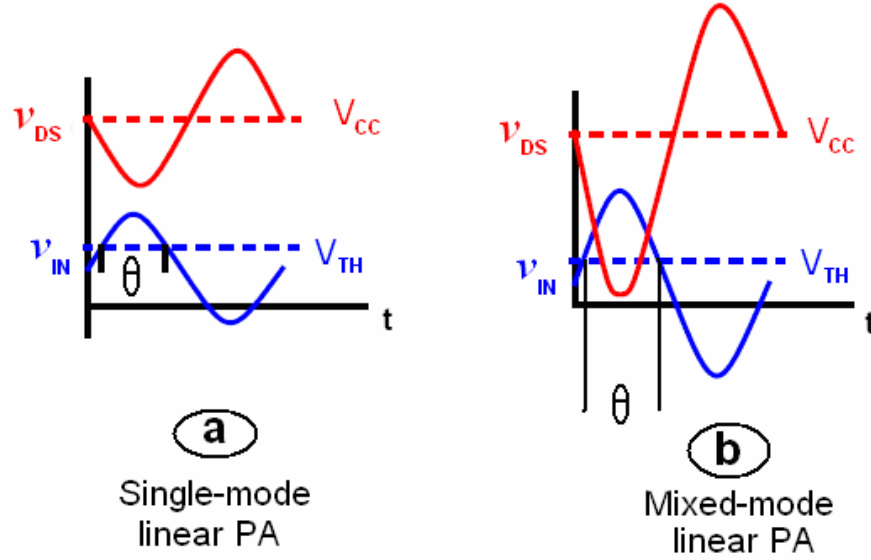


Fig. 2.6 Comparison between the single-mode linear PA and mixed-mode linear PA. with conduction angle  $\theta$ , Fig. 2.6a shows that the PA stays solely in saturation region and in the case shown in Fig. 2.6b the PA stays between the saturation and triode regions.

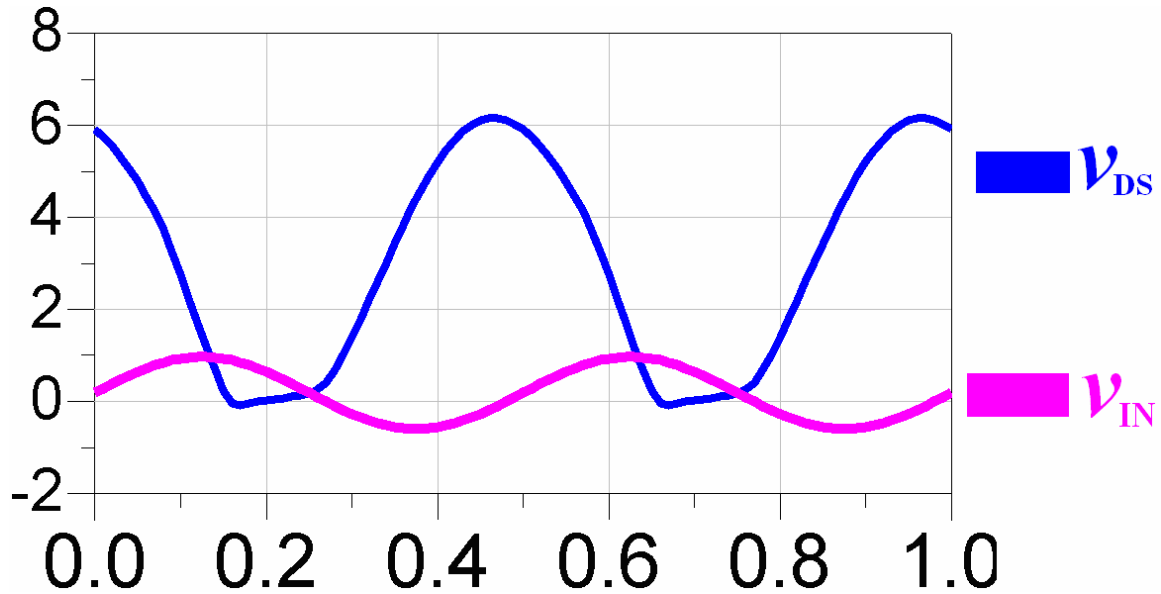


Fig. 2.7 Simulation result of the mixed mode class C PA shows the phase difference between  $v_{IN}$  and  $v_{DS}$  is not  $\pi$ .

**c. Phase difference shifts between  $v_{IN}$ ,  $i_{GS}$  and  $v_{DS}$ .**

Due to the drain-gate capacitance the phase difference between  $v_{IN}$  and  $i_{GS}$  at high frequency around GHz may not be  $\frac{\pi}{2}$  and the phase difference between  $v_{IN}$  and  $v_{DS}$  may not be  $\pi$ , which makes the analysis of mixed-mode linear PA even more difficult. Fig. 2.7 shows the simulation result of a mixed mode class C PA<sup>2</sup>. It's obvious that phase difference between  $v_{IN}$  and  $v_{DS}$  is not  $\pi$ .

## Summary

Normally when designing the linear PA the classic simple analysis in [2.2] and [2.5] only provides a rough initial starting point. Load-pull and source-pull simulation are often used to achieve optimum goals and avoid complex analysis involving the mixed-mode and phase shift situations.

## 2.2.3 Nonlinear Power Amplifier

### 2.2.3.1 Introduction

In contrast to the linear PAs, the active device of a nonlinear power amplifier (switching PA) is driven with a large signal input signal, turning the device on and off as a switch [2.2]. Class D, E and F are in this category. Compared to the linear PAs, the switching PAs provide higher drain efficiency. However, the output signal is not a function of the input signal any more, generally restricting these amplifiers to applications that require power amplification of constant amplitude signals [2.3]. In the following sections the class D, E, F PA will be introduced and a choice for this project will be made.

### 2.2.3.2 Class D Power Amplifier

Voltage-mode class-D, generally known as class-D or VMCD, implements a push-pull switching approach to amplification. Each switch is driven 180° out of phase. As shown in Fig. 2.8 when the switch  $M_1$  is on, the switch  $M_2$  is off, and vice versa.

---

<sup>2</sup> The simulation result is from the class C PA which is designed in section 3.4.4 and the details can be found there.

Therefore, the voltage  $v_{DS}$  is forced to be a square wave and there is no voltage-current overlap on  $M_1$  and  $M_2$ , resulting in a 100% drain efficiency. The filter ( $L_1$  and  $C_1$ ) gets rid of the harmonics in the output current to the load. The driving signal should be a square wave with a very sharp edge in order that switches  $M_1$  and  $M_2$  don't be switched on at the same time. At radio frequencies such driving signal is difficult to obtain. Besides, the device parasitic capacitance of  $M_1$  and  $M_2$  at point A could result in a large current-voltage overlap region during the device transition from the on to the off state and vice versa. For the VMCD the output capacitance is the dominant loss mechanism, which

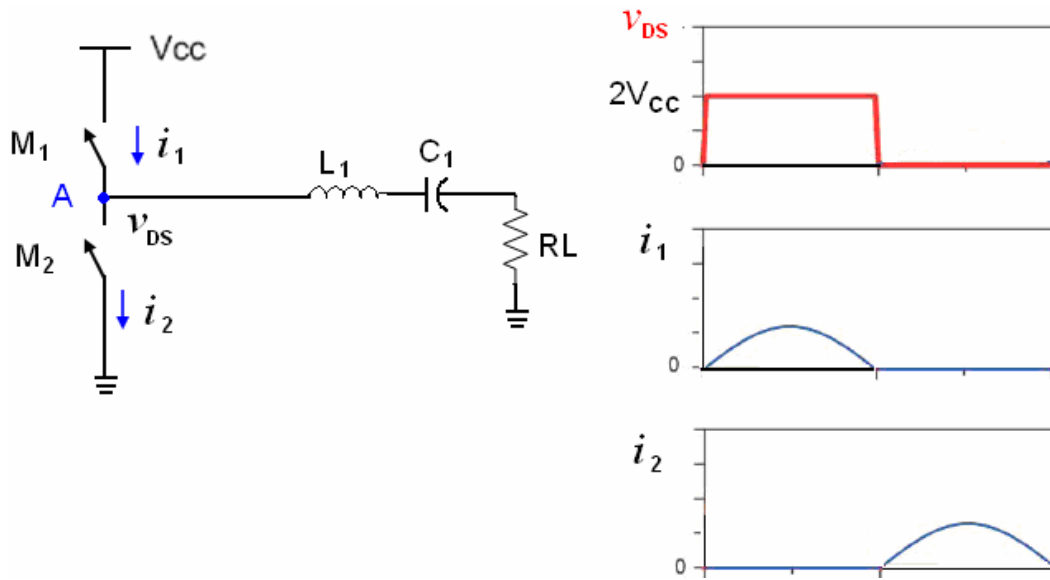


Fig. 2.8 Schematic of ideal class D power amplifier and its waveform.

limits this class to lower frequencies, in the MHz range [2.1]. However, two papers demonstrate that 75% drain efficiency at 0.9 GHz [2.29] and 60% at 1 GHz [2.30] can be obtained by the current-mode class-D (CMCD) power amplifier. CMCD is related to the VMCD by an interchange between the voltage and current waveforms. The series filter at the output of the device is exchanged for a parallel tank circuit, so the output capacitance is no longer the dominant loss mechanism as it can be absorbed into the design of the filter. Due to the filter resonance, the harmonics are bypassed and only the fundamental frequency reaches the load. There is no voltage across the transistor at each switch time so the switching loss is reduced [2.29]. Though CMCD could be potentially applied beyond GHz it's not chosen in this work.

### 2.2.3.3 Class F Power Amplifier

#### Ideal harmonic analysis

A class F PA uses an output filter to control the harmonic content of its drain voltage and drain current waveforms, thereby shaping them to reduce the power dissipation by the transistor [2.5]. For an ideal class F PA shown in Fig 2.9a, the switch  $M_1$  sees the optimum load  $R$  at fundamental frequency, zero impedance at even harmonics and

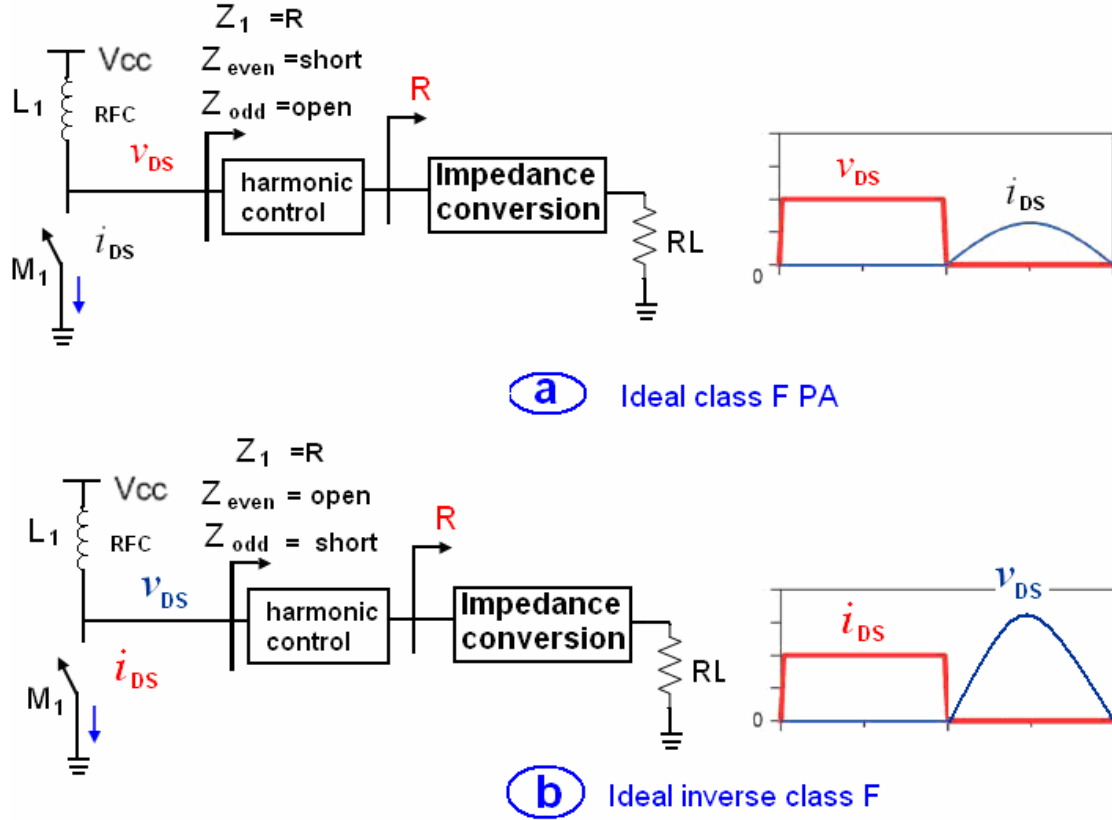


Fig. 2.9 Schematic of ideal class F and inverse class F power amplifier and its waveform.

infinite impedance at odd harmonics. Therefore, the voltage waveform on the switch is a square wave while the current is a half-rectified sinusoid and there is no overlap as shown in Fig. 2.9a. This suggests that the maximum achievable drain efficiency of the PA is 100%. Given this characteristic of harmonic termination the analysis of the class F PA in most of the papers is in frequency domain [2.6-2.7], [2.25-2.28]. Among those class-F-PA-related papers mostly the analysis uses the ideal switch model, which means the switch-on resistance is not accounted for the switched transistor. Though a more complete model of the sub-micron CMOS transistor is included in the analysis of the



class F PA [2.39] the closed-form equations couldn't be achieved and only the numerical results are obtained using Matlab.

Like the class D PA, the dual of class F, the inverse class F PA, interchanges the voltage and current waveforms shown in Fig. 2.9b. The voltage waveform of  $v_{DS}$  is a half sinusoidal and  $i_{DS}$  is a square wave, which is enabled by the opposite harmonic terminations. Since  $v_{DS}$  is half sinusoid the inverse class F PA imposes higher voltage stress on the transistor and is less used when the breakdown voltage is of more concern than the maximum drain current [2.33]. However, the following discussions on the class F PA applies to the inverse class F PA.

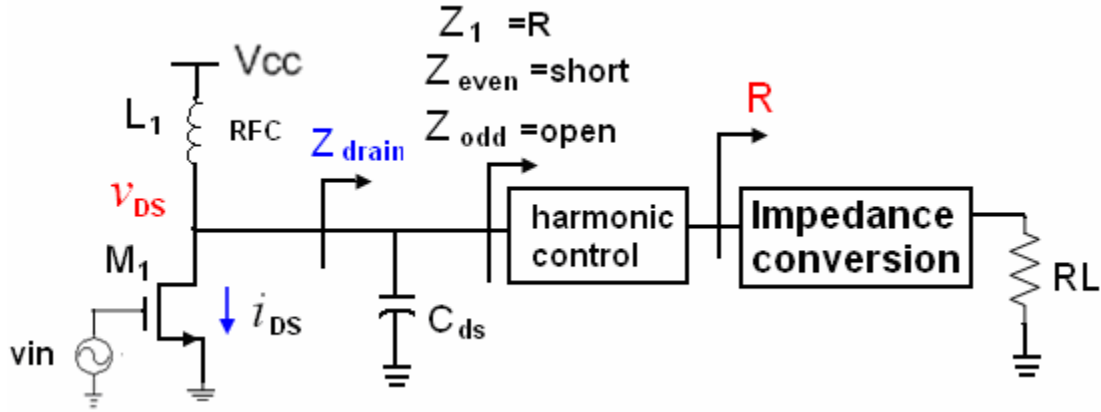


Fig. 2.10 Schematic Class F PA using the transistor as a switch.

### Practical limitations

Generally the implementation of above-stated ideal class F PA faces three practical limitations:

1. The drain-source capacitance  $C_{ds}$  provides short-circuit termination at high harmonics. In reality the switch  $M_1$  is usually implemented by a FET transistor (e.g. a NMOS transistor as shown in Fig. 2.10). Like for all switching PA modes the width of the transistor  $M_1$  is very large to achieve a small switch-on resistance. As a byproduct the drain-source capacitance  $C_{ds}$  is large as well. Therefore, the ideal case of infinite impedance at odd harmonics is undermined in practice by the output capacitance  $C_{ds}$  of the transistor  $M_1$ .
2. Zero/open at even/odd harmonics is not feasible. In practice the purely zero/open at even/odd harmonics is not realizable. Instead, the idea of low/high impedance

at even/odd harmonics is used, where low harmonic termination value means that it is less than  $\frac{1}{3R}$  and a high value means that the impedance is greater than  $3R$  [2.1];  $R$  is the optimum load for the class F PA shown in Fig. 2.9.

3. Infinite harmonic termination and finite harmonic termination. Sometime it's hard to implement the harmonic termination for infinite harmonics due to the complex filter network. Instead, the class F PA with finite harmonic termination is another option, where until finite number of even/odd harmonics the short/open impedance condition is satisfied [2.6-2.7]. Based on the number of the harmonic termination the class F PA can be categorized into two groups, namely, infinite harmonic class F and finite harmonic class F.

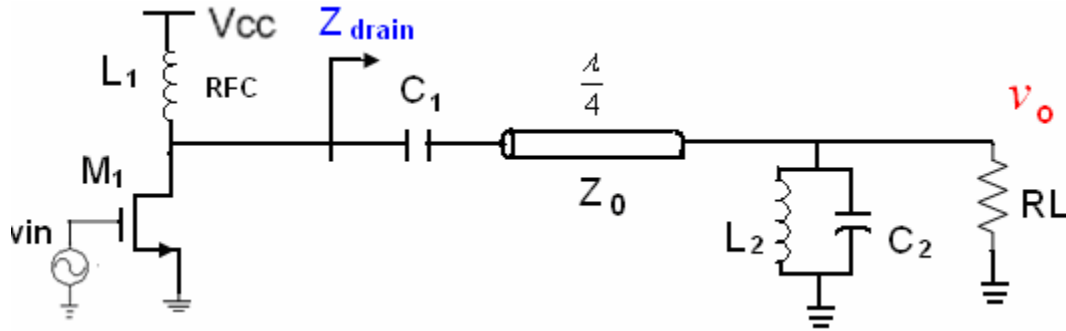


Fig. 2.11 Infinite harmonic class F power amplifier.

### Infinite harmonic class F PA

To realize zero/open at infinite even/odd harmonics the quarter-wavelength transmission line is used as shown in Fig. 2.11 [2.5]. The parallel tank  $L_2$  and  $C_2$  resonates at the fundamental frequency and it provides open at fundamental frequency and short at harmonics. Therefore, the drain of the transistor  $M_1$  sees  $R$  at fundamental and zero/open at infinite even/odd harmonics. The output voltage is given by [2.7]

$$v_o = \frac{\alpha V_{cc} \times RL}{Z_0} \quad (2.3)$$

, where  $\alpha$  is the ratio between the fundamental and DC component of the drain voltage;

$V_{cc}$  is the supply voltage;  $RL$  is the load;  $Z_0$  is the characteristic impedance of the  $\frac{\lambda}{4}$

transmission line. For the ideal infinite harmonic class F PA with square-wave drain waveform,  $\alpha$  is  $\frac{4}{\pi}$ .

However, as shown in Fig. 2.12 the capacitance  $C_{ds}$  of the transistor  $M_1$  undermines the higher-order odd harmonic termination. A small inductor  $L_{ds}$  is used to tune out  $C_{ds}$  at fundamental frequency [2.31] to mitigate the problem. It's trivial that the  $L_{ds}$  and  $C_{ds}$  is a parallel tank resonating at the fundamental frequency  $\omega_0$ , therefore,  $L_{ds}$  and  $C_{ds}$

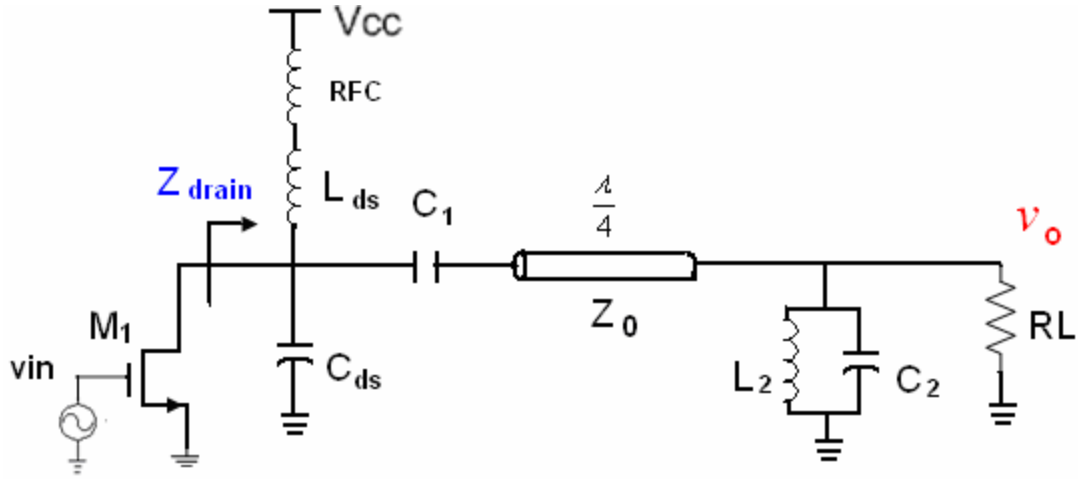


Fig. 2.12 Infinite harmonic class F power amplifier with drain-source capacitance  $C_{ds}$ .

provides impedance  $\frac{1}{j \times 2N \times \omega_0 C_{ds}}$  at odd harmonic  $(2N+1) \times \omega_0$  ( $N$  is an arbitrary positive integer). Though in practice the small  $L_{ds}$  is absorbed into RFC, it's plotted in Fig. 2.12 just for better illustration. Thus at higher-order odd harmonics the transistor  $M_1$  still sees a short, which degrades the efficiency dramatically. Actually, the problem of  $C_{ds}$  is very severe for the transmission line infinite harmonic class F PA and there are not so many papers using this topology.

### Finite harmonic class F PA

[2.6] and [2.7] shows that the first four harmonics determine the class F operation the most. When zero/open at the first four harmonics is satisfied the theoretical drain efficiency can be as high as 90%. Therefore, the finite harmonic topology trades the drain efficiency for a less complex harmonic control block and would save a lot chip

area for monolithic PAs. Another advantage is that the drain-source capacitance  $C_{ds}$  can be incorporated in the filter network and will be no harm to the harmonic

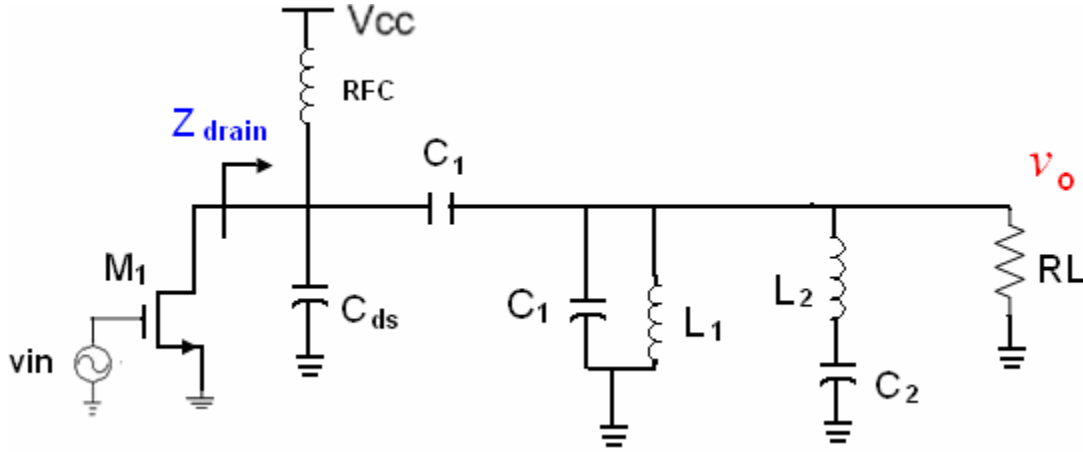


Fig. 2.13 An example of finite harmonics class F PA incorporating  $C_{ds}$ .

termination. Fig. 2.13 [2.26] is an example of the finite harmonic topology incorporating  $C_{ds}$ . In fact most of relevant papers on the class F PA are about the finite harmonic termination [2.25-2.28], [2.32] and the design of finite harmonic class F PA is similar to the filter design, which tries to realize low/high impedance at finite even/odd harmonics.

### 2.2.3.3 Class E Power Amplifier

The class E PA was first introduced by Ewing [2.8] in his doctoral thesis, and then was further elaborated by many other researchers [2.9], [2.10-2.13]. It also utilizes the active device as a switch, and thus can achieve high efficiency. This class uses a high-order

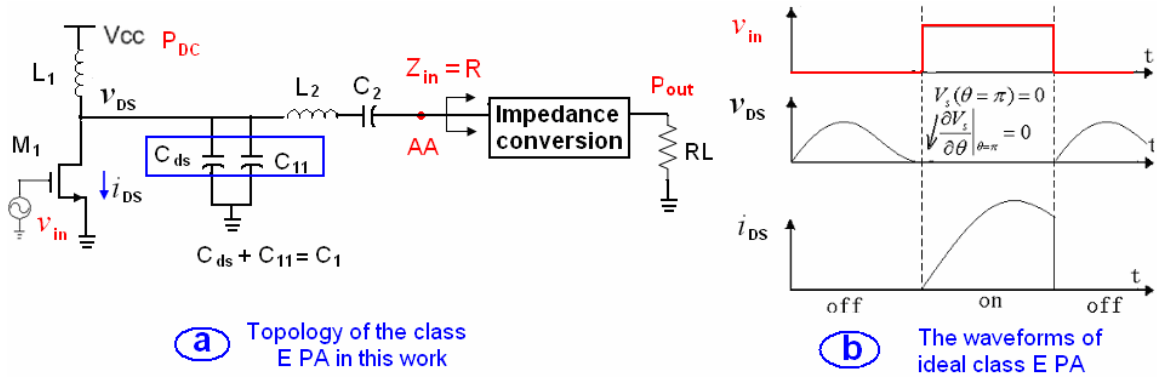


Fig. 2.14 Topology of the single stage class E power amplifier and its waveforms.

reactive network ( $L_1, C_1, C_2$  and  $L_2$ ) shown in Fig. 2.14 that reduces switch losses by helping the switch voltage to reach both zero slope and zero value at the turn-on of the switch, also known as zero voltage switching or ZVS [2.5]. As can be seen, the parasitic capacitance  $C_{ds}$  is included in the filter network.

### Time domain solutions of class E mode

Since the class E condition is in the time domain, most of the design equations are derived in time domain, which is different than in class F PA. The difference between those analysis equations is mostly in the way of switched-transistor modeling, which can be divided into three groups [1.4], [2.10-2.11] and [2.14]:

1. Zero  $R_{on}$  (the switched-on resistance of the transistor  $M_1$ ), infinite  $L_1$  and finite  $jX$  (Raab's model). To reduce the analytical complexity [2.10-2.11] assumes the drain inductance  $L_1$  is infinite and switch-on resistance  $R_{on}$  of the transistor is zero. The filter  $L_2$  and  $C_2$  at the fundamental frequency is tuned to the reactance  $X$ .
2. Non-zero  $R_{on}$ , finite  $L_1$  and finite  $jX$  [2.14] (Wang's model). The filter  $L_2$  and  $C_2$  of this PA topology in the fundamental frequency is tuned to the reactance  $X$  as well. This method has the most complete model for the switch  $M_1$ . However, only the numeric solution can be obtained.
3. Zero  $R_{on}$ , finite  $L_1$  and zero  $jX$  [1.4] (Andrei's equation). This method is a compromise between the previous two models in terms of the switch modeling. It's different from the previous two models that the filter  $L_2$  and  $C_2$  of this PA topology in the fundamental frequency is tuned to zero. Though this model doesn't include  $R_{on}$  the closed-form design equations has been achieved, which makes the design and optimization very convenient. Table 2.1 lists the input variables and output variables of the design equation of Wang's and Andrei's model. As can be seen, Andrei's equation can not work if the load  $R$  is the input variable. As a result, the mathematical function  $f(x)$  between the output power of the class E PA and the load seen by the PA block,  $Z_{in}$ , can not be achieved, which supposes to be given by  $P_{out} = f(Z_{in})$

Table. 2.1 The input variables and output variables calculated by the design equations of two models.

	Input Variable					Calculated Output				
<b>Wang's model [2.14]</b>	$f$	$V_{cc}$	$Q$	$L_1$	$C_1$	$R$	$P_{out}$	$P_{DC}$	$C_2$	$L_2$
<b>Andrei's model [1.4]</b>	$f$	$V_{cc}$	$Q$	$P_{DC}^3$		$R$	$P_{out}$	$L_1$	$C_2$	$L_2$

### Frequency domain solutions of class E mode

[2.34] derives the optimal load for the PA at fundamental and harmonic frequency using the frequency domain analysis. This frequency domain is used especially to design the class E PA implemented by the transmission lines. Actually the impedance of the load network at fundamental frequency is equal that in Raab's model [2.11]. Similar to the class F PA, however, it's very difficult to realize infinite harmonic termination in a reasonable board area. [2.34-2.37] are the major papers implementing a class E PA by transmission lines and impedance termination maximally until fifth order harmonic are realized.

### 2.2.4 Summary

Since high efficiency of the combining structure is of prime interest in this work the linear PA modes are discarded. Due to the bad capability of  $C_{ds}$  handling, the class D and class F modes are not chosen, though the finite harmonic class F could incorporate  $C_{ds}$  it still needs more passive components than class E PA and its theoretical drain efficiency is less than 90%.

As a result, the class E mode is chosen for the combining structure in this work.

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<sup>3</sup> In Andrei's model the power input variable is denoted as the expected power output. However, this model assumes no energy loss. Thus this power input variable is actually the dc power  $P_{DC}$  mentioned in Fig. 2.10

## 2.3 Power Combining Network Block

### 2.3.1 Introduction

The primary requirement of a good combining network is low loss. High power loss affects the efficiency of the whole power combining system and could make the effort of combining fruitless.

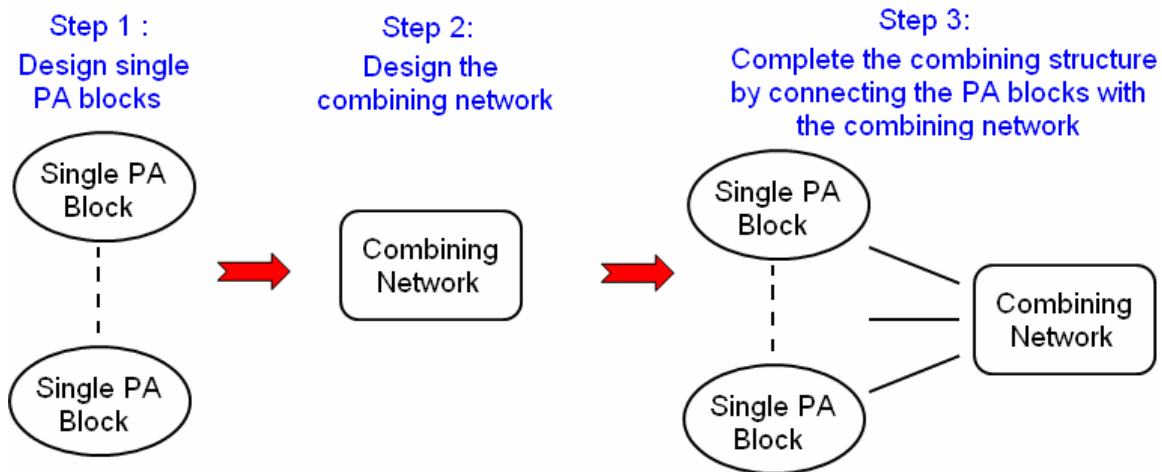


Fig. 2.15 The flow chart of the power combining structure design.

As reviewed in previous section, the design equations and analysis of each PA mode is an approximation of the PA performance to some order. Therefore, to design a single PA and achieve an optimum result is already not easy, let alone designing the power combining system containing several PA blocks. The method proposed in this work is to divide the design of the whole combining system into three steps illustrated in Fig. 2.15:

1. Design the individual PA blocks separately.
2. Design the combining network according the first step.
3. Connect the PA blocks designed in step 1 with the combining network designed in step 2.

The first step is just the same as the single PA design and any previously related experience and knowledge can be used. The procedure of the second step is the focus of this work.

This design method avoids the complexity of the large system design and could save time and efforts. However, it has the following requirement on the combining network:

- a. Provide the optimum load to each PA as designed in the first step so that the PA blocks perform optimally as expected in the first step.

- b. Each PA doesn't affect the performance of any other PA in the same combining network; which is called good isolation. Since the PA blocks are designed and optimized in the first step assuming it is single, any interference caused to the PA blocks by the combining network would degrade the design expectation.

What is preferable but not necessary function is that the combining network can be a universal module for different PA modes.

There are many techniques for power combining from multiple transistors in microwave engineering. Most of these generally fall under the category of being either planar techniques or spatial techniques [2.2] [2.15] [2.17][2.38]. Spatial power combiners are 3-D structures which combine power in waveguides, or in free space. However, in RFIC design the frequency range only covers the lowest frequency spectrum of microwave engineering thus the spatial combining technique demands much more area and space than it does in the normal microwave bands, for example, higher than 10 GHz. Only the planar combining technique is of interest in this work. In the following section the planar combining technique will be divided into two classes, namely, off-chip technique and on-chip technique, depending on the way to implement.

### **2.3.2 On-chip Power Combining Technique**

To keep the circuit as compact as possible it's desirable to integrate the power combining block in the same chip as the PA blocks. This type of power combining technique is called on-chip power combining technique. One way is the implementation of the transmission lines on-chip and uses the theory of off-chip power combining technique, which will be discussed in the later chapter. The other way is electromagnetically-coupling power combining. One example is shown in Fig. 2.16. The output power from each PA block is coupled from the primary slab inductors to the circular secondary slab inductors. Meanwhile the coupling structure provides the optimum resistive load and part of the harmonic control block to each PA block. This technique is called distributed active transformer (DAT) which was introduced in [2.21] - [2.23] and the simulated efficiency of the combining network is reported to be 70%. By far this is the only fully integrated CMOS power combining system.



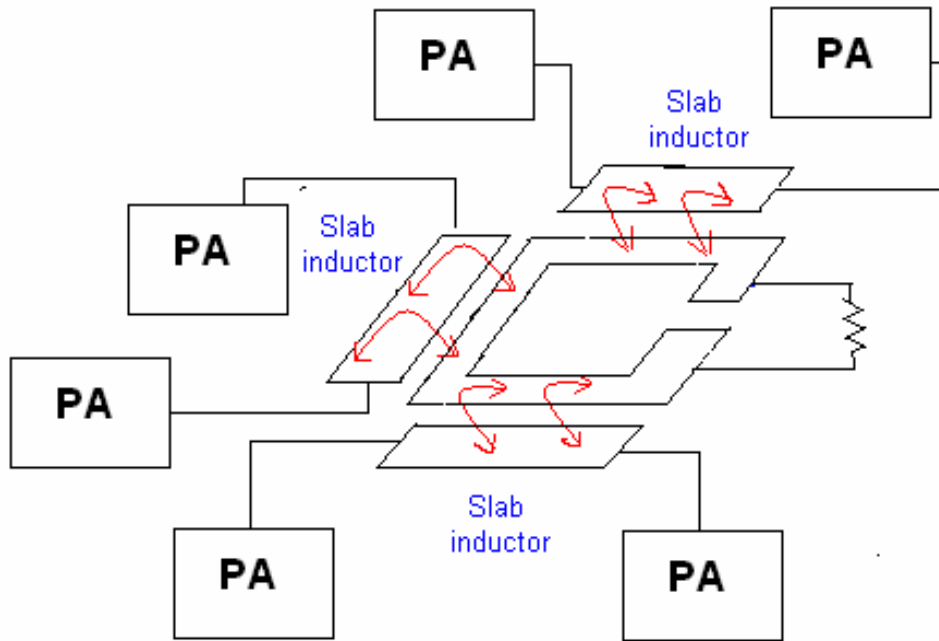


Fig. 2.16 An example of on-chip power combining technique

### Limitations facing on-chip combining network

Unlike the off-chip transmission line with inherent low loss advantages the on-chip technique has to deal with two problems:

1. Low coupling factor  $k$ . A simple electromagnetically-coupling slab inductor pair has been simulated in Sonnet shown in Fig. 2.17. This inductor pair is similar to the DAT structure shown in Fig. 2.16. Both the primary and secondary slab inductors are  $500 \times 8$   $\mu\text{m}$ . From the current density color it's shown that the mutual coupling is not high.
2. Low Q of passive elements. A  $1000 \times 40$   $\mu\text{m}$  slab inductor both in the normal CMOS18 process and the high-frequency CMOS18 process has been simulated in Sonnet. The results are shown in Fig. 2.17. Though the high-frequency CMOS18 process has higher substrate resistivity than the normal CMOS18 process the Q factor at 2 GHz is still around 7.

As a result the on-chip combining structure would be very lossy and the mutual coupling factor  $k$  could be low between the primary and the secondary coupling elements.

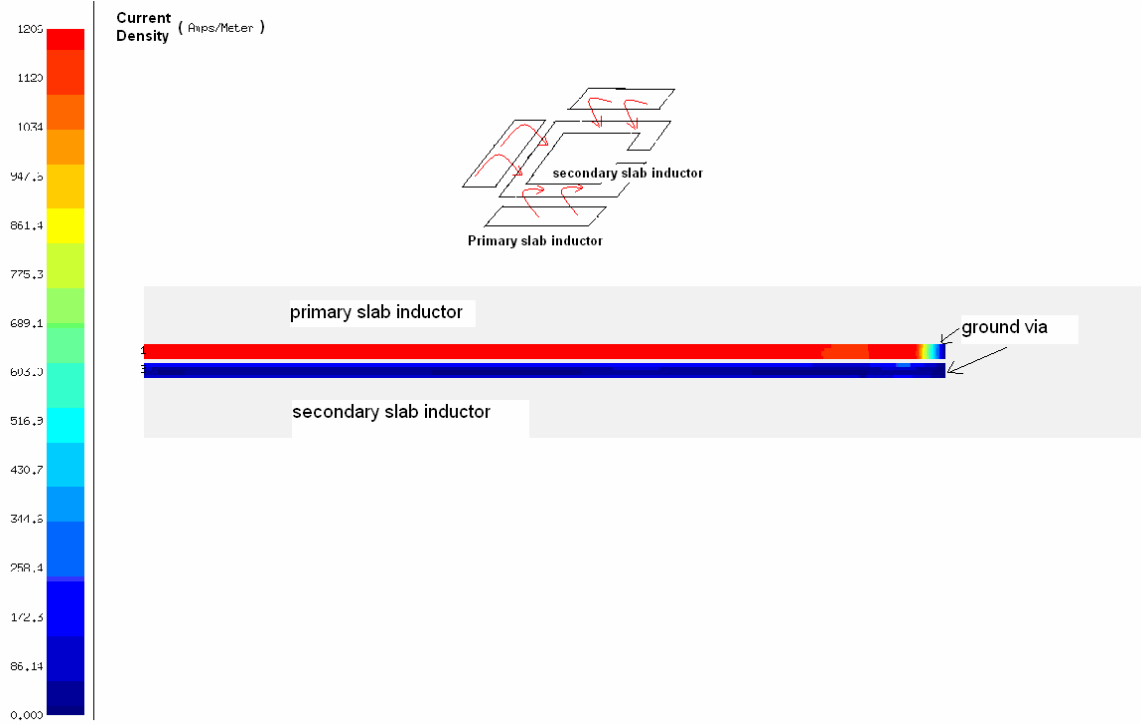


Fig. 2.17 Simulation result of the mutual coupling

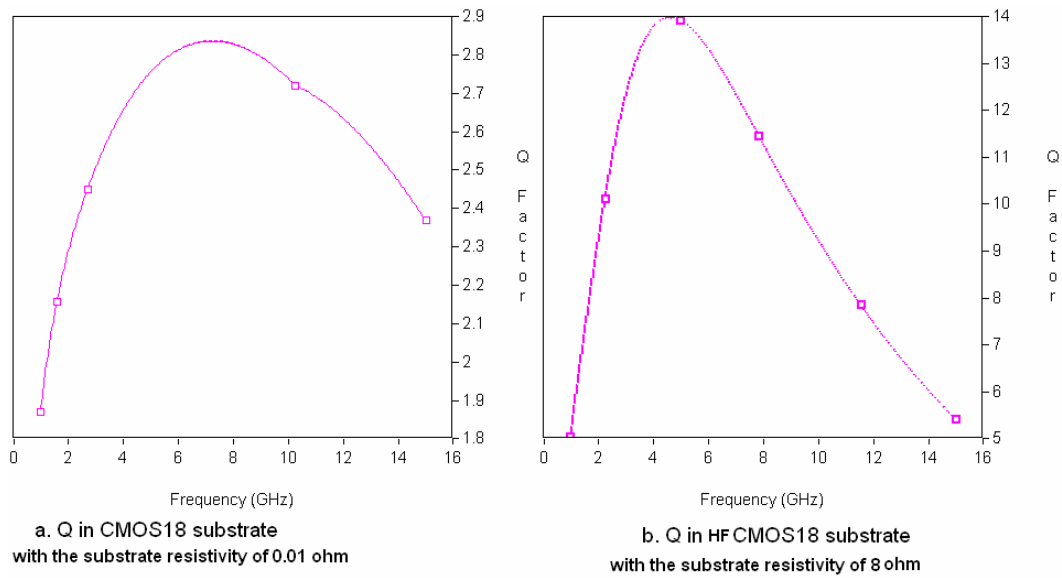


Fig. 2.18 Simulation results of Q for slab inductor in two process

### 2.3.3 Off-chip Power Combining Technique

Mostly the transmission line is used as an important element in the planar combining [2.2] [2.17]. In this work the techniques using transmission lines are classified as off-chip

technique since in RFIC design the transmission line is generally implemented in low loss PCB (printed circuit board) as microstrip lines.

The Wilkinson combiner can be generalized to an N-device combiner and all ports are isolated from each other. A disadvantage is that the combiner requires crossovers of the resistors for  $N > 3$ . This makes fabrication difficult in planar form [2.16], [2.17].

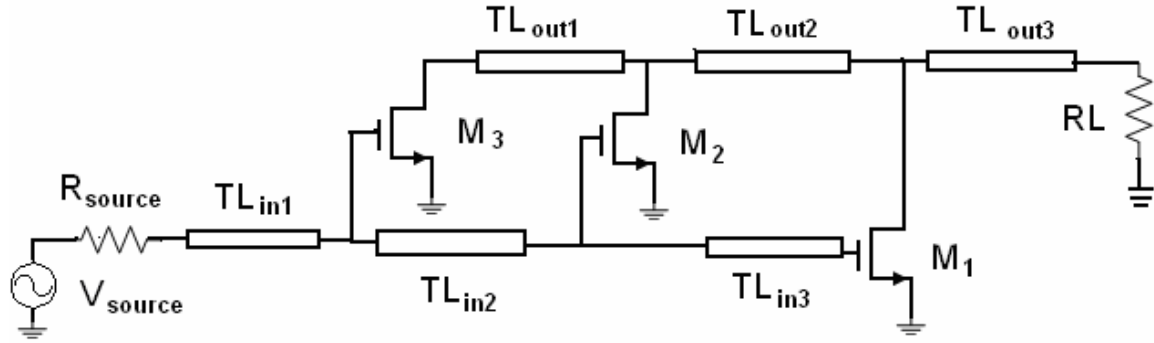


Fig. 2.19 Schematic example of a 3-device extended resonance power combining structure.

### 2.3.3.1 Extended resonance technique

One interesting method of combining power from solid-state devices was introduced, based on an extended resonance technique [2.18]-[2.20]. A standing-wave structure similar to a waveguide coupled-cavity filter is realized by resonating the device admittances with each other in order to cancel their susceptance and combine their conductance [2.18]. As shown in Fig. 2.19 the transistors  $M_1 - M_3$  are modeled as a current source controlled by the signal at the gate. The transmission lines at the input and output of the transistors are designed so that the phase delay is compensated and the power output are in phase and combined in the load. Four discrete 1-W Siemens CLY5 GaAs MESFET's with 67% power-added efficiency at 935 MHz have been combined by this technique [2.20]. A detailed analysis is given in the appendix 2.1 trying to utilize this technique. However, the extended resonance technique is based on two assumptions:

1. The input impedance of the transistor is a constant impedance and the input signal in the input branch is sinusoidal.
2. The transistors at the output branch are modeled as current source with output capacitance.

The input signal of the PA is large signal, especially for the switching PAs and the input impedance at the gates varies with the amplitude of the input signal and is not constant. What's more, the transistors in the switching PAs are a switch rather than a current source. As a result, the two assumptions are undermined.

### 2.3.3.2 The class F PA voltage summation structure

#### Old analysis reviews

[2.31] uses a parallel quarter-wavelength lines to build a digital-controlled amplification system for the infinite harmonic class F PAs shown in Fig. 2.20. It claims that the switched nMOS output transistor  $M_j$  shown in Fig. 2.20a are used as low-impedance voltage source  $V_{Mj}$  driving  $\frac{\lambda}{4}$  transmission lines shown in Fig. 2.20b. The low-impedance  $r_{sj}$  is the effective on-resistance when the transistor  $M_j$  is driven with a large gate-to-source input voltage and based on (2.3)  $V_{Mj}$  is  $\alpha \times RL \times V_{cc} \times \frac{1}{Z_{0j}}$ . After analyzing the equivalent circuit shown in Fig. 2.20b the output voltage is the summation of all voltage source  $V_{Mj}$  when  $r_{sj}$  is very small, which is given as [2.31]

$$V_{oT} = V_{M1} + V_{M2} + \dots + V_{Mn} = \alpha \times RL \times V_{cc} \times \sum_{j=1}^n \frac{1}{Z_{0j}} \quad (2.4)$$

As can be seen the analysis is based on two assumptions:

1. The switched transistor can be modeled as a voltage source with low source impedance.
2. The parasitic drain-source capacitance of the switched transistor is neglected.

Nevertheless, as discussed before the drain-source capacitance of the switched transistor provide short-circuit in every higher-order harmonic and impose a huge problem for the transmission line infinite harmonic class F. What's more, the switched transistor is on and off during each half period and is not a linear device. As a result, these two assumptions undermine the reasonability of the result in (2.4).

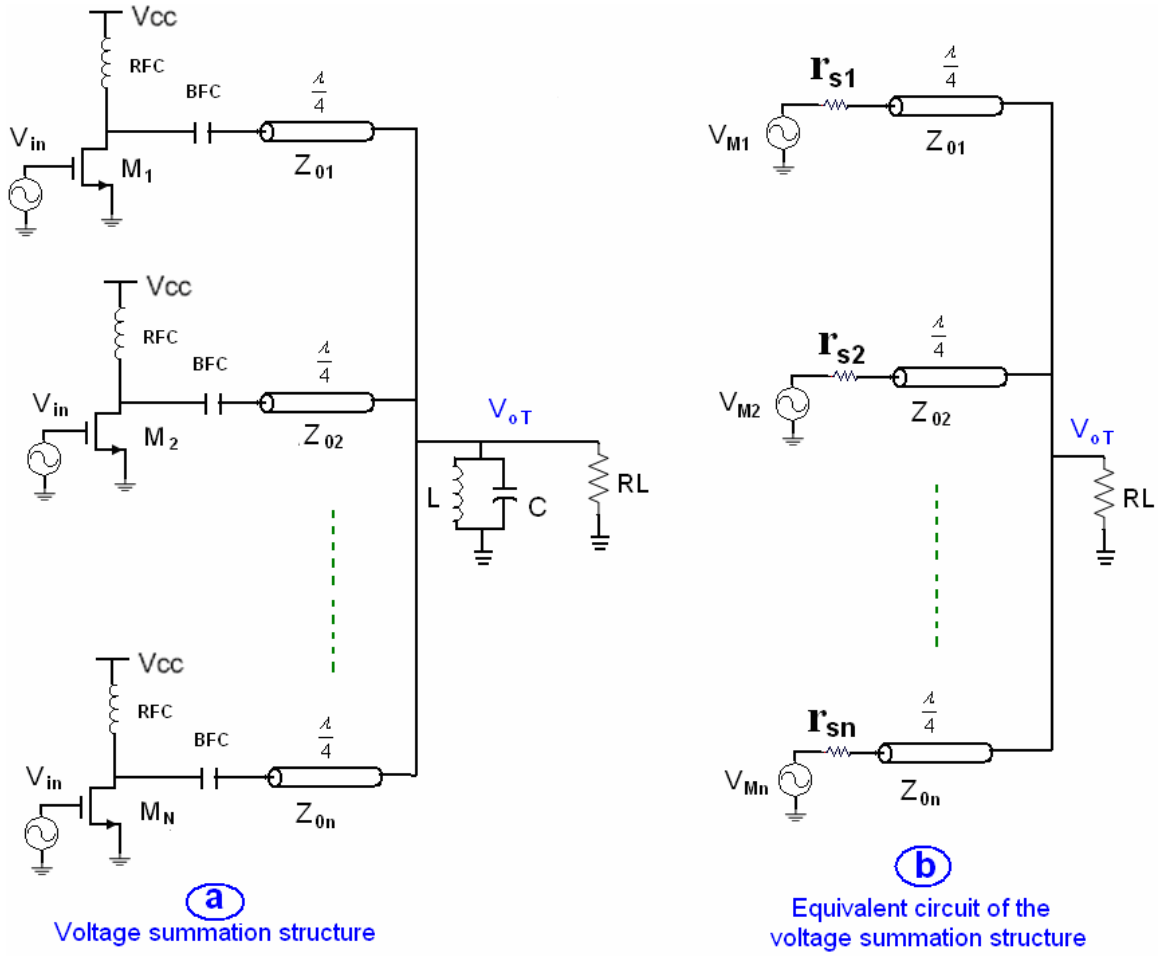


Fig. 2.20 Schematic of the class F voltage summation structure and its equivalent circuit in [2.31]

### 2.3.3.3 Summary

The parallel transmission line structure shows the potential for the power combining design in this work, though a solid analysis is not available. In the next chapter a new analysis for this voltage summation structure is proposed and this structure is explored.

## 2.4 Summary

The three-step designing method of the power combining structure for this work is proposed. Based on the designing method the PA block and combining network block are chosen. The linear PA modes are not suitable for PA block of the power combining structure due to the low efficiency and class E mode is chosen. The parallel transmission line structure will be fully analyzed and explored in the next chapter for the combining network block.



## Chapter 3

### *N*-device Unbalanced Combining Technique

#### 3.1 Introduction

In this chapter the parallel transmission line structure is fully analyzed and a new power combining technique is proposed based on this structure, which theoretically can combine the output power of  $N$  arbitrary PAs. At first the parallel transmission line is explored. Secondly a theoretical analysis for the new power combining technique is presented. The simulation results to verify the theory are followed. At last a discussion and summary end this chapter

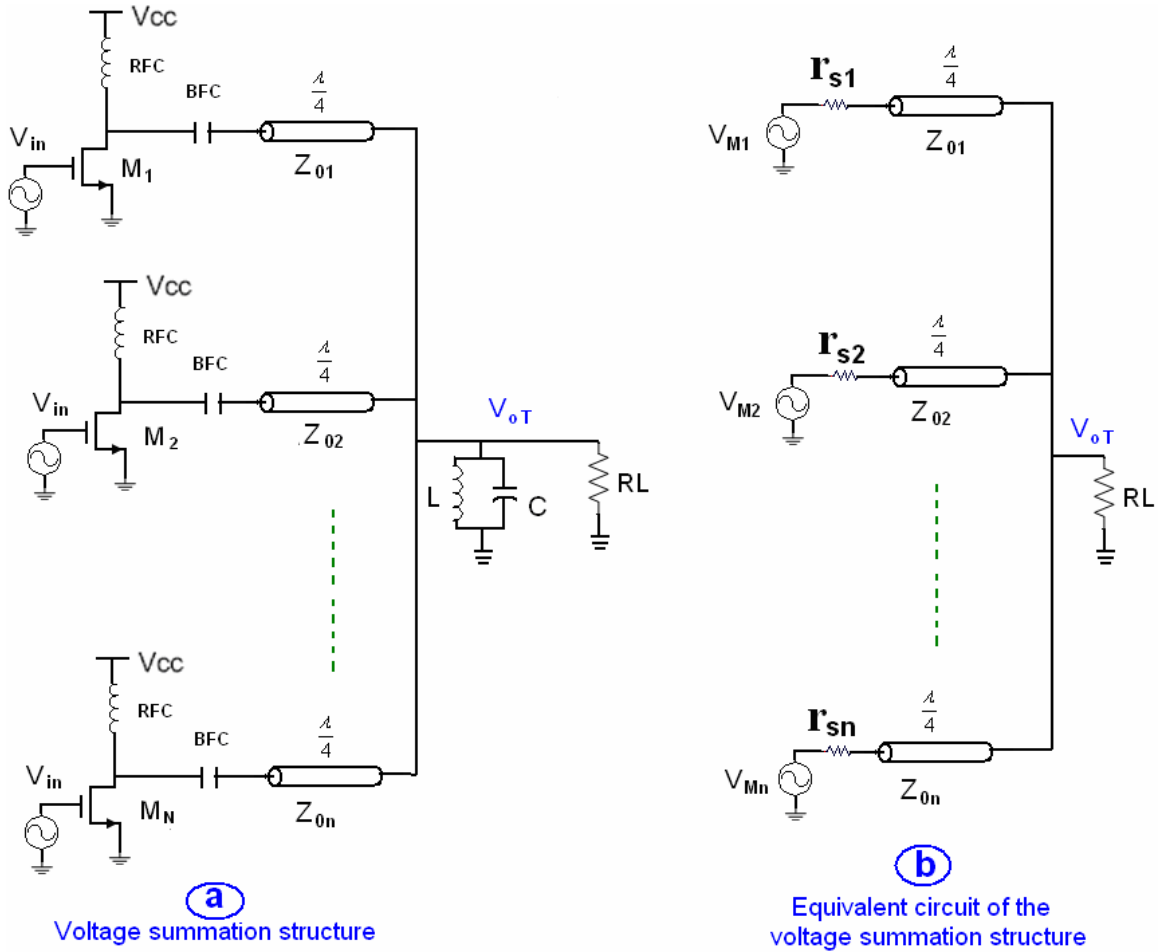


Fig. 3.1 Schematic of the class F voltage summation structure and its equivalent circuit in [2.31].

### 3.2 Voltage summation structure

As discussed in section 2.3.3.2, the parallel quarter-wavelength transmission line structure sums the output voltage of each class F PA shown in Fig. 3.1 (redrawn of Fig. 2.31). However, the two assumptions the analysis based on [2.31] is not solid. Due to the potential usefulness of the parallel quarter-wavelength transmission line structure, a more reasonable analysis is proposed for this voltage summation structure and a verification using simulations is given.

#### 3.2.1 New analysis for the voltage summation structure

As shown in Fig.3.2b in the new analysis the switched transistor is modeled by an ideal switch instead of a voltage source. The supply voltage is not necessarily the same for a more general case. As introduced previously in section 2.2.3, *BFC* and *RFC* are DC block capacitance and DC feed inductor respectively, the parallel tank *L* and *C* is assumed to be an ideal filter with high *Q*. Thus they are assumed to have no non-ideal effect in the summation structure and can be neglected in the following analysis.

##### Analytical derivation

In fact the voltage summation structure shown in Fig.3.2b is the voltage combination of *N* arbitrary single-stage class F PAs, which are connected directly to a load *RL* without changing anything. Fig. 3.2a and 3.2b together give a good illustration. The first impression is that all the PA blocks in the summation structure will interact with each other and it's very complex to make a full analysis for the whole system either in time or frequency domain. Therefore, a more straightforward and easier equivalent circuit shown in Fig. 3.2c is used, which can satisfy the following conditions to ensure that the equivalent circuit is the same as the summation circuit shown in Fig. 3.2b:

$$RL_1 // RL_2 // \dots // RL_n = RL \quad (3.1)$$

$$V_{oT} = V_{o1}' = V_{o2}' = \dots = V_{on}' \quad (3.2)$$

For the ideal infinite harmonic class F PA block *PA<sub>j</sub>*, any value of the load *RL<sub>j</sub>* corresponds to an optimal condition, where different output power will be generated. (While for ideal class E PA there is only one optimal value for *RL<sub>j</sub>*; this difference



between ideal class E and class F PA is a key point for understanding the following analysis). The voltage output of PA block  $PA_j$  of the equivalent circuit is given by (2.3)

$$V_{oj}' = \frac{\alpha_j V_{ccj} \times RL_j}{Z_{0j}} \quad (3.3)$$

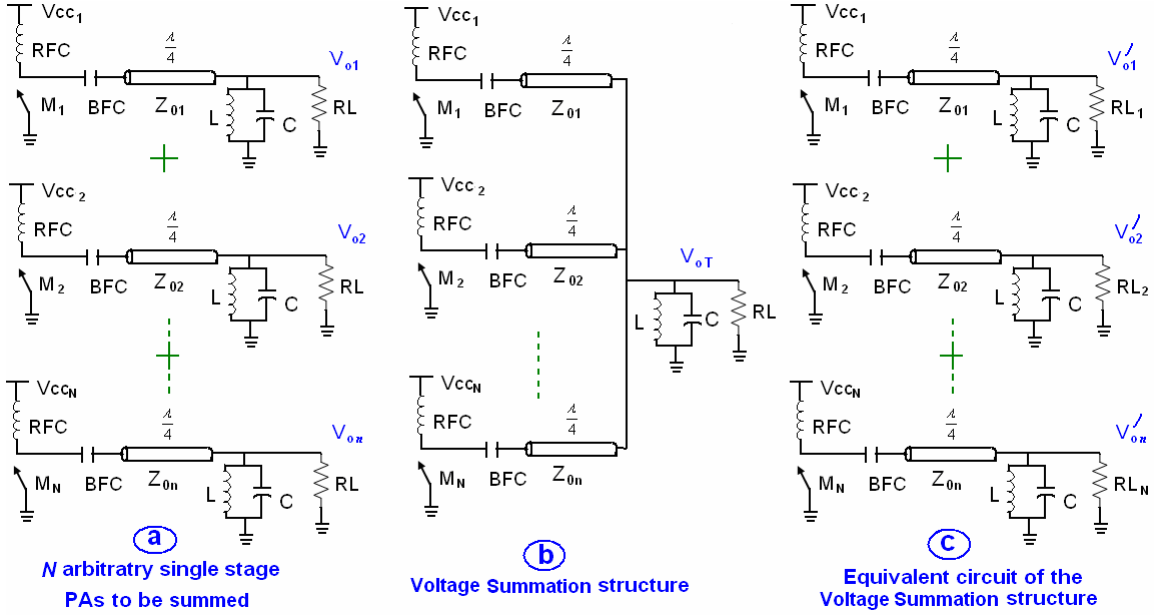


Fig. 3.2 The voltage summation structure for ideal class F PAs and its equivalent circuit.

Now for the equivalent circuit in Fig. 3.2c let  $\frac{\alpha_j V_{ccj}}{Z_{0j}} = \frac{1}{K_j \times Z_0}$  and  $RL_j = K_j \times RL$  where  $K_j$  and  $Z_0$  are just intermediate algebra variables.

Using (3.3) the output voltage  $V_{oj}'$  for the equivalent circuit is given by

$$V_{o1}' = V_{o2}' = \dots = V_{on}' = \frac{RL}{Z_0} \quad (3.4)$$

Therefore, the equivalent circuit is equal to the voltage summation structure shown in Fig. 3.2b;  $RL_j = K_j \times RL$  is the value for each load in the equivalent circuit and satisfies (3.1). Thus substituting  $RL_j = K_j \times RL$  into (3.1) gives

$$\begin{aligned} \frac{1}{K_1 \times RL} + \frac{1}{K_2 \times RL} + \dots + \frac{1}{K_n \times RL} &= \frac{1}{RL} \\ \Leftrightarrow \frac{1}{K_1} + \frac{1}{K_2} + \dots + \frac{1}{K_n} &= 1 \end{aligned} \quad (3.5)$$

Based on (2.3) the output voltage summation of each single-stage PA in Fig. 3.2a is given by

$$V_{o1} + V_{o2} + \dots + V_{on} = \frac{RL}{K_1 \times Z_0} + \frac{RL}{K_2 \times Z_0} + \dots + \frac{RL}{K_n \times Z_0} \quad (3.6)$$

Assembling (3.4-3.6) gives

$$\begin{aligned} V_{o1} + V_{o2} + \dots + V_{on} &= \frac{RL}{Z_0} = V_{oT} \\ \Leftrightarrow V_{oT} &= V_{o1} + V_{o2} + \dots + V_{on} \\ &= RL \times \sum_{j=1}^n \frac{\alpha_j \times V_{ccj}}{Z_{0j}} \end{aligned} \quad (3.7)$$

Note that the result of [2.31] shown in (2.4) is the special case when  $\alpha_j$  and the supply voltage  $V_{ccj}$  are the same for each single-stage class PA.

(3.7) gives the combined output power of the voltage summation structure

$$P_{oT} = \frac{V_{oT}^2}{2 \times RL} = \frac{(V_{o1} + V_{o2} + \dots + V_{on})^2}{2 \times RL} \quad (3.8)$$

The power output summation of the voltage summation structure shown in Fig. 3.2a is given by

$$P_{o1} + P_{o2} + \dots + P_{on} = \frac{V_{o1}^2}{2 \times RL} + \frac{V_{o2}^2}{2 \times RL} + \dots + \frac{V_{on}^2}{2 \times RL} < \frac{(V_{o1} + V_{o2} + \dots + V_{on})^2}{2 \times RL} \quad (3.9)$$

Comparing (3.8) and (3.9) tells that the voltage summation structure sums the voltage output of each PA block rather than the power output.

### Simulation verification

A two-device voltage summation structure is simulated in ADS shown in Fig. 3.3. The voltage-controlled switch component “SwitchV”<sup>1</sup> is used to build the ideal infinite harmonic class F power amplifier  $PA_1$  and  $PA_2$ .

Before the summation each PA is simulated in single stage. Table 3.1 shows the simulation parameters for  $PA_1$  and  $PA_2$ . Due to the non-zero switch-on resistance of the switch the drain efficiency couldn't achieve completely 100% and the simulated voltage output for  $PA_1$  and  $PA_2$  is not exactly the same as it was calculated from 2.3. However,

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<sup>1</sup> To save the simulation time the switch-on resistance of the switch isn't set too small. 0.05 ohm is a reasonable value being used.

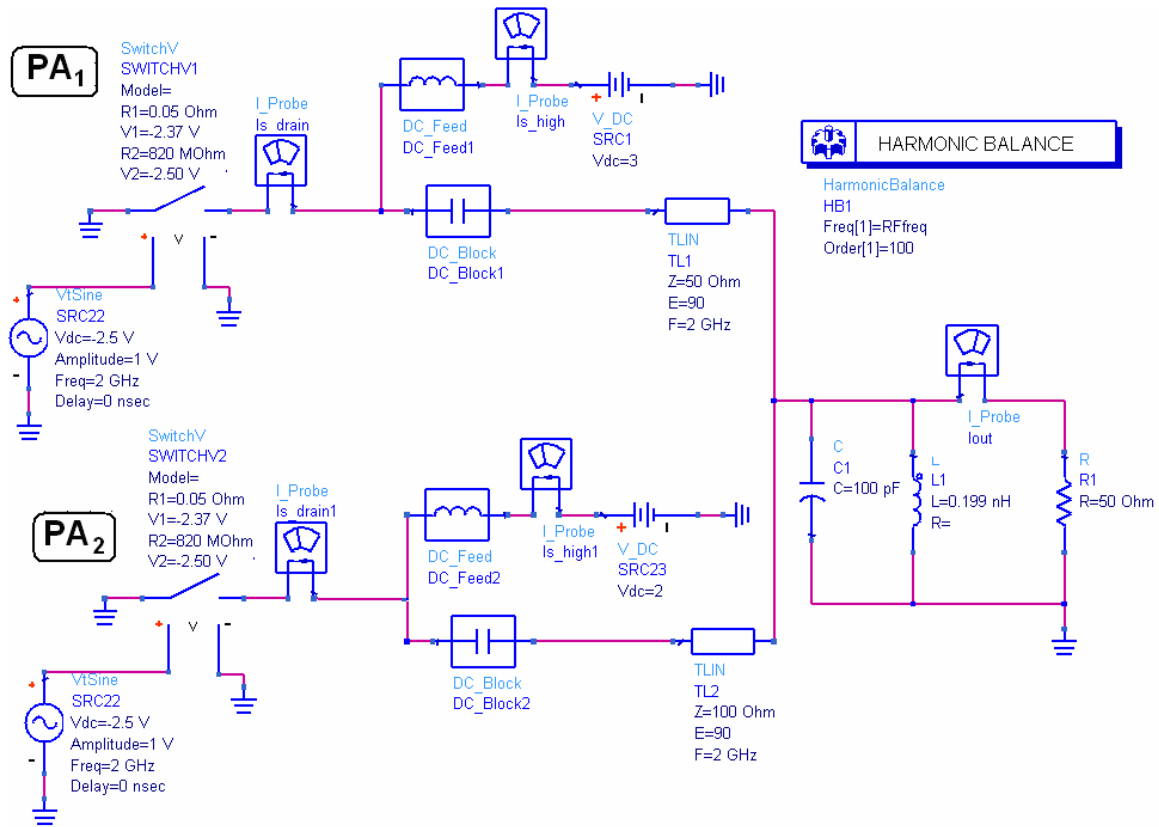


Fig. 3.3 The simulation circuit of the two-device voltage summation structure.

Table. 3.1 The simulation parameters of  $PA_1$  and  $PA_2$  when they are in single stage.

		$PA_1$	$PA_2$
$V_{cc}$ (V)		3	2
$RL$ (ohm)		50	50
$Z_0$ (ohm)		50	100
$V_o$ ( V )	Simulated output voltage	3.81	1.272
	Calculated output voltage	3.82	1.273
Drain efficiency		99.8%	99.9%
Output power ( mW)		145	16

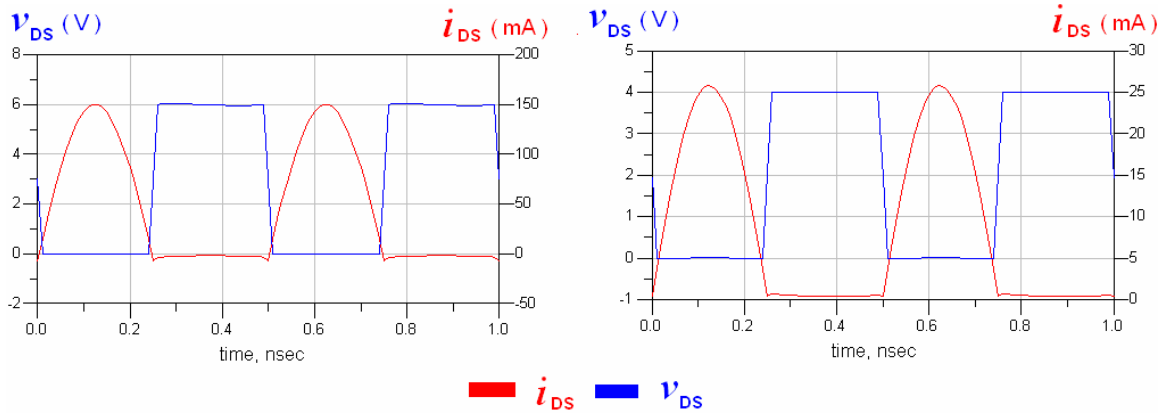


Fig. 3.4 The simulation result of the drain voltage and current waveform of  $PA_1$  and  $PA_2$  when they are in single stage.

it's reasonable to say that the  $PA_1$  and  $PA_2$  are the ideal infinite harmonic class F PA, which could also be verified by the waveform simulation result of the drain voltage and current shown in Fig. 3.4.

After putting  $PA_1$  and  $PA_2$  into the voltage summation structure shown in Fig. 3.3. The simulation results of the output voltage and power of  $PA_1$  and  $PA_2$  are listed in Table 3.2, which shows the output voltage of  $PA_1$  and  $PA_2$  are added together. At last the minor difference between the values of “summation  $V_o$ ” should be noticed. The major reason is the minor phase difference between the output voltage of  $PA_1$  and  $PA_2$ , which is around 0.1 degree. This shows that the derived result (3.7) is valid when there is no phase difference between the output voltages to be summed. This equal-phase assumption

Table 3.2 The simulation results of  $PA_1$  and  $PA_2$  before and after summation.

	Before summation		After summation
	$PA_1$	$PA_2$	Total
Single $V_o$ ( V )	3.81	1.272	None
Summation $V_o$ ( V )	5.082		5.078
Drain efficiency	99.8%	99.9%	99.7%
Output power (mW)	145	16	258
	161		

will be discussed further in section 4.2. In summary the parallel quarter-wavelength transmission lines can provide voltage summation for  $N$  arbitrary single-stage class F PAs and therefore is called voltage summation structure.

### 3.2.2 Limitations for the voltage summation structure

The general result of the voltage summation structure derived in (3.7) seems to have high potential. Within the voltage summation structure the output voltage of each PA block is summed and the combined power is even larger than the power output summation of the  $N$  arbitrary single-stage class F PAs. However, (3.7) is based on the ideal transmission-line infinite harmonic class F PA with an ideal switch. In practice there are two major limitations:

1. Non-zero drain-source capacitance of the switched transistor
2. Non-zero switch-on resistance of the switched transistor.

#### Non-zero drain-source capacitance effect

As discussed in 2.2.3.3 the drain-source capacitance  $C_{ds}$  provides a short to the switched transistor at all high harmonics, which undermines the class F condition of “open at odd harmonics”. Though a small inductance can tune out  $C_{ds}$  at the fundamental frequency, at high harmonics it still doesn't help. To show the effect of the drain-source capacitance  $C_{ds}$  an infinite harmonic class F PA is simulated in ADS at 2 GHz shown in Fig 3.5.

Though the drain-source capacitance of the transistor is nonlinear the simple linear capacitance component  $C_{ds}$  in Fig3.5 can still show the effect on class F PA. Based on the simulation result in Cadence Spectre, the effective switch-on resistance of the NMOS transistor in Philips CMOS18 process is around 0.1 ohm when the width is 6800 um, which results a 6.3 pF effective  $C_{ds}$ . Thus the switch-on resistance is set to 0.1 ohm and  $C_{ds}$  is swept from 0 to 6 pF. The inductor  $L_{ds}$  is resonant with  $C_{ds}$  at the fundamental frequency. As shown in Fig. 3.6, though the output voltage stays almost the same, the drain efficiency drops drastically from 99.6% when  $C_{ds}$  is zero to 24.5% when  $C_{ds}$  is 6 pF. Note that even with  $C_{ds}$  being 1 pF the drain efficiency already drops to 63%,

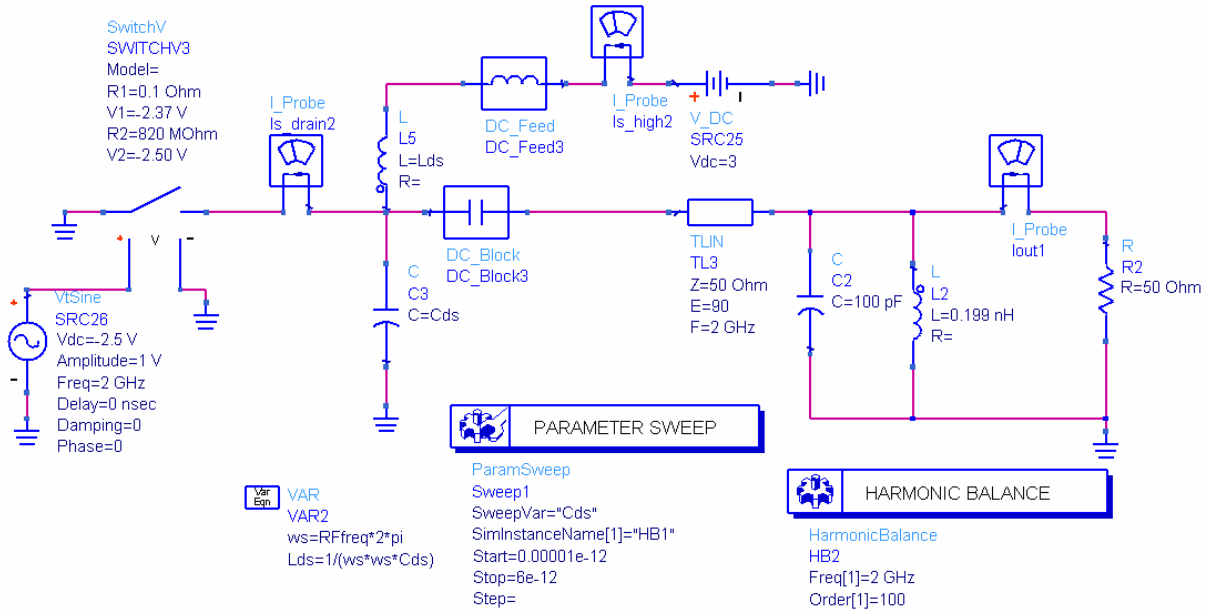


Fig. 3.5 Simulation circuit of the infinite harmonic class F PA with parasitic capacitance  $C_{ds}$ .



Fig. 3.6 Simulation results of the effect on the output voltage and drain efficiency of infinite harmonic class F PA by  $C_{ds}$ .

meaning that a very small  $C_{ds}$  would degrade the infinite harmonic class F PA a lot. Finally Fig. 3.7 shows that the drain current waveform degrades from the half sinusoid and causes large overlaps with the drain voltage when  $C_{ds}$  is 6 pF. Since an ideal switch is used the drain voltage still keeps the square-wave shape. If a real transistor is used, the drain voltage degrades further and more overlap happens.

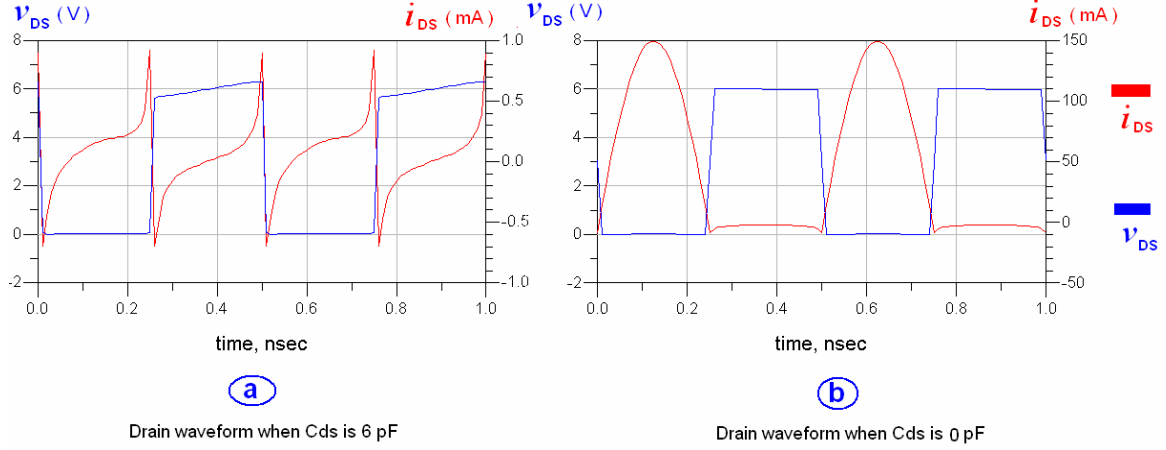


Fig. 3.7 Drain waveform comparisons between when  $C_{ds}$  is 0 pF and 6 pF.

### Non-zero switch-on resistance $R_{on}$

The non-zero switch-on resistance obviously reduces the drain efficiency. Even worse, it degrades the voltage summation capability for the voltage summation structure. Looking back in section 3.2.1 the analytical derivation is based on the assumption that for each PA block the output voltage, characteristic impedance and the resistive load hold

$$V_{oj} = \frac{K_j \times RL_j}{Z_{0j}} \quad (3.10)$$

However, the non-zero switch-on resistance  $R_{on}$  will invalidate (3.10), which degrades the voltage summation.

Though the equation for the output voltage of the infinite harmonic class F PA including non-zero  $R_{on}$  is not available so far, a simulation result illustrates this problem. The infinite harmonic class F using an ideal switch with 2-ohm  $R_{on}$  is simulated shown in Fig. 3.8 and the simulated result is shown in Fig. 3.9. The real function between the output voltage  $V_o$  and the load  $RL$  is obtained by curve fitting the simulation result, which is given by

$$V_o = K \times RL + A \quad (3.11)$$

, where  $K = 0.0377$  and  $A = 0.4675$ .

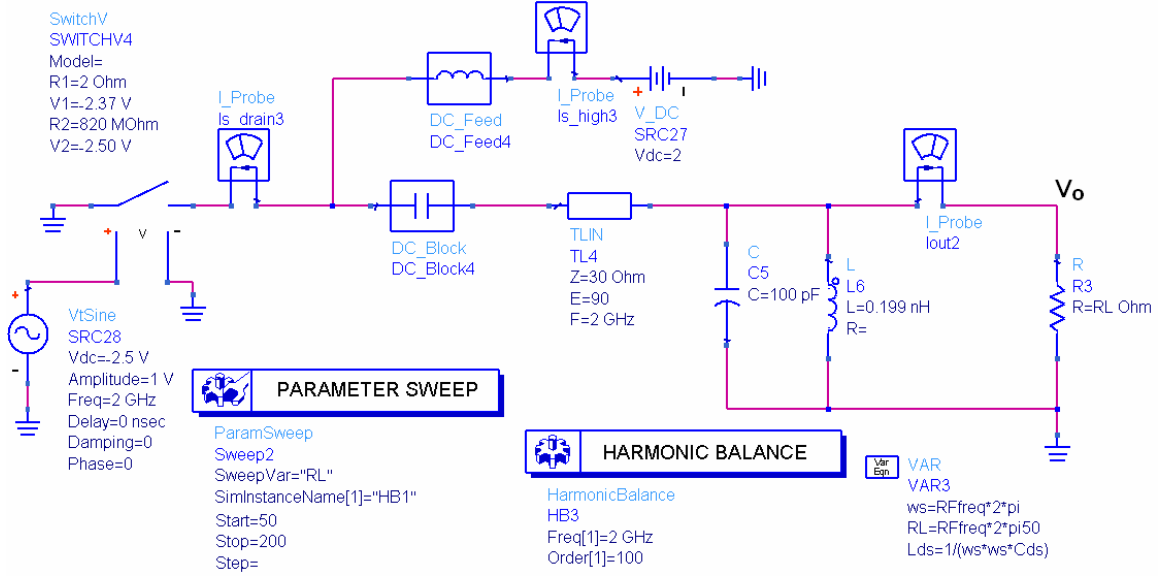


Fig. 3.8 The simulation circuit of the infinite harmonic class F with non-zero  $R_{on}$ .

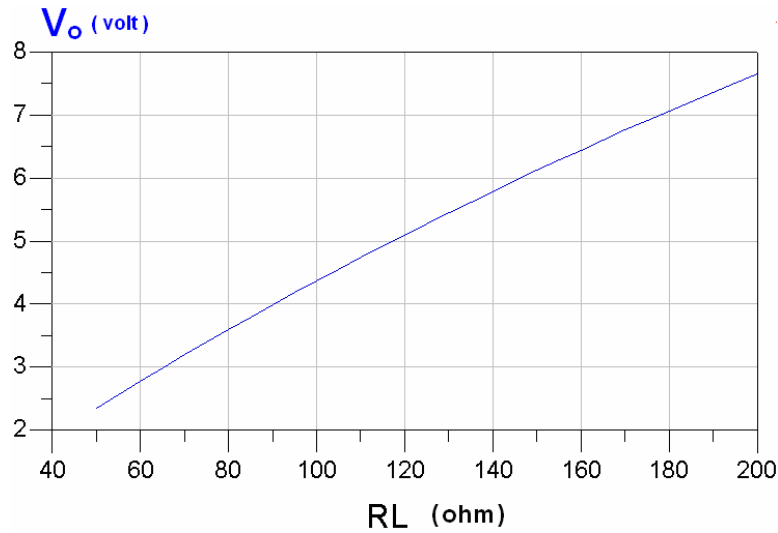


Fig. 3.9 The simulation result of output voltage VS the sweeping load resistance  $RL$ . After obtaining the real function between the output voltage  $V_o$  and  $RL$  for the PA block the  $N$ -device identical voltage summation shown in Fig. 3.10a can be analyzed. The load  $RL$  in the voltage summation structure shown in Fig. 3.10a is divided into  $N$  loads in parallel (with the value of  $N \times RL$ ) and the equivalent circuit shown in Fig. 3.10b is obtained by equally splitting the voltage summation structure into  $N$  identical single-stage



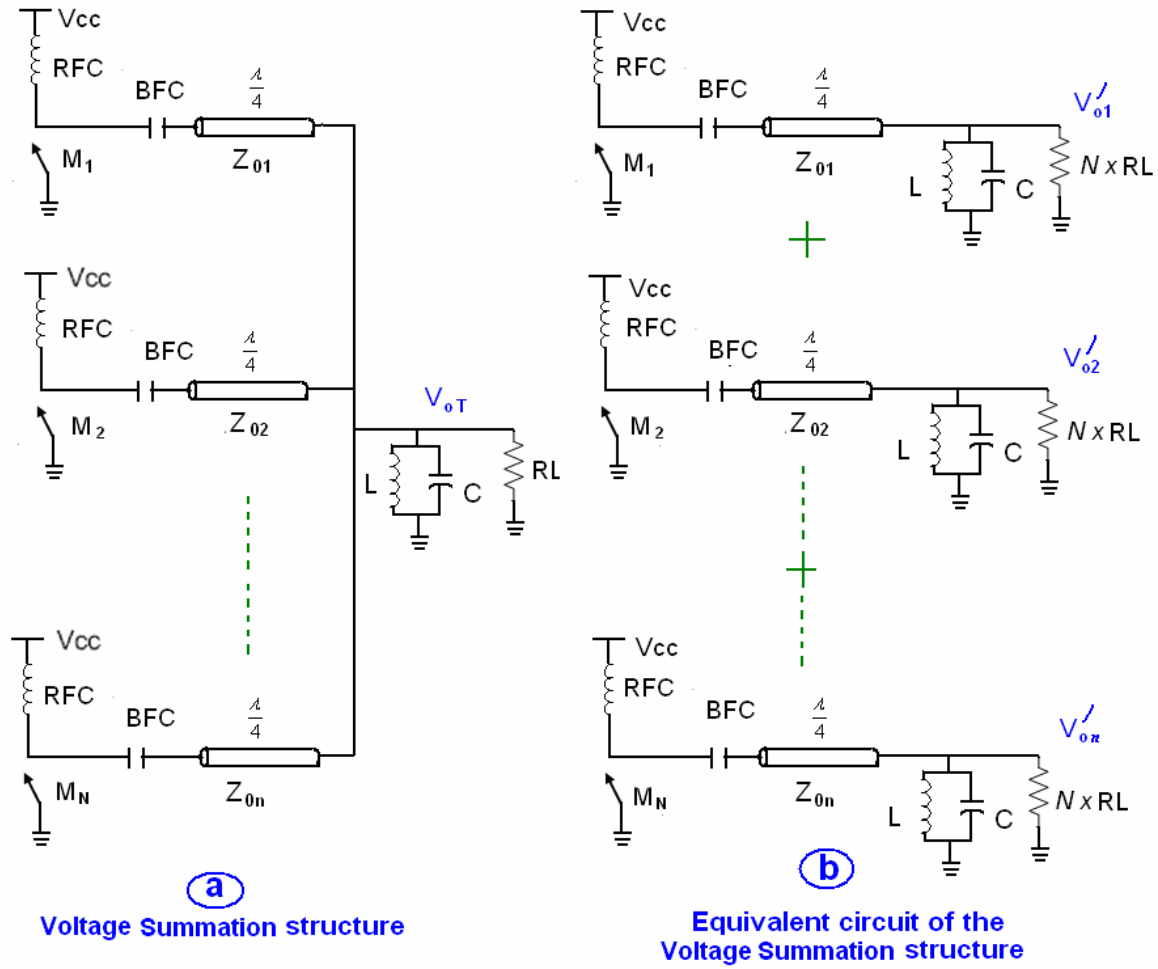


Fig. 3.10  $N$ -device identical voltage summation structure and its equivalent circuit.

PAs. As a result, the summed voltage output  $V_{oT}$  is equal to the output voltage  $V_{oj}'$  in the equivalent, which is given by

$$V_{oT} = V_{o1}' = V_{o2}' = \dots = V_{on}' \quad (3.12)$$

For the output voltage  $V_{oj}'$  of each single-stage PA in the equivalent circuit (3.11) can be used and gives

$$V_{o1}' = \dots = V_{oj}' = \dots = V_{on}' = K \times N \times RL + A = N \times V_o - (N-1) \times A \quad (3.13)$$

Combining (3.12) and (3.13) the voltage output of the voltage summation structure shown in Fig. 3.10a is given by

$$V_{oT} = N \times V_o - (N-1) \times A \quad (3.14)$$

However, based on (3.7) the ideal value of  $V_{oT}$  is  $V_{oT} = N \times V_o$ , where is difference is  $(N-1) \times A$ .

As a result the voltage summation has a negative offset of  $(N-1) \times A$  compared to the ideal value. For example, in a 3-device identical voltage summation structure using the PA block shown in Fig. 3.8  $N=3$ ,  $K=0.0377$  and  $A=0.4675$ . The expected voltage summation is  $7.056\text{ V}$  but the real value is  $6.121\text{ V}$ .

### 3.2.3 Voltage summation or power summation

As discussed in the previous section, due to the non-zero drain-source capacitance and switch-on resistance of the switched transistor, the infinite harmonic class F degrades the voltage summation of the parallel quarter-wavelength transmission line structure. As a result, the class E PA block might replace the class F mode for the voltage summation structure and this idea is explored in this section. For better understanding the ideal of the voltage summation is generalized at first.

#### General model of voltage summation

The voltage summation structure discussed in section 3.2.1 and 3.2.2 can be generalized as shown in Fig. 3.11 based on the proposed design method of the power combining structure in section 2.3.1.

1. Design the individual PA blocks separately shown in Fig. 3.11a.
2. Design the combining network according to the first step. As shown in Fig. 3.11b, in the voltage summation structure the parallel quarter-wavelength transmission lines are directly used from the circuit in Fig. 3.11a accordingly. Therefore, the parallel quarter-wavelength transmission lines serve as both the output matching and voltage summation network.
3. Connect the PA blocks designed in step 1 with the combining network designed in step 2.

The analysis of the voltage summation structure shown in Fig. 3.11b involves many PA blocks and their interaction with each other, which is very complex. Therefore, the equivalent circuit shown in Fig. 3.11c is used to save the time and efforts, where the summation structure is divided into  $N$  arbitrary single-stage PA blocks. This converts

the complex problem back to the single-stage PA analysis, which most people are familiar with. Note that for each PA block only the load  $RL_j$  changes in the equivalent

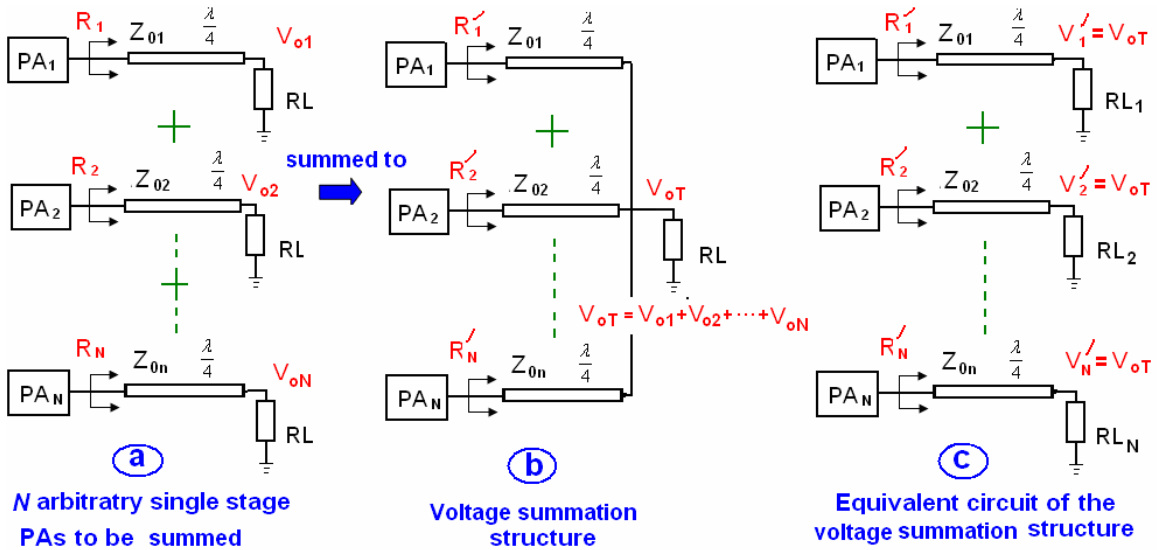


Fig. 3.11 Illustration of the general voltage summation circuit.

circuit compared with the original single-stage PA blocks show in Fig. 3.11a.

As discussed previously, the voltage summation result is achieved only if (3.10) is satisfied for each PA block, otherwise the voltage summation capability is degraded or even disappears. The voltage summation structure using non-ideal infinite harmonic class F PA is an example.

### Class E block option

As another high-efficiency PA mode, class E PA block might be suitable for the voltage summation structure. As been known, each class E PA is designed optimally in step 1 shown in Fig. 3.11a. Assume the class E PA is ideal (using ideal switch) and designed based on Andrei's model discussed in section 2.2.3.3. The output voltage for PA block  $PA_j$  is given by [1.4]

$$V_{oj} = \frac{1.65 \times V_{cc} \times RL}{Z_{0j}} \quad (3.15)$$

However, (3.15) only holds for the optimum class E mode. Any changes in the PA block such as  $Z_{0j}$  or  $RL$  would deviate from the optimum condition, which is in a different case from the ideal infinite harmonic class F PA. As long as the harmonic termination holds the class F PA stays in the optimum condition even  $Z_{0j}$  or  $RL$  changes.

In the equivalent circuit, the load that each class E PA block  $PA_j$  sees changes from  $RL$  to  $RL_j$ , while any other components of the class E PA keep unchanged compared with the original single PA block shown in Fig. 3.11a and Fig. 3.11b. Definitely the PA blocks go out of the optimum condition and (3.10) will not hold. As a result, even the ideal class E PA block using the ideal switch is not suitable for this voltage summation structure.

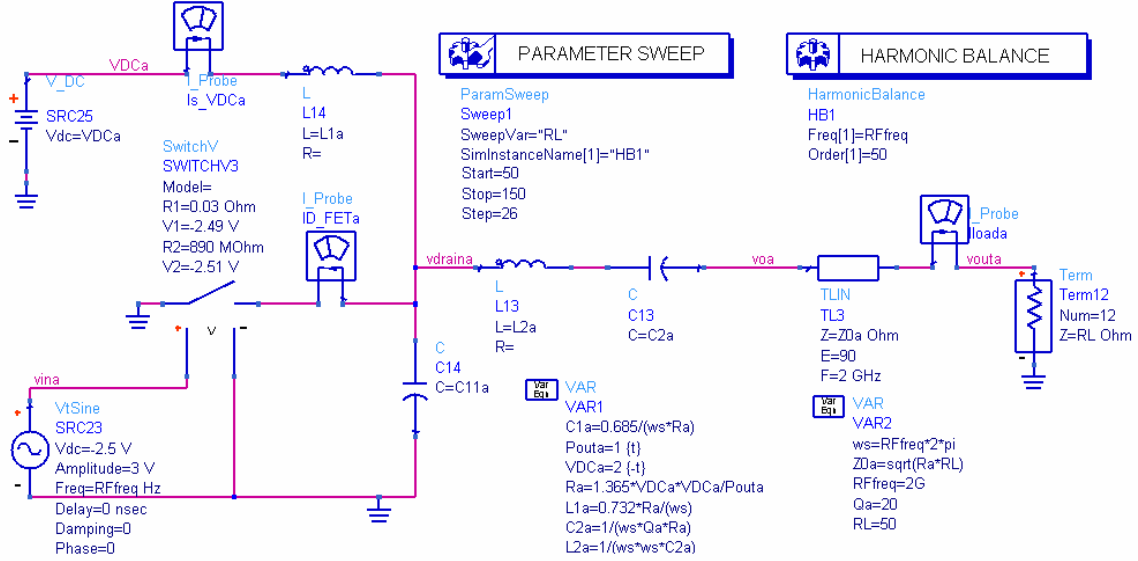


Fig. 3.12 Simulation circuit to check the effect of the changing  $RL$  on ideal class E PA.

The same simulation as shown in Fig. 3.8 could illustrate the effect of changing  $RL$  on the ideal class E PA. The ideal single-stage class E using ideal switch with 0.03 ohm  $R_{on}$  is simulated shown in Fig. 3.12. By sweeping  $RL$  from 50 ohm to 150 ohm<sup>2</sup> the effect on the output voltage is shown in Fig. 3.14. It can be seen in Fig. 3.13 how the optimal class E condition been changed by the change of  $RL$ <sup>3</sup>. The real function between the output voltage  $V_o$  and  $RL$  is obtained by curve fitting the simulation result, which is also given by

$$V_o = K \times RL + A \quad (3.16)$$

, where  $K = 0.1511$  and  $A = 2.315$ .

Since the function (3.16) is similar to that of a class F PA, (3.13) and (3.14) can be applied for the class E  $N$ -device identical voltage summation structure. As a result, the

<sup>2</sup> The optimum value of  $RL$  for this ideal class E PA is 50 ohm.

<sup>3</sup> The big current spike shown in Fig. 3.13b is due to the usage of a ideal switch in the simulation.

summation voltage has a negative offset of  $(N-1) \times A$  compared to the ideal value and the class E PA block is not suitable for the voltage summation structure. Take a 3-device identical voltage summation structure as an example, where the single-stage class E PA

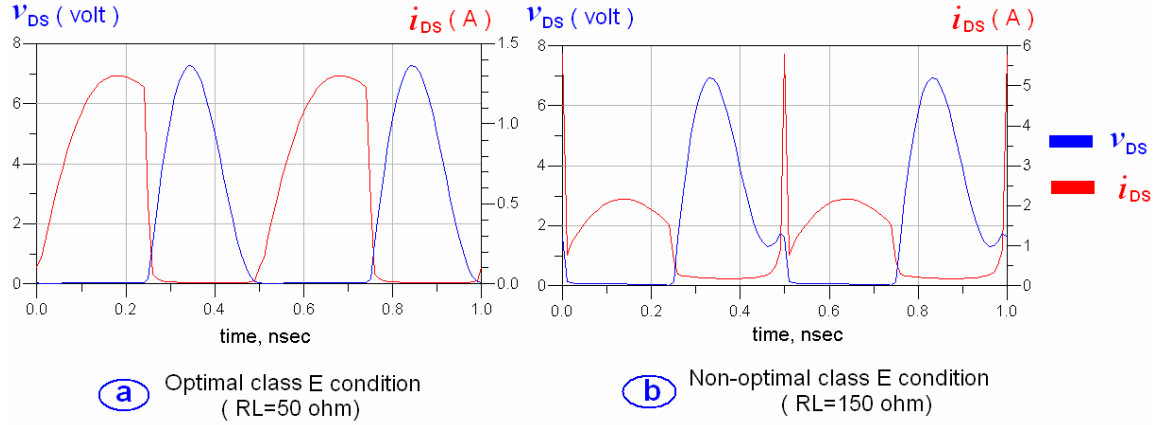


Fig. 3.13 The drain waveform of an optimal class E and a non-optimal class E condition.

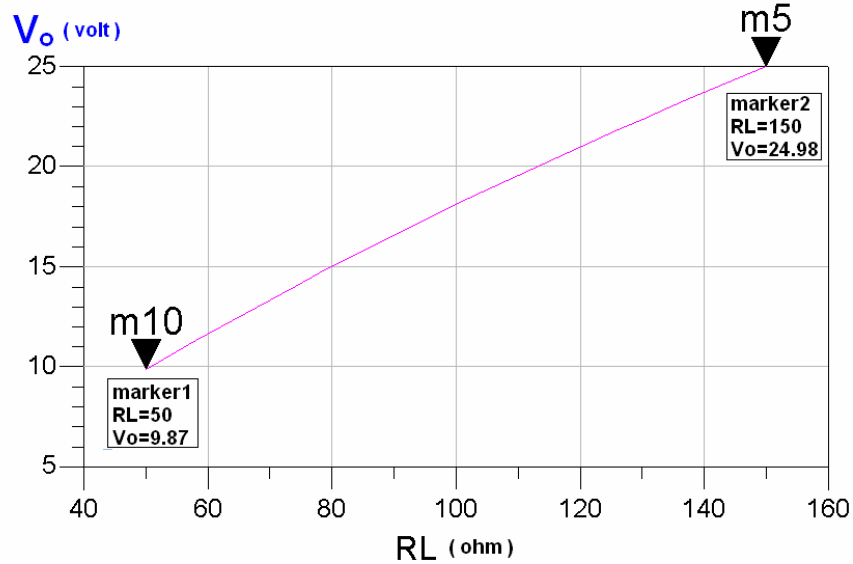


Fig. 3.14 Simulation result of an ideal class E PA with the change of  $RL$ . block shown in Fig. 3.12 is used. Using (3.13), (3.14) and (3.16) predicts the voltage summation is 24.98 V rather than the expected value 29.61 V.

### Power summation

Although the voltage summation structure is very promising, only the ideal class F PA block can be used in it, which impedes the practical application for the power combining. Therefore, the power summation could be the choice in this work rather than the voltage

summation. Instead of adding the output voltage from each PA block, the power outputs are added, which is illustrated by Fig. 3.15a and Fig. 3.15b. Compared with the voltage summation structure shown in Fig. 3.15c and 3.15d, the difference lays in that the characteristic impedance of each transmission line is redesigned so that each PA block still sees the same optimal resistance as in single stage. Therefore, each PA block delivers the same output power when they are in the power summation structure and the power output delivered to the load  $RL$  is  $P_T = P_1 + P_2 + \dots + P_n$  shown in Fig. 3.15b.

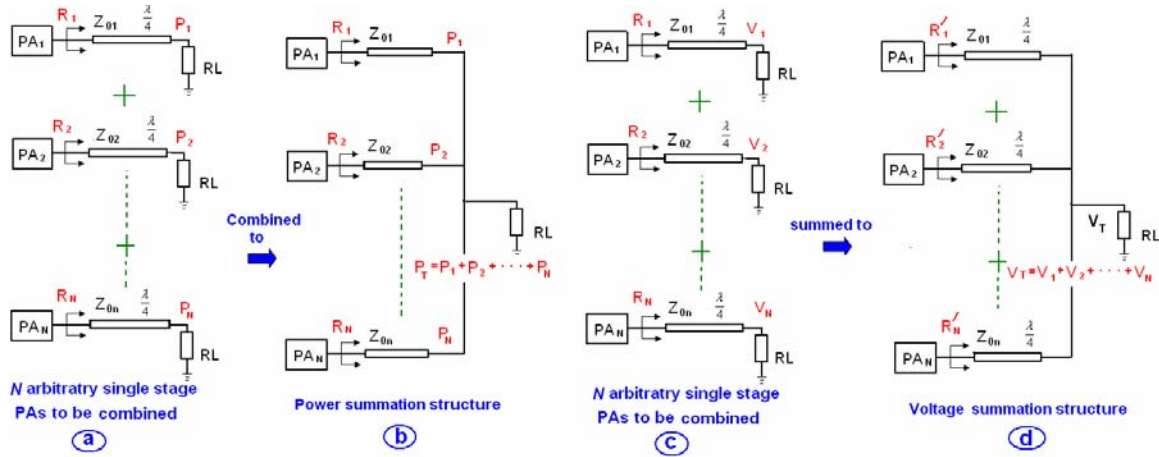


Fig. 3.15 Comparisons of the power summation and voltage summation structure.

In summary Table 3.3 shows the advantages and disadvantages of the power summation structure and the voltage summation. Since the objective of this work is power combination the idea of power summation meets the goal more directly. In the next section the general model of power summation is proposed and analyzed.

Table 3.3 The advantages and disadvantages of the power summation structure and the voltage summation.

	Advantages	Disadvantages
<b>Power summation structure</b>	<ol style="list-style-type: none"> <li>1. No need to hold (3.10) for each PA block. each PA block remains the original optimal condition in the combining structure.</li> <li>2. Theoretically applicable for different PA modes.</li> </ol>	<ol style="list-style-type: none"> <li>1. Bad voltage summation capability.</li> </ol>

	3. Meet the goal of power combining directly.	
<b>Voltage summation structure</b>	1. Good voltage summation capability.	1. Each PA block has to hold (3.10). 2. (3.10) limits the application only to ideal class F PA mode. 3. Meet the goal of power combining indirectly.

### 3.3 Theoretical Analysis of N-device Unbalanced Combining Technique

#### 3.3.1 Introduction

##### Symbol Convention

The symbol convention is clarified before the analysis. In chapter 2.2 it has been discussed that the PA contains an input matching, an active device, a harmonic control block and an impedance conversion block. However, for simplicity in the following analysis the first three sub-blocks of the PA together, before the impedance conversion

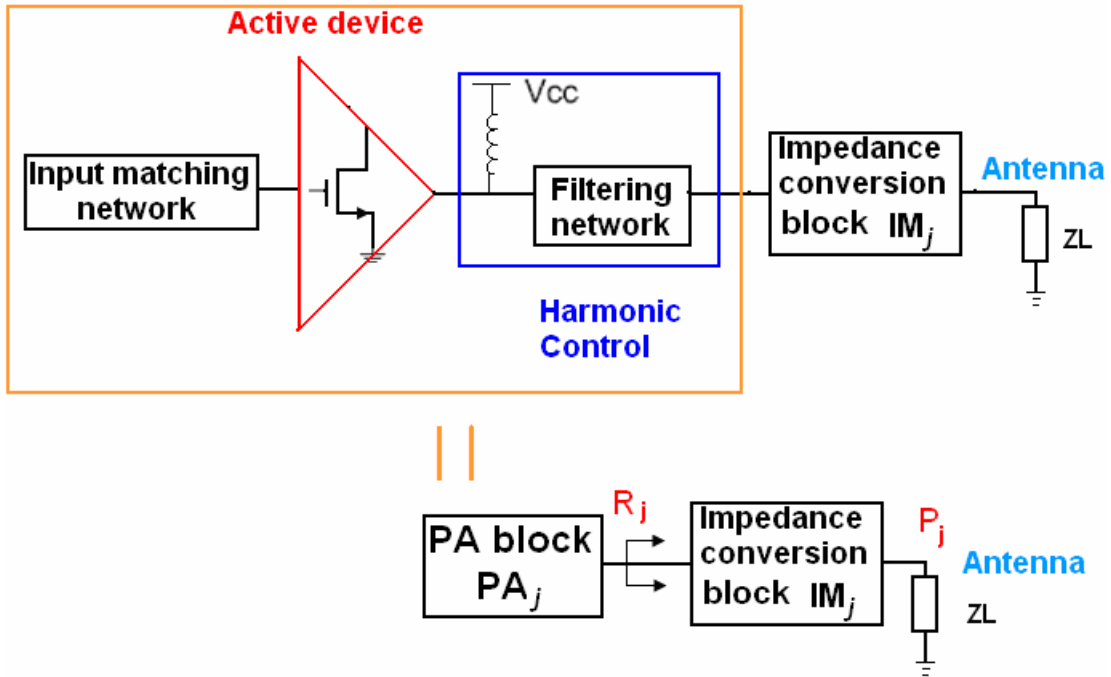


Fig. 3.16 Illustration of symbols for the PA.

block, will be referred as PA block  $PA_j$ . Fig. 3.16 illustrates the symbol convention, where  $IM_j$  represents the impedance conversion block,  $PA_j$  denotes the PA block,  $P_j$  is the output power of this  $PA_j$  when the load is  $R_j$  and  $R_j$  is the optimal resistive load the  $PA_j$  needs to see ( $j \in [1, 2, \dots, N]$ ,  $N$  is an arbitrary positive integer).

##### Basics of the new power combining technique

As discussed in section 2.3.1 the designing method of the combining structure in this work is divided into three steps:



1. Design the individual PA blocks separately.
2. Design the combining network according to the first step.
3. Connect the PA blocks designed in step 1 with the combining network designed in step 2.

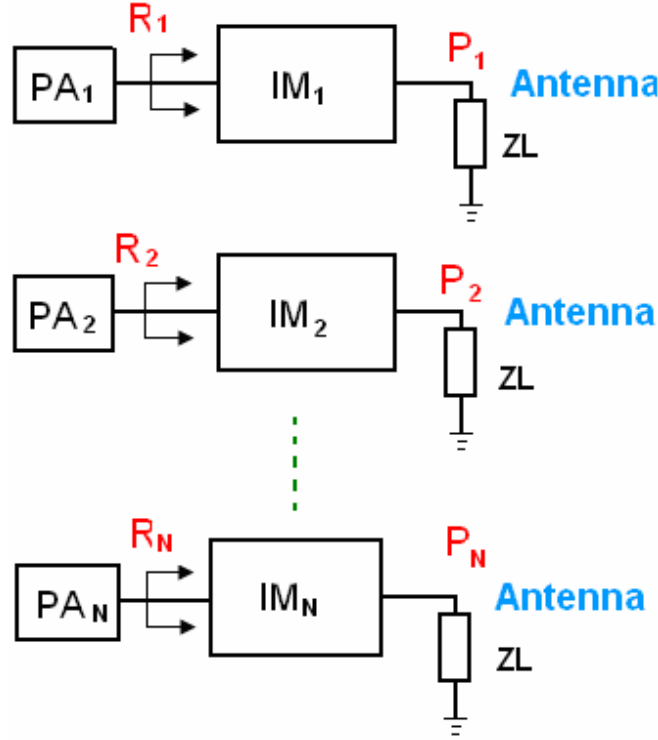


Fig. 3.17  $N$  arbitrary single stage PAs to be combined.

The first step is just the same as the normal single PA design and any previously related experience and knowledge can be used. The design procedure in the second step is the focus of this work and will be given in this section. Therefore, in this analysis it's assumed that  $N$  arbitrary single stage PAs have been designed in advance and the task is to sum their power output rather than voltage output. Shown in Fig. 3.17 are the arbitrary single stage PAs. For each single-stage PA to-be-combined only the output power  $P_j$  and the according optimal load  $R_j$  is of interest for the analysis of the combining structure. The other designed values such as PA classes, drain efficiency, power-added efficiency (PAE), voltage supply and etc. are not required in the following analysis. In other words, those to-be-combined single stage PAs can be arbitrary classes and have different power performance. Therefore, the proposed combining technique for this general case is named *N-device unbalanced power combining technique*.

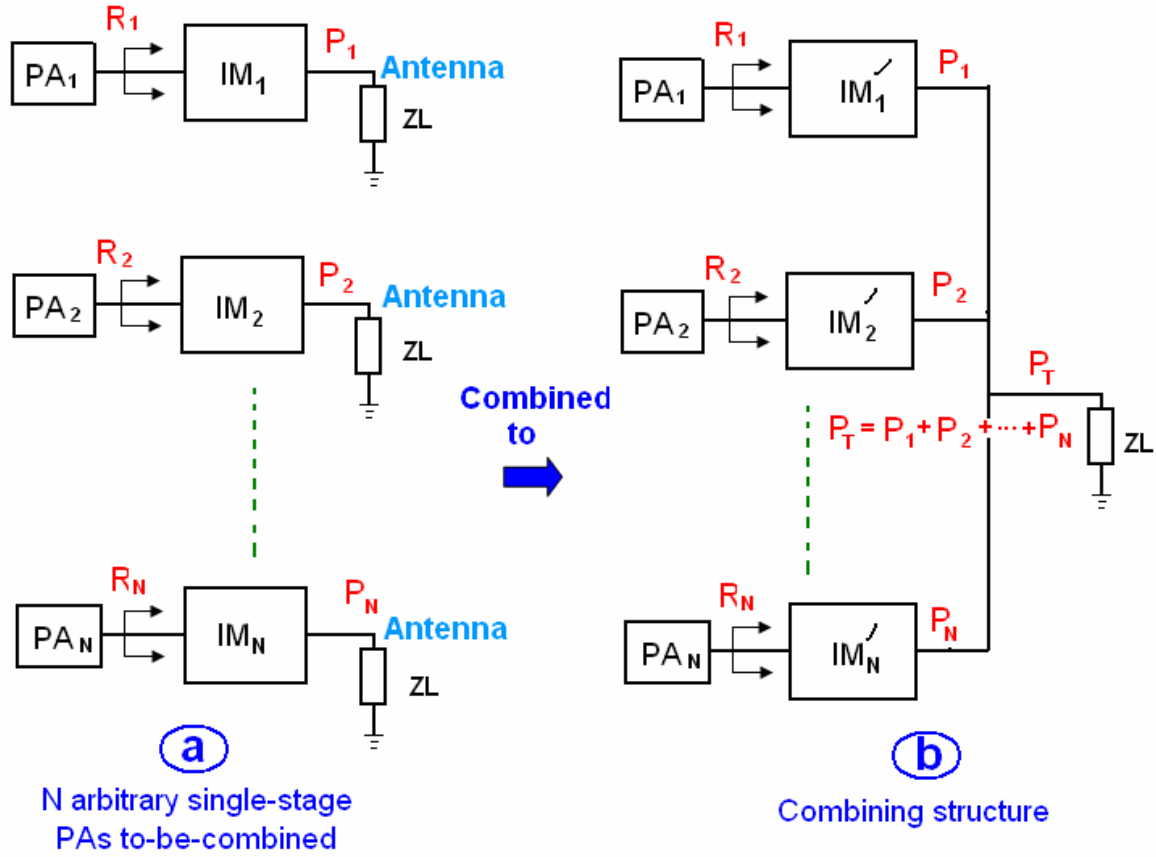


Fig. 3.18  $N$ -device unbalanced power combining structure

Fig. 3.18b shows the schematic of the unbalanced combining structure which combines the power output of  $N$  arbitrary single stage PAs shown in Fig. 3.18a. This combining structure can achieve the following goals:

1. Each PA block is isolated from each other meaning that the load each PA sees is still  $R_j$  thus the combining network doesn't affect the performance of PA blocks. In other words, each single PA block delivers the same power after being combined.
2. All the power produced from each single stage PA has been combined to one load  $ZL$ ,

$$P_T = P_1 + P_2 + \dots + P_N \quad (3.17)$$

To approach these two goals the impedance conversion blocks need changing to build the combining network. This change is represented in Fig. 3.18 by the symbol changing from  $IM_j$  to  $IM'_j$  ( $j \in [1, 2, \dots, N]$ ,  $N$  is an arbitrary positive integer).

In the next section the analysis model will be presented for the combining structure.

### 3.3.2 Analysis Model

The combining structure in Fig. 3.18b is complex and not easy to analyze. Fig. 3.19 shows the process how the combining structure shown in Fig. 3.19a is equivalent to its analysis model in Fig. 3.19c. The process steps are listed as follows:

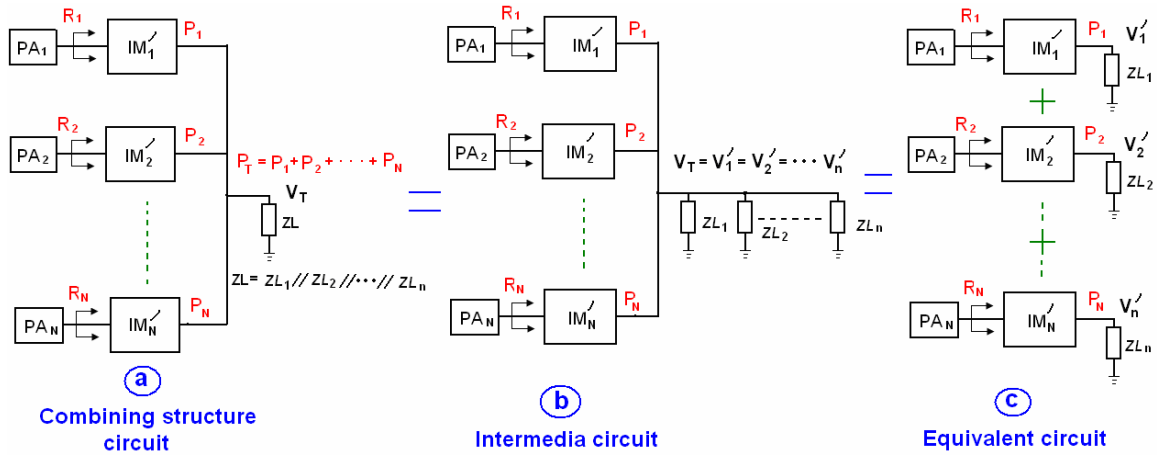


Fig. 3.19 Analysis model for the power combining structure.

1. The load  $ZL$  in Fig. 3.19a is divided into  $N$  loads in parallel, namely  $ZL_1 - ZL_n$ ,

$$ZL = ZL_1 // ZL_2 // \dots // ZL_n \quad (3.18)$$

, which turns Fig. 3.19a into Fig. 3.19b.

2. Fig. 3.19b is split into  $N$  single stage PAs shown in Fig. 3.19c where the output voltage is equal.

$$V'_1 = V'_2 = \dots = V'_n = V_T \quad (3.19)$$

Thus the combining structure circuit in Fig. 3.19a is equivalent to its analysis model in Fig. 3.19c.

In Fig. 3.20 the single-stage PAs to be combined and the analysis model of the combining structure are put together for better illustration. At this stage the analysis interest is about designing the impedance block  $IM'_j$  in Fig. 3.20b so that each PA block still see the expected load  $R_j$  and the expected power output  $P_j$  will be delivered.

As shown in Fig. 3.21 the general procedure to design the combining structure is:

1. **Pick PA blocks** as shown in Fig. 3.21b. Each PA block from the to-be-combined single stage power amplifiers in Fig. 3.21a is used without any change in the combining structure.

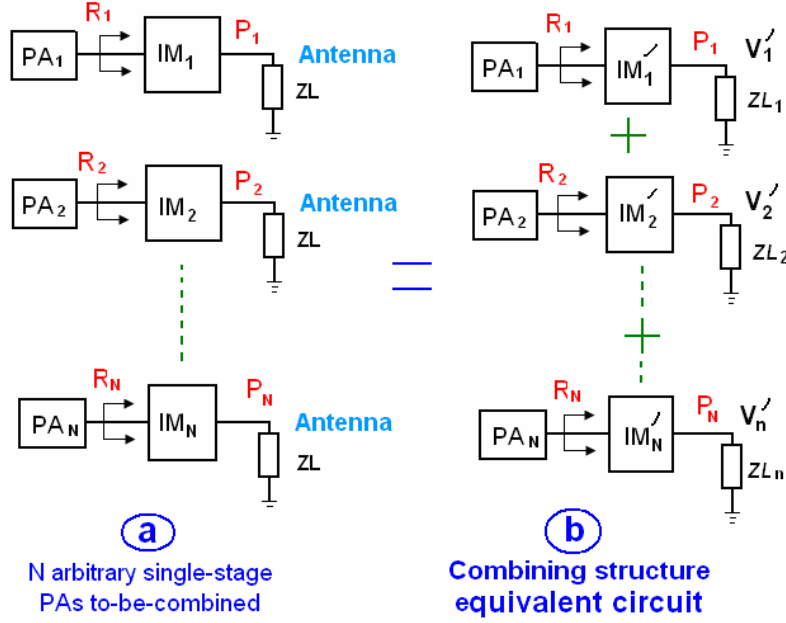


Fig. 3.20 Analysis model of the combining structure compared with the single-stage to-be-combined PAs

**2. Design new impedance conversion blocks and build the equivalent circuit for the combining structure.**<sup>4</sup> Design new impedance conversion block  $IM_j'$  shown in Fig. 3.21c then connect it to the PA block  $PA_j$  and load  $ZL_j$  to build the equivalent circuit shown in Fig. 3.21d for the combining structure ( $j \in [1, 2, \dots, N]$ ,  $N$  is an arbitrary positive integer). The following objectives should be achieved in the equivalent circuit:

a.  $V_1' = V_2' = \dots V_n'$  (3.20)

b.  $ZL_1 // ZL_2 // \dots ZL_n = ZL$

(3.21)

c. Each PA block in Fig. 3.21d still delivers the same power  $P_j$  as it does before being combined in Fig. 3.21a, which means the impedance conversion block  $IM_j'$  transforms  $ZL_j$  to  $R_j$ .

<sup>4</sup> The design equations for  $IM_j'$  and  $ZL_j$  is dependent on the type of the impedance conversion block. Closed-form equations will be derived in the next section for the quarter-wavelength transmission line impedance conversion block.

3. Check whether the above stated three conditions in step 2 are satisfied, as shown in Fig. 3.21e. (3.20) should be satisfied both in phase and amplitude.
4. Build the combining structure. Use the new impedance conversion block  $IM_j'$  designed in step 2 to connect the PA blocks mentioned in step 1 to the load  $ZL$ . Then the combining structure in Fig. 3.21b is completed.

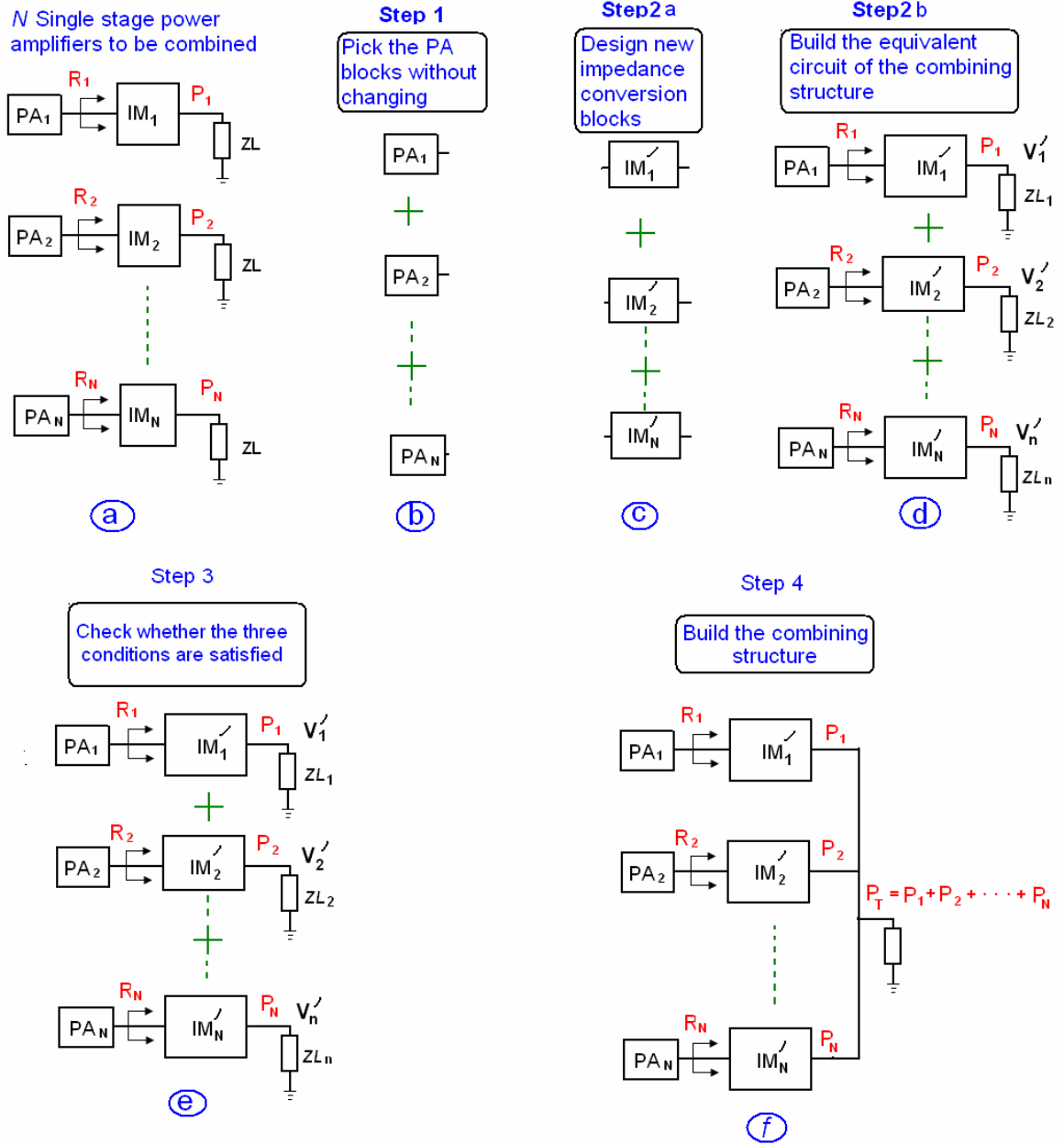


Fig. 3.21 Illustration of the design steps of the  $N$ -device unbalanced combining structure.

So far the general procedure to design the combining structure has been presented. In the next section the quarter-wavelength transmission line will be used as the impedance conversion block to build the combining network. Closed-form design equations will be derived.

### 3.3.3 Design equations for the quarter-wavelength combining network

The previous section, illustrated by Fig. 3.19, Fig. 3.20 and Fig. 3.21 actually shows the basic analysis model of the proposed power combining technique. Nevertheless, closed-form design equations can only be derived after the impedance conversion technique is chosen. There are a few kinds of impedance conversion block [2.5] and the quarter-wavelength transmission line is used in this work since it's easy to design for the single frequency application.

#### Basics of the quarter-wavelength transmission line

At first in Fig. 3.22 the basic of the quarter-wavelength transmission line impedance conversion block is introduced. A quarter-wavelength transmission line with characteristic impedance of  $Z_0$  converts load  $Z_L$  into impedance  $Z_{in}$  given by [2.17]

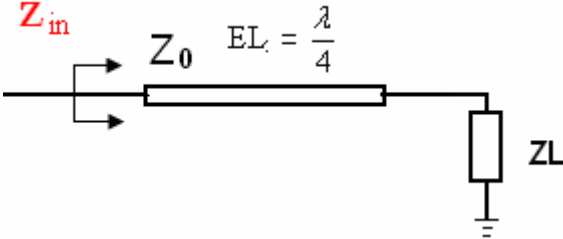
$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (3.22)$$


Fig. 3.22 Impedance transformation by quarter-wavelength transmission line

Usually the quarter-wavelength transmission line impedance conversion block is used to convert a resistive load to a resistive impedance. In the following analysis the antenna is assumed to be a resistive impedance  $RL$ .

#### Analysis model of the combining structure

Fig. 3.23 shows the  $N$  arbitrary PAs to be combined and the combining structure using the quarter-wavelength transmission line. The known value of the  $N$  arbitrary to-be-combined PAs are listed as follows:

1.  $P_j$  is the power output each single stage PA is designed to deliver.
2.  $Z_{0j}$  is the characteristic impedance of the quarter-wavelength transmission line for PA block  $PA_j$ .
3.  $R_j$  is the designed load each PA block wants to see ( $j \in [1, 2, \dots, N]$ ).

$$R_j = \frac{Z_{0j}^2}{RL} \quad (3.23)$$

The proposed combining structure and its analysis model are shown in Fig. 3.23b and Fig. 3.23c respectively. They are used to derive the formula. To combine the power output from each single stage PA shown in Fig. 3.23a the quarter-wavelength transmission lines in the combining structure is redesigned to fulfill the following goals shown in Fig. 3.23c:

1. Convert the new load  $RL_j$  to the same optimal load  $R_j$  so that the PA block  $PA_j$  still delivers power output  $P_j$ .
2. Equation (3.18) and (3.19) are satisfied, which makes sure the analysis model in Fig. 3.23c is equivalent to the combining structure in Fig. 3.23b.

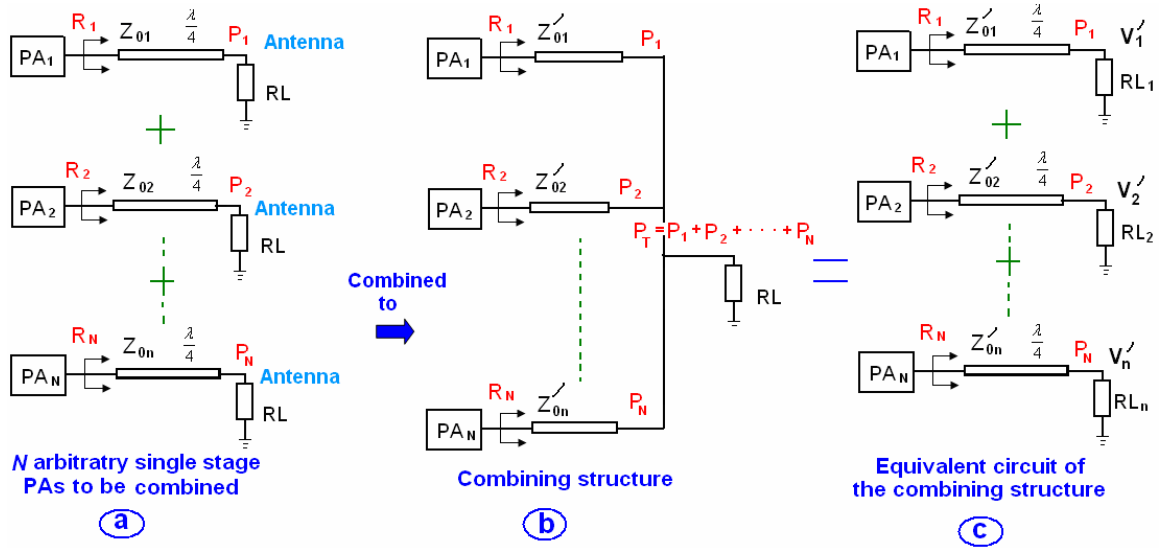


Fig. 3.23 Illustration for the analysis of quarter-wavelength transmission line combining structure

### Equations derivation

For an arbitrary PA block  $PA_j$  in Fig. 3.23c at the load the power output is

$$P_j = \frac{V_j'^2}{2RL_j} \quad (3.24)$$

If (3.19) is satisfied, (3.24) reduces to

$$P_j = \frac{V_T^2}{2RL_j} \quad (3.25)$$

In the combining structure shown in Fig. 3.23b

$$P_T = P_1 + P_2 + \dots + P_n = \frac{V_T^2}{2 \times RL} \quad (3.26)$$

Combining (3.25) and (3.26)

$$\Rightarrow RL_j = \frac{V_T^2}{2 \times P_j} = \frac{RL \times P_T}{P_j} \quad (3.27)$$

$$\Rightarrow RL_1 // RL_2 // \dots // RL_n = \frac{1}{\sum_{j=1}^n \frac{1}{RL_n}} = \frac{RL}{\sum_{j=1}^n \frac{P_j}{P_T}} = RL \quad (3.28)$$

, which verifies that the single-stage PAs of the analysis model in Fig. 3.23c can be connected at the output nodes and the resulting structure is equivalent to the combining structure circuit in Fig. 3.23b. Actually at this stage it is assumed that the voltages  $V_j'$  at the output node in Fig. 3.23c are in phase between each other. The equivalent circuit will not be equal to the combining structure if voltages  $V_j'$  have different phase though the same amplitude.

For any PA block  $PA_j$  in Fig. 3.23c the impedance conversion block gives

$$Z_{0j}' = R_j \times RL_j \quad (3.29)$$

Combining (3.22), (3.26) and (3.29) yields

$$\Rightarrow Z_{0j}' = Z_{0j} \times \sqrt{\frac{P_T}{P_j}} = Z_{0j} \times \sqrt{\frac{\sum_{j=1}^n P_j}{P_j}} \quad (3.30)$$

## Discussions

As can be seen above the phase difference information between  $V_j'$  shown in Fig. 3.23b is not involved in the design equations. The design equations are based on the assumption



that there is no phase difference among  $V_j'$ . Therefore, following the design equations can only guarantee the amplitude of  $V_j'$  is equal but not the phase. Additional care is needed to check whether there is phase difference between each voltage  $V_j'$  when the combining structure is designed.

The above-stated equation derivation is valid for the PAs at one single frequency. However, in reality the output of the PA always has harmonic components, which can be measured by the parameter THD (Total harmonic distortion). High THD will degrade the performance of the combining structure from the design expectation more or less. This issue will be mentioned in one of the design example in the next section.

The special case of this combining technique is that when all the PA blocks to be combined are identical. This is named as  $N$ -device balanced power combining structure. In this case the design equations (3.27) and (3.30) can be simplified as

$$RL_j = RL \times N \quad (3.31)$$

$$Z_{0j}' = Z_{0j} \times \sqrt{N} \quad (3.32)$$

, where  $N$  is the number of identical PAs to be combined.

Since each PA block and the impedance conversion block are the same each voltage  $V_j'$  has the same phase. (3.31) and (3.32) are adequate for the design of  $N$ -device balanced power combining structure.

### Design procedure

Finally (3.27) and (3.30) can be used to design the quarter-wavelength transmission lines in the combining structure. After some modification from Fig. 3.21 the procedure to design the quarter-wavelength transmission line combining structure for  $N$  arbitrary single stage PAs is listed:

1. **Pick PA blocks.** Each PA block from the to-be-combined single-stage power amplifiers in Fig. 3.24a is used in the combining structure without any change shown in Fig. 3.24b.
2. **Design new quarter-wavelength transmission lines.** Design the characteristic impedance  $Z_{0j}'$  of each new quarter-wavelength transmission line based on equation (3.30) shown in Fig. 3.24c. In equation (3.30)  $P_T$  is the sum of the

power output from each single-stage to-be-combined power amplifier in Fig. 3.24a.  $Z_{0j}$  is the characteristic impedance of the quarter-wavelength transmission line for the single-stage to-be-combined power amplifier  $PA_j$ .  $P_j$  is the power output of  $PA_j$ .

3. **Build the equivalent circuit and check whether (3.20) is satisfied.** Connect the quarter-wavelength transmission lines designed in step 2 to the PA blocks mentioned in step 1 and the load  $RL_j$  respectively as shown in Fig. 3.24d. The load  $RL_j$  is designed by equation (3.27).
4. **Build the combining structure.** Use the new quarter-wavelength transmission line designed in step 2 to connect the PA blocks mentioned in step 1 to the load  $RL$ . Then the combining structure in Fig. 3.23b is completed in Fig. 3.24e.

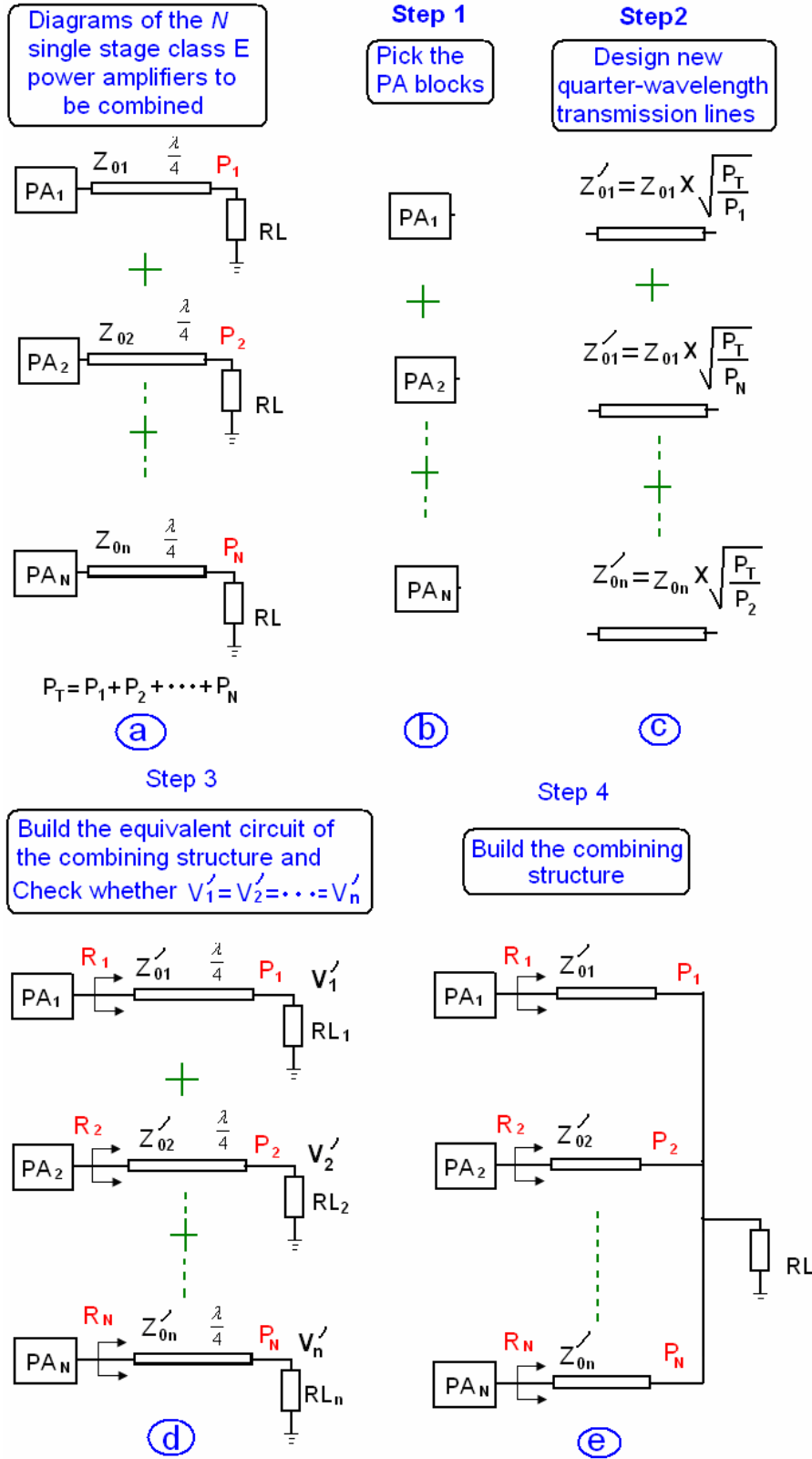


Fig. 3.24 Illustration of the design steps of the  $N$ -device unbalanced quarter-wavelength transmission line combining structure.

### 3.4 Design examples

#### 3.4.1 Introduction

To illustrate the  $N$ -device unbalanced power combining technique three design examples will be given in this section. The quarter-wavelength transmission lines are used for the combining network.

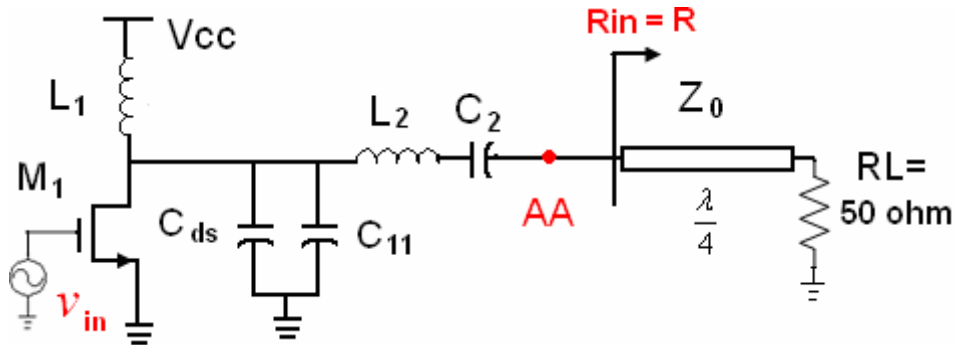


Fig. 3.25 The schematic of the pre-designed single stage class E PA3.3 Simulation verification

At first a two-device balanced combining structure and a four-device unbalanced combining structure are designed and simulated in Cadence Spectre. As mentioned in Chapter 2, the Class E power amplifier is chosen as the PA block due to its high drain efficiency. Fig. 3.25 shows the schematic of the single stage class E PA circuit used in the first two examples. The ideal transmission line model “Tline” from “analogLib” in Spectre is used<sup>5</sup>. Since an RFIC PA normally works above 1 GHz, the working frequency is chosen to be 2 GHz. The input signal source of each PA block is a 2 GHz sinusoid voltage source which has an amplitude of 1 volt and a DC bias of 1 volt. The design equation for the single stage PAs to be combined is based on [1.4]. The transistor in the PA block is from the Philips CMOS18 process.

Secondly, to show the general application of the power combining technique a two-device balanced combining structure using class C PA block is designed and simulated in ADS.

<sup>5</sup> This is the only ideal transmission line model in Spectre though it is not supported by Periodic Steady State (PSS) analysis. The transient analysis has to be used in replacement of PSS, which needs more simulation time.

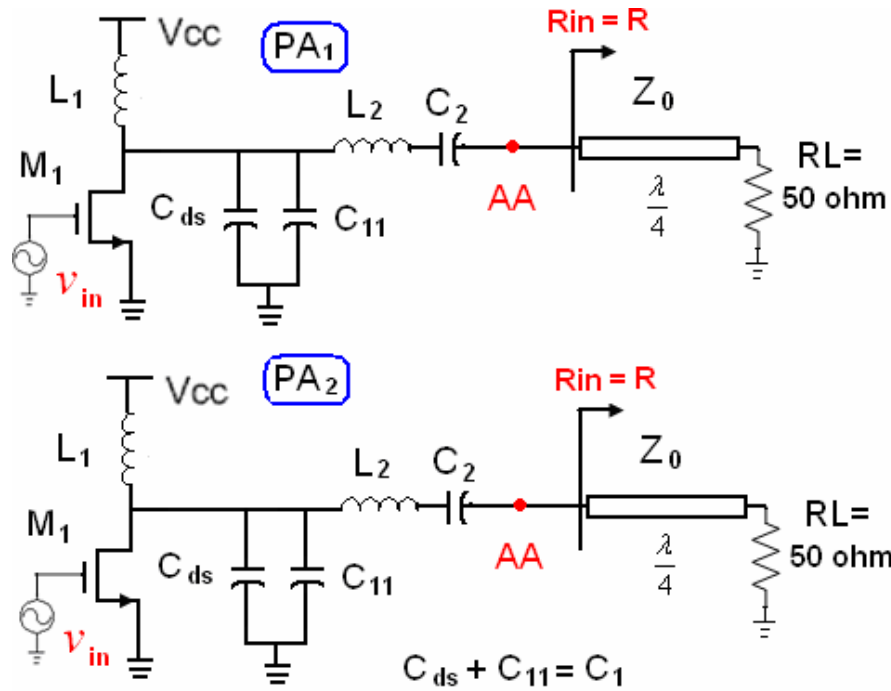


Fig. 3.26 Schematics of the two identical single stage class E PAs to be combined

### 3.4.2 Simulation results of a two-device balanced combining structure

In this section it's shown that the combining structure achieves the power summation from two identical single stage class E power amplifiers. To show the universality of this technique two identical single stage class E PAs with randomly chosen performance are designed. The design values of these two arbitrary single stage PAs is listed in Table 3.4 and the parameter names in Table 3.4 are referred to Fig. 3.26.

Table 3.4 Design value of two single stage class E PAs to be combined

PA Block	Vcc (V)	f (GHz)	W (um)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)	L <sub>1</sub> (nH)	L <sub>2</sub> (nH)	Z <sub>0</sub> (ohm)	R (ohm)	Pout (mW)
PA <sub>1</sub>	0.6	2	5000	4.99	0.729	0.636	8.69	23.4	10.95	44.43
PA <sub>2</sub>										

Following the design procedure summarized in section 3.3.3 the combining structure is designed and shown in Fig. 3.27.<sup>6</sup> Table 3.5 lists the design value of the quarter-wavelength transmission lines using (3.32).

<sup>6</sup> As discussed in the previous section there is no need to build the equivalent circuit and check the voltage phase when designing the balanced power combining structure.

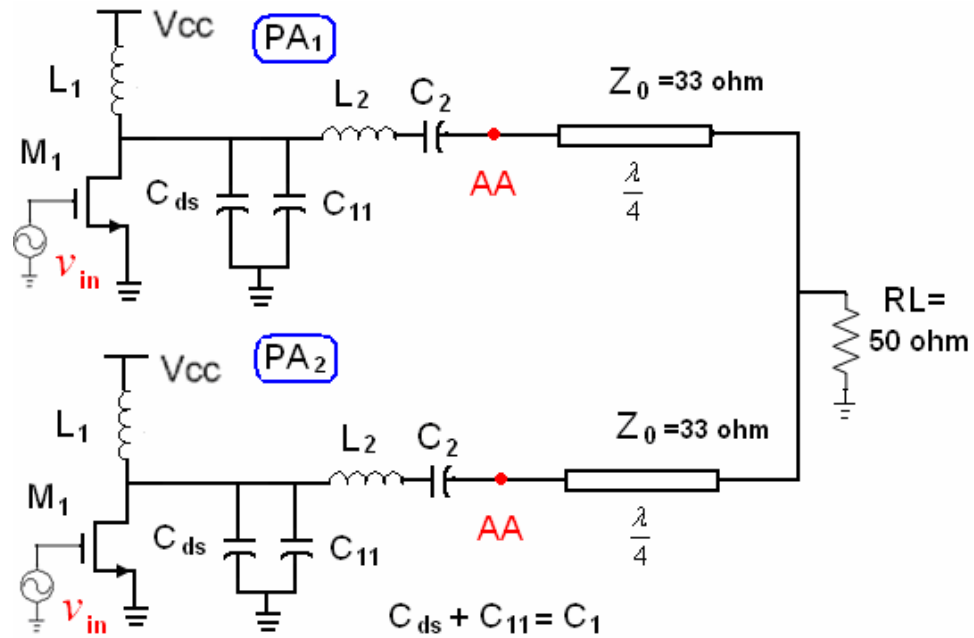


Fig. 3.27 Schematics of the two-device balanced power combining structure

Table 3.5 The old and newly designed value of the quarter-wavelength transmission lines

	PA <sub>1</sub>	PA <sub>2</sub>
$Z_0$ (ohm)	23.4	
$Z_0'$ (ohm)	$Z_0' = Z_0 \times \sqrt{2} \approx 33$	

The comparison of the simulation results between the single stage PAs before and after combining are listed in Table 3.6. It shows that two identical single stage class E PAs keep the same power performance in the combining structure and the power output delivered by them is combined.

Table 3.6 Performance Comparison

	Before Combining		After Combining	
PA Block	PA1	PA2	PA1	PA2
DC Power Input (mW)	49.57	49.57	49.57	49.57

Power Output (mW)	44.43	44.43	44.43	44.43
Total Power Output (mW)	88.86		88.86	

### 3.4.3 Simulation results of four-device unbalanced combining structure

In this section it's shown that the combining structure achieves the power combination from four arbitrary single stage class E power amplifiers. To show the universality of this theory four single stage class E PAs with randomly chosen performance are designed shown in Fig. 3.28. However, the design should make sure that the voltage phase at node A1-A4 is the same. The design values of these four arbitrary PAs are listed in Tables 3.7 and the parameter names in Table 3.7 are referred to Fig. 3.28.

Table 3.7 Design value of four single stage class E PAs to be combined

PA Block	Vcc (V)	f (GHz)	W (Kum)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)	L <sub>1</sub> (nH)	L <sub>2</sub> (nH)	Z <sub>0</sub> (ohm)	R (ohm)	Pout (mW)
PA <sub>1</sub>	0.6	2	1	2.88	0.421	1.1	15.04	30.74	18.9	21.34
PA <sub>2</sub>	0.6		10	28.84	4.21	0.11	1.5	9.72	1.89	212.9
PA <sub>3</sub>	0.9		3	5.547	0.81	0.57	3.35	22.17	9.83	101.4
PA <sub>4</sub>	0.9		7	12.94	1.889	0.245	7.82	14.51	4.21	236.7

Since the transmission line is frequency dependent it converts the load  $RL$  to  $R_j$  for the PA blocks at fundamental frequency  $f_0$  but not at the harmonic frequencies, while ideally the PA blocks need to see  $R_j$  both at fundamental and harmonics. This problem actually is shared by all the single-frequency impedance conversion technique. Therefore, the simulation shows THD of the output voltage is around 7%, which mostly is caused by the second harmonic  $2f_0$ . Not only does this problem bring high THD to the output signal, but it also has a negative effect on the combining structure design as mentioned section 3.3.3.





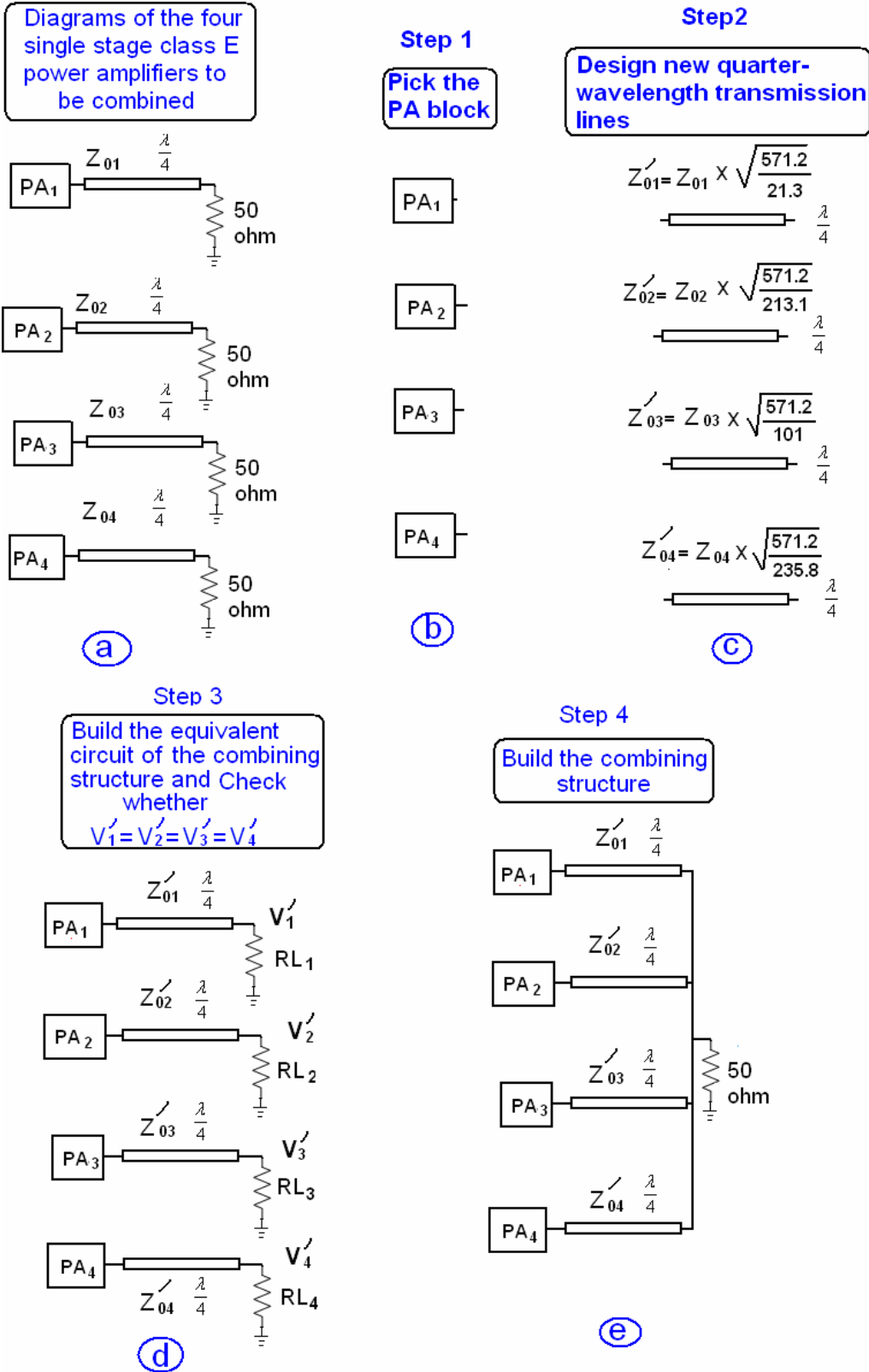


Fig. 3.29 Illustration of the design steps of the four-device unbalanced combining structure

The combining structure is designed as follows

- 1. Design new quarter-wavelength transmission lines.** Design the characteristic impedance  $Z_{0j}'$  of the new quarter-wavelength transmission lines based on equation (3.30) for the combining structure shown in Fig. 3.29c. The summation of the power output from each single-stage PA to be combined in Fig. 3.29a is given by

$$P_T = \sum_{j=1}^4 P_j \approx 571.2 \text{ mW} \quad (3.33)$$

Thus the new quarter-wavelength transmission lines are designed based on (3.30) and the values are listed in Table 3.8.

Table 3.8 The old and newly designed value of the quarter-wavelength transmission lines

	$PA_1$	$PA_2$	$PA_3$	$PA_4$
$Z_0$ (ohm)	49.57	15.67	28.98	18.72
$Z_0'$ (ohm)	$Z_{01} \times \sqrt{\frac{P_T}{P_1}}$ $= Z_{01} \times \sqrt{\frac{571.2}{21.3}}$ $\approx 159.2$	$Z_{02} \times \sqrt{\frac{P_T}{P_2}}$ $= Z_{02} \times \sqrt{\frac{571.2}{213.1}}$ $\approx 15.9$	$Z_{03} \times \sqrt{\frac{P_T}{P_3}}$ $= Z_{03} \times \sqrt{\frac{571.2}{101}}$ $\approx 125.4$	$Z_{04} \times \sqrt{\frac{P_T}{P_4}} =$ $Z_{04} \times \sqrt{\frac{571.2}{235.8}}$ $\approx 22.58$

- 2. Build the equivalent circuit of the combining structure and check whether (3.20) is satisfied.** Based on (3.27) the loads in the equivalent circuit are calculated and given in Table 3.9.

Table 3.9 The value of the load in the equivalent circuit.

	$PA_1$	$PA_2$	$PA_3$	$PA_4$
$RL_j$ (ohm)	$RL \times \frac{P_T}{P_1}$ $\approx 1340$	$RL \times \frac{P_T}{P_2}$ $\approx 134$	$RL \times \frac{P_T}{P_3}$ $\approx 283$	$RL \times \frac{P_T}{P_4}$ $\approx 121.1$
$RL_1 // RL_2 // RL_3 // RL_4$ (ohm)	$\approx 50$			

**4 Build the combining structure.** Use the new quarter-wavelength transmission line designed in step 2 to connect the PA blocks mentioned in step 1 to the load  $RL$ . Then the combining structure is completed shown in Fig. 3.29e and Fig. 3.30.

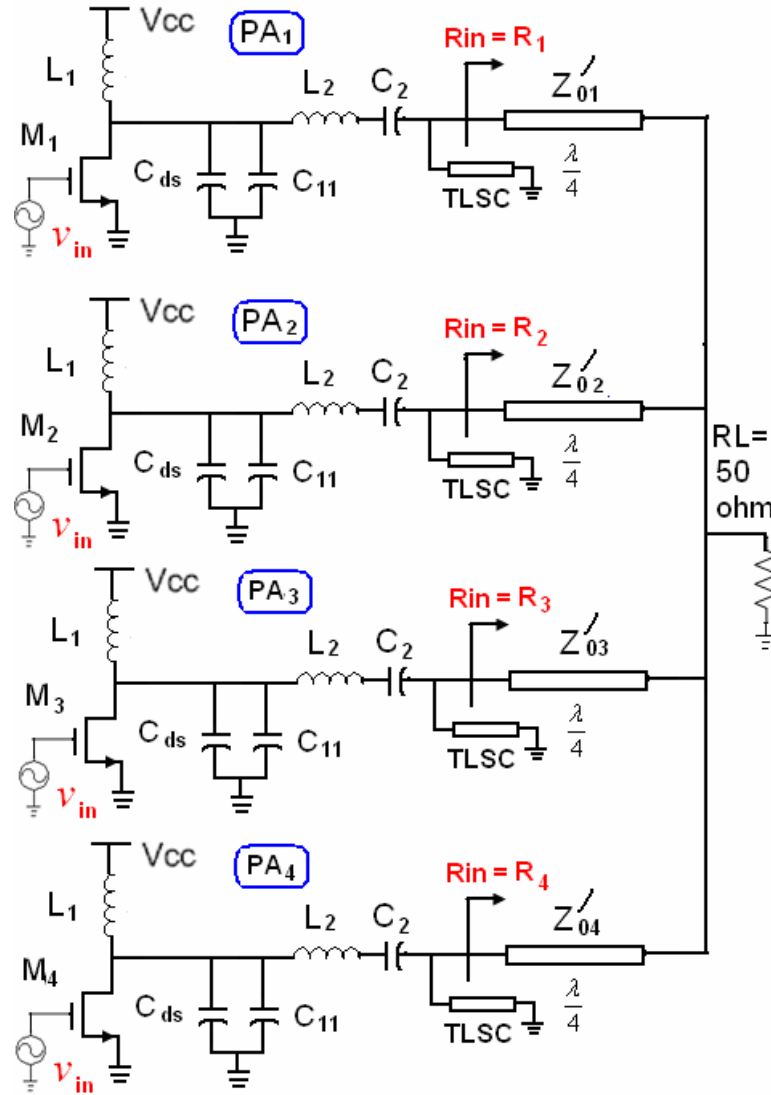


Fig. 3.30 Schematic of the 4-device unbalanced power combining structure

The comparison of the simulation results between the single stage PAs and the combining structure is listed in Table 3.10. Although there is minor difference in the power output, the results in Table 3.10 shows that four different single stage class E PAs keep the same power performance in the combining structure and the power output delivered by them is combined. The minor difference in the power output is due to:

1. The value of characteristic impedance  $Z_0$  in the simulation circuit are rounded from the design value
2. THD in the output of each PA block.

Table 3.10 Performance Comparison

	Before Combining				After Combining			
Name	PA <sub>1</sub>	PA <sub>2</sub>	PA <sub>3</sub>	PA <sub>4</sub>	PA <sub>1</sub>	PA <sub>2</sub>	PA <sub>3</sub>	PA <sub>4</sub>
DC Power Input (mW)	25.6	255.7	116	269.7	25.6	255.9	115.7	269.3
Power Output (mW)	21.3	213.1	101	235.8	20.8	218	100.1	230.1
Total Power Output (mW)	571.2				570.7			

### 3.4.4 Simulation results of two-device class C balanced combining structure

To show the general application of the power combining technique a two-device balanced combining structure using the class C PA block is designed and simulated in ADS at 2 GHz. The design procedure of this example is the same as the first example in

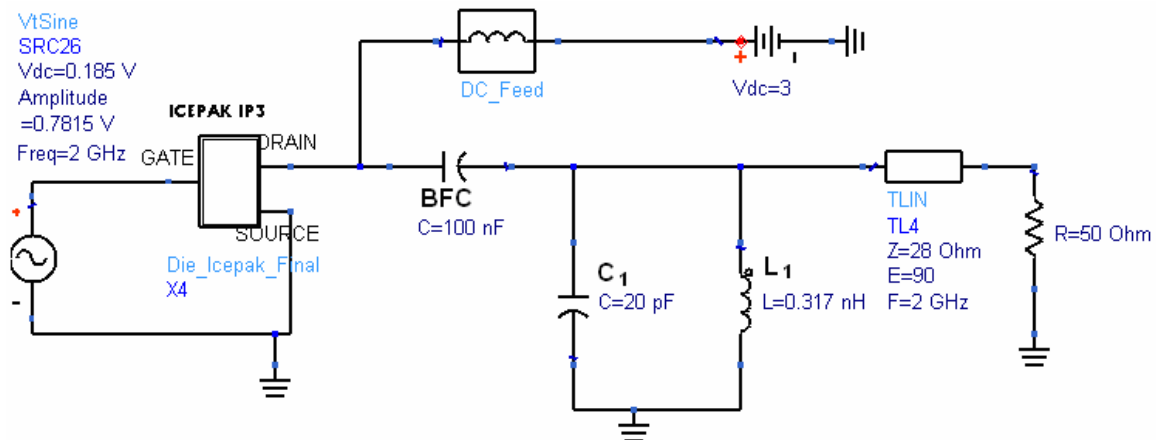


Fig. 3.31 Schematics of the single stage class C PA to be combined.

section 3.4.2 except that the PA block is class C mode. Fig. 3.31 shows the schematic of the class C PA block, where the Agilent ATF501P8 MESFET transistor die model<sup>7</sup> is used;  $C_1$  and  $L_1$  is the harmonic filter tank; the component “DC\_FEED” is for the DC current feeding and a 100 nF capacitance is for the DC block.

<sup>7</sup> In the website [5.4] of Avago Technologies the ADS model can be downloaded

The gate DC bias is 0.185 V and is below the threshold voltage (0.3 V) of the transistor, which makes the PA in class C mode. The simulation drain waveform of the single stage class C PA is shown in Fig. 3.32. Due to the reason mentioned in section 2.2.2 such as non-constant  $G_m$  and mixed-mode operation the drain current is not sinusoid-like pulse as expected in the ideal class C PA.

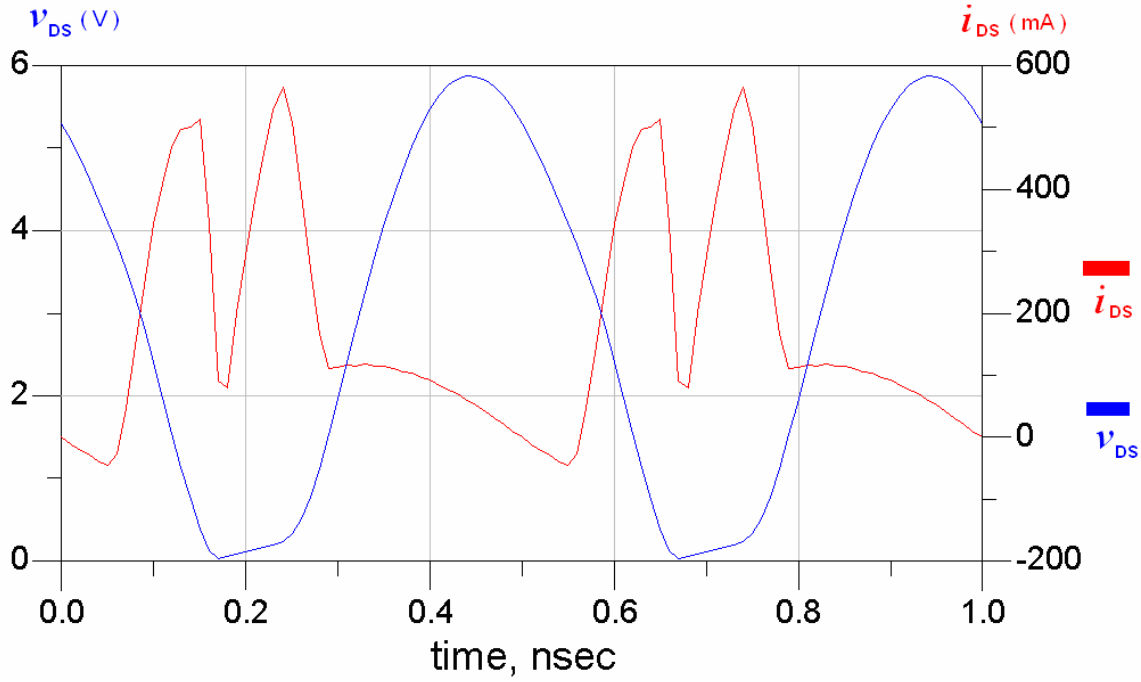


Fig. 3.32 The drain waveform of the class C PA shown in Fig. 3.31.

The design procedure of the two-device class C balanced combining structure is the same as in section 3.4.2 and thus there is no need to repeat the detail. The simulation circuit of the two-device class C balanced combining structure is shown in Fig. 3.33. Table 3.11 lists the characteristic impedance of the parallel quarter-wavelength transmission lines before and after the power summation.

Table 3.11 The old and newly designed value of the quarter-wavelength transmission lines

	PA <sub>1</sub>	PA <sub>2</sub>
$Z_0$ (ohm)	28	
$Z_0'$ (ohm)	$Z_0' = Z_0 \times \sqrt{2} \approx 39.6$	

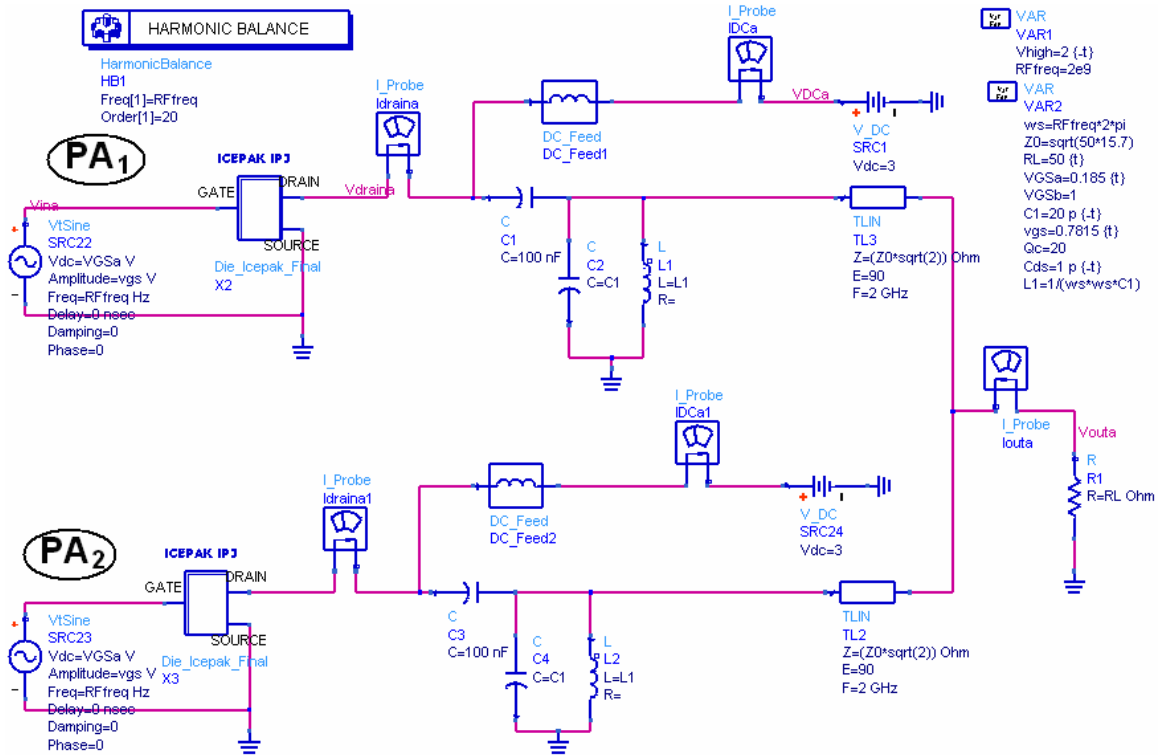


Fig. 3.33 Schematics of the two-device class C balanced power combining structure.

The comparison of the simulation results between the single stage PAs before and after combining is listed in Table 3.12. It shows that two identical single stage class C PAs keep the same power performance in the combining structure and the power output delivered by them is combined.

Table 3.12 Performance Comparison

PA Block	Before Combining		After Combining	
	PA <sub>1</sub>	PA <sub>2</sub>	PA <sub>1</sub>	PA <sub>2</sub>
DC Power Input (mW)	541.2	541.2	541.2	541.2
Power Output (mW)	289	289	None	
Total Power Output (mW)	578		578	

### 3.5 Discussion

#### Choice of the impedance conversion technique

After a little modification on Fig. 3.20 the issue of the impedance conversion technique choosing can be illustrated more clearly in Fig. 3.34. To simplify the analysis it's assumed that the voltages  $V_j'$  at the output nodes in Fig. 3.34b are in phase. The issue of

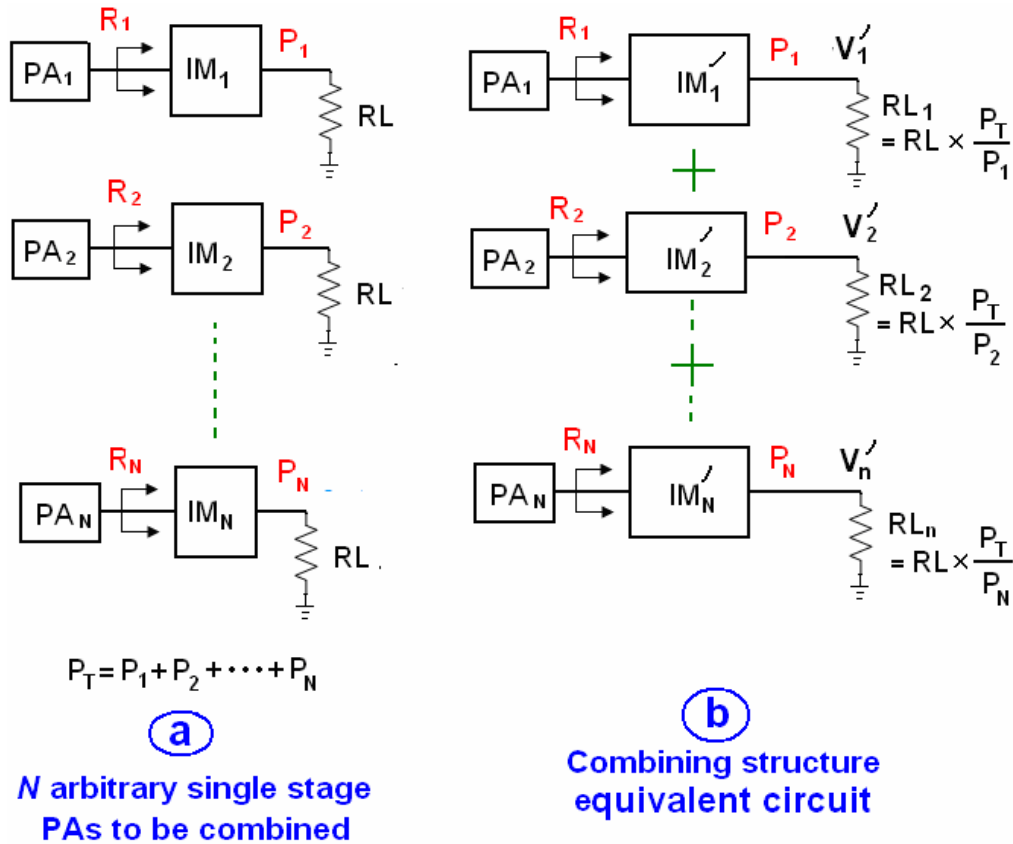


Fig. 3.34 Illustration of the difference of the impedance-transformation ratio for the impedance conversion blocks before and after combining.

the phase difference between the voltages  $V_j'$  will be discussed in the next chapter. Thus (3.27) and (3.30) can be used to design any impedance conversion block which could transfer the resistive antenna load to a resistive load. For any kind of impedance conversion technique the impedance-transformation ratio  $r$  is a figure of merit, which is defined as [2.22]

$$r = \frac{R_{Load}}{R_{in}} \quad (3.34)$$

where  $R_{in}$  is the load transformed by the impedance conversion block from  $R_{Load}$ .

The impedance-transformation ratio for each new impedance conversion block in Fig. 3.34b is given by

$$r' = \frac{RL_j}{R_j} = \frac{RL}{R_j} \times \frac{P_T}{P_j} \quad (3.35)$$

where  $RL$  is the antenna load;  $R_j$  is the optimal load the each PA block needs to see;  $P_j$  is the power delivered by the PA block  $PA_j$  and  $P_T$  is the sum of the delivered power from all the single stage PA to be combined.

The impedance-transformation ratio for the according impedance conversion block in the single stage PA to be combined  $PA_j$  shown in Fig. 3.34a is given by

$$r = \frac{RL}{R_j} \quad (3.36)$$

It's obvious that in the combining structure the impedance-transformation ratio is required  $\frac{P_T}{P_j}$  times larger than that in the according single stage power amplifier.

Practically for some type of impedance conversion techniques the higher the impedance-transformation ratio the more difficult it is to implement. For example, in the resonant LC impedance-transformation block the larger is the  $r$  the higher is the loss of this conversion block [2.22].

However, the following will show that for the quarter-wavelength transmission line it's an advantage. The characteristic impedance for any single stage to-be-combined PA and the according PA block in the equivalent circuit are given respectively by

$$Z_0^2 = RL \times R_j \quad (3.37)$$

$$Z_0'^2 = \frac{P_T}{P_j} \times RL \times R_j = \frac{P_T}{P_j} \times Z_0^2 \quad (3.38)$$

, which shows that the characteristic impedance of the transmission line in the combining

is required to be  $\sqrt{\frac{P_T}{P_j}}$  times larger. Usually the quarter-wavelength transmission line is

implemented as the microstrip line on PCB. The width of the microstrip line should stay less than either a quarter-wavelength or 20 times of the substrate thickness to satisfy its design equation assumptions [2.17]. Approximately the microstrip transmission line with



$N$  times smaller characteristic impedance is  $N$  times wider, which increases the inaccuracy of the microstrip design equation [2.17]. However, as show in (3.38) the combining structure guarantees each quarter-wavelength microstrip line has a larger characteristic impedance than that before combining, which makes the microstrip implementation much easier.

As a conclusion, the proposed power combining technique demands a higher impedance-transformation ratio. Therefore, the impedance conversion technique which suffers from a high impedance-transformation ratio is not preferred in the combining structure. Yet the quarter-wavelength transmission line implemented by the microstrip benefits for this combining structure.

### **To combine or not to**

It's just been discussed that the proposed unbalanced power combining technique can bring benefits for the impedance conversion technique using quarter-wavelength microstrip line. In the last part of this discussion section the balanced power combining technique will illustrate the advantage of the high impedance-transformation ratio. The combination of the identical PA blocks is a special case of the proposed unbalanced power combining technique. As shown in Fig. 3.35a each node in these  $N$  identical PAs has the same voltage and they can be connected and equal to the circuit in Fig. 3.35b. Thus the power combining structure for the  $N$  identical PA blocks with  $W$ -wide transistor in Fig. 3.35c is equivalent to the single stage PA with  $NW$ -wide transistor in Fig. 3.35b. Using one single stage PA with  $N$  times larger transistor makes the circuit more compact. Nevertheless, as shown in Fig.3.35b the characteristic impedance of the microstrip transmission line is  $N$  times smaller than that in Fig. 3.35c, which demands approximately  $N$  times wider transmission line [2.17] and makes the implementation difficult.



board it consumes is very large, especially in lower frequency. For example, the quarter-wavelength microstrip line is around 20mm at 2GHz. Therefore, this combining technique has more advantages in higher carrier frequencies in terms of the board area. For the low frequency application the on-chip transmission line might be one option to save the board area. As shown in Fig. 3.36 cascades of  $n$  segments of  $\pi$  L-C ladder low pass networks can be used to emulate the quarter-wavelength transmission line on-chip

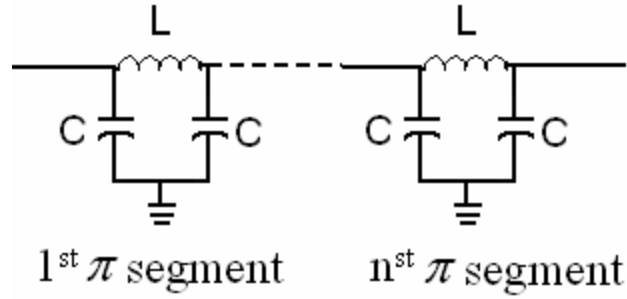


Fig. 3.36 The  $\pi$  LC ladder network to emulate the quarter-wavelength transmission line on-chip

[2.5] [2.31] [3.1], where  $L$  and  $C$  are given by [3.1]

$$L = \frac{Z_0}{4nf_0} \quad (3.39)$$

$$C = \frac{1}{4nf_0 Z_0} \quad (3.40)$$

$f_0$  is the operating frequency,  $Z_0$  is the characteristic impedance and  $n$  is the number of  $\pi$  segment. The more segments are used the closer it is to the quarter-wavelength transmission line while the on-chip loss also increases.

Recalled from Fig 3.35 is that  $N$ -device identical combining structure benefits in terms of the microstrip implementation compared with the big single PA. Following it'll check whether this advantage remains by the emulating on-chip line.

Assume that the characteristic impedance of the  $\frac{\lambda}{4}$  transmission line for the big single PA is  $\frac{Z_0}{\sqrt{N}}$ . Thus the characteristic impedance of the  $\frac{\lambda}{4}$  transmission line for each PA block in the combining structure is  $Z_0 \sqrt{N}$ . Using (3.39) and (3.40) the inductance and

capacitance of the on-chip LC ladder can be obtained and are shown in Fig. 3.37. Due to the symmetry in Fig. 3.37b, each according node is identical and can be connected together. As a result, the passive components are added and the network in Fig. 3.37b actually is equal to the LC line in Fig. 3.37a. In this sense the  $N$ -device identical combining structure is exactly the same as the single PA using  $N$  times wide transistor. Therefore, the on-chip emulating LC line doesn't provide benefit to the power combining

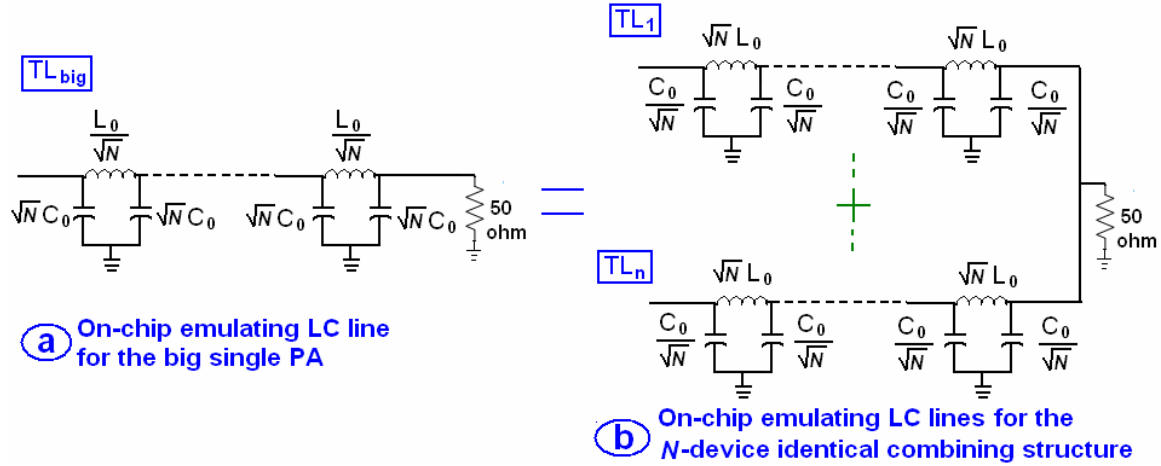


Fig. 3.37 The emulating quarter-wavelength transmission line network for big single PA and  $N$ -device identical combining structure.

structure as the real transmission line does. However, the on-chip emulating LC line may find its application for the cascode combining circuit shown in Fig. 3.38. Since the two power-output nodes from the cascode transistors are very close and it might be hard for the off-chip transmission lines to connect such close nodes.

The disadvantage of the CMOS on-chip emulating transmission line is high loss. Although the on-chip LC ladder is 14 times shorter than its distributed counterpart [2.31] reports a 6dB loss for the  $\pi$  LC ( $Z_0=25\text{ohm}$ ) in 0.25  $\mu\text{m}$  CMOS technology at 1.4 GHz and the maximum PAE of the whole PA degrades to 10%-15% range. Therefore, the on-chip emulating transmission line is not used in [2.31]. However, an on-chip 4-LC-ladder has been used in [3.1] in a standard 0.18  $\mu\text{m}$  CMOS at 8 GHz. Since the measurement results haven't shown the S21 parameter of this emulating line the information of the loss can not be found in [3.1].

In summary the advantages and disadvantages of the on-chip emulating transmission and off-chip transmission line are listed in Table 3.13.

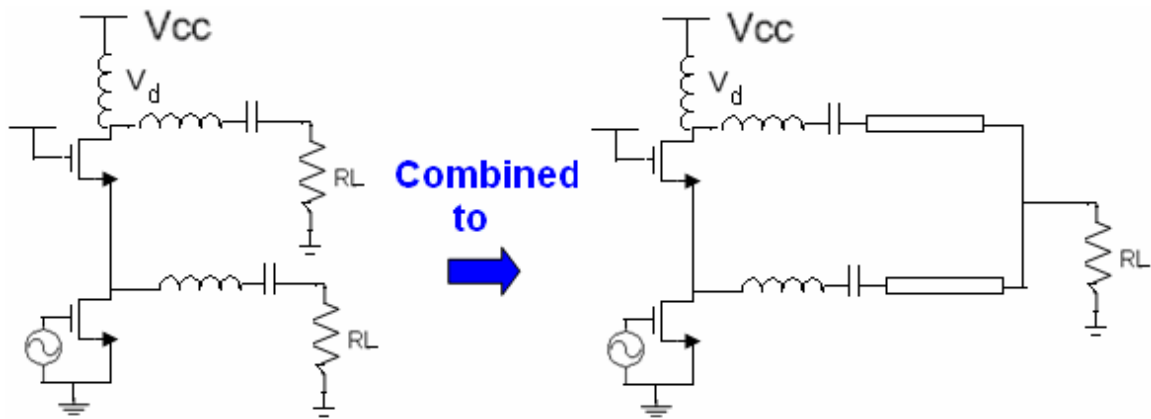


Fig. 3.38 The combining cascode structure.

Table 3.13 The advantages and disadvantages of on-chip and off-chip TLIN

	Advantages	Disadvantages
On-chip TLIN	<ol style="list-style-type: none"> <li>1. Provide connection to very close PA blocks</li> <li>2. Less area consumption</li> </ol>	<ol style="list-style-type: none"> <li>1. High loss</li> <li>2. No benefit for the N-device identical combining structure</li> </ol>
Off-chip TLIN	<ol style="list-style-type: none"> <li>1. Very low loss</li> <li>2. Provide benefit for the N-device identical combining structure</li> </ol>	<ol style="list-style-type: none"> <li>1. Large area consumption in lower carrier frequency</li> </ol>

### 3.6 Summary

In this chapter a complete analytical method for the voltage summation structure using parallel quarter-wavelength transmission line has been proposed. It's found that the promising characteristic of voltage summation is only valid for the ideal infinite harmonic class F PA and has limited practical application. Therefore, the power summation structure is proposed to implement the power combining, which is named as *N-device unbalanced power combining technique*. The basic idea is to redesign the impedance conversion blocks without changing the PA block so that the same optimal load is still provided by the combining network. Theoretically it's applicable for different PA modes and the verification has been given by the simulation results of both class E and C mode. The design formulas for the combining network are dependent on which impedance conversion circuit is implemented. The analysis model in Fig. 3.20 can be used to derive the design formulas if one impedance conversion technique is chosen.

The proposed power combining structure demands high impedance-transformation ratio and benefits when the quarter-wavelength microstrip line impedance conversion technique is used in practice. Therefore, in this work the quarter-wavelength transmission line is used as the combining network for class E PA blocks. The design formula is derived under two assumptions:

1. The voltages  $V_j'$  at each output node of the equivalent are in phase as shown in Fig. 3.23c.
2. The external operating conditions of the PA blocks don't change, such as the DC supply and the driving signal.
3. The antenna is a purely resistive load.

In the next chapter the nonidealities effect on the combining structure caused when either one of the assumptions are not satisfied will be discussed.

## Chapter 4

### Nonidealities in the $N$ -device unbalanced combining technique

#### 4.1 Introduction

The analysis of the proposed power combining technique is based on three assumptions, namely, equal phase, equal amplitude and a real antenna impedance. This chapter discusses the effects of nonidealities in the  $N$ -device unbalanced combining technique when either one of the assumptions is not satisfied.

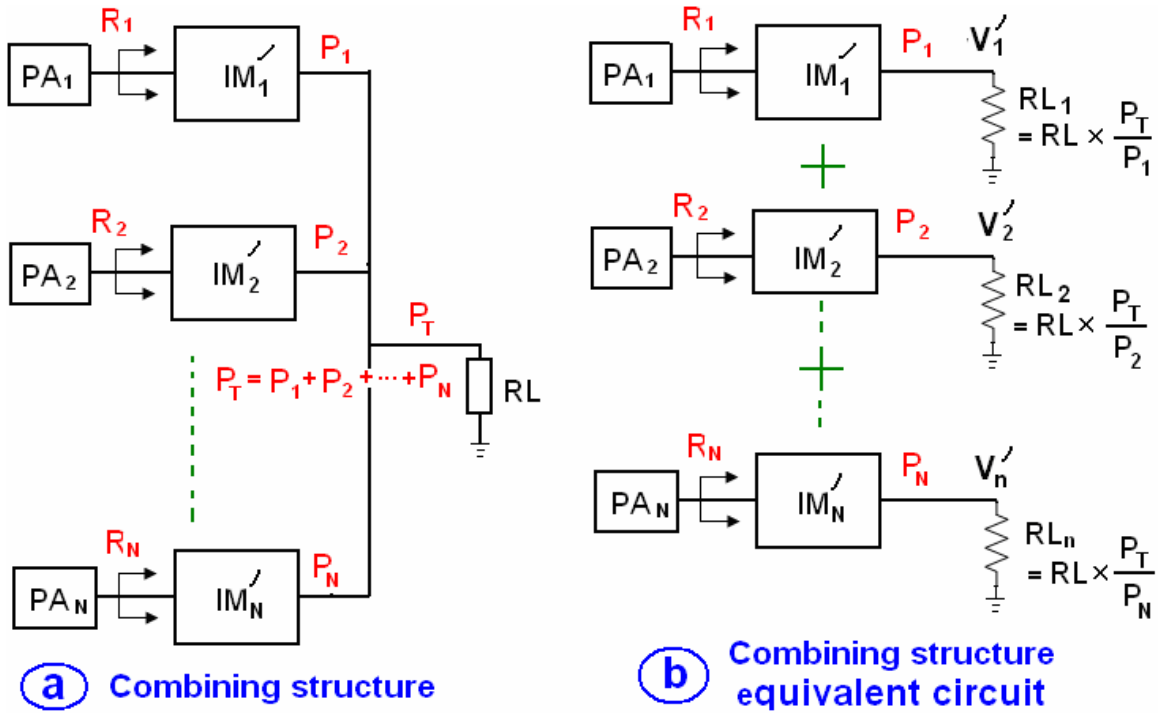


Fig. 4.1. The  $N$ -device combining structure and its equivalent circuit.

- 1. Phase nonidealities:** Following the design equation (3.27) and (3.30) only guarantees the amplitude of the output voltage  $V_j'$  in the equivalent circuit shown in Fig. 4.1b is equal. In case the phase of  $V_j'$  is different the combining structure designed by the equivalent circuit will be not valid and phase nonidealities happen.

- 2. Amplitude nonidealities:** For the ideal combining structure, where the output voltage  $V_j'$  are equal in both amplitude and phase, the equivalent circuit shown in Fig. 4.1b is valid. Due to some external changes such as the change of the supply voltage in the PA blocks the amplitude of the output voltage  $V_j'$  will be not the same and the combining structure is affected. Those external changes which cause the amplitude difference between the output voltage  $V_j'$  are denoted as the amplitude nonidealities.
- 3. Non-resistive antenna nonidealities.** The analysis of the proposed technique assumes that the antenna is a resistive load. When the combining structure delivers the power to a antenna with a reactive part, nonidealities happen.

In this chapter firstly the issues of the phase nonidealities are discussed such as the effect to the combining structure, the sources of the phase nonidealities and the methods for phase compensation. Secondly the issues of the amplitude nonidealities are discussed such as the effect to the combining structure, the sources of the amplitude nonidealities and the model to analyze the effect of the amplitude nonideality. Thirdly, the issue of non-resistive antenna is discussed. The summary ends this chapter.



## 4.2 Phase nonidealities

### 4.2.1 Introduction

In chapter 3 it's been discussed that (3.27) and (3.30) can be used to design the equivalent circuit shown in Fig. 4.1b and build the combining structure for  $N$  arbitrary single stage PAs. However, the assumption these two design equations are based on is that ideally all the voltages  $V_j'$  at the output nodes of the equivalent circuit shown in Fig. 4.1b are in phase. As a result the design equations (3.27) and (3.30) only guarantee the output voltages  $V_j'$  in the equivalent circuit are equal in magnitude. In case the output voltages  $V_j'$  of the equivalent circuit are not in phase the combining structure built from the equivalent circuit wouldn't operate as expected.

In the following sections the effect on the combining structure caused by the phase difference between the voltages  $V_j'$  is discussed. Secondly the sources which contribute to the phase difference are discussed. Finally the methods of phase difference compensation are discussed.

### 4.2.2 The effect of phase difference on the combination structure

Fig. 4.2 illustrates the nonideality caused by the phase difference. Based on (3.27) and (3.30) the equivalent circuit in Fig. 4.2a is built, which guarantee the following two requirements are satisfied:

1. Each PA block sees the optimal load  $R_j$
2. The output voltages  $V_j'$  have the same amplitude  $V_T$ .

However due to some reasons which will be mentioned in the next section the voltages  $V_j'$  may have different phase  $\varphi_j$  as shown in Fig. 4.2a. How the PA blocks interact with each other in the combining structure shown in Fig. 4.2b is a very complex subject. To completely solve out the exact effect on the combining structure in Fig 4.2b is very time-consuming and closed-form equations might not be achieved due to the complex variable

involvement. Notice that the PA block has a similar character to the power source, which is that both of them deliver the optimal power to the optimal load. The effect of the phase

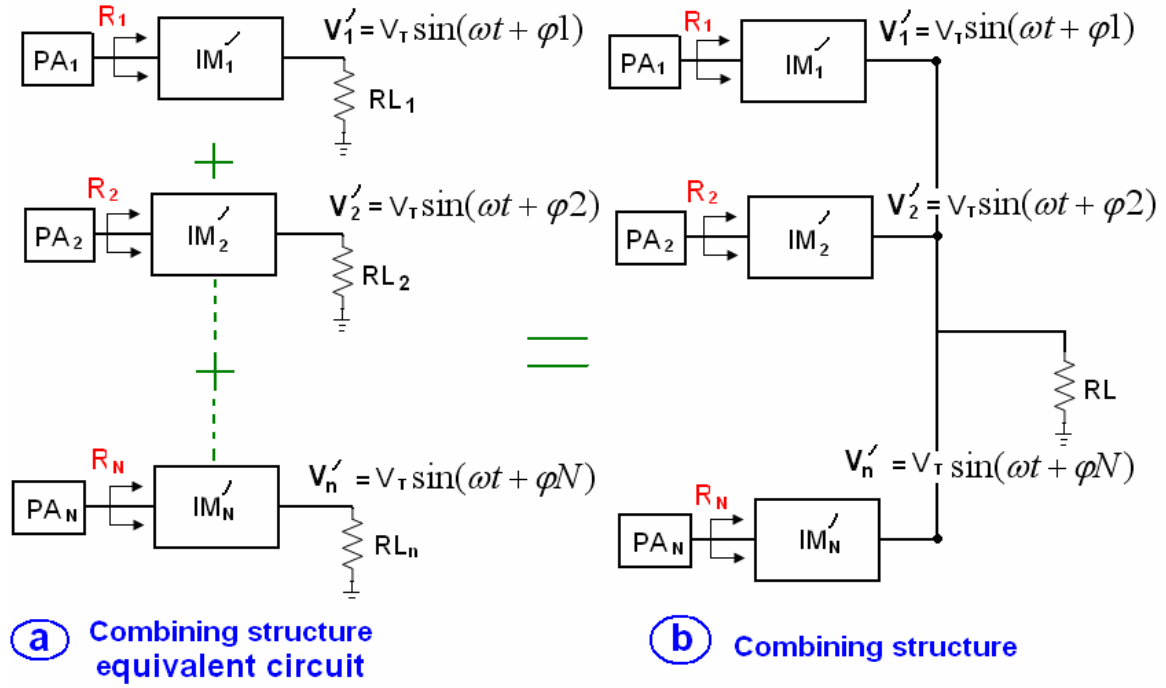


Fig. 4.2 The phase difference at the output voltages  $V'_j$  of the combining structure difference can be understood by analyzing the power-source combination shown in Fig. 4.3, where  $N$  power sources deliver the same amount of maximum power to the load  $R_s$ . However they are not in phase shown in Fig. 4.3a. The supposition method can be used to calculate the output voltage  $V_o$  in Fig. 4.3b when the power sources in Fig. 4.3a are connected at their output nodes.

#### Equations for the effect of phase differences

The derivation can be found in appendix 4.1 and the combined output voltage  $V_o$  in Fig. 4.3b is given by

$$V_o = \frac{1}{N} \times (V'_1 + V'_2 + \dots + V'_N) \quad (4.1)$$

If the voltages  $V'_j$  don't have the phase difference the combined voltage in Fig. 4.3b is given by

$$V_o = \frac{1}{N} \times (N \times V_T) = V_T \quad (4.2)$$

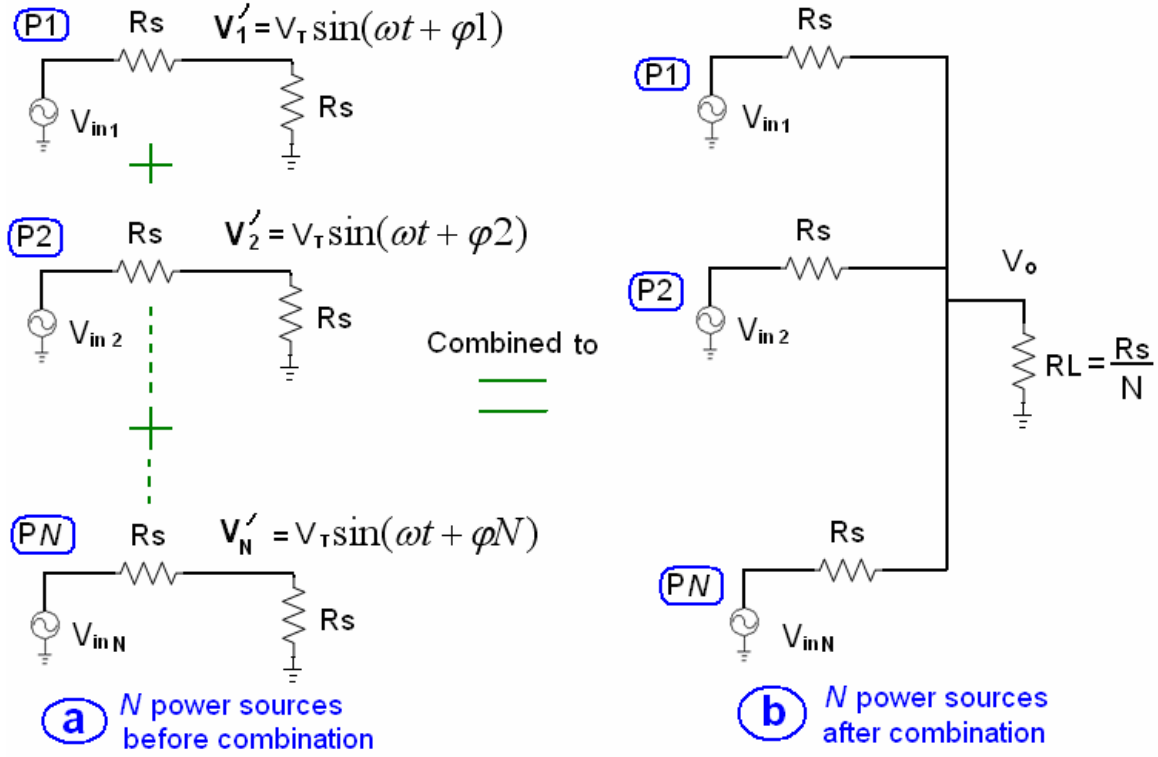


Fig. 4.3 The  $N$  power sources are combined with the phase differences in the output voltages

If the voltages  $V_j'$  do have phase difference as shown in Fig. 4.3a the combined output voltage  $V_o$  is given by

$$\begin{aligned}
 V_o &= \frac{V_T}{N} \times [\sin(\omega t + \phi_1) + \sin(\omega t + \phi_2) + \dots + \sin(\omega t + \phi_N)] \\
 &= \frac{V_T}{N} \times \sum_{j=1}^N \sin(\omega t + \phi_j)
 \end{aligned} \tag{4.3}$$

With  $A = [\sin(\phi_1) + \sin(\phi_2) + \dots + \sin(\phi_N)]$  and  $B = [\cos(\phi_1) + \cos(\phi_2) + \dots + \cos(\phi_N)]$

(4.3) is rearranged to

$$V_o = \frac{V_T}{N} \times \sqrt{A^2 + B^2} \cos(\omega t - \arctan \frac{B}{A}) \tag{4.4}$$

The amplitude of (4.4) is of interest. After some trigonometric function transforms in the appendix 4.2 the amplitude of  $V_o$  is given by (App.4.7)

$$\begin{aligned}
& \text{Amp}[V_o] \\
&= \frac{V_T}{N} \times \sqrt{N + 2 \sum_{i=2}^N \cos(\varphi_1 - \varphi_i) + 2 \sum_{i=3}^N \cos(\varphi_2 - \varphi_i) + \dots + 2 \sum_{i=N-1}^N \cos[\varphi(N-2) - \varphi_i] + 2 \cos[\varphi(N-1) - \varphi_N]}
\end{aligned} \tag{4.5}$$

When the phase difference between the voltages  $V_j'$  is small enough that each elements with the cosine function is approximated to 1 an (4.5) is approximated to

$$\text{Amp}[V_o] \approx \frac{V_T}{N} \times \sqrt{N + 2[(N-1) + (N-2) + \dots + 1]} = \frac{V_T}{N} \times \sqrt{N^2} = V_T \tag{4.6}$$

which is the same as the ideal result given in (4.2) when there is no phase difference. It shows that the effect on the combined output voltage  $V_o$  caused by the small phase differences can be neglected. Fig.4.4 gives a better illustration of the change of the output voltage  $V_o$  caused by the phase difference, where the combined output voltage  $V_o$  is normalized to the ideal output voltage  $V_T$  given in (4.2). The phase difference between the output voltage  $V_j'$  and  $V_{j+1}'$  shown in Fig.4.3a is assumed to be

$$\Delta\varphi = \varphi(j+1) - \varphi_j \tag{4.7}$$

As can be seen in Fig. 4.4 the more devices are combined the more effect caused by the phase difference to the output voltage  $V_o$ .

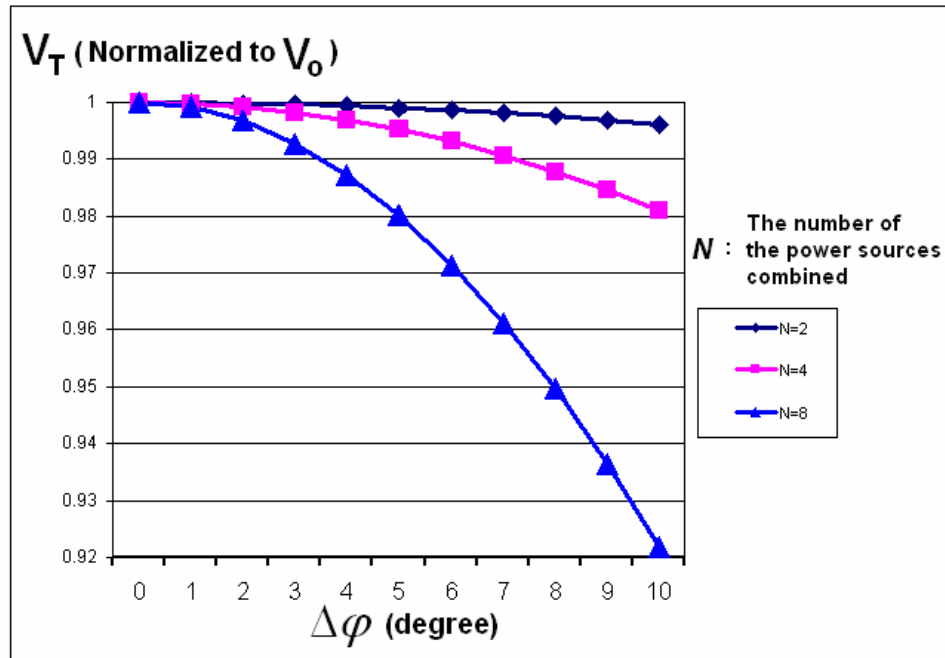


Fig. 4.4 The effect of the phase difference on the combined output voltage.

However, the full analysis of the phase difference effect on the combining network involves complex analysis and hasn't been done in this work.

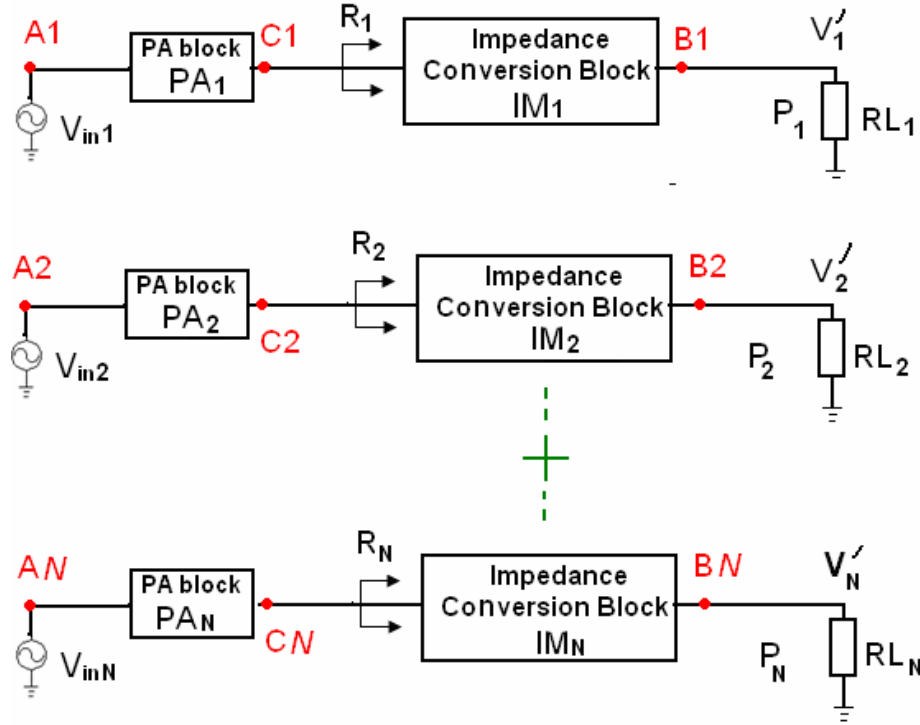


Fig. 4.5 Three sources of the phase nonidealities.

### 4.2.3 The sources of the phase nonidealities

There are three sources contributing to the phase difference between the voltages  $V_j'$  in the equivalent circuit, namely the input signal, the PA block and the impedance conversion block as illustrated in Fig. 4.5.

#### 4.2.3.1 The phase-difference source from the input signal

This source is trivial. Any phase difference between the input signal  $V_{inj}$  results the phase difference at the output voltages  $V_j'$ .

#### 4.2.3.2 The phase-difference source from the impedance conversion block

The impedance conversion technique introduces a phase shift between the input and output node of the impedance conversion block. The phase shift is not constant in some impedance conversion techniques such as a LC resonant network. As shown in Fig. 4.6 the ideal LC resonance network transforms the load  $R_{Load}$  to a smaller resistive load  $R_{in}$  at

one single frequency. As derived in the appendix 4.3 the ratio of the voltage at input node port 1 and output node port 2 is given by

$$\frac{V_{out}}{V_{in}} = 1 + j\sqrt{r-1} \quad (4.8)$$

Where  $r = \frac{R_{Load}}{R_{in}}$  the impedance-transformation ratio as is denoted in (3.31).

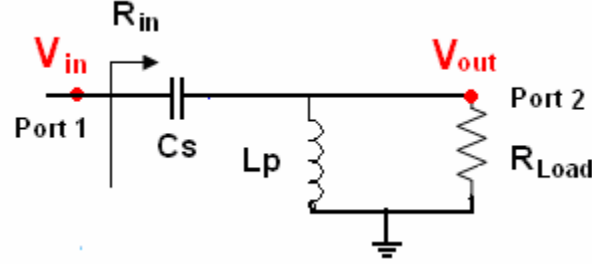


Fig. 4.6 Ideal LC resonance impedance conversion

For the LC resonance impedance conversion blocks having different impedance-transformation ratio a different phase shift is introduced between the input and output node, which results the phase difference between the output voltages  $V_j'$ .

Yet some impedance conversion techniques introduce a constant phase shift between the input and output node of the impedance conversion block such as the quarter-wavelength transmission line shown in Fig. 4.7. From equations (App.2.8) and (App.2.9) the ratio of the voltages at input node port 1 and output node port 2 is given by

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{V(0)}{V(-l)} = \frac{V_0^+ (1 + \Gamma_1)}{V_0^+ (e^{j\beta l} + \Gamma_1 e^{-j\beta l})} \\ &= \frac{Z_0}{\cos \beta l \times Z_0 - \sin \beta l \times ZL + jRL \sin \beta l} \end{aligned} \quad (4.9)$$

where  $Z_0$  is the characteristic impedance of the transmission line,  $\beta l$  is the electrical length which is 90 degree,  $ZL = RL + jXL$  is the load. In the equivalent circuit of the combining structure the load  $ZL$  is resistive. Therefore, the phase shift between the voltage at input node port 1 and output node port 2 for any quarter-wavelength transmission line is 90 degree, which results no phase difference at output voltages  $V_j'$ .

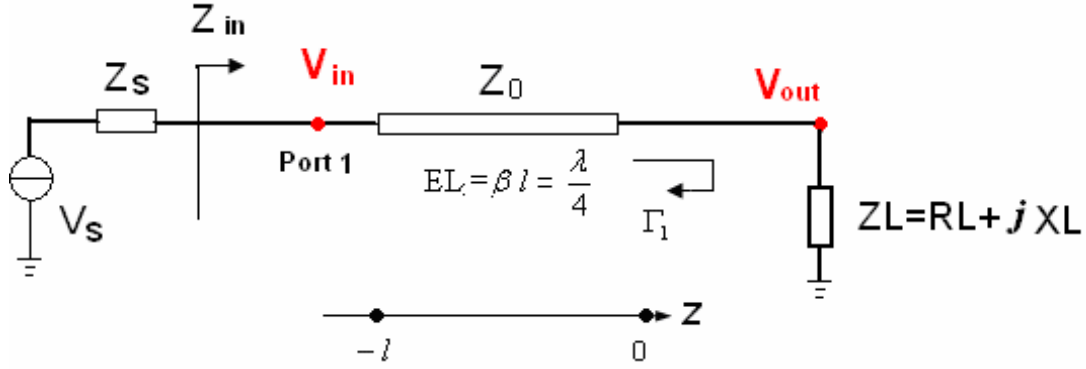


Fig. 4.7 Quarter-wavelength transmission line impedance conversion

#### 4.2.3.3 The phase-difference source from the PA block

Compared to the first two phase-difference sources, the PA block contributions to the phase difference is more complex. Since class E PA block is chosen to build the power

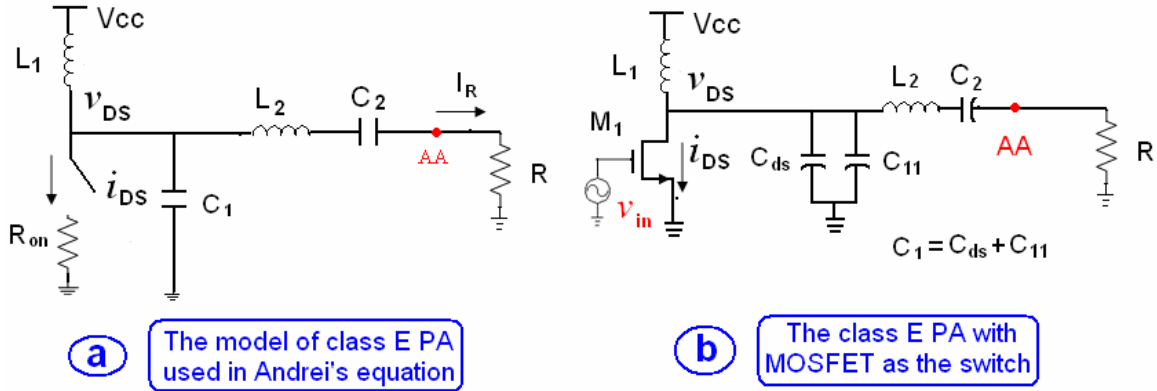



Fig. 4.8 The analysis model for the class E PA.

combining structure in this work the following analysis is focused on the phase difference caused by the class E PA block.

#### Review of Andrei's equations for Class E PA

As mentioned in Chapter 2 the class E PA is designed based on the Andrei's equations [1.4]. In their analysis to solve the design equations for the class E PA the circuit model shown in Fig. 4.8a is used [1.4], where the switching-on resistance  $R_{on}$  is zero. To design the class E PA using Andrei's equations, at first the parameter values such as the expected power output  $P_{exp}$ , working frequency  $f$ , supply voltage  $V_{cc}$  and quality factor  $Q$  of the filter block ( $L_2$  and  $C_2$ ) are input to the equations. Then the values of the

Table 4.1 The input and output variables of Andrei's equations

	Input Variables		Calculated Output
<p><b>Andrei's model</b> <b>[1.4]</b></p>	$f$ $V_{cc}$ $Q$ $P_{exp}$		$R = \frac{1.365 \times V_{cc}^2}{P_{exp}}$ $C_1 = \frac{0.685}{\omega R}$ $L_1 = \frac{0.732 \times R}{\omega}$ $C_2 = \frac{1}{\omega R Q}$ $L_2 = \frac{R Q}{\omega}$

elements such as  $L_1$ ,  $L_2$ ,  $C_1$ ,  $C_2$  and  $R$  are calculated<sup>1</sup>. Table 4.1 illustrates this calculation process. Note that in the Andrei's equations the phase of the output voltage at node AA shown in Fig. 4.8 is a fixed value of 15.155 degree. However, in the real class E PA circuit using the wide MOSFET transistor as the switch the switching-on resistance  $R_{on}$  is not zero. As a result, two issues can be met when using Andrei's equations to design the class E PA shown in Fig. 4.8b:

1. The phase of the output voltage at node AA is not constant, which is the reason that class E PA blocks introduce phase difference to the output voltages  $V_j'$ .
2. The drain efficiency  $\eta_{drain} = \frac{P_{out}}{P_{DC}}$  is smaller than 100%. Therefore the input variable  $P_{exp}$ , the expected power output, is approximately equal to the DC input power  $P_{DC}$  of the simulation result.

<sup>1</sup> It can be found in Table 4.1 that all the passive elements in the class E PA such as  $L_1$ ,  $L_2$ ,  $C_1$ ,  $C_2$  are all only determined by  $R$ , which is a useful information for the later analysis.



### $\frac{R_{on}}{R}$ controls the change of output phase and drain efficiency

As discussed just before the non-zero switch-on resistance  $R_{on}$  in the real class E PA causes the difference between the simulation result and Andrei's equation expectation. The closed-form equations to describe the effect of  $R_{on}$  on class E PA haven't been achieved due to the complex computation. Yet observations have been made to find out that  $R_{on}$  is not the factor which changes the output phase and the drain efficiency from the ideal values but  $\beta$  is.  $\beta$  is defined as the ratio between the optimal load and switching-on resistance shown in Fig. 4.8a, which is given by

$$\beta = \frac{R_{on}}{R} \quad (4.10)$$

For example, no matter  $R_{on}$  is 0.1 ohm or 10 ohm for all the class E PAs with the same  $\beta$  the output voltage phase and drain efficiency are the same. This conclusion is understandable because for a certain value of  $\frac{R_{on}}{R}$ , actually all the elements in Fig. 4.8a such as  $L_1$ ,  $L_2$ ,  $C_1$ ,  $C_2$ ,  $R_{on}$ ,  $R$  are all proportional to  $R$ . No matter how much the value of these elements changes it's just like the scaling. This conclusion can be verified by the simulation results of the circuit in Fig. 4.8b<sup>2</sup>. Table 4.2 shows the input variable of this

Table 4.2 The parameters of the simulation.

Input variables				
Fixed parameters			Sweeping parameter	
			Main sweep	Nested sweep
$f$ (GHz)	$V_{cc}$ (V)	$Q$	$\beta$	$P_{exp}$
2	0.6	10	Sweeping from 0.013 to 1	Sweeping from 10 mW to 100 mW

<sup>2</sup> The simulation setting is all the same with that in chapter 3.4.1 except that PSS analysis is used. PSS is much faster than the transient analysis, which enables a larger number of parameters sweep in a short time with accurate results.

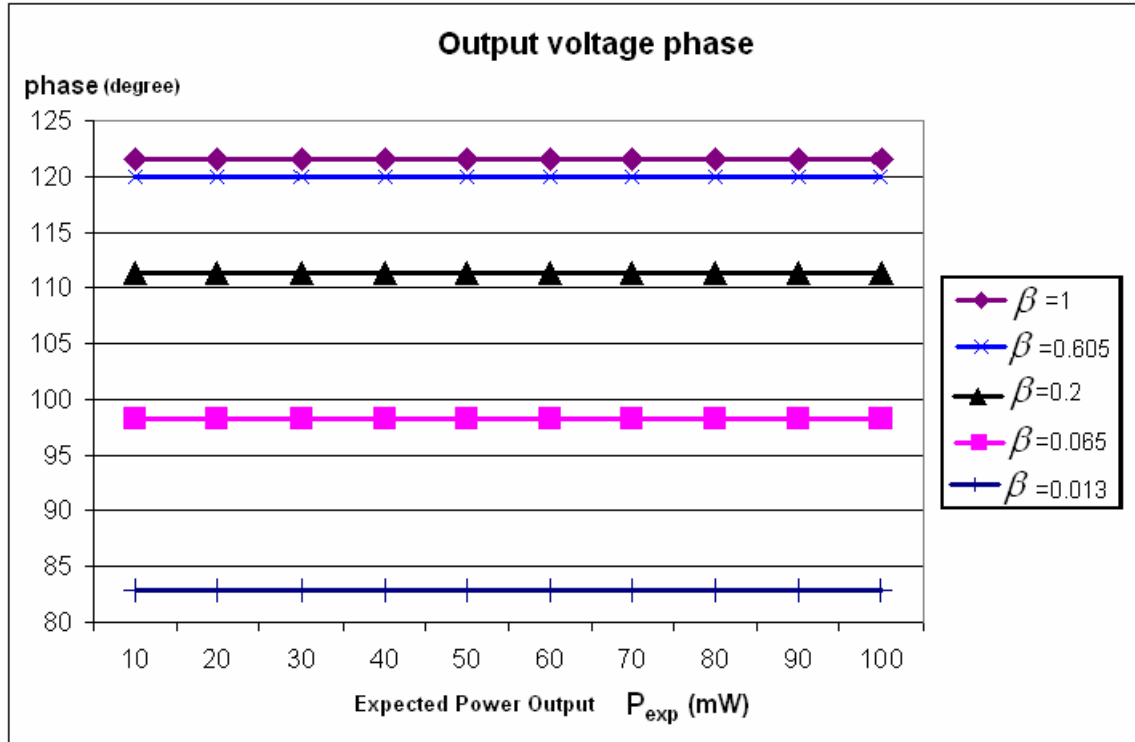


Fig. 4.9 The output voltage phase of the class E PA with the different  $\beta$ .

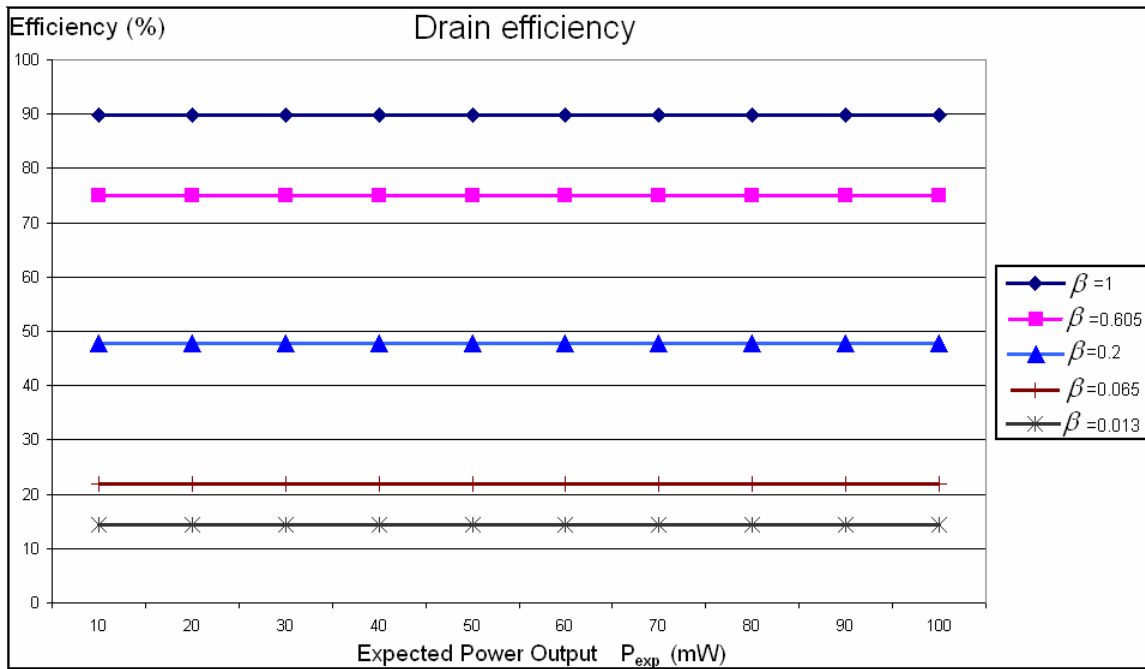


Fig. 4.10 The drain efficiency of the class E PA with the different  $\beta$ .

simulation for Andrei's equations. By the nesting sweeping ( $\beta$  is the main sweep and  $P_{\text{exp}}$  is the nested sweep) the values of  $L_1$ ,  $L_2$ ,  $C_1$ ,  $C_2$ ,  $R_{\text{on}}$ ,  $R$  and  $W/L$  (the ratio of the width to the length of the transistor) change, which shows the universality of this simulation. The simulation results in Fig. 4.9 and 4.10 show that for a given value of  $\beta$  the output phase and the drain efficiency of the class E PA don't change no matter what values are the elements such as  $L_1$ ,  $L_2$ ,  $C_1$ ,  $C_2$ ,  $R_{\text{on}}$ ,  $R$ .

### The extreme values of the output phase and drain efficiency for class E PA

As derived in appendix 4.4 the drain efficiency of the class E PA in Fig. 4.8 is given by

$$\eta_{\text{drain}} = (1 - 4.58 \times C_1 \omega R_{\text{on}}) \times 100\% \quad (4.11)$$

Substituting the equation of  $C_1$  shown in Table 4.1 into (4.11) yields

$$\begin{aligned} \eta_{\text{drain}} &= (1 - 2.1373 \times \frac{R_{\text{on}}}{R}) \times 100\% \\ &= (1 - 2.1373 \times \beta) \times 100\% \end{aligned} \quad (4.12)$$

Although (4.11) is an approximate model to predict the drain efficiency of the class E PA designed by Andrei's equations, it shows that the drain efficiency decreases with the increasing of  $\beta$ . This trend is verified by the simulation results shown in Fig. 4.11. In the nesting simulation  $P_{\text{exp}}$ <sup>3</sup> is the main sweep (from 10 mW to 100 mW in 20 linear steps) and  $\beta$  is the nest sweep (from 0.013 to 1 in 10 linear steps). Fig.4.11 shows that the trend of drain efficiency changing is only determined by  $\beta$ , which has nothing to do with other values such as  $P_{\text{exp}}$ . Fig. 4.12 shows that the output voltage phase increases with the increase of  $\beta$ .

Knowing that only  $\beta$  determines the change of the drain efficiency and output voltage phase another conclusion can be drawn that for a class E PA with a fixed-width transistor the drain efficiency can not be as high as anyone wants, it has a maximum value.

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<sup>3</sup> This simulation has the same values of  $f$ ,  $V_{\text{cc}}$ ,  $Q$  as those in Table.4.2. Based on the equation in Table 4.1 20 different samples of  $P_{\text{exp}}$  produces 20 different samples of class E PA with different power performance, which shows that the change of drain efficiency is only determined by  $\beta$ .

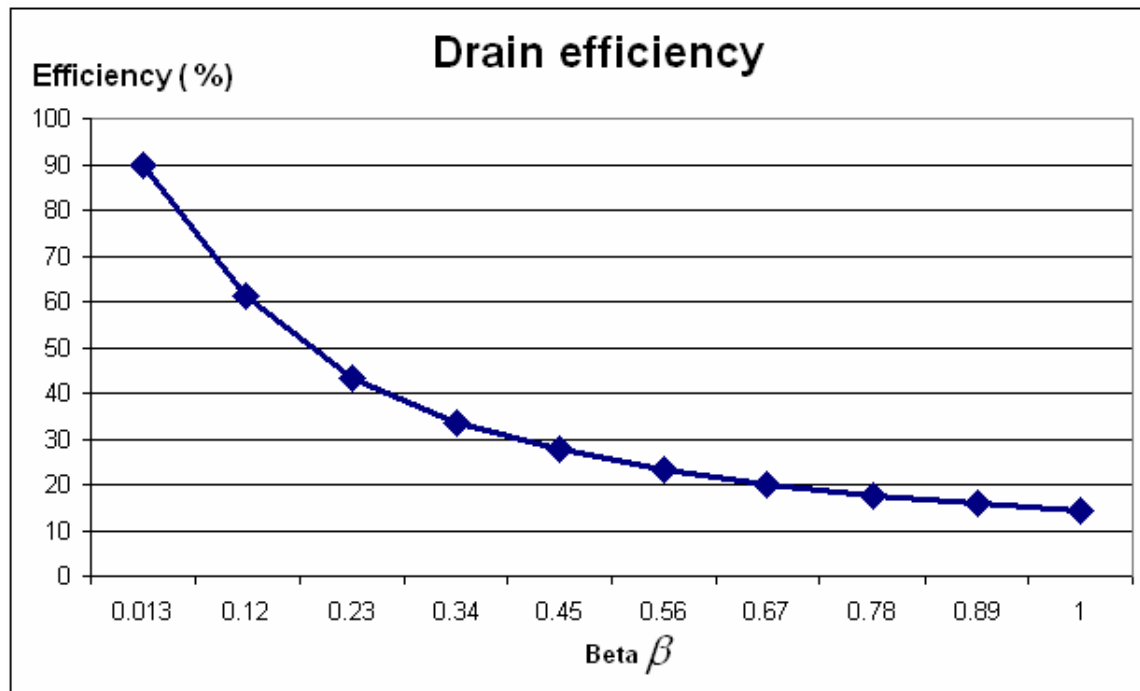


Fig. 4.11 Simulation result shows the drain efficiency changes only with  $\beta$ .

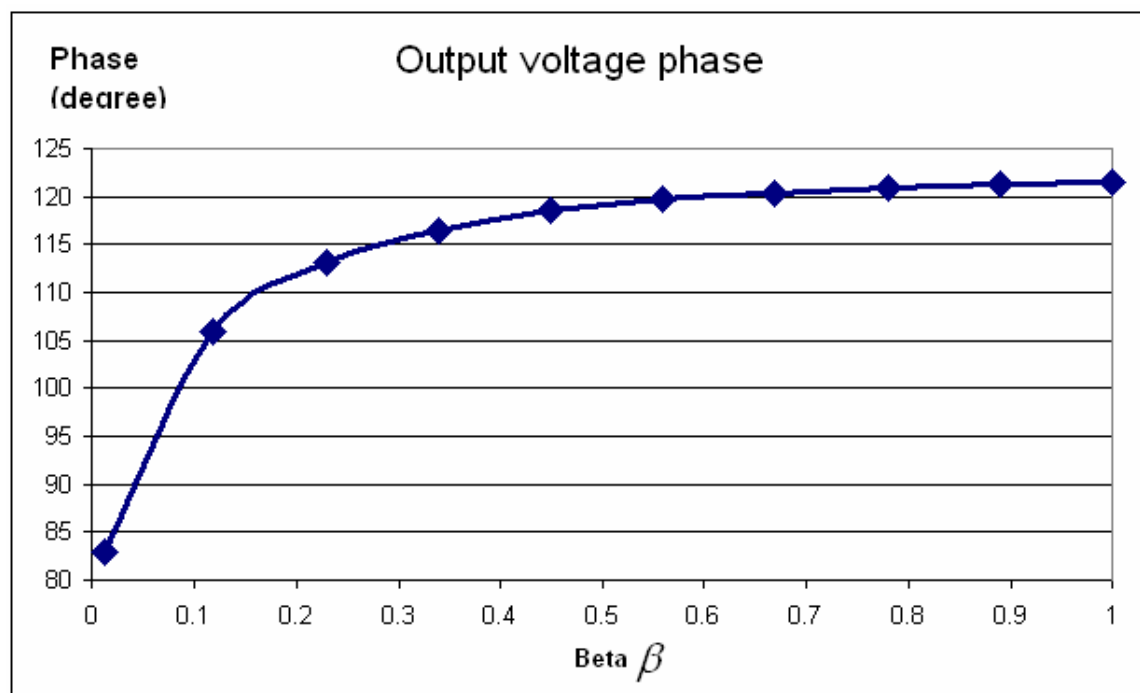


Fig. 4.12 Simulation result shows the output voltage phase changes with  $\beta$ .

Following explains this conclusion. The equations (App.4.20) and (App.4.21) in the appendix 4.5 gives

$$C_{ds} = \frac{k_c}{k_{Ron} R_{on}} = \frac{k_c k_{Ron}}{R\beta} \quad (4.13)$$

$$C_1 = C_{ds} + C_{11} = \frac{0.685}{\omega R} \geq C_{ds} , \quad (4.14)$$

where  $C_{11}$  is the external capacitance added to the drain as shown in Fig. 4.8b.

Combining (4.13) and (4.14) yields

$$\beta \geq \frac{k_c k_{Ron} \omega}{0.685} \quad (4.15)$$

For a given CMOS process  $k_c$  and  $k_{Ron}$  have approximately a fixed value thus a given CMOS process has a fixed minimum  $\beta$ , which results a maximum drain efficiency. For the CMOS18 process used in the simulation of this work  $\beta$  is larger than 0.01165 based on the simulation results. This is the reason that the lowest  $\beta$  set in the simulation is 0.013, as can be seen in Fig. 4.9-4.12. However, the equivalent switch-on resistance  $R_{on}$  and  $C_{ds}$  varies with the supply voltage a little, which result that  $k_c$  and  $k_{Ron}$  are weak function of the supply voltage and thus the minimum  $\beta$  will varies a little with supply voltage in a given CMOS process.

## Summary

Based on the observation of a large amount of class E PA simulation results it's concluded:

1.  $\beta$  determines the changes of output voltage phase and drain efficiency.
2. A given process has a maximum value of drain efficiency and a minimum value of output voltage phase for a given supply voltage.
3. Comparing the  $\beta$  of the class E PAs can check whether there are output voltage phase difference.
4. In the balanced combining structure the PA blocks are identical and will not introduce any phase difference.

5. Referring to Fig. 4.11 and 4.12 the phase and drain efficiency can be found for any class E PA with a certain value of  $\beta$ .<sup>4</sup>

#### 4.2.4 Methods of Phase Compensation

To obtain the power combining performance as expected by the design equations (3.27) and (3.30) measures are desirable to be taken to eliminate the phase difference at the output voltage  $V_j'$ . Three kinds of measures can be taken accordingly in the three sources of the phase difference.

1. Measures taken in the design of the PA blocks.
2. Measures taken in the design of the impedance conversion blocks.
3. Measures taken in the design of the driving signal blocks.

These three kinds of measures are discussed as follows.

##### Measures taken in the design of the impedance conversion blocks

When both the PA blocks and impedance conversion blocks introduce the phase difference to the output voltages  $V_j'$  it's possible to make the phase difference caused by the PA block and the impedance conversion compensated by each other and leave the output voltages  $V_j'$  in phase for the equivalent circuit. Fig. 4.13 illustrates the phase counteraction in the equivalent circuit of a two-device combining structure. Between nodes AA1 and AA2 the phase difference caused by the PA blocks  $PA_1$  and  $PA_2$  are  $\phi_1 - \phi_2$  while the impedance conversion blocks  $IM_1$  and  $IM_2$  introduce a phase difference  $\phi_2 - \phi_1$ . As a result the voltages  $V_{o1}$  and  $V_{o2}$  at nodes BB1 and BB2 respectively can be in phase. For example, when the LC resonance network is used for impedance conversion blocks  $IM_1$  and  $IM_2$  the phase shift between node AA and BB is

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<sup>4</sup> Since Fig. 4.11 and 4.12 is the sweep simulation result with fixed supply voltage and Quality factor of the filter block Q, for the class E PA with other fixed values of supply voltage and Quality factor, Fig. 4.11 and 4.12 need replotting.

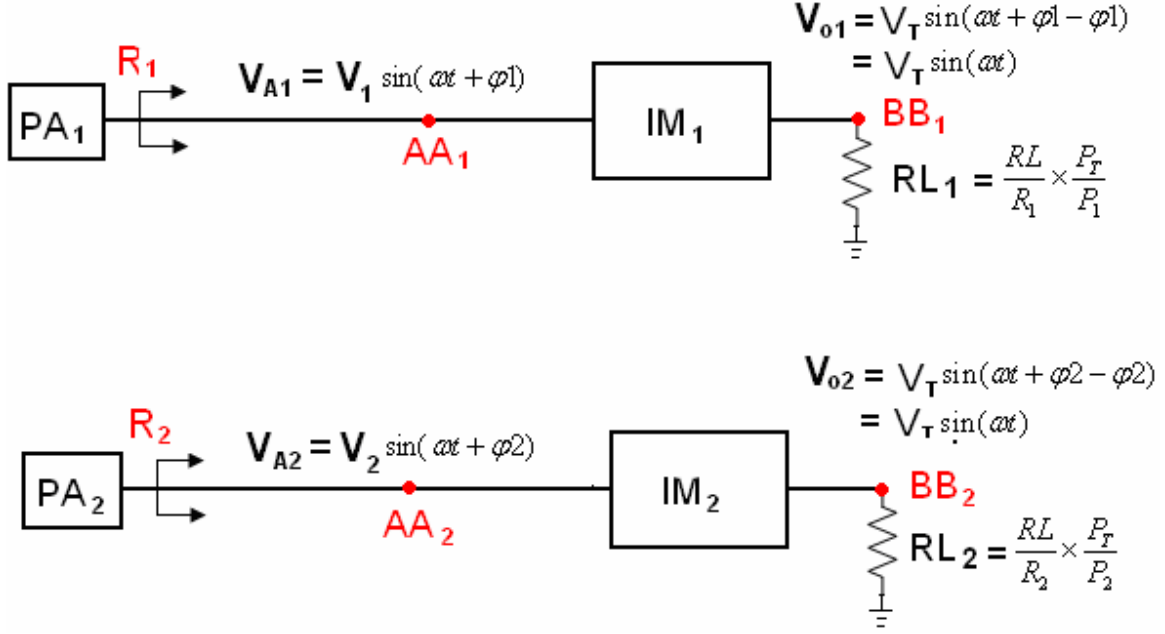


Fig. 4.13 Synthesize the design of the impedance conversion blocks and PA blocks to enable the output voltages in phase.

given by ( derived in the appendix 4.3)

$$\phi_1 = \arctan \sqrt{r_1 - 1} = \arctan \sqrt{\frac{RL}{R_1} \times \frac{P_T}{P_1} - 1} \quad (4.16)$$

$$\phi_2 = \arctan \sqrt{r_2 - 1} = \arctan \sqrt{\frac{RL}{R_2} \times \frac{P_T}{P_2} - 1} \quad (4.17)$$

where  $R_1$  and  $R_2$  are the optimal load each PA blocks need to see;  $P_1$  and  $P_2$  are the power output of the PA blocks  $PA_1$  and  $PA_2$  respectively, their summation is  $P_T$ .

Assuming  $P_1$ ,  $P_2$ ,  $R_1$  and  $R_2$  are fixed the only variable can be adjusted is  $\Gamma = \frac{R_{on}}{R}$ .

Since the change of  $\Gamma$  affects the power efficiency resulting the change of the output power  $P_1$ ,  $P_2$  this method needs to be synthesized by the simulation.

### Measures taken in the design of the driving signal blocks

As shown in Fig. 4.14b a phase shift circuit is added to the driving signal of the PA in Fig. 4.14a. Ideally the phase shift  $-\phi_1$  introduced by the phase shifter compensates the phase shift in the PA block and enables the phase of the output voltage  $V_{o1}$  go back to the

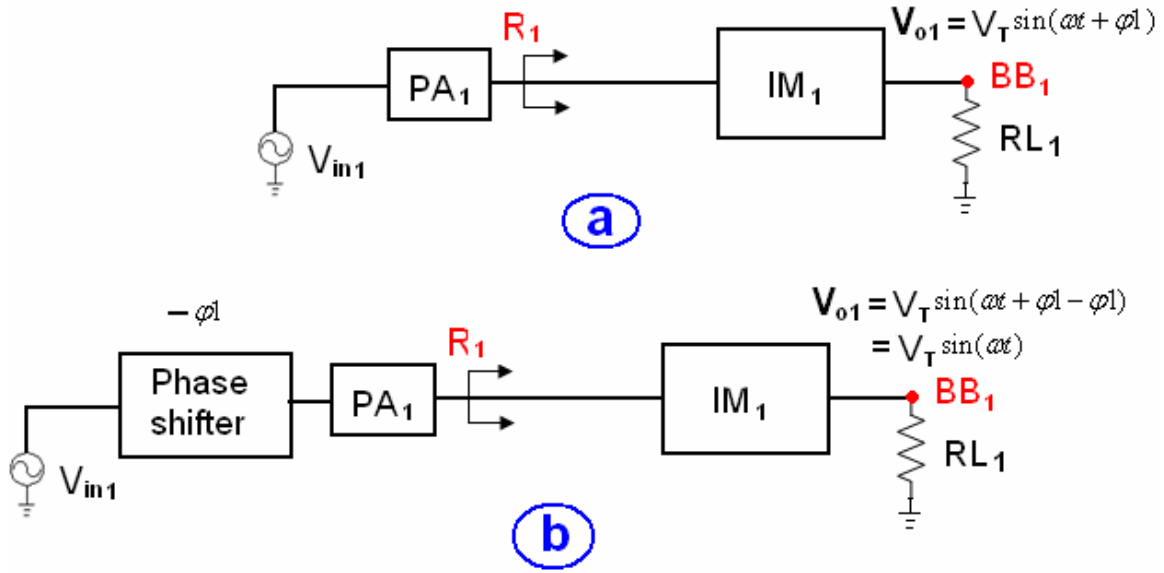


Fig. 4.14 The phase shifter is used to compensate the output voltage phase.

expected value 0. In the digital circuits world the delay locked loop (DLL) is used to introduce delays to the output clock [4.1], which could be useful to build the phase shifter. The inverter could also be used to build the phase shifter by manipulating its propagation delay time  $t_p$ . One example is discussed as follows.

As shown in Fig. 4.15 is the original PA block with the inverter as the driving stage, where  $C_{gate}$  is the equivalent gate capacitance of the inverter;  $C_{ini}$  is the equivalent intrinsic capacitance of the inverter consists of the diffusion and Miller capacitances. The

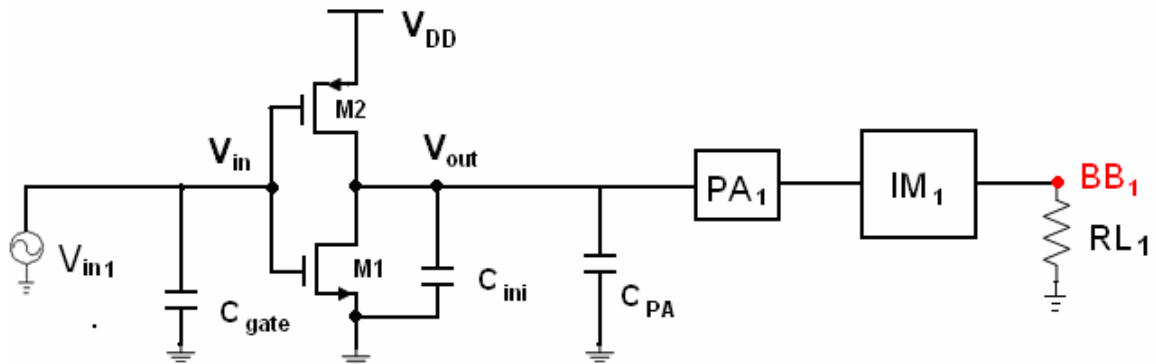


Fig. 4.15 The class E PA using the inverter as the driving stage.

capacitance of the PA transistor's gate seen by the inverter is modeled as a linear capacitor  $C_{PA}$ .  $C_{gate}$  and  $C_{ini}$  are proportional to the width of the transistor in the inverter [4.1], which are given by



$$C_{gate} = (\alpha \times K_{gatep} + K_{gaten})W_1$$

(4.18)

$$C_{ini} = (\alpha \times K_{inip} + K_{inin})W_1 \quad (4.19)$$

where  $\alpha$  is the width ratio of PMOS  $M2$  over NMOS  $M1$ ;  $K_{gatep}$  and  $K_{gaten}$  are the multiplication factor to relate the equivalent gate capacitance  $C_{gate}$  to the width of PMOS  $M2$  and NMOS  $M1$  respectively;  $K_{inip}$  and  $K_{inin}$  are the multiplication factor to relate the equivalent intrinsic capacitance  $C_{ini}$  to the width of PMOS  $M2$  and NMOS  $M1$  respectively;  $W_1$  is the width of NMOS  $M1$ .

The first-order approximation of the propagation delay for the inverter is given by [4.1]

$$t_p = 0.69 \times (C_{ini} + C_{PA}) \times \left( \frac{R_{eqn} + R_{eqp}}{2} \right) \quad (4.20)$$

within which the pull-down and pull-up equivalent resistance of NMOS  $M1$  and PMOS  $M2$  are  $R_{eqn}$  and  $R_{eqp}$ . They are linear to the transistor width [4.1] and given by

$$R_{eqn} = \frac{K_m}{W_1} \quad (4.21)$$

$$R_{eqp} = \frac{K_{rp}}{\alpha W_1} \quad (4.22)$$

$K_m$  and  $K_{rp}$  are the multiplication factor to relate the equivalent resistances  $R_{eqn}$  and  $R_{eqp}$  respectively to the width NMOS  $M1$  and PMOS  $M2$

Substituting (4.18), (4.19), (4.21) and (4.22) into (4.20) yields

$$t_p = \frac{0.69}{2} \left[ (K_m K_{inin} + K_{rp} K_{inip}) + \alpha K_m K_{inip} + \frac{1}{\alpha} (K_{rp} K_{inin} + \frac{K_{rp} C_{PA}}{W_1}) \right] \quad (4.23)$$

When  $\alpha = \frac{\sqrt{C_{PA} K_{rp} + K_{inin} K_{rp} W_1}}{\sqrt{K_{inip} K_m W_1}}$  the minimum value of  $t_p$  is given by

$$t_{p,min} = \frac{0.69}{2} \times \left( \sqrt{2 \times K_{inip} K_m K_{rp} \left( \frac{C_{PA}}{W_1} + K_{inin} \right) + K_m K_{inin} + K_{rp} K_{inip}} \right) \quad (4.24)$$

To the first order  $K_m$ ,  $K_{rp}$ ,  $K_{inip}$ ,  $K_{inin}$  are constant determined by the fabrication process. Thus for a given PA block the delay time introduced to the output voltage of the

PA can be adjusted by changing the width of the NMOS M1 and the width ratio  $\alpha$ . Note that increasing  $\alpha$  and  $W_1$  will increase the driving power  $P_{drive}$  and dynamic power consumption  $P_{dyn}$  of the inverter as  $P_{dyn}$  is given by [4.1]

$$P_{dyn} + P_{drive} = V_{DD}^2 f \times (C_{ini} + C_{PA} + C_{gate}) = [(\alpha \times K_{inip} + K_{gatep}) + K_{inin} + K_{gaten}] W_1 \quad (4.25)$$

### Measures taken in the design of the PA blocks

Choose the PA blocks with small difference in  $\beta$ . As discussed in the previous section the smaller the difference between the values of  $\beta$  the smaller phase difference will be introduced between the output voltages  $V_j'$  in the equivalent circuit designed by (3.27) and (3.30).

The balanced combining network uses identical PA blocks that have the same  $\beta$ . Mismatch should be avoided to make sure the PA blocks are identical. Unfortunately, every fabrication has component variation and the class E PA block will be affected, which can be reflected by the changing of  $Z_{in}$  shown in Fig. 4.20. As been derived in appendix 4.6, the variation of impedance  $Z_{in}$  is given by

$$1 + jQ_L \left( \frac{\Delta L}{L_0} + \frac{\Delta C}{C_0} \right) \quad (4.26)$$

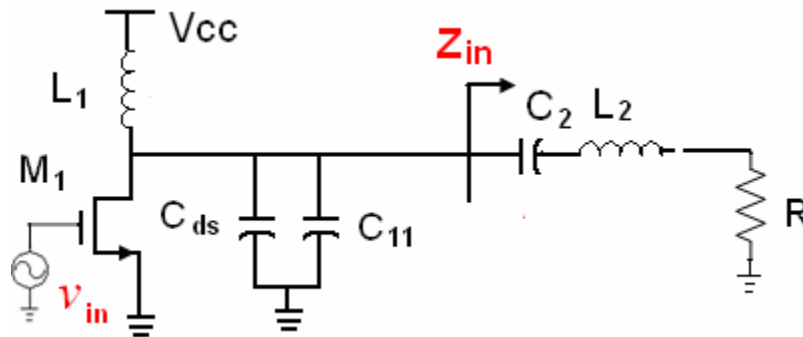


Fig. 4.20 Illustration of the Class E PA

As a result, the higher  $Q_L$  causes higher load-impedance variation for the transistor, which makes the PA more sensitive to the component variation. However, low  $Q_L$  brings high THD in the output signal. With the TLSC introduced in section 3.4.3 to short-

circuit all the even harmonics the combination of low  $Q_L$  and TLSC ensures a high component variation tolerance and a decent THD.

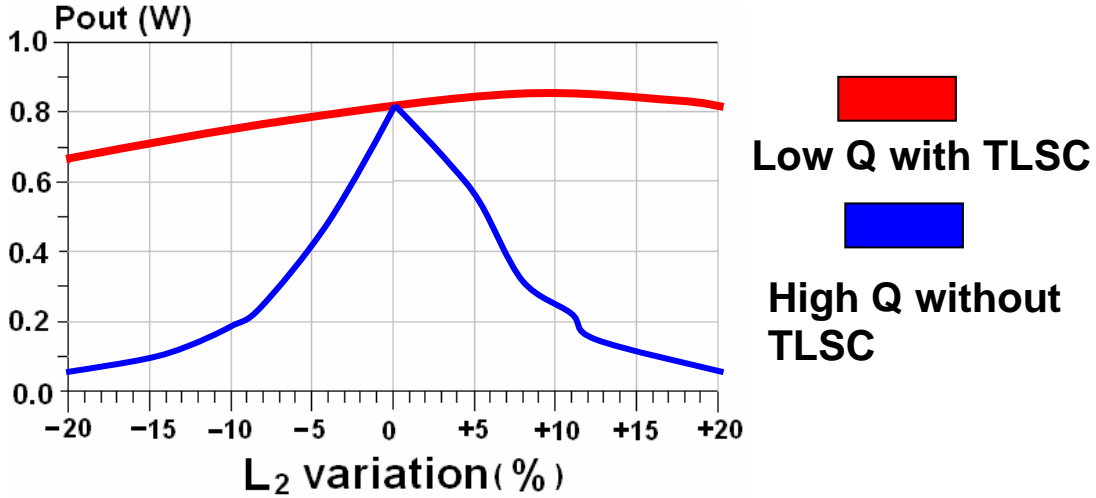


Fig. 4.21 The simulation result of the output power sensitivity over the variation of  $L_2$ .

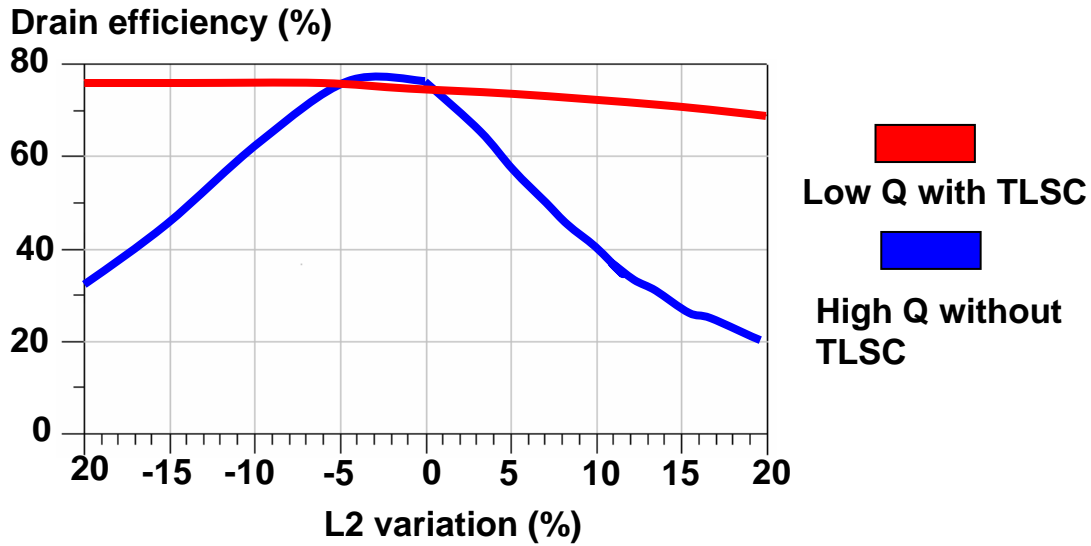


Fig. 4.18 The simulation result of the drain-efficiency sensitivity over the variation of  $L_2$ .

Fig. 4.21 and 4.18 shows the variation of power output and drain-efficiency caused by the variation of inductor  $L_2$ , where the red curve (in the upper position) responses to the result with  $Q$  of 2 and a TLSC; the blue curve (in the lower position) responses to the result with  $Q$  of 20 and no TLSC. However, the obvious improvement of the component

variation contributed by the low Q and TLSC pays the price of relatively higher THD shown in Fig. 4.19,

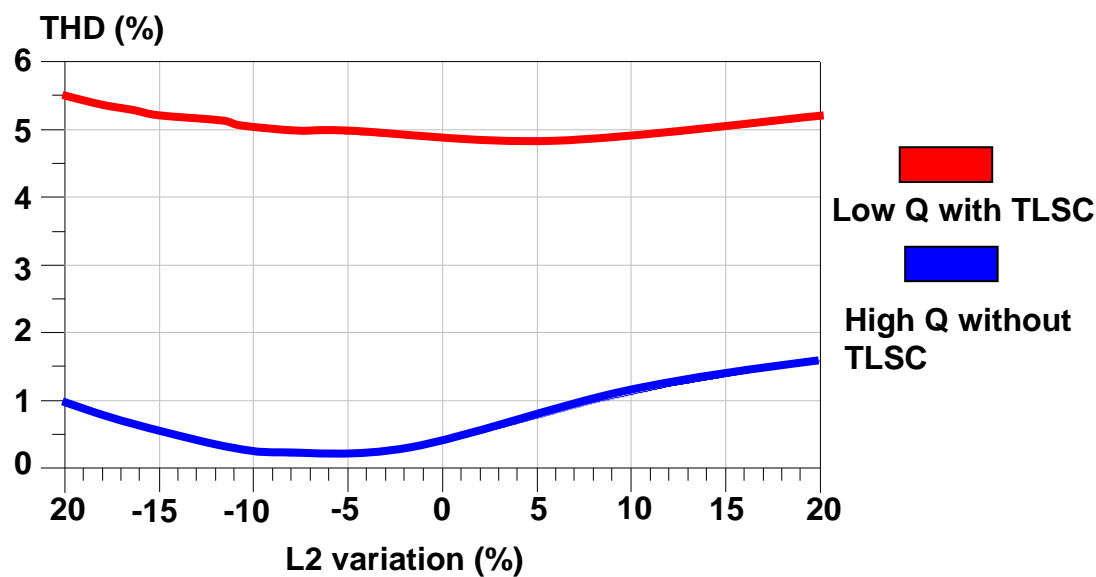


Fig. 4.19 The simulation result of the THD.

## 4.3 Amplitude nonidealities

### 4.3.1 Sources of the amplitude nonidealities

The equivalent circuit for the combining structure shown in Fig. 4.1b is valid only when the output voltages  $V_j'$  are equal both in phase and amplitude. Following the design equation (3.27) and (3.30) for the combining structure can only 100% guarantee the output voltages  $V_j'$  are equal in amplitude while the phase can be different due to three reasons. However, even the ideal combining structure which satisfies that the voltages  $V_j'$  are equal in phase and amplitude may still have nonidealities caused by the working conditions. The nonidealities for the operating ideal combining structure usually come externally shown in Fig. 4.20, which mostly are:

1. **The supply voltages** for some PA blocks in the combining structure change from the expected value as denoted by the change from  $V_{cc}$  to  $V_{cc}'$  in  $PA_1$  shown in Fig 4.20.
2. **The driving signals** for some PA blocks in the combining structure change from the expected waveform as denoted by the change from  $V_{in}$  to  $V_{in}'$  in  $PA_1$  shown in Fig 4.20.

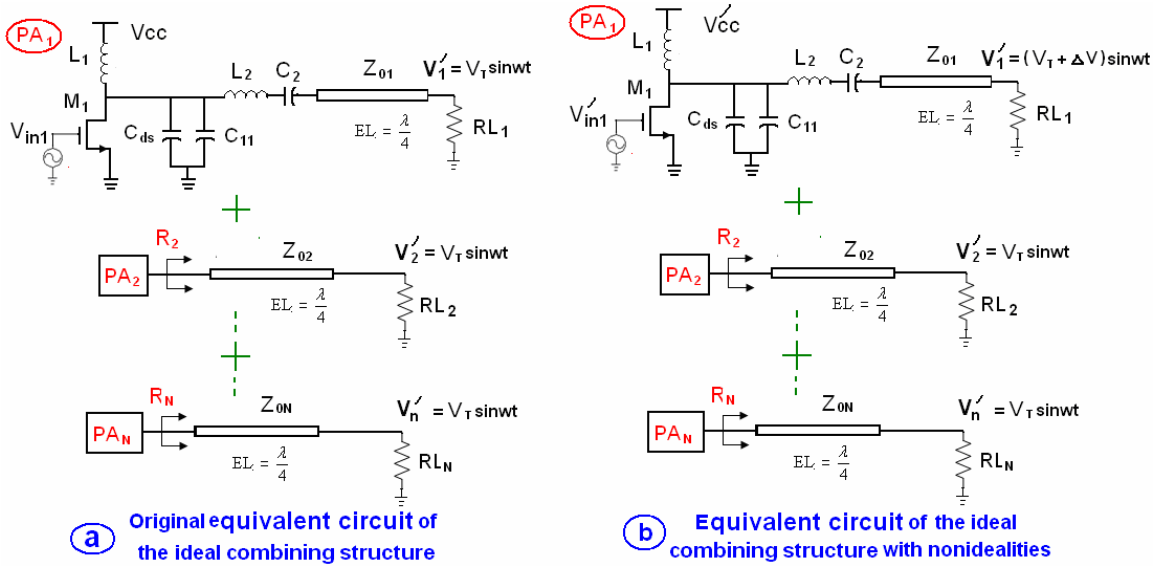


Fig. 4.20 The amplitude nonidealities in the PA block  $PA_1$  of the combining structure equivalent circuit

To obtain specific understanding of this issue the PA block will use class E mode and the quarter-wavelength transmission line is used for impedance conversion in the following analysis. Fig. 4.20 shows the equivalent circuit of the combining structure, where the amplitude nonidealities are assumed to only happen in  $PA_1$ . To illustrate the nonidealities the PA block  $PA_1$  is not denoted by the diagram but by a class E schematic shown in Fig. 4.20. In the original equivalent circuit of the ideal combining structure shown in Fig. 4.20a the voltages  $V_j'$  are equal in phase and amplitude. Fig. 4.20b shows that either the change of the supply voltage from  $V_{cc}$  to  $V_{cc}'$  or the change of the driving signal from  $V_{in}$  to  $V_{in}'$  result the change in the output voltage  $V_1'$ , which are listed as follows:

1. **Class E PA changes caused by the change of supply voltage  $V_{cc}$ .** Theoretically the power output and input of class E PA scales  $k^2$  times when  $V_{cc}$  scales  $k$  times [2.14]. Therefore the output voltage  $V_1'$  only changes in the amplitude as shown in Fig. 4.20b. This implies a perfect application of class-E power amplifiers in envelope elimination and restoration (EER) systems, where the envelope variation of the modulated signal is imposed to the switching power amplifier through the power supply. However, this power scaling conclusion assumes the constant switching-off capacitance  $C_1$  and constant switching-on resistance  $R_{on}$ . The nonlinearity of  $C_1$  and  $R_{on}$  of the transistor may introduce some errors such as that the power scaling factor is not exactly  $k^2$  or the phase of  $V_1$  changes a little. Yet in this analysis it's still assumed that the change of the supply voltage only results the amplitude change of  $V_1'$  from  $V_T$  to  $V_T + \Delta V$  shown in Fig. 4.21b.
2. **Class E PA changes caused by the change of driving voltage  $V_{in}$ .** In section 4.2 it's been discussed that the phase changes of  $V_{in}$  results the phase changes in the output voltages  $V_j'$ . To simplify the analysis it's assumed here the change of the driving  $V_{in}$  only results in the amplitude change for the output voltages  $V_j'$ .

Therefore, this section is about the amplitude changes at output voltages  $V_j'$  of the equivalent circuit shown in Fig. 4.20b caused by those two kinds of nonidealities happening to the operating ideal combining structure. Once any one of the output voltages  $V_j'$  is different from others in amplitude the equivalent circuit shown in Fig. 4.20b is not valid to analyze the combining structure.

### 4.3.2 The effect of amplitude nonidealities

Fig 4.21b illustrates the amplitude change in  $V_1'$  caused by the nonidealities  $V_{in1}'$  and  $V_{cc}'$  in the equivalent circuit. Compared with the PA block  $PA_1$  in the equivalent circuit of the ideal combining structure in Fig. 4.21a the output voltage of  $PA_1$  changes from

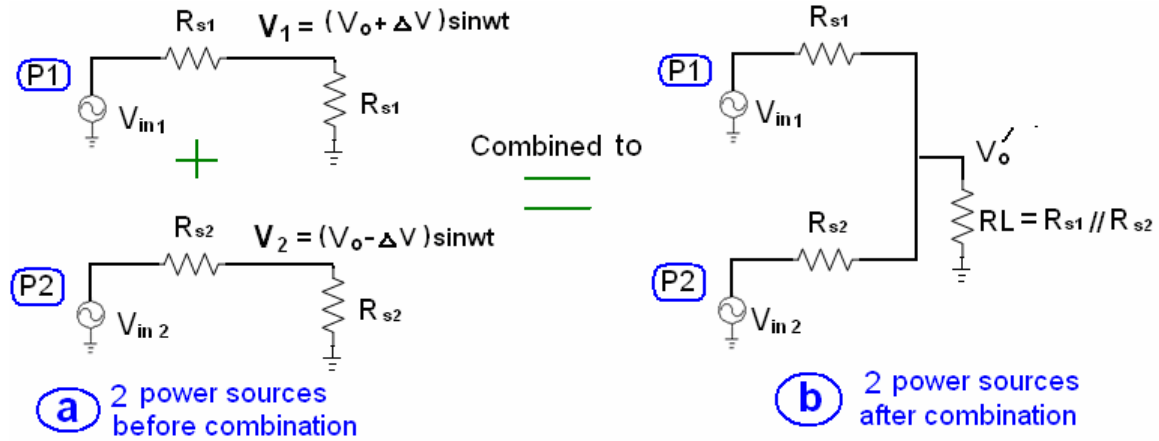


Fig. 4.21 Amplitude difference between the output voltages of the power sources.  $V_1 \sin \omega t$  to  $(V_1 + \Delta V) \sin \omega t$ . Note that the PA block has similarity to the power source which only delivers maximum power to the load when the load is a conjugate of the source impedance. Therefore the effect of the amplitude difference can be understood by analyzing the power source combination shown in Fig. 4.21. Two power sources are expected to deliver the maximum power to the load  $R_{s1}$  and  $R_{s2}$ , where the output voltages  $V_1$  and  $V_2$  are supposed to be  $V_o$  and they can be connected at the output node directly shown in Fig. 4.21b. Therefore, the circuit in Fig. 4.21a is the equivalent circuit of that in Fig. 4.21b and the output voltage of the combined circuit is  $V_o$ . However, if the output voltages of the two power sources changes to  $V_o + \Delta V$  and  $V_o - \Delta V$  respectively, this equivalent circuit shown in Fig. 4.21a is not valid any more. As derived in the

appendix 4.7 the real combined voltage in Fig. 4.21b change into  $V_o'$ ,

$$V_o' = V_o + \frac{R_{s1} - R_{s2}}{R_{s1} + R_{s2}} \Delta V, \text{ which shows that the larger the amplitude difference the more}$$

different the output voltage is from the designed value.

### 4.3.3 General mathematical model

In this subsection a mathematical model is used to explain the general effect of the amplitude difference caused by the amplitude nonidealities. Before the discussion of the general model an expression about class E PA is introduced.

#### Power-load function

As shown in Fig. 4.22 the power output of the class E PA can be expressed as a function of  $Z_{in}$ , the load the PA block sees, given by

$$P_1 = f_1(Z_{in}) \quad (4.27)$$

Theoretically only when  $Z_{in}$  is equal the optimal load  $R$  the class E PA operates optimally (e.g. in the highest drain efficiency). However, in practice the PA block might not see  $R$  due to some nonidealities. Thus it's of interest to know the power-load function  $f_1(x)$  between  $P_1$  and  $Z_{in}$  given by (4.27). When any parameters in the PA block changes such as  $V_{cc}$ ,  $V_{in}$ ,  $L_1$ ,  $L_2$ ,  $C_1$ ,  $C_2$  and  $R$  the function  $f_1(x)$  will change denoted by the change from  $f_1(R)$  to  $f_1'(R)$ . However, the function  $f_1(R)$  can not be derived by just using class E condition<sup>5</sup>. To derive a simple closed-form equation for the function  $f_1(R)$  is complicated and tedious. Yet this expression still will be used in the following analysis.

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<sup>5</sup> If the load  $R$  is optimal, the class E condition is satisfied, where the drain voltage and its slope is zero at the switch-off time. As a result, differential equations can be built based on this class E condition and be solved. For the load other than the optimal value, class E condition is not valid and equations can not be built based on this class E condition.



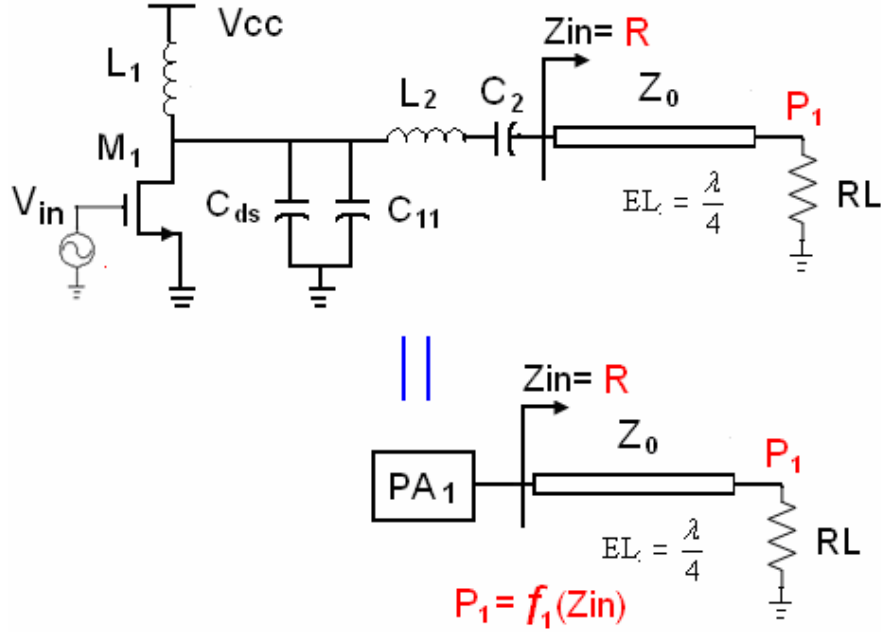


Fig. 4.22 Illustration of the assumption for one single stage class E PA.

### Equivalent circuit for the combining structure with nonidealities

As been discussed before the equivalent circuit shown in Fig. 4.23a is used to design the  $N$ -device combining structure. For each PA block in this original equivalent circuit the output power is assumed to be given by

$$P_j = f_j(R_j) \quad (4.28)$$

( $j \in [1, 2, \dots, N]$ ,  $N$  is an arbitrary positive integer).

It's assumed that the amplitude nonidealities only happen in the PA blocks,  $PA_1 - PA_K$ , of the combining structure, where the power output function changes from  $f_m(x)$  to  $f'_m(x)$  ( $m \in [1, 2, \dots, K]$ ,  $K$  is an arbitrary positive integer smaller than  $N$ ). Therefore the output power of the PA blocks,  $PA_1 - PA_K$ , is not  $P_m = f_m(R_m)$  as given by (4.28) anymore but  $P_m = f'_m(R_m)$  though the PA blocks still see the optimal load  $R_m$ . As a result, the output voltage  $V_m$  of the PA blocks,  $PA_1 - PA_K$ , are not equal to  $V_T$  shown in Fig. 4.23b and the equivalent circuit is not valid for the analysis of the combining structure ( $m \in [1, 2, \dots, K]$ ,  $K$  is an arbitrary positive integer smaller than  $N$ ).

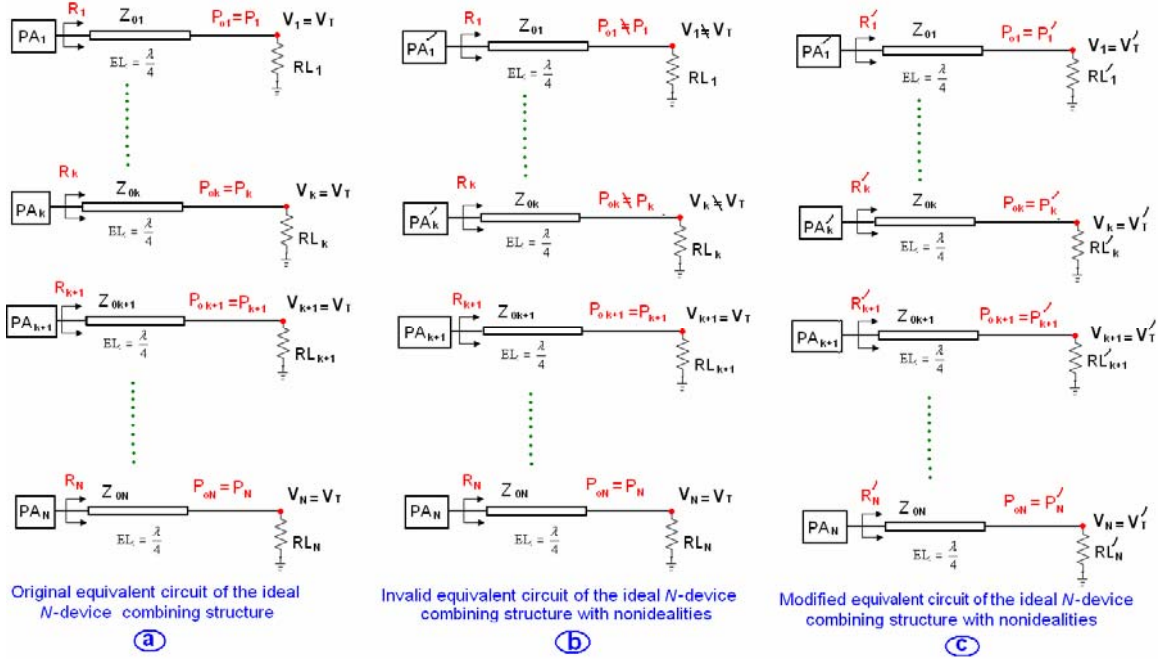


Fig. 4.23 Original and the modified equivalent circuit of the combining structure.

A new equivalent circuit shown in Fig. 4.23c is needed to analyze the combining structure with amplitude nonidealities, where the loads change from  $RL_j$  to  $RL'_j$  so that the voltages  $V'_j$  at the output nodes are equal again, which is given by

$$V_1 = V_2 = \dots = V_N = V_T' \quad (4.29)$$

As a result, the load each PA block sees changes from  $R_j$  to  $R'_j$  ( $j \in [1, 2, \dots, N]$ ,  $N$  is an arbitrary positive integer) while the new loads  $RL'_j$  still satisfy

$$RL'_1 // \dots // RL'_k // \dots // RL'_N = RL \quad (4.30)$$

once the new loads  $RL'_j$  are calculated the new equivalent circuit can be build for the analysis of the combining structure with amplitude nonidealities.

### Equations for the new loads $RL'_j$

For the PA blocks with nonidealities,  $PA_1 - PA_K$ , the power output are given by

$$P_m' = f_m'(R_m') \quad (4.31)$$

$$\Rightarrow P_m' = f_m'(R_m') = f_m'\left(\frac{Z_{0m}^2}{RL_m'}\right) = \frac{V_m^2}{2RL_m'} = \frac{V_T'^2}{2RL_m'} \quad (4.32)$$

For the combining structure with nonidealities the new combined power out  $P_T'$  is given by

$$P_T' = \frac{V_T'^2}{2RL} \quad (4.33)$$

Substituting (4.33) in (4.32) yields

$$P_m' = f_m' \left( \frac{Z_{0m}^2}{RL_m'} \right) = \frac{P_T' \times RL}{RL_m'} \quad (4.34)$$

$$\Leftrightarrow RL_m' = g_m(P_T')$$

( $p \in [1, 2, \dots, K]$ ,  $K$  is an arbitrary positive integer smaller than  $N$ )

Therefore, the new loads in the PA blocks,  $PA_1 - PA_K$ , with amplitude nonidealities are represented as a function of the combined power  $P_T'$ .

Similar results can be obtained for the new loads in the PA blocks without amplitude nonidealities,  $PA_{K+1} - PA_N$ , which are given by

$$RL_n' = g_n(P_T') \quad (4.35)$$

( $n \in [K+1, K+2, \dots, N]$ ,  $K$  is an arbitrary positive integer smaller than  $N$ ).

Substituting (4.34) in (4.33) into (4.30) yields

$$g_1(P_T') // g_2(P_T') // \dots // g_N(P_T') = RL \quad (4.36)$$

By solving (4.36) the power output  $P_T'$  of the combining structure with amplitude nonidealities can be achieved. Substituting the solved value of  $P_T'$  into (4.34) and (4.35) the loads for the modified equivalent circuit of the operating ideal combining structure with amplitude nonidealities shown in Fig. 4.23c are also obtained. As a result the influence of the amplitude nonidealities on the combining structure can be predicted by analyzing the modified equivalent circuit. Yet the key factor of building the modified equivalent circuit is the power-load function (4.28), which is not available so far<sup>6</sup>. One numeric method to obtain the approximate power-load function  $f_1(R)$  is curve fitting. After sweeping the load of a PA the curve fitting of the simulation result can be used to

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<sup>6</sup> Although this mathematical function is not available in a closed-form, it can be approximated by curve fitting the simulation result or load-pull result.

find the power-load function  $f_1(R)$ .

#### 4.3.4 Example of the amplitude difference nonidealities

After the general analysis of the combining structure with amplitude nonidealities, one special example of the amplitude nonidealities is discussed.

In the  $N$ -device balanced combining structure shown in Fig. 4.24a the PA blocks,  $PA_1 - PA_K$ , are disabled denoted by the check (e.g. due to transistor breakdown or for power control application). The highly symmetric property of the balanced combining structure provides additional conditions and enables the analysis relatively easier.

##### The modified equivalent circuit

Since it is a balanced combining structure the transmission lines and PA blocks in each branch are identical and the following conditions are given:

1. The characteristic impedance of the quarter-wavelength transmission lines is given by

$$Z_{01} = Z_{02} = \dots Z_{0n} = Z_0 \quad (4.37)$$

2. The impedance  $Z_{off}$  contributed to output node AA by the shut-off PA blocks is the same shown in Fig. 4.24a. The impedance  $Z_{off}$  is seen by looking into each shut-off PA block at the output node AA of the combining structure, which is given by

$$Z_{off} = \frac{Z_0^2}{Z_{PA}} \quad (4.38)$$

, where  $Z_{PA}$  is the equivalent impedance seen by the transmission line looking into the shut-off PA block.

Thus the total impedance  $Z_{Toff}$  contributed by shut-off PA blocks,  $PA_1 - PA_K$ , shown in Fig. 4.24a and Fig. 4.24b is  $K$  pieces of  $Z_{off}$  in parallel and given by

$$Z_{Toff} = \frac{Z_{off}}{K} = \frac{Z_0^2}{K \times Z_{PA}} \quad (4.39)$$

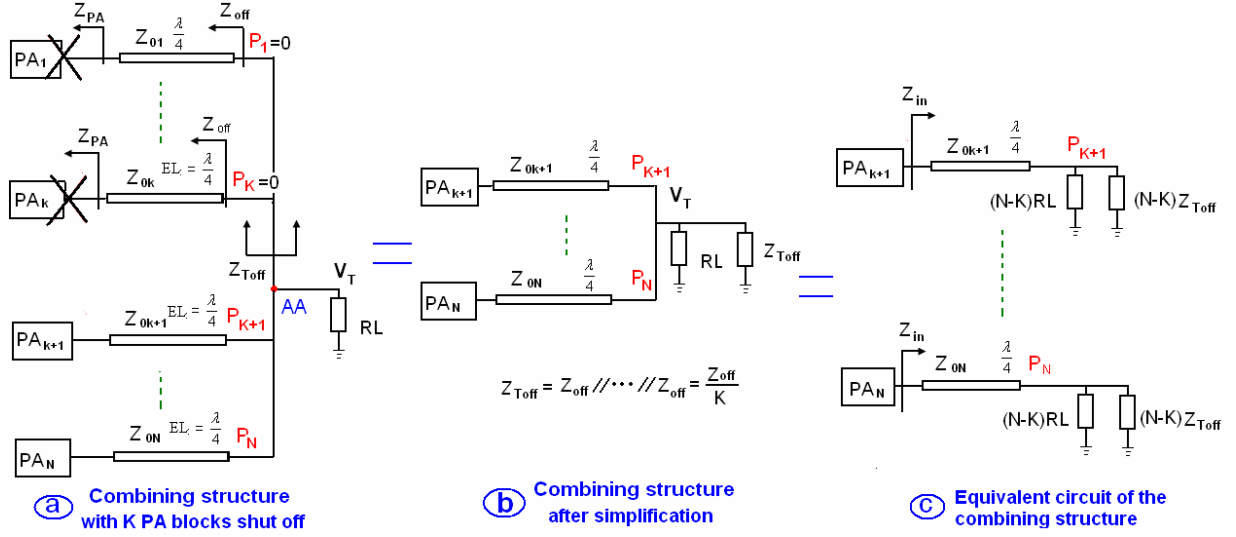


Fig. 4.24 The  $N$ -device balanced combining structure with  $K$  PA blocks shut-off

The total impedance  $Z_{Toff}$  contributed by the shut-off PA blocks,  $PA_1 - PA_K$ , in parallel with the load  $RL$  forms the new load for the changed combining structure shown in Fig. 4.24b, where only PA blocks,  $PA_{K+1} - PA_N$ , are working. The equivalent circuit for the changed combining structure in Fig. 4.24b consists of  $(N-K)$  identical single stage PAs shown in Fig. 4.24c. For any PA block in the equivalent circuit shown in Fig. 4.24c the new load it sees is given by

$$Z_{in} = \frac{Z_0^2}{[(N-K) \times RL] // [(N-K) \times Z_{Toff}]} = \frac{Z_0^2}{(N-K) \times RL \times Z_{Toff} / (RL + Z_{Toff})} \quad (4.40)$$

$$= \frac{Z_0^2}{(N-K) \times RL} \times \left(1 + \frac{RL}{Z_{Toff}}\right)$$

Substituting (4.39) into (4.40) yields

$$Z_{in} = \frac{Z_0^2}{(N-K) \times RL} \times \left(1 + \frac{RL}{Z_0^2} \times K \times Z_{PA}\right) = \frac{Z_0^2}{(N-K) \times RL} + \frac{K \times Z_{PA}}{(N-K)} \quad (4.41)$$

Therefore, the modified equivalent circuit for the balanced combining structure with PA blocks shut-off is built as shown in Fig. 4.25b.

### The effect caused to the combining by the shut-off PA blocks

Compared with the ideal balanced combining structure shown in Fig. 4.25a, the load  $Z_{in}$  each of the PA blocks,  $PA_{K+1}-PA_N$ , sees is different than the optimal load  $R$  shown in Fig. 4.25a. The optimal load  $R$  is given by

$$R = \frac{Z_0^2}{N \times RL} \quad (4.42)$$

As a result, the PA blocks are not working under the optimal class E mode.

As discussed in the appendix 4.8 the load seen by the transmission line looking into the shut-off PA block  $Z_{PA}$  varies and is dependent on how the PA block is shut-off, which makes the calculation of  $Z_{in}$  more complex. When some control circuits such as parallel

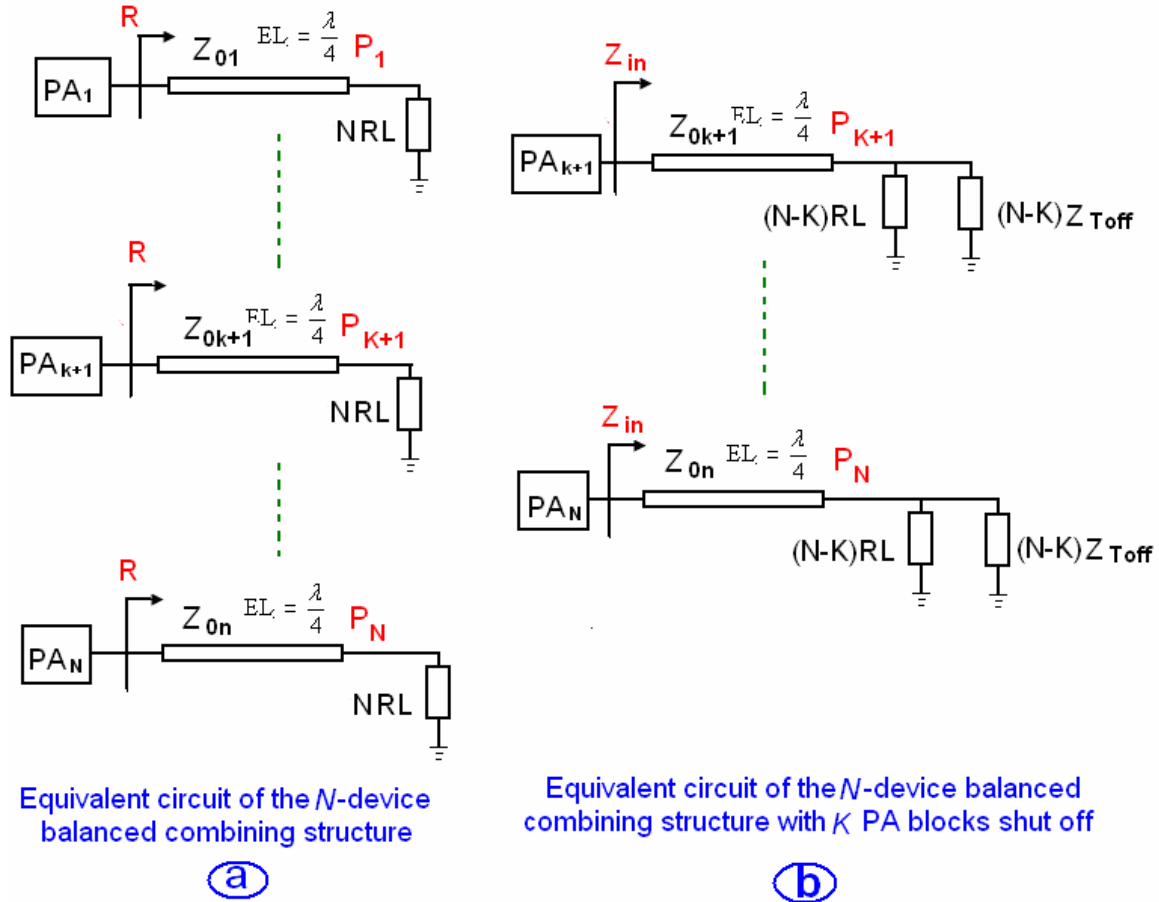


Fig. 4.25 Comparison between the equivalent circuits of the original combining structure and the one with shut-off PA blocks.

PMOS transistor short the shut-off PA block,  $Z_{pA}$  can be approximated to be zero and the load  $Z_{in}$  is simplified to a real load given by

$$Z_{in} = \frac{Z_0^2}{(N-K) \times RL} \quad (4.43)$$

which is  $\frac{N}{N-K}$  times larger than the optimal load  $R$  given in (4.42).

Due to the reason mentioned in section 4.3.3 that the power-load function is not available the power performance of the PA blocks,  $PA_{K+1}-PA_N$ , still can not be calculated even knowing (4.43). However, based on the observation of large amount of simulation results it's reasonable to say that PA blocks  $PA_{K+1}-PA_N$ , which see  $\frac{N}{N-K}$  times larger load than the optimal load, will deliver lower output power and lower drain efficiency than in

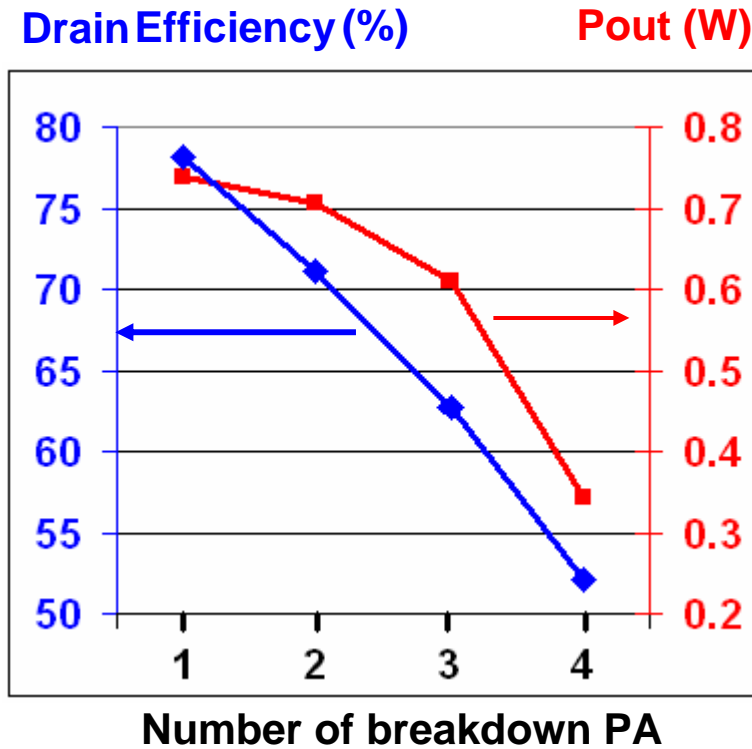


Fig. 4.25 Transistor breakdown effect on the working class E PA in a four-device balanced combining network.

the ideal balanced combining structure. A balanced combining network with four class E PAs is simulated in ADS to show the transistor breakdown effect on the other working PA blocks. It's shown in Fig. 4.25 that as more PAs broken-down the drain efficiency and the out power decrease due to the increasing load they see.

Although the conclusion above-stated is for the balanced combining network a similar conclusion should be true for the unbalanced combining network. However, it can not be obtained by closed-form formula derivation since the closed-form of function (4.27) is unknown, as mentioned in section 4.3.3.

### **Possible solution**

For the balanced combining network the quarter-wavelength transmission line network is designed in such a way that the load impedance  $Z_{in}$  each PA block sees is their optimal value  $R$ . At this condition where the class E condition is satisfied the drain efficiency  $\eta = \frac{P_{out}}{P_{DC}}$  is at the maximum but the output power and PAE may not be their maximal value). As the number of the short-circuit transistors (the breakdown transistors or the disabled transistors in the power control application) increases, the load impedance  $Z_{in}$  for each PA block increases and the power output, PAE and drain efficiency all decreases.

To keep the overall efficiency of the combining network from decreasing as the number of the short-circuit transistors increase, the combining network can be designed at the beginning in such a way that the load impedance  $Z_{in}$  is lower than  $R$ , say,  $\frac{R}{N}$  ( $N > 1$ ).

Thus, when the number of the short-circuit transistors increase, the load impedance  $Z_{in}$  increases from  $\frac{R}{N}$  but may still be smaller than  $R$ . Assuming the power input  $P_{in}$  is appropriate to  $f \times C_{in} \times V_{dd}^2$  it will not change. For  $PAE = \eta_{drain} - \frac{P_m}{P_{DC}}$ , at this time compared to the class E condition  $\eta_{drain}$  is smaller  $P_{DC}$  is larger and PAE may only slight smaller. This solution shows more interest for the people who are concern more of PAE than  $\eta_{drain}$ .

To further investigate this topic some knowledge should be clear at first:



1. Power-load function in (4.27) so that the power output  $P_{out}$  and DC input  $P_{DC}$  can be calculated when the load impedance  $Z_{in}$  is not the optimal value  $R$ .
2. The driving stage is known so that the  $P_{in}$  and PAE can be calculated.

## 4.4 Non-resistive antenna nonidealities

Ideally the antenna which the power is delivered to is assumed to be a resistive load. This assumption enables the analysis much easier as presented in the previous section. The design equations of the quarter-wavelength transmission line combining structure are derived based on this resistive antenna assumption<sup>7</sup>. When the antenna is not purely resistive the nonidealities will happen. For the simplicity of the analysis, the non-resistive antenna is represented by its resistive part in parallel with a reactive part. The situation is divided into two cases, namely, small reactive part in parallel, large reactive part in parallel.

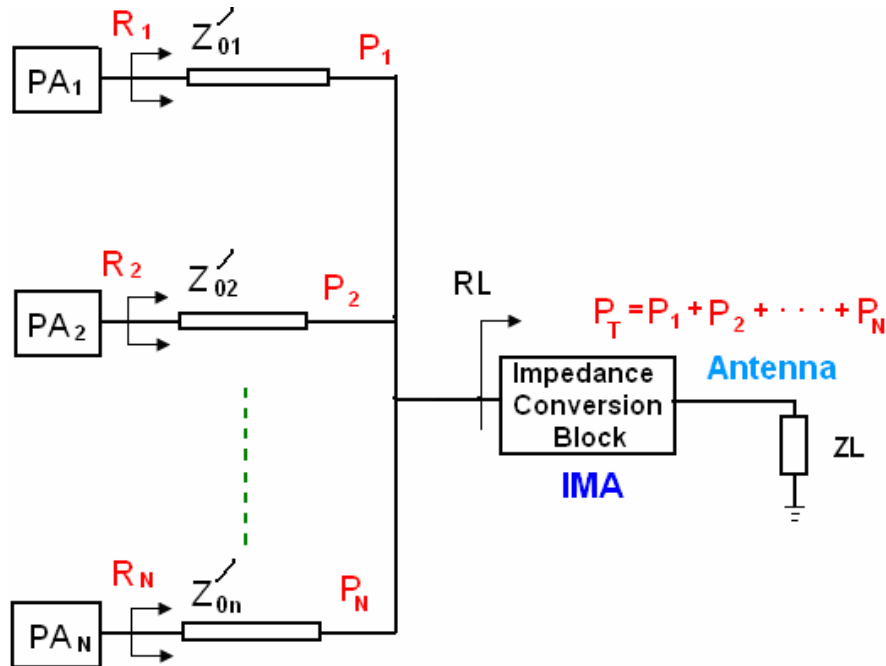


Fig. 4.26 Schematic of the combining structure where the antenna has reactance

### 4.4.1 Antenna with small reactive part in parallel

If the antenna has a relatively small reactance in parallel with the resistive part there are two options to use this combining structure.

1. Use one additional impedance matching block *IMA* to convert the reactive load of the antenna to a resistive  $RL$  shown in Fig. 4.26 and (3.30) can still be used to design the quarter-wavelength transmission line combining structure.

<sup>7</sup> The quarter-wavelength transmission line can not match a non-real load to a resistive impedance [2.17].

2. Chose another impedance matching technique for this combining structure which can convert the reactive load of the antenna to the optimal resistive load  $R_j$  that PA block wants to see. Then derive the new design equations based on the new impedance matching technique. This will not be included in this work.

#### 4.4.2 Antenna with large reactive part in parallel

In case the reactance in parallel is considerably large compared to the real part, the quarter-wavelength transmission line combining structure might be still used. Fig. 4.27a illustrates the combining structure designed by (3.27) and (3.30) for the real load antenna  $RL$ . The equivalent circuit of the ideal combining structure is shown in Fig. 4.27b. The same combining structure with a non-real antenna is shown in Fig. 4.27c with its equivalent circuit shown in Fig. 4.27d. The equivalent circuit shown in Fig. 4.27b is built based on (3.27) and (3.30) to analyze the combining structure shown in Fig. 4.27a and the loads  $RL_j$  is given by

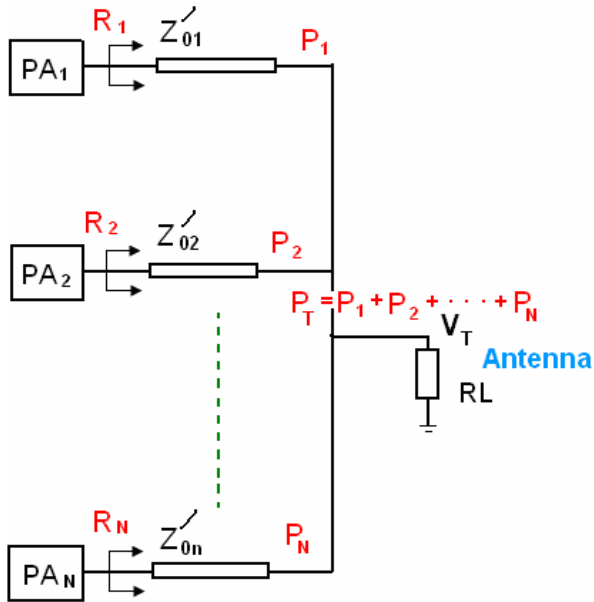
$$RL_j = \frac{RL \times P_T}{P_j} = K_j \times RL \quad (4.44)$$

where  $P_T$  is the ideal combined power;  $P_j$  is the ideal power output of PA block  $PA_j$ . For the equivalent circuit shown in Fig. 4.27d of the combining structure with non-real load antenna shown in Fig. 4.27c, firstly it's assumed the multiplication factor  $K_j$  in (4.44) still holds for  $XL_j$ , which is given by

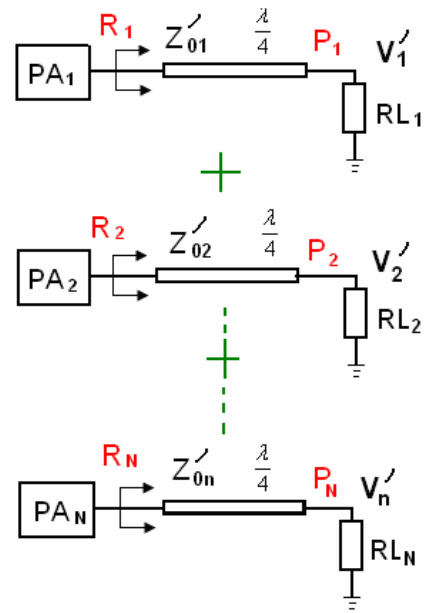
$$XL_j = K_j \times XL = \frac{P_T}{P_j} \times XL \quad (4.45)$$

Thus as shown in Fig. 4.27d the load each PA block sees in the equivalent circuit for the non-real load combining structure is given by

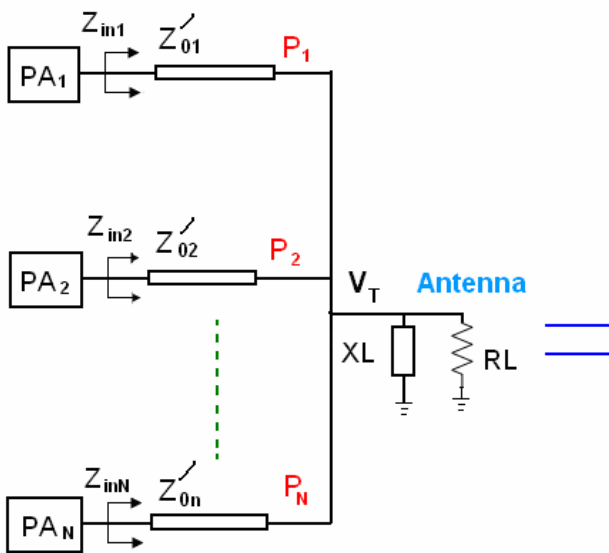
$$\begin{aligned} Z_{inj} &= \frac{Z_{0j}^2}{RL_j // jXL_j} = \frac{Z_{0j}^2}{K_j \times RL_j // K_j \times jXL_j} \\ &= \frac{Z_{0j}^2}{N \times RL} \times \left( \frac{RL}{jXL} + 1 \right) \end{aligned} \quad (4.46)$$



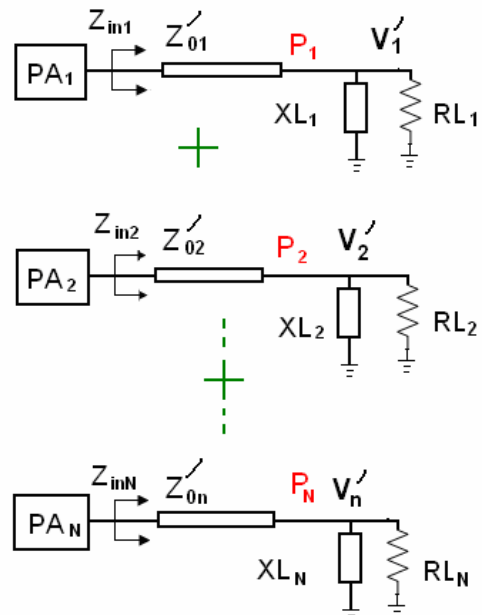
(a) Ideal combining structure with real load antenna



(b) Equivalent circuit of the combining structure with real load antenna



(c) Combining structure with the antenna having small reactance



(d) Equivalent circuit of the combining structure with the antenna having small reactance

Fig. 4.27 Comparisons between the real-load-antenna combining structure and non-real-load-antenna combining structure.

Note that as shown in Fig. 4.27a and Fig. 4.27b the optimal load each PA block is expected to see is given by

$$R_j = \frac{Z_{0j}^2}{N \times RL} \quad (4.47)$$

Comparing (4.46) and (4.47) tells that:

1. When the reactance  $XL$  in parallel is relatively larger than the real antenna  $RL$ ,  $Z_{inj}$  is very close to the optimal load  $R_j$  each PA block is expected to see and the effect caused by the reactance to the combining structure can be neglected.
2. When the reactance  $XL$  in parallel is relatively smaller than the real antenna  $RL$ , each PA block in the combining structure sees  $Z_{inj}$  different than it's expected. As a result, the output voltage  $V_j'$  shown in Fig. 4.27d are not equal both in phase and amplitude and this equivalent circuit based on (3.27) and (3.30) is not valid any more, which is the effect of both phase nonidealities and amplitude nonidealities.

Though the conclusion can be drawn from above-stated analysis that the reactive antenna has not big effect on the combining network, we still couldn't release ourselves yet. In reality not only the antenna has a reactive part, but it also varies with the time and the neighbor environment. Further work has to be done to get a complete analysis

## 4.5 Summary

When either of the three assumptions for the combining technique is not satisfied nonidealities will happen to the combining structure. In this chapter three kinds of nonidealities for the  $N$ -device combining structure are discussed, namely phase nonidealities, amplitude nonidealities and non-resistive antenna. The phase nonidealities are the issues which need to take care of before the design. The major source of the phase nonidealities is the PA block, which can be checked by the value of  $\beta$ . Several methods to mitigate the effect of the phase nonidealities on the combining structure have been discussed such as choosing the transistor for each PA block with small  $\beta$  difference or introducing additional phase compensation block. In the balanced combining structure the PA block will not introduce phase difference. On the contrary the amplitude nonidealities mostly come externally when the ideal combining structure is operating. The effect on the combining structure can be analyzed numerically. The analysis and design equations of the combining technique are based on the real-antenna assumption. When the reactive in parallel with the resistive part of the antenna is relatively large the combining structure is still valid. When the reactive in parallel is relatively small, additional impedance converting network is needed for the combining network.

## Chapter 5

### The implementation of the microstrip combining network

#### 5.1 Introduction

Microstrip is particularly useful to implement transmission lines in distributed circuit designs at frequencies from below 1 GHz through some tens of GHz [5.1]. It can be fabricated by photolithographic processes and is easily integrated with other passive and active microwave devices. To realize the quarter-wavelength transmission line for the proposed power combining network the microstrip has been used in this work. The major issues are the effect on the transmission lines caused by discontinuities in the microstrip implementation. Considerations on the microstrip implementation will be discussed at first, namely, substrate choice, layout choice and measurement. To shows the measures taken to reduce the discontinuities, in the end a design example of the quarter-wavelength microstrip combining network for three unidentical class E PAs will present an overview of the microstrip implementation.

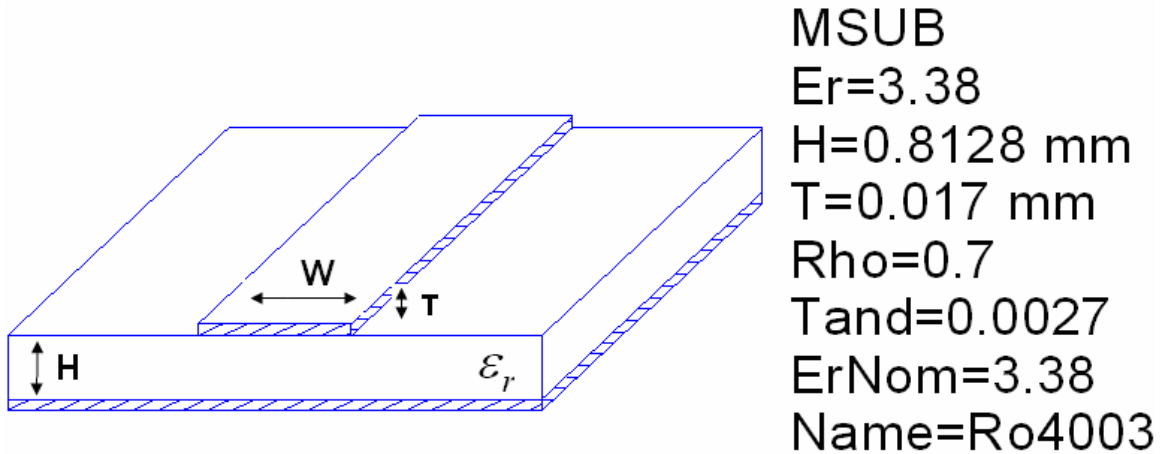


Fig. 5.1 Geometry illustration of a microstrip line.

## 5.2 Choice of the microstrip

The geometry of a microstrip line is shown in Fig. 5.1. A conductor of width  $W$  and thickness  $T$  is printed on a thin, grounded dielectric substrate of thickness  $H$  and relative permittivity  $\epsilon_r$ . The most important dimensional parameters are the microstrip width  $W$  and the height of the substrate  $H$ . Also of great importance is the relative permittivity of the substrate,  $\epsilon_r$ . In RF and microwave applications the thickness of the metal strip  $T$  is generally of much less importance [5.1].

Although the abrupt dielectric interfaces between the substrate and the air above it do not allow pure TEM mode field, the energy transmitting along the microstrip has quasi-TEM field distribution. Therefore, good approximations can be obtained by using several design formulas [2.17].

Before the microstrip design several choices need to be determined, namely, the substrate material, the layout topology of the microstrip lines and the fabrication process. This section discusses these issues respectively.

### 5.2.1 Choice of the substrate material

A PCB substrate provides the following options for designer to choose shown in Fig. 5.1.

1. Substrate material dielectric constant  $\epsilon_r$ .
2. Substrate thickness  $H$ .
3. Metal foil thickness  $T$ .

Although the microstrip line has very low loss it's always of interest to lower the loss as much as possible. Since the power efficiency is critical for the combining network the attenuation of the microstrip determines the choice of the substrate material in this work.

The attenuation model of the microstrip has been build and the detailed analysis is given in the appendix 5.1. The following guidelines have been obtained for choosing the PCB material:

- Substrate material with low dielectric constant  $\epsilon_r$
- High substrate thickness  $H$ .
- Thin Metal foil thickness  $T$ .



## 5.2.2 Choice of microstrip trace topologies

In the theoretical analysis the quarter-wavelength transmission lines are connected directly at their terminals to the load by perfect wires shown in Fig. 5.2a. On PCB inevitable discontinuities at bends, adjacent microstrip, and junctions can cause degradation in circuit performance. This is because such discontinuities introduce parasitic reactance that can lead to phase and amplitude errors, input and output mismatch, and crosstalk coupling. As a result, the three major discontinuities of microstrip layout are

1. Bend discontinuities
2. Crosstalk discontinuities
3. Junction discontinuities

Their influence must be taken into account in the design of the microstrip combining network. Fig. 5.2 takes an example of a 3-device balanced combining network to illustrate the PCB discontinuities. Fig. 5.2b and Fig. 5.2c show two layout topologies for the combining network shown in Fig. 5.2a.

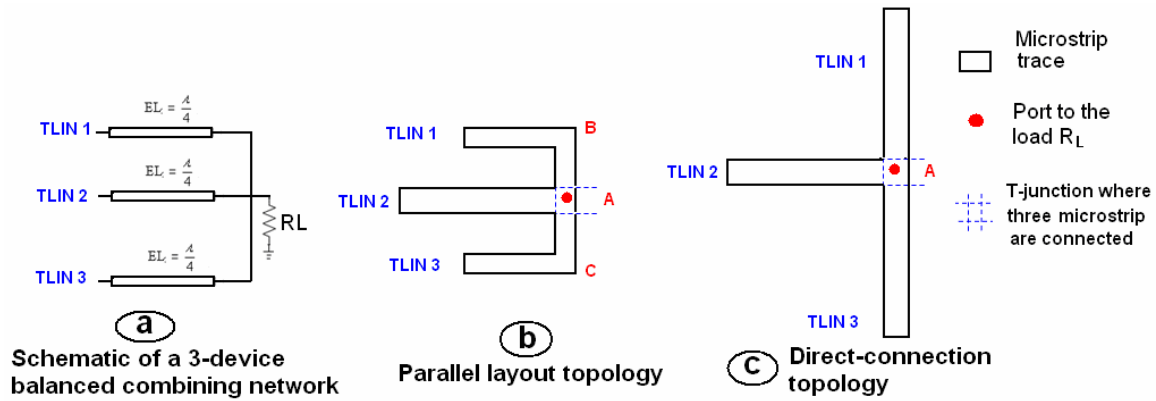


Fig. 5.2 The schematic of layout topologies of a 3-device balanced combining network.

Three major discontinuities involved are listed:

1. Bends at region B and C in Fig. 5.4b. In the parallel layout shown in Fig. 5.4b the microstrip  $TLIN1$  and  $TLIN2$  are bended to save the dimension area of the board. Thus, compared with the direct-connection topology the additional discontinuities at bending region B and C are introduced. Besides that, the crosstalk coupling between  $TLIN1$ ,  $TLIN2$  and  $TLIN3$  are severer.

2. Crosstalk between  $TLIN1$ ,  $TLIN2$  and  $TLIN3$  especially in the parallel layout topology shown in Fig. 5.4b.
3. T-junction A in both topologies. The microstrip component “T junction” has to be used to connect three microstrip traces to the load port.

Measures have to be taken to minimize the effect of the discontinuities on the combining network. Detailed analysis about the discontinuities has been made, which is given in the appendix 5.2, and resulted in the following measures to reduce the discontinuities:

1. **Bend compensation.** As shown in Fig. 5.3 when the straight microstrip line has been bended, the mitered-bend and curve bend layout can compensate the parasitic capacitance of the right-angle bend shown in Fig. 5.3a.

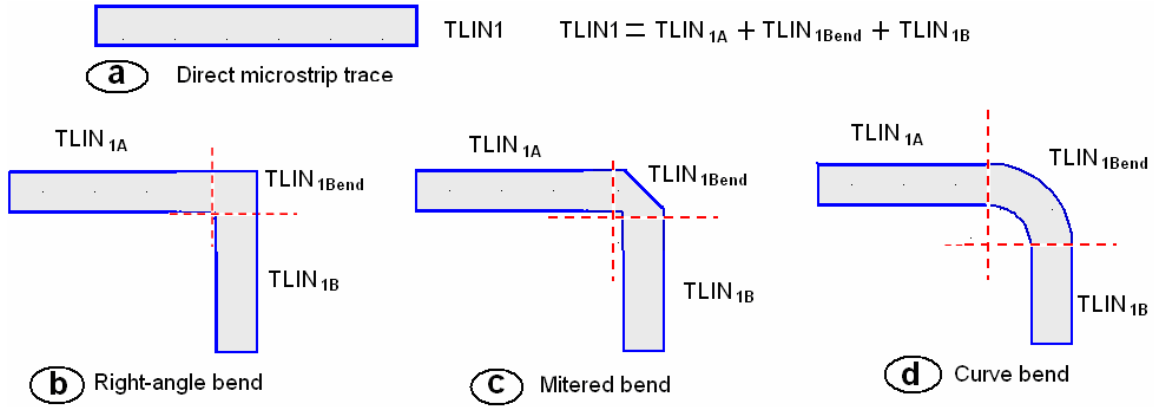


Fig. 5.3 Three kinds of bends of a microstrip trace.

2. **Crosstalk compensation.** When two parallel microstrip lines are very close to each other, the cross talk between them will affect their characteristic. For example,  $TLIN1$ ,  $TLIN2$  and  $TLIN3$  in Fig. 5.2b have crosstalk between each other. Actually the effect is similar to the even mode coupling and the effective characteristic impedance of  $TLIN1$ ,  $TLIN2$  and  $TLIN3$  in the combining network would increase. Due to the low coupling factor on PCB the crosstalk effect can be neglected, when the distance between two parallel lines is larger than 4mm. Adjusting the physical dimension of the microstrip lines can compensate the crosstalk effect to some extent.
3. **Overall physical tuning of the whole combining network.** In the microstrip combining network all the discontinuities have their own effects. These effects

interact with each other and an overall optimization at the final design is required. In the design example presented in section 5.3 ADS has been used at the final design stage to adjust all the physical dimension of the overall combining network. The overall performance of the microstrip combining network is the only judgment to determine the optimal dimension parameters of the network. The smaller minimum line width of a fabrication process enables a higher physical tuning resolution and better optimization can be achieved.

### **5.3 Measurement of microstrip**

After the design of the microstrip combining network the last work is fabricating and measuring the combining network. As been discussed in chapter 4 any nonidealities involved in the quarter-wavelength transmission lines would introduce phase or amplitude nonidealities, which degrade the performance of the combining structure. In this work the quarter-wavelength transmission lines are implemented as the microstrip on PCB. How accurate the microstrip fabricated on PCB could be compared to its design value in the simulation tools is of interest in this chapter. While simulation tools allow helpful insights into predicting structure performance, more test and measurement tools are needed to measure and verify the actual parameters. Therefore, the measurements of the microstrip on PCB are useful to compare the actual parameter such as electrical length and characteristic impedance with the expected values. A few quarter-wavelength (at 2 GHz) microstrip lines with different characteristic impedance are designed and fabricated on RO4003C (0.0032" thickness and ½ OZ copper cladding) substrate by [5.3]. The electrical length and characteristic impedance of these microstrip lines are the measurement objectives.

In the original plan the task was divided into two steps:

1. Design and fabricate some microstrip line samples and measure the PCB fabrication error.
2. Integrate the fabrication error information into the final design of the microstrip combining network. Fabricate and measure the final microstrip combining network for PAs using discrete transistors.

The step 1 takes much longer time than it's expected due to lack of experience on this area at that moment and step 2 hasn't been done within the limited time. However, step 1 has been completed with decent results and quite a lot knowledge and experience about the microstrip line measuring have been gained. The detailed discussion on the microstrip measurement is given in the appendix 6. Only the final conclusions and results will be presented in this subsection.

#### **5.3.1 Methods of measurement and accuracy**

Two kinds of instruments are available in the lab to measure the microstrip:

1. TDR (Time domain reflectometer) measurement by the Agilent 86100A oscilloscope.
2. S-parameter measurement by the Agilent network analyzer 8510C.

TDR generates a step signal which propagates down the coaxial cable to the DUT (device under test). By monitoring the reflected voltage waves on the oscilloscope the discontinuities at each point along the DUT can be characterized. The network analyzer generates a small signal at each sampling frequency to get the S parameter of the DUT.

The theoretical models for the measurement accuracy of both instruments have been built and analyzed. It's found that

1. The minimum electrical length of the microstrip can be defined by the TDR is around 10 degree.
2. The minimum electrical length of the microstrip can be defined by the network analyzer is around 1 degree.

In summary the TDR is suitable for the characteristic impedance measurement and the network analyzer is suitable for the electrical length.

In practice the measurement accuracy is worse than what the theoretical model predicts. The following lists the major reasons:

1. The limited rising time and shooting time of the step signal in TDR degrades the measurement accuracy of the characteristic impedance. To test a longer microstrip line can reduce the error.
2. The discontinuities (e.g. parasitic capacitance and inductance) brought by the soldering not only degrade the accuracy of the electrical length measurement but also the impedance measurement.

It's very critical to maintain the measurement accuracy as high as possible so that the fabrication accuracy can be tested correctly. In case the fabrication error is less than the measurement error, what's been measured will be the measurement error rather than the fabrication error. In addition to the measurement accuracy modeling it's best to measure a precisely-defined microstrip standard after the calibration of the instruments. Only by doing this can the overall measurement error be quantized. However, there is no such microstrip standard available in the lab during the measurement of this work. As a result, the real fabrication error is less than or equal to the result we can measured.

### 5.3.2 Calibration and de-embedding

Every RF measurement needs calibration to remove the errors in the test setup before DUT is measured. The normal calibration procedure and calibration standards are for the coaxial DUT (DUT with coaxial ports). For non-coaxial DUT such as the microstrip line, first of all a test fixture, an additional setup, is required to interface the instrument with the microstrip line. A cheap way is to solder the SMA connector to the microstrip board. As a result, additional calibration is necessary to de-embed the effect of the test fixture in the measurement result. After comparisons a method called TRL calibration is suggested for de-embedding.

### 5.3.3 Measurement result

#### Characteristic impedance

Agilent 86100A oscilloscope is used to conduct the TDR measurement for the microstrip lines' characteristic impedance and the measurement results are listed in Table 6.1. It can be concluded that the average fabrication error in terms of the characteristic in less than 3%.

Table. 5.1 The measurement result of the characteristic impedance of the microstrip lines

Number label	Designed characteristic impedance (ohm)	Measured characteristic Impedance (ohm)	Deviation
D1	50	48.55	2.9%
C2	40	38.79	3.0%
B2	30	29.7	1.0%
C1	22.36	21.33	4.6%
B1	15	15.23	1.5%

#### Electrical length

After the S parameter's been obtained it needs to be interpreted into the parameter "electrical length". A method using the periodic characteristics of the S parameter in the measurement frequency range is proposed.

Due to the lack of knowledge of the test fixture in the first-round microstrip lines measurement TRL calibration hasn't been taken into consideration. Nevertheless, if only analyze the period of  $dB(S_{11})$ ,  $dB(S_{21})$  and  $phase(S_{21})$ , it's reasonable to say that the electrical length of the microstrip lines is quarter-wavelength.

## 5.5 Design example

In this section the microstrip combining network on RO4300C is designed to combine the output power of three unidentical class E PAs, namely, PA1 PA2 and PA3 as shown in Fig. 5.4. Since the major purpose of this chapter is to show the performance of the

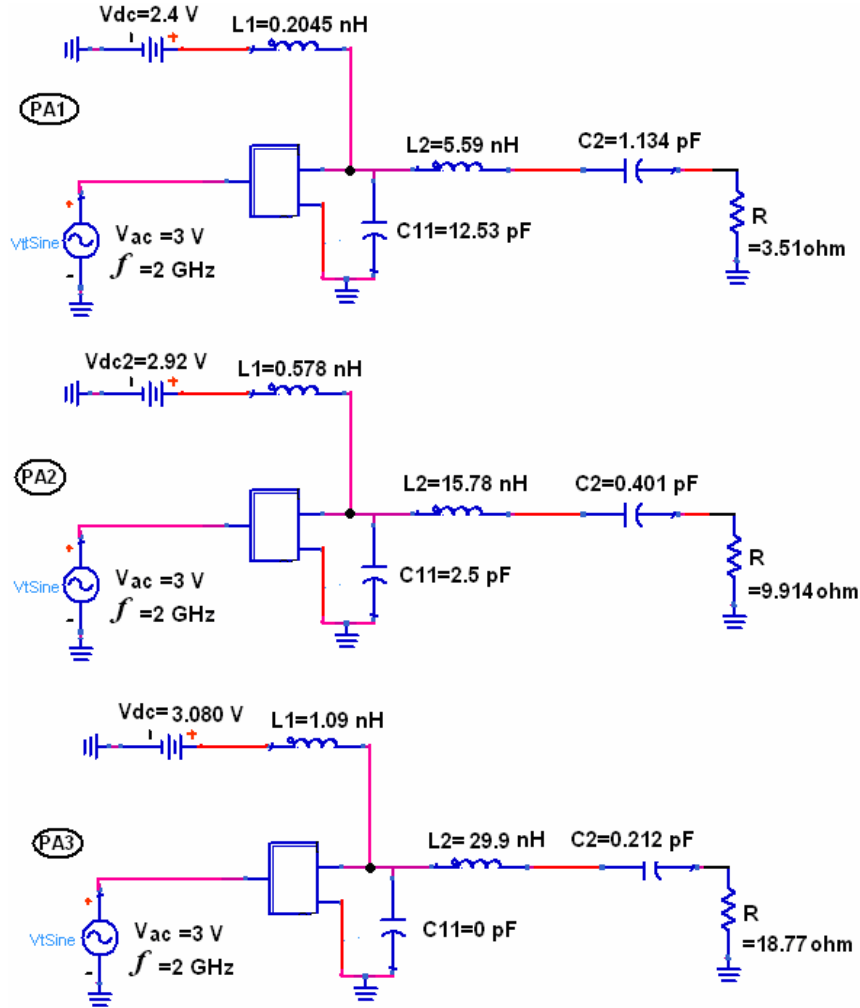


Fig. 5.4 Schematic of three unidentical class E PAs to be combined.

quarter-wavelength microstrip combining network on PCB it's better to minimize the error attributed by other elements except the combining network. Therefore, the inductors and capacitances in the PA block are ideal and an ideal sinusoid voltage source is used for the input single instead of using any driving stage circuit. The CMOS18 MOSFET model used in chapter 3 can not be supported in ADS, thus Agilent ATF501P8 MESFET transistor die model is used to build the PA. The working frequency is 2 GHz. The power performance and the circuit parameter of these three single PAs are listed in Table 5.2.



Table 5.2 Design value of three single stage class E PAs to be combined

PA Name	Vcc (V)	f (GHz)	C11 (pF)	C2 (pF)	L1 (nH)	L2 (nH)	R (ohm)	Pout (W)	Drain Efficiency
PA1	2.4	2	12.5	1.134	0.205	5.59	3.51	1.505	73.3%
PA2	2.92		2.5	0.401	0.578	15.78	9.91	0.985	70.8%
PA3	3.08		0	0.212	1.09	29.9	18.77	0.576	58.9%

Based on the procedure discussed in Section 3.4 the 3-device unbalanced combining structure is designed using the data in Table 5.2 and the schematic is shown in Fig. 5.4, where three quarter-wavelength transmission lines within the dash-line block consist of the combining network. The tool “LineCalc” in ADS is used to design the physical dimension of the quarter-wavelength microstrip lines on Rogers4003C, which are denoted in Fig.5.5.

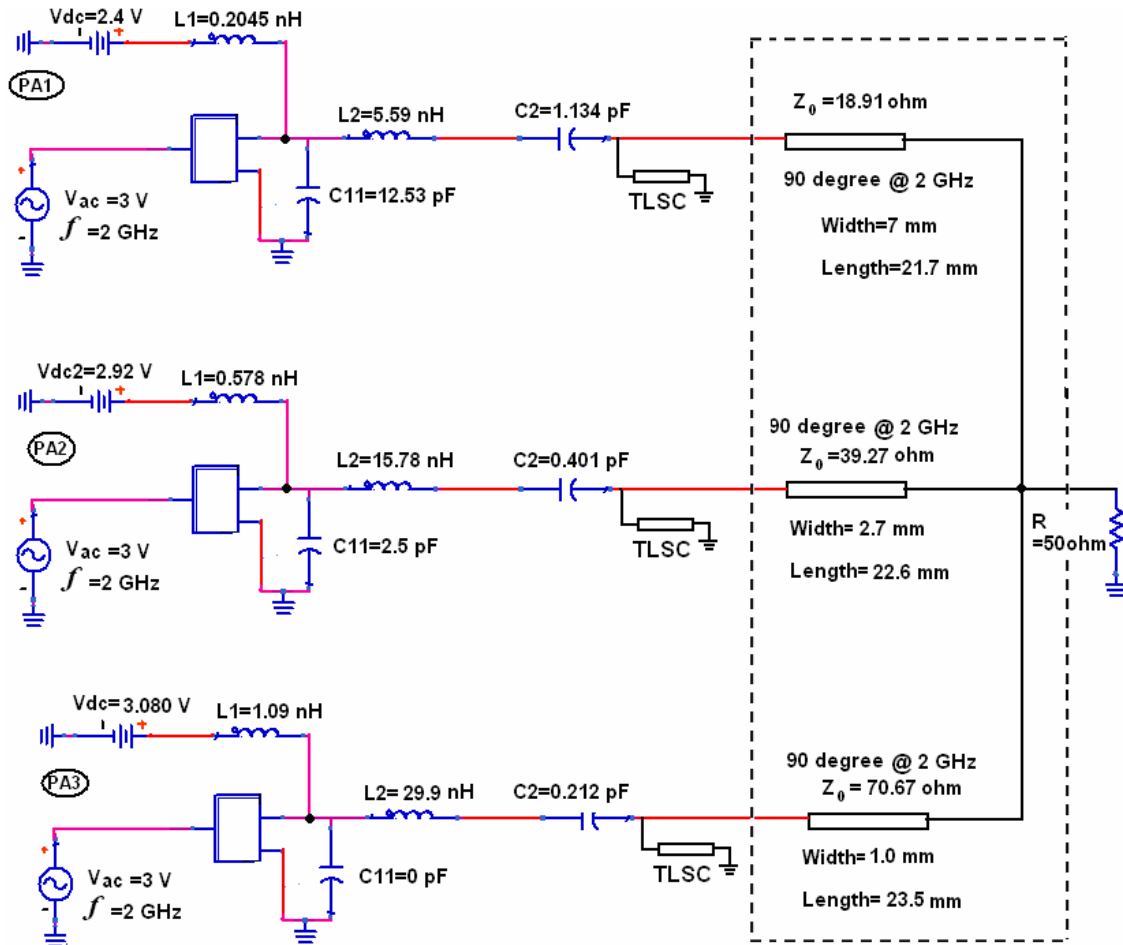


Fig. 5.5 Schematic of the 3-device unbalanced combining structure.

### Combining network topology design

The component “T junction” has to be used to connect TL1, TL2 and TL3 to the load shown in Fig. 5.6, where Port1, Port2 and Port3 are connected to PA1, PA2 and PA3 respectively; Port4 at the T-junction is connected to the load. As mentioned in the

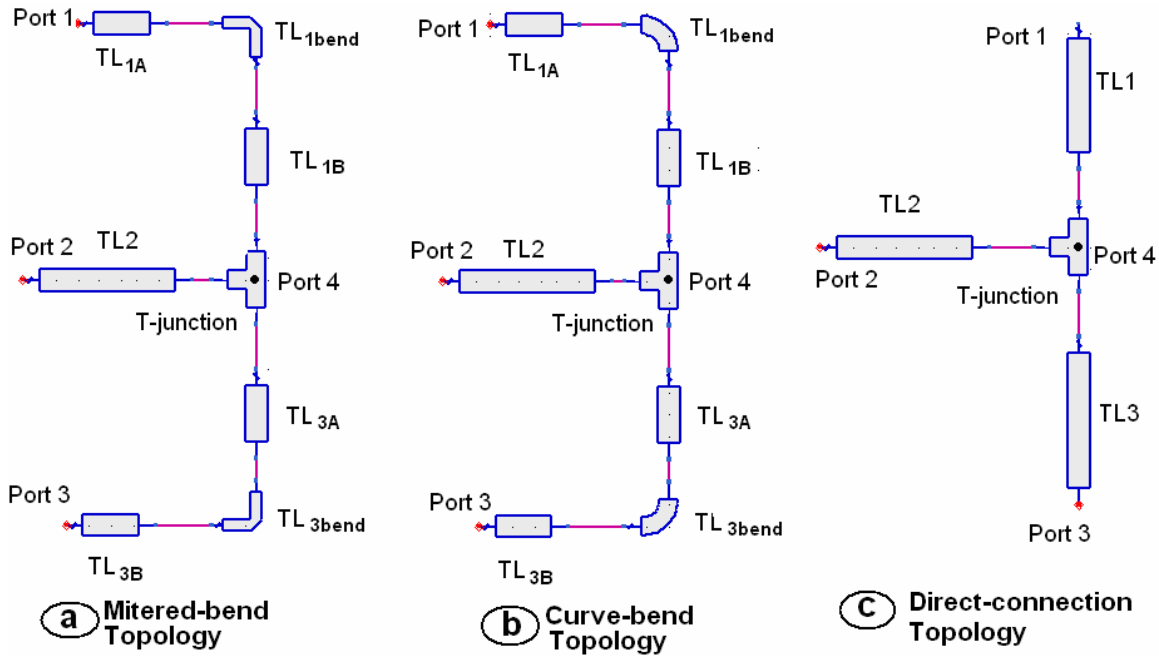


Fig. 5.6 Schematics of three different topologies of the microstrip combining network.

previous section there are three options for the topology as shown in Fig. 5.6:

1. Direct-connection topology. As shown in Fig. 5.6c three quarter-wavelength microstrip lines TL1, TL2 and TL3 are directly connected to the T junction. This topology has the lowest discontinuity, which is located in the T junction. It also has the lowest crosstalk effect. However, the board area of this topology is the biggest. Suppose the length of TL1, TL2 and TL3 are approximately  $L \text{ mm}$  and the total board area is around  $2L^2 \text{ mm}^2$ .
2. Bend topology. As shown in Fig. 5.6a and 5.5b the quarter-wavelength microstrip lines TL1 and TL3 are bended and connected with TL2 by T-junction. For

example, TL1 consists of two short microstrip lines  $TL_{1A}$  and  $TL_{1B}$  and a step  $TL_{1step}$ . To limit the discontinuities caused by the bend the mitered-bend and curve-bend are used. This topology option has more discontinuities such as crosstalk and bend than direct-connection topology but consumes less board area. Suppose the length of TL1, TL2 and TL3 are approximately  $L \text{ mm}$  and  $TL_{3A}$ ,  $TL_{3B}$ ,  $TL_{1A}$  and  $TL_{1B}$  are  $\frac{L}{2} \text{ mm}$ , the board area is  $L^2 \text{ mm}^2$ , which is half of the area of the direction-connection topology.

### Overall optimization of the combining network layout

Fig. 5.7 shows the layouts of the three topologies in Fig. 5.7 accordingly. The bend compensation is used to limit the discontinuities. In the final design all the physical parameters are open to tuning to get an overall optimum performance.

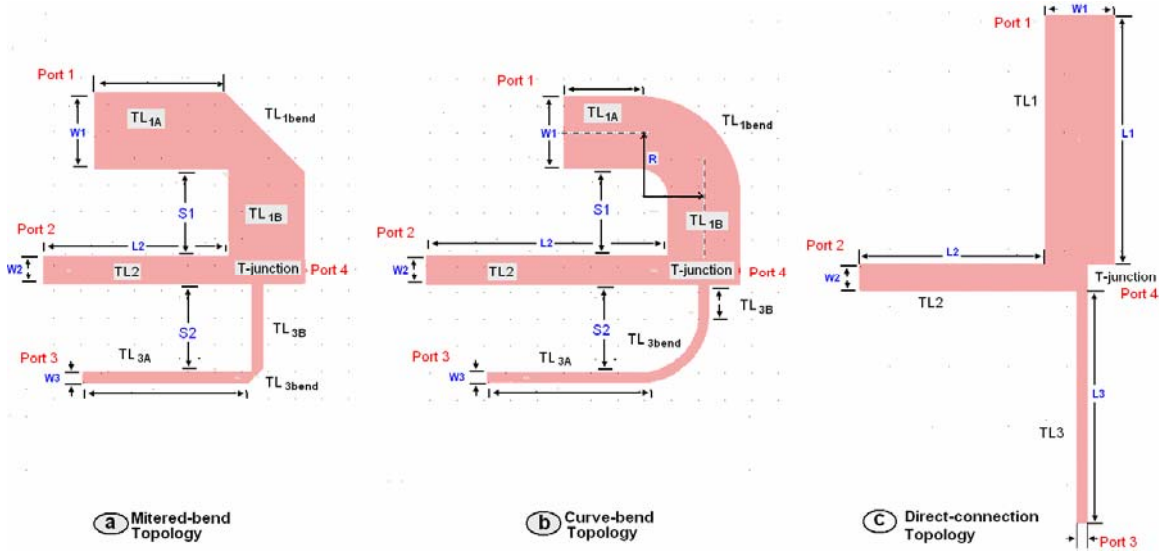


Fig. 5.7 Layouts of three different topologies of the microstrip combining network

For the direct-connection topology layout shown in Fig. 5.7c it's relatively easier for tuning since the six variables, namely,  $W1, W2, W3, L1, L2, L3$ , are not related. Changing any of them would not affect the value of others. For the mitered-bend layout shown in Fig. 5.7a some physical variables are related such as the parallel distance variables  $S1, S2$  with the length and width of  $TL_{1B}$ ,  $TL_{1A}$ ,  $TL_{3B}$  and  $TL_{3A}$ , which makes the tuning more

complex. Comparatively the curve-bend topology layout has the most variables to be tuned and involves the most complex tuning.

### Final design values and simulation results

To save the synthesis time<sup>1</sup> the variables  $S1$ ,  $S2$  for the two bend layouts are both set to 8 mm; the radius variable  $R$  of  $TL_{1bend}$  and  $TL_{3bend}$  in curve-bend layout are set equal. Table 5.3 lists the final physical parameters of the three topology layouts and Table 5.4 lists the simulation power performance of the 3-device unbalanced combining structure shown in Fig. 5.7 using these three topology layouts.

As can be seen in the column “Overall combining network” of Table 5.4 the microstrip combining network on RO4300C achieves the power combining very well. The efficiency of the combining network is above 98%. Note that the original design of the microstrip combining network and the expected power performance of each PA block are based on the ideal transmission lines. Due to the layout discontinuities each PA block in

Table 5.3 Physical parameters of the microstrip combining network with three different layouts.

Physical parameters names		TL1		TL2		TL3		S1 (mm)	S2 (mm)	R (mm)	Board area ( $mm^2$ )
		W1 (mm)	L1 (mm)	W2 (mm)	L2 (mm)	W3 (mm)	L3 (mm)				
Original design		7	21.7	2.7	22.6	1.0	23.5	None	None	None	None
After tuning	Mitered-bend	7.1	20.1	2.7	17.1	1.1	21.1	8	8	None	651
	Curve-bend	6.8	21.8	2.9	25.8	1	25.9	8	8	6	870

<sup>1</sup> The optimizer simulator in ADS2005A is used to tune the physical variables so that the impedances at Port1, Port2 and Port3 seen by PA1, PA2 and PA3 respectively are as close to the optimum as possible.

	Direction-connection	6.9	23.7	2.7	19.6	1.1	22.3	None	None	None	1290
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Table 5.4 Power performance of the combining structure for three layouts

Simulation result Names		PA1		PA2		PA3		Overall Combining system		$\eta_{combiningnetwork}$
		$P_{out}$ (W)	$\eta_{drain}$	$P_{out}$ (W)	$\eta_{drain}$	$P_{out}$ (W)	$\eta_{drain}$	$P_{out}$ (W)	$\eta_{drain}$	
Expected value		1.505	73.3%	0.98	70.8%	0.576	58.9%	3.06	70.3%	None
After tuning	Mitered- bend	1.346	75%	1.038	72.1%	0.579	59.3%	2.944	70.4%	99.3%
	Curve- bend	1.493	72.5%	1.02	73.6%	0.604	58.8%	3.062	69.3%	98.7%
	Direction- connection	1.483	74.7%	0.991	72.8%	0.602	60.4%	3.024	69.6%	98.3%

the real microstrip combining network don't perform exactly the same as the ideal case. This effect can be understood by comparing the impedance provided to each PA block by the microstrip combining networks in Fig. 5.7 at Port 1, Port 2 and Port 3. Table 5.5 lists the impedance provided by the microstrip combining networks and its ideal value. As can be seen, ideally the load provided by the combining network should be resistive, while the impedance provided by the microstrip combining networks has reactance and the real part is a little different from the expected.

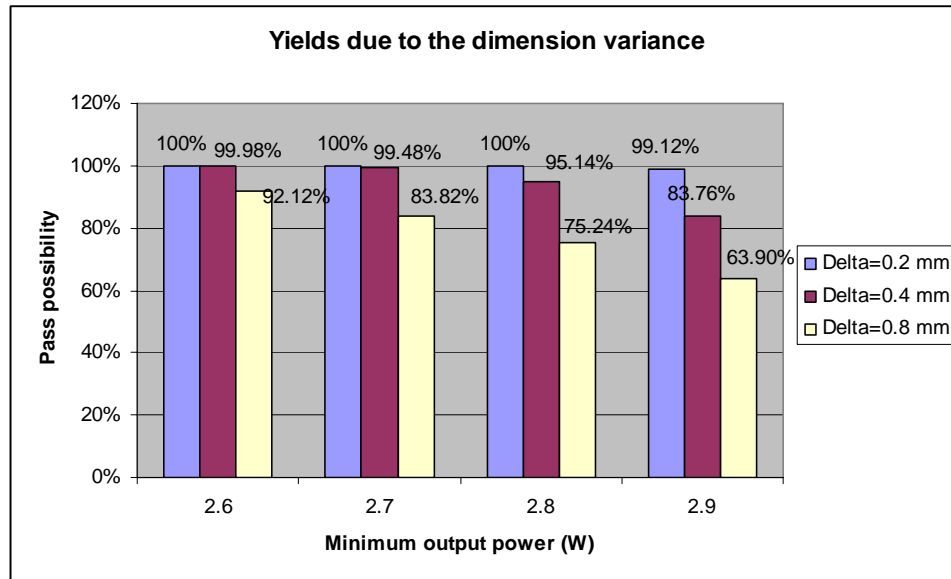
Table 5.5 The load provided to each PA block by the combining networks.

	$Z_{L1}$ (ohm)	$Z_{L2}$ (ohm)	$Z_{L3}$ (ohm)
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Expected value	3.51	9.91	18.77
Mitered-bend	3.78-j0.54	9.47+j0.16	19.51-j0.17
Curve-bend	3.66+j0.36	9.11-j1.15	18.76-j1.13
Direction-connection	3.59-j0.09	9.69-j0.81	18.53-j0.252

As predicted previously the mitered-bend layout consume half board area of the direct-connection layout. Due to the length increasing of  $TL1$  and  $TL2$  in the curve-bend layout the board area is larger than half of the direct-connection layout. Judged on the board area the mitered-bend layout is suggested for the quarter-wavelength microstrip combining network.

Finally a yield simulation<sup>2</sup> is conducted for the combining structure with mitered-bend layout. The effect of the dimensional parameters' variance on the combined power output can be shown. Suppose the dimensional parameters change uniformly with three variation values, namely, 0.2 mm, 0.4 mm and 0.8 mm. As shown in Fig. 5.8 the value of the bar is the possibility that the combined output meet the minimum output power specification. When the dimensional variance is 0.2 mm out of 5000 trials there are 99.12% trials where the combined power is still above 2.9 W. Note that the ideal expected power output is 3.06 W and the combined output without fabrication error is 2.944 W as shown



<sup>2</sup> The yield simulation has 5000 trials so that the prediction is as accurate as possible.

Fig. 5.8 Simulation results of the sensitivity on the combined power output due to dimensional variance.

in Table 5.4.

For a process where the minimum line width is 0.1 mm, it's reasonable that the dimensional variation stays around 0.2 mm, thus the combined power output will not be affected by the fabrication error too much.

## **5.4 Summary**

Before the design of the microstrip combining network the substrate material is chosen. To have low microstrip attenuation the substrate with low dielectric constant and higher thickness is preferred; to obtain high-precision defined microstrip lines thin metal foil on the substrate is preferred.

After the substrate material is determined the layout discontinuities of the combining network should be considered. Compensation methods are involved in the design such as mitered-bend and dimensional parameter adjusting, which are all integrated in the final synthesis of the microstrip combining network. The simulation results shows the 3-device unbalanced combining structure meets the design objective well and is not sensitive to the fabrication variation within 0.2 mm.





## Chapter 6

### Conclusion and future work

Due to the low breakdown voltage of the transistor in the normal CMOS process the output power from power amplifiers is limited. One solution for this problem is to combine the output power from multiple PA into the antenna load.

Based on the analysis of the parallel quarter-wavelength transmission line network the *N-device unbalanced power combining technique* is proposed. The power output of each PA block is combined through the parallel quarter-wavelength transmission lines so that the output power of each PA blocks is added rather than adding the output voltage. Though the voltage summation method is promising for voltage adding, the power summation provided by this technique is more practical for implementation. Using the three-step design method the characteristic impedance  $Z_0$  of the quarter-wavelength transmission lines is only dependent on three parameters, namely, the power output expected from each PA block  $P_o$ , the load impedance  $Z_{in}$  wanted by each PA block and the resistive load  $RL$  that the combined power delivered. As a result each PA block can remain its original optimal operation condition. The relationship between  $Z_0$ ,  $P_o$ ,  $Z_{in}$  and  $RL$  implies that the supply voltage for each PA can be different.

However, the three assumptions that the theoretical analysis is based on are what should be considered before the design.

First of all the phase difference between the output voltage of each PA block caused the phase difference nonidealities. The effect is dependent on the number of the combining PA blocks and the phase difference between each other. The exact effect represented in closed-form equations still need to be investigated. The major source of this phase difference comes from the difference in  $\beta$ <sup>1</sup> between each class E PA block. Using PA

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<sup>1</sup>  $\beta$  is defined as  $\frac{R_{on}}{R}$  in section 4.2.2.3 in page 84, where  $R_{on}$  is the switch-on resistance of the transistor;  $R$  is the load that the class E PA wants to see.

Secondly, if the combining network is originally designed so that each PA block is in class E condition, any changes in the combining network during operating will force the PA blocks out of the class E condition. This nonideality can be analyzed by the general model in chapter 4 only numerically and thus the exact effect on the combining network in the closed-form is not amiable yet. A special case of the amplitude nonidealities is when some PA blocks are short-circuit due to transistor breakdown or power control reason. The impedance that each working PA block sees will increase due to the short-circuit PA blocks. As a result the drain efficiency and power output of the working PA blocks decreases. One potential solution is that originally designing the combining network in such a way that the PA blocks are not in class E condition and the impedance they see is smaller than the optimal value. The benefit may be seen in PAE though the drain efficiency won't have obvious benefits. To further investigate this direction the power-load function (4.27) and driving input power needs to be known. An efficient driving-stage circuit can improve the PAE and is good direction for the further research.

Last but not the least, the antenna impedance for the combining network is assumed to be resistive. Further research on how to use the combining network for the varying reactive antenna load is important.

In practice the implementation of the combining network in low-loss microstrip PCB the layout design involves a lot consideration about discontinuities in microstrip lines. Several measures taken in this work, e.g. special choice in substrate, layout topologies and final physical optimization by the simulation, show the reduction of the discontinuities effect on the combining network.

As a conclusion using *N-device unbalanced power combining technique* can increase the available power output from PAs with low supply voltage in CMOS process. This combining technique is advantageous when low power loss in the combining network is preferred rather than fully integration. It has potentials in the increase of overall reliability for PAs and the power control application. The disadvantage is that using off-chip transmission line more board area is needed. When more PAs are combined, discontinuities in the layout will play a more complex and important role and it'll be more difficult to fully analyze.

Finally Fig 7.1 shows one implementation possibility for the combining network. The

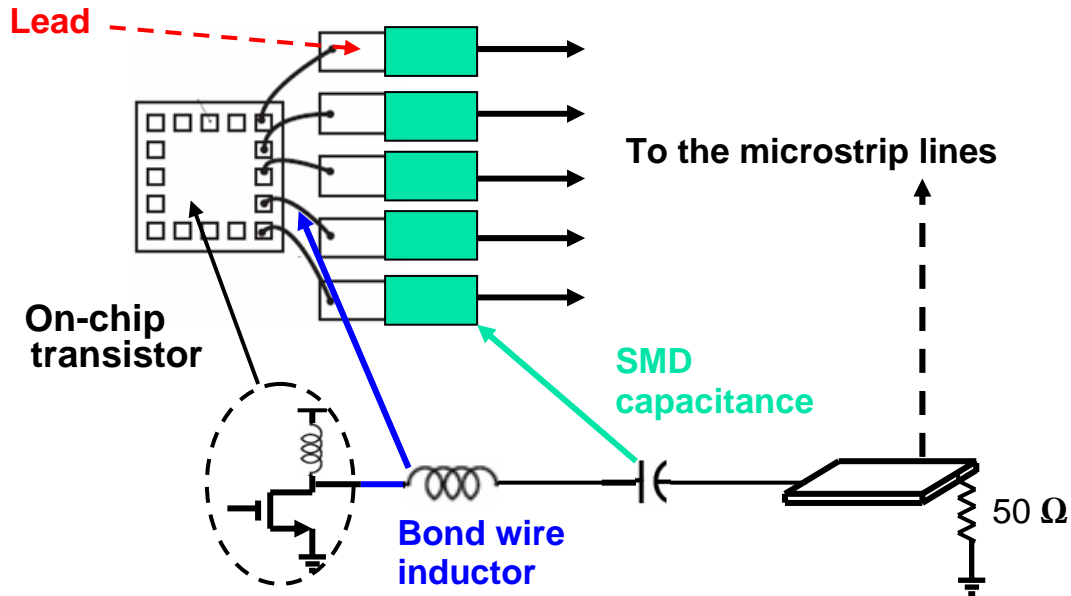


Fig. 7.1. An illustration of one possible implementation of the combining network. Transistors on the die is connected to the SMD capacitance by the bond wire. To control the inductance of the bond wire needs a lot experience due to the mutual inductance between the bond wires. Since the die is very small the SMD capacitors are very close to each and thus the quarter-wavelength lines connected to the capacitors are also very close and should be taken into account in the microstrip layout design.

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## **Appendix**

### ***Appendix of chapter 2 Extended resonance technique***

#### ***Appendix 2.1. Introduction***

This appendix consists of two parts. The first part is about the detail analysis of extended resonance technique and its ideal models on power combining and input signal distribution. Although the idea was introduced in [2.18]-[2.20], the analysis in these papers is not deep enough for fully understanding. Thus the detail analysis of extended resonance technique is discussed in the first part. The second part is about its application on class-e PA power combining and input signal distribution. The method of extended resonance technique was introduced [2.18]-[2.20]. The combining process takes advantage of the complex input and output devices impedances, instead of first matching each device to real impedance. Transmission lines can be used to convert the admittance at one device to its conjugate value at the next device, canceling the susceptive components and adding the conductance. This condition guarantees that equal power split among the devices for power dividing/combining purposes. The advantages of using this power-combining technique are that the overall size of the resulting structure is much smaller than with hybrid combiners [2.20].

#### ***Appendix 2.2. Theory analysis of extended resonance technique***

Following are five conclusions about the extended resonance technique presented in a step-by-step order for easy understanding. Along with the last conclusions the simulation result for verification are shown.

##### **2.2.1. Conclusion 1 : Complex conjugate admittance conversion**

As shown in Fig.App.2.1 to transfer the load admittance  $G + jB$  to its complex conjugate the electrical length EL of the transmission line should be:

$$\tan \theta = \tan \beta l = \frac{2BY_0}{B^2 + G^2 - Y_0^2} \quad (\text{App.2.1})$$

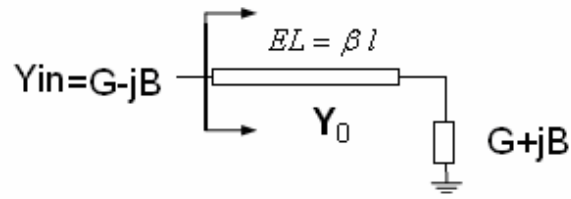


Fig.App. 2.1 Transmission line that can convert the load admittance to its complex conjugate.

where  $Y_0$  is the characteristic admittance of the transmission line

The derivation goes as following:

Based on the theory of transmission line [2.17]

$$Y_{in} = G - jB = Y_0 \frac{Y_L + jY_0 \tan \beta l}{Y_0 + jY_L \tan \beta l}, \text{ where } Y_L = G + jB \quad (\text{App.2.2})$$

$$\Leftrightarrow GY_0 + i(BY_0 + \tan \beta l Y_0^2) = GY_0 + i(B^2 \tan \beta l + G^2 \tan \beta l - BY_0)$$

$$\Rightarrow \tan \theta = \tan \beta l = \frac{2BY_0}{B^2 + G^2 - Y_0^2} \quad (\text{App.2.3})$$

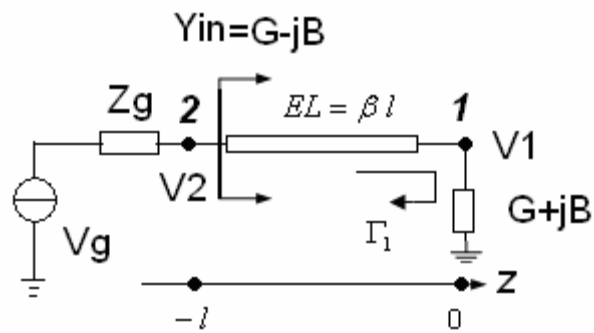


Fig. App. 2.2 The voltage at both sides of the transmission line which can convert the load admittance to its complex conjugate.

### 2.2.2. Conclusion 2 : Relationship between $V_1$ and $V_2$

As shown in Fig. App 2.2 only if the transmission line can transfer the load admittance (point 1) to its conjugate (point 2), then the amplitude of voltage in point 1 and 2 are equal and  $V_1$  has a phase delay  $\phi$  compared with  $V_2$ .

$$\frac{V_1}{V_2} = e^{j\phi} ; \tan \phi = -\frac{G \tan \beta l}{Y_0 - B \tan \beta l} = \frac{2BG}{B^2 - G^2 + Y_0^2} \quad (\text{App.2.4})$$

Derivation steps go as following:

$$\therefore \Gamma_1 = \frac{Y_0 - Y_L}{Y_0 + Y_L} = \frac{Y_0 - (G + jB)}{Y_0 + G + jB} = |\Gamma_1| e^{j\phi} \quad (\text{App.2.5})$$

While conclusion 1 (App.3.3)

$$\Rightarrow \tan \phi = \frac{2BY_0}{B^2 + G^2 - Y_0^2} = \tan \beta l \quad (\text{App.2.6})$$

Thus

$$\begin{cases} \Gamma_1 = |\Gamma_1| e^{j\phi} = |\Gamma_1| e^{j\beta l} \\ 1 + \Gamma_1 = \frac{2Y_0}{Y_0 + G + jB} \\ 1 - \Gamma_1 = \frac{2(G + jB)}{Y_0 + G + jB} \end{cases} \quad (\text{App.2.7})$$

Regarding to the voltage along the transmission line in Fig. App 2.2 the equations in [2.18] gives

$$V(z) = V_0^+ (e^{-j\beta z} + \Gamma_1 e^{j\beta z}) \quad (\text{App.2.8})$$

Thus along the Z axis

$$\begin{aligned} \frac{V_1}{V_2} &= \frac{V(0)}{V(-l)} = \frac{V_0^+ (1 + \Gamma_1)}{V_0^+ (e^{j\beta l} + \Gamma_1 e^{-j\beta l})} = \frac{1 + \Gamma_1}{e^{j\beta l} + \Gamma_1 e^{-j\beta l}} = \frac{1 + \Gamma_1}{\cos \beta l (1 + \Gamma_1) + j \sin \beta l (1 - \Gamma_1)} \\ &= \frac{Y_0}{(Y_0 \cos \beta l - B \sin \beta l) + jG \sin \beta l} \end{aligned} \quad (\text{App.2.9})$$

Thus the phase delay and amplitude ratio between  $V_1$  and  $V_2$  are:

$$\tan \phi = -\frac{G \tan \beta l}{Y_0 - B \tan \beta l} = \frac{2BG}{B^2 - G^2 + Y_0^2} \quad (\text{App.2.10})$$

and

$$\left| \frac{V_1}{V_2} \right| = \left| \frac{1 + \Gamma_1}{e^{j\beta l} + \Gamma_1 e^{-j\beta l}} \right| = \left| \frac{(1 + |\Gamma_1| e^{j\beta l}) e^{-j\beta l}}{1 + |\Gamma_1| e^{-j\beta l}} \right| = \left| \frac{1 + |\Gamma_1| \cos \beta l + j|\Gamma_1| \sin \beta l}{1 + |\Gamma_1| \cos \beta l - j|\Gamma_1| \sin \beta l} \right| = 1 \quad (\text{App.2.11})$$

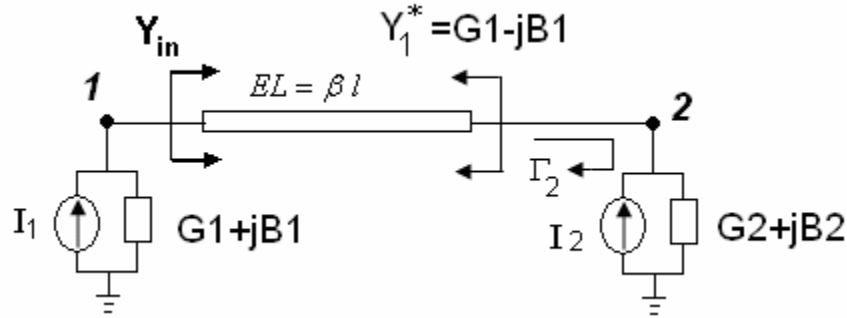


Fig.App. 2.3 The voltage at both sides of the transmission line which can convert the load admittance to its complex conjugate.

### 2.2.3. Conclusion 3: Power combining of two current source

If the following conditions are satisfied as shown in Fig. App2.3:

1. The transmission line has a certain electrical length that can transfer load admittance (point 1) to its conjugate (point 2)
2. The current source  $I_1$  and  $I_2$  are equal in amplitude,  $I_2 = I_1 e^{j\phi}$  and the phase difference is  $\phi$ ,  $\tan \phi = \frac{2B_1 G_1}{B_1^2 - G_1^2 + Y_0^2}$

$$\text{difference is } \phi, \tan \phi = \frac{2B_1 G_1}{B_1^2 - G_1^2 + Y_0^2}$$

Then at point 2 the voltage  $V_{12}$  contributed by  $I_1$  will be exactly the same as  $V_{22}$  contributed by  $I_2$ , which means the power from current source  $I_1$  and  $I_2$  is combined. Note that the phase  $\phi$  has nothing to do with the admittance at point 2, which implies that the power is combined at point 2 regardless of the load at point 2.

Derivation steps are presented as following.

Firstly only consider the voltage effect of current source  $I_1$  at point 1 ( $V_{11}$ ) and point 2 ( $V_{12}$ ).

At point 1  $V_{11} = \frac{I_1}{G_1 + jB_1 + Y_{in}}$  (App.2.12)

where  $Y_{in} = Y_0 \frac{1 - \Gamma_2 e^{-2j\beta l}}{1 + \Gamma_2 e^{-2j\beta l}} = Y_0 \frac{e^{j\beta l} - \Gamma_2 e^{-j\beta l}}{e^{j\beta l} + \Gamma_2 e^{-j\beta l}}$  and  $\Gamma_2 = \frac{Y_0 - G_2 - jB_2}{Y_0 + G_2 + jB_2}$

$$\begin{aligned} \therefore V_{11} &= \frac{I_1}{G_1 + jB_1 + Y_0 \frac{e^{j\beta l} - \Gamma_2 e^{-j\beta l}}{e^{j\beta l} + \Gamma_2 e^{-j\beta l}}} \\ &= \frac{I_1 (e^{j\beta l} + \Gamma_2 e^{-j\beta l})}{(G_1 + jB_1) \times (e^{j\beta l} + \Gamma_2 e^{-j\beta l}) + Y_0 (e^{j\beta l} - \Gamma_2 e^{-j\beta l})} \end{aligned} \quad (\text{App.2.13})$$

Based on (App.2.11) the ratio between  $V_{11}$  and  $V_{12}$  is  $\frac{1 + \Gamma_2}{e^{j\beta l} + \Gamma_2 e^{-j\beta l}}$

$$\begin{aligned} \therefore V_{12} &= V_{11} \times \frac{1 + \Gamma_2}{e^{j\beta l} + \Gamma_2 e^{-j\beta l}} \\ &= \frac{I_1 (e^{j\beta l} + \Gamma_2 e^{-j\beta l})}{(G_1 + jB_1) \times (e^{j\beta l} + \Gamma_2 e^{-j\beta l}) + Y_0 (e^{j\beta l} - \Gamma_2 e^{-j\beta l})} \times \frac{1 + \Gamma_2}{e^{j\beta l} + \Gamma_2 e^{-j\beta l}} \\ &= \frac{I_1 \times (1 + \Gamma_2)}{(G_1 + jB_1) \times (e^{j\beta l} + \Gamma_2 e^{-j\beta l}) + Y_0 (e^{j\beta l} - \Gamma_2 e^{-j\beta l})} \end{aligned} \quad (\text{App.2.14})$$

Euler rule results in  $e^{j\beta l} = \cos \beta l + j \sin \beta l$  ;  $e^{-j\beta l} = \cos \beta l - j \sin \beta l$

Thus

$$\begin{aligned} V_{12} &= \frac{I_1 (1 + \Gamma_2)}{(G_1 + jB_1) \times [\cos \beta l + j \sin \beta l + \Gamma_2 (\cos \beta l - j \sin \beta l)] + Y_0 \times [(\cos \beta l + j \sin \beta l - \Gamma_2 (\cos \beta l - j \sin \beta l))]} \\ &= \frac{-I_1 \times jY_0}{(B_1 Y_0 \cos \beta l + B_2 Y_0 \cos \beta l - B_1 B_2 \sin \beta l + G_1 G_2 \sin \beta l + Y_0^2 \sin \beta l) - j(G_1 Y_0 \cos \beta l + G_2 Y_0 \cos \beta l - B_2 G_1 \sin \beta l - B_1 G_2 \sin \beta l)} \end{aligned} \quad (\text{App.2.15})$$

Secondly only consider the effect voltage of current source  $I_2$  on point 2  $V_{22}$

$$V_{22} = \frac{I_2}{G_1 + G_2 + j(B_2 - B_1)} \quad (\text{App.2.16})$$

Combining (App.2.15) and (App.2.16) gives

$$\frac{V_{12}}{V_{22}} = \frac{-\frac{I_1}{I_2} \times jY_0 \times [G_1 + G_2 + j(B_2 - B_1)]}{(B_1 Y_0 \cos \beta l + B_2 Y_0 \cos \beta l - B_1 B_2 \sin \beta l + G_1 G_2 \sin \beta l + Y_0^2 \sin \beta l) - j(G_1 Y_0 \cos \beta l + G_2 Y_0 \cos \beta l - B_2 G_1 \sin \beta l - B_1 G_2 \sin \beta l)}$$

(App.2.17)

After simplification

Then the amplitude ratio of  $\frac{V_{12}}{V_{22}}$  goes as following:

$$\left| \frac{V_{12}}{V_{22}} \right|^2 = \left| \frac{I_1}{I_2} \right|^2 \quad (\text{App.2.18})$$

The angle of  $\frac{V_{12}}{V_{22}}$  goes as following:

$$\text{Angle}\left[\frac{V_{12}}{V_{22}}\right] = \text{Angle}\left[\frac{I_1}{I_2}\right] - \phi \quad (\text{App.2.19})$$

$$\text{Where } \tan \phi = \frac{2B_1G_1}{B_1^2 - G_1^2 + Y_0^2} \quad (\text{App.2.20})$$

As a conclusion the power contributed by  $I_1$  and  $I_2$  is combined at point 2 regardless of the load at node 2 if the phase delay between  $I_1$  and  $I_2$  is  $\phi$ ,  $\tan \phi = \frac{2B_1G_1}{B_1^2 - G_1^2 + Y_0^2}$

#### 2.2.4. Conclusion 4: Input signal distribution.

In Fig. App.2.4 each transistor is modeled by their gate admittance  $G_k + jB_k$  ( $n \geq k \geq 1$ ) while the conductance  $G_k$  is assumed to be all equal to  $G$ . Those transmission lines are designed to convert the admittance at one point to its complex conjugate at the next point. For example, transmission line  $EL_{n-1}$  is designed to convert the admittance ( $Y_{n-1}$ ) seen at point n-1 to its conjugate  $Y_{n-1}^*$  so that the total admittance seen at point n is  $Y_n = G_n + jB_n + Y_{n-1}^*$ .

To analyze the voltage relationship between each point of this network we can use the conclusion 2 repeatedly. The analysis starts from the very left point of the network (point n) shown in Fig. App. 2.5. At point n-1 the admittance seen by looking to the right is  $Y_{n-1}$



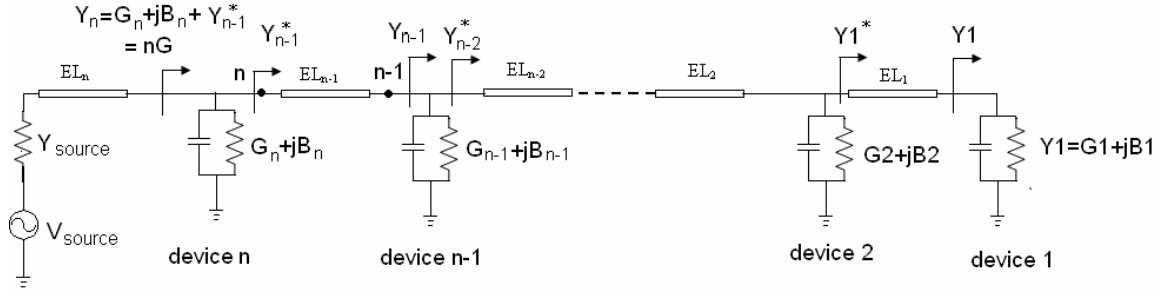


Fig. App.2.4 Input signal distribution network

while at node  $n$  an equivalent voltage source  $V_g$  is used. By using conclusion 2 it's obvious that the amplitude of voltage in point  $n$  and  $n-1$  are equal and  $V_{n-1}$  has a phase

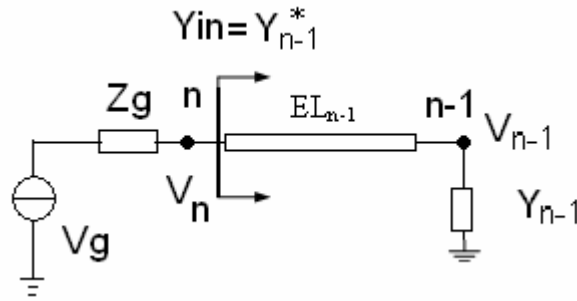


Fig. App.2.5 Equivalent model when analyzing the voltage relationship between point  $n$  and point  $n-1$ .

delay  $\phi$  compared with  $V_n$ :  $\frac{V_n}{V_{n-1}} = e^{j\phi} \quad \tan \phi = -\frac{G_{n-1} \tan \beta l}{Y_0 - B_{n-1} \tan \beta l} = \frac{2B_{n-1}G_{n-1}}{B_{n-1}^2 - G_{n-1}^2 + Y_0^2}.$

(Note that conclusion shows that the equivalent voltage source  $V_g$  and its internal impedance  $Z_g$  plays no role in the equation, which makes it easy to just use this equivalent voltage source again and again in the analysis of next points.) The same applies to all the neighbor points. In summary, for two neighbor points  $k$  and  $k-1$  ( $n \geq k \geq 1$ ) in this network

$$\frac{V_k}{V_{k-1}} = e^{j\phi} \quad \tan \phi = \frac{2B_{n-1}G_{n-1}}{B_{n-1}^2 - G_{n-1}^2 + Y_0^2}.$$

The susceptance  $B_n$  at

point  $n$  can be designed so that  $Y_n = G_n + jB_n + Y_{n-1}^* = nG = \frac{Y_0^2}{Y_{source}}$  to combine all the

conductance of the transistor inputs and match the input impedance shown in Fig. App.2.4. Through the  $n$ th transmission line (quarter wavelength) maximum power transfer can be achieved from the source. In a word, this network distributes the input

signal equally to each gate of transistor and achieves input matching at the same time.

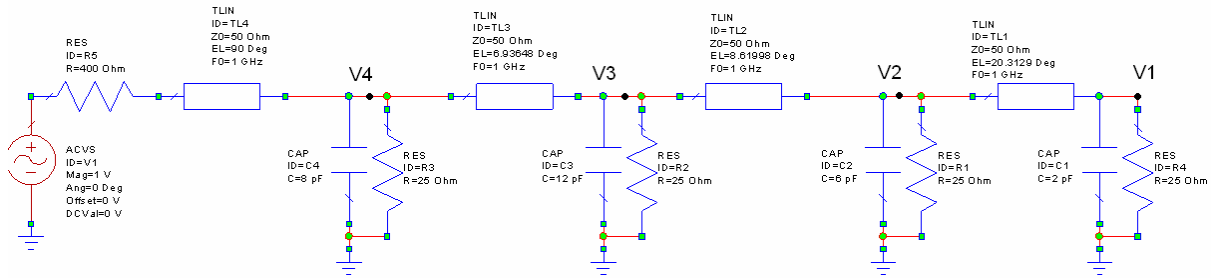


Fig. App.2.6 A four-device input distribution network in Microwave Office  
A four-device input distribution network implemented by ideal transmission line model in Microwave Office is shown in Fig. App.2.6. The simulation result in Fig. App.2.7

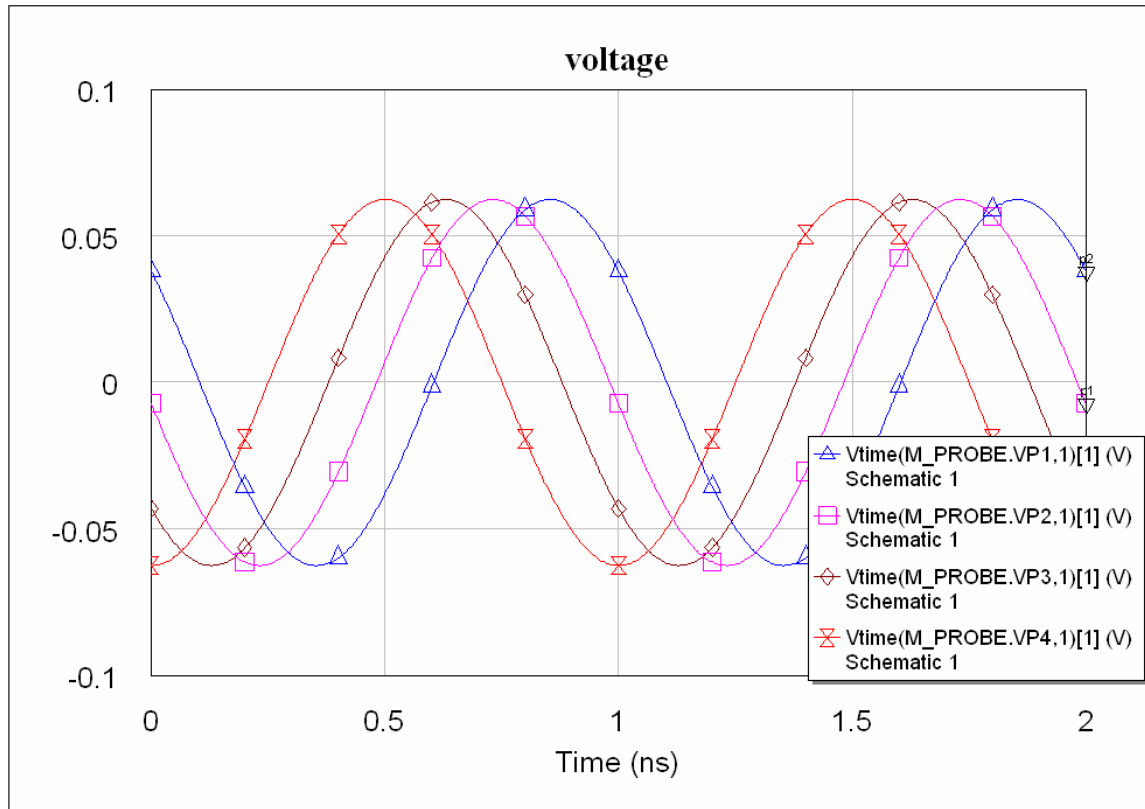


Fig. App.2.7 Simulation result shows that input signal is equally distributed.  
shows that input sinusoid signal is distributed equally to each of the device as conclusion 4 expects, in other words, the voltage amplitude at point 1, 2, 3 and 4 in Fig. App.2.6 are equal.

### 2.2.5. Conclusion 5: Output power combining

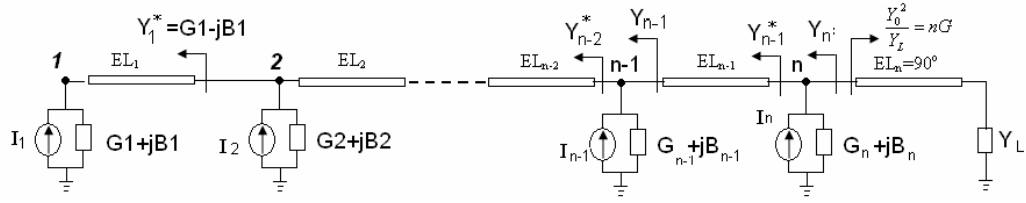


Fig. App.2.8 Output power combining network

In Fig. App.2.8 the network has  $N$  current sources each of which has the admittance  $G_k + jB_k$  ( $n \geq k \geq 1$ ), where the conductance  $G_k$  is assumed to be all equal to  $G$  and the amplitude of current is assumed to be all equal to  $I$ . Those transmission lines are designed to convert the admittance at one point to its conjugate value at the next point. For example, transmission line  $EL_{n-1}$  is designed to convert the admittance  $Y_{n-1}$  seen at point  $n-1$  to its conjugate  $Y_{n-1}^*$  so that the total admittance seen at point  $n$  is  $Y_n = G_n + jB_n + Y_{n-1}^*$ . Transmission line  $EL_n$  is designed to be quarter wavelength so as to convert the load admittance  $Y_L$  to  $nG$ . The susceptance  $B_n$  at point  $n$  is designed so that  $Y_n = G_n + jB_n + Y_{n-1}^* = nG$ , which enables the power-maximum-transfer to load  $Y_L$ . To analyze the capacity of power combining of this network the superposition method is used. Analysis is applied sequentially from the very right point of the network (point  $n$ ) to the very left point (point 1) which is much easier than from the left point to the right.

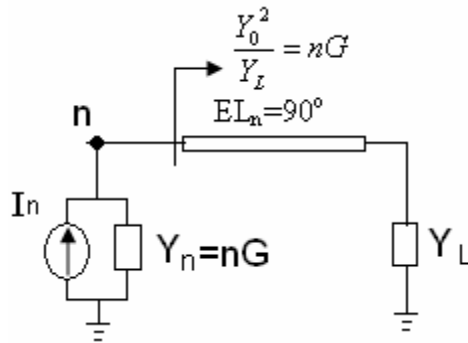


Fig. App.2.9 Equivalent model when only analyzing current source  $I_n$

At first we only consider current source  $I_n$ . As shown in Fig 8 the admittance seen by looking to the left of point  $n$  is  $Y_n = nG$ , thus the equivalent model for the whole network

only considering current source  $I_n$  is shown in Fig. App.2.9. The voltage at point n is

$$V_{n,n} = \frac{I_n}{Y_n + \frac{Y_0^2}{Y_L}} = \frac{I_n}{2nG} \quad (\text{App.2.21})$$

Next only consider current  $I_{n-1}$  and  $I_n$ . The equivalent model in Fig.App.2.10 is used.

Based on conclusion 3 the voltage  $V_{n,n-1}$  and  $V_{n,n}$  at point n contributed respectively by

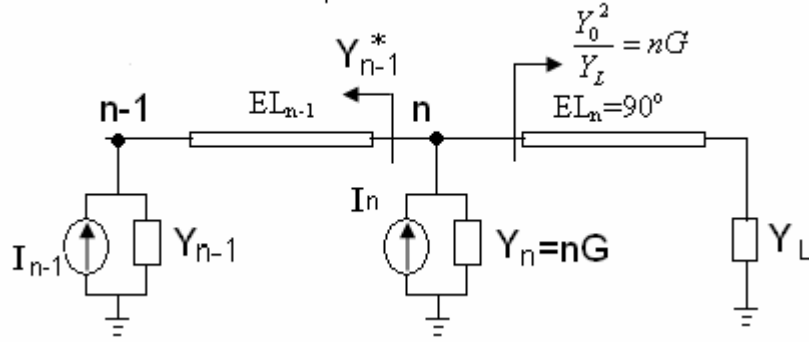


Fig. App.2.10 Equivalent model for analyzing the voltage at point n caused by  $I_{n-1}$ .

$I_{n-1}$  and  $I_n$  are equal in amplitude and the phase difference is  $\phi$ ,

where  $\tan \phi = \frac{2B_{n-1}G_{n-1}}{B_{n-1}^2 - G_{n-1}^2 + Y_0^2}$ . This conclusion works for the rest of any couple points.

Thus by designing the susceptance of each current source their voltage effect on point n can be in phase taking into account the phase delay between  $I_{n-1}$  and  $I_n$ . In that case the whole overlapping voltage  $V_n$  at point n

$$V_n = nV_{n,n} = \frac{nI_n}{2nG} = \frac{I_n}{2G} \quad (\text{App.2.22})$$

Thus the power transferred to the load by the network in Fig. App.2.8 is

$$\frac{V_n^2 nG}{2} = \frac{nI_n^2}{8G} \quad (\text{App.2.23})$$

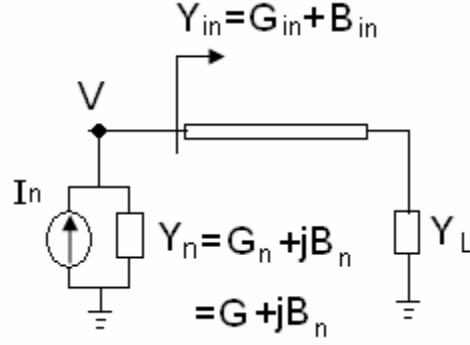


Fig.App.2.11 Equivalent model for analyzing current source maximum power transfer.

Following we can calculate that maximum power transferred to the load  $Y_L$  by each single current source is  $\frac{I_n^2}{8G}$ .

As shown in Fig.App.2.11 to achieve maximum power transfer a transmission line is used to convert  $Y_L$  to  $Y_{in}$ . The power transferred to the load is

$$\frac{1}{2} \times |V|^2 \times G_{in} = \frac{1}{2} \times \frac{G_{in} \times |I_n|^2}{(G_{in} + G)^2 + (B_n + B_{in})^2}, \text{ when } G_{in} = G, B_{in} = -B_n \text{ the maximum}$$

power is  $\frac{I_n^2}{8G}$ , which is nth of the power combined in load by the network in Fig. App.2.8 shown in (App.2.23).

In summary, the network is capable of combining the maximum power each current source can deliver to the load  $Y_L$ . As shown in Fig.2.12 a four-device power combining network is implemented by ideal transmission line model in Microwave Office, where  $I=1\text{mA}$ ,  $G=0.04\text{S}$ . From (App.2.23) the total delivered to the load is

$$\frac{nI_n^2}{8G} = \frac{4 \times 1}{8 \times 0.04} = 12.5\mu\text{W}, \text{ while the maximum power one current source can deliver to}$$

$$\text{the same load is } \frac{I_n^2}{8G} = \frac{1}{8 \times 0.04} = 3.05\mu\text{W}. \text{ Fig.App.2.13 shows the simulation results}$$

agrees with the theory expectation.

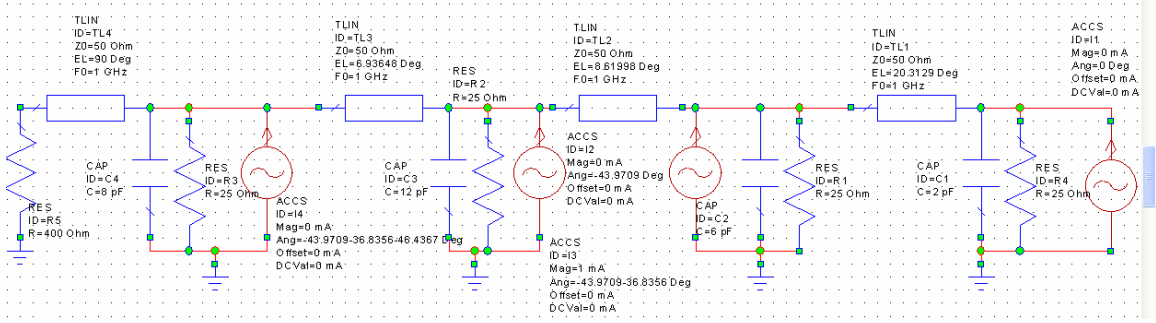


Fig. App.2.12 A four-device power combining network

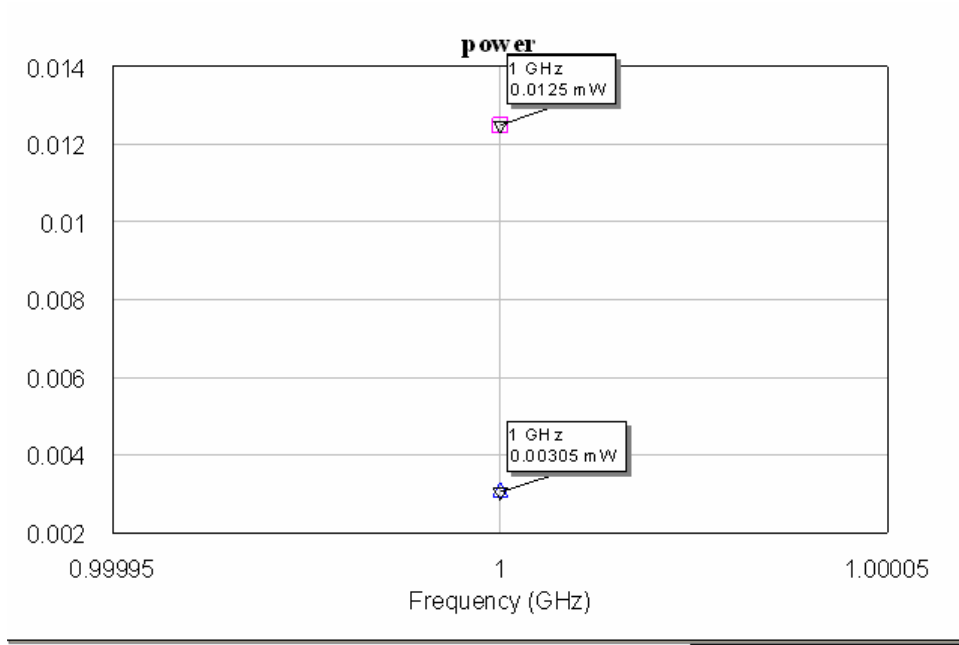


Fig. App.2.13 Simulation result of power delivered to the load by power combining network and one single current source.

### 2.3. Discussion

As shown in Fig. App.2.13 the input signal distribution network in Fig. App.4 is connected with the transistor of several PAs. As the conclusion 4 says the voltage of each gate of the transistors should be equal and with phase shift of  $\phi$ , where

$$\tan \phi = \frac{2B_{n-1}G_{n-1}}{B_{n-1}^2 - G_{n-1}^2 + Y_0^2}$$

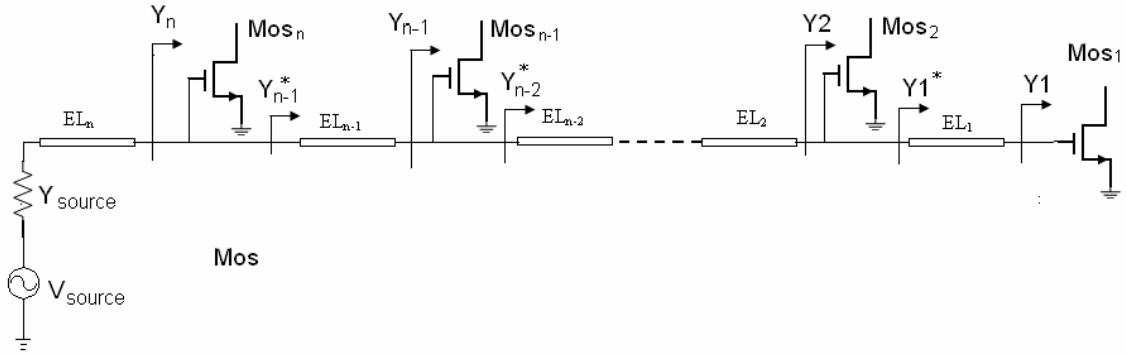


Fig.App.2.13 Input signal distribution network for class-e PAs

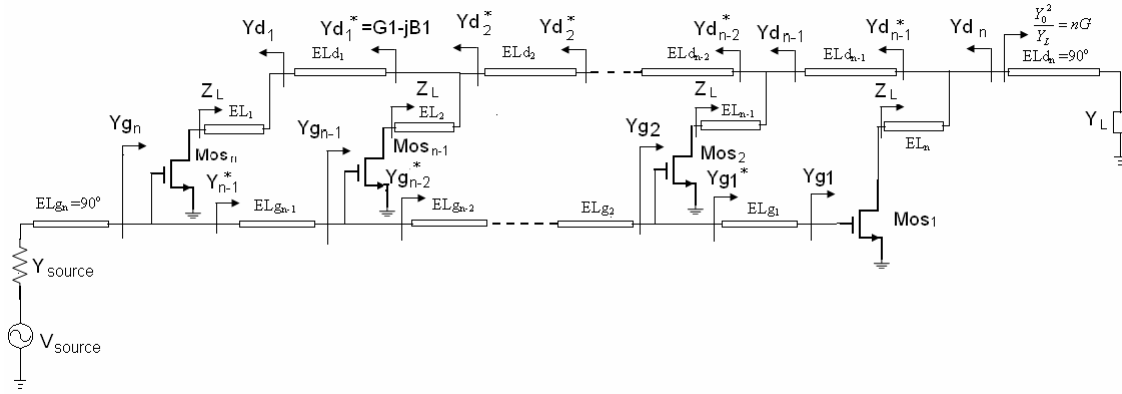


Fig.App.2.14 Power output combining network for class E PAs

As shown in Fig. App.2.14 transmission lines  $ELd_1$  to  $ELd_n$  are playing the role of power combining network as shown in Fig.App.2. 8. Then transmission lines  $EL_1$  to  $EL_n$  which connect the drain the those transistors to the power combining network provide the tuning filter susceptance for the class-e operation. Since the input signal on the gates of these transistors have phase shift the output of each class-e PA is introduced the same shift. For power to be combined coherently between each device, the phase delay between the drain sand gates must be equal [2.20]. However, the extended resonance technique is purely based on the linear analysis and the power sources to be combined are single-frequency current or voltage source. It is not clear that the switching transistor in class E PA can be modeled as single-frequency current or voltage source. This confusion hasn't been solved in this work.

## Appendix of chapter 4

### Appendix 4.1

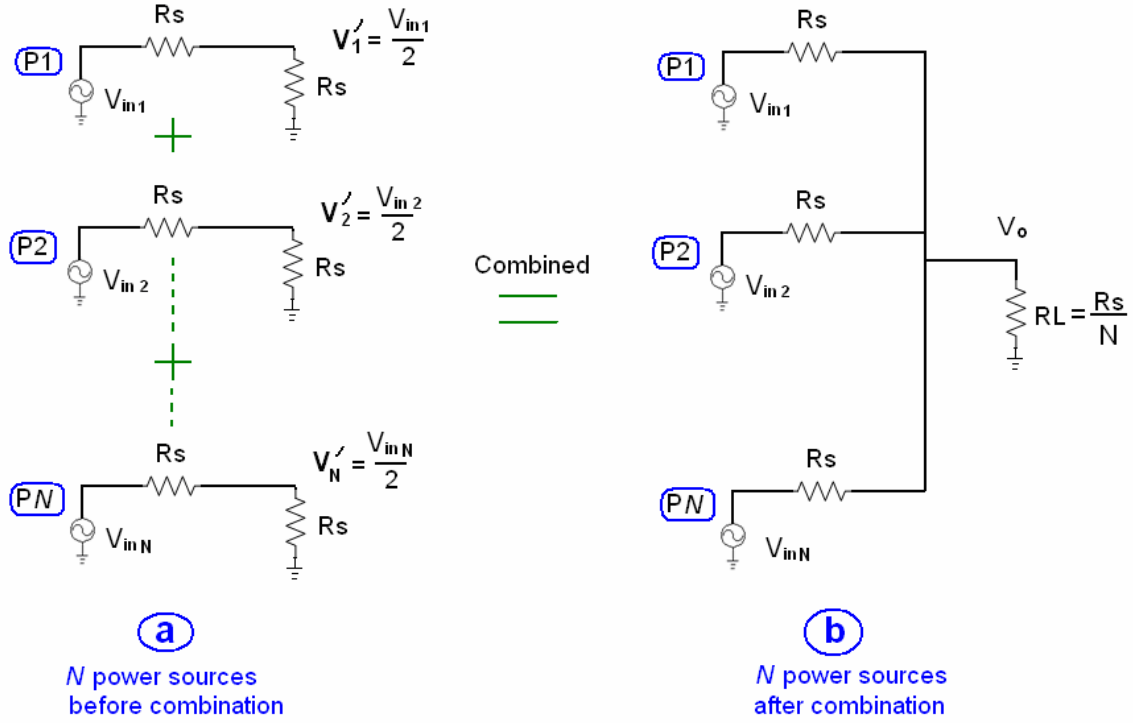


Fig. App. 4.1 The  $N$  combined power sources

The method of supposition is used to calculate the output voltage  $V_o$  in Fig. App. 4.1b.

For each power source  $V_{inj}$  its voltage output at the output node is given by

$$V_{oj} = \frac{R_s // \frac{R_s}{2(N-1)}}{R_s + R_s // \frac{R_s}{2(N-1)}} \times V_{inj} = \frac{V_{inj}}{2N} \quad (\text{App.4.1})$$

Thus the total voltage output contributed by all power sources  $V_{inj}$  are given

$$V_o = \sum_{j=1}^N V_{oj} = \frac{1}{2N} \times (V_{in1} + V_{in2} + \dots + V_{inN}) \quad (\text{App.4.2})$$

Since the load is equal to the source resistance so as to deliver the maximum power to the load the output voltage  $V_1'$  is given by



$$V_1' = \frac{V_{inj}}{2} \quad (\text{App.4.3})$$

Substituting (App.4.3) into (App.4.2) yields

$$V_o = \frac{1}{N} \times (V_1' + V_2' + \dots + V_N') \quad (\text{App.4.4})$$

## Appendix 4.2

Following is the trigonometric function:

$$\begin{aligned} \sin(\omega t + \phi 1) + \sin(\omega t + \phi 2) + \dots + \sin(\omega t + \phi N) &= \sum_{j=1}^N \sin(\omega t + \phi j) \\ &= \sin(\omega t) \cos(\phi 1) + \cos(\omega t) \sin(\phi 1) + \dots + \sin(\omega t) \cos(\phi N) + \cos(\omega t) \sin(\phi N) \\ &= [\cos(\phi 1) + \cos(\phi 2) + \dots + \cos(\phi N)] \times \sin(\omega t) + [\sin(\phi 1) + \sin(\phi 2) + \dots + \sin(\phi N)] \times \cos(\omega t) \end{aligned} \quad (\text{App.4.5})$$

With  $A = [\sin(\phi 1) + \sin(\phi 2) + \dots + \sin(\phi N)]$  and  $B = [\cos(\phi 1) + \cos(\phi 2) + \dots + \cos(\phi N)]$

(App.4.5) is transformed to

$$A \cos(\omega t) + B \sin(\omega t) = \sqrt{A^2 + B^2} \cos(\omega t - \arctan \frac{B}{A}) \quad (\text{App.4.6})$$

The amplitude is given by

$$\begin{aligned} &\sqrt{A^2 + B^2} \\ &= [\cos(\phi 1) + \cos(\phi 2) + \dots + \cos(\phi N)]^2 + [\sin(\phi 1) + \sin(\phi 2) + \dots + \sin(\phi N)]^2 \\ &= \cos(\phi 1)^2 + \sin(\phi 1)^2 + \cos(\phi 2)^2 + \sin(\phi 2)^2 + \dots + \cos(\phi N)^2 + \sin(\phi N)^2 \\ &\quad + 2 \cos(\phi 1) \cos(\phi 2) + 2 \sin(\phi 1) \sin(\phi 2) + \dots + 2 \cos[\phi(N-1)] \cos(\phi N) + 2 \sin(\phi(N-1)) \sin(\phi N) \\ &= \sum_{i=1}^N [\cos(\phi i)^2 + \sin(\phi i)^2] \\ &\quad + 2 \sum_{i=2}^N [\cos(\phi 1) \cos(\phi i) + \sin(\phi 1) \sin(\phi i)] \\ &\quad + 2 \sum_{i=3}^N [\cos(\phi 2) \cos(\phi i) + \sin(\phi 2) \sin(\phi i)] \\ &\quad + 2 \sum_{i=4}^N [\cos(\phi 3) \cos(\phi i) + \sin(\phi 3) \sin(\phi i)] \end{aligned}$$

$$\begin{aligned}
& \vdots \\
& \vdots \\
& + 2 \sum_{i=N-1}^N \{ \cos[\varphi(N-2)] \cos(\varphi i) + \sin[\varphi(N-2)] \sin(\varphi i) \} \\
& + 2 \sum_{i=N}^N \{ \cos[\varphi(N-1)] \cos(\varphi i) + \sin[\varphi(N-1)] \sin(\varphi i) \} \\
& = \sum_{i=1}^N 1 \\
& + 2 \sum_{i=2}^N \cos(\varphi 1 - \varphi i) \\
& + 2 \sum_{i=3}^N \cos(\varphi 2 - \varphi i) \\
& + 2 \sum_{i=4}^N \cos(\varphi 3 - \varphi i) \\
& \quad \vdots \\
& \quad \vdots \\
& + 2 \sum_{i=N-1}^N \cos[\varphi(N-2) - \varphi i] \\
& + 2 \cos[\varphi(N-1) - \varphi N] \\
& = N + 2 \sum_{i=2}^N \cos(\varphi 1 - \varphi i) + 2 \sum_{i=3}^N \cos(\varphi 2 - \varphi i) + \cdots 2 \sum_{i=N-1}^N \cos[\varphi(N-2) - \varphi i] + 2 \cos[\varphi(N-1) - \varphi N]
\end{aligned}$$

(App.4.7)

### Appendix 4.3

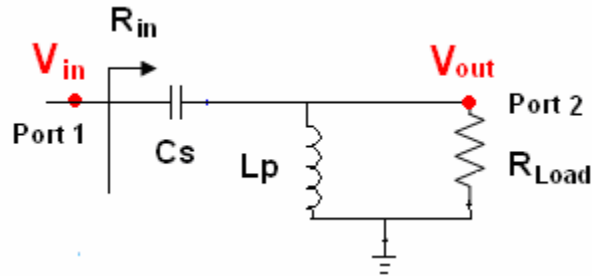


Fig. App. 4.2 Ideal resonant LC impedance-conversion network (L matching network)

This simple ideal L matching network converts the load  $R_{Load}$  to a smaller resistive load  $R_{in}$ . The impedance-transformation ratio  $r$  is defined by [2.22]

$$r = \frac{R_{Load}}{R_{in}} \quad (\text{App.4.8})$$

The function between  $R_{Load}$  and  $R_{in}$  is given by

$$\begin{aligned} R_{in} &= \frac{1}{jC_s\omega_0} + j\omega_0 L_p // R_{Load} \\ &= \frac{(\omega_0 L_p)^2 \times R_{Load}}{R_{Load}^2 + (\omega_0 L_p)^2} + j\left(\frac{\omega_0 L_p R_{Load}^2}{R_{Load}^2 + (\omega_0 L_p)^2} - \frac{1}{C_s\omega_0}\right) \end{aligned} \quad (\text{App.4.9})$$

Based on (App.4.9) the capacitor  $C_s$  and the inductor  $L_p$  are calculated as

$$C_s = \frac{1}{R_{in}\omega_0\sqrt{r-1}} = \frac{r}{R_{Load}\omega_0\sqrt{r-1}} \quad (\text{App.4.10})$$

$$L_p = \frac{R_{Load}}{\omega_0\sqrt{r-1}} \quad (\text{App.4.11})$$

Thus the ratio of the voltage at port 1 and port 2 is

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{R_{Load} // j\omega_0 L_p}{R_{in}} = \frac{R_{in} - \frac{1}{j\omega_0 C_s}}{R_{in}} \\ &= 1 + j\sqrt{r-1} \end{aligned} \quad (\text{App.4.12})$$

which indicates that the L matching network introduces a phase shift  $\arctan\sqrt{r-1}$ .

## Appendix 4.4

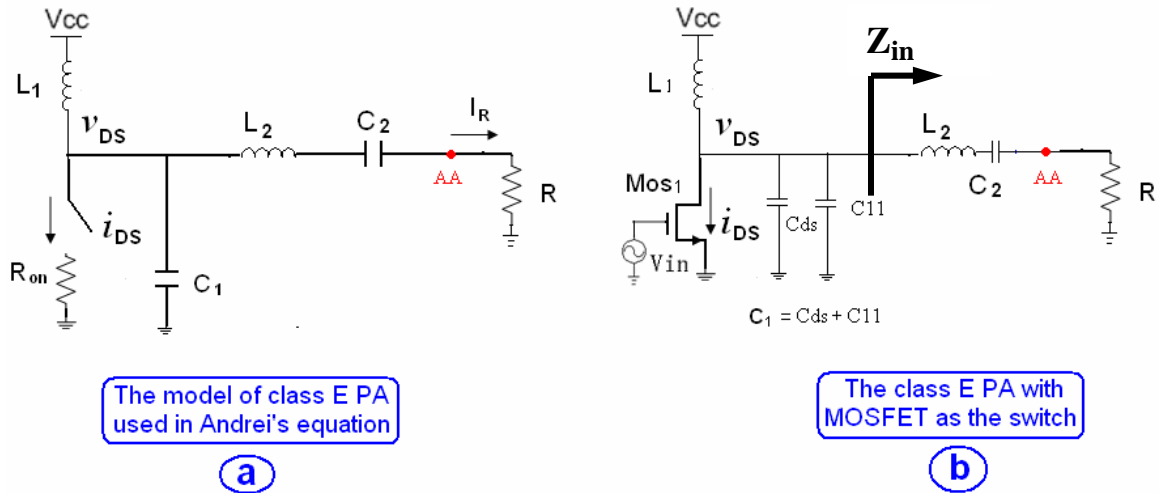


Fig. App. 4.3 Andrei's analysis model for the class E PA.

In Andrei's equations [1.4] the model shown in Fig. App. 4.3a is used for the class E PA, where the switching-on resistance  $R_{on}$  is zero. In practice  $R_{on}$  is not zero and the energy consumed in the switching-on resistance is the power loss of the class E PA. In the following derivation it's assumed that Andrei's equations are still valid when  $R_{on}$  is not zero but small. Therefore, the equation for the switching-on current  $i_s$  is used to calculate the power loss on  $R_{on}$ .

The switching-on current is given by [1.4]

$$i_s = \frac{V_{cc}}{\omega L_1} \omega t + I_R [\sin(\omega t + \varphi) - \sin \varphi] \quad (\text{App.4.13})$$

$$\text{where } I_R = \frac{1.21 V_{cc}}{\omega t \times L_1}$$

Thus the power loss on  $R_{on}$  is given by

$$\begin{aligned} P_{loss} &= \frac{1}{2\pi} \times \int_0^\pi i_s^2 R_{on} d(\omega t) = \frac{1}{2\pi} \times \int_0^\pi \left( \frac{V_{cc}}{\omega L_1} \omega t + I_R [\sin(\omega t + \varphi) - \sin \varphi] \right)^2 R_{on} d(\omega t) \\ &= \frac{2.2954 \times V_{cc}^2}{(\omega L_1)^2} \times R_{on} \end{aligned} \quad (\text{App.4.14})$$

Substituting  $L_1 = 0.732 \times \frac{R}{\omega}$ ,  $R = \frac{1.365 \times V_{cc} \times V_{cc}}{P_{out}}$  [1.4] into (App.4.14) yields

$$P_{loss} = \frac{2.2954 \times P_{DC}^2}{V_{cc}^2} \times R_{on} \quad (\text{App.4.15})$$

Therefore the power output is given by (App.4.16)

$$P_{out} = P_{DC} - P_{loss} = P_{DC} - \frac{2.2954 \times P_{DC}^2}{V_{cc}^2} \times R_{on}$$

And the drain efficiency is given by

$$\begin{aligned} \eta_{drain} &= \frac{P_{out}}{P_{DC}} \times 100\% = \frac{P_{DC} - \frac{2.2954 \times P_{DC}^2}{V_{cc}^2} \times R_{on}}{P_{DC}} = \left( 1 - \frac{2.2954 \times P_{DC}}{V_{cc}^2} \times R_{on} \right) \times 100\% \\ &= (1 - 4.58 \times C_1 \omega R_{on}) \times 100\% \end{aligned} \quad (\text{App.4.17})$$

## Appendix 4.5

In the class E PA the transistor is used as the switch shown in Fig. App. 4.3b. The wider is the transistor the smaller is the switching-on resistance  $R_{on}$  and the larger is the parasitic capacitance  $C_{ds}$ . Though the switching-on resistance and parasitic capacitance are nonlinear during the class E operation the constant equivalent  $R_{on}$  and  $C_{ds}$  could be used for the design and analysis. The relationship with the width of the transistor is given by

$$R_{on} = \frac{k_{Ron}}{W} \quad (\text{App.4.18})$$

$$C_{ds} = k_c W \quad (\text{App.4.19})$$

where  $W$  is the width of the switching transistor;  $k_{Ron}$  is the linear factor between the  $R_{on}$  and transistor width;  $k_c$  is the linear factor between  $C_{ds}$  and transistor width.

Combining (App.4.18) and (App.4.19) yields

$$C_{ds} = \frac{k_c k_{Ron}}{R_{on}} \quad (\text{App.4.20})$$

For the class E PA the capacitance in parallel with the switch,  $C_1$ , consists of the parasitic capacitance  $C_{ds}$  and external capacitance  $C_{11}$  shown in Fig. App. 4.3b, which is given by [1.4]

$$C_1 = \frac{0.685}{\omega R} = C_{ds} + C_{11} \geq C_{ds} \quad (\text{App.4.21})$$

## Appendix 4.6

In the Andrei's design equation the filter network ( $L_2, C_2$ ) and optimal load  $R$  actually consists of a series RLC resonant circuit shown in Fig. App. 4.3b, where

$$\omega_0 L_2 = \omega_0 L_0 = R \times Q_L \quad (\text{App.4.22})$$

$$\omega_0 C_2 = \omega_0 C_0 = \frac{1}{R \times Q_L} \quad (\text{App.4.23})$$

At the first glance high value of  $Q_L$  is the choice in the design since it keeps the THD lower. However, in practice, the components variation should be taken into account and

the performance of the PA should be insensitive to the components variation. As will be shown, higher value of  $Q_L$  causes higher sensitivity to the components variation.

The series RLC resonant circuit provides impedance  $Z_{in}$  to the transistor, which is given by

$$Z_{in} = j\omega L_2 + \frac{1}{j\omega C_2} + R \quad (\text{App.4.24})$$

Where,  $L_2 = L_0 + \Delta L$ ;  $C_2 = C_0 + \Delta C$ ,  $L_0$  and  $C_0$  are the design value and given by (App.4.22) and (App.4.23),  $\Delta L$  and  $\Delta C$  represent the component variation.

At fundamental frequency  $\omega_0$  (App.4.24) can rearranged into

$$\begin{aligned} Z_{in} &= j\omega_0(L_0 + \Delta L) + \frac{1}{j\omega_0(C_0 + \Delta C)} + R \\ &= jRQ_L + \frac{1}{j(\frac{1}{RQ_L} + \frac{\Delta C}{C_0 RQ_L})} + jRQ_L \frac{\Delta L}{L} + R \\ &\approx jRQ_L(\frac{\Delta L}{L_0} + \frac{\Delta C}{C_0}) + R \end{aligned} \quad (\text{App.4.25})$$

Since the design value of  $Z_{in}$  at fundamental frequency  $\omega_0$  is  $R$  the impedance variation the transistor sees is given by

$$\frac{Z_{in}}{R} = 1 + jQ_L(\frac{\Delta L}{L_0} + \frac{\Delta C}{C_0})$$

As a result, for the same component variation ( $\frac{\Delta L}{L_0}$  or  $\frac{\Delta C}{C_0}$ ) higher  $Q_L$  causes higher impedance variation for the transistor, which makes the PA more sensitive to the component variation. However, low  $Q_L$  brings high THD in the output signal.

## Appendix 4.7

The power sources P1 and P2 both deliver the maximum power to their load  $R_{s1}$  and  $R_{s2}$  shown in Fig. App. 4.4a. Assume the voltage sources  $V_{in1}$  and  $V_{in2}$  are in phase. When the output voltage  $V_1$  and  $V_2$  are equal in amplitude their output nodes can be connected directly and the power is combined to the load  $RL$  shown in Fig. App. 4.4b.

When  $V_1$  and  $V_2$  are different in amplitude the output voltage  $V_o'$  in Fig. App. 4.4b can be calculated using the method of supposition.

### Equation derivation

For the power source P1 the effective voltage output at the output node in Fig. App. 4.4b is given by

$$V_{1o} = \frac{R_{s1} // \frac{R_{s2}}{2}}{R_{s1} + R_{s1} // \frac{R_{s2}}{2}} \times V_{in1} = \frac{R_{s2}}{2(R_{s1} + R_{s2})} \times V_{in1} \quad (\text{App.4.26})$$

The similar result for the power source P2 is

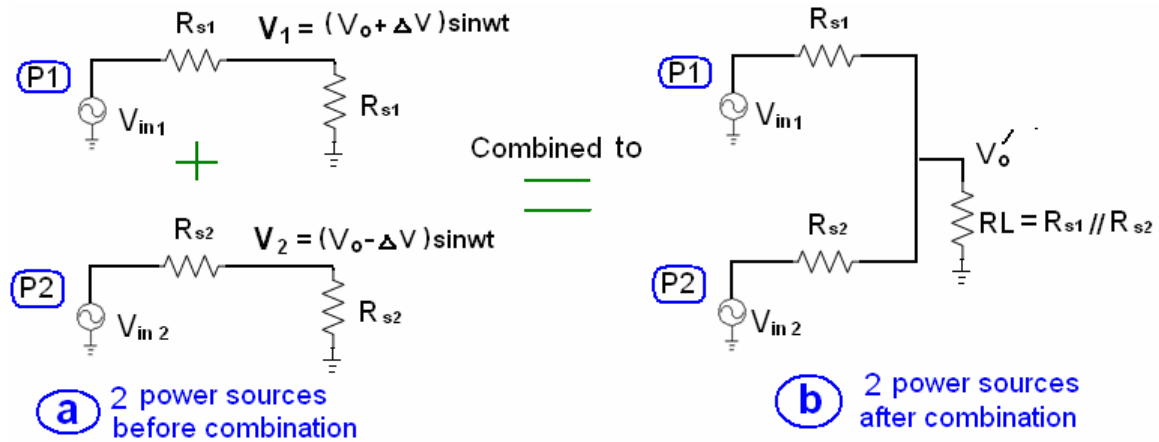


Fig. App. 4.4 Two-power-source combination.

$$V_{2o} = \frac{R_{s1}}{2(R_{s1} + R_{s2})} \times V_2 \quad (\text{App.4.27})$$

Since the power sources P1 and P2 deliver the maximum power to the load

$$V_{in1} = 2V_1 = 2(V_o + \Delta V) \quad (\text{App.4.28})$$

$$V_{in2} = 2V_2 = 2(V_o - \Delta V) \quad (\text{App.4.29})$$

There the combined output voltage is given by

$$V_o' = V_{1o} + V_{2o} = V_o + \frac{R_{s1} - R_{s2}}{R_{s1} + R_{s2}} \Delta V \quad (\text{App.4.30})$$

## Appendix 4.8

When the class E PA is working the load  $Z_{PA}$  seen by the transmission line by looking into the PA block is time-variant since the transistor is switching on or off. When the PA is shut off load  $Z_{PA}$  can be constant as show in Fig. App.4.5. The filter block  $L_2$  and  $C_2$  is tuned at the fundamental frequency [1.4] thus the impedance  $Z_{PA}$  is  $j\omega L_1 // Z_X$ . The

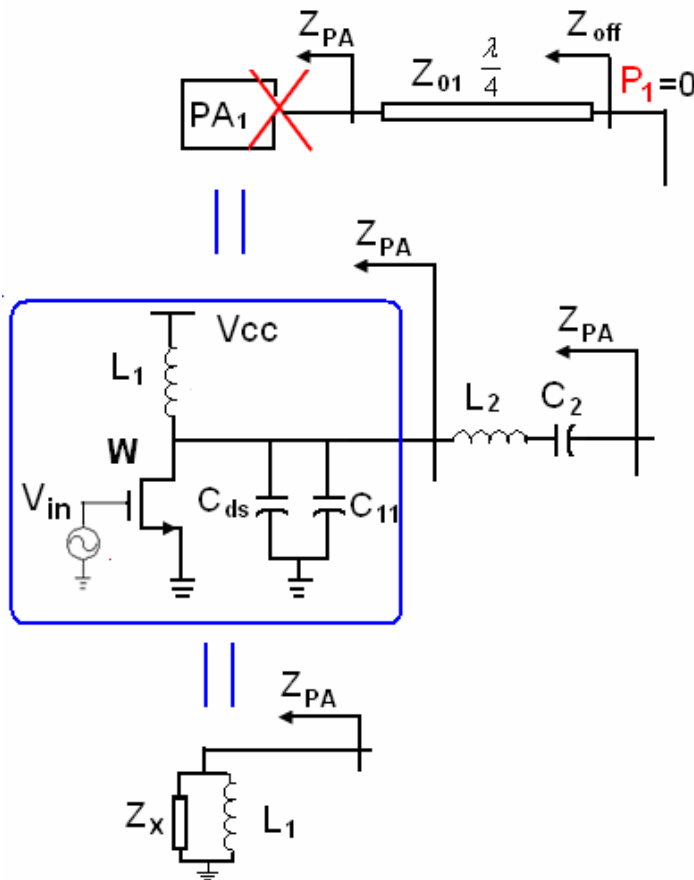


Fig. App. 4.5 Illustration of the impedance seen looking into the switched-off PA block.

impedance  $Z_X$  is not necessarily equal to the combination of the external capacitance  $C_{11}$  and the intrinsic capacitance of the transistor  $C_{ds}$ , among which  $C_{ds}$  is dependent the



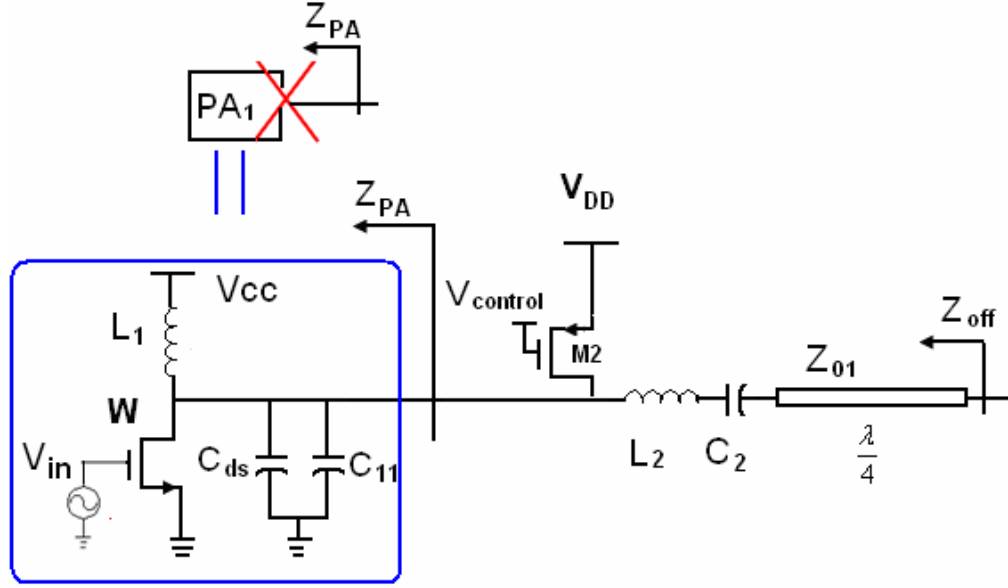


Fig. App. 4.6 The shut-off PA block is short-circuited by the PMOS M2.

condition of the transistor. It's dependent on how this PA block is shut off. The supply voltage could be zero or the driving voltage could be zero or the transistor could be breakdown. Therefore,  $Z_{PA}$  is used to denote the impedance contributed by the PA block and impedance  $Z_{off}$  contributed by the switched-off PA blocks is given by

$$Z_{off} = \frac{Z_0^2}{Z_{PA}} \quad (\text{App.4.31})$$

The varying  $Z_{PA}$  makes it not easy to anticipate the effect on the combining structure caused by the shut-off PA blocks. A PMOS M2 with a control signal can be added in parallel to the switching transistor shown in Fig. App. 4.6. When the PA is shut-off the PMOS M2 is controlled to short-circuit the switching . Therefore  $Z_{off}$  can be calculated in advance without depending on the variety of  $Z_{PA}$ .

## Appendix 5

### Choice of the microstrip

Before the microstrip design several choices need to be determined, namely, the substrate material, the layout topology of the microstrip lines and the fabrication process. This section discusses these issues respectively.

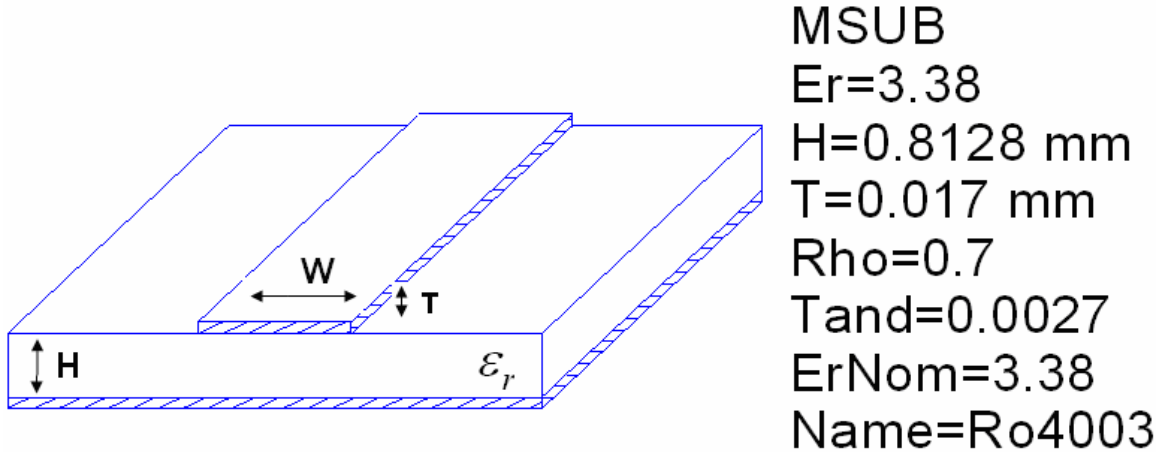


Fig. 5.1 Geometry illustration of a microstrip line.

### 5.1 Choice of the substrate material

A PCB substrate provides the following options for designer to choose shown in Fig. App.5.1.

1. Substrate material dielectric constant  $\epsilon_r$ .
2. Substrate thickness  $H$ .
3. Metal foil thickness  $t$ .

#### Substrate dielectric constant and thickness choices

Although the microstrip line has very low loss it's always of interest to lower the loss as much as possible. Since the power efficiency is critical for the combining network the attenuation of the microstrip determines the choice of the substrate material in this work.

The attenuation  $\alpha$  of the microstrip consists of two parts, namely, dielectric loss attenuation  $\alpha_d$  and conductor loss  $\alpha_c$ . For most microstrip substrates, conductor loss is much more significant than dielectric loss [2.17] [5.1] and thus only the conductor loss  $\alpha_c$  is used to characterize the loss of the microstrip in this work.

The conductor attenuation is approximately given by [2.17]

$$\alpha_c = \frac{R_s}{Z_0 W} \text{ Np/m} \quad (\text{App.5.1})$$

, where  $R_s = \sqrt{\omega\mu_0/2\sigma}$  is the surface resistivity of the conductor.

The wavelength of the microstrip is

$$\lambda = \frac{c}{f\sqrt{\epsilon_e}} \quad (\text{App.5.2})$$

, where  $c$  is the light speed,  $f$  is the operating frequency and  $\epsilon_e$  is the effective dielectric constant and approximately is appropriate to the relative permittivity  $\epsilon_r$  of the substrate.

so in terms of wavelength the attenuation is

$$\alpha \approx \alpha_c \times \lambda = \frac{R_s}{Z_0 W} \times \frac{c}{f\sqrt{\epsilon_e}} \quad (\text{App.5.3})$$

, where the characteristic impedance  $Z_0$  is given by [2.17]

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_e} \left[ \frac{W}{H} + 1.393 + 0.667 \ln\left(\frac{W}{H} + 1.444\right) \right]} \quad (\text{App.5.4})$$

Substituting (App. 5.4) in (App. 5.3) gives

$$\alpha \approx \frac{R_s \times c}{120\pi f} \times \left[ \frac{1}{H} + \frac{1.393 + 0.667 \ln\left(\frac{W}{H} + 1.444\right)}{W} \right] \quad (\text{App.5.5})$$

Since the derivative of (App. 5.5) with respect to  $W$  is negative it's known that the attenuation per one wavelength  $\alpha$  increases with the decrease of  $W$ .

As a result, following conclusions can be drawn based on equations (App.5.3- App.5.5):

1. For fixed  $Z_0$ , frequency  $f$  and thickness  $H$ , the higher  $\epsilon_r$  the smaller is the width  $W$ , the larger is the attenuation per one wavelength.
2. For fixed  $Z_0$ , frequency  $f$  and dielectric constant  $\epsilon_r$ , the thicker substrate (larger  $H$ ) the larger is the width  $W$ , therefore the smaller the attenuation per one wavelength.

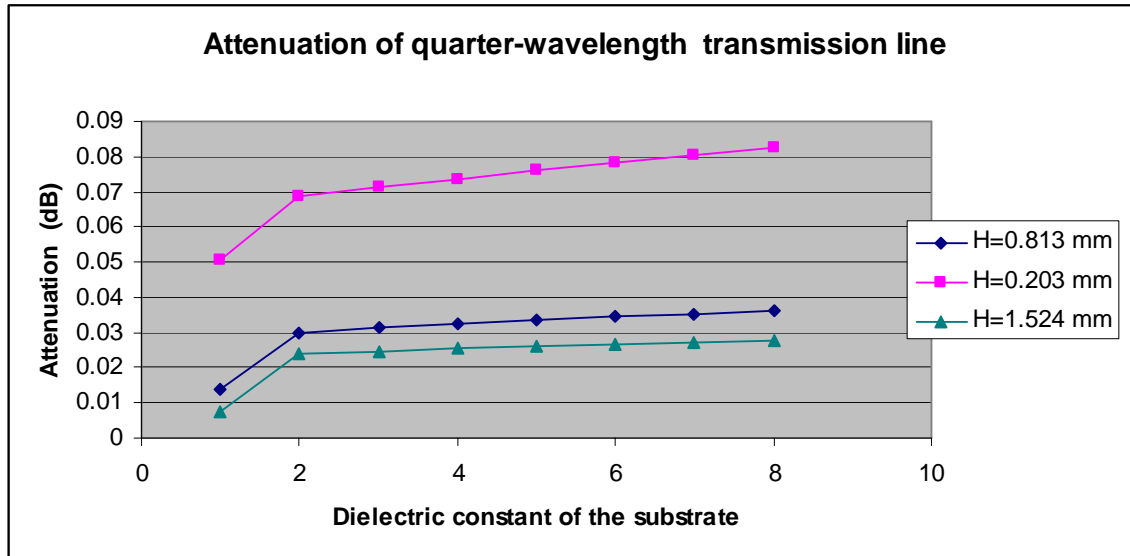


Fig. App.5.2 The simulation result of the attenuation of a 50-ohm quarter-wavelength microstrip on Rogers4003C substrate.

As a result, for the quarter-wavelength microstrip used in the combining network, thick substrate with low dielectric constant  $\epsilon_r$  should be chosen to keep the attenuation of the quarter-wavelength microstrip as small as possible. The simulation results shown in Fig. App.5.2 verify this conclusion about substrate choice. A 50-ohm quarter-wavelength microstrip on the Rogers4300C substrate with three different thicknesses is simulated at 2 GHz in “TXLINE” of Microwave office. As can be seen, the thickest substrate (H=0.813 mm) has the lowest attenuation and the attenuation increases with the increases of the dielectric constant of the substrate.

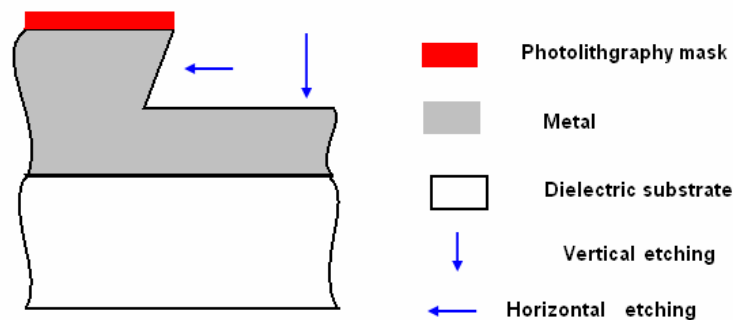


Fig. App.5.3 Illustration of the PCB etching.

## Metal foil thickness

The thickness of the metal foil doesn't really play a role in affecting the microstrip performance. There are three or five metal-foil-thickness choices for a certain type of PCB material. However, a thick metal foil will impose stricter demand on the photolithography aspect-ratio of the PCB process as shown in Fig. App.5.3. To define the metal region a mask is used to protect it from etching. The region without the mask will be etched. However, every photolithography has a finite aspect-ratio. This means during vertical-etching of the unwanted metal region, the horizontal etching happens as well. The thicker is the metal foil the longer is the vertical-etching, which results more undercut and low-precision defined metal strip track.

Table. App.5.1 The microstrip track width and spacing standard of [5.3]

Thickness of Cu-foil (um)	Minimum track width/spacing (um)
9.0	100
17.5	150
35	300
70	500

As a result, to obtain the high-precision defined microstrip a thinner metal foil is desirable. For example, the thicker metal foil (Copper) the larger is the minimum track width provided by the microstrip fabrication service [5.3] shown in Table. 5.1.

In summary, to obtain low microstrip attenuation the substrate with low dielectric constant and higher thickness is preferred; to obtain high-precision defined microstrip lines thin metal foil on the substrate is preferred.

## 5.2 Choice of the microstrip trace topologies

In the theoretical analysis the quarter-wavelength transmission lines are connected directly at their terminals to the load by perfect wires shown in Fig. App.5.4a. On PCB inevitable discontinuities at bends, adjacent microstrip, and junctions can cause degradation in circuit performance. This is because such discontinuities introduce parasitic reactance that can lead to phase and amplitude errors, input and output mismatch, and crosstalk coupling. Their influence must be taken into account in the

microstrip combining network designing. Fig. App.5.4 takes an example of a 3-device balanced combining network to illustrate the PCB discontinuities. Fig. App.5.4b and Fig. App.5.4c shows two layout topologies for the combining network shown in Fig. App.5.4a.

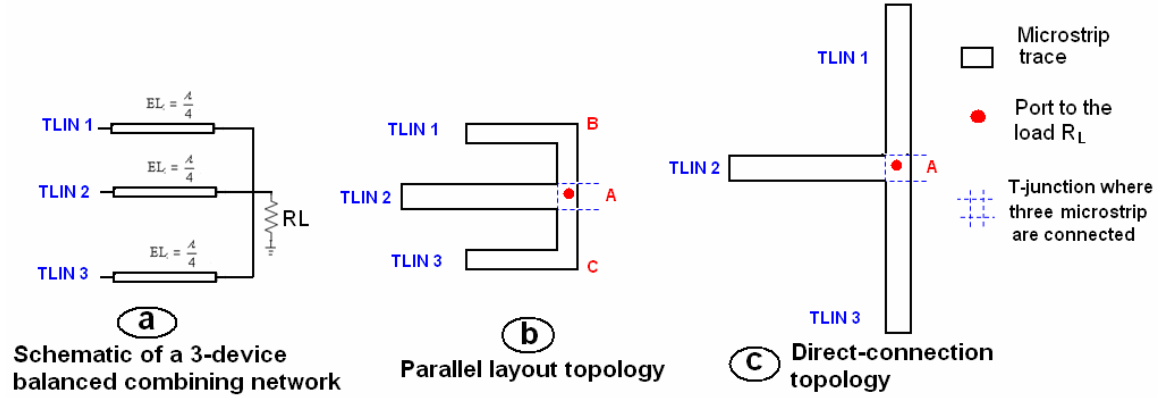


Fig. App.5.4 The schematic of layout topologies of a 3-device balanced combining network.

The three major discontinuities involved are listed:

1. Bends at region B and C in Fig. App.5.4b. In the parallel layout shown in Fig. App.5.4b the microstrip  $TLIN1$  and  $TLIN2$  are bended to save the dimension area of the board. Thus, compared with the direct-connection topology the additional discontinuities at bending region B and C are introduced. Besides that, the crosstalk coupling between  $TLIN1$ ,  $TLIN2$  and  $TLIN3$  are severer.
2. Crosstalk between  $TLIN1$ ,  $TLIN2$  and  $TLIN3$  especially in the parallel layout topology shown in Fig. App.5.4b.
3. T-junction A in both topologies. The microstrip component “T junction” has to be used to connect three microstrip traces to the load port.

Following the three major discontinuities are discussed.

### Right-angle bend and compensation methods

To save the board area a direct microstrip trace  $TLIN1$  can be bended shown in Fig. App.5.5. As a result  $TLIN1$  is divided into two short microstrip lines  $TLIN_{1A}$ ,  $TLIN_{1B}$  and the bend  $TLIN_{1Bend}$ . The straightforward right-angle bend shown in Fig. App.5.5b has a parasitic discontinuity capacitance caused by the increased conductor area near the

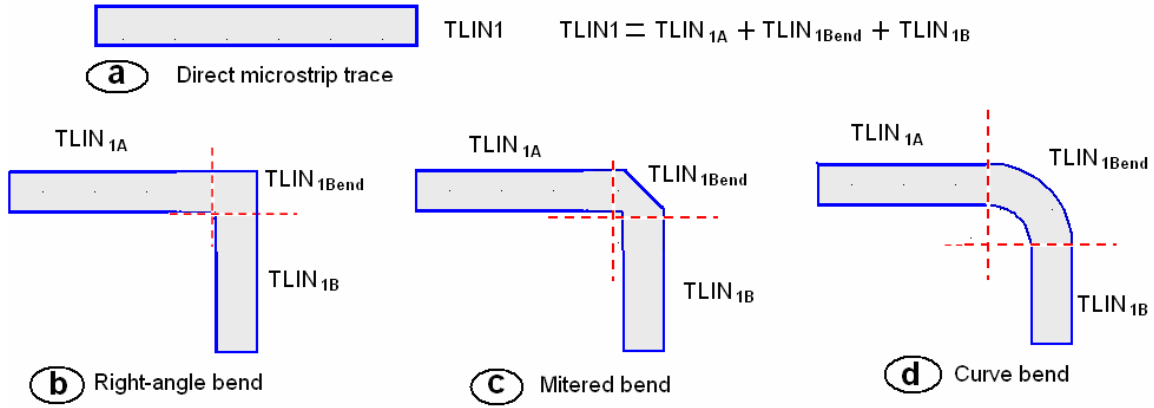


Fig. App.5.5 Three kinds of bends of a microstrip trace.

bend. Two adjusted alternative bends shown in Fig. App.5.5c and Fig. App.5.5d can be used to limit the discontinuities caused by the right-angle bend. As shown in Fig. App.5.5c, in the mitered bend certain amount of conductor is cut to reduce the parasitic capacitance. An optimal formula to design the mitered bend is given by [5.2]

$$M = 52 + 65 \times \left[ \exp\left(-1.35 \times \frac{W}{H}\right) \right] \quad (\text{App.5.4})$$

$$L = W \times \left( \frac{M}{50} - 1 \right) \quad (\text{App.5.5})$$

$$D = 100 \times \frac{X}{M} \quad (\text{App.5.6})$$

, where the parameters are referred in Fig. App.5.6.

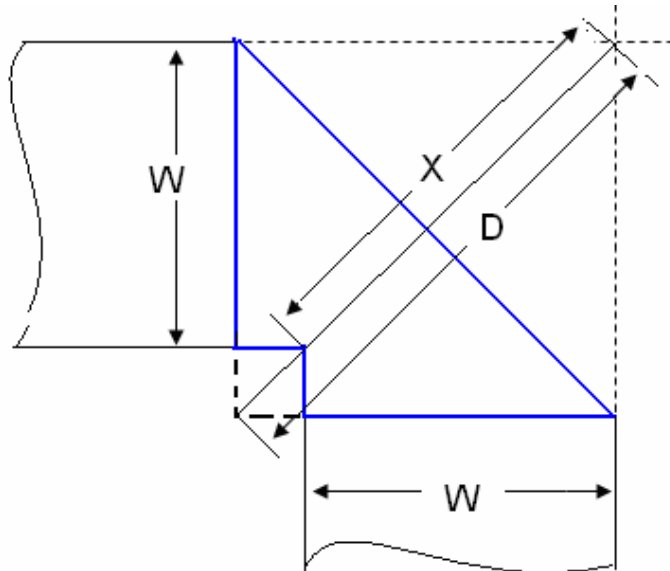


Fig. App.5.6 Illustration of the mitered bend.

Compared to the mitered bend the curve bend involves less parasitic since the width of the microstrip doesn't change at the bend. However, it takes more space as shown in Fig. App.5.5d.

To illustrate the discontinuities happening in different bends a 50-ohm quarter-wavelength microstrip on RO4300C <sup>1</sup> is bended in three ways, namely, right-angle, mitered, and curve shown in Fig. App.5.7. The microstrip lines are connected to a 100-ohm load and a sinusoid source with 50-ohm internal source impedance. Theoretically the input impedance  $Z_{in}$  is 25 ohm if the characteristic impedance  $Z_0$  of the microstrip is 50 ohm and the electrical length is 90 degree. Thus, the input impedance  $Z_{in}$  is used to illustrate the effect of the bend's discontinuities on the microstrip. Table 5.2 shows the simulation results. Notice even the input impedance  $Z_{in}$  converted by the microstrip with direct trace shown in Fig. App.5.7a has an imaginary part. This is because that the physical dimension accuracy of the microstrip is determined by the minimum line width of the process. In this work the dimension is rounded to 0.1 mm, which is the minimum line width provided by [5.3]. As can be seen for the bended trace, the input impedance  $Z_{in}$  all has imaginary part and the real part is not 25 ohm, which is the result of the discontinuities of the bends. The ratio between the real and imaginary part of  $Z_{in}$  can be

Table App. 5.2 Simulation results of the input impedance converted by the 50-ohm quarter-wavelength microstrip with different layout.

Microstrip trace	Real (Zin) (ohm)	Imag (Zin) (ohm)	Real (Zin)/Imag(Zin)
Direct	24.44	-0.3	81.72
Curve	23.71	-1.222	19.4
Mitered	25.61	3.146	8.139
Right-angle	22.5	3.628	6.202

<sup>1</sup> In the rest of this chapter the RO4003C substrate (0.0032" thickness and ½ OZ copper cladding) from Rogers are used in the simulation of ADS2005A and is referred to RO4300C.



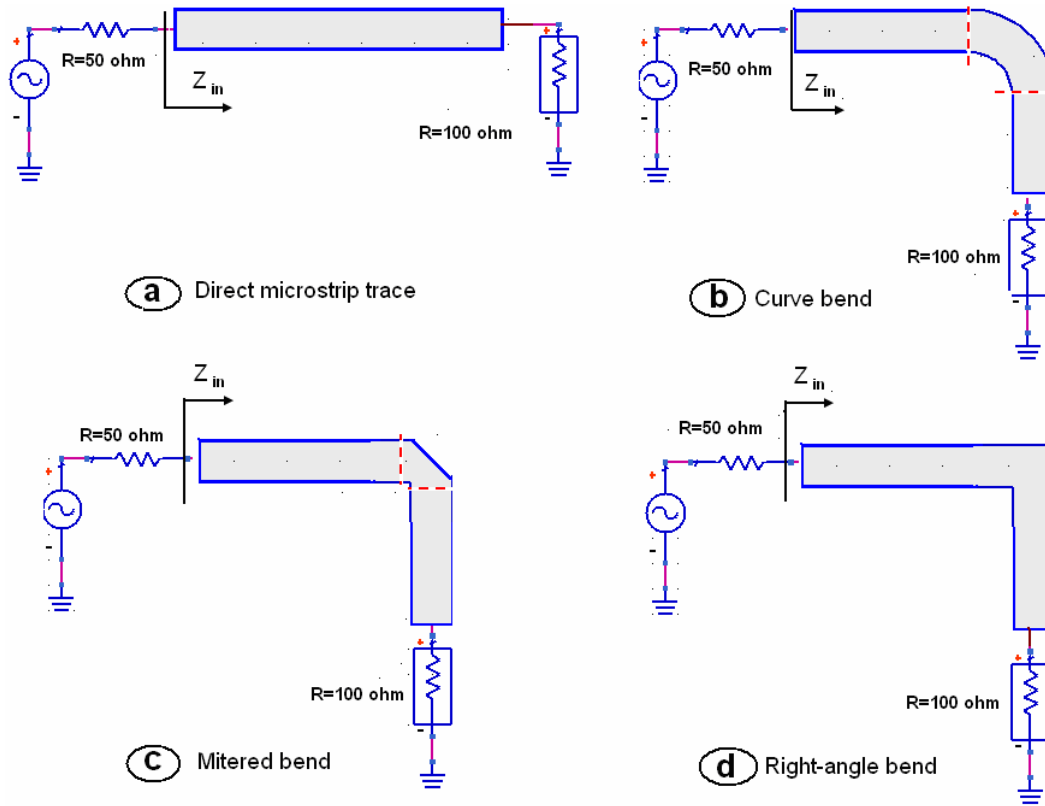


Fig. App.5.7 Schematic of the test circuit of bended quarter-wavelength microstrip lines.

used to compare the performance of three bended microstrip lines. The higher the ratio the less are the discontinuities involved in the microstrip. Obviously the right-angle bend without any compensation has the most discontinuities while the curve bend mitigate the bend discontinuities the most.

### Cross talk coupling

When two parallel microstrip lines are very close to each other, the cross talk between them will affect their characteristic. For example, *TLIN1*, *TLIN2* and *TLIN3* in Fig. App.5.4b have crosstalk between each other. The coupled line theory can be utilized to approximate the crosstalk effect on the microstrip lines in the combining network.

Usually two special types of excitations for the coupled line are considered as illustrated in Fig. App.5.8: the even mode, where the currents in the strip conductors are equal in amplitude and in the same direction, and the odd mode, where the currents in the strip conductors are equal in amplitude but in opposite directions. The characteristic impedance for each mode is given as follows [5.1]

$$Z_{0e} = Z_0 \sqrt{\frac{1 + 10^{C'/20}}{1 - 10^{C'/20}}} \quad (\text{App.5.7})$$

$$Z_{0o} = Z_0 \sqrt{\frac{1 - 10^{C'/20}}{1 + 10^{C'/20}}} \quad (\text{App.5.8})$$

, where  $C'$  is the coupling factor.

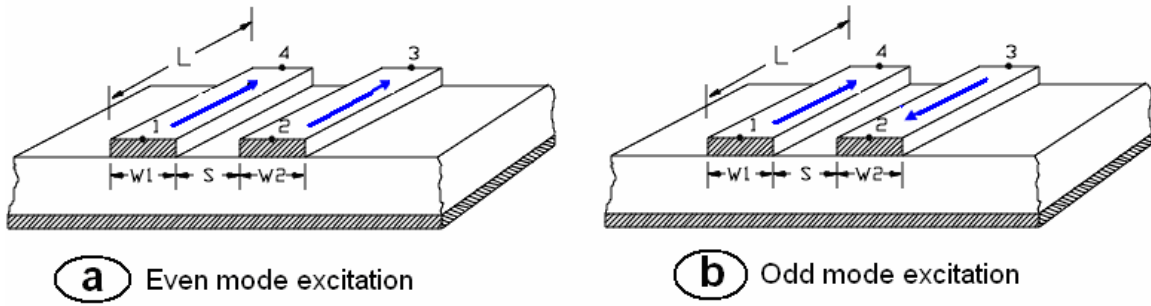


Fig. App.5.8 Illustration of even mode and odd mode coupling.

It's trivial that in the even mode coupling the characteristic impedance  $Z_{0e}$  is larger than the original characteristic impedance  $Z_0$  and in the odd mode coupling the characteristic impedance  $Z_{0o}$  is smaller than the original characteristic impedance  $Z_0$ . Therefore, for two closely parallel microstrip lines  $TLIN1$  and  $TLIN2$  shown in Fig. App.5.9 the characteristic impedance of them will increase resulting a higher input impedance  $Z_{in}$ . The circuit shown in Fig. App.5.9 is simulated to show the crosstalk effect on the characteristic impedance and electrical length of two adjacent identical 50-ohm quarter-wavelength microstrip lines. For an ideal 50-ohm quarter-wavelength transmission line the input impedance  $Z_{in}$  seen at the voltage source should be 25 ohm. Since the same current flow through both in  $TLIN1$  and  $TLIN2$  it's similar to the even mode coupling and it could be predicted that the characteristic impedance of  $TLIN1$  and  $TLIN2$  will increase. Fig 5.10 shows the changes of the imaginary and real part of input impedance  $Z_{in}$  caused by the changes of the distance  $S$  between  $TLIN1$  and  $TLIN2$ . The brown line denotes the ideal value when there is not any cross talk and the blue line shows the changes caused by the crosstalk. When the distance  $S$  between  $TLIN1$  and  $TLIN2$  is smaller than 3 mm both the real and imaginary part deviate from the ideal value even

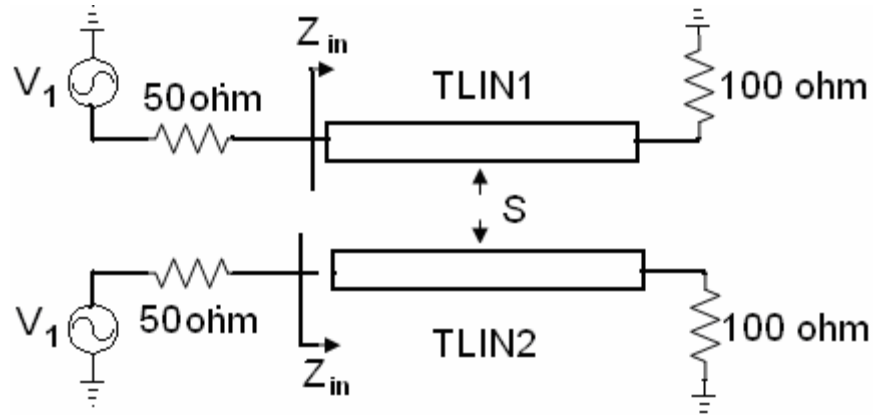


Fig. App.5.9 Bird eye view of two closely parallel 50-ohm quarter-wavelength microstrip lines.

worse. However, the crosstalk effective is not as bad as it sounds like. When the distance  $S$  between  $TLIN1$  and  $TLIN2$  are larger than 4mm the input impedance  $Z_{in}$  is near the ideal value, which means that the crosstalk effect could be neglected. Therefore, the spacing between two parallel microstrip lines is not necessarily very large, which could keep the board more compact.

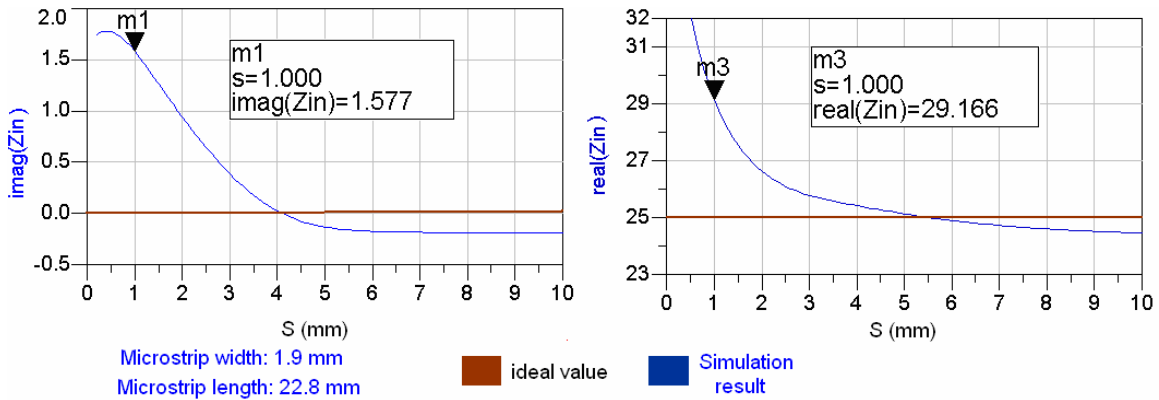


Fig. App.5.10 Simulation results of the input impedance  $Z_{in}$  for the 50-ohm quarter-wavelength microstrip line.

If the spacing needs to be very small the crosstalk effect could be compensated by adjusting the width and length of the microstrip lines. Equation (App.5.3) tells that increasing the width of a microstrip decreases the characteristic impedance  $Z_0$ , therefore, by increasing the width of the microstrip lines the cross talk effect could be minimized. For instance, when  $TLIN1$  and  $TLIN2$  are very close ( $S = 1 \text{ mm}$ ), the input impedance is quite different from the ideal value shown by marker 1 and 2 in Fig. App.5.10. By

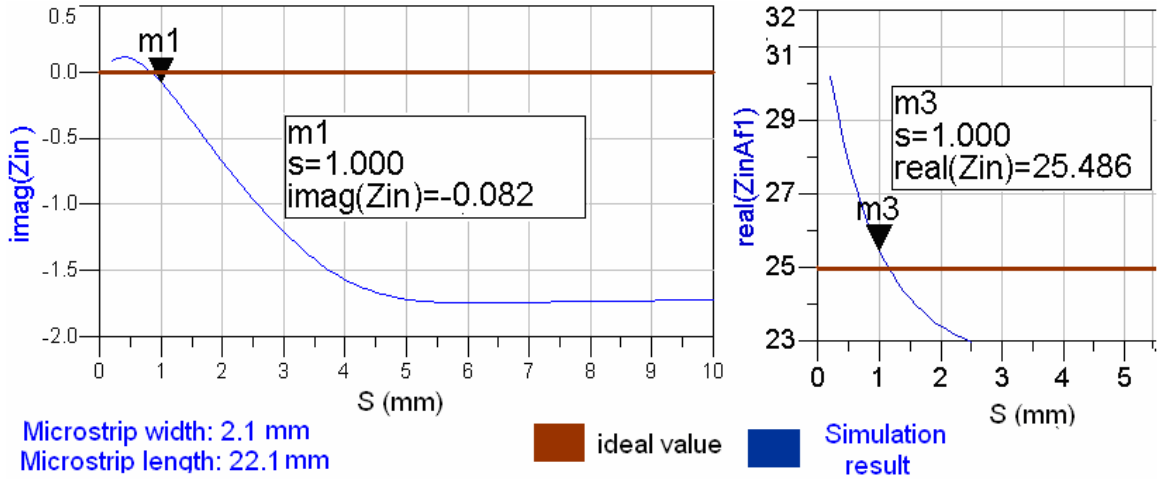


Fig. App.5.11 Simulation results of the input impedance  $Z_{in}$  for the 50-ohm quarter-wavelength microstrip line after dimension tuning.

increasing the width from the original value 1.9 mm to 2.1mm and tuning the length as well, marker 1 and 2 in Fig.App.5.11 show that the crosstalk effect on the input impedance are compensated.

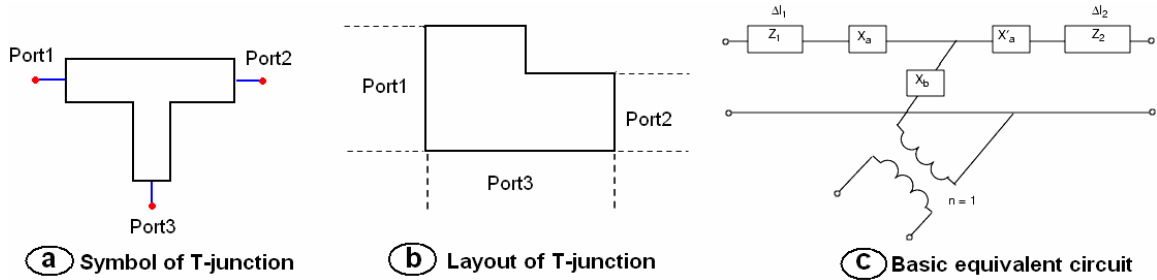


Fig. App.5.12 Illustration of the T-junction.

## T-junction

The T-junction shown in Fig. App.5.12 necessarily occurs in a wide variety of microstrip circuits. Examples range through stub-matching elements, stub filters, branch-line couplers. The elementary equivalent includes parasitic reactance and a transformer. Two compensation methods are shown in Fig. App.5.13 [5.1]. Since these component compensation methods are mostly based on experiments and no simple design formula are available. What's more, the width of the T-junction is dependent on the microstrip lines connected. The width of the microstrip lines is not fixed until the tuning of them is done, therefore, designing the T-junction based on the compensation methods without considering the tuning of the microstrip is not efficient and they are not used in this work.

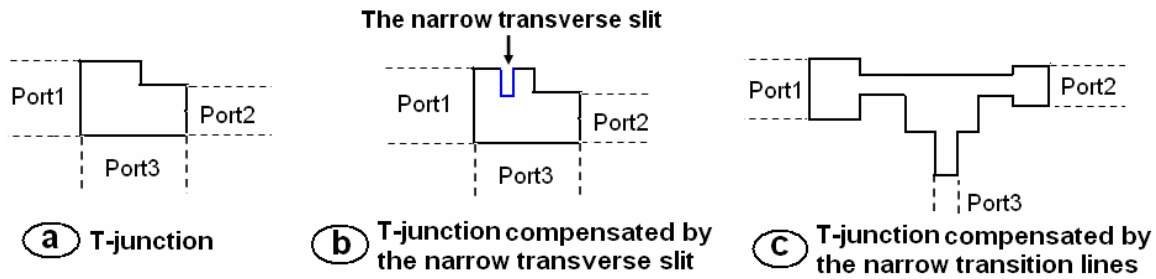


Fig. App.5.13 Illustration of the T-junction compensation.

In the design of the microstrip combining network layout the above-stated three discontinuities are interacted and makes the design complex. An efficient way to compensate the discontinuities is to tune all microstrip components in the combining network at the same time. For example, for the bend topology shown in Fig. App.5.4b the width and length of *TLIN1*, *TLIN2* and *TLIN3* are tuned together with the distance between them resulting the tuning of the T-junction. At the end the overall performance of the microstrip combining network is the only judgment to determine the optimal dimension parameters of the network.

### 5.2.3 Fabrication choice

In fact the PCB fabrication is not like IC fabrication which has various processes. The only concern of the PCB fabrication is the minimum line width and fabrication accuracy. These two process tolerances affect the minimum tuning resolution of the microstrip when adjusting the physical dimension.

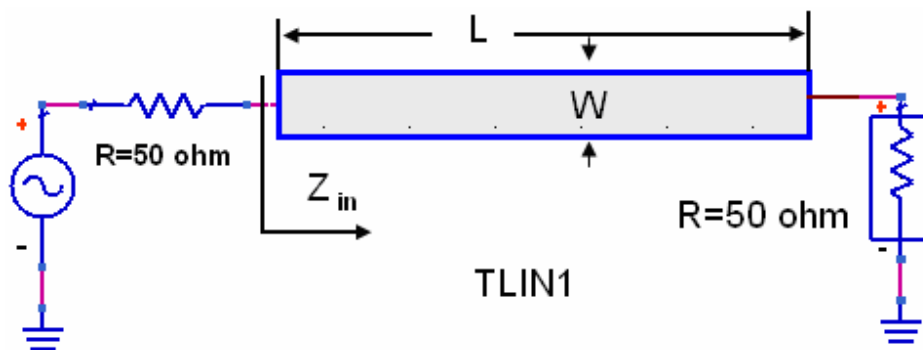


Fig. App.5.14 Schematic of the circuit with one microstrip line.

To illustrate the effect on tuning resolution the microstrip *TLIN1* is connected to a 50-ohm load and a sinusoid voltage source with a 50-ohm internal source shown in Fig. App.5.14. Suppose [5.3] provides the fabrication of the microstrip. Similar to the

previous example, the input impedance  $Z_{in}$  is used to determine the characteristic impedance and electrical length of  $TLIN1$ . The microstrip is designed to be a 50-ohm quarter-wavelength transmission line at 2 GHz. However, the length and width have to be rounded to 0.1 mm, which is the minimum line width of the fabrication process [5.3]. Thus the input impedance  $Z_{in}$  will never be equal to 50 ohm, which can be seen in the imagery part of  $Z_{in}$  in Fig. App.5.15.

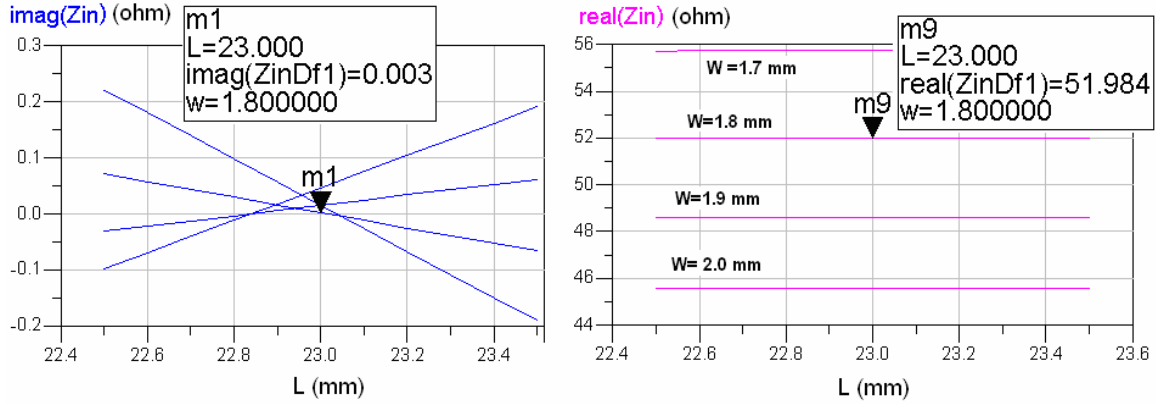


Fig. App.5.15 Simulation result of the  $Z_{in}$  for different width and length of  $TLIN1$ .

In the simulation the width and length of  $TLIN1$  are swept. The simulation results shown in Fig. App.5.15 tells at  $L = 23 \text{ mm}$  the electrical length is very close to 90 degree and the real part of  $Z_{in}$  is closest to the characteristic impedance of  $TLIN1$ . Thus the real part of  $Z_{in}$  at  $L = 23 \text{ mm}$  for different width is used to approximate characteristic impedance of  $TLIN1$ . Since the width can only be changed by the amount no less than 0.1mm, not any desired characteristic impedance can be achieved by tuning the physical width. Fig. App.5.15 shows that tuning the width from 1.7mm to 2.0mm can only achieve according four discrete characteristic impedance values.

In summary the minimum line width of the fabrication process sets an upper limitation for the design optimization. Fortunately, the minimum line width is generally good enough and doesn't impose big problems for the example designing in the next section.

## Appendix 6

### The measurement of microstrip lines

#### **6.1 Introduction**

As been discussed in chapter 4 any nonidealities involved in the quarter-wavelength transmission lines would introduce phase or amplitude nonidealities, which degrade the performance of the combining structure. In this work the quarter-wavelength transmission lines are implemented as the microstrip on PCB. How accurate the microstrip fabricated on PCB could be compared to its design value in the simulation tools is of interest in this chapter. While simulation tools allow helpful insights into predicting structure performance, more test and measurement tools are needed to measure and verify the actual parameters. Therefore, the measurements of the microstrip on PCB are useful to compare the actual parameter such as electrical length and characteristic impedance with the expected values. A few quarter-wavelength (at 2 GHz) microstrip lines with different characteristic impedance are designed and fabricated on RO4003C (0.0032" thickness and ½ OZ copper cladding) substrate by [5.3]. The measurement result of them is discussed in this chapter.

At first some important knowledge about RF measurements is introduced. Secondly, the discussion of the measurement methods of microstrip lines is given. Afterwards two ways to interpret the S parameter of microstrip lines are proposed. Finally the discussion on the measurement results ends this chapter.

#### **6.2 Basics of RF measurements**

##### **6.2.1 Calibration**

Every RF measurement needs calibration to remove the errors in the test setup before the device under test (DUT) is measured. The measurement calibration is a process which mathematically derives the error model and removes the error. For example, in Agilent network analyzer 8510C the error model is an array of vector coefficients used to establish a fixed reference plane of zero phase shift, zero magnitude and known impedance. The array coefficients are computed by measuring a set of "known" devices

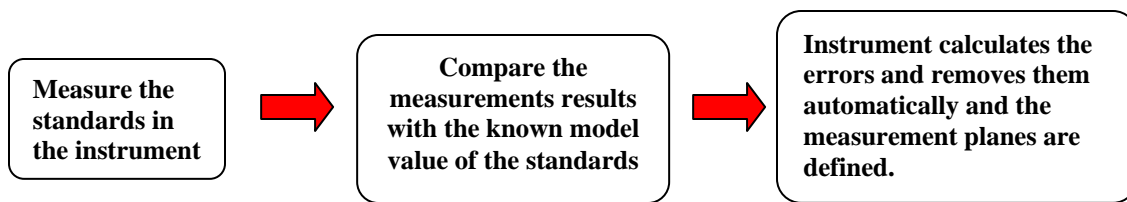


Fig. App. 6.1 Illustration of the calibration procedure.

connected at the fixed point and solving as the vector difference between the modeled and measured response. These “known” devices are called standards, which have a precisely known magnitude and phase response. Fig. App. 6.1 illustrates the basics of the calibration before the measurement of the DUT. After the calibration the measurement

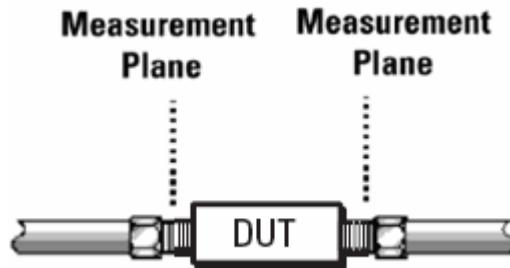


Fig. App. 6.2 The measurement planes are defined at the interfaces between the DUT and the instruments after the calibration.

plane is determined at the output ports of the instrument shown in Fig. App. 6.2. Defining the measurement plane is a key ingredient in the calibration process, because it is the point at which the instrument makes its measurement. Consequently, careful determination of this point ensures that undesired electrical characteristics that occur before the measurement plane are not included in the results. The measurement plane should ideally be at the RF connections of the DUT as shown in Fig. App. 6.2.

### 6.2.2 Classification of RF measurements

Generally the RF measurement instruments use coaxial cable with coaxial connectors such as SMA or N-type connectors to connect with DUT shown in Fig. App.6.3. Mostly the calibration standards provided along with the instruments are coaxial-connector-based as well and thus the measurement planes are defined at the coaxial connector ports. For example, Agilent network analyzer 8510C provides the calibration standards, namely,



SHORT, OPEN, LOAD and THRU(through) shown in Fig. App.6.4a. After the SOLT (Short-

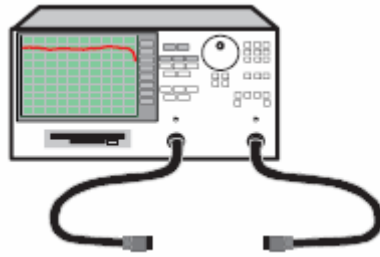


Fig. App.6.3 Illustration of the RF measurement instruments with coaxial cable and connectors.

Open-Load-Through)<sup>1</sup> calibration using the commercial calibration standards the measurement planes are defined right at the coaxial ports of 8510C shown in Fig. App. 6.4b [5.4]. Very accurate measurements can be made for the DUT with coaxial connectors by just connecting the DUT with the instruments directly shown in Fig. App.6.5. However, not every DUT has coaxial connectors with them such as microstrip

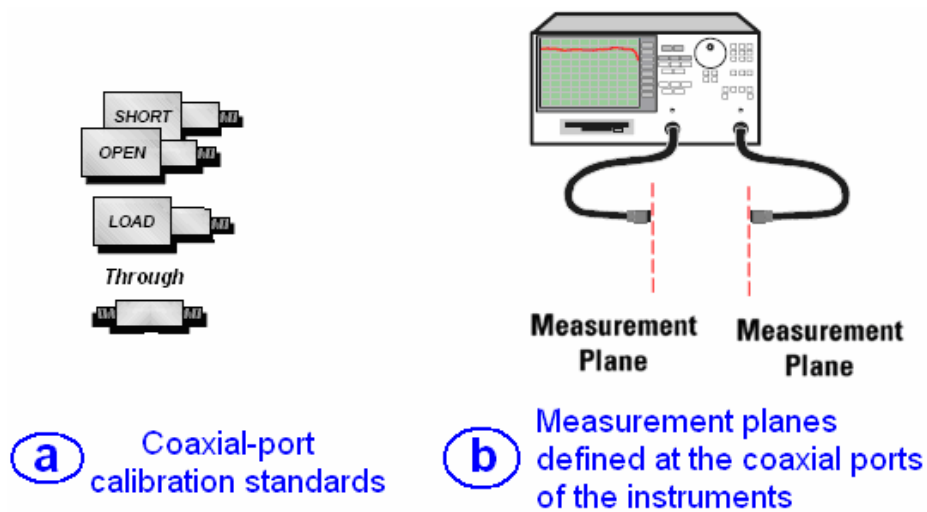


Fig. 6.4 Agilent network analyzer 8510C after the measurement planes being defined and the commercial calibration standards.

and SMD (surface-mounted-device) components. Therefore, in terms of the type of DUT's connectors the RF measurements is categorized into two groups in this work:

1. **Coaxial DUT.** DUT with coaxial connectors.

<sup>1</sup> SOLT is the standard calibration procedure for 8510C the detail information can be found in [6.1].

2. **Non-coaxial DUT.** DUT without coaxial connectors such as microstrip and SMD components.

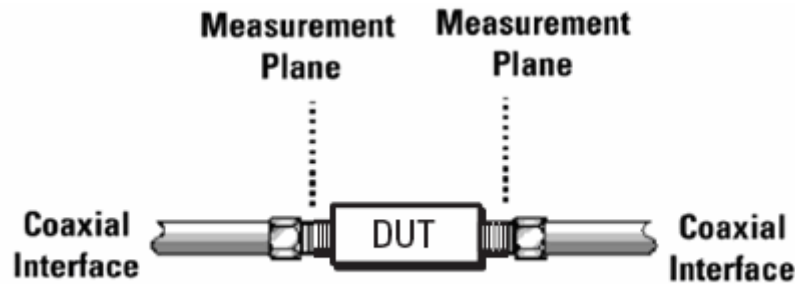


Fig. App. 6.5 Illustration of the DUT with connectors being tested.

Table App.6.1 shows the difference in the test requirements between coaxial DUT and non-coaxial DUT. As can be seen, making quality RF measurements on devices with standard coaxial connectors is relatively easy. Devices without connectors are difficult to measure since some sort of test fixture is required additionally to provide electrical and mechanical connection between DUT and the coaxial-connector-based test equipment [5.5]. In the next chapter the test fixture will be discussed.

Table App. 6.1 comparisons of the test requirements between DUTs with coaxial connectors and without coaxial connectors.

	<b>Coaxial DUT</b>	<b>Non-coaxial DUT</b>
<b>Test Requirements</b>	<ol style="list-style-type: none"> <li><b>a.</b> No need of test fixture.</li> <li><b>b.</b> Coaxial calibration standards are needed and are available</li> </ol>	<ol style="list-style-type: none"> <li><b>a.</b> Test fixture is needed.</li> <li><b>b.</b> Non-coaxial calibration standards are needed but might not available.</li> </ol>

### 6.2.3 Test Fixture

#### Introduction

The test fixture is a transition from the coaxial environment of the instrument to the non-coaxial DUT. Ideally it should deliver the test RF signal without any distortion to the DUT. It should provide easy mechanical support to the DUT. For example, the DUT should be easily inserted in and removed out of the test fixture with good contacts. There are very expensive commercial test fixtures for the non-coaxial DUT from Agilent, Anritsu, Inter-Continental microwave and etc. Fig. App.6.6 shows two Agilent test

fixtures for SMD and microstrip respectively [5.6]. The commercial test fixtures are intended for manufacturing applications and allow quick insertion, alignment and clamping. They are very rugged and mechanically sophisticated, since many thousands of parts are expected to be inserted in the fixture over their lifetime. However, for R&D applications like in this work the PCB-based test fixture which is much simpler, cheaper and less rugged could be built although it produces less accurate measurement results of DUT.

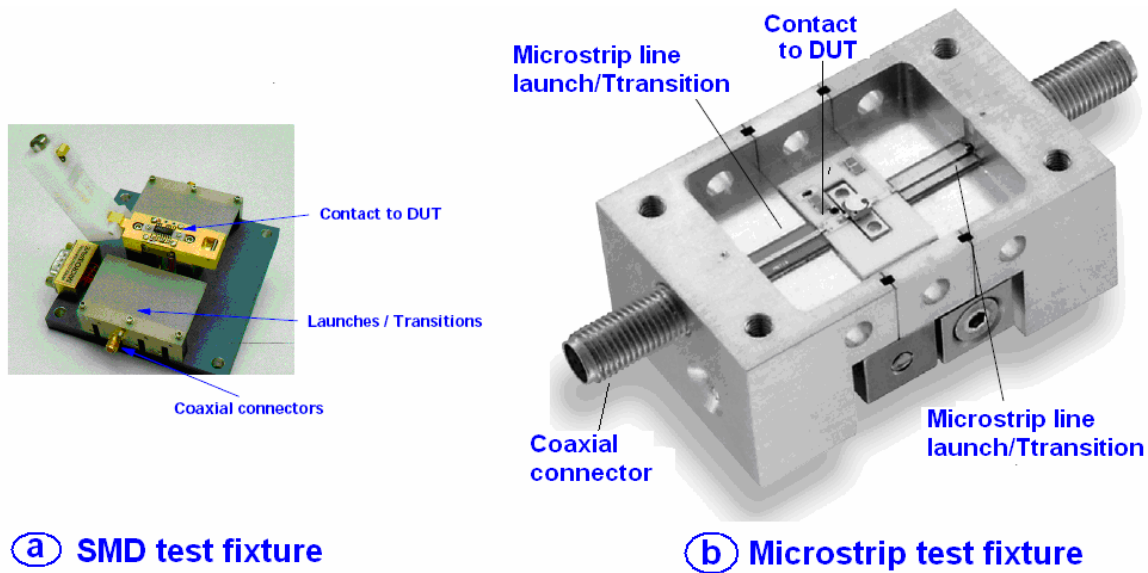


Fig. App. 6.6 Two examples of the non-coaxial DUT test fixture.

### Calibration concerns of the test fixture

Normally the calibration standards provided along with the instrument are coaxial-based and the measurement planes are defined at the interfaces between the instrument and the test fixture as shown in Fig. App.6.7. Therefore, the measurement results will include the region between the coaxial measurement plane and the DUT plane, which is the transition between the test fixture and the DUT. This is a new concern facing the non-coaxial DUT measurement. New non-coaxial calibration standards and procedure are necessary to calculate and remove the new error caused by the test fixture. Along with the commercial test fixture the non-coaxial calibration standards normally are provided. For example, in Agilent network analyzer 8510C the SOLT coaxial calibration defines the coaxial measurement planes at the coaxial interfaces shown in Fig. App.6.7. After SOLT the additional non-coaxial calibration procedure such as TRL or TRL\* will define the measurement plane further to the DUT plane by using the non-coaxial calibration

standards provided along with the commercial test fixture. Thus the errors brought by the fixture can be removed in the measurement of the non-coaxial DUT.

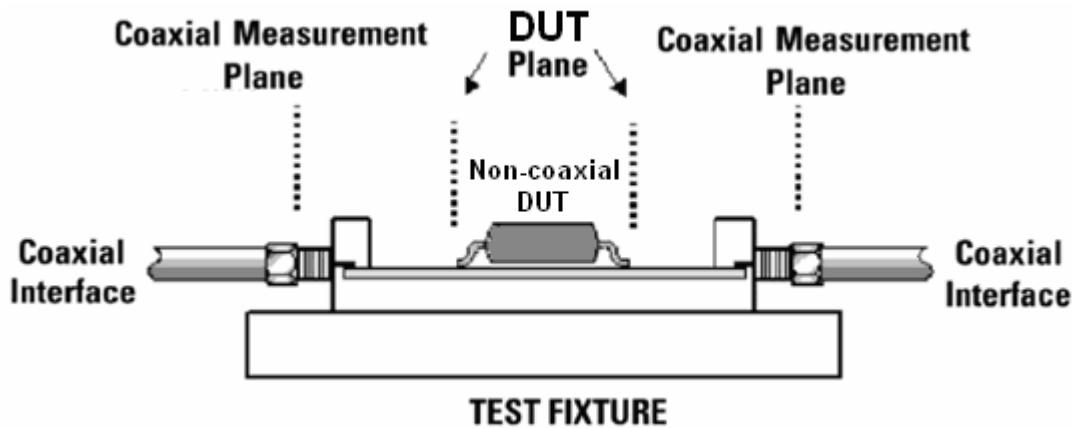


Fig. App. 6.7 The illustration of the defined measurement planes issue of the test fixture.

In case the commercial test fixture is not available the self-built non-coaxial calibration standards and test fixture are necessary. Normally the coaxial connectors such as SMA

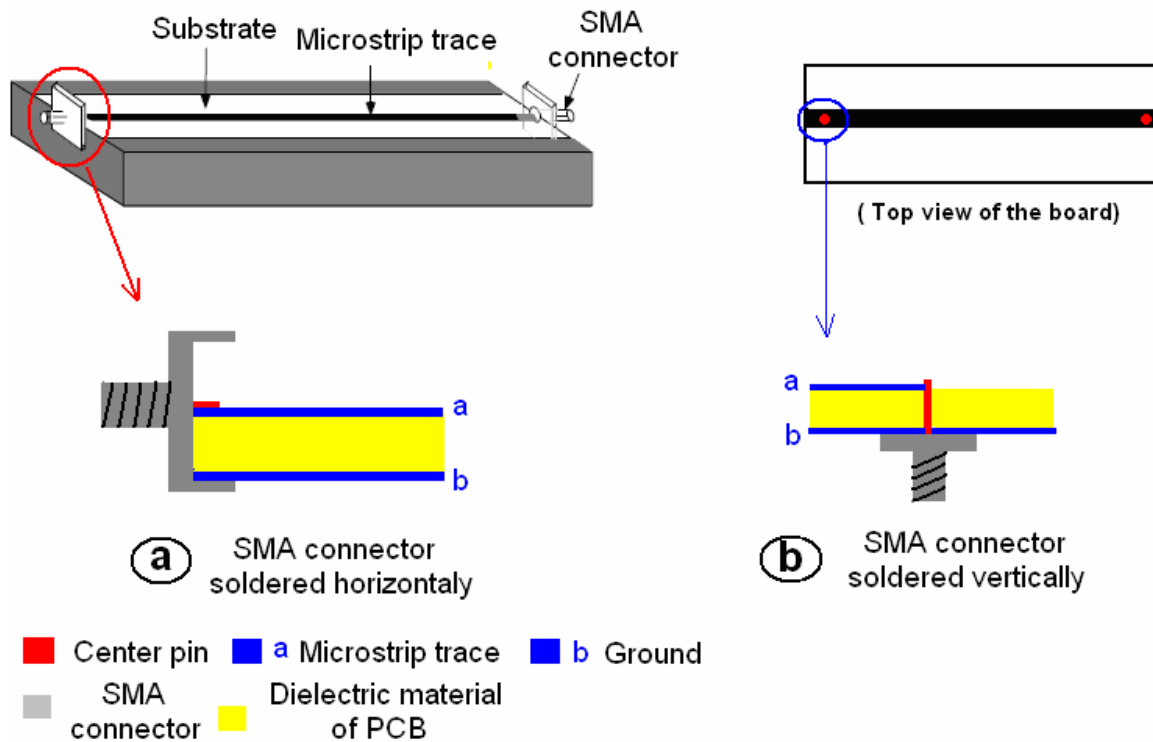


Fig. App. 6.8 Illustration of the coaxial-to-microstrip transition provided by the SMA connector.

connectors are soldered on the PCB with the microstrip to provide the coaxial-to-microstrip transition as illustrated in Fig. App.6.8. Most of the connectors are designed to be soldered horizontally shown in Fig. App.6.8a and some can be soldered vertically shown in Fig. App.6.8b.

### 6.3 Methods of microstrip measurements

Two kinds of instruments are available to measure the microstrip:

1. TDR (Time domain reflectometer) measurement.
2. S-parameter measurement.

Following these two measurements are discussed respectively.

#### 6.3.1 TDR measurement

TDR employs a step generator and an oscilloscope in a system which might be described as “closed-loop radar.” Refer to Fig. App. 6.9. In the operation, a voltage step is propagating down the coaxial cable to the DUT. As an impedance discontinuity is encountered in the DUT, some of the energy is reflected. Both the incident and reflected voltage waves are monitored on the oscilloscope at a particular point on the line [5.7]. Agilent 86100A Oscilloscope in this lab can provide TDR.

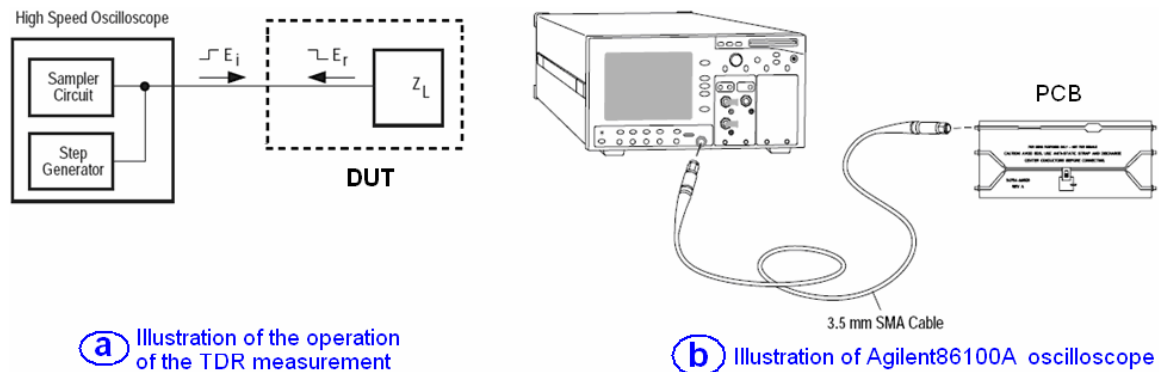


Fig. App. 6.9 Illustration of the operation of the TDR measurement and Agilent 86100A oscilloscope.

#### Normalization and impedance magnitude measurement

The calibration procedure of the TDR is called *normalization*. It utilizes the built-in software together with coaxial standards such as OPEN, 50-ohm-LOAD to remove the measurement errors and predict how the DUT will respond to an ideal step of the user-specified rising time. However, for the microstrip under test, the measurement reference

only can be defined in the interface between the SMA connector and the TDR as shown shown in Fig. App. 6.10. Fig. App. 6.10 is the TDR measurement result of a 50 ohm quarter-wavelength microstrip on RO4003C substrate with two 3.5mm SMA connectors soldered shown in Fig. App. 6.11. The yellow line is the response after normalization, which shows that

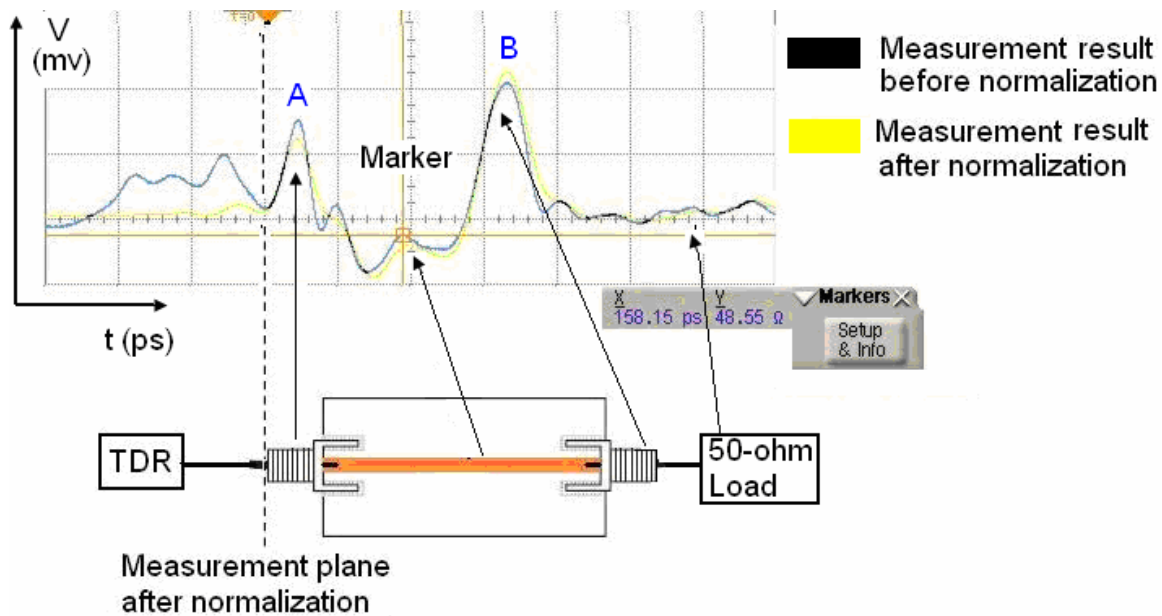


Fig. App. 6.10 TDR measurement result of the 50 ohm quarter-wavelength microstrip shown in Fig. App. 6.11.

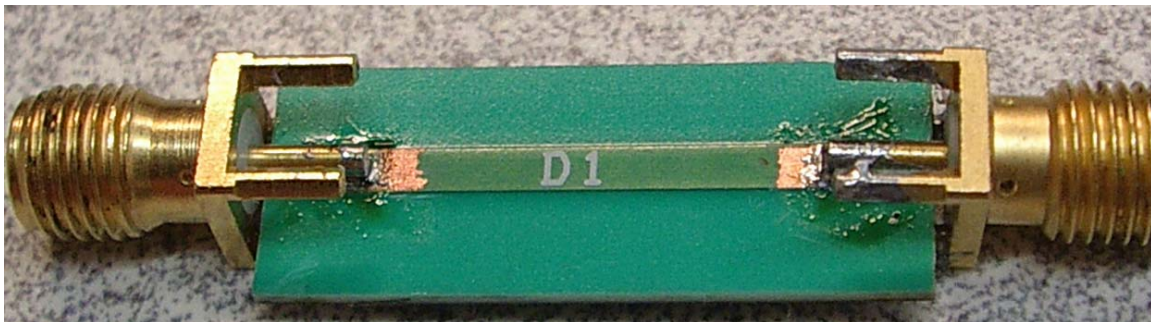


Fig. App. 6.11 The 50 ohm quarter-wavelength microstrip on Rogers4003 substrate with two 3.5mm SMA connectors soldered

the mismatch reflection within the TDR setup (before region A) is removed compared to the deep blue line. However, discontinuities caused by the two SMA connectors soldered on the PCB are included on the measurement result represented by the peak A and B. Between peak A and B is the response of the microstrip, the characteristic impedance of

which is shown by the marker. In this measurement the characteristic impedance is measured to be 48.55 ohm for this 50 ohm microstrip.

### Minimum electrical length resolution

Including the impedance magnitude TDR can also measure the time delay within the DUT. As shown in Fig. App. 6.10 the time can be defined at the X axis. However, the accuracy of the time delay between two adjacent discontinuities is determined by the rising time of the TDR system, which is explained in appendix 7.1 in detail. Equation (App. 7.2) gives the minimum electrical length can be defined by the TDR measurement ideally, which is rewritten:

$$EL = 180 \times f_0 \times t_{rise} \text{ (degree)}$$

(App. 6.1)

, where  $f_0$  is the operating frequency of the microstrip.

The fastest step of Agilent 86100A Oscilloscope that can be achieved with normalization is in the 15 to 35 picosecond range [5.8-5.10]. As a result, the ideal minimum electrical length of the microstrip can be defined by the TDR is around 10 degree. However, in practice two other more nonidealities degrades the resolution of the electrical length, namely,

- a. **Shooting time of the step voltage.** In appendix (7.1) the analysis is based on the assumption that the step input has no shooting time. Practically the transition between two discontinuities need more time to settle due to the shooting time of the step input.
- b. **Non-resistive discontinuity reflection.** In appendix 7.1 the analysis of (App. 6.1) is about the resistive impedance transition. However the SMA connectors soldered on the microstrip introduces complex discontinuities rather than resistive impedance transition. For example, the soldering tin brings inductance and capacitance at the discontinuities shown in Fig. App. 6.12.



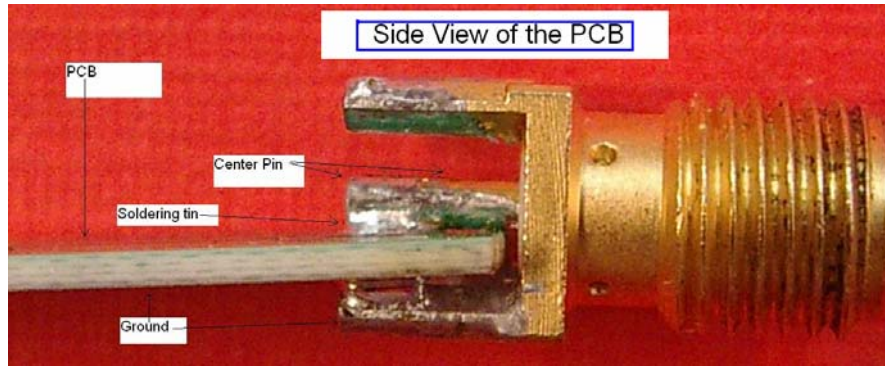


Fig. App. 6.12 Side view of the discontinuities of the SMA connector soldered on the microstrip board taken from the side.

As a result, the minimum electrical length can be defined is much larger than 10 degree. Notice that actually the two nonidealities stated above not only degrade the resolution of the minimum electrical length but also degrades the accuracy of the impedance measurement results. As can be seen in Fig. App. 6.10 the response between peak A and B is for the microstrip, however, the response is not flat as supposed and it's difficult to determine where the microstrip begins in the response. Therefore, TDR can not measure the electrical length of the microstrip with very high accuracy.

[5.10] mentions the additional instrument *Picosecond Pulse Labs 4020 TDR/TDT source enhancement module* could help Agilent 86100A improve the TDR edge speeds 35 ps to as fast as 9 picoseconds. However, the claimed improvement hasn't been verified in this work since this module isn't available.

### Summary of the TDR's capabilities

The capabilities of TDR are listed as follows [5.11]:

1. Reveal the characteristic impedance of the line under test.
2. Show both the position and the nature (resistive, inductive, or capacitive) of each discontinuity along the line.
3. Can't define the electrical length of the transmission line less than 10 degree.

### 6.3.2 S parameter measurement

Another way to measure the electrical length and characteristic impedance of the microstrip is S parameter measurement. In this work the S parameter of the microstrip with SMA connectors is measured by Agilent network analyzer 8510C and the electrical length and characteristic impedance can be calculated afterwards. Though this method is



indirect compared with the TDR higher resolution on the electrical length might be achieved.

### Fixture coaxial-microstrip transition errors

The coaxial-microstrip transition provided by the SMA connectors soldered on the PCB is the region between the coaxial measurement plane A and the DUT plane B illustrated in Fig. App. 6.13. The standard coaxial calibration procedure SOLT only defines the measurement plane at the coaxial measurement plane A. Directly measuring the S Besides, what is not illustrated in Fig. App. 6.13 is the inductance and capacitance brought by the SMA soldering as shown in Fig. App. 6.12, which includes more errors and will be shown in section 6.4.1.

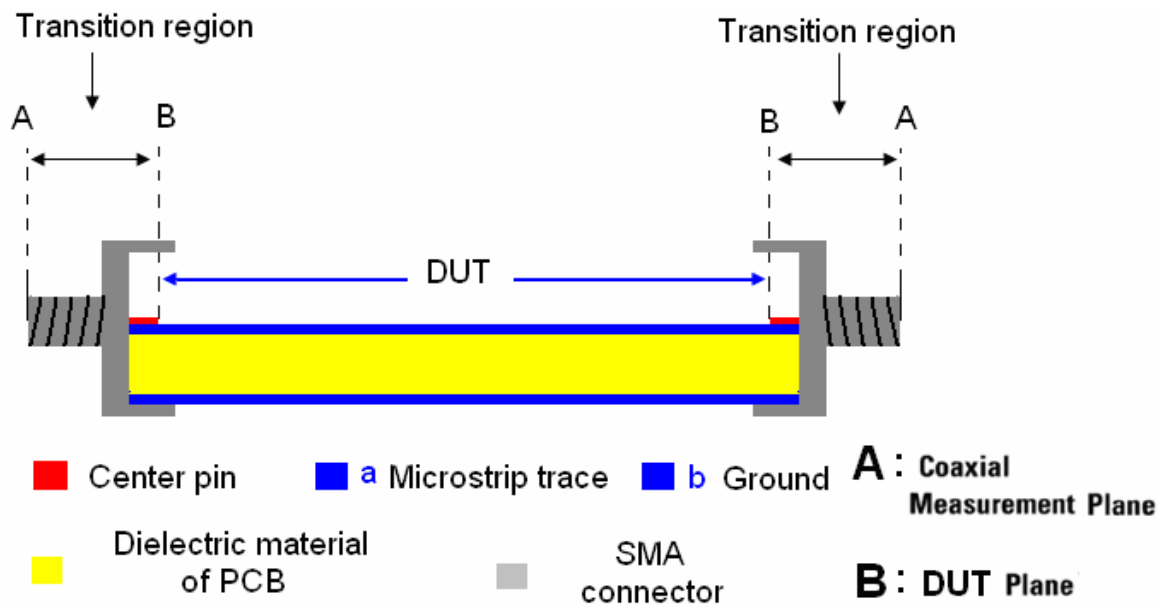


Fig. App. 6.13 Illustration of the transition provided by the SMA connectors.

There are two ways to remove the fixture errors, namely, de-embedding and direct measurement.

#### 1. De-embedding.

- Model the test fixture and de-embed it from the measurement.
- Measure S parameter of the test fixture and de-embed it from the measurement.

#### 2. Direct measurement. For example, TRL non-coaxial calibration.

### Removing fixture errors: De-embedding

Modeling the fixture can be the most accurate but it's the hardest to be realized. All of the non-linear effects such as dispersion, radiation and coupling that can occur in the fixture are needed to be included. Complex 3-D electromagnetic (EM) simulator, such as HFSS has to be used to calculate the fixture when the physical test fixture characteristics are modeled correctly in the simulator [5.19-5.21]. However, the physical test fixture characteristics can not be fully input in the simulator. For example, the vendors of the normal SMA connector only provide the dimension information but not the dielectric material information. How the SMA connector is soldered in the PCB and how much soldering tin is spread on the board can not be really modeled accurately.

Measuring the S parameter of the test fixture has been tried but not very good result comes out. The conclusion is that the S parameter of the test fixture without DUT is not the same as the test fixture with DUT. Therefore the S parameter is not accurate enough for de-embedding the test fixture. The details discussion can be found in appendix 7.2.

As a result the “**Direct measurement**” method is suggested to remove fixture errors.

#### **Removing fixture errors: Direct measurement TRL**

For fixtures that are not based on simple transmission lines, determining a precise model usually is harder than using the direct measurement method [5.5]. As shown in Fig. App. 6.13, after the coaxial calibration has defined the coaxial measurement plane at the interface between the fixture and the network analyzer, non-coaxial calibration can be used to remove the error of the transition region and define the measurement plane on the DUT plane as shown in Fig. App. 6.13. Direct measurement usually involves measuring non-coaxial calibration standards and calculating error terms. It has the advantage that the precise characteristics of the fixture do not need to be known beforehand. They are measured during the calibration process. However, the accurate non-coaxial standards have to be built by the researcher themselves. Though theoretically non-coaxial SOLT calibration standards can be built, which are SHORT, OPEN, LOAD and THRU, it's actually more difficult to build impedance standards that are easily characterized. In microstrip, for example, short circuits are inductive, open circuits radiate energy and it's difficult to build a high quality purely resistive load. Because of these limitations, an alternative method named TRL (THRU-REFLECT-LINE) for calibration in non-coaxial environments is suggested in [5.5-5.6] for non-coaxial DUT such as microstrip and SMD

component.

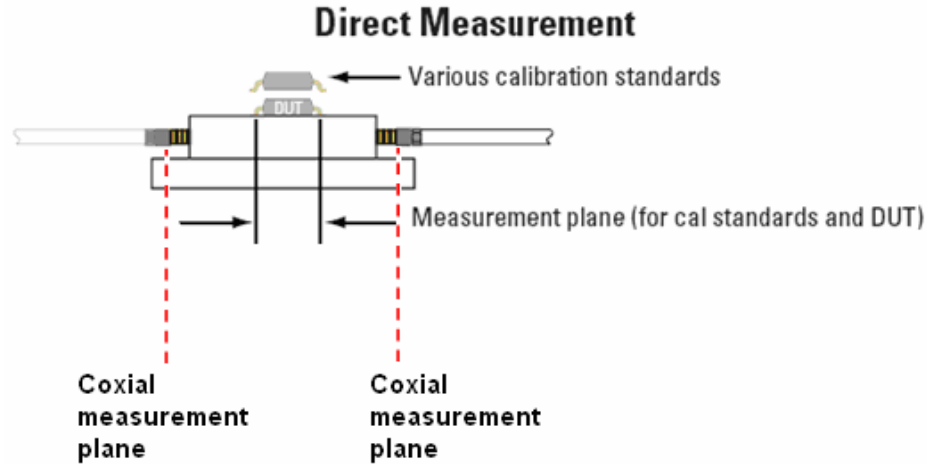


Fig. App. 6.13 Illustration of the "direct measurement" method to remove the test fixture error.

TRL only relies on transmission lines rather than a set of discrete impedance standards, which are listed as follows [5.5-6.6] (Referring to Fig. App. 6.14) :

1. **THRU**. A short length of transmission line between port 1 and port 2, zero length is also a choice if it is feasible.  $Z_0$  of the THRU must be the same as the LINE. The electrical length must be specified to set the DUT measurement plane. Attenuation of the THRU need not be known.
2. **REFLECT**. The identical one-port high reflection coefficient standards used to connect to each port (typically open or short circuits).
3. **LINE**. A short length of transmission line that is inserted between port 1 and 2.  $Z_0$  of the LINE establishes the reference impedance of the measurement. The optimal length is a quarter wavelength longer than the THRU at the center frequency. The insertion phase difference between the THRU and LINE must be between 20 and 160 degrees.

More detail about TRL calibration procedure can be found in [5.5-6.6] and [5.12-5.16].

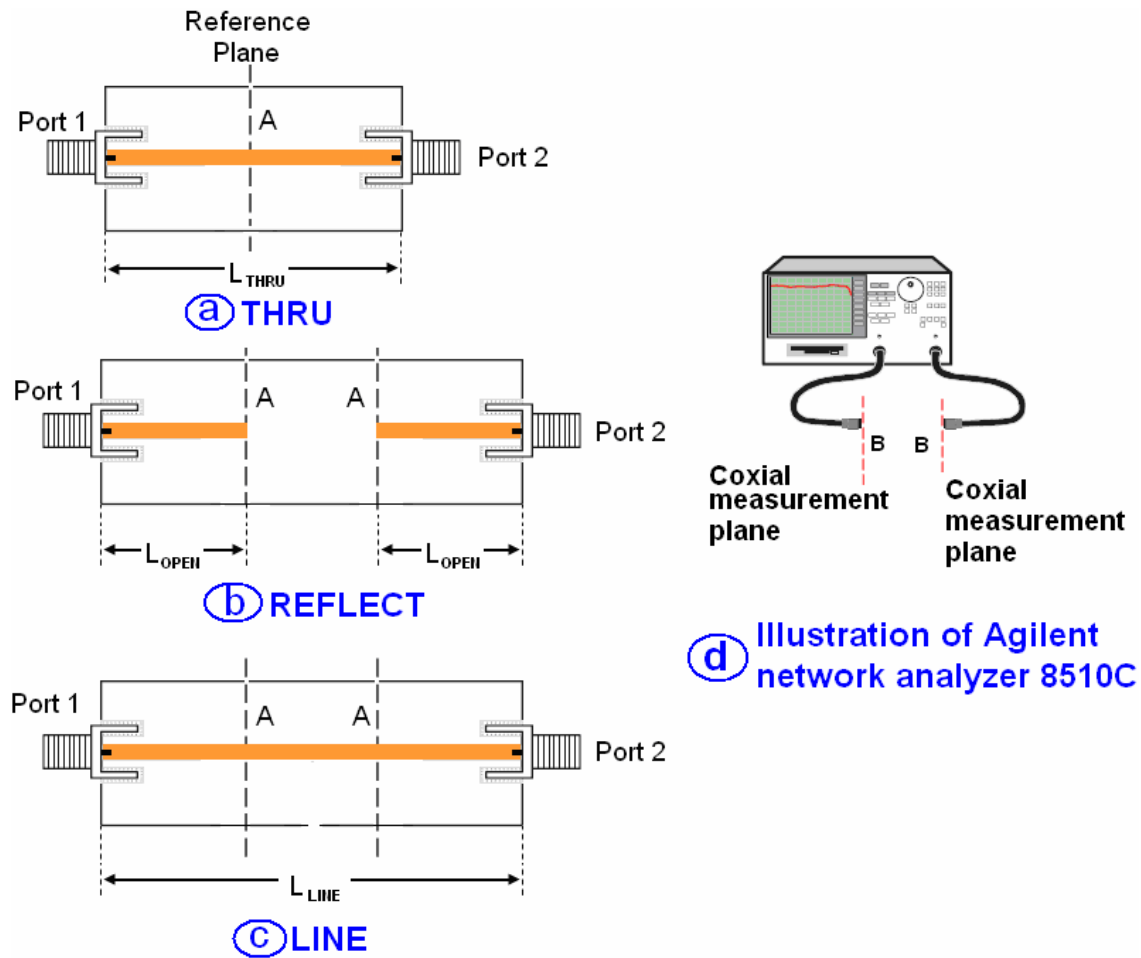


Fig. App. 6.14 Microstrip TRL standards.

Fig App. 6.14 illustrates the three microstrip TRL non-coaxial standards, namely, THRU, REFLECT and LINE. The TRL calibration procedure is given as follows:

1. Conduct the coaxial SOLT calibration for the network analyzer shown in Fig. App. 6.14d and the coaxial measurement planes are defined at Plane B.
2. Connect THRU, REFLECT and LINE shown in Fig. App. 6.14a, b and c respectively to the network analyzer in Fig. App. 6.14d to conduct TRL calibration.
3. The characteristic impedance of these three standards should be designed to be 50 ohm since the reference impedance of the measurement is set by that.
4. The length of the LINE is a quarter wavelength longer than that of the THRU, which is given by

$$L_{LINE} - L_{THRU} = \frac{\lambda}{4}$$

(App. 6.2)

5. The length,  $L_{open}$ , of the REFLECT (open microstrip) should be the same as The length of the THRU,  $L_{THRU}$ .
6. The length value of the THRU,  $L_{THRU}$ , is input to the network analyzer during TRL calibration to define the reference plane A.

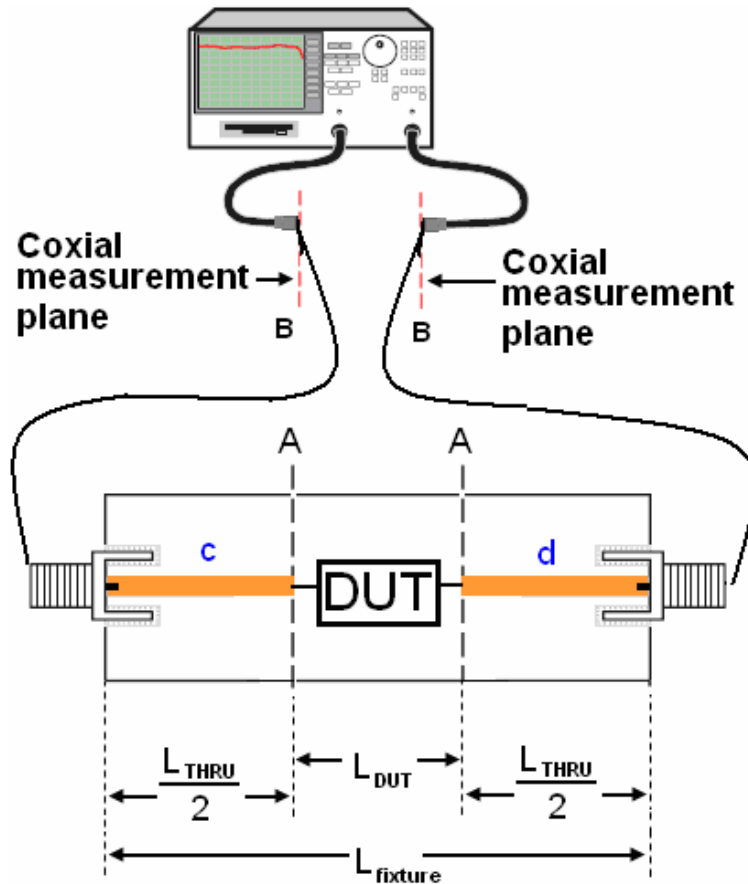


Fig. App. 6.15 Test Fixture for non-coaxial DUT after TRL calibration

After the TRL calibration the measurement will start at the reference plane A defined by the THRU. Fig App. 6.15 illustrates the test fixture for non-coaxial DUT after TRL calibration. The S parameter of the DUT could be achieved by directly connecting the test fixture to the network analyzer. Since the measurement plane starts from plane A the S parameter obtained in the network analyzer right now is purely from DUT without

involvement of the test fixture. For different DUT the length of the test fixture is changing, which is given by

$$L_{\text{fixture}} = L_{\text{THRU}} + L_{\text{DUT}} \quad (\text{App. 6.3})$$

and the characteristic impedance always be the same of the THRU. Fig. App. 6.16 shows two test fixture examples for two different microstrip lines. Microstrip B in Fig. App. 6.16a has the same width as that of the test fixture while Microstrip E's is different.

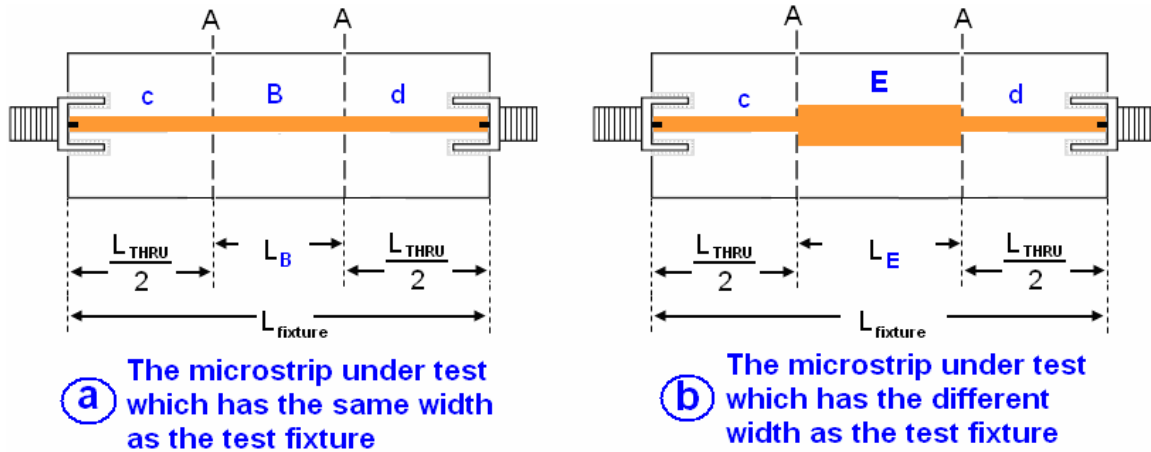


Fig. App. 6.16 Two test fixture examples of after TRL calibration.

### Practical concerns

1. Since the measurement reference impedance is defined by the characteristic impedance of the LINE, any difference between  $Z_0$  of the LINE and 50 ohm will introduce errors into the measurement.
2. The DUT at the test fixture should be exactly at the reference plane A defined by the THRU since the measurement will start from the reference plane A. The error position of plane A will introduce electrical length error for microstrip B but cause both the electrical length and  $Z_0$  errors for microstrip C. Since any shift of the plane A only changes the length of microstrip B but introduces two step discontinuities to microstrip E if the plane A is shifted shorter.
3. The SMA connectors must be consistent on all standards and fixtures. Substrate and connector grounds must be void of gaps and cracks. An illustration of good connector soldering can be found in [5.14] show in Fig. App. 6.17. However, due

to the hand-soldering to build the non-coaxial standards, this practical issue always exists and is the price for the cheap self-made test fixture.

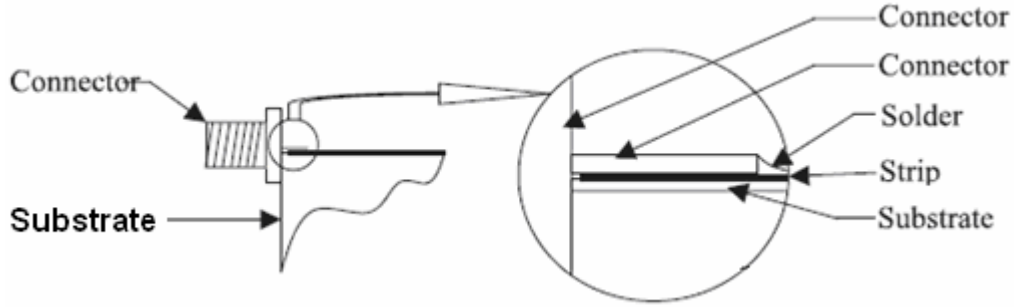


Fig. App. 6.17 Illustration of good soldering connector [5.14].

## 6.4 Interpretation of $S$ parameters for microstrip

After the network analyzer measurement of the microstrip is finished the  $S$  parameters need to be converted to the parameters of interest such as characteristic impedance  $Z_{TL}$  and electrical length  $EL$ . In this section two ways to interpret the  $S$  parameter for microstrip are proposed, namely

1. Using  $S$  matrix at one frequency to interpret  $S$  parameter.
2. Using periodic character of  $S$  parameter to interpret  $S$  parameter.

### 6.4.1 The interpretation using $S$ matrix at one frequency

In appendix 7.3 the relationship between  $S_{11}$ ,  $S_{21}$  with  $Z_{TL}$  and  $EL$  for an ideal transmission line are derived in (App.7.42), (App.7.43), (App.7.55), and (App.7.56), which are rewritten as follows:

#### 1. Determine $Z_{TL}$ and $EL$ by $S_{11}$

$$Z_{TL} = 50 \times \sqrt{\frac{\cos \theta + |S_{11}|}{\cos \theta - |S_{11}|}}$$

(App. 6.4)

$$EL = \beta l = \begin{cases} \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] & \text{when } \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] > 0 \\ \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] + \pi & \text{when } \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] \leq 0 \end{cases}$$

(App. 6.5)

, where  $S_{11} = |S_{11}| \angle \theta$ . The quadrant angle of  $EL$  in (App. 6.5) can be identified in Fig. App. 6.18.

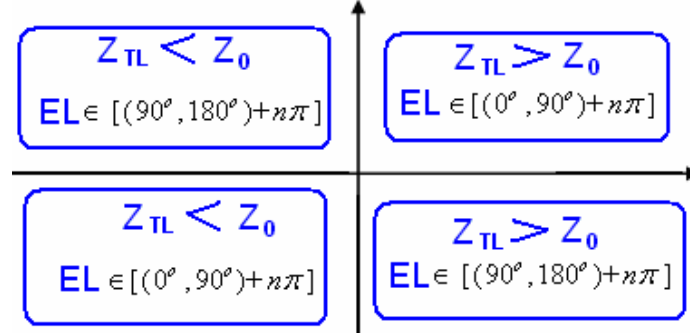


Fig. App. 6.18 The quadrant phase angle of  $S_{11}$  determined by  $EL$ ,  $Z_{TL}$  and  $Z_0$ .

## 2. Determine $Z_{TL}$ and $EL$ by $S_{21}$

$$Z_{TL} = \begin{cases} Z_0 \sqrt{\frac{\tan(\angle S_{21}) + \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}{\tan(\angle S_{21}) - \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}} \\ or \\ Z_0 \sqrt{\frac{\tan(\angle S_{21}) - \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}{\tan(\angle S_{21}) + \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}} \end{cases} \quad (\text{App. 6.6})$$

$$\tan \beta l = \frac{-2Z_0 Z_{TL} \tan(\angle S_{21})}{(Z_{TL}^2 + Z_0^2)} \quad (\text{App. 6.7})$$

Ideally only a set of S parameter at one single frequency is enough to calculate  $Z_{TL}$  and  $EL$  and (App. 6.4-App. 6.7) only need to be used once. However, in reality the S parameter spreads in a certain range. The wide distribution of the S parameter requires many times usage of (App. 6.4-App. 6.7). Besides, the best way to process the measurement data is to use the data which covers as broad range as possible, since by averaging the data in a large quantity the error caused at certain single point could be compensated. Therefore, the accurate



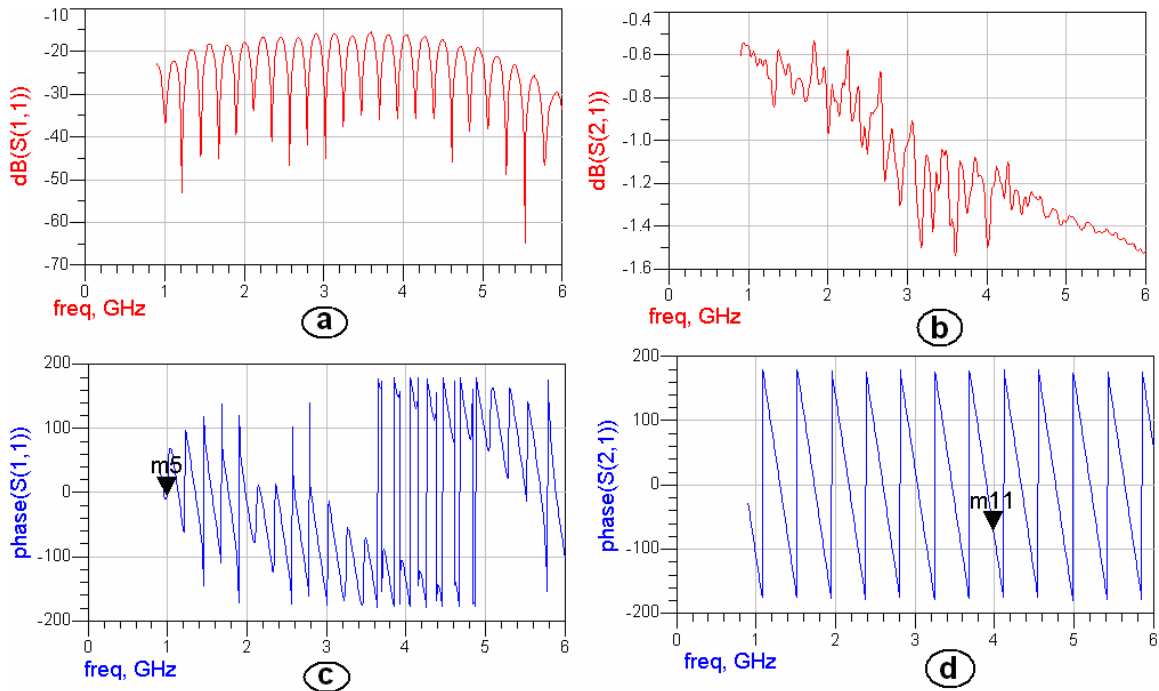


Fig. App. 6.19 The S parameter of a commercial coaxial cable measured in 8510C. characteristic impedance  $Z_{TL}$  and electrical length  $EL$  of the transmission line can not be obtained by using (App. 6.4-App. 6.7) only once at one single frequency. For example, a commercial coaxial cable is measured in 8510C<sup>2</sup> and the results are shown in Fig. App. 6.19. It's expected from (App.7.45), (App.7.46) and (App.7.52) that the minimum or maximum value of the magnitude of  $S_{11}$  or  $S_{21}$  should stay the same. It can be seen that the real measurement result involves some errors and make it difficult to utilize (App. 6.4-App. 6.7).

#### 6.4.2 The interpretation using periodic character of S parameter

It's observed that the periodic characteristic is well kept in the measurement result as it's expected from (App.7.45), (App.7.46) and (App.7.52), although the magnitude information is degraded by the measurement error. The electrical length can be easily calculated by finding out the period of the S parameter.

<sup>2</sup> Measuring frequency range is from 0.9 GHz-6.0 GHz and the sampling point is the maximum setting, 801 points. The S parameter measurement result is exported in the default "citifile" format to the floppy disk and then imported into ADS directly by using the component "SN2P" in "Data items" palette. There is no need to convert "citifile" format into standard "touchstone" format. ADS enables the import and export of S parameter files very convenient and fast.

The equations of  $S_{11}$  or  $S_{21}$  derived in appendix 7.3 and rewritten as follows for better illustration:

$$\tan(\angle S_{11}) = \frac{2Z_0 Z_{TL}}{\tan \beta l \times (Z_{TL}^2 + Z_0^2)} \quad (\text{App. 6.8})$$

$$|S_{11}| = \frac{|\tan \beta l \times (Z_{TL}^2 - Z_0^2)|}{\sqrt{(\tan \beta l)^2 \times (Z_{TL}^2 + Z_0^2)^2 + 4Z_0^2 Z_{TL}^2}} \quad (\text{App. 6.9})$$

$$\tan(\angle S_{21}) = \frac{-\tan \beta l \times (Z_{TL}^2 + Z_0^2)}{2Z_0 Z_{TL}} = \frac{-\sin \beta l \times (Z_{TL}^2 + Z_0^2)}{2Z_0 Z_{TL} \cos \beta l} \quad (\text{App. 6.10})$$

$$|S_{21}| = \frac{2Z_0 Z_{TL}}{\sqrt{(\sin \beta l)^2 \times (Z_{TL}^2 + Z_0^2)^2 + 4Z_0^2 Z_{TL}^2 (\cos \beta l)^2}} \quad (\text{App. 6.11})$$

$$\text{Note that the electrical length } EL = \beta l = f \times \frac{2\pi L}{c} \quad (\text{App. 6.12})$$

which means the electrical length of a certain transmission line changes periodically with the frequency.

Equations (App. 6.8-App. 6.11) tell following information:

1.  $|S_{11}|$  reaches its minimum value when  $EL = \beta l = K\pi$  ( $K$  is an arbitrary positive integer<sup>3</sup>). The frequency difference between two adjacent minimum points is the frequency period of  $|S_{11}|$ ,  $f_T$ . Based on (App.6.46) the electrical length at frequency  $f_0$  is given by

$$EL(\text{degree}) = f_0 \frac{180^\circ}{f_T} \quad (\text{App. 6.13})$$

the electrical length is half-wavelength at the frequency where the first minimum point locates. Fig. App. 6.20 is the simulation result of a 30-ohm microstrip on RO4003C (0.0032" thickness and 1/2 OZ copper cladding) designed in ADS2005A. In Fig. App. 6.20a it can be found at the first glance that at 2 GHz locates the first trough and the period  $f_T$  is 2 GHz, therefore this microstrip is quarter-wavelength at 1 GHz.

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<sup>3</sup> Obviously zero electrical length is of no practical interest and  $K = 0$  is out of consideration.

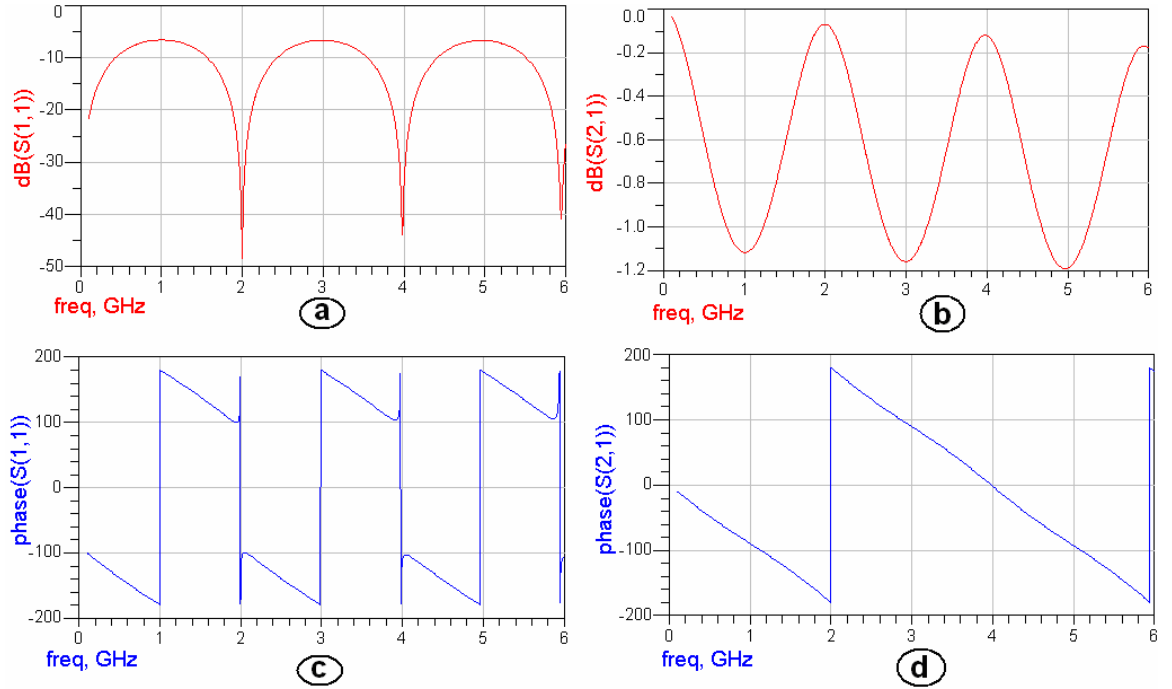


Fig. App. 6.20 The simulation S parameter of a 30-ohm microstrip.

2. The phase of  $S_{11}$ ,  $\angle S_{11}$ , reaches zero when  $EL = \beta l = \frac{K\pi}{2}$  ( $K$  is an arbitrary positive integer). Based on (App.7.46) the electrical length at frequency  $f_0$  is given by

$$EL(\text{degree}) = f_0 \frac{180^\circ}{f_T} \quad (\text{App. 6.14})$$

The electrical length is quarter-wavelength at the frequency where the first minimum point locates. As shown in Fig. App. 6.20c at 1 GHz locates the first trough and the period  $f_T$  is 2 GHz therefore this microstrip is quarter-wavelength at 1 GHz.

3. The phase of  $S_{21}$ ,  $\angle S_{21}$ , reaches zero when  $EL = \beta l = K\pi$  ( $K$  is an arbitrary positive integer). Based on (App.7.56) the electrical length at frequency  $f_0$  is given by

$$EL(\text{degree}) = f_0 \frac{360^\circ}{f_T} \quad (\text{App. 6.15})$$

The electrical length is half-wavelength at the frequency where the first minimum point locates. As shown in Fig. App. 6.20d. at 2 GHz locates the first zero and the period  $f_T$  is 4 GHz therefore this microstrip is quarter-wavelength at 1 GHz.

## 6.5 Measurement results and discussion

The microstrip lines to be tested are designed to be quarter-wavelength at 2 GHz with different characteristic impedance. They were cut into separate small board and soldered with two SMA connectors as shown in Fig. App. 6.11.

### 6.4.1 Measurement results of the microstrip lines

Refer to the number labels in Table App. 6.2, microstrip lines D1, C2, B2, C1 and B1 were soldered with SMA connectors and measured both in Agilent 86100A oscilloscope and Agilent network analyzer 8510C.

#### TDR measurement results

Agilent 86100A oscilloscope is used to conduct the TDR measurement for the microstrip lines and the measurement results are listed in Table App. 6.2. It shows that the measurement results are very close to the expectation.

Table. App. 6.2 The measurement result of the characteristic impedance of the microstrip lines

Number label	Designed characteristic impedance (ohm)	Measured characteristic Impedance (ohm)	Deviation
D1	50	48.55	2.9%
C2	40	38.79	3.0%
B2	30	29.7	1.0%
C1	22.36	21.33	4.6%
B1	15	15.23	1.5%

#### S parameter measurement results

Due to the lack of knowledge of test fixture and non-coaxial calibration before the design of the first-round microstrip test samples the coaxial-microstrip transition errors caused by the SMA connectors were not taken into consideration in the design. The S parameters measured include two SMA connectors and the parasitic inductance and

capacitance brought by the soldering tin. Therefore, the S parameter measurement can not be interpreted satisfactorily.

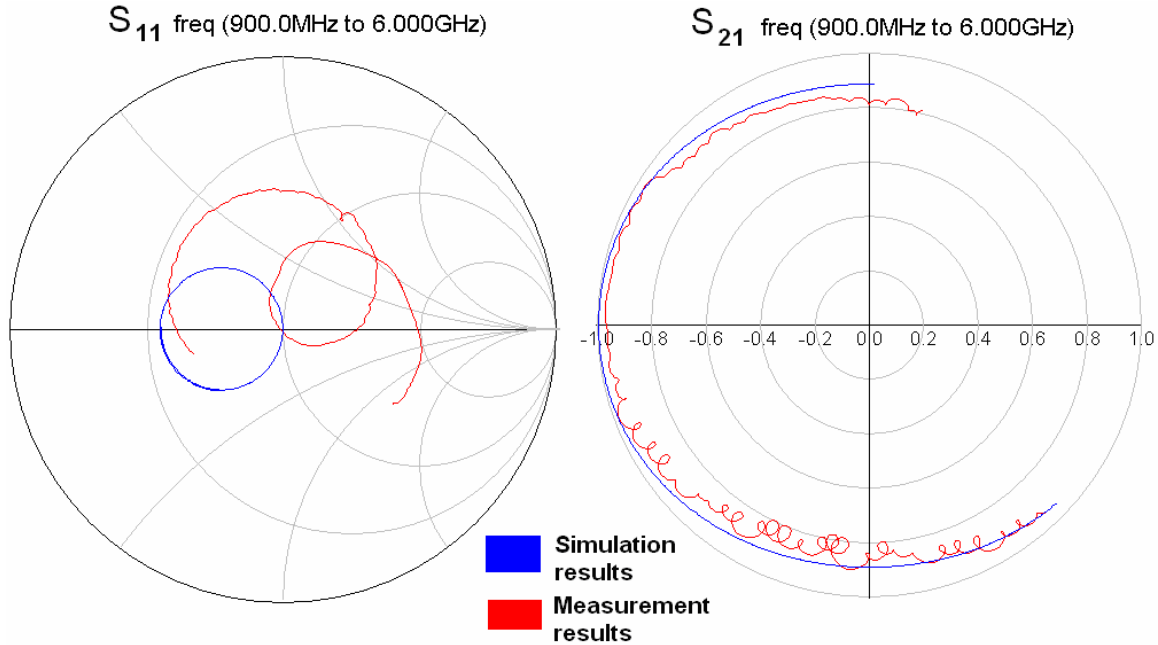


Fig. App. 6.21 The Smith chart comparison between the simulation and measurement result of microstrip B2

Compared with the ADS simulation results of the S parameter of all the microstrip examples, it's observed that the measurement result of  $S_{21}$  agrees with the expected value well but  $S_{11}$  doesn't. Take the Smith chart of microstrip B2 as an example shown in Fig. App. 6.21. Actually only the phase of  $S_{11}$  is different very much among the S parameter if the Smith chart is transformed into rectangular scalar shown in Fig. App. 6.22. If only analyze the period of  $dB(S_{11})$ ,  $dB(S_{21})$  and  $phase(S_{21})$  as proposed in section 6.4.2, it's reasonable to say that the electrical length of microstrip B2 is quarter-wavelength. However, to draw a completely solid conclusion about the electrical length measurement the TRL calibration and according test fixture are needed.

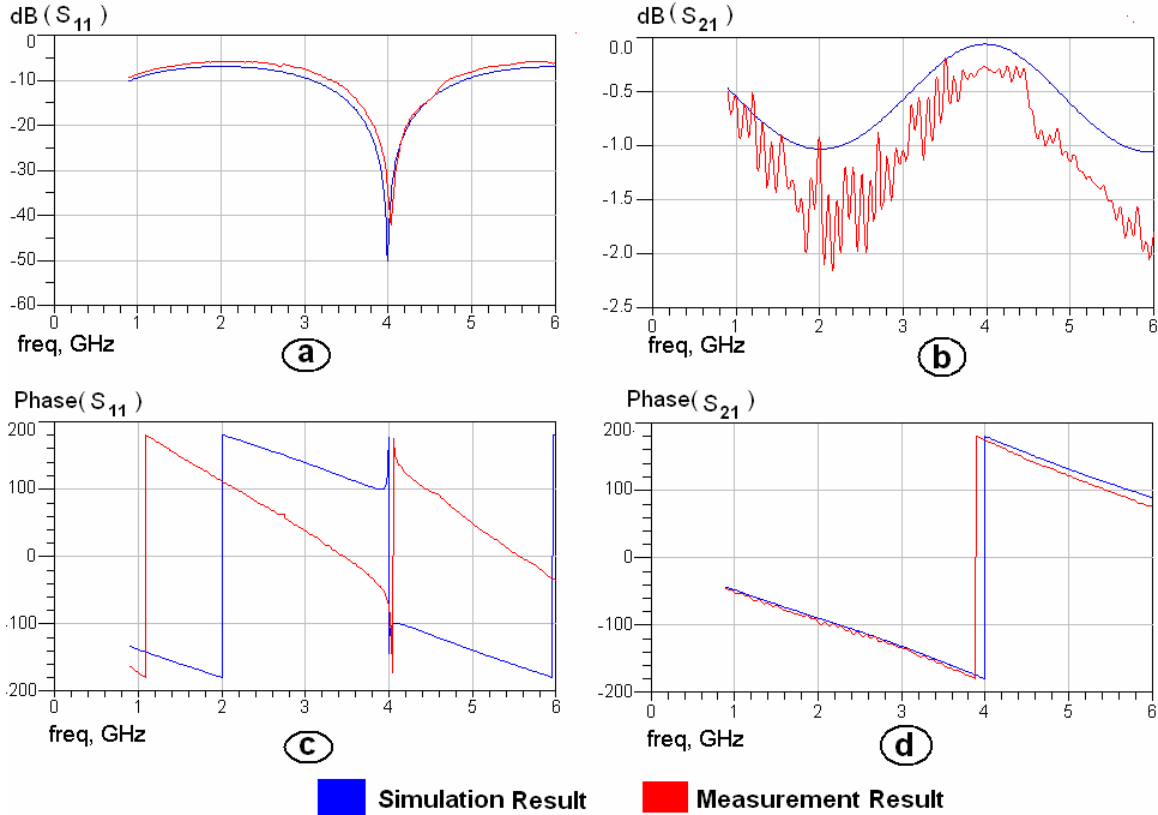


Fig. App. 6.22 The S parameter comparison between the simulation and measurement result of microstrip B2 in rectangular scalar.

### 6.5.2 The accuracy of the measurement

In order to check how accurate the fabrication of the microstrip can be the measurement of the microstrip is needed. Therefore, the measurement accuracy of the instruments is of critically importance. It should be higher than the fabrication accuracy of microstrip lines otherwise the measurement can not characterize the fabrication accuracy. Following this subject is discussed.

#### The measurement accuracy of network analyzer

The network analyzer 8510C can sample at most 801 data points within the frequency span. Therefore the minimum frequency resolution of 8510C is given by

$$\Delta f = \frac{f_{range}}{NOP - 1} \quad (\text{App. 6.16})$$

Where :  $\Delta f$  = the frequency resolution

$f_{range}$  = the frequency span

$NOP$  = the number of the data points sampled.

Suppose the periodic interpretation method is used and  $N$  period of the  $S$  parameter is needed. Thus the frequency span is given by

$$\Delta f = N \times f_T \quad (\text{App. 6.17})$$

, where  $f_T$  is the period of the  $S$  parameter.

For a certain transmission line with a given physical length the electrical length changes with the frequency, which can be represented by the transform of (App. 6.12) as

$$\frac{EL_1}{EL_2} = \frac{f_1}{f_2} \quad (\text{App. 6.18})$$

$$\Rightarrow \Delta EL = EL_0 \frac{\Delta f}{f_0} \quad (\text{App. 6.19})$$

Therefore, for  $S_{21}$  the electrical length resolution is obtained by combining (App. 6.15), (App. 6.1App. 6) and (App. 6.17) as follows

$$\Delta EL = \frac{N \times 360^\circ}{NOP - 1} \quad (\text{App. 6.20})$$

Combining (App. 6.13), (App. 6.1App. 6) and (App. 6.17) the similar results is obtained for  $S_{11}$ , which is given by

$$\Delta EL = \frac{N \times 180^\circ}{NOP - 1} \quad (\text{App. 6.21})$$

As a result, decreasing the number of period of  $S$  parameter and using the maximum data points could achieve the lower electrical length resolution. Using the maximum data point 801, if two periods of  $S_{21}$  is needed the measurement accuracy of the electrical length is 0.9 degree or 1% for a quarter-wavelength transmission line.

### **The measurement accuracy of TDR**

This issue has been discussed in section 6.3.1. The limited rising time, shooting time and the discontinuities brought by the soldering not only degrade the accuracy of the electrical length measurement but also the impedance measurement.

### **Measures to improve the measurement accuracy**

The measurement accuracy can never be 100% due to the systematic errors such as the limited rising time of TDR, the limited resolution of the electrical length and random errors which can not be anticipated. It's very critical to maintain the measurement

accuracy as high as possible so that the fabrication accuracy can be tested correctly. Based on the discussion and measurement results in this chapter It's been learned that several cautions should be taken for TDR and S parameter measurement to improve the measurement accuracy as follows:

1. Use the commercial test fixture and non-coaxial calibration standards if they are available.
2. Good soldering of the SMA connectors minimizes the parasitic. When self-building the PCB test fixture keep the soldering of SMM connectors consistent.<sup>4</sup>
3. It's best to measure a precisely-defined microstrip standard after the calibration of the instruments. Only by doing this can the calibration be qualified and the total measurement errors be known. However, there is no such microstrip standard available during the measurement of this work.
4. When using the TDR to measure the characteristic impedance of the microstrip, the long microstrip is preferred. Since it keeps the two discontinuities at the ends of the long line very far the response will settle down in the middle of the line and accurate characteristic impedance can be measured.
5. Use TRL calibration discussed in section 6.3.2 when the commercial test fixture is not available.
6. Use the microstrip line longer than quarter-wavelength in the S parameter measurement.
7. Divide S parameter measurement in two rounds, namely, coarse measurement and fine measurement. At first, use broad frequency span which could show more periods of S parameter to locate the data position of interest. Secondly, use shallow frequency span centered at the interested frequency to obtain the S parameter.
8. Since TDR is good at measuring the characteristic impedance of the microstrip and the network analyzer can measure the electrical length accurately. It's suggested to use TDR and network analyzer share the measurement job.

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<sup>4</sup> A trial universal test fixture 3680 from Anritsu (Wiltron) was available during time of the first-round measurement. Since it's for evaluation the calibration kits provided are not complete and the microstrip measurement still can not be conducted on it. However, using the commercial test fixture solves the soldering problem and some experience on using this universal test fixture 3680 is given in appendix 6.4.



9. Before making any connections to the measurement ports, be sure to discharge (ground) the body by grasping the outer conductor of the measurement port or the metal part of the coaxial cable attached to the port. Also, any device being attached to either port must be discharged; that includes both the outer and inner conductors. Never touch the center conductor of the measurement ports [5.15].

In summary the assumption that the measurement accuracy is higher than the fabrication accuracy is the key point which makes the measurement meaningless. Although theatrically it's been shown that the measurement accuracy of both TDR and network analyzer are reasonably high, a microstrip standard is preferred to characterize the overall measurement accuracy including the instruments and the human-handling. However, this kind of standard is not available in this work yet.

## **6.6 Summary**

In this chapter the measurement results of several microstrip lines samples are presented. A test fixture is necessary for the measurement of non-coaxial DUT. Additional non-coaxial calibration is therefore required. When the commercial test fixture is not available the PCB test fixture and calibration standards need to be built by the researchers themselves. However, the coaxial-to-microstrip transition in the test fixture introduces quite a few errors to the measurement. The TRL calibration procedure is suggested for the microstrip S parameter measurement to remove the test fixture errors.

TDR provides easy excess to the accurate characteristic impedance measurement and the network analyzer is good at the accurate electrical length measurement. The proposed periodic interpretation of S parameter enables quick characterization of the microstrip.

The first-round measurement of the microstrip lines with SMA connectors soldered has been done by TDR and S parameter measurement. The characteristic impedance measurement results show a close agreement to the design expectation considering the measurement errors. Due to the lack of knowledge of the test fixture during the time of the first-round microstrip-sample design the TRL calibration hasn't been taken into consideration for the S parameter. Nevertheless, if only analyze the period of  $dB(S_{11})$ ,

$dB(S_{21})$  and  $phase(S_{21})$  as proposed in section 6.4.2, it's reasonable to say that the electrical length of the microstrip lines is quarter-wavelength.

The fact that the measurement accuracy is higher than the fabrication accuracy is the key assumption of the measurement in this work. However, the overall measurement accuracy can not be determined due to the lack of well-defined microstrip standards.

## Appendix 7

### Appendix 7.1 The measurement accuracy of TDR

In the TDR measurement the two reflection responses move close to each other as the physical separation between adjacent discontinuities decreases. Fig. App. 7.1 illustrates this problem. In this illustration the ideal microstrip line is used and the step voltage input of TDR is assumed to only have rising time but no shooting.

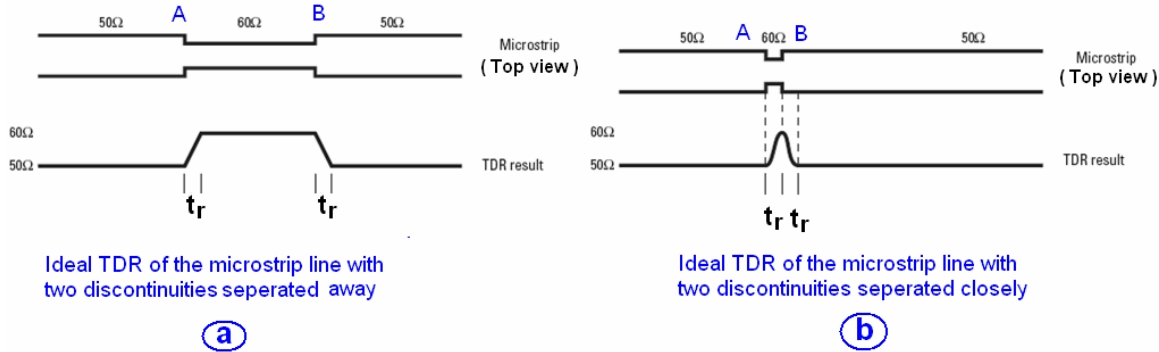


Fig. App. 7.1 The minimum space between two adjacent discontinuities is determined by the rising time of TDR system.

Between two ideal 50-ohm microstrip lines is a 60-ohm microstrip line, which introduces two discontinuities at plane A and B and therefore reflections shown in Fig. App.6.1a. The step voltage input of TDR remains at the 50-ohm level until plane A is encountered and then changes to 60-ohm level. After the second reflection site in plane B the step response changes back to the 50-ohm level. Since the step generator of TDR has rising time the response of the discontinuities do not change abruptly. The time required to reach the full 60-ohm level from 50-ohm level at plane A is simply the rising time of the step generator. The time required to transit completely from the 60-ohm level back to the 50-ohm level at plane B is once again the rising time of the TDR system. As the 60-ohm microstrip becomes shorter shown in Fig. App.7.1b the two transition responses at plane A and B move to each other. The minimum space between two discontinuities is defined when the end of the step response of plane A is at the same time as the beginning of the transition response of plane B. The TDR waveform will not have sufficient time to reach the full amplitude and the measurement of the magnitude of the impedances will be

in error. Therefore, the ideal minimum physical distance can be defined by the TDR measurement is given by [6.5]

$$L = \frac{c \times t_{rise}}{2\sqrt{\epsilon_{eff}}} \quad (\text{App. 7.1})$$

, where  $c$  is the velocity of light in the air,  $t_{rise}$  is the rising time of the step generator of TDR and  $\epsilon_{eff}$  is the effective dielectric constant of the microstrip.<sup>1</sup> For the microstrip line with two discontinuities at the end, the shortest electrical length can be defined is given by

$$EL = 180 \times f_0 \times t_{rise} \text{ (degree)} \quad (\text{App. 7.2})$$

, where  $f_0$  is the operating frequency of the microstrip.

## Appendix 7.2 Measuring the test fixture

When the microstrip board shown in Fig. App.7.2a is measured by 8510C network analyzer the S parameter block actually include two transition regions AB and BA shown in Fig. App. 7.2b. Suppose the two SMA are symmetric and thus can be represented by the same S parameter block  $S_{SMA}$ . The S parameter measurement  $S_{NW}$  is the summation of three cascaded S parameter blocks, namely,  $S_{SMA}$ ,  $S_{DUT}$  and  $S_{SMA}$ . Transformed into ABCD parameter<sup>2</sup> the cascaded block is given by

$$A_{NW} = A_{SMA} \times A_{DUT} \times A_{SMA} \quad (\text{App. 7.3})$$

Thus the ABCD parameter of the DUT is calculated as

$$A_{DUT} = A_{SMA}^{-1} \times A_{NW} \times A_{SMA}^{-1} \quad (\text{App. 7.4})$$

Therefore, the parameter of the SMA transition is desired for the calculation of the DUT's parameter.

In section appendix 6.3.2 it's been introduced that for de-embedding the test fixture in the DUT measurement there are two ways to obtain the S parameter of the test fixture, namely, modeling and measuring. Due to the complex modeling of the SMA transition

<sup>1</sup> The effective dielectric constant of the microstrip is different from the dielectric constant of the substrate material of the microstrip.

<sup>2</sup> Only ABCD and T parameter can represent the cascade blocks by multiplying the parameter matrix of each block directly.

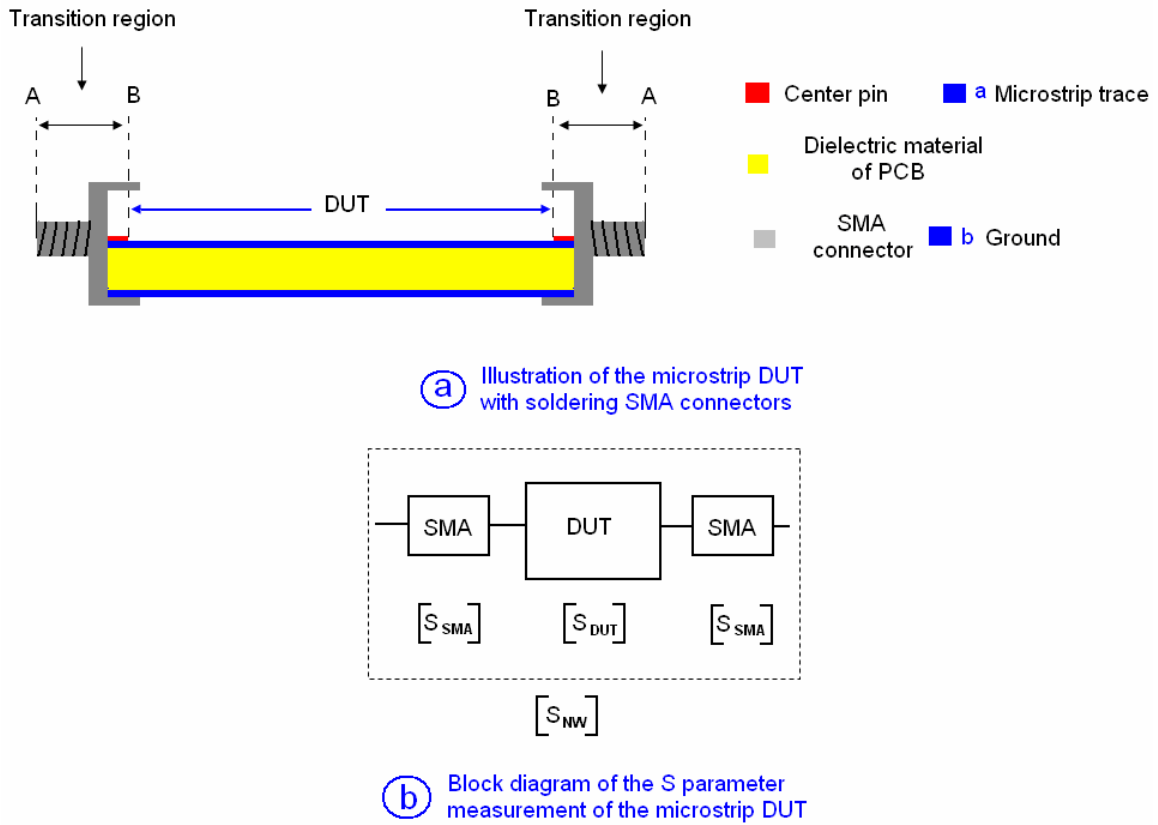


Fig. App. 7.2 Illustration of the S-parameter measurement of the microstrip DUT with two SMA connectors soldered.

“measuring” has been tried to obtain the S parameter of the SMA transition block instead of “modeling”. As shown in Fig. App. 7.3 the two-SMA structure is built to model the cascade of two SMA transitions. The S parameter of this cascaded SMA block shown Fig. 7.3 can be measured as  $S_{SMA} \times S_{SMA}$  and the S parameter  $S_{SMA}$  of single SMA transition can be calculated. Right now the focus shifts to the computation of the square root of a matrix. However, the direct command functions provided by Matlab and Mathematica can only give one square root of the 2x2 matrix. In this case S parameter matrix  $S_{SMA} \times S_{SMA}$  is a complex 2x2 matrix and has four square roots. Therefore, some manipulation of the matrix is needed.

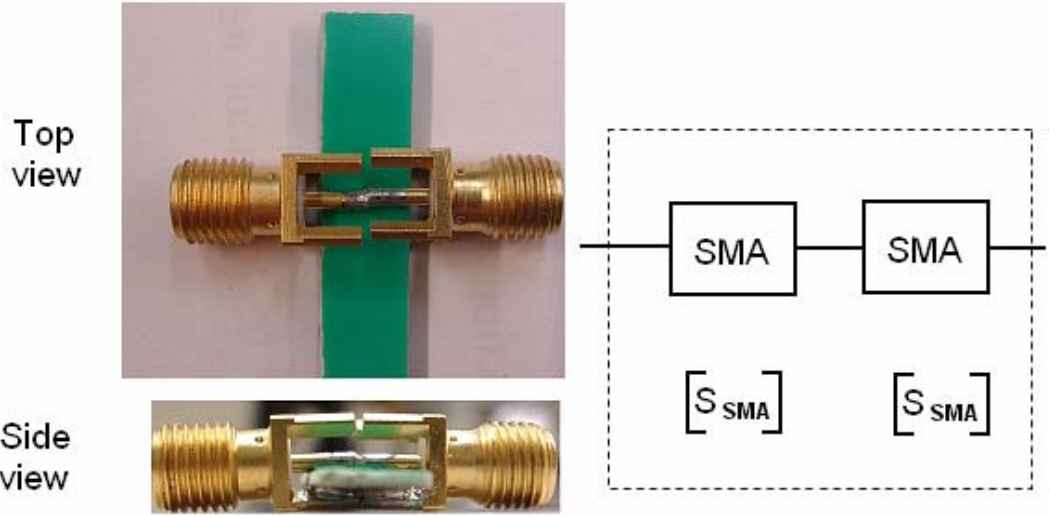


Fig. App. 7.3 The two-SMA structure used to measure the S-parameter  $S_{SMA}$  of the SMA transition block .

### Calculation of the four square roots of a complex 2x2 matrix

A complex 2x2 matrix  $A$  can be represented by

$$A = V \times D \times V^{-1} \quad (\text{App. 7.5})$$

, where  $D$  is the diagonal eigenvalue matrix of the matrix  $A$ ,  $V$  is the eigenvector matrix of  $A$  and  $V^{-1}$  is the inverse of  $V$ .

The diagonal eigenvalue matrix  $D$  is real-number 2x2 and has four square roots which can be calculated easily. Let's say matrix  $F_1$  is one of the four square roots and suppose the matrix  $B_1$  is given by

$$B_1 = V \times F_1 \times V^{-1} \quad (\text{App. 7.6})$$

$$\Rightarrow B_1 \times B_1 = V \times F_1 \times V^{-1} \times V \times F_1 \times V^{-1} = V \times F_1 \times F_1 \times V^{-1} = V \times D \times V^{-1} = A \quad (\text{App. 7.7})$$

Thus  $B_1$  is one square root of matrix  $A$  and the rest of the square roots of  $A$  can also be easily calculated by computing the square roots of the real-number diagonal eigenvalue matrix  $D$ . The computation is programmed in Matlab and the algorithm of calculating  $S_{SMA}$  is given as follows:

1. In the network analyzer 8500C set measurement frequency range and points as (0.9 GHz – 6 GHz) and 801 respectively and measure S parameter matrix  $S_{SMA} \times S_{SMA}$  of the SMA-structure shown in Fig. App. 7.3.

2. Convert S parameter matrix  $S_{SMA} \times S_{SMA}$  into ABCD matrix  $A^3$ .
3. Using command “[V,D] = eig(A)” to calculate the eigenvalue and eigenvector matrices of A, namely, V and D.
4. Calculate the four square roots of the real-number eigenvalue matrix D.
5. Using (App. 7.6) to calculate the four square roots of A,  $A_{SMA}$
6. Using (App. 7.4) to calculate  $A_{DUT}$ , the ABCD parameter of the DUT.
7. Convert the ABCD parameter of the DUT  $A_{DUT}$ , into the S-parameter matrix  $S_{DUT}$ .

However, the calculated  $S_{DUT}$  still don't agree with the S parameter of a transmission line.

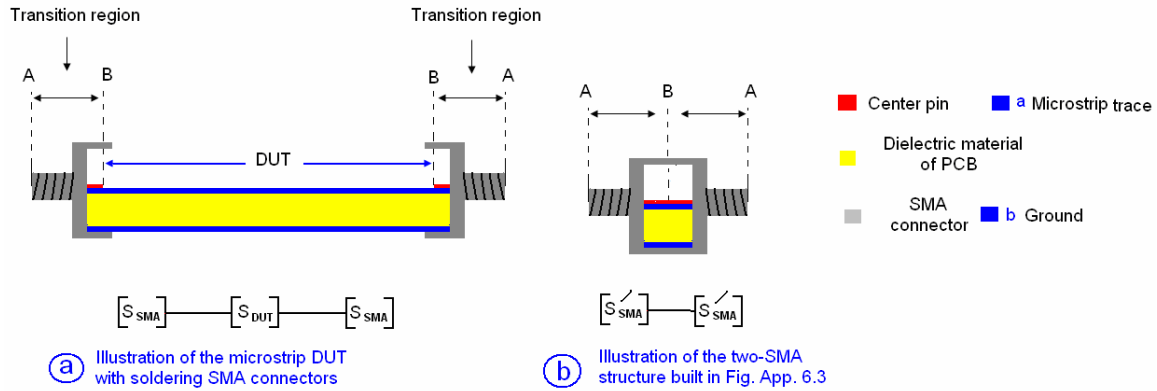


Fig. App. 7.4 Illustration of the difference of the SMA transition region.

The major reason is that the S parameter block of the SMA transition shown in Fig. App. 7.3 is different from that in Fig. 7.2b. Refer to Fig. App. 7.4, the neighbor of the SMA transition AB in Fig App. 7.4a and App. 7.4b are different, although they themselves are the same. Therefore the S-parameter blocks of them will not be the same.

In summary calculation of the S-parameter matrix of the SMA transition AB shown in Fig. App. 7.2a is difficult either by modeling or direct measurements.

<sup>3</sup> The transformation between S, Y, Z, ABCD, T parameter can be easily achieved by a simple command in RF toolbox in Matlab.

## Appendix 7.3 The interpretation of S parameter of transmission lines

### 7.3.1. S parameter basics

Systems can be characterized in numerous ways. To simplify the analysis the system is generally considered as a black box inside which the internal structure details are discarded. Only the input and output behavior of the black box are of interest. At lower frequency the most common representations use impedance (Z parameter analysis) or admittance (Y parameter analysis) or a hybrid of these two (H parameter analysis). Open-circuit or short-circuit easily enable the determination of Z, Y, H parameters. However, at high frequency it's difficult to provide adequate shorts or open (lead inductance and capacitance make short and open circuits difficult to obtain). Scattering parameter then is used to characterize the system at RF frequency. Instead of open-circuit or short-circuit the ports of the system under test are terminated with the reference impedance of their own,  $Z_{0n}$ , to determine the S-parameter. As shown in Fig. App. 7.5 the DUT (device under test) is connected with the source and load by transmission lines, the characteristic impedance of which is the same as the reference impedance of that port [2.17]. Thus at port 1, 2 of the two port system the incident and reflected wave consist of the traveling wave to characterize the system. At each port there will be no reflected wave if it's terminated by reference impedance of that port  $Z_{0n}$ .

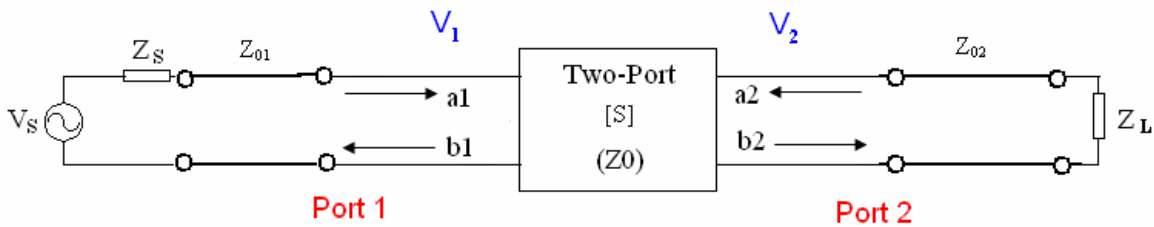


Fig. App. 7.5 Two-port block terminated by the source and load.

#### Definition of generalized S-parameter

Refer to Fig. App. 7.5, the generalized scattering parameters are defined as following:

$$\begin{aligned} b_1 &= s_{11}a_1 + s_{12}a_2 \\ b_2 &= s_{21}a_1 + s_{22}a_2 \end{aligned} \quad (\text{App. 7.8})$$

, where



$$a_1 = \frac{V_{i1}}{\sqrt{Z_{01}}}, V_{i1} \text{ is the incident voltage wave on port 1;}$$

$$a_2 = \frac{V_{i2}}{\sqrt{Z_{02}}}, V_{i2} \text{ is the incident voltage wave on port 2;}$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_{01}}}, V_{r1} \text{ is the reflected voltage wave on port 1;}$$

$$b_2 = \frac{V_{r2}}{\sqrt{Z_{02}}}, V_{r2} \text{ is the reflected voltage wave on port 2.}$$

Usually  $Z_{01}$  and  $Z_{02}$  are all set to 50 ohm denoted as  $Z_0$ , which is given by

$$Z_{01} = Z_{02} = Z_0 \quad (\text{App. 7.9})$$

### Port reflection coefficients, voltages and currents

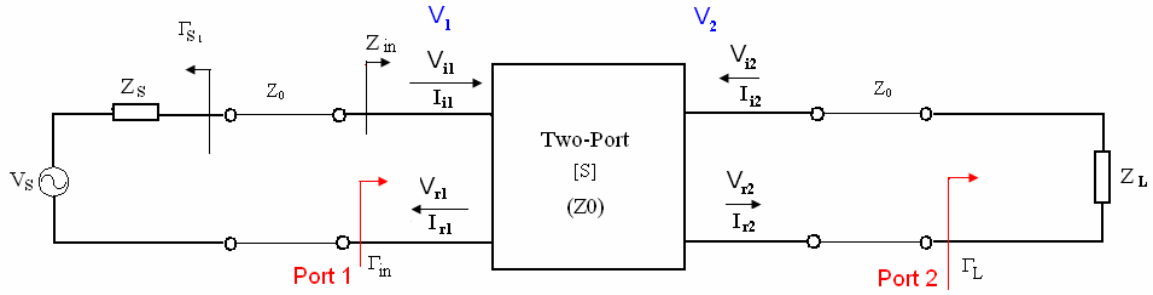


Fig. App. 7.6 Two-port network for S parameter.

Refer to Fig. App. 7.6, on port 1 the port voltage, current and reflection coefficients are

$$V_{i1} + V_{r1} = V_1 \quad (\text{App.7.10})$$

$$I_{i1} - I_{r1} = \frac{V_{i1}}{Z_{01}} - \frac{V_{r1}}{Z_{01}} = I_1 \quad (\text{App.7.11})$$

Thus, at port 1

$$V_{i1} = \frac{V_1 + I_1 Z_{01}}{2} = \frac{V_1 + I_1 Z_0}{2} \quad (\text{App.7.12})$$

$$V_{r1} = \frac{V_1 - I_1 Z_{01}}{2} = \frac{V_1 - I_1 Z_0}{2} \quad (\text{App.7.13})$$

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \quad (\text{App.7.14})$$

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \quad (\text{App.7.15})$$

where the  $\Gamma_s$  is the reflection coefficient seen looking toward the source and  $\Gamma_{in}$  is the reflection coefficient seen looking toward port 1.

The same results apply to port 2.

$$V_{i2} = \frac{V_2 + I_2 Z_{02}}{2} = \frac{V_2 + I_2 Z_0}{2} \quad (\text{App.7.16})$$

$$V_{r2} = \frac{V_2 - I_2 Z_{02}}{2} = \frac{V_2 - I_2 Z_0}{2} \quad (\text{App.7.17})$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (\text{App.7.18})$$

where  $\Gamma_L$  is the reflection coefficient seen looking toward the load.

### Power parameters of the two-port network

After the basic terms of the two-port network are obtained the power values of the two-port network are calculated.

At port 1 the total voltage  $V_1$  is given by

$$V_1 = V_{i1} + V_{r1} = V_{i1}(1 + \Gamma_{in}) = V_s \frac{Z_{in}}{Z_s + Z_{in}} \quad (\text{App.7.19})$$

$$\text{where } Z_{in} = Z_{01} \frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} = Z_0 \frac{1 + \Gamma_{in}}{1 - \Gamma_{in}}$$

Substituting (App.7.18) and (App.7.14) into (App.7.11) yields

$$V_{i1} = \frac{V_s}{2} \frac{(1 - \Gamma_s)}{(1 - \Gamma_s \Gamma_{in})} \quad (\text{App.7.20})$$

The average power delivered to the two-port network is

$$\begin{aligned} P_{in} &= \frac{1}{2} \text{Re} \{V_1 \times (I_1)^*\} = \frac{1}{2} \text{Re} \left\{ V_1 \times \left( \frac{V_1}{Z_{in}} \right)^* \right\} = \frac{1}{2} \text{Re} \left\{ V_1 \times (V_1)^* \times \left( \frac{1}{Z_{in}} \right)^* \right\} \\ &= \frac{1}{2} \text{Re} \left\{ |V_1|^2 \times \left( \frac{1}{Z_{in}} \right)^* \right\} = \frac{1}{2} \text{Re} \left\{ |V_{i1}|^2 \times |1 + \Gamma_{in}|^2 \times \left( \frac{1}{Z_{in}} \right)^* \right\} \\ &= \frac{1}{2} |V_{i1}|^2 \times |1 + \Gamma_{in}|^2 \times \text{Re} \left\{ \left( \frac{1 - \Gamma_{in}}{Z_0 (1 + \Gamma_{in})} \right)^* \right\} \end{aligned} \quad (\text{App.7.21})$$

Substituting  $\Gamma_{in} = A \cos \theta + jA \sin \theta$  into (App.7.20) yields

$$P_{in} = \frac{1}{2Z_0} \times |V_{i1}|^2 \times (1 - |\Gamma_{in}|^2) \quad (\text{App.7.22})$$

For the power delivered to the load at port 2 the similar result can be derived, which is given by

$$P_L = \frac{1}{2Z_0} \times |V_{r2}|^2 \times (1 - |\Gamma_L|^2) \quad (\text{App.7.23})$$

Manipulating (App. 7.8) yields

$$V_{r2} = S_{21}V_{i1} + S_{22}\Gamma_L V_{r2} \quad (\text{App.7.24})$$

$$\Rightarrow V_{r2} = \frac{S_{21}}{1 - S_{22}\Gamma_L} V_{i1} \quad (\text{App.7.25})$$

Substituting (App.7.25) into (App.7.23) yields

$$P_L = \frac{1}{2Z_0} \times \left| \frac{S_{21}}{1 - S_{22}\Gamma_L} V_{i1} \right|^2 \times (1 - |\Gamma_L|^2) \quad (\text{App.7.26})$$

Therefore the power gain or the power efficiency of the two-port system is given by

$$G = \eta = \frac{P_{in}}{P_L} = \left| \frac{S_{21}}{1 - S_{22}\Gamma_L} \right|^2 \times \frac{(1 - |\Gamma_L|^2)}{(1 - |\Gamma_{in}|^2)} \quad (\text{App.7.27})$$

where  $\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$  and  $Z_{in} = Z_0 \frac{1 + \Gamma_{in}}{1 - \Gamma_{in}}$ .

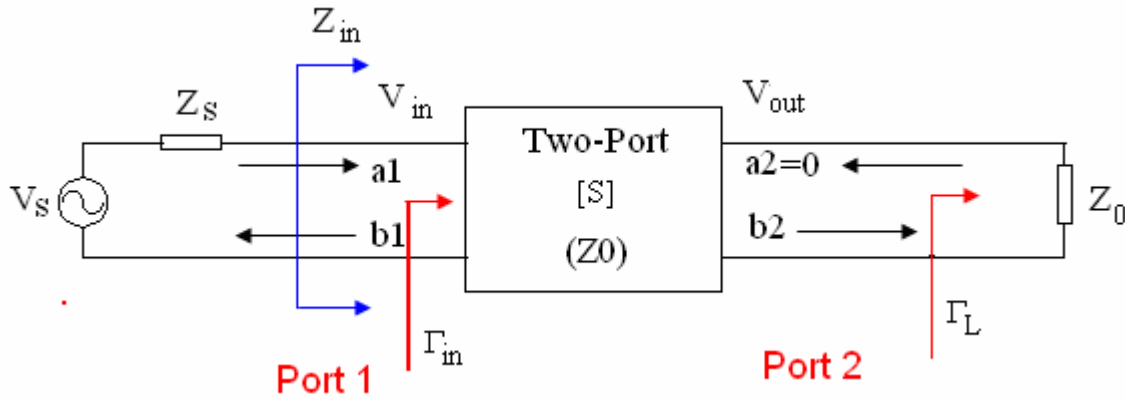


Fig. App. 7.7 Two-port network for the measuring of  $S_{11}$  and  $S_{21}$  with port 2 terminated by  $Z_0$ .

### 7.3.2 Interpretation of $S_{11}$ and $S_{21}$

#### Mathematic derivations

When measuring  $S_{11}$  and of  $S_{21}$  the two-port network port 2 is terminated by the reference impedance  $Z_0$  shown in Fig. App. 7.7. Thus at port 2 there is no reflection wave, which means

$$a_2 = 0 \quad (\text{App.7.28})$$

Substituting (App.7.28) into (App.7.8) yields

$$S_{11} = \frac{b_1}{a_1} = \frac{V_{r1}}{V_{i1}} = \frac{\frac{V_1 - I_1 Z_0}{2}}{\frac{V_1 + I_1 Z_0}{2}} = \frac{\frac{V_1}{I_1} - Z_0}{\frac{V_1}{I_1} + Z_0} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \quad (\text{App.7.29})$$

$$= \Gamma_{in}$$

and

$$S_{21} = \frac{b_2}{a_1} \quad (\text{App.7.30})$$

Based on the definition of the generalized S-parameter in (App.7.8) the voltages at port 1 and 2 are given by

$$V_{in} = V_{i1} + V_{r1} = \sqrt{Z_0}(a_1 + b_1) \quad (\text{App.7.31})$$

$$V_{out} = V_{i2} + V_{r2} = \sqrt{Z_0}(a_2 + b_2) = \sqrt{Z_0}b_2 \quad (\text{App.7.32})$$

$$\text{Therefore: } \frac{V_{out}}{V_{in}} = \frac{b_2}{a_1 + b_1} \quad (\text{App.7.33})$$

Combining (App.7.28), (App.7.29) and (App.7.32) gives

$$S_{21} = \frac{V_{out}}{V_{in}}(1 + S_{11}) = \frac{\frac{V_{out}}{V_{in}}}{\frac{1 + \Gamma_{in}}{1 + \frac{Z_{in} - Z_0}{Z_{in} + Z_0}}} = \frac{V_{out}}{V_{in}} \frac{Z_{in} + Z_0}{2Z_{in}} \quad (\text{App.7.34})$$

$$\text{where } V_{in} = \frac{Z_{in}}{Z_{in} + Z_s} V_s \quad (\text{App.7.35})$$

When the source impedance  $Z_s = Z_0$  and the voltage source  $V_s$  is 2 volt shown in Fig. App. 7.8.

$$S_{21} = \frac{V_{out}}{\frac{V_s}{2}} = V_{out} \quad (\text{App.7.36})$$

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = \frac{2Z_{in}}{Z_{in} + Z_0} - 1 = \Gamma_{in} - 1 \quad (\text{App.7.37})$$

Refer to Fig. App. 7.8 now, this simple model can be used to calculate the S parameter of the two-port network easily, where the source impedance of the voltage source  $V_s$  and the load impedance are equal to the characteristic impedance of the two-port network,  $Z_0$ .

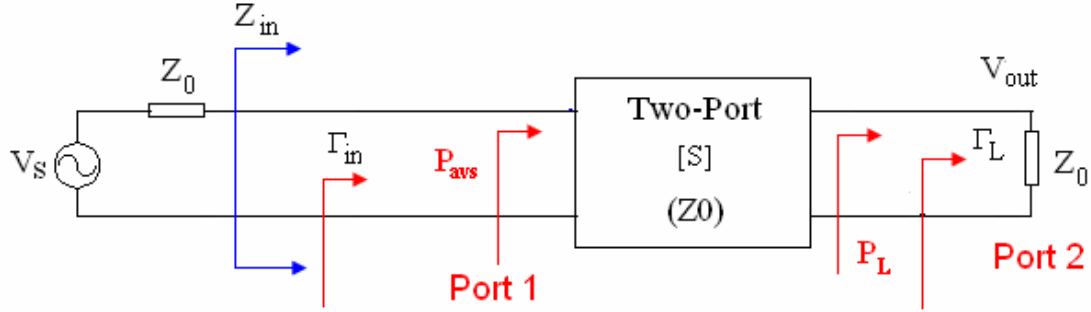


Fig. App. 7.8 Simple model used to calculate the S parameter of a two-port network.

It's trivial that the maximum available power delivered to port1,  $P_{avs}$ , is given by

$$P_{avs} = \frac{1}{2Z_0} \left| \frac{V_s}{2} \right|^2 \quad (\text{App.7.38})$$

while the power delivered to the load  $Z_0$  from port 2,  $P_L$ , is given by

$$P_L = \frac{|V_{out}|^2}{2Z_0} \quad (\text{App.7.39})$$

Thus the transducer power gain  $G_T$  is given by

$$G_T = \frac{P_L}{P_{avs}} = \left| \frac{V_{out}}{\frac{V_s}{2}} \right|^2 = |S_{21}|^2 \quad (\text{App.7.40})$$

## Summary

The simple procedure to calculate the S parameter of a two-port network is listed as follows:

1. Insert the two-port DUT in the circuit shown in Fig. App. 7.8, where the source impedance of the voltage source  $V_s$  and the load impedance are equal to the characteristic impedance of the two-port network,  $Z_0$ .

2.  $S_{11}$  equals to the reflection coefficient  $\Gamma_{in}$  or  $V_{out} - 1$  when the voltage source  $V_s = 2$  volt.
3.  $S_{21}$  equals to  $V_{out}$  at the load, when  $V_s = 2$  volt.
4. The transducer power gain  $G_T$  of this two-port network equals to  $|S_{21}|^2$
5. The efficiency (power gain) of this two-port network  $G$  equals to

$$\left| \frac{S_{21}}{1 - S_{22}\Gamma_L} \right|^2 \times \frac{(1 - |\Gamma_L|^2)}{(1 - |\Gamma_{in}|^2)}.$$

### 7.3.3. Characterization of the ideal transmission line using s parameter

When microstrip transmission lines are designed and fabricated their characteristic impedance  $Z_{TL}$  and electrical length  $EL = \beta l$  are usually measured for comparison with the design value. However, the measurement data from the network analyzer is S parameter instead of  $Z_{TL}$  and  $EL$ . Following will discuss the relationship between the S parameter and of  $Z_{TL}$  and  $EL$  of the ideal transmission line.

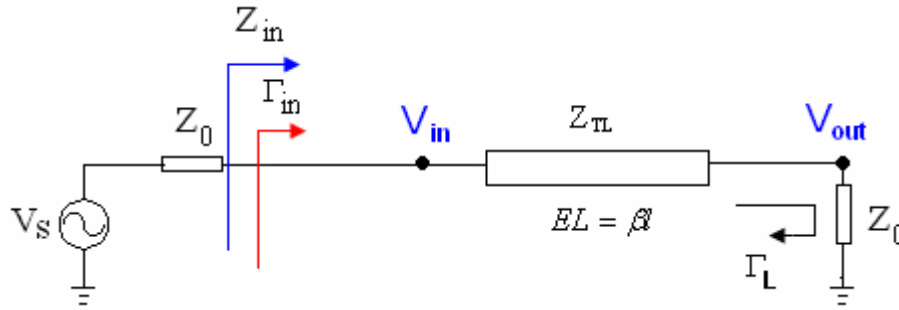


Fig. App. 7.9 Circuit model used to calculate the S parameter of an ideal transmission line.

The summary in appendix 7.3.2 can be used for the characterization of the transmission line. As shown in Fig. App. 7.9 the microstrip is inserted into the circuit shown in Fig. App. 7.8, where the reference impedance of the measurement is  $Z_0 = 50$  ohm.

#### Relationship between $S_{11}$ , $Z_{TL}$ and $EL$ of the Transmission line

Based on the equations about the transmission line [2.17] and the previous summary the following equation set is obtained

$$\begin{cases} \Gamma_{in} = S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \\ Z_{in} = Z_{TL} \times \frac{Z_0 + jZ_{TL} \tan \beta l}{Z_{TL} + jZ_0 \tan \beta l} \end{cases} \quad (\text{App.7.41})$$

where  $S_{11} = |S_{11}| \angle \theta$ .

Solving (App.7.41) gives

$$Z_{TL} = 50 \times \sqrt{\frac{\cos \theta + |S_{11}|}{\cos \theta - |S_{11}|}} \quad (\text{App.7.42})$$

$$EL = \beta l = \begin{cases} \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] & \text{when } \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] > 0 \\ \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] + \pi & \text{when } \arctan\left[-\frac{\sqrt{(\cos \theta)^2 - |S_{11}|^2}}{\sin \theta}\right] \leq 0 \end{cases} \quad (\text{App.7.43})$$

However, during the solving process trigonometric function is involved and cautions should be taken about the quadrant angle of the solution (App.7.43). It's good to know the phase angle of  $S_{11}$ , which helps to build a first judgment when the S parameter measurement is being interpreted.

#### Phase angle of $S_{11}$

Following is the derivation of the phase angle of  $S_{11}$ .

$$\begin{aligned} S_{11} = \Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} &= \frac{Z_{TL} \times \frac{Z_0 + jZ_{TL} \tan \beta l}{Z_{TL} + jZ_0 \tan \beta l} - Z_0}{Z_{TL} \times \frac{Z_0 + jZ_{TL} \tan \beta l}{Z_{TL} + jZ_0 \tan \beta l} + Z_0} = \frac{j \tan \beta l \times (Z_{TL}^2 - Z_0^2)}{2Z_0 Z_{TL} + j \tan \beta l \times (Z_{TL}^2 + Z_0^2)} \\ &= \frac{(\tan \beta l)^2 \times (Z_{TL}^2 - Z_0^2) \times (Z_{TL}^2 + Z_0^2) + 2j \tan \beta l \times Z_0 Z_{TL} \times (Z_{TL}^2 - Z_0^2)}{(\tan \beta l)^2 \times (Z_{TL}^2 + Z_0^2)^2 + 4Z_0^2 Z_{TL}^2} \end{aligned} \quad (\text{App.7.44})$$

$$\Rightarrow \tan(\angle S_{11}) = \frac{2Z_0 Z_{TL}}{\tan \beta l \times (Z_{TL}^2 + Z_0^2)} \quad (\text{App.7.45})$$

$$|S_{11}| = \frac{|\tan \beta l \times (Z_{TL}^2 - Z_0^2)|}{\sqrt{(\tan \beta l)^2 \times (Z_{TL}^2 + Z_0^2)^2 + 4Z_0^2 Z_{TL}^2}} \quad (\text{App.7.46})$$

(App.7.45) tells that the plot of the phase angle of  $S_{11}$  over frequency is a periodic curve with the period of  $f_T$ , which is given by

$$f_T = f_0 \frac{180^\circ}{EL(\text{degree})} \quad (\text{App.7.47})$$

where  $f_0$  is the operating frequency of the transmission line.

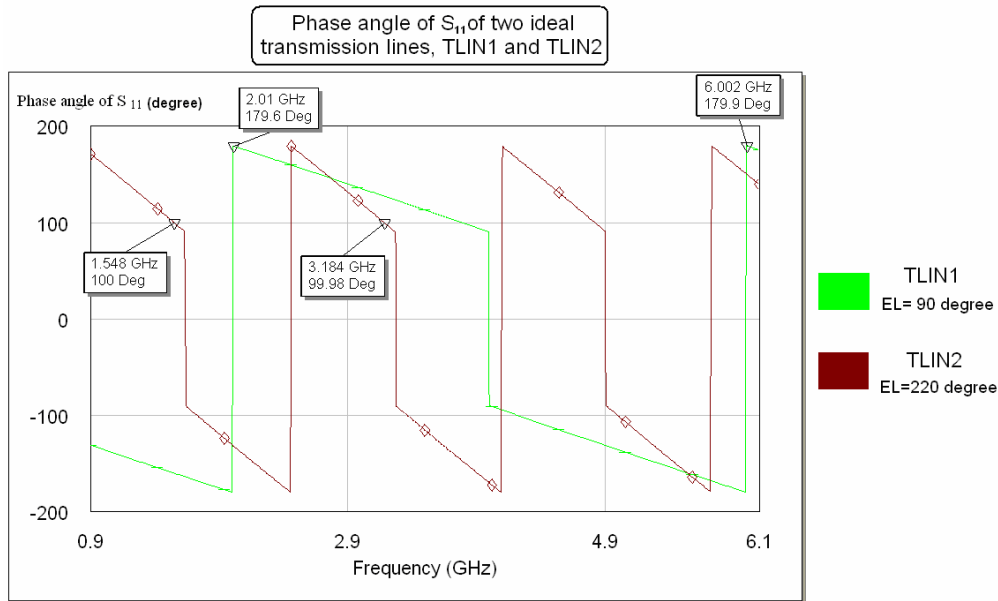


Fig. App. 7.10 Phase angle of  $S_{11}$  two ideal transmission lines, TLIN1 and TLIN2.

For example, Fig App.7.10 shows the simulation plot<sup>4</sup> of the phase angle of  $S_{11}$  of two transmission lines with characteristic impedance  $Z_0 = 40$ , while TLIN1's electrical length is 90 degree and TLIN2's is 220 degree at 2 GHz. Equation (App.7.47) tells that the TLIN1's and TLIN2's periods of the phase angle of  $S_{11}$  are

$$f_{T,TLIN1} = \frac{180^\circ}{90^\circ} \times 2 \text{ GHz} = 4 \text{ GHz} \quad (\text{App.7.48})$$

$$f_{T,TLIN2} = \frac{180^\circ}{220^\circ} \times 2 \text{ GHz} = 1.636 \text{ GHz} \quad (\text{App.7.49})$$

<sup>4</sup> The simulation result is obtained in AWR Microwave office.



, which are verified by the plot shown in Fig App.7.10.

As a conclusion, the characteristic impedance  $Z_{TL}$  and electrical length  $EL$  of an ideal transmission line can be calculated from  $S_{11}$  by using (App. 7.41) and (App. 7.43). The relationship between quadrant phase angle of  $S_{11}$ ,  $EL$ ,  $Z_{TL}$  and  $Z_0$  can be found out in Table App. 7.1 and Fig. App.7.11. Note that For the quarter-wavelength transmission line  $\angle S_{11}$  is on the jumping point from  $-\pi$  to  $\pi$ .

Table App. 7.1

$\angle S_{11}$	$Z_{TL} < Z_0$	$Z_{TL} > Z_0$
$EL = \beta l \in [(0^\circ, 90^\circ) + n\pi]$	$(-\pi, -\frac{\pi}{2})$	$(0, \frac{\pi}{2})$
$EL = \beta l \in [(90^\circ, 180^\circ) + n\pi]$	$(\frac{\pi}{2}, \pi)$	$(-\frac{\pi}{2}, 0)$

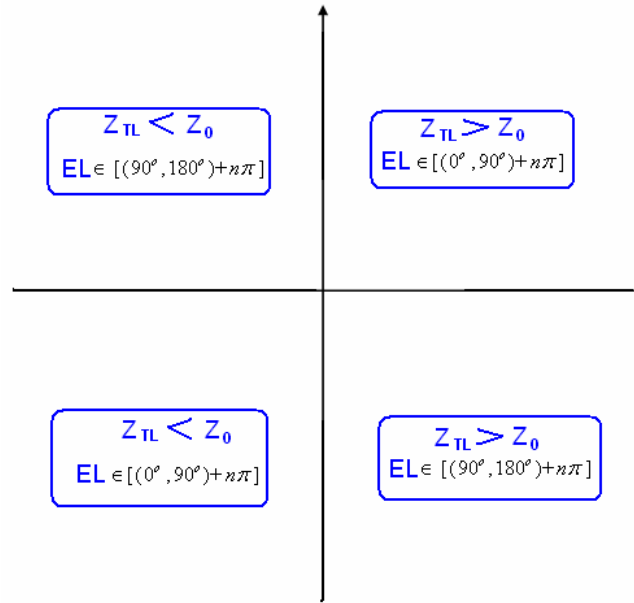


Fig. App. 7.11 The quadrant phase angle of  $S_{11}$  determined by  $EL$ ,  $Z_{TL}$  and  $Z_0$ .

#### Relationship between $S_{21}$ , $Z_{TL}$ and $EL$ of the Transmission line

Secondly the relationship between  $S_{21}$  and the electrical length and the characteristic impedance of the transmission line is derived.

Equation (App.2.9) gives that

$$\frac{V_{out}}{V_{in}} = \frac{1 + \Gamma_L}{\cos \beta l (1 + \Gamma_L) + j \sin \beta l (1 - \Gamma_L)} = \frac{Z_0}{Z_0 \cos \beta l + j Z_{TL} \sin \beta l} \quad (\text{App.7.50})$$

$$\text{where } \Gamma_L = \frac{Z_L - Z_{TL}}{Z_L + Z_{TL}} = \frac{Z_0 - Z_{TL}}{Z_0 + Z_{TL}}$$

Substituting (App.7.29) and (App.7.50) into (App.7.34) gives

$$\begin{aligned} S_{21} &= \frac{Z_0}{Z_0 \cos \beta l + j Z_{TL} \sin \beta l} \times \left[ 1 + \frac{(\tan \beta l)^2 \times (Z_{TL}^2 - Z_0^2) \times (Z_{TL}^2 + Z_0^2) + 2j \tan \beta l \times Z_0 Z_{TL} \times (Z_{TL}^2 - Z_0^2)}{(\tan \beta l)^2 \times (Z_{TL}^2 + Z_0^2)^2 + 4Z_0^2 Z_{TL}^2} \right] \\ &= \frac{-2j Z_0 Z_{TL}}{\sin \beta l \times (Z_{TL}^2 + Z_0^2) - 2j Z_0 Z_{TL} \cos \beta l} \\ &= \frac{4Z_0^2 Z_{TL}^2 \cos(-\beta l) + 2j Z_0 Z_{TL} (Z_{TL}^2 + Z_0^2) \sin(-\beta l)}{(\sin \beta l)^2 \times (Z_{TL}^2 + Z_0^2)^2 + 4Z_0^2 Z_{TL}^2 (\cos \beta l)^2} \end{aligned} \quad (\text{App.7.51})$$

$$\Rightarrow \begin{cases} \tan(\angle S_{21}) = \frac{-\tan \beta l \times (Z_{TL}^2 + Z_0^2)}{2Z_0 Z_{TL}} = \frac{-\sin \beta l \times (Z_{TL}^2 + Z_0^2)}{2Z_0 Z_{TL} \cos \beta l} \\ |S_{21}| = \frac{2Z_0 Z_{TL}}{\sqrt{(\sin \beta l)^2 \times (Z_{TL}^2 + Z_0^2)^2 + 4Z_0^2 Z_{TL}^2 (\cos \beta l)^2}} \end{cases} \quad (\text{App.7.52})$$

To find out the solution of electrical length  $\beta l$  the trigonometric function manipulation will be involved and cautions should be taken about the quadrant angle of trigonometric functions. However, if (App.7.52) is rearranged well there will be no need to worry about the quadrant angle.

At first calculate the formulas of  $\sin \beta l$  and  $\cos \beta l$  in terms of  $\tan(\angle S_{21})$ ,  $|S_{21}|$ ,  $Z_0$  and  $Z_{TL}$ . This is simple algebraic derivations and no quadrant angle is involved. The results are listed as follows:

$$\begin{cases} \sin \beta l = \pm \frac{2Z_0 Z_{TL} \tan(\angle S_{21})}{|S_{21}| \times \sqrt{Z_0^4 + [\tan(\angle S_{21})]^2 Z_0^4 + 2Z_0^2 Z_{TL}^2 + 2[\tan(\angle S_{21})]^2 Z_0^2 Z_{TL}^2 + Z_{TL}^4 + [\tan(\angle S_{21})]^2 Z_{TL}^4}} \\ \cos \beta l = \pm \frac{Z_0^2 + Z_{TL}^2}{|S_{21}| \times \sqrt{Z_0^4 + [\tan(\angle S_{21})]^2 Z_0^4 + 2Z_0^2 Z_{TL}^2 + 2[\tan(\angle S_{21})]^2 Z_0^2 Z_{TL}^2 + Z_{TL}^4 + [\tan(\angle S_{21})]^2 Z_{TL}^4}} \end{cases} \quad (\text{App.7.53})$$

Secondly substitute (App.7.53) into the equation  $(\sin \beta l)^2 + (\cos \beta l)^2 = 1$ . Only after algebraic simplification it gets

$$\frac{Z_0^4 + 2 \times (1 + 2 \times [\tan(\angle S_{21})]^2) Z_0^2 Z_{TL}^2 + Z_{TL}^4}{|S_{21}|^2 (1 + [\tan(\angle S_{21})]^2) (Z_0^2 + Z_{TL}^2)^2} = 0 \quad (\text{App.7.54})$$

Solving (App.7.52) yeilds

$$Z_{TL} = \begin{cases} Z_0 \sqrt{\frac{\tan(\angle S_{21}) + \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}{\tan(\angle S_{21}) - \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}} \\ or \\ Z_0 \sqrt{\frac{\tan(\angle S_{21}) - \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}{\tan(\angle S_{21}) + \sqrt{(1 - |S_{21}|^2)(1 + [\tan(\angle S_{21})]^2)}}} \end{cases} \quad (\text{App.7.55})$$

One of these two solutions will be larger than  $Z_0$ , 50 ohm, and the other smaller.

Finally dividing  $\sin \beta l$  by  $\cos \beta l$  from (App.7.53) yields

$$\tan \beta l = \frac{-2Z_0 Z_{TL} \tan(\angle S_{21})}{(Z_{TL}^2 + Z_0^2)} \quad (\text{App.7.56})$$

Now (App.7.53) and (App.7.54) can be used to calculate the characteristic impedance and electrical length the transmission line from  $S_{21}$ . It's good to know how the phase angle plot of  $S_{21}$  should look like. It can help to build a first judgment when you see the S parameter measurement.

### Phase angle of $S_{21}$

(App.7.52) tells the following information about the phase angle of  $S_{21}$ .

1. The phase angle of  $S_{21}$  is at the same quadrant as  $-\beta l$ . Usually the electrical length is in the range of  $(0^\circ, 180^\circ)$  and the phase angle of  $S_{21}$  will be in the range of  $(-0^\circ, -180^\circ)$ .
2. The plot of the phase angle of  $S_{21}$  over frequency is a periodic curve with the period of  $f_T$ , which is given by

$$f_T = f_0 \frac{360^\circ}{\beta l(\text{degree})} \quad (\text{App.7.57})$$

where  $f_0$  is the operating frequency of the transmission line.

For example, Fig. App. 7.11 is the simulation<sup>5</sup> plot of the phase angle of  $S_{21}$  of one transmission lines with characteristic impedance  $Z_0 = 30$ , while TLIN1's electrical length is 40 degree and TLIN2's is 220 degree at 1 GHz. Equation (App.7.55) tells that the TLIN1's and TLIN2's periods of the phase angle of  $S_{21}$  are

$$f_{T,TLIN1} = \frac{360^\circ}{40^\circ} \times 1 \text{ GHz} = 9 \text{ GHz} \quad (\text{App.7.58})$$

$$f_{T,TLIN2} = \frac{360^\circ}{220^\circ} \times 1 \text{ GHz} = 1.636 \text{ GHz} \quad (\text{App.7.59})$$

which are verified by the plot shown in Fig App.7.12.

3. For the quarter-wavelength transmission line  $\angle S_{21}$  is always  $-90^\circ$  no matter whatever the characteristic impedance is.

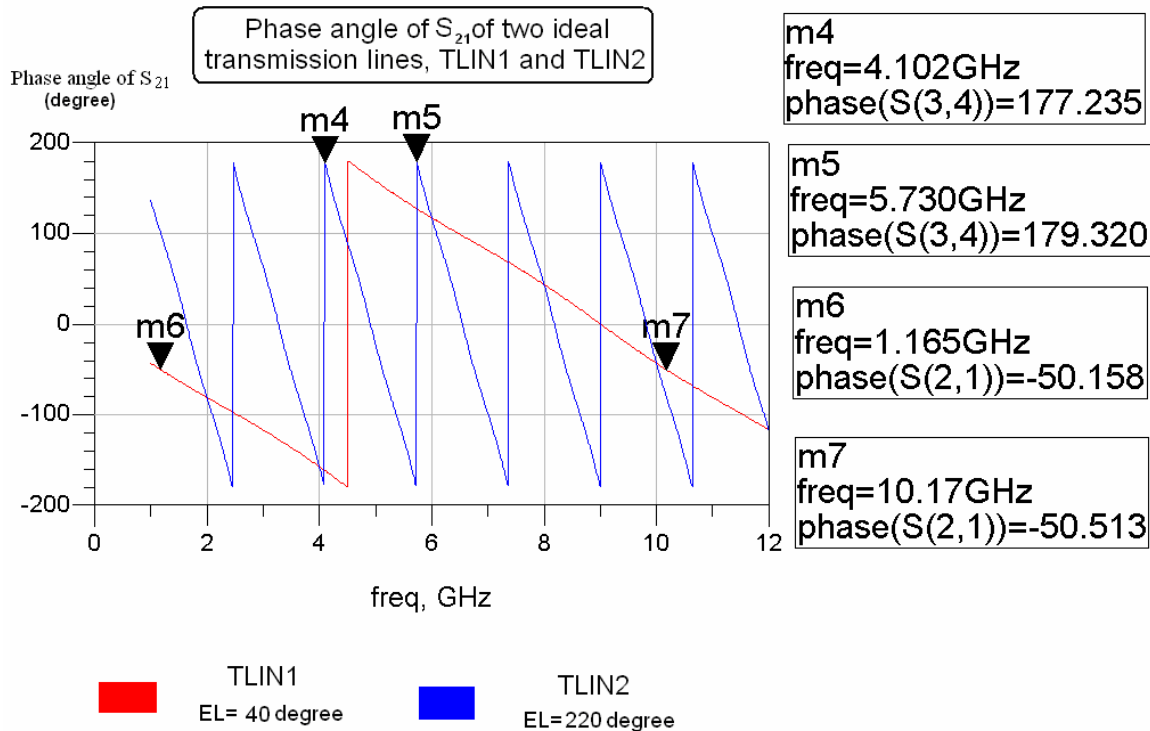


Fig. App. 7.12 Phase angle of  $S_{21}$  of two ideal transmission lines, TLIN1 and TLIN2.

<sup>5</sup> This simulation result is obtained in ADS2005.

### 7.3.4. Characterization of the low loss cable using s parameter

In [7.12-7.13] a set of equations are derived to calculate the propagation constant  $\gamma$  of the cable, which can also be used to interpret the S parameter for microstrip. Although it includes the lossy component  $\alpha$  in the propagation constant  $\gamma$  the derivation assumption is still based on the lossless transmission line equations. The equations are written as follows:

$$\gamma l = \alpha l + j\beta l = \ln X \quad (\text{App.7.60})$$

where,

$$X = \frac{S_{11} + S_{21} - \Gamma}{1 - (S_{11} + S_{21})\Gamma} \quad (\text{App.7.61})$$

$$\Gamma = \frac{S_{11}}{S_{11}^2 - S_{22}^2 + 1} \quad (\text{App.7.62})$$

## ***Appendix 7.4 The usage of Anritsu 3680 universal test fixture***

When using the Anritsu 3680 universal test fixture the microstrip board is inserted between two launches shown in Fig. App. 7.13. The signal center pin inside the hole is forced to contact with the metal strip by the two clamps. Except the signal center pin the whole launch is grounded, therefore, caution should be taken not to let the metal strip in contact with the launch. This concern is illustrated in Fig. App. 7.14, where the front view of region A of one launch is magnified. Fig. App. 7.14a shows good contact between the microstrip line metal and the center pin. However, the width of the contact door of the launch,  $W_H$ , is only around 5 mm. In case the microstrip line metal is wider than 5 mm, it will be in contacted with upper launch shown in Fig. App.7.14b. This is like short-circuiting the microstrip and will degrade the measurement result. It's always good to keep this issue in mind before designing the microstrip under test. For the wide microstrip lines a smaller contacting stub is needed to be in contact with the center signal pin as shown in Fig. 7.15. However, two step discontinuities are introduced to this

microstrip line and some errors might be resulted. This is one deficiency of this test fixture.

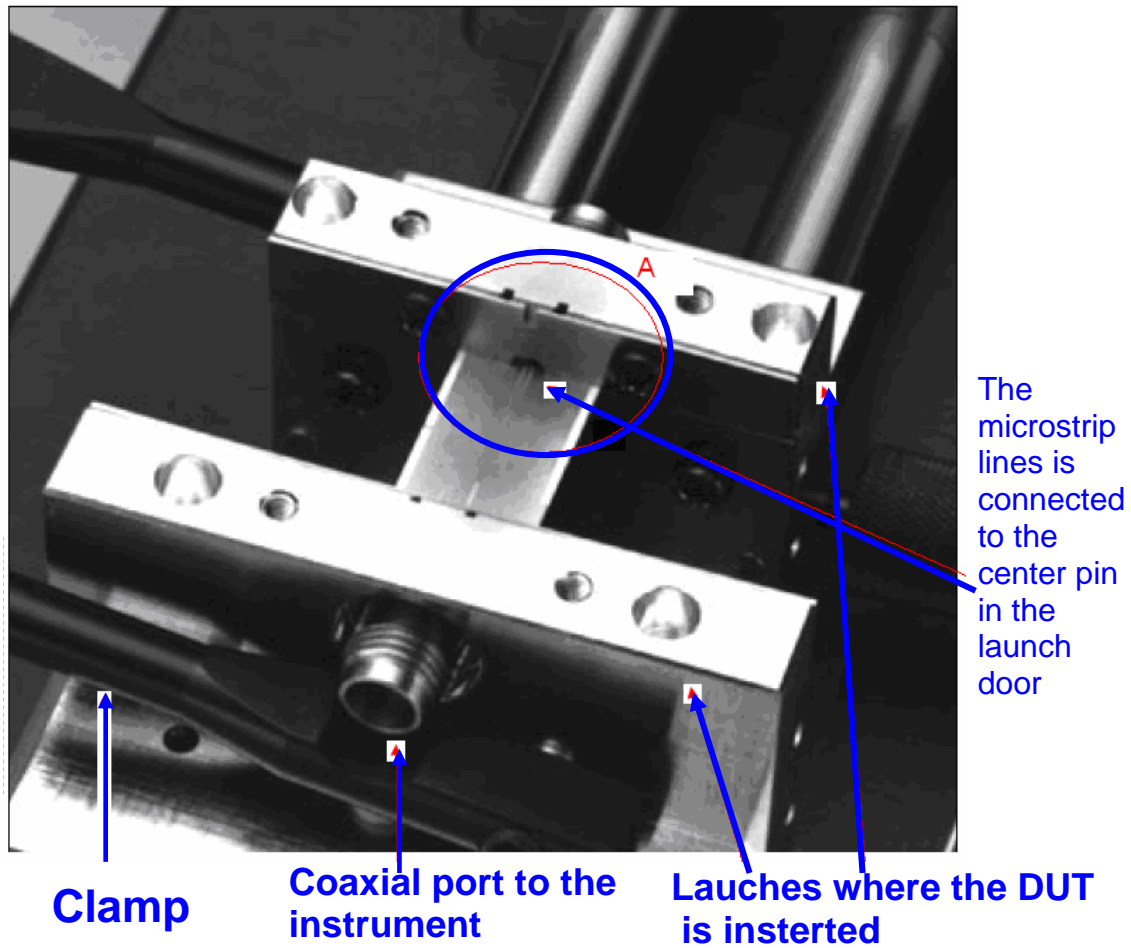


Fig. App. 7.13 Photo of Anritsu 3680 universal test fixture.

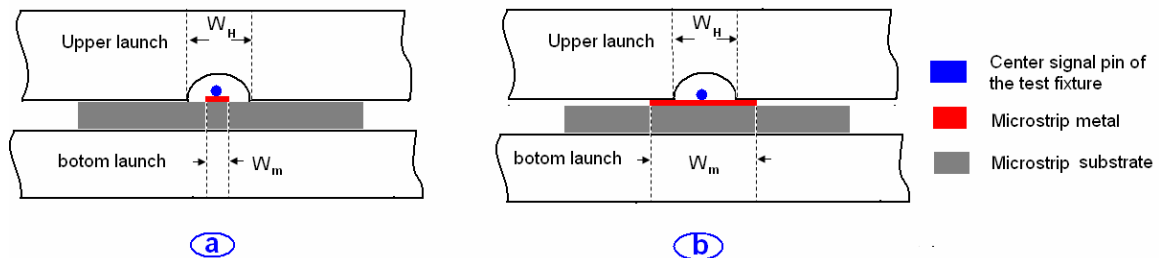


Fig. App. 7.14 The front view of the Anritsu 3680 universal test fixture.

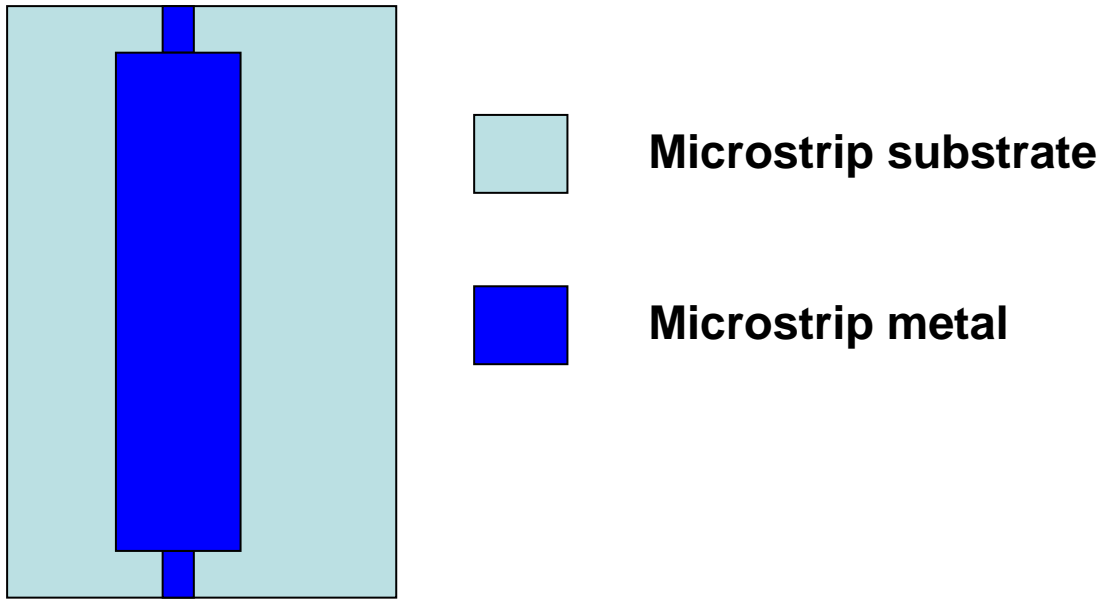


Fig. App. 7.15 Additional thin contacting stub is necessary for the wide microstrip measured in the Anritsu 3680 universal test fixture