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Doping extraction in FinFETs

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This master thesis report is dedicated to:
My beloved mother
M.L. van Rossem - Wijkhuizen 1950-2009

Abstract

In the past decades the minimum transistor size has been down-scaled according to Moore's law. However, scaling of conventional MOSFET devices is limited due to short channel effects, gate insulator tunneling and limited control of doping concentrations. FinFETs are the most promising device structures in order to overcome these negative effects. The gate in a FinFET is wrapped around a thin silicon fin to exercise more control over the conducting channel.

The objective is to try to find a unique doping profile in and near the channel region such that its electrical subthreshold behavior, obtained through device simulations, matches its experimentally determined counterpart, in order to understand which device parameters influence the electrical behavior the most. An advantages of this technique, also known as inverse modeling, is that it is nondestructive.

A (quasi-2D) theoretical model for the subthreshold I-V behavior is deduced, which takes into account the Subthreshold Slope (SS) and the threshold voltage. The device parameters that influences the electrical characteristics the most are the doping profile in the fin, and hence electrical channel length, the oxide thickness, the dielectric constant of the oxide and gate work function. The model is accurate at low and high drain-source voltages for long and short channel devices.

A manual routine is developed to easily extract various device parameters and give insight into the importance of these parameters using device simulations. An initial attempt on automating this routine shows promising results. The routine is verified by extracting device parameters of FinFETs fabricated by IMEC/NXP in Leuven (Salsa 2). The simulation results fit well with its measured counterpart. Only for very short channel devices ($\leq$ 35nm) the doping profile estimation has to be improved. The results show that the electric behavior of FinFETs cannot be described with 2D simulations only.

Nevertheless, it is questionable whether a unique doping profile in and near the channel region can be obtained, because some device parameters are derived based on specifications given by IMEC, such as equivalent dielectric layer thickness, fin dimensions and the doping of the device. When such a parameter is different in reality, a different combination of other device parameters would give similar simulated electrical behavior, such that it still fits nicely with its measured counterpart. Moreover, possibly another combination of lateral and vertical doping profile can be obtained. In order to determine the doping profiles in and near the channel region accurately, especially across the height of the fin, more information is needed.

Contents

Chapter 1

Introduction

1.1 The FinFET structure

For the past decades the advancements in the electronics industry have been primarily based on down-scaling the minimum transistor size according to Moore's law. However, scaling of conventional MOSFET devices is limited due to short channel effects, gate insulator tunneling and limited control of doping concentrations.

An important short channel effect is the so called Drain Induced Barrier Lowering (DIBL). DIBL becomes more prominent as the length of the device is reduced. DIBL is a secondary effect in MOSFETs referring to a reduction of threshold voltage at higher drain voltages. Due to the higher drain voltage the depletion region between the drain and body increases in size and extends under the gate. The potential energy barrier for electrons in the channel is lowered, and hence the drain current increases. As a result, the potential barrier is less affected by the gate, i.e. gate control becomes less, which is not desired.

The effect of DIBL reduces when the gate control on the channel is more prominent [1]. Conventionally this is achieved by reducing the dielectric layer thickness. The down-scaling of gate dielectric thickness is however bounded by the high leakage currents caused by the quantum mechanical phenomenon of electron tunneling. Since the thinner dielectric layer causes the energy barrier width between the gate and the channel to reduce, electron tunneling and thus leakage current through the dielectric layer increases. Gate tunneling is reduced by using thicker gate oxides of insulators with a higher dielectric constant, the so called high-k materials, which increases the barrier width between the gate and the channel. In this way the gate capacitance is kept the same, yielding the same threshold voltage.

The short channel effects can also be suppressed by developing multigate devices [2][3]. In a multigate device, the channel is surrounded by several gates on multiple surfaces, so the control over the channel is improved. Various types of multigate devices are under research such as double gate transistors, FinFETs and gate-all-around FETs.

FinFETs are the most promising device structures to address short channel effects and leakage issues in deeply scaled CMOS, as FinFETs can be fabricated using conventional CMOS processes, and because these can be made in a self aligned pro-

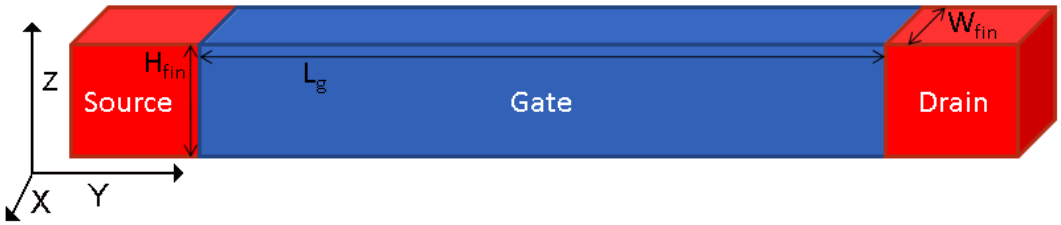


Figure 1.1: A schematic representation of a FinFET including the device dimensions

cess. Moreover the FinFET is an ultrathin body device which eliminates the need of channel doping, thereby reducing parametric spread due to dopant fluctuations and reducing junction leakage due to high electric fields [4]. A steeper Subthreshold Slope Subthreshold Slope (SS) is obtained compared to conventional CMOS, because of the better electrostatic control and absence of doping. Besides the reduction of the leakage current, the multigate topology of the FinFET also increases the drain-source saturation current of the device with a factor two at the same bias condition [1].

In very thin (or narrow) multigate devices, such as a FinFET, volume inversion takes places [5]. In volume inversion charge carriers are not confined near the $(Si - SiO_2)$ interface, but throughout the entire body of the device. Therefore the charge carriers experience less interface scattering. As a result an increase of the mobility and transconductance is expected in multigate devices.

Besides the multiple advantages of the FinFET there are also some drawbacks. Silicon on Insulator (SOI) process is used to fabricate the FinFETs used in this thesis. This process ensures ultra-thin device regions, but could result in problems as self-heating, higher costs and higher defect densities [6].

The short channel effects are reduced by the multiple gate structure of the FinFET. By reducing the fin width the control over the channel is further improved and results in a maximum suppression of short channel effects, but the smaller dimensions of the fin increases the source/drain resistance [7].

The characteristic of the FinFET is that the conducting channel is wrapped around a thin silicon "fin", which forms the body of the device. The dimensions of the fin determine the effective channel length and gate width of the device. Figure 1.1 shows the device parameters. When the fin is cut in the z direction, a FinFET can be considered as double gate device. The top gate is not taken into account. A 2D representation of a FinFET is depicted in figure 1.2.
The crucial geometric device dimensions are:

$L_{\mathbf{gate}}$ = Printed gate length, defined as the length of the gate metal.

$H_{\mathbf{fin}}$ = Height of the fin defined as the distance between the Buried Oxide (BOX) and the top gate oxide.

$W_{\mathbf{fin}}$ = Width of the fin

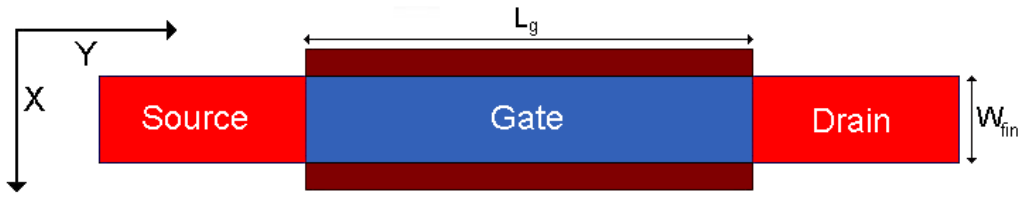


Figure 1.2: A 2D cross-section of the FinFET

Because the channel is wrapped around the surface of the fin, the gate width of a FinFET is commonly assumed to be twice the fin height (H_{fin}) plus the fin width (W_{fin}) at strong inversion mode [8]. If the aspect ratio is high the channel width can be approximated by twice the fin height[8]. The electrical or effective channel length L_{eff} is defined as the spacing between the electrical source and the drain depletion layers inside the channel region. An important note is that in this work we assume that the designed gate length (design on layout, DOL) equals the physical gate length L_{g} (design on silicon, DOS). In reality the difference between these two parameters could be considerable and induce a Δ L. Also we neglect the effect of line-edge roughness (LER).

The maximum gate width of a FinFET is determined by the technological limit of the aspect ratio ($H_{\text{fin}}/W_{\text{fin}}$). The width can also be increased by placing multiple fins in parallel, which results in an integer number of possible gate widths.

1.2 Motivation

Due to the down scaling of transistors, the extension of the source and drain doping profiles into the channel region has a large influence on the performance of the device, because the electrical channel length is adjusted. In fabricated FinFETs the doping profiles are not accurately known.

The objective is to try to find a unique doping profile in and near the channel region, or in short "the doping profile", such that its electrical subthreshold behavior, obtained through device simulations, matches its experimentally determined counterpart, in order to understand which device parameters influence the electrical behavior the most and thereby understanding the functioning of the device better.

An estimation of the device parameters and especially the "doping profile" can be made by inverse modeling [9] of the subthreshold current. In this technique the device is built in a device simulation and by adjusting the device parameters the simulated electrical behavior is fitted to its experimentally determined counterpart. One of the advantages of this technique is that is nondestructive: the devices will still function after using this technique, but no special test structures are needed.

A common technique to determine the doping profile is the capacitance voltage method through inverse modeling. The small signal capacitance of a depletion region is measured for various depletion widths. Then the doping profile can be calculated from the CV data.The sensitivity of CV methods is excellent, especially

for low doping levels [10]. However for the small devices special test structures are needed.

In literature an inverse modeling technique is described for the characterization of two-dimensional doping profiles in conventional deep submicrometer MOSFET's using current-voltage characteristics in the subthreshold region [11].

The characterization of the doping profile is done in the subthreshold regime, because the subthreshold I_{ds}-V_{gs} characteristic is sensitive to electrostatic potential distribution in the depletion region of the channel, which in turn depends on the applied potential at the source, drain, bulk and gate and the doping.

The technique as proposed in [11] is based on obtaining a 2-D doping profile such that the simulated subthreshold I_{ds}-V_{gs} characteristics, over a broad range of bias conditions (i.e. V_{gs}, V_{ds} and V_{bs}) match the corresponding experimental data. The only parameter information needed in advance are the gate width, gate dielectric thickness and dielectric constant.

Since the surface potential (φ_s) depends on the net dopant distribution in the device, a measure of φ_s at different biases provides information of the dopant distribution [1]. The I_{ds}-V_{gs} dependence of V_{ds} contains information referring to the source/drain junction configuration. In addition the shift of the I_{ds}-V_{gs} curves due to the body effect as V_{bs} is applied also provides doping information in the depth direction.

For extracting the doping profile of a device, the parameters representing the 2-D profile are varied until a best fit is achieved at various bias conditions.

The main advantages of the subthreshold technique are as follows [11]:

- It is capable of extracting the 2-D doping profile (including channel-length) of deep submicron devices because of its immunity to parasitic resistance, capacitance, noise, and fringing electric fields.
- It does not require any special test structures since only subthreshold I_{ds}-V_{gs} data are used.
- It has very little dependence on mobility and mobility models.

The method for extracting the doping profile of conventional MOSFETs in the subthreshold regime can be applied on FinFETs as well which is believed to be novel. As with conventional MOSFETs the electrical behavior of FinFETs is governed by the applied bias conditions. However the SOI FinFET does not have a bulk contact, therefore the dopant distribution in the depth direction is harder to determine.

[1] The doping dependence of the surface potential in a FinFET is only in the direction of the current flow. For bulk MOSFET however, the surface potential is also affected by the doping perpendicular to the current flow.

1.3 Aim and Outline

The aim of this thesis is to investigate whether a (unique) doping profile in and near the channel region, or in short we address this by "the doping profile", can be extracted from subthreshold current. The doping profile in FinFETs will be determined through device simulations in the subthreshold region.

This thesis consists of several parts. In chapter 2, a theoretical model of the subthreshold current, for long and short channel devices, is discussed in order to understand which device parameters have significant influence on the variation of the SS.

In chapter 3 some device parameters are deduced from measurements such as the work function of the gate material and the channel length and the theoretical and measured I_{ds}-V_{gs} behavior is compared.

In chapter 4 the process parameters are extracted by simulations. First a long channel device is fitted in order to subtract the gate work function then down-scaled devices are simulated in order to determine other device parameters. By looking at the threshold voltage, DIBL and SS a model of the device can be obtained that is hopefully close to the real device.

Chapter 5 describes an automated method to extract the device parameters.

Chapter 2

Theory

I_d - V_{gs} measurements on FinFETs across a wafer show variations in the SS. In order to understand which device parameters have significant influence on the variation of the SS, some theory of the subthreshold current will be discussed in this chapter.

In the first section a formula for the subthreshold current is derived. In the other paragraphs important parameters that have an influence on the subthreshold current are discussed, such as the SS and the effective channel length (L_{eff}). Per parameter is discussed how device variables influence the behavior of the subthreshold current.

2.1 Subthreshold current

To model the subthreshold current, only the diffusion component is considered, as in subthreshold the drift component of the current is negligible.

By applying low gate-source voltages, electrons diffuse from the source to the drain yielding the electron injection at the edge of the source-fin depletion layer for a NMOS being:

$$n_p(x_{dp}) = n_{p0} = \frac{n_i^2}{p} \approx n_i e^{\frac{\psi(x)}{\mu_t}}, \tag{2.1}$$

And at the drain side:

$$n_p(x_{dp} + L_{eff}) = n_{p0} e^{\frac{-V_{ds}}{\mu_t}}, \tag{2.2}$$

The carrier density in the y-direction, i.e. perpendicular to the gate dielectric, is presumed constant, since the surface potential in the subthreshold regime is constant. n_p is the minority concentration (in this case electrons), x_{dp} the position of the depletion layer edge at the source side of the channel, n_i the intrinsic carrier concentration, p the hole concentration, $\psi(x)$ the (surface) potential, μ_t the thermal voltage ($\frac{kT}{q}$) and (L_{eff}) the electrical or effective channel length, defined as the

spacing between the electrical source and the drain depletion layers (as discussed in paragraph 2.3). The diffusion current density can be expressed as [12]:

$$J_n(x) = qD_n \frac{dn}{dx}, \tag{2.3}$$

where n is the electron density at the source and drain side given by equation (2.1) and equation (2.2) respectively and D_n the diffusion constant.

(2.1), (2.2) and (2.3) (assuming no recombination between the source and the drain) results in:

$$J_n(x) = qD_n \frac{n_p(x_{dp} + L_{eff}) - n_p(x_{dp})}{L_{eff}} \tag{2.4}$$

$$= qD_n \frac{n_i}{L_{eff}} e^{\frac{\psi(x)}{\mu_t}} \left(1 - e^{\frac{-V_{ds}}{\mu_t}}\right). \tag{2.5}$$

Now the drain source current (I_{ds}) can be calculated from the current density, since the distribution of the electron concentration is constant perpendicular to the gate dielectric (volume inversion):

$$I_{ds} = J_n W_{fin} H_{fin}, \tag{2.6}$$

with J_n the current density and W_{fin} the fin width and H_{fin} the height of the fin, respectively. The formula for the drain current in subthreshold becomes:

$$I_{ds} = qD_n \frac{n_i W_{fin} H_{fin}}{L_{eff}} e^{\frac{\varphi_s}{\mu_t}} \left(1 - e^{\frac{-V_{ds}}{\mu_t}}\right). \tag{2.7}$$

To relate the potential (φ_s) to the applied voltage V_{gs}.

The gate-source voltage is distributed over the oxide and the silicon: V_{gs}= V_{si}+V_{ox} with V_{ox} the charge over C_{ox} and V_{si} is $\varphi_s + \Delta\phi_f$. Because the inversion carrier concentration in subthreshold is generally negligible, we could state that the gate voltage falls only over the Silicon: V_{gs}=$\varphi_s + \Delta\phi_f$. I.e. the surface potential is equal to V_{gs}-$\Delta\phi_f$ [1]. However, because of the depletion capacitances from the source- and drain-body junctions the subthreshold current is less controlled by the gate as will be explained later. This is modeled with the so-called ideality factor (m) which gives information on the SS. Implementing this in equation (2.7) gives

$$I_{ds} = qD_n \frac{n_i W_{fin} H_{fin}}{L_{eff}} e^{\frac{V_{gs} - \Delta\phi_f}{m\mu_t}} \left(1 - e^{\frac{-V_{ds}}{\mu_t}}\right). \tag{2.8}$$

The SS depends on a charge divider circuit of the oxide capacitance and the depletion (sidewall) capacitances from the source- and drain-body junctions. The depletion capacitance depends on the doping of the body, while the oxide capacitance is determined by the thickness and permittivity of the gate oxide.

For long channel devices the ideality factor is 1, because the current is insensitive for variation in the thickness and permittivity of the oxide and the doping of the device. For long channel devices the work function difference ($\Delta\phi_f$) is the most important parameter that determines the subthreshold current. Therefore the

$\Delta\phi_f$ can be extracted from the current voltage behavior of a long channel device, as shown in chapter 3.

Since the SS gives information on the doping profile in and near the channel region of shorter channel devices some explanation on this topic is required.

2.2 Subthreshold slope

From equation (2.8) we obtain:

$$\begin{aligned} \log I_{ds} &= \log(I_0 e^{\frac{V_{gs}}{m\mu_t}}) \\ \log I_{ds} &= \frac{\ln(I_0 e^{\frac{V_{gs}}{m\mu_t}})}{\ln(10)} \\ \log I_{ds} &= \frac{\ln(I_0) + \frac{V_{gs}}{m\mu_t}}{\ln(10)} \end{aligned} \tag{2.9}$$

The SS is defined as the variation of gate voltage necessary for producing one decade change in the drain current. The SS is expressed in mV/dec.

$$SS = (\frac{\mathrm{d}\log I_{ds}}{\mathrm{d}V_{gs}})^{-1} \tag{2.10}$$

$$\begin{aligned} \frac{\mathrm{d}\log I_{ds}}{\mathrm{d}V_{gs}} &= \frac{1}{m\mu_\mathrm{t}\ln(10)} \\ SS &= m\mu_\mathrm{t}\ln(10) \\ SS &= m59{,}6\ \mathrm{mV/dec} \end{aligned} \tag{2.11}$$

with m the ideality factor which depends on a charge divider circuit of the oxide capacitance and the depletion capacitances.

This relation for m is only valid for long channel devices and does not hold for short channel devices due to the short-channel effects. When the devices become shorter the channel potential changes by the capacitances between the channel region and the source/drain junction. Figure 2.1 depicts a small signal representation of the capacitance divider circuit.

When this effect is taken into account the SS can be adjusted to [13]:

$$m = 1 + \frac{C_{//}}{C_{ox}}. \tag{2.12}$$

For $C_{//}$ holds:

$$C_{//} = C_{SC} + C_{DC}, \tag{2.13}$$

The depletion capacitance in (fully depleted) FinFETs is negligible because Q_{fin} is zero, which results in:

$$m \approx 1 + \frac{C_{SC}}{C_{ox}} + \frac{C_{DC}}{C_{ox}}, \tag{2.14}$$

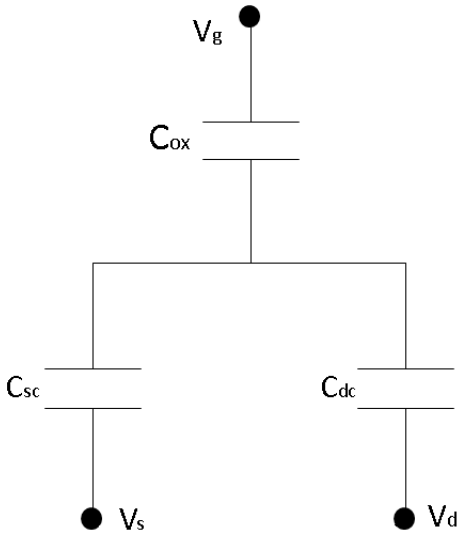


Figure 2.1: Small signal capacitor model of SCE, according to [13]

where C_{SC} and C_{DC} represent the channel-junction capacitance at the source respectively drain side. The channel-junction capacitance is a function of channel length and drain source voltage as will be explained next in a qualitative way.

The source/drain-channel junction capacitance can be calculated by:

$$C_{sc/dc} = \frac{\mathrm{d}Q_{s/d}}{\mathrm{d}V_{g,s/d}}, \tag{2.15}$$

with

$$Q_{s/d} = qN_aW_{fin}h_{fin}, \tag{2.16}$$

where N_a the doping-concentration in the channel region.

The voltage over the source-channel capacitance is defined as

$$V_{g,s} = V_{bi} - \psi(x_0), \tag{2.17}$$

and for the drain-channel capacitance

$$V_{g,d} = V_{bi} + V_{ds} - \psi(x_0), \tag{2.18}$$

with V_{bi} the built-in potential between the channel and source/drain junction, $\psi(x_0)$ minimum potential in the channel. The minimum channel potential is obtained by determining at which point the electric field is zero

$$\frac{\partial\psi}{\partial x}|_{x=x_0} = 0 \tag{2.19}$$

and calculating the channel surface potential at this point.

The surface potential can be calculated by applying Gauss's law to a rectangular box (Gaussian box) of height W_{fin} and length Δx in the channel depletion region

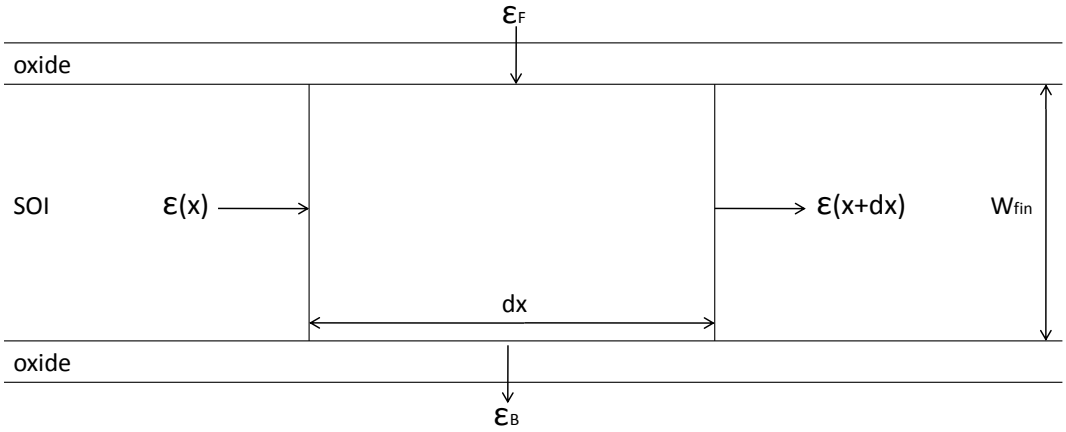


Figure 2.2: Rectangular box (Gaussian box) of height W_{fin} and length Δx of a 2D representation of the FinFET with the influence of the lateral and orthogonal electric fields.

and neglecting mobile charge see figure 2.2, in which a 2D cross section from Fig. 1.1 is taken. The following equation can be derived [14] under the assumption that the electric field does not depend on y, hence the junction depth is constant and consists of an abrupt doping profile

$$-W_{fin}\frac{\partial\varepsilon(x)}{\partial x} - 2C_{ox}(V_{gs} - \Delta\phi_f - \psi_s) = qN_aW_{fin}, \tag{2.20}$$

where $\varepsilon(x)$ is the lateral electric field, C_{ox} the oxide capacitance, V_{gs} the gate-source voltage, $\Delta\phi_f$ the work function difference, ψ_s the surface potential, N_a the channel doping and W_{fin} the fin width.

The solution to the above equation under the boundary conditions of $\psi_s(0)=V_{bi}$ and $\psi_s(L)=V_{ds} + V_{bi}$ is

$$\psi_s(x) = \psi_{sL} + (V_{bi} + V_{ds} - \psi_{sL})\frac{\sinh(\frac{x}{l})}{\sinh(\frac{L_g}{l})} + (V_{bi} - \psi_{sL})\frac{\sinh(\frac{L_g-x}{l})}{\sinh(\frac{L_{ch}}{l})}, \tag{2.21}$$

with $\psi_{sL}=V_{gs}$-$\Delta\phi_f$ the long channel surface potential. V_{bi} is the built-in potential between the source-channel and drain-channel junctions and l is the characteristic length defined as

$$l = \sqrt{\frac{\epsilon_{si}W_{fin}}{2C_{ox}}}. \tag{2.22}$$

The minimum potential can be solved by $\psi_{smin}=\psi_s(x_0)$, which results in

$$\psi_{smin} = \psi_{sL} + (V_{bi} + V_{ds} - \psi_{sL})\frac{\sinh(\frac{x_0}{l})}{\sinh(\frac{L_g}{l})} + (V_{bi} - \psi_{sL})\frac{\sinh(\frac{L_g-x_0}{l})}{\sinh(\frac{L_{ch}}{l})}. \tag{2.23}$$

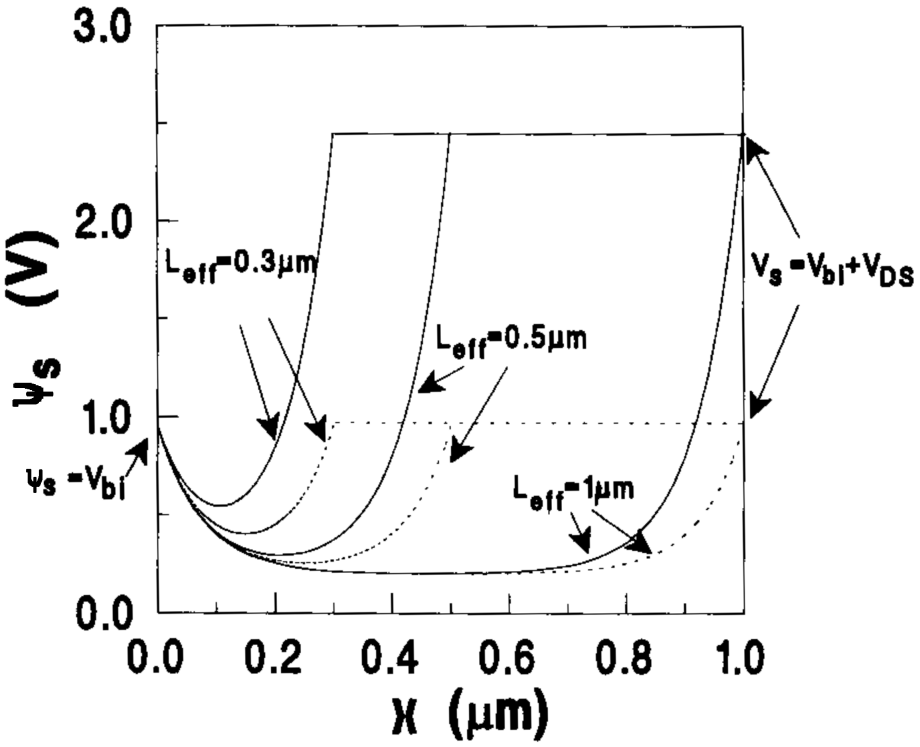


Figure 2.3: Minimum surface potential versus effective channel length [14]

The minimum potential is mainly determined by the effective channel length and the applied bias voltages. For low drain-source voltages the minimum potential is located at the center of the channel (x_0=0.5 L_g). For higher V_{ds} the minimum potential point shifts towards the source. The location of the minimum potential when $L_g \gg l$ can be found by equation 2.24 [14]

$$x_0 = \frac{L_{ch}}{2} - \frac{l}{2}\ln(\frac{V_{bi} - V_{sL} + V_{ds}}{V_{bi} - V_{sL}}), \tag{2.24}$$

with V_s the minimum surface potential, L_g the gate length and V_{ds} the drain-source voltage.

The minimum potential increases with decreasing gate length. For high V_{ds} the minimum surface potential will increase even more as depicted in figure 2.3.

Due to the increase of the minimum surface potential, the channel-source/drain capacitance will increase and accordingly the SS increases (see also equation (2.14)).

The fin width also has influence on the SS. The charge in the capacitors between the channel and source/drain junction depends on the fin width, see equation (2.16). This influence is rather small, a linear dependence, compared to the influence on the minimum surface potential, which is exponential according to equation (2.19). The minimum surface potential is indirectly affected by the fin width, because of the fin width dependence of the characteristic length, see equation (2.22). When the

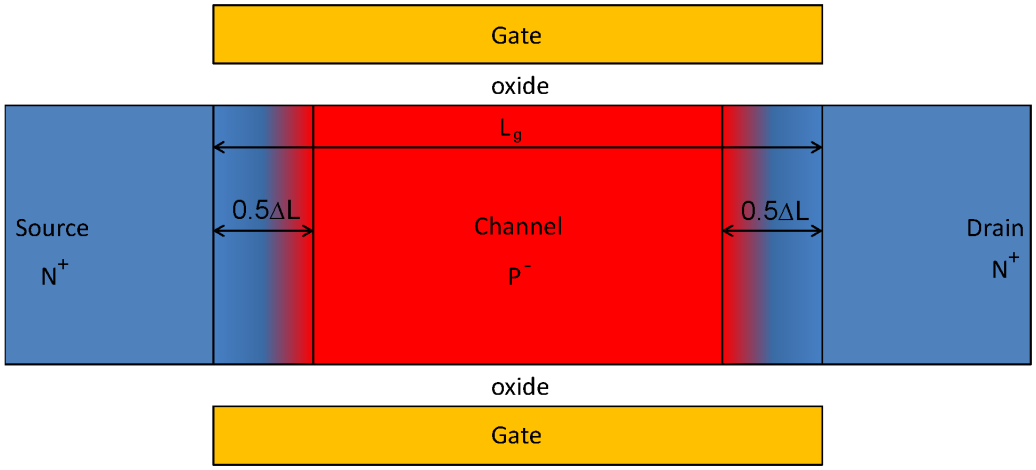


Figure 2.4: The effective channel length defined as the (physical) gate length (L_g) minus ΔL

fin width decreases, the characteristic length decreases, accordingly the minimum surface potential decreases. As a result the channel-source/drain capacitance will decrease and accordingly the m decreases.

All in all the SS becomes more sensitive to variations in thickness and permittivity of the dielectric layer, the doping profile in and near the channel region of the fin and fin width when the length of the device is decreased, because of the characteristic length (see equation (2.22)). However the thickness and permittivity of the oxide will hardly vary at a given process node, as a result the SS is mainly influenced by the doping profile in and near the channel region.

2.3 Electrical channel length

As integrated circuit technology advances and the geometric dimensions shrink, the channel length shrinks too. Accurate determination of L_{eff} becomes more important, because it is critical for the performance of the device.[15]

As stated earlier, the electrical or effective channel length Leff is defined as the spacing between the electrical source and the drain depletion layers inside the channel region. The difference between effective channel length and the physical gate length (L_g) is defined by a parameter ΔL, as depicted in figure 2.4. The ΔL could be caused by side-diffusion of source/drain dopants into the fin region, non-ideal patterning of the gate structure and modulation of the doping of the source/drain regions under or near the gate

$$L_{eff} = L_g - \Delta L. \tag{2.25}$$

For long channel devices the ΔL is negligible. However, for short channel devices the ΔL affects the effective channel length significantly. Accordingly the position of the minimum surface potential is affected and as a result the SS is affected. An important note is that in this work we assume that the designed gate length (design

on layout, DOL) equals the physical gate length LG (design on silicon, DOS). In reality the difference between these two parameters could be considerable and induce an additional ΔL. However analogue to an earlier report [11] we neglect this ΔL. Also we neglect the effect of line-edge roughness (LER).

2.4 Threshold voltage

The threshold voltage can be adjusted by using a metal gate with an appropriate gate work-function [1]. However when the fin thickness is decreased below 10 nm, two more contributions to the threshold voltage have to be taken into account [16].

The first contribution originates from the fact that the potential at which the mobile charge at the Si - SiO_2 interface is inverted is larger then the classical $2\phi_b$ [17] for a partially depleted FinFET in bulk Silicon.

The second contribution arises from the splitting of the conduction and valence band into subbands, due to quantum confinement, therefore the minimum energy of the subbands increases when the fin thickness decreases, which increases the gate voltage needed to reach threshold.

Combining the gate work function difference between the gate and the silicon fin, the increase in potential and the increase in bandgap results in the following threshold voltage formula [16]:

$$V_{th} = \Delta\phi_f + \frac{kT}{q}\ln\frac{2C_{ox}kT}{q^2 n_i W_{fin}} + \frac{\pi^2 h^2}{2qm^* t_{si}^2}, \tag{2.26}$$

with W_{fin} the fin thickness, h Planck's constant and m^* the quantization effective mass.

The FinFETs used in this thesis have a doped fin. The doping (N_a) of the device has influence on the threshold voltage.

As a result the threshold voltage relation for a partially depleted FinFET in bulk silicon becomes:

$$V_{th} = \Delta\phi_f + (2\phi_b + V_{bs}) + \frac{\sqrt{2\epsilon_{si}qN_a(2\phi_b + V_{bs})}}{C_{ox}} + \frac{kT}{q}\ln\frac{2C_{ox}kT}{q^2 n_i W_{fin}} + \frac{\pi^2 h^2}{2qm^* t_{si}^2}, \tag{2.27}$$

with

$$\phi_b = \frac{kT}{q}\ln\frac{N_a}{n_i}. \tag{2.28}$$

The FinFETs used in this thesis do not have a bulk contact, because of the SOI layer. These equations hold for long channel devices. For short channel devices the diffusion of the source/drain junction into the channel region becomes significant. As a result of the diffusion of the source/drain junctions the fin doping changes and accordingly the threshold voltage changes.

For long channel devices the threshold voltage is determined by the work function difference. For short channel devices the variation of doping concentration in the fin

due to indiffusion of the source/ drain doping becomes significant and will result in a shift of the threshold voltage. Therefore the shift in the subthreshold current gives information about the magnitude of the indiffusion of the source/ drain doping into the fin.

2.5 Gate induced drain leakage

Gate Induced Drain Leakage (GIDL) can arise when a high electric field is present under the gate/drain overlap region. This high electric field in combination with a ultra-small depletion layer width causes band-to-band tunneling in the drain region underneath the gate. When there is a large gate to drain bias, there can be sufficient energy band bending near the interface between the silicon and the gate dielectric for valence band electrons to tunnel into the conduction band. GIDL depends on the shape and height of the doping profile in and near the channel region but also on interface states. Interface states are energy states in which electrons are localized in the vicinity of a material's surface. Interface states introduce energy levels in the band gap at the Si-SiO_2 interface. However GIDL is not necessarily determined by interface traps, but also by band-to-band (b2b) tunneling, but also just by (bulk) traps [17] [18].

The interface traps charge and discharge governed by the applied bias, thereby affecting the charge distribution inside the device, the V_g-ϕ_s relationship and thus the current-voltage characteristic and the SS [18]

$$\Delta V_g(\text{interface states}) = -\frac{Q_{it}(\phi_s)}{C_{ox}}, \tag{2.29}$$

with ΔV_g(interface states) the change in applied bias and Q_{it} the charge due to the interfacial traps.

For example when an n type MOSFET is biased into inversion the surface fermi level lies close to the valence band and all traps will be empty. If the states are assumed to be donor like (positively charged when empty and neutral when filled with an electron), Q_{it}, the charge due to the interfacial traps, will be positive. Changing the bias to depletion condition positions the surface fermi level near the middle of the band gap. Now the lower interface will be filled and Q_{it} decreases. Finally when the device is biased in accumulation all the interface states will be filled with electrons and Q_{it} approaches it's minimum.

Besides the influence on GIDL and SS, the interface states also affect the threshold voltage.

$$V_{th} = V_{th'} - \frac{Q_{it}(\phi_s)}{C_{ox}}, \tag{2.30}$$

with $V_{th'}$ the threshold voltage as determined without interface states.

In summary, the interface states affect the behavior of the devices negatively in several ways. Despite of the possible importance, obtaining the correct interface traps (and density) is beyond the scope of this thesis. On the other hand, since

there is volume inversion it is expected that the SS is much less affected in FinFETs than it is for the bulk counterparts.

2.6 Discussion

In this chapter several relationships between the important parameters affecting the subthreshold current were derived or introduced. The parameter that has the largest influence on the device characteristics is the doping profile in and near the channel region in the fin (and hence the effective channel length), the oxide thickness, the dielectric constant of the oxide and gate work function.

The doping profile in and near the channel region has influence on the drain current of the device, because it has influence on the effective channel length and threshold voltage. The work function difference has also an influence on the threshold voltage.

The gate work function can be derived from the current voltage behavior of long channel devices, while the shape of the doping profile in and near the channel region can be extracted from the SS and shift in the threshold voltage for short channel devices.

A way of extracting the different device parameters from measurements is described in the next chapter.

Chapter 3

Measurements

According to theory the electric behavior is determined by various device parameters. In this chapter will be investigated wether current voltage characteristic behaves according to theory. It will be shown that some device parameters can be deduced from measurements such as the work function of the gate material and the electrical channel length.

The FinFETs used in this thesis are fabricated by IMEC/NXP Research in Leuven. The maskset is Salsa 2, the modules measured [1] are module E20N, module E21N, module E01N and E07N, this are a N type devices with a fin width of 10nm, 20nm, 5nm and 30nm respectively, with various gate lengths (20nm, 25nm, 30nm, 35nm, 45nm, 70nm, 90nm, 130nm, 250nm, 1μm, 10μm). Module E20N and module E21N are single FinFETs, while module E01N and E07N 5 fins are placed in parallel with a pitch of 200nm [4], [19].

3.1 Current voltage behavior

According to equation (2.8) there are several device parameters that influence the current voltage behavior of the device. The dependence on the channel length (L_{eff}), width (W_{fin}) and applied drain voltage can be deduced from measured I_{ds}-V_{gs} characteristics.

For increasing gate length the subthreshold current ($V_{gs} < V_{th}$) is expected to decrease according to equation (2.8). When the transistor is turned on ($V_{gs} > V_{th}$) a channel is created which allows a relatively high current to flow between the drain and source. The current from drain to source is modeled as [17],[20]:

$$I_{ds} = \frac{\mu_n C_{ox} W_{eff}}{L_{eff}}((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}), \tag{3.1}$$

with μ_n the charge-carrier effective mobility, W_{eff} the effective channel width and L_{eff} the effective channel length. In first order approximation the effective channel width W_{eff} equals the channel width. However, additional physical effects in FinFETs such as corner effects and current spreading in the channel region could

[1] courtesy of Dr.ir. M.J.H. van Dal at TSMC Belgium (formerly with NXP Research)

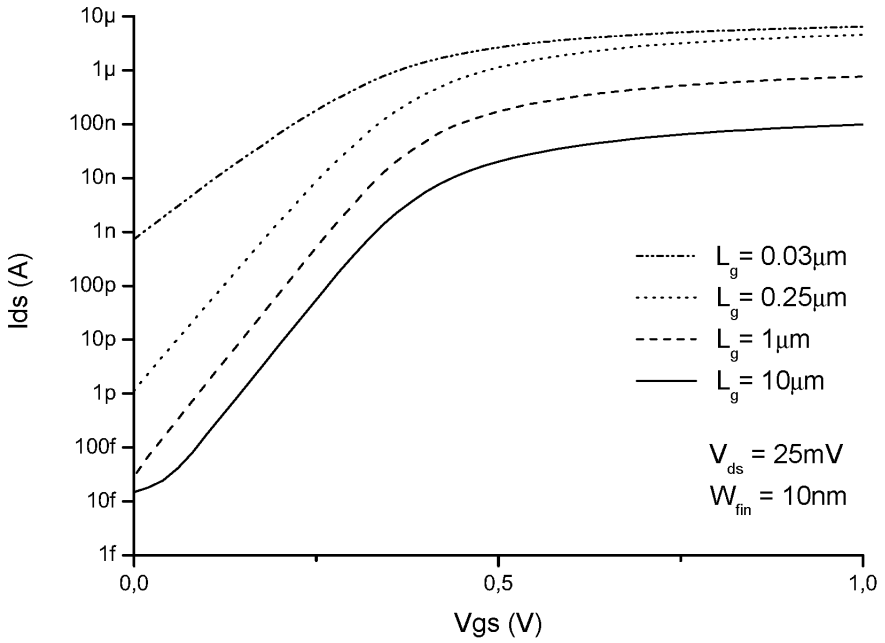


Figure 3.1: Measured and theoretical I_{ds}-V_{gs} characteristic for different gate lengths with W_{fin} = 10nm, and V_{ds} = 25mV of the Salsa2 module E20N

cause the W_{eff} to be bigger than the W. These effects will be addressed in chapter 4. The current in super threshold is, as in subthreshold, inversely dependent on the gate length. The measured I_{ds} - V_{gs} characteristic for various gate lengths at a fin width of 10nm, and a V_{ds} of 25mV is depicted in figure 3.1.

The doping profile in the device has influence on the effective channel length of the device. The ΔL is caused by side-diffusion of source/drain dopants into the fin region (as discussed in paragraph 2.3). For short channel devices the indiffusion of the source/drain junctions becomes significant and consequently the effective channel length is reduced significantly. This reduction of the channel length affects the current-voltage behavior of the device.

The (actual) channel width of the device also has influence on the current-voltage behavior. The channel width of the device is commonly defined as twice the height of the fin plus the width of the fin (W=2H_{fin}+W_{fin})[8]. The current increases with increasing fin width in subthreshold due to volume inversion, while in active or superthreshold mode the current voltage characteristic is determined by the perimeter or width of the gate and consequently the current scales with W, as depicted in equations (2.8) and (3.1). In superthreshold the variation in channel width due to variation in fin width is small because the channel width is mainly determined by twice the fin height accordingly the variation in fin width has a small influence on the current-voltage behavior. The measured current voltage behavior for two channel widths, W_{fin}=10nm and W_{fin}=20nm at a gate length of 0.25μm and a V_{ds} of 25mV is depicted in figure 3.2.

For short channel devices the the fin width does not only influences the mag-

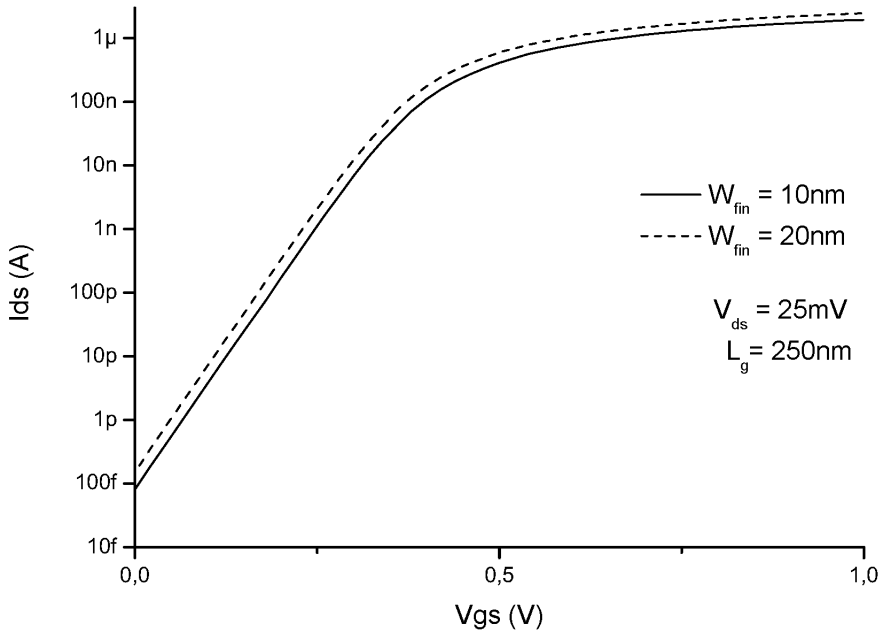


Figure 3.2: Measured I_{ds}-V_{gs} characteristic for different fin widths with $L_g = 0.25\mu$m and V_{ds} = 25mV of the Salsa2 module E20N and module E21N

nitude of the current, but also the SS, as described in paragraph 2.2. Short channel effects reduce when the gate control on the channel is more prominent, this is achieved by reducing the fin width. The measured current voltage behavior for two channel widths, W_{fin}=5nm and W_{fin}=30nm at a gate length of 35nm and a V_{ds} of 25mV is depicted in figure 3.3.

The figure depicts that the SS increases at smaller fin width, so the short channel effects indeed reduce at smaller fin width.

Besides the influence of the dimensions of the device the applied drain voltage governs the current voltage characteristic of a FinFET. In subthreshold the drain current varies with one minus the inverse exponent of the drain - source voltage divided by the thermal voltage ($1\text{-}e^{\frac{-V_{ds}}{\mu_t}}$). As a result the drain current increases with increasing V_{ds}. When a drain-source voltage of 25mV is applied this term is 0.6; for a drain-source voltage of 1V this term is 1, both at room temperature. When the transistor is turned on and $V_{ds} \ll V_{gs} - V_{th}$, substituting in equation (3.1), the drain current is a linear function of V_{ds} [17],[20]:

$$I_{ds} \approx \frac{\mu_n C_{ox} W_{eff}}{L_{eff}} (V_{gs} - V_{th}) V_{ds}. \tag{3.2}$$

According to this equation the drain current varies linearly with the overdrive voltage and drain voltage.

As the V_{ds} becomes equal to $V_{gs} - V_{th}$ the drain current (more or less) saturates. However when the V_{ds} becomes larger than $V_{gs} - V_{th}$ the inversion layer does not

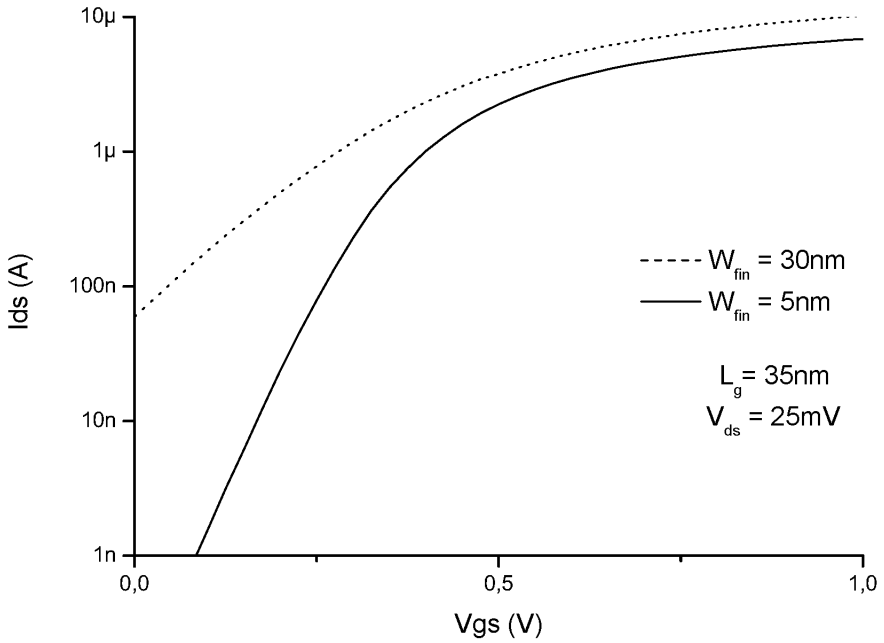


Figure 3.3: Measured I_{ds}-V_{gs} characteristic for different fin widths with L_g = 0.035μm and V_{ds} = 25mV of the Salsa2 module E01N and module E07N

end at the drain region but at $x \leq L_{eff}$ and the channel is 'pinched off'. The actual channel length therefore reduces as the potential difference between the gate and drain increases. This effect is called channel length modulation. Writing $L'_{eff} = L_{eff} - L_{var}$ i.e. $\frac{1}{L'_{eff}} \approx \frac{(1+\frac{L_{var}}{L_{eff}})}{L_{eff}}$ and assuming a first-order relationship between $\frac{L_{var}}{L_{eff}}$ *and* V_{ds} such as $\frac{L_{var}}{L_{eff}} = \lambda V_{ds}$. Substituting in equation (3.1) for $V_{ds} \gg (V_{gs} - V_{th})$, The drain saturation drain current then becomes [17],[20]:

$$I_{ds} \approx \frac{\mu_n C_{ox} W_{eff}}{2L_{eff}} (V_{gs} - V_{th})^2 (1 + \lambda V_{ds}). \tag{3.3}$$

According to this equation the drain current varies quadratically with the overdrive voltage and linearly with the drain voltage. For shorter devices the channel length modulation effects becomes more prominent. The measured current voltage behavior for a device with a gate length of 10μm and fin width of 10nm for various V_{ds}, 25mV and 1V respectively, is depicted in figure 3.4.

In the figure can be seen that for a V_{ds} of 25mV in active mode the drain current increases slightly with increasing overdrive voltage. For a V_{ds} of 1V in active mode the drain current increases faster with the overdrive voltage then at a V_{ds} of 25mV, as expected. For low gate-source voltages the current increases, which is caused by GIDL, as described in paragraph 2.5.

At high V_{ds} and short channel devices the fin width also affects the SS, as described in paragraph 2.2. At high drain-source voltage short channel effects are prominent. These effects are reduced by reducing the fin width and therefor im-

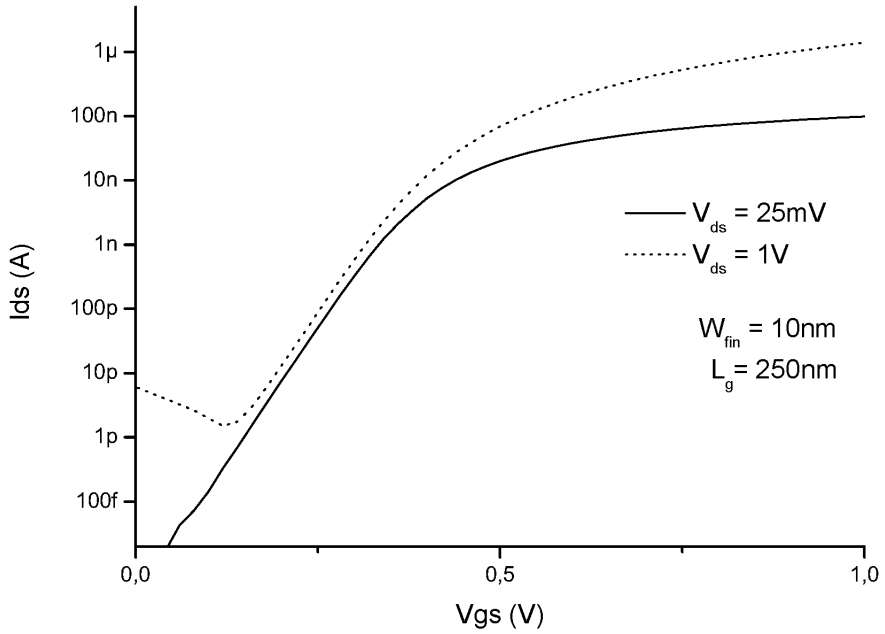


Figure 3.4: Measured I_{ds}-V_{gs} characteristic for different drain voltages with L_g = 10μm and W_{fin} = 10nm of the Salsa2 module E20N

proving the gate control on the channel. The measured current voltage behavior for two channel widths, W_{fin}=5nm and W_{fin}=30nm at a gate length of 35nm and a V_{ds} of 1V is depicted in figure 3.5.

Discussion

In this paragraph several parameters are discussed that have influence on the current-voltage behavior of FinFET's. Besides the influence of these parameters the doping profile also has significant influence on the current-voltage behavior. Parameters that are directly influenced by the doping profile such as the SS, effective channel length and threshold voltage can be deduced from measurements.

3.2 Subthreshold slope versus gate length

When devices become shorter the surface potential changes by the capacitances between the channel region and the source/drain junction. The capacitances between the channel region and the source/drain junction are influenced by the indiffusion of the source/drain doping into the fin. The SS of the device is related to the surface potential.

For a long channel device the ideality factor is close to one and hence the SS is approximately 60 mV/dec (see equation(2.10)). For shorter channel devices the capacitances between the channel region and the source/drain junction become significant and will influence the magnitude of the SS according to equation (2.14). Because the SS for short channel devices is influenced by the indiffusion of the source/drain junctions into the fin the behavior of the SS versus gate length plot is

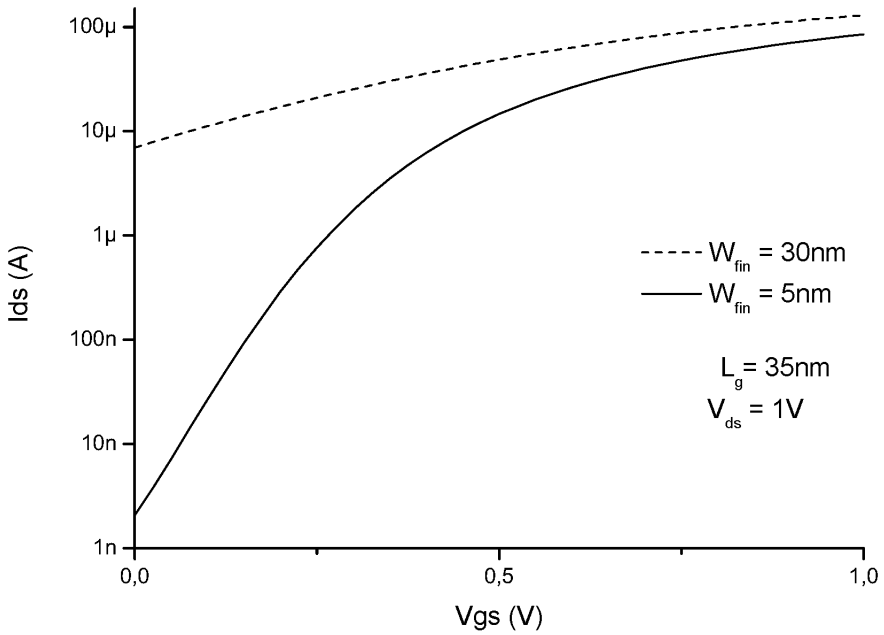


Figure 3.5: Measured I_{ds}-V_{gs} characteristic for different fin widths with L_g = 0.035μm and V_{ds} = 1V of the Salsa2 module E01N and module E07N

unique for a certain doping profile for a given source/drain doping at a certain V_{gs}, in case of a double gate device. The measured SS versus gate length at a W_{fin} of 10nm, a V_{gs} of 0.2V, and a V_{ds} of 25mV is depicted in figure 3.6.

3.3 Work function

The threshold voltage for long channel devices with a fin width of 10 nm is determined by the work function difference, the doping of the fin and a term due to the fact that the concentration of charge carriers needs to be larger in order to reach threshold ($\frac{kT}{q} \ln \frac{2C_{ox}kT}{q^2 n_i t_{si}}$).

The work function difference is determined by the work function of the gate material and that of electron affinity of silicon (χ_{si}). The electron affinity of semiconductors are known, the work function difference can be deduced by measurements. From the electron affinity in combination with doping (and parasitic charge) the gate work function can be determined.

A possible and perhaps novel method for measuring the gate work function is based on the work of J.-L. van der Steen et al. [21]. The current density J of the electrons collected by the sample (a long channel device i.e. m=1) depends on the metal work function W of the sample and is given by the RichardsonDushman equation

$$J = J_0^2 e^{\frac{-\Delta\phi_f}{kT}} e^{\frac{V_{gs}}{\mu_t}}, \tag{3.4}$$

with k the Boltzmann constant, T the temperature in Kelvin and $\Delta\phi_f$ the work

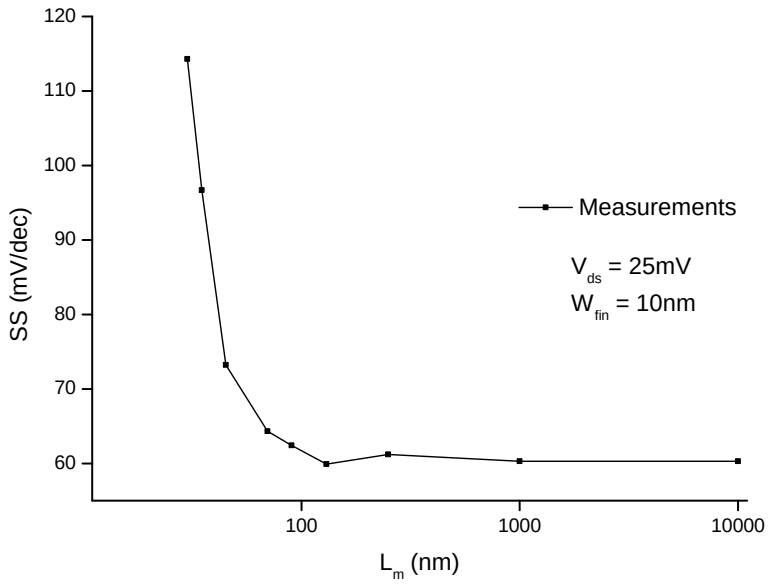


Figure 3.6: Measured subthreshold slope versus gate length with $W_{fin} = 10$nm, and a $V_{ds} = 25$mV of the Salsa2 module E20N

function difference.

The current density (J_0) depends more or less quadratically on the temperature, however since the work function difference (and the gate voltage) is in the exponent, J depends exponentially on the temperature. Hence, from the temperature dependence the work function difference can be extracted. Rearranging the equation yields:

$$\ln(J) = \ln(J_0^2) - \frac{\Delta\phi_f}{kT} + \frac{V_{gs}}{\mu_t}. \tag{3.5}$$

Plotting $\ln(I_{ds})$ vs. $\frac{1}{T}$ for a certain V_{gs} results in a graph with a slope of $\frac{\Delta\phi_f}{k}$. From this graph the work function difference can be deduced. Multiplying the slope by the Boltzmann constant results in the work function difference at a certain V_{gs}.

For flatband conditions the work function difference is the difference between the gate work function and the conduction band, as depicted in the band diagram of figure 3.7.

$$\Delta\phi_f = \phi_m - \chi_{si}. \tag{3.6}$$

When a gate bias is applied the potential is influenced. The potential falls over the silicon and the oxide.

$$V_{gs} = V_{si} + V_{ox} \tag{3.7}$$

$$V_{gs} = \psi_s + \Delta\phi_f + \frac{Q_{tot}}{C_{ox}} \tag{3.8}$$

$$\tag{3.9}$$

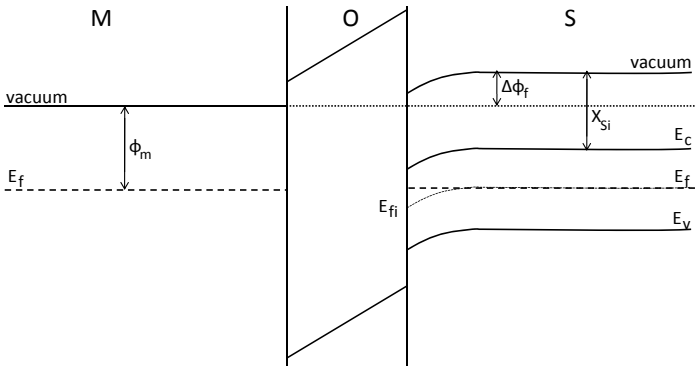


Figure 3.7: Band diagram at V_{gs}=0V with a work function difference

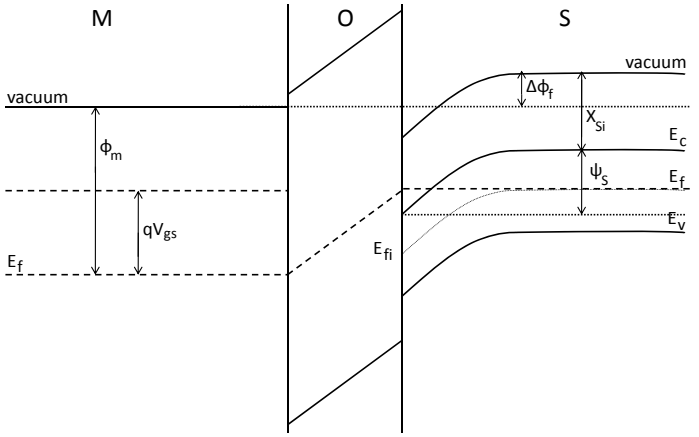


Figure 3.8: Band diagram at a positive V_{gs}

For FinFETs in subthreshold the total charge (Q_{tot}) is negligible. So for an applied gate-source voltage the work function difference is the difference between the gate source voltage minus the surface potential (ψ_s), as depicted in the band diagram of figure 3.8.

$$\Delta\phi_f = V_{gs} - \psi_s. \tag{3.10}$$

From the measurements the work function difference is determined, then the gate work function can be calculated:

$$\phi_m = \Delta\phi_f + \chi_{si}. \tag{3.11}$$

Note that all parameters are defined in eV or V respectively.

This method is applied to the FinFETs used in this thesis. The drain current versus 1/T relation for the measured long channel devices (L_g = 10 μm) at a V_{gs} of 0.14V is depicted in figure 3.9. The temperature of the devices is swept using a chuck heater. The current of the devices is measured at 25 °C, 50 °C and 125°C.

The calculated work function of the gate material is around 4.52 eV. The work function of the different devices measured varies within few tenths of an eV, proba-

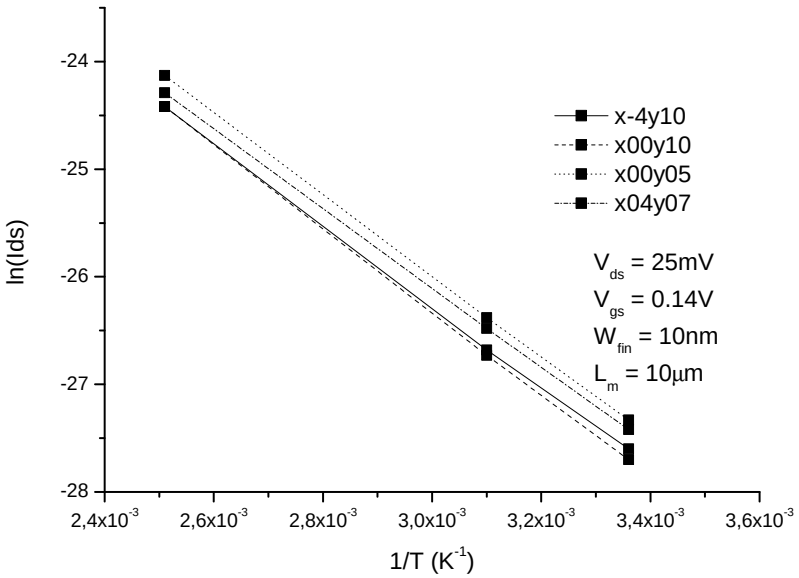


Figure 3.9: Measured drain current versus 1/T at a gate length of 10μm, W_{fin} = 10nm and V_{ds} = 25mV of the Salsa2 module E20N

bly caused by process variations and measurement uncertainty. Taking into account the fact that the concentration of inversion carriers needs to be larger in order to reach threshold results in an absolute gate work function for long channel devices of 4.56 eV.

The SS of a FinFET theoretically changes with temperature according to the thermal voltage variation over temperature for long channel devices (see figure (2.10))

$$SS = \frac{kT}{q} \ln(10) \text{ V/dec.} \tag{3.12}$$

The SS behavior as a function of temperature can be extracted from the measurements, by plotting $(\frac{\mathrm{d}I_{ds}}{\mathrm{d}V_{gs}})^{-1} \ln(10)$. Plotting the theoretical and measured subthreshold voltage variation over temperature in one figure results in figure 3.10.

In the figure can be seen that the theoretical and measured SS versus temperature behavior are in good agreement. Only the measured SS increases slightly faster then theoretically predicted.

3.4 Effective gate length

Accurate determination of the effective channel length (L_{eff}) becomes more important, because the L_{eff} is critical for the performance of the device. The difference between effective channel length and the physical gate length (L_g) is defined by a parameter ΔL. The ΔL could be caused by side-diffusion of source/drain dopants into the fin region, non-ideal patterning of the gate structure and modulation of the doping of the source/drain regions under or near the gate, as addressed in paragraph

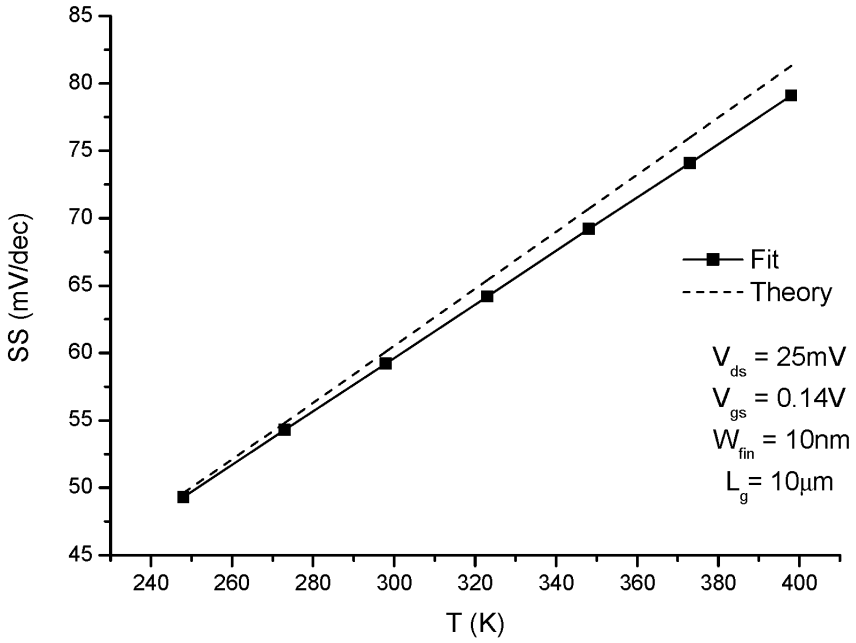


Figure 3.10: Measured subthreshold slope versus T at a gate length of 10μm, W_{fin} = 10nm and V_{ds} = 25mV of the Salsa2 module E20N

(2.3).

The variation in channel length (ΔL) can be estimated from the measurements. Because the drain current is inversely proportional to the gate length

$$I_{ds} \propto \frac{K}{L_{eff}}, \tag{3.13}$$

with K= $q\ D_n n_i t_{si} e^{\frac{V_{gs}-\Delta\phi_f}{m\mu_t}} (1\text{-}e^{\frac{-V_{ds}}{\mu_t}})$. The ΔL can be calculated when the drain current of two long channel devices are measured and assuming that the K factors are equal:

$$I_{ds1}(L_1 - \Delta L) = I_{ds2}(L_2 - \Delta L) \tag{3.14}$$

$$\Delta L = \frac{\frac{I_{ds1}}{I_{ds2}} L_1 - L_2}{-1 + \frac{I_{ds1}}{I_{ds2}}} \tag{3.15}$$

The best result is obtained as only long channel devices are used. When short channel devices are used the ΔL is overestimated due to short channel effects, hence the potential barrier is lowered. Determining the ΔL for devices with gate lengths 10 μm and 1 μm result in a ΔL of 21nm.

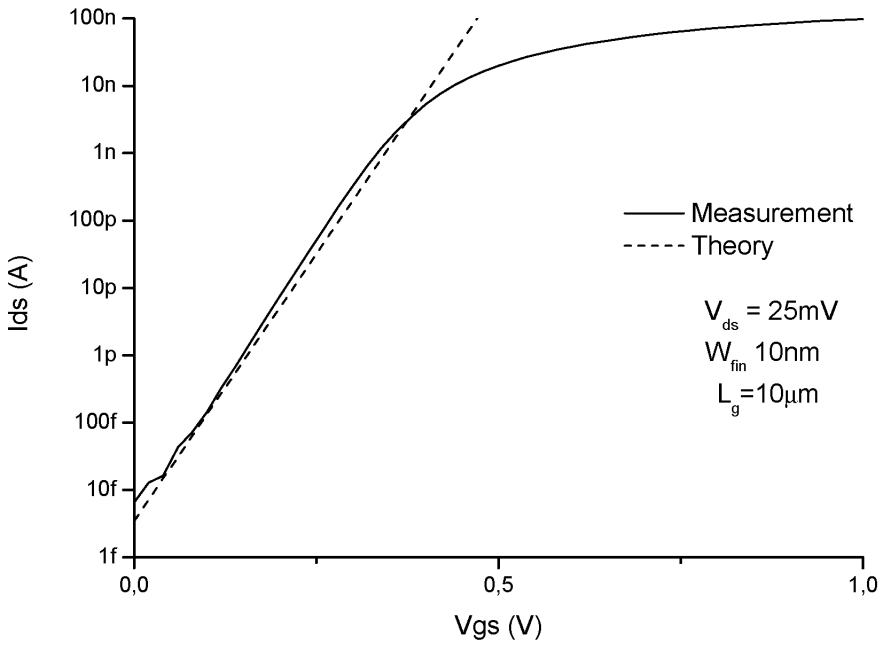


Figure 3.11: Comparison between measurement and theory of the drain current versus gate voltage behavior with W_{fin} = 10nm, L_g = 10μm, and V_{ds} = 25mV of the Salsa2 module E20N

3.5 Comparison between measurements and theory

In chapter 2 a theoretical model was discussed that describes the I_{ds}-V_{gs} characteristic including short channel effects, equations (2.8). The theoretical I_{ds}-V_{gs} characteristic is affected by the ideality factor, as described in equation (2.14) and by the threshold voltage, as described by equation (2.27). The theoretical model is compared with measurements for different gate length devices for low and high drain-source voltage.

Figure 3.11 depicts the current-voltage characteristic for a long channel (10μm) at low V_{ds} (25mV) and fin width of 10nm. The theoretical SS (59.66mV/dec) and measured SS (59.6mV/dec) are in good agreement.

The theoretical model also holds at a high drain-source voltage. The I_{ds}-V_{gs} curve for a 10μm channel device, with a fin width of 10nm at a V_{ds} of 1V is depicted in figure 3.12. The SS at high V_{ds} is correct, however the subthreshold current of the model is slightly too low. This difference is possibly caused by a different fin width. The fin width in the model is possibly smaller then the fin width of the measured device, the current in subthreshold increases accordingly, as discussed in paragraph 2.5.

For short channel devices the SS depends on the capacitances between the channel region and the source/drain junction. The capacitances between the channel region and the source/drain junction depend on the charge between the source/drain and channel divided by the voltage difference between the source/drain potential

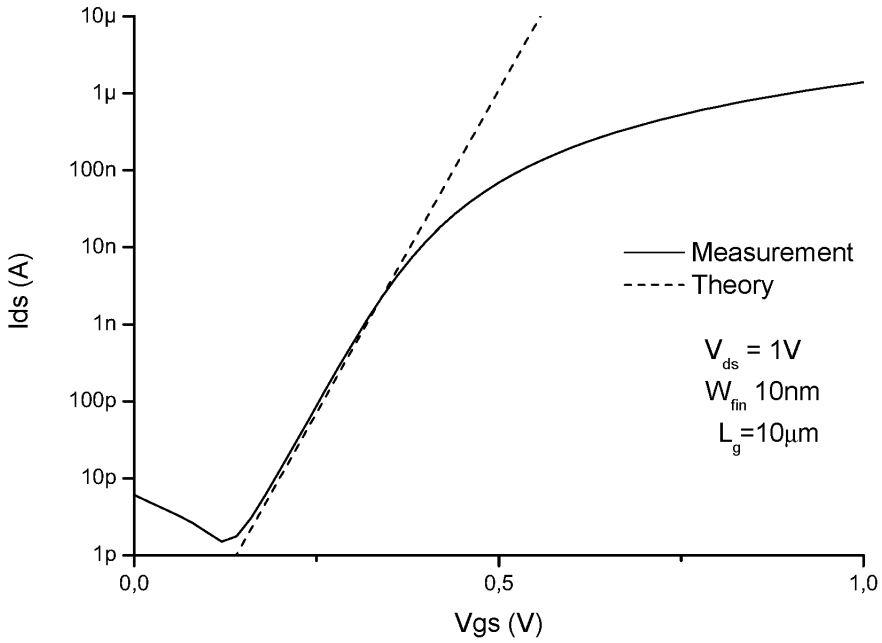


Figure 3.12: Comparison between measurement and theory of the drain current versus gate voltage behavior with $W_{fin} = 10$nm, $L_g = 10\mu$m, and a $V_{ds} = 1$V of the Salsa2 module E20N

and the minimum surface potential. The minimum surface potential depends on the effective channel length and hence the applied bias conditions, as described in paragraph (2.2). The current-voltage characteristic for a device with a gate length of 30nm at a V_{ds} of 25mV and fin width of 10nm is depicted in figure 3.13. The subthreshold current is accurate, however the SS is slightly underestimated.

The I_{ds}-V_{gs} plot of a short channel (L_g=30nm) device at high V_{ds} (1V) and fin width of 10nm is depicted in figure 3.14.

For a short channel device at high V_{ds} the minimum surface potential is no longer at half the effective channel length, but shifts towards the source. In paragraph 2.2 an equation was derived that described the position of the minimum surface potential (equation 2.24). This equation is only valid when $L \gg l$ and is not that accurate for the shortest channels (L_g=30nm and L_g=35nm) as can be seen in the figure. Also it can be seen that the threshold voltage differs a lot from the measured graph. The threshold voltage as described in paragraph 2.4 does not cover short channel effects. The enhanced threshold voltage reduction in very short channel devices can be derived from the quasi two dimensional model of the channel potential, as described in [14] for bulk devices.

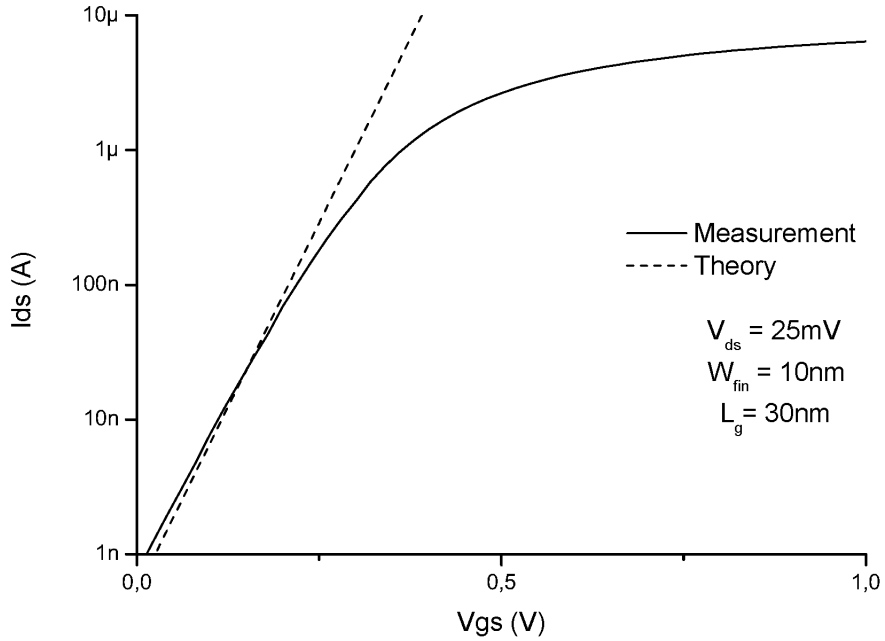


Figure 3.13: Comparison between measurement and theory of the drain current versus gate voltage behavior with $W_{fin} = 10$nm, $L_g = 30$nm, and a $V_{ds} = 25$mV of the Salsa2 module E20N

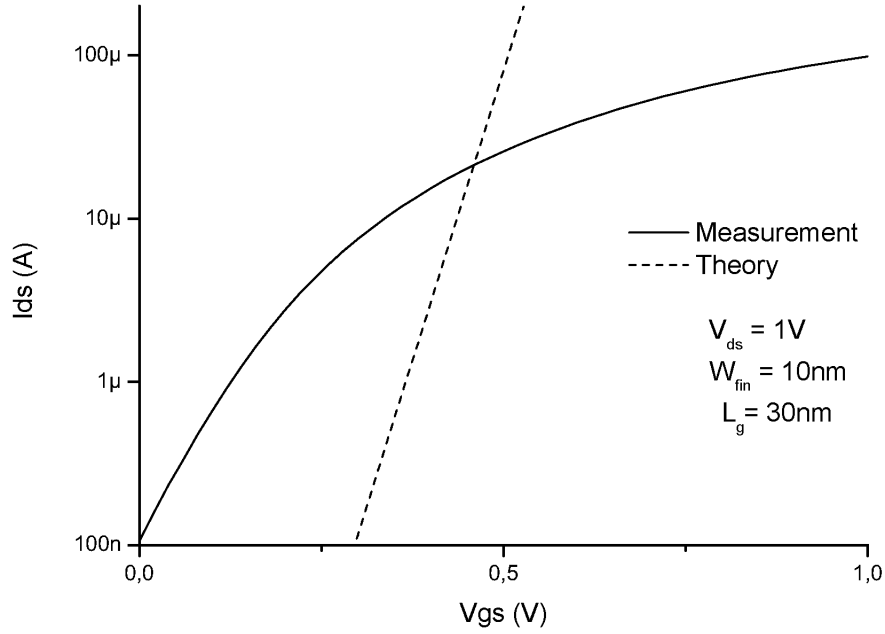


Figure 3.14: Comparison between measurement and theory of the drain current versus gate voltage behavior with $W_{fin} = 10$nm, $L_g = 0.03\mu$m, and $V_{ds} = 1$V of the Salsa2 module E20N

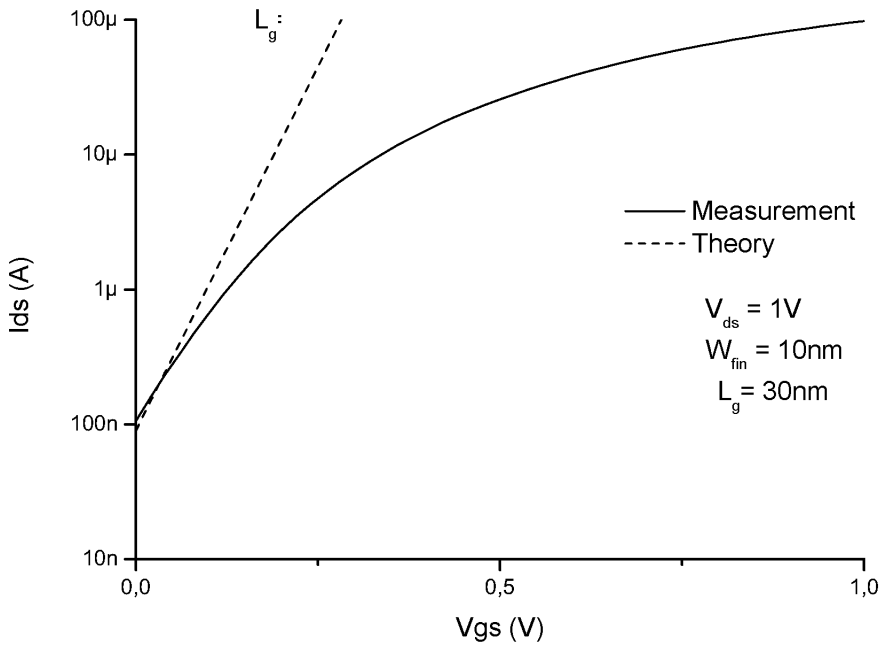


Figure 3.15: Comparison between measurement and theory (eq. 3.16) of the drain current versus gate voltage behavior for a short channel $L_g = 0.03\mu$m, at $V_{ds} = 1$V and $W_{fin} = 10$nm of the Salsa2 module E20N, including the accelerated threshold voltage reduction in very short channel devices

$$\Delta V_{th} = \frac{2(V_{bi}-2\phi_b)+[V_{ds}+(V_{bi}-2\phi_b)](1-e^{\frac{-L_{eff}}{l}})}{4\sinh^2\frac{L_{eff}}{2l}} + \frac{2\sqrt{(V_{bi}-2\phi_b)^2+(V_{bi}-2\phi_b)[V_{ds}+(V_{bi}-2\phi_b)](e^{\frac{L_{eff}}{l}}-1)}}{4\sinh^2\frac{L_{eff}}{2l}}, \tag{3.16}$$

with ΔV_{th} the accelerated threshold voltage reduction in very short channel devices, V_{bi} the built-in potential between the channel and source/drain junction, $2\phi_b$ the built-in potential of the depletion layer under a MOS gate, V_{ds} the drain-source voltage, L_{eff} the effective channel length and l the characteristic length.

The theoretical current-voltage relation, including the accelerated threshold voltage reduction in very short channel devices ($W_{fin} = 10$nm, $L_g = 0.03\mu$m, and $V_{ds} = 25$mV) is depicted in figure 3.15.

When the accelerated threshold voltage reduction in very short channel devices is taken into account, the theoretical threshold voltage describes the measured behavior well. The SS for very short channel devices at high drain-source voltage is underestimated. However, the theoretical model does describe ideal devices, effects such as variation in fin width, recombination and quantum confinement are not taken into account.

3.6 Discussion

In this chapter the electrical behavior as determined by different device parameters were investigated, initial values for device parameters were deduced from measurements such as the work function of the gate material and the variation in channel length. Finally the measured current-voltage behavior was compared with a theoretical model.

The electrical behavior scales with the device parameters and applied bias voltages, such as fin width, gate length and V_{ds} as predicted by theory.

The work function of the gate material as determined by the measurements is around 4.56 eV. The work function of the different devices measured varies within few tenths eV, probably caused by process variations and measurement uncertainty.

The ΔL is determined for long channel devices. When short channel devices are used, the ΔL is overestimated due to short channel effects and reduction in potential barrier. Determining the ΔL for devices with gate lengths 10 μm and 1 μm results in a ΔL of 21 nm.

The theoretical model of the subthreshold current-voltage behavior of FinFETs, described in this report, is accurate. For very short channel devices the model underestimates the short channel effects slightly, probably caused by variation in fin width. For very short channel accelerated threshold voltage reduction has to be taken into account. The model is also accurate at high drain-source voltages.

Now that we have estimated several device parameters through measurements, and obtained some initial values for device parameters. The device parameters can hopefully be deduced through inverse modeling more accurately. This is done by adjusting device parameters in simulations under various bias conditions, as described in the next chapter.

Chapter 4

Simulations

Device Simulations can give physical insight for explaining the effects observed through measurements. In this thesis we would like to know the doping profile in and near the channel region dependence of the subthreshold current of FinFETs. Through inverse modeling process parameters are linked to electrical characteristics. This is done by adjusting device parameters in simulations under different bias conditions. First a long channel device is fitted in order to extract the gate work function (see also chapter 3). Then short channel devices are simulated in order to determine other device parameters. By looking at the threshold voltage, DIBL and SS, a model of the device will be obtained that is hopefully close to the real device. An important note is that non-idealities such as interface states, fixed charge, stress effects and quantum-confinement were not taken into account.

4.1 The simulation environment

The simulations are performed using a set of Synopsys tools, namely the Sentaurus Structure Editor and Sentaurus Device. Analogue to [11], in this work we did not use a process simulator. Sentaurus Device calculates the electrical behavior of the created structure. Once the structure is created and the simulation is performed, a comparison with measurements is performed.

Calculating the electrical behavior of the structure may take a long time, especially for 3D structures, for obtaining an accurate calibration. In order to reduce the simulation time only half of the device is simulated, which is possible because the FinFET is (in principle) a symmetrical device. Of course, in order to compare the simulation results with the measurements, the current should be multiplied by 2. The simulation time can be further optimized by minimizing the number of vertices at a required level of accuracy. To achieve accurate simulation results, the mesh should be denser in those regions of the device where the current density, electric field (depletion regions or interfaces) and charge generation are high. So the mesh close to the Si-SiO_2 interface and the source-fin and drain-fin regions should be denser than in other parts of the mesh, as shown in figure 4.1. For the used structure editor files see paragraphs C.1, C.3

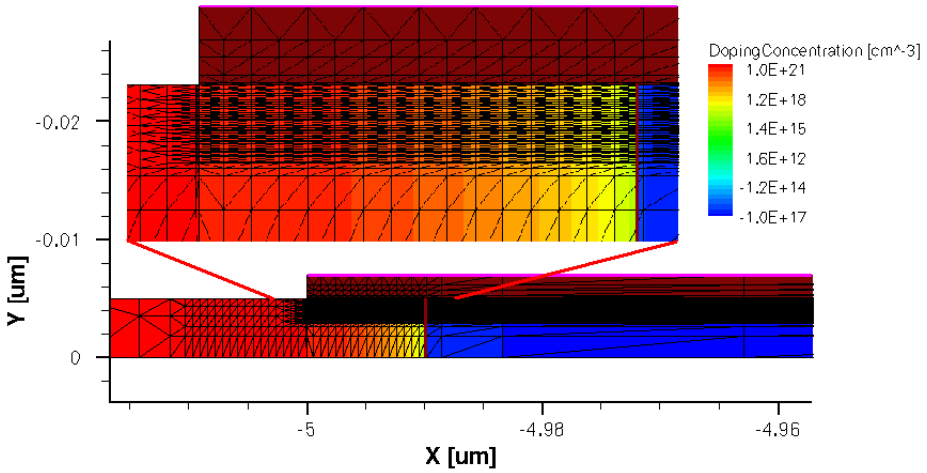


Figure 4.1: 2D representation of the placement of the mesh

The structure editor and device simulator offer many tunable device and physical variables. The main device variables that influence the current behavior are: doping profile in and near the channel regions, oxide thickness (t_{ox}), dielectric constant of the oxide (ε_{ox}), electrical gate length and gate work function (ϕ_m). Moreover other device parameters have to be set in order to built the structure, such as the doping of the fin and source/drain junctions and the dimensions of the device: fin width (W_{fin}), fin height (H_{fin}), gate length (L_g) and length of the source/drain junctions (L_{sd}). The device simulator offers more variables, such as those used by physical models i.e. the mobility models (for the used Sentaurus Device files see paragraphs C.2, C.4). The most important variables of the device simulator are discussed in the next paragraph.

In order to calculate the electrical behavior under various bias conditions, contacts have to be placed at the gate, source and drain. The gate is assumed to be ideal (gate depletion is not taken into account), i.e. a metal gate is placed on top of the gate oxide. The source and drain contacts are placed at the end of the source drain junctions. A schematic 2D representation of the placement of the contacts and some device parameters is shown in figure 4.2.

Physical parameters

For device simulations the physical models used influence the electrical behavior strongly i.e for narrow devices ($W_{\text{fin}} < 15$nm) quantum confinement has to be taken into account, for the current in super threshold the mobility models are very important. The devices used in this thesis have device widths of 10nm or 20nm, but quantum confinement is not taken into account. In the device simulators there are various mobility models to choose from. The total mobility is a combination of different scattering mechanisms. For each mechanism or effect there are different models originating from different research groups. When the important mobility effects have been chosen, the user must choose the different models (a particular

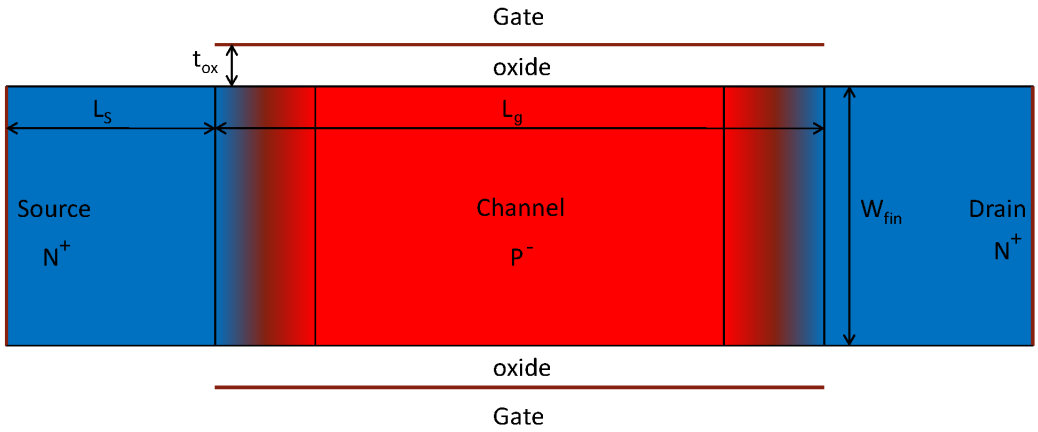


Figure 4.2: Schematic 2D representation of the placement of the contacts

effect can only be described by one of the sub models). This paragraph describes the mobility models that have significant influence on the simulations.

Mobility models

The total mobility is the result of a combination of different mobility effects. The different mobility contributions are combined following Mathiessen's rule i.e. the lowest mobility has the largest influence on the overall mobility:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + .. + \frac{1}{\mu_n} \tag{4.1}$$

Mobility degradation at interfaces

In the channel region of a MOSFET, the high transverse electric field forces carriers to interact strongly with the semiconductor insulator interface. Carriers are subjected to scattering by acoustic surface phonons and surface roughness. The mobility degradation at interfaces will predominantly affect the current at high gate bias. The Lombardi and/or Lucent mobility model describe these effects.

High-field saturation

In high lateral electric fields, the carrier drift velocity is no longer proportional to the electric field. Instead, the velocity saturates to a finite speed. The high field saturation model will uniquely affect the current for high drain bias. This is described by the Canali model. The Canali model comprises three sub-models: the actual mobility model, the velocity saturation model, and the driving force model.

Philips unified mobility model

The Philips unified mobility model, proposed by Klaassen [22], unifies the description of majority and minority carrier bulk mobilities. In addition to describing the temperature dependence of the mobility, the model takes into account electron - hole scattering, screening of ionized impurities by charge carriers, and clustering of

impurities. Hence this model describes the Coulomb scattering in low transversal fields of MOSFETs.

In the Philips unified mobility model, there are two contributions to carrier mobilities. The first, $\mu_{i,L}$, represents phonon (lattice) scattering and the second, $\mu_{i,DAeh}$, accounts for all other bulk scattering mechanisms (due to free carriers, and ionized donors and acceptors). These partial mobilities are combined to give the bulk mobility $\mu_{i,b}$ for each carrier according to Mathiessen's rule:

$$\frac{1}{\mu_{i,b}} = \frac{1}{\mu_{i,L}} + \frac{1}{\mu_{i,DAeh}} \tag{4.2}$$

Device parameters specified by the factory

Some of the device parameters are specified by the factory. These parameters are discussed in this paragraph.

The equivalent dielectric layer thickness for the high-k material HfSiO as given by IMEC is 2nm; the relative permittivity of SiO_2 is 3.9. An equivalent SiO_2 layer thickness can be calculated when the layer thickness and permittivity of the high-k material is known [23].

$$t_{ox} = \frac{\kappa_{ox} t_{highk}}{\kappa_{highk}}, \tag{4.3}$$

with t_{ox} the SiO_2 oxide thickness, κ_{ox} the permittivity of SiO_2, t_{highk} the high-k thickness and κ_{highk} the permittivity of the high-k material.

The fin dimensions are measured by IMEC. The fin width is 10nm or 20nm, the fin height 60nm and the physical gate length 10μm, 1μm, 250nm, 130nm, 90nm, 70nm, 45nm, 35nm or 30nm.

The doping of the fin and source/drain junctions are determined from the conditions of the implantations as specified by the manufacturer. For the fin a doping of 10^{15} At/cm^2 at an angle of 45° is shot into the fin. At a fin width of 10 nm this results in a doping concentration of 10^{17} At/cm^3.

Before the source/drain junctions are doped, the resistance of the source/drain junctions are reduced by applying selective epitaxial growth (SEG) to the source/drain. The contact resistance is further reduced by applying a high source/drain doping. The junctions are doped with $3{\cdot}10^{15}$ At/cm^2 at an angle of 45°. This results in a peak doping concentration of 10^{21} At/cm^3 in the source/drain region [24].

4.2 Inverse modeling strategy

The effective channel length and work function of the gate material are not known in advance and have do be determined through inverse modeling. Initially a work function as deduced from the measurements is used.

The effective channel length of the device is influenced by the variation in gate length depends also on the gaussian doping profile in the lateral direction. Initially the measured metal gate length minus the indiffusion of the source/drain junctions as deduced from measurements, see chapter 3, is used as effective channel length. In this work it is assumed that the physical gate length equals the designed gate length. Some additional assumptions are that the oxide thickness is uniform in the fin and that the fin has a perfect rectangular shape. Of course in realistic devices this won't be the case. However, if in this work a more realistic device would have been chosen, (1) a process simulator was required and (2) meshing was difficult to control. In other words, many complications would have been introduced with probably a low amount of success.

Because of the non-planar structure of FinFETs, 3D simulations are required to describe the full electric behavior of the device. However, 3D simulations are rather time consuming. Therefore, initially 2D simulations are performed to give insight into the values of the different lateral device parameters. Subsequently 3D simulations are performed to obtain the doping profile in the vertical direction. The results obtained in this chapter are found by manipulating the device parameters manually until a best fit is achieved.

Simulation outline

The best approach seems to be to first perform a simulation with initial parameters as deduced from measurements and as specified by the manufacturer. Then device parameters are adjusted subsequently to obtain a fit between the measurements and simulations under various bias conditions.

The first physical parameter to determine is the work function of the gate material. The work function of the gate can be determined from the subthreshold current-voltage characteristic of long channel devices, since the dielectric layer thickness is not important here. For long channel devices the threshold voltage is determined by the work function difference (equation 2.26). Because the depletion charge in the long channel FinFET is not important (see chapter 2), the simulated subthreshold current-voltage characteristic can be fitted to the experimental data by adjusting only the gate work function.

When the gate work function is known the SS can be adjusted. For shorter channel devices the capacitances between the channel region and the source/drain junction become significant and will affect the SS strongly according to equation 2.14. Because the dielectric layer thickness was specified by IMEC and is assumed to be constant, the SS can be modified by adjusting the doping profile in and near the channel region.

By using device simulations the doping profile in and near the channel region can be extracted by fitting the measured graph for short channel devices. Because the SS and the threshold voltage are influenced by the doping profile in and near the channel region, the agreement between the measured and simulated current-voltage characteristic is a good indication whether a doping profile in and near the channel region is realistic.

Moreover, the SS versus gate length plot is unique for a certain doping profile in and near the channel region at a given source/drain and fin doping for a 2D device, as will be shown later on in this thesis. By plotting the measured and simulated SS versus gate length at a certain V_{gs}, the curves can be fitted by adjusting the doping profile in and near the channel region.

The next step is the fine-tuning of the doping profile in and near the channel region according to the gate-drain/source overlaps to obtain a good DIBL. This can be verified by fitting the simulated and the measured subthreshold current-voltage characteristic at high V_{ds}. At high V_{ds} DIBL becomes significant, especially for short devices.

When the doping profile in lateral direction is determined, the doping profile in the height of the fin can be worked out, for this 3D simulations are required. By plotting the measured and simulated SS versus gate lengths at a certain V_{gs} for different doping profiles in the height direction and by plotting the measured and simulated current-voltage characteristic for short channel devices, a doping profile in the height direction can be obtained, which is hopefully close to reality .

With the previous steps, the simulated subthreshold current are fitted to the measurements in the subthreshold regime. In the final step the mobility parameters, source/drain dimension and doping can be adjusted to get the right on-current.

A schematic representation of the different steps for extracting device parameters through inverse modeling is depicted in figure 4.3.

4.3 2D Simulation results

A 2D simulation of a double gate device gives a reasonable description of the electrical behavior of a FinFET, especially for a fin with a high aspect ratio from which hardly any effect from the top and bottom (substrate) gate is expected. Therefore, initially 2D simulations were performed to give insight into the values of the different device parameters.

Note that when a device is simulated in 2D, Synopsys Device assumes by default that the third dimension has a height of 1μm, so the simulated current is given in A/μm. In order to compare the simulation results with measurements the height of the fin has to be taken into account, by multiplying the simulated current with the height (in μm) of the fin.

Step 1: Obtaining the gate work function

The first physical parameter to look at is the work function of the gate material.

$\mathbf{I_{ds}}$-$\mathbf{V_{gs}}$

The work function of the gate can be determined from the current-voltage characteristics for long channel devices. A correct gate work function in the simulations

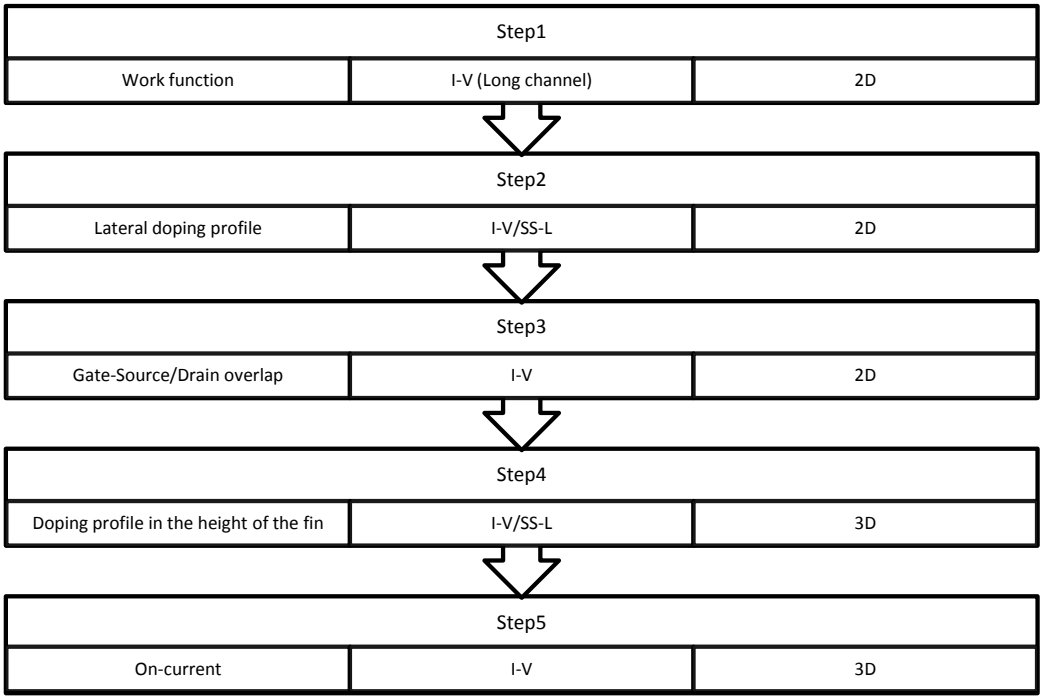


Figure 4.3: Flow diagram of extracting device parameters by inverse modeling

yields a good match with the subthreshold current measurements. The work function difference causes the current-voltage characteristics to shift along the V_{gs} axis. Because the subthreshold current for long channel devices depends on the work function difference, e.g when the work function difference increases, the I_{ds}-V_{gs} graph shifts to the right (see also equation (2.8)). This behavior is confirmed by simulations.

Current voltage characteristics for various gate work functions, at a gate length of 10μm, a V_{ds} of 25mV and a fin width of 10nm, is depicted in figure 4.4. The measured I_{ds}-V_{gs} characteristic is depicted in the figure as well.

For a gate work function of 4.55eV, the simulated and measured curves match. This value is close to the gate work function as determined by measurements, see section 3.3. Above threshold the measured and simulated current-voltage characteristics diverge. This is mainly due to the absence of the top gate (and bottom, but is expected to be less important) in 2D simulations, which will be discussed in section 4.5.

Step 2: Lateral doping profile extraction

When the gate work function is known, the SS can be extracted. The SS is influenced by the indiffusion of the source/drain junctions into the fin, the oxide capacitance and the depletion capacitance, see equation 2.14. Because the dielectric layer thickness, and consequently the oxide capacitance, is specified by IMEC and is assumed

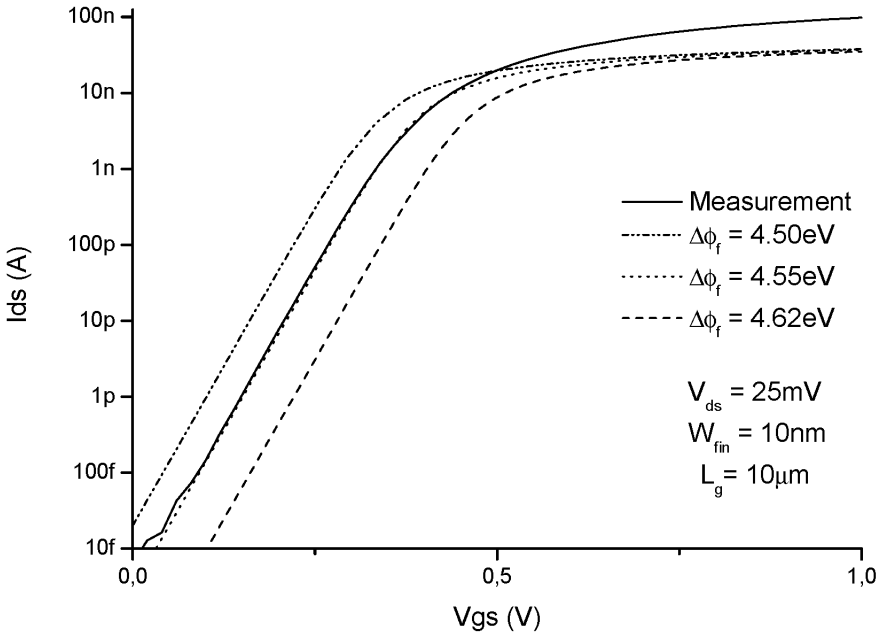


Figure 4.4: Measured and simulated current-voltage characteristic for various gate work functions with W_{fin} = 10nm, L_g = 10μm, and V_{ds} = 25mV of the Salsa2 module E20N

to vary little, the SS can be modified by tuning the doping profile in and near the channel region at a given source/drain and fin doping.

SS-L

By plotting the measured and simulated SS versus gate length at a certain V_{gs} the curves can be fitted by adjusting the standard deviation of the doping profile. The gate-source/drain overlap can be fitted later on by looking at I_{ds}-V_{gs} behavior at high V_{ds}. From figure 4.5 can be observed that the SS depends more on the doping profile in and near the channel region for short channel devices than for long channel devices, as expected, see paragraph 2.2. If the standard deviation of the doping profile increases, the doping of the source/drain will diffuse further into the channel. The effective channel length reduces and short channel effects are more prominent. As a result the SS increases.

The standard deviation of the lateral gaussian doping profile can be extracted by fitting the measured and simulated SS versus gate length. The SS versus gate length, for a V_{ds} of 25mV, a V_{gs} of 0.2V and a fin width of 10nm, is plotted for various doping profiles, as depicted in figure 4.5. For a standard deviation of 0.01μm of the lateral gaussian doping profile the simulated and measured SS versus gate length curves agree well. However for very short channel devices the SS is less accurate then for long channel devices, because the indiffusion of the doping profile is a significant part of the effective channel length.

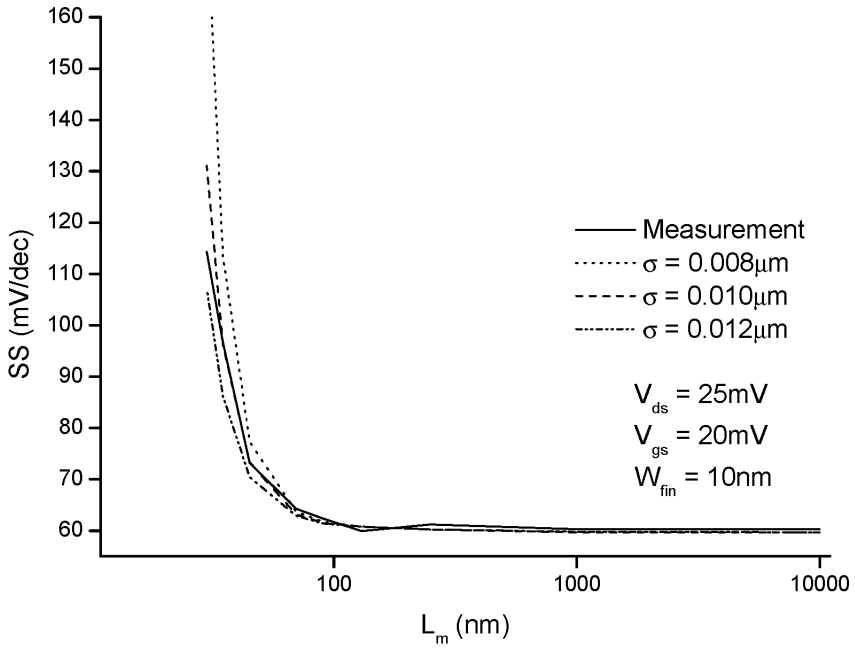


Figure 4.5: Measured and simulated subthreshold slope versus gate length for different standard deviations of the doping profile with $W_{fin} = 10$nm and $V_{ds} = 25$mV of the Salsa2 module E20N

$\mathbf{I_{ds}}$-$\mathbf{V_{gs}}$

The doping profile can also be extracted by fitting the simulated subthreshold current-voltage characteristic to measured curve for short channel devices. Because the SS and the threshold voltage are influenced by the doping profile, fitting the simulated current-voltage characteristics provides a good estimate of the doping profile.

The current-voltage characteristics for various standard deviations of the doping profile of a 2D device with a gate length of 45nm, a V_{ds} of 25mV and a fin width of 10nm, is depicted in figure 4.6.

The figure shows that the SS changes when the standard deviation of the doping profile changes, due to the variation in effective channel length. The diffusion of the source/drain into the channel also influences the doping of the channel. A larger standard deviation yields more lateral diffusion of the doping. The (p-type) doping in the channel reduces and consequently subthreshold current increases, as shown the figure.

The simulated and measured I_{ds}-V_{gs} behavior around the threshold voltage differs significant. This difference is caused by corner effects, as addressed in paragraph 4.5.

When the gate length of the device is decreased below a gate length of 45nm, the current-voltage behavior of the device starts to deviate from the measured curve. The current-voltage characteristic, for a gaussian lateral doping profile with various

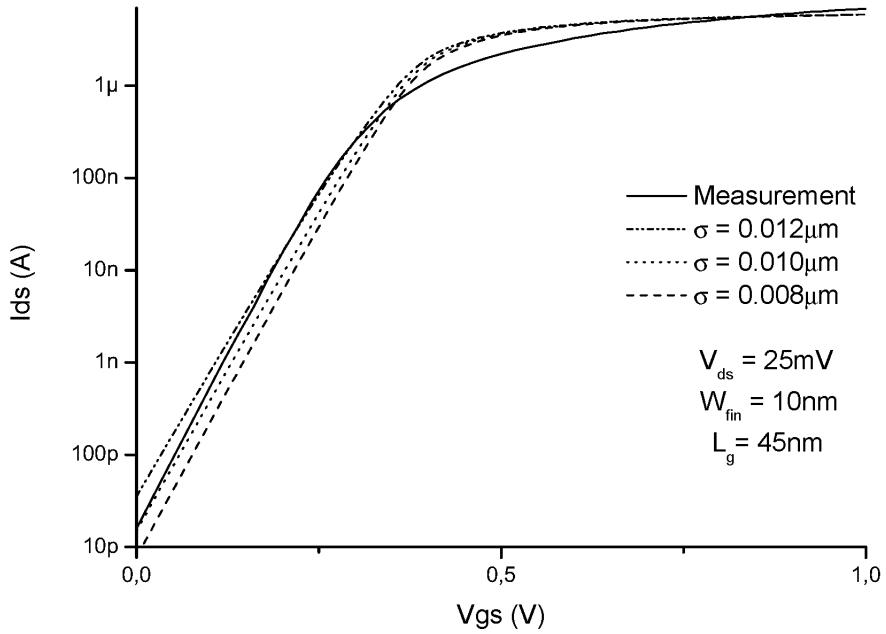


Figure 4.6: Measured and simulated current-voltage characteristic for various standard deviations of the doping profile with W_{fin} = 10nm, L_g= 0.045μm, and V_{ds} = 25mV of the Salsa2 module E20N

standard deviations for a device with a gate length of 30nm, a fin width of 10nm and a V_{ds} of 25mV is depicted in figure 4.7.

For small gate lengths the simulated and measured I_{ds}-V_{gs} characteristics cannot be fitted by a lateral gaussian doping profile only. This is probably due to the fact that the doping profile of a device is not solely determined by a lateral doping profile. The doping profile might vary in depth across the fin height or fin width and has to be taken into account. This requires 3D simulations.

Step 3: Extracting the gate-source/drain overlap

When devices become shorter, short channel effects, such as DIBL [12], become important. DIBL is a secondary effect referring to a reduction of threshold voltage at higher drain voltages. Due to the higher drain voltage, the depletion region between the drain and body increases in size and extends under the gate. The potential energy barrier for electrons in the channel is lowered, and hence the drain current increases. Due to DIBL the current-voltage characteristics at high drain-source voltage depend even more on the doping profile, especially on the gate-source/drain overlaps.

$\mathbf{I_{ds}}$-$\mathbf{V_{gs}}$

The doping profile determined at a low drain-source voltage can be optimized by fitting the simulation I_{ds}-V_{gs} data at high drain-source voltage.

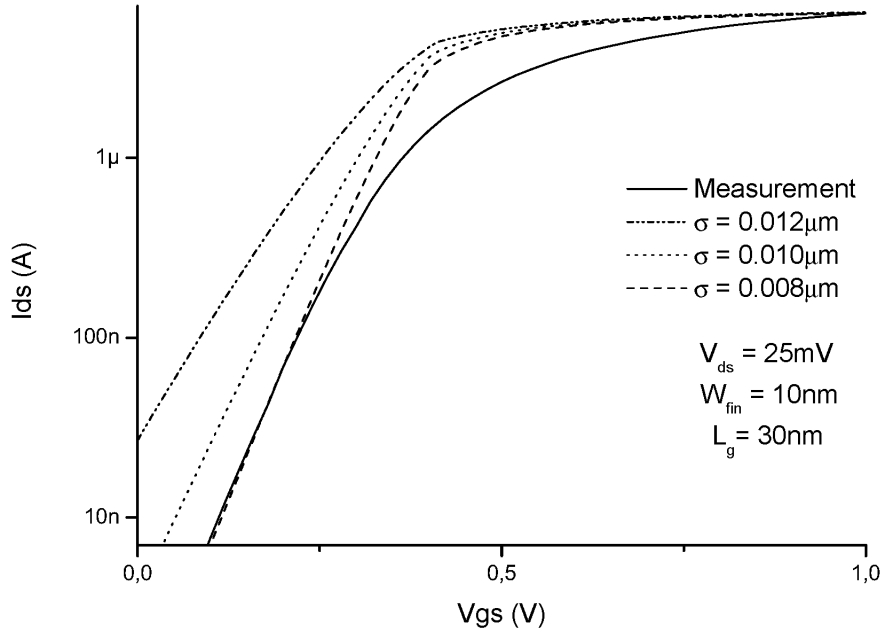


Figure 4.7: Measured and simulated current-voltage characteristic for various standard deviations of the doping profile with W_{fin} = 10nm, L_g= 0.03μm, and V_{ds} = 25mV of the Salsa2 module E20N

The current-voltage characteristics for various standard deviations of the doping profile of a 2D device with a gate length of 45nm, a V_{ds} of 1V and a fin width of 10nm, is depicted in figure 4.8.

For a standard deviation of 10nm, the simulated and measured current-voltage curves are in good agreement at high drain-source voltage in subthreshold. For low gate-source voltages the measured current increases due to GIDL, as discussed in paragraph 2.5.

Discussion

A gate work function of 4.55eV is determined by fitting the measured and simulated I_{ds}-V_{gs} characteristics for long channel devices.

The standard deviation of the lateral doping profile was extracted by fitting the measured and simulated SS versus gate length and by fitting the I_{ds}-V_{gs} characteristic in subthreshold for low and high drain-source voltage for various gate lengths. The SS versus gate length plot is not that accurate for very short channel devices, since the SS is determined at a single V_{gs} instead of throughout the whole subthreshold region. For very short channel devices the electric behavior can't be fitted with a lateral doping profile only. A doping profile in the height of the fin has to be taken into account, which requires 3D simulations.

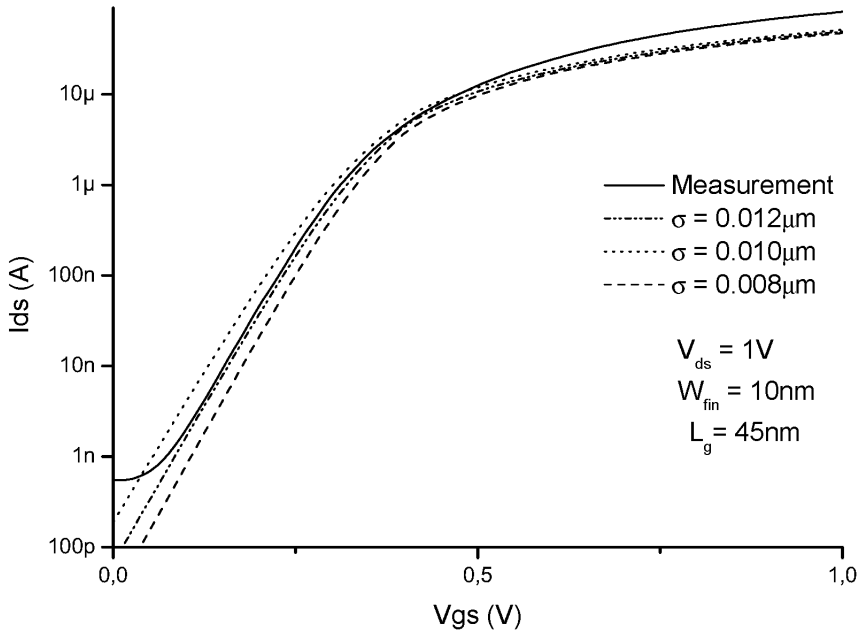


Figure 4.8: Measured and simulated current-voltage characteristics for various standard deviations of the doping profile with $W_{fin} = 10$nm, $L_g = 0.045\mu$m, and $V_{ds} = 1$V of the Salsa2 module E20N

4.4 3D Simulation results

Performing 2D simulations gave insight into the values of the device parameters. However, in 2D simulations certain 3D effects are not taken into account such as the influence of the top gate, corner effects, current spreading and the doping profile in the height of the fin. These effects can only be taken into account by 3D simulations. The inverse modeling routine is continued from step 4 i.e. according to figure 4.3.

As for 2D simulations the simulation time is reduced by simulating only half of the device. Of course, in order to compare the simulation results with the measurements, the current should be multiplied by 2.

The gate is again assumed to be ideal (gate depletion is not taken into account). The gate contact is placed on top of the gate oxide. The source and drain contacts are placed at the end of the source/drain junctions. For the doping profile in the height of the fin a step function is used, which is a rough simplification of a gaussian profile. The placement of the contacts and the step function of the doping profile in the height of the fin is depicted in figure 4.9.

Step 4: Extraction of the doping profile in the height of the fin

Until now the doping profile in the vertical/height direction of the fin was kept constant. However in reality the doping in the vertical/height direction of the fin isn't constant, but may depend on the diffusion of the doping into the fin. The doping is shot into the top of the fin at an angle of 45 degrees. The position of the maximum

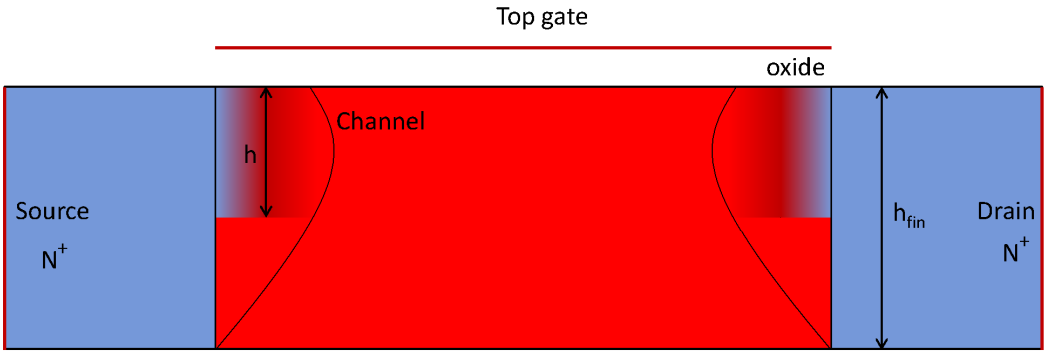


Figure 4.9: Doping profile in the height of the fin

of the doping depends on the implantation energy. From this position the doping diffuses three dimensionally into the fin.

When a variation in doping in the height direction is present, the diffusion of the source/drain doping into the channel varies and accordingly the channel length varies. The variation in channel length due to the doping profile in the height of the fin has an effect on the current-voltage characteristic. The variation in channel length influences the SS and the threshold voltage. The channel length positioned near the top gate determines the SS mostly: the threshold voltage is lowest because this region is drawn into inversion first, while deeper into the fin the channel length may vary. Accordingly the SS varies and the threshold voltage is higher, because the applied gate bias needs to be higher in order to reach inversion there. Due to the different threshold voltages and the dependence of the SS on the effective channel length, it could be that the derivative of the subthreshold slope doesn't have a constant slope for doping variation in the depth direction. The ΔL due to channel length variation in the height of the fin is expected to be prominent for short channel devices.

The derivative of the SS for a device with a gate length of 35nm and 10μm, a fin width of 10nm and a V_{ds} of 25mV is plotted in figure 4.10.

In the figure can be observed that up to 0.25V the derivative of the SS is quite constant, but above 0.25V the derivative diminishes. This could indicate that there is a certain doping profile variation in the height of the fin. However the fact that the derivative is not zero could also be due to the measurement accuracy.

For the doping profile in the height of the fin a step function is used. From the top gate to the position of the step function the standard deviation of the lateral gaussian doping profile is set to the value as determined for the lateral direction, while below the step function the channel length is equal to the physical gate length, this is depicted in figure 4.9. The SS versus gate length and I_{ds}-V_{gs} curves at low and high V_{ds} are used to determine the doping profile in the height of the fin.

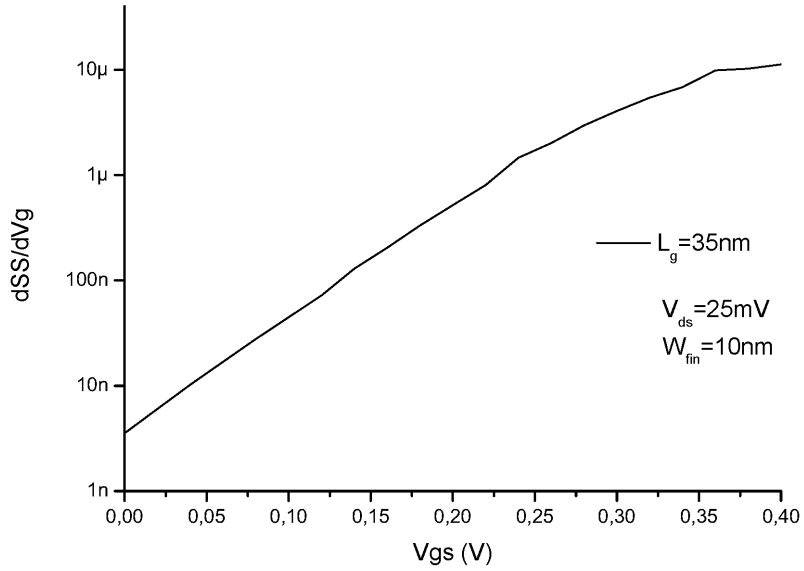


Figure 4.10: Derivative of the measured SS for a device with a gate length of 35nm and 10μm, W_{fin} = 10nm and V_{ds} = 25mV of the Salsa2 module E20N

SS-L

The SS is influenced by the indiffusion of the source/drain junctions into the fin and the doping profile in the height of the fin. By plotting the measured and simulated SS versus gate length at a certain V_{gs}, the curves can be fitted by adjusting the position of the step of the doping profile in the height of the fin.

The SS versus gate length plot for various positions of the step in the doping profile for a fin width of 10nm, a V_{ds} of 25mV, a V_{gs} of 0.2V and a V_{gs} of 20mV is depicted in figure 4.11.

The SS for short channel devices depends strongly on the doping profile in the height of the fin, as expected. When the step function shifts towards the top gate the effective channel length of the device decreases, and the SS decreases accordingly. However all the curves follow the shape of the simulated SS versus gate length more or less, but none of the curves fits exactly, perhaps due to the fact that the doping profile in the height of the fin should be a gaussian function instead of a step function, or because the SS versus gate length plot is determined at a single V_{gs} instead of throughout the whole subthreshold region.

$\mathbf{I_{ds}}$-$\mathbf{V_{gs}}$

Because the channel length throughout the fin varies, the SS and the threshold voltage change. By plotting the measured and simulated I_{ds}-V_{gs}, the dependence of the doping profile in the height of the fin on the SS and the threshold voltage can be observed. By fitting the simulated I_{ds}-V_{gs} curve a doping profile in the vertical direction can be extracted, which is hopefully unique.

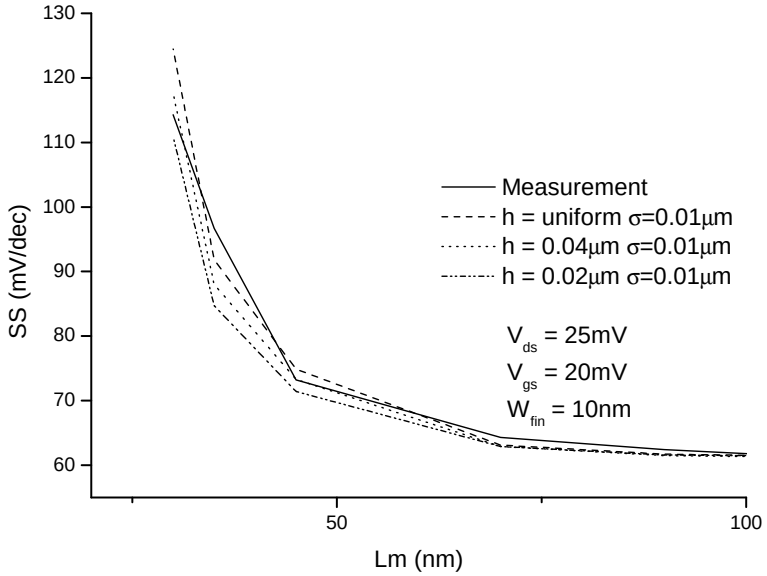


Figure 4.11: Measured and simulated subthreshold slope versus gate length for various positions of the step in the doping profile with W_{fin} = 10nm and V_{ds} = 25mV of the Salsa2 module E20N

The current-voltage curve for various vertical positions of the step in the doping profile for a gate length of 30nm, fin width of 10nm and a V_{ds} of 25mV is depicted in figure 4.12.

The effective channel length increases when a step in doping profile in the height of the fin is applied, accordingly the SS increases, as depicted in figure 4.12. The threshold voltage is also influenced by the change in effective channel length. When the step function is located at 0.04 μm from the top-gate, the measured and simulated subthreshold I_{ds}-V_{gs} curves almost agree. However the current in super threshold is reduced due to the decrease of effective channel width, because in the simulations the inversion charge is mostly situated at the top 0.04 μm of the device instead of throughout the whole fin. However, in super threshold other issues may be important, such as source/drain resistances and current spreading. These issues were not studied for this work.

High drain-source voltage

The I_{ds}-V_{gs} behavior at high V_{ds} is more sensitive to gate-source/drain overlap. The doping profile can be optimized by fitting simulated and measured I_{ds}-V_{gs} characteristics at high V_{ds}.

The current-voltage curve for various vertical positions of the step in the doping profile for a gate length of 0.03μm, a fin width of 10nm and a V_{ds} of 1V is depicted in figure 4.13.

When the step function is located at 0.04 μm from the top-gate, the measured

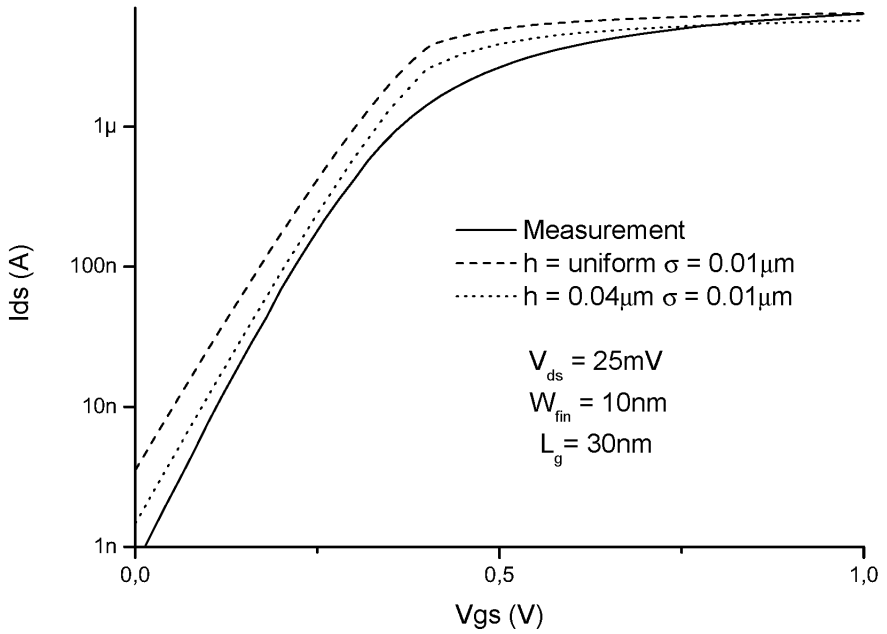


Figure 4.12: Measured and simulated drain current against the gate voltage for various vertical positions of the step in the doping profile with $L_g = 30$nm $W_{fin} = 10$nm and $V_{ds} = 25$mV of the Salsa2 module E20N

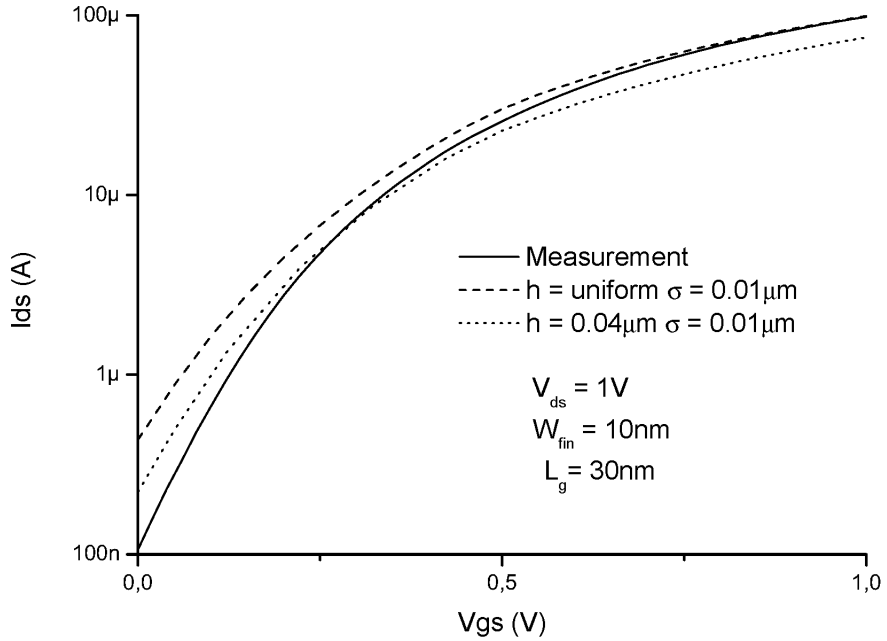


Figure 4.13: Measured and simulated drain current against the gate voltage for various vertical positions of the step in the doping profile with $W_{fin} = 10$nm, $L_g = 0.03\mu$m, and $V_{ds} = 1$V of the Salsa2 module E20N

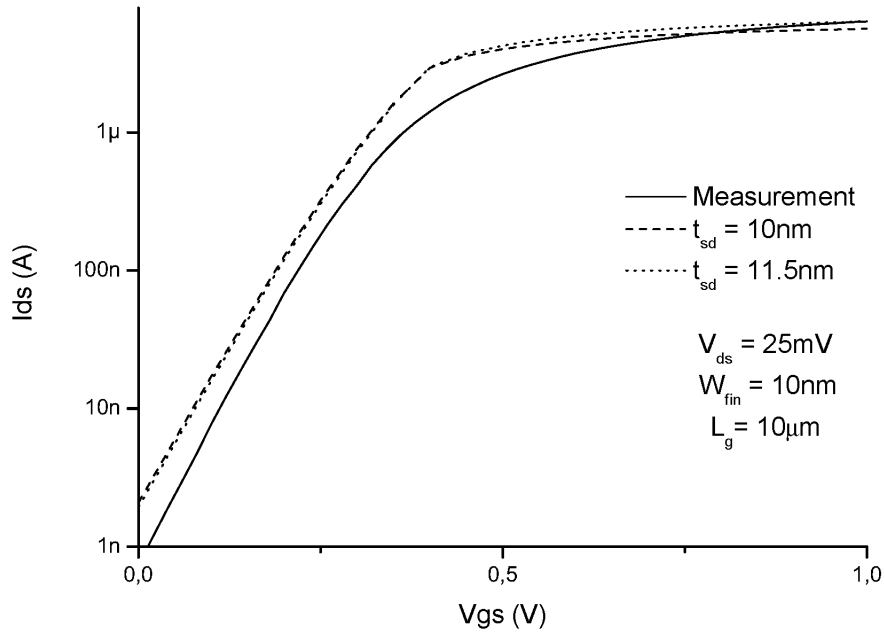


Figure 4.14: Comparison of the measured and simulated drain current versus gate voltage for different source/drain junction widths with W_{fin} = 10nm, L_g = 30nm, h=40nm, σ=10nm and V_{ds} = 25mV of the Salsa2 module E20N

and simulated I_{ds}-V_{gs} characteristic at high drain-source voltage of 3D structure do almost agree in subthreshold, however the current in super threshold again differs. Hence, the doping profile as applied in the simulations is not completely similar to the real doping profile in the devices, but seems to be accurate for short channel devices. For very short channel devices ($L_g \leq$ 35nm) the simulations appear to improve, when a doping profile in the vertical direction of the fin is taken into account. In order to get a better estimate of the doping profile, more information about the sensitivity of the doping profile on the electrical behavior is needed. A possible alternative is discussed in the recommendations (chapter Recommendations).

Step 5: Adjusting the super threshold current

With the previous steps the current of the simulation and measurement are fitted in the subthreshold regime. In the final step the source/drain dimensions, the doping and the position of the contacts can be adjusted to get the right on-current.

The doping of the source/drain junctions was determined earlier (see [24]). The resistivity of the source/drain junctions is reduced by selective epitaxial growth, thus increasing the width of the source/drain junctions.

The influence of the wider source/drain regions, due to selective epitaxial growth, on the I_{ds}-V_{gs} characteristic of a long channel device (L_g = 30nm, W_{fin} = 10nm, h=40nm, σ=10nm and V_{ds} = 25mV) is depicted in figure 4.14.

The current increases proportional to the width of the source/drain junctions, as

expected. For a source/drain layer width of 11.5nm, the simulated current in super threshold corresponds with the measurement at a V_{gs} of 1V. The current around the threshold voltage still differs may be due to corner effects.

4.5 Supplementary simulation results

As mentioned before the simulated I_{ds}-V_{gs} characteristics around the threshold voltage deviate from its measured counterpart, which could be due to corner effects. It was also noticed that for 2D simulations the current in super threshold is lower than for 3D simulations. The impact of these effects on the current-voltage behavior is discussed in this section.

In the previous section the doping profile in the lateral direction and in the height of the fin was obtained through inverse modeling. The uniqueness of the obtained doping profiles is verified in this section.

Corner effect

The simulated current-voltage characteristics for short channel devices at low drain-source voltage around the threshold voltage do not match, while they fit nicely in the subthreshold and on-region, as discussed in paragraph 4.4 (figures 4.6, 4.7 and 4.12). This deviation may be caused by corner effects as will be discussed in this section.

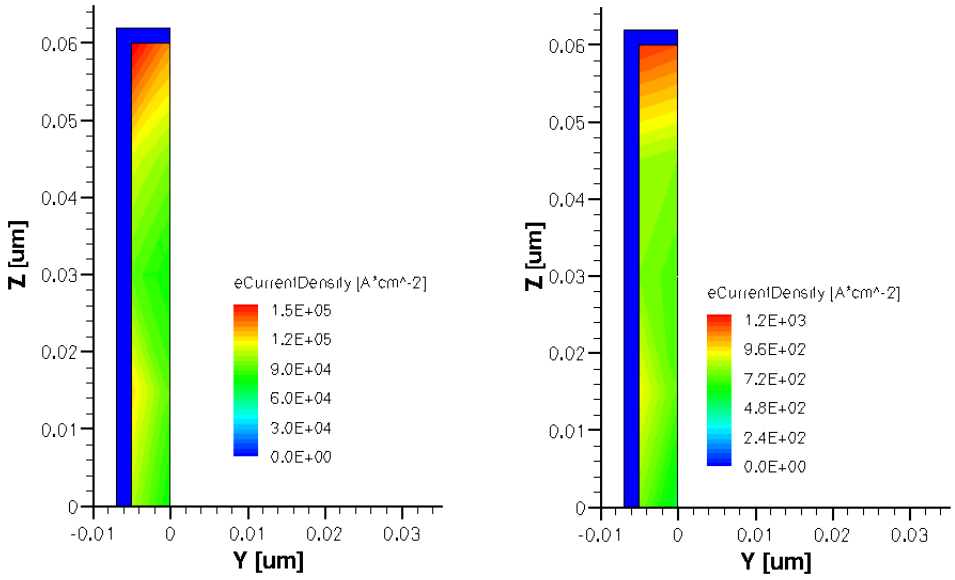
In the corners of the fin premature inversion can take place because of charge sharing effects of the two adjacent gates [25]. At these regions the electric field is much higher, so a higher current density is obtained, which influences the current-voltage characteristic of the device around the threshold voltage.

The electron current density in the middle of a device with a gate length of 90nm at an applied gate bias of 0.4V, a fin width of 10nm and drain source voltage of 25mV is depicted in figure 4.15a.

The plot shows the corner effect. At the corner where two gate electrodes merge, the electron current density is roughly two times higher than at a point where only one gate governs the electric behavior. The current, at V_{gs} around the threshold voltage ($V_{th} \approx 40$mV), for a short channel device at low drain-source voltage is significantly affected by corner effects.

The current, at V_{gs} around the threshold voltage, for a short channel device at high drain-source voltage is not significantly affected by corner effects. The increase of the electron current density is in the same order of magnitude for both high and low drain-source voltage. Therefore, the increase of the total current around the threshold voltage at high V_{ds} due to corner effects is not significant.

For long channel devices the electron current density in the corners also increases due to two adjacent gates as depicted in figure 4.15b. However the increase in total current is negligible. The current, at V_{gs} around the threshold voltage, for a long



(a) (b)

Figure 4.15: Simulated electron current density in the fin for a device with a gate length of 90 nm (a) and 10μm (b) respectively, W_{fin} = 10nm, V_{ds} = 25mV, V_{gs} = 40mV and $V_{th} \approx$ 40mV

channel device at high drain-source voltage is not significantly affected by corner effects either.

Comparison 2D vs 3D

The results obtained from the 2D and 3D simulation showed similar subthreshold behaviors, while in the near or super threshold the graphs differ. In figure 4.16 the 2D and 3D current-voltage characteristics are depicted and compared for a 10μm device. In subthreshold the current voltage characteristic is determined by the area of the device, which is equal for the 2D and 3D simulation (for the 2D simulations the current densities were multiplied with H_{fin}), while in super threshold the perimeter of the gate (or actually gate width) is important. For the 3D simulation an inversion layer is created underneath all gates, whereas for a 2D simulation the top gate (and bottom gate) is not taken into account. Accordingly, the perimeter of gate in the 2D case is underestimated. This effect can be taken into account by adding the current caused by the top gate inversion layer to the 2D result, which results in a quasi 3D representation. The quasi-3D representation is plotted in figure 4.16. The quasi-3D representation is an accurate description of the current in super threshold. Consequently using a 2D simulation and simply compensating for the height of the fin isn't an accurate description of a real 3D device, the top gate has to be taken into account.

When the SS versus gate length characteristic of 2D and 3D (including uniform doping profiles in vertical direction) are compared for a 10nm wide fin at a V_{ds} of 25mV, a V_{gs} of 0.2V, it is observed that the curves differ for very short channel devices, as depicted in figure 4.17.

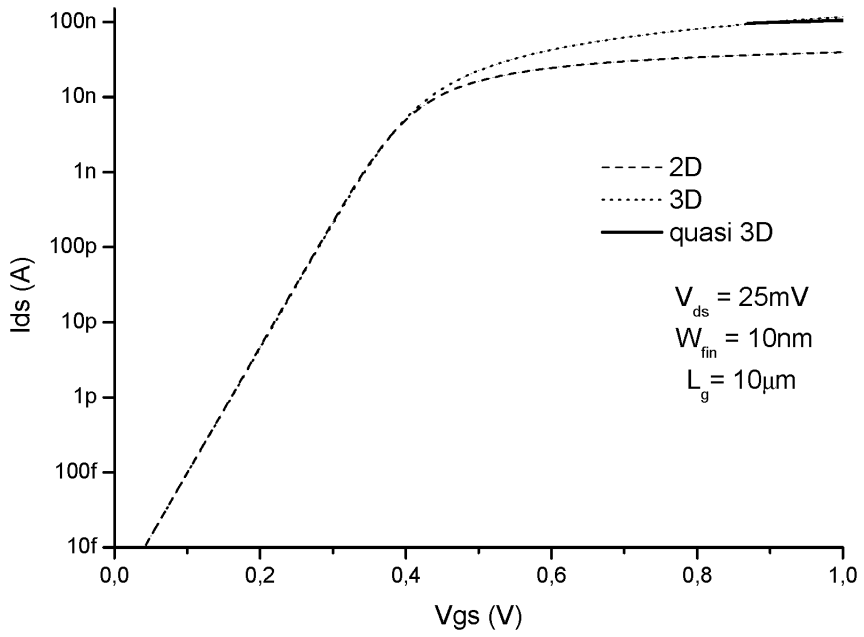


Figure 4.16: Comparison of the simulated drain current versus gate voltage behavior for 2D, 3D and quasi 3D with W_{fin} = 10nm, L_g = 10μm, and V_{ds} = 25mV of the Salsa2 module E20N

This difference in SS is caused by the variation in standard deviation, as depicted in figure 4.18. The standard deviation is set to 0.01 μm for 2D as well as for 3D, but the mesh is not exactly the same. Therefore the doping profiles differ slightly, but for very short channel devices the difference is significant. For 3D the doping profile diffuses slightly further into the fin, resulting in a shorter channel and a weaker SS.

Uniqueness of the doping profile

In the previous chapter the lateral doping profile was determined first, subsequently a doping profile in the height of the fin was worked out. However, it is possible to obtain a fit for slightly other doping profiles in the lateral direction and in the height of the fin. Simulations are performed with a number of doping profiles and various positions of the step in the doping profile in the height of the fin. The simulated and measured current-voltage behavior of very short channel devices, L_g=0.03μm with a fin width of 10nm, are plotted for low as well as high drain-source voltages (figure 4.19 and figure 4.20 respectively). The SS versus gate length for the various doping profiles is plotted in figure 4.21.

The SS versus gate length for the various doping profiles does not differ much. On the other hand, the I_{ds}-V_{gs} curves at low and high V_{ds} indicate that slight variations in applied doping profiles do influence the electrical behavior of the simulated device. However none of the doping profiles does describe the electrical behavior very accurately, which makes it hard to determine which doping profiles estimates the real doping profile best. In order to determine the doping profiles accurately,

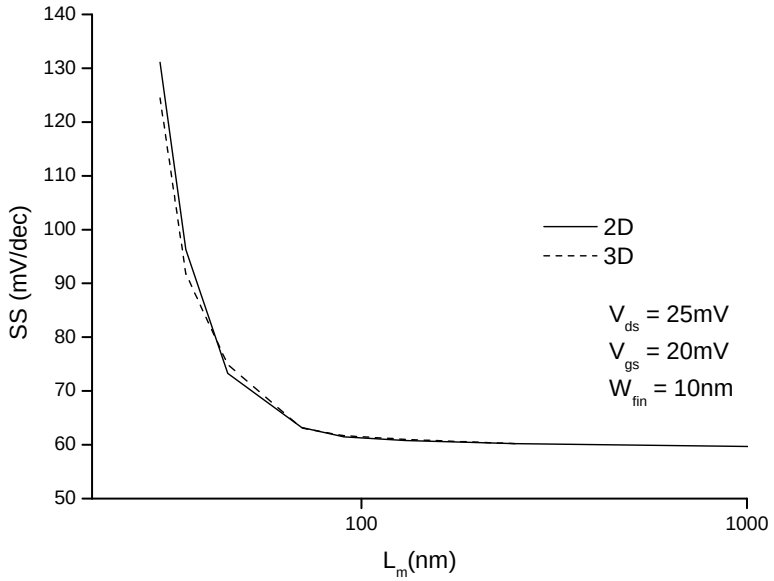


Figure 4.17: Simulated SS vs gate length for 2D and 3D with W_{fin} = 10nm and V_{ds} = 25mV of the Salsa2 module E20N

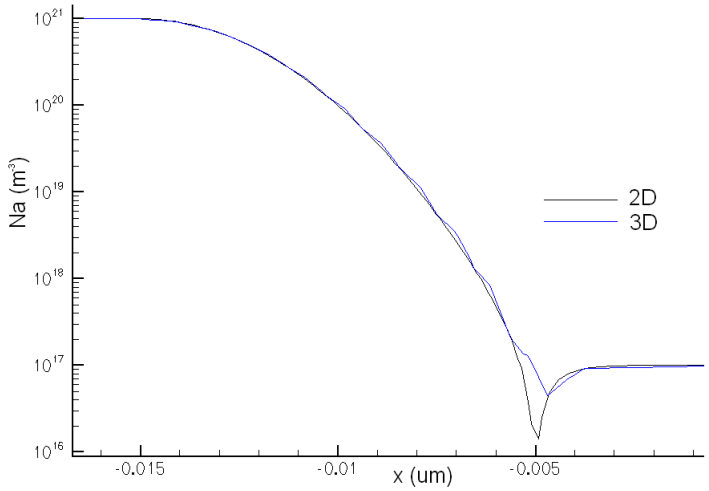


Figure 4.18: Simulated doping profile for 2D and 3D

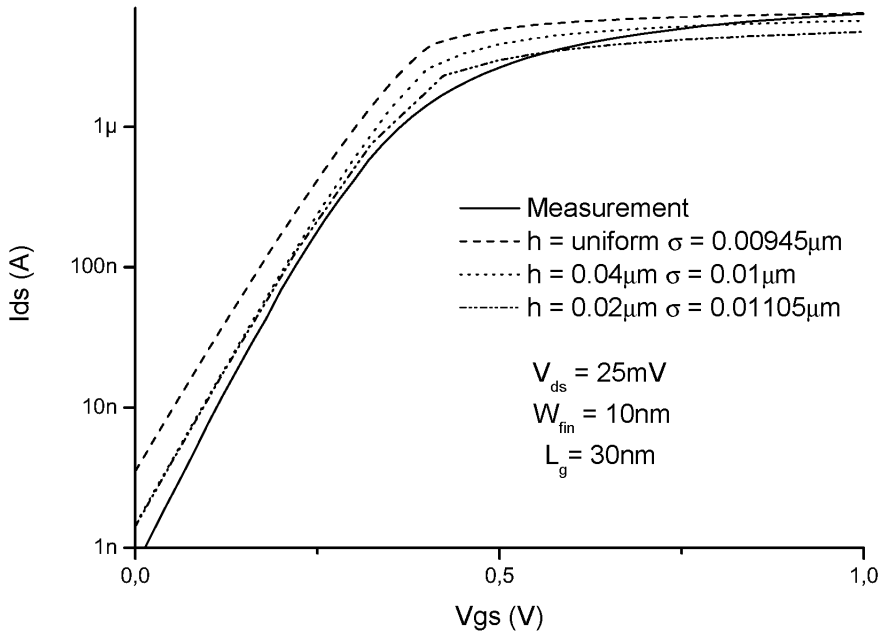


Figure 4.19: Measured and simulated drain currents against the gate voltage for various vertical positions of the step in the doping profile and slopes of the lateral doping profiles. $W_{fin} = 10$nm, $L_g = 0.03\mu$m, and $V_{ds} = 25$mV (Salsa2 module E20N)

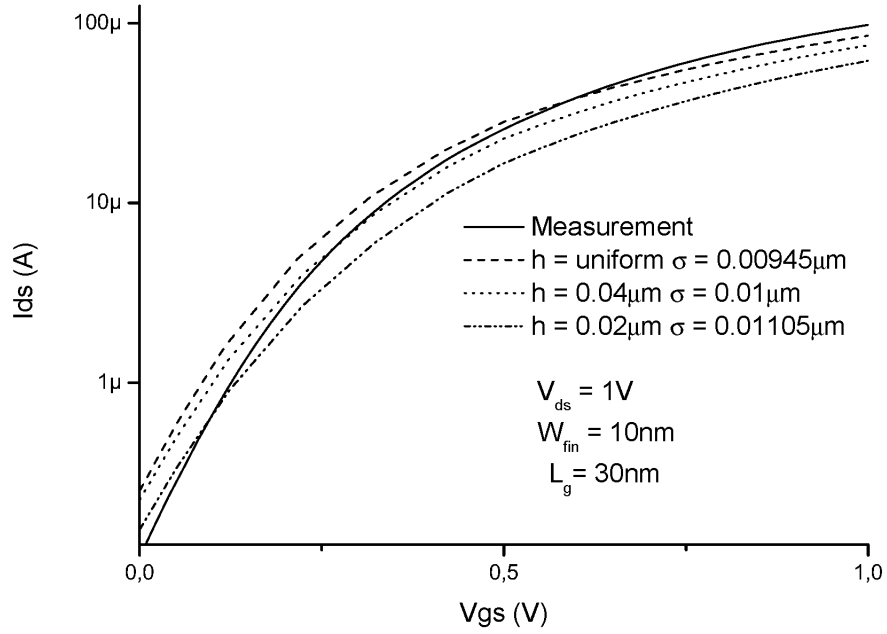


Figure 4.20: Measured and simulated drain currents against the gate voltage for various vertical positions of the step in the doping profile and slopes of the lateral doping profiles. $W_{fin} = 10$nm, $L_g = 0.03\mu$m, and $V_{ds} = 1$V (Salsa2 module E20N)

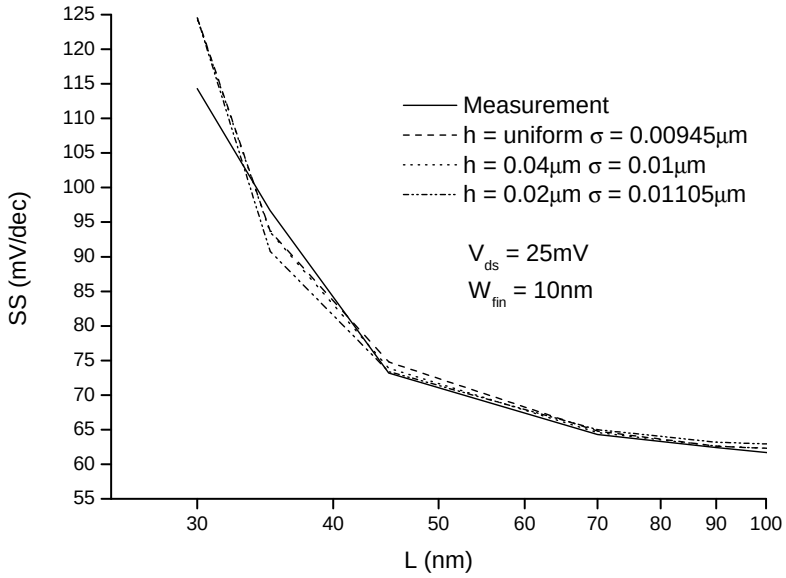


Figure 4.21: Measured and simulated SS vs gate length for various positions of the step in the doping profile and lateral doping profiles with W_{fin} = 10nm and V_{ds} = 25mV of the Salsa2 module E20N

especially in the height of the fin, more information is needed. A possible method to determine the doping profile more accurately is by using the BOX contact of the device, as will be discussed in chapter Recommendations.

It is possible that the found doping profiles obtained with the simulation approach used in the thesis is actually far from the reality. Some device parameters were determined on the basis of specification given by IMEC, i.e. equivalent dielectric layer thickness, fin dimensions and the doping of the device. However the derived device parameters could differ from reality and due to a compensating effect of some device parameters the simulated electrical characteristics nevertheless fits nicely with its measured counterpart. For example the same DIBL can be obtained with high source/drain doping (1E21) and short overlap (σ = 10nm) or with low doping (1E19) and long overlap (σ = 66nm). Some values of the device parameters, such as the doping levels, can be verified by looking at the electrical behavior as a function of the applied voltage to the BOX contact.

4.6 Discussion

In this chapter process parameters were deduced through inverse modeling. First the work function of the gate material was determined by examining the current-voltage characteristics for long channel devices. A correct gate work function yields a good fit in the subthreshold regime. Fitting 2D simulations resulted in a gate work function of 4.55eV, which is close to the gate work function as determined by measurements.

The lateral doping profile was extracted for 2D simulations by fitting the SS

versus gate length and by fitting the subthreshold current-voltage characteristic for various standard deviations of the doping profile, especially for short channel devices. This resulted in a standard deviation of 10nm. However the current-voltage behavior for very short channel devices could not be fitted accurately with a 2D lateral doping profile only.

Therefore 3D simulations are performed with a step in the doping profile in the height of the fin. By examining the SS versus gate length and the I_{ds}-V_{gs} curves it was concluded that the electrical behavior of the device with a step function positioned at 0.04 μm from the top gate of the device agrees best with the measured electrical behavior. Still the simulated and measured electrical behavior does not coincide completely. Especially around the threshold voltage the simulated and measured I_{ds}-V_{gs} curves differ probably due to corner effects.

The current in super threshold can be fitted by adjusting the source/drain width and contact dimensions and positioning of the contacts. In reality the resistivity of the source/drain junctions is reduced by selective epitaxial growth, thus increasing the width of the source/drain junctions. For a source/drain width of 11.5nm the simulation and measurement fit well.

The 2D and 3D simulations are in good agreement for long channel devices, while in super threshold the graphs differ. In subthreshold the current-voltage characteristic is determined by the area of the fin, which is the same for the 2D and 3D simulations, while in super threshold gate width is important. In a 2D simulation the top gate is not taken into account. Accordingly the perimeter of the inversion layer in the 2D case is underestimated.

For very short channels the SS for 2D and 3D do not correspond precisely. This difference is caused by the variation in standard deviation, since the mesh is not exactly the same for 2D and 3D. Therefore the doping profile differs slightly, which becomes significant for very short channel devices.

Nevertheless, it is questionable whether a unique doping profile can be obtained, because some device parameters are derived based on specifications given by IMEC, i.e. equivalent dielectric layer thickness, fin dimensions and the doping of the device. When such a parameter is different in reality, a different combination of other device parameters gives similar electrical behavior in simulation, such that it still fits nicely with its measured counterpart.

Chapter 5

Automated determination of device parameters

In this thesis a method is described to obtain a 2-D doping profile such that the simulated subthreshold I_{ds}-V_{gs} characteristics, over a broad range of bias conditions (i.e. V_{gs}, V_{ds} and V_{bs}) match the corresponding experimental data. The results obtained in the previous chapter are found by manipulating the device parameters manually until a best fit is achieved. The device parameters can also be extracted automatically by using a optimization function, such as the lsqnonlin function of Matlab.

The least square function minimizes the normalized difference between the measured and simulated I_{ds}-V_{gs} curve. The function starts at initial device parameter values, as stated by the user, and finds the minimum of the sum of squares of the normalized difference by sweeping device parameter values. The device parameters that are deduced automatically are the gate work function, the position of the peak doping, the standard deviation of the lateral gaussian doping profile and the doping profile in the height of the fin.

5.1 Outline

The process parameters are extracted by inverse modeling. The simulation outline for the automatic determination of the device parameters corresponds to the outline of the manual determination. However, the routine is slightly reduced to reduce the the total simulation time. The SS and source/drain overlaps are determined simultaneously by looking at the I_{ds}-V_{gs} behavior at high drain-source voltage (step 2 and 3 of the flow diagram of figure 4.3 are combined) and the simulations are only performed in the subthreshold regime up to a V_{gs} of 40mV.

The first physical parameter to determine is the work function of the gate material for a 2D simulation. The work function of the gate can be determined from the subthreshold I_{ds}-V_{gs} characteristic of long channel devices.

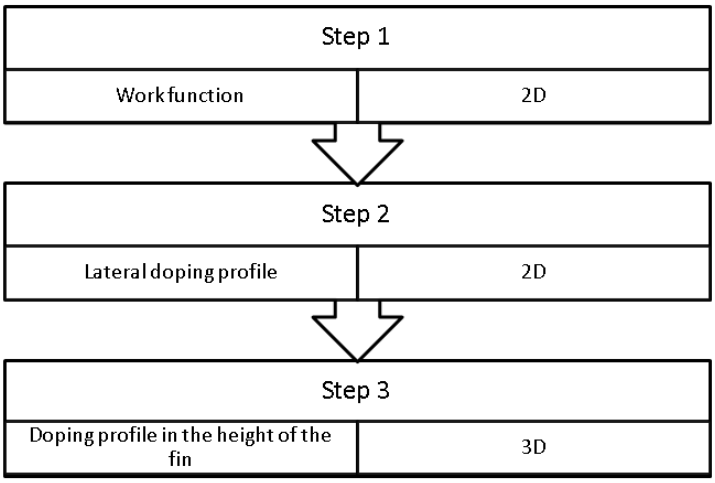


Figure 5.1: Flow diagram of the automatic extraction of device parameters

When the gate work function is known the SS and the drain-source overlaps can be adjusted. The SS can be modified by adjusting the lateral doping profile and the gate-drain/source overlaps to obtain a good DIBL. This can be verified by fitting the simulated and the measured subthreshold current-voltage characteristic at high V_{ds}. At high V_{ds} DIBL becomes significant, especially for short devices.

When the doping profile in lateral direction is determined, the doping profile in the height of the fin can be worked out, this requires 3D simulations. By plotting the measured and simulated current-voltage characteristic for very short channel devices at high V_{ds}, a doping profile in the height direction can be obtained, which is hopefully close to reality.

A schematic representation of the different steps for extracting device parameters through inverse modeling is depicted in figure 5.1.

5.2 The simulation environment

The device parameter values are swept by the lsqnonlin function of Matlab until a best fit is achieved (paragraphs C.5, C.6). The initial values of the doping profile and the swept parameter values are each exported to a text file in order to include the parameter values in the simulation files. The device simulation is performed

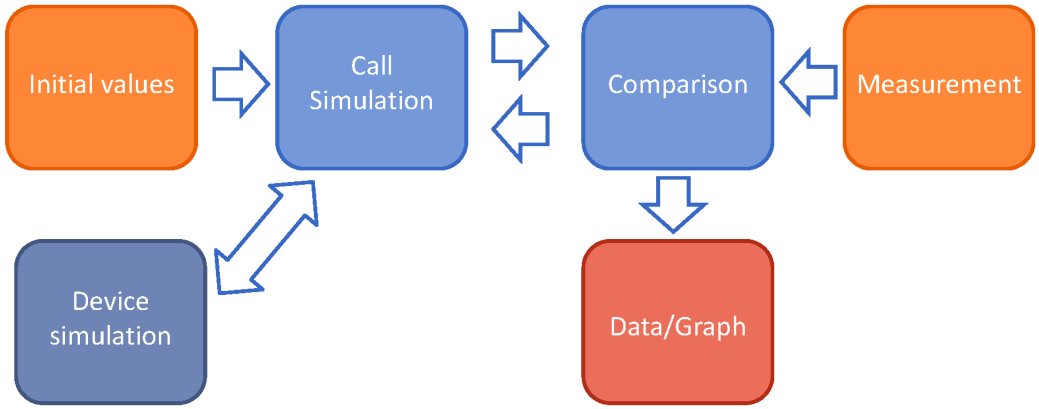


Figure 5.2: Various steps in the automatic extraction of device parameters

by running a shell script (paragraph C.7) that includes the swept device parameter values in the simulations files and runs Sentaurus Structure Editor (paragraph C.1, C.3), Sentaurus Device (paragraph C.2, C.4) and Inspect (paragraph C.8) . A device structure is created by Sentaurus Structure Editor, the electrical behavior of the created structure is calculated by Sentaurus Device and the simulation result is extracted by plotting the current-voltage behavior in Inspect and writing the current-voltage data to a text file. Then the normalized difference between the measured and simulated current-voltage behavior is determined. The simulation and comparison is started with initial values, the routine is repeated until a minimum normalized error is achieved. A schematic representation of the various steps in the automatic extraction procedure is depicted in figure 5.2.

When the simulation is done some operations are performed in Matlab such that the simulated I_{ds}-V_{gs} data can be compared with the measured data. The simulation data includes information about the sweeping of the bias conditions to the initial values. This information is not relevant for the current-voltage behavior and is therefore removed. Accordingly the least square function determines the normalized difference between the measured and simulated current-voltage behavior. The measured and simulated gate-source voltages must correspond in array length. This is done by interpolating the drain current of the simulation results logarithmicly. The result of the extraction of a device parameter is written to a text file so it can be used in the next inverse modeling steps.

For the simulation of the 3D structure an extra operation is required. The lsqnonlin algorithm changes the swept device parameter value by a small step, in order to determine if and in what direction the device parameter has to be adjusted, in order to find the minimum of the sum of squares of the normalized difference between the measured and reference current-voltage behavior. For the position of the step in the doping profile in the height of the fin, this adjustment is smaller then the mesh resolution. Hence, a new simulation yields identical results. In order to make the small step of the position in the doping profile in the height of the fin larger then

the mesh resolution, the initial parameter value is reduced with a factor 1E5. Before the device parameter is written to a text file in order to include it in the simulation files, the device parameter value is compensated for the factor. Consequently the step in the device parameter value as given by the lsqnonlin algorithm is increased with the same factor.

5.3 Results

Initially the automatic extracting of the device parameter values is verified with previous simulation results instead of measurement data, in order to determine the accuracy of the extraction of the parameter values and the required number of iterations. Then the automated extraction of the device parameters is applied to measurement data.

Note that only half of the device is simulated, which is possible because the FinFET is (in principle) a symmetrical device. Of course, in order to compare the simulation results with the measurements, the current should be multiplied by 2. Another important note is that non-idealities such as interface states, fixed charge, stress effects and quantum-confinement are not taken into account.

Gate work function

The first physical parameter to look at is the work function of the gate material.

Initially the automatic extracting of the device parameter values is verified with previous simulation results instead of measurement data for a device with a gate length of 10μm, a V_{ds} of 25mV and a fin width of 10nm. The automatic routine is compared to a simulation result with a gate work function of 4.56eV, as reference. The used initial value is 4.59eV, the initial parameter value have to be chosen close to the expected final values otherwise an other optimum for the normalized error may be found. Different results of the iteration of the automatic routine are depicted in figure 5.3. The reference I_{ds}-V_{gs} characteristic is depicted in the figure as well.

In the figure are depicted the first, third and last iterations. The second iteration consist of a small step in gate work function in order to determine whether the gate work function has to increase or decrease. Each iteration takes a few minutes; the whole routine consists of 5 to 8 iterations and takes approximately twenty minutes. The final gate work function is 4.5599eV, which is an excellent result.

The automated routine for the extraction of the gate work function is applied to I_{ds}-V_{gs} measurement data of a device with a gate length of 10μm, at a V_{ds} of 25mV and a fin width of 10nm. In 8 iterations and approximately twenty minutes the routine determines a gate work function of 4.5568eV.

Note that for 2D simulations the simulated and measured I_{ds}-V_{gs}, in the near or super threshold the graphs differ, as discussed in paragraph 4.5. In order to determine the gate work function accurately, the normalized difference between the

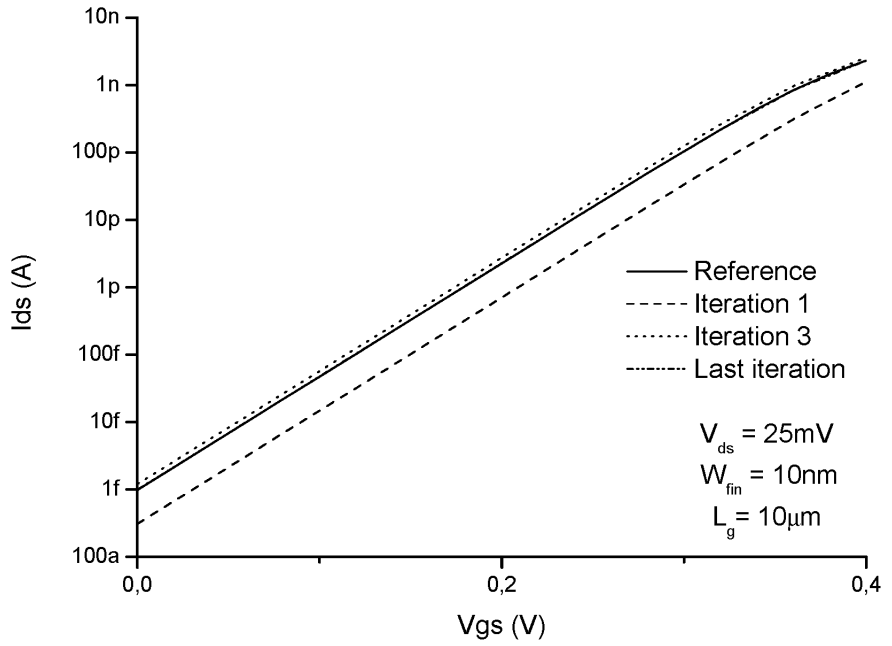


Figure 5.3: Measured and simulated current-voltage characteristic for various iterations for determining the gate work functions with $W_{fin} = 10\text{nm}$, $L_g = 10\mu\text{m}$, and $V_{ds} = 25\text{mV}$

measured and simulated I_{ds}-V_{gs} curve have to be weighted: deep in subthreshold the normalized difference is more important than close to the threshold voltage.

Lateral doping profile

The next step is to adjust the lateral doping profile and the gate-drain/source overlaps to obtain a good DIBL.

Initially the automatic extracting of the device parameter values is verified with previous simulation results instead of measurement data for a device with a gate length of 30nm, a V_{ds} of 1V and a fin width of 10nm. The automatic routine is compared to a simulation result with a standard deviation of 10nm and no gate-source/drain overlap, as reference. The initial parameter value is 11nm. Different results of the iteration of the automatic routine are depicted in figure 5.4. The reference I_{ds}-V_{gs} characteristic is depicted in the figure as well.

As for the determination of the gate work function the figure depicts the first, third and last iterations. Each iteration takes a few minutes, the whole routine consists of 12 iterations and takes approximately half an hour. The final standard deviation of the lateral doping profile is 10.0025nm and a gate-source/drain overlap of $2.55 \cdot 10^{-4}$nm, hence an excellent result.

The automated routine for the extraction of the lateral doping profile is applied to I_{ds}-V_{gs} measurement data of a device with a gate length of 45nm, at a V_{ds} of 1V and a fin width of 10nm. In 7 iterations and approximately twenty minutes the

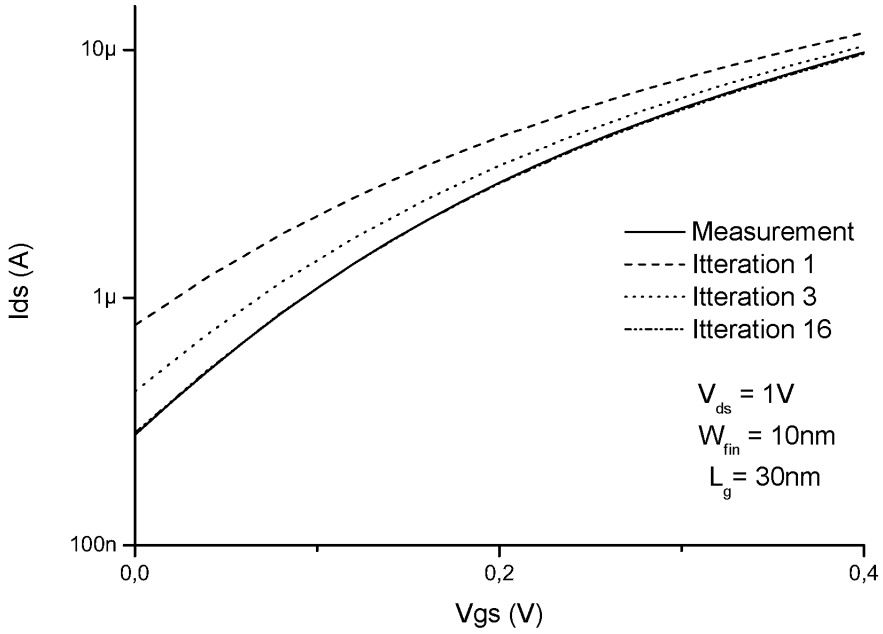


Figure 5.4: Measured and simulated current-voltage characteristic for various iterations for determining the gate work functions with $W_{fin} = 10$nm, $L_g = 30$nm, and $V_{ds} = 1$V

routine determines a standard deviation of 9.3nm and a gate source/drain overlap of $4.062 \cdot 10^{-4}$nm.

Note that for short devices at high drain-source voltage GIDL becomes significant, as discussed in paragraph 2.5. The effects of GIDL are not taken into account in the device simulations. In order to determine the lateral doping profile accurately, the normalized difference between the measured and simulated I_{ds}-V_{gs} curve has to be weighted. At low V_{gs} and close to the threshold voltage the normalized difference has to be weighted less.

Doping profile in the height of the fin

Subsequently the vertical doping profile is determined with 3D simulations, by looking at the I_{ds}-V_{gs} characteristic for very short channel devices at high V_{ds}.

The simulations are performed for a device with a gate length of 30nm, a V_{ds} of 1V and a fin width of 10nm. The automatic routine is compared to a simulation result with a step function located at 40nm from the top-gate, as reference. The initial parameter value is 20nm. After two iterations the automated routine determines that a h at 31nm from the top gate is an optimal value. The resulting simulated and measured curve don't match as well as expected. The deviation may be caused by adjusting the step size of the least square algorithm, as discussed in paragraph 5.2, or by a mesh which is not dense enough in certain areas or because the tolerance of the least square function of Matlab is not tight enough.

The tolerance of the least square function determines the termination tolerance

	Manual extraction	Automated extraction
Gate work function (eV)	4.55	4.5568
Standard deviation (nm)	10	9.37
Gate-source/drain overlap (nm)	0	0

Table 5.1: Comparison between the manual extraction routine and the automated routine

of the function. When the tolerance is lowered a more accurate fit is achieved, but as a consequence the number of iterations is increased and hence the simulation time increases accordingly.

The automated extraction of the doping profile in the height of the fin by 3D simulation has to be improved in order to derive the vertical doping profile accurately.

Comparison between automatic and manual parameter extraction

In chapter 4 the device parameters were extracted manually in this chapter the same device parameters were extracted with an automated routine. The resulting parameter values are compared in the table 5.1.

The extracted device parameter values agree quite well. Especially the gate work function and the gate-source/drain overlaps coincide well. The standard deviation of the lateral doping profile is quite off, enlarged by the difference in gate work function.

5.4 Discussion

In this chapter a routine was discussed which determines the device parameter values automatically. The routine consists of three steps: extracting the gate work function, determine the lateral doping profile and deduce the vertical doping profile.

In 8 iterations and approximately twenty minutes the routine determines a gate work function of 4.5568eV. The standard deviation and gate source/drain overlap are deduced in 7 iterations and approximately twenty minutes, the resulting values are 9.3nm and $4.062 \cdot 10^{-4}$nm respectively. The vertical doping profile does not match as well as expected. The deviation may be caused by adjusting the step size of the least square algorithm, as discussed in paragraph 5.2, or by a mesh which is not dense enough in certain areas or because the tolerance of the least square function of Matlab is not tight enough.

The extracted automated device parameter values agree quite well with its manually determined counterpart.

Chapter 6

Conclusions

The aim of this thesis is to investigate whether a (unique) doping profile can be extracted from subthreshold current.

A theoretical model of the subthreshold current, for long and short channel devices, is deduced in order to understand which device parameters have significant influence on the SS.

The device parameters that have the largest influence on the device characteristics are the doping profile in the fin, and hence electrical channel length, the oxide thickness, the dielectric constant of the oxide and gate work function.

The doping profile has influence on the drain current of the device, in particular for short channel devices (<70nm), because of its influence on the effective channel length and minimum surface potential, and consequently the threshold voltage. The work function difference also influences the threshold voltage.

The theoretical model was compared with the measured current-voltage behavior. The model of the current-voltage behavior of FinFETs is accurate for long and short channel devices at low and high drain-source voltage. For very short channel devices the model underestimates the short channel effects slightly, probably caused by the variation in fin width. For very short channel devices (<45nm) accelerated threshold voltage reduction has to be taken into account.

The process parameters are extracted by inverse modeling employing 2D or 3D device simulations. An important note is that non-idealities such as interface states, fixed charge, stress effects and quantum-confinement were not taken into account.

The gate work function can be derived from the current voltage behavior of long channel devices, while the doping profile can be extracted from the SS and shift in the subthreshold current for short channel devices.

First the work function of the gate material was determined from the current voltage behavior of long channel devices. A correct gate work function yields a good fit in the subthreshold regime. Fitting 2D simulations resulted in a gate work func-

tion of 4.55eV.

The lateral doping profile was extracted for 2D simulations by fitting the SS versus gate length and by fitting the subthreshold current-voltage characteristic for various standard deviations of the doping profile, for short channel devices. This resulted in a standard deviation of 10nm. However the current-voltage behavior for very short channel devices could not be fitted accurately with a 2D lateral doping profile only.

3D simulations were required to determine the vertical doping profile. The vertical doping profile in the simulation consists of a step profile in the height of the fin. By examining the SS versus gate length and the I_{ds}-V_{gs} curves it was concluded that the electrical behavior of the device with a step function positioned at 0.04 μm from the top gate of the device agrees best with the measured electrical behavior. Still the simulated and measured electrical behaviors did not coincide completely. Especially around the threshold voltage the simulated and measured I_{ds}-V_{gs} curves differ, probably due to corner effects. In order to determine the doping profiles accurately in the height of the fin, more information is needed.

It was shown that the 2D and 3D simulations are in good agreement in subthreshold, while in super threshold the graphs differ. In subthreshold the current-voltage characteristic is determined by the area of the fin, which is the same for the 2D and 3D simulations, while in super threshold the effective channel width is important. In a 2D simulation the top gate is not taken into account. Accordingly the (effective) perimeter of the inversion layer in the 2D case is underestimated.

The current in super threshold can be fitted by adjusting the source/drain width and contact dimensions and positioning of the contacts. In reality the resistivity of the source/drain junctions is reduced by selective epitaxial growth, thus increasing the width of the source/drain junctions. For a source/drain width of 11.5nm the simulation and measurement fit well.

Besides the manuals extraction of the device parameters, an automated routine is developed for extracting the device parameters. The routine consists of three steps: extracting the gate work function, determining the lateral doping profile and deducing the vertical doping profile.

In 8 iterations and approximately twenty minutes the routine determines a gate work function of 4.5568eV. The standard deviation and gate source/drain overlap are deduced in 7 iterations and approximately twenty minutes, the resulting values are 9.3nm and $4.062 \cdot 10^{-4}$ respectively.

The vertical doping profile does not match as well as expected. The deviation may be caused by adjusting the step size of the least square algorithm, as discussed in paragraph 5.2, or by a mesh which is not dense enough in certain areas or because the tolerance of the least square function of Matlab is not tight enough. Another reason could be that the doping profile should be gaussian. The extracted automated device parameter values agree quite well with their manually determined counterparts.

It is possible to extract device parameters from the measured subthreshold current by inverse modeling. However it is questionable whether a unique doping profile is obtained, because some device parameters were determined on the basis of specification given by IMEC, i.e. equivalent dielectric layer thickness, fin dimensions and the doping of the device. The derived device parameters could differ from reality and due to a compensating effect of some device parameters the simulated electrical characteristics nevertheless fit nicely with their measured counterparts. Supposing that specifications given by IMEC are valid, it is still questionable wether a unique combination of the lateral and vertical doping profile is obtained, because perhaps another combination of lateral and vertical doping profile is possible. In order to determine the doping profiles accurately, especially in the height of the fin, more information is needed and the automated routines should perhaps be scanned through the realistic (fitting) parameter space [9].

Chapter 7

Recommendations

In this thesis a technique is described for obtaining a doping profile such that the simulated subthreshold I_{ds}-V_{gs} characteristics match the corresponding experimental data over a broad range of bias conditions (i.e. V_{gs} and V_{ds}).

The method is suitable for determining the gate work function and the lateral doping profile. However, the accuracy of the doping profile in the height of the fin is questionable. More research is needed to develop the technique further. Some recommendations for future work is proposed in this chapter.

7.1 Doping profile in the height of the fin

For the doping profile in the height of the fin a step profile was used, which is a rough simplification of a gaussian profile. A step in the profile is however not a realistic doping profile. In reality doping profiles do not change abruptly, but show a gaussian behavior. The standard deviation of the gaussian doping profile in the vertical direction can be extracted by looking at the SS vs gate length and the I_{ds}-V_{gs} characteristic, as discussed in paragraph 4.4 of this thesis.

7.2 Bulk-source voltage

The accuracy of the doping profile in the height of the fin, as determined in paragraph 4.4, is questionable, because multiple fits can be achieved for slight variance in the doping profiles, as described in paragraph 4.5. In order to determine the doping profile in the height of the fin accurately, more information about the influence of the doping profile in the height of the fin on the electrical behavior is needed. A method often used for determining doping profile in the bulk of a MOSFET is the body effect. The doping profile is extracted by evaluating the device behavior as a function of the substrate bias (body effect). By applying a bulk-source voltage, the depletion depth is changed. For a NMOS the depletion depth increases for a more negative V_{bs}. The current changes according to the change in depletion depth, because due to a change in depletion layer depth, the depletion charge changes, which causes a corresponding change in the inversion charge. Consequently the current changes as

a result of applying a V_{bs}. Because the body effect depends on the doping in the substrate, the doping profile in the height of the fin can be determined by fitting the measured I_{ds}-V_{gs} curve with simulations at a different bulk source voltages [26].

For the FinFets used in this thesis no bulk contact exists. However, by applying a high voltage to the BOX contact, the bulk source voltage of the device is indirectly changed. The change in applied back gate voltage causes a shift in the I_{ds}-V_{gs} curves. This shift provides information on the doping profile in the depth direction.

Simulations are performed at different V_{bs} bias voltages at different steps in the doping profile, namely at 60nm and 40nm from the top gate. (With a BOX layer of 0.1μm thickness). The results of the simulation are depicted in figure 7.1

The simulated current-voltage relation of the devices with different doping profile in the height direction behaves differently to the applied V_{box} voltages. When the doping profile is uniform, the shift in threshold voltage due to the applied bulk voltage is larger than for a step at 40nm from the top gate. Because the shift in threshold voltage at different substrate bias is unique for a certain doping profile, according to [26], the body effect can be used to deduce the vertical doping profile in the fin.

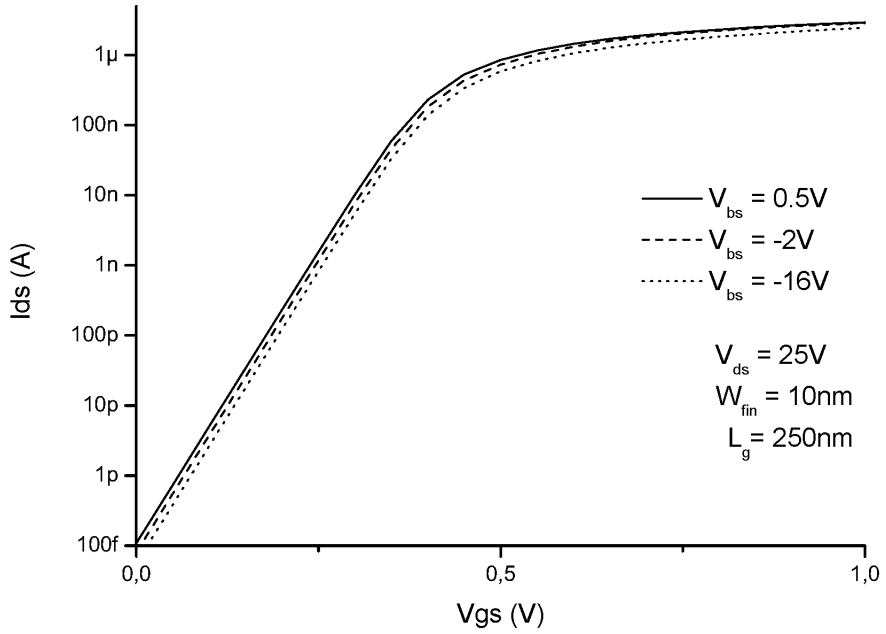
7.3 Influence of interface states on the SS and threshold voltage

As discussed in paragraph 2.5, the interface traps charge and discharge governed by the applied bias, thereby affecting the charge distribution inside the device and thus the current-voltage characteristic, i.e. the threshold voltage and the SS [18]. On one hand the effect of the interface states on the SS is expected to be much less in FinFETs than for its bulk counterparts, because of volume inversion. On the other hand less doping is present in the channel region, so the influence of the interface states on the SS is expected to be more prominent. The influence of the interface states may explain differences between the measured and simulated I_{ds}-V_{gs} curve, which can't be explained by variations in the doping profile.

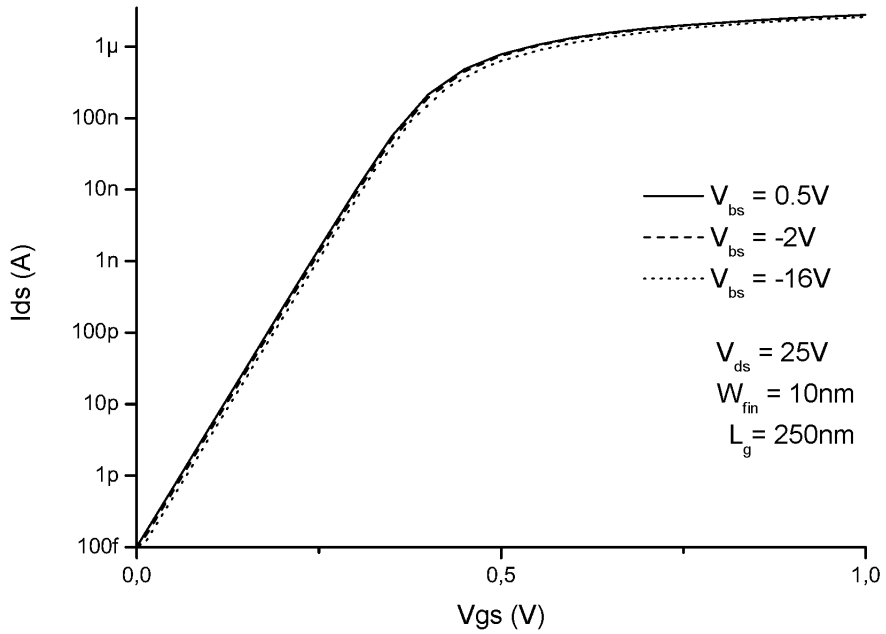
7.4 Extend the algorithm for the automatic determination of device parameters

In chapter 5 was concluded that the extraction of the vertical doping profile by the automated routine was not yet accurate. This might be caused by adjusting the step size of the least square algorithm, as discussed in paragraph 5.2, or by a mesh which is not dense enough in certain areas or because the tolerance of the least square function of Matlab is not tight enough. The routine can be improved for the extraction for the doping profile in the vertical direction.

The routine consists of three steps: extracting the gate work function, determining the lateral doping profile and deducing the vertical doping profile (in specific



(a)



(b)

Figure 7.1: Simulated I_{ds}-V_{gs} relation for different V_{bs} voltages for two different step profiles (a) 60nm (b) 40nm from the top gate

order). With this setup it is not sure whether the obtained doping profile is unique, because perhaps another combination of lateral and vertical doping profile is possible. Combining the extraction of the doping profile in lateral and vertical direction may result in an unique combination of doping profiles. However, when the two steps are combined, the doping profiles have to be extracted using 3D simulations, consequently the simulation time will increase. To optimize the automated extraction of device parameters a lot of work has to be done.

Appendix A

List of acronyms

DIBL Drain Induced Barrier Lowering

SOI Silicon on Insulator

BOX Buried Oxide

GIDL Gate Induced Drain Leakage

SS Subthreshold Slope

Appendix B

List of Symbols

A	Area	m^2
$C_{//}$	Short channel capacitance	F
C_{dep}	Depletion capacitance	F
C_{ox}	Oxide capacitance	F
C_{sc}	Source-channel capacitance	F
C_{dc}	Drain-channel capacitance	F
D_n	Electron diffusion constant	$cm^2\ s^{-1}$
E_c	Conduction band	eV
E_v	Valence band	eV
H_{fin}	Height of the fin	m
I_{ds}	Drain-source current	A
$J_n(x)$	Diffusion current density	Am^2
k	Boltzmann constant	$m^2\ kg\ s^{-2}\ k^{-1}$
L_{eff}	Effective channel length	m
L_{gate}	Printed gate length	m
L_g	Metallurgical gate length	m
l	Characteristic length	
m	Ideality factor	
m^*	effective mass	kg
N_a	Acceptor doping concentration	m^{-3}
n_i	Intrinsic carrier concentration	m^{-3}
n_p	Minority concentration	m^{-3}
n_{p0}	Minority concentration at the source	m^{-3}
p	Hole concentration	m^{-3}
h	planck's constant	$m^2\ kg\ s^{-1}$
$Q_{s/d}$	Charge in source/drain-channel capacitance	C
q	Elementary charge	C
S	Subthreshold Slope	V/dec
Si	Silicon	
SiO_2	Silicon-oxide	
T	Temperature	K

V_{bi}	Build in voltage between source/drain-channel	V
V_{ds}	Drain-source voltage	V
V	Voltage over source/drain-channel capacitance	V
V_{gb}	Gate-channel voltage	V
V_{gs}	Gate-source voltage	V
V_{sL}	Long channel surface potential	V
V_{th}	Threshold voltage	V
W	Depletion depth	m
W_{fin}	Width of the fin	m
x_0	Position of the minimum surface potential	m
x_{dp}	The position of the depletion layer at the source side of the channel	m
$\Delta\phi_f$	Work function difference	eV
ΔL	Variation in channel length	m
ϵ	Electric field	Vm^{-1}
ϵ_{ox}	Relative permittivity of Silicon oxide	
ϵ_{si}	Relative permittivity of Silicon	
μ_t	Thermal voltage	V
ϕ_b	Built in potential	V
ϕ_m	Gate work function	eV
χ_{si}	Electron affinity	V
$\psi(x)$	Potential	V
$\psi(x0)$	Minimum surface potential	V
$\psi_s(0)$	Channel surface potential at the source	V
$\psi_s(L)$	Channel surface potential at the drain	V
$\psi_s(x)$	Channel surface potential	V
ψ_{smin}	Minimum surface potential	V

Appendix C

Simulation files

C.1 Sentaurus Structure Editor file for 2D simulations

```
; template file for symmetric DG NMOS

; Reinitialize SDE
(sde:clear)

; --- Begin user settings ---
;
; define/set global device parameters
(define Lg @DopingAtDepth@)    ; total gate length
(define Lsd 0.25) ; source/drain length
(define Toxf 0.002) ; front oxide thickness
(define Toxb Toxf)  ; back oxide thickness
(define Tsi @tsi@)  ; body thickness
(define Tpoly 0.0)  ; ideal gates

;
; --- End user settings ---

; temp global parameters
(define ref 2.5)  ; temp refinement factor

; meshing resolution (in microns)
(define rx_body 2)
(define ry_body 1)
(define rx_poly 2)
(define ry_poly 1)
(define rx_sd 0.1)
(define ry_sd ry_body) ; var
(define rx_oxf  rx_body)
(define ry_oxf  0.05)
(define rx_box  0.8)
(define ry_box  0.1)

; define/set internal geometry parameters, symmetric around (x,y)=(0,0)
(define Lgneg (* Lg -0.5) )
(define Lgpos (* Lg 0.5) )
(define Tsineg (* Tsi -0.5) )
(define Tsipos (* Tsi 0.5) )
(define fgmin (- (- Tsineg Toxf) Tpoly) )
(define bgmax (+ (+ Tsipos Toxb) Tpoly) )

; Select default Boolean expression for overlapping regions; ABA means 'new
    region replaces old'
(sdegeo:set-default-boolean "ABA")
```

```
; Create device regions
(sdegeo:create-rectangle (position Lgneg (- Tsineg Toxf) 0.0) (position Lgpos Tsineg 0.0) "SiO2" "R.fgox")
(sdegeo:create-rectangle (position Lgneg Tsineg 0.0) (position Lgpos 0.0 0.0) "Silicon" "R.body")
(sdegeo:create-rectangle (position (- Lgneg Lsd) Tsineg 0.0) (position Lgneg 0.0 0.0) "Silicon" "R.source")
(sdegeo:create-rectangle (position Lgpos Tsineg 0.0) (position (+ Lgpos Lsd) 0.0 0.0) "Silicon" "R.drain")

; Define contacts
(sdegeo:define-contact-set "source" 4 (color:rgb 1 0 0 )"##" )
(sdegeo:define-contact-set "drain" 4 (color:rgb 0 1 0 )"##" )
(sdegeo:define-contact-set "fgate" 4 (color:rgb 1 1 0 )"##" )

; Setting contacts at edges
(sdegeo:define-2d-contact (find-edge-id (position (- Lgneg Lsd) -0.001 0.0)) "source")
(sdegeo:define-2d-contact (find-edge-id (position (+ Lgpos Lsd) -0.001 0.0)) "drain")
(sdegeo:define-2d-contact (find-edge-id (position 0.0 fgmin 0.0)) "fgate")

; Define doping profiles - per material
(sdedr:define-constant-profile "Const.Silicon" "BoronActiveConcentration" 1e+17)

; Define doping profiles - per region
(sdedr:define-constant-profile "Const.SD" "ArsenicActiveConcentration" @Doping@)
(sdedr:define-constant-profile "HDD" "ArsenicActiveConcentration" @Doping@)
(sdedr:define-constant-profile "HDD2" "ArsenicActiveConcentration" @Doping@)

;Define refinement window
(sdedr:define-refeval-window "profile" "Line" (position (- Lgpos @hd@) Tsineg 0.0) (position (- Lgpos @hd@) 0 0.0))
(sdedr:define-refeval-window "profile2" "Line" (position (+ Lgneg @hd@) Tsineg 0.0) (position (+ Lgneg @hd@) 0 0.0))

;Gaussian profile
(sdedr:define-gaussian-profile "doping.profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" @Doping@ "ValueAtDepth" 1e+17 "Depth" @hdd@ "Gauss" "Factor" 1e20)
(sdedr:define-gaussian-profile "doping.profile2" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" @Doping@ "ValueAtDepth" 1e+17 "Depth" @hdd@ "Gauss" "Factor" 1e20)

;Gaussian doping placement
(sdedr:define-analytical-profile-placement "place" "doping.profile" "profile" "Positive" "NoReplace" "Eval")
(sdedr:define-analytical-profile-placement "place2" "doping.profile2" "profile2" "Negative" "NoReplace" "Eval")

; Place doping profiles
(sdedr:define-constant-profile-material "PlaceCD.Silicon" "Const.Silicon" "Silicon")
(sdedr:define-constant-profile-region "PlaceCD.Source" "Const.SD" "R.source" 0 "Replace")
(sdedr:define-constant-profile-region "PlaceCD.Drain" "Const.SD" "R.drain" 0 "Replace")
(sdedr:define-constant-profile-region "PlaceCD.hdd" "HDD" "R.hdd" 0 "Replace")
(sdedr:define-constant-profile-region "PlaceCD.hdd2" "HDD2" "R.hdd2" 0 "Replace")

; Default meshing strategy per region
; xmax, ymax, xmin, ymin
(sdedr:define-refinement-size "RefDef.Body" rx_body ry_body (/ rx_body ref) (/ ry_body ref))
(sdedr:define-refinement-region "PlaceRF.Body" "RefDef.Body" "R.body")
```

```
(sdedr:define-refinement-size "RefDef.S" rx_sd ry_sd (/ rx_sd ref) (/ ry_sd
    ref))
(sdedr:define-refinement-region "PlaceRF.S" "RefDef.S" "R.source")
(sdedr:define-refinement-size "RefDef.D" rx_sd ry_sd (/ rx_sd ref) (/ ry_sd
    ref))
(sdedr:define-refinement-region "PlaceRF.D" "RefDef.D" "R.drain")
(sdedr:define-refinement-size "RefDef.fgox" rx_oxf ry_oxf (/ rx_oxf ref) (/ ry
    _oxf ref))
(sdedr:define-refinement-region "PlaceRF.fgox" "RefDef.fgox" "R.fgox")

; define mesh refinement near Si/SiO2 interface...
(sdedr:define-refinement-size "RefDef.if" rx_body 0.0001 (/ rx_body ref)
    0.0001)

; ...and near S/D junctions
(sdedr:define-refinement-size "RefDef.jun" 0.0005 ry_body 0.0005 (/ ry_body
    ref))

; define refinement windows...
(sdedr:define-refinement-window "RefWin.iff" "Rectangle" (position Lgneg
    Tsineg 0.0) (position Lgpos (+ Tsineg 0.002) 0.0))

(sdedr:define-refinement-window "RefWin.S" "Rectangle" (position (- Lgneg
    0.015) Tsineg 0.0) (position (+ Lgneg 0.015) Tsipos 0.0))
(sdedr:define-refinement-window "RefWin.D" "Rectangle" (position (- Lgpos
    0.015) Tsineg 0.0) (position (+ Lgpos 0.015) Tsipos 0.0))

; ...and place mesh refinement
(sdedr:define-refinement-placement "PlaceRF.iff" "RefDef.if" "RefWin.iff")
(sdedr:define-refinement-placement "PlaceRF.S" "RefDef.jun" "RefWin.S")
(sdedr:define-refinement-placement "PlaceRF.D" "RefDef.jun" "RefWin.D")

;create files (new format)
(sde:build-mesh "snmesh" "" "n@node@_msh")
```

C.2 Sentaurus Device file for 2D simulations

```
# initial solution
sdevice_init "

    File {
      Grid        = "n@previous@_msh.tdr"
  Current     = "@plot@"
    Output      = "@log@"
  Plot        = "@tdrdat@"
      # parameter file for Lucent mobility model
      Parameter = "lucent.par"
    }

    Electrode {
        { Name="drain"     Voltage=@VDINI@ }
        { Name="source"    Voltage=@VSINI@ }
        { Name="fgate"     Voltage=@VGINI@  Workfunction = @workfunctie@}
    }

    Physics {
        Temperature=300
        AreaFactor=0.06
        EffectiveIntrinsicDensity( Slotboom )
        Recombination( SRH( ElectricField( Lifetime = Hurkx
                  DensityCorrection = None))  )
   # Lucent mobility model
        Mobility( PhuMob Enormal eHighFieldSaturation hHighFieldSaturation )
     }

     # quantities to be shown in 2D cross-section (Tecplot)
     Plot {
```

```
        Doping
32      DonorConcentration
        AcceptorConcentration
34      EffectiveBandGap
        ConductionBandEnergy
36      ValenceBand
        SpaceCharge
38      ElectricField
        Potential
40      eDensity
        hDensity
42      eMobility
        hMobility
44      eCurrent
        hCurrent
46      eVelocity
        hVelocity
48      TotalRecombination
    }
50  # plot the following quantities at coordinates (X Y) in Inspect
    CurrentPlot {
52      Potential ((0.0 0.0))
        eDensity ((0.0 0.0))
54      hDensity ((0.0 0.0))
    }
56
    # some math options. no need to change these
58  Math {
  Wallclock
60      RelErrControl
        Extrapolate
62      Iterations=20
        Number_of_Threads=maximum
64
  # stop simulation if draincurrent is smaller than 1E-17 A/um
66      BreakCriteria
        {
68        Current (Contact = "drain" minval = 1E-17)
        }
70  }

72 # solve initial conditions
Solve {
74      Poisson
        Coupled { Poisson }
76      Coupled { Poisson Electron Hole}
}
78
Solve {
80  Quasistationary
        (
82              Goal { Name="drain" Voltage=@VDS@ }
        )
84      {
          Coupled ( Iterations=10 ) { Poisson Electron Hole}
86        Plot
                (FilePrefix="n@node@_vg0")
88
                Save(FilePrefix="n@node@_vg0")
90      }

92 Quasistationary (InitialStep=0.1 MaxStep=0.05 MinStep=0.0001 Increment=2
    Decrement=1.5
  Goal { Name="fgate" Voltage=0.4})
94  {Coupled ( Iterations=10) {Poisson Electron Hole}
    Plot
96              (
                FilePrefix="n@node@_vg04")
```

```
98
                Save(FilePrefix="n@node@_vg04")
100         }

102 Quasistationary (InitialStep=0.010 MaxStep=0.10 MinStep=0.00001 Increment=1.5
        Decrement=2
             Goal { Name="fgate" Voltage=@VGEND@})
104         {Coupled ( Iterations=15 ) { Poisson Electron Hole}
                Plot
106             (
                )
108         }
        }
```

C.3 Sentaurus Structure Editor file for 3D simulations

```
1 ; template file for symmetric DG NMOS

3 ; Reinitialize SDE
  (sde:clear)
5
  ; --- Begin user settings ---
7 ;
  ; define/set global device parameters
9 (define Lg @DopingAtDepth@)    ; total gate length
  (define Lsd 0.25) ; source/drain length
11 (define Toxf 0.002) ; front oxide thickness
  (define Toxb Toxf)  ; back oxide thickness
13 (define Tsi @tsi@)  ; body thickness
  (define Tpoly 0.0)  ; ideal gates
15
  ;
17 ; --- End user settings ---

19 ; temp global parameters
  (define ref 2.5)  ; temp refinement factor
21
  ; meshing resolution (in microns)
23 (define rx_body 2)
  (define ry_body 1)
25 (define rx_poly 2)
  (define ry_poly 1)
27 (define rx_sd 0.1)
  (define ry_sd ry_body) ; var
29 (define rx_oxf  rx_body)
  (define ry_oxf  0.05)
31 (define rx_box  0.8)
  (define ry_box  0.1)
33
  ; define/set internal geometry parameters, symmetric around (x,y)=(0,0)
35 (define Lgneg (* Lg -0.5) )
  (define Lgpos (* Lg 0.5) )
37 (define Tsineg (* Tsi -0.5) )
  (define Tsipos (* Tsi 0.5) )
39 (define fgmin (- (- Tsineg Toxf) Tpoly) )
  (define bgmax (+ (+ Tsipos Toxb) Tpoly) )
41
  ; Select default Boolean expression for overlapping regions; ABA means 'new
      region replaces old'
43 (sdegeo:set-default-boolean "ABA")

45 ; Create device regions
  (sdegeo:create-rectangle (position Lgneg  (- Tsineg Toxf)   0.0) (position
      Lgpos Tsineg  0.0) "SiO2" "R.fgox")
47 (sdegeo:create-rectangle (position Lgneg  Tsineg   0.0) (position Lgpos  0.0
       0.0) "Silicon" "R.body")
```

```
(sdegeo:create-rectangle (position (- Lgneg Lsd) Tsineg  0.0) (position Lgneg
    0.0  0.0) "Silicon" "R.source")
(sdegeo:create-rectangle (position Lgpos  Tsineg  0.0) (position (+ Lgpos Lsd
    ) 0.0  0.0) "Silicon" "R.drain")

; Define contacts
(sdegeo:define-contact-set "source" 4 (color:rgb 1 0 0 )"##" )
(sdegeo:define-contact-set "drain" 4 (color:rgb 0 1 0 )"##" )
(sdegeo:define-contact-set "fgate" 4 (color:rgb 1 1 0 )"##" )

; Setting contacts at edges
(sdegeo:define-2d-contact (find-edge-id (position (- Lgneg Lsd)  -0.001 0.0))
    "source")
(sdegeo:define-2d-contact (find-edge-id (position (+ Lgpos Lsd)  -0.001 0.0))
    "drain")
(sdegeo:define-2d-contact (find-edge-id (position  0.0  fgmin 0.0)) "fgate")

; Define doping profiles - per material
(sdedr:define-constant-profile "Const.Silicon" "BoronActiveConcentration" 1e
    +17)

; Define doping profiles - per region
(sdedr:define-constant-profile "Const.SD" "ArsenicActiveConcentration"
    @Doping@)
(sdedr:define-constant-profile "HDD" "ArsenicActiveConcentration" @Doping@)
(sdedr:define-constant-profile "HDD2" "ArsenicActiveConcentration" @Doping@)

;Define refinement window
(sdedr:define-refeval-window "profile" "Line" (position  (- Lgpos @hd@)
    Tsineg  0.0) (position (- Lgpos @hd@)  0  0.0))
(sdedr:define-refeval-window "profile2" "Line" (position  (+ Lgneg @hd@)
    Tsineg  0.0) (position  (+ Lgneg @hd@)  0  0.0))

;Gaussian profile
(sdedr:define-gaussian-profile "doping.profile" "ArsenicActiveConcentration" "
    PeakPos" 0 "PeakVal" @Doping@ "ValueAtDepth"  1e+17  "Depth" @hdd@ "Gauss"
     "Factor" 1e20)
(sdedr:define-gaussian-profile "doping.profile2" "ArsenicActiveConcentration"
    "PeakPos" 0 "PeakVal" @Doping@ "ValueAtDepth" 1e+17 "Depth" @hdd@ "Gauss"
    "Factor" 1e20)

;Gaussian doping placement
(sdedr:define-analytical-profile-placement "place" "doping.profile" "profile"
    "Positive" "NoReplace" "Eval")
(sdedr:define-analytical-profile-placement "place2" "doping.profile2" "profile
    2" "Negative" "NoReplace" "Eval")

; Place doping profiles
(sdedr:define-constant-profile-material "PlaceCD.Silicon" "Const.Silicon" "
    Silicon")
(sdedr:define-constant-profile-region "PlaceCD.Source" "Const.SD" "R.source" 0
     "Replace")
(sdedr:define-constant-profile-region "PlaceCD.Drain" "Const.SD" "R.drain" 0 "
    Replace")
(sdedr:define-constant-profile-region "PlaceCD.hdd" "HDD" "R.hdd" 0 "Replace")
(sdedr:define-constant-profile-region "PlaceCD.hdd2" "HDD2" "R.hdd2" 0 "
    Replace")

; Default meshing strategy per region
; xmax, ymax, xmin, ymin
(sdedr:define-refinement-size "RefDef.Body" rx_body ry_body (/ rx_body ref) (/
     ry_body ref))
(sdedr:define-refinement-region "PlaceRF.Body" "RefDef.Body" "R.body")
(sdedr:define-refinement-size "RefDef.S" rx_sd ry_sd (/ rx_sd ref) (/ ry_sd
    ref))
(sdedr:define-refinement-region "PlaceRF.S" "RefDef.S" "R.source")
(sdedr:define-refinement-size "RefDef.D" rx_sd ry_sd (/ rx_sd ref) (/ ry_sd
    ref))
```

```
(sdedr:define-refinement-region "PlaceRF.D" "RefDef.D" "R.drain")
(sdedr:define-refinement-size "RefDef.fgox" rx_oxf ry_oxf (/ rx_oxf ref) (/ ry_oxf ref))
(sdedr:define-refinement-region "PlaceRF.fgox" "RefDef.fgox" "R.fgox")

; define mesh refinement near Si/SiO2 interface...
(sdedr:define-refinement-size "RefDef.if" rx_body 0.0001 (/ rx_body ref) 0.0001)

; ...and near S/D junctions
(sdedr:define-refinement-size "RefDef.jun" 0.0005 ry_body 0.0005 (/ ry_body ref))

; define refinement windows...
(sdedr:define-refinement-window "RefWin.iff" "Rectangle" (position Lgneg Tsineg 0.0) (position Lgpos (+ Tsineg 0.002) 0.0))

(sdedr:define-refinement-window "RefWin.S" "Rectangle" (position (- Lgneg 0.015) Tsineg 0.0) (position (+ Lgneg 0.015) Tsipos 0.0))
(sdedr:define-refinement-window "RefWin.D" "Rectangle" (position (- Lgpos 0.015) Tsineg 0.0) (position (+ Lgpos 0.015) Tsipos 0.0))

; ...and place mesh refinement
(sdedr:define-refinement-placement "PlaceRF.iff" "RefDef.if" "RefWin.iff")
(sdedr:define-refinement-placement "PlaceRF.S" "RefDef.jun" "RefWin.S")
(sdedr:define-refinement-placement "PlaceRF.D" "RefDef.jun" "RefWin.D")

;create files (new format)
(sde:build-mesh "snmesh" "" "n@node@_msh")
```

C.4 Sentaurus Device file for 3D simulations

```
# initial solution
sdevice_init "

    File {
      Grid        = "n@previous@_msh.tdr"
  Current     = "@plot@"
      Output      = "@log@"
  Plot        = "@tdrdat@"
      # parameter file for Lucent mobility model
      Parameter = "lucent.par"
    }

    Electrode {
        { Name="drain"     Voltage=@VDINI@ }
        { Name="source"    Voltage=@VSINI@ }
        { Name="fgate"     Voltage=@VGINI@  Workfunction = @workfunctie@}
    }

    Physics {
        Temperature=300
        AreaFactor=0.06
        EffectiveIntrinsicDensity( Slotboom )
        Recombination( SRH( ElectricField( Lifetime = Hurkx
                  DensityCorrection = None))  )
  # Lucent mobility model
        Mobility( PhuMob Enormal eHighFieldSaturation hHighFieldSaturation )
     }

    # quantities to be shown in 2D cross-section (Tecplot)
    Plot {
        Doping
        DonorConcentration
        AcceptorConcentration
        EffectiveBandGap
        ConductionBandEnergy
```

```
36          ValenceBand
            SpaceCharge
38          ElectricField
            Potential
40          eDensity
            hDensity
42          eMobility
            hMobility
44          eCurrent
            hCurrent
46          eVelocity
            hVelocity
48          TotalRecombination
        }
50      # plot the following quantities at coordinates (X Y) in Inspect
        CurrentPlot {
52          Potential ((0.0 0.0))
            eDensity ((0.0 0.0))
54          hDensity ((0.0 0.0))
        }
56
        # some math options. no need to change these
58      Math {
     Wallclock
60          RelErrControl
            Extrapolate
62          Iterations=20
            Number_of_Threads=maximum
64
    # stop simulation if draincurrent is smaller than 1E-17 A/um
66          BreakCriteria
            {
68              Current (Contact = "drain" minval = 1E-17)
            }
70      }

72 # solve initial conditions
   Solve {
74          Poisson
            Coupled { Poisson }
76          Coupled { Poisson Electron Hole}
   }
78
   Solve {
80    Quasistationary
            (
82                  Goal { Name="drain" Voltage=@VDS@ }
            )
84          {
              Coupled ( Iterations=10 ) { Poisson Electron Hole}
86            Plot
                    (FilePrefix="n@node@_vg0")
88
                    Save(FilePrefix="n@node@_vg0")
90          }

92 Quasistationary (InitialStep=0.1 MaxStep=0.05 MinStep=0.0001 Increment=2
       Decrement=1.5
     Goal { Name="fgate" Voltage=0.4})
94   {Coupled ( Iterations=10) {Poisson Electron Hole}
       Plot
96                  (
                    FilePrefix="n@node@_vg04")
98
                    Save(FilePrefix="n@node@_vg04")
100         }

102 Quasistationary (InitialStep=0.010 MaxStep=0.10 MinStep=0.00001 Increment=1.5
```

```
    Decrement=2
        Goal { Name="fgate" Voltage=@VGEND@})
104     {Coupled ( Iterations=15 ) { Poisson Electron Hole}
            Plot
106         (
            )
108     }
    }
```

C.5 Matlab file for automatic extraction of device parameters

```
1  clear;

3  ; Parameter deffinitions
   global x;
5  global Rexp;
   global aangeroepen;
7  global b0;

9  aangeroepen=0;

11 ; Initial parameter values
   a0=[4.59];
13 b0=[0 0.01];
   d0=[0.0000003];
15 ; Print initial parameter value to txt file
   fid = fopen('b0.txt', 'wt');
17 fprintf(fid, '%40.39f\n', b0(1,1),b0(1,2));
   fclose(fid)
19
   ; Extraction of gate work function
21 [a,resnorm,residual,exitflag,output]=lsqnonlin('recfun3',a0,[],[],optimset('
       TolFun',1E-6,'TolX', 1E-6))

23 ; Extraction of lateral doping profile
   [b,resnorm,residual,exitflag,output]=lsqnonlin('recfun2',b0,0,1,optimset('
       TolFun',1E-6,'TolX', 1E-6)) % run the lsqnonlin with start value b0,
       returned parameter values stored in b
25
   ; Extraction of vertical doping profile
27 [d,resnorm,residual,exitflag,output]=lsqnonlin('recfun3D',d0,0,0.06,optimset('
       TolFun',1E-6,'TolX',1E-6))
```

C.6 Matlab file for extracting the gate work function

```
1  function y=recfun2(b)

3  ; Parameter deffinitions
   global x;
5  global Rexp;
   global aangeroepen;
7  global simulatie;

9  aangeroepen=aangeroepen+1;

11 ; Measurement data
   data=dlmread('meting.txt', '\t', 1, 0);
13 x=data(:,1);
   Rexp=data(:,2);
15
   ; Print parameter values to txt file
17 fid = fopen('exp.txt', 'wt');
   fprintf(fid, '(define x %40.39f)',b(1,1));
19 fclose(fid)
```

```
fid = fopen('exp2.txt', 'wt');
fprintf(fid, '(define o %40.39f)', b(1,2));
fclose(fid)

fid = fopen('aangeroepen.txt', 'wt');
fprintf(fid, 'aangoerepen = %d\n)', aangeroepen);
fprintf(fid, '%40.39f\n',b(1,2),b(1,1));
fclose(fid)

fid = fopen('lp.txt', 'wt');
fprintf(fid, '%40.39f\n',b(1,2),b(1,1));
fclose(fid)

data2=dlmread('wf.txt', '\t', 0, 0);
a=data2(1,1);

fid = fopen('expWF.txt', 'wt');
fprintf(fid, 'set WF %40.39f\n', a(1,1));
fclose(fid)

; Run device simulations
system('sh sim.sh')

; Read simulation result from text file
simulatie=dlmread('simulation.txt','\t', 1,0);
x_simulatie=simulatie(:,1);
Rsimulatie=2.*simulatie(:,2);

; Remove initial sweep of bias voltages
i=1;
n=1;
c=0;
Rres=0;
while(c==0)
      i=i+1;
      c=x_simulatie(i);
end;
i=i-1;
d=length(Rsimulatie);

while(i<d)
      Rres(n,1)=Rsimulatie(i,1);
      xres(n,1)=x_simulatie(i,1);
      n=n+1;
      i=i+1;
end;

Rres(n,1)=Rsimulatie(i,1);
xres(n,1)=x_simulatie(i,1);

; Initialize parameter
Rres_int_log=0;

; Logarithmic interpolation
Rres_log=10.*log10(Rres);
Rres_int_log=interp1(xres,Rres_log,xex);
R=10.^(Rres_int_log./10);

; Write simulation results to txt file
fid = fopen('Rres.txt', 'wt');
fprintf(fid, '%10.9e\n' , R);
fclose(fid)

; Weigh the importance
y(1:6)=0.1*((R(1:6)-Rex(1:6))./Rex(1:6));
y(6:20)=1*((R(6:20)-Rex(6:20))./Rex(6:20));

```

```
; Plot measurement and simulation in one graph
semilogy(xex,Rex,'ro',xex,R,'b');
```

C.7 Script file for running device simulations

```
; Combine device parameter values with structure file
echo "(sde:clear)" > sde_tmp.scm
cat exp.txt >> sde_tmp.scm
cat exp2.txt >> sde_tmp.scm
cat sde3_dvs.cmd >> sde_tmp.scm

export FILEIN=symDGN

; Set SDE variable, in this case the Si body thickness (in um!)
export SDEVAR=0.010

; Make the structure & mesh (as defined in scm file)
sde -e -l sde_tmp.scm

; run sdevice for temperature 'i'
for i in 300;
do
  ; Combine device parameters with the device simulation file
  echo -e "set TEMP ${i}\n" > idvg_tmp.cmd
  cat expWF.txt >> idvg_tmp.cmd
  echo -e "set VDS \"1\" " >> idvg_tmp.cmd
  cat sdevice5_des.cmd >> idvg_tmp.cmd

  ; Run the simulation with the input file created above
  sdevice --tcl idvg_tmp.cmd

  ; Run inspect to write the simulation data to a text file
  inspect -f inspect.cmd

# end simulation loop per temperature
done
```

C.8 Inspect file for extracting simulation data

```
  set inputf "salsa_T300_msh_des.plt"
    set inputp "salsa_T300_msh_des"

  proj_load $inputf

cv_createDS IdVgs1 \
 "$inputp fgate OuterVoltage" "$inputp drain TotalCurrent" y

 cv_write txt /icenas/home/rossemf/afstuderen/Synopsys/simulaties/automatisch/
     simulation.txt IdVgs1

  script_exit
```

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