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Design of a High Speed Digital to Analog Converter

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MSc. Thesis

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Abstract

The DAC proposed in this work is totally awesome. A simulated intermodulation distortion of lower than $-77dBc$ at $1GS/s$ is obtained. By switching current sources in a (thermometer encoded) digital-to-analog (D/A) converter directly and using a (trimmable) charge redistribution network, high INL and DNL performance is obtained with small output devices. This means that there is little feedback (small overlap capacitances) from the output node to the references nodes; this reduces output dependency of reference voltages (so called memory effect) and thus distortion.

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Chapter 1

Introduction

The growing digital telecommunications market has generated an unprecedented demand for high-speed digital-to-analog (D/A) converters. These converters are mainly used to reconstruct (digitally generated) complex waveforms. To get the highest possible bit-error-rate and getting the most out of the channel capacity, it is required that this signal conversion is done without adding too much noise and without distorting the signal. Advances in very-large scale integration ($VLSI$) allows more processing to be done in the digital domain, which tightens the requirements of the signal conversion even more. A typical wireless transmitter will for example use a digital quadrature modulator to generate an intermediate frequency (IF) signal at high frequency. This relaxes the filter requirements in the analog domain when it is up-converted to the transmit frequency. Furthermore, high bandwidth signals can be generated.

There are many reasons for the drive towards digital signal processing, which include higher spectral efficiency and capacity, lower power consumption, added services, programmability (flexibility) etc.

In $UMTS$ base-stations for example, a total of $60MHz$ of bandwidth is used in 12 channels. These signals could be generated with using only one high-speed D/A converter. Since the output power of these base-stations is quite high ($40W$ and more), a very high signal-to-distortion ratio D/A converter is required. If, for example, the-signal-to distortion ratio is $50dB$ of a base-station radiating $4W$ in a given channel, there will be $-30dBm$ of out-of-channel power transmitted. This out-of-channel power may distort other users in the area that communicate with another base-station. $UMTS$ requirements specify that the adjacent channel leakage power ratio must exceed $45dB$[1].

A frequently used type of D/A converter is a so-called current steering converter[2]. A differential current output of one section is controlled by a differential switching pair that directs a constant current to either of the outputs. An $n-bit$ converter typically uses 2^n-1 (thermometer encoded) of these unity sections (see figure 1.1). An advantage of this type of setup is that DNL (differential non-linearity) matching of these converters easily obtained (device scaling) and the monotonicity is intrinsically guaranteed. Since the area consumption scales rapidly with the number of bits, high resolution (thermometer encoded) converters consume (too) much area. Therefore, mostly a multistage type is used in high-resolution converters. The converter then consists of a high-significant stage and a low-significant stage. The high-significant stage

then controls the *coarse* output current and the low-significant stage the *fine* output current. This means that not many bits $(6-8)$ need to be used in the thermometer-encoded high-significant stage. Note that (for low differential non-linearity) the most-significant stage needs to be accurate at the LSB level of the converter; it needs to be much more accurate than the bit with the lowest significance of the most-significant stage itself. The low-significant stage has much lower linearity requirements: the bit with the lowest significance of this stage is the LSB of the converter.
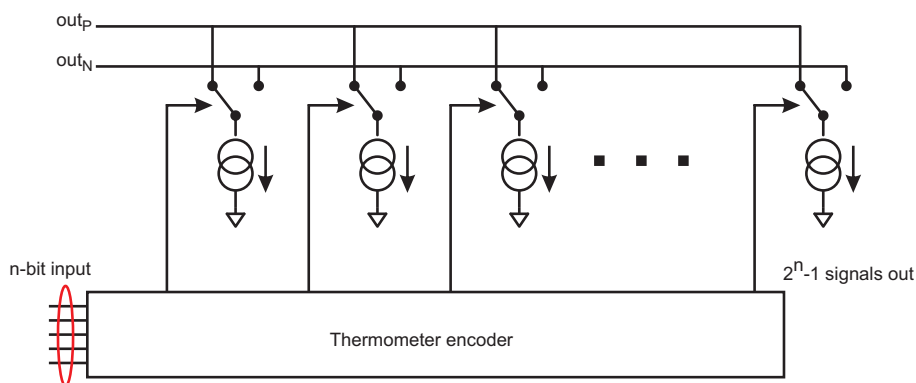
Figure 1.1: Thermometer encoded D/A converter topology

Drawbacks of the 'conventional' current-steering topologies include the requirement of high-precision (voltage) references and accurate switch timing. If (due to capacitive coupling) the voltage references are disturbed the reference will become signal dependent. This feeds to the output and may lead to distortion. Since device sizes will have to be significant (to obtain low INL), capacitive coupling is significant. Also, if the voltage reference retains dependance on the history of the output code, inter-symbol interference is introduced.

1.1   Thesis outline

This thesis focuses on a high-significant thermometer-encoded stage of a multistage D/A converter. In stead of using a switched differential pair it is investigated whether a (directly) modulated current source with dynamic voltage references can be used. With this approach the output current of a single section can be (digitally) 'trimmed' which means that small transistors can be used (with poor passive matching performance).

The remainder of the current chapter informs the reader on some general aspects of the proposed solution. Chapter 2 deals with *some* D/A converter design considerations; required output resistance and impedance, matching and noise performance. Chapter 3 reviews *some* aspects of a conventional (current-steering) converters. The impact of capacitive coupling (overlap capacitances) between the output nodes and the voltage references as well as distortion due to non-linear output capacitance are analyzed. In chapter 4 a number of solutions are presented with their pro's and cons. Section 4.4 describes the proposed

'soft' switching solution, of which it's implementation is further considered in chapter 5. Simulation analyses and results are found in chapter 6.

If the reader only wishes to be informed about the proposed solution; general information is found below and further details and implementation aspects are found in section 4.4 and further.

1.2 Proposed solution - general aspects

This work investigates whether it is possible to used a modulated current source in a D/A converter. Typically, high-precision high-speed D/A converters use a thermometer encoded topology. This means that for an n-bit converter $(2^n - 1)$ unity current sources are used of which each can be connected to the positive or negative output. In this work, each section in a thermometer encoded converter uses two current sources that separately drive the positive or negative output (see figure 1.2). By applying the inverter digital input signal to the current source that is connected to the negative output, the same result is obtained.
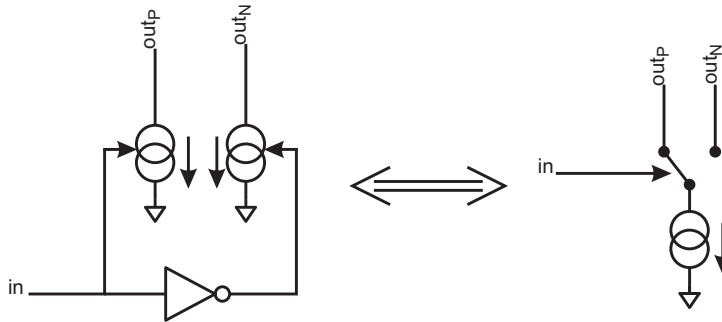
Figure 1.2: Two independent current sources drive the differential output

When modulating the current source directly, switching edges will be much slower than what is found with using a current steering topology. Having limited rise and fall times means that when for two consecutive periods the output signal of a given current source needs to be high, not twice the charge of one period is injected into the output. This leads to inter-symbol interference (see figure 1.3).

To overcome this problem, a current source should not be turned *ON* for more than one period. To be able to output current for consecutive periods, two separate current sources should be used (in a single channel). These current sources then will be used alternatively; each current source outputs a pulse into the output.

Since a differential output is assumed, each section in a thermometer encoded D/A converter consists of 4 current sources. Note that *ONE* (and only *ONE*) current source will generate an output pulse in one period. All other current sources are *OFF* at that period. This means that there is always one current source generating a pulse and three that are off. This is very a useful reasoning when analyzing the noise and differential and integral non-linearity: there is always *ONE* source that injects the noise of a current source carrying a *HIGH* signal to an output and three sources that inject the noise of a current source carrying a *LOW* signal to the output.
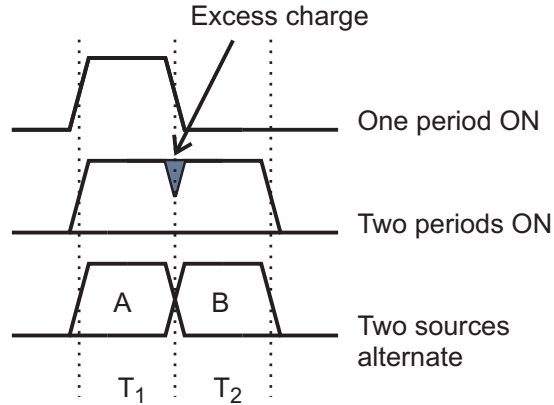
Figure 1.3: Finite switching edges - inter-symbol interference

There will be some digital logic that generates appropriate signals for the sources.

1.2.1   Current source implementation

The proposed solution (as described in section 4.4) uses a charge redistribution network (capacitive divider) and a switch to drive a current source transistor. This is shown in figure 1.4.
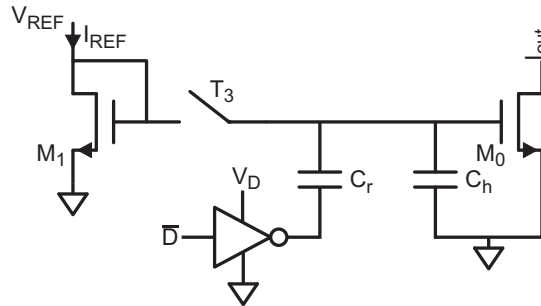
Figure 1.4: current source implementation

The digital input (D) drives a capacitive divider network. This means that the voltage step on the gate of M_0 will be a fraction of voltage V_D:

$$\Delta V_{G,M_0,p-p} = V_D \frac{C_r}{C_r + C_h}$$

This determines the peak-peak switching voltage on the gate of M_0. It is required however that the voltage on the gate node switches between two 'fixed' levels (see figure 1.5). Therefore, a switch is placed which connects the gate node to a reference voltage. When the input signal D is high (the voltage on the gate of M_0 is then high), the switch is closed. The voltage on the gate is then V_{REF}. When the voltage needs to be set low, first the switch is opened

and the the signal D is switched low. This subtracts a fixed amount of charge from C_h and the voltage on the gate node drops.
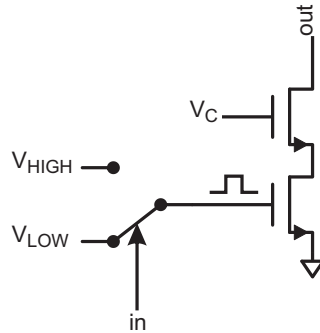
Figure 1.5: Equivalent circuit: gate voltage switches between fixed levels

The output voltage is then determined by the reference voltage, the voltage on node V_D and by the capacitor ratio C_r/C_h. Note that the current source is never turned OFF (gate voltage is never $0V$), instead, it is switched to a LOW current. The 'effective' output current of a single section in a thermometer encoded converter is then the $HIGH$ current minus the LOW current. Not switching OFF transistor M_0 entirely has a number of advantages:

1. Transistor M_0 and M_1 keep carrying significant current. This means that the transition frequency of these transistors is still reasonably high and the settling time of the voltages and currents is still relatively short. If the transistors would be switched OFF entirely, the voltage at the source of M_1 would be (more or less) 'floating' (it will take a long time to settle to a stable value).

2. A substantial amount of charge is accumulated in the channel of M_0 and M_1 below the threshold voltage if the devices are switched off entirely. This charge is dropped and accumulated each cycle which leads to severe voltage/current dumping. The resulting spikes may drive the transistors out of their 'normal' operating region which may lead to distortion.

3. By 'adjusting' the capacitor ratio (C_r/C_h) the LOW voltage and current level can be 'trimmed'. If this is implemented properly, very small output transistors can be used (with very poor passive matching). This reduces problems with overlap capacitances and output impedance variation (discussed in detail in chapter 2).

1.2.2 Trimming the current source

This capacitor ratio 'adjusting' can be done by implementing the charge redistribution capacitor C_r as a bank of (binary weighted) capacitors (see figure 1.6). Note that only a fraction of the capacitor C_r needs to be altered (only to compensate mismatch). Therefore, in the final proposed solution a 'nominal' capacitor and a 'small' (configurable) bank of capacitors are used. The 'nominal' capacitor will add and subtract a large amount of charge from the hold capacitor, which is always the same.

Since the *HIGH* voltage is determined by the V_{REF} voltage (it is connected with a low-ohmic switch) the *LOW* current is effectively trimmed. Since the (effective) output current is $I_{HIGH} - I_{LOW}$ it is possible to 'trim' the output current by altering the peak-peak voltage swing on the gate of M_0.

When the output current of a given current source needs to be increased, the voltage swing on the gate must be increased. This means that a higher (effective) capacitor C_r is required. Instead of actually adding and removing capacitors, the driving signal of some of the capacitors is altered. A capacitor in the binary weighted capacitor bank can for example be connected to ground instead of the driving signal 'D'. In this 'single-edge' trimming solution it means that this capacitor adds to C_h and no longer injects charge into the hold capacitor. Another possibility is connecting a capacitor in the bank to the inverted 'D' signal. In this 'double-edge' trimming solution *this* capacitor injects and subtracts charge in the opposite direction, and thus lowering the voltage swing on the gate of M_0.
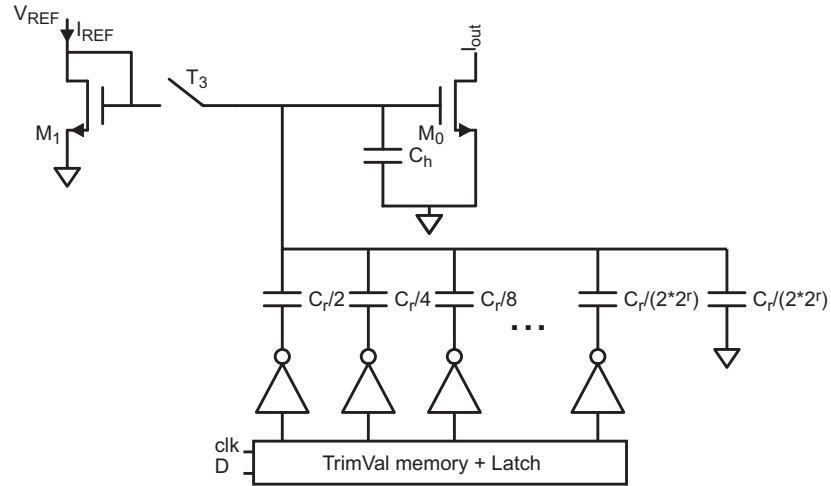
Figure 1.6: Segmented charge redistribution capacitor - trim output current

There are two ways to trim the circuit: trim the differential non-linearity (DNL) of the integral non-linearity (INL). In the first case only the output current 'step size' is compared with a 'reference' step. This means that difference between the output current at digital input code N and at code $N + 1$ is compared with a 'reference' and compensated. Note that this 'reference' step can be a previously trimmed step; this way each step is compared with another until all steps are equal. This reduces the DNL *and* the INL. The integral non-linearity can also be trimmed; in this case the *absolute* value of the output is corrected. Starting from code zero, each value is measured and compensated. Note that this type of trimming requires that the output current is measured absolute and with high accuracy; in practice this will mean that external (off-chip) measurement systems need to be used. A DNL trim mechanism, however, only requires two 'values' to be compared with each other; the 'trim' code can than be increased until the values are equal. This *is* implementable on the same chip.

Chapter 2

DAC design considerations

This chapter deals with various general design issues of current-mode output D/A converters. The first section deals with the required DC output resistance of a current source used in a D/A converter. It is seen there, that there is a minimum required DC output resistance to obtain a converter with sufficiently low low-frequency distortion; this leads to design criteria (current source dimensions). In the next section, the integral non-linearity (INL) due to device mismatch is analyzed for various converter types. In a conventional D/A topology, low INL is obtained by device scaling.

The third section shows how transistor dimensions can be optimized to obtain low output capacitance. In some types of D/A converters this output capacitance is switched (between outputs); high current-source output capacitance may lead to distortion. With the design criteria in section 2.1 and 2.2, a cascoded current source is optimized for low output capacitance.

The last section deals with various noise sources of (switched) current source circuits.

2.1 Current source output resistance modulation

Intuitively, it is easily understood that the output resistance of a current source needs to be high to obtain accurate output currents that are independent of output voltage. In practice, however, the output resistance of a (cascoded) current-source will be finite. Refer to fig. 2.1. In the figure, R_{Ox} are the output resistances of a current source. For reasonable ratios of output resistance and load resistance this is, other then a little power loss, not a big problem.

In current output D/A converters, however, these current sources consist of a (thermometer encoded) series of switched current sources of equal value. This means that the output conductance increases proportionally with the output current. If more current sources are added to one output, the output conductance will increase proportionally. This effectively means that the (small signal) gain of the circuit is inversely proportional to the output voltage level (an LSB step is smaller if the output current is high), which means that it introduces distortion to time varying output signal; a signal is added to the output which is dependent on the input signal and it behaves non-linear. The output voltage of the given circuit is described by eq. 2.1 (see also appendix
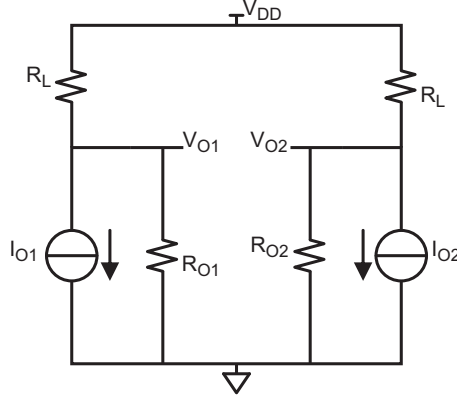
Figure 2.1: D/A converter output stage modeling - finite current source output resistance

B).

$$V_{OUT} = \frac{V_{DD} - R_L I_{O1}}{1 + \frac{R_L}{R_T}\frac{I_{O1}}{I_{NS}}} - \frac{V_{DD} - R_L I_{O2}}{1 + \frac{R_L}{R_T}\frac{I_{O2}}{I_{NS}}} \tag{2.1}$$

rewritten

$$V_{OUT} = V_0 \frac{I_{IN}/I_{DC}}{1 - B^2 \frac{I_{IN}^2}{I_{DC}^2}}$$

where

$$B = \frac{R_L \frac{I_{DC}}{I_{NS}}}{R_T + R_L \frac{I_{DC}}{I_{NS}}} \tag{2.2}$$

Where R_L is the load resistance, R_T the full-scale output resistance (all sources are ON), I_{NS} the full-scale output current and I_{DC} the average single channel (DC) output current.

The intermodulation distortion of the third harmonic ($IM3$)can be evaluated by solving the Fourier integral ratio at $\omega = \omega_0$ and $\omega = 3\omega_0$. If there are no other (more significant) tones at the output, this is the same as the spurious-free dynamic range ($SFDR$). Assuming the following full-scale sinusoidal input signal:

$$I_{IN} = I_{DC} sin(\omega_0 t)$$

The fourier integral:

$$F(n) = V_0 \int_{-2\pi}^{2\pi} \frac{sin(\omega_0 t)}{1 + B^2 sin^2(\omega_0 t)} sin(n\omega_0 t)\, dt$$

The solution at the first (ω_0) and third harmonic ($3\omega_0$):

$$F(1) = V_0 \frac{-4\pi(\sqrt{1 - B^2} - 1)}{B^2 \sqrt{1 - B^2}}$$

$$F(3) = V_0 \frac{-4\pi(4 - 3B^2 + B^2\sqrt{1 - B^2} - 4\sqrt{1 - B^2})}{B^4 \sqrt{1 - B^2}}$$

The spurious-free dynamic range is then:

$$\sqrt{SFDR}(B) = \frac{F(1)}{F(3)} = \frac{(\sqrt{1-B^2}-1)B^2}{4-3B^2+B^2\sqrt{1-B^2}-4\sqrt{1-B^2}}$$

It can be expected that B will be much smaller than 1, therefore, this function can be approximated with a Taylor-series at $B = 0$. Substituting $B^2 = x$, and multiplying with x:

$$R(x) = x\sqrt{SFDR(\sqrt{(x)})} = \frac{(\sqrt{1-x}-1)x^2}{4-3x+x\sqrt{1-x}-4\sqrt{1-x}}$$

The Taylor approximation then is:

$$R'(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + ...$$

The constants are evaluated (using 'l Hopital's rule subsequently) and the first constants are found to be $-4, 0, 4, 6, 0$. The SFDR can then be written as:

$$\sqrt{(SFDR(B))} = \frac{a_0}{B^2} + a_1 + a_2 B^2 + a_3 B^4 + ...$$

For high signal-to-distortion ratio's (more then $40dB$) only the first term in the approximation is required. In this case B^2 is quite small, and the first term in the Taylor series is dominant. The function can then be approximated by $4/B^2$. The error for higher signal-to-distortion ratios is smaller than 1% (B is defined by equation 2.2).

$$SFDR(dB) = 20\log_{10}\frac{4}{B^2} = 40\log_{10}2(\frac{2R_T}{R_L}+1) \tag{2.3}$$

The SFDR due to output resistance modulation (eq. 2.3) is shown in fig. 2.2. For a resistance ratio of 250 (when the load resistance is 50Ω, the output resistance would have to exceed $12.5k\Omega$) the SFDR will be greater than $120dB$.

This situation is also simulated in Matlab. A sinusoidal input signal is generated (with DC-offset) and a fast-fourier transform operation is done on the output of eq. 2.1. The result is shown in fig. 2.3. The signal is normalized to the power of the input tone. It is seen in the figure that indeed the power of the third harmonic is $120dB$ lower than that of the signal.

Note that the input signal is now full-scale (the output swings over the entire DC output current range). If this ratio is decreased the distortion (ratio) will be higher.

2.1.1   MOST parameter choice for low LF distortion

To estimate MOST dimensions for the cascode circuit in fig. 2.4, the first order MOST approximations in eq. 2.4 are used. The MOST parameters for CMOS065 are given table 2.1 (see appendix A). The values in the table are interpolated at $V_{GT} \approx 0.1$ and $V_{DS} \approx 0.5$. Note that these parameters hold for small device-lengths (smaller than $0.3\mu m$ a maximum error of 12% in λ_0).

$$I_D = \frac{1}{2}k_0\frac{W_{eff}}{L_{eff}}V_{GT}^2(1+\frac{\lambda_0}{L}V_{DS}) \tag{2.4}$$
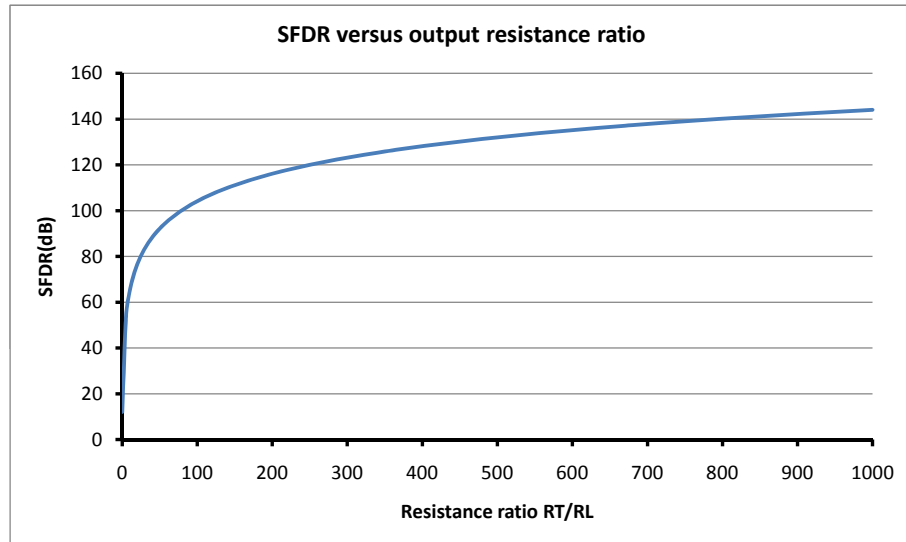
Figure 2.2: SFDR versus resistance ratio output resistance and load resistance
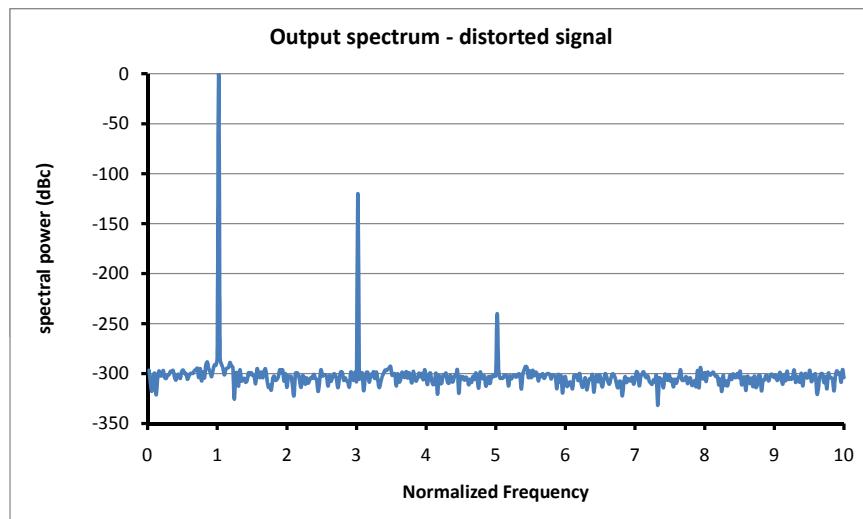
Figure 2.3: Output spectrum of output resistance modulated current source; $R_T = 12.5k\Omega$, $R_L = 50\Omega$
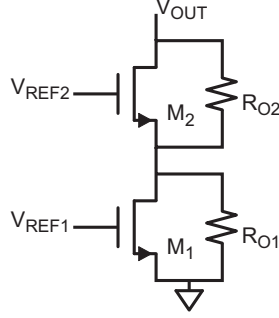
Figure 2.4: Cascoded current source device with output resistances

The output resistance of a single MOST

$$R_O = \frac{\delta V_{DS}}{\delta I_D} = (\frac{1}{2}k_0\frac{W_{eff}}{L_{eff}}V_{GT}^2\frac{\lambda_0}{L})^{-1} \approx \frac{L}{\lambda_0 I_D}$$

The total output resistance of a cascoded current source can be approximated by the multiplication of the output resistance of the current source (M_1) and the gain of the cascode transistor, as is shown in eq. 2.5.

$$
\begin{aligned}
R_{OUT} &= R_{O1}R_{O2}gm_2 = \frac{L_1}{\lambda_0 I_D}\frac{L_2}{\lambda_0 I_D}\sqrt{2k_0 I_D\frac{W_{eff,2}}{L_{eff,2}}} \\
&= \frac{L_1 L_2}{\lambda_0^2 I_D}\sqrt{\frac{2k_0 W_{eff,2}}{I_D L_{eff,2}}} = \frac{2L_1 L_2}{\lambda_0^2 I_D V_{GT,2}}
\end{aligned}
\tag{2.5}
$$

where (rewriting eq. 2.4)

$$\frac{k_0 W_{eff,2}}{L_{eff,2}I_D} = \frac{2}{V_{GT,2}^2}$$

Note that the total output current will usually be limited (due to a conventional load resistance of 50Ω). Therefore, the drain current of a single cascoded current source in a thermometer encoded D/A converter can be written as a function of the maximum (single channel) output current.

$$I_D = \frac{I_M}{2^n - 1}$$

substituting this eq. 2.5

$$R_{OUT} = (2^n - 1)R_T = \frac{2L_1 L_2(2^n - 1)}{\lambda_0^2 I_M V_{GT,2}}$$

Note that R_T is the output resistance of a single channel which is carrying the maximum output current, I_M. This means the following condition should hold

$$R_T = \frac{2L_1 L_2}{\lambda_0^2 I_M V_{GT,2}}$$

Most Parameter	Value	Dim
λ_0	0.11	$\mu m/V$
k_0	225.6	$\mu A/V^2$

Table 2.1: First order most parameters of a CMOS65 NMOST

An error in the driving voltage (threshold voltage mismatch or noise at the gate) leads to only little output current error if the transconductance of the current-source transistor is low. This means that the overdrive voltage of this device should be high (see eq. 2.6).

$$gm = \frac{\delta I_D}{\delta V_{GS}} = k_0 \frac{W_{eff}}{L_{eff}} V_{GT} = \frac{2I_D}{V_{GT}} \qquad (2.6)$$

where (rewriting eq. 2.4)

$$k_0 \frac{W_{eff}}{L_{eff}} = \frac{2I_D}{V_{GT}^2}$$

If, for example, a 10 bit thermometer coded D/A converter is considered with a $1V$ supply voltage ($V_{GT,0} = 0.2$), an output current range of $10mA$ and a SFDR of more then $100dB$ then eq. 2.7 should hold. Note that the full-scale current single channel output resistance should be lower than $R_T > 4.2k\Omega$; this means each individual current source must have an minimum output resistance of $4.2k\Omega(2^n - 1) \approx 4.2M\Omega$. The current in each individual source is $10mA/(2^n - 1) \approx 10\mu A$.

$$L_1 L_2 = 0.0508 \qquad (2.7)$$

If L_1 is chosen $0.3\mu m$, $L_2 \approx 0.15\mu m$ then W_2 will be $2.361\mu m$ (cascode overdrive voltage is $0.1V$). The total output resistance then would be $4.78k\Omega$ (ProMost). Note that the performance deteriorates quickly with small transistor dimensions, it is therefore advisable to choose the transistor lengths greater than $0.2\mu m$.

2.2   Current source mismatch

This section deals with current source mismatch in thermometer coded, binary coded and multisection D/A converters. A cascoded current source is considered with gate-source voltage mismatch as is described by eq. 2.8

$$\sigma_{Vgs} = \frac{A_{Vgs}}{\sqrt{WL}} \qquad (2.8)$$

Two current sources of equal value will then have a current mismatch which is defined by σ_i, which is the product of σ_{Vgs} and the transconductance (see eq. 2.9).

$$\sigma_i = \sigma_{Vgs} gm = \frac{A_{Vgs}}{\sqrt{WL}} \sqrt{2k_0 \frac{W}{L} I_D} = \frac{A_{Vgs}}{L} \sqrt{2k_0 I_D} \qquad (2.9)$$

A_{Vgs} is defined as the mismatch standard deviation of a 1-by-1μm *single* device.

2.2.1 Thermometer coded D/A converter

In thermometer coded D/A converters $(2^n - 1)$ current-sources are switched between the positive and negative output. At $\frac{1}{2}$ full-scale the differential output level is zero. If the digital input is increased by b, then b current sources are switched to the positive output. An advantage of such a converter is that monotonicity is intrinsically guaranteed. The transfer of a thermometer coded D/A converter is shown in fig. 2.5. Another nice property of some thermometer encoded D/A converters is that the maximum output level is exactly the same as minus the negative maximum output signal. This is the case when the same current-sources are used in the positive and negative channel (differential switching pair). Note that this even holds when the output conductance (modulation) of the individual channels is finite; it is only important that the maximum positive output current is equal to the maximum negative output current.
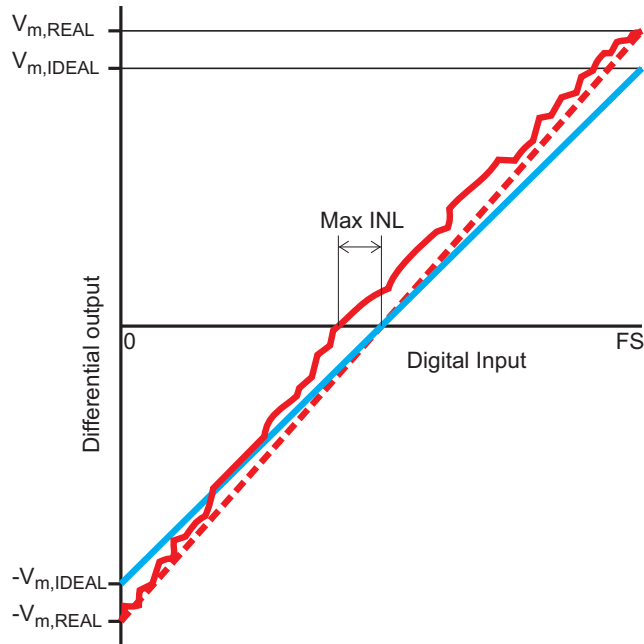
Figure 2.5: Transfer of thermometer coded D/A converter

Considering a stand-alone thermometer coded D/A converter, a result of mismatch is that there will be an error in the gain. If the gain is considered the maximum minus the minimum output current divided by the code range, the integral error will be low near the edges; code zero and full-scale will match exactly. In the figure, the dashed (red) line indicates this situation. It is intuitively understood that the maximum INL is then found at a digital input of $\frac{1}{2} full - scale$. The error at this code is given in eq. 2.10. All error currents are summed and directed to the output. Note that one LSB output current (ΔI) is twice the average current of a current source (differential output with the same current sources). Note that the average INL will be lower then this; at the edges the INL reduces to zero as the fitted gain error matches the actual

value exactly.

$$INL_{MAX,MSB} = \frac{1}{2}\sqrt{2^n - 1}\frac{\sigma_i}{\Delta I} \qquad (2.10)$$

If this thermometer coded converter is used as a (MSB) section of a multi-stage D/A converter, the accuracy of this (part of the) converter needs to be higher then one LSB over the entire input range of the converter. The gain error must then be considered as non-linearity of the transfer. The straight (blue) line in figure 2.5 indicates this situation. It is clear that the INL will be the same for all digital input codes and equal to what is shown in eq. 2.10 (all current sources contribute to the error for all codes).

Transistor dimensions for low INL

Substituting equation 2.9 in 2.10 yields the size requirement of the current source (equation 2.11).

$$INL_{MAX,MSB} = \frac{1}{2}\frac{A_{Vgs}}{L}\sqrt{\frac{2k_0}{I_M}}(2^n - 1) \qquad (2.11)$$

with I_M the full-scale single channel output current. Rewriting

$$L = \frac{1}{2}A_{Vgs}\sqrt{\frac{2k_0}{I_M}}\frac{2^n - 1}{INL_{MAX,MSB}}$$

If this section is the MSB part of a multi-stage converter, with a total resolution of nr bits, the length can be written in terms of LSB integral non-linearity. This is shown in equation 2.12.

$$INL_{MAX,LSB} = INL_{MAX,MSB}\frac{2^{nr} - 1}{2^n - 1} \qquad (2.12)$$

substituting into equation 2.11

$$L = \frac{1}{2}A_{Vgs}\sqrt{\frac{2k_0}{I_M}}\frac{2^{nr} - 1}{INL_{MAX,LSB}}$$

If, for example, a $10b$ ($n = 10$) thermometer coded D/A converter MSB section that is part of a $13b$ ($nr = 13b$) multistage converter is considered, with a max (LSB) INL of 1 bits, the length of the current source transistor must be at least $3.48\mu m$ (in $CMOS065$, with $A_{Vgs} = 4mV\mu m$ and a maximum output current of $10mA$). The width of the current source transistor will be $10.71\mu m$ ($V_{GT,1} = 0.2V$). This is quite substantial.

2.2.2   Binary coded D/A converter

When using a binary coded D/A converter it is custom to minimize the differential error-current to LSB at MSB flip-over. At this code, $\frac{1}{2}2^n - 1$ current-sources will be replaced by $\frac{1}{2}2^n$ other current sources. The error is given by eq. 2.13.

$$DNL_{Half-Scale} = \frac{1}{2}\sqrt{2^n - 1}\frac{\sigma_i}{\Delta I} \qquad (2.13)$$

2.3 Cascoded current-source output impedance

In this section the output impedance of a cascoded current source is evaluated. Reference voltages that bias the gates of the current source and the cascode transistor are assumed to have low impedance. Consider fig. 2.6. If a current source is connected directly to the output of a (thermometer encoded) converter and the current is modulated by switching the gate of M_1 to a reference or ground, the effect of C_2 on the output will be (more or less) constant; i.e. the capacitance will not be time-varying (only lower the output pole). Therefore, it is not necessary to minimize this capacitance in this case and only output impedance change due to current variation (ON/OFF) in transistor M_1 needs to be minimized.

When the current source is used with a differential switching pair that directs the current to either the positive or negative output, the total output impedance is connected to either output. This means that it is better to maximize the total output impedance.
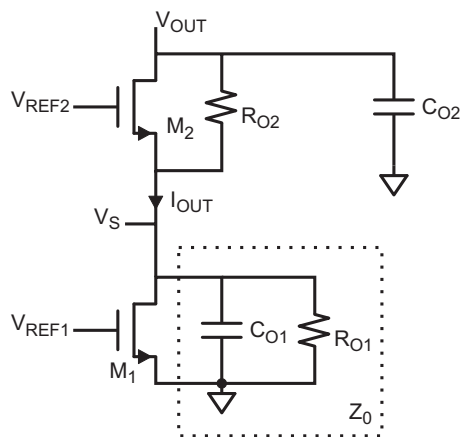
Figure 2.6: Cascoded current source - equivalent circuit

maximize (part of) output impedance (M_1 modulation)

The output impedance of this network is described by eq. 2.14. Note that capacitor C_{O2} is considered not to be (a time varying) part of the output impedance of the network. Z_0 is the equivalent output impedance of transistor M_1.

$$I_{out} = \frac{V_s}{Z_0} = -gm_2 V_s + \frac{V_{out} - V_s}{R_{O2}}$$

rewriting

$$\frac{V_s}{Z_0} + gm_2 V_s + \frac{V_s}{R_{O2}} = \frac{V_{out}}{R_{O2}}$$

$$I_{out} Z_0 (\frac{1}{Z_0} + gm_2 + \frac{1}{R_{O2}}) = \frac{V_{out}}{R_{O2}}$$

$$\frac{V_{out}}{I_{out}} = R_{O2}(1 + gm_2 Z_0 + \frac{Z_0}{R_{O2}}) = R_{O2} + Z_0(1 + gm_2 R_{O2})$$

with

$$Z_0 = \frac{R_{O1}}{1 + j\omega R_{O1} C_{O1}}$$

$$Z_{out} = R_{O2} + \frac{R_{O1}(1 + gm_2 R_{O2})}{1 + j\omega R_{O1} C_{O1}} \tag{2.14}$$

It is seen in the equation that the output impedance scales with the gain of the cascode stage. In a thermometer encoded D/A converter, the output impedance (of a single section) scales inversely proportional to the output code. For low distortion, a first order approximation will be that this impedance needs to be larger than the required output resistance that was described in chapter 2.1. For frequencies higher than the cut-off frequency of the current source (Z_0) the output impedance can be approximated by eq. 2.15. Note that the output impedance needs to be much higher than R_{O2}.

$$Z_{out} = \frac{1}{j\omega \frac{C_{O1}}{1+gm_2 R_{O2}}} \tag{2.15}$$

In section 2.2 the current source transistor length was dimensioned to be larger than $3.48\mu m$ for a $10b$ thermometer coded $13b$ resolution converter stage with an INL of $2LSB$. With an overdrive voltage of $200mV$ the width of this transistor will be approximately $10.7\mu m$ which means that the output capacitance of this device will be $6.5fF$ (overlap, junction). To keep the output impedance below the minimum required DC output resistance at $500MHz$ the gain of the cascode device would then have to exceed $85x$. If the cascode overdrive voltage is $0.1V$ the size of the cascode will have to be $14.32\mu m/1.3\mu m$.

maximize (total) output impedance (differential switching pair)

Note that the cascode output capacitance of M_2 (C_2) is not incorporated in this optimization. It may therefore be more suitable to optimize to low total output impedance: in case of a current-steering converter it is beneficial to have a low total output capacitance since this load is switched between outputs. The width of the cascode transistor for low output capacitance is evaluated in equation 2.16.

$$Z_{OUT} \approx R_{O2} gm_2 \frac{1}{j\omega C_{O1}} // \frac{1}{j\omega C_{O2}} = \frac{1}{j\omega} \frac{1}{C_{O2} + \frac{C_{O1}}{gm_2 R_{O2}}} \tag{2.16}$$

the output resistance of a transistor can be approximated by the following

$$R_{O2} = \frac{L}{\lambda I_D}$$

$$gm_2 R_{O2} = \frac{2L}{V_{GT,2}\lambda}$$

$$Z_{OUT} \approx \frac{1}{j\omega} \frac{1}{C_{DS,0} W_2 + \frac{C_{O1} V_{GT,2}\lambda}{2L_2}}$$

with as fit (see appendix A)

$$\lambda = AL + B$$

and

$$L_{eff,2} = \frac{k_0 W_{eff,2} V_{GT,2}^2}{2I_D}$$

assuming $L_{eff,2} \approx L_2$

$$
\begin{aligned}
Z_{OUT} &= \frac{1}{j\omega} \frac{1}{C_{DS,0}W_2 + \frac{C_{O1}I_D}{k_0 W_2 V_{GT,2}^2}(A\frac{k_0 W_2 V_{GT,2}}{2I_D} + B)} \\
&= \frac{1}{j\omega} \frac{1}{C_{DS,0}W_2 + \frac{V_{GT}AC_{O1}}{2} + BC_{O1}\frac{I_D}{k_0 V_{GT,2}W_2}} = \frac{1}{j\omega C_{EQ}}
\end{aligned}
$$

$$(2.17)$$

In this equation it is seen that there is an optimum in W_2; there is a proportional and an inversely proportional term in the sum. It's maximum is found where the denominator is minimum

$$\frac{\delta C_{EQ}}{\delta W_2} = 0$$

where

$$C_{EQ} = C_{DS,0}W_2 + \frac{V_{GT}AC_{O1}}{2} + BC_{O1}\frac{I_D}{k_0 V_{GT,2}W_2}$$

$$C_{DS,0} - BC_{O1}\frac{I_D}{k_0 V_{GT,2}W_2^2} = 0$$

$$W_2 = \sqrt{B\frac{C_{O1}}{C_{DS,0}}\frac{I_D}{k_0 V_{GT,2}}}$$

If the current source's output capacitance is equal to $6.54 fF$ (device length is $3.48\mu m$, see chapter 2.2), the cascode gate-overdrive voltage $0.1V$, $C_{DS,0} = 184aF/um$, output current $10\mu A$ the width of the cascode will be $1.32\mu m$ ($B = 0.11$, $A = 0$).

It is seen in this section that a small cascode transistor should be used if the total output impedance needs to be maximized. If only the 'change' in output impedance is relevant, a much larger cascode transistor can be used. The output impedance *change* is then much smaller than the *absolute* output impedance.

2.4 Noise contributions

This section deals with various significant noise contributors that may degrade the performance of the D/A converter.

2.4.1 Output transistor noise

The (current) noise for long-channel devices can be described as shown in equation 2.18.

$$i_n^2 = 4k_B T \gamma gm [A^2/Hz]$$

$$(2.18)$$

with $\gamma = 2/3$, $gm = \frac{2I_D}{V_{GT}}$
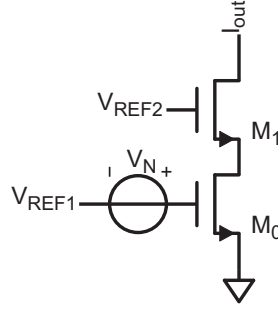
Figure 2.7: Single current source section of a thermometer encoded D/A converter

The noise of a single section (see fig. 2.7) in a thermometer encoded D/A converter transfers directly to an output *at all times*. This means that the noise power of each section should be summed to evaluate the signal-to-noise ratio. For an n-bit converter, this is shown in equation 2.19.

$$I_D = \frac{I_M}{2^n - 1} \tag{2.19}$$

with I_M the maximum (full-scale) single channel output current (differential output assumed)

$$i_n^2 = 4k_B T \gamma \frac{2I_M}{(2^n - 1)V_{GT}}$$

$$i_{n,total}^2 = (2^n - 1)i_n^2 = 4k_B T \gamma \frac{2I_M}{V_{GT}}$$

the signal power (differential output)

$$I_S^2 = \frac{I_M^2}{2}$$

yielding the following signal-to-noise ratio:

$$SNR_{CS} = \frac{1}{BW} \frac{I_M V_{GT}}{16 k_B T \gamma} \tag{2.20}$$

with BW the signal (Nyquist) bandwidth ($\frac{Fs}{2}$).

The signal-to-noise ratio depends on the DC settings of the output transistor; these are usually limited by the supply voltage. With a fixed load (usually $R_L = 50\Omega$) $I_M R_L$ of voltage headroom needs to be accommodated for output voltage swing. This leaves $V_{DD} - I_M R_L$ of minimum voltage for the drain-source of the transistor and thus the maximum overdrive voltage. In a practical situation, however, a cascode transistor is used to meet the output impedance requirements. For a D/A converter operating with a $1V$ supply this means that the total voltage available on the current source will be $0.5V$ ($10mA$ output current). This means that the overdrive voltage of the current source is limited to approximately $0.3V$. With these conditions the signal-to-noise ratio is limited to $81.3dB$ (ENOB is $13.2b$) in a bandwidth of $500MHz$ ($Fs = 1GHz$). Other noise contributors thus need not to be much lower than this.

2.4.2 Current mirror noise

If a current source transistor is implemented as a current mirror, additional noise is added by the reference transistor. This noise is modeled as $V_{N,1}$ in fig. 2.8.
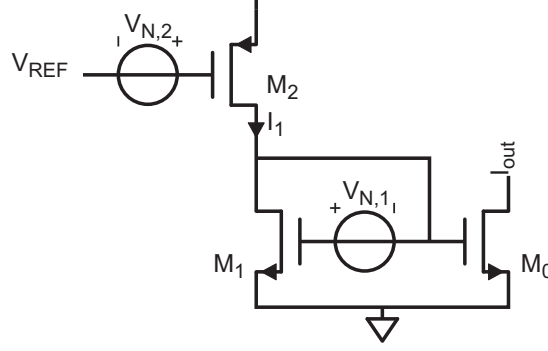
Figure 2.8: Current mirror noise analysis

The output noise as a function of the noise in transistor M_1 and M_2 is given in equation 2.21.

Transistor x current noise

$$i_{n,x}^2 = 4k_B T \gamma gm_x \tag{2.21}$$

the equivalent noise on the gate of M_0

$$V_{g,n,m0}^2 = \frac{i_{n,1}^2 + i_{n,2}^2}{gm_1^2} = 4k_B T \gamma \left(\frac{1}{gm_1} + \frac{gm_2}{gm_1^2}\right)$$

output noise current

$$i_{n,out}^2 = V_{g,n,m0}^2 gm_0^2 = 4k_B T \gamma gm_0 \left(\frac{gm_0}{gm_1} + \frac{gm_0 gm_2}{gm_1^2}\right)$$

with

$$gm_x = \frac{2I_{D,x}}{V_{GT,x}}$$

and

$$i_{n,0}^2 = 4k_B T \gamma gm_0$$

$$i_{n,out}^2 = i_{n,0}^2 \frac{I_{OUT}}{I_1}\left(1 + \frac{V_{GT1}}{V_{GT2}}\right)$$

To reduce the noise contribution of M_1 and M_2 the overdrive voltage of M_2 should be larger than the overdrive of M_1 and the current in M_1 should be larger than the output current.

2.4.3 Hold capacitor noise

If a transistor is biased with a switched holding capacitor (as shown in fig. 2.9), the noise on this capacitor transfers to the output. The noise on a switched
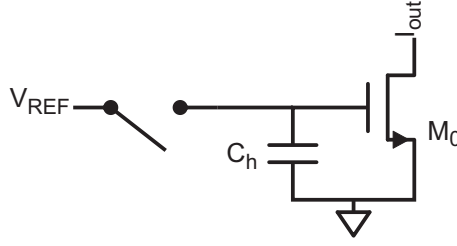
Figure 2.9: Hold capacitor noise contribution

capacitor can be described as shown in equation 2.22. Note that this noise is found in the Nyquist signal band.

$$v_{n,c}^2 = \frac{k_B T}{C_h} \tag{2.22}$$

the output noise

$$i_n^2 = v_{n,c}^2 gm^2 = \frac{k_B T}{C_h} \frac{4I_D^2}{V_{GT}^2}$$

with

$$I_D = \frac{I_M}{2^n - 1}$$

$$i_n^2 = v_{n,c}^2 gm^2 = \frac{k_B T}{C_h} \frac{4I_M^2}{(2^n - 1)^2 V_{GT}^2} \tag{2.23}$$

The total noise contribution of all current sources is the sum of the noise of all individual sources. The signal to noise ratio with respect to the noise contribution of the current source is shown in equation 2.24.

$$i_{n,total}^2 = (2^n - 1)i_n^2 = \frac{k_B T}{C_h} \frac{4I_M^2}{(2^n - 1)V_{GT}^2}$$

the signal power (differential output)

$$I_S^2 = \frac{I_M^2}{2}$$

signal-to-noise ratio

$$SNR_C = \frac{C_h(2^n - 1)V_{GT}^2}{8k_B T} \tag{2.24}$$

Usually, the signal-to-noise ratio is a system specification and the noise contribution of the hold capacitor needs to be low enough to meet this requirement. The required total hold capacitance is given by equation 2.25.

$$C_T = (2^n - 1)C_h = \frac{SNR8k_B T}{V_{GT}^2} \tag{2.25}$$

This shows that for a $81dB$ SNR system with $0.3V$ available overdrive the total required holding capacitance is $46pF$, for $0.2V$ overdrive this is $104pF$. For $87dB$ this is respectively $184pF$ and $415pF$ (note that for a differential setup only $2^n - 1$ hold capacitors are assumed, some switching circuitry should

thus connect the hold capacitor to the respective output transistor). It is seen that the required capacitance is quite substantial. In a 'normal' input signal voltage sampling system the signal-to-noise ratio is linear with $1/V_{IN}^2$ (for comparison shown in equation 2.26) in stead of $1/V_{GT}^2$ and is usually thus much lower.

$$v_n^2 = \frac{k_B T}{C_h}$$

the signal level (single ended)

$$v_s^2 = \frac{V_{PP}^2}{8}$$

signal-to-noise ratio

$$SNR_{C,norm} = \frac{V_{PP}^2 C_h}{8 k_B T}$$

from which the required capacitance follows:

$$C_h = \frac{SNR_{C,norm} 8 k_B T}{V_{PP}^2} \tag{2.26}$$

With a maximum peak-peak signal level of $1V$ a hold capacitor of $3.3pF$ is required, for $87dB$ this is $16.6pF$.

Intermediate stages

If there are intermediate stages present, as shown in fig. 2.10, the noise transfer of the holding capacitor may be reduced: if the total transconductance of the voltage on the input node (gate of M_2) to the output current is lower than the transconductance of the output device itself, a smaller hold capacitor can be used. This is shown in equation 2.27.
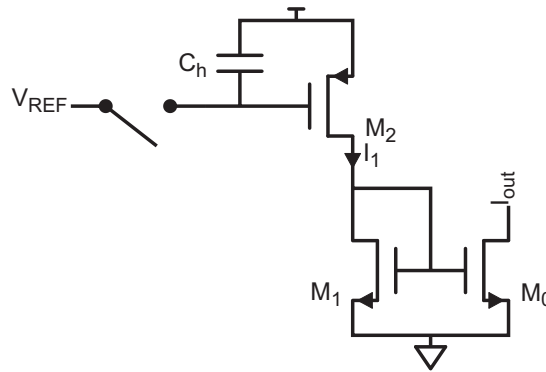
Figure 2.10: Hold capacitor noise contribution - intermediate stages

$$v_{n,c}^2 = \frac{k_B T}{C_h} \tag{2.27}$$

the noise contribution on the output

$$i_{n,out}^2 = v_{n,c}^2 \frac{gm_2^2}{gm_1^2} gm_0^2$$

with

$$gm_x = \frac{2I_{D,x}}{V_{GT,x}}$$

$$i_{n,out}^2 = \frac{k_B T}{C_h} \frac{4I_{OUT}^2}{V_{GT,2}^2}$$

with

$$I_{OUT}^2 = \frac{I_M^2}{(2^n - 1)^2}$$

$$i_{n,out}^2 = \frac{k_B T}{C_h} \frac{4I_M}{(2^n - 1)^2 V_{GT,2}^2}$$

In comparison with the result in equation 2.22 it is seen that the noise contribution of this holding capacitor can be much smaller (if $V_{GT,2}$ is chosen larger than $V_{GT,0}$), and thus the hold capacitor can be chosen smaller. The total output noise current

$$i_{n,out,total}^2 = i_{n,out}^2 (2^n - 1) = \frac{k_B T}{C_h} \frac{4I_M}{(2^n - 1)V_{GT,2}^2}$$

yielding a signal-to-noise ratio given by

$$SNR_{Ch,i} = \frac{C_h (2^n - 1)V_{GT,2}^2}{8k_B T I_M}$$

from which the total required capacitance follows:

$$C_h (2^n - 1) = C_T = \frac{SNR_{Ch,i} 8 k_B T I_M}{V_{GT,2}^2}$$

It is seen that the capacitance will be $\frac{V_{GT,2}^2}{V_{GT,0}^2}$ smaller than is shown in equation 2.26. This means that for the given conditions above and an overdrive voltage of $0.4V$ in stead of $0.2V$ the capacitor will be only $26pF$ ($SNR = 81dB$).

2.4.4   Switch (resistive) noise

If a transistor's bias is switched (see fig. 2.11), the switch ON resistance introduces noise to the output signal if it is closed. Since resistance voltage noise density is linear with $1/\sqrt{R}$, it can be expected that the noise will be lower if the switch size is increased (lowering R_{ON}). The minimum required switch resistance is evaluated in equation 2.28, with BW signal bandwidth of the converter, the thermal noise of switch resistance

$$v_n^2 = 4k_B T BW R_{SW} \tag{2.28}$$

the current noise at the output (when a source is turned ON)

$$i_n^2 = 4k_B T BW R_{SW} \frac{4I_D^2}{V_{GT}^2}$$

with I_M the maximum total single ended output current (all sources in a thermometer encoded D/A converter)

$$I_D = \frac{I_M}{2^n - 1}$$

with $(2^n - 1)$ sources that contribute noise to the output

$$i^2_{n,total} = 4k_B T BW R_{SW} \frac{4I_M^2}{(2^n - 1)V_{GT}^2}$$

output signal

$$I^2_{OUT} = \frac{I_M^2}{2}$$

the signal-to-noise ratio

$$SNR_R = \frac{(2^n - 1)V_{GT}^2}{32k_B T BW R_{SW}}$$

rewriting, the required switch resistance

$$R_{TS} = \frac{R_{SW}}{(2^n - 1)} = \frac{V_{GT}^2}{32k_B T BW SNR_R}$$

where R_{TS} is the *ON* resistance of all used switches in parallel; note that this is independent of the number of bits. With a signal bandwidth of $500MHz$, a signal to noise ratio of $81dB$ and an overdrive voltage of $0.2V$ the minimum (total) required switch resistance (R_{TS}) is 4.79Ω.

Note that a current source may be implemented with two sections, which are used alternatively. This way, a source is *ON* only for one period, which reduces inter-symbol interference. Although there will be frequency-translation of the noise, the output noise will be the same (noise is white).
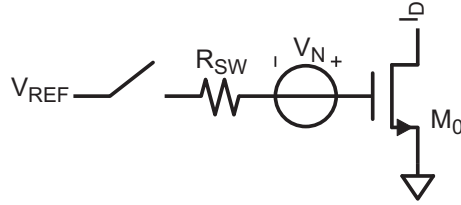
Figure 2.11: Switch noise contribution

Chapter 3

Conventional design approach

In conventional current-output D/A converters usually so-called current steering topologies are used. In this converter type, a current-source output is switched to either the negative or positive output node. The two differential pair MOS switches are driven by large clock-latched data signals as shown in figure 3.1. This chapter deals with *some* difficulties with these type of converters.

Difficulties in designing these type of data-converters are found in the timing of the inverted and non-inverted clock signal; if, for example, D and $!D$ are simultaneously high the outputs are shorted. In case both signals are low, the current source transistor will be set in triode and the current is low. Usually well-designed data-laches are used to overcome this problem.

Another issue with these type of converters is charge injection. When charge from the output is injected into the gate line of the cascode transistor (due to the cascode overlap capacitance) the reference voltage of the cascode device deviates proportional to the output signal. This voltage feeds to all other current sources which generate an error signal that causes distortion. Section 3.1 deals with this type of charge injection.

Another problem is found with output capacitance modulation. Each source in a current-steering D/A converter is switched to one of both outputs. This means that the (equivalent) output capacitance of the current source is also switched between nodes. This is described in section 3.2.

3.1 Distortion due to gate charge injection on cascode transistor

This section deals with distortion that is introduced due to charge injection from voltage disturbances on the drain node to the gate line. If the gate of the cascode transistor is common for all current sources in a thermometer coded D/A converter this disturbance spreads and may introduce significant distortion.

A single switched current cell is shown in fig. 3.1. It can be expected that there will be some interconnect resistance between the gate of the cascode device and the reference source (V_s). At each gate-node there is some (equivalent) capacitance to ground (C_F) which represents the gate-source (channel and overlap) capacitance of M_1 in series with the output capacitance of M_0

(overlap and junction capacitance). Note that the gate-source capacitance of M_1 will be much higher than the output capacitance of M_0 (and the settling time of the cascode is much smaller than the sample time, T_S), therefore C_F will be approximately equal to the output capacitance of M_0. C_P and R_P are the capacitances and interconnect resistance of all other current sources in parallel. It can be said thus that (due to symmetry) R_P and C_P are respectively $R_F/(2^n-2)$ and $C_F(2^n-2)$. An ideal voltage reference source is assumed with an output resistance R_S.

Figure 3.1: Gate charge injection - equivalent circuit

Due to the cascode drain-gate overlap capacitance, it can be expected that some charge is injected into the cascode gate reference circuit if the digital code of the section changes and the (differential) output voltage is not zero. The amount of charge injected is proportional to the differential output signal (the node is switched from one side to another). This causes a voltage disturbance on the cascode lines (V_P) of all other sources in the converter. Via the cascode transistor, this disturbance transfers to the drain of the current source transistor (M_0) and it leads to output current deviation (due to finite output resistance of M_0). This causes distortion.

The charge injection to the gate line of *one* source switching results in a voltage step on the gate node (V_L). This is shown in equation 3.1.

$$V_{step} = V_{step,out} \frac{C_{GD,1}}{C_{GD,1} + C_F} \tag{3.1}$$

This voltage step on the gate node of the cascode transistor leads to a voltage disturbance on the gate line of all *other* cascode transistors (node V_P). A simplified (small signal) schematic of the entire converter sis shown in fig. 3.2. The voltage disturbance on node V_P can be expressed as is shown in equation 3.2 (see appendix C).

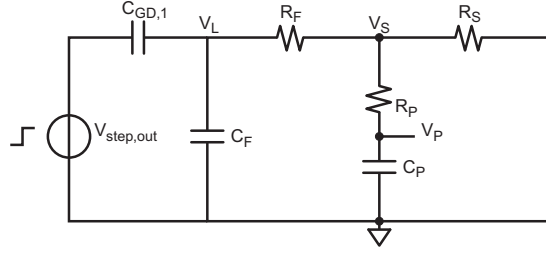$$V_P = A e^{\frac{t}{\tau_0}} + B e^{\frac{t}{\tau_1}} \tag{3.2}$$

Figure 3.2: Simplified small-signal equivalent of fig. 3.1

This voltage thus represents the disturbance on an other current source that shares the same cascode reference voltage. Assuming that the cascode settling time of the cascode transistor (M_1) is much smaller than the sample-period, this voltage transfers to the drain of the current source (M_0). The charge injected into the output node (in one sample-period) is approximately the integral of this voltage divided by the output resistance of the current source transistor, see equation 3.3.

$$Q_{OUT,s} = \int_0^{T_S} \frac{V_P}{R_{DS}} \, dt \tag{3.3}$$

Equation 3.3 thus gives the amount of charge injected into the output in *one* period by one source as *one* source switches. In other words, $Q_{OUT,s}$ gives the amount of charge injected in the output per volt output signal ($\sim D_{IN}$), per number of sources that are switched ($\sim \frac{\delta D_{IN}}{\delta T_S}$), per number of sources that are *ON* ($\sim D_{IN}$), per period.

Assuming a full-scale output signal, with frequency ω_0 the non-distorted output signal for the positive respectively the negative output node

$$V_P = I_M R_L \left(\frac{1}{2} + \frac{1}{2} \sin(\omega_0 t) \right)$$

and

$$V_N = I_M R_L \left(\frac{1}{2} - \frac{1}{2} \sin(\omega_0 t) \right)$$

leading to the differential output voltage

$$V_{OUT,0} = V_P - V_N = I_M R_L \sin(\omega_0 t) = \frac{2 I_M R_L}{NS} D_{IN}$$

with

$$D_{IN} = 0.5 NS \sin(\omega_0 t)$$

and

$$NS = 2^n - 1$$

The current I_M represents the summed (positive and negative) output current. In thermometer encoded D/A converters with sections as shown in fig. 3.1, where all sources are always *ON*, this I_M is constant. However, due to the signal dependent charge injection described above, this I_M is actually signal dependent:

$$I_M = \frac{Q_T}{T_S} = Q_T f s$$

$$Q_T = \frac{I_{NS}}{fs} + Q_{DS}$$

Where Q_T is the total amount of charge injected into the output (of all sources summed); Q_{DS} is the amount of charge injected due to signal disturbance on the cascode gate nodes and I_{NS} is the DC total output current. The charge injection Q_{DS} can be described as:

$$Q_{DS} = Q_{OUT,s}V_{OUT,0}\frac{\delta D_{IN}}{\delta t}\frac{1}{fs}NS \qquad (3.4)$$

Noting that

$$\frac{\delta D_{IN}}{\delta T_S} = \frac{\delta D_{IN}}{\delta t}\frac{\delta t}{\delta T_S} = \frac{\delta D_{IN}}{\delta t}\frac{1}{fs}$$

substituting 3.4 in 3.1 then gives the total current

$$
\begin{aligned}
I_M &= I_{NS} + Q_{OUT,s}V_{OUT,0}\frac{\delta D_{IN}}{\delta t}NS \\
&= I_{NS} + Q_{OUT,s}I_{NS}R_L\sin(\omega_0 t)\frac{1}{2}NS^2\omega_0\cos(\omega_0 t)
\end{aligned}
$$

and the total output signal:

$$V_{OUT} = I_{NS}R_L\sin(\omega_0 t)\left(1 + Q_{OUT,s}R_L\sin(\omega_0 t)\frac{1}{2}NS^2\omega_0\cos(\omega_0 t)\right)$$

This equation shows that there is third harmonic distortion in the output signal. The power at this frequency can be calculated by expanding the equation, see equation 3.5.

$$V_{OUT} = V_{OUT,0} + \frac{1}{2}R_L^2 I_{NS}NS^2 Q_{OUT,s}\omega_0\cos(\omega_0 t)\sin^2(\omega_0 t) \qquad (3.5)$$

$$V_{OUT} = V_{OUT,0} + \frac{1}{2}R_L^2 I_{NS}NS^2 Q_{OUT,s}\omega_0\cos(\omega_0 t)(\frac{1}{2} - \frac{1}{2}\cos(2\omega_0 t))$$

It is seen that there is some (small) signal at the fundamental frequency. Since only the third order harmonic power is of interest, this signal at the fundamental frequency is added to $V_{OUT,0}$ (resulting in $V_{OUT,1}$)

$$V_{OUT} = V_{OUT,1} - \frac{1}{4}R_L^2 I_{NS}NS^2 Q_{OUT,s}\omega_0\cos(\omega_0 t)\cos(2\omega_0 t)$$

$$V_{OUT} = V_{OUT,1} - \frac{1}{4}R_L^2 I_{NS}NS^2 Q_{OUT,s}\omega_0(\frac{1}{2}\cos(\omega_0 t) + \frac{1}{2}\cos(3\omega_0 t))$$

Also in this equation some signal at the add fundamental frequency is observed, this is also added to $V_{OUT,1}$ (resulting to $V_{OUT,2}$)

$$V_{OUT} = V_{OUT,2} - \frac{1}{8}R_L^2 I_{NS}NS^2 Q_{OUT,s}\omega_0\cos(3\omega_0 t)$$

the error signal power

$$P_{ERROR} = \frac{1}{2}(\frac{1}{8}R_L^2 I_{NS}NS^2 Q_{OUT,s}\omega_0)^2$$

and the $SFDR_{dB}$

$$
\begin{aligned}
SFDR_{dB} &= 10 \log \frac{P_{SIGNAL}}{P_{ERROR}} \\
&= 20 \log \left(\frac{I_{NS} R_L}{\frac{1}{8} R_L^2 I_{NS} N S^2 Q_{OUT,s} \omega_0} \right) \\
&= 20 \log \left(\frac{1}{\frac{1}{8} R_L N S^2 Q_{OUT,s} \omega_0} \right)
\end{aligned}
\tag{3.6}
$$

3.1.1 Design example

When thermometer encoded D/A converter current sources are matched using device size matching, the current source MOST must be $W_1/L_1 = 10.71/3.48$ (see section 2.2.1). To increase the output impedance to higher than the minimum required DC resistance the cascode transistor should have a gain larger than $Mu = 85$. With an overdrive voltage of $0.1V$ this means that the cascode transistor should be $W_2/L_2 = 14.32/1.3$ (see section 2.3). The feedback capacitance of the cascode transistor is then $C_{GDO,o} = 2.431 fF$. Assuming a source impedance of $R_S = 50\Omega$ and resistance of $R_F = 10\Omega$ the total charge injected into the gate line of the cascode is $Q_{OUT,s} = 0.2156 aC/V/Code^2/Period$. Note that 'Code' represents the digital input code of the D/A converter.

Substituting this into equation 3.6 yields the result shown in fig. 3.3 (with $n = 10$, $I_{NS} = 10mA$, $R_L = 50\Omega$ and $\omega_0 = 10MHz..1GHz$. It is seen in the figure that the SFDR decreases significantly with operating frequency. Note that due to the predictability of this distortion a (digital) pre-distortion filter may be used to partly compensate for this. Due to batch-to-batch mismatch this will be limited though.

Note that the cascode transistor was sized to reduce the effective output capacitance of the current source MOST. In the given situation (see fig. 3.1), however, it is better to optimize to low total output capacitance (including the capacitance of the cascode MOST as well). In this case, the cascode transistor will be significantly smaller (see section 2.3).

3.2 Distortion due to non-linear output capacitance

In section 2.1 non-linearity due to output resistance variation was described. In this section, the same will be done for output capacitance variation. In both thermometer coded and binary weighted D/A converters it can be expected that the output capacitance on a single output of the D/A converter increases for higher output currents. This is because for current-steering D/A converter the output of a current source (and thus it's capacitance) is switched between outputs. If a current source is modulated (instead of switched between outputs) the output capacitance may vary itself. In either case, for each source in a thermometer encoded converter, there will be a *low* capacitance connected to the positive output if the signal is LOW and a *high* capacitance if the signal is $HIGH$. On the negative output it is the other way around. For a single channel (i.e. only positive output), this is shown in fig. 3.4.

In the figure, capacitance $C_a(D)$ depends on the digital input code (and thus the output signal) and C_0 is constant. Assuming each current source adds
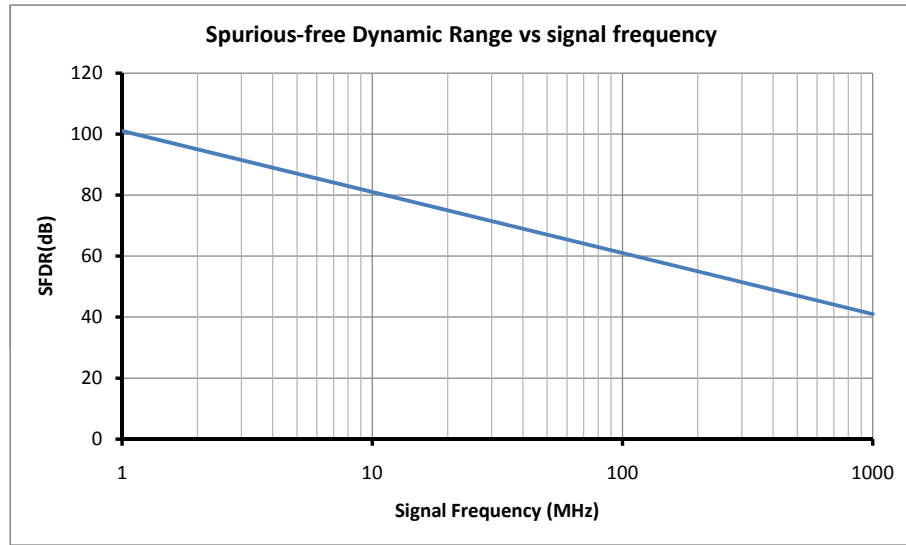
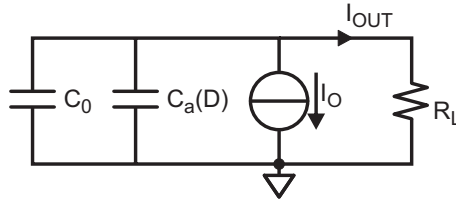Figure 3.3: Spurious free dynamic range - third harmonic distortion due to cascode gate charge injection

Figure 3.4: Output capacitance modulation - simplified model

C_u of additional capacitance to the output, $C_a(D)$ can be written as is shown in equation 3.7.

$$C_a(D) = \frac{I_O}{I_M}(2^n - 1)C_u \tag{3.7}$$

where I_M is the maximum single channel output current and I_{OUT} is the (code dependent) output current.

With this capacitance variation it can be expected that less charge is injected into the load in an *lsb* step at high output current on a single channel in comparison with when the output current is low; with high output current the capacitance is high as well, and more charge is stored in this capacitance. It has to be stated that this 'charge storage' variation is linear with the output current. This means that the error signal would be linear with the output signal, and thus only second harmonic distortion is observed. To evaluate the quantity of this error, the total output charge that is injected into the output

in one period is evaluated (equation 3.8).

$$Q_{OUT} = \int_0^{T_s} I_{OUT}\,dt = \frac{1}{R_L}\int_0^{T_s} V_{OUT}(t)\,dt \qquad (3.8)$$

$$V_{OUT}(t) = V_e - V_s e^{-\frac{t}{R_L C}}$$

with V_e the *end* voltage and V_s the *step* voltage (in one period) of the transient signal and where $C = C_0 + C_a$

$$V_{OUT}(t) = V_b + V_s - V_s e^{-\frac{t}{R_L C}} = V_b + V_s(1 + e^{-\frac{t}{R_L C}})$$

with V_b the *beginning* voltage of the transient signal

$$Q_{OUT} = \frac{1}{R_L}\int_0^{T_s} V_{OUT}(t)\,dt = \frac{V_b + V_s}{R_L}T_s - V_s C(1 - e^{-\frac{T_s}{R_L C}})$$

where $\frac{V_b + V_s}{R_L} = I_O$

Usually the settling time of the output network is smaller than the period time. Therefore this equation reduces to the following

$$Q_{OUT} = I_O T_s - V_s C$$

with

$$V_s = (I_O((n+1)T_s) - I_O(nT_s))R_L \approx \frac{\delta I_O}{\delta t}T_s R_L$$

where $I_O(nT_s)$ is this sample's current and $I_O((n+1)T_s)$ is the current at the next sample. Then, the average output current in a single period

$$I_{OUT} = \frac{Q_{OUT}}{T_s} = I_O - \frac{\delta I_O}{\delta t}R_L(C_0 + C_u\frac{I_O}{I_M}(2^n - 1))$$

In this equation, it is seen that there is a squared component - the derivative of I_O and I_O in C_a. Because there are no higher order components in the equation, it would be expected that third and higher order harmonic distortion is not present in the signal. The power of this error signal, and the signal-to-distortion ratio is given in equation 3.9.

The error signal:

$$D_{2,0} = \frac{\delta I_O}{\delta t}\tau_u\frac{I_O}{I_M}(2^n - 1) \qquad (3.9)$$

with $\tau_u = R_L C_u$, assuming a sinusoidal full-scale output signal

$$I_O = \frac{I_M}{2} + \frac{I_M}{2}sin(\omega_0 t)$$

$$D_{2,0} = \frac{\omega_0 I_M}{2}cos(\omega_0 t)\tau_u(\frac{1}{2} + \frac{1}{2}sin(\omega_0 t))(2^n - 1)$$

Note that there is some power at the fundamental frequency in the previous. The second harmonic distortion signal

$$D_2 = \frac{\omega_0 I_M}{2}cos(\omega_0 t)\tau_u\frac{1}{2}sin(\omega_0 t)(2^n - 1)$$

$$D_2 = \frac{1}{8}\omega_0 I_M \tau_u sin(2\omega_0 t)(2^n - 1)$$

with signal amplitude

$$A_2 = \frac{1}{8}\omega_0 I_M \tau_u (2^n - 1)$$

The signal level at the fundamental frequency is

$$A_1 = \frac{I_M}{2}$$

and the signal-to-distortion ratio is

$$SND_2 = \frac{A_1}{A_2} = \frac{1}{\frac{1}{4}\omega_0 \tau_u (2^n - 1)}$$

in dB

$$SND_{2,dB} = -20\log_{10}(\frac{1}{4}\omega_0 \tau_u (2^n - 1)) = -20\log_{10}(\frac{\pi}{2}f_{in}\tau_u (2^n - 1)) \quad (3.10)$$

In a differential setup, the second channel will have a symmetrical signal

$$I_O = \frac{I_M}{2} - \frac{I_M}{2}sin(\omega_0 t)$$

This leads to the same harmonic error signal, and therefore this signal will not be present at the differential output. In practice however, the output symmetry and thus the common-mode rejection (CMR) will be limited. In that case, the distortion is reduced by CMR (see equation 3.11), where CMR represents the channel matching (V_{CM}/V_{OUT}).

$$SND_{2,Diff,dB} = -20\log_{10}(\frac{\pi}{2}f_{in}\tau_u (2^n - 1)) + 20\log_{10}(CMR) \quad (3.11)$$

Note that this analysis assumes that it is irrellevant what the shape of the errorsignal is in a cycle; it assumes it is only relevant how much error energy there *is* in a cycle. In practice, however, there is a small effect that introduces some higher order harmonic distortion due to the shape of the error signal. Using PWM theory[3], this is evaluated to what is shown in equation 3.12.

n-th harmonic signal strength

$$D_n = 2^{N-1}J_{n-1}(2\pi f_{in}\tau_u 2^{N-1})\frac{sin(\pi f_{in}nT_s)}{\pi f_{in}nT_s} \quad (3.12)$$

where $J_p(x)$ is the p-th order Bessel function of the first kind. Note that for small x ($x << 1$) the Bessel function can be simplified by 1, $x/2$, $x^2/8$ and $x^3/48$ for respectively the zeroth, first, second and third order. With these assumptions, and for low frequencies, the signal-to-distortion ratios are given in equation 3.13, which is the same result as shown in equation 3.10.

$$SND_2 = \frac{1}{\frac{\pi}{2}f_{in}\tau_u 2^n} \quad (3.13)$$

and the third order distortion

$$SND_3 = \frac{1}{2(\frac{\pi}{2}f_{in}\tau_u 2^n)^2} = \frac{1}{2}SND_2^2$$

In a differential circuit, the third harmonic distortion is relevant when it exceeds the residue of the second order harmonic distortion. This is shown in equation 3.14

$$SND_{2,Diff} < SND_3 = \frac{1}{2}SND_2^2 \qquad (3.14)$$

$$SND_{2,Diff} = SND_2 CMR$$

$$\frac{1}{2}SND_2^2 > SND_2 CMR \rightarrow SND_2 > 2CMR$$

the output distortion level is then

$$SND_3 = SND_{2,Diff} = \frac{1}{2}CMR^2$$

This means that if the third and second order harmonic distortion levels are equal *at the output*, then the distortion level will be the square of the common mode rejection. In a well-balanced system, the common-mode rejection may be as high as $35dB$. In this case the distortion will be $64dB$ at a frequency where the third and second harmonic distortion are equal. Reasoning this the other way around: if a distortion ratio higher than $64dB$ is required, and the common mode rejection is no more than $35dB$, only second order harmonic distortion is relevant. Note that for a $35dB$ channel matching, the load resistances must match within 0.6% (three sigma yield).

Chapter 4

Solution exploration

It was seen in chapter 2 and 3 that if good performance (i.e. high LF linearity & noise) is required, large device sizes limit high-frequency performance (distortion). A solution to this problem may be found in meeting the current mismatch requirements elsewhere. A possible implementation may be using switched compensated biasing of current sources; relatively small output transistors will be used that each have a specific (trimmed) bias voltage that it stored on a hold-capacitor. This way, by measuring and compensating, all current sources in a thermometer encoded D/A converter will have equal currents.

It must be noted that with this type of biasing only switched current sources can be driven. Using hold capacitors, there is no DC reference; this means that a current source can only be *ON* for one period. If, for example, in a thermometer encoded D/A converter, a current source is *ON* during many clock-cycle, hold-capacitor droop will cause an error (i.e. the amount of charge injected into the output differs from one period to another). Also, when a current source is *ON* for two consecutive periods, the average current will be higher than if it is *ON* only one cycle due to the fact that switching edges are finite; a source that switches *ON* and *OFF* in one period carries less current to the output than a source that is only switched *ON* in one period and stays *ON* for two periods (inter-symbol interference).

For these reasons, it is only possible to use this type of switched current sources only one in two periods, and twice as many current-sources are required to able drive output currents each period.

This chapter deals with some switched current source implementations that can (digitally) be trimmed.

4.1 Direct switched biasing

An example of a switched bias network is shown in fig. 4.1. In this circuit a transistor (M_0) is biased with a hold capacitor (C_h). This hold capacitor is first connected to a reference voltage and the hold capacitor voltage settles (at this time the gate voltage of transistor M_0 is low, T_2 is closed). After it is disconnected from the reference, a small amount of charge is injected by current source I_{PULSE}. The charge that is injected compensates the error that is caused by the mismatch of the reference transistor M_1 and transistor M_0. Finally, the hold capacitor is connected to transistor M_0 and it is used as a

bias reference. With this scheme the output current is trimmed by I_{PULSE} and the mismatch of the sources can be compensated. Note that I_{PULSE} may be an actual current source transistor that is switched *ON* for a variable amount of time, or it is a charge redistribution network that injects some (variable amount of) charge onto capacitor C_h.
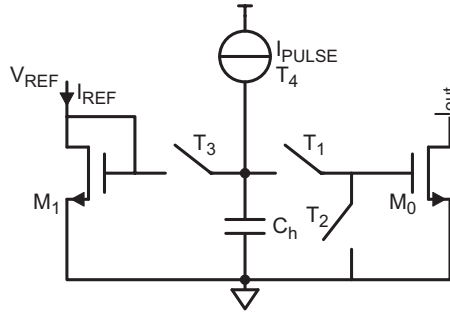

Figure 4.1: Current source bias with hold capacitance

In section 2.4.3 the noise contribution of a hold capacitor bias network is evaluated. It is seen there that for low noise contribution the hold capacitance needs to be quite large. This is a significant disadvantage of this topology; due to fast settling requirements the voltage reference needs to have a very low output resistance and the switch needs to be very large. Therefore, it is beneficial to investigate possibilities which require a smaller hold capacitor.

4.2 Mirrored switched biasing

An example of a circuit that requires a smaller hold capacitance is shown in fig. 4.2. In this circuit, the output current is a copy of a switched reference current. This current is generated using a P-type transistor with a switched bias network (M_2). When the current ratio I_{M_1}/I_{OUT} and overdrive ratio $V_{GT,2}/V_{GT,0}$ is chosen greater than one the requirements of the hold capacitor relaxes. This is shown in section 2.4.3. The switching mechanism is comparable to that of the circuit in fig. 4.1; the hold capacitor is connected to the reference, a small amount of charge is added to compensate for mismatch and is then used to bias the output transistor.

A drawback of this circuit however is that the fall time of the voltage on the gate of M_0 will be very high; when the current in M_1 is low, the output resistance of it ($1/gm$ of M_1) increases, which leads to a high fall time. It is thus difficult to make this circuit operate fast.

Mirrored switched biasing - low output resistance reference

The circuit shown in fig. 4.3 uses a reference voltage that is always *ON* and therefore has low resistance at all times. In this case the voltage on the gate of M_0 is switched between ground and this reference.

A problem with this circuit is that V_{REF} is referenced to the supply voltage. This means that the output resistance of M_2 must be very high for a high supply rejection ratio. In practice this means that a cascode transistor is required.
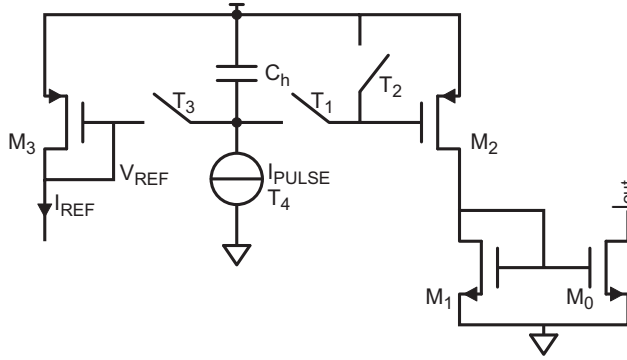
Figure 4.2: Current source with mirrored hold capacitance bias - low hold capacitance
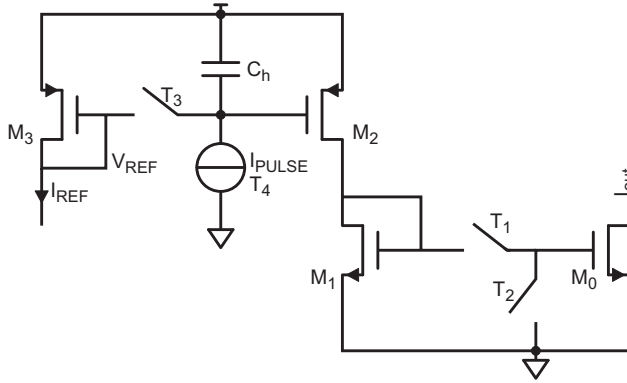

Figure 4.3: Current source with mirrored hold capacitance bias - low falltime

This contradicts with the high overdrive voltage that is required for a low hold capacitor.

4.3 Direct switched biasing - coarse and fine

The circuit in fig. 4.4 separates the trimming current from the coarse current. In this case the current source which is biased with a hold capacitor is much smaller and carries much less current. The noise voltage generated by the hold capacitor thus has a smaller transfer to the output (gm of M_1). It is easily understood that the hold capacitor can be N^2 times smaller than what is shown in fig. 4.1 if the ratio of the transistors W_{M_1} and $W_{M_1} + W_{M_0}$ is N. This is shown in equation 4.1 (see appendix E.1).

$$C_T = (2^n - 1)C_h = \frac{8SNRk_BTN^2}{V_{GT,1}^2} \tag{4.1}$$

The choice of N depends on the required trim range, and thus on the mismatch of the output device and the reference voltage. Assuming low reference
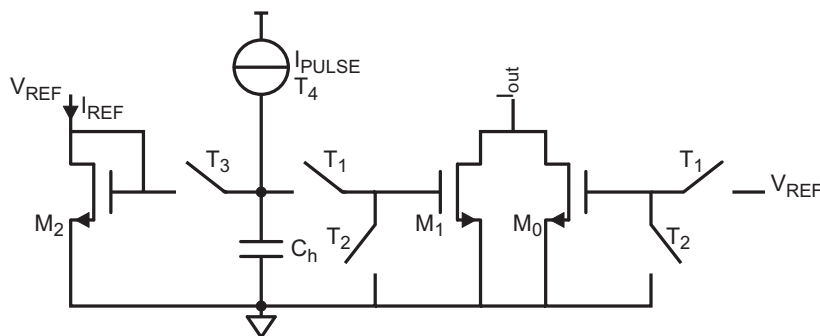
Figure 4.4: Dual current source - coarse and trim

mismatch, the value of N is evaluated in equation 4.2 (see appendix E.2).

$$N > \frac{\alpha \sigma_{i_T}}{I_{OUT}} = \alpha \frac{A_{VT}}{\sqrt{W_T L}} \frac{2}{V_{GT}} \tag{4.2}$$

where α is the trim range (usually 3) and σ_{i_T} is the current variance. Substituting this result into 4.1 yields the required hold capacitor

$$C_T = \frac{32 k_B T \alpha^2 A_{VT}^2 SNR}{V_{GT}^4 W_T L}$$

With a width of $1.075 \mu m$, a length of $0.3 \mu m$ (meeting DC requirements, section 2.1), an overdrive voltage of $0.2V$ and $\alpha = 3$ (see also appendix A), $3.7pF$ of total capacitance is required at a signal-to-noise ratio of $80dB$ ($\approx 13b$).

A problem with this implementation is that when the output transistor is switched ON and entirely OFF that a lot of charge is accumulated in the channel of the device. With such a large gate voltage swing, it can also be expected that a residue of the edges will be present on the output node (capacitively coupled). This leads to a highly peaking transient response; when the transistor is turned on, charge is accumulated and a positive current is flowing out of the device. This will also be the case with the cascode device; since the peaking is dependent on the output voltage, this may lead to distortion and is therefore unwanted. To obtain low distortion, it is necessary that the charge injected into the output is constant over output voltage.

A result of a transient simulation is shown in figure 4.5. The setup is a cascoded current source (with transistor dimensions and biasing as described in section 2.1). In the figure the turn ON edge of the output current is seen. During the first $30ps$ of the simulation the current source is turned ON (input risetime is $30ps$). It is seen in the figure that the output current varies with the DC output voltage. Figure 4.6 shows the relative (to total output charge in one cycle) output charge due to this effect. It is seen there, that especially for low output voltages the total charge is not constant. Note that at the lowest output voltage the drain-source voltage of the cascode transistor is still $200mV$ ($V_{GT} = 100mV$). From the figure, it can be seen that if low distortion is required, the output voltage should not be lower than approximately $650mV$. This substantially reduces the output swing. Figure 4.7 shows the resulting distortion if this charge error is present. If the output voltage on each channel

(in a differential setup) varies from $0.5V$ to $0.8V$ the third harmonic will be found at approximately $-60dBc$. Note that this distortion is independent of output frequency; the output charge differs as a function of the output *voltage*, and is thus equal for all frequencies.
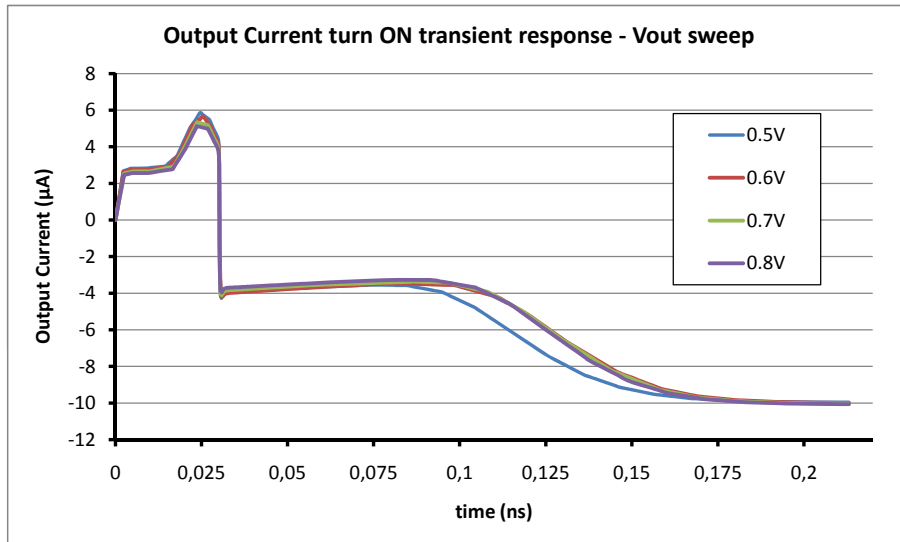

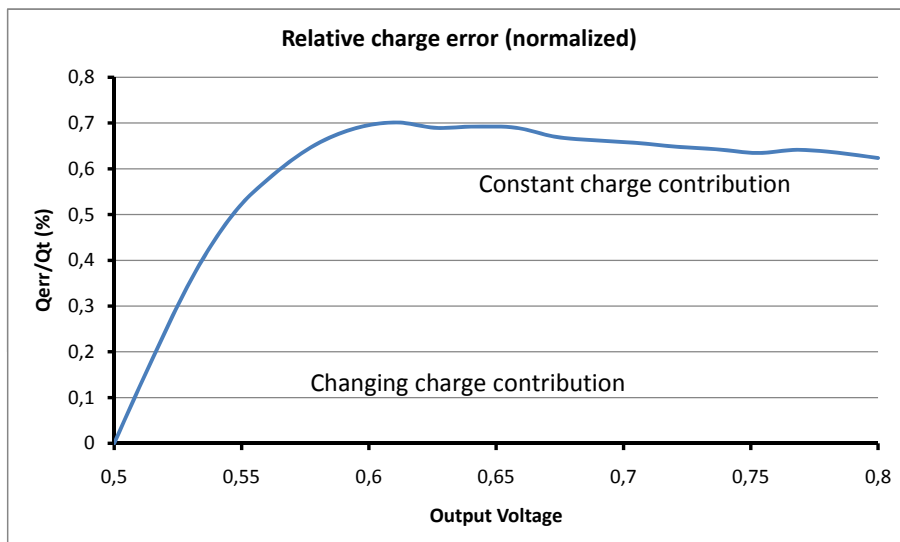Figure 4.5: Output current peaking - channel charge

Figure 4.6: Relative output charge error (%) versus output (drain) voltage

Another issue with direct switching topologies is cascode voltage settling. If a current source is switched OFF the voltage on the cascode source node
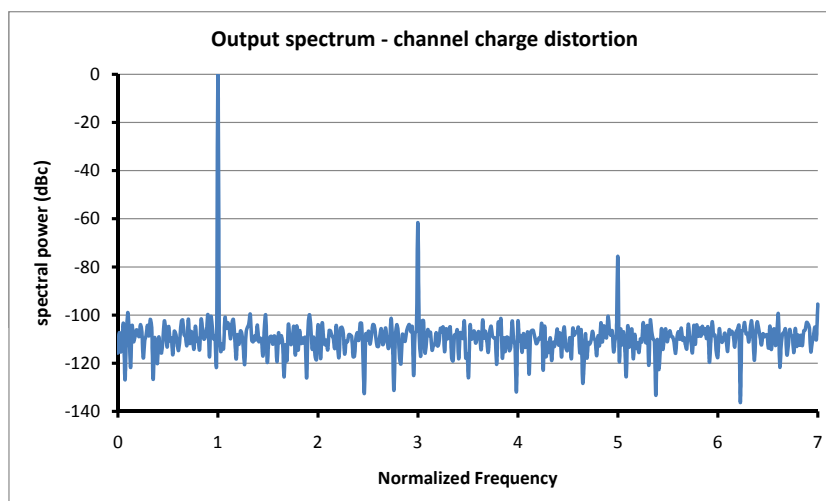
Figure 4.7: Distortion due to channel charge accumulation

will rise quite slowly. This is because the gm of the transistor decreases when the transistor is turned off. With (parasitic) capacitance on the node, RC settling is very slow. It can be expected that the total output charge at the next cycle depends on how much the voltage is settling. This in turn will lead to inter-symbol interference, and thus, distortion.

4.4 'soft' switching current source

A solution to channel charge accumulation is not turning the transistor entirely OFF, but to keep the gate just above the threshold voltage. Since a lot of charge is accumulated below the threshold voltage, channel charge accumulation will be much smaller if the device is not switched OFF entirely. The current peak will thus be significantly smaller if the device is not switched entirely OFF but instead is switched to a LOW current. In fig. 4.8 an implementation of this 'soft' switching current source is shown. During operation, the gate voltage is now switched to the reference voltage to generate a 'high' current (ON). The voltage on the gate of M_0 is lowered by a charge redistribution network (C_r) to generate a LOW current. Given correct switch timing, a 'fixed' amount of charge is then subtracted from the 'hold' capacitor (C_h). When the capacitor ratio is chosen correctly, the voltage will drop from the reference voltage to just above the threshold voltage. Note that the hold capacitor has to be disconnected from the reference first (switch open) before the charge is redistributed on the up and downgoing edge.

A nice property of this circuit is that the same amount of charge is subtracted from the capacitor C_h as there is added. This means that the voltage on the gate node (given correct switch-timing) will rise and fall to exactly the correct voltages. The switch is then only required for DC transfer and to improve noise performance, of which the latter will be determining the switch size.
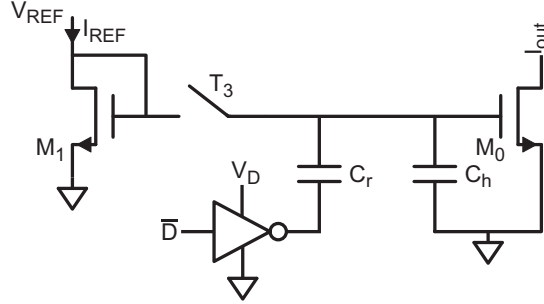
Figure 4.8: Trim the low-level current of the current source

When the switch is opened, the transfer of the output of the inverter to the gate-node is easily evaluated (see equation 4.3). When D transits from 'high' to 'low' the gate voltage of M_0 drops with the respective capacitive ratio. A transition from 'low' to 'high' restores the previous situation. Note that it is important that the voltage step on the the output of the inverter (the capacitor redistribution driving signal) is very stable. This means that the voltage V_D needs to be very constant; any signal dependency leads to distortion of the output signal. To ensure on high supply rejection ratio, it may be useful to use a separate reference voltage to drive the inverter.

$$V_{GS,0} = -\frac{C_r}{C_r + C_h} V_D \overline{D(t)} + V_{REF} \qquad (4.3)$$

where V_D is the output voltage of the inverter and $D(t)$ the digital input signal of a single cell.

Another nice property of this circuit is that C_r can be used to trim the output current. By separating this capacitor in a (binary weighted) bank of capacitances, a configurable amount of charge can be added or subtracted from the 'hold' capacitor (see figure 4.9). In this case the LOW current is trimmed and the ON current is fixed. It is not relevant what the average current level is; a certain amount of *excess* charge needs to be injected into the output if the given bit is high.

The effective output current (I_{OUT}) of a single section is $I_{HIGH} - I_{LOW}$, where I_{HIGH} is the 'high' current (ON) and I_{LOW} is the 'low' current (LOW). The 'effective' output current is shown in equation 4.4 (see appendix D.1).

$$I_{OUT} = \frac{1}{2}k\frac{W}{L}V_D H(2(V_{REF} - V_{TH}) - V_D H) \qquad (4.4)$$

where H is the (trim dependant) voltage transfer of the reference voltage V_D to the gate of transistor M_0.

It is thus the 'effective' output current that is trimmed ($I_{HIGH} - I_{LOW}$) by varying I_{LOW}. If, for example, the effective output current is too low, some additional capacitance is used to inject charge into the hold capacitor (C_h). This increases the voltage swing on the gate of M_0. Since the $HIGH$ voltage is equal to the reference voltage (V_{REF}) the LOW voltage decreases.

In the next subsections the circuit is further evaluated. First the (dynamic) bias conditions are evaluated. This section shows how the 'low' and 'high'
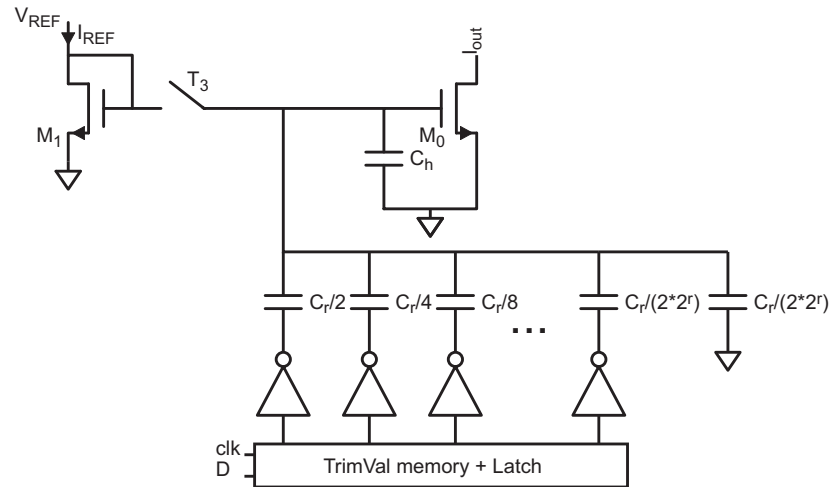
Figure 4.9: Segmented charge redistribution capacitor - trim output *LOW* current

gate voltage should be chosen. In section 4.4.2 the trimming mechanism is considered with its trim capacitances. Section 4.4.3 deals with the noise contribution of the hold capacitor and output transistor. The section concludes with a design example.

4.4.1   (Dynamic) bias conditions

In this section the bias conditions are evaluated. To be able to 'trim' the circuit, it is necessary that the *LOW* current is higher than the required trim range if the circuit must be able to trim two ways. Note that it is not strictly necessary to be able to trim two ways in a differential converter; it is required that the differential error is *low*. If, for example, there is a positive error in the differential output, the negative output's current should be increased. A major drawback of this one-way trimming mechanism is however is that the gain of the individual channels differs significantly. This means that when there is second order distortion in the output signal (which in the ideal case is common-mode) it will not entirely be canceled. The circuit will thus be trimmed in two directions; if the differential error is positive, the positive output current is decreased and the negative is increased.

Fig. 4.10 shows a simplified circuit of the soft-switching implementation. In the figure, the the trimming capacitors are modeled as a linear equivalent capacitance of which the value depends on the trim value (DT, ranging from 0 to 1). An offset voltage (V_{OS}) is included to represent mismatch of various devices/references. Note that there is a 'nominal' capacitor $C_{r,0}$ that switches the gate to the desired voltage levels if no mismatch is present. Since the voltage on the gate node of M_0 needs to have a large step with small variation it is beneficial to have a 'nominal' capacitance which is slightly modulated. Choosing capacitor $C_r(DT)$ enables a 'fine' trim of the gate voltage swing.

The 'effective' output current, of a circuit that includes device mismatch,
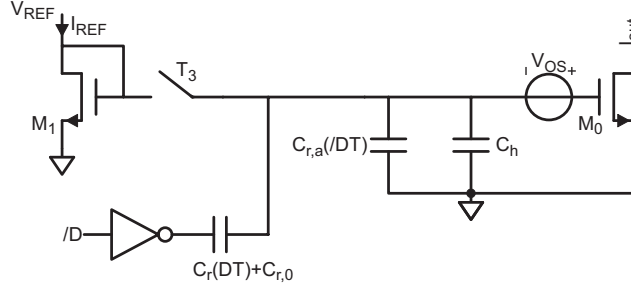
Figure 4.10: Simplified 'soft' switching topology

is shown in equation 4.5 (see appendix D.2).

$$I_{OUT} = \frac{1}{2}k\frac{W}{L}V_D H(2(V_{REF} + V_{OS} - V_{TH}) - V_D H) \tag{4.5}$$

where

$$H = \frac{C_r(DT) + C_{r,0}}{C_c}$$

with

$$C_r = C_r(DT) + C_{r,a}(\overline{DT})$$

and

$$C_c = C_r + C_{r,0} + C_h$$

Trim range

Equation 4.4 gives the output current as a function of an offset voltage in the gate line. Device mismatch can be modeled as such a source. By differentiating to V_{OS} the transfer of mismatch to the output current can be evaluated. The current range that has to be trimmed is then

$$I_{TRIM} = \frac{\delta I_{OUT}}{\delta V_{OS}}\alpha\sigma_{V_{TH}} = k\frac{W}{L}V_D H\alpha\sigma_{V_{TH}} \tag{4.6}$$

where α is the required matching criteria (usually 3)

Bias conditions

To be able to trim the current source the LOW current needs to be higher than the trim-range; if, in a given section, the output current (I_{OUT}) is too 'low', the LOW current needs to be reduced to compensate. This implicitly sets the 'nominal' conditions for the circuit: at ON current the gate voltage is V_{REF} and it needs to be lowered such that the LOW current is nominally I_{TRIM} or larger (see figure 4.11). Since the LOW current cannot be reduced further than zero, it needs to be larger than I_{TRIM} to guarantee sufficient trimming range.

The nominal transfer determines the 'nominal' capacitance that is required; at half of the full-scale trimming range, the transfer should be equal to H_0. The nominal transfer H_0 is given in equation 4.7 (see appendix D.3). The nominal
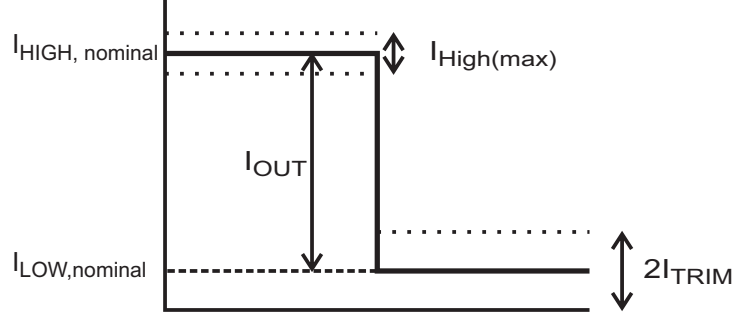
Figure 4.11: Output current error and trim range

capacitance value should thus be chosen such that the condition in equation 4.8 is met.

$$H_0 = \frac{V_{GT,H} \pm \sqrt{2V_{GT,H}\alpha\sigma_{VTH}}}{V_D} = \frac{V_{G,PP}}{V_D} \tag{4.7}$$

where $V_{G,PP}$ is the peak-peak gate voltage swing.

$$\frac{C_r(0.5) + C_{r,0}}{C_r(0.5) + C_h} = H_0 \tag{4.8}$$

The current ratio is given by equation 4.9.

$$R = \frac{I_{HIGH}}{I_{LOW}} = \frac{V_{GT,H}^2}{V_{GT,L}^2} = \frac{V_{GT,H}^2}{(V_{GT,H} - V_{G,PP})^2} \tag{4.9}$$

which reduces to (see equation 4.7)

$$R = \frac{V_{GT,H}}{2\alpha\sigma_{VTH}}$$

If the high overdrive-voltage is $0.2V$, $\sigma_{VTH} = 7.3mV$, $V_D = 0.7V (= V_{REF})$ and $\alpha = 3$ then the nominal transfer needs to be 0.1520 ($V_{G,PP} = 106mV$). The current ratio is approximately 4, which is quite low (noise performance, see section 4.4.3).

4.4.2   Trim

In this section the requirements of the trim capacitors are determined. To be able to trim the error current described in equation 4.6, a certain minimum trim range is required. Furthermore, a maximum trim step (i.e. how many bits are needed to trim the circuit) needs to be determined; this defines the accuracy of the post-trim output signal.

First the the trim sensitivity, i.e. the output current change as a function of trim value change, is evaluated. The sensitivity is defined as $S = \frac{\delta I_{OUT}}{\delta DT}$, where DT is the (digital) trim value. This is required to determine the capacitance range and trim accuracy (LSB capacitance change), given a maximum output current error and a required (current) trim step.

Trim sensitivity

There are two ways to drive the trim-capacitors; with a single edge or with double edges. In the first case, if the signal swing on the gate of M_0 needs to be smaller (lowering the output effective current), a capacitor is connected to ground in stead of the driving signal (D). In this case this capacitor adds to the hold capacitor. In the second case the inverted signal of D is used as well; if the signal swing on the gate needs to be lowered, some capacitance is connected to the inverted driving signal. An advantage of the latter is that with the same capacitance the trim step is twice as high and thus less trim capacitance is required.

A disadvantage of the latter is, however, that a reference signal, V_D, is required that needs to be stable *at all times*. When during a certain period the output level of a current source is *LOW*, there is a (capacitively dividing) transfer network from the reference signal of the capacitor driver (V_D) to the gate of M_0. In the first case, when the current is *LOW*, *ALL* capacitors are connected to ground. Since the gate voltage is referenced to (the local) ground there is no transfer path from any reference to the gate.

For double edge driving and single edge driving the sensitivity is shown respectively in equation 4.10 and 4.11 (see appendix D.4).

$$S_{T,1} = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_D - 2V_D^2 H_0)\frac{2C_{r,T}}{C_c} \tag{4.10}$$

$$S_{T,2} = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_D - 2V_D^2 H_0)\frac{C_{r,T}}{C_c} = \frac{1}{2}S_{T,1} \tag{4.11}$$

Trim capacitance value - trim range

With the sensitivity and the required trimming range evaluated in the previous sections, the size of the trim capacitor can be determined. This is shown in equation 4.12 to 4.14. Note that the result in equation 4.13 uses a small-signal assumption; at the nominal conditions a sensitivity is determined and extrapolated to zero current. In the second case (equation 4.14) the assumption is made that $V_{GT,L}$ needs to be able to be trimmed to zero (large signal). The second case will thus yield a slightly higher capacitance.

$$S_{T,x}\frac{DT_{MAX}}{2} > \Delta I_{OUT} = \alpha\sigma_i = \alpha k\frac{W}{L}V_D H_0 \sigma_{V_{TH}} \tag{4.12}$$

with $DT_{MAX} = 1$ a requirement for the sensitivity is found

$$S_{T,x} > 2\alpha k\frac{W}{L}V_D H_0 \sigma_{V_{TH}}$$

$$S_{T,2} = \frac{1}{2}S_{T,1} = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_D - 2V_D^2 H_0)\frac{C_{r,T}}{C_c}$$

thus

$$(V_{GT,H}V_D - V_D^2 H_0)\frac{C_{r,T}}{C_c} = 2\alpha V_D H_0 \sigma_{V_{TH}}$$

rewriting

$$\frac{C_{r,T}}{C_c} = \frac{2\alpha H_0 \sigma_{V_{TH}}}{V_{GT,H} - V_D H_0} = \frac{2\alpha H_0 \sigma_{V_{TH}}}{V_{GT,L}} \tag{4.13}$$

with the LOW current criteria in equation 4.7

$$V_{GT,L}^2 > 2\alpha H_0 \sigma_{V_{TH}} V_D$$

this reduces to

$$\frac{C_{r,T}}{C_c} = \frac{V_{GT,L}}{V_D} \tag{4.14}$$

With the conditions given in the previous example, the capacitor ratio $C_{r,T}/C_c$ should exceed $71.12 \cdot 10^{-3}$.

Trim accuracy - trim step

In this section the required LSB capacitor size is determined to achieve low integral non-linearity (INL). The INL of a thermometer coded D/A converter is evaluated in section 2.2.1 (equation 4.15).

$$INL_{max,LSB} = \frac{1}{2} \frac{2^{nr} - 1}{\sqrt{2^n - 1}} \frac{\sigma_i}{\Delta I} \tag{4.15}$$

where, nr is the number of bits of the total converter (MSB and LSB section), ΔI the output current of a single section ($I_{HIGH} - I_{LOW}$) and σ_i the after-trim error residue.

The smallest (LSB) voltage step on the gate node of M_0 should be smaller than the the maximum tolerable voltage error residue (see equation 4.16). With the given mismatch voltage transfer in section 4.4 the maximum tolerable voltage error residue on the gate node is given by equation 4.17 (see also appendix D.6). This means that there is a minimum size for the smallest capacitance change (C_{LSB}).

$$V_{STEP,LSB} = \frac{C_{LSB}}{C_c} V_D < \sigma_v \tag{4.16}$$

$$\sigma_v = \sqrt{2} INL_{max,LSB} \frac{\sqrt{2^n - 1}}{2^{nr} - 1} (2V_{GT,H} - V_{G,PP}) \tag{4.17}$$

$$C_{LSB} < \sqrt{2} INL_{max,LSB} \frac{\sqrt{2^n - 1}}{2^{nr} - 1} \frac{2V_{GT,H} - V_{G,PP}}{V_D} C_c \tag{4.18}$$

With the result from equation 4.16 the number of steps (C_T/C_{LSB}) can be calculated and herewith the number of required trim bits $\ln(C_T/C_{LSB})/\ln 2$.

4.4.3   Noise contributions

In this section various noise contributions are evaluated. First the output noise from the (equivalent) hold capacitor is determined. This gives a criterium for the hold capacitor size. After this the noise of the output transistor is evaluated.

Hold capacitor noise contribution

When the voltage on the gate is high (V_{REF}) and the switch is closed, the noise is determined by the noise of the reference source and by the (resistive noise of) the switch. Note that since the bandwidth of interest (Nyquist band) is smaller than the noise bandwidth, not all noise on the gate node is relevant.

The noise contribution of the switch ON resistance will determine the switch size (see section 2.4.4).

When the (current and) voltage is LOW, the noise is determined by the (effective) hold capacitor which is connected to the gate (the noise is sampled). The noise contribution of a hold capacitor biasing a transistor is described in section 2.4.3. This situation is similar to what is described there. However, in this case, the transconductance is much lower (a factor $\sqrt{R}$, with R the current ratio) and the sources have different ON and OFF times. In this case there are always three sources (in stead of 1) that feed noise to the output (see also section 1.2). - there is always one in four sources that is ON. Therefore, the noise addition is three times as high (see equation 4.19).

$$SNR_C = \frac{C_c(2^n - 1)V_{GT,H}^2 R}{24k_B T}$$
(4.19)

the required capacitance

$$C_{ALL} = 4C_c(2^n - 1) = \frac{96k_B T SNR_C}{V_{GT,H}^2 R} = \frac{12C_T}{R}$$

where C_{ALL} is the total capacitance required for ALL sources, and C_T the capacitance that would be required if a 'normal' hold capacitor would be used (the total hold capacitance required when the $HIGH$ voltage is sampled on a hold capacitor and the LOW voltage is zero, see section 2.4.3).

Hold capacitor size

With the information in the previous sections, the size of all hold capacitors summed (of a single section) C_c can be determined. Given the current ratio in equation 4.9 and the noise criteria in equation 4.19 a requirement of the hold capacitor is found, as shown in equation 4.20 (see appendix D.5).

$$C_c = \frac{C_{ALL}}{4(2^n - 1)} = \frac{3C_T}{R_0\sqrt{2^n - 1}}$$
(4.20)

where

$$C_T = \frac{SNR 8k_B T}{V_{GT,H}^2}$$

and

$$R_0 = \frac{V_{GT,H}\sqrt{W_{TOTAL}L_1}}{2\alpha A_{VT}}$$

R_0 can be determined by the DC requirements that $need$ to be met. For matching, it is beneficial to choose the current source transistor as large as possible; then the matching is high and the hold capacitor size requirement is low.

From chapter 2.1 it was found that for low LF distortion the current-source transistor length can be chosen $0.3\mu m$ (the cascode length is then $0.15\mu m$). For a maximum output current of $10mA$ for each channel, the total width $W_{TOTAL} = W_1(2^n - 1)$ should be $1114\mu m$. R_0 then evaluates to 152 which means a total of $131.52pF$ of capacitance (C_{ALL}) is required for 8 bits of resolution, $186pF$ for 9 bit and $263.32pF$ for 10 bits of resolution ($V_{GT,H} = 0.2V$, $\alpha = 3$ and $SNR = 81dB$).

With these conditions the peak-peak gate voltage will be ($V^2_{GT,H} = RV^2_{GT,L}$) 135.2mV, 122.88mV and 108.3mV for respectively 8, 9 and 10 bits of resolution.

Note that the transistors may be chosen even larger; this way matching will be better, and lower hold-capacitors are required. A disadvantage of large transistors is, however, that due to capacitive coupling to reference nodes and output capacitance non-linearity, distortion at high frequencies will increase.

Output transistor noise

In the 'soft' switching topology there is always current flowing through the output transistor. This means that the noise contribution of a single section is higher than when the transistor is turned *ON* and *OFF*. The noise contribution of a current source transistor was described in section 2.4.1. It is seen there that the output noise power is proportional to the transconductance (gm). Since the transconductance scales with the square-root of the current, it can be expected that the noise contribution of a *LOW* current feeding transistor adds $1/\sqrt{R}$ the noise power of a *HIGH* current feeding transistor, with R the current ratio.

Note that there are always 3 transistors feeding a *low* current to an output and one transistor a *high* current. Summing the noise of all sections the total signal to noise ration is shown in equation 4.21 (see section D.7). It is seen in this equation that the output transistor noise increases significantly (SNR decreases 6dB for $R = 4.5$ to 3dB for $R = 15.8$).

$$SNR = \frac{I^2_S}{I^2_{n,total}} = \frac{(1 - \frac{1}{R})^2}{1 + \frac{3}{\sqrt{R}}} \frac{I_M V_{GT,H}}{16 k_B T \gamma B} \tag{4.21}$$

4.4.4 Design example

With the conditions described above for 8 bits of resolution, a total hold capacitance (C_{ALL}) of 131.52pF is required (SNR is 81dB). This means that locally (at each current source, C_c) the hold capacitor will be 129fF (see section 4.4.3). Assuming a digital driving signal with an amplitude of 0.8V, the nominal transfer (H_0) will be 0.169 (see section 4.4.1). Assuming single edge driving, the 'nominal' driving capacitance ($0.5C_{r,T} + C_{r,0}$) will be 21.8fF and the total 'trim' capacitance ($C_{r,T}$) will be 10.449fF (see section 4.4.2). For less than 1 *LSB* integral non-linearity in a 12 bit converter system, the minimum switched capacitance will have to be $C_{LSB} = 0.326fF$. This means that there will have to be 5 trim bits and the minimum trim step is 0.04 *LSB*.

In fig. 4.13 and 4.14 respectively the integral and differential non-linearity are shown. It is seen in the figure, that the *DNL* and *INL* decrease significantly after the circuit is trimmed. For this simulation 255 Monte-Carlo runs were done of the circuit shown in fig. 4.10. The reference current was chosen equal to the output current and the device sizes were chosen equal. Note that a 'nominal' simulation was done with $DT = 16/31$ to evaluate the 'nominal' output output current. This current is subtracted from the Monte-Carlo outputs to find the error current. A sample of the output signal is shown in fig. 4.12. To evaluate the 'effective' output current, the transient response is first integrated from 2ns to 4ns. The collected charge is then the result of a 'high' signal and a 'low'

signal combined. To correct this, 2 times the charge transferred to the output in the time interval $1ns$ to $2ns$ is subtracted. The result is a 'high' current minus a 'low' current.

Note that the result shown here is the result of half of a single channel simulation. In practice each channel (differential output) will have two times $2^n - 1$ current sources. Considering a full single channel, the DNL will be $\sqrt{2}$ smaller than shown in the figure (each current is the average of two current-sources). In a differential system (two full single channels), the DNL then is decreased another $\sqrt{2}$ (σ_i increases by $\sqrt{2}$, and the signal level, thus the LSB current, increases by a factor 2). In total it can thus be expected that the DNL and INL is half of what is shown in the figure for a fully differential setup. To reduce simulation time, however, only half of a single channel is shown.
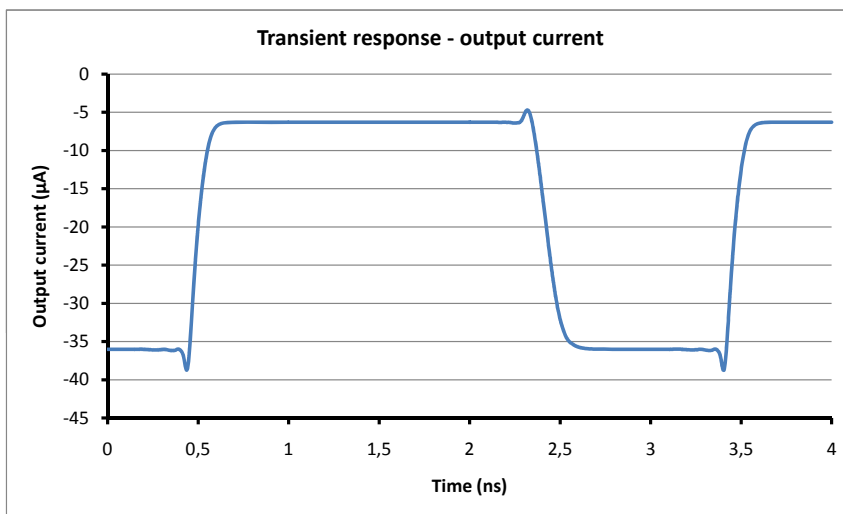

Figure 4.12: Transient output signal - output current

As was stated in the introduction (see section 1.2.2) there are two ways to trim the circuit: trimming DNL and trimming INL. The results are shown in the following sections.

Trim DNL

In figure 4.13 it is seen that the integral non-linearity is significantly reduced. Note that there is a substantial gain error in the non-trimmed INL; this is due to the non-linearity of the output transistor. When the error voltage is positive, the (absolute) output error current will be much higher than when it's negative. In many dataconverters this gain error is not a big issue. In figure 4.15 the gain error is subtracted (INL at code zero and full-scale is zero). It is seen there that the mismatch residue is indeed approximately 1 LSB. Because of the nature of the trim (the DNL is trimmed) the DNL is decreased more significantly than the INL.

In figure 4.16 and 4.17 histograms of respectively the trim code (the digital value that is required to trim the respective cell) and the output differential
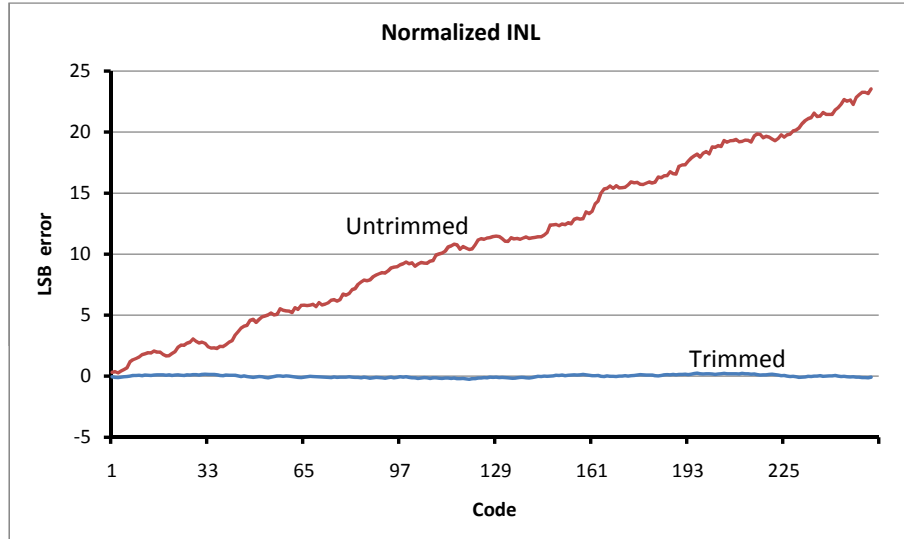
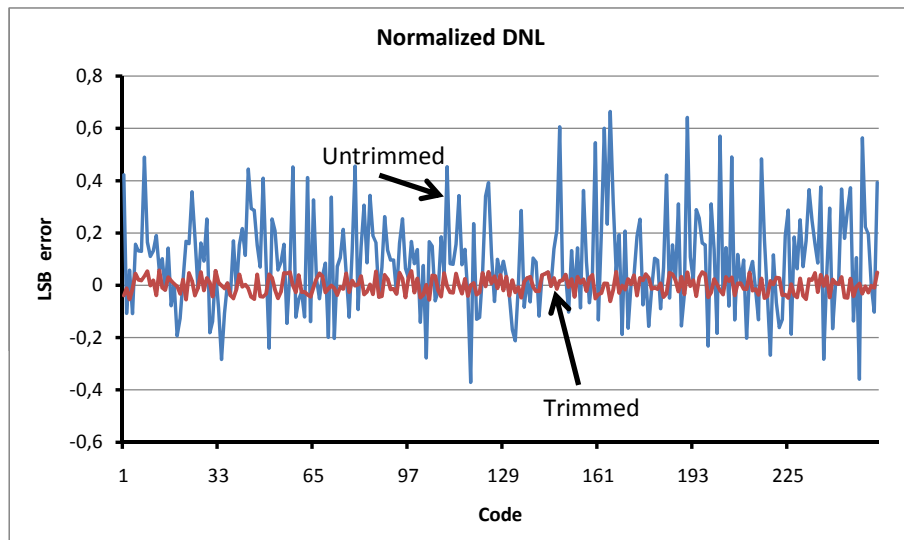Figure 4.13: Normalized integral non-linearity

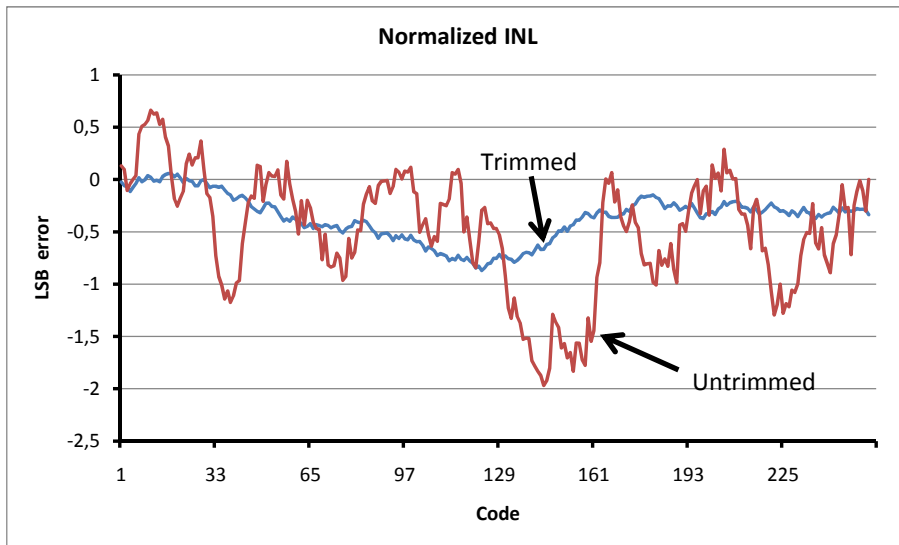Figure 4.14: Normalized differential non-linearity

Figure 4.15: Normalized integral non-linearity - subtract gain-error

error. It is seen that the trim code is gaussian distributed with a variance that is substantially smaller than the trim range (the current trim range should be 3 times of the current variance). In the DNL histogram it is seen that pre-trim distribution is gaussian. After the trim the distribution is uniform. This is easily understood by the fact that the output signal is bounded within a small range (trim accuracy). If this range is smaller than the pre-trim variance, the distribution will be (more or less) uniform.

Trim INL

It is also possible to trim the circuit for low INL; when this is done the INL over the entire range will be smaller than the trimstep. The DNL and INL of the low-INL trim is shown in figure 4.18 and 4.19. It is seen there that the INL is always smaller than the LSB trim step (0.04 LSB); this means that the DNL will not be higher than twice the LSB trim step. With this type of trimming thus higher trim steps can be used (fewer trim bits). A disadvantage of this method is that when the INL is trimmed the value of each output code needs to be measured, whereas with the DNL trim only sources need to be 'matched'. This measurement needs to have the same accuracy as the desired result, which is quite high. For on-chip trimming, this is undesirable. When trimming the differential error, however, only a comparison needs to be made; when using a successive approximation trim algorithm it is only required to know whether a given current is larger or smaller than another. For stand-alone (single D/A packaged) high precision devices it may be feasible to use high precision (off-chip) instrumentation to trim the INL (costly).
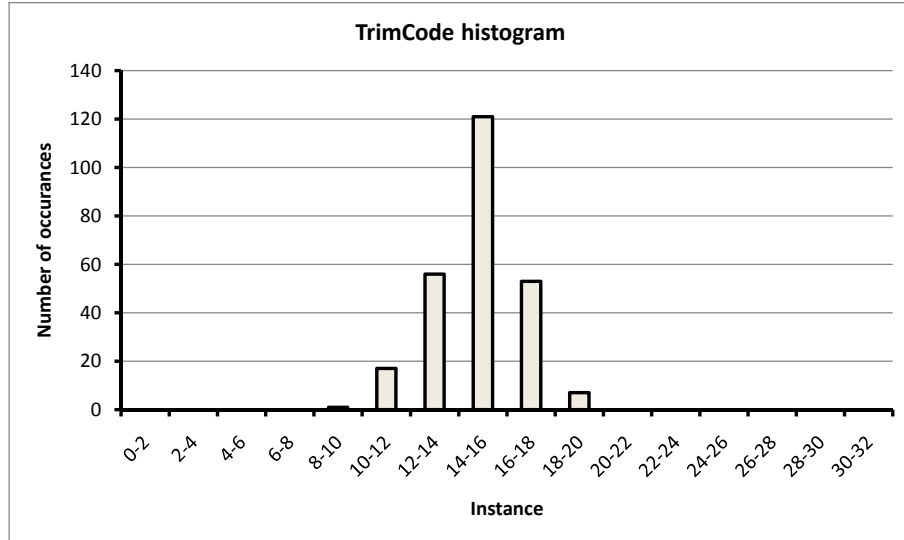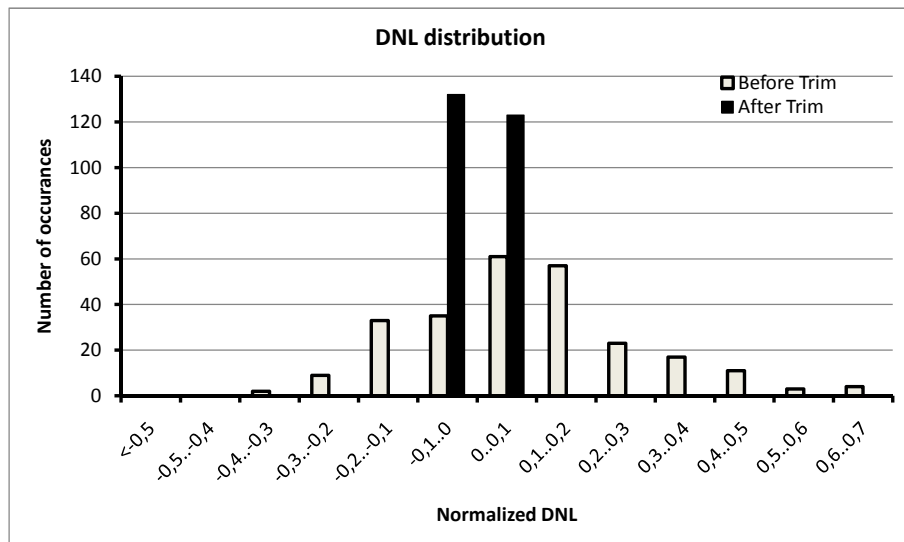
Figure 4.16: Trimcode histogram

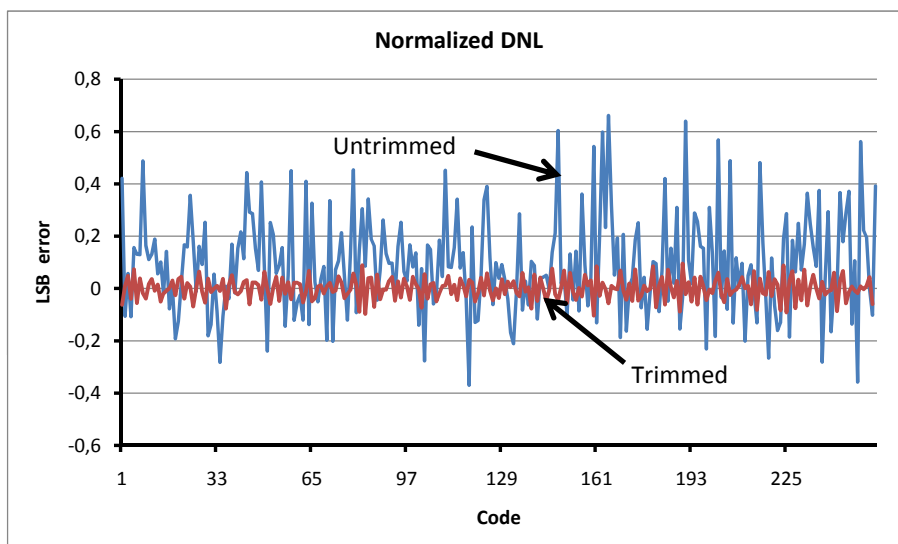Figure 4.17: Differential non-linearity histogram

Figure 4.18: Normalized differential non-linearity - optimize INL
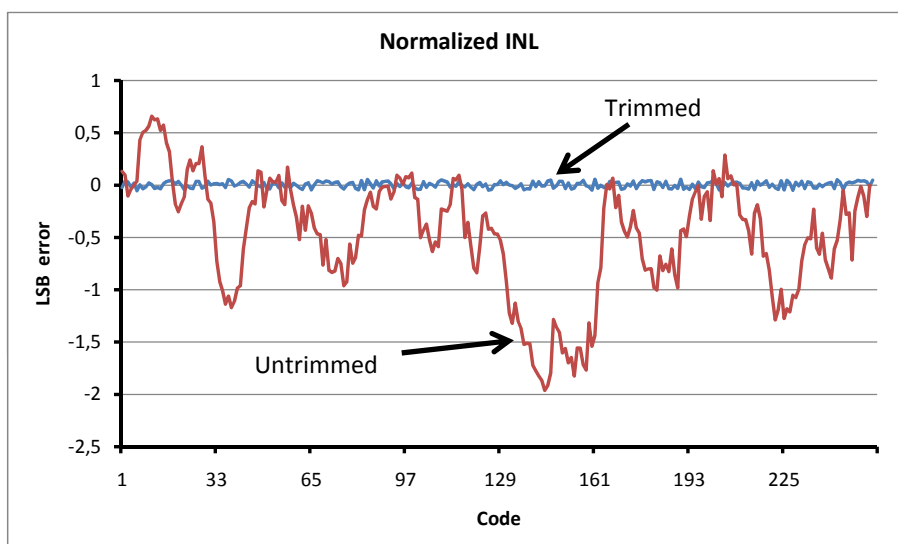
Figure 4.19: Normalized integral non-linearity residue

Chapter 5

Implementation aspects

This chapter deals with some implementation issues of a 'soft' switching D/A converter. It is necessary to have four independent current cells in each section of a thermometer encoded converter. A single cell with then output a 'high' current during only a single period (T_S). If consecutive 'high' pulses need to be output on a single channel, it will be generated alternately by two cells. The implementation of a single section of a thermometer encoded D/A converter is shown in fig. 5.1. In the figure these two cells (for each channel) are seen. It is also seen that alternating the left and the right channel is 'selected' by CD and nCD.

The reason for this alternation is that there will be inter-symbol interference due to slow rise and fall times; if a single cell outputs two consecutive 'high' values, more charge is being driven into the output than when twice a single 'high' output pulse is generated. Without proving that the slopes of the output signal are insufficiently fast it can intuitively be accepted that this non-return-to-zero operation will lead to high distortion. It may be argued that a true return-to-zero operation can also be used in this application; in this case however very high-speed settling of references is required. The reference needs to be stable when used in generating the next pulse.

Figure 5.1: Top-view section implementation - four cells in a single section of a thermometer encoded D/A converter

In section 5.1 an implementation of a single cell (as shown in fig. 5.1) will be described with some properties and aspects. After that the required digital

control logic is described.

5.1   Cell-implementation

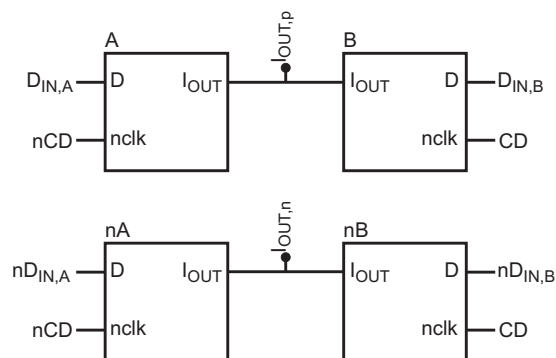In section 4.4 performance aspects of the 'soft' switching current cell were described. This section deals with implementation aspects of the cell. Some requirements of the cell are related to timing. These are met by means of digital logic.

A simplified model of a cell's output section is shown in fig. 5.2. The figure shows the output section of of one cell in figure 5.1. Other (digital) parts of the cell are described in section 5.1.2 and 5.1.3. In figure 5.2, an output transistor is shown that is driven by a capacitive voltage divider and a switch.
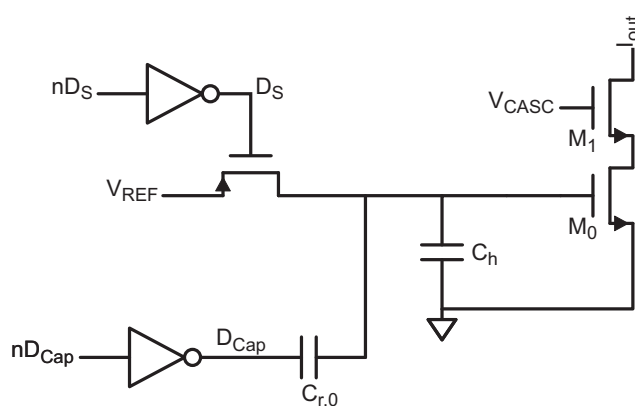
Figure 5.2: Simplified model of a cell's output section

5.1.1   Cell timing

For correct operation the timing timing of the signals that feed to the cell should be as shown in fig. 5.3. Note that the timing shown in the figure is when the data signal is 'high' over time; for data 'low' D_{Cap} should be maintained 'low' and D_S should be 'high'.

It is seen in the figure that with this timing (after the $nCLK$ fall) the capacitor will be driven first (D_{Cap} 'high'), then the switch is closed and opened (D_S 'low' and 'high') and finally the capacitor network restores the voltage to it's 'idle' value (D_{Cap} 'low').

Note that for the output current only the timing of the capacitor driver is relevant; the capacitor network determines when the current source switches ON and OFF, the switch merely is there for noise reduction and low frequency referencing.

This behavior can be implemented using some logic gates.

5.1.2   Capacitor driver

As seen in fig. 5.3, the capacitor driving signal D_{Cap} must go 'high' as soon as the inverted clock goes 'low' and it must wait until the switch driving signal (D_S) goes 'high' before in may be return to it's 'low' state.
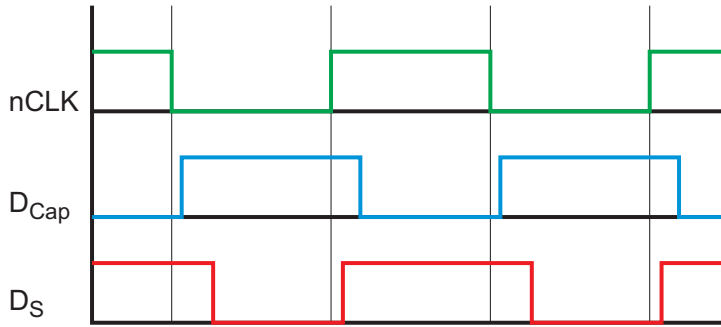
Figure 5.3: Cell timing

The capacitor driver circuit is shown in fig. 5.4. Before a $nCLK$ falling edge, $D_{S,0}$ is 'high', and D_{Cap} is 'low'. When the falling $nCLK$ edge arrives, the D_{Cap} rises (after thee consecutive inverting stages). After some time the switch driver will close the switch and $D_{S,0}$ is set 'low'.

After the following rising edge of $nCLK$ $M4$ will close. At this point in time the output of this stage does not fall; $M6$ is still 'open' ($D_{S,0}$ is 'low'). Finally, after the switch has been opened ($D_{S,0}$ is set 'high'), the voltage at the output of the cascaded inverter ($M4$ to $M6$) and thus D_{Cap} will go 'low'.

The voltage on the output of the cascoded inverter stages thus is 'floating' for a small period of time. The output capacitance of the stage and the input capacitance of the next stage acts as a holding capacitor during this short interval.

It is thus found that there is a 2-inverter, one cascoded inverter (falling input) and one transmission gate delay between an incoming falling edge of the $nCLK$ signal and the output rising. The output fall signal is initiated by the rise of $D_{S,0}$ and then has a two inverter and one cascoded inverter delay.
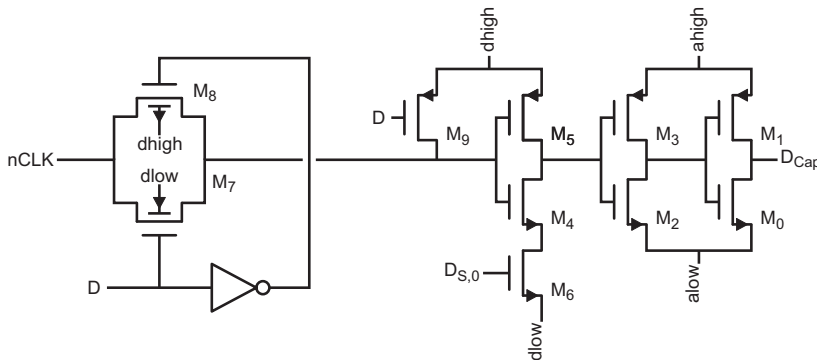
Figure 5.4: Capacitor driver circuit

The input signal D is coupled into the signal path around the transmission gate ($M7$ and $M8$). If data is 'high', the gate will conduct and the clock signal is fed to the capacitor driver circuit. If data is 'low', then the gate is 'open'. $M9$ connects the node to *dhigh* to keep the output node of the transmission gate from floating. In this case no clock signal is fed to the capacitor driver

circuit and the output remains constant.

5.1.3 Switch driver

The switch driving network is a charge redistribution network which results in a high switch overdrive voltage. This is required because the switch resistance needs to be quite low to meet noise requirements. This is described in section 2.4.4. The implementation of the switch driver is seen in fig. 5.5.
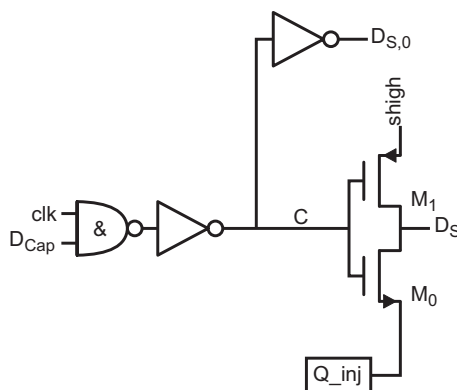
Figure 5.5: Switch driver implementation

It was seen in the previous sections that the switch needs to be closed (D_S 'low') after D_{Cap} is 'high'. It must open as soon as the $nCLK$ rises (CLK fall edge).

In the circuit, the *AND* gate (inverted *NAND*) ensures that the switch is not driven until the capacitor driver has raised it output (D_{Cap} AND CLK must be 'high'). On the falling edge of the clock, the switch is opened by CLK directly; in this state D_{Cap} is still 'high'.

A 'copy' of the D_S signal ($D_{S,0}$) is made which is used in the capacitor driver circuit; this is done because the voltage levels of D_S are incompatible with the digital gate used there. It takes two inverters and one NAND-gate delay before the $D_{S,0}$ signal is set 'high'.

It was seen above that there is a delay of two inverters, one transmission gate and one cascoded inverter (falling input) from a falling $nCLK$ edge to the rising of the output of the capacitor driver network. It takes the delay of four inverters, a NAND-gate and a cascoded inverter (rising input) until the output of the capacitor driver falls. This brings some asymmetry into the output signal.

Note that instead of a inverted NAND-gate also a transmission gate may be used in the switch driver network. This will lead to a shorter delays and a more symmetrical output signal (the total delay is then that of three inverters, a cascoded inverter and a transmission). There will be some additional assymetry due to the fact that there is an additional delay in the CLK signal with respect to the $nCLK$ signal (CLK is later).

To reach sufficiently low voltages on the gate of the switch, the charge redistribution network (Q_inj) is included.

charge redistribution network

To ensure a high switch overdrive voltage, a charge redistribution network is included. In fig. 5.6 the charge redistribution network is shown, with the output inverter of figure 5.5. When data is 'low', the switch should not be closed. In this case the multiplexer connects signal A to it's output, A_0. The voltage on the high side of the capacitors C_0 and C_1 are alternating between *dhigh* and *dlow*. If there is some charge in the capacitors, the voltage on the low side of the C_0 and C_1 will drop below *dlow* which results in M_3 and M_4 conducting. If this is done in an alternating fashion charge is maintained in the capacitors. The NAND-gate latch ensures a break before make operation. It is unwanted that both MOST's (M_3 and M_4) are *ON* at the same time as this discharges the capacitors. The NAND gate that drives C_0 'waits' until the voltage on the high side of C_1 the has gone up before lowering it's output and vice versa.

Note that the body diodes of M_3 and M_4 will ensure a startup current; if there is no charge in the capacitors, the voltage on the low-side will go above *dlow*: in this case the body diodes will conduct.

Figure 5.6: Charge redistribution network to drive switch

If the data signal is 'high', the method of driving C_1 slightly differs. The reason for this is that the output voltage D_S is going down in two stages; first is it connected to ground and then charge redistribution ensures it goes well below ground. To do this, accurate timing is critical. First signal C will go up; at this point in time A_0 must be 'low'. This makes sure that M_2 conducts and the charge that is required to lower the D_S voltage is fed to ground. After this, signal A_0 goes up (M_2 opens) and then D_A is lowered. The charge stored in C_2 is then (partly) relocated to the gate capacitance of the switch and MOST capacitances of M_0 and M_1.

When the switch has to open up it is best to first rise D_A, then C can go down. This way, the charge that came from C_2 is flowing back and there is no net charge transfer. If C switches before D_A there will be a current flowing from *dhigh* directly to C_2 which may disturb the capacitor voltage. The last

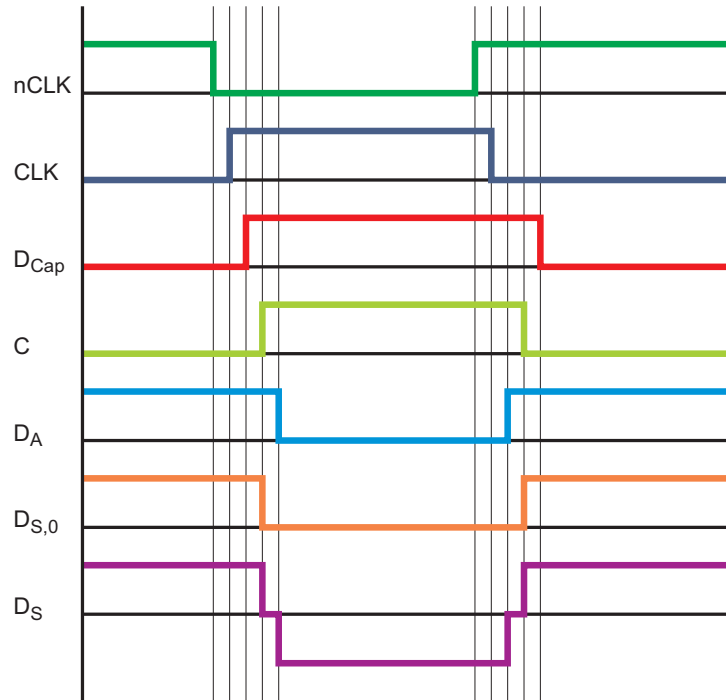step is to lower the voltage on A_0. In fig. 5.7 the required timing of various signals is summarized.

Figure 5.7: Required timing for the charge redistribution network

signal generation

An implementation that meets the timing criteria described above is shown in fig. 5.8. In the circuit is seen that signal C will go up with the rise of D_{Cap} and will fall on the falling CLK edge. Signal D_A will go down with the rise of C. The rise of D_A will be initiated by the fall of the CLK signal.

Note that if a transmission gate is used to generate the C signal, also for the D_A signal a transmission gate should be used. In this case the $nCLK$ signal (which is slightly earlier than the CLK signal) is used to trigger the rise of D_A.
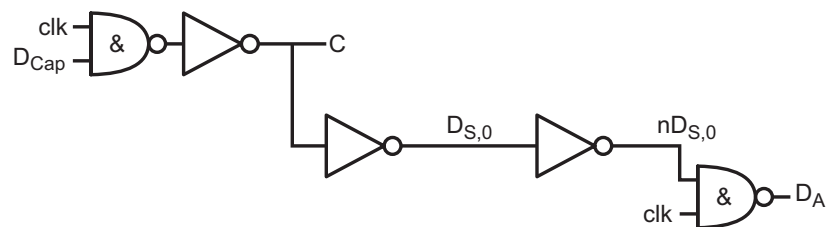

Figure 5.8: Digital signal generation for charge redistribution network

A_0 multiplexer

The last part of digital logic that is required for the charge redistribution network is the A_0 multiplexer, which is shown in fig. 5.9. The multiplexer has to feed the signal A to it's output (A_0) if D is 'low', and signal $D_{S,0}$ inverted if D is 'high'. Note that (due to data inclusion in the capacitor driver path) the signal $D_{S,0}$ will be 'high' at all times when D is 'low'. Therefore only a single $NAND$ need to be used to feed the $D_{S,0}$ signal to the output. If D is 'low', A will be fed to the output.
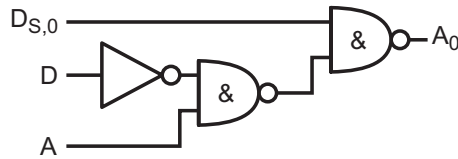

Figure 5.9: Implementation A_0 multiplexer

5.2 Digital control of single section

As described above, the output will be driven by two stages alternating. When for example the A side is active (two left sections in figure 5.1) either the positive side ($D_{IN,A} = 1$) or the negative cell ($D_{IN,A} = 0$) will generate an output pulse. When the left-side is active, the right side data can be clocked into a hold latch. This is also shown in fig. 5.10. In the figure, the arrows indicate when data (D) is latched in a hold register. It is seen that when the left side is active (nCD is 'low') then the data can be latched into $D_{IN,B}$. Note that it is important to keep the latch output $D_{IN,B}$ and $D_{IN,A}$ stable around CD and nCD edges; due to the implementation of the cell, there is a delay between the CD and nCD edge and output stability.

If the data is pre-latched, this can be done at the positive edge of $dclk$. If no separate data latch is used the digital part can be clocked at the negative edge of $dclk$, and stability must be guaranteed at the next negative edge.

The implementation of the digital control of one section is shown in fig. 5.11. Two clocked DFF generate a clock signal for the individual cells. Both flip-flops use the same input clock signal to generate symmetrical signals. In the the lower part of the figure the datapath is shown. It is seen there that when CD is 'high' the data gets clocked into section A, if it is 'low' it is clocked into section B. Note that the combinational logic that generates the thermometer coded data needs to settle before the falling edge of the $dclk$ signal.

5.3 Jitter

This section deals with some aspects that are relevant during D/A converter operation; main clock jitter and cell jitter. It is relevant what the sensitivity of the circuit is to clock jitter and how much jitter the circuit produces itself. First, it needs to be known how clock jitter transfers to the output and how much noise it generates. Second, it needs to be known how much jitter the circuit itself produces.
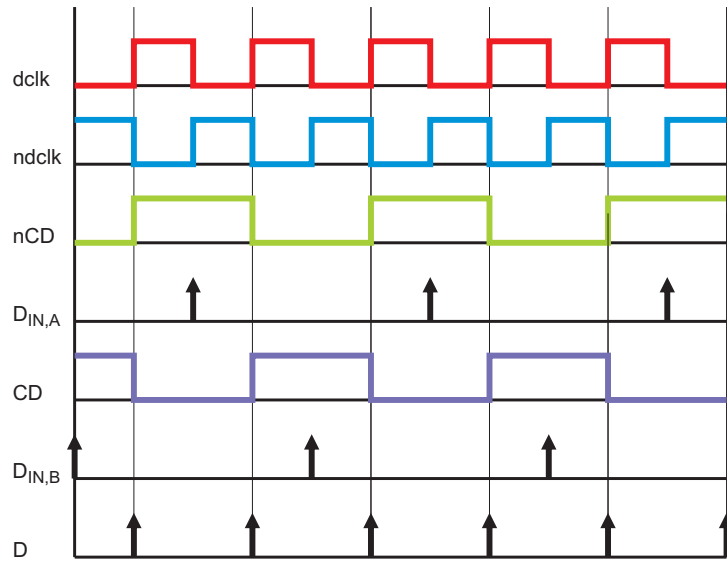
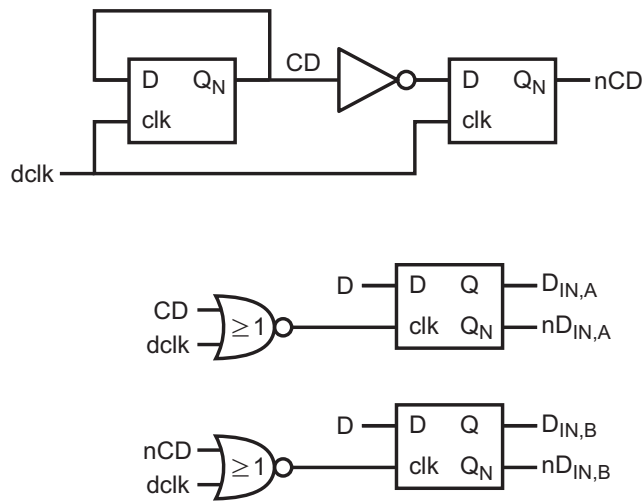Figure 5.10: Data availability requirements for cell

Figure 5.11: Digital logic for single section

5.3.1 Main clock jitter transfer

As is seen in fig. 5.1 the implementation of a cell is dual and differential. If the output is a DC signal level, it can be expected that clock jitter cancels. Assume that a certain cell has constant 'high' output (D_A and D_B remain 'high'). Because both cells A and B operate on the same clock signal, a delayed edge of the clock will result in more charge being injected into the output by cell A but an equal and opposite amount of charge by cell B (see also figure 5.10). By this simple reasoning it is seen that steady-state jitter cancels. If, for example, the second rising edge of the $dclk$ signal in figure 5.10 is delayed the CD 'low' time will be longer. This means that cell B will output more charge. It is also seen that the nCD 'low' time is reduced; this reduces the cell A output charge.

The dynamic clock jitter, however, is more significant. The amount of error-charge that is transferred to the output for a single section is given by equation 5.1.

$$\sigma_{Q,c} = 2\sigma_T I_H \qquad (5.1)$$

with T_s the clock period and I_H the mean 'high' current of a cell. Note that there is a factor 2 in the charge error because there are two cells affected by the clock jitter; for example a 'high' cell that outputs more charge into the positive output and a 'low' cell that outputs too little charge into the negative output.

The amount of error-charge thus depends on the number of sources 'switching' in a given cycle. The signal-to-noise ratio due to main clock jitter is shown in equation 5.2 (see appendix F.1).

$$SNR_{dB} = 20\log\left(\frac{T_{in}}{\sigma_T}\right) \qquad (5.2)$$

where T_{in} is the period of the input signal.

5.3.2 Cell jitter

It was already found in section 5.1.2 and 5.1.3 that a falling clock-signal is transferred through 2 inverter stages, one cascoded inverter stage (falling input) and a transmission gate. The rising edge is transferred through a minimum of 3 inverter stages a cascoded inverter stage (rising input) and a transmission gate. An approximation of the jitter of a 'logic' gate can be made by means of small circuit analysis with noisy models of the transistors. The equivalent small signal circuit of an inverter stage is shown in fig. 5.12. Note that this circuit also holds for $NAND$ and NOR gates; it is merely the load, the output impedance and the transconductance that differ.
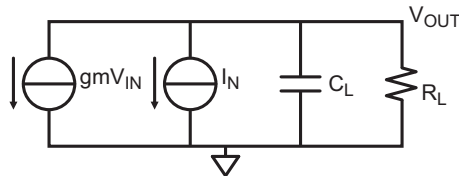

Figure 5.12: Equivalent small signal circuit of an inverter stage

To find the jitter contribution of the gate, the output referred equivalent noise needs to be determined. This voltage noise transfers to timing jitter (an voltage error at the next stage's switching threshold). This is seen in equation 5.3 (see appendix F.2).

$$\sigma_T = \sqrt{\frac{2kT\gamma Mu}{C_L}}\frac{1}{S} \tag{5.3}$$

where $S[V/s]$ is the slope of the output signal.

It is seen in this equation that the jitter decreases with transistor size (C_L is scales linear with transistor width while Mu is constant over width). If the load capacitance is $0.22fF$, $Mu = 8.14$ and the voltage rise-time is $30ps$ (output swing $1V$) then the RMS jitter is $0.6ps$.

Note that transmission gates introduce very little jitter to the signal.

Chapter 6

Simulation results

This chapter describes simulation setup and results. To estimate the dynamic performance of the D/A converter, a transient analysis is done. By transforming the signal to the frequency domain the spurious free dynamic range ($SFDR$) can be determined. The $SFDR$ is defined as the ratio of the power at the input frequency (at maximum output swing) over the power in the highest spur in the Nyquist frequency band. Since there will be no non-harmonic spurs (only the input frequency and the clock frequency and harmonics are present in the system) the highest signal is expected to be found at the third harmonic of the input signal, possibly folded back into the Nyquist region. Due to the fact that an 'ideal' symmetrical output is used in the simulations, second order harmonic distortion cancels entirely.

This chapter first deals with the simulation test bench setup and testing. In section 6.2 the signal processing is described; using quantization error estimation the noise-floor is lowered; this reduces simulation time. Finally, section 6.3 shows the simulation results.

6.1 Test bench setup

The test bench consists of a digital input signal generator, the D/A converter and output signal generation. This is shown in fig. 6.1. The thermometer coded input signal is generated using an 'ideal' flash D/A converter and an 'ideal' sinusoidal signal generator.
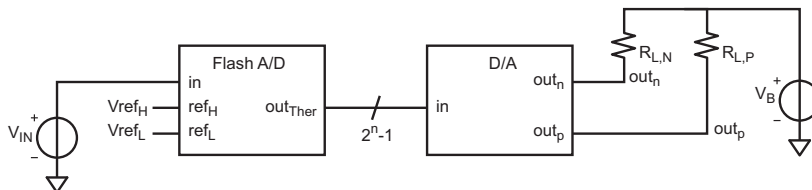

Figure 6.1: D/A converter test-bench

Flash A/D converter

The implementation of the 'ideal' flash A/D converter is shown in fig. 6.2. A resistor chain is connected between two reference voltages. The voltages on the nodes of each resistor is used as a reference voltage for a clocked comparator. An ideal amplifier senses the voltage difference between the respective reference and the input signal and generates a single-ended output voltage. This voltage is 'captured' by an ideal sample-and-hold. An ideal multiplexer, with an input reference of $0V$, consecutively switches between the digital 'high' and 'low' voltage.
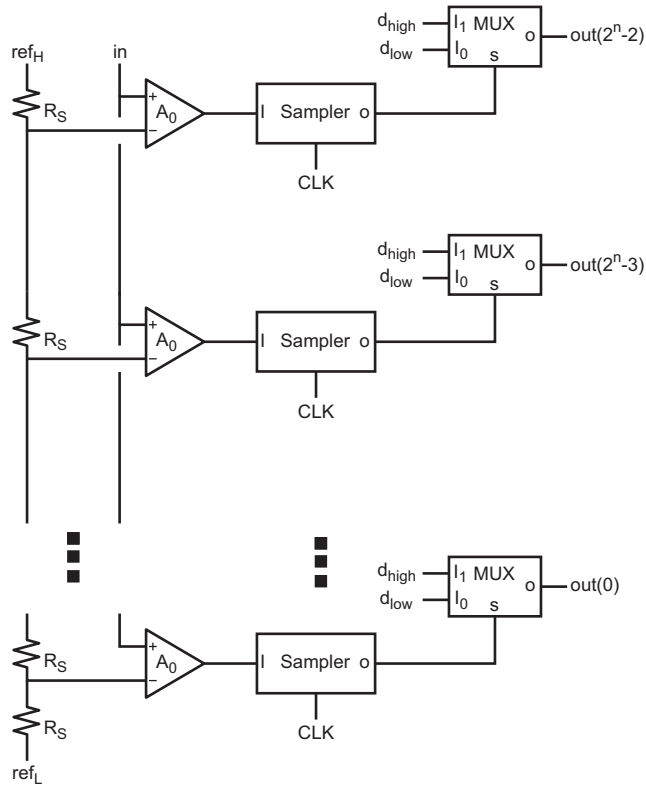
Figure 6.2: Ideal flash A/D converter

The digital part that is described in section 5.2 is used to generate the individual 'cell' signals.

Ideal D/A converter

To test the 'ideal' flash A/D converter (and some logic), an ideal D/A converter is used. The signals D_A, nD_A, CD and nCD from each cell is connected to an AND gate that determines if a current source should be ON or OFF.

The output signal of the A/D and D/A converter combined is shown in fig. 6.4. In runtime in this simulation was $100ns$ (starting from $50ns$, which is a settling delay) with an input frequency of $490MHz$ and a sample frequency of $1.01GHz$. The signal-to-noise ratio in this case is $47.48dB$, which

Figure 6.3: Ideal D/A converter

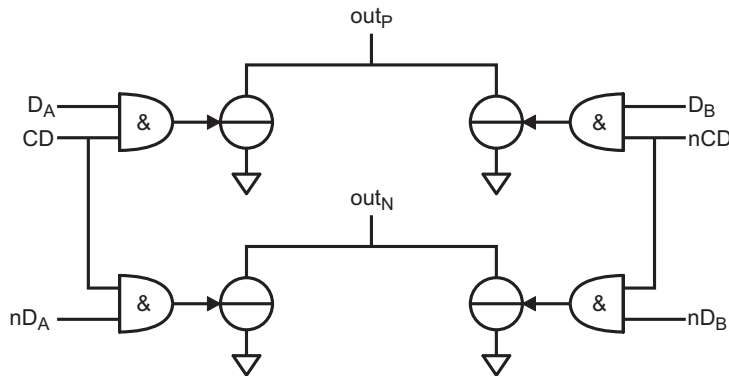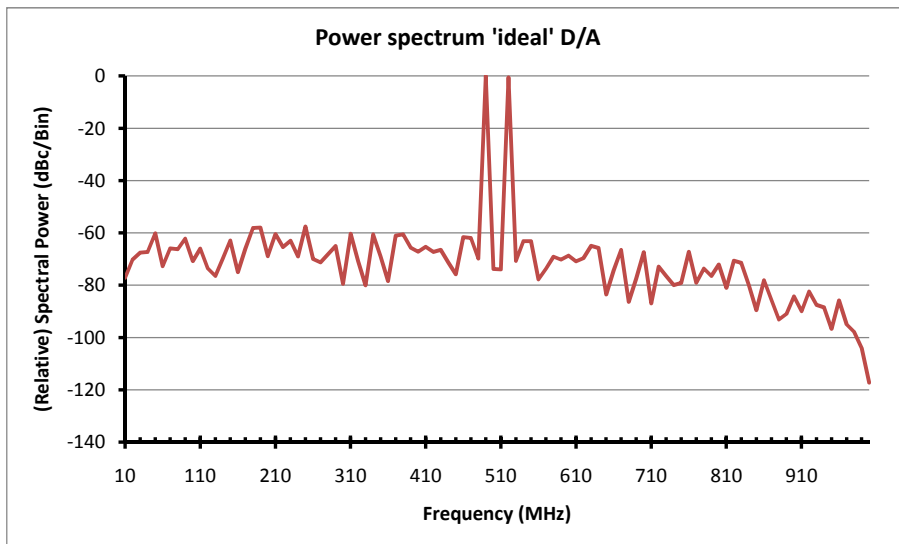Figure 6.4: Power spectral density - 'ideal' A/D and D/A converters

is approximately $2.5dB$ lower than the theoretical (8-bit quantization noise) limit of 49.95. If the signal is re-sampled (sample when the signal is stable) the signal-to-noise ratio increases to $49.89dB$, which approaches the theoretical limit.

Note that there is some SNR degradation due to the 'hold' function of the D/A converter. In the digital domain this is similar to over-sampling; if the signal is sampled at $2fs$ in stead of fs it manifests itself as a time-shifted addition. Since the input signal is very close to the Nyquist frequency, the signal-voltage does not double, but in stead it is $\sqrt{2}$ times larger than in the fs sampled signal. The quantization noise, however, since the most power is in the low-frequency range, will add with little phase-shift. This means that the observed quantization power (nearly) quadruples, while the signal power only doubles. This means that a maximum of $3dB$ signal-to-noise ratio decrement

will be observed. Note that part of the quantization noise voltage (at higher frequency) will not be in-phase; therefore the reduction will be slightly lower than $3dB$. This is also seen in equation 6.1 (see appendix G).

$$\Delta SNR = \frac{|sinc(\frac{\pi f_{sig}}{fs})|^2}{\int_0^{\frac{fs}{2}} 2\frac{|sinc(\frac{\pi f_{in}}{fs})|^2}{fs} \, df_{in}} \tag{6.1}$$

which reduces to (evaluate integral)

$$\Delta SNR = 1.2925|sinc(\frac{\pi f_{sig}}{fs})|^2$$

With an input frequency of $490MHz$ and a sample frequency of $1.01GHz$ the SNR reduction will be $2.55dB$. This is in accordance with the simulation result seen above ($2.47dB$).

6.2   Output signal transformation and analysis

The simulation results of a transient result need to be interpreted, which requires some processing. To determine the dynamic performance ($SFDR$) of the D/A converter, a frequency transformation (FFT) of the output signal is done. To get a frequency resolution of the output signal of Δf, a simulation time of $\Delta = 1/\Delta F$ is required. To ensure that all signal power is accumulated in a single bin there need to be an exact amount of input signal periods and sample periods in this time interval. Therefore the sample-rate is chosen $fs = N/\Delta$ and the input frequency M/Δ. In this case no FFT window is required. By choosing M and N such that they have no common divider, each sample will be unique and the frequency resolution will be $1/\Delta$.

The transient output result from the simulator does not contain equidistant samples (the simulator chooses time steps). To evaluate the output spectrum this needs to be corrected. This is done (in *MatLab*) by means of first order interpolation.

With 8 bits of conversion resolution it can be expected that the total in-band signal-to-noise ratio will approximately be $50dB$ (see section 6.1 for a more detailed approximation). With N frequency bins the power in each bin will on average be $-50dB - 10\log(N)$. Harmonic components that have lower power than this will thus not be visible. Note that there will be quite some variance on the quantization noise spectrum; it is therefore possibly difficult to say whether the power level at for example $3fin$ is due to quantization noise or if it is harmonic distortion. A solution for this problem may be increasing the number of samples in the simulation (choose higher N). This will increase the frequency resolution and spread (and thus lower) the quantization noise level.

Another solution is found in estimating and subtracting the quantization noise. Since the non-quantized signal is known (this is the input of the 'ideal' flash A/D converter), it is possible to calculate the quantization error. The circuit has a certain gain and adds some delay (due to data re-clocking and from gate delays) to the signal which need to be compensated. By calculating the cross-correlation of the output signal and the 'ideal' quantized input signal, and finding its maximum, the time-delay of the circuit is recovered. Then the gain of the circuit needs to be recovered. To do this, first the output signal

is divided by the quantized digital (time shifted) input signal. The result of this is the 'unit' transient response (output response normalized to digital input code)in each period. By summing the transient responses of all periods the average (normalized) 'unit' transient response (one period) is obtained. Then the quantization error is generated. By multiplying the input (LSB) quantization error (quantized input signal minus non-quantized input signal) in each respective period with the 'unit' transient response, the effective output quantization error is obtained.

By subtracting this signal from the output signal the quantization error is cancelled. Fig. 6.5 shows a simulation result of a (partly ideal) circuit with and without quantization error subtraction. The circuit is an ideal A/ D converter and ideal D/A converter with a 2/0.1 cascode transistor on each output current source (for testing purposes only). It is seen that the noise level is reduced significantly and that harmonic distortion becomes visible. Note that (on parts of the spectrum) there seems to be correlation between the noise of both signals. This is because there is a pole at the output of the converter. If the noise floor needs to be lowered by $20dB$, this means that the noise power needs to be estimated with 1% accuracy. It is easily evaluated that the pole (of a first order system) needs to be at a frequency of $10\omega_{in}$, or, for a $490MHz$ input signal this is $5GHz$.

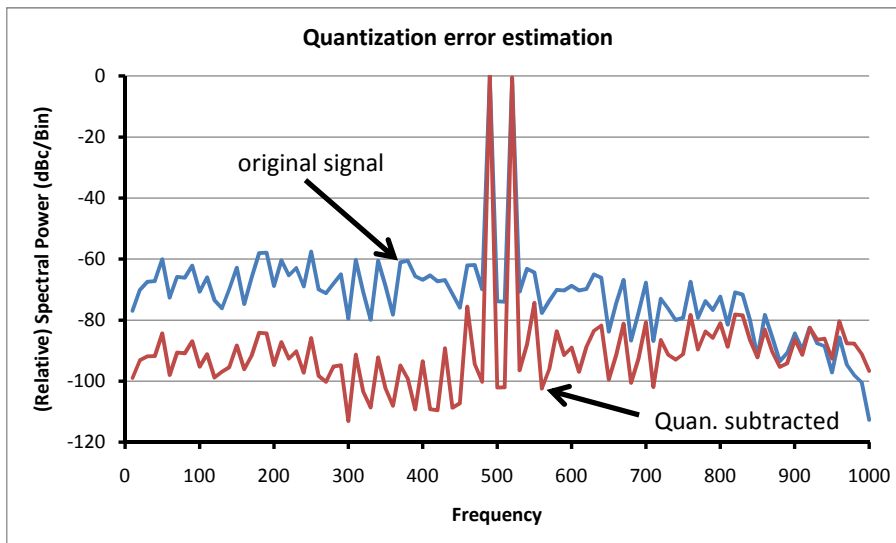A *MatLab* routine of this method is found in appendix H.

Figure 6.5: Quantization error estimation and subtraction - lowering the noise floor

6.3 Simulation results

A transient analysis was done on the entire circuit to obtain the spectral performance of the D/A converter operating at $1.01GS/s$ with a full-scale input input tone at $490MHz$. The result is seen in fig. 6.6. It is seen there that the

input tone (at $490MHz$) and its image (at $520MHz$) have an intermodulation distortion of lower than $-74dB$ (at $460MHz$).
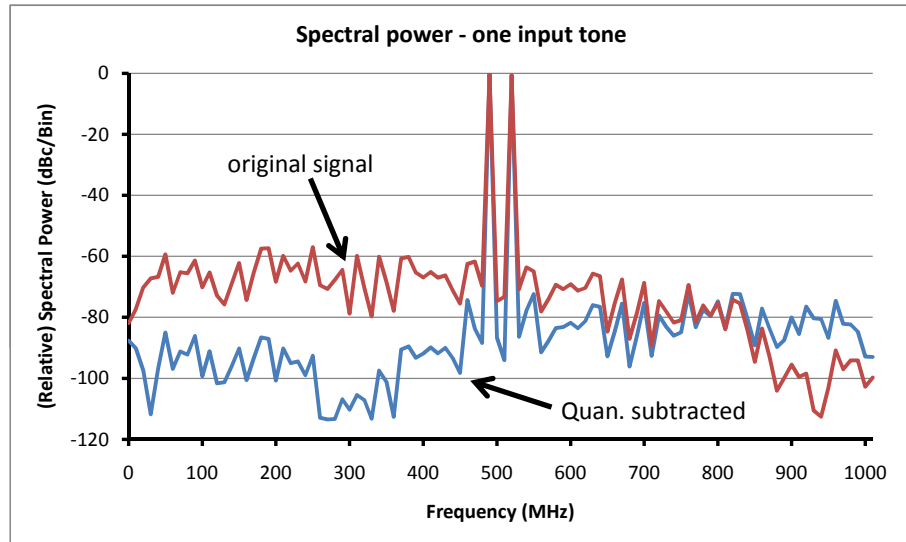

Figure 6.6: Simulation result - one tone input ($0dBFS$ at $490MHz$)

Also a test with an input frequency of $410MHz$ was done. The result is shown in figure 6.7. Note that the input level is $6dB$ lower than the full-scale (sinusoidal) output power. With an input frequency of $410MHz$ and it's image at $600MHz$ the power at the third order product ($220MHz$) is seen to be very low (lower than the 'noise').

Finally a two-tone test was done, this result is shown in figure 6.8. With an input frequency of 410 and $430MHz$ the third order product should be found at $390M$; the power in this bin is $-77dBc$. Note that the shape of the spectrum (around this frequency) is similar to the signal as 'original' (no quantization estimation). This implies that the power at these bins may be a residue of the quantization error. The single ended spectrum of the two-tone test is found in figure 6.9. It is seen there that there is substantial $2nd$ order distortion; at a frequency of $20MHz$ the power is $50.4dBc$ Around $170MHz$ the second order product of the input tones and the image is found ($-50dBc$). Note that this distortion is canceled if the (differential) output (load) is well balanced.
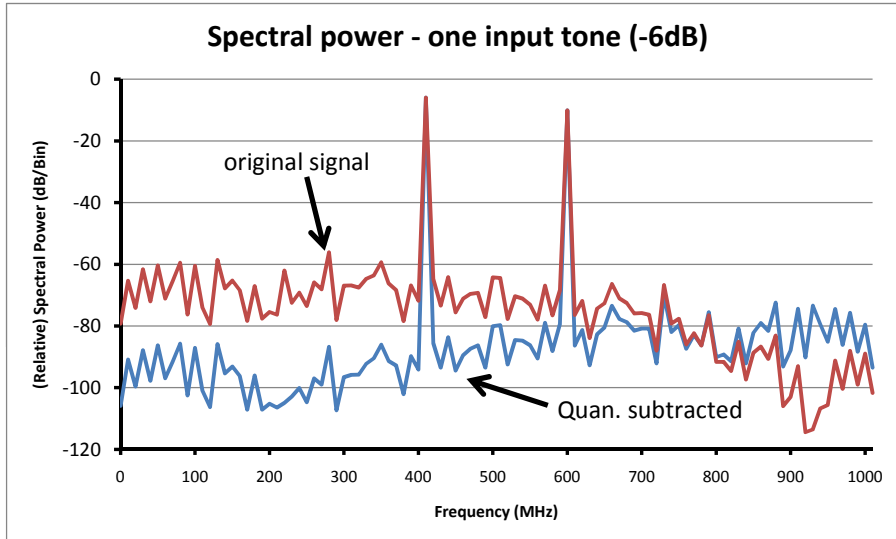
Figure 6.7: Simulation result - one tone input ($-6dBFS$ at $410MHz$)
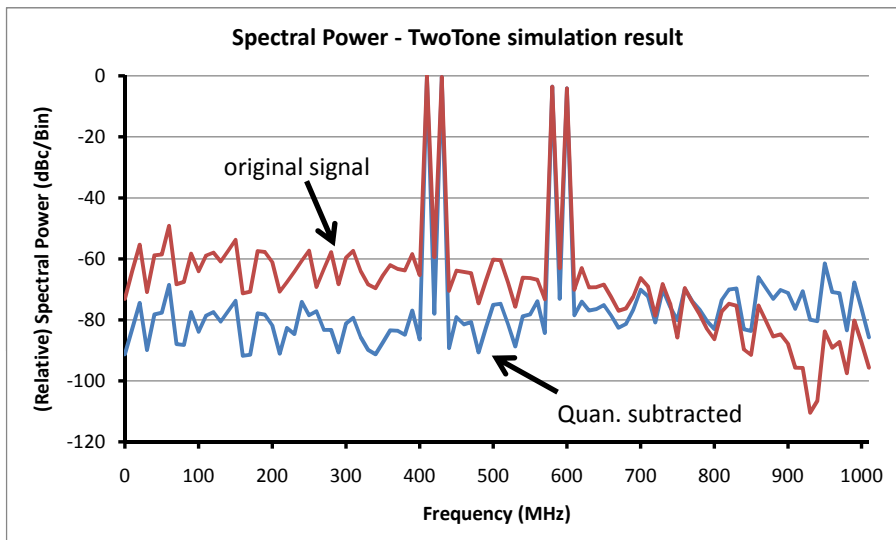
Figure 6.8: Simulation result - Two input tones ($-6dBFS$ at 410 and $430MHz$)

Figure 6.9: Simulation result - Two input tones ($-6dBFS$ at 410 and $430MHz$), single ended output
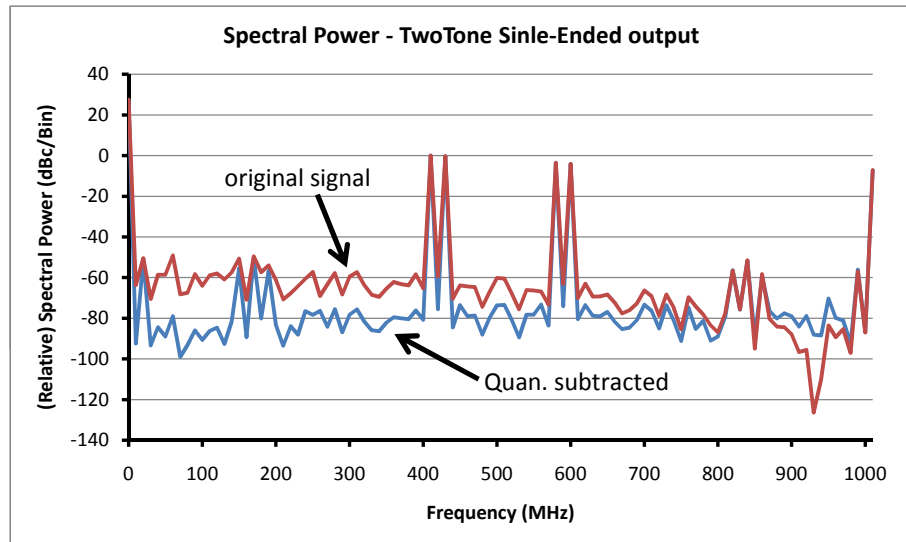
Chapter 7

Conclusions

In was demonstrated that it is feasible to implement a thermometer-encoded current-mode D/A converter using current-source modulation instead of current-steering. The output transistor is biased with a switching reference network. A *HIGH* voltage on the gate is achieved by switching it to a reference voltage and a *LOW* voltage is obtained by means of a charge redistribution network: a capacitive dividing network lowers the voltage on the gate. Given correct timing (switch must be 'open' before charge redistribution network is driven), the voltage on the gate of the transistor will switch between the *HIGH* and *LOW* state without loading the reference voltage. Note that the transistor is not turned *OFF*; it is switched to a *LOW* current. This *LOW* current is determined by the transfer-ratio of the charge redistribution network. By implementing this network with a bank of (binary) scaled capacitors, the *LOW* current can be 'trimmed'. This effectively trims the output current. When (digitally) trimming the output current, small output transistors can be used (with poor matching) and still a high DNL/INL performance can be obtained.

To reduce inter-symbol interference, an transistor outputs a 'fixed' amount of charge only during one period. This means two sources are required in each section; these are driven alternatively.

An advantage of this implementation type is that no differential high-precision switch driving signals (switched differential pair) are required and there is reduced feedback from the output to reference lines (small output devices); this reduces distortion. Furthermore, since there is no net charge transfer from the reference voltage to the load, reference voltages have reduced dependance on the output code. Since the reference voltages are only used one in every two periods, and it is unloaded when it is not used, it will settle quickly to a stable value before it is re-used.

7.0.1 Simulation results

Simulation results have shown that a $1.01GS/s$ D/A converter with a $490MHz$ (full-scale) output signal will have a signal-to-distortion ratio of more than $74dB$. A two-tone test (410 and $430MHz$, each full-scale-6dB) showed virtually no intermodulation distortion (noise floor at -77dBc). The single ended output second harmonic distortion was found at $-50dBc$.

7.0.2 further research

This work has been a feasibility study on whether it is possible to drive a current source directly. It is shown that this indeed is the case. The next step is to investigate (more common) problems such as scaling of (digital) devices (jitter), binary to thermometer encoder and clock and signal distribution.

Also startup effects need to be investigated; when the power is switched on, charge redistribution networks will be un-initialized. This means that the first time a current source is used, the output current is incorrect and a lot of charge is withdrawn from the reference lines. A solution to this problem may be found in using a startup routine, which initializes all current sources.

Furthermore, a trim algorithm and its (analog) circuits need to be implemented. Solutions may be found in using a successive approximation approach; it then needs to be determined whether the (differential) output current is positive or negative. This is non-trivial, because it needs to be determined whether the 'charge' injected into the output during *one* clock-cycle is either positive or negative (integrating output current).

When the current in a cascoded transistor is turned LOW, the operating speed (gm/C) of the cascode device is quite low and the settling time is high. The source of this transistor then has one cycle to settle to a stable value. If this settling time is too long, it can be expected that the charge injected into the output depends on the next (digital) value. It needs to be investigated what type (mainly $2nd$ order) and how much distortion this introduces and what the requirements are in terms of LOW current. Since high $3rd$ order distortion performance is obtained, it is expected that this effect is minor.

Appendix A

First-order CMOS65 approximations

In this chapter some simple parameters and equations are derived that match CMOS65 behavior. These equations are specifically used for hand calculations. Parameters are determined by simulations, some are curve-fitted. Equation A.1 is used as a reference.

$$I_D = \frac{1}{2} k_0 \frac{W_{eff}}{L_{eff}} (V_{GS} - V_{TH})(1 + \alpha \frac{\lambda(L)}{L} (V_{DS} - V_{DS,0})) \qquad \text{(A.1)}$$

The equation is interpolated around a drain-source voltage of $V_{DS,0} = 500mV$. Numerical output from ProMost is used to determine parameters.

Effective width and length and current factor

Keeping constant current and overdrive voltage, the effective width and the current factor are determined by plotting W_{eff} as a function of L and realizing that the $\frac{W_{eff}}{L_{eff}}$ should be constant (eq. A.2). Note that the effective width and current factor is interpolated at $V_{DS} = 500mV$.

$$\frac{W_{eff}}{L_{eff}} = 2I_D k_0 V_{GT}^2 \qquad \text{(A.2)}$$

The width as a function of the length is approximated by a sum of a polynomial and an exponential function, as shown in eq. A.3.

$$
\begin{aligned}
W &= AL + B + Ce^{-\frac{L}{L_0}} \\
W_{eff} &= W - Ce^{-\frac{L}{L_0}} \\
AL_{eff} &= A(L + \frac{B}{A}) \\
W_{eff} &= AL_{eff}
\end{aligned}
$$

$$\text{(A.3)}$$

with

$$\frac{B}{A} = L_1$$

With a least-square linear approximation constants A and B were obtained, C and L_0 were obtained by visual curve fitting. Note that the term with C can be considered negligible for lengths larger than $150nm$. The results are shown in table A.1.

Param	Value
A	8.551
L_1	0.1195
L_0	0.01
C	500

Table A.1: Curve fitting parameters

The current factor is then determined as is shown in eq. A.4

$$
\begin{aligned}
k_0 &= \frac{2I_d L_{eff}}{W_{eff} V_{GT}^2} \\
k_0 &= \frac{2I_d}{A V_{GT}^2} = 225.6\mu A/V^2
\end{aligned}
$$
(A.4)

The above parameters were obtained using $I_d = 10\mu A$, $V_{GT} = 101.8mV$.

Channel length modulation

This section describes how the channel length modulation as a function of the drain-source voltage can be modelled. In eq. A.1 this effect is seen as $\lambda(L)$. This value is quite dependent on the operating conditions of the device. A linear approximation is used (see eq. A.5) to determine the length dependence of the channel length modulation effect. The results in various ranges is shown in table A.2.

$$\lambda(L) = AL + B \tag{A.5}$$

A [$1/V$]	B [$\mu m/V$]	conditions
$A = 0$	$B = 0.11$	$L < 150nm$
$A = 0.1302$	$B = 0.0850$	$150nm < L < 1\mu m$
$A = 0.0645$	$B = 0.1489$	$1\mu m < L < 8\mu m$
$A = 0$	$B = 0.8$	$8\mu m < L$

Table A.2: Curve fitting paramters for the channel length modulation effect

The variable α models the drain-source voltage dependence on the channel length. It is approximated by $\alpha = 3 - V_{DS,DC}/0.2$. Note that this voltage is only used to determine the draincurrent; it should not be used in determining the output resistance.

MOST ON-resistance

When using a MOS-transistor as a switch element, the ON-resistance of the device is important. Usually switches are implemented minimum length. A

first order approximation of the drain current at low drain-source voltage is given by eq. A.6.

$$I_D = \mu C_{OX} \frac{W}{L}(V_{GT}V_{DS} - \frac{1}{2}V_{DS}^2) \tag{A.6}$$

In triode mode ($V_{DS} << V_{GT}$), this reduces to

$$I_D = \mu C_{OX} \frac{W}{L}(V_{GT}V_{DS}) \tag{A.7}$$

the output resistance

$$R_D = \frac{\delta V_{DS}}{\delta I_D} = \frac{1}{\mu C_{OX}\frac{W}{L}V_{GT}} \tag{A.8}$$

From *ProMost*, numerical results as shown in table A.3 are obtained.

$V_{GT} = 0.2V$	$R_{ON} = \frac{L}{WV_{GT}}13.28k\Omega$
$V_{GT} = 0.4V$	$R_{ON} = \frac{L}{WV_{GT}}8.004k\Omega$

Table A.3: R_{ON} approximation

Out- and input capacitance

The output capacitance of a MOS transistor in saturation is usually dominated by the gate-drain overlap capacitance. For CMOS065 this capacitance is $C_{GS,o} \approx C_{GD,o} = 170.2aF/\mu m$. The input capacitance of the transistor in saturation can be modelled as $C_{GS} = 2/3C_{OX}WL$ and is approximated by $7.085fF/\mu m^2$.

A diode connected transistor's impedance can be approximated by an RC parallel network. The cut-off frequency indicates the operating frequency range of the transistor. This frequency is given by eq. A.9.

$$\omega_0 = \frac{gm}{C} = \frac{2I_D}{V_{GT}W(C_{GS,o} + C_{GS}L)} \tag{A.9}$$

with

$$W = \frac{2I_D L}{kV_{GT}^2}$$

$$\omega_0 = \frac{kV_{GT}}{L(C_{GS,o} + C_{GS})}$$

For a device with a length of $0.3\mu m$ and an overdrive voltage of $0.2V$ ($k = 225\mu A/V^2$), the frequency is at $10.4GHz$ ($\tau = 15.31ps$).

Transistor Mismatch

Transistor size mismatch can be modelled as a gate-source voltage mismatch (σV_{gs}). This is shown in fig. A.10.

$$\sigma_{Vgs} = \frac{A_{Vgs}}{\sqrt{WL}} \tag{A.10}$$

It is seen that the gate-source mismatch voltage decreases with transistor size. In CMOS065 the mismatch coefficient is approximately $4mV\,\mu m$.

Transistor noise

Transistor noise can be modeled by eq. A.11. It is seen that the noise (power) is proportional to gm, and thus the output current.

$$\sigma_i = \sqrt{4k_B T B \gamma gm} = \sqrt{\frac{4k_B T B \gamma 2 I_D}{V_{GT}}} \tag{A.11}$$

with B the noise bandwidth, k_B the Bolzman constant, $\gamma = 2/3$ and T the absolute temperature.

Appendix B

Output resistance modulation - output voltage vs input signal

The output voltage of a D/A converter with output resistance modulation is evaluated in this section (see also section 2.1). A differential output model of a current-mode D/A converter is shown in figure B.1. In this figure, the output resistance of a channel is inversely proportional to the output current of the same channel. The output voltage is the difference between the two outputs (eq. B.1).
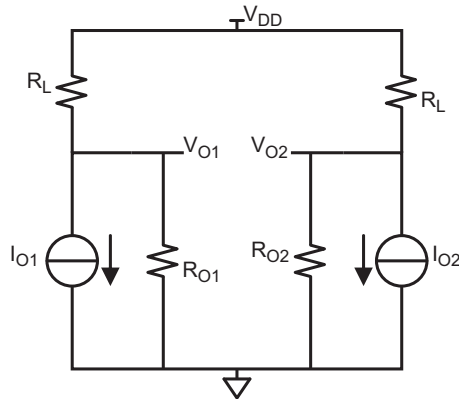

Figure B.1: D/A converter output stage modeling - finite current source output resistance

positive output

$$V_{O1} = V_{DD}\frac{R_{O1}}{R_{O1} + R_L} - I_{O1}\frac{R_{O1}R_L}{R_{O1} + R_L} \qquad \text{(B.1)}$$
$$= \frac{V_{DD}R_{O1} - I_{O1}R_{O1}R_L}{R_{O1} + R_L}$$

negative output

$$V_{O2} = \frac{V_{DD}R_{O2} - I_{O2}R_{O2}R_L}{R_{O2} + R_L}$$

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with:

$$R_{Ox} = \frac{R_T I_{FS}}{I_{Ox}}$$

Where R_L is the load resistance, R_T the full-scale output resistance (all sources are ON) I_{FS} the full-scale output current and V_{DD} the supply voltage. If both sides are equal (the same output resistance and load resistance):

$$
\begin{aligned}
V_{OUT} \quad &= \quad V_{O1} - V_{O2} \\
&= \quad \frac{V_{DD} R_T \frac{I_{FS}}{I_{O1}} - R_T I_{FS} R_L}{R_T \frac{I_{FS}}{I_{O1}} + R_L} - \frac{V_{DD} R_T \frac{I_{FS}}{I_{O2}} - R_T I_{FS} R_L}{R_T \frac{I_{FS}}{I_{O2}} + R_L} \\
&= \quad \frac{V_{DD} - R_L I_{O1}}{1 + \frac{R_L}{R_T} \frac{I_{O1}}{I_{FS}}} - \frac{V_{DD} - R_L I_{O2}}{1 + \frac{R_L}{R_T} \frac{I_{O2}}{I_{FS}}} \quad\quad\quad \text{(B.2)}
\end{aligned}
$$

with:

$$I_{O1} = I_{DC} - I_{IN}$$

and

$$I_{O2} = I_{DC} + I_{IN}$$

substituting and rewriting:

$$
\begin{aligned}
V_{OUT} \quad &= \quad \frac{V_{DD} - R_L I_{DC} + R_L I_{IN}}{1 + \frac{R_L}{R_T} \frac{I_{DC}}{I_{FS}} - \frac{R_L}{R_T} \frac{I_{IN}}{I_{FS}}} - \frac{V_{DD} - R_L I_{DC} - R_L I_{IN}}{1 + \frac{R_L}{R_T} \frac{I_{DC}}{I_{FS}} + \frac{R_L}{R_T} \frac{I_{IN}}{I_{FS}}} \\
&= \quad \frac{R_T}{R_T + R_L \frac{I_{DC}}{I_{FS}}} \Big(\frac{V_{DD} - R_L I_{DC} + R_L I_{IN}}{1 - \frac{R_L \frac{I_{IN}}{I_{FS}}}{R_T + R_L \frac{I_{DC}}{I_{FS}}}} - \frac{V_{DD} - R_L I_{DC} - R_L I_{IN}}{1 + \frac{R_L \frac{I_{IN}}{I_{FS}}}{R_T + R_L \frac{I_{DC}}{I_{FS}}}} \Big)
\end{aligned}
$$

with:

$$B = \frac{R_L \frac{I_{DC}}{I_{FS}}}{R_T + R_L \frac{I_{DC}}{I_{FS}}}$$

$$
\begin{aligned}
&= \quad \frac{R_T}{R_T + R_L \frac{I_{DC}}{I_{FS}}} \Big(\frac{V_{DD} - R_L I_{DC} + R_L I_{IN}}{1 - B \frac{I_{IN}}{I_{DC}}} - \frac{V_{DD} - R_L I_{DC} - R_L I_{IN}}{1 + B \frac{I_{IN}}{I_{DC}}} \Big) \\
&= \quad \frac{R_T}{R_T + R_L \frac{I_{DC}}{I_{FS}}} \frac{2 R_L I_{IN} + 2(V_{DD} - R_L I_{DC}) B \frac{I_{IN}}{I_{DC}}}{1 - B^2 \frac{I_{IN}^2}{I_{DC}^2}} \\
&= \quad \frac{2 R_T}{R_T + R_L \frac{I_{DC}}{I_{FS}}} \frac{1}{1 - B^2 \frac{I_{IN}^2}{I_{DC}^2}} \Big(R_L I_{IN} + \frac{(V_{DD} - R_L I_{DC}) \frac{I_{IN}}{I_{FS}} R_L}{R_T + R_L \frac{I_{DC}}{I_{FS}}} \Big) \\
&= \quad \frac{2 R_L R_T}{R_T + R_L \frac{I_{DC}}{I_{FS}}} \frac{I_{IN}}{1 - B^2 \frac{I_{IN}^2}{I_{DC}^2}} \Big(1 + \frac{V_{DD} - R_L I_{DC}}{R_T I_{FS} + R_L I_{DC}} \Big) \\
&= \quad \frac{2 R_L R_T I_{DC}}{R_T + R_L \frac{I_{DC}}{I_{FS}}} \Big(1 + \frac{V_{DD} - R_L I_{DC}}{R_T I_{FS} + R_L I_{DC}} \Big) \frac{I_{IN}/I_{DC}}{1 - B^2 \frac{I_{IN}^2}{I_{DC}^2}} \\
&= \quad V_0 \frac{I_{IN}/I_{DC}}{1 - B^2 \frac{I_{IN}^2}{I_{DC}^2}} \quad\quad\quad\quad\quad\quad\quad\quad\quad \text{(B.3)}
\end{aligned}
$$

Appendix C

Reference node disturbance - cascode charge injection

This section deals with the reference voltage disturbance as a function of the switching of a single section in a D/A converter. Refer to figure C.1 and section 3.1.
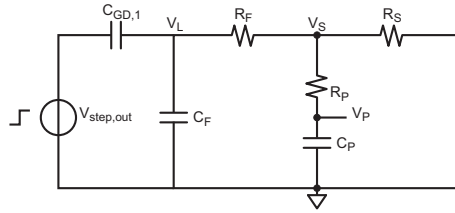
Figure C.1: Simplified small-signal equivalent of section

The transient response to a charge injection in C_F can be evaluated as shown in equation C.1

KCL, rewritten to voltage on node V_S

$$V_S = R_S C_F \frac{\delta V_L}{\delta t} + R_S C_P \frac{\delta V_P}{\delta t} \tag{C.1}$$

KVL

$$V_S = V_L + R_F C_F \frac{\delta V_L}{\delta t} \tag{C.2}$$

and

$$V_S = V_P + R_P C_P \frac{\delta V_P}{\delta t}$$

derivative

$$\frac{\delta V_S}{\delta t} = \frac{\delta V_P}{\delta t} + R_P C_P \frac{\delta^2 V_P}{\delta t^2} \tag{C.3}$$

rewriting C.1, integrating and solving to V_L

$$V_S - R_S C_P \frac{\delta V_P}{\delta t} = R_S C_F \frac{\delta V_L}{\delta t}$$

$$V_L = \frac{1}{R_S C_F} \int V_S \, dt - \frac{C_P}{C_F} V_P$$

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substitute in C.2

$$V_S = \frac{1}{R_S C_F} \int V_S \, dt - \frac{C_P}{C_F} V_P + \frac{R_F}{R_S} V_S - R_F C_P \frac{\delta V_P}{\delta t}$$

differentiating:

$$\frac{\delta V_S}{\delta t} = \frac{1}{R_S C_F} V_S - \frac{C_P}{C_F} \frac{\delta V_P}{\delta t} + \frac{R_F}{R_S} \frac{\delta V_S}{\delta t} - R_F C_P \frac{\delta^2 V_P}{\delta t^2} \qquad \text{(C.4)}$$

substitute C.3 in C.4

$$\frac{\delta V_P}{\delta t} + R_P C_P \frac{\delta^2 V_P}{\delta t^2} = \frac{1}{R_S C_F}(V_P + R_P C_P \frac{\delta V_P}{\delta t}) -$$

$$\frac{C_P}{C_F} \frac{\delta V_P}{\delta t} + \frac{R_F}{R_S}(\frac{\delta V_P}{\delta t} + R_P C_P \frac{\delta^2 V_P}{\delta t^2}) - R_F C_P \frac{\delta^2 V_P}{\delta t^2}$$

reordering

$$\frac{\delta^2 V_P}{\delta t^2}(R_P C_P(1 - \frac{R_F}{R_S}) + R_F C_P) + \frac{\delta V_P}{\delta t}(1 + \frac{C_P}{C_F}(1 - \frac{R_P}{R_S}) - \frac{R_F}{R_S}) - \frac{V_P}{R_S C_F} = 0$$
$$\text{(C.5)}$$

Solving the characteristic equation yields the time constants of the response on node V_P (solved with Maple, large expression)

$$V_P = A e^{\frac{t}{\tau_0}} + B e^{\frac{t}{\tau_1}}$$

The initial conditions are given by equation C.6.

$$V_P(0) = 0 \rightarrow A = -B \qquad \text{(C.6)}$$

After injection, the current through capacitor C_P can be expressed as follows

$$C_P \frac{\delta V_P}{\delta t} = I_P(0)$$

$$I_P(0) = \frac{V_{STEP}}{R_F + R_S // R_P}$$

$$I_P(0) = V_{STEP} \frac{R_S + R_P}{R_F(R_S + R_P) + R_S R_P}$$

Solving the time constants and initial conditions yields a transient signal that is present on the gates of the cascode transistors of *all* other devices.

Appendix D

Soft-switching - design equation derivations

In this appendix various design equations are derived and is only used for reference (see section 4.4).

D.1 Effective output current

This section evaluates the effective output current of a single section, refer to figure 4.8.

$$I_{OUT} = I_{HIGH} - I_{LOW} = \frac{1}{2}k\frac{W}{L}(V_{GT,H}^2 - V_{GT,L}^2) \tag{D.1}$$

with

$$V_{GT,H} = V_{REF} - V_{TH}$$

and

$$V_{GT,L} = V_{REF} - V_{TH} - V_D H = V_{GT,H} - V_D H$$

substituted in D.1

$$I_{OUT} = \frac{1}{2}k\frac{W}{L}(V_{GT,H}^2 - (V_{GT,H} - V_D H)^2)$$

$$I_{OUT} = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_D H - V_D H^2) = \frac{1}{2}k\frac{W}{L}V_D H(2V_{GT,H} - V_D H)$$

substituting $V_{GT,H}$

$$I_{OUT} = \frac{1}{2}k\frac{W}{L}V_D H(2(V_{REF} - V_{TH}) - V_D H) \tag{D.2}$$

D.2 Output current - mismatch transfer

This section evaluates the output current where an offset voltage is present which represents the (equivalent) mismatch of various devices and references, refer to figure 4.10 and section 4.4.1.

$$I_{OUT} = I_{HIGH} - I_{LOW} = \frac{1}{2}k\frac{W}{L}(V_{GT,H}^2 - V_{GT,L}^2) \tag{D.3}$$

with

$$V_{GT,H} = V_{REF} + V_{OS} - V_{TH}$$

and

$$V_{GT,L} = V_{REF} + V_{OS} - V_{TH} - V_D H = V_{GT,H} - V_D H$$

substituted in D.3

$$I_{OUT} = \frac{1}{2} k \frac{W}{L} (V_{GT,H}^2 - (V_{GT,H} - V_D H)^2)$$

$$I_{OUT} = \frac{1}{2} k \frac{W}{L} (2V_{GT,H} V_D H - V_D H^2) = \frac{1}{2} k \frac{W}{L} V_D H (2V_{GT,H} - V_D H)$$

substituting $V_{GT,H}$

$$I_{OUT} = \frac{1}{2} k \frac{W}{L} V_D H (2(V_{REF} + V_{OS} - V_{TH}) - V_D H) \qquad (D.4)$$

with

$$H = \frac{C_r(DT) + C_{r,0}}{C_r + C_{r,0} + C_h} = \frac{C_r(DT) + C_{r,0}}{C_c}$$

where

$$C_r = C_r(DT) + C_{r,a}(/DT)$$

D.3   Bias condition: Nominal transfer

This section evaluates the nominal transfer that is required. If the digital trim value is halfway its maximum, the output current should drop to the nominal *LOW* current. Refer to section 4.4.1, *Bias conditions*.

Given that the *LOW* current must be higher than the required trim range

$$I_{LOW} > I_{TRIM} = k \frac{W}{L} V_D H_0 \alpha \sigma_{V_{TH}} \qquad (D.5)$$

the nominal *LOW* drain-current (see section D.1)

$$I_{LOW} = \frac{1}{2} k \frac{W}{L} (V_{REF} - V_{TH} - V_D H_0)^2$$

thus

$$\frac{1}{2} (V_{GT,H} - V_D H_0)^2 > V_D H_0 \alpha \sigma_{V_{TH}} \qquad (D.6)$$

collecting H_0

$$\frac{1}{2} H_0^2 V_D^2 - H_0 (V_{GT,H} V_D + V_D \alpha \sigma_{V_{TH}}) + \frac{1}{2} V_{GT,H} > 0$$

the required nominal transfer

$$H_{0_{1,2}} = \frac{V_{GT,H} + \alpha \sigma_{V_{TH}} \pm \sqrt{(V_{GT,H} + \alpha^2 \sigma_{V_{TH}}^2)^2 - V_{GT,H}^2}}{V_D}$$

rewriting

$$H_{0_{1,2}} = \frac{V_{GT,H} + \alpha \sigma_{V_{TH}} \pm \sqrt{\alpha \sigma_{V_{TH}} + 2V_{GT,H} \alpha \sigma_{V_{TH}}}}{V_D}$$

assuming $V_{GT,H} \gg \alpha\sigma_{VTH}$

$$H_0 = \frac{V_{GT,H} - \sqrt{2V_{GT,H}\alpha\sigma_{VTH}}}{V_D} = \frac{V_{G,PP}}{V_D}$$

where $V_{G,PP}$ is the peak-peak gate voltage swing.

D.4 Trim sensitivity

In this section the sensitivity of the trim is derived ($S = \frac{\delta I_{OUT}}{\delta DT} = \frac{\delta I_{OUT}}{\delta H}\frac{\delta H}{\delta DT} = S_H\frac{\delta H}{\delta DT}$). Refer to section 4.4.2, *Trim sensitivity*. S_H is given in equation D.7.

$$S_H = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_D - 2V_D^2 H_0) \tag{D.7}$$

$$H(C_r(DT)) = \frac{C_r(DT) + C_{r,0}}{C_r(DT) + C_{r,a}(/DT) + C_{r,0} + C_h} \tag{D.8}$$

double-edge driving sensitivity

When two edges are used to drive the trim capacitors the equivalent capacitor can be modeled as is shown in equation D.9. DT is the digital trim signal normalized to 0 to 1 with a nominal value of 0.5.

$$C_r(DT) = C_{r,T}DT - C_{r,T}/DT \tag{D.9}$$

with

$$/DT = 1 - DT$$

where $C_{r,T}$ is the sum of all trim capacitances (constant). Rewriting D.9

$$C_r(DT) = C_{r,T}(2DT - 1)$$

note that

$$C_{r,T} = C_r(DT) + C_{r,a}(/DT)$$

substituting in equation D.8

$$H_1 = \frac{C_{r,T}(2DT - 1) + C_{r,0}}{C_{r,T} + C_{r,0} + C_h} = \frac{C_{r,T}(2DT - 1) + C_{r,0}}{C_c}$$

with a nominal transfer of ($DT = 0.5$)

$$H_{1_0} = \frac{C_{r,0}}{C_c}$$

and with the sensitivity to DT

$$S_1 = \frac{\delta H_1}{\delta DT} = \frac{2C_{r,T}}{C_c} \tag{D.10}$$

the total sensitivity of I_{OUT} becomes

$$S_{T,1} = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_D - 2V_D^2 H_0)\frac{2C_{r,T}}{C_c}$$

single-edge driving sensitivity

In the single edge driving solution the capacitors are either switched to ground or to the driving signal. Equation D.11 describes the transfer and sensitivity.

$$C_r(DT) = C_{r,T}DT \tag{D.11}$$

note that

$$C_{r,T} = C_r(DT) + C_{r,a}(/DT)$$

substituting in equation D.8

$$H_2 = \frac{C_{r,T}DT + C_{r,0}}{C_{r,T} + C_{r,0} + C_h} = \frac{C_{r,T}DT + C_{r,0}}{C_c}$$

with a nominal transfer of $(DT = 0.5)$

$$H_{2_0} = \frac{0.5C_{r,T} + C_{r,0}}{C_c}$$

and with the sensitivity to DT

$$S_2 = \frac{C_{r,T}}{C_c} = \frac{1}{2}S_1$$

the total sensitivity of I_{OUT} becomes

$$S_{T,2} = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_D - 2V_D^2 H_0)\frac{C_{r,T}}{C_c}$$

D.5 Hold capacitor size (C_c)

In this section the derivation of the total required hold capacitor is shown (C_c). Note that this equivalent capacitor is the sum of C_h, $C_{r,T}$ and C_0 (see also section 4.4.3, *Hold capacitor size*).

Evaluating the current ratio (see equation 4.9)

$$R = \frac{V_{GT,H}\sqrt{W_1 L_1}}{2\alpha A_{VT}} \tag{D.12}$$

where W_1 and L_1 are the dimensions of the current source transistor (M_0), and A_{VT} the mismatch coefficient (see section A). The 'total' required width of all current sources is $W_{TOTAL} = W_1(2^n - 1)$, substituting

$$R = \frac{V_{GT,H}\sqrt{W_{TOTAL}L_1}}{2\alpha A_{VT}\sqrt{2^n - 1}} = \frac{R_0}{\sqrt{2^n - 1}}$$

From the noise criteria the capacitor size is found

$$C_{ALL} = \frac{12C_T}{R} = \frac{12C_T\sqrt{2^n - 1}}{R_0}$$

where

$$C_T = (2^n - 1)C_c = \frac{SNR8k_BT}{V_{GT,H}^2}$$

Note the capacitance required at each current source

$$C_c = \frac{C_{ALL}}{4(2^n - 1)} = \frac{3C_T}{R_0\sqrt{2^n - 1}}$$

D.6 LSB trim capacitor size - C_{LSB}

The LSB trim capacitance size (which determines the trim resolution) is evaluated in this section. The INL of a thermometer coded D/A converter is evaluated in section 2.2.1 (equation D.13). Refer to section 4.4.2, *Trim accuracy - trim step*.

$$INL_{max,LSB} = \frac{1}{2}\frac{2^{nr}-1}{\sqrt{2^n-1}}\frac{\sigma_i}{\Delta I} \tag{D.13}$$

where, nr is the number of bits of the total converter (MSB and LSB section), ΔI the output current of a single section ($I_{HIGH} - I_{LOW}$) and σ_i the after-trim error residue.

$$\Delta I = \frac{1}{2}k\frac{W}{L}(V_{GT,H}^2 - V_{GT,L}^2)$$

where ΔI is the output current of a single section and

$$V_{GT,L}^2 = (V_{GT,H} - V_{G,PP})^2 = V_{GT,H}^2 - 2V_{GT,H}V_{G,PP} + V_{G,PP}^2$$

$$\Delta I = \frac{1}{2}k\frac{W}{L}(2V_{GT,H}V_{G,PP} - V_{G,PP}^2)$$

evaluating the integral non-linearity (substituting in D.13)

$$INL_{max,LSB} = \frac{2^{nr}-1}{\sqrt{2^n-1}}\frac{\sigma_i}{k\frac{W}{L}(2V_{GT,H}V_{G,PP} - V_{G,PP}^2)}$$

The error current of a single stage is given in equation D.14 and the resulting INL is given in equation D.15. σ_v is the maximum tolerable equivalent error voltage on the gate (V_{OS}). This means that the resolution of the trim should exceed this value. Note that the output current error (σ_i) is the average of the currents of two transistors; each channel (2 channels in a differential setup) is implemented in two sections with each $2^n - 1$ transistors.

$$\sigma_i = \frac{1}{\sqrt{2}}\frac{\delta I_{OUT}}{\delta V_{OS}}\sigma_v \tag{D.14}$$

from equation 4.6

$$\sigma_i = \frac{1}{\sqrt{2}}k\frac{W}{L}V_D H_0 \sigma_v = \frac{1}{\sqrt{2}}k\frac{W}{L}V_{G,PP}\sigma_v$$

$$INL_{max,LSB} = \frac{1}{\sqrt{2}}\frac{2^{nr}-1}{\sqrt{2^n-1}}\frac{V_{G,PP}\sigma_v}{2V_{GT,H}V_{G,PP} - V_{G,PP}^2} \tag{D.15}$$

$$= \frac{1}{\sqrt{2}}\frac{2^{nr}-1}{\sqrt{2^n-1}}\frac{\sigma_v}{2V_{GT,H} - V_{G,PP}}$$

rewriting

$$\sigma_v = \sqrt{2}INL_{max,LSB}\frac{\sqrt{2^n-1}}{2^{nr}-1}(2V_{GT,H} - V_{G,PP})$$

where

$$V_{STEP,LSB} = \frac{C_{LSB}}{C_c}V_D < \sigma_v$$

$$C_{LSB} < \sqrt{2}INL_{max,LSB}\frac{\sqrt{2^n-1}}{2^{nr}-1}\frac{2V_{GT,H} - V_{G,PP}}{V_D}C_c$$

D.7 Output transistor noise

The noise of a single transistor is shown in equation D.16 (see section 2.4.1). In equation D.17 the noise contribution of the output transistor of the 'soft' switching topology is given. Refer to section 4.4.3, *Output transistor noise*.

$$i_n^2 = 4k_B T \gamma B g m \tag{D.16}$$

with B the bandwidth and

$$gm = \sqrt{2k\frac{W}{L}I_D} = \frac{2I_D}{V_{GT}}$$

$$i_n^2 = 4k_B T \gamma B \frac{2I_D}{V_{GT}}[A^2/Hz]$$

$$I_{n,low}^2 = \frac{I_{n,high}^2}{\sqrt{R}} \tag{D.17}$$

where $I_{n,low}$ and $I_{n,high}$ are respectively the noise contribution of a transistor that carries a *low* and *high* current. Then the total noise contribution

$$I_{n,total}^2 = (2^n - 1)I_{n,high}^2 + 3(2^n - 1)I_{n,low}^2$$

$$I_{n,total}^2 = (1 + \frac{3}{\sqrt{R}})(2^n - 1)I_{n,high}^2$$

$$I_{n,total}^2 = (1 + \frac{3}{\sqrt{R}})(2^n - 1)4k_B T \gamma B \frac{2I_H}{V_{GT,H}}$$

$$I_{n,total}^2 = (1 + \frac{3}{\sqrt{R}})8k_B T \gamma B \frac{I_M}{V_{GT,H}}$$

Note that there are always $2^n - 1$ sources feeding a *high* current to an output, and $3(2^n - 1)$ sources that feed a *low* current to the output. The output current of a single current source is given by the *high* and *low* current difference

$$I_{OUT,M} = (I_H - I_L)(2^n - 1) = I_H(1 - \frac{1}{R})(2^n - 1) = I_M(1 - \frac{1}{R})$$

The output signal (differential output)

$$I_S^2 = \frac{I_{OUT,M}^2}{2}$$

and the total Nyquist signal-to-noise ratio

$$SNR = \frac{I_S^2}{I_{n,total}^2} = \frac{(1 - \frac{1}{R})^2}{1 + \frac{3}{\sqrt{R}}} \frac{I_M V_{GT,H}}{16k_B T \gamma B} \tag{D.18}$$

Appendix E

design equation derivations: direct switching - coarse and fine

In this appendix some derivations of design criteria are shown of the direct switching - coarse and fine implementation (see section 4.3).

E.1 Hold capacitor dimension

This section shows the derivation of the hold capacitor size with respect to noise contribution of the direct switching (coarse and fine) implementation. The voltage noise of a hold capacitor is shown in equation E.1

$$\sigma_v^2 = \frac{k_B T}{C_h} \tag{E.1}$$

with

$$I_{M_1} = N I_{OUT}$$

and

$$gm_1^2 = \frac{4N^2 I_{OUT}^2}{V_{GT,1}^2}$$

$$\sigma_i^2 = \frac{k_B T}{C_h} \frac{4N^2 I_{OUT}^2}{V_{GT,1}^2} = \sigma_v^2 gm_1^2$$

total noise contribution into the output (assuming n-bit thermometer coded output section)

$$i_n^2 = (2^n - 1)\sigma_i^2$$

the signal level

$$i_s^2 = \frac{i_m^2}{2}$$

with

$$i_m = (2^n - 1) I_{OUT}$$

signal-to-noise ratio

$$SNR = \frac{C_h V_{GT,1}(2^n - 1)}{8N^2 k_B T}$$

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and the required (total) hold capacitance

$$C_T = (2^n - 1)C_h = \frac{8SNRk_BTN^2}{V_{GT,1}^2} \tag{E.2}$$

E.2 Coarse and fine trim - current ratio N

This section shows how the current and device ratio N should be chosen.

Device mismatch

$$\sigma_{v_x}^2 = \frac{A_{VT}^2}{W_x L} \tag{E.3}$$

$$\sigma_{i_x}^2 = \frac{A_{VT}^2}{W_x L} gm_x^2$$

with

$$gm_x^2 = \frac{4I_{D,x}^2}{V_{GT,x}^2}$$

$$\sigma_{i_x}^2 = \frac{A_{VT}^2}{W_x L} \frac{4I_{D,x}^2}{V_{GT,x}^2}$$

given that

$$I_{M_1} = NI_{OUT}$$

which implies

$$I_{M_0} = (1 - N)I_{OUT}$$

$$W_{M_0} = (1 - N)W_T$$

and

$$W_{M_1} = NW_T$$

the mismatch of the devices

$$\sigma_{i_0}^2 = \frac{A_{VT}^2}{W_0 L} \frac{4I_{M_0}^2}{V_{GT,0}^2}$$

substituting variables

$$\sigma_{i_0}^2 = \frac{A_{VT}^2}{W_T(1 - N)L} \frac{4(1 - N)^2 I_{OUT}^2}{V_{GT,0}^2}$$

and

$$\sigma_{i_1}^2 = \frac{A_{VT}^2}{W_T L} \frac{4NI_{OUT}^2}{V_{GT,1}^2}$$

then, the total mismatch is the sum of both

$$\sigma_{i_T}^2 = \frac{A_{VT}^2}{W_T L} 4I_{OUT}^2 \left(\frac{1 - N}{V_{GT,0}} + \frac{N}{V_{GT,1}} \right)$$

when the overdrive voltages are equal this reduces to

$$\sigma_{i_T}^2 = \frac{A_{VT}^2}{W_T L} \frac{4I_{OUT}^2}{V_{GT}^2} = \frac{\sigma_{v_T}^2}{V_{GT}^2} 4I_{OUT}^2$$

the required trim range ($\alpha\sigma$ trim range)

$$i_{M_1} = NI_{OUT} > \alpha\sigma_{i_T}$$

$$N > \frac{\alpha\sigma_{i_T}}{I_{OUT}} = \alpha\frac{A_{VT}}{\sqrt{W_T L}}\frac{2}{V_{GT}}$$

Appendix F

Jitter

This appendix deals with the derivation of various jitter equations.

F.1 Dynamic SNR with clock jitter

This section the signal to noise ratio is derived. This means that due to clock jitter in combination with an input signal 'white' noise is generated at the output. Refer to section 5.3, *Main clock jitter transfer*. Number of 'steps' in a cycle

$$\frac{\delta D_{IN}}{\delta T_s} = \frac{\delta D_{IN}}{\delta t}\frac{\delta t}{\delta T_s}.$$

with D_{IN} the digital input value

$$D_{IN} = (2^n - 1)(\frac{1}{2} - \frac{1}{2}\cos{(\omega_{in}t)})$$

$$\frac{\delta D_{IN}}{\delta T_s} = \frac{2^n - 1}{2}\sin{(\omega_{in}t)}\frac{\omega_{in}}{2\pi}T_s$$

Note that the derivative needs to be normalized to 'steps' per second and not 'radians' per second (divide by 2π). The error output charge is then

$$\sigma_{Q,T} = \frac{\delta D_{IN}}{\delta T_s}\sigma_{Q,c} = (2^n - 1)\sin{(\omega_{in}t)}\frac{\omega_{in}}{2\pi}T_s\sigma_T I_H$$

the average output error current then is

$$\sigma_{I,RMS} = (2^n - 1)\frac{\omega_{in}}{\sqrt{2}2\pi}\sigma_T I_H = \frac{\omega_{in}}{\sqrt{2}2\pi}\sigma_T I_M =$$

the signal power

$$I_S^2 = \frac{I_M^2}{2}$$

signal-to-noise ratio

$$SNR_{dB} = 10\log{(\frac{4\pi^2}{\omega_{in}^2\sigma_T^2})} = 20\log{(\frac{T_{in}}{\sigma_T})}$$

where T_{in} is the period of the input signal.

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F.2   Logic gate jitter

In this section the added jitter of a digital gate ($NAND$, NOR, inverter, etc.)
is derived. Refer to figure 5.12 (see also section 5.3, *Cell jitter*).

$$V^2_{N,OUT} = i^2_{N,t} |\frac{R_L}{1 + j\omega R_L C_L}|^2$$

where $V^2_{N,OUT}$ is the noise power spectral density, $i_{N,t}$ the equivalent current
noise spectral density noise of all transistors. The output noise power

$$V^2_{N,OUT,T} = \int_0^\infty i^2_{N,t} |\frac{R_L}{1 + j\omega R_L C_L}|^2 \, d\omega \approx \int_0^{\omega_c} i^2_{N,t} R_L^2 \, d\omega$$

where ω_c is the cut-off frequency $(1/R_L C_L)$

$$V^2_{N,OUT,T} = i^2_{N,t} R_L^2 \omega_c = i^2_{N,t} \frac{R_L}{C_L}$$

note that (when there is no resistive load)

$$Mu = gmR_L$$

$$V^2_{N,OUT,T} = i^2_{N,t} \frac{Mu}{gmC_L}$$

with (MOS model, see section A.11)

$$i_{N,t} = 2kT\gamma gm$$

$$V^2_{N,OUT,T} = \frac{2kT\gamma}{C_L} Mu$$

This voltage (with the threshold voltage of the next stage) transfers to timing
jitter

$$\frac{\delta V_{OUT}}{\delta t} \sigma_T = \sigma_V \qquad\qquad\qquad (F.1)$$

rewriting

$$\frac{\delta t}{\delta V_{OUT}} \sigma_V = \sigma_T = \sqrt{\frac{2kT\gamma Mu}{C_L}} \frac{1}{S}$$

where $S[V/s]$ is the slope of the output signal.

Appendix G

Hold function - sinc filtering

This appendix shows the derivation of the signal-to-noise degradation due to the sinc filtering effect that occurs when a 'hold' function is used (in comparison with 'ideal' sampling).

Note that the 'hold' function can be modelled as an over-sampled hold signal (i.e. time shifted versions of the input signal combined).

The input 'reference' signal is a time-shifted signal, this would then be the middle of a pulse-shaped signal.

$$S_1 = A_0 \sin\left(\omega_0(t - T_0)\right)$$

with

$$T_0 = \frac{1}{2fs}$$

where fs is the sample-frequency. A delayed version of this signal

$$S_x = A_0 \sin\left(\omega_0(t - T_0) - \phi\right)$$

with

$$\phi = 2\pi \frac{i \Delta T}{T_{in}}$$

where T_{in} is the input signal period time $(1/f_{in})$ and integer i

$$i = -\frac{OSR - 1}{2} \cdots \frac{OSR - 1}{2} = -N \cdots N$$

and

$$\Delta T = \frac{T_s}{OSR}$$

where T_s is the sample period and OSR the over-sampling ratio. Substituting

$$S_x = A_0 \sin\left(\omega_0(t - T_0) - \frac{2\pi f_{in} i}{fsOSR}\right)$$

rewriting the phase difference to a cosine and sine part

$$S_x = A_0 S_{x,s} \sin\left(\omega_0(t - T_0)\right) + A_0 S_{x,c} \cos\left(\omega_0(t - T_0)\right)$$

where

$$S_{x,s} = \cos\left(-\frac{2\pi f_{in} i}{fsOSR}\right)$$

and

$$S_{x,c} = \sin\left(-\frac{2\pi f_{in} i}{f_s OSR}\right)$$

adding the sine and cosine part of the output signal

$$S_{x,s,sum} = \sum_{i=-N}^{N} S_{x,s} = \sum_{i=-N}^{N} \cos\left(-\frac{2\pi f_{in} i}{f_s OSR}\right)$$

with $\cos(x) = -\cos(x)$

$$S_{x,s,sum} = 1 + 2\sum_{i=1}^{N} \cos\left(\frac{2\pi f_{in} i}{f_s OSR}\right)$$

the sine part (due to symmetry) is zero ($\sin(x) = -\sin(-x)$ and $\sin(0) = 0$)

$$S_{x,c,sum} = \sum_{i=-N}^{N} \sin\left(-\frac{2\pi f_{in} i}{f_s OSR}\right) = 0$$

Then, the output voltage amplitude transfer

$$|H(f_{in})| = 1 + 2\sum_{i=1}^{N} \cos\left(\frac{2\pi f_{in} i}{f_s OSR}\right)$$

rewriting sum to integral (valid for large N)

$$\begin{aligned} |H(f_{in})| &= 1 + 2\int_{i=1}^{N} \cos\left(\frac{2\pi f_{in} i}{f_s OSR}\right) di \\ &= 1 + 2\frac{f_s OSR}{2\pi f_{in}}\left(\sin\left(\frac{2\pi f_{in} N}{f_s OSR}\right) - \sin\left(\frac{2\pi f_{in}}{f_s OSR}\right)\right) \end{aligned}$$

note that $N = \frac{OSR-1}{2}$

$$|H(f_{in})| = 1 + 2\frac{f_s(2N+1)}{2\pi f_{in}}\left(\sin\left(\frac{2\pi f_{in} N}{f_s(2N+1)}\right) - \sin\left(\frac{2\pi f_{in}}{f_s(2N+1)}\right)\right)$$

for large N this reduces to

$$|H(f_{in})| \approx 1 + 2\frac{f_s N}{\pi f_{in}}\sin\left(\frac{\pi f_{in}}{f_s}\right) = 1 + 2N sinc\left(\frac{\pi f_{in}}{f_s}\right)$$

when normalized to Low-Frequency transfer

$$|H(f_{in})| = 1 + 2N sinc\left(\frac{\pi f_{in}}{f_s}\right)$$

Thus, the signal and noise spectrum is shaped with this function. The output noise power is described by the following

$$P_{Noise} = \int_{0}^{\frac{f_s}{2}} |H(f_{in})|^2 PSD_0 \, df_{in} = \int_{0}^{\frac{f_s}{2}} |H(f_{in})|^2 \frac{2P_{N,0}}{f_s} \, df_{in}$$

$$\frac{P_{Noise}}{P_{N,0}} = \int_0^{\frac{fs}{2}} 2\frac{|H(f_{in})|^2}{fs}\, df_{in}$$

where PSD_0 is the noise floor ($2P_{N,0}/fs$, with $P_{N,0}$ the total (original) noise power). Thus, the signal to noise reduction is given by

$$\Delta SNR = \frac{|H(f_{sig})|^2}{P_{Noise}/P_{N,0}}$$

substituting

$$\Delta SNR = \frac{|1 + 2Nsinc(\frac{\pi f_{sig}}{fs})|^2}{\int_0^{\frac{fs}{2}} 2\frac{|1+2Nsinc(\frac{\pi f_{in}}{fs})|^2}{fs}\, df_{in}}$$

For large OSR ($N \to \infty$) this reduces to

$$\Delta SNR = \frac{|sinc(\frac{\pi f_{sig}}{fs})|^2}{\int_0^{\frac{fs}{2}} 2\frac{|sinc(\frac{\pi f_{in}}{fs})|^2}{fs}\, df_{in}}$$

which reduces to (evaluate integral)

$$\Delta SNR = 1.2925|sinc(\frac{\pi f_{sig}}{fs})|^2$$

Appendix H

MatLab code - quantization error estimation and subtraction

```
Tstart = 50e-9;
Tend = 150e-9;
fhigh = 1e9;
delta = Tend-Tstart;
M = 101;
N = 49;
OSR = 1000;
fin = N/delta;
Fs = M/delta;
trise = 0;%5e-12;
tdelay = 0;%-50e-9/M;%10e-9;
Tstep = 1/Fs/OSR;
t = (Tstart+1/2/OSR/Fs:Tstep:Tend);

%Load cadence data and interpolate
out = ipolcaddata('IDEAL_CASC_11.csv',t);

%evaluate the power spectral density
[f,fout] = fftb(out, Fs, OSR);
foutdb = fft2db(fout, 1);

%evaluate the nyquist signal-to-noise ratio
SNROld = SNREval(fout, Fs, fin, OSR)

torig = (Tstart:1/Fs:Tend-1/2/Fs);

%the originating signal
origp = 128+128*sin(2*pi*fin*(torig-tdelay+1/2*trise));

%a quantized version of the signal
orig_qp = round(origp+0.50);
for(i=1:1:length(orig_qp))
    if(orig_qp(i) == 129)
```

```
        orig_qp(i) = 128;
    end
end

%differential quantized signal
orig_q = -orig_qp+(256-orig_qp)+1;

%apply the hold function
orig2 = zeros(1,length(orig_qp)*OSR);
orig2_q = zeros(1,length(orig_qp)*OSR);

for(i=1:OSR:length(out))
    for(j=0:1:OSR-1)
        orig2(i+j) = origp((i-1)/OSR+1);
        orig2_q(i+j) = orig_q((i-1)/OSR+1);
    end
end

%shift the signal in time domain (one period total delay in digital part)
shift = -OSR+1;
orig2 = shiftdata(orig2, shift);
orig2_q = shiftdata(orig2_q, shift);

% resize signal (differential)
orig2 = -2*(orig2-128);

%use cross-correlation for finding optimum timing!
%for(i=0:1:2*OSR)
% shift = i;
% temp = orig2_q(length(orig2_q)-shift:length(orig2_q));
% shifted(shift+2:length(orig2_q)) = orig2_q(1:length(orig2_q)-shift-1);
% shifted(1:shift+1) = temp(1:shift+1);
% corr(i+1) = sum(shifted.*out);
%end
%plot(corr);

% when optimal timing is found, the value should be assigned to timcomp
timcomp = -64;
%quantized signal
shifted = shiftdata(orig2_q, timcomp);
%non-quantized signal
shiftednq = shiftdata(orig2, timcomp);

%in evaluating the unit step, the normalized signal:
units = out./shifted;

% this routine collects signals that have larger than 0.1*max output signal
% (small signals tend to have a large relative error, we do not incorporate
% this in the evaluation of the average 'step')
cnt = 0;
```

```
maxa = max(shifted);
sumunit = zeros(1, OSR);
for(i=1/2*OSR:OSR:length(shifted)-OSR)
   if(abs(shifted(i)) > 0.1*maxa)
       for(j=0:1:OSR-1)
           sumunit(j+1) = sumunit(j+1) + units(i+j-1);
       end
       cnt = cnt+1;
   end
end

%the unit step:
sumunit = sumunit/cnt;

%shift the data back to zero
sumunit = shiftdata(sumunit, -1/2*OSR-timcomp+3);
%the actual quantization error
qerror = (shifted-shiftednq);

%outx will be the rebuilt quantization error signal
timcomp = -timcomp;
outx(1:timcomp) = sumunit(length(sumunit)-timcomp+1:length(sumunit)).*qerror(1:timcomp);
for(i=timcomp+1:OSR:length(shifted)-OSR)
    outx(i:i+OSR-1) = sumunit.*qerror(i:i+OSR-1);
end
outx(length(qerror)-length(sumunit)+timcomp+1:length(qerror)) =
sumunit(1:length(sumunit)-timcomp).*
qerror(length(qerror)-length(sumunit)+timcomp+1:length(qerror));

%subtract quantization error from output signal and determine spectrum
fudge = 1.039;
[f,ferrcmp] = fftb(out-fudge*outx, Fs, OSR);
ferrcmpdb = fft2db(ferrcmp, 1);

%the 'new' signal to noise ratio
SNRNew= SNREval(ferrcmp, Fs, fin, OSR)

%plot results
fstop = 101;
figure;
%error compensated signal
plot(f(2:fstop), ferrcmpdb(2:fstop),'red');
hold on;
%original signal
plot(f(2:fstop), foutdb(2:fstop));
```

Bibliography

[1]   3rd Generation Partnership Project *Technical Specification Group Radio Access Networks; UE Radio Transmission and Reception (FDD)*, Release 5, 2002, 3GPP Organizational Partners (ARIB, CWTS, ETSI, T1, TTA,TTC).

[2]   Lin, C-H., van der Goes, F., Westra, J., Mulder, J., Lin, Y., Arslan, E., Ayranci, E., Liu, X., Bult, K., *A 12b 2.9GS/s DAC with IM3 − 60dBc beyond 1GHz in 65nm CMOS*, Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International , vol., no., pp.74-75,75a, 8-12 Feb. 2009

[3]   Doris, K., Van Roermund, A., Leenaerts, D. *Wide-Bandwidth High Dynamic Range D-A Converters*, Springer, 2006