UNIVERSITY OF TWENTE.

A Simulation Study and Analysis of advanced Silicon Schottky Barrier Field Effect Transistors

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1. Introduction and Motivation

Ever since the MOSFET made its debut in the world of electronics, device performance and functionality increases were mostly obtained due to the aggressive down scaling methods upheld by the industry. The first scaling method used was the so called constant field scaling method proposed in 1972 [1]. As the name implies this method was based on keeping a constant electric field throughout the channel length of the MOSFET by means of scaling down voltages and device dimensions by a certain factor κ and conversely up scaling doping concentrations (N_A, N_D) by that same factor. This allowed the power consumed per area (power density) to remain constant while the circuit delay went down by κ and the circuit density increased with κ^2. Although appealing true constant field scaling was never widely applied since the industry (up to the ~1 μm node) preferred a method closer to constant voltage scaling. This method as the name implies keeps the supply voltage at certain predetermined voltage nodes (i.e. at 5V, 3.3V, 1.5V, 0.9V etc) while down scaling device dimensions, only switching to lower nodes when reliable operation due to increasing electric fields is not possible. The constant voltage scaling is a specific application of the "general scaling" [2] method which until recently was the main downscaling guideline. This guideline allowed the electric field to be increased by a factor α and power density by α^3 (or α^2 if velocity saturated) while circuit delay and density still improved. However V_{DD} and device speed scaling according to this generalized scaling method slowed down drastically to manage the increasingly high power dissipation levels. The limitations facing scaling of *conventional MOSFET* nowadays however are not easily circumvented due to the fact that some fundamental barriers, such as the 60mV/dec subthreshold[1] swing (S), simply cannot be surpassed.
The subthreshold swing of a conventional long channel MOSFET is given by:

$$\textbf{(Eq. 1)} \qquad S = \frac{dV_{gs}}{d(\log I_d)} = \frac{kT}{q} \ln(10)(1 + \frac{C_{dm}}{C_{ox}}) \quad ,$$

with C_{ox} the oxide capacitance and C_{dm} the bulk depletion capacitance, T the temperature and the rest fundamental constants. It is clear that at a fixed temperature there are not many variables one can engineer to improve the subthreshold swing. Assuming thin effective oxide thicknesses ($C_{ox} >> C_{dm}$) and room temperature the subthreshold swing therefore converges to 60mV/dec without much possibility of further improvement. The semiconductor industry has consequently after 4 decades of somewhat straight forward downscaling entered "the era of material-limited device scaling"[3], where short-channel issues such as channel transportation limitations, source – drain electrostatic coupling, gate tunneling and other quantum/parasitic effects have become major problems.
The dawn of this new era has therefore created a widespread interest across all fronts in novel FET designs and materials to obtain better performance as we scale to the sub 50nm regime. When it comes down to scaling in this new era one can divide the development into two main camps. The "long-channel like" camp and the "new injection mechanism" camp. The "long channel like" camp focuses mainly on novel

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[1] Change in gate voltage that must be applied in order to create a one decade increase in output current, which limits the on/off current ratio of the conventional MOSFET

engineering solutions to create improved device architectures. For instance the introduction of new gate dielectrics (high-k materials), high mobility bulk materials (strained Si, SiGe etc) and novel designs with great electrostatic control, like the increasingly popular FinFET [4], belong to this camp.

This development route wants to minimize the above mentioned short channel issues to create sub 50 nm devices which are more "long-channel" like in their behavior.

A more elegant and certainly more, long term focused approach however is that of the "new injection mechanism" camp. As the name implies this camp focuses on the exploitation of new transport mechanisms and physical phenomena made possible due to new materials and small device dimension. FETs belonging to this camp should therefore in theory not be limited by the diffusion based 60mV/dec subthreshold swing barrier. Devices based on band to band tunneling [5, 6] or those that utilize source side impact ionization like the IMOS[7-9] are some examples of devices that utilize source-channel transport mechanisms other than diffusion which were able to break the fundamental subthreshold barrier.

The novel device designs in both camps usually have one thing in common which is ease of integration in the existing CMOS semiconductor infrastructure. The Schottky Barrier MOSFET [3] is such a device.

A Schottky barrier (SB-)FET is a MOSFET in which the doped silicon source and/or drain is replaced with a metallic (typically silicided) source/drain, with the actual SB (junction) forming at the metal semiconductor (MS) interface.

One of the main advantages of metals is their intrinsically high conductivity (σ), allowing junction depths (r_j) and obviously widths (W) to be scaled down drastically while still maintaining low parasitic S/D (R_S, R_D) resistances.

(Eq. 2)
$$R_S, R_D \propto 1/\sigma W r_j$$

This for example allows for the reduction of short channel effects (SCE's) without the added complexity of using techniques such as shallow S/D extensions, halo implants etc. The use of metallic source and drains was also shown [10] to lead to SB-FETs being immune to parasitic bipolar actions like latchup. Furthermore the low-thermal budget, abrupt metal/semiconductor junctions, integration on novel bulk semiconductors (i.e. CdS [11]) and the overall ease of fabrication make these devices a viable candidate for the deca-nanometer range.

The idea of completely replacing doped S/Ds with metal is by no means a new one as Nishi proposed doing this in his submitted Japanese patent in 1966 [12], while Lepselter and Sze published a paper on this type of device in 1968 [13]. The first actual surge in SB-FET research however came in the 80s with the introduction of the first SB-NMOS device [14], the first asymmetric Schottky device [15] and devices employing S/D channel interfacial layers (i.e. [9]). Although this era provided the proof of concept it was only since 1994, after Tucker *et al.*[16] saw the advantages of implementing SB-FETs in advanced process technology that a new surge of interest in these devices was awoken. SB junctions have since been incorporated in everything from the standard symmetric SB-MOSFET to FinFETs [17, 18] and nanowires [19].

1.1.   Motivation and goal

The goal of this work is to investigate, through device simulations and a literature study, various device characteristics across both symmetric and asymmetric SB-FET designs while focusing on expanding the characterization of the novel asymmetric Schottky Tunneling Source SOI MOSFET (STS-FET) proposed by Jhaveri in [20-23]. This asymmetric field effect transistor uses gate controlled Schottky tunneling as the (source) current injector and an Ohmic junction (created using a highly doped drain-side pocket implant) at the drain. The main strength of this asymmetric SOI design, as was shown earlier on bulk Si [15], is the reduction of the channel resistance and the high drain leakage currents (caused by ambipolar conduction) plaguing so many of the symmetric SB device concepts. With the knowledge obtained from the aforementioned simulation study a new *full-metal* asymmetric device, the so-called asymmetric Gate (AsymG) SB-FET, is proposed, designed, simulated and compared with other (in particular Jhaveri's) SB-FETs obtained from literature.

1.2.   Outline

This thesis is outlined as follows:
Chapter 2 focuses on the Metal Semiconductor contact and the physics governing the carrier flow through these junctions.
Chapter 3 introduces the Schottky barrier FET, the difference between diffusion and tunneling limited SB-FETs and highlights some of the pros and cons of the symmetric and asymmetric SB-FET designs.
Chapter 4 focuses on device simulation calibration and the expansion of some of the more detailed (DC) aspects of the asymmetric SB-FET as proposed by Jhaveri *et al* [20-23].
Chapter 5 introduces the newly proposed asymmetric full-metal Schottky barrier FET.
And finally conclusions are drawn as well as possible future directions and recommendations are given.

2. Metal-Semiconductor (MS) Contacts

With respect to the device behavior, the main difference between conventional MOSFETs (highly doped semiconductor S/D) and Schottky-FETs (metallic S/D) lies in the channel current injection mechanism. To better understand and highlight these differences this chapter will treat carrier flow through MS contacts.

2.1.   MS Contacts in equilibrium

For MS contacts [24] at equilibrium, *work function*[2] ($\Phi_{M,S}$), *electron affinity*[3] (χ) and the resulting *Schottky Barrier Height*[4] (Φ_B or SBH in general) are the most important factors determining the type of MS-contact.

$$\Phi_M = E_0 - E_{FM}$$
$$\Phi_S = E_0 - E_{FS}$$
$$\chi = E_0 - E_c$$
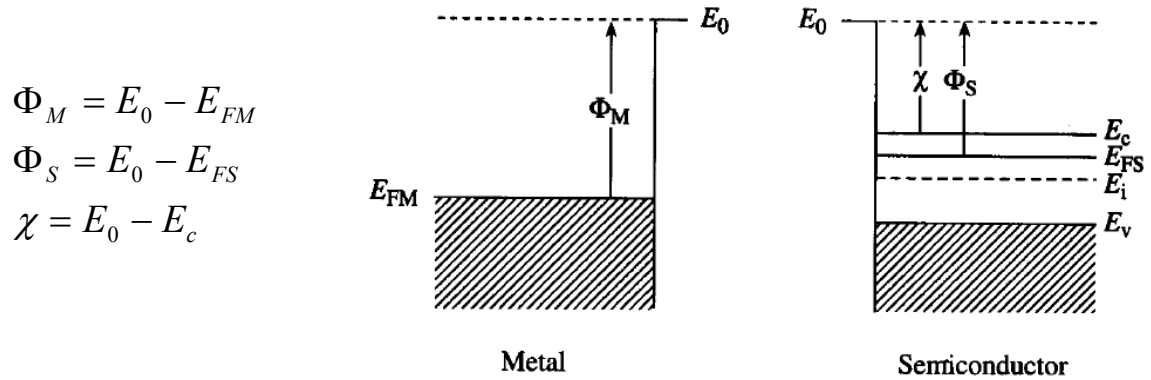
Figure 2.1: Metal and Semiconductor schematic band diagrams depicting the work functions Φ_M, Φ_S, electron affinity χ and how to calculate them. The parameters E_c, E_v, $E_{FM,S}$, E_i, and E_0 are respectively, the (bottom of the) conduction band energy, (top of the) valence band, the Fermi level, the intrinsic Fermi level, and the vacuum energy level.[25]

The workfunction is considered to be a metal characteristic since the Fermi level of a metal (E_{FM}) is constant with respect to the free electron energy (E_0). For semiconductors on the other hand the workfunction is not constant and therefore cannot be considered a semiconductor characteristic because the Fermi level of the semiconductor (E_{FS}) changes depending on doping. The electron affinity however is constant and therefore considered a semiconductor specific characteristic. When a MS-contact is created these two material properties determine (in the ideal case) the characteristic MS-junction Schottky Barrier Heights (Φ_{Bn}, Φ_{Bp} Figure 2. 2 (a) and (b), or SBH in general). It is this SBH that will form the most important parameter throughout this work in explaining observed device behavior.

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[2] The amount of energy needed for an average electron to reach the free electron energy level E_0

[3] The amount of energy required to free an average conduction band electron

[4] Energy barrier to be surmounted by carriers (Φ_{bn} – electrons , Φ_{bp} – holes) moving from metal to semiconductor

It should be noted that when taking into account N- and P-type semiconductors together with the fact that Φ_M can be either larger or smaller than Φ_S, 4 separate cases of MS-contacts can be distinguished. Among these cases the 2 most relevant to situations occurring in SB-FETs, are shown in Figure 2. 2 a and b.
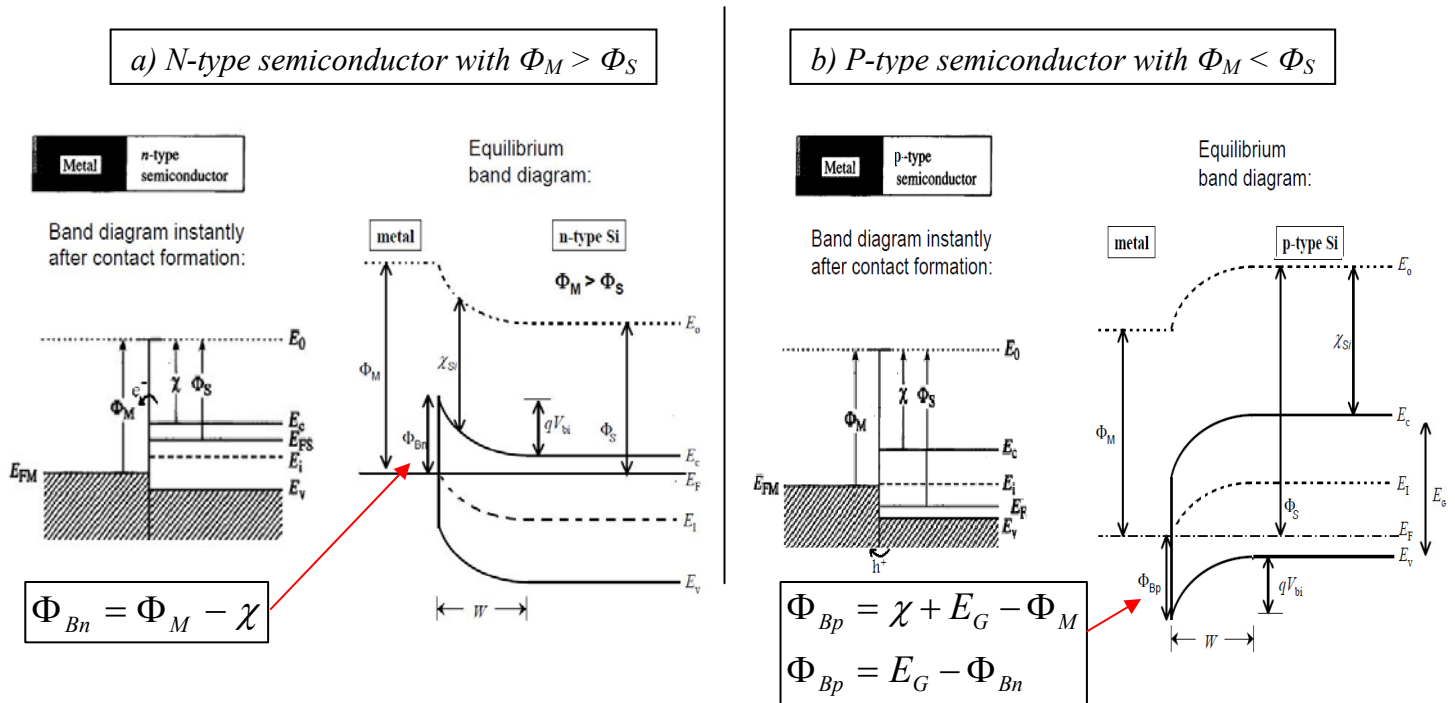
Figure 2. 2: Schematic band diagrams of two types of MS-contacts[25]:
(a) $\Phi_M > \Phi_S$, an n-type Schottky contact
(b) $\Phi_M < \Phi_S$, a p-type Schottky contact

a) N-type semiconductor with $\Phi_M > \Phi_S$:
For this situation with $\Phi_M > \Phi_S$ reaching equilibrium means that there is a net electron flow from the semiconductor surface contact region to the metal. This net electron flow leaves behind ionized dopants (N_D^+) through a depletion layer width (W) resulting in an E-field (proportional to the slope of the bands) and a built-in potential drop V_{bi}. A similar situation occurs in an SB-FET with an applied positive gate bias which will be discussed chapter 3.

b) P-type semiconductor with $\Phi_M < \Phi_S$:
This is basically the inverse of (a) in which mobile electrons flow from metal to semiconductor before reaching thermal equilibrium. A similar situation as seen in this band diagram occurs in SB-FETs when the applied gate bias is negative. It is important to note the inverse/complementary nature of Φ_{Bp} compared to Φ_{Bn}, since it will be important in explaining the ambipolar behavior of the symmetric SB-FET.

In both cases a so-called Schottky (potential) barrier is formed. This barrier can be controlled by the applied bias at the MS-contact which is important for the realization of switches or rectifiers (diodes).

2.2.   Schottky diode current flow

As thermionic emission forms an integral part of the SB-FET current injection, a short qualitative analysis of this mechanism with respect to the Schottky diode will be given.
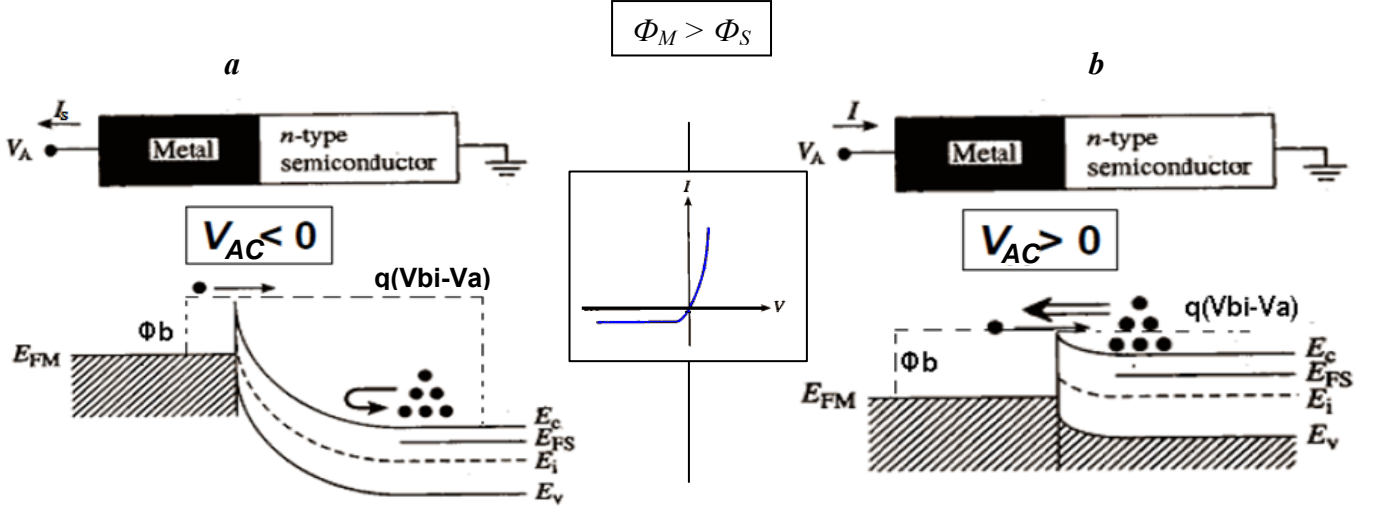

Figure 2.3: Qualitative view of the Schottky diode under reverse (a) and forward (b) bias [25]

Thermionic emission theory:

When applying a *forward* bias (V_{AC}>0V) to a MS-contact (meaning a positive potential on the anode) the potential drop across the interface region reduces (Figure 2.3(b)). This reduction results in a potential barrier decrease seen by mobile electrons flowing from S→M allowing for an exponential[5] increase (area on the right of the I-V curve in Figure 2.3) in the cross barrier current. When applying a *reverse bias (*Figure 2.3(a), V_{AC}<0V*,* increasing S→M barrier*)* therefore this S→M cross barrier current is exponentially reduced. Furthermore since the SBH or Φ_B is not influenced by the applied bias[6] there is always a constant cross barrier M→S electron flow (Figure 2.3(a) and (b)). This relatively small negative flow is overshadowed in the case of the large forward bias (S→M) electron flow (Figure 2.3(b)), but becomes visible as the saturation current when reverse biasing (Figure 2.3(a)). Deriving the 1D equation for this barrier height dependent thermionic emission (TE, J_{TE}) current (see Appendix A or [11]) leads to:

(Eq. 3)
$$J_{TE} = \left[A^* T^2 \exp(-\frac{q\Phi_B}{kT}) \right] \, ,$$

where A^* is the effective Richardson's constant[7].

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[5] The Fermi Dirac statistics predict that there is an exponential decline in the probability that available states will be filled for increasing energy levels above the conduction band [11]

[6] not including image force barrier lowering

[7] The Richardson's constant characterizes the number of electrons at the interface having enough energy and the correct direction of velocity to cross the barrier

Eq.(4) describes a total diode current density similar to conventional PN diodes ,albeit with saturation current densities that are quite different:

(Eq. 4)
$$J_n = J_{TE}\left[\exp(\frac{qV_A}{kT}) - 1\right] \ .$$

The exponential term describes the S→M electron flux, while the -1 term describes the M→S electron flux. Hence, the TE current is limited by the SBH only, while the diffusion current flowing through a conventional (short base) PN diode, is also affected by its device dimensions.

Tunneling current:

The total current density across a Schottky barrier consists not only of the thermionic emission component (J_{TE}) but also of a field assisted (thermionic) tunneling component ($J_{(T)FE}$)[26]. This tunneling current will however only start to play a (significant) role when the depletion/tunneling width (W_{tun}, figure 2.4) is < 10 nm [11].

(Eq. 5)
$$J_{TOT} = J_{TE} + J_{(T)FE}$$
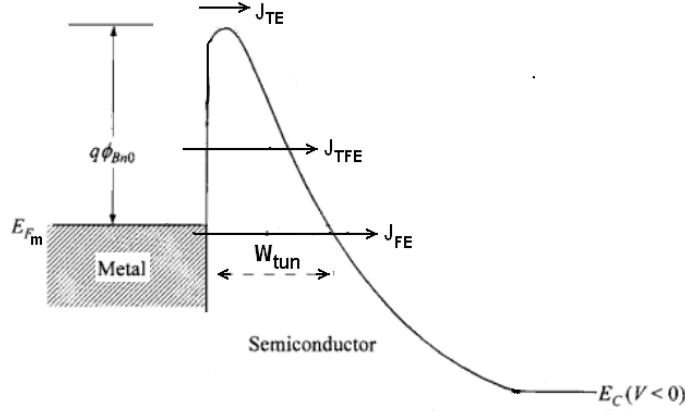
Figure 2.4: Current components in a Schottky diode (under reverse bias)

Tunneling through the Schottky barrier is proportional to the tunneling probability multiplied by the amount of filled states from which-, and the amount of empty states to which tunneling can occur. This can be mathematically described using [11]:

(Eq. 6)
$$J_{(T)FE\,M \to S} \propto \int_{E_c}^{E_{Fm}+q\Phi_{Bn}} F_s \Gamma(E)(1 - F_M)dE \ \ ,$$

where F_M and F_S are the Fermi-Dirac distribution functions of the metal and the semiconductor, resp. and $\Gamma(E)$ is the energy (and tunneling width) dependent tunneling probability.

A widely used [27-29], analytical approximation of the above equation was first proposed by Padovani and Stratton in 1966 [26] and is given by:

$$\textbf{(Eq. 7)} \qquad J_{(T)FE} = \frac{q^2\xi^2}{8\pi h\Phi_B}\exp\left[-\frac{8\pi}{3hq\xi}\sqrt{2m^*(q\Phi_B)^3}\right] ,$$

where ξ is the electric field at the Schottky barrier, and h is Planck's constant.

Two things to note from the above expression are that (1) there is no (strong) T dependence (typical for tunneling), and (2) that there is in fact strong electric field (ξ) dependence. From (Eq. 5) it can thus be concluded that the total MS current will be strongly influenced by the electric field at the Schottky barrier. This important electric field (ξ) can be adjusted for instance by, applying a reverse bias (i.e. "Zener" breakdown in Schottky diode), applying a lateral field (i.e. SB-FET) or by simply changing the semiconductor doping (i.e the tunneling dominated current flow of reverse biased degenerately doped SM ("Ohmic") contacts).

J_{FE} vs J_{TFE} :

It is important to realize that the tunneling component can be separated in a pure field emission component (J_{FE}) and a thermionic field emission component (J_{TFE}). The difference between these two lies in the fact that pure field emission is tunneling of carriers at energy levels around the Fermi level , while thermionic-field emission is the tunneling of thermally exited carriers above this energy. Judging by the (thermal) nature of the J_{TFE} tunneling it is clear that its T dependence will lie somewhere between the minimally T dependent J_{FE} component and the highly T dependant J_{TFE} component [11]. This distinction between J_{FE} and J_{TFE} will be important in explaining the T dependence [30] of the tunneling dominated SB-FETs.

Schottky diode vs. PN diode

From the above sections it can be concluded that the Schottky diode contrary to the PN diode is mostly a majority carrier device. Meaning that when it comes to current density the majority-carrier thermionic emission overshadows the minority-carrier diffusion which is the main current contributor in the conventional PN-diode. This is the reason why the transient response of the Schottky diode is considerably better. But the presence of the Schottky Barrier itself on the other hand results in these diodes having a relatively high series resistance compared their PN counterparts.

The non-ideal MS contact

Experimental data shows that metals with larger work functions indeed have systematically larger SBHs (when forming MS contacts) than those with lower workfunctions. The actual dependence however is usually weaker than predicted by the ideal cases shown in Figure 2. 2. This is because unlike a p-n junction, which occurs within a single crystal, a Schottky barrier junction includes a termination of the semiconductor crystal as a whole. The semiconductor surface contains surface states due to defects associated with the physical interface non-idealities such as dangling bonds in addition to intrinsic, metal-induced gap states (MIGS). These MIGS are localized energy states caused by the sudden termination of allowed metal energy states at levels corresponding to energies within the semiconductor bandgap. Figure 2.5 illustrates how MIGS would be incorporated in a schematic band diagram showing that those states below E_F are filled and above E_F are empty. It should be mentioned that MIGS can either be donor or acceptor states and that making a distinction between the two is rather complex and goes beyond the scope of this work. For more on how to separate the two types of MIGS the reader is referred to e.g. [11].
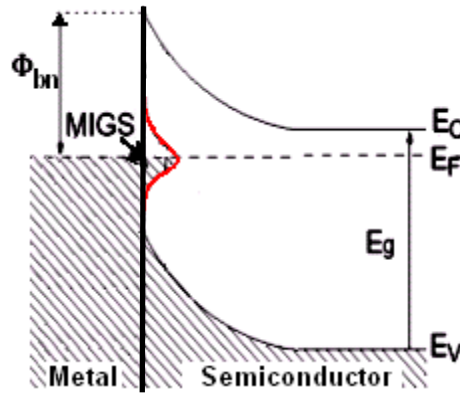

Figure 2.5: Schematic band diagram of a MS-junction in which the metal in direct vicinity of the (n-type) Si creates metal induced gap states (MIGS) [31].

Because of the interface non-idealities mentioned above simply knowing Φ_M and χ in reality is usually not enough to calculate the actual SBHs. For instance the theoretical Φ_{Bn} of Cr ($\Phi_M \sim 4.5\ eV$) on Si ($\chi_{si} \sim 4.05\ eV$) should be around 0.45 eV while the actual value can be as high as 0.60 eV [11]. This partial insensitivity seen between experimental barrierheights and Φ_M is commonly referred to as *Fermi level pinning* [32]. This phenomenon is important for both the SB-FETs treated here as well as the typical metal poly-Si connections of conventional MOSFETs with high-*k* gate-dielectrics [33, 34] where for instance it can cause V_T-shifts. Circumventing Fermi level pinning (also known as depinning) and creating MS junctions with specific SBHs is therefore a field of great technological interest and an active research field in itself.
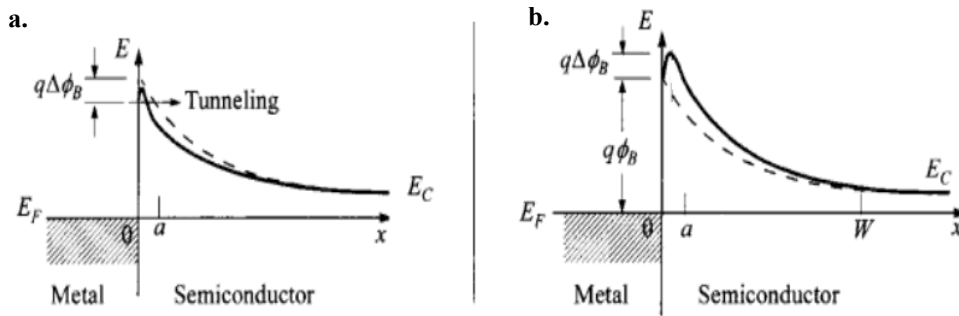
Barrier-Height Adjustment:

Since electrons at a certain distance x from a metal induce equal but opposite image charges at the metal surface an additional attractive (image) force is created between these charges. This resultant extra force directed towards the metal makes it easier for the electrons to cross the Schottky barrier (image force barrier lowering), resulting in an effective Φ_B reduction which can be approximated [11] using:

(Eq. 8)
$$\Delta\Phi_B = \sqrt{\frac{q\xi_0}{4\pi\varepsilon_s}} \quad,$$

where ξ_0 is the maximum electric field at the MS interface.

Since J_{TE} is exponentially dependent on Φ_B (see (Eq. 3)) any change in the electric field at the MS interface influences the total thermionic emission current.

An example of influencing this electric field (and as such the effective SBH) would be through the use of heavily doped interface pocket (<10nm) implants. Solving the Poisson's equation and determining the new ξ_0's using these pocket implants shows that a heavily doped, but also fully-depleted, P^+ pocket leads to an increase in electron barrier height ([35], Figure 2.6b) while a heavily doped N^+ type pocket leads to a decrease ([36], Figure 2.6a). Pocket implants can therefore, to a certain extend, be useful in suppressing or increasing the thermionic emission current J_{TE} (see also Chapter 4.6: "Source Side Pocket effect")

Figure 2.6: Electron barrierheight adjustment (a) decrease[8], by employing a fully-depleted n+-type pocket (b) increase by employing a fully depleted p+-type pocket in an n-type Schottky contact– Dashed line indicates the original uniform doping barrier [11]

Another way of reducing the effective SBH is by essentially "depinning" the MS-junction. It was shown by Yee-Chia *et al.* in [37] that there is less Fermi level pinning associated with metal/insulator junctions than for direct MS-contacts. This implies that a reduced effective barrier can be achieved with an insulator thin enough to allow tunneling of free carriers, but thick enough to block the gap states (MIGS). A schematic band diagram illustrating this effect is shown in Figure 2.7.

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[8] this decrease is actually a combined effect of a SBH reduction (increased J_{TE}) and a tunneling width (W_{Tun}, Figure 2.4) reduction near the top of the barrier, resulting in an increase in J_{TFE}
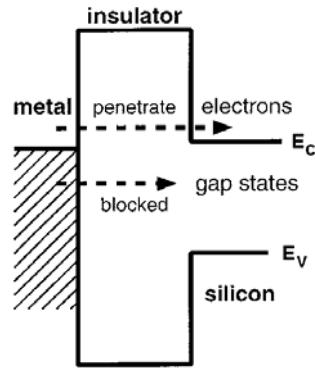
Figure 2.7: Schematic band diagram showing an MS-Junction with insulator allowing free carries to tunnel while blocking the MIGS [31].

The introduction of the interfacial oxide reduces the MS junction dipole moment and thus effectively reduces the thermionic barrier (height) associated with the Si conduction band. However, it does so by introducing a thin barrier through which electrons must tunnel to reach the Si conduction band. The resistance in such a junction is the result of a competition between a thicker tunnel barrier and a lower thermionic barrier. It was however shown that for sufficiently thin oxides the reduction in current due to the interfacial tunnel barrier presented by the insulator is less than the increase in current due to the significantly lowered thermionic barrier (height). One possible explanation is that gap states at the pinning point within the Si bandgap are blocked by the insulator more strongly than free states at the Si conduction band. This is because the tunneling probability is (exponentially) lower further away from the top of a barrier. Thus, the insulator prevents metal states from penetrating into the Si gap and producing MIGS, while still permitting a high current flow of electrons into or out of the Si conduction band.

2.3. Ohmic contact

One of the most common ways of creating non-rectifying ("Ohmic") MS contacts is through heavy doping of the semiconductor. This degenerately doping, results in a drastic reduction of the semiconductor depletion width and as such the tunneling distance W_{tun} (Figure 2.8 (a)) at equilibrium. Having this narrow tunneling distance at equilibrium allows for $J_{(T)FE}$ to be large enough at small negative V_A values to significantly influence the current. By essentially shifting, what is also known as, avalanche breakdown to low negative V_A the I–V curve characteristic therefore flows ,without showing rectifying behavior, from tunneling dominated (reverse bias) to cross barrier dominated (forward bias) carrier injection. From this it can be concluded that both Schottky tunneling ($J_{(T)FE}$) and thermionic emission (J_{TE}) play an important role in creating Ohmic junctions. Simulating MS junctions with known contact resistances is consequently an excellent way to calibrate Schottky tunneling ($J_{(T)FE}$) and thermionic emission (J_{TE}) simulations model interaction.. This is therefore used in chapter 4 as the preliminary (simulation) model calibration method. If a non-rectifying *linear* I-V curve (as seen in Figure 2.8) is obtained across the full I-V range it is the drift current that will be the important limiting factor, as carrier injection through cross barrier diffusion or tunneling should be large enough not to limit the total current.
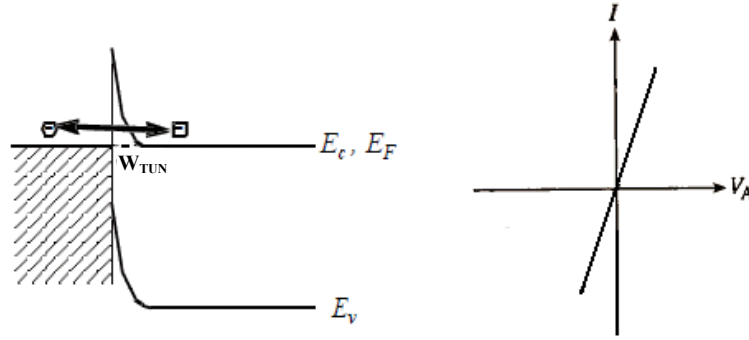
Figure 2.8: Schematic band diagram of an Ohmic MS junction at equilibrium and a typical non-rectifying (and linear) I-V curve.

2.4.   The universal Schottky tunneling (UST) model

The model used throughout the simulation work of the Schottky junctions is the so-called "universal Schottky tunneling model". This unified model for Schottky and Ohmic contacts was derived and developed by Matsuzawa *et al.* [38] and is based on the calculation of *localized* tunneling rates at specific grid locations ($G_\mathrm{T}(x)$, Figure 2.9) near the Schottky contact. This is illustrated (for electrons) in Figure 2.9.

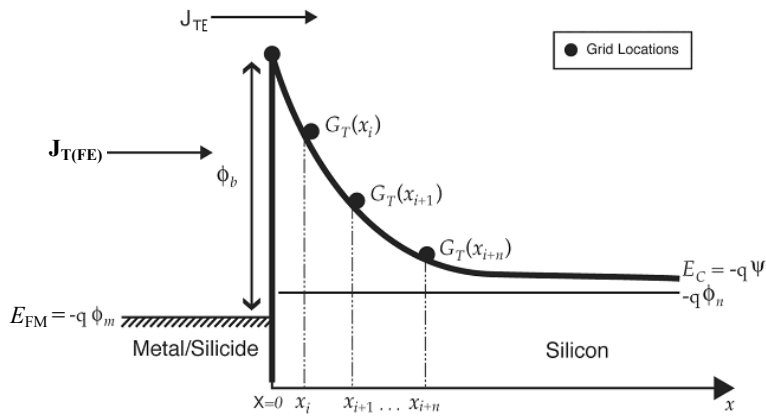**Figure 2.9: Local tunneling generation rate representation of the universal Schottky tunneling model [39]. The tunneling component ($J_{\mathrm{T(FE)}}$) is shown to be divided into localized generation rates ($G_\mathrm{T}(x)$) on the Si conduction band edge which will subsequently be incorporated in the generation-recombination term of the current continuity equations.**

The tunneling current density $J_{T(FE)}$ is described using:

(Eq. 9)
$$J_{T(FE)} = \frac{A*T}{k} \int_{E_C - E_{FM}}^{\infty} \Gamma(E) \ln\left(\frac{1 + F_S(E)}{1 + F_M(E)}\right) dE \quad ,$$

with $A*$ the effective Richardson's constant, $\Gamma(E)$ the tunneling probability[9], $F_S(E)$ and $F_M(E)$ the Fermi-Dirac distribution functions in semiconductor and metal and E the carrier energy.

Since integrals are non-local in nature obtaining the localized tunneling rates ($G_T(x)$, Figure 2.9) requires the following transformation to be performed:

(Eq. 10)
$$\frac{\partial J_{(T)FE}}{\partial x} = \frac{\partial J_{(T)FE}}{\partial E} \cdot \frac{\partial E}{\partial x} = \frac{\partial J_{(T)FE}}{\partial E} \cdot -q \frac{\partial V}{\partial x} = q \cdot \frac{\partial J_{(T)FE}}{\partial E} \cdot \xi$$

resulting in [39]:

(Eq. 11)
$$G_T(x) = \frac{1}{q} \nabla J_{T(FE)} = \frac{A*T\xi}{k} \Gamma(x) \ln\left(\frac{1 + n/\gamma_n N_c}{1 + e^{-\frac{(E_c - E_{FM})}{kT}}}\right) \quad ,$$

with ξ the local electric field, n the local electron concentration, N_c the local conduction band density of states, γ_n the local Fermi-Dirac factor, E_c the local conduction band edge energy and E_{FM} the Fermi level of the metal.

The J_{TE} component is simply implemented using the well known thermionic emission equation (see (Eq. 3)) with the inclusion of barrier lowering ((Eq. 8). Both the localized thermionic emission (J_{TE}) and tunneling ($J_{T(FE)}$) components are then implemented in the generation-recombination term of the current continuity equation for electrons and holes [38].

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[9] Calculated using the WKB approximation with a triangular potential barrier.

3. The Schottky Barrier MOSFET (SB-FET)
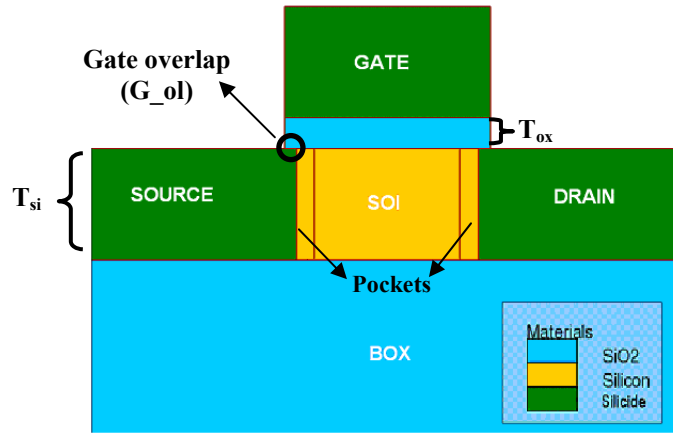
Figure 3.1: Schematic cross-section of a SOI based SB-FET, showing some of the important parameters influencing the device performance. Typical values for these device parameter are listed in Table 4.1

In chapter 2 it was mentioned that because of the strong electric field dependence of the Schottky tunneling component (Eq. 7) the tunneling current could be modulated by the electric field. A gate modulated (tunneling) current can therefore be achieved by changing the electric field at the Schottky junction perpendicular to the current flow. As stated earlier however, the total current density (Eq. 5) across the Schottky barrier consists not only of this tunneling component ($J_{(T)FE}$) but also of the cross barrier thermionic emission component (J_{TE}). If one therefore wants to benefit from a tunneling current as the modulating current it is important to design a SB-FET to operate in a regime in which the tunneling component is larger than the thermionic component (high Φ_{Bn}, Figure 3.2(c)). The latter being independent of gate bias as seen in Figure 3.2 (b) and (c). If however a SB-FET with diffusion current modulation similar to that of conventional (thin body) MOSFETs should be realized [40], low Φ_{Bn}'s will be of interest (see Φ_{Bn}, Figure 3.2(b)). Lundstrom *et al.* [41] showed[10] however that for these cases, low none negative SB's (as seen in Figure 3.2(b)) will always result in an on-state performance inferior to that of conventional (thin body) MOSFETs. This is because quantum confinement (in thin body devices) raises electron energy levels in silicon, resulting in an effective barrier height increase (see [41] for more details). A negative barrier height would therefore be necessary to obtain the effective barrier height of 0 *eV* needed to achieve on-state performance comparable to that of conventional FETs.

Finally it should be noted that this work focuses on thin body (SOI) based devices because of their increased benefits with respect to suppression of short channel effects [42] and a range of other Schottky device specific SOI based advantages (discussed in Chapter 4). An example of such a (SOI based) Schottky specific advantage is improvement of carrier injection when scaling down T_{SI} (see [42] and chapter 4.4).

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[10] Using an in-house simulation model based on a quantum approach solving the (2-D) Poisson equation self-consistently with the Schrödinger equation using the Greens function formalism.
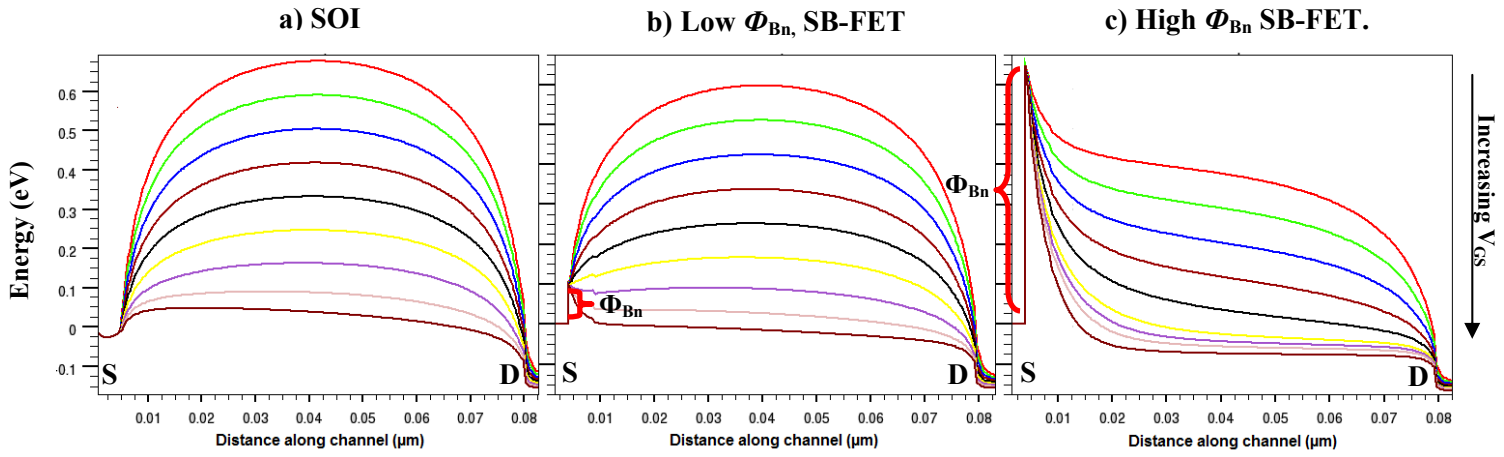
Figure 3.2: Conduction band edge modulation along a (80 nm) device channel for various applied gate biases (-1.0 V <V_{GS}< 1.0V @ V_{DS} = 0.1V). (a) depicts behavior seen in a conventional SOI-FET, (b) a low Φ_{Bn} diffusion current modulated SB-FET, and (c) a high Φ_{Bn} $J_{(T)FE}$ modulated SB-FET.

3.1. The working principles of the symmetric SB-FET

In this paragraph the general carrier flow through a conventional symmetric (n-type) SB-FET will be described. Schematic energy band representations for various bias conditions are depicted in Figure 3.3 [28]. Diagram (a) is for a device in thermal equilibrium. Here the electron barrier as seen from the bands is not simply Φ_{Bn} but the sum of the electron Schottky barrier Φ_{Bn} and an electrostatic barrier denoted as q.ς_S (Figure 3.3 (a)). By increasing the gate voltage this electrostatic barrier q.ς_S is reduced until inversion occurs and Φ_{Bn} alone remains as the electron barrier (Figure 3.3 (b1)). The inversion electrons supplied through tunneling and/or cross barrier thermionic emission are then swept across from source to drain by increasing the drain voltage (Figure 3.3(b)).
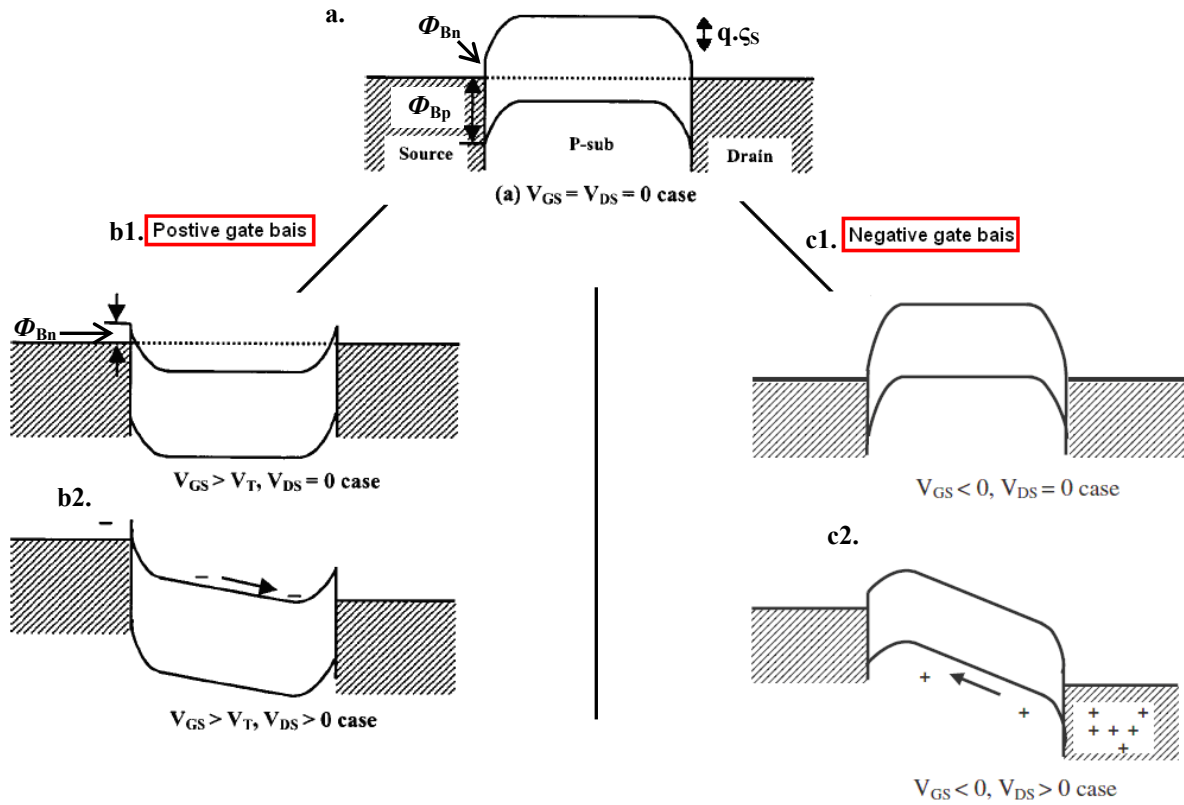

Figure 3.3: Band diagrams of a symmetric SB-nFET at (a) equilibrium, (b) positive gate bias and (c) negative gate bias

From the band diagrams and the known complementary nature of hole and electron SBHs (see Figure 2. 2 (a) and (b)) one can deduce that for a diffusion limited SB-nFET (Figure 3.2b), metals with high Φ_{Bp} should be chosen such that Φ_{Bn} is as low as possible. From a technological point of view it should be realized however that metals with small electron SBHs (Φ_{Bn}) on p-type bulk (nFET) are less common than those with small hole SBHs (Φ_{Bp}) on n–type bulk (pFET), making it more difficult to create diffusion limited SB-nFETs than SB-pFETs [3, 11, 14].

For a tunneling limited SB-nFET on the other hand, Φ_{Bn} should be high (Figure 3.2c). A high Φ_{Bn} however means that Φ_{Bp} reduces which, in the case of symmetric SB-FETs, will result in an increased (ambipolar) hole leakage current (Figure 3.3 (c2) and Figure 3.6 (a))[43, 44].

This happens because a metallic source or drain, unlike (to certain extent) their conventional highly doped n or p-type counterparts, can supply both n and p-type carriers making two ways conduction possible and one of the main problems faced when dealing with symmetric SB-FETs. A comparison between the positively biased and negatively biased symmetric SB-nFET of Figure 3.3 (b) and (c) illustrates this ambipolar nature. Depending on the applied gate bias either holes (Figure 3.3 (c)) or electrons (Figure 3.3 (b)) are injected in the channel [29]. Through an applied negative gate voltage holes will be supplied by the drain which will understandably be detrimental to the off-state current. This unwanted ambipolar hole current at low/negative gate voltages can be interpreted as a severe form of gate induced drain leakage (GIDL) known from conventional MOSFETs [11, 25]. It should be mentioned however that GIDL in conventional FETs is due to band to band tunneling in the (deeply depleted and highly doped) region near the drain edge, which is a different mechanism than that seen in the symmetric SB-FETs discussed above.

3.2.   The Asymmetric SB-FET

Since this thesis partly focuses on the asymmetric Schottky Tunneling Source FET, as initially proposed by Bing-Yue and Kimura [15, 45] and expanded upon by Jhaveri *et al.* [20-22] some of the main advantages of this design compared to the (more conventional) symmetric design will be discussed.
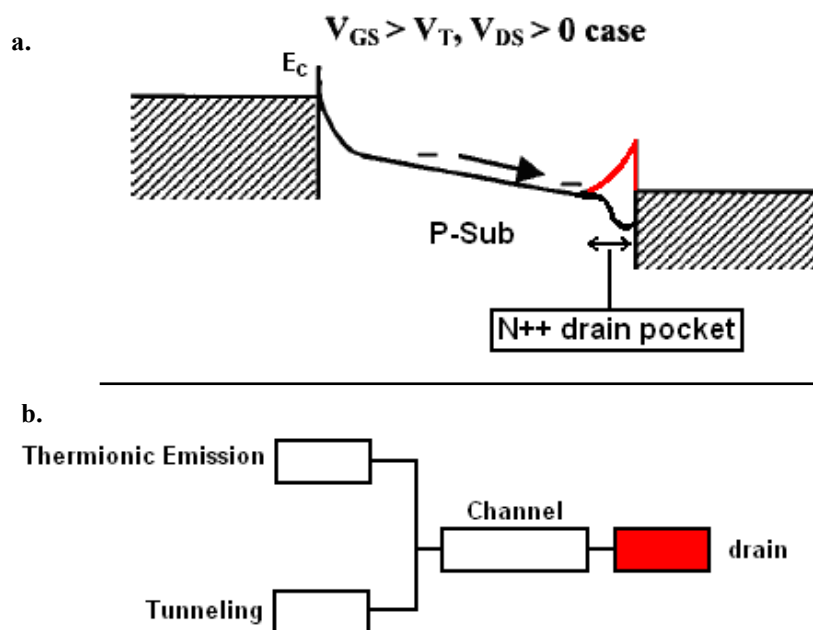

Figure 3.4: a) Schematic conduction band edge plot (@low V_{DS}) of the symmetric (red) and asymmetric (black) SB-nFET
b) Simplified equivalent "resistance" network of the symmetric (red) and asymmetric (black) SB-nFET

The symmetric SB-FET (at low V_{DS}'s) has a drain side (potential) Schottky barrier impeding current flow, which is caused by the presence of a forward biased drain-bulk Schottky diode (red conduction band edge increase, Figure 3.4). Although this potential barrier reduces as the forward bias (higher V_{DS}'s) is increased (see Chapter 2.2) the built-in potential associated with the drain-bulk Schottky diode will continue to impede current flow in the linear operation region and as such increases the saturation voltage V_{DSAT} [44]. In Figure 3.5 (a) it is seen that at low V_{DS}'s ($<\sim 0.2$ V) the presence of the drain side Schottky barrier result in sub linear I_D-V_{DS} behavior, which is characteristic for symmetric SB-FETs [3, 13, 44].

One of the main reasons behind the introduction of the asymmetric SB-FET was therefore improving performance in the linear operation region. The asymmetric SB-FET accomplishes this by using a drain side Ohmic contact (created using a heavily doped drain side pocket implant, Figure 3.1) by means of which one essentially removes the drain-bulk Schottky diode (Figure 3.4 (a)). By removing this drain side (Schottky) potential barrier the performance in the linear region is therefore improved as seen in Figure 3.5 (b).

Furthermore, the asymmetric SB-FET's Ohmic drain contact also eliminates the ambipolar nature of its symmetric counterpart (N++ doped drain side junction is not an effective hole source) which as discussed previously (Chapter 3.1) caused high off state leakage currents.

One should realize however that introducing an Ohmic drain through a drain side pocket negates some of the technological advantages of the SB-FET discussed in the introduction. One of these being the low thermal budget since having a heavily doped region will necessitate high activation temperatures not necessary in the case of the all metal symmetric SB-FET solutions. Also one might yet again obtain relatively high off currents due to band to band tunneling [45, 46] (at low/negative V_{GS}'s) caused by having a gated diode at the abrupt P^+N^+ junction at the channel (drain-side) pocket interface (see Appendix B.3). Note that this classical form of GIDL was not taken into consideration in the work of Jhaveri *et al.* [22]
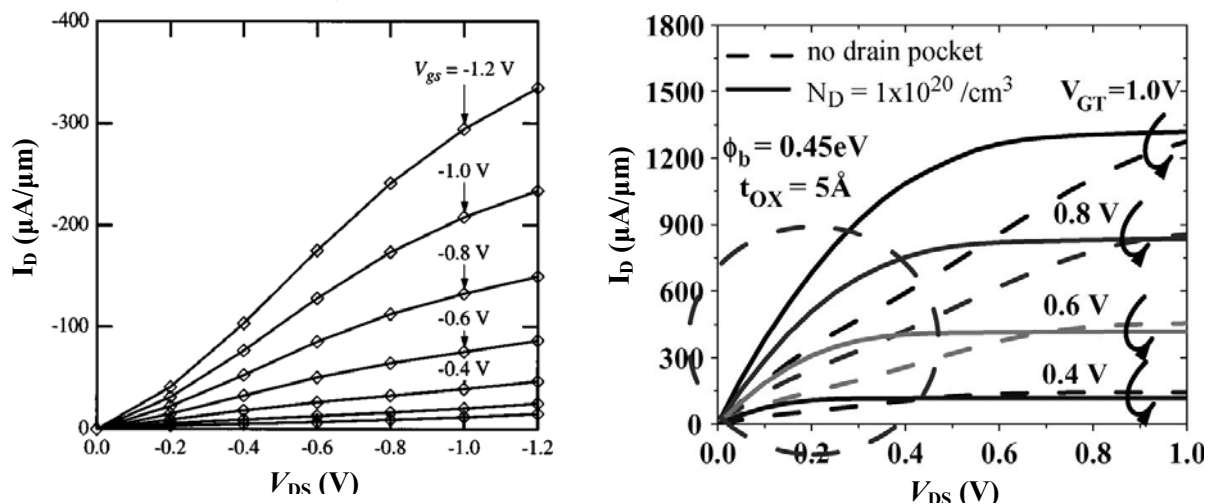
Figure 3.5: a) I_D-V_{DS} **measurements results by Wang *et al.* [44] (showing sublinear behavior, $V_{DS} <$ $\sim 0.2V$) for a PtSi ($\sim \Phi_{Bp} \sim 0.20eV$) SB-pFET with 19Å gate oxide, ~40nm channel length and p$^+$ -poly gate.**

b) I_D-V_{DS} **simulation results by Jhaveri *et al.* [22] for a symmetric (dotted) and asymmetric (solid) SB-nFET with $\Phi_{Bn} \sim 0.45eV$, a 5Å gate oxide, ~80nm channel length and n$^+$ -poly gate. A clear improvement in the linear region of the asymmetric variant is visible due to the presence of the highly doped ($N_D = 10^{20}$ cm^{-3}) drain side pocket**

3.3.   Electrical analysis of a tunneling limited SB-nFET

Now that the basic flow mechanisms within the asymmetric and symmetric SB- FETs have been discussed, a quick overview will be given as to how to distinguish different regimes of operation from the SB-FET I_D-V_{GS} curves.

(a) Diffusion limited

(c) (Thermionic) Field emission limited

(b) Thermionic emmission limited

(d) Channel resistance (drift) limited
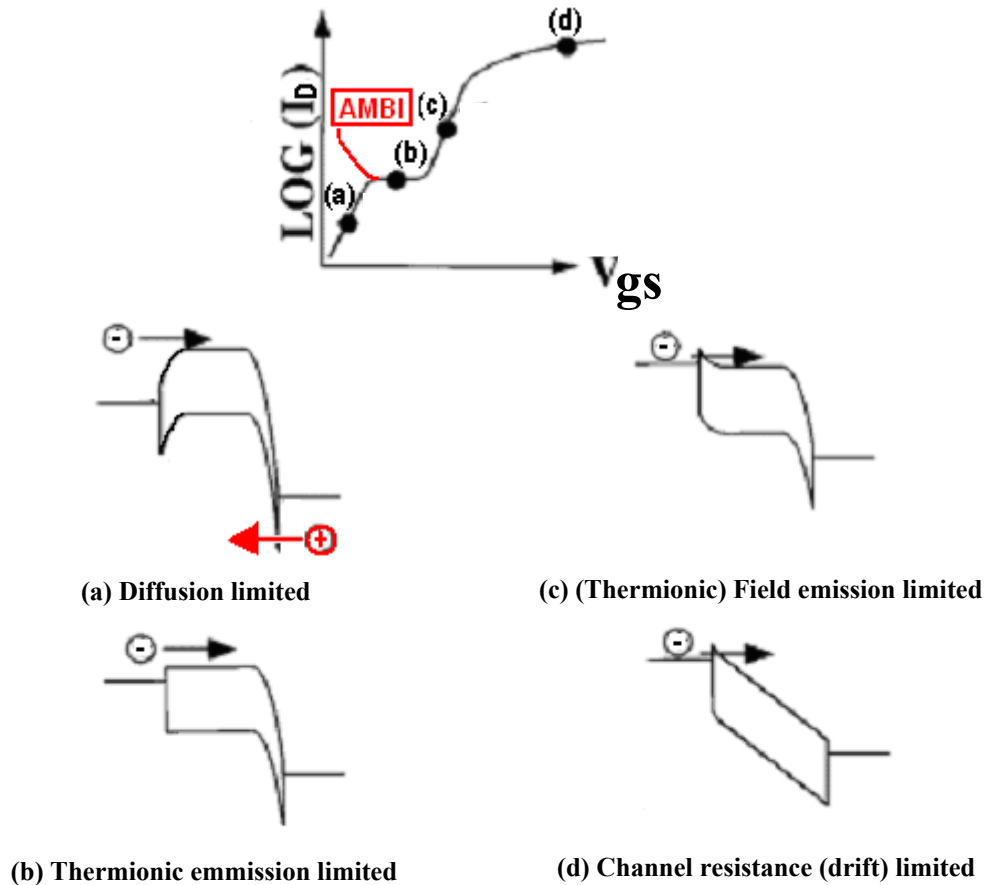
Figure 3.6: Schematic band diagram description of the different current flow regimes seen in an I_D-V_{GS} plot of a symmetric tunneling limited SB-nFET[30]. With (a) the diffusion limited regime, (b) the thermionic emission "current plateau" regime, (c) the (thermionic) field emission regime and (d) the channel resistance limited (drift) regime

In Figure 3.6 (a) the device is in its off state with bias applied only to the drain, the electron leakage current is limited by diffusion because of the high electron energy barrier Φ_{Bn} + q.ς_S (see Figure 3.3 (a)). In this regime the electrons flow via diffusion from source to drain. Changing the gate voltage in this stage simply modulates the amount of electron current entering the channel, which can be traced back as the (exponentially) increasing I_D in region (a) of Figure 3.6. In this regime, because of the high drain side electric field, a symmetric SB-device will also have an ambipolar hole tunneling component (Figure 3.6 (a)) resulting in an increased I_{off} (indicated in red in the I_D-V_{GS} curve of Figure 3.6) .

Eventually, with increasingly positive gate bias, the fixed electron Schottky barrier remains constant and the current is limited by thermal emission across this barrier. This stage results in the (exaggerated) current plateau, with no I_D increase for increasing V_{GS}, seen in Figure 3.6 (b).

With an even further increase in gate bias, electrons eventually tunnel through the Schottky barrier and I_D once again begins to increase, as seen in the ''(thermionic) field emission regime" (Figure 3.6 (c)).

Finally for a further increase in V_{GS}, I_D becomes channel resistance (Figure 3.4b) limited and cross channel (electron) drift becomes the dominant transport mechanism (Figure 3.6d). In this final "on-state" regime of V_{GS} the current drive of the device is more or less similar to that of conventional MOSFETs [30].

## 3.4.   Subthreshold Swing of FD-SOI based SB-FETs.

The subthreshold swing of the diffusion limited regime of tunneling SB-FETs (Figure 3.6 (a)) is similar to that of a conventional MOSFET [11] as the mechanism of importance in both cases is diffusion. In the tunneling limited regime (Figure 3.6 (c)) on the other hand we are dealing with a different mechanism (tunneling) and as such the subthreshold slope is not necessarily limited to the known 60mV/dec value. Knoch, Appenzeller and Zhang did extensive research into the (tunneling) subthreshold behavior of these FD-SOI based devices and published a series of papers on the subject [42, 47-49]. They derived the following analytical formula (which fitted experimental data well) for the subthreshold swing of FD-SOI based SB-FETs:

$$\textbf{(Eq. 12)} \qquad S = \frac{kT}{q}\ln(10)\frac{1}{1-e^{-d/\lambda}} \qquad ,$$

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{si}t_{ox}}$$

where λ is the so-called screening or characteristic length, which describes the lateral extension of the potential in the channel length direction [50] and d a fitting parameter[11] or the so-called tunneling distance. For dimensions beyond this distance the tunneling probability $T(E)$ is set to 0 and below this distance to 1 (Figure 3.7)

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[11] Using the transmission probability an expression for d can be calculated showing weak dependence on the SBH as well as t_{si} and t_{ox} [49]
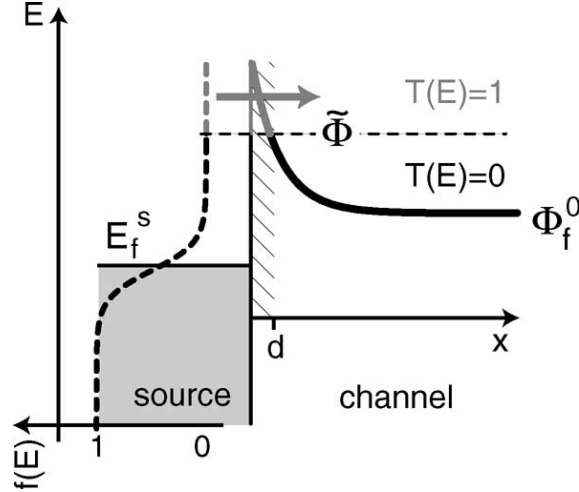
Figure 3.7: Potential distribution at the source Schottky diode. For the analytical approximation, the tunneling probability (*T(E)*) =1 for energies above *Φ* and zero otherwise. Φ_f^0 is the surface potential *λ* away from the interface.[48]

In the interest of brevity the exact derivations of the above equation will not be treated but one should realize that for a constant *d* a small *λ* leads to better gate control over the effective barrier *Φ* which ultimately leads to a 60m*V*/dec limit being reached yet again. The approximations used to obtain (Eq. 12) do not allow an exact conclusion to be drawn as to the true origin of this 60m*V*/dec limit. But the fact that the analytical formula matches device measurements can lead to the assumption that the dominance of the thermionic emission component J_{TFE} has something to do with this 60m*V*/dec limit. Why exactly this thermionic field emission current is also limited to 60m*V*/dec however is still not completely understood in the literature (or by us) but it is safe to assume (from the many experimental results[49]) that realistically one should not expect subthreshold swings lower than 60m*V*/dec when using Schottky tunneling devices.

A quick comparison between the subthreshold swing of the conventional bulk MOSFETs (Eq. 1)[12] and that of the FD-SOI based SB-FETs (Eq. 12) shows that even though both are limited to 60m*V*/dec the pre-factors are different.

(Eq. 13)
$$ m = \left(1 + \frac{C_{dm}}{C_{ox}}\right) \approx \left(1 + \frac{3t_{ox}}{W_{dm}}\right) \qquad n = \left(1 - e^{-d \big/ \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}}\right)^{-1} $$

Conv. MOSFET   **FD-SOI SB-FET**

These pre-factors indicate how well the gate bias at the Si-SiO$_2$ interface is linked to the channel surface potential. Comparing both pre-factors shows that for conventional MOSFETs *S* scales linearly with C_{dm}/C_{ox} while in the case of the FD-SOI based SB-FETs *S* scales as the square-root of the SOI and oxide thickness. The latter T_{Si} and T_{OX} dependence of *S* will be discussed more in depth in chapters 4.3 and 4.4

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[12] for FD-SOI based MOSFETs with T_{Si}< Debye length, C_{dep}=0 [11], which is one of the reasons why FD-SOI MOSFETs have superior subthreshold behavior compared to conventional bulk or non FD-SOI.

4. Simulator calibration and DC simulations

All simulations throughout this project were performed using Silvaco's Atlas device simulator [51]. Older versions of Silvaco's Atlas package had known issues simulating field assisted tunneling necessitating external ("postprocessing") analytical calculations. Therefore using the newly implemented UST model [38] some initial calibration runs and comparative analysis were performed. The latter was performed using the Synopsys-TCAD, Dessis device simulator [52] and measurement results obtained by Jhaveri *et.al*. This was then followed by more expansive simulations focusing on the finer aspects of the (asymmetric) SB-FET and its responds to a wide range of device parameter changes. Some of these parameters and their standard values are listed in Table 4.1 with a cross-sectional view of the device depicted in Figure 3.1

Parameter	Standard Value
Gate Length	90nm
Gate Overlap (S/D)	5nm
S/D pocket width	5nm
Oxide thickness	0.5nm
Silicon Thickness	25nm (FD-SOI)
Channel doping	1e17 Atoms/cm^3
D-Pocket	1e20 Atoms/cm^3
Source electron Barrierheights (Φ_{Bn})	0.45eV (~TiW), 0.25eV(Ti,ErSi$_2$) and 0.65eV(~Al,NiSi)
Gate work function (Φ_M)	4.17eV (~χ_{si})

Table 4.1: Summary of the device parameters and their standard values used for the simulation work

Finally to get a better idea about the ATLAS input file structure and to see all the different (bandgap, mobility etc) physical models used the reader is referred to Appendix C, which lists some sample input files. Unless stated otherwise however, it should be noted beforehand that for all asymmetric SB-FET simulations pure band to band tunneling at the drain side gated P$^+$N$^+$ diode (as mentioned in Chapter 3.2) has not been taken into account. In practice however GIDL reduction techniques usually employed in conventional MOSFETs (e.g. Gaussian instead of abrupt pocket implants etc) can be used to reduce this otherwise inevitable tunneling leakage current (Appendix B.3).

4.1.   Calibration using Ohmic junctions:

Before the actual SB-FETs were simulated metal on (degenerately doped) semiconductor (Ohmic) junctions were simulated as the preliminary test devices. Using the UST model and no extra external calculations Ohmic behavior was indeed observed for these junctions. Hence the conclusion was drawn that the UST model is indeed effective in modeling the $J_{(T)FE}$ and J_{TE} components both of which are necessary to model Ohmic behavior (see Chapter 2.3).The results of this comparative analyses are shown in the table below.

Φ_{Bn} (eV)	Doping (n type atoms/cm^3)	R_c simulated (Ω-cm^2)	R_c calculated/measured [11] (Ω-cm^2)
0.4	1e20	6e-07	2.8e-8
0.5	1e20	6.9e7	5.5e-8
0.7	1e20	1.3e-6	8.7e-6
0.4	1e19	1.1e-5	1.1e-5

Table 4.2: Comparison between simulated and measured [11] contact resistance values

It can be seen that the simulated results (extracted from the simulated *I-V* curves) show agreement with measurements [11] albeit with some small differences. These differences could be caused by simulation specific problems such as meshing and the physics models used (for instance for bandgap narrowing).

4.2.   Symmetric and Asymmetric SB-FET device behavior

To test the UST model behavior with a three terminal device both symmetric and asymmetric SB-FETs (as proposed by Jhavari *et al.*) were simulated. The resulting I_{D^-} V_{GS} behavior is shown in Figure 4.1 for three devices, each having a different source electron SBH. The results shown here coincide with our theoretical expectations from Chapter 3.

For instance the previously discussed complementary nature (Φ_{Bp} = E$_G$- Φ_{Bn}) of hole barrier height (Φ_{Bp}) to electron barrier height (Φ_{Bn}) leads to an ambipolar hole leakage drop for decreasing electron barrier heights (Φ_{Bn}'s). Also clearly visible when decreasing Φ_{Bn} is the smaller tunneling range (red dotted area), the higher current plateau (green dotted area) and the increasing diffusion limited current (blue dotted area). The conduction band edge for the boundary conditions of each of these different injection regimes (distinguished by the Greek numerals) of a 0.65e*V* (source) barrier height device are also shown in Figure 4.2. All of which agree with the theory discussed in the previous sections. In Figure 4.1 for instance the absolute values of the current plateaus, which are thermionic emission current limited, indeed show behavior proportional to exp(-Φ_B/*UT*) which is in agreement with (Eq. 3).
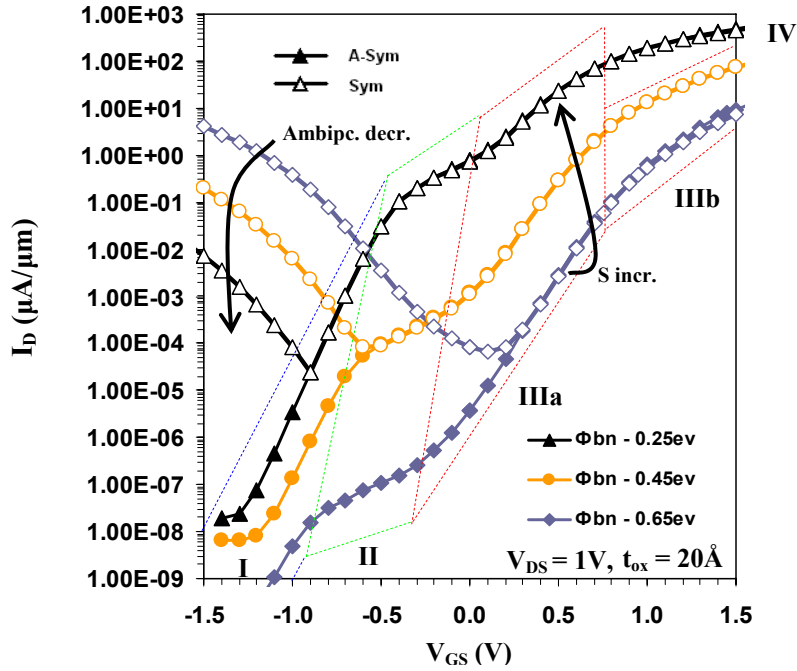
Figure 4.1: *I*$_D$-*V*$_{GS}$ **plot for both symmetric and asymmetric SB-FETs showing their behavior for three different source electron barrier heights. With the blue area (I) the diffusion limited range, the green area (II) the thermionic emission limited current plateau and red area (III) the tunneling (IIIa, *J*$_{TFE}$ and IIIb, J$_{FE}$) range. IV depicts the Channel resistance (drift) limited part of the curve.**

Finally it is worth noting that there is an increase in subthreshold swing for decreasing Φ_{Bn}'s in the (thermionic) tunneling range (IIIa). This is possibly due to the fact that the tunneling width for larger SBHs is more strongly modulated by the applied gate bias. Meaning that if one were to look at the change in tunneling width across a fixed biasing range (ie. from V_{GS}=0.1V to 0.8V in the above figure), the change in tunneling width for the high (source) Φ_{Bn} devices would be larger.
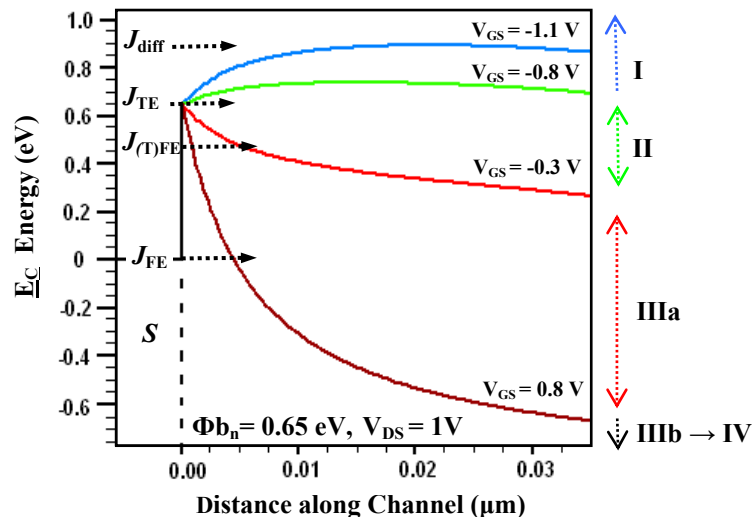

Figure 4.2: Conduction band edge modulation showing boundary conditions (green, red, brown) of each of the different injection regimes of the 0.65e*V* (source) SBH device seen in Figure 4.1.
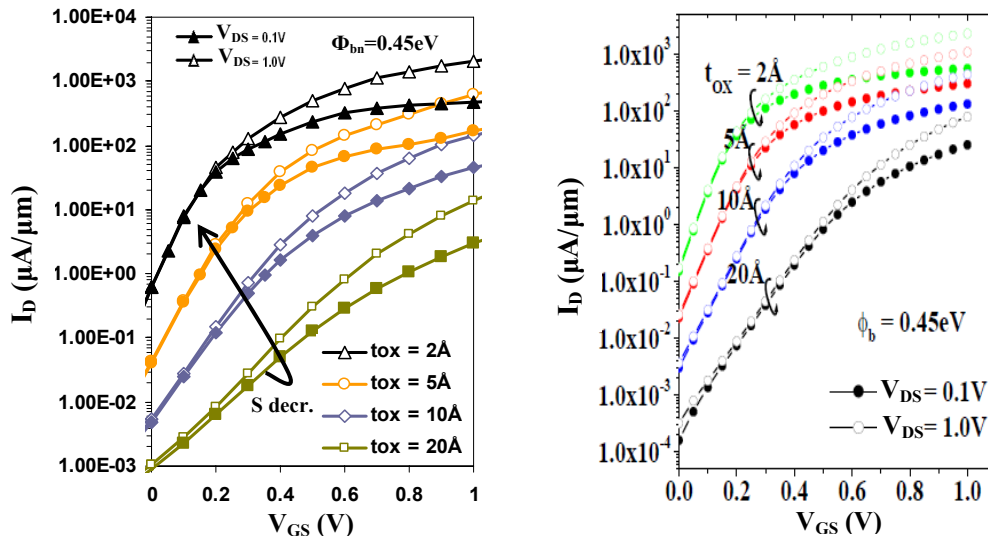
4.3. Effect of Gate Dielectric Thickness

Figure 4.3: a) I_D-V_{GS} **characteristics of devices for various gate oxide thicknesses**
b) Same results but those obtained by Jhaveri [24] using the Dessis
device simulator [52]

As known from (Eq. 12 the subthreshold swing is a strong function of the oxide thickness which combined with an I_{on} increase is clearly seen in Figure 4.2. Plotting the different subthreshold swings as a function of oxide thickness (Figure 4.4(a)) shows a linear dependence with a minimum swing of ~60mV/dec. This is in agreement with the relationship described in (Eq. 12.) Therefore if decent subthreshold swings are desired, high-k dielectrics will have to be used to obtain the aggressive EOTs needed. Furthermore the lack of drain induced barrier lowering (DIBL, see red dotted area in Figure 4.2(a)) should be noted when comparing the I-V curves at V_{DS}=1V and V_{DS}=0.1V. This is caused by the fact that the drain has little influence on the (source) SBH (Figure 4.4(b)) which dictates the subthreshold behavior. This is the case because the for SB devices important tunneling width is in the range of the characteristic length, which is much smaller than the channel length of the device. The latter obviously being of importance for the conventional MOSFETs (for more see paragraph 4.7). It was however shown in [22] that as the SBH is reduced and the device becomes more diffusion limited, DIBL as expected, once again becomes a problem. Finally it is important to note that comparable (apart from the one order current shift, Figure 4.3) results are obtained with Silvaco's device simulator package [51] and those obtained by Jhaveri using the Dessis device simulator package [52].
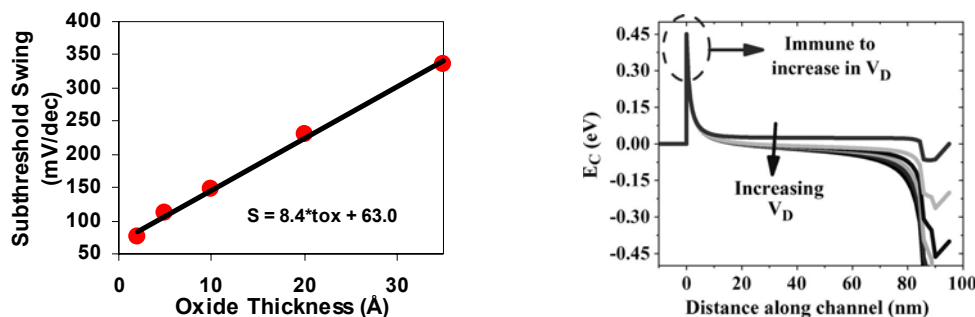

Figure 4.4: a) Simulated subthreshold swing against the oxide thicknesses
b) Conduction band edge along channel for different V_D [23]
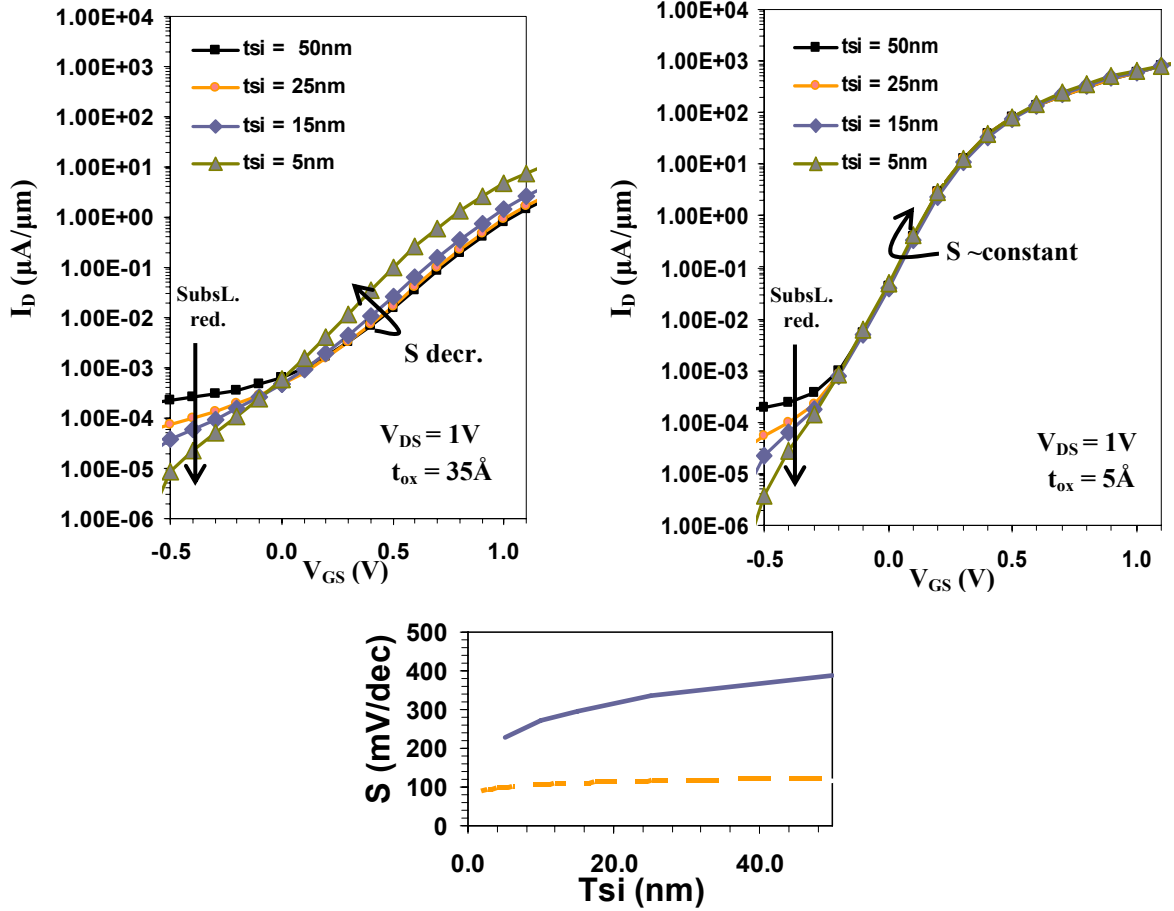
4.4. Effect of Si Film thickness

Figure 4.5: a) I_D-V_{GS} **characteristic for different silicon film thicknesses –** T_{OX} **= 35 Å**
b) I_D-V_{GS} **characteristic for different silicon film thicknesses –** T_{OX} **= 5 Å**
c) The simulated subthreshold swings at different film thicknesses for both T_{OX} **= 35 Å (solid line) and** T_{OX} **= 5 Å (dotted line)**

It can be seen from Figure 4.5 (a) that the device with an oxide thickness of 35 Å shows an S decrease for decreasing Si film thicknesses (t_{Si}). This is consistent with (Eq. 12 as proposed by Knoch *et al.* For the 5 Å oxide devices however S is shown to be almost entirely independent of t_{si} variations, which does not agree with (Eq. 12. The same effect was observed and addressed in [49] by Knoch *et al.* This resulted in a rule of thumb formula stating that SOI SB-MOSFETs show improvements of carrier injection (subthreshold swing) when $t_{si} <= 6\sim7*t_{ox}$. The derivation of this formula will not be treated, but it does coincide with the observation shown in Figure 4.5. The above observation has the important implication that devices with rather thick EOT's can still exhibit steep subthreshold swings if the body is scaled to extremely small thicknesses such as the case in nanoribbons, or in "two-dimensional" gate devices such as nanowires or nanotubes.

Also worth noting is that the always present thermionic subsurface leakage which happens along the complete channel depth (unlike the upper ~5nm along which tunneling dominates) is indeed reduced with decreasing Si film thickness. This

reduction is clearly visible at negative V_{GS}'s where the tunneling component is still less than the thermionic emission component.

Finally it can be observed that the current levels in Figure 4.5 (a) are lower than those in Figure 4.5 (b), which is directly related to the reduced gate induced electric field at the source SB due to the thicker gate oxides.

4.5.　　*Temperature dependence*

It was previously claimed by Jhaveri *et al.* [22] that because of the barrier tunneling nature of the carriers in SB-FETs the subthreshold swing would only be weakly dependent on the temperature *T*. This would therefore lead to superior subthreshold characteristics at typical device operating temperatures (~85^{0}C), even though the same 60m*V*/dec hard limit was observed at room temperatures (Chapter 4.3).
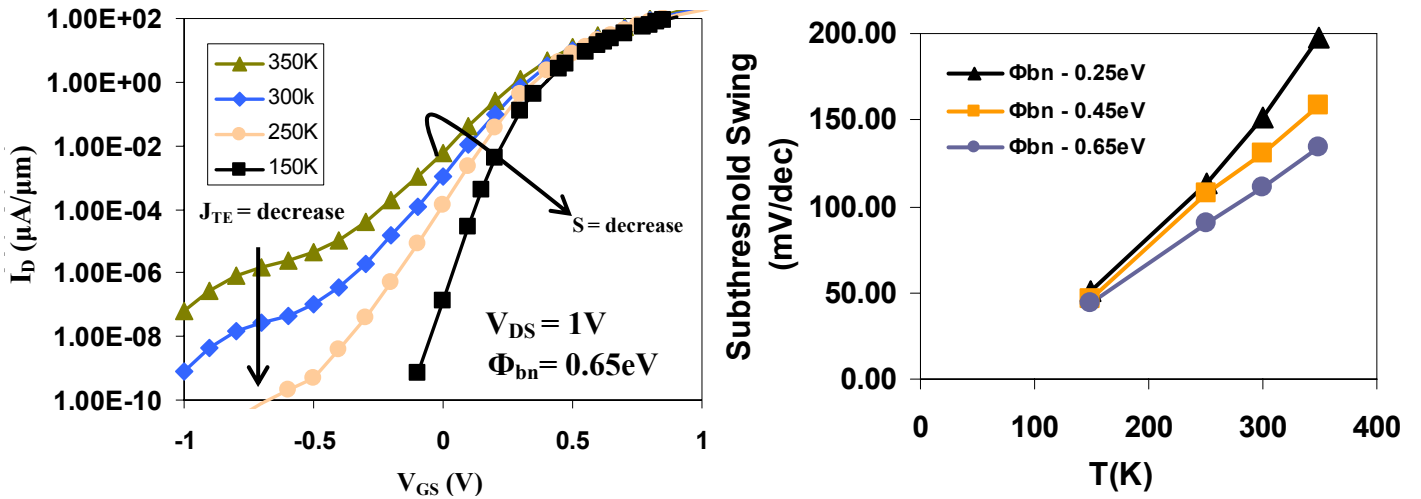

Figure 4.6: a) *I_D-V_{GS}* **characteristic showing** *T* **dependence of the tunneling limited subthreshold slope**
b) Extracted subthreshold slopes at different *T***'s and different source barrierheights.**

This claim was incorrect as seen in the above graphs which show strong reliance of *S* on *T*. This observed behavior is also consistent with (Eq. 12) as proposed by Knoch *et al.* and with the experimental results obtained by Snyder *et al.* in [30].
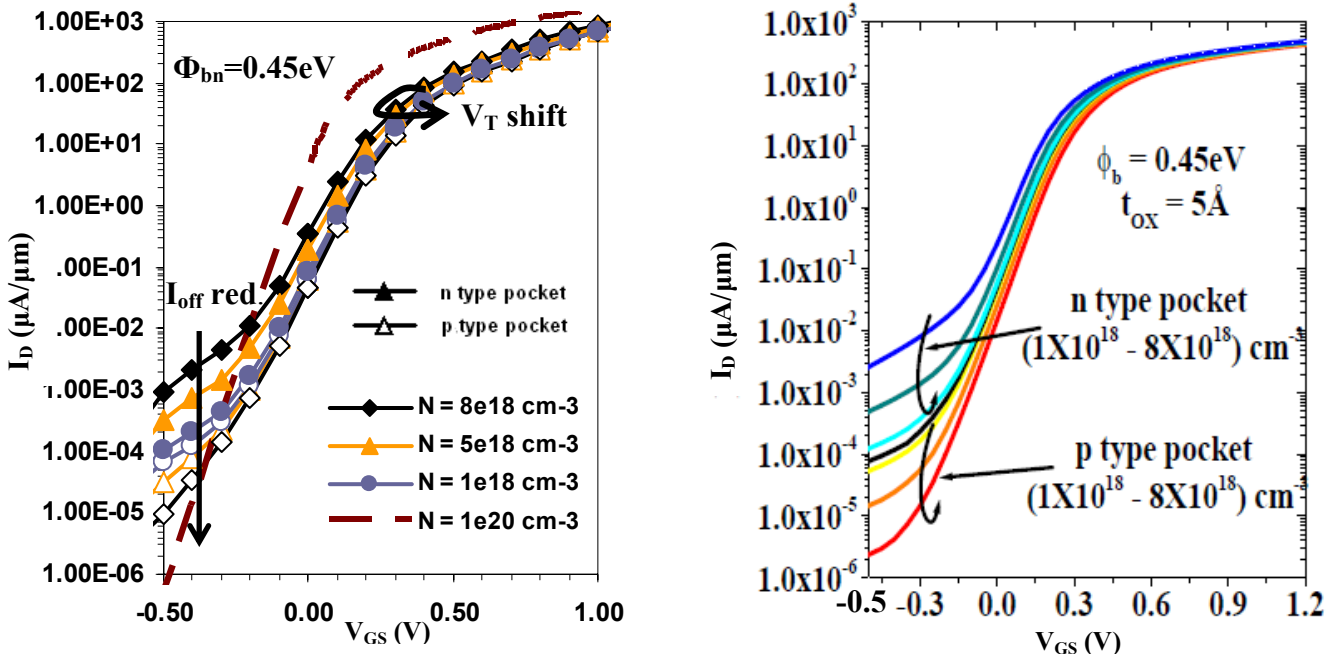
4.6.   *Source Side Pocket effect*

Figure 4.7: a) I_D-V_{GS} **characteristics with changing source side pocket doping**
       b) Same results but those obtained by Jhaveri [24] using Dessis's device simulator

As discussed in chapter 2.2 ("Barrier-Height Adjustment" section) pocket implants next to Schottky junctions can be used to increase or decrease the SBH. It was shown that p-type pockets resulted in an increased electron barrier height while n-type pockets resulted in a decrease. While the subthreshold swing is relatively constant it can be clearly seen in Figure 4.7 that the p-type pockets indeed suppressed the subsurface conduction (reduced I_{off}). This is because of the higher barrier for the thermionic leakage present along the complete Schottky junction depth. The reason why this effect is not noticeable in the subthreshold slope and also not in I_{on} is that the gate induced electric field (at V_{GS} >0V) has a larger influence on the Schottky barrier reduction than the slight barrier increase created by the p-type pocket implant. However there is a slight threshold voltage (V_T) shift observed due to the pocket implants. Since the (p-type) pocket implants reduce I_{off} while keeping I_{on} relatively constant one could use these to increase the I_{on}/I_{off} ratio of these devices. Obviously aggressive pocket implants such as these are technologically complex and should only be used if the benefits outweigh the added device complexity.

Furthermore it should be noted that the pocket implants should be completely depleted. If for instance a 5 *nm* pocket with a doping of 10^{20} *cm*$^{-3}$ is used the maximum depletion layer width would be around ~3.5 *nm* (thus not fully depleting the pocket) essentially creating a conventional MOSFET (see I_D-V_{GS} characteristic dotted line Figure 4.7a) with a narrow (~1.5 *nm*), but still conventional, highly doped source instead of a SB source.

4.7. V_T roll-off

Before focusing on device scalability with respect to V_T roll-off it is important to briefly elaborate the V_T extraction method used. There are numerous ways of extracting V_T experimentally of which the two most often used are the "slope" method and the constant current method [53].

For the Schottky tunneling FETs it turned out that because of the more quadratic (instead of exponential) nature of the subthreshold regimes, V_T extraction through the slope method resulted in obtained V_T's that showed a decreasing trend for increasing channel length, which seemed highly unlikely. The constant current method on the other hand showed a decreasing V_T trend for decreasing channel lengths and for that reason was the method used (Figure 4.8).
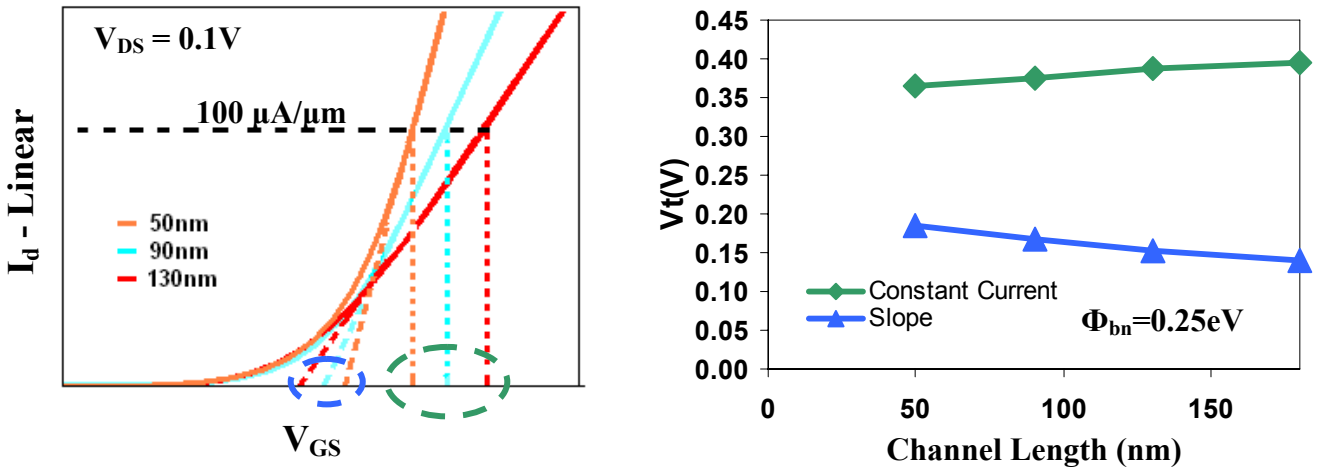

Figure 4.8: a) (Exaggerated) I_D-V_{GS} curve representation showing the origin of the differences in extracted V_T's b) Actual V_T values using both extraction methods for an asymmetric STS-FET with a source Φb_n=0.25eV

In Figure 4.9 it can be seen that the V_T roll-off for SB-FETs is much less than the threshold shift noticed in conventional SOI MOSFET showing once again that these SB-FETs are highly immune to short channel effects (SCE) and therefore highly scalable, without the need of for instance halo doping and shallow S/D extensions. From the V_T roll-of graph Figure 4.9 it can also be seen that the SB-FET SCE's are actually increasing for increasing barrier heights, which initially might seem counter intuitive. This can however be explained by the fact that an increase in barrier height yields an increase in the metal workfunction Φ_M resulting in an increased built-in potential V_{bi} (Φ_s is constant, since bulk doping is constant). Because of this the depletion layer width W_{DMAX} (Eq. 14) is increased resulting in a larger tunneling width and as such a stronger V_T change (through "drain induced tunneling width modulation") when going to shorter channel lengths (Figure 4.4(b)).

(Eq. 14) $$W_{DMAX} = \sqrt{\frac{2\varepsilon_{si}2V_{bi}}{qN_D}} \qquad V_{bi} = \Phi_M - \Phi_S$$
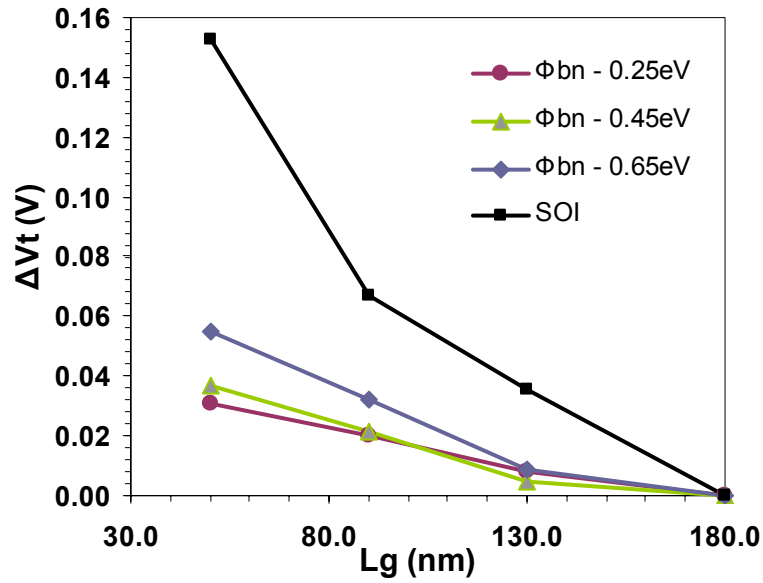
34

Figure 4.9: Absolute V_T-Roll off normalized at V_T of an 180nm long device.

The all around higher V_T roll-off immunity of the SB-FETs is directly related to its previously mentioned high immunity to DIBL (Figure 4.4(b)). In the conventional MOSFET the drain current is controlled by the gate bias which modulates the full channel potential under the gate electrode and in the (tunneling limited) SB-FETs the drain current is solely modulated by the electric field (tunneling width) at the source-channel Schottky barrier. This leads to a weaker electrostatic coupling of the drain and source (@ short channel lengths) such that the drain bias can not affect the potential barrier at the source junction as heavily as for the conventional MOSFETs. This results in the smaller V_T shifts for SB-FETs. Therefore only when channel lengths start entering the regime of tunneling widths will there be significant drain influence on (tunneling limited) SB-FET behavior (see (Figure 4.4(b)). For conventional (diffusion limited) MOSFETs (where the potential along the complete channel is of importance) on the other hand significant drain influence on device behavior can already be seen at larger channel lengths (as seen in Figure 4.9).

4.8.   *Source gate underlap*

For STS devices good gate electrostatic control of the SB at the metal - silicon interface is needed. This because the modulated tunneling current is governed by the gate induced electric field at the Schottky junction. Keeping this in mind the formation of an underlap between the gate and the Schottky junction (see Figure 4.10a) would drastically reduce the gate modulation of the tunneling current and consequently the maximum saturation current. The reduction of the latter has to do with an increased tunneling resistance (which is proportional to the tunneling width) which limits the maximum current flow (Figure 4.10b). Figure 4.10 visualizes the importance of good gate (-source) electrostatic control for these STS-FETs, showing that minor nm range gate (-source) underlaps (due to process glitches etc) could have a drastic influence on the behavior of these devices. The necessity of good gate electrostatic control for STS-FETs has been discussed in numerous papers [3, 18, 40, 54, 55] and everything from using thin sidewall spacers to gate last techniques have been proposed to keep underlap to a minimum.
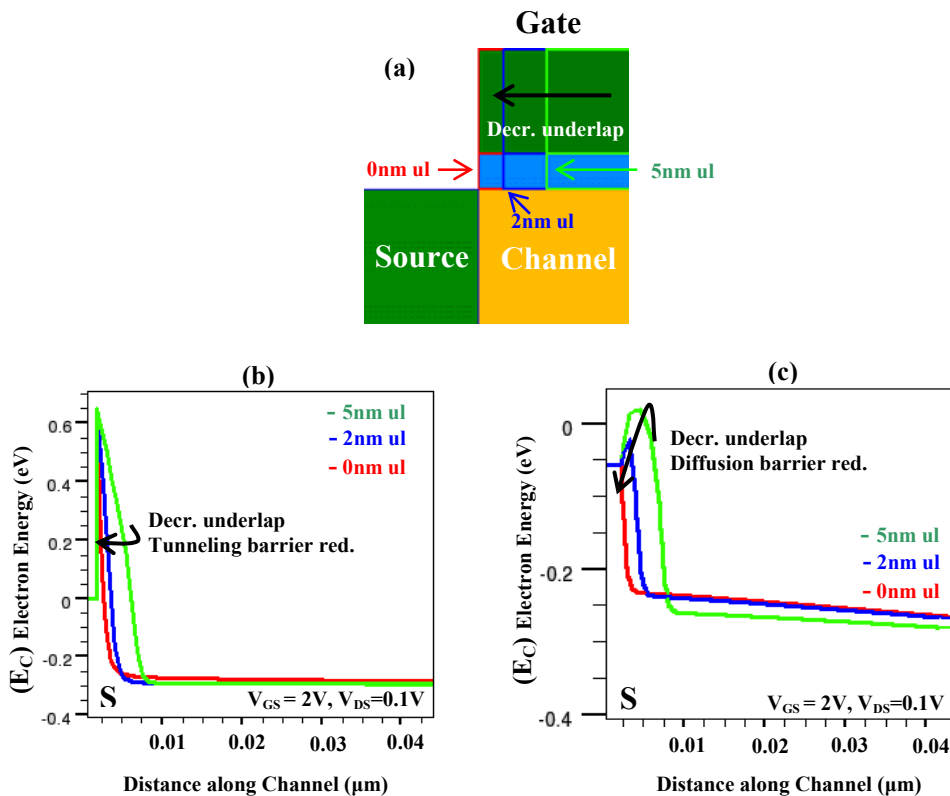

Figure 4.10: Modulation of the conduction band edge profile @ different gate underlap lengths (5 *nm* 2 *nm*, 0 *nm*) for a tunneling limited SB-FET(b) and a conventional diffusion limited SOI MOSFET (c)

When comparing the effect of gate underlap between the conventional SOI FET and the STS-FET it's clear that the reduction of gate control, although present, is much less for the conventional diffusion based devices (see Figure 4.11, note different scale). This strong reliance on gate position with respect to the available (Schottky) tunneling current will be exploited (and treated more in depth) in the newly proposed asymmetric gate SB-FET (AsymG SB-FET) described in chapter 5.
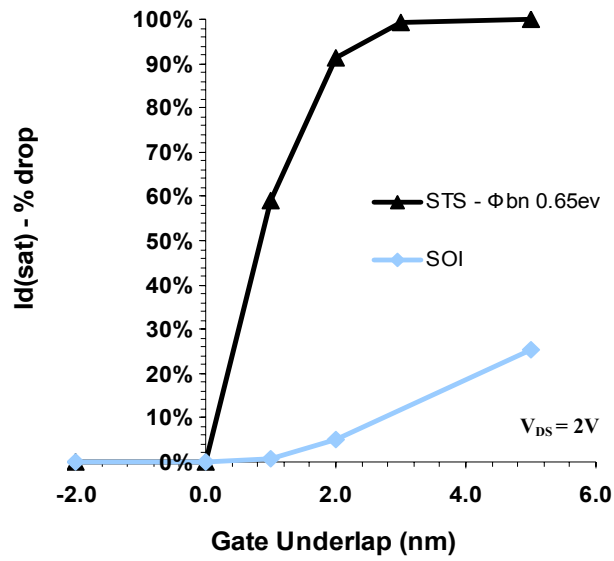
Figure 4.11: Gate underlap and its effect on gate electrostatic control loss (given in I_{Dsat} % drop) for conventional and STS-FETs

Although gate overlap is more desirable than gate underlap (see Figure 4.11) it is important to have the least amount of overlap particularly as one scales to increasingly aggressive gate lengths. This is because the degraded subthreshold slopes, steeper V_T roll-offs (due to SCE's) and increased capacitances associated with close S to D placement will start to offset any advantages of having an overlap [55].

5. The asymmetric Gate SB-FET (AsymG SB-FET)

Since the device advantages of the asymmetric Schottky tunneling source Fet (STS-FET) by Jhaveri *et al.* (chapter 4) are based on the creation of a drain side Ohmic contact through a highly doped pocket, the thermal budget advantages associated with a metallic source and drain will be reduced. Pocket activation will not only increase the thermal budget but also complicate the overall process as these types of narrow abrupt implants are technologically difficult to produce. In this chapter a novel doping free asymmetric Schottky tunneling device will be proposed (The Asymmetric gate SB-FET, AsymG SB-FET [Boksteen *et al.*[56]][13]) that alleviates the technological complications faced with pocket implants while still maintaining some of the advantages of the STS-FET [57].

The basic premise of the AsymG SB–FET is tunneling leakage reduction through creation of a drain side gate underlap (Figure 5.1a). Since the modulated tunneling current is a strong function of the gate induced electric field at the Schottky junction (chapter 4.8) it is reasonable to assume that reducing the gate induced electric field at the drain (through underlap) will also reduce the reverse drain tunneling leakage (Figure 5.1b) and consequently the ambipolar effect. Lin *et al.* used a variation of this technique in their 2002 paper [57] on ambipolar poly-silicon TFTs while more recently Krishnamohan *et al.* used drain side gate underlap to reduce band to band tunneling leakage in their double gate tunneling FET [58]. However, a comprehensive analysis of Schottky tunneling leakage suppression through a gate-drain underlap as performed in the coming sections was never performed and only briefly mentioned by Tucker *et al.* in [16].
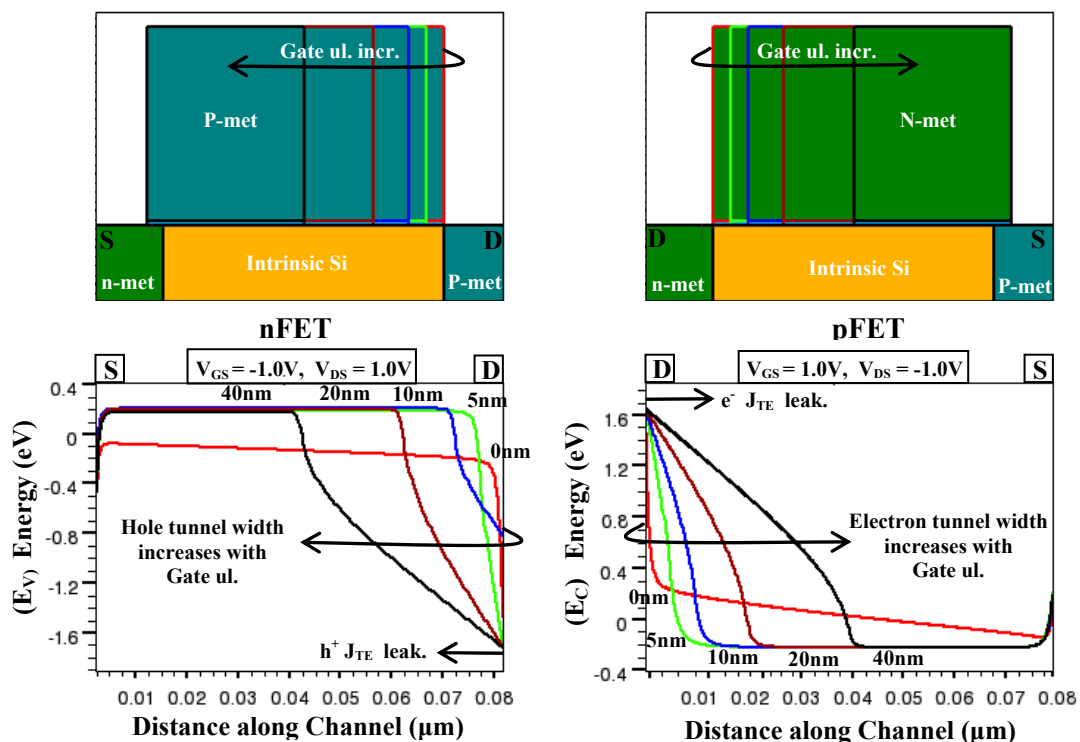

Figure 5.1: a) Schematic cross-section showing gate underlap (0, 5, 10, 20, 40 *nm*) chances for N (left) and P (right) FETs

b) Band graphs showing tunneling leakage barrier width increases with increasing gate underlap

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[13] to be submitted to IEEE Electron Device Letters (EDL) 2010

5.1. *Device parameters*

The Asymmetric gate SB-FET behavior depends on the use of different metal types as source, drain and gate materials. The names used to distinguish these different metals are listed in Table 5.1.

Metal type	Workfunction (eV)	Barrierheight (eV)	
N+ type	4.17 (χ_{si})	-	
Midgap	4.73 (χ_{si} + 0.5 E_G)	$\Phi_{Bn\,p}$ = 0.56	
P+ type	5.29 (χ_{si} + E_G)	-	Metal
N-metal	4.82	Φ_{Bn} = 0.65	Al, NiSi
P -metal	4.57	Φ_{Bp} = 0.72	Er

Table 5.1: The different metal types used in the simulations

The naming convention "N" and "P" metal seen in Table 5.1 is not based on the metal's workfunction similarity to N or P doped Si (which is the conventional naming method) but rather on the type of carriers passing the Schottky barriers created between these metals and the Si channel. An N-Metal in this case therefore denotes a metal acting as an electron tunneling source while a P-metal denotes a hole tunneling source. Furthermore Φ_{bn} and Φ_{bp} are the electron and hole barrier height of resp. the N and P-metals. The barrier height values of the N and P- metals summarized above are the standard values used throughout this chapter and correspond with actual measured barrier heights [59] of the metals stated in Table 5.1. Unless stated otherwise the metals used as gate material will be the same as the drain metal type (P-metal gate for the nFET and N-metal gate for the pFET, Figure 5.1a). This on the one hand has to do with tuning V_T of the devices while on the other hand minimizing the amount of metals used (for a more in-depth analysis see chapter 5.5). Finally the channel material used will simply be intrinsic Si unless stated otherwise. The choice of lowly doped/intrinsic Si, as was mentioned by Larson *et al.* [3], is possible due to the built-in SB at the MS-interface which acts as a quasi-pocket or halo implant allowing for low channel doping without deteriorating the SCEs[14].

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[14] In conventional short-channel FETs with lowly doped Si the source and drain PN junctions would strongly influence the Si depletion underneath the gate (provided that no halo or pocket implants are used) causing large V_T shifts (Figure 4.9)

5.2.   *The Asymmetric Gate SB-FET working principles*

Comparing the band plots from Figure 5.1b and their corresponding I_D-V_{GS} curves depicted in Figure 5.2 indicates that a drain side gate underlap is indeed effective in suppressing the reverse tunneling leakage current. For instance for the nFET if there is no gate underlap and a gate-voltage of V_{GS} = -1.0V is applied, the channel region will be completely filled with holes (volume inversion), with the (ambipolar) current limited only by the holes tunneling at the drain (Figure 5.1b). Increasing the underlap region increases the tunneling width (which is a barrier to hole injection) reducing the hole concentration under the gate resulting in the reduced ambipolar effect as seen in Figure 5.2b. It is seen that at ~40 *nm*[15] underlap the reverse tunneling leakage is completely suppressed and will therefore (unless stated otherwise) be the underlap length used for all coming simulations. The same holds for the pFET making CMOS digital circuit implementations using the same n- and p-type metals a possibility. This is the case because a gate overlapping the N-metal will modulate the source side electron tunneling current (and the P-metal underlap will minimize the hole leakage current modulation) creating a nFET, while an overlap across the P-metal will result in hole tunneling modulation creating a pFET.
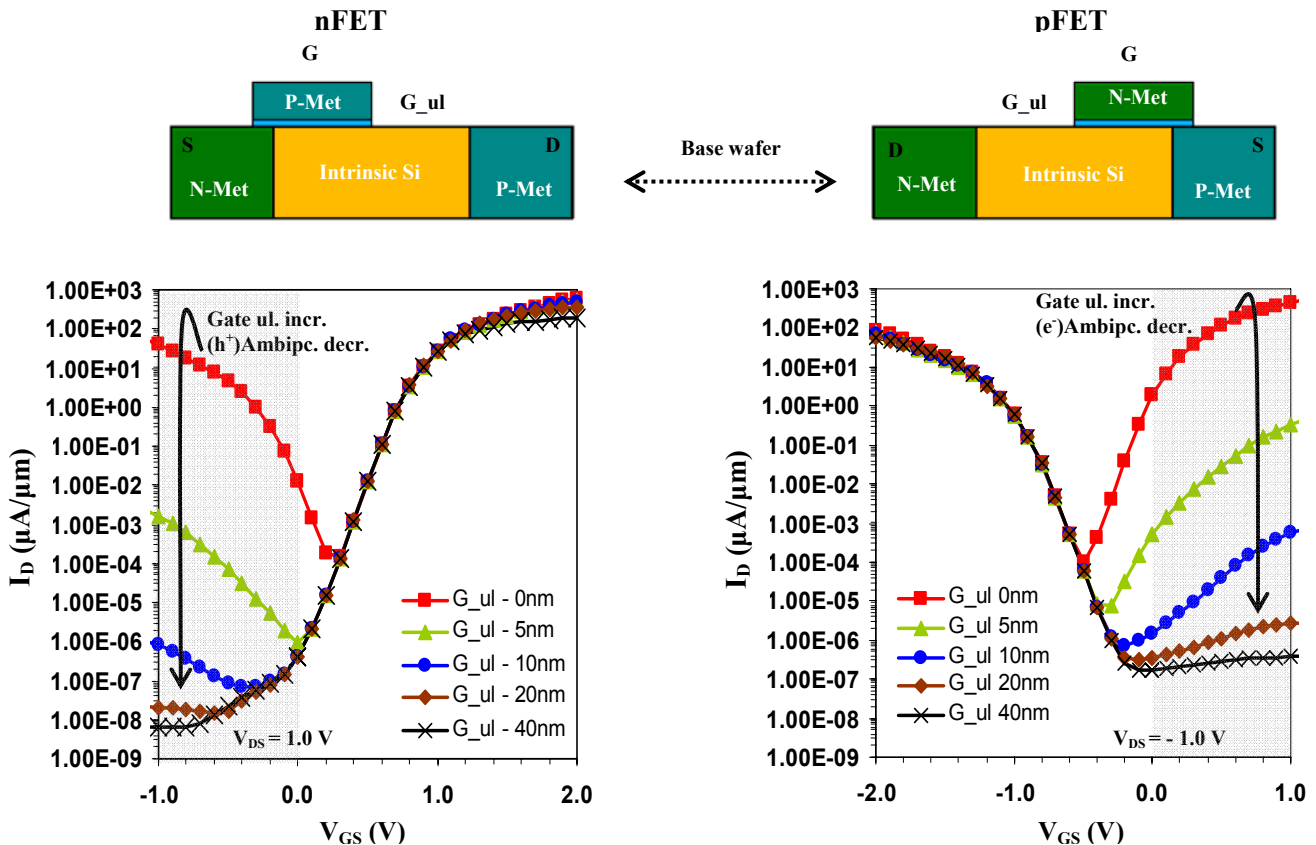

Figure 5.2:a) Schematic cross-section of both the N and P-type AsymG SB-FET (BOX under active area not shown, Channel length = 80nm)
b) I_D-V_{GS} characteristics of (a) N and (b) pFETs with different gate underlap lengths

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[15] The same underlap length was used by Krishnamohan *et al.* [58] for effective Band to Band leakage suppression.

There could be some technological advantages of the gate position alone deciding the type of FET manufactured. For instance a gate last technique would create an opportunity through which a base wafer (figure 5.2a) with standardized Source/Drain metal formations can be mass produced, with the type of FET being created simply decided later in the process by the position of the gate.
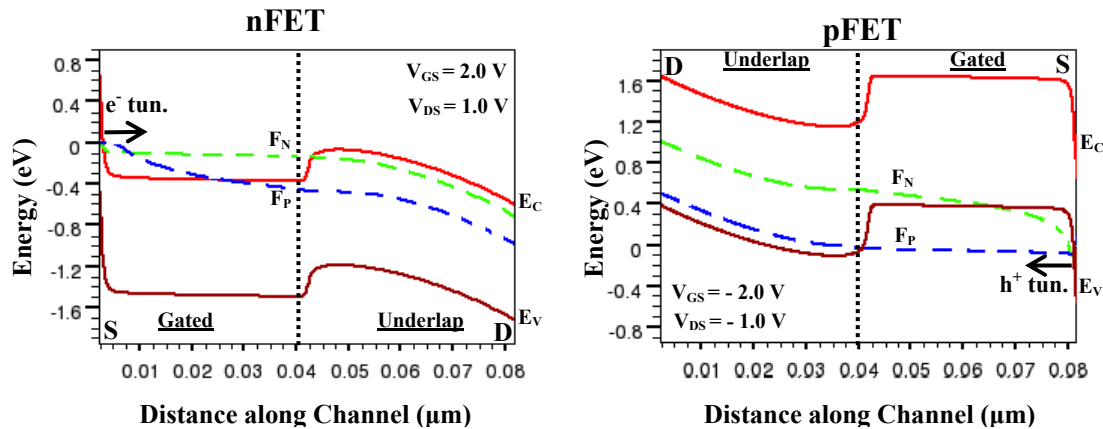

Figure 5.3: Simulated band diagrams of the n- and pFET in on-state showing the conduction band (E_C), valance band (E_V), the electron quasi Fermi Level (F_N) and the hole quasi Fermi level (F_P)

As shown in Figure 5.3, the band diagram of the AsymG SB-FET in on-state indicates a series coupling of a normal gate modulated FET (the gated region) and a region containing a potential barrier. The later basically forms a forward biased diode (of poor quality) in the underlap region. In this state the lateral electric field created by the applied drain potential causes the source injected carriers (e^- for a nFET or h^+ for a pFET) to be swept from the tunneling source, through the gated region and the forward biased diode, eventually to the drain.
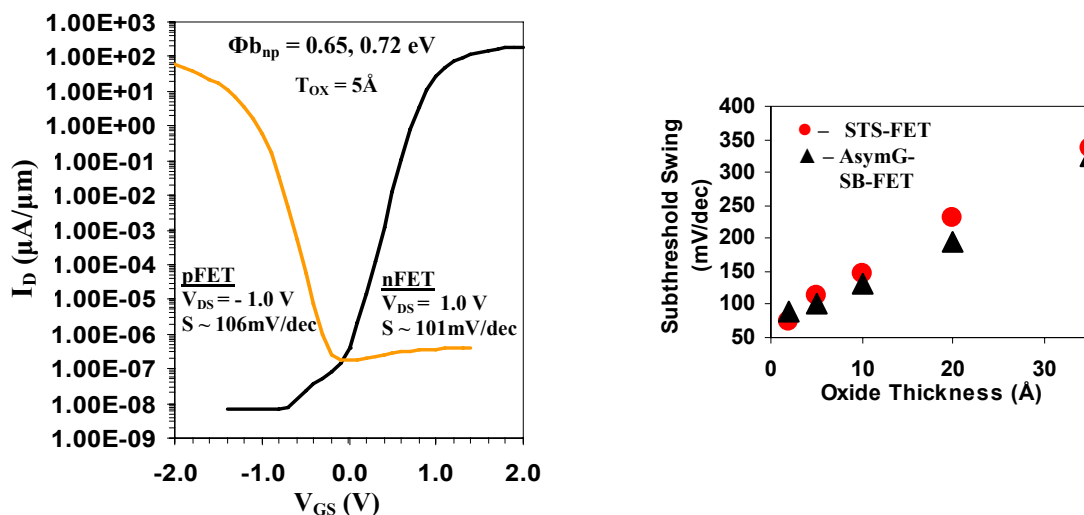

Figure 5.4: a) I_D-V_{GS} curve of both the AsymG n and p SB-FET with 40nm underlap
b) (nFET) Subthreshold swing vs. oxide thickness plot comparison between the STS-FET and the AsymG SB-FET

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Figure 5.4a shows the I_D-V_{GS} characteristics of both the simulated n- and pFETs while Figure 5.4b (and Figure B.1) shows the subthreshold swing (S) vs. oxide thickness comparison of the AsymG SB-FET and its previously discussed STS-FET counterpart. There is a slight difference seen between the subthreshold swing of the p and nFET (Figure 5.4a) which is caused by asymmetric source drain metal choice. Furthermore the subthreshold swings characteristics with respect to oxide thickness for the STS-FET and the AsymG-FET (Figure 5.4b and Figure B.1) are similar, allowing the conclusion to be drawn that drain underlap does not influence the device's subthreshold characteristics. This is caused by the fact that the drain does not (strongly) influence the source side tunneling modulation (Figure 4.4b). Finally a (max) $I_{ON} - I_{OFF}$ ratio of ~8 orders of magnitude for the pFET and ~10 orders for the nFET is obtained. With the difference between these values mainly caused by the reverse thermionic emission leakage as addressed in the following chapter.

5.3. *Drain side thermionic leakage*

From the band graphs in Figure 5.1b it can be seen that although the tunneling leakage is reduced with increased gate overlap, the thermionic leakage current (J_{TE}) stays the same. The inability of the gate underlap technique to minimize the reverse thermionic emission leakage and the differences in the used metal barrier heights are the main causes for the off current difference seen in Figure 5.4a. In chapter 2.2 the thermionic emission was described as being inversely proportional to the exponent of the SBH (eq. 3). Consequently for effectively minimizing the thermionic leakage high drain barrier height (Φ_{Bp} for nFETs, Φ_{Bn} for pFETs) metals should be used, as clearly seen in Figure 5.5a and b. The ability to "freely" choose such a high drain barrier height metal is one of the main advantages associated with having asymmetry in the source and drain metals.
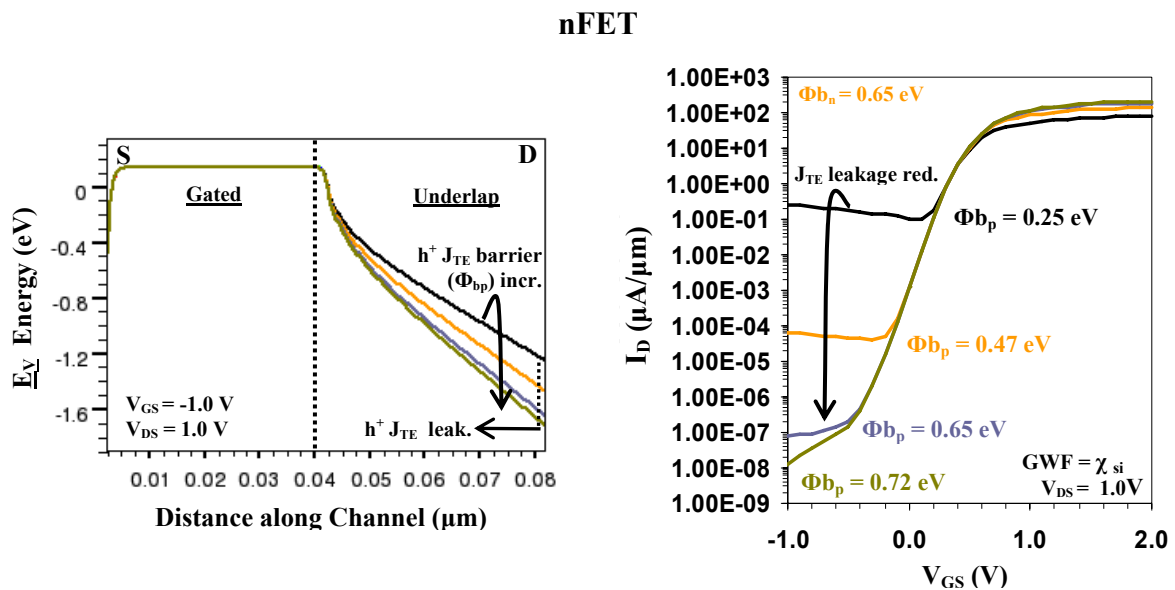
nFET

Figure 5.5: a) Valence band edge at different drain barrier heights (Φb_p)
b) I_D-V_{GS} curve showing the impact of drain barrier height (Φb_p) on the thermionic leakage current

5.4.   *The single metal AsymG SB-FET*

Figure with y-axis labeled $I_D^{'}$ ($\mu A/\mu m$) ranging from 1.00E-06 to 1.00E+03, x-axis labeled V_{GS} (V) from -2.0 to 2.0. Annotations: $\Phi b_{np} = 0.56$ eV; pFET V_{DS} - 1.0 V, S ~ 119mV/dec; nFET V_{DS}= 1.0 V, S ~ 112mV/dec
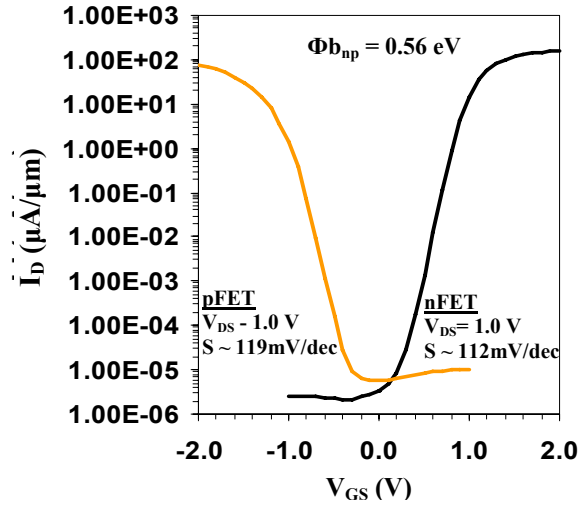
Figure 5.6: I_D-V_{GS} characteristics of the single (midgap) metal AsymG n- and p SB-FET

Now that the main cause of leakage current in the AsymG SB-FET has been discussed it is understandable that a single metal device solution for the creation of both n- and pFETs will necessitate the use of a midgap metal. Figure 5.6 shows the n- and pFET I_D-V_{GS} characteristics obtained when using such a metal. The difference seen in off current between the n- and pFET is likely due to J_{TE} being proportional to the Richardson's constant (Eq. 3) which is dependant on the slightly different hole/electron (DOS) effective mass(M_p>M_n). And since the tunneling current ($J_{(T)FE}$) on the other hand is *inverse* exponentially dependant on the effective tunneling mass (Eq. 7) this could explain the slightly better nFET subthreshold swing.

Choosing a midgap metal will maximize the I_{ON}-I_{OFF} ratio obtainable for a single metal nFET, pFET solution. If however a non-midgap metal is used either one of the created FETs will have a higher off current than shown for the ideal situation depicted in Figure 5.6. The cause of this being the complementary nature of SBHs (Φ_{Bp} + Φ_{Bn} = E_G, Figure 2. 2). This shift from ideal behavior is clearly seen when comparing the I_{ON}/I_{OFF} ratio of the AsymG SB-FET in Figure 5.5 with a drain metal barrier height of Φ_{Bp} = 0.47eV [16] and that of the nFET in Figure 5.6. Keeping in mind the complementary nature of the barrier heights it should be noted that if only one type of FET is to be created, a single metal setup where the source barrier height is below midgap might result in better I_{ON} at low V_{GS}'s (Figure 4.1 and see chapter 5.6 why it might not be the case) because of the smaller source side resistance (causing increased J_{TE} and J_{FE}, Figure 3.4) associated with lower source barrier heights. Eventually going below this midgap barrier height will result in the creation of a diffusion limited AsymG SB-FET (see chapter 3 for more on the diffusion limited SB devices).

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[16] This is a single metal device since the drain (Φb_p=0.47 eV, Φb_n=0.65 eV) and source (Φb_n=0.65 eV, Φb_p=0.47 eV) metals are the same

5.5.   *Gate work function engineering:*

Gate workfunction engineering is the act of shifting the threshold voltage through changing the gate workfunction. The relation of these values can be understood if one keeps in mind that for FD-SOI the threshold voltage is more or less equal to the flatband voltage ($V_T \sim V_{FB}$) [11]. With the flatband voltage being:

(Eq. 15)
$$V_{FB} = \Phi_M - \Phi_S$$

where Φ_M is the gate metal workfunction and Φ_S the Si channel workfunction.

If $V_T \sim V_{FB}$ it is clear that the V_T shift is negative for a gate workfunction decrease and positive for a gate workfunction increase (see Figure 5.7).

Because of this shift, the ideal setup to minimize the amount of metals is to use the drain metal as the gate metal, thereby creating an nFET with a P-metal gate and a pFET with a N-metal gate. In the case depicted in the figures below this is seen to be a viable option giving the best I_{ON}/I_{OFF} ratio (with low V_T). The final gate metal choice is however, just like with conventional FETs, based on tradeoffs between device functionality and technological feasibility. An example of such a tradeoff would be the decision to use a midgap metal gate for the pFET (light blue line, Figure 5.7(b)). This would result in similar I_{ON}/I_{OFF} performance (compared to the case of the AsymG SB-FET with the same drain and gate metal) while reducing V_T, however this increases device complexity.
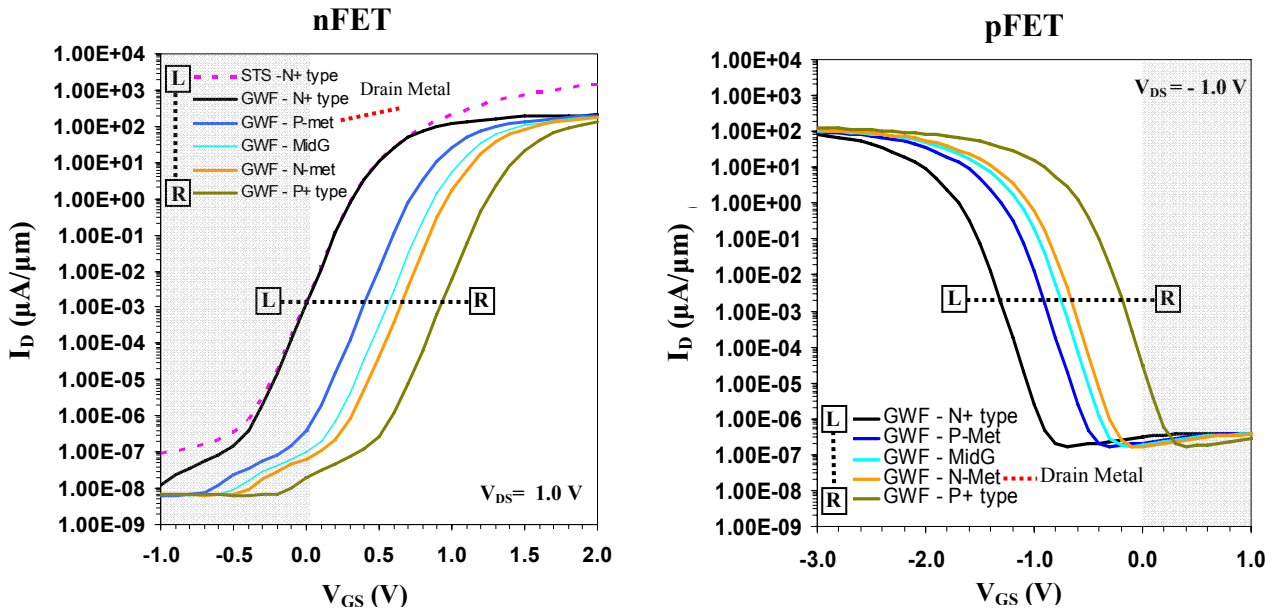

Figure 5.7: Full V_T **shift range due to gate work function engineering for both the AsymG n- (a) and p SB-FET(b). In these graphs *only* the gate metals are altered. Also included in (a) is chapter 4's STS-FET showing comparable I_D-V_{GS} characteristics.**

5.6. *Maximum theoretical obtainable $I_{ON} - I_{OFF}$ range*

After reading sections 5.3 and 5.5 it is understandable how one would obtain the maximum theoretical I_{ON}/I_{OFF} ratio using the AsymG device structure (Figure 5.8). This maximum is reached by using full bandgap (E_G=1.12eV) barrier height metals, essentially using a P+ type ($\Phi_M = 1.12eV + \chi_{si}$) N-metal and an N+ type ($\Phi_M = \chi_{si}$) P-metal.
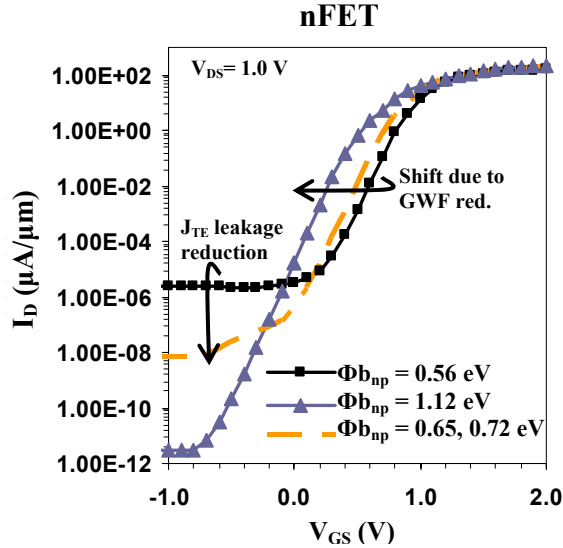
nFET

Figure 5.8: $I_D - V_{GS}$ **characteristic showing the maximum theoretical attainable** $I_{ON} - I_{OFF}$ **ratio with both the single metal (midgap) and dual metal AsymG SB-FETs as comparison**

The choice of both the source and drain metals having resp. full electron / hole bandgap barrier heights is again based on wanting to use the base metals for both the creation of n and pFETs (as discussed in chapter 5.4). Furthermore this full-bandgap barrier height S/D solution is a good example of a case where (because of the gate workfunction influence on the V_T shift, chapter 5.5) using the drain metal as the gate metal gives undesirably high I_{OFF}. Simply using a (third metal) gate with a higher workfunction than that of the N+type metal gate used here should however shift the curve to the right (Figure 5.7a) resulting in better I_{OFF}. This, as seen in chapter 5.5 shows that, although more complex, introducing a third metal as gate will result in the most ideal situation.

Finally it can be seen that the I_{ON} current of the AsymG-FET is not effected by the choice of the source barrierheight. This is caused by the potential barrier at the gate-underlap region, which unlike with the STS-FET[17] of Figure 4.1, forms and important additional current limiting factor.

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[17] Where the SBH clearly is the I_{ON} current limiting factor

5.7.　　*The AsymG SB-FET based CMOS inverter:*

The CMOS inverter forms one of the most important blocks in today's ultra large scale integrated (ULSI) circuits. The main advantage of this complementary MOS combination is its low power consumption. This can be easily illustrated when analyzing the basic inverter circuit of Figure 5.9a. As seen the inverter consists of an n and pFET of which the drains are connected to one another forming the output, while the input terminal is the common connection to the transistor gates. Since the pFET has a negative and the nFET a positive threshold voltage (Figure 5.4a, Figure 5.6), a positive V_{IN} turns the nFET on and the pFET off, connecting V_{OUT} to GND. Conversely a zero voltage on V_{IN} results in the full V_{DD} voltage being measured at V_{OUT} as the nFET is then turned off while the pFET is turned on. This results in the creation of an inverter with low power consumption since there is a series connection of which one of the devices is turned off for either state.
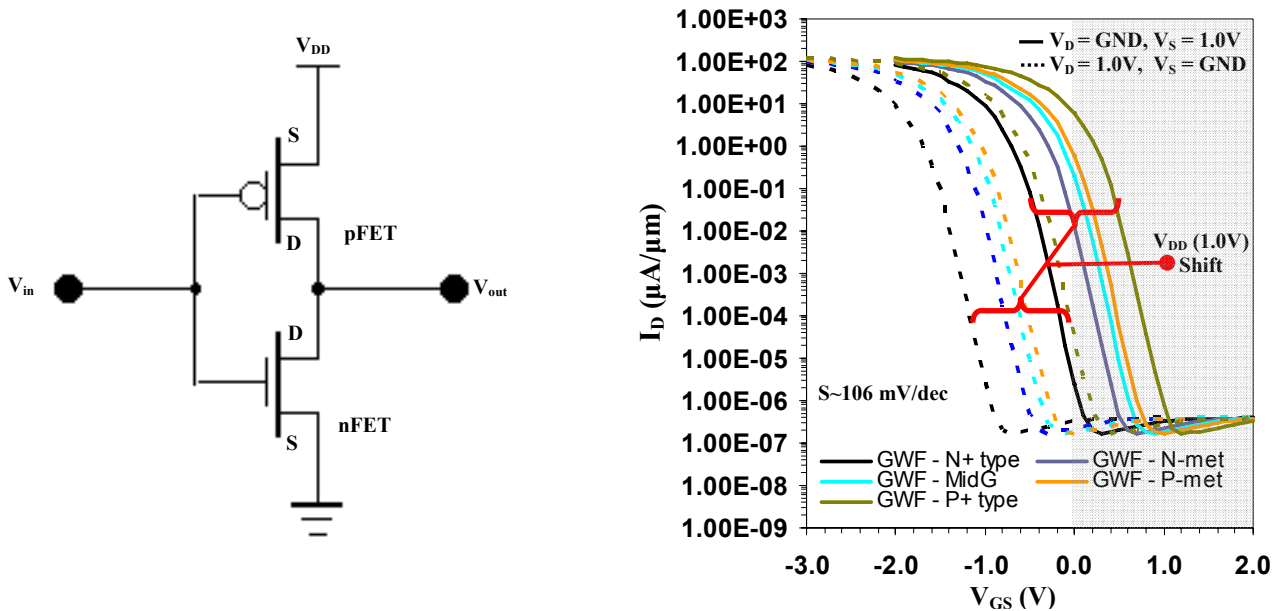

Figure 5.9: a) CMOS inverter
> **b) I_D-V_{GS} characteristics showing a shift due to source side channel potential modulation**
> **(solid lines) compared to the conventional drain side potential modulation (dotted lines)[20]**

Since in the case of the CMOS inverter one actually modulates the pFET channel by applying a source instead of a drain side potential (still resulting in the negative V_{GS}[19] necessary to turn on the device) it was important to verify that this did not influence the AsymG-p SB-FET device behavior. The reason for this verification being that since Schottky tunneling carrier injection is highly sensitive to source side conditions the extra source potential could possibly influence device behavior. Figure 5.9b however, shows that apart from the expected curve shift, source side channel potential modulation has no effect on device behavior (I_{ON}/I_{OFF} and subthreshold swings are the same). Thus making a straight forward AsymG n- and pFET implementation in CMOS based technologies a possibility.

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[18] Due to the rather high subthreshold swing it is seen that the device (using a P-Metal) isn't completely on when shifted by a V_{DD} of $1V$ this can be remedied by using a higher V_{DD} if necessary.

[19] $V_{GS} = V_G$-V_S , with $V_G = 0V$ and V_S = Positive

5.8.   *Intrinsic Channel I_D–V_{DS} behavior*

As previously mentioned the AsymG SB-FET can be interpreted as a series coupling of a gated FET and a (poor) diode (underlapped region). With this in mind the I_D-V_{DS} behavior seen in Figure 5.10b can be explained.
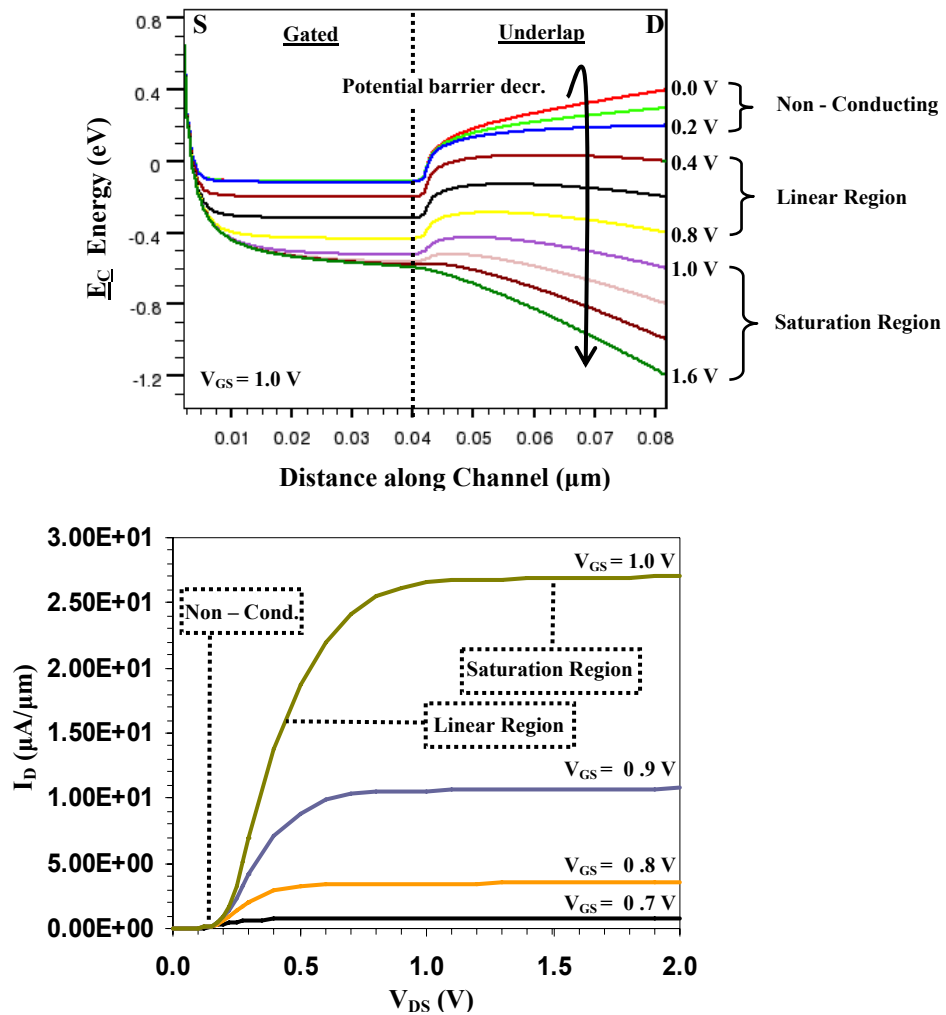

Figure 5.10: a) Drain bias influence on the conduction band edge showing a reduction of the in channel potential barrier with increasing drain biases.
b) I_D-V_{DS} plot of the implantless AsymG SB-FET showing a non-conducting region at low V_{DS}'s caused by the in channel potential barrier

Seen in the non-conduction region of Figure 5.10a is that the drain potential is essentially not strong enough to forward bias the series diode, resulting in a potential barrier blocking cross channel carrier transport (non-conduction region Figure 5.10b).

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As the drain potential is increased the non-conducting region is surpassed and the series diode gradually enters its forward biased regime allowing increasing amounts of carriers (linear region Figure 5.10) to flow from the injection source to drain. Ultimately this V_{DS} increase, as is the case in standard MOSFETs, results in saturation whereby the in channel potential barrier, seen in both the non-conducting and the linear region, is completely suppressed. Finally it is worth mentioning that the same behavior is observed (albeit with a reduction in I_{Dsat}) when using midgap metals instead of the N- and P-metals used above. However because of the higher (electron for nFETs and hole for pFETs) drain barrier height associated with midgap metals the non conducting (non-linear) region at low V_{DS}'s will increase while I_{DSAT} will reduce, thus resulting in worse I_D-V_{DS} behavior.

5.9. *Doped Channel I_D – V_{DS} behavior*

For analog purposes and ultra low power digital switching (low V_{DD}, V_{DS}) the situation seen in Figure 5.10b with its non conducing low V_{DS} range is anything but ideal. To alleviate this problem the potential barrier at low V_{DS} (Figure 5.10a) needs to be suppressed, which can be achieved by doping (N^+ for nFET, P^+ for pFET) the previously intrinsic underlapped region (see Figure 5.12).
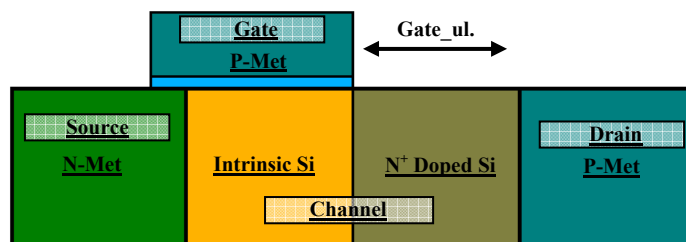

Figure 5.11: Schematic cross-section of the Asymmetric Gate SB-FET using drain side doping to reduce the in channel potential barrier

The positive effect of this type of pocket doping is clearly seen in the graphs of Figure 5.13 and Figure 5.14. The conduction band edge plot of Figure 5.13 (and the full band representation in Figure B.2) shows that the potential barrier at low V_{DS} is indeed lowered through a doping increase, which expectedly reduces the non-conducting region seen in Figure 5.13b. This leads to a drastic I_{ON} performance increase at low V_{DS}'s (Figure 5.14a) and a slight increase at higher V_{DS}'s (Figure 5.14b). The latter slight increase being the case since high V_{DS}'s already lower the potential barrier through drain side modulation (Chapter 5.8, Figure 5.10a).
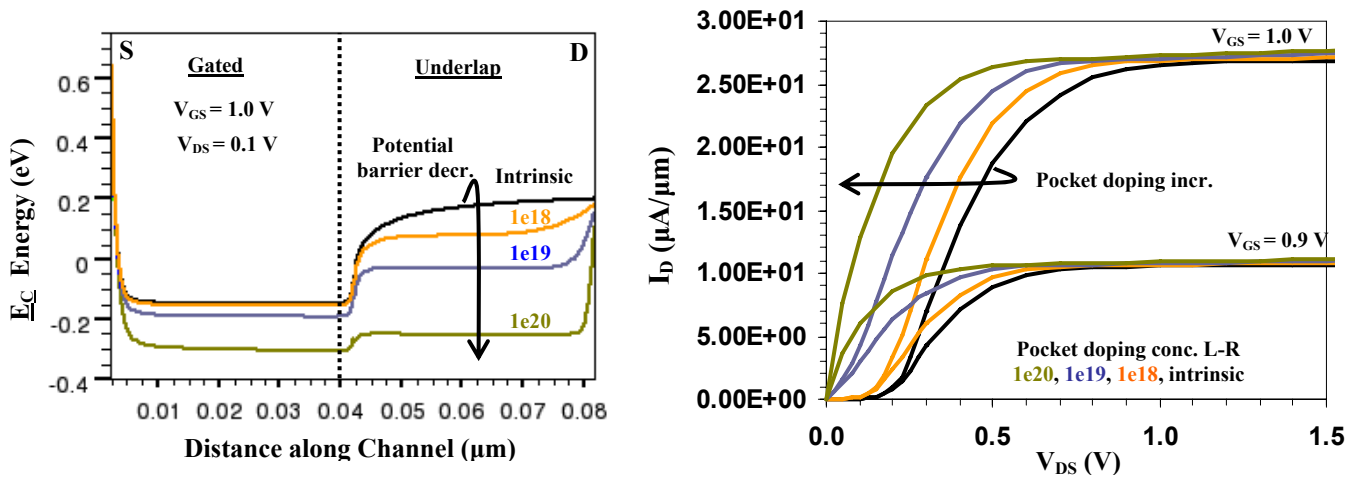
Figure 5.12: a) Conduction band edge/ potential barrier lowering for increased N$^+$ pocket doping
b) I_D-V_{DS} plot showing a reduction in the non-conducting region at low V_{DS}'s due to the potential barrier lowering caused by the increasing N+ pocket doping.

It should be noted that the use of these drain side pocket implants at high enough doping levels essentially results in the creation of the STS-FET (with its drain side Ohmic contact) discussed in Chapter 4. The I_D-V_{GS} comparison between the STS-FET (dotted line, Figure 5.14) and the (10^{20} cm^{-3}) doped AsymG-FET clearly shows that this is in fact the case with the only variation (curve shift) being due to the difference in gate workfunctions.
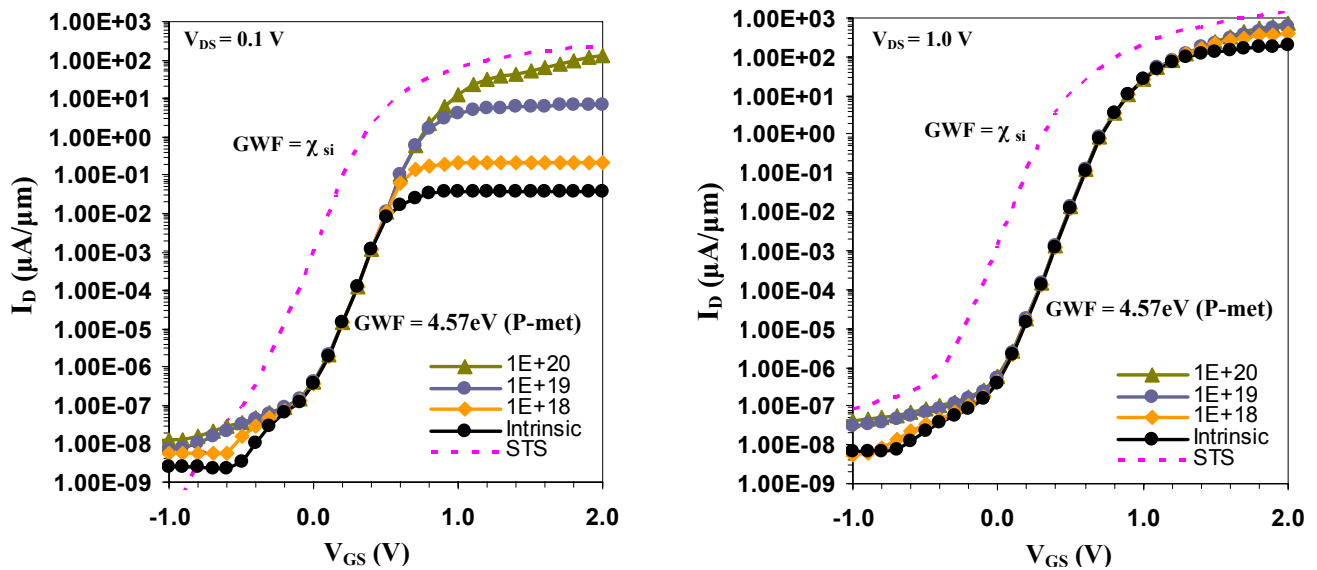

Figure 5.13: I_D-V_{GS} characteristics at $V_{DS} = 0.1V$ (a) and $V_{DS} = 1.0V$ (b) for different pocket doping concentrations showing drastic I_{ON} improvements at low V_{DS} (a) .

Since doping is once again introduced the benefits gained (i.e low thermal budget) using the previously implantless AsymG SB-FET compared to the STS-FET are lost once again.

The STS-FET due to the abruptness and the highly doped nature of its drain side pocket, was mentioned to possibly suffer off current limitations due to GIDL caused by straight band to band tunneling. This same problem will be faced when using the highly doped underlap regions proposed here. The band representations of Figure 5.15 in fact clearly visualize this, showing that at negative gate bias (essentially creating a P+ layer under the gated region) for high pocket (10^{19} and 10^{20} cm^{-3}) doping levels the B2B tunneling distance is reduced to such an extend that tunneling leakage is unavoidable and will start to influence the device's off current.

Due to time constraints band to band tunneling simulations necessary to predict the exact influence of this GIDL could not be performed. Some preliminary simulations however were performed of which the results are shown in appendix B.3. These results show the expected increase in I_{OFF} with increasing doping levels which matched the behavior seen by Krishnamohan *et al.* in [58] and the measurement results of Jhaveri *et al.* in [22].
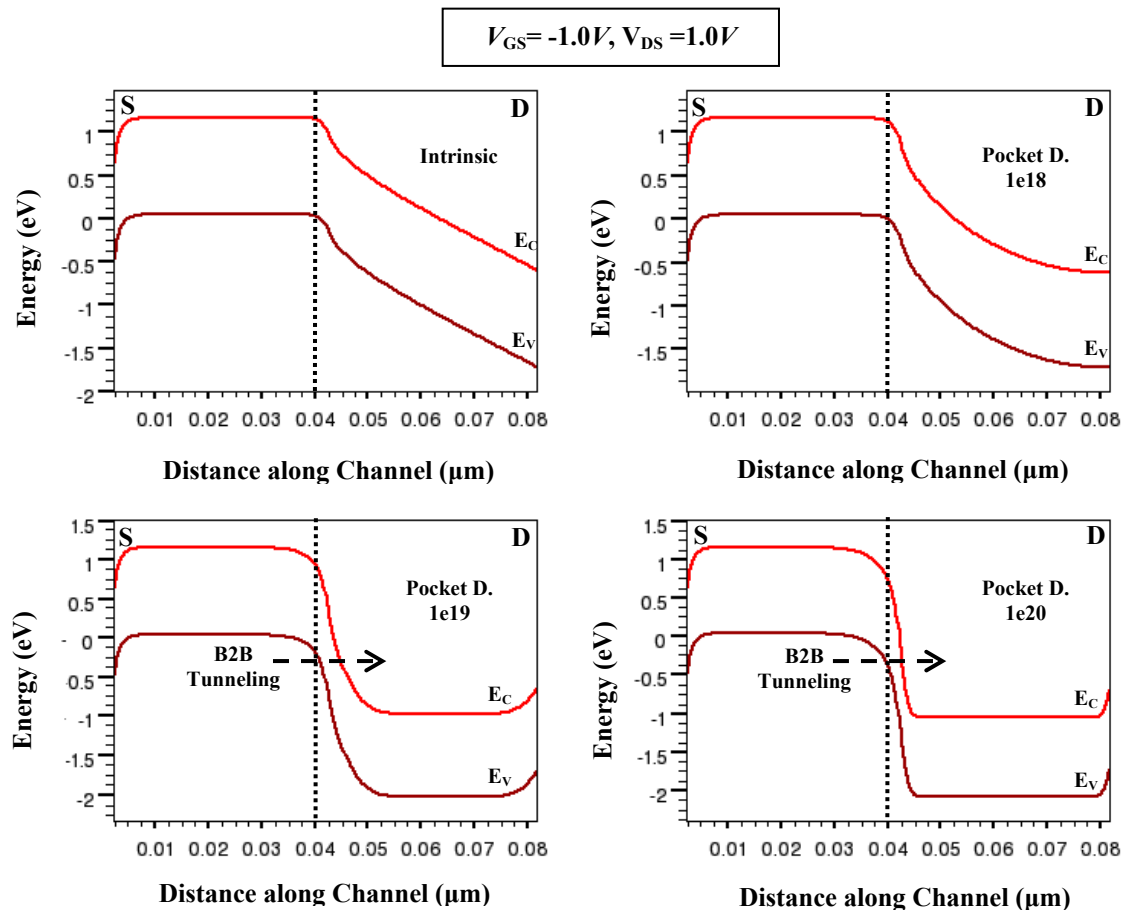

Figure 5.14: Band diagrams showing increased possibility of band to band tunneling at low/ negative V_{GS}'s due to increased drain side pocket doping implants

5.10.   *The AsymG SB-FET Scalability*

It should be clear by now that the reverse tunneling leakage suppression using the proposed drain side underlap technique is strongly related to the underlap distance which will understandably start posing a problem towards increasingly aggressive channel lengths. A rough estimate can be made with respect to the scaling limit if one looks at the effectiveness of ambipolar tunneling suppression for different gate underlap lengths. Judging by the observed leakage suppression seen in Figure 5.2 it can be concluded that the minimum underlap which still reasonably suppresses the tunneling leakage is ~10 *nm*. This same 10 *nm* is also at the lower limit of source side gate overlap needed to create a gate induced electric field which can effectively modulate the source tunneling current in the subthreshold regime. This therefore makes the minimum theoretical channel length roughly 20 *nm*.
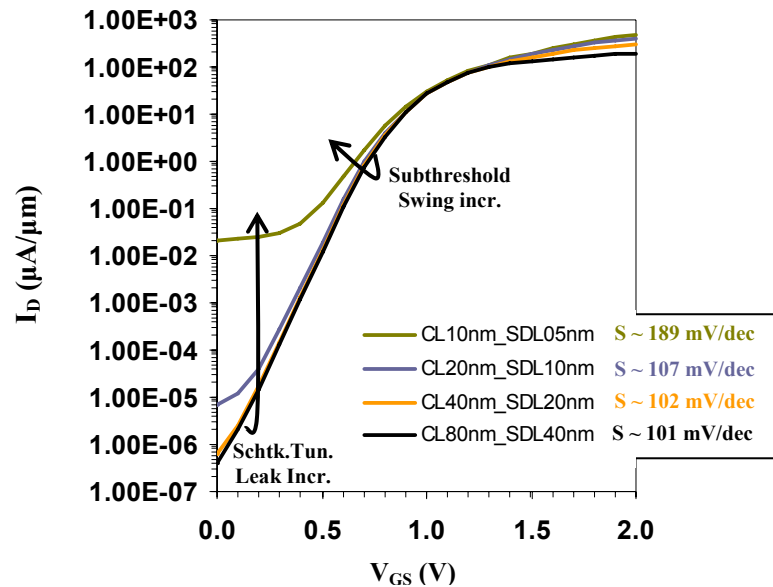

Figure 5.15: I_D-V_{GS} **characteristics for channel length (CL) downscaling of the AsymG-FET with equal source overlap and drain underlap lengths (SDL).**

Figure 5.16 shows that there is indeed a severe off current increase (caused by reverse Schottky tunneling) when going below the predicted 20 *nm* channel length with 10 *nm* drain underlap limit. While the drastic subthreshold slope increase indicates that the gate is also less effective in modulating the (source side) Schottky tunneling barrier when dealing with (source) overlap lengths shorter than 10 *nm*. Figure 5.17 also shows that at the aggressive channel lengths of 20 nm (and lower) device saturation behavior is affected by channel length modulation. In saturation regime, due to the narrow underlap, the drain starts to influence the potential distribution below the 10 *nm* gated region.
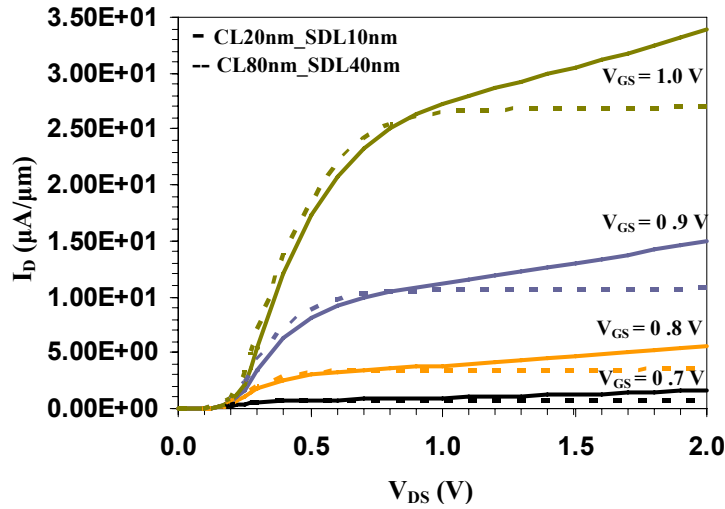
Figure 5.16: I_D-V_{DS} characteristic comparison between the 20nm (solid line) and the 80nm channel device (dotted line, also Fig 5.11). With the 20nm device's saturation current clearly influenced by SCE's.

Note that although it might seem from the non-linear (quadratic) I_{Dsat} step increases[20] (Figure 5.10 andFigure 5.17) that we are dealing with a long channel device without velocity saturation, this is not the case. The quadratic increase is due to the fact that I_{Dsat} at "low" V_{GS} is limited by the source tunneling width. It is the modulation of this source tunneling barrier with increasing V_{GS} that results in the "long-channel" like quadratic I_{Dsat} step increase. Figure 5.18 shows that when the source tunneling barrier is narrow enough (high V_{GS}) to not limit I_{Dsat}, indeed a more linear like I_{Dsat} step increase associated with short-channel (velocity saturated) FETs is obtained.
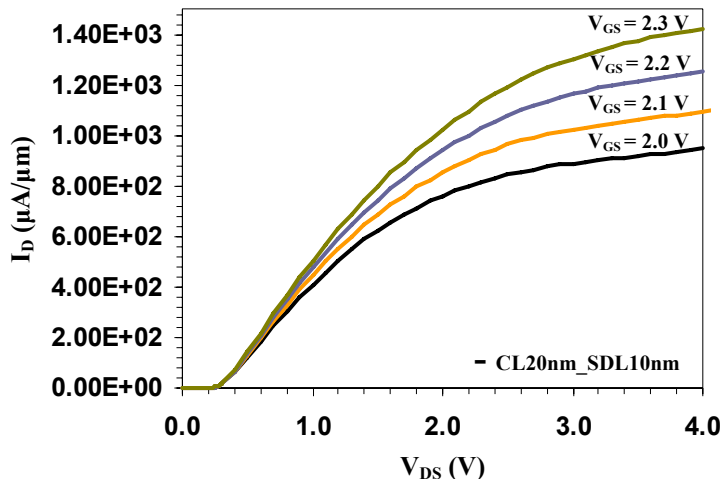

Figure 5.17: I_D-V_{DS} characteristic for high gate potentials showing the more linear like I_{Dsat} step increases associated with short-channel (velocity saturated) FETs.

---

[20] In conventional MOSFETs it is known that I_{Dsat} for short-channel FETs is proportional to $(V_{GS}-V_{TH})$ instead of the $(V_{GS}-V_{TH})^2$ known from the square law model [11]
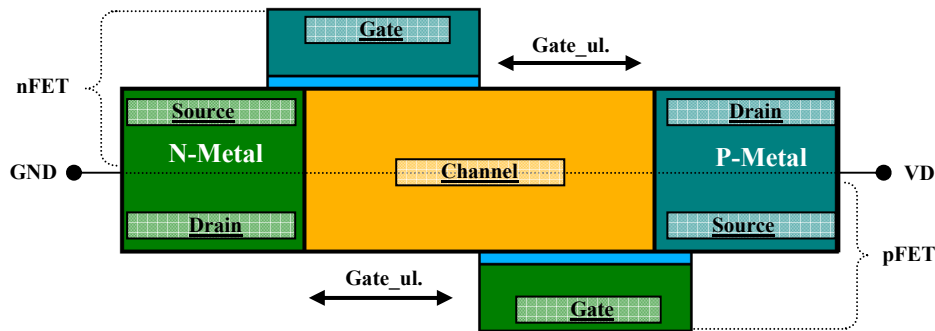
5.11. *The dual gate AsymG-FET*

Figure 5.18: Schematic cross-section of an asymmetric dual gate N / P-Fet selectable structure. This embodiment could be formed in a nanoribbon (NR), nanowire (NW) or nanotube (NT).

Based on the non-implanted AsymG SB-FET a novel asymmetric dual gate FET (Figure 5.19) can be realized whereby depending on the applied gate potential either n- or pFET behavior is seen. Resulting in what can be interpreted as a programmable FET.

Although the device concept is straight forward, realization however might prove to be difficult as gate workfunctions, the applied gate and drain potentials etc, all will need to be chosen such that one device in off-state does not impede the on-state operation of the other.

For instance, when using the device as an nFET, turning off the pFET will necessitate the application of a constant positive voltage on the P-Gate. This positive voltage could however adversely influence the nFET on-state electron flow since the P-Gate induced band bending (for thin channel thicknesses) will form a barrier to electron conduction in the nFET active area (opposite to the P-Gate).

This is a simple example of one of the problems one might face when creating this dual gate device. Extensive problem analysis and all-round device characterization however is not performed and might be a point of interest for future research.

6. Conclusions

Extensive simulations were performed on both the existing STS-FET and the newly proposed AsymG SB-FET. The asymmetric nature of these devices was shown to improve the device behavior (Table 6.1) compared to the more conventional symmetric Schottky FETs.

Furthermore the AsymG SB-FET was shown to keep most of the improvements seen with the STS-FET while reducing the device's technological complexity and maintaining a low thermal budget. The latter being possible due to its undoped fully metallic design.

Finally, due to the subthreshold characteristic of these devices being (more) a function of the source tunneling properties rather than the drain/channel potential (strong SCE immunity), the device designs were shown to be highly scalable without the need for conventional techniques such as channel extensions and halo or pocket implants.

	SC		Metal	
	Symmetric		Asymmetric	
	MOSFET	**SB-FET**	**STS-FET**	**AsymG**
DIBL	x	-	-	-
GIDL	x	-	x	-
Ambipolar leakage	-	x	-	-
Bipolar interaction	x	-	-	-
High thermal budget	x	-	x	-
Linear I_D-V_{DS}	-	x	-	-/x
Break $60mV$/dec S	x	x	x	x

Table 6.1: Comparison between a non-optimized MOSFET and the SB-FETs discussed in this work.

6.1. *Future work*

- Realize the actual devices and perform measurements to get a better understanding of the technological difficulties faced with fabrication. The latter is especially the case for the AsymG SB-FET as, contrary to the STS-FET, such a device has yet to be made. Also having (more) measurement data will help in better understanding, confirming and fine tuning simulation results and the models used to obtain them.

- Find the origin of the 60mV/dec Schottky tunneling subthreshold limit and derive an analytical model for both STS and the AsymG SB-FETs.

- Although a wide range of AC simulations were performed (especially with respect to the STSFET) of which some of the results are listed in appendix A.4 a more in-depth AC analysis of both the STS-FET and AsymG SB-FET should be performed. This will help in better understanding aspects such as the high-cutoff frequencies associated with the conventional SB-FETs [60] and how this applies to the more novel STS and AsymG SB-FETs designs

- Incorporate gate underlap as seen in the AsmyG SB-FET in more novel devices. An example would be the creation of a undoped fully metallic (S/D and Gate) FinFET, which would solve the technological difficulties faced with these devices and controlled dopant implantation and activation.

- Work on alternative AsymG SB-FET structures such as one containing a dual *EOT* across the complete gated channel region in which the *EOT* at the drain is larger than at the source, or by employing a gated drain-overlap across the gate-underlap region.

6.2. *Acknowledgements*

Appendix A: Thermionic emission theory (quantitative analysis)

The *cross barrier* current density from semiconductor to metal (J_{s-m}) is limited by the concentration of carriers with kinetic energy (KE) sufficient to surpass the barrier in the direction (x) of transport. Therefore electrons can cross the junction if:

(Eq A.1 a)
$$KE_x = \frac{1}{2} m_n^* v_x^2 \geq q(V_{bi} - V_A)$$

(Eq A.1 b)
$$|v_x| \geq v_{min} \equiv \sqrt{\frac{2q}{m_n^*}(V_{bi} - V_A)}$$

- m_n: effective electron mass
- v_x: electron velocity in direction x

The current density for electrons at a given velocity is:

(Eq A.2)
$$J_{S \to M, v_x} = -q v_x n(v_x)$$

- $n(v_x)$: number of electrons with velocity component in direction x

Therefore the total current density across the barrier is:

(Eq A.3)
$$J_{S \to M, v_x} = -q \int_{-\infty}^{-v_{min}} v_x n(v_x) dv_x$$

Resolving $n(v_x)$ and solving the above integral results in [11]:

(Eq A.4)
$$J_{S \to M} = \left[\frac{4\pi q m_n k^2}{h^3}\right] T^2 \exp(-\frac{q\Phi_B}{KT}) \exp(\frac{qV_A}{K})$$

$$J_{S \to M} = A^* T^2 \exp(-\frac{q\Phi_B}{KT}) \exp(\frac{qV_A}{KT})$$

- A^*: effective Richardson constant

As was previously mentioned the carrier flow from M→S doesn't change under bias. Thus as there is no net current flow at equilibrium $J_{S \to M}$ @ $V_A = 0$ V *should* be exactly opposite to the constant $J_{M \to S}$ component:

(Eq A.5)
$$J_{M \to S} = -A^* T^2 \exp(-\frac{q\Phi_B}{KT})$$
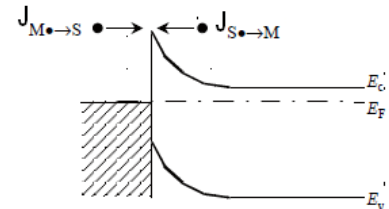
Knowing both $J_{S \rightarrow M}$ and $J_{M \rightarrow S}$ the total diode current density equation is:

(Eq A.6)
$$J_n = J_{TE}\left[\exp(\frac{qV_A}{kT}) - 1\right] \ ,$$

- J_{TE} : barrierheight dependent thermionic emission component

with

(Eq A.7)
$$J_{TE} = \left[A^*T^2 \exp(-\frac{q\Phi_B}{kT})\right]$$

Appendix B – Additional simulation results

B.1 T_{OX} influence on AsymG SB-FET subthreshold slope
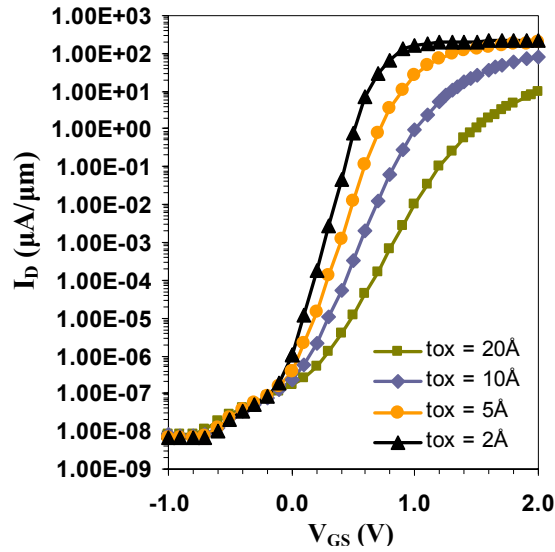
Figure B.1: (AsymG SB-FET) I_D-V_{GS} **characteristics showing subthreshold swing reduction for decreasing gate oxide thicknesses**

B.2 Channel potential barrier lowering for the AsymG-FET
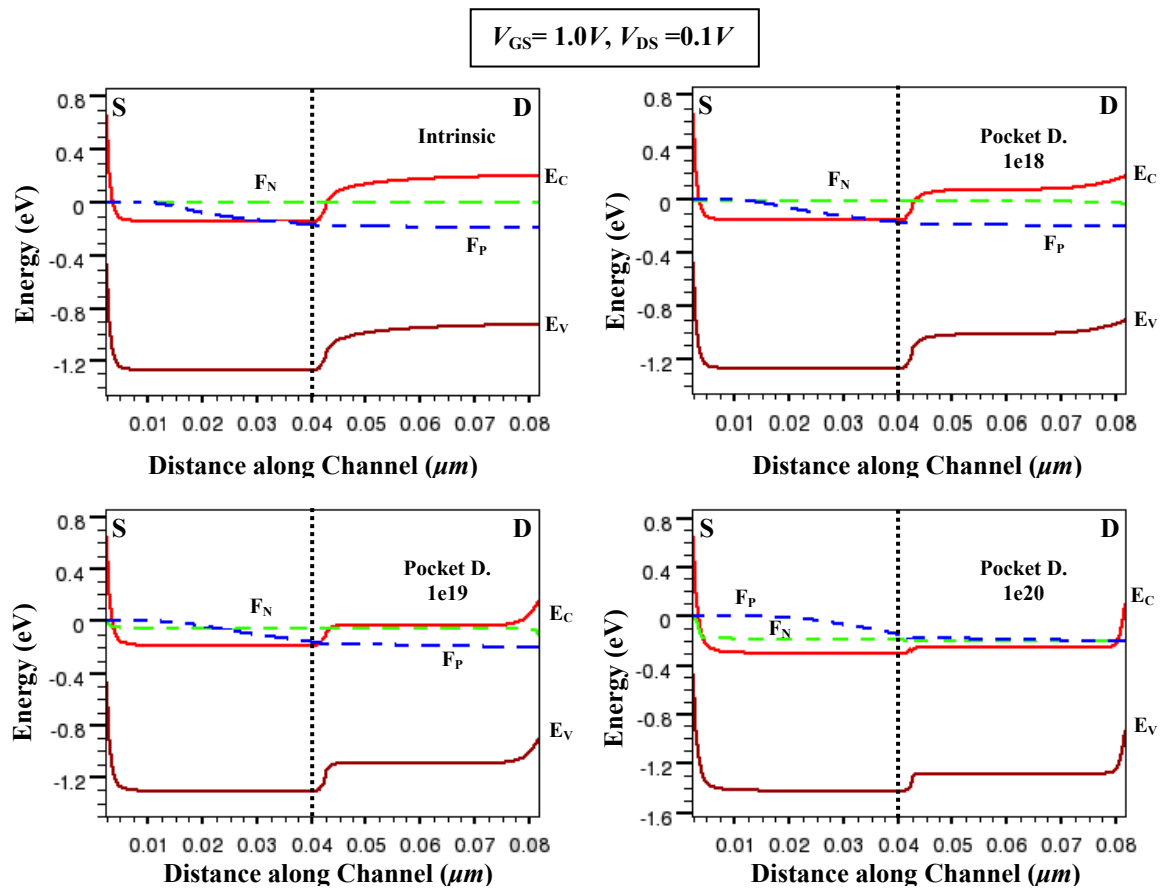
Figure B.2: Full band diagrams clearly showing the potential barrier reduction with increasing pocket doping concentration.

B.3 Band to Band Tunneling calibration and implementation
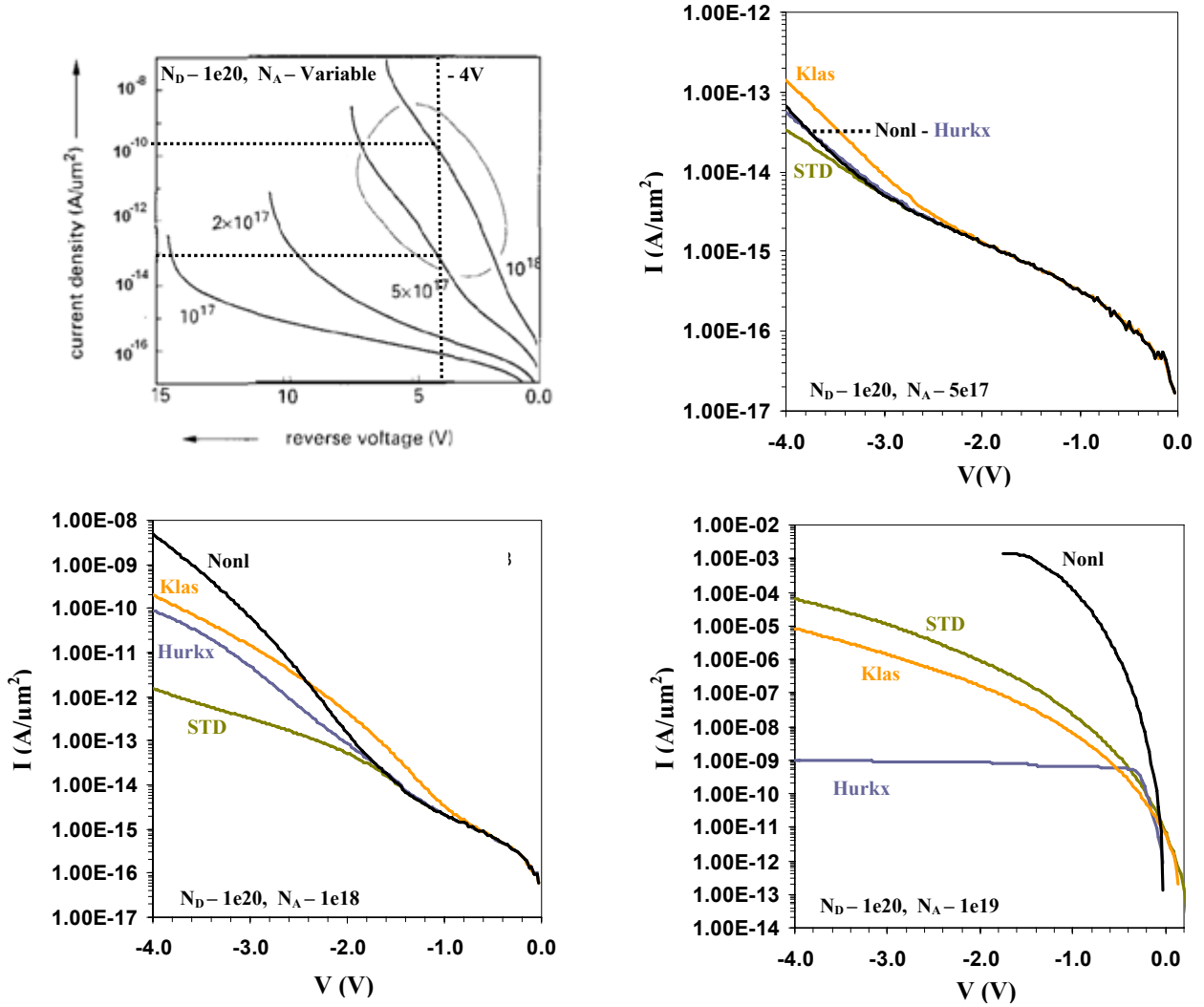
Figure B.3: Comparative analysis of Esaki diode measurements done by Hurx *et al.* and results obtained using 4 different ATLAS BBT models

To get an indication of the limitations faced using the different Atlas band to band tunneling models, the tunneling diodes (with $N_D = 10^{20}$ cm^{-3} and N_A = variable) measured by Hurkx *et al.* in their 1992 paper [62] were simulated (Figure B.3). Comparing the *I-V* characteristics it was seen that for $N_A = 5 \cdot 10^{17}$ and 10^{18} cm^{-3} (Figure B.3 b and c) the simulation results (using different Atlas models[21]) were comparable to those measured (Figure B.3 a). At higher doping levels however the different Atlas models started showing peculiar behavior resulting in large *I-V* discrepancy between one another (Figure B.3d, with $N_A = 10^{19}$ cm^{-3}). The "Hurkx" model (at high reverse voltages) for instance was limited to a constant tunneling current value, both the "Klaassen" (Klas) and "standard" (STD) BBT models showed a rather large current flowing at what should have been equilibrium conditions (*V*= 0 *V*), while the nonlocal tunneling model output showed strong meshing based dependencies, used e.g. by Boucart and Ionescu [63]. Further analysis and calibration could likely produce better results (esp. with respect to the nonlocal tunneling model)

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[21] For more information about the differences and the precise nature of these models refer to the Atlas user manual [39].

but due to time constraints this was not possible. Because of these time constraints and since at lower N_A values (Figure B.3 (b) and (c)) there was a good correlation between Klaassen's (Klas) model and the results obtained by Hurkx *et al.*, it was this BBT model that was chosen to be implemented for BBT modeling of both the STS-FET (Chapter 4) and the doped AsymG SB-FET (Chapter 5.9). It should be noted that the results obtained using this model (Figure B.4 and Figure B.5) simply serve as an *indication* of the effect band to band tunneling can have on the off current of these devices and that additive calibrations, simulations and if possible measurements will be necessary to give a definite answer as to its *exact* influence.

Using in-house quantum tunneling simulation tools Krishnamohan *et al.* in their 2008 paper [58] also studied the tunneling leakage influence of drain side pockets similar to those of the AsymG SB-FETs discussed in Chapter 5.9. The off current leakage levels they obtained and the overall current behavior (although based on a somewhat different device) showed a large amount of similarities to those obtained for the AsymG SB-FET (Figure B.4), giving some merit to the viability of using Klaassens model as the BBT model.
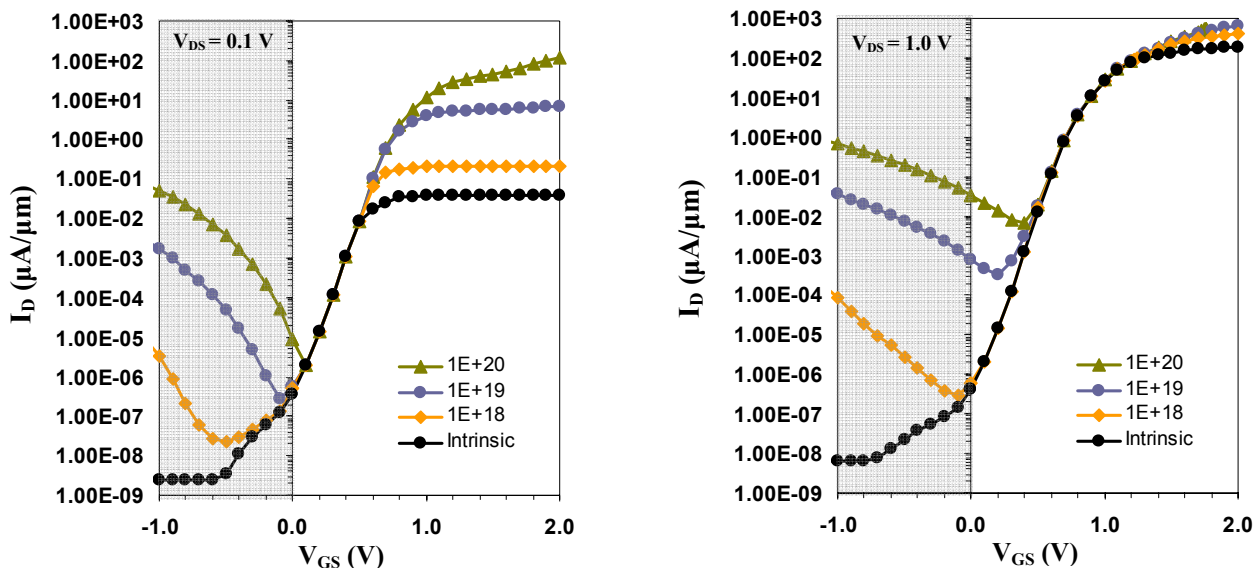
Figure B.4: Doped AsymG-FET I_D-V_{GS} characteristics (similar to those seen in Figure 5.14), with Klaassen's BBT model enabled.

The results obtained for both the doped AsymG SB-FET (Figure B.4) and the STS-FET (Figure B.5) show that having highly doped (abrupt) drain side pockets indeed (Chapter 5.9, Figure 5.15) results in band to band tunneling leakage which can adversely influence I_{OFF}. It can therefore be concluded that this "pocket induced" tunneling leakage, if not dealt with properly (i.e. use of pocket implants with less abrupt Gaussian junctions etc), can have similarly bad effects on I_{OFF} as the reverse Schottky tunneling leakage it was initially meant to suppress.
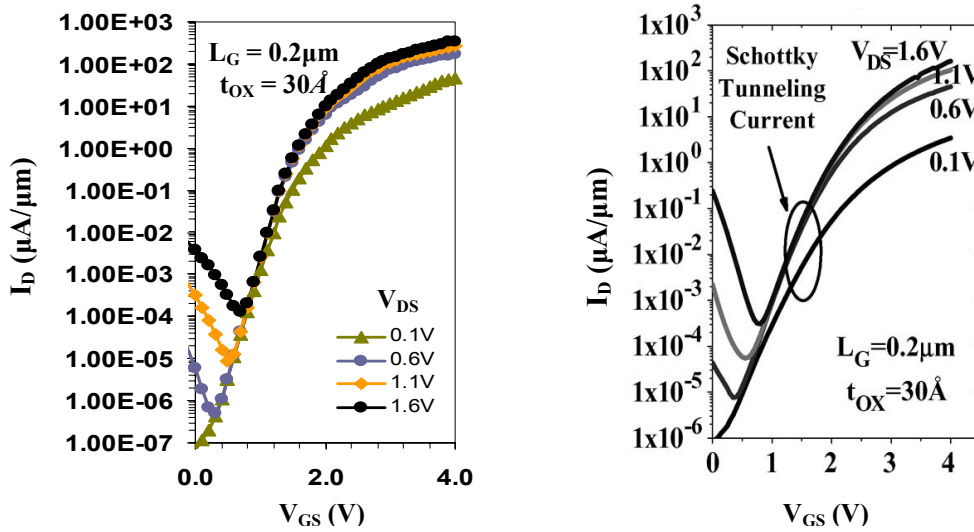
Figure B.5: a) Simulation results of Jhaveri's STS-FET with Klaassen's band to band tunneling enabled b) Jhaveri's STS-nFET measurement results [22]

Finally when comparing the STS-nFET simulation results with measurements done by Jhaveri (Figure B.5) similar off current behavior is observed. The ambipolar behavior observed in Figure B.5(b) was initially explained by Jhaveri as a reverse Schottky tunneling effect caused by insufficient dopant concentration of the drain side pocket. As seen from the above comparison this could actually also be due to pocket induced band to band tunneling. Claims with respect to the exact cause (reverse Schottky or B2B GIDL) of the observed tunneling leakage can however not be made either way, since for that to be possible better tunneling model calibration and more device measurements are necessary.

B.4 STS-FET AC-Simulations

In this section some of the AC simulations performed with respect to the STS-FET will simply be listed. Due to time constraints (a more in-depth) analysis with respect to these results is left for a future work.

Simulation parameters and values:

- *Operating frequency (f_{oper})* = 1GHz
- *Gate lengths (L_G)* = 130,90 and 50nm
- *Source barrierheights (Φ_B)* = 0.25, 0.45 and 0.65eV
- *Transconductance (g_m)* = g_{dg} (Atlas AC output) = $\Delta I_d / \Delta V_g$
- *Output Resistance (R_{out})* = $1/ g_{dd}$ (Atlas AC output) = $\Delta V_d / \Delta I_d$
- *Intrinsic Gain* = $g_m * R_{out}$
- *Cutoff Frequency (f_t)* = $\dfrac{g_m}{2\pi C_G}$

* Simulated SOI devices are not optimized (no halo implants or S/D extensions) in the interest of "1on1" comparison

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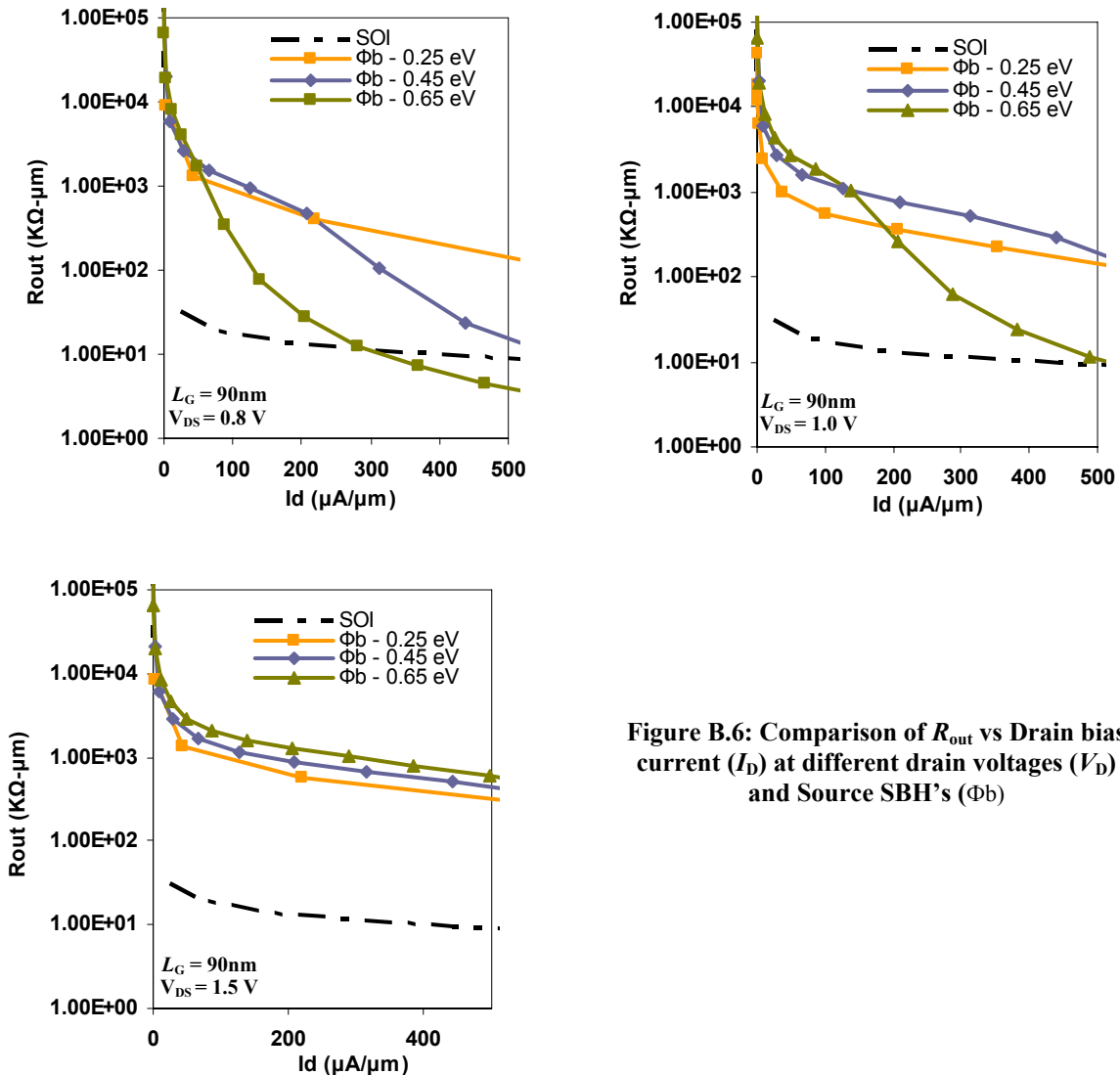
Figure B.6: Comparison of R_{out} vs Drain bias current (I_D) at different drain voltages (V_D) and Source SBH's (Φb)

65
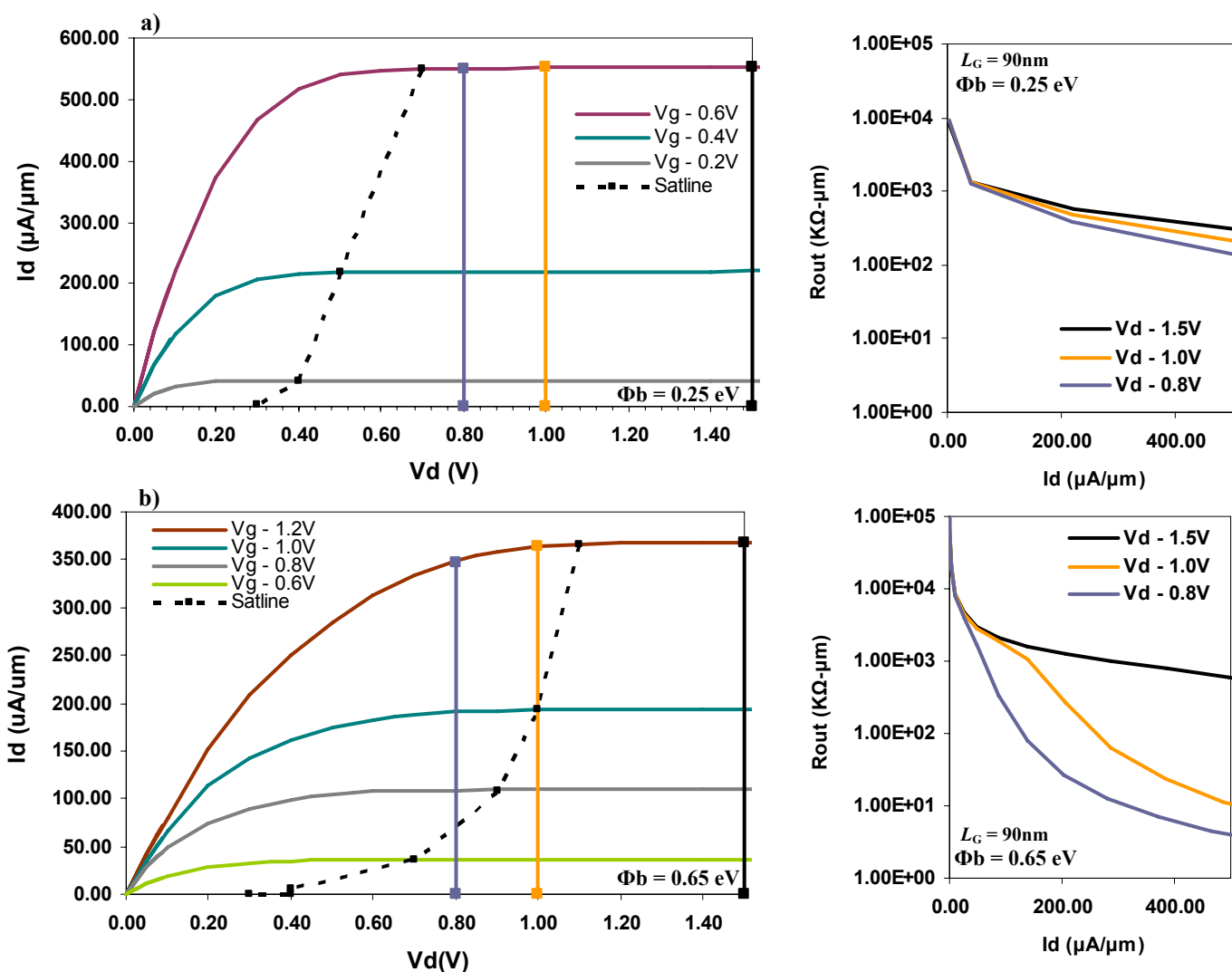
Figure B.8: Plots showing the origin of the R_{out} drop seen at low V_{DS}'s and high source SBH's. The I_D-V_{DS} plots show that in these situations the pronounced R_{out} drop is due to the device leaving the saturation regime (see V_{DS}= 1V in b).
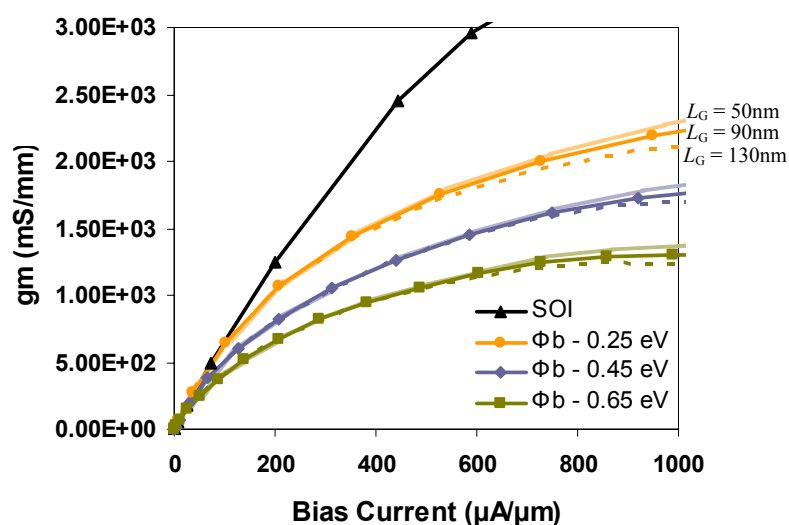
Figure B.7: Transconductance (g_m) as a function of bias current for different gate lengths (L_G) and Source SBH's (Φb)
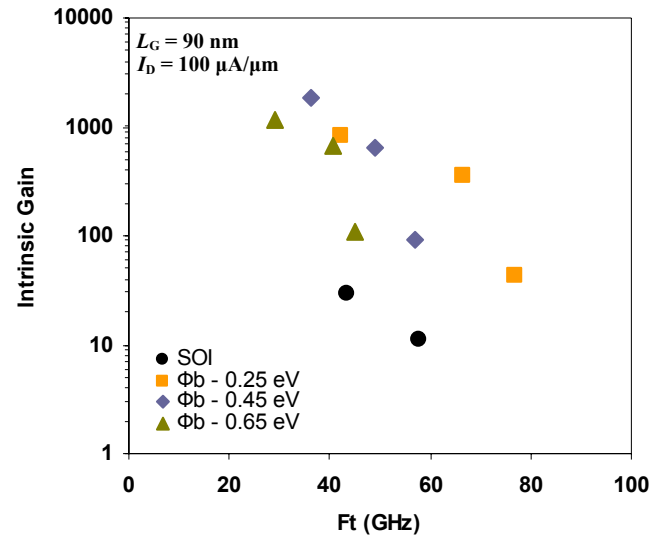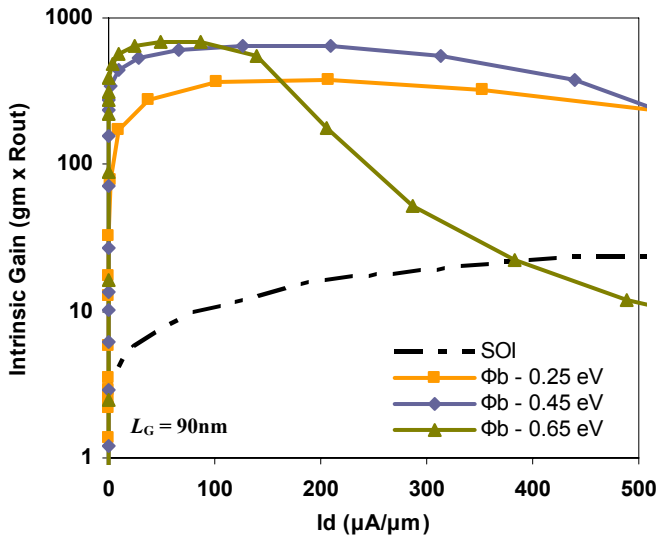
Figure B.9: a) Intrinsic Gain at different bias currents for STS-FETs w. different Source SBH's and a conventional SOI FET

b) F_T – Intrinsic Gain performance for the STS-FETs and SOI -FET at a biasing current of 100 μA/μm

It's clear from the R_{out} plots (Figure B.6) that the STS-FETs in general have a much larger output resistance than that of the non-optimized conventional SOI-FET, the cause of this being the previously mentioned STS-FET's strong immunity to SCE's. This leads to the higher intrinsic gains seen in Figure B.9(a) and the better Intrinsic Gain vs Cutoff Frequency (F_T) performance seen in Figure B.9(b).

One particular analog advantage corresponding to these high intrinsic gains is that non- linearities (in R_{out}) will play less of a role since gain can be sacrificed through the introduction of a parallel load resistance (assuming $R_{out} \gg R_L$) suppressing the influence of non-linearities in the device's R_{out}.

Appendix C: Atlas sample files

This appendix will list some code samples used to simulate the Schottky devices discussed in this work. No details will be given as to the precise meaning and function of the implemented models and calculation methods used, for those details the reader is referred to the Silvaco Atlas user manual [39].

C.1 AsymG nFET I_D-V_{GS} / I_D-V_{DS} code sample file

--Code Start--

```
## Start Atlas ##

GO ATLAS

## Start loop statement and assign variables to be loaded in code for each subsequent step ##

LOOP steps=1 print

## Variable assignment (current example shows a single step program thus a single value is assign for
each variable); "devname and exname" are variables defined to distinguish the saved (.str and .log)
output files ; "name" is a variable that  is used to load the separate device structure and mesh made in
devedit or an equivalent tool ##

ASSIGN name=devname   c1="AsymG_nFET"
ASSIGN name=exname     c1="SD_BH6572ev_40UL _TOX5A "
ASSIGN name=name          c1="AsymG_nFET _40UL_TOX5A"

## Variables defining Si affinity and metal workfunctions ##

ASSIGN name=si_affinity      n.value=(4.17)
ASSIGN name=s_metal_wf    n.value=(4.82)
ASSIGN name=d_metal_wf    n.value=(4.57)

## Loading the device structure (definened with variable "name" ) saved in the directory the code is
run from ##

MESH infile= ${name}.str

----------------------------------------------------------------------------------------------------

## Adjust material parameters ##

MATERIAL material=silicon affinity=${si_affinity} eg300=1.12 NC300=3.23e19
              NV300=2.69e19 TAUP0=2.5e-5 TAUN0=2.5e-5 NSRHN=1.33e17
              NSRHP=3.4e15  augp=1.83e-31 augn=2.78e-31

## Defining  the simulation models used; "ust" being the important Universial Schottky Tunneling
model (see chapter 2.4) ##

MODELS ust cvt kla bgn.klassen fermi temperature=300 print
```

Defining the (metal) schottky contacts

```
CONTACT   name=gate    workf=${d_metal_wf}
CONTACT   name=source  workf=${s_metal_wf}  surf.rec barrier
CONTACT   name=drain   workf=${d_metal_wf}  surf.rec barrier
```

Variables to be included in the .str output files

```
OUTPUT E.field Recombination con.band val.band impact.i Schottky flowlines
        e.mobility e.velocity charge j.drift j.total j.diffusion
```

Start calculations process

```
METHOD newton carriers=0
```

Initial solution (all terminal voltages set to zero) calculation and .str output

```
SOLVE   init
SAVE    outfile=Init_${devname}_${exname}.str
```

Simultaneous calculations of charge carriers and potential (Newton-Raphson)

```
METHOD NEWTON carriers=2 AUTONR
```

Ramp down VGS to negative values to avoid initial tunneling calc and convergency errors

```
SOLVE NAME=gate vgate=0 vfinal=-2 vstep=-0.1
```

Slow VD ramp up with outputs saved for subsequent ID-VGS simulations

```
SOLVE vdrain = 0.001
SOLVE vdrain = 0.01
SOLVE vdrain = 0.05
SOLVE vdrain = 0.1 outf=solve_${devname}_${exname}_vdrain01
SOLVE vdrain = 0.25
SOLVE vdrain = 0.5
SOLVE vdrain = 1   outf=solve_${devname}_${exname}_vdrain1
```

Solution loop (DC and AC) – ID-VGS / -2V to 2V @ VD = 0.1

```
LOAD INFILE = solve_${devname}_${exname}_vdrain01
LOG   OUTFILE = Log_${devname}_${exname}_after_Vd01.log

SAVE  outfile=Str_${devname}_${exname}_after_Vd01_Vgn2.str

SOLVE name=gate vgate=-2 vfinal=0 vstep=0.1 AC freq=1e9
SAVE  outfile=Str_${devname}_${exname}_after_Vd01_Vg0.str
```

Binary output file creation at each step to be used for the ID-VDS simulations

SOLVE name=gate vgate=0 vfinal=2 vstep=0.1 AC freq=1e9
        outf=VD01_${exname}1

SAVE outfile=Str_${devname}_${exname}_after_Vd01_Vg2.str

End outfile logging

LOG off

Solution loop (DC and AC) – ID-VGS / -2V to 2V @ VD = 1

LOAD INFILE = solve_${devname}_${exname}_vdrain1
LOG OUTFILE = Log_${devname}_${exname}_after_Vd1.log

SAVE outfile=Str_${devname}_${exname}_after_Vd1_Vgn2.str

SOLVE name=gate vgate=-2 vfinal=0 vstep=0.1 AC freq=1e9
SAVE outfile=Str_${devname}_${exname}_after_Vd1_Vg0.str

SOLVE name=gate vgate=0 vfinal=1.2 vstep=0.1 AC freq=1e9
SAVE outfile=Str_${devname}_${exname}_after_Vd1_Vg12.str

SOLVE name=gate vgate=1.3 vfinal=1.6 vstep=0.1 AC freq=1e9
SAVE outfile=Str_${devname}_${exname}_after_Vd1_Vg16.str

SOLVE name=gate vgate=1.7 vfinal=2 vstep=0.1 AC freq=1e9
SAVE outfile=Str_${devname}_${exname}_after_Vd1_Vg2.str

End outfile logging

LOG off

End loop

l.end

End simulation

quit

---------------------------- Place following code section in different File -------------------------

Determining I_D-V_{DS}, with "infile" a variable pointing to the I_D-V_{GS} outfile above

LOAD   infile= ${infile}
SOLVE name=drain vdrain=0.1 vfinal=0 vstep=-0.1
log outfile=Log_IDVD_${exname}.log
solve name=drain vdrain=0 vfinal=0.3 vstep=0.025
solve name=drain vdrain=0.3 vfinal=2 vstep=0.1

End simulation
quit

C.2 Device meshing and creation in Atlas

Most structures used in this work were created and meshed using Devedit and simply imported into Atlas using the "MESH" statement as seen in the code sample above. However, in some cases using Atlas itself to create and mesh the device is easier or sometimes even necessary (i.e. when using certain non-local band to band tunneling models [39]).

Below is an Atlas code sample of this process, with a cross-section of the to be realized AsmyG SB-FET given in Figure C.1
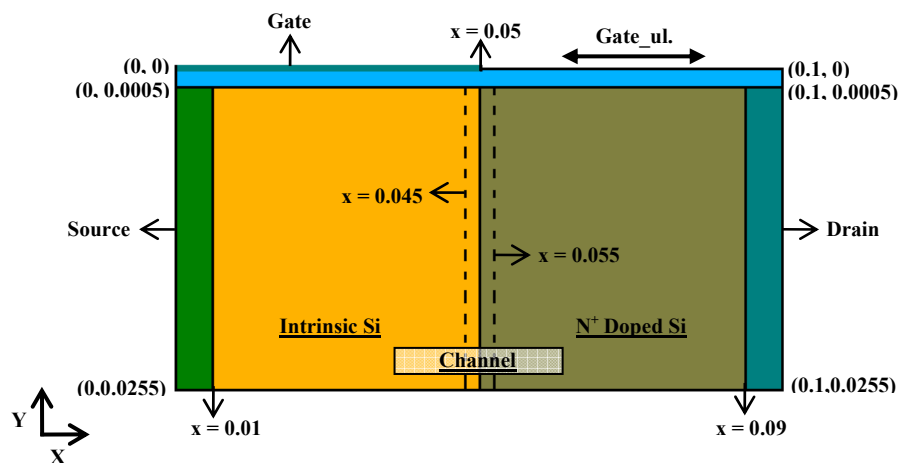
Figure C.1: Cross-section (not to scale) of the AsymG SB-FET created in the code sample given below with distances in μm and mesh not shown

---Code Start--

Start Atlas

GO ATLAS

MESH space.mult=1.0

Horizontal mesh divination

```
X.MESH loc=0.00          spac=0.01
X.MESH loc=0.01          spac=0.001
X.MESH loc=0.09          spac=0.001
X.MESH loc=0.1           spac=0.01
```

Constant mesh in vertical direction across 5 Angstrom oxide en 25 nm Channel

```
Y.MESH loc=0             spac=0.0001
Y.MESH loc=0.0005        spac=0.0001
Y.MESH loc=0.0255        spac=0.0001
```

Quantum tunneling mesh for nonlocal BBT between gated and underlapped region (Fig 5.15)

```
QTX.MESH loc=0.045       spac=0.0005
QTX.MESH loc=0.055       spac=0.0005
QTY.MESH loc=0.0005      spac=0.001
QTY.MESH loc=0.0255      spac=0.001
```

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Define material positions

```
REGION  num=1  material=silicon
REGION  num=2  material=oxide  x.min=0     x.max=0.1   y.min=0        y.max=0.0005
REGION  num=3  material=NiSix  x.min=0     x.max=0.01  y.min=0.0005  y.max=0.0255
REGION  num=4  material=NiSix  x.min=0.09  x.max=0.1   y.min=0.0005  y.max=0.0255
```

Define electrodes

```
ELECTR  name=gate    x.min=0     x.max=0.005  y.min=0        y.max=0
ELECTR  name=source  x.min=0     x.max=0.01   y.min=0.0005  y.max=0.0255
ELECTR  name=drain   x.min=0.09  x.max=0.1    y.min=0.0005  y.max=0.0255
```

Define doping profiles
Source-side implant here none / intrinsic

```
#DOPING n.type conc=0e0 uniform  x.min=0.01 x.max=0.05
```

Drain-side implant

```
doping n.type conc=1e20 uniform  x.min=0.05 x.max=0.09
```


------------------------------ Follow up with code as seen in **C.1** -------------------------------

Define electrodes

List of Symbols

Symbol:	Description:	Unit:
A^*	Richardson's constant	$Acm^{-2}K^{-2}$
C_{dm}	Bulk depletion capacitance	F
C_{ox}	Oxide capacitance	F
E_0	Vacuum/ free electron energy level	eV
E_C	Conduction Band Energy	eV
E_F	Fermi level	eV
E_{FM}	Metal Fermi level	eV
E_{FS}	Semiconductor Fermi level	eV
E_I	Intrinsic Fermi level	eV
E_V	Valance band energy	eV
F_N	Electron quasi-Fermi level	eV
F_P	Hole quasi-Fermi level	eV
G_ul	Gate underlap	nm
$J_{(T)FE}$	Thermionic field emission current density	Acm^{-2}
J_{FE}	Field emission current density	Acm^{-2}
J_{TE}	Thermionic emission current density	Acm^{-2}
k	Boltzmann's constant	eVK^{-1}
m_0	Free electron mass	kg
m_n	Electron effective mass	kg
m_p	Hole effective mass	kg
N_A	Acceptor doping concentration	cm^{-3}
N_c	Conduction band density of states	cm^{-3}
N_D	Donor doping concentration	cm^{-3}
N_v	Valance band density of states	cm^{-3}
q	Elementary charge	C
R_c	Contact Resistance	$\Omega\text{-}cm2$
R_{out}	Device Output resistance	$K\Omega\text{-}cm$
T	Temperature	K
T_{OX}	Oxide thickness	nm
T_{Si}	Substrate tickness	nm
V_{bi}	built-in potential	V
V_{DD}	Supply voltage	V
V_{FB}	Flat band voltage	V
V_T	threshold Voltage	V
W_{dm}	Max gate depletion width	nm
W_{tun}	Tunneling width	nm
ε_{ox}	Permittivity of (silicon)-oxide	Fcm^{-1}
ε_{Si}	Permittivity of silicon	Fcm^{-1}
ξ	Electric field	Vcm^{-1}
ξ_0	Maximum electric field at MS interface	Vcm^{-1}
σ	Conductivity	Scm^{-1}
χ_{Si}	Silicon electron affinity	eV
Γ	Tunneling probability	-

Symbol:	Description:	Unit:
$\mathit{\Phi}_B$	Schottky Barrier Height (*q)	eV
$\mathit{\Phi}_{Bn}$	Electron barrier height (*q)	eV
$\mathit{\Phi}_{Bp}$	Hole barrier height (*q)	eV
$\mathit{\Phi}_M$	Metal work function (*q)	eV
$\mathit{\Phi}_S$	Semiconductor work function (*q)	eV

List of Acronyms

Acronym:	Description:
AsymG	Asymmetric Gate
B2B	Band to Band
BBT	Band to Band tunneling
BOX	Buried Oxide
D-met	Drain metal
DOS	Density of States
EOT	Effective Oxide thickness
FD-SOI	Fully depleted SOI
FET	Field Effect Transistor
GWF	Gate workfunction
MOSFET	Metal oxide semiconductor field effect transistor
MS	Metal Semiconductor
NMOS	N channel MOSFET
QFL	Quasi Fermi Level
PMOS	P channel MOSFET
S	Subthreshold Swing
SB	Schottky Barrier
SBH	Schottky Barrier Height
SCE	Short channel effects
S/D	Source Drain
S-met	Source metal
SOI	Silicon on insulator
STS-FET	Schottky Tunneling Source FET

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