University of Twente
The Netherlands

Investigation of the band gap widening effect in thin silicon double gate MOSFETs

Master thesis

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Author
J.L.P.J. van der Steen

Supervisors
dr. ir. R.J.E. Hueting
dr. ir. C. Salm
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Semiconductor Components Group
Faculty of Electrical Engineering,
Mathematics & Computer Science
University of Twente
P.O. Box 217
7500 AE Enschede
The Netherlands

Author
J.L.P.J. van der Steen

Supervisors
dr. ir. R.J.E. Hueting
dr. ir. C. Salm
prof. dr. J. Schmitz

Abstract

The topic of this project is the analysis of the subthreshold current in thin silicon Double Gate (DG) MOSFETs, with a particular focus on observing the so-called effective band gap widening effect using electrical measurements. DG MOSFETs with a very thin silicon layer are expected to be promising candidates for the next generation CMOS technology: moving from single to double gate gives better control over the channel region, which improves the short channel performance and gives rise to an ideal subthreshold slope. As for the drain current, the charge carriers have to traverse an energy barrier when flowing from source to drain. For low gate bias, the height of the barrier is mainly determined by the band gap, making particularly the subtreshold current suitable for observing changes in the effective band gap. As the silicon layer thickness (i.e. the channel region) is shrunk to values below about 15 nm, quantum mechanical effects are expected to show up in the device characteristics. One of those effects is the widening of the effective band gap, which originates from splitting of both the conduction and valence band into subbands, due to confinement of the charge carriers in the very thin silicon layer between the Si/SiO_2 interfaces.

The effective band gap widening effect is investigated using temperature dependent IV and CV measurements. Essentially, both measurements rely on the strong temperature dependence of diffusion, which constitutes the dominant part of carrier transport in the subthreshold regime. Generally speaking, by comparing the characteristics of a device with a 'thick' silicon layer to the characteristics of a thin device (i.e. in which carrier confinement is important), the effective band gap widening effect should become apparent.
The results obtained from the IV measurements indicate that an increase in effective band gap occurs for decreasing silicon layer thickness. For a detailed quantitative analysis however, the measurements should be repeated on a larger number of devices, with thinner layers, fabricated in a more accurate process.
The CV measurements show that the device behavior in depletion and weak inversion is dominated by the implanted p^+ and n^+ regions adjacent to the intrinsic channel, being more pronounced for shorter devices. This should be investigated further with additional simulations, particularly concerning the temperature dependence.

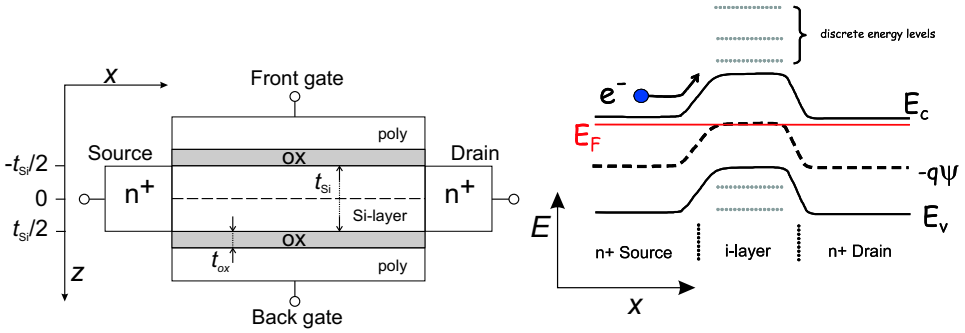
Contents

Chapter 1

Introduction

This report has been written in conclusion to a masters' project in the Semiconductor Components group at the University of Twente. The topic of this project is the analysis of the subthreshold current in thin silicon Double Gate (DG) MOSFETs, with a particular focus on measuring the so-called effective band gap widening effect. This report reflects the work which has been done during this project, offering a concise yet complete overview of the measurements and the theoretical background.

DG MOSFETs with a (very) thin silicon layer are expected to be promising candidates for the next generation CMOS technology: moving from single to double gate gives better control over the channel region, which improves the short channel performance and gives rise to an ideal subthreshold slope. A schematic cross-section of a DG device is depicted in figure 1.1(a), in which z is the direction perpendicular to the gates (which are along the x-axis). The silicon thickness is denoted with t_{Si}; z ranges from $-t_{\mathrm{Si}}/2$ to $t_{\mathrm{Si}}/2$, with $z = 0$ located midway the silicon film. In fact, the device to be investigated is not fully symmetric, but a Silicon-On-Insulator (SOI) based device of which the behavior equals the 'ideal' DG behavior under circumstances to be discussed later on.
The corresponding band diagram is given in figure 1.1(b). It is clearly visible that the charge carriers (in this case electrons) have to traverse an energy barrier when flowing from source to drain. The height of this barrier depends on the band gap, i.e. the difference between the conduction and valence band edge, and the gate-source voltage (V_{GS}). Note that when V_{GS} is increased up to or above the threshold voltage (V_{th}), the barrier will gradually decrease. Since this project aims at investigating the band gap, particularly the subthreshold region ($V_{\mathrm{GS}} < V_{\mathrm{th}}$) will be of interest. Hence, given a low V_{GS}, the band gap mainly determines the height of the barrier which the charge carriers have to cross.
Furthermore, as the device thickness is shrunk to values below about 10 nm,



(a) Schematic cross-section of a fully symmetric DG device; t_{Si} and t_{ox} denote the silicon film thickness and oxide thickness resp.

(b) Corresponding band diagram; E_F is the Fermi level, E_c and E_v are the conduction band and valence band edge resp.

Figure 1.1: Definition of the references

quantum mechanical effects are expected to show up in the device characteristics, among which the so-called band gap widening effect. This effect originates from splitting of both the conduction and valence band into subbands, due to structural confinement as a result of the small dimension in the quantization direction z. The emerging subbands give rise to an effective band gap which is larger than the band gap in a bulk semiconductor. Because the confinement of the charge carriers is stronger as the semiconductor film thickness decreases, the band gap widening effect is expected to be more pronounced for thinner semiconductor films.
In order to investigate the effective band gap widening effect, SOI DG devices with very thin layers will be studied. The project focusses on the subthreshold current since particularly in this region changes in the effective band gap can be observed.

Outline This report is organized as follows: after this introductory chapter the results of the literature survey will be presented, starting with the semi-classical subthreshold current model. As we are dealing with very thin SOI layers, quantum mechanical effects are likely to occur, which will be discussed in the subsequent section. The last part of chapter 2 concerns the theoretical principles behind the effective band gap extraction. In fact, the band gap widening effect is investigated using DC IV and CV measurements, both having the temperature as parameter. After having discussed the essential theory, the results of the measurements will be shown in chapter 3. In order to conclude this report, an overview of the findings and conclusions is presented in chapter 4. Some additional material can be found in the appendix.

Chapter 2

Theory

The first part of this chapter mainly deals with the results of the initial literature survey, i.e. the comparison of two commonly used approaches to describe the subthreshold current in symmetric Double-Gate (DG) devices: the semi-classical model by Y. Taur [1] and the quantum-mechanical approach according to G. Baccarani [2] and D. Munteanu [3]. Actually, these models can be used to describe the full range of operating regimes, but this thesis concentrates on the subthreshold region and in particular the diffusive part of the subthreshold current for which the drain-source voltage (V_{DS}) is only a few tens of mV.

The outline of this chapter is as follows: first the semi-classical method will be described briefly. This involves a few assumptions which hold in our region of interest, being below the threshold voltage (V_{th}), in which the subthreshold current originates from diffusion of charge carriers in the channel. In the next section the quantum-mechanical model will be introduced, starting from a rather general solution of the Schrödinger equation. This gives a mathematical description of electron confinement in very thin silicon layers. After having described the two approaches, the third section eventually deals with the comparison of the subthreshold current or, to be more precise, the charge in the channel, to which the subthreshold current is proportional. This comparison will be carried out with the silicon film thickness as parameter. In fact, as the thickness is scaled down, the differences between the semi-classical and the quantum mechanical model are expected to increase. This effect originates from the fact that quantum mechanical effects are more pronounced for thinner films, as will be explained in section 2.2. Literature suggests [1] that quantum mechanical effects are noticeable in devices with a film thickness less than 5 nm, resulting in a significant discrepancy between the classical and quantum mechanical model. As mentioned before, the devices used in this project are SOI based MOSFETs operated in DG mode rather than fully symmetric DG devices. So an

additional model which proved to describe correctly the subthreshold current in SOI devices will be discussed briefly in section 2.4. Finally, the last section concerns the effective band gap widening effect.

2.1 The semi-classical method

This section deals with the semi-classical method to calculate the inversion charge and the subthreshold current. The theory is based on [1] and assumes a fully symmetric DG device. The DG structure in combination with a thin silicon layer allows (in theory) for setting the threshold voltage by choosing a gate-material with an appropriate work function, which is assumed to be poly-crystalline silicon, thereby reducing the need for dopants in the silicon body (i.e. the channel region). Therefore in the following a lightly doped or even undoped body is assumed, which means that hardly any accumulated charge is present when the device is off. One can state that the amount of depletion charge can be neglected in the subthreshold region. Furthermore, as the body of the DG structure is very thin (i.e. $t_{\mathrm{Si}} \leq 15\,\mathrm{nm}$) the channel will enter (weak) inversion as a whole, provided that the gate voltage is low (i.e. below threshold). This effect is called *volume inversion* [4] and it basically means that the charge is uniformly distributed throughout the thickness (z) of the semiconductor film. However, as the gate voltage is increased up to or above the threshold voltage, the uniform inversion layer will gradually split and ultimately two separate channels will emerge along both Si/SiO_2-interfaces.
When the analysis is restricted to the 'volume inversion' region, there will be no sheet charge at or close to the Si/SiO_2-interfaces across which voltage drops. Instead, the uniform charge distribution in the (ultra) thin film results in a constant potential along the z-direction (i.e. the silicon layer). Note however that when V_{GS} is very close to the threshold voltage, the inversion charge density close to the gates will be slightly higher than in the center of the film (i.e. $z = 0$). As a result, a small voltage will drop across the inversion charge, giving a symmetric potential along z with a minimum at $z = 0$ (assuming a symmetric device). Nevertheless, when $V_{\mathrm{GS}} < V_{\mathrm{th}}$, the voltage drop across the inversion charge is negligible due to the uniformly distributed charge throughout the channel. Hence, the potential at the silicon surface $\psi_{\mathrm{s,cl}}$, i.e. at $z = \pm t_{\mathrm{Si}}/2$, will be approximately equal to the potential at $z = 0$ and is directly proportional to V_{GS}. This translates into

$$\psi_{\mathrm{s}}(V_{\mathrm{GS}}) = -\Delta\phi_{\mathrm{i}} + V_{\mathrm{GS}} \tag{2.1}$$

with $\Delta\phi_{\mathrm{i}}$ the work function difference between the gate and the intrinsic silicon layer. Note that the above equation assumes the potential to be constant in the transport direction, so the widely used 'gradual channel approximation' is assumed to hold. Otherwise, a 2D Poisson equation should

be solved which relates the potential profile to the charge distribution.
The charge density ρ_{cl} depends on ψ_{s} via

$$\rho_{\mathrm{cl}} = n_{\mathrm{i}} \exp\left(\frac{\mathrm{q}\psi_{\mathrm{s}}(V_{\mathrm{GS}})}{\mathrm{k}T}\right) \tag{2.2}$$

with 'q' the elementary charge, 'k' Boltzmann's constant, T the temperature and n_{i} the intrinsic carrier concentration. Equation (2.2) employs Boltzmann's approximation, which is applicable for diffusion currents. The intrinsic carrier concentration is given by

$$\begin{aligned} n_{\mathrm{i}} = \sqrt{np} &= \sqrt{N_{\mathrm{C}} N_{\mathrm{V}}} \exp\left(-\frac{E_{\mathrm{g}}}{2\mathrm{k}T}\right) \\ &= \left(\frac{\mathrm{k}T}{\pi\hbar^2}\right)^{\frac{2}{3}} \sqrt{m_{\mathrm{n}}^{3/2} m_{\mathrm{p}}^{3/2}} \exp\left(-\frac{E_{\mathrm{g}}}{2\mathrm{k}T}\right) \end{aligned} \tag{2.3}$$

N_{C} and N_{V} are the effective Density of States (DoS) in the bulk conduction and valence band respectively; E_{g} is the band gap, and m_{n} and m_{p} denote the bulk effective mass of electrons and holes respectively. Integrating the charge density over the film thickness, which is just multiplying with t_{Si} in case of a uniform charge distribution, and multiplying with the elementary charge gives the total charge per unit area

$$Q_{\mathrm{e,cl}}(V_{\mathrm{GS}}) = -\mathrm{q} \cdot t_{\mathrm{Si}} \cdot \rho_{\mathrm{cl}}(V_{\mathrm{GS}}) \tag{2.4}$$

Below threshold the current mainly originates from diffusion, so only the diffusive part of the Drift-Diffusion equation [5] will be taken into account. After incorporating the device geometry and assuming an NMOS device, the following equation for the drain-source current per unit width (W) results:

$$I_{\mathrm{DS,cl}} = \frac{\mu_{\mathrm{n}}\mathrm{k}T}{\mathrm{q}L} Q_{\mathrm{e,cl}}(V_{\mathrm{GS}}) \left[1 - \exp\left(-\frac{\mathrm{q}V_{\mathrm{DS}}}{\mathrm{k}T}\right)\right] \tag{2.5}$$

in which μ_{n} is the electron mobility and L the length of the channel. Equation (2.5) is clearly directly proportional to the total inversion charge, so in the following usually the charge density will be considered, given a constant V_{DS}. This allows for a geometry and mobility independent comparison with values given in literature.

2.2 The quantum mechanical approach

After having described the semi-classical method, which was rather straightforward given the above simplifications, this section will deal with the slightly more involved quantum mechanical (QM) approach.
The same assumptions hold as described above, being a very low net doping

($N_A - N_D \approx 0$) and $V_{GS} < V_{th}$. For completeness equation (2.1) is restated below

$$\psi_s(V_{GS}) = -\Delta\phi_i + V_{GS} \tag{2.6}$$

However, confinement of the charge carriers (in this analysis only electrons, see also section 2.4) in the very thin silicon layer will result in splitting of the conduction band into multiple subbands. This means that in the conduction band 'forbidden' zones will appear, in which no electron can reside. This originates from the rearrangement of the allowed energies into so-called ladders of energy subbands, depending on the location of the energy minima (called *valleys*) in the 3D (bulk) silicon crystal and the orientation of the gates (i.e. the quantization direction z). The emerging of the subbands (and the gaps in between) results in a reduced DoS compared to bulk silicon, in which the conduction band consists of a virtually infinite number of energy levels. So, in order to relate the gate voltage to the inversion charge density, the charge distribution should be calculated taking into account the allowed subbands. Since quantum confinement has been dealt with extensively in literature [6][7][8] only the most essential steps will be mentioned here. The band structure will be calculated using the commonly employed Effective Mass Approximation (EMA). This model assumes a parabolic energy dispersion, which actually is a valid assumption only close to the band edges. However, this analysis focusses on the subthreshold current meaning that the charge carriers only occupy energy levels close to the band edges. Hence, it is legitimate to use the EMA.
The confinement of the electrons in the silicon layer can be regarded as a potential well, with barriers formed by the Si/SiO_2 interfaces. Initially, the height of these barriers is assumed to be infinite.

2.2.1 Infinite Si/SiO_2 barrier

The energy dispersion of an electron in the quantization direction (z) is given by the solutions of the Schrödinger equation:

$$-\frac{\hbar^2}{2m^*_{z,k}}\frac{d^2}{dz^2}\Psi(z) = E_n\Psi(z) \tag{2.7}$$

with $\hbar$ the reduced Plank's constant and $m^*_{z,k}$ the electron effective quantization mass for valley k, in which several quantum mechanical effects are incorporated. The absolute value of the wave function Ψ gives for each subband n the probability of an electron residing at a specific position along the z direction, according to

$$\Psi(z) = \sqrt{\frac{2}{t_{Si}}}\sin\left[\frac{n\pi}{t_{Si}}\left(z + \frac{t_{Si}}{2}\right)\right] \tag{2.8}$$

Furthermore, the minima (lowest energies) for each subband n in valley k are given by the eigenvalues $E_{\mathrm{k,n}}$ of eq. (2.7), and can be calculated with

$$E_{\mathrm{k,n}} = \frac{\hbar^2}{2m^*_{\mathrm{z,k}}} \left(\frac{\pi n}{t_{\mathrm{Si}}}\right)^2 \tag{2.9}$$

Summing the probability functions over all valleys k and subbands n gives the following charge density:

$$\rho_{\mathrm{qm}}(z) = \sum_k \sum_n |\Psi(z)|^2 N_{\mathrm{k}} \exp\left(-\frac{E_{\mathrm{k,n}} + E_{\mathrm{g}} - \mathrm{k}T \ln \frac{N_{\mathrm{V}}}{N_{\mathrm{C}}}}{2\mathrm{k}T}\right) \exp\left(\frac{\mathrm{q}\psi_{\mathrm{s}}(V_{\mathrm{GS}})}{\mathrm{k}T}\right) \tag{2.10}$$

with

$$N_{\mathrm{k}} = \frac{m^*_{\mathrm{d,k}} \mathrm{k}T}{\pi\hbar^2} \tag{2.11}$$

in which $m^*_{\mathrm{d,k}}$ denotes the DoS effective mass for valley k. Actually, eq. (2.10) is just eq. (2.2) with the 'classic' n_{i} replaced by the quantum mechanical intrinsic inversion charge. The latter depends strongly on the silicon film thickness via eq. (2.8) and eq. (2.9), in contrast to the the classical inversion charge density. Equation (2.10) depends on the gate voltage via $\psi_{\mathrm{s}}(V_{\mathrm{GS}})$ since the potential along the z direction controls the occupation of the subbands. Integration of the charge density along the z direction gives the total inversion charge and, incorporating the device geometry, the current:

$$\begin{aligned} Q_{\mathrm{e,qm}}(V_{\mathrm{GS}}) &= \int_{<t_{\mathrm{Si}}>} \rho_{\mathrm{qm}}(z)\mathrm{d}z \\ &= \sum_k \sum_n N_{\mathrm{k}} \exp\left(-\frac{E_{\mathrm{k,n}} + E_{\mathrm{g}} - \mathrm{k}T \ln \frac{N_{\mathrm{V}}}{N_{\mathrm{C}}}}{2\mathrm{k}T}\right) \exp\left(\frac{\mathrm{q}\psi_{\mathrm{s}}(V_{\mathrm{GS}})}{\mathrm{k}T}\right) \end{aligned} \tag{2.12}$$

$$I_{\mathrm{DS,qm}} = \frac{\mu_{\mathrm{n}} \mathrm{k}T}{\mathrm{q}L} Q_{\mathrm{e,qm}}(V_{\mathrm{GS}}) \left(1 - \exp\left(-\frac{\mathrm{q}V_{\mathrm{DS}}}{\mathrm{k}T}\right)\right) \tag{2.13}$$

Note that this analysis assumes that only electron confinement occurs, as already mentioned before. Hence the reference is the intrinsic Fermi level E_{FI}, which is equal to $E_{\mathrm{g}}/2 + \mathrm{k}T/2 \cdot \ln(N_{\mathrm{V}}/N_{\mathrm{C}})$. Furthermore, the energy minima $E_{\mathrm{k,n}}$ calculated in [2] and [3] should be divided by two, as eq. (2.10) shows.

2.2.2 Finite Si/SiO_2 barrier

The previous calculation of the inversion charge density imposed closed boundary conditions for solving the Schrödinger equation, basically meaning that no charge could penetrate through the Si/SiO_2 barrier into the oxide. Hence, the integral over the wave function $|\Psi(z)|^2$ in the silicon film (see eq. (2.12)) is just equal to one, as the probability that an electron will enter the oxide is zero. Assuming, however, confinement in a potential well with infinite barriers could be questionable in reality. On the other hand, this project mainly focusses on the subthreshold current with low drain and gate voltages, hence the charge carriers are very unlikely to reach high energies. To verify this assumption the charge distribution will be calculated using a barrier of 3 eV, which is a realistic value for the Si/SiO_2 interface. As in the previous section, only the most essential steps will be mentioned, but the original and more elaborate derivation of the equations for motion between two finite potential barriers can be found in [9].

The slightly rewritten Schrödinger equation for motion within the potential well with finite barrier V_0 is given by

$$\frac{\mathrm{d}^2\Psi}{\mathrm{d}z^2}(z) + \kappa^2\Psi(z) = 0 \qquad \kappa^2 = \frac{2m^*_{\mathrm{z,k}}}{\hbar^2}(V_0 + E_{\mathrm{k,n}}) \tag{2.14}$$

Outside the well (i.e. $|z| > a = t_{\mathrm{Si}}/2$) the wave function will decrease exponentially with γ, according to

$$\frac{\mathrm{d}^2\Psi}{\mathrm{d}z^2}(z) - \gamma^2\Psi(z) = 0 \qquad \gamma^2 = \frac{2m^*_{\mathrm{z,k}}|E_{\mathrm{k,n}}|}{\hbar^2} \tag{2.15}$$

Because the wave function should be continuous both in itself and in its first derivative, one could equivalently require that the logarithmic derivative of the wave function be continuous. This results in the following equation for the even symmetry solutions (eigenvalues) at the Si/SiO_2 interface:

$$\tan(\kappa a) = \frac{\gamma}{\kappa} = \sqrt{\frac{\beta^2}{(\kappa a)^2} - 1} \qquad \beta^2 = \frac{2m^*_{\mathrm{z,k}}V_0a^2}{\hbar^2} \tag{2.16}$$

The odd symmetry minima can be found by solving

$$\operatorname{cotan}(\kappa a) = -\sqrt{\frac{\beta^2}{(\kappa a)^2} - 1} \tag{2.17}$$

Once the minima $E_{\mathrm{k,n}}$ of the subbands are known, the wave functions can be calculated. The wave function within the silicon film can be written as

$$\Psi_{\mathrm{Si}}(z) = \alpha\frac{t_{\mathrm{Si}}}{2}\sin\left(\kappa z + \frac{n\pi}{2}\right) \tag{2.18}$$

with κ as defined above and α a normalization constant, calculated from the requirement that the total probability of an electron being at any position along the z direction equals one, as given below.

$$\int_{-\infty}^{\infty} |\Psi_{\text{fin}}|^2(z)\mathrm{d}z = 1 \tag{2.19}$$

Hence, Ψ_{fin} in eq. (2.19) is the total wave function, consisting of Ψ_{Si} and the exponentially decaying parts in the top and bottom oxide. These are denoted with $\Psi_{\text{ox,t}}$ and $\Psi_{\text{ox,b}}$ respectively, and are given by

$$\begin{aligned}
\Psi_{\text{ox,t}}(z) &= \Psi_{\text{Si}}\left(\tfrac{-t_{\text{Si}}}{2}\right) \cdot \exp\left(-\gamma\left[-z - \frac{t_{\text{Si}}}{2}\right]\right) \\
&= \Psi_{\text{Si}}\left(\tfrac{-t_{\text{Si}}}{2}\right) \cdot \exp\left(\gamma\left[z + \frac{t_{\text{Si}}}{2}\right]\right) \\
\Psi_{\text{ox,b}}(z) &= \Psi_{\text{Si}}\left(\tfrac{t_{\text{Si}}}{2}\right) \cdot \exp\left(-\gamma\left[z - \frac{t_{\text{Si}}}{2}\right]\right)
\end{aligned} \tag{2.20}$$

Replacing $\Psi(z)$ and $E_{\text{k,n}}$ in eq. (2.10) by $\Psi_{\text{fin}}(z)$ and the eigenvalues calculated with finite barrier respectively, the charge distribution within the finite potential well is obtained.

2.3 Comparison classic and QM model

In this section the charge distribution and total inversion charge resulting from the calculations in the previous sections will be discussed. The charge distribution along the z-direction is depicted in figure 2.1, comparing the classical model with the quantum mechanical approach. The latter has been calculated using an infinite barrier and a 3 eV barrier. Furthermore, the charge density is normalized on the silicon film thickness. In the remainder silicon (100) is assumed, with the quantization direction z along the [001] axis.

2.3.1 Charge distribution

Figure 2.1 clearly shows that according to the classical model the charge distribution is independent of the silicon film thickness. One should assure, however, that t_{Si} is thin enough for the assumption of volume inversion to hold (i.e. one uniformly distributed channel). In contrast to the constant classical charge distribution, the quantum mechanical approach predicts a maximum at the center of the channel, the magnitude of which depends on t_{Si}: the inversion charge density is inversely proportional to the silicon film thickness, up to approximately 15 nm. This can be explained as follows: the minima of the subbands go up in energy as t_{Si} decreases (see also eq. (2.9)).

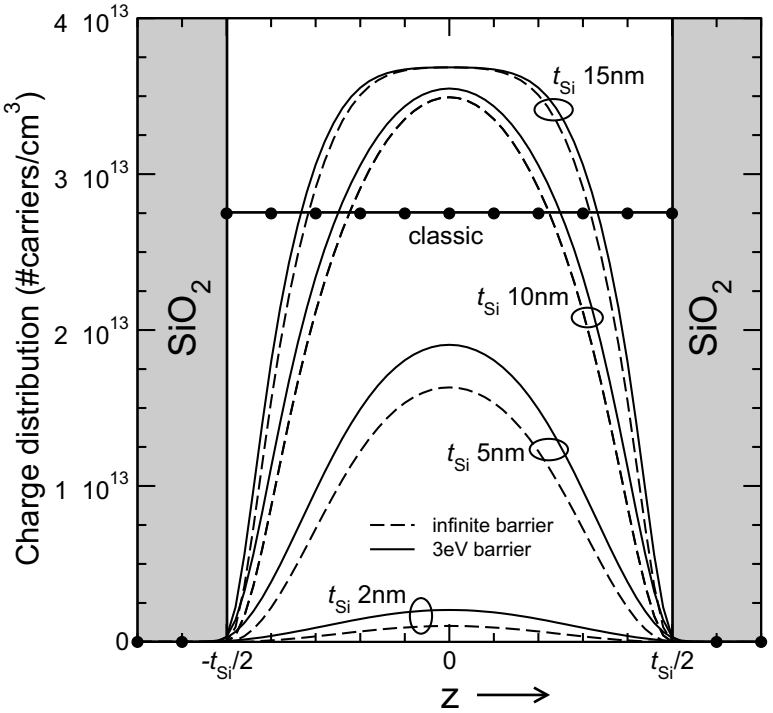


Figure 2.1: QM and classical charge distribution throughout the channel depth for several t_{Si}; Calculated with $N_{\mathrm{C}} = 2.8 \times 10^{19}\,\mathrm{cm}^{-3}$, $N_{\mathrm{V}} = 1.04 \times 10^{19}\,\mathrm{cm}^{-3}$, $T = 300\,\mathrm{K}$ and $V_{\mathrm{GS}} = 0.2\,\mathrm{V}$.

Hence less electrons will occupy a given subband, as they need more energy to enter that particular subband. This will result in a reduction of the inversion charge density. Above $t_{Si} = 15\,\text{nm}$ however, the subbands have merged into one quasi-continuous conduction band, making the effect of structural quantum confinement negligible. Furthermore, the figure shows that for $t_{Si} = 15\,\text{nm}$ the maximum in the charge density flattens, and one would expect that eventually the total integrated charge density (hence the total inversion charge) will equal the total inversion charge given by the classical model. This, however, appears to be strongly dependent on the values of N_C and N_V used in eq. (2.3).
As for the influence of the barrier height, we can conclude that compared to the total inversion charge, the amount of charge which penetrates into the oxide is negligible. Much more apparent however, is the effect of the minima of the subbands moving downward in energy due to the finite barrier height: the difference in maximum charge density as calculated with either an infinite or a finite (here 3 eV) barrier ranges from almost zero for $t_{Si} = 15\,\text{nm}$ via 15% for $t_{Si} = 5\,\text{nm}$ up to approximately 50% when t_{Si} equals 2 nm.

2.3.2 Inversion charge

The next figure shows the total inversion charge as function of the gate voltage for several silicon thicknesses. Hence the total charge is the integral over the charge distribution within the channel region as shown in figure 2.1. Obviously the exponential dependence of the total inversion charge on the gate voltage gives a straight line on logarithmic scale. Furthermore, the figure shows that the classical and quantum-mechanical model almost coincide when the silicon film is relatively thick ($\geq 10\,\text{nm}$). For the thinnest layer however, the difference in total charge between the classical and quantum-mechanical model is more than one order of magnitude. Moreover it appears that the influence of the potential barrier height is appreciable for the thinnest film. This was already observed in the previous figure, though the effect of the barrier height is less when the *total* charge is taken into account, rather than only the maximum at the center of the channel.

In short, one could state that the influence of the silicon layer thickness through quantum-mechanical effects (here *electron* confinement) is most pronounced for very thin layers, below approximately 5 nm. Furthermore, the influence of the potential barrier height is only significant for the thinnest layers (around 2–3 nm). Since the thickness of the devices used in this project is above 4 nm, an infinite barrier will be assumed in the remainder of this report. The resulting analytical equations for the energy states greatly simplify the calculations, yet giving a sufficiently accurate description of quantum confinement in the devices used in this project.

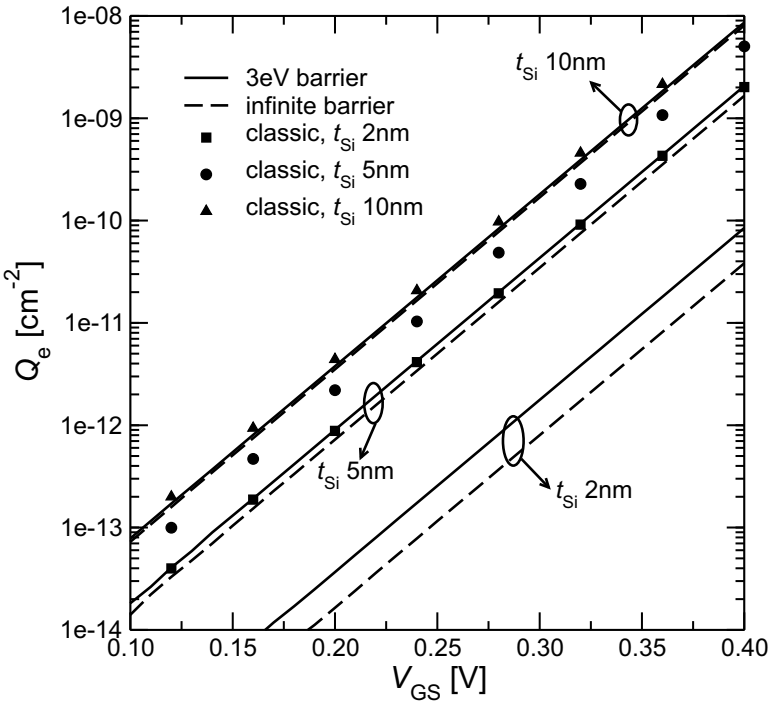


Figure 2.2: QM and classical inversion charge density for t_{Si} 2, 5 and 10 nm.

2.4 Subthreshold current model SOI based devices

As already mentioned before, the devices used in this project are SOI based MOSFETs, rather than fully symmetric DG devices. This means that the 'backgate' of the SOI devices controls the inversion charge in the channel through a relatively thick Buried Oxide (BOX) layer, while the 'front' dielectric is only tens of the BOX layer thickness. Hence, the models discussed previously are not fully applicable to SOI devices posing the demand for a model which incorporates the asymmetric SOI geometry appropriately.
The model suitable for describing the subthreshold current in asymmetric SOI devices is derived and presented in [10], so only the resulting equations and conclusions will be mentioned below.
The inversion charge density for either an NMOS (lower sign) or PMOS device (upper sign) is given by

$$Q_{\mathrm{i}} = \pm \mathrm{q} \cdot t_{\mathrm{Si}} \cdot n_{\mathrm{i}} \cdot u_{\mathrm{T}} \cdot \left[\frac{\exp\left(\mp \frac{\psi_{\mathrm{SB}}}{u_{\mathrm{T}}}\right) - \exp\left(\mp \frac{\psi_{\mathrm{SG}}}{u_{\mathrm{T}}}\right)}{\psi_{\mathrm{SB}} - \psi_{\mathrm{SG}}} \right] \tag{2.21}$$

with the thermal voltage $u_{\mathrm{T}} = \mathrm{k}T/\mathrm{q}$, and ψ_{SG} and ψ_{SB} the surface potential at the front and back gate respectively. In fact, these potentials depend on the geometry (t_{ox} and t_{Si}), the work function differences and the gate volt-

ages. However, in case of 1) either a fully symmetric DG device or an SOI based device in which the front gate oxide is much thinner than the thickness of the BOX layer, and 2) equally biased front and back gate, eq. (2.21) reduces to the expression in eq. (2.4). For single gate (SG) operation (i.e. front and back gate biased differently) one should employ eq. (2.21), which comprises the effect of the unequal gate potentials. Furthermore, in absence of quantum confinement (hence relatively thick Si layers) n_i equals the definition in eq. (2.2). In order to incorporate quantum confinement, the product $t_\mathrm{Si} \cdot n_\mathrm{i}$ should be replaced by the following expression for the quantum mechanical charge distribution:

$$N_\mathrm{i} = \left(\frac{\mathrm{k}T}{\pi\hbar^2}\right) \sqrt{\sum_k \sum_n m^*_{\mathrm{dk,c}} \exp\left(-\frac{E_{\mathrm{kn,c}}}{\mathrm{k}T}\right)} \times \sqrt{\sum_k \sum_n m^*_{\mathrm{dk,v}} \exp\left(-\frac{E_{\mathrm{kn,v}}}{\mathrm{k}T}\right)} \exp\left(-\frac{E_\mathrm{g}}{2\mathrm{k}T}\right) \tag{2.22}$$

Note that in eq. (2.22) besides the electron confinement (see eq. (2.9)) also hole confinement is taken into account. This can be explained by noting that the motion of the holes as well as the electrons is confined between the front and back oxide. Hence, the confining potential can be described by a squared potential well rather than the approximately triangular shaped potential distribution which confines either the electrons or the holes in n or p type inversion layers in conventional bulk MOS devices. As a result of confinement in the very thin silicon layer between the two oxide barriers, a DG device will exhibit quantization in both the conduction and the valence band. In fact, the silicon layer thickness below which quantum confinement becomes apparent will be higher than the value mentioned in the previous section, due to the combination of electron and hole confinement ($t_\mathrm{Si} \approx 15\,\mathrm{nm}$). It is important to note that quantum confinement effectively results in a widening of the band gap, which will be explained in more detail in the next section.
Furthermore, the front gate oxide in the devices to be investigated is much thinner than the thickness of the BOX layer, hence the devices will nearly behave as symmetric DG devices. So, in the remainder of this report equations (2.4) and (2.22) will be employed to compare the experimental data with the theoretical values.

2.5 Effective band gap extraction

After having introduced the equations for the inversion charge density either with or without quantum confinement, this section will deal with the theoretical background of the effective band gap extraction. Ultimately, the

aim is to observe the effective band gap widening effect by means of electrical measurements. The analysis starts with the discussion of the DC IV measurements, followed by the CV measurements.

2.5.1 DC IV measurements

In order to observe the effective band gap widening effect, the drain current is to be measured for devices with different layer thicknesses. As stated in section 2.4, hole and electron confinement is expected to occur in devices with a very thin silicon layer (i.e. t_{Si} below 15 nm), resulting in splitting of the conduction and valence band into subbands: gaps or 'forbidden' zones will emerge and the edge of the conduction (valence) band will move to a higher (lower) energy. Since particularly in the subthreshold region only the highest valence subband and the lowest conduction subband are most likely to be occupied, the 'energy offsets' of the first valence and conduction subband introduced by the quantization will give rise to a wider effective band gap compared to the band gap in devices in which no quantum confinement occurs (thicker layers, or bulk silicon). So, in short, depending on the Si layer thickness effective band gap widening will be noticeable.
By taking the ratio of the measured drain currents at equal gate voltage for two devices with different layer thicknesses, the following expression is obtained:

$$I_{\mathrm{rat}} = \frac{I_{\mathrm{thick}}}{I_{\mathrm{thin}}} = \frac{\mu_{\mathrm{thick}}(T) Q_{\mathrm{i,thick}}(t_{\mathrm{Si}}, T)}{\mu_{\mathrm{thin}}(T) Q_{\mathrm{i,thin}}(t_{\mathrm{Si}}, T)} \tag{2.23}$$

with $\mu(T)$ the temperature dependent mobility, and Q_{i} the amount of inversion charge. Depending on t_{Si}, Q_{i} can be replaced by eq. (2.21) or eq. (2.4) in presence or absence of quantum confinement respectively. If we now assume that at least in the thinnest layer quantum confinement occurs, then the wider effective band gap of the thinnest device will give rise to an exponential temperature dependence of I_{rat}, according to

$$I_{\mathrm{rat}} = \frac{I_{\mathrm{thick}}}{I_{\mathrm{thin}}} \propto \frac{\{\mu(T) g(T, t_{\mathrm{Si}})\}_{\mathrm{thick}}}{\{\mu(T) g(T, t_{\mathrm{Si}})\}_{\mathrm{thin}}} \cdot \exp\left(\frac{\Delta E_{\mathrm{g,eff}}}{\mathrm{k}T}\right) \tag{2.24}$$

in which $g(T, t_{\mathrm{Si}})$ is a function incorporating the effective density of states. A few remarks should be made regarding the temperature dependence of the above equation. First of all, the inversion charge concentration depends on the temperature either via n_{i} in eq. (2.2) (classical model) or N_{k} in eq. (2.10) (QM approach). Furthermore, the band gap itself is also temperature dependent, as commonly described by the following semi-empirical equation

$$E_{\mathrm{g}} = E_{\mathrm{g},0} - \frac{\alpha T^2}{T + \beta} \tag{2.25}$$

with typical values $E_{g,0} = 1.125\,(\text{eV})$, $\alpha = 4.73 \cdot 10^{-4}\,(\text{eV/K})$ and $\beta = 636\,(\text{K})$.
If we now assume that the temperature dependence of μ and the density of states is approximately equal for both devices, equation (2.24) reduces to

$$I_{\text{rat}} = \frac{I_{\text{thick}}}{I_{\text{thin}}} \propto \frac{\{\mu g(t_{\text{Si}})\}_{\text{thick}}}{\{\mu g(t_{\text{Si}})\}_{\text{thin}}} \cdot \exp\left(\frac{\Delta E_{\text{g,eff}}}{\text{k}T}\right) \tag{2.26}$$

So, when plotting $\log(I_{\text{rat}})$ versus the inverse temperature, one would expect a linearly increasing curve with slope equal to $\Delta E_{\text{g,eff}}$.

2.5.2 *CV* measurements

Similar to the *IV* measurements above, *CV* measurements could be used to observe the effective band gap widening effect. In fact, as the current is related to the charge through (a.o.) the mobility, eq. (2.26) needs only slight modification, giving

$$Q_{\text{rat}} = \frac{Q_{\text{thick}}}{Q_{\text{thin}}} \propto \frac{\{f(t_{\text{Si}})\}_{\text{thick}}}{\{f(t_{\text{Si}})\}_{\text{thin}}} \cdot \exp\left(\frac{\Delta E_{\text{g,eff}}}{\text{k}T}\right) \tag{2.27}$$

with $f(t_{\text{Si}})$, again, a function which incorporates the effective density of states. Furthermore, note that in subthreshold the charge is directly proportional to the capacitance, as given by

$$C(V_{\text{GS}}) = -\frac{\text{d}Q_{\text{e}}}{\text{d}V_{\text{GS}}} = \frac{\text{d}}{\text{d}V_{\text{GS}}} \text{q} n_{\text{i}} t_{\text{Si}} \exp\left(\frac{V_{\text{GS}}}{u_{\text{T}}}\right) = \frac{\text{q} n_{\text{i}} t_{\text{Si}}}{u_{\text{T}}} \exp\left(\frac{V_{\text{GS}}}{u_{\text{T}}}\right) \tag{2.28}$$

using eq. (2.3).
A second note concerns the parasitic capacitances which could affect the measurements. In an attempt to eliminate the influence of the parasitics, differential measurements will be used: devices with different channel lengths will be measured for each layer thickness. By plotting the difference and assuming that for each combination of channel lengths the parasitic capacitances are equal, the actual intrinsic capacitance $C_{\text{int}}\,(\text{F}/\mu\text{m}^2)$ can be obtained as follows

$$\begin{aligned} C_1 &= \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \cdot W L_1 + C_{\text{par}} \\ C_2 &= \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \cdot W L_2 + C_{\text{par}} \\ \text{with} \quad \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} &\equiv C_{\text{int}} \\ \Rightarrow C_{\text{int}} &= \frac{C_1 - C_2}{W(L_1 - L_2)} \end{aligned} \tag{2.29}$$

By doing so, *ideally* the effect of the parasitics will be eliminated. Furthermore, as already mentioned in the above, the inversion charge is directly

proportional to the capacitance. So, by observing the $C(V_{\mathrm{GS}})$ characteristic in the transition region from depletion to inversion, the gate voltage depencence of the charge with the temperature as parameter can be derived. The effective band gap widening effect should become apparent when this measurement is carried out for several silicon layer thicknesses.

Chapter 3

Results

This chapter deals with the experiments which have been carried out to investigate the effective band gap widening effect electrically. The discussion starts with the results of the IV measurements, followed by the CV measurements in section 3.2. Basically, both measurements rely on the strong temperature dependence of diffusion, which constitutes the dominant part of carrier transport in the subthreshold regime. Generally speaking, when the characteristics of a device with a 'thick' silicon layer are compared to the device characteristics of a 'thin' layer (i.e. in which carrier confinement is important), the effective band gap widening effect should become apparent as was pointed out in the previous chapter.

3.1 IV measurements

The devices used for these experiments are SOI based n-type and p-type MOSFETs, of which a schematic cross section is shown in figure 3.1.
Fig. 3.2a depicts a TEM image of the channel–drain transition in an actual SOI DG NMOS device with a BOX layer thickness of 400 nm. The channel length is fairly large (26 μm) to make sure that no short channel effects occur. Figure 3.2b shows a more detailed TEM image of the center of the channel for which t_{Si} is 5 nm.[1] The DG SOI devices can be operated in Single Gate (SG) or Double Gate (DG) mode. In SG mode, the front (top) gate is swept, while the back gate is kept constant at 0V. When the device operates in DG mode, both the front and back gate are swept simultaneously. To denote the difference in subthreshold current, figure 3.3 shows a typical $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ curve for an n-type device operating in either mode.

Though the difference is modest, the plot clearly shows that operating

[1] The devices were realized by T. Hoang at MESA+, University of Twente.
The samples were prepared by MASER Engineering using Focused Ion Beam;
TEM analysis was carried out at Philips Research Eindhoven.

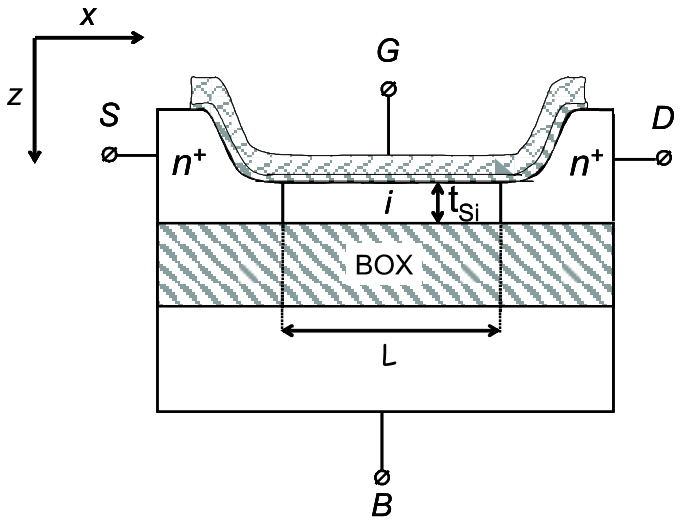
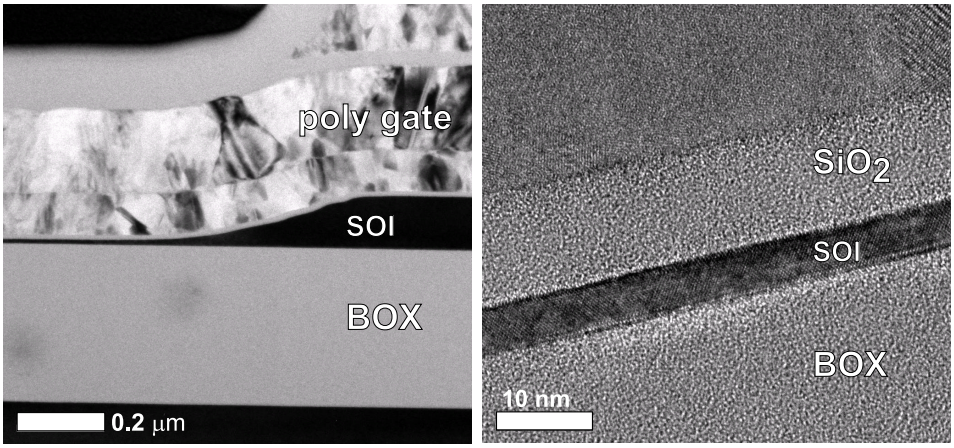


Figure 3.1: Schematic cross-section SOI DG NMOS



(a) Channel–Drain transition region (b) Detailed image channel area

Figure 3.2: TEM images DG SOI device; t_{Si} 5 nm; t_{BOX} 400 nm; t_{ox} 45 nm.

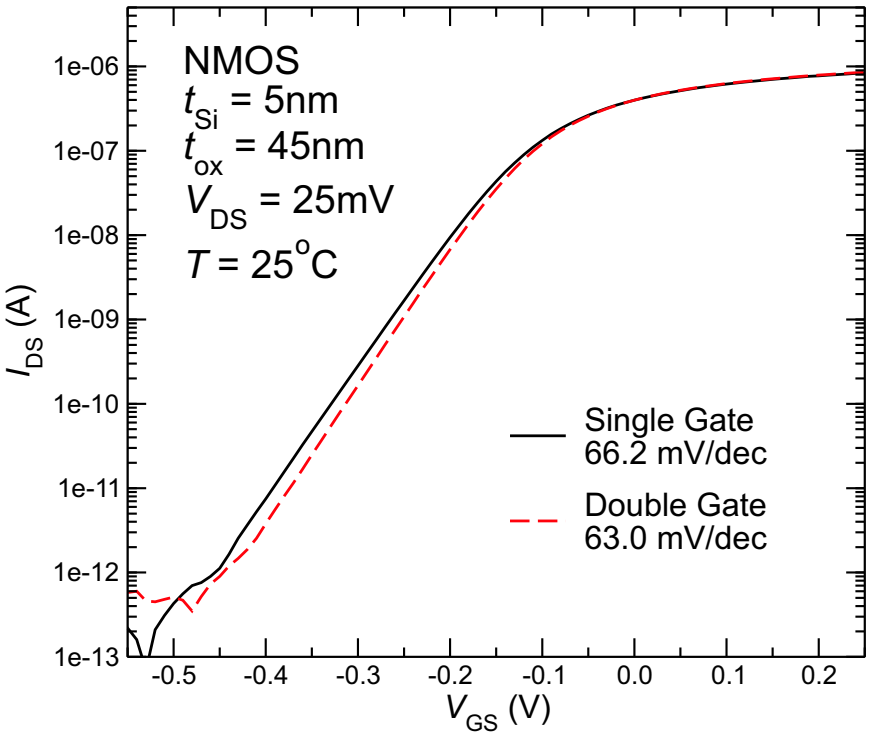


Figure 3.3: typical I_{DS} curve for SG and DG operation mode.

the device in DG mode results in a slightly steeper subthreshold slope (63 mV/dec) compared to the slope in SG mode (66 mV/dec). This originates from the fact that in DG mode both the front and back gate control the charge in the channel, rather than just the front gate when the device is in SG mode. As a result, by operating the device in DG mode a better control of the inversion charge, hence the current, is achieved. This reduces the voltage needed to increase the current with one decade, yielding a steeper subthreshold slope. Moreover, as was described in [10], when the thickness of the BOX layer in a DG SOI MOSFET is far thicker than the front gate oxide, the device will behave as a fully symmetric device. Since t_{ox} in the devices at hand is only approximately one tenth of the BOX layer thickness, this requisite readily holds thus making the subthreshold slope and temperature dependent behavior comparable to a fully symmetric device. Therefore, as for the *IV* measurements only DG operation will be considered.

3.1.1 Temperature dependence

As already mentioned before, the subthreshold current is strongly temperature dependent, a fact which can be exploited to extract the effective band gap. To illustrate the influence of the temperature, a typical set of *IV* curves is shown in figures 3.4 and 3.5 (PMOS and NMOS respectively) for several well–defined temperatures ranging from −25°C to 200°C. Three regions can

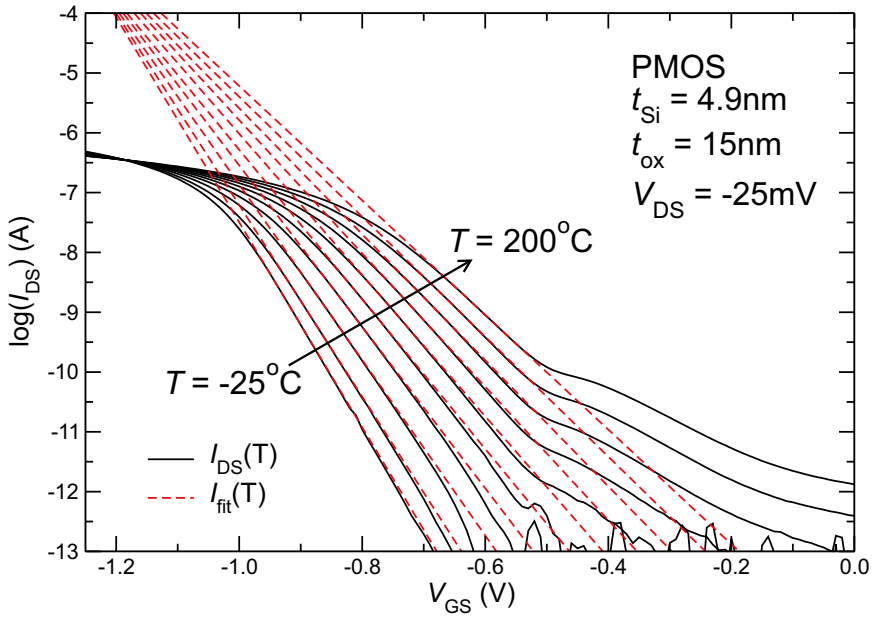


Figure 3.4: PMOS $I_{DS}(V_{GS})$ for $T = -25 \ldots 200$°C (solid lines); the dashed lines have been fit to the ideal subthreshold region to eliminate the influence of channel resistance on the band gap extraction.

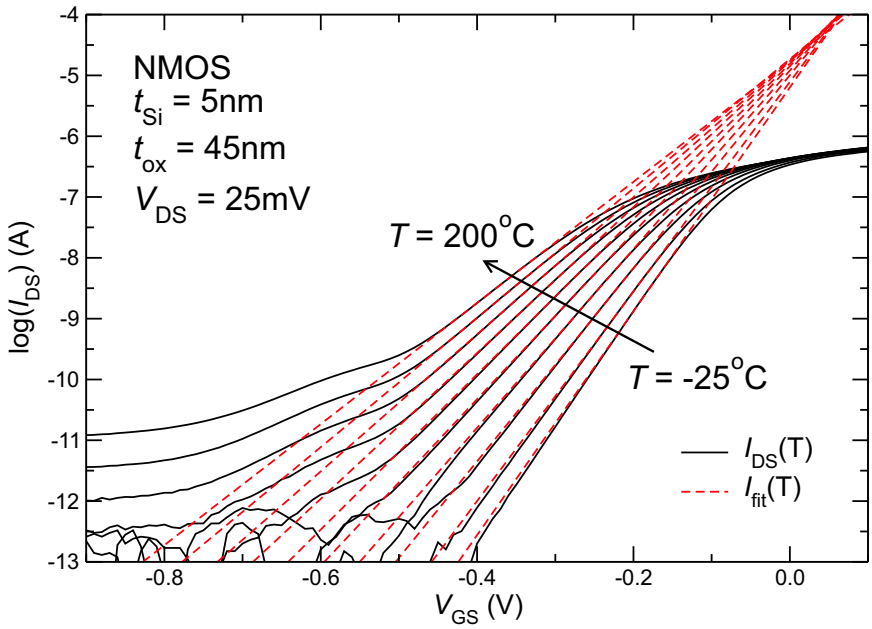


Figure 3.5: Temperature dependent $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ measurements on the thinnest NMOS device.

be distinguished in the plots: first the region above threshold in which the current starts to saturate and the series resistance (i.e. channel resistance) becomes visible. In this region, the current is limited by V_{DS} rather than V_{GS}. Then, entering the subthreshold region (i.e. increasing or decreasing V_{GS} for PMOS or NMOS resp.), the current clearly depends exponentially on the gate voltage (hence a straight line on logarithmic scale). This region will be referred to as the 'ideal' subthreshold region. Note however that the gate voltage at which the transition from above–threshold to sub–threshold occurs is strongly temperature dependent, making the range in which the subthreshold is 'ideal' fairly large at the lowest temperature whereas only a very small ideal subthreshold region can be observed at the highest temperature. Later on, values of the drain current are to be plotted versus the temperature, at a gate voltage being equal for all temperatures. Hence, one could run into problems when the ideal subthreshold region at the highest temperature starts beyond the point where the 'low temperature' subthreshold is already below the noise level (i.e. $I_{\mathrm{DS}} \leq 0.1\,\mathrm{pA}$). In order to overcome this potential problem, lines have been fit to the ideal subthreshold part, making extraction of $I_{\mathrm{DS}}(T)$ over a wider V_{GS}-range possible. In the last region, where $|V_{GS}| < 0.5\,\mathrm{V}$ or $V_{GS} < 0.5\,\mathrm{V}$ for PMOS and NMOS respectively, an additional effect shows up: the current starts to deviate from the ideal subthreshold curve. Since this effect is more pronounced for higher temperatures, it is very likely that the number of thermally generated charge

carriers is higher than the amount of gate induced inversion charge. This means that for the combination of high temperatures and low gate voltages, the gate is no longer able to control the total charge in the channel to the full extent, making the current less dependent on the gate voltage. As a result, the corresponding subthreshold slope will be weaker.

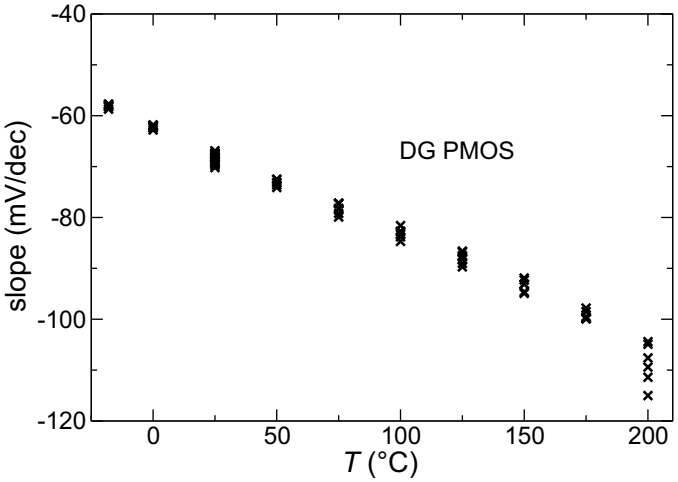
3.1.2 Accuracy

After having shown the typical temperature dependence of the subthreshold current, this section will deal with the accuracy and reproducibility of the experiments, starting with an overview of the measured devices in table 3.1. All devices have equal channel lengths, BOX layer thicknesses (400 nm) and equally thick gate oxide (15 nm). To the latter there are two exceptions, being the devices with *silicon* film thickness of 5 nm and 23 nm, for which t_{ox} equals 45 nm. However, this is still much thinner than the BOX layer thickness, so the assumption made in the first part of this chapter still holds. Furthermore, the silicon thicknesses of these supposedly 5 nm and 23 nm devices have not been determined more accurately yet, which explains the relatively large uncertainty in t_{Si} for these devices.

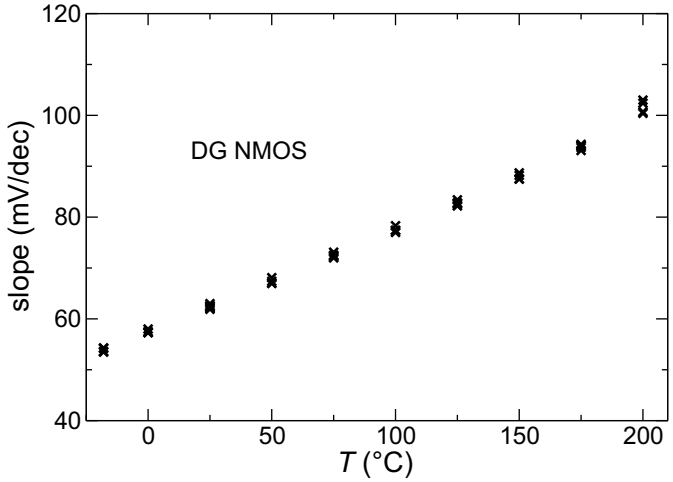
t_{Si} (nm)	Δt_{Si} (nm)	PMOS	NMOS
27.3	± 0.2	$\surd$	$\surd$
23.0	± 2.0	$\surd$	$\surd$
19.1	± 0.3	$\surd$	$\surd$
9.7	± 0.2	$\surd$	
5.15	± 0.25	$\surd$	
5.0	± 2.0	$\surd$	$\surd$

Table 3.1: All SOI DG devices of which the temperature dependent $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ curves have been measured. See also the appendix.

In order to examine the temperature depencence of the subthreshold slope and its spread across different devices, the slopes in the 'ideal' subthreshold region have been extracted and depicted in the figures 3.6a and 3.6b. Ideally, the slopes should be equal for all devices assuming that the silicon film is at least sufficiently thin for only one channel to exist. The plots clearly show that indeed the subthreshold slope is linearly proportional to the temperature, as could be inferred from eqs. (2.2) and (2.10). Moreover, since the subthreshold slope is defined as the voltage which is needed to increase the current by one decade, generally a low subthreshold slope is desired. Hence, the lower the subthreshold slope, the higher the ability of the gate to control the amount of inversion charge in the channel and thus the current. The clear linear temperature dependence shown in figure 3.6 reveals that, besides the temperature, no significant (physical) side effects do occur which could deteriorate the device behavior in subthreshold.



(a) PMOS



(b) NMOS

Figure 3.6: Subthreshold slopes vs temperature for all available (a) PMOS and (b) NMOS devices.

More quantitatively speaking, the devices show a nearly ideal slope: at room temperature the average slope is -68.5 mV/decade and 62.4 mV/decade for the PMOS and NMOS devices respectively. Furthermore, the spread throughout the entire temperature range is ±1.2 mV/dec for the PMOS. The NMOS spread is slightly smaller, ±0.6 mV/dec. The larger spread at the highest temperature is due to the fact that the ideal part of the subthreshold region is only very small, which makes fitting a line and extracting the corresponding slope slightly less accurate. But in general, the spread is negligibly small, to within the measurement accuracy.
In short, the above observations suggest that, as for the subthreshold slope, the devices show a nearly ideal intrinsic behavior with the expected temperature dependence.

As the devices will be measured across different wafers, devices with supposedly equal layer thickness might not exhibit the same behavior. In addition to this, each wafer consists of several devices with equal layer thickness. So, in order to get an idea of the process accuracy and to make a reasonable estimate of the spread which has to be taken into account, all devices were measured at least at room temperature. The resulting $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ curves are depicted in figure 3.7 for the PMOS devices with the thickest layer. The fig-

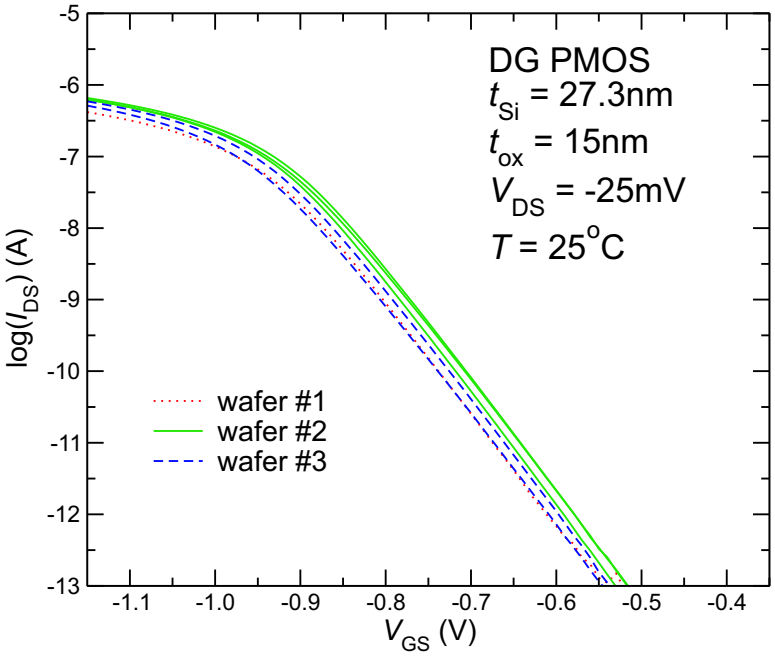


Figure 3.7: Shift along V_{GS}, obtained from the thickest DG PMOS device on different wafers. The layer thickness is determined accurately only for devices on wafer 2, on which the thickest device is 27.3 nm. Detailed information on device parameters and wafer numbers can be found in appendix B.

ure indicates that a reasonable spread across the devices occurs: the slopes are more or less equal (as described previously) but the curves are shifted along the V_{GS} axis. To illustrate this, the V_{GS} 'offsets' have been depicted in figure 3.8, showing a maximum shift of approximately 30 mV. Note that the measurements are very accurate and reproducible, so the observed spread surely is a device property, rather than a measurement uncertainty. The

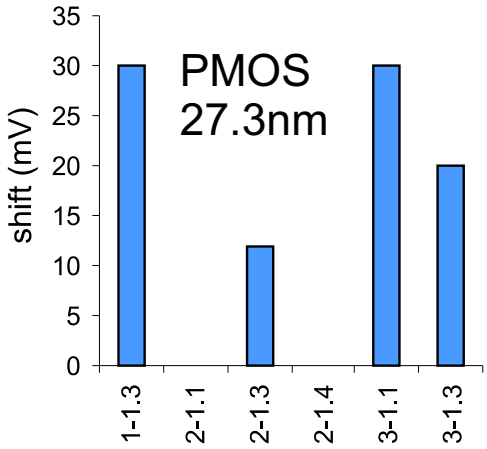


Figure 3.8: Shift in V_{GS} for the thickest PMOS device, for which t_{Si} = 27.3 nm on wafer 2.

shift along the V_{GS} axis could originate from a difference in silicon layer thickness, a difference in stress introduced during the oxidation, or a difference in work function. As for the first, the exact silicon layer thickness has only been determined for one single device for each layer thickness on one wafer (no. 2, see also appendix). So, the layer thicknesses on the other wafers may differ slightly, which could explain the observed V_{GS} shift. In addition to this, the layer thickness can also vary from device to device on the same wafer. This is sustained by the plot, which shows that a V_{GS} shift also occurs between devices located on the same wafer. However, currently the layer thicknesses have not been measured for all devices, which makes drawing definite conclusions about the exact origin of the V_{GS} shift not trivial at all. Especially as there is also a possible work function difference across the devices, which directly results in a change in the gate voltage needed to obtain the same level of inversion, according to eqs. (2.1) and (2.4).
Moreover, it is very likely that during e.g. the oxidation steps stress is introduced, which locally changes the lattice constant thereby modifying the band structure. The resulting change in effective band gap leaves the slope unaffected, but appears as a shift along V_{GS} instead. Consequently this could contribute to the observed spreading.
Summarizing, one can conclude from the above considerations that in the extraction of the effective band gap a reasonable error has to be taken into

account, which amounts to approximately ±15 mV for the thickest devices. Likewise, this uncertainty has been calculated for the other devices, the plots of which can be found in appendix A.

3.1.3 Effective band gap extraction

Now that an estimate of the measurement and device accuracy is obtained, this section will finally present the results of the effective band gap extraction. As already stated in section 2.5 the increase in effective band gap can be extracted from the slope of I_{rat}, which is the ratio of the current in a relatively thick and a thin device. However, before doing that, figure 3.9 is given to illustrate the temperature dependence of the current. The values of I_{DS} have been taken at $V_{\mathrm{GS}} = 0.7\,\mathrm{V}$ and correspond to the intersections of the black dashed line and the $I_{\mathrm{DS}}(T)$ curves in the inset (see also fig. 3.4). The plot clearly demonstrates the truly exponential relation between I_{DS}

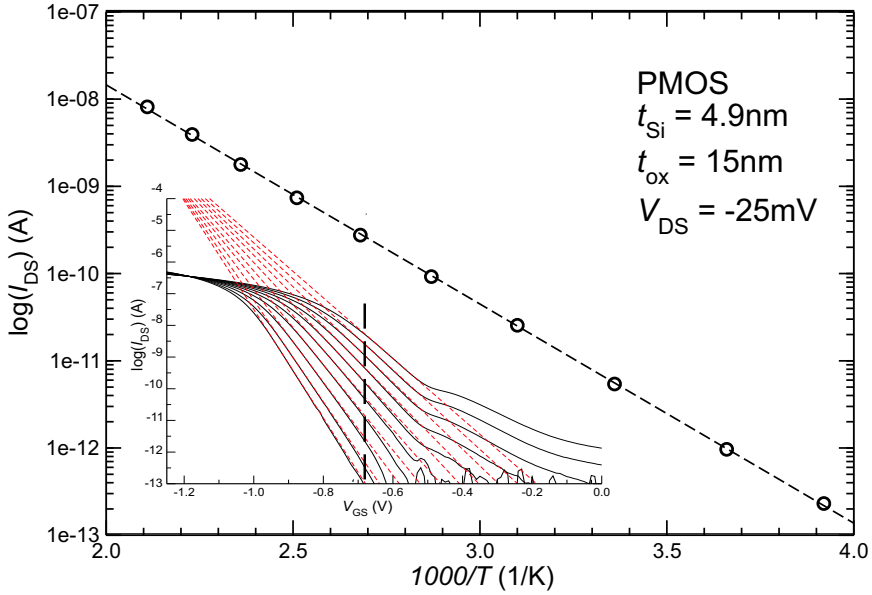


Figure 3.9: $I_{\mathrm{DS}}(T)$ at $V_{\mathrm{GS}} = -0.7\,\mathrm{V}$ (see inset) for DG PMOS with $t_{\mathrm{Si}} = 4.9\,\mathrm{nm}$. All data points are almost perfectly on the exponential regression line (dashed line), except for the two outermost points, which show a small deviation.

and the inverse temperature: on a logarithmic scale the curve is almost perfectly linear. Similar to the temperature depencence of the slope, one can conclude that no additional effects show up, thereby suggesting that the results obtained with this experiment are quite reliable.
In order to extract the increase in effective band gap, I_{rat} has been depicted for all PMOS devices in figure 3.10. The thickest device serves as the ref-

erence, because its silicon layer is assumed to be sufficiently thick so that no quantum confinement, hence no band gap widening, occurs. This plot

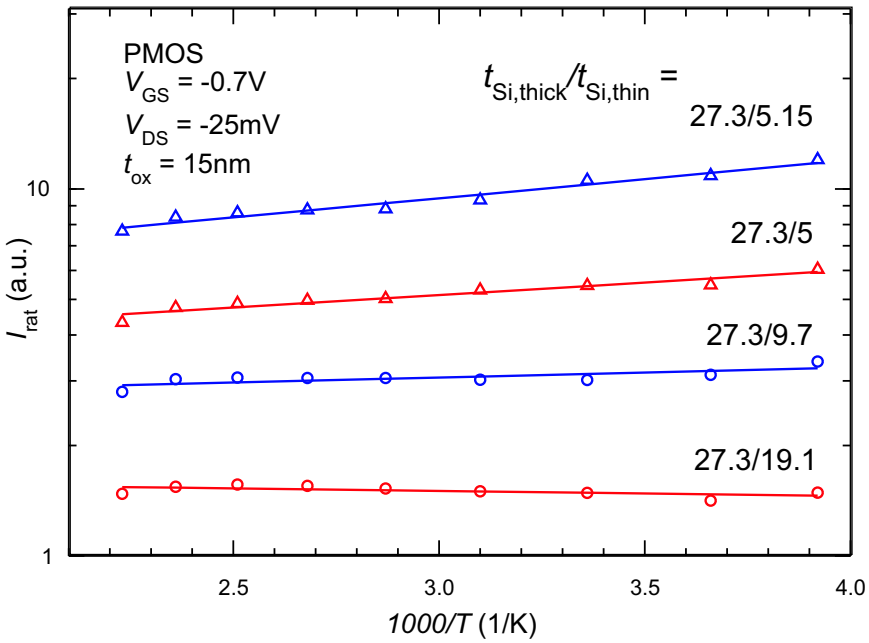


Figure 3.10: $I_{\text{thick}}/I_{\text{thin}}$ ($= I_{\text{rat}}$) vs temperature, for the DG PMOS devices with the 27.3 nm device as reference. Note that I_{rat} increases for thinner layers, which is either due to a lower mobility or a reduced DoS. The layer thickness of the 5 nm device is given with ± 2 nm accuracy, and t_{ox} of this device is 45 nm.

deserves a few remarks.
First of all, the figure indicates that in general indeed the slope of I_{rat} increases with decreasing layer thickness. Furthermore, the slope of I_{rat} is clearly positive for the two thinnest devices, meaning that the effective band gap widens. However, I_{rat} of the 5 nm device is smaller than I_{rat} for the device with 5.15 nm layer thickness. This could be explained by recalling that the layer thickness of the 5 nm device is given with ± 2 nm accuracy which makes the '5 nm' label rather misleading. Instead, the supposedly 5 nm device will probably be thicker, given the lower I_{rat} compared to the 5.15 (± 0.2) nm device.
Furthermore, I_{rat} is essentially constant for the 9.7 nm device, except for the data points at the lowest and highest temperature, which give rise to a slightly positive overall slope. In addition to this, the ratio of the current in the 27 nm and 19 nm device even shows a negative slope, which corresponds to an effective band gap narrowing. However, based on the theory one would expect either an enlarged band gap or no change in the width of the band gap at all, rather than a smaller band gap (assuming intrinsic or

lightly doped devices). Hence, as already pointed out before, in absence of quantum confinement the offsets of the conduction and valence band vanish, making the band gap equal to the one in bulk silicon. So, when comparing devices with layer thicknesses above the 'critical quantum confinement thickness' (i.e. $\approx 15\,\mathrm{nm}$), a possible modulation of the band gap width can not be attributed to quantum confinement related effects. Instead, as already discussed in the previous section, the IV measurements across devices with supposedly equal layer thickness do not fully coincide, but show a significant spread along the V_{GS} axis. At this point errors are introduced, since the $I_{\mathrm{DS}}(T)$ graphs (figs. 3.4 and 3.10) have been obtained at equal gate voltage (i.e. $-0.7\,\mathrm{V}$ and $-0.35\,\mathrm{V}$ for PMOS and NMOS devices respectively). Of course, compensation for the spread among the devices is possible, but this makes interpretation of the results even more involved since the spread is in the same order of magnitude as the expected widening of the band gap. Furthermore, the exact source of the observed spread can only be speculated about, so the validity of this step might be questionable.
The second note concerns the slight deviation of the data points. Although the points in e.g. figure 3.9 were virtually all perfectly on a straight line, as were the $I_{\mathrm{DS}}(T)$ graphs of the other devices (not shown), plotting the ratio of the currents results in data points which are slightly off the ideal straight line. Hence, the division operation gives rise to an amplification of the errors. Similar to the suggestion in the previous note, one could first fit a line through the single device $I_{\mathrm{DS}}(T)$ graphs, and then observe the ratio of the thus obtained perfectly linear curves. Obviously the resulting $I_{\mathrm{rat}}(T)$ curves will be perfectly linear, but the (increase in) band gap is of course equal to the one obtained with the first method. Nevertheless, extracting the effective band gap using the first method is preferred, because the uncertainty in the measurements remains visible.

When the above procedure is repeated for all devices, figure 3.11 is obtained, showing the effective band gap versus the silicon layer thickness. The change in effective band gap, $\Delta E_{\mathrm{g,eff}}$, has been extracted by multiplying the slope of I_{rat} with 2k/q. Note that in fig. 3.11 the effective band gap is given, which can be calculated by offsetting the experimental values of $\Delta E_{\mathrm{g,eff}}$ with $1.12\,\mathrm{eV}$, i.e. the band gap of bulk silicon. The theoretical values are depicted as well, and have been calculated with equation (2.24) assuming both hole and electron confinement as given by eq. (2.22). Furthermore, the error bars along the $E_{\mathrm{g,eff}}$ axis stem from the V_{GS} shift of $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ as described previously. Some points have a fairly large uncertainty in t_{Si}, as those thicknesses have not yet been determined more accurately with TEM analysis. Moreover, note that as for the extracted effective band gap no distinction can be made between hole and electron confinement as either type of confinement occurs in both PMOS and NMOS devices. So, sorting the data by device type has a practical purpose, rather than a physical rel-

evance.

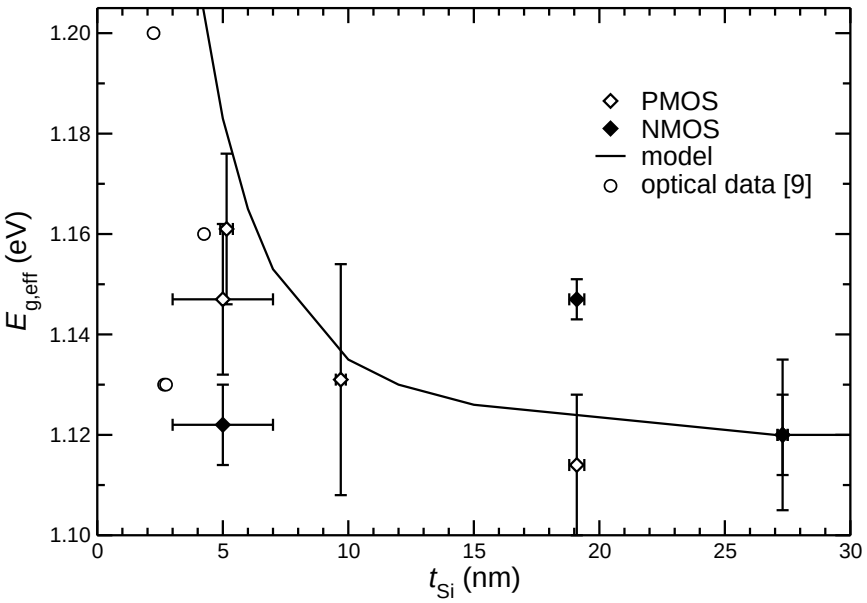


Figure 3.11: Change in effective band gap, extracted from the slope of I_{rat}.

The figure demonstrates that in the PMOS devices with t_{Si} below 10 nm the band gap widens. However, taking into account the fairly large uncertainty particularly in the vertical direction, interpretation of the results is restricted to only a rather qualitative analysis. Nevertheless, the general trend indicates that the effective band gap is very likely to increase for decreasing silicon film thickness. Due to the limited number of available devices (see also Appendix B) and in particular the large spreading in $\Delta E_{\mathrm{g,eff}}$, no definite conclusions can be drawn at this regard. Furthermore, the 19 nm NMOS device exhibits a larger increase in band gap than does the device with supposed thickness of 5 nm. This issue could be related to stress, which possibly has been introduced during the oxidation steps in the process. Also, damage due to the implantation of arsenic could be a possible reason for the different behavior of the NMOS devices. As shown in the next section, this is conjecture is sustained by the CV measurements.
In addition to the results of this work, optical data obtained from [11] are depicted in the same figure, showing that the increase in effective band gap observed with the electrical and optical experiments are more or less in agreement.
Based on the above results one could state that temperature dependent IV measurements can be used to characterize devices and particularly for observing quantum mechanical effects such as a widening of the effective band gap. As the proposed method relies on the comparison of different devices, the results are inherently prone device spreading due to process variations.

Hence, in order to experimentally verify the theoretical relation between the silicon layer thickness and the widening of the effective band gap, devices fabricated in a more accurate process are required.

3.2 *CV* measurements

This section will present the results of the *CV* measurements. Similar to the previously described *IV* measurements, they aim for a comparison of the electrical characteristics of a 'thick' and a thin device, in which the latter is expected to exhibit a widening of the band gap due to spatial carrier confinement. Theoretically, as already pointed out in (2.28), the effective band gap can be extracted from the strongly temperature dependent subthreshold slope, i.e. the onset of inversion. In practice however, this procedure is not that straightforward, so this section mainly deals with the description of the measurement procedure and the complications involved.

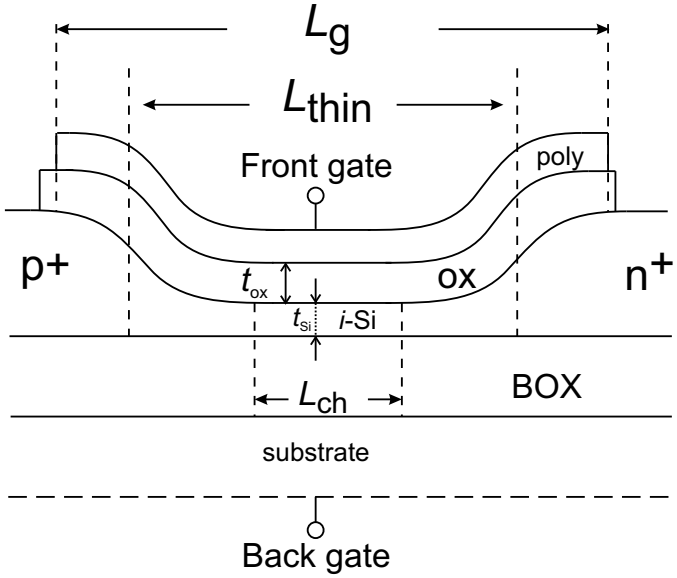


Figure 3.12: Schematic cross-section PiN diode, showing the (lateral) device dimensions.

The *CV* measurements have been carried out on so-called PiN diodes, of which a schematic cross section is given in fig. 3.12. These devices consist of a p^+-type and a n^+-type region while the actual channel region is (nearly) intrinsic or, to be more precise, lightly p-type doped. Such a structure allows for the hole and electron inversion charge to be measured separately. As for the channel region, devices with a layer thickness (t_{Si}) of 5 nm and 23 nm are available. Furthermore, all devices have a width of 60 μm but there is a variation in available channel lengths, ranging from approximately 10 up

to 60 μm. However, as depicted in fig. 3.12, three different lateral device dimensions have been defined: L_{g}, which is the length of the gate; L_{thin}, the distance between halfway the slopes of the thinned down regions, and finally the length of the actual channel region which is denoted with L_{ch}. The corresponding values are given in table 3.2.

L_{g}	L_{thin}	L_{ch}	$L_{\mathrm{g}} - L_{\mathrm{ch}}$
15	14	10	5
28	24	20	8
35	33.5	27.5	7.5
42	44	36	6
56	54	48	8
62	64	55	7

Table 3.2: Lateral device dimensions in (μm) of the available PiN diodes.

The table shows that the length of the transition region from the 'thinned' channel to the 'unthinned' p^+ or n^+ region (denoted with $L_{\mathrm{g}} - L_{\mathrm{ch}}$) differs significantly from device to device. As particularly the CV characteristic of the channel region is of interest and the transition region is considered as a parasitic capacitance, ideally devices should be chosen with equal transition region length, to make the results generally better comparable. In addition to this, differential CV measurements will be carried out to eliminate the influence of parasitics thus obtaining the 'most' intrinsic behavior, as was described in chapter 2. This results in the need for devices with at least three different channel lengths for each layer thickness. Moreover, the influence of a possible deviation in the channel length will be less for longer channels, thereby posing yet another requirement on the selection of devices. Combining the above considerations, it turns out that the devices with L_{ch} of 20, 27.5 and 48 μm should be used. The slightly shorter transition region of the 27.5 μm device compared to the 20 μm and 48 μm devices could be an issue, as will be described in the course of this section.
One note concerning the frequency used for the CV measurement. A series of test measurements was carried out at different frequencies by means of a check, but the influence of the frequency on the results was found to be negligible for frequencies above approximately 10 kHz. In the results presented in this section the frequency is 100 kHz.

3.2.1 Single *CV* measurements

The discussion of the CV measurements starts with figure 3.13 and 3.14, respectively showing the total capacitance of the above mentioned devices with $t_{\mathrm{Si}} = 5$ nm in case of p-type and n-type inversion. Note that, unlike the IV measurements, the presented CV measurements have been carried out in SG mode (i.e. front gate sweeping and back gate at 0 V). There are

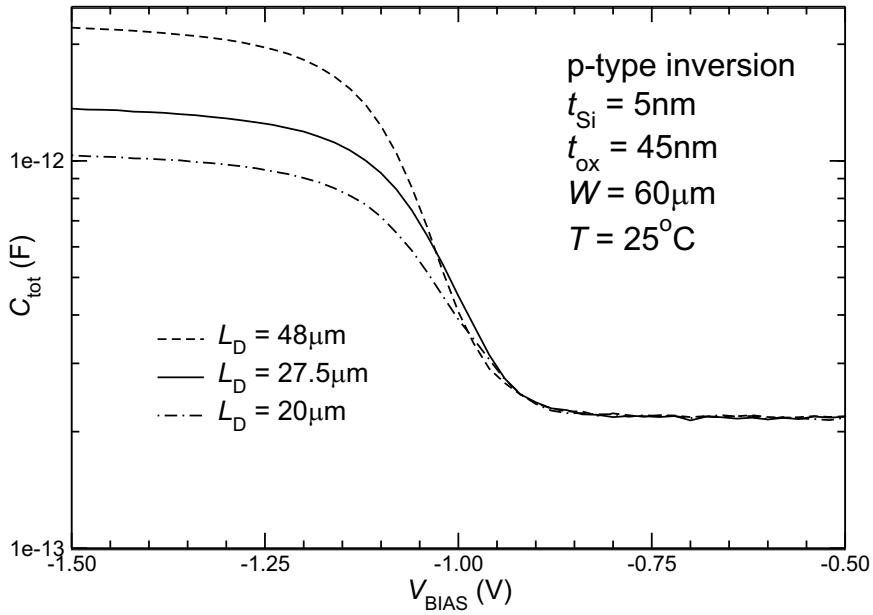


Figure 3.13: Single CV measurement (hole inversion) on PiN diodes with L_{D} 20, 27.5 and 48 μm.

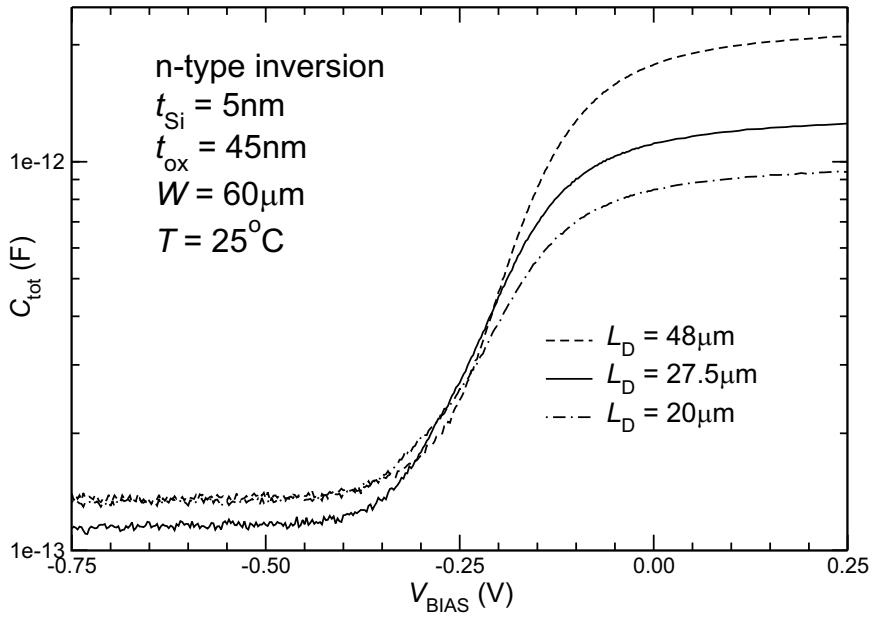


Figure 3.14: Single CV measurement (electron inversion) on PiN diodes with L_{D} 20, 27.5 and 48 μm.

quite a few things to comment on these plots.

First of all, the 27.5 μm device shows an electron depletion capacitance which is systematically lower than the electron depletion capacitance of the 20 and 48 μm device. This difference is also observed in the devices with t_{Si} equal to 23 nm. Despite the fact that the strong inversion capacitance and in particular the weak inversion region are of greater importance, the observed difference in depletion capacitance may suggest that not all devices are fully equal (except for the wanted variations in L_{ch} and t_{Si}). In fact, as can be seen in table 3.2, the difference between L_{g} and L_{ch} (in the remainder denoted with L_{eff}) in the 27.5 μm device is smaller than L_{eff} in the 20 μm and 48 μm devices. The resulting shorter transition region of the 27.5 μm device could explain the observed difference in depletion capacitance, as the latter is dominated by the highly doped regions. This will be verified with simulations in section 3.2.3.
The second issue concerns the weak inversion region, that is the region in which the capacitance increases with the bias voltage according to an exponential fashion. The plots clearly show that the curves cross in the weak inversion region. Moreover, the devices differ in the point at which weak inversion starts. This could be due to the rather poorly defined transition in the silicon layer from highly doped n^+ or p^+ region to the actual channel: it is likely that doping atoms have diffused into the channel region, the amount and the extent of which may vary from device to device. Hence, the 'diffusive' transition from depletion to weak inversion is strongly determined by the dopant implantations. This could as well explain the fact that the weak inversion region exhibits a truly exponential behavior in only a very small range with rather smooth transitions from the exponential part to the depletion and strong inversion region. As a result of the above observations, one cannot extract the subthreshold slope without ambiguity.
As a last point of comment on figures 3.13 and 3.14, the capacitance in strong inversion is considered. The strong inversion capacitance (denoted with C_{inv}) consists of a contribution of the channel region, which scales with L_{ch}, and a parasitic capacitance (C_{par}) stemming from the p^+-type and n^+-type implanted regions. The resulting strong inversion capacitance can then be described by

$$C_{\mathrm{inv}} = C_{\mathrm{int}} L_{\mathrm{ch}} W + C_{\mathrm{par}} \tag{3.1}$$

with C_{int} the capacitance of the channel region per unit area (recall also eq. (2.29)) and W the width of the device. In order to determine C_{par}, C_{inv} has been depicted versus L_{ch} in figure 3.15 for both the hole and electron inversion.
The plot shows a nicely linear dependence of C_{inv} on L_{ch}, thereby allowing for estimating the parasitic capacitance according to eq. (3.1). Hence, the parasitic capacitance for hole and electron inversion ($C_{\mathrm{P,par}}$ and $C_{\mathrm{N,par}}$

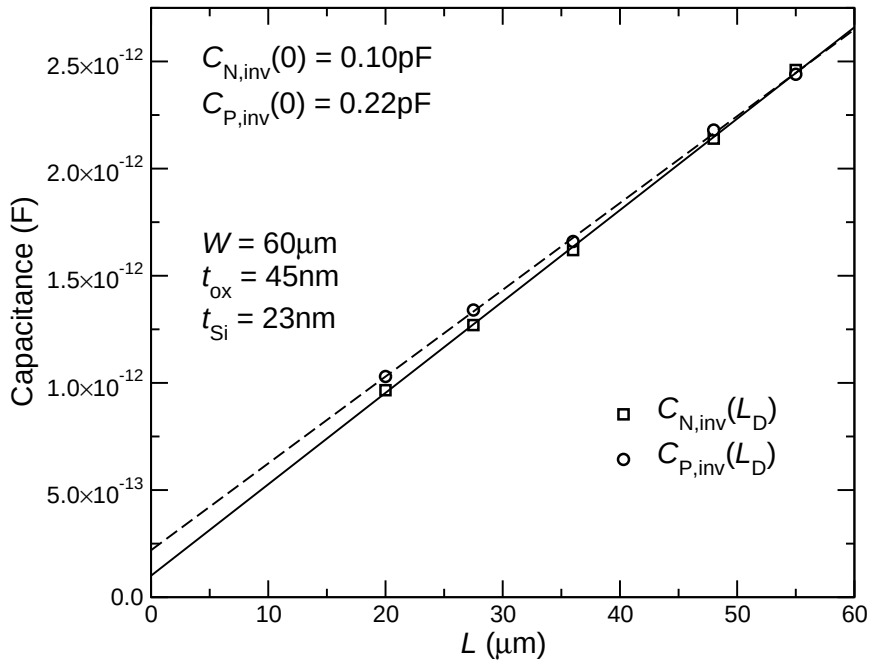


Figure 3.15: The hole ($C_{\mathrm{P,inv}}$) and electron ($C_{\mathrm{N,inv}}$) capacitance in strong inversion vs L_{ch}, demonstrating a clearly linear relation between C_{inv} and L_{ch}. The parasitic capacitances ($C_{\mathrm{P,par}}$ and $C_{\mathrm{N,par}}$ for holes and electron resp.) can be obtained by extrapolating the curves to $L_{\mathrm{ch}} = 0\,\mu$m, giving $C_{\mathrm{P,par}} = 0.22\,\mathrm{pF}$ and $C_{\mathrm{N,par}} = 0.10\,\mathrm{pF}$.

resp.) is given by $C_{\mathrm{P,inv}}$ and $C_{\mathrm{N,inv}}$ at $L_{\mathrm{ch}} = 0\,\mu$m, being 0.22 pF and 0.10 pF respectively. Note that the thus obtained values for C_{par} are only those parts of total parasitic capacitance which are located in the channel region (i.e. underneath L_{ch}), probably due to diffusion of implanted impurities into the channel region; in addition to these contributions, the total parasitic capacitance consists of the parasitics of the implanted regions. As already suggested in section 2.5.2 and sustained by the apparent occurrence of parasitics in the channel region, differential measurements could help to reduce the influence of parasitics.
Before discussing the differential measurements, some single CV measurements at different temperatures are depicted in fig. 3.16. The figure illustrates the temperature dependence of the capacitance measured on the $48\,\mu$m and $20\,\mu$m device. At the highest temperature, the capacitance in strong inversion increases due to the thermally generated electrons. This effect was also observed in the IV measurements (e.g. figure 3.5). As a result, the ability of the gate to control the charge is reduced, which shows up in the device characteristics (in the IV and the CV measurements) as a weaker subthreshold slope for higher temperatures. Furthermore, the increase in depletion capacitance is higher than the increase of the capacitance in strong inversion. This can be explained by noting that the highly doped regions, which dominate the depletion capacitance, exhibit a different temperature dependence compared to the intrinsic channel region, which determines the capacitance in strong inversion.
As for the channel length, the plot shows that the longest device is less sensitive to an increase in temperature than is the shortest device. Though the difference is modest, the longest device shows a smaller increase in strong inversion capacitance. In addition to this, the longest device generally exhibits a steeper subthreshold slope, suggesting that the influence of the 'diffusive' transition region decreases for increasing channel length. This is confirmed by the previously described figure 3.15. Hence, in order to reduce the influence of the parasitics due to the implanted and diffusive regions, devices with very long channels should be measured, so as to achieve device behavior which is as 'intrinsic' as possible.

3.2.2 Differential *CV* measurements

As indicated in the previous section and in eq. (2.29), differential measurements can be used to minimize the influence of the parasitics. Therefore, from now on only differential measurements will be considered, with the $48\,\mu$m device as reference. Ideally, subtracting the CV measurements of two devices with different channel length should result in the CV characteristic of the intrinsic region, that is without the parasitics. Such a differential measurement is shown in figure 3.17, depicting the hole and electron inversion at room temperature, for the devices with t_{Si} equal to 5 nm and channel

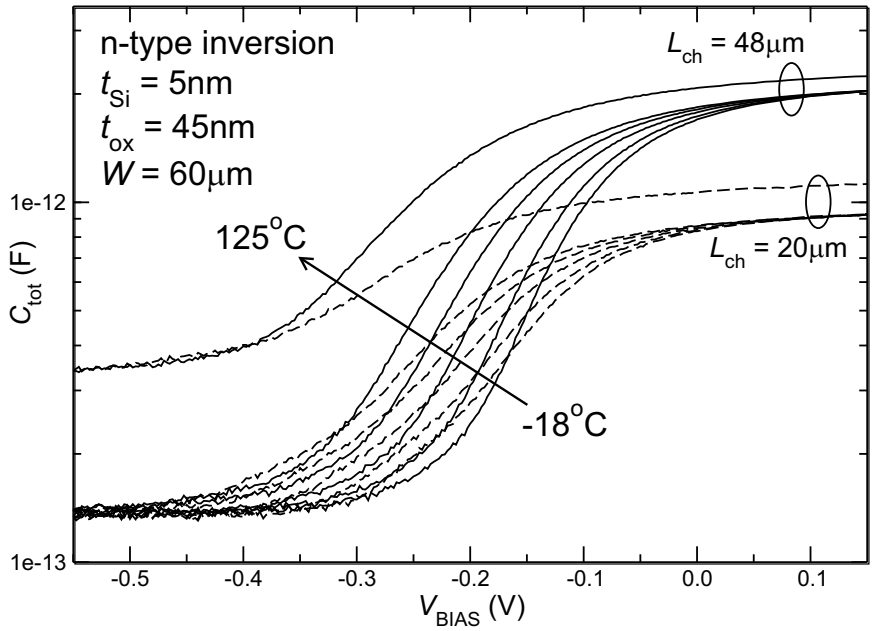


Figure 3.16: Single CV measurement (n-type inversion) at $T = -18, 0, 25, 50, 75, 125\,(^{\circ}\mathrm{C})$, demonstrating the different temperature dependence of the implanted regions (dominant in depletion region) and the intrinsic channel region (dominant in strong inversion).

lengths equal to 27.5 μm and 20 μm. Note that the capacitance is given in (F/μm^2), hence normalized on the area (WL_{ch}). The figure demonstrates

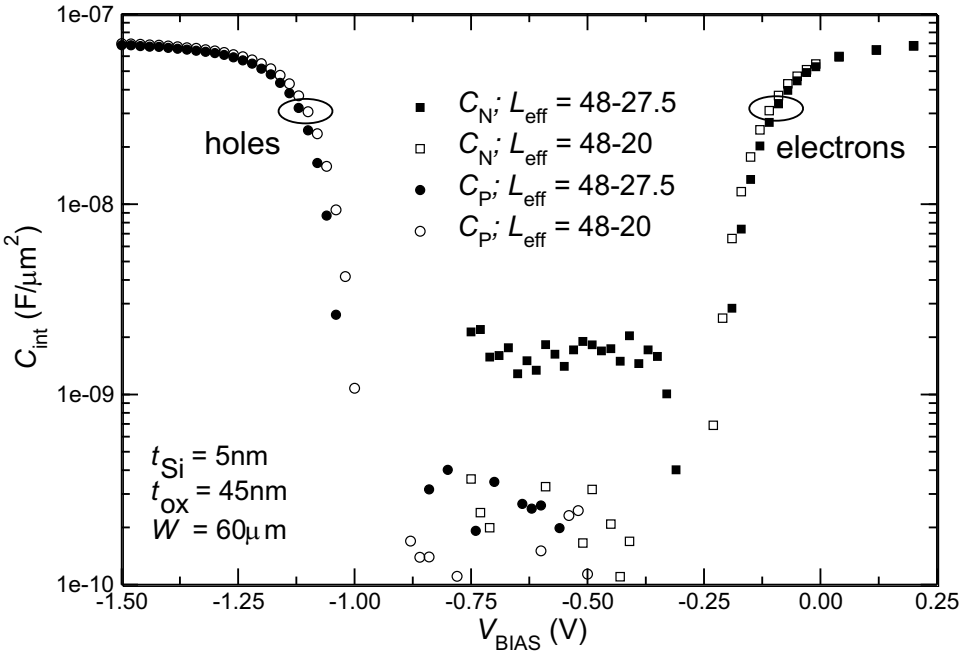


Figure 3.17: Differential CV measurement, showing the electron and hole inversion at room temperature. L_{eff} is given in (μm).

that the curves of the two devices nicely coincide when strong inversion is reached, as one would expect for the normalized capacitance. The difference in inversion capacitance is less than 1%. Furthermore, the lower depletion capacitance of the 27.5 μm n-type inversion (see fig. 3.14) clearly results in a differential depletion capacitance which is far above the depletion capacitances of the other devices, thereby effectively rising the 'noise floor'. This means that only a very limited range of the actual subthreshold region can be used. In addition, the transition from depletion to strong inversion is quite steep and occurs in a fairly small V_{bias} range: subtraction of two 'single' CV measurements, both of which show a very steep subthreshold region, results in a differential CV characteristic having only a few data points in the region of interest. Of course, the resolution of the measurements can be increased to obtain a higher accuracy in the subthreshold region (which has been done in the subsequent figures), but fitting a line and extracting accurately the corresponding subthreshold slope remains quite problematic.

This issue is even more apparent for higher temperatures, as is illustrated in figure 3.18, depicting the electron inversion versus gate bias at -18, 25 and 125°C. Clearly, increasing the temperature gives a shift of the CV curve in

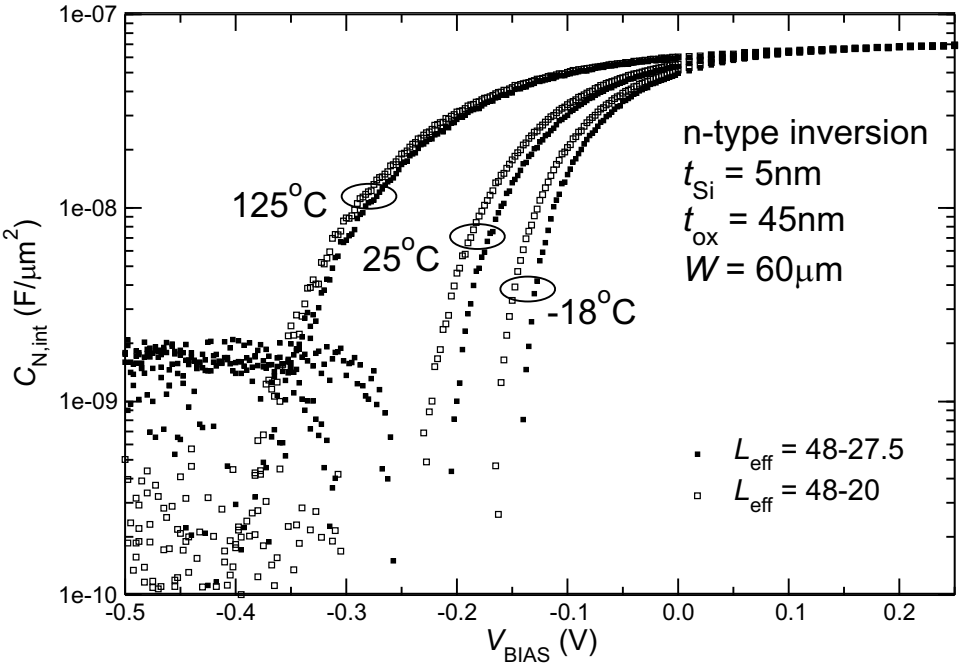


Figure 3.18: Differential CV measurement (n-type inversion) for $T = -18, 25, 125$ (°C).

the negative V_{bias} direction. The high temperature results in a larger amount of thermally generated charge (see also figs. 3.16 and 3.5), thereby lowering the gate voltage at which inversion is reached. Also, a band gap *narrowing* due to the high doping level of the regions adjacent to the intrinsic channel could explain the observed shift in V_{bias} because, as was also demonstrated in fig. 3.16, the implanted regions are very likely to dominate the depletion and subthreshold region particularly for the shortest devices.
Besides the shift in V_{bias}, figure 3.18 shows that the subthreshold region is more affected by noise when the temperature is increased, making extraction of the subthreshold slope less accurate. In addition to this, the slope varies continuously with the gate voltage, which makes it difficult to define the actual subthreshold region without ambiguity. These effects can be attributed to the dominant behavior of the highly doped regions as well.

In short, the combination of a rather steep and noisy transition region, a small range from which the slope could be determined and the strong temperature dependence of the V_{bias} shift, drastically reduces the accuracy of the CV measurements.

The influence of the silicon layer thickness is depicted in figure 3.19, showing the differential (n-type) capacitance and the inversion charge for t_{Si} equal

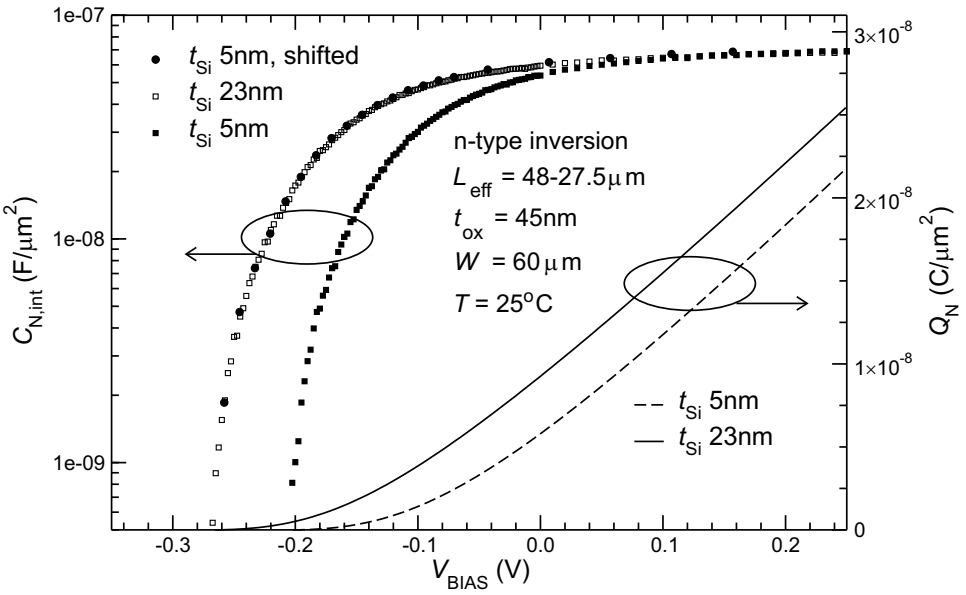


Figure 3.19: Differential n-type capacitance and inversion charge for t_{Si} equal to 5 nm and 23 nm. The solid circles denote the shifted characteristic of the 5 nm device.

to 5 nm and 23 nm. The shifted curve of the 5 nm device appears to coincide completely with the 23 nm curve. Hence, apart from the bias level, no significant t_{Si} related effects are noticeable. The same holds of course for the inversion charge density, which has been calculated by integrating the capacitance. Thus, at a given gate bias, the inversion charge density in the 23 nm device is higher than in the 5 nm device. This can be explained by noting that the total inversion charge increases with t_{Si}, as can be seen in e.g. equation (2.21) and figure 2.2. Likewise, the capacitance in the weak inversion region depends on $n_{\mathrm{i}}t_{\mathrm{Si}}$ as was described with eq. (2.28).

3.2.3 Simulations

As mentioned previously, the experimental CV data exhibits only a very small and noisy region in which the slope is approximately constant, making a quantitative interpretation of the results rather inaccurate and demonstrating a potential band gap widening effect even impossible. So, to find an adequate explanation for the observed behavior, a comparison with theoretical data is appropriate. Section 3.2.1 already suggested that diffusion of dopant atoms from the highly doped region into the channel region could be a potential source of non-idealities. Additionally, the heavily doped regions will most probably differ significantly in temperature dependent behavior from the intrinsic region. To verify these conjectures, some simulations have been carried out for devices with and without a diffusive transition region

from the heavily doped regions to the channel [12]. The results are depicted in figure 3.20. Although the device geometry is not fully equal to the actual available devices (10, 30 and 50 μm gate length), the simulations are certainly useful for determining the origin of the measured non-ideal behavior. Note that the silicon film is relatively thick (20 nm), as the simulation only employs classical models (i.e. no quantum mechanical effects incorporated).

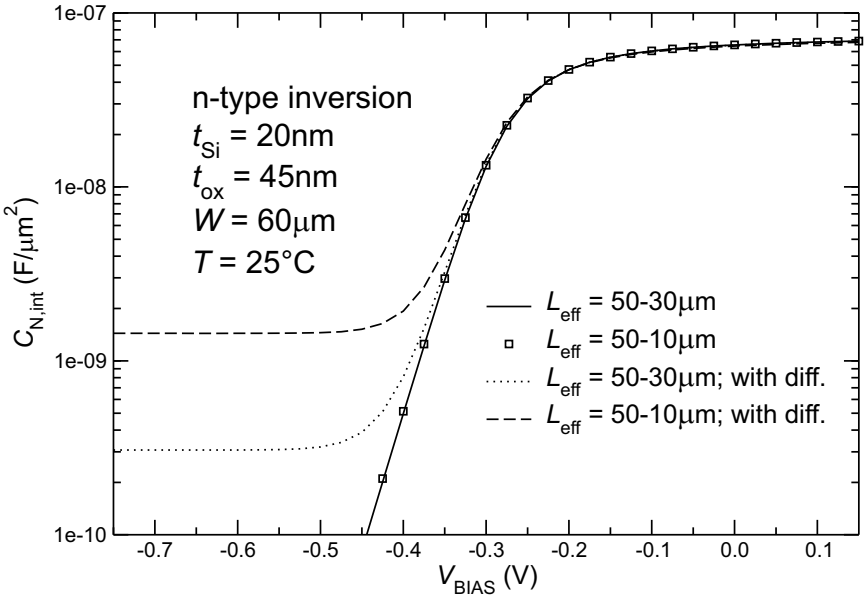


Figure 3.20: Simulated CV characteristic (n-type inversion) with and without 'diffusive' junctions, clearly showing that the diffused dopants strongly affect the depletion capacitance. The difference between long devices should be observed to reduce the influence of the diffusive junctions.

The solid line and open symbols denote the differential characteristics of the ideal devices with a perfect junction, i.e. an abrupt transition from the highly doped regions to the intrinsic channel region, whereas the dashed lines depict the simulation data incorporating diffusive transition regions. The plot clearly demonstrates that in absence of dopant diffusion into the channel region the characteristics with unequal effective channel length (L_{eff}) completely coincide, in contrast to e.g. the curves in fig. 3.18 which do coincide in strong inversion but show a reasonable deviation in the subthreshold region. Since the simulated devices are fully equal except for the channel length, the effect of the parasitics is perfectly cancelled thereby obtaining the capacitance of the intrinsic region only. Obviously, in practice the devices are not perfectly identical but suffer from process variations, which could explain the observed deviation in the subthreshold region.
Moreover, the simulations reveal that indeed the diffusive transition region

could be responsible for the scattered points in the depletion region. The depletion capacitance significantly rises for increasing effective area (WL_{eff}). This severely limits the range of the subthreshold, and additionally results in a significant weaker slope: both ideal devices exhibit a slope of 67 mV/dec, while the 50-30 μm and 50-10 μm 'diffusive' devices show 77 mV/dec and 96 mV/dec respectively. Hence, to reduce the effect of the highly doped and diffusive regions as much as possible, devices with very long channels should be used.
Furthermore, in order to investigate the temperature dependence of the highly doped regions, additional simulations should be run at different temperatures.

To stress the limited accuracy of the experimental CV results, the subthreshold slopes have been extracted at temperatures ranging from -18°C up to 125°C (figure 3.21, n-type inversion). After all, the aim was to compare the exponential part of the CV characteristics for a thick and thin device as function of the temperature, in order to observe an increase in the effective band gap. A plot of the slope versus the temperature gives a reasonable indication of the absolute uncertainty in the measurements (compare figure 3.6). Unlike the IV measurements, the slopes for the CV measure-

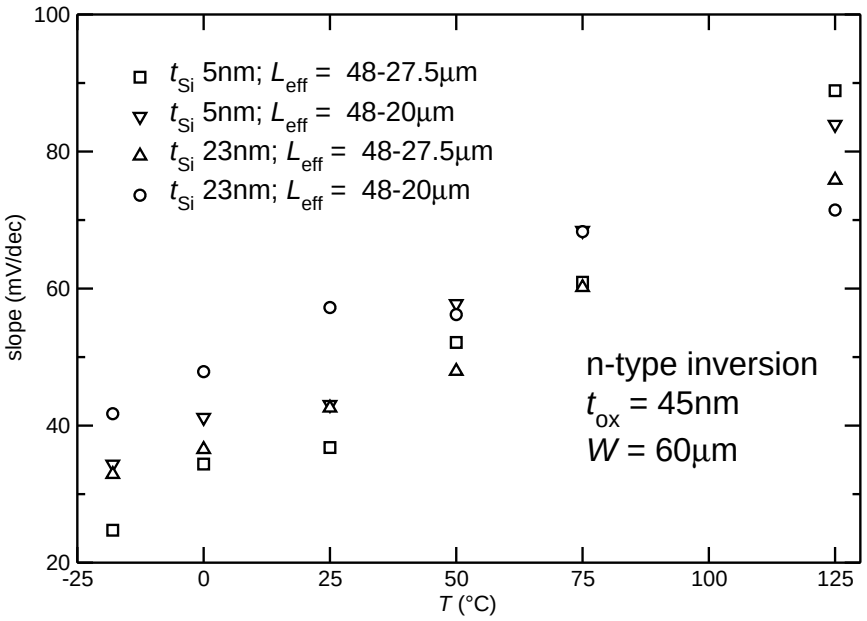


Figure 3.21: Subthreshold slope vs the temperature (n-type inversion). Extracted using $C_{\text{min}} = 2.3\,\text{nF}/\mu\text{m}^2$ and $C_{\text{max}} = 5.5\,\text{nF}/\mu\text{m}^2$.

ments cannot be obtained at a gate voltage equal for all devices, due to the strongly temperature dependent V_{bias} range. By means of a work-around,

the range in which the slope is extracted has been specified in terms of capacitance, rather than gate bias, so as to compare the slopes of all devices. Figure 3.21 readily shows a large spread across the devices, though one can infer that the slope is linearly proportional to the temperature. However, as for a quantitative comparison or even extraction of the effective band gap, the accuracy of these experimental data is clearly not sufficient.

Summarizing the above findings, one could state that the band gap widening effect cannot be observed based on the currently present experimental CV data. The measurements suggest that, particularly for shorter devices, the highly doped regions and diffusive junctions dominate the device behavior rather than the intrinsic channel region. This can be observed in the weak inversion region, which is rather steep and affected by noise. Furthermore, simulations show that also the high depletion capacitance can be attributed to the diffusive junctions.
Moreover, the highly doped p^+ and n^+ regions are very likely to differ in their temperature dependence from the intrinsic channel, due doping induced band gap narrowing. This is to be confirmed with additional simulations at different temperatures.

Chapter 4

Conclusions

This project aimed at observing the effective band gap widening effect using electrical measurements. To this purpose, SOI based n-type and p-type devices are available with several silicon layer thicknesses. By comparing the temperature dependent characteristics of these devices a widening of the effective band gap is expected to become apparent, as explained in chapter 2. The enlargement of the band gap stems from the modification of the band structure for semiconductor films with thickness less than approximately 15 nm due to spatial confinement of the charge carriers. Note that quantization of both the conduction *and* the valence band occurs, because the double gate structure results in *two* confining barriers. In order to investigate the band gap widening effect, two types of measurements have been proposed, both of which rely on the comparison of a relatively thick device and a device of which the silicon layer is sufficiently thin for quantum confinement to occur. Furthermore, this project focusses on the subthreshold current, in which diffusion is the dominant transport mechanism. In the measurements the temperature is an important parameter, as diffusion is strongly temperature dependent. The results of the measurements will be summarized briefly below.

***IV* measurements** Only rather qualitative conclusions can be drawn based on these results, given the limited accuracy of the process and consequently the unwanted variations among the devices. Nevertheless, keeping this in mind, the IV measurements on the available devices nicely serve as a proof of concept, showing that observing the band gap widening effect by means of this type of electrical measurement is possible. The results indicate that the effective band gap is likely to increase for decreasing silicon layer thickness. For a detailed quantitative analysis however, the measurements should be repeated on devices with thinner layers, fabricated in a more accurate process. Furthermore, a larger number of devices should be measured to allow for an accurate statistical analysis of the experimental data.

***CV* measurements** As for observing the effective band gap widening effect using CV measurements, the device behavior is dominated by the highly doped regions adjacent to the channel region. These regions are likely to have a temperature dependence different from the intrinsic region, caused by band gap narrowing due to the high doping levels. The influence of the highly doped regions on the overall device behavior is stronger in devices with short channels. This suggests that very long channel devices should be measured to reduce the dominant behavior of the highly doped regions as much as possible.
Moreover, the experimental data is depicted differentially, which ideally should eliminate the influence of parasitics and the highly doped regions. However, this procedure assumes fully identical devices except for the intrinsic channel length, for the parasitics to be cancelled perfectly. The obtained CV characteristics show a rather steep and noisy subthreshold region without a truly exponential part, in particular for high temperatures. Furthermore, some preliminary simulations indeed point to the diffusive junctions from the highly doped regions to the intrinsic channel region as a potential source of the observed non-ideal behavior. As a result, no conclusions can be drawn with respect to the effective band gap widening effect from the currently available experimental CV data. The concept should be investigated further with simulations, particularly focussing on the temperature dependence.

Recommendations

In general, more devices are needed realized in a more accurate process, preferably with thinner silicon layers. This allows for a more quantitative analysis of the band gap widening effect based on the IV measurements and reduces the dominant behavior of the diffusive junctions which strongly affects the accuracy of the CV measurements.
Further, though not mentioned before in this report, the number of properly functioning n-type devices is considerably lower than the number of working p-type devices. As this phenomenon occurs in both the DG MOSFETs and the PiN diodes, it could be related to crystal damage due to the implantation of arsenic. Its larger mass compared to boron could explain the difference between failing n-type and p-type devices. To get an overview of the working and failing devices, wafer maps have been depicted in appendix B.

Acknowledgement

I would like to thank Ray Hueting, my supervisor, for the great guidance and support. I am looking forward to the collaboration during my next challenge, my PhD!
Of course, the experiments in this thesis could not have been carried out without the devices Tu Hoang provided me with. So I really would like to express my gratitude to him.

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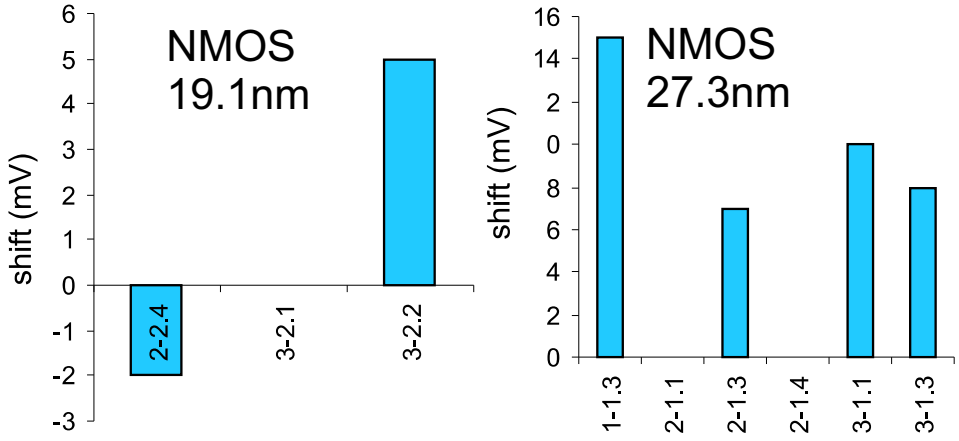
Appendix A

Additional experimental data

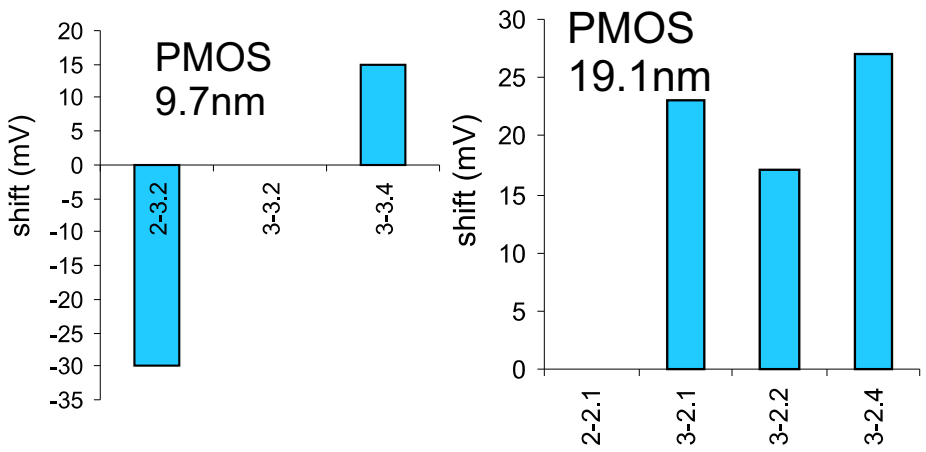
V_{GS} shift

In addition to figure 3.8 the measured shift along V_{GS} for the remaining devices is depicted in this appendix. The average values were used for the (vertical) error bars in figure 3.11.



(a) $t_{Si} = 19.1\,nm$ (b) $t_{Si} = 27.3\,nm$

Figure A.1: Shift in V_{GS} across all NMOS devices on 3 wafers



(a) $t_{Si} = 9.7\,nm$ (b) $t_{Si} = 19.1\,nm$

Figure A.2: Shift in V_{GS} across all PMOS devices on 3 wafers

Appendix B

Overview SOI MOSFETs

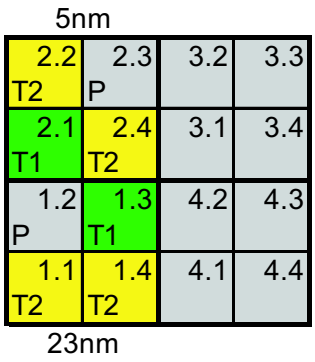
In the figures B.1 and B.2 an overview of the the available devices is given. The numbering of the devices is shown in the left column and the corresponding thicknesses in the right column. Each square consists of an 'unthinned' (150 nm) and a 'thinned' (t_{Si}) device.
The devices are colored as follows:

grey device not used

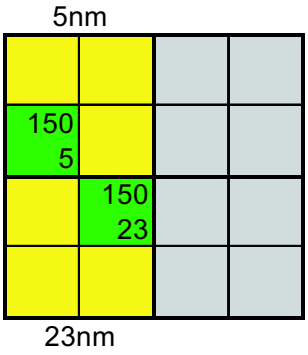
yellow device not measured

green device functions properly

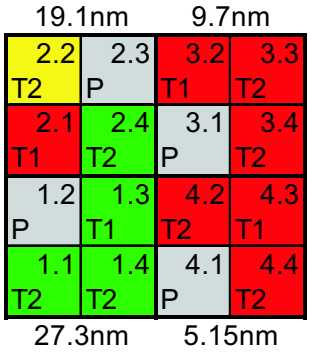
red failing device



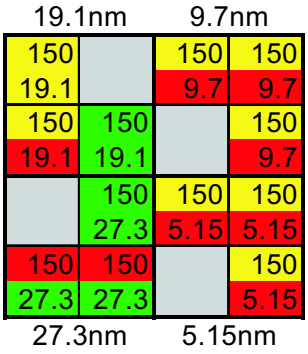
(a) Map wafer 1



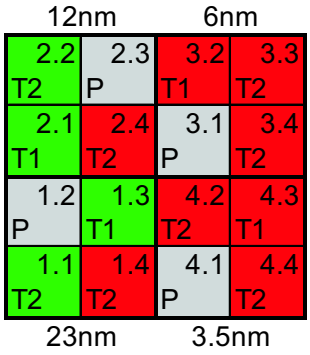
(b) Measured devices



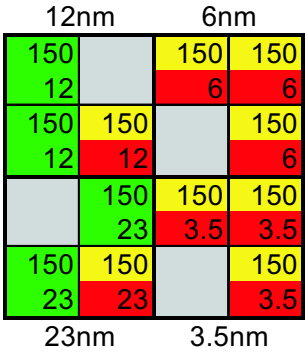
(c) Map wafer 2



(d) Measured devices

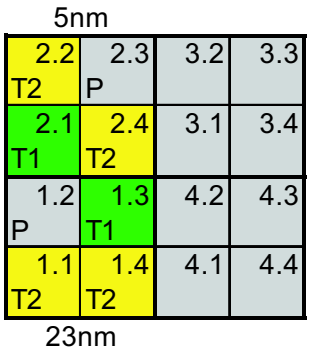


(e) Map wafer 3

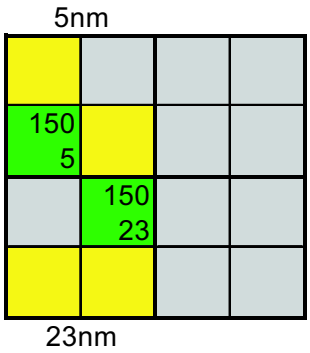


(f) Measured devices

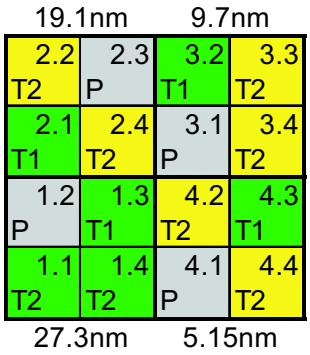
Figure B.1: Overview of failing and working NMOS devices.



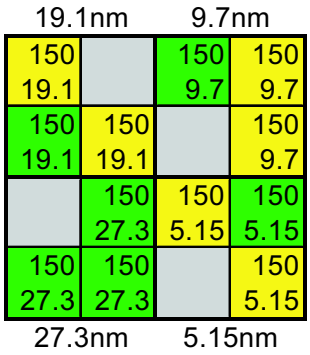
(a) Map wafer 1



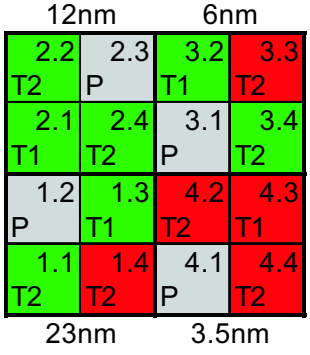
(b) Measured devices



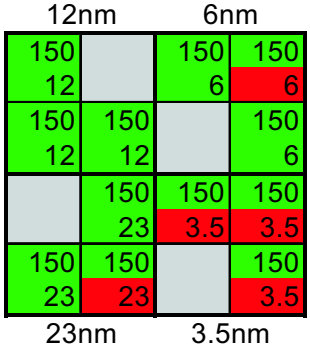
(c) Map wafer 2



(d) Measured devices



(e) Map wafer 3



(f) Measured devices

Figure B.2: Overview of failing and working PMOS devices.

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