MASTER THESIS

DESIGN OF A 1.2 VOLT REFERENCE VOLTAGE STABILIZER IN 180NM CMOS

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Project description

This master thesis describes the design of a reference voltage stabilizer in a 180 nm CMOS process technology.

A voltage reference is an analog circuit block that generates a voltage of known magnitude with little dependence on supply or process variations and with a well defined dependence on temperature. The supply variations can be caused by numerous internal and external sources and over a wide range of frequencies: from a slowly declining battery level to fast transients of the switching digital circuits. The reference voltage stabilizer circuit aims to minimize the sensitivity of the reference voltage for these fluctuations. The circuit can be applied for instance to bias other circuits or stabilize the supply to other circuits as part of a voltage regulator.

The assignment was to design and implement a voltage stabilization circuit, competitive to voltage reference devices currently on the market. This design assignment was provided by Axiom IC Twente. For this assignment an analysis has been made of products currently available on the market and the design aims have been set for competitive specifications. The circuit is designed and dimensioned to maintain a 1.2 volt output voltage over a wide input current range. Robustness to process variation and temperature fluctuation has been evaluated by simulation. Finally a chip layout was created for possible future fabrication and measurements.

Contents

Chapter 1

Introduction

Portable, battery powered devices such as mobile phones require low power, low cost, and compact components, in order to be easy to use and affordable. Since the early 1970s the electronics industry has moved from circuits built from discrete components via multiple chips on a printed circuit board (PCB), towards the integration of a complete system on a single chip known as the System-on-Chip (SoC). This process of integration has proved to reduce the physical dimensions of components and devices, and improve power-, and cost efficiency.

Although much of the signal processing in modern systems is performed within the digital domain, some functions cannot be performed (efficiently) by digital circuits. Since the system's environment is always analog, the interaction with the environment is also analog. Therefore analog-to-digital and digital-to-analog signal conversion (ADC and DAC) is still needed at the interface between system and environment. The limitations of these converters (in terms of accuracy, bandwidth and power consumption) limit the system's overall capabilities.

Therefore there is an ongoing need for integration of mixed-signal systems in the future, combining analog and digital circuits on a single chip. But both digital and analog circuits need to be fabricated with a process most suitable for digital circuits: sub-micron or nanometer complementary metal oxide semiconductor (CMOS) technology. The reason is that CMOS offers more and more transistors for digital circuits on a small die-area at relative low cost and low power. But sub-micron CMOS needs to operate at a low supply voltage. This is a challenge for the analog/mixed-signal designer: one can stack only a few transistors between supply and ground that need to operate with very limited voltage headroom. Also, the switching behavior of the digital circuits impose transients on the power supply of the analog circuits, thereby strongly impeding the performance of the analog circuits.

One of the often used analog sub-circuits that is strongly affected by these supply distortions is the voltage reference. Often a large segment of the total power dissipation is allocated to the voltage reference circuit in order to obtain a usable reference for other sub-circuits.Therefore improving the power efficiency of a voltage reference, greatly improves the efficiency of the whole mixed-signal circuit and therein lies the challenge of this thesis.

1.1 Voltage reference and voltage stabilizer - definition

A voltage reference is an analog circuit block that generates a voltage of known magnitude with little dependence on supply or process variations and with a well defined dependence on temperature. Voltage references are applied in order to *bias* other circuits (i.e. to set transistors in the proper operating region), to *quantify* a physical property (i.e. to use a signal as a standard by A/D and D/A converters and measurement systems such as temperature sensors), and to *stabilize* supply as part of a voltage regulator.

The latter, voltage stabilization, may also be a needed in order to the voltage reference itself in order to suppress sensitivity to supply variations. This kind of sub circuit is referred to as a reference voltage stabilizer.

The supply variations it aims to suppress can be caused by numerous internal and external sources and over a wide range of frequencies: from a slowly declining battery level to fast transients of the switching digital circuits.

1.2 Context of this research

1.2.1 History

In Section 12.1 of *Current Sources and Voltage References* by L. T. Harrison [1], a historic overview of the development of voltage references is presented.

In summary, the history of the voltage reference starts in the nineteenth century with wet-chemical cells, commonly known as batteries, like the Clark Cell and the Weston Cell which were used in laboratory setups.

The first discrete semiconductor voltage reference was created in the late 1950s by Clarence Zener. The *zener diode* is still widely used as a discrete component and is refined over the passed decades in terms of performance and circuit integration. In modern implementations a *buried* zener device is created inside the substrate to make monolithic voltage references with good performance compared to the earlier monolithic 'surface' zener diode references created from diode-connected bipolar transistors.

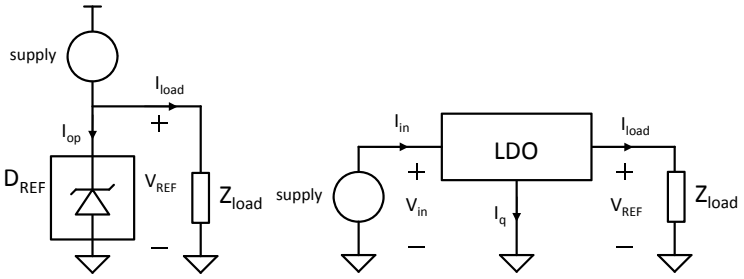
A decade after the introduction of the zener diode, the first integrated (*monolithic*) voltage reference circuit was introduced by R. J. Widlar as part of a voltage regulator IC. The concept he introduced has become known as the *bandgap reference* (BGR). It is a concept similar to the emitter-base voltage reference concept introduced by D. F. Hilbiber in 1964, but more suitable for low voltage operation and monolithic construction [2].

Besides buried zener references and bandgap references, other (monolithic) precision reference techniques have been developed. For example the XFET (eXtra-implanted junction Field Effect Transistor) references from Analog Devices and the FGA (Floating Gate Analog) references from Intersil (previously Xicor). Both types require special proprietary process technologies and are therefore not available for on-chip reference design.

1.2.2 Basic operation

Two types of voltage references can be distinguished from their basic configuration: the shunt type and the series type. The shunt type reference is a two terminal device and basically operates like a reverse biased zener diode.

The load is connected in parallel (a.k.a. shunt) with the diode. As the reverse voltage across the diode passes the breakdown voltage, the impedance of the diode drops and the current increases steeply. In order to limit the current –in its most basic configuration– a setting resistor is connected in series with the loaded reference diode. This basic configuration is shown in the schematic of Figure 1.1a. Excess current is essentially drained off by the diode, thus dissipating the surplus of power.



(a) Shunt reference (b) Series reference

Figure 1.1: Schematics of basic reference configurations

The series type reference is a three terminal device and has a dedicated input, output, and ground terminal. Depending on the application, it can also be referred to as low-drop out regulator (LDO). With the supply at the input and the load at the output, the reference and load are essentially series connected. This is shown in Figure 1.1b. Again the reference adjusts its impedance from input to output to maintain a constant output voltage, but now it only drains a small amount of *quiescent* current from input to ground in order to do so. This quiescent current has little dependence on supply or load variation. This attributes to a low and constant power consumption, which is the main advantage of the series type reference over the shunt type. On the other hand, the advantage of the shunt reference is its wide applicability. By selecting the proper setting resistor, the same design can be used in for instance low-dropout voltage or high supply voltage applications. It can even be part of a series reference.

1.2.3 Primary performance metrics

The properties of a good voltage reference as defined in 1.1 can be expressed by a number of primary performance metrics.

Process spread

The prime specification of a voltage reference device is the reference voltage V_{REF} it puts out. But the magnitude of this voltage is hard to fix by design. Process variation and mismatch, but also mechanical stress (BGRs) and along-term drift (Zeners) cause different devices of the same type to provide different reference voltages. The process variation robustness is embodied in the *initial*

accuracy or *initial error* (ϵ_{init} [%]) figure and is calculated by

$$\epsilon_{init} = \frac{\Delta V_{REF}}{V_{REF,nom}} \cdot 100\% \tag{1.1}$$

With nominal output reference voltage $V_{REF,nom}$.

Temperature dependence

The temperature dependence is expressed by the *temperature coefficient* (TC). The definition of TC varies, (e.g. the *slope* or the *box* method is used). TC is expressed in [PPM/°C]. With the box method the TC is calculated by:

$$TC = \frac{V_{out,max} - V_{out,min}}{V_{out,nom}} \cdot \frac{1}{T_{max} - T_{min}} \cdot 10^6 \tag{1.2}$$

With maximum and minimum output voltages $V_{out,max}$ and $V_{out,min}$ over the specified temperature between T_{max} and T_{min} and $V_{out,nom}$ the nominal voltage at e.g. room temperature: $T_{nom} \approx 27°C$.

Supply dependence

The metrics for sensitivity to supply variation differ for series and shunt references. For series devices transfer characteristics the static (DC) line sensitivity and the dynamic (AC) supply dependence are expressed by *line regulation* (LNR [ppm/V]) and *power supply ripple rejection* (PSRR [dB]) respectively.

For shunt devices, static transfer is expressed by *change of voltage with change of current* (ΔV(ΔI) [mV]) and dynamic transfer by *dynamic impedance* Z. It's convenient in order to normalize it to obtain a more universal figure of merit, because the dynamic impedance varies with the input current and depends on the output voltage level. In this thesis it is referred to as the impedance scaling factor and it is calculated by:

$$ZS = \frac{Z}{V_{REF}/I_{op,dc}} \tag{1.3}$$

where V_{REF} and $I_{op,dc}$ represent the DC reference voltage and DC operating current. Both ZS and PSRR should be specified with a bandwidth indication, because they describe dynamic (frequency dependent) behavior.

Noise

The noise characteristics of a voltage reference are described by the frequency dependent noise, dominant at low-frequencies ($1/f$) and by the wide band noise density. These characteristics are similar to operational amplifier (OpAmp) noise characteristics.

The low-frequency voltage noise e_N is expressed by either the peak-to-peak voltage [V_{p-p}] or the integral noise voltage [V_{rms}] and is specified over a bandwidth of usually 0.1 to 10[Hz]. In order to convert one figure to the other it is often assumed that the noise signal is 0.1% of the time out of the peak-to-peak range [3], so

$$[V_{p-p}] \approx 6.6 \cdot [V_{rms}] \tag{1.4}$$

The wide band noise is specified by the spectral noise density $N_V(f)$ in $[V/\sqrt{Hz}]$. It is sufficient to collect noise density figures from the product datasheets at 1 kHz at this point.

The low-frequency and wide band figures are linked by the noise corner frequency fc, N. At the corner frequency the noise power contributions of low-frequency noise and the wide band noise are equal. So the spectral noise density is $\sqrt{2}$ times the wide band noise density if it is expressed by $[V/\sqrt{Hz}]$.

The relation between V_{rms} (and thus V_{p-p}), $N_V(f = 1kHz)$, and fc, N -in case the low frequency band is lower than the corner frequency [3]- is:

$$V_{rms} \approx N_V(1kHz)\sqrt{f_{c,N}\frac{f_H}{f_L}} \tag{1.5}$$

with the integral bandwidth defined by the lower frequency bound f_L and the high frequency bound f_H (in this case their values are 0.1 and 10 Hz respectively).

Power efficiency

The power dissipation of the series type reference is characterized by the quiescent current: the reference current in case of zero load current. This is a good indication of the power consumption of the reference, because the current drained to establish the output reference voltage varies very little with supply or load.

For the shunt type reference this is not the case, current drained by the reference varies strongly with supply an load variations. However, the minimum operating current is a useful alternative to compare the power efficiency of different shunt references. Impedance scaling and stability and noise need to be taken in to account, in order to make a proper evaluation on power efficiency. So if for dynamic impedance and noise figures are provided the operating conditions in terms of input current range and load capacitance range should be specified.

1.2.4 Market

In Appendix A of this thesis an overview is included of a number of low-voltage off-chip references ($V_{in} \leq 2V$) currently on the market. The series type and shunt type references are listed separately. All these low-voltage reference components are based on the bandgap principle. The buried zener references and the proprietary XFET and FGA references are only available for higher input voltage ranges.

First the series references are considered. All 1.25 V references need at least 1.8 V supply to meet their specifications. Low-dropout series references are only available for higher output levels. The MAX6018A reference of Maxim-IC and the LM4121 reference of National Semiconductor show the best supply rejection performance: both 82 dB PSRR at 1 kHz cut-off frequency. The MAX6018A also has the lowest quiescent current of just 5 μA and the LM4121 the fastest start-up response of about 8 μs. In terms of noise performance the majority has a low-frequency noise level below 20 μV_{p-p} over the 0.1 to 10 Hz band and a wideband output noise of less then 1 $\mu V/\sqrt{Hz}$. The LM4140 from

National Semiconductor has the best noise performance: 20 μV_{p-p} and 200 nV/$\sqrt{\text{Hz}}$.Most series devices require an external output capacitor for stability and some also need a bypass capacitor at the input. Large capacitors may improve the noise and supply rejection performance.

For shunt type references low voltage operation is inherent to their configuration. Considering their dynamic behavior, most references show best impedance scaling performance at 100 μA (for f_{in} <100 Hz), the REF1004 and LT1004 by Texas Instruments in particular with 96 dB Ω. The cut-off frequency of this behavior lies below 1 kHz for most devices, accept for the MAX6138 which is 6 kHz with 72 dB impedance scaling at lower frequencies (I_{op} =1 mA) The REF1112 by TI, the MAX6006 by Maxim-IC, and the LT1389 by Linear Technology have the lowest mimimum operating current levels of 1.2, 1.0 and 0.8 μA respectively. The AD589 by Analog Devices and the LM113 by National Semiconductor have the best wideband noise performance of about 50 nV/$\sqrt{\text{Hz}}$ (if the recommended 1 nF output capacitor is used) and the other shunt references by Analog Devices (ADR510, AD1580, ADR1581, ADR1500) have the lowest noise level at low-frequencies (4 to 5 μV_{p-p}). More than half of the shunt devices listed do not require an external output capacitor for stability although it may be recommended for low-noise purposes. The REF1112 requires 10 nF, the MAX6006 also 10 nF, the LM113 200pF and the LT1389 needs 100 pF.

On-chip references are also on the market, for instance incorporated into mixed-signal products such as the AD7949 of Analog Devices[1]. Precision mixed-signal products with on-chip references such as the AD7949 often also provide the option of connecting an external reference for improved performance. In general, these on-chip references are hard to compare, because the datasheets of this type of products lack detailed specifications on the voltage reference sub-circuits. Therefore they are not included in this overview.

1.3 Motivation and objectives

The goal of this research is to further develop the reference voltage stabilizer concept provided by A. J. M. van Tuijl and to design and implement a circuit based on this concept: A widely applicable shunt stabilizer with high supply rejection characteristics. The design should have power efficient and robust operating behavior in a wide range of conditions (i.e. supply, process, load and temperature variations) and it has to be compatible with the UMC180 mixed mode process library (.18μm CMOS technology). The design needs to be able to operate in a mixed signal environment and may become part of a self-calibrating voltage reference (sub-)system. Such a sub-system includes a bandgap reference and a control circuit that will generate a trim signal for the stabilizer for improved initial accuracy. The design should not require any external capacitors, while maintaining stable operation with a wide range of capacitive loads.

The most important performance requirements for the voltage stabilizer design is summarized in Table 1.1.

[1] http://www.analog.com/static/imported-files/data_sheets/AD7949.pdf

Table 1.1: Requirements - Shunt stabilizer circuit

Description	Symbol	Value
Minimum operating current [1]	$I_{op,min}$	$\leq 20\ \mu A$
Maximum operating current [1]	$I_{op,max}$	≥ 5 mA
Output voltage	V_{out}	1.2 V
Impedance scaling [2]	$ZS\|_{I_{op}=1\text{ mA},f=10\text{ kHz}}$	80 dB
Low-frequency voltage noise	$e_N\|_{f=0.1..10\text{ Hz}}$	$20\ \mu V_{p\text{-}p}$
Spectral noise density	$N_V\|_{f=1\text{ kHz}}$	$300\ nV/\sqrt{Hz}$

[1] Current range for which the circuit remains within specifications
[2] Figure of Merit as explained in Appendix A, Note 1

1.4 Acknowledgements

First of all, I would like to thank professor Ed van Tuijl, affiliated with both the ICD group at the University of Twente and Axiom-IC Twente. I want to thank him for his guidance during my master studies: for supervising both my internship with NXP Research in Eindhoven and this master thesis project with Axiom-IC, and I would like to thank him for providing me with this assignment, which has given me the opportunity to learn allot about IC design and research over the past nine months.

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Finally, I would like to thank Suzanna Treumann for spell checking this report and for her patience and support during the past few months.

1.5 Thesis outline

First a number of system level considerations will be addressed in Chapter 2 to provide a context for voltage stabilizer of which the circuit design is discussed in Chapter 3. Chapter 4 provides the simulation results. Finally, in Chapter 5 the conclusions of this thesis are presented.

Chapter 2

System level design

The system level design of a voltage reference discussed in this section is added to provide an example context for the stabilization circuit design of this thesis. This shows how a voltage reference system may benefit from a stabilization circuit in terms of improved supply stability and power efficiency. Within the context of this voltage reference system a comparison of the stabilization circuit with other voltage reference products can be made.

In Figure 2.1 the system level overview of the voltage reference is shown.

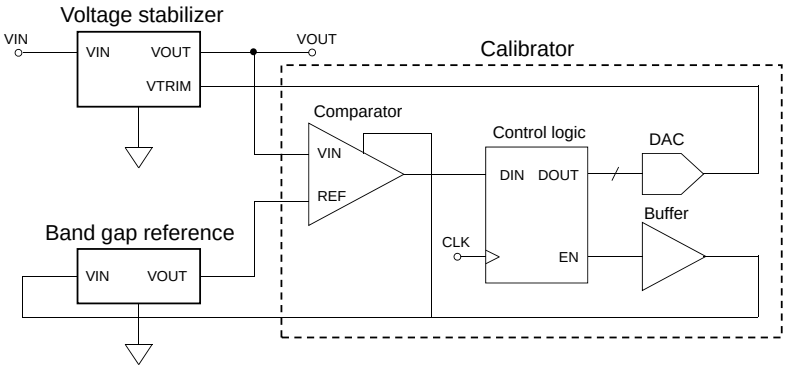


Figure 2.1: System level overview

Three main system blocks can be distinguished: the voltage stabilizer, the bandgap reference, and the calibrator. The voltage stabilizer should provide constant output with good supply ripple rejection and low noise. At start-up the calibator adjusts the trim signal of the voltage stabilizer to get a better defined output level after comparing the output to a BGR with a much higher initial accuracy. This combines the good initial accuracy and well a defined temperature dependence of the bandgap and the power efficient supply rejection and low noise characteristics of the stabilizer. After the start-up calibration is complete the BGR and the comparator circuits are switched off and the system can start normal operation.

One disadvantage of this system is an increased start-up time, because the calibration loop needs some time to settle after the BGR is completely turned on. Another disadvantage is the possible drift of the voltage level after calibration due to environment temperature variations or self-heating of the chip. However, depending on the characteristics of the total system, it may be possible to recalibrate at a convenient interval.

The calibrator coordinates a successive approximation (SA) scheme much like those used in SA ADCs to match the output of the stabilizer to the output of the BGR. In each step the two outputs are evaluated by the comparator in order to decide to either lifted or lower the trimming signal of the stabilizer. After a number of steps the outputs are approximately equal so the calibration process holds and the unneeded sub circuits are switched off.

Chapter 3

Circuit design

This Chapter is about the circuit design of the reference voltage stabilizer. Starting from the basic concept in Section 3.1, then extending the circuit towards its final form in Section 3.2, followed by small signal analysis in Section 3.3, and this Chapter finishes with some noise considerations for the design in Section 3.4.

3.1 Basic Concept

The starting point of the two-terminal circuit design is the well controlled source-drain resistance of a MOST. The high R_{off} and low R_{on} make it suitable to adjust impedance and maintain a constant output voltage for a wide input current range. A sensitive error sensing sub-circuit is needed to steer the impedance adjustments. The basic concept of this circuit is shown in Figure 3.1.

The sensing part consists of two connected current mirrors: a symmetric NMOS mirror (M1 & M3) and an asymmetric PMOS mirror (M2 & M4). The asymmetry is determined by the multiplying factor m and the source degeneration resistor R_t at the output MOST M4 of the PMOS mirror.

Since the current mirror transfer characteristics of the two mirrors are different and copied current levels intersect at a point defined by the m and R_t, the difference between the currents at the outputs of the two mirrors at node **y** is a measure for error with respect to this intersection level. This is illustrated by Figure 3.2.

The error current charges or discharges the gate of M5, so the gate-source voltage of M5 (V_{gs5}) changes and thereby adjusts the impedance of M5. This alters the voltage at node **ref** and consequently the current through the current mirrors.

So, if the asymmetric mirror has an effective mirror ratio higher than the ratio of the symmetric mirror, then the drain-source current (I_{ds}) from M4 is bigger the I_{ds} from M3 ($I_{ds4} > I_{ds3}$) and V_{gs5} is increased and thus the impedance of M5 is decreased. As a result, I_{ds5} decreases, and the current at the input of the current mirrors increases. The output current of the asymmetric current mirror becomes more affected by the degeneration, lowering the effective mirror ratio (I_{ds4}/I_{ds2}). If on the other hand the asymmetric mir-

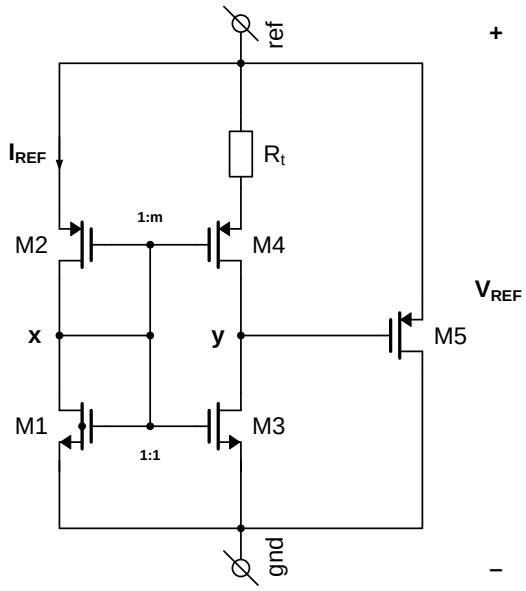


Figure 3.1: Basic circuit concept

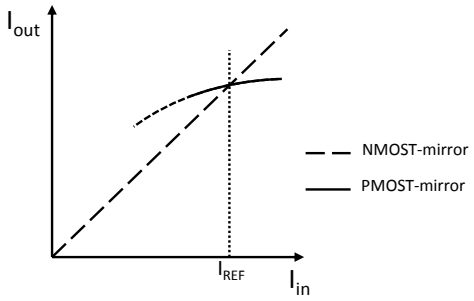


Figure 3.2: Current mirror transfer

ror has an effective mirror ratio lower than the ratio of the symmetric mirror ($I_{ds4} < I_{ds3}$), then the circuit adjusts in the opposite direction.

Eventually the output currents of both current mirrors will converge to the intersection level, because of this negative feedback mechanism. This ensures a constant quiescent reference current (I_{REF}) through the inputs of the current mirrors (diode connected MOSTs M1 & M2)) and a constant output reference voltage (V_{REF}).

3.1.1 Device models for operating point analysis

For the MOSTs that operate in the strong inversion (SI) and saturation (SAT) region, the simplified quadratic MOST model can be used to estimate the reference current. If channel length modulation is neglected, the drain-source

current for this SI–SAT model is

$$I_{ds,SI-SAT} = \frac{1}{2} \cdot \beta \cdot (V_{gs} - V_{th})^2 \tag{3.1}$$

With gate source voltage V_{gs}, threshold voltage V_{th} and current factor β. The current factor itself is modeled as:

$$\beta = \mu \cdot C_{OX} \cdot \frac{W}{L} \tag{3.2}$$

With charge carrier mobility μ, gate oxide capacitance per unit area C_{OX} and gate dimensions; width W and length L. For ease of notation, a positive sign convention for both NMOS and PMOS devices is maintained throughout this thesis. So $V_{sg,p}$, $-V_{th,p}$, and $I_{sd,p}$ are noted as V_{gs}, V_{th}, and I_{ds} respectively.

For the MOSTs that operate in the weak inversion (WI) and saturation region, the simplified exponential WI model of the MOST applies. Now, the drain current can be approximated by:

$$I_{ds,WI-SAT} \approx I_0 \cdot e^{\frac{V_{gs}}{n \cdot U_T}} \tag{3.3}$$

$$I_0 = 2n \cdot U_T^2 \cdot \beta_p \cdot e^{\frac{-V_{TH}}{n \cdot U_T}} \tag{3.4}$$

Where I_0 is the current at $V_{gs} = V_{th}$, slope factor n is given by $n = 1 + C_D/C_{OX}$ (C_D is the depletion layer capacitance), and the thermal voltage U_T represents $U_T = kT/q$ with T for temperature, Boltzmann constant k and elementary electron charge q.

3.1.2 Reference current

The reference current level -after convergence- can be estimated by comparing the current transfer characteristics of both current mirrors. So $I_{ds3}\,(I_{ds1})$ and $I_{ds4}\,(I_{ds2})$ need to be found, where $I_{ds1} = I_{ds2} = I_{REF}$, to be able to find I_{REF} for:

$$I_{ds3}\,(I_{REF}) = I_{ds4}\,(I_{REF}) \tag{3.5}$$

Starting with the NMOS mirror: both gate source voltages are equal ($V_{gs3} = V_{gs1}$), and both M1 and M3 operate in the SI–SAT region, so with (3.1) the output current can be expressed as:

$$\begin{aligned} I_{ds3} &= \frac{1}{2} m_n \cdot \beta_n \cdot (V_{gs1}\,(I_{ds1}) - V_{th,n})^2 \\ &= m_n \cdot I_{ds1} \end{aligned} \tag{3.6}$$

Since $I_{ds1} = I_{ds2} = I_{REF}$:

$$I_{ds3}\,(I_{REF}) = m_n \cdot I_{REF} \tag{3.7}$$

With multiplying factor m_n to scale the dimensions of M3 with respect to M1 such that $\beta_{M1} = \beta_n$ and $\beta_{M3} = m_n \cdot \beta_n$. Where β_n is the current factor base (3.2) of the NMOS mirror.

For the PMOS mirror the gate-source voltage of M4 is degenerated by the voltage-drop over R_t:

$$V_{gs4}(I_{ds4}) = V_{gs2}(I_{ds2}) - I_{ds4} \cdot R_t \tag{3.8}$$

With $V_{gs2}(I_{ds2})$ generated by the diode connected M2 operating in SI-SAT region (3.1). So

$$V_{gs2}(I_{ds2}) = \sqrt{\frac{2}{\beta_p}} \cdot \sqrt{I_{ds2}} + V_{th,p} \tag{3.9}$$

Now, depending on the operating region of M4, I_{ds4} can be expresses with either the quadratic or the exponential model.

If M4 operates in the SI–SAT region, then (3.1) is used to find an expression for I_{ds4}:

$$I_{ds4,SI} = \frac{1}{2} m_p \cdot \beta_p \cdot \left(V_{gs2}\left(I_{ds2}\right) - I_{ds4} \cdot R_t - V_{th,p}\right)^2 \tag{3.10}$$

With multiplying factor m_p to scale the dimensions of M4 with respect to M2 such that $\beta_{M2} = \beta_p$ and $\beta_{M4} = m_p \cdot \beta_p$. Where β_p is the current factor base of the PMOS mirror (3.2).

Figure 3.3 illustrates the current transfer of the SI-SAT PMOST mirror. It also shows the effect of source degeneration.

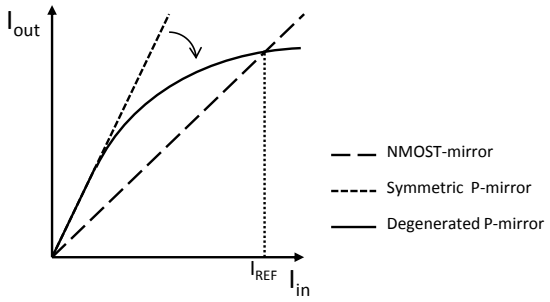


Figure 3.3: Current mirror transfer - SI-SAT M4

If M4 operates in the WI–SAT region, then (3.3) is used to find an expression for I_{ds4}:

$$I_{ds4,WI} = I_0 \cdot m_p \cdot e^{\frac{V_{gs4}}{n \cdot U_T}} \tag{3.11}$$

and substitution of (3.8) and (3.9)

$$I_{ds4,WI} = I_0 \cdot m_p \cdot e^{\frac{\sqrt{\frac{2}{\beta_p}} \cdot \sqrt{I_{ds2}} + V_{th,p} - I_{ds4} \cdot R_t}{n \cdot U_T}} \tag{3.12}$$

and since $I_{ds1} = I_{ds2} = I_{REF}$, it can be shown that

$$I_{ds4,WI}(I_{REF}) = \frac{n \cdot U_T}{R_t} \cdot \mathbf{W}\left(2\beta_p \cdot m_p \cdot R_t \cdot U_T \cdot e^{\frac{\sqrt{\frac{2}{\beta_p}} \sqrt{I_{REF}}}{n \cdot U_T}}\right) \tag{3.13}$$

Where $\mathbf{W}()$ is the Lambert W-function defined as

$$y = ze^z \iff z = \mathbf{W}(y), z \in \mathbb{C} \tag{3.14}$$

The effects that R_t and m_p have on the current transfer of the PMOS mirror described by (3.11) are illustrated by the graphs of Figure 3.4. These rela-

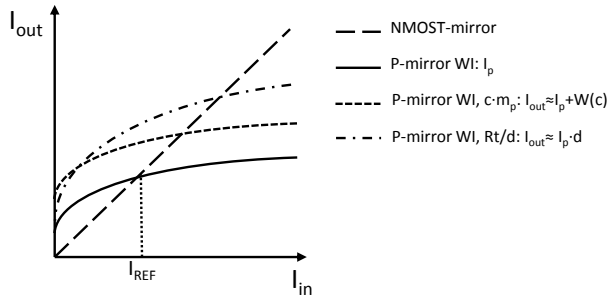


Figure 3.4: Current mirror transfer - WI-SAT M4

tions can also be recognized if (3.13) is approximated with the more intuitive equation:

$$I_{ds4,WI}(I_{REF}) \approx \frac{n \cdot U_T}{R_t} \left(\Omega \left(\frac{2}{\beta_p} \cdot \frac{I_{REF}}{n^2 \cdot U_T^2} \right)^{\Omega} + \mathbf{W}\left(2\beta_p \cdot m_p \cdot U_T \cdot R_t\right) \right) \tag{3.15}$$

where $\Omega = \mathbf{W}(1) \approx 0.567814$. So the current transfer in the region of interest is similar to a lifted square-root function. Although slightly steeper, because $\mathbf{W}(1) > 0.5$. This approximation can be made because of the exponent inside the Lambert W-function.

Finally, the converged reference current level can be estimated by solving $I_{ds4}(I_{REF}) = I_{ds3}(I_{REF})$ for both the SI and the WI case, with I_{ds3} defined by (3.6).

For the SI case, with $I_{ds4}(I_{REF})$ defined by (3.10), the solution is:

$$I_{REF} = \frac{2}{\beta_p \cdot m_n^2 \cdot R_t^2} \cdot \left(1 - \sqrt{\frac{m_n}{m_p}}\right)^2 \tag{3.16}$$

For the WI case where $I_{ds4}(I_{REF})$ is defined by (3.13) the equation

$$I_{REF} \cdot m_n = I_0 \cdot m_p \cdot e^{\frac{V_{gs2}(I_{REF}) - I_{REF} \cdot m_n \cdot R_t}{n \cdot U_T}} \tag{3.17}$$

cannot be solved algebraically for I_{REF}. So numerical methods are used to find the reference level.

3.1.3 Operating current range

The total operating current of the stabilizer is equal to the sum of the current through the reference current path, the mirrored current path and the drain current of M5:

$$I_{OP} = (m_n + 1)I_{REF} + I_{ds5} \tag{3.18}$$

If large and small signal effects are not considered, then a coarse estimate of the current range can be found by switching M5 off and on. If it is assumed that the drain current of M5 -when switched off- is negligible, then minimum operating current is approximately:

$$I_{OP,min} \approx (m_n + 1)I_{REF} \tag{3.19}$$

If on the other hand the drain current of M5 is maximum, then the reference current and its mirror are negligible and the maximum current is approximately equal to maximum drain current of M5 $I_{ds5,max}$ for which the SI-SAT model of (3.1) applies:

$$I_{OP,max} \approx I_{ds5,max} = \frac{1}{2} \cdot \beta \cdot (V_{gs5,max} - V_{th})^2 \tag{3.20}$$

The maximum gate-source voltage of M5 is ultimately limited by the reference voltage ($V_{gs} = V_{REF} - V_y$). This would lead to the conclusion that the maximum current can be set by simply adjusting the (W/L) of M5.

However, the voltage level of node **y** strongly affects current mirror operation: The reference current and voltage levels are altered by the -previously neglected- channel length modulation of the MOSTs at the output of both mirrors. Also, SAT operation of the current mirror output MOSTs is lost as V_y approaches either V_{REF} or ground.

Since rigid current-mirror operation is key to maintain a constant reference level over a large operating current range, a number of design alterations should be made. The discussed issues are also common in operation amplifier (OpAmp) design and the same remedies can be applied:

In order to reduce the effects of channel length modulation cascode stages can be added to both current mirrors. But the cascode stages restrict the operable range of V_y even further, since these stages need to operate in SAT as well. This calls for another adjustment.

First note that two opposing requirements on node **y** apply. On one hand V_y swing needs to be minimal in order not to disturb the current mirrors and on the other hand the swing needs to be maximal in order to put M5 on or off as much as possible in order to have a large operating range.

This problem can be solved by inserting a common-source (CS) amplifier stage at node **y**. Node **y** is split into nodes **y1** and **y2** while the swing voltage is amplified from the first node to the later, so both requirements can be met.

Finally the PMOST M5 is replaced by an NMOST in order to maintain negative feedback, because the CS stage has a negative gain.

These (and other) circuit extensions are discussed in more detail in the subsequent sections of this chapter, including the stability issue that arises from the added amplifier stage. But first other aspects of the basic concept are to be examined more closely.

3.1.4 Reference voltage

The reference voltage can be estimated by adding the gate-source voltages of the diode connected M1 and M2:

$$\begin{aligned} V_{REF} &= V_{gs1}(I_{REF}) + V_{gs2}(I_{REF}) \\ &\approx \sqrt{\frac{2}{\beta_n}} \cdot \sqrt{I_{REF}} + V_{th,n} + \sqrt{\frac{2}{\beta_p}} \cdot \sqrt{I_{REF}} + V_{th,p} \end{aligned} \tag{3.21}$$

assuming that both M1 and M2 are operating in SI–SAT region.

3.1.5 Temperature dependence

This study on how temperature variations affect circuit operation starts with the device models.

The drain current expression of the quadratic model of a MOST operating in SI–SAT region (3.1) contains two variables that change with temperature: the threshold voltage V_{th} and the mobility μ as part of β (3.2).

The drain current expression of the exponential model of a MOST operating in WI–SAT region (3.3) also contains a temperature term as part of the thermal voltage ($U_T = kT/q$).

It is assumed that the temperature sensitivity of the passive circuit elements is negligible at this point. Simulation with a high ohmic resistor "RNHR1000" from the UMC018 process library has shown a negative temperature coefficient of the resistance of $\frac{\partial R_{HR}}{\partial T} \approx -880ppm/^\circ C$. This amounts to $-88\mu V/t^\circ C$ for a $100k\Omega$ resistor with 1uA current (typical values in this design).

In Section 9.1.3 of *CMOS: Circuit design, layout, and simulation* by R.J. Baker [4] it is shown that the change of threshold voltage with change of temperature can be approximated by

$$\frac{\partial V_{th}}{\partial T} \approx -\frac{k}{q} \cdot \ln \frac{N_{gate}}{N_{sub}} \tag{3.22}$$

Where N_{gate} and N_{sub} are the doping concentrations in the gate and the substrate respectively. For the NMOST of UMC18 process technology $N_{gate} \approx 1 \cdot 10^{23}[cm^{-3}]$ and $N_{sub} \approx 3.74 \cdot 10^{17}[cm^{-3}]$ and for the PMOST $N_{gate} \approx 1 \cdot 10^{23}[cm^{-3}]$ and $N_{sub} \approx 6.13 \cdot 10^{17}[cm^{-3}]$, so

$$\frac{\partial V_{th,n}}{\partial T} \approx -1mV/^\circ C \tag{3.23}$$

$$\frac{\partial V_{th,p}}{\partial T} \approx -1mV/^\circ C \tag{3.24}$$

The temperature dependence of mobility can be modeled by

$$\mu(T) = \mu(T_0) \cdot \left(\frac{T_0}{T}\right)^{\mu_{te}} \tag{3.25}$$

Where μ_{te} is the mobility temperature exponent (typically 1.5).

In summary, as temperature increases the threshold voltage goes down (approximately) linearly, as does the resistance, and mobility reduces with a declining slope.

The next step is to apply these relations to the circuit under consideration and estimate the influence of temperature on the reference current and voltage.

For a reference current with one PMOST operating in the WI region (3.13), the output current scales up while the I_{in}–I_{out} transfer characteristic of the symmetric current mirror remains the same. This yields a approximately linear positive temperature coefficient (PTC) reference current. By means of a taylor approximation at $T = 27^\circ C = 300K$ and $I_{REF} = 1\mu A$ an estimate has been found of:

$$\frac{\partial I_{REF}}{\partial T} \approx +3nA/^\circ C \tag{3.26}$$

The temperature sensitivity of the reference voltage can now be estimated by the partial differential of (3.21) with respect to temperature and combining the found temperature coefficients. The partial differential is:

$$\frac{dV_{ref}(T)}{dT} = \frac{\partial V_{th,n}(T)}{\partial T} + \frac{\partial V_{th,p}(T)}{\partial T} + \frac{\partial}{\partial T}\left(\sqrt{\frac{2 \cdot I_{REF}(T)}{\beta_n(T)}}\right) + \frac{\partial}{\partial T}\left(\sqrt{\frac{2 \cdot I_{REF}(T)}{\beta_p(T)}}\right) \quad (3.27)$$

Where

$$\begin{aligned}\frac{\partial}{\partial T}\left(\sqrt{\frac{2 \cdot I_{REF}(T)}{\beta_n(T)}}\right) &\approx \sqrt{\frac{2}{\beta_{n,0}}} \cdot \frac{\partial}{\partial T}\left(\sqrt{\frac{I_0 + \frac{\partial I_{REF}}{\partial T}(T - T_0)}{\left(\frac{T_0}{T}\right)^{1.5}}}\right) \\ &\approx \frac{1}{2} \cdot \sqrt{\frac{2}{\beta_{n,0} \cdot I_0}} \cdot \left(\frac{1.5 \cdot I_0}{T_0} + \frac{\partial I_{REF}}{\partial T}\right)\end{aligned} \quad (3.28)$$

With I_0 and $\beta_{n,0}$ representing the reference current and current factor at $T_0 = 300K$ respectively. For a typical I_{REF} of $1\mu A$ this becomes $4 \cdot 10^{-6} \cdot \sqrt{2/(\beta_{n,0})}$. So for a square gate NMOST the temperature coefficient is about $0.35mV/^\circ C$. The PMOST dimensions will be scaled to get about the same current factor, so the TC is in the same order of magnitude.

Finally (3.27) can be estimated by filling in the partial differentials of al the terms:

$$\frac{\partial V_{REF}}{\partial T} \approx (-1 - 1 + 0.35 + 0.35)mV/^\circ C \approx -1.3mV/^\circ C \quad (3.29)$$

Although the reference current goes up with temperature, the decreased threshold has a dominant effect on the diode voltages, resulting in a reference voltage with a negative temperature coefficient (NTC). By decreasing the current factor -i.e. the (W/L)- of the diodes at smaller temperature coefficient can be obtained. But as shown by (3.25) the mobility does not decrease linearly. Therefor it is better to adjust the circuit to (partially) compensate the NTC of the diode voltages by sending the PTC reference current through a resistor, thereby creating an extra PTC voltage contribution to the diode stage.

If the TC of the resistor itself is not considered, then the ideal compensation resistor value can easily be found by

$$R_c = \frac{\partial V_{REF}}{\partial T} / \frac{\partial I_{REF}}{\partial T} = \frac{1.3mV/^\circ C}{3nA/^\circ C} \approx 0.43M\Omega \quad (3.30)$$

This would minimize the slope at T_0. Other optimizations may be preferred, because the temperature characteristic is not linear. For instance by minimizing the maximum voltage difference over the full operating temperature range for a minimal box temperature coefficient.

Mind that, unlike bandgap references, this circuit does not utilize rational to absolute temperature properties of a pair of weak-inversion or (parasitic) bipolar devices.

3.2 Circuit extensions

In Subsection 3.1.3 it is suggested to add cascode stages to the current mirrors and a CS-stage between the current sensing and the current carrying part of the circuit in order to improve operation over a wide input current range. In Subsection 3.1.5 it is suggested to insert a resistor in the biasing stage of the current mirrors to improve temperature behavior as well. This Section expands on these suggestions and explains the circuit extensions and design considerations that have been incorporated into the final circuit.

3.2.1 Cascode stages

It has previously been suggested that by means of cascoding -i.e. adding common gate (CG) stages to the outputs of both mirrors- the current mirror operation is shielded from variations of V_y. But the cascodes improve the output impedance of the mirrors as well. This has a positive effect on the low-frequency voltage gain.

Output impedance

The output resistances of the PMOST and NMOST branch can be approximated by

$$R_{o,p} \approx \frac{g_{m8} \cdot R_t}{g_{ds7} \cdot g_{ds8}} \tag{3.31}$$

$$R_{o,n} \approx \frac{g_{m6}}{g_{ds5} \cdot g_{ds6}} \tag{3.32}$$

respectively. Where g_m and g_{ds} represent the small signal parameters transconductance and drain-source conductance. Note that the transistors have been relabeled, in accordance with Figure 3.5.

The output resistance of the two branches combined is approximately equal to a parallel connected because the small signal at node **ref** is considered DC at the moment (at least compared to the signal at node **y**). This means that the much lower impedance of the NMOST branch detemines the value of total resistance to ground at node **y**. By adding a source resistor to the NMOST-mirror the output resistance can be lifted to the same order of magnitude level. So the output resistance of the NMOST branch becomes:

$$R_{o,n} \approx \frac{(g_{m6} + g_{mb6}) \cdot R_s}{g_{ds5} \cdot g_{ds6}} \tag{3.33}$$

Where g_{mb} represents the bulk or back gate transconductance. By the way, the input of the NMOST mirror is also equiped with a source resistor in order to maintain symmetry.

Further small signal analysis will be treated in Section 3.3.

Biasing

The input side of the current mirror is also cascoded in order to maintain symmetry as much as possible. Because the voltage headroom is very limited low-voltage cascode mirrors are applied. Meaning that at the input of the

current mirror the feedback line of the diode connected MOST is not connect from the gate of input MOST to its own drain, but to the drain of its cascode MOST. It minimizes the voltage needed to maintain the MOSTs in saturation. This modification is also discussed in Section 5.2 of *Design of Analog CMOS Integrated Circuits* by B. Razavi [5].

The gates of the GS-stages of the cascodes need to be biased. The bias voltage should be at high enough to maintain the mirrors saturated: $V_b \geq V_{gs2} + (V_{gs1} - V_{th1}) + V_{R_S}$. If the aspect ratio (W/L) of the cascode MOST is sufficiently high then V_{gs2} is lower than threshold and the SAT condition minimal: $V_{dsat} = 2n \cdot U_T$. The same considerations hold for the other cascode MOSTs. This biasing voltages for both the NMOST and PMOST mirror can be created by adding a single biasing resistor R_b between the current mirrors at the input side. The two biasing voltages are referred to as V_{b1} and V_{b2}. This approach is known as self biasing.

The schematic of the self-biased cascoded current mirrors as described in this Subsection is shown in Figure 3.5.

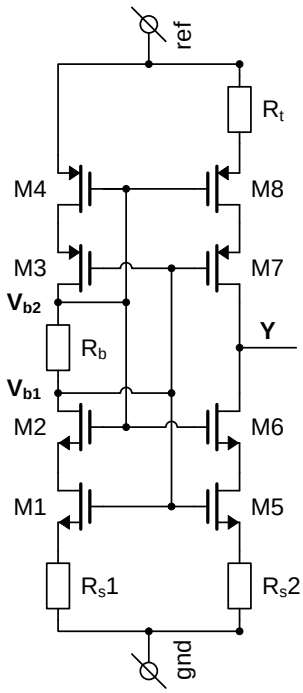


Figure 3.5: Schematic - Self-biased cascoded current mirrors

With these adjustments the reference voltage of (3.21) becomes:

$$\begin{aligned} V_{REF} &= V_{gs1}(I_{REF}) + V_{gs4}(I_{REF}) + V_{R_s} + V_{R_b} \\ &\approx \sqrt{\frac{2}{\beta_n}} \cdot \sqrt{I_{REF}} + V_{th,n} + \sqrt{\frac{2}{\beta_p}} \cdot \sqrt{I_{REF}} + V_{th,p} + I_{REF} \cdot (R_s + R_b) \end{aligned} \tag{3.34}$$

The added resistors in this current path also provide some temperature compensation as discussed in Subsection 3.1.5.

3.2.2 Common-source stage

In Subsection 3.1.3 it was explained that the insertion of a common-source (CS) amplifier stage reliefs the tight constraint that the saturation condition of the cascoded current mirrors put on the gate voltage range and therefore the current range of the current shunting MOST.

After splitting node **y** into nodes **y1** and **y2** and adding the CS stage a new concern arises: Now there are two high voltage gain nodes inside the negative feedback control. Both attribute a pool to the loopgain of the circuit and along with another pool attributed by the load capacitance a phase shift of more than 180° at unity gain becomes possible and the circuit can become instable.

The circuit needs to be carefully dimensioned in order to circumvent instability for a unknown but certain capacitive load. The dominant pole will need to be placed such that a sufficient phase margin is maintained. Therefore the capacitor $C1$ is added to node **y1**.

The voltage gain, output resistance, and capacitances to node **y2** vary with the voltage level of that node. The voltage range needs to be large in order to enable the current shunting MOST to conduct al large range of current levels. So characterization and design of this node for the various operating points is crucial. Especially the variable gate- source capacitance of the current shunting MOST needs to be investigated. It varies because the bias conditions of this MOST vary depending on the current it needs to shunt.

If the gate-source voltage is low, below threshold, then the gate-source capacitance consists mostly of the gate-source overlap capacitance C_{gsov}. As the channel becomes more inverted and charge builds up with the increasing gate voltage, the gate-source capacitance increases untill it enters SI-SAT operation and settles at about:

$$C_{gs} = \frac{2}{3} \cdot W \cdot L \cdot C_{ox} + C_{gsov} \tag{3.35}$$

The gate-drain capacitance remains constant and equal to the gate-drain overlap capacitance C_{gdov}. For the triode region both gate-source and gate-drain capacitance would change, but this need not to be considered: saturation of the MOST is guarantied in this circuit because V_{gs} cannot become larger than V_{ds}.

In Subsection 3.1.3 it was already stated the current shunting MOST should become a n-type MOST to achieve negative feedback. The CS stage, the current shunting NMOST, and the added capacitor $C1$ are depicted in Figure 3.6

Biasing

For the biasing current source of the CS stage an NMOST with biasing voltage at the gate is suitable. The saturation requirement also holds for the output of CS-stage in order to maintain the output impedance needed for voltage gain. So a low saturation voltage is required to enable a low minimum current for M11 while maintaining output resistance and consequently voltage gain. The output resistance of the current source should be in the same order as output resistance of the input transistor of the CS-stage.

There are two voltages available from the cascoded current mirrors to bias the current source of the CS stage. Because the current source is a N-type

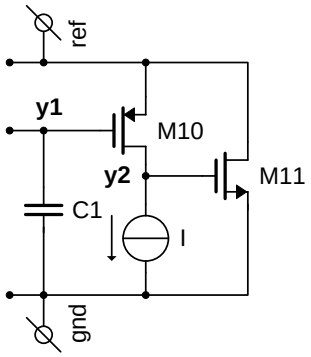


Figure 3.6: Schematic - Common-source stage with

MOST, the gate voltage from the NMOST mirror would be the simplest solution. It would only require an extra source resistor to match with the current mirror.

However, this approach has a major drawback that only became apparent after dimensioning the current mirrors for noise and output resistance at higher than room temperatures: The gate voltage level was too high, so current source NMOST was forced out of its saturation region at current levels higher than the minimum circuit requirement. Also, because the mirror voltage is temperature compensated by the source resistor and the threshold of M11 has an negative TC, the problem increased with higher temperatures.

Simply lowering the gate voltage of the mirror by degreasing the source resistance or shortening the gate length decreased the output impedance of the mirror or increased the $1/f$ noise. Increasing the width of the gate resulted in a loss of bandwidth, due to the increased gate capacitances.

Alternatively, the biasing voltage can be created from the gate voltage of the PMOST mirror. This voltage is not temperature compensated, so it has about the same negative TC as the V_{th11}. It requires a set of PMOSTs (including cascode) to copy the current from the mirror and another NMOST mirror to copy it to the CS-stage. In this case no source resistor is needed at the NMOST mirror and the gate voltage can be adjusted without affecting the mirror set that creates the reference current.

The drawback of the later approach compared to the former is the need for an extra current path. Although it turns out to be less than $1\mu A$, which is a small price compared to the current needed to keep devices in the first solution in saturation at higher temperatures.

In the next Subsection it is shown how al these circuit extensions combine to form the final circuit schematic.

3.2.3 Final circuit schematic

The final two-terminal reference stabilizer circuit is depicted in Figure 3.7

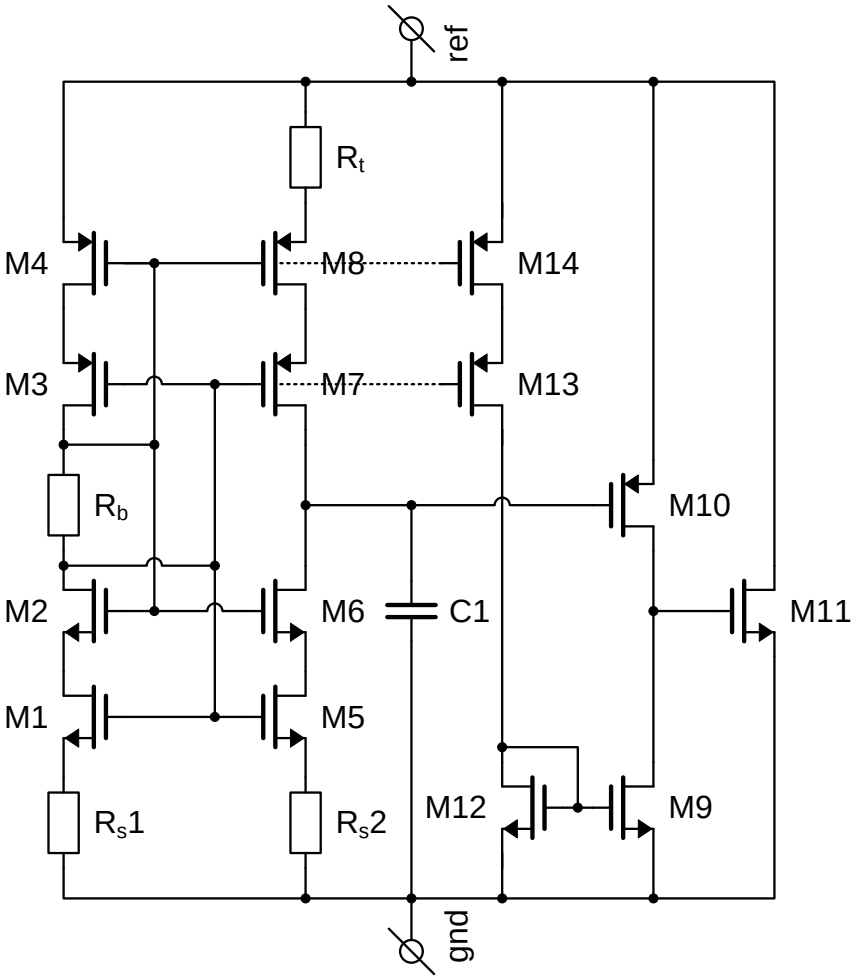


Figure 3.7: Schematic - Final circuit

3.3 Small signal analysis

This small signal analysis starts with the identification of the transfer paths in the feedback system. Then, a simplified small signal model is derived. From this model the dynamic impedance and the loop gain are derived. The dynamic impedance is an important performance characteristic of the reference stabilizer circuit and the loop gain is useful for stability of the circuit so instability (for a certain capacitive load) can be prevented. Finally, the dynamic impedance and loop gain are reduced to simplified expressions in terms of zeros, poles, and gain, in order to make a judgement on performance and stability for the different operating points.

3.3.1 Feedback analysis

The transfer of a feedback system is often expressed as the closed loop gain

$$A_{cl} = \frac{A_o}{1 - A_o \cdot \beta} \tag{3.36}$$

In the circuit of Figure 3.7 a voltage -current feedback loop as depicted by Figure 3.8 can be recognized. It consists of a transimpedance amplifier with

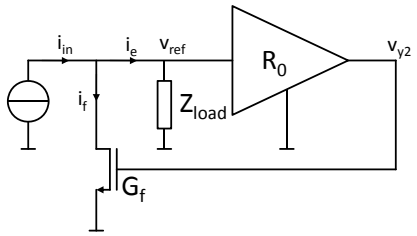


Figure 3.8: Block diagram - Voltage-current feedback

openloop transimpedance gain in the forward path ($A_o = R_o$) and a transconductance in the feedback path ($\beta = G_f$). Node voltage v_{y2} of the circuit is in this case the output of the loop. It steers the feedback transconductor M11 to shunt draft current from the input current i_{in} to minimize the (small signal) 'error' current i_e into the sensing network: the transimpedance amplifier that includes both the balanced current mirrors stage and the CS voltage amplifier stage. The load impedance Z_{load} is at the input side of the loop. So in this analysis the reference voltage v_{ref} of the circuit is mapped to the node voltage at the input of the loop and the dynamic impedance of the circuit is actually the closed-loop input impedance of the feedback model of Figure 3.8. So the voltage-current feedback loop is actually utilized to decrease the input impedance. The closed loop input impedance $Z_{in,cl}$ can also be calculated from the open loop input impedance $Z_{in,ol}$:

$$Z_{in,cl} = \frac{Z_{in,ol}}{1 + A\beta} \tag{3.37}$$

The combined term $A_o\beta$ in the denominator of (3.36) and (3.37) is known as the loop gain of the system. The loop gain of a feedback system can be determined by cutting the loop open, inject a signal in the direction of the loop and determine the output at the other end of the cut. The cut can be made at any point in the loop. For the system depicted in Figure 3.8 the loop is cut at loop output voltage node y2. So a voltage signal v_t is injected into the feedback transconductor while the output V_y2 is monitored at the output of the transimpedance amplifier.

3.3.2 Small signal model

The small signal model is created by first replacing all devices with their small signal equivalent circuits. Next negligible impedances are removed to reduce the amount of nodes and simplify calculations. In order to prevent oversimplification the transfer characteristic is compared to the results of LT-Spice

ac-simulation of the original circuit. Figure 3.9 shows the small signal model that resulted from this process.

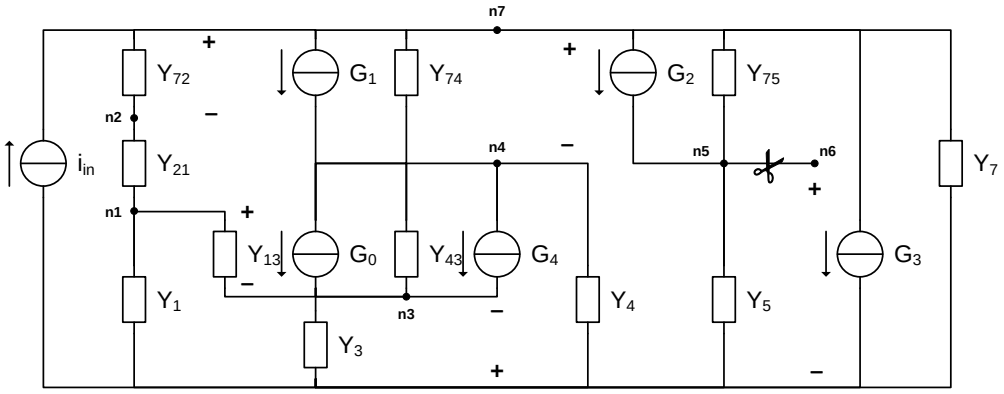


Figure 3.9: Schematic - Simplified small signal equivalent circuit

The loop has been cut open at node **5** (**y2**) by creating an extra node **6**. In case of loop gain analysis the voltage gain from node 6 to 5 is calculated while the input current is 0. In case of impedance analysis the two nodes are recombined and transfer of input current i_{in} to the voltage at node **7** ($= v_{ref}$) is calculated. The set of linear equations found by applying Kirchhoff's Current Law (KCL) to each node is expressed in matrix form $\mathbf{Av} = \mathbf{i}$, where the entries of matrix $\mathbf{A}$ represent the node-to-node transfers, vector $\mathbf{v}$ represents the node voltages and vector $\mathbf{i}$ is the input current vector.

For the impedance calculations the following matrix is used:

$$[\mathbf{A}|\mathbf{i}]_z = \begin{bmatrix} -Y_{21}-Y_1-Y_{13} & Y_{21} & Y_{13} & 0 & 0 & 0 & 0 & 0 \\ Y_{21} & -Y_{72}-Y_{21} & 0 & 0 & 0 & 0 & Y_{72} & 0 \\ Y_{13}+G_0 & 0 & -Y_{13}-Y_3-Y_{43}-G_4-G_0 & Y_{43} & 0 & 0 & 0 & 0 \\ -G_0 & -G_1 & Y_{43}+G_4+G_0 & -Y_{74}-Y_{43}-Y_4 & 0 & 0 & G_1+Y_{74} & 0 \\ 0 & 0 & 0 & -G_2 & -Y_{75}-Y_5 & 0 & G_2+Y_75 & 0 \\ 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & Y_{72}+G_1 & 0 & Y_{74}+G_2 & Y_{75} & -G_3 & -Y_{72}-G_1-Y_{74}-G_2-Y_{75}-Y_7 & -i_{in} \end{bmatrix} \tag{3.38}$$

For the loop gain calculations the unity link between nodes 5 and 6 are removed by putting all entries in row 5 to zero. Also, i_{in} is set to 0. So the matrix becomes:

$$[\mathbf{A}|\mathbf{i}]_{A\beta} = \begin{bmatrix} -Y_{21}-Y_1-Y_{13} & Y_{21} & Y_{13} & 0 & 0 & 0 & 0 & 0 \\ Y_{21} & -Y_{72}-Y_{21} & 0 & 0 & 0 & 0 & Y_{72} & 0 \\ Y_{13}+G_0 & 0 & -Y_{13}-Y_3-Y_{43}-G_4-G_0 & Y_{43} & 0 & 0 & 0 & 0 \\ -G_0 & -G_1 & Y_{43}+G_4+G_0 & -Y_{74}-Y_{43}-Y_4 & 0 & 0 & G_1+Y_{74} & 0 \\ 0 & 0 & 0 & -G_2 & -Y_{75}-Y_5 & 0 & G_2+Y_75 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & Y_{72}+G_1 & 0 & Y_{74}+G_2 & Y_{75} & -G_3 & -Y_{72}-G_1-Y_{74}-G_2-Y_{75}-Y_7 & 0 \end{bmatrix} \tag{3.39}$$

By means of gaussian-jordian elimination these matrices can be represented in row echelon form. This form provides expressions for each node voltage in terms of currents, admittances and transimpedances in the last non-zero column. This operation is performed with the help of mathematical analysis

software Maple. The results cannot be displayed in print because of their size. With the derived expression for node voltage v_7 -the reference node- from (3.38) the (closed-loop) dynamic impedance can be calculated:

$$Z_{cl} = \frac{v_{ref}}{i_{in}} = \frac{\mathbf{v}_7}{i_{in}} \tag{3.40}$$

and with the node voltages $mathbfv_5$ and $mathbfv_6$ derived from (3.38) the loop gain can be calculated:

$$A\beta = R_o G_f = \frac{v_{y2}}{v_t} = \frac{\mathbf{v}_5}{\mathbf{v}_6} \tag{3.41}$$

Transconductances and admittances

The impedances and transconductances have been combined to create node-to-node admittances and transconductances.

The transconductances are:

$$G_0 = g_{m5} \tag{3.42a}$$
$$G_1 = \frac{g_{m8}}{1 + g_{m8}\, R_t} \tag{3.42b}$$
$$G_2 = g_{m10} \tag{3.42c}$$
$$G_3 = g_{m11} \tag{3.42d}$$
$$G_4 = g_{mb5} \tag{3.42e}$$

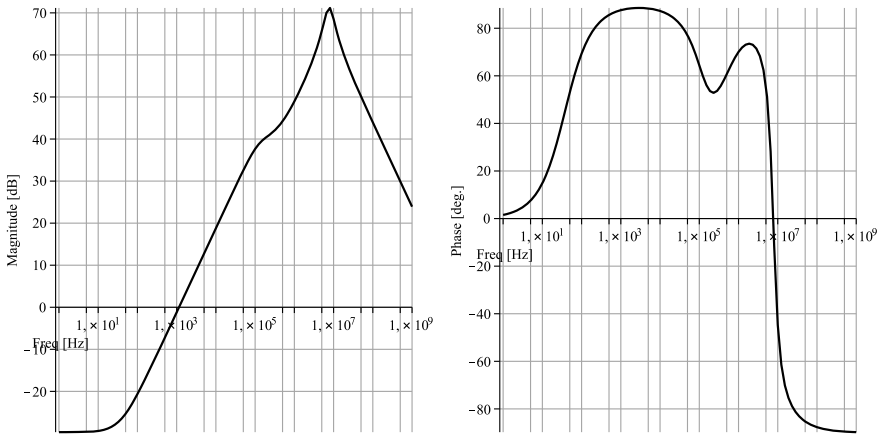
where G_1 incorperates the source degeneretion of PMOST M8 by R_t and G_4 incorperates the bulk (or back gate) effect of R_s on M5. The admittances are notated in the Laplace-domain, so in terms of the complex $s = \sigma + j\omega$:

$$Y_1 = \frac{g_{m1}}{1 + (g_{m1} + g_{mb1})\, R_s} + \frac{sC_{gs1}\ (1 + g_{mb1}\, R_s)}{1 + (g_{m1} + g_{mb1})\, R_s} \tag{3.43a}$$
$$Y_{13} = sC_{gs5} \tag{3.43b}$$
$$Y_{21} = {R_b}^{-1} \tag{3.43c}$$
$$Y_3 = {R_s}^{-1} \tag{3.43d}$$
$$Y_4 = sC1 \tag{3.43e}$$
$$Y_{43} = \frac{g_{ds5}\, g_{ds6}}{g_{m6} + g_{mb6}} \tag{3.43f}$$
$$Y_5 = g_{ds9} + sC_{gs11} \tag{3.43g}$$
$$Y_7 = g_{ds11} + sC_{load} \tag{3.43h}$$
$$Y_{72} = g_{m4} + g_{ds4} + s\,(C_{gs4} + C_{gs14}) \tag{3.43i}$$
$$Y_{74} = \frac{g_{ds7}\, g_{ds8}}{g_{m8}\ (1 + g_{m7}\, R_t)} \tag{3.43j}$$
$$Y_{75} = g_{ds10} + sC_{gd11} \tag{3.43k}$$

where Y_1 incorporates source degeneration and bulk effect of M1, Y_{43} attributes the bulk effect and cascode contribution of the output admittance of M6 to M5 and $Y74$ incorporates source degeneration and the effect of cascoding by M7 into the output admittance of M8. The load impedance is model as a capacitance in Y_7.

3.3.3 Dynamic impedance and Stability

The transfers characteristic of the dynamic impedance Z_{ref} obtained from calculating (3.40) can also be depicted by a bode plot. In Figure 3.10 such a bode plot is shown. The general shape of the magnitude plot of Z_{ref} (Figure



(a) Magnitude (b) Phase

Figure 3.10: Bode plot - Dynamic impedance

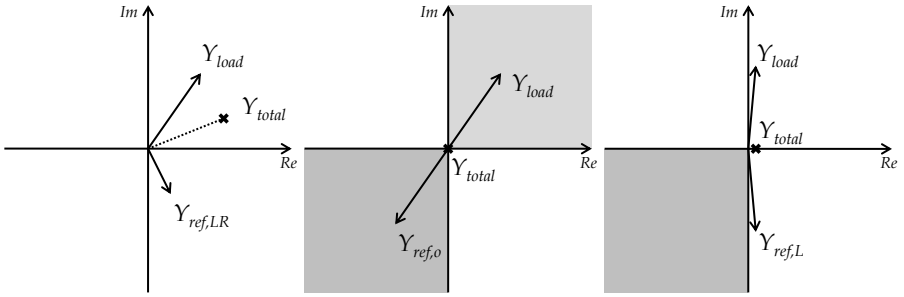
3.10a) starts with a low dynamic impedance at low frequencies. Then the dynamic impedance goes up from the first knee frequency (in this example at about 200Hz with a slope of 20dB/dec). And finally -at high frequencies- it goes down again.

Stability

Instability occurs if a system behavior is such that for some bounded input the output is unbound (goes to infinity). In this case a linearized circuit, with supply- and load impedances connected to it, is considered and instability happens if the total dynamic impedance goes to infinity, or equivalently, if the total admittance Y_{total} goes to zero. For the reference stabilizer circuit designer, the supply and load impedances are unknown: it depends on the application. Therefore it can only be assumed, or rather demanded, that the dynamic load and supply impedances are within the capacitive- and positive resistive domain. So the design can made to avoid opposite and compensating inductive and negative resistive domain.

This is illustrated by the complex admittance vector plots of Figure 3.11. The reference admittance is defined as $Y_{ref} = 1/Z_{ref}$ and the load admittance as $Y_{load} = 1/Z_{load}$. Supply impedance is ignored in this calculation. Because the two admittances are parallel connected, they can simply be vector-added to find the total admittance (Figure 3.11a). If the two admittances lay in opposing quadrants of the complex plane, zero total admittance can occur, as illustrated by 3.11b, with instability as result. If the reference admittance is kept outside the lower left quadrant by design, it cannot totally compensate the load admittance and stability for all load impedances in the upper right

quadrant is guaranteed. This is the stability criterion for the reference stabilizer circuit. So the angle of the reference admittance should remain within the -90 to +180° range.



(a) Addition of admittances (b) Zero total admittance (c) Possible ringing

Figure 3.11: Complex admittance vector plots

Even though the system is found stable for all load capacitances, it can show unwanted ringing behavior for (high) capacitive loads. Figure 3.11c illustrates this. It shows that for a mostly inductive reference admittance (close to -90°), the total admittance can become very small as both admittance approach the vertical axis, and thus approaching oscillation conditions. When inspecting the bode plot of dynamic impedance of the stabilizer, in stead of the admittance, the corresponding admittance can easily be reconstructed by flipping both the logarithmic magnitude plot and the phase around their horizontal axis. So the -90° angle becomes a maximum phase shift of +90°.

In order to avoid ringing al together the load capacitance should be smaller than the zero phase shift crossing of Z_{ref}. However, it depends on the application to determine whether this is required. Also, a smaller phase margin may be hold. The more phase margin at some frequency in the positive phase shift (inductive) area of the reference stabilizer impedance, the less ringing will occur if a capacitive load is added at the same frequency.

If the stability criterium is tested for the dynamic impedance of the reference stabilizer circuit, it should be tested for all (DC) operating conditions. The stability at all operating corners is evaluated by means of simulation and the results are presented in Chapter 4.

3.3.4 Impedance scaling factor

This characteristic should first be normalized to DC operating current and output voltage in order to become useful for performance evaluation. This normalized characteristic is called the impedance scaling factor (see subsection 1.2.3) and is calculated with (1.3).

The magnitude plot of ZS has the shape as the plot of Z_{ref}, but is scaled (shifted on the logarithmic axis) such that the 0 level represents the DC V_{REF}/I_{op}. The magnitude of the transfer characteristic ZS is shown in Figure 3.12. Assuming that the upward and downward slopes are +/- 20 dB/dec, the simplified shape of the impedance scaling characteristic can be desribed by three numbers. The low-frequency impedance gain for the floor ZS_{LF}, the

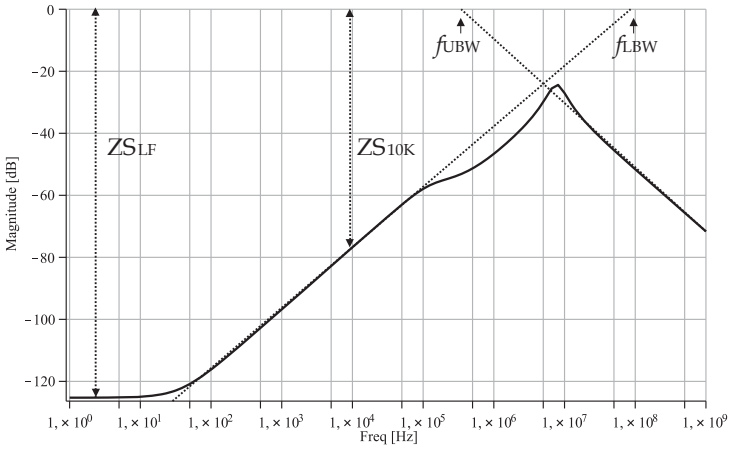


Figure 3.12: Magnitude plot - Impedance scaling factor

extrapolated 0 dB intersection frequency for lower bandwidth slope f_{LBW}, and the extrapolated 0 dB intersection frequency for upper bandwidth slope f_{UBW}.

Besides these three numbers another number is indicated in the Figure 3.12: the impedance scaling at 10 kHz ZS_{10K}. This seems to overlap with the f_{LBW} figure, however the first order slope assumption of 20 dB/dec doesn't hold for all systems and the most important region for stabilizer applications is assumed to be near the 10 kHz band.

ZS_{LF} and f_{LBW} or ZS_{10K} can be calculated with some simple approximations that are helpful for finding the appropriate dimensions of the design.

Low frequency impedance scaling

At low frequencies a couple of simplifications can be applied to the small signal model by removing capacitances to approximate the ZS gain and f_{LBW} with a relatively simple expression.

First of all; admittance Y_{13}, the gate-source capacitance of M5, can be omitted. This allows for the elimination of node 3 such that the transconductance and admittance from node 4 to ground (with contributions from M5, M6, R_s and $C1$) can be simplified:

$$G_0' = \frac{g_{m5}}{1 + (g_{m5} + g_{mb5})R_s} \tag{3.44}$$

$$Y_4' = \frac{g_{ds5} \cdot g_{ds6}}{(1 + (g_{m5} + g_{mb5})R_s)(g_{m6} + g_{mb6})} \tag{3.45}$$

The gate-source capacitances can also be removed from Y_1 and Y_{72}:

$$Y_1' = \frac{g_{m1}}{(g_{m1} + g_{mb1})R_s} \tag{3.46}$$

$$Y_{72}' = g_{m4} + g_{ds4} \tag{3.47}$$

The low frequency impedance scaling factor can simply be estimated by the assuming that approximately all small signal current is supplied by the large

transconductor G_3, while this current is steered by v_5, an amplification of v_{ref} with voltage gain A_v. So

$$ZS_{LF} = \frac{v_{ref}}{i(v_{ref})} = \frac{1}{G_3 \cdot A_v} \tag{3.48}$$

Voltage gain is obtained over two stages: A_{v1} from node **7** (**ref**) to node **4** and A_{v2} from node 4 to node 5. Both can be expressed with the simplified admittances and transconductances, where admittances Y_1', Y_{21}, and Y_{72}' form a resistive voltage ladder that provide the voltage division of v_{ref} to steer G_0' and G_1:

$$A_{v1} = \frac{G_1 \cdot \frac{{Y_{72}'}^{-1}}{{Y_1'}^{-1}+Y_{21}^{-1}+{Y_{72}'}^{-1}} - G_0' \cdot \frac{{Y_1'}^{-1}}{{Y_1'}^{-1}+Y_{21}^{-1}+{Y_{72}'}^{-1}}}{Y_4' + Y_{74}} \tag{3.49}$$

$$A_{v2} = -\frac{G_2}{Y_{75} + Y_5} \tag{3.50}$$

After replacing these equation into (3.48), an estimate of the low frequency impedance scaling factor is found:

$$ZS_{LF} \approx \frac{1}{G_3} \cdot \frac{Y_4' + Y_{74}}{G_1 \cdot \frac{{Y_{72}'}^{-1}}{{Y_1'}^{-1}+Y_{21}^{-1}+{Y_{72}'}^{-1}} - G_0' \cdot \frac{{Y_1'}^{-1}}{{Y_1'}^{-1}+Y_{21}^{-1}+{Y_{72}'}^{-1}}} \cdot \frac{Y_{75} + Y_5}{G_2} \tag{3.51}$$

Impedance scaling bandwidth

The LBW frequency can be found by combining this ZS_{LF} gain with the first knee frequency f_{z1} that corresponds to the dominant zero in ZS.

$$f_{LBW} = f_{z1} \cdot 10^{-(ZS_{LF}[dB])/20} \tag{3.52}$$

Where f_{z1} is linked to node **4** (**y1**), the first gain stage. The cut-off frequency can be estimated by calculating the total resistance R_{n4} and the total capacitance C_{n4} to ground form this node. The first knee frequency can therefor be expressed in terms of admittances Y_{74} and Y_4' of the simplified small signal model, which connect to this node:

$$\begin{aligned} f_{z1} &\approx \frac{1}{2\pi \cdot R_{n4} \cdot C_{n4}} \\ &\approx \frac{\mathfrak{Re}\{Y_4'\} + Y_{74}}{2\pi \cdot \mathfrak{Im}\{Y_4'\}} \\ &\approx \frac{\frac{g_{ds5} \cdot g_{gds6}}{(1+R_s(g_{m5}+g_{mb5}))(g_{m6}+g_{mb6})} + \frac{g_{ds7} \cdot g_{gds8}}{(1+g_{m7} \cdot R_t)g_{m8}}}{2\pi \cdot C1} \end{aligned} \tag{3.53}$$

The upper bandwidth frequency corresponds to the 0dB crossing frequency of total capacitance to ground impedance at node **ref**, after scaling. So

$$f_{UBW} = f_{Z,C_{REF}} \cdot \frac{I_{OP}}{V_{REF}} \tag{3.54}$$

with

$$f_{Z,C_{ref}} = \frac{1}{2\pi C_{ref}} \tag{3.55}$$

The same operating corners as discussed in Subsection **??** have to be taken in consideration while evaluating the design with these performance metrics.

3.4 Noise considerations

With the insight gained from the small sign analysis of the previous Section the noise contributions of devices and resistors to the output reference voltage can be estimated.

If the loop is cut at the reference voltage node it becomes clear that noise from the first stages is amplified the most by the high loop gain. So noise produced by the devices of the active current mirrors: M1, M4, M5, and M8, are clear suspects for low-frequency $(1/f)$ noise contributions. However, M8 is expected to have the smallest contribution because of its large dimensions compared to the other devices. Also, the wide band noise sources can be found in this stage of the circuit; resistances Rs1, Rs2 and Rt are 'prime suspects' for their thermal noise contributions, but also the thermal noise from the active current mirror devices have a significant contribution.

The noise analysis tools from LT Spice and Cadence are used to evaluate the output referred noise and the individual contributions of the devices of this design and the design is modified to meet the requirements set in Chapter 1.

With the general noise models of resistors and MOSTs the required modifications are estimated and the design is adjusted accordingly. The dimensioning of the circuit is conducted in several iteratations, because the dimensions of the devices as well as the resistor values, determine the large and small signal behavior as well. The device noise models that were used for this thesis are described in Chapter 7 of [5].

Chapter 4

Simulation

This Chapter reports on the simulation results for the characterization of the stabilizer circuit. The first Section discusses the circuit model that was used. The second Section discusses the method of analysis and reports the results obtained for each characteristic. In the final Section of this Chapter these results are evaluated.

4.1 Circuit model and test bench

The final circuit design of Figure 3.7 has been modeled with both LT Spice and the Cadence Virtuoso Schematic editor. Most simulation results presented in this Chapter have been produced with Cadence, because the Spectre simulator of Cadence provides more setup options and includes flicker noise in its noise analysis. Also, the schematic could more easily be equipped with process library models for (non-ideal) passive components. The Cadence final schematic is stored as cell 'shuntstabi_real' in the 'stabi2'library. This schematic is depicted in Figure 4.1.

In this circuit, the NMOST and PMOST devices are represented by the N_18_MM and P_18_MM models from the model library of the UMC .18μm mixed-mode CMOS process technology. For capacitor $C1$ the 'NCAP_MM' gate-capacitor component model is used and for the resistors the 'RNHR1000' high ohmic resistance component model is used. Both component models have an extra terminal, which is connected to substrate, because these models include parasitics to substrate in order to describe more realistic electral behavior.

The multiplying factor m_p of PMOST M8 is implemented by a nested cell 'P_18_MM_x_10'. Which was created for the occasion, because the library model does not support the multiplier parameter.

For characterization purposes, the design model is embedded in a test bench model. Besides the design, the test bench contains an ideal current source and an ideal load capacitor. It is stored in the cell 'tb_shuntstabi_real_current_cload' as part of the 'stabi2' library. Figure 4.2 shows the schematic of the test bench.

The setup for each simulation is done with the Virtuoso Analog Design Environment (ADE). A number design variables are inserted in place of static instance parameters for easy manipulation of both the design and test bench with the ADE tool.

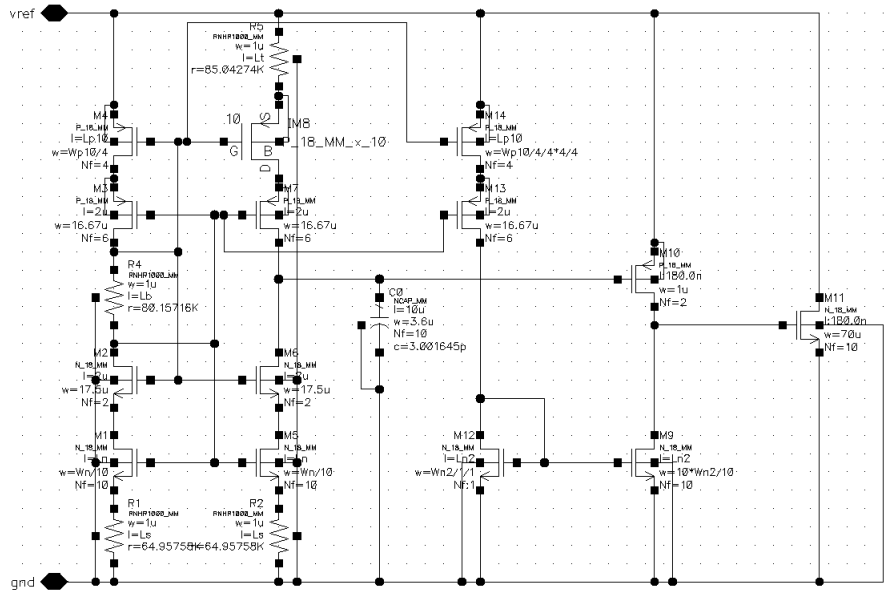


Figure 4.1: Schematic model - Stabilizer circuit

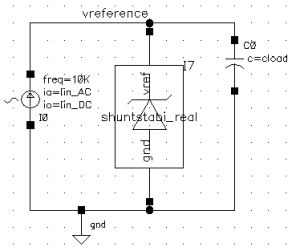


Figure 4.2: Schematic model - Test bench

The dimensioning of the components has been an iterative process starting with the considerations discussed in the previous Chapter and evaluating the characteristics by means of simulation. In this Chapter the final performance characteristics are presented and if possible the corresponding dimensioning considerations are explained.

4.2 Characterization by simulation

4.2.1 Typical circuit behavior

Unless otherwise specified the typical operating conditions for the simulations discussed in this section are $T = 27°C$, $I_{op} = 100\mu A$ (with a 10% AC component) and $C_{load} = 10pF$. Also the typical sections of the library models are used (e.g. 'tt' or 'typ').

DC Current to Voltage transfer characteristic

'DC Analysis' is used to characterize of the DC current to voltage transfer of the circuit. A logarithmic sweep of input variable I_{op} over a range of $0.1\mu A$ till $500mA$ with a 100 points per decade is setup. The simulation output is the reference voltage, selected in the ADE by the expression 'VS("/vreference")'.

The result of this simulation is shown in Figure 4.3. A number of cursor points have been added to show the approximate values at points of interest.

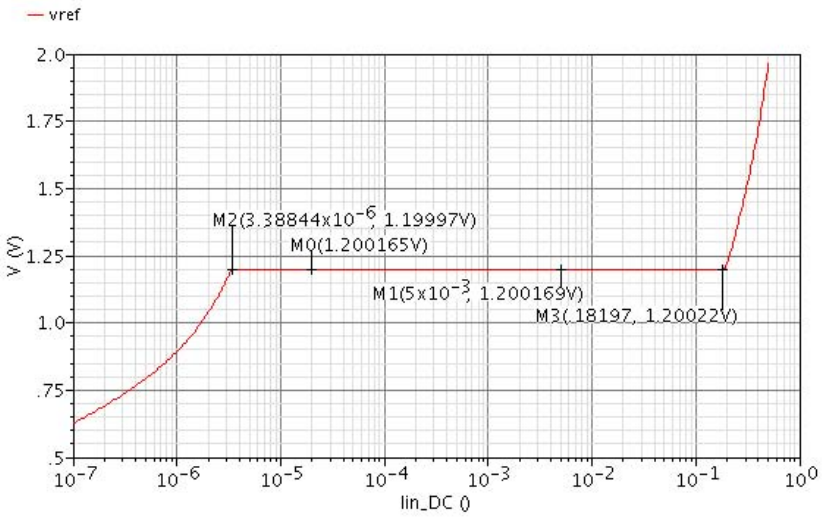


Figure 4.3: DC transfer characteristic - Reference voltage vs. input current

A number of observations can be made from this graph: the operating current range for which the reference voltage is 'flat' stretches from $3.39\mu A$ till $181mA$, that's about a factor of fifty thousand or more than 4 orders of magnitude ($10^{4.7}$); the voltage difference over this range is $-1.19997+1.20022 \approx 250\mu V$; and the voltage difference over the specified current range of $20\mu A$ till $5mA$ is $-1.200165 + 1.200169 \approx 4\mu V$.

These characteristics are the result of the incorporating the following considerations to the dimensioning the design: The W/L of M11 is set for a very large g_m and enable it to shunt the high maximum operating current within the voltage headroom ($V_{gs11,max} = V_{REF} - V_{ds10,sat}$).

The current mirrors are dimensioned for a reference current of $1.5\mu A$ per path such that along with current through the common-source stage the total the quiescent current is about $8uA$, this leaving enough headroom within the minimal operating current to ensure the saturation operation of M9 at the specified minimum operating current of $20uA$. This includes headroom for the NTC drain current of M11 due to the PTC quiescent current and the NTC threshold of M11, because both mechanisms lower the V_{ds} of M9.

Note that the saturation of M9 is not mandatory for stabilization operation: a minimum of $3.4\mu A$ operating current is sufficient. In this case the CS stage shunts currents excessive of 2 times the reference current plus the current needed for biasing the CS stage while M11 is switched off. However, the high

output impedance obtained by saturation and consequently the higher gain of the CS stage and high g_m of M11 offer better wide band supply rejection and is therefore considered 'normal' operation.

The analysis of Sections 3.1 and 3.2 are used to dimension for the $1.5\mu A$ reference current and the related 1.2V reference voltage. The aspect ratios of the gates of the NMOST mirror is set at 1 and the gates of PMOST are scaled to match the current factor. M8 is set in WI operation, so reference is well defined with trimming resistor ($\propto 1/R_t$) in stead of ($\propto 1/R_t^2$) and the reference current has a approximately linear PTC.

The cascode stages are operated in WI aswell, this minimizes their saturation voltage ($V_{ds,sat,WI} \approx 2nU_T \approx 75mV$) and allows low voltage operation.

Dynamic impedance

This 'AC analysis' is setup with a AC input current source frequency sweep from 0.1 till 100GHz with 20 points per decade, in order to find the dynamic impedance characteristic. The capacitive load is removed to characterize only the impedance of the stabilizer circuit. Since the AC current has unity amplitude for this analysis, the dynamic impedance is set as 'VF("/vreference")/1' as simulator output. The magnitude ('dB20') and phase plot that describe the frequency response of Z are depicted in Figure 4.4

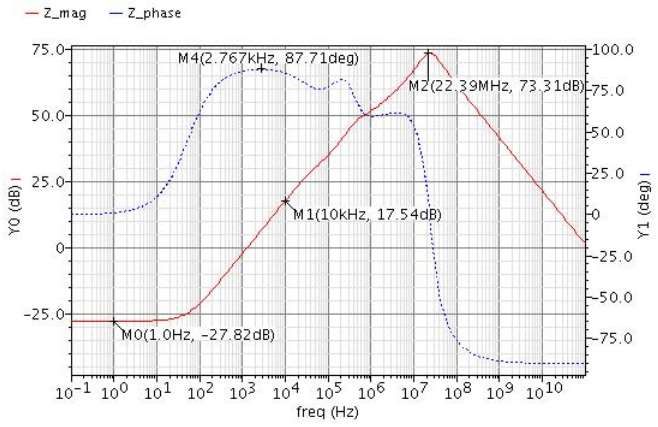


Figure 4.4: Frequency response characteristic - Dynamic Impedance at $I_{op,dc} = 100\mu A$

The dynamic impedance is normalized in accordance with (1.3) in order to characterize the dynamic behavior for the entire operating current range. With the ADE the impedance gain or scaling factor ZS is calculated from the Z by 'dB20((VF("/vreference") / (VS("/vreference") /(-1 * IS("/I0/Minus")'. The frequency response of ZS for current levels of $20\mu A$, $100\mu A$, and $5mA$, is shown in Figure 4.5.

In Subsection 3.3.3 two spots in the ZS transfer are marked as particulary interesting for characterization: 1 Hz for low frequency performance and 10kHz for bandwidth performance. So for this simulation the same calculation is used,

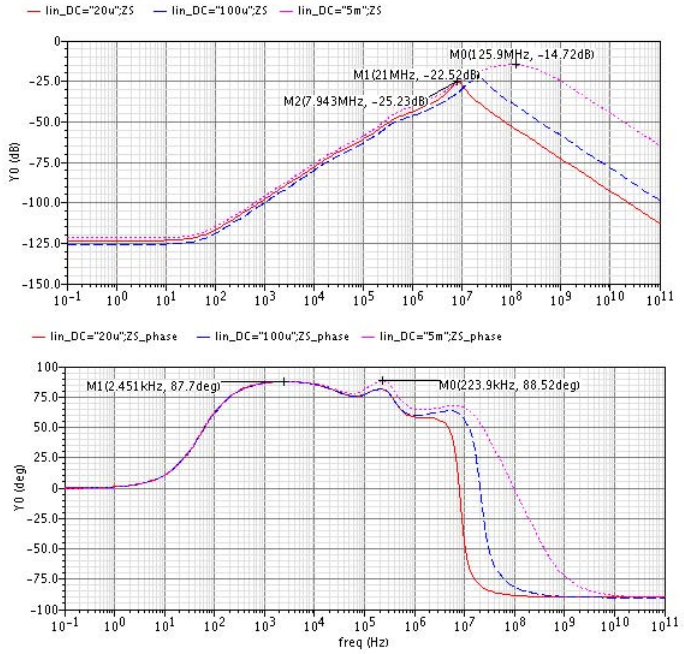


Figure 4.5: Frequency response characteristic - Impedance scaling at $I_{op,dc} = \{20\mu A, 100\mu A, 5mA\}$

but this time a DC current sweep is setup instead of a frequency sweep. The resulting AC-DC (or rather ZS-I_{op}) characteristic is shown in Figure 4.6.

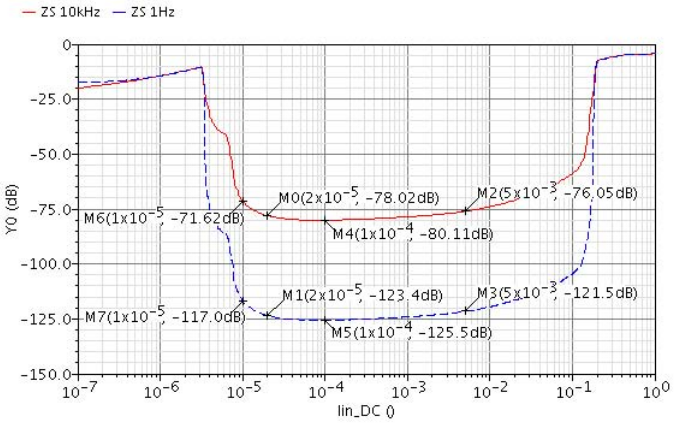


Figure 4.6: AC-DC characteristic - Impedance scaling at $f = \{1Hz, 10kHz\}$

The most important numbers that can be read from this figure are that the stabilizer has a peak performance at $100\mu A$ of -125dB ZS at low frequencies and -80dB at 10 kHz, while within the $20\mu A$ till $5mA$ operating range ZS is lower than -121dB and -76dB respectively.

M10 of the CS-stage is set in its WI region for maximum g_m. The amount of biasing current required for this stage is determined by the output impedance and g_m levels it is required to generate. The bandwidth and stability of the circuit are mostly determined by the impedances at the input and output nodes of this stage. This is discussed in more detail at the next Subsubsection.

Stability

From the phase characteristics of Figure 4.4 it can be concluded that the impedance and thus admittance remains within +/- 90°, therefore the real part of the impedance remains positive, so stability for each capacitive/resistive load is maintained according to the stability criterion discussed in the previous Chapter. However, for high load capacitances, the stabilizer shows ringing behavior. The closer the phase of Z_{ref} approaches +90° phase shift (inductive impedance) the stronger the ringing will be is, if the load capacitance is matched to this inductance. The effect of capacitive loading is illustrated by Figure 4.7. The phase shifts marked in this Figure show the margin with respect to +90°

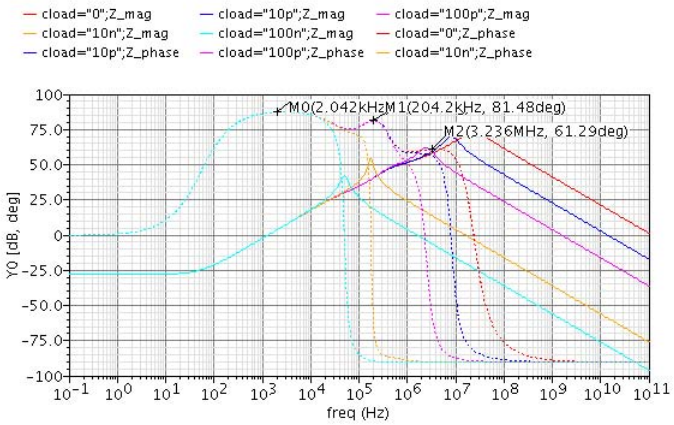


Figure 4.7: Frequency response characteristic - Dynamic impedance - Load capacitor at $I_{op} = 20\mu A$

In order to stay within the +/- 90° phase constrain, the resistive and capacitive impedances of nodes **y1** and **y2** need to be designed properly such that the consecutive zeros and poles have the proper distance and ringing is limited for large capacitors.

The distances between the pole of **y1** and the first zero of **y2** and the pole of **y2** are of particular interest. The behavior of node **y2** is set by the biasing current and the voltage level swing needed to steer M11. Also C_{gs5} plays a part in this region, the zero it introduces cannot be shifted up easily due to noise requirements. The pole and zero of y1 is easily steered with $C1$. The dominance of this node is required to ensure overall stability.

Transients

The switching behavior of digital circuits cause transients on the supply of a system. Without any additional circuits the stabilizer would have a response as depicted by Figure 4.8, for a nearly block shaped waveform with $100ps$ rise and fall time (linear edges) and an amplitude that is 10% of the DC supply current. For this analysis a $10pF$ capacitive load is assumed. The Figure shows plots for three different DC current levels.

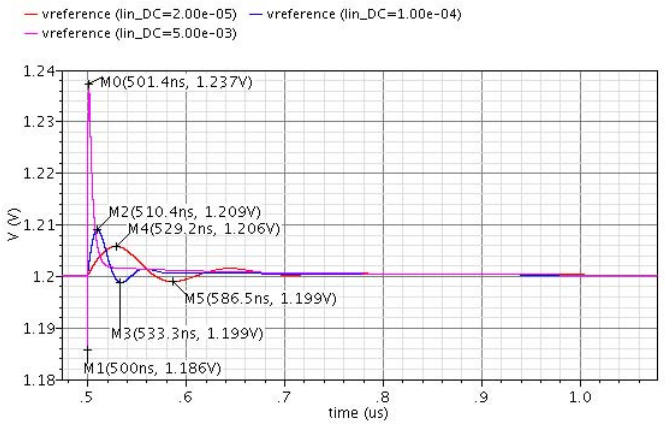


Figure 4.8: Transient response - Stabilizer circuit - for $I_{op,dc} = \{20\mu A, 100\mu A, 5mA\}$

The bandwidth of the voltage stabilizer circuit is limited, so for better stabilization at higher frequencies additional circuitry is required. For instance: a low-pass passive filter with a 20kHz cut-off frequency would make the impedance scaling at least -70dB over the entire frequency range. An on chip RC-filter at the output is a feasible implementation of such a filter: it would require a resistor and a capacitor of for instance $80k\Omega$ and $100pF$. Figure 4.9 shows the response of the stabilizer with the described output filter.

The peaks are significantly reduced by the RC-filter and no ringing occurs. The filter can be a useful addition. But, whether to add an RC-filter or not depends not only on the supply conditions, but also on the loading conditions. In case of a resistive load, for instance, because the voltage divider that arises could cause a unwanted voltage drop at the output.

Noise analysis

The noise analysis simulation is set for a logarithmic frequency sweep from 0.1 till 100GHz with 100 points per decade. With the output noise voltage defined as the voltage on the reference node ('/vreference') with respect to ground ('/gnd').

From the simulation results a spectral noise density plot is obtained. Also, by means of the 'Noise summary' tool of the ADE, the integral noise is calculated and the most significant noise contributors are identified. The spectral noise density plot is shown in Figure 4.10. The spectrum is marked by cursors

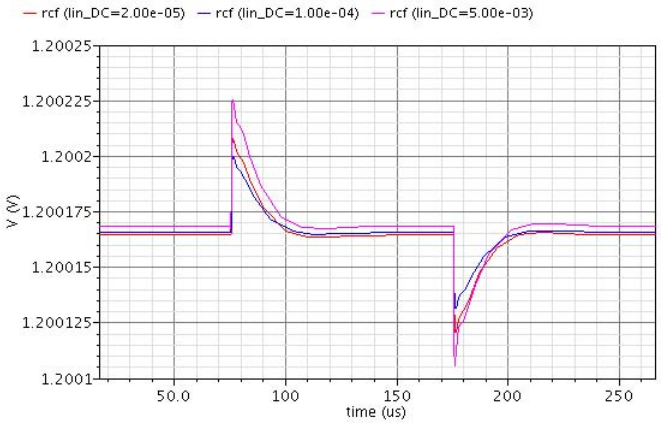


Figure 4.9: Transient response - Stabilizer circuit with RC-filter - for $I_{op,dc} = \{20\mu A, 100\mu A, 5mA\}$

at a points of interest: The noise density at $1kHz$ for the wide band noise density figure $N_V|_{f=1kHz}$; and $\sqrt{2} \cdot N_V|_{f=1kHz}$, indicating the noise corner frequency.

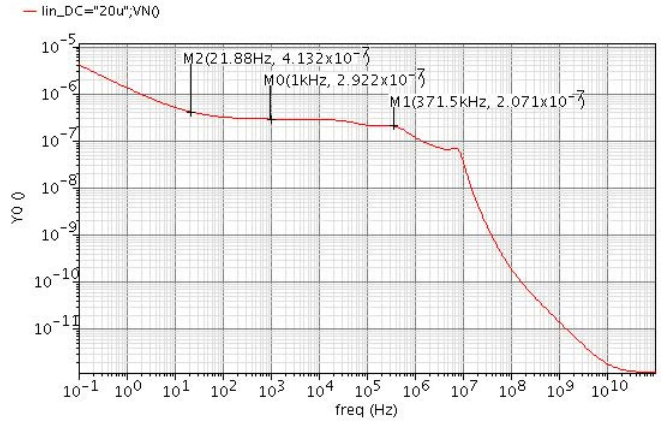


Figure 4.10: Spectral noise density plot - Output noise voltage

The wide band noise density level is $N_V|_{f=1kHz} \approx 292nV/sqrtHz$ and the corner frequency is $f_{c,N} \approx 22Hz$. This corresponds to the integral noise of at low frequencies of $e_N|_{f=0.1..10Hz} \approx 2.98\mu V_{RMS} \approx 19.7\mu V_{pp}$, found with noise summary. This matches to the relation of (1.5) between low frequency and wide band noise.

The main contributors ($> 10\%$) to LF integral noise are: M5 (42.5%); M4 (24.2%); and M1 (22.0%). The main contributors ($> 10\%$) to wide band noise density (spot noise at $1kHz$) are: R_t (23.7%); R_{s2} (22.8%); M4 (17.6%); and R_{s1} (11.8%).

Remark: These results on noise performance are somewhat unreliable, because ProMOST (single transistor simulation tool) warns for possible model pa-

rameter incorrectness while loading the 'MM180_REG_V124- -N' BSIM3 model, because of negative flicker noise at $vds = 0$, $vgs = 1$. Unfortunately, this is the only model available for this device.

As indicated by Section 3.4, the dimensions of the mirror had to be scaled up to the order of tens of microns in order to obtain the required noise performance.

4.2.2 Temperature

While investigating the effect temperature has on circuit behavior, at first a typical circuit is assumed. In the subsequent Subsection of this Section non-typical circuit models will be considered.

The DC voltage-temperature characteristic is obtained with DC Analysis with sweep variable temperature going from -40°C till 125°C. The result is shown in Figure 4.11. According to the box method of (1.2) the TC is 67$ppm/°C$.

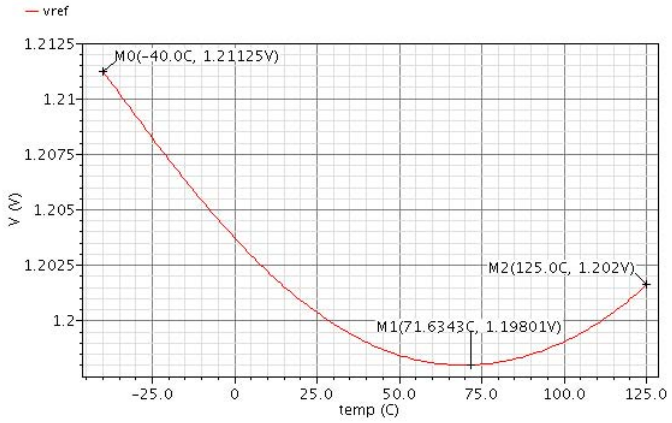


Figure 4.11: DC Temperature characteristic - Reference voltage at $I_{op,ac} = 20\mu A$

The dynamic characteristics of Figure 4.6 can be simulated for other temperatures by performing a 'Parametric Analysis' from the ADE. A parametric set is used with variable name 'temp' and value list '(-40 27 85 125)'. ZS at 1Hz is shown in Figure 4.12 and ZS at 10kHz is shown in Figure 4.13

With increased temperature dynamic performance decreases, especially at low operating current levels. At $I_{op,dc} = 20uA$ the performance loss for 125°C is about 15dB compared to room temperature performance. At $I_{op,dc} = 10uA$ it's 30dB. For a operating temperature of 85°C the loss is less severe: about 5dB at $I_{op,dc} = 20uA$ and 15dB at $I_{op,dc} = 10uA$.

The plot of Figure 4.14 illustrates this observed relation to temperature of ZS in more detail by means of a temperature sweep. It shows the impedance scaling at 10 kHz AC input for the entire temperature range at different current levels. This Figure clearly shows that at low operating current levels like $20\mu A$, impedance scaling degenerates with the increasing temperature with an increasing slope. While at high current levels de slope decreases with higher temperature.

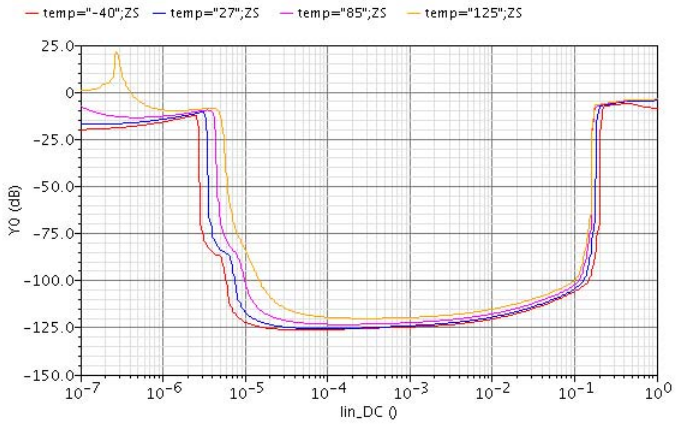


Figure 4.12: AC-DC characteristic - Impedance scaling at $f_{I_{op,ac}} = 1Hz, T = \{-40, 27, 85, 125\}°C$

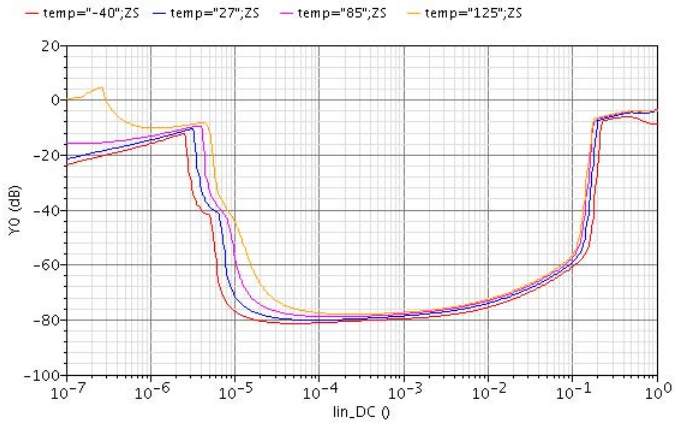


Figure 4.13: AC-DC characteristic - Impedance scaling at $f_{I_{op,ac}} = 10kHz, T = \{-40, 27, 85, 125\}°C$

4.2.3 Production spread characterization

A number of characterizations are reexamined for process corner analysis. A process corner is by selecting the appropriate section of the process library in the 'ADE'>'Setup'>'Model Library' dialog box.

First just the MOST models are considered. The models are in library file 'MM180_REG18_V124.lib.scs' and contain sections: ss,tt,ff,snfp, and fnsp, for slow, typical, and fast NMOSTs and PMOSTs. In order to incorporate temperature corners as well, the DC characterization of Subsection 4.2.2 is done for all the available model sections. The results are depicted in Figure 4.15.

From this plot it can be concluded that the 'ss' corner has the largest positive voltage shift and 'ff' the most negative, both about 75mV at room temperature.

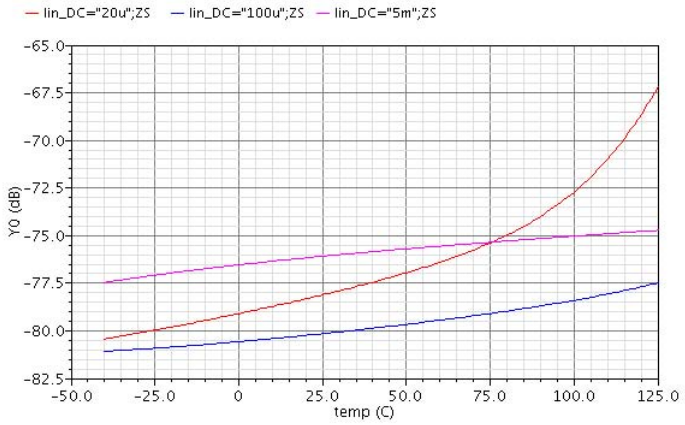


Figure 4.14: AC-DC characteristic - Impedance scaling at $f_{I_{op,ac}} = 10kHz, I_{op,dc} = \{20\mu A, 100\mu A, 5mA\}$

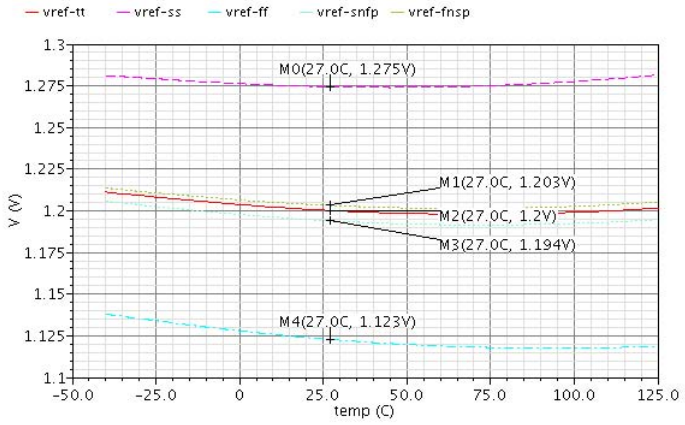


Figure 4.15: DC characteristic - MOST corners - Reference voltage at $I_{op,ac} = 20\mu A$

Next, the resistor model is considered. The model is located in library file 'MM180_RES_V133.lib.scs' and contains sections: res_min, res_typ, and res_max for minimum, typical and maximum resistances. The same characterizations are used, so temperature corners are considered. The results are depicted in Figure 4.16. From this plot it can be concluded that the 'res_min' corner has a positive voltage shift of about 84mV and 'res_max' a negative shift of about 54mV at room temperature.

Now, the most extreme corners of the independent MOST and resistor corners are combined. So 'ss' with 'res_min' and 'ff' with 'res_max'. The DC characteristic of Figure 4.19 shows the maximum voltage error of the circuit. At room temperature the maximum voltage shift due to process spread is +164mV incase of the 'ss-res_min' corner and -128mV incase of the 'ff-re_max' corner.

The dynamic performance -in terms of impedance scaling at 10kHz- at these

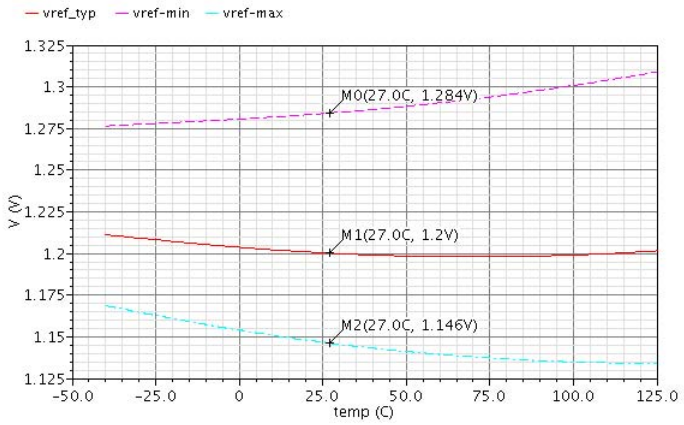


Figure 4.16: DC characteristic - Resistor corners - Reference voltage at $I_{op,ac} = 20\mu A$

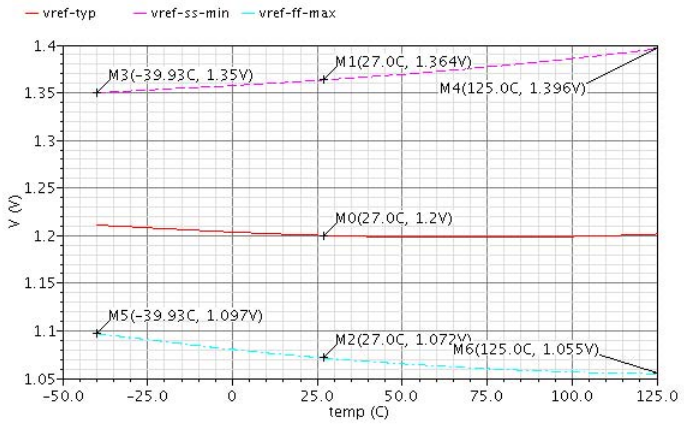


Figure 4.17: DC characteristic - MOST and resistor corners - Reference voltage at $I_{op,ac} = 20\mu A$

corners is depicted in Figure 4.18.

In this plot it can be seen that the 'ff-res_max' corner has 3dB to 5dB impedance scaling loss.

These deviations in reference voltage, TC, and impedance scaling require more attention. In the next Subsection one method for compensating this initial inaccuracy is investigated: resistor trimming.

Mismatch is not considered because the devices in the current mirrors are relatively large.

4.2.4 Trimming

In this subsection the use of resistor trimming of this stabilizer circuit is evaluated. The aim of trimming is to optimize the (initial) accuracy of the reference

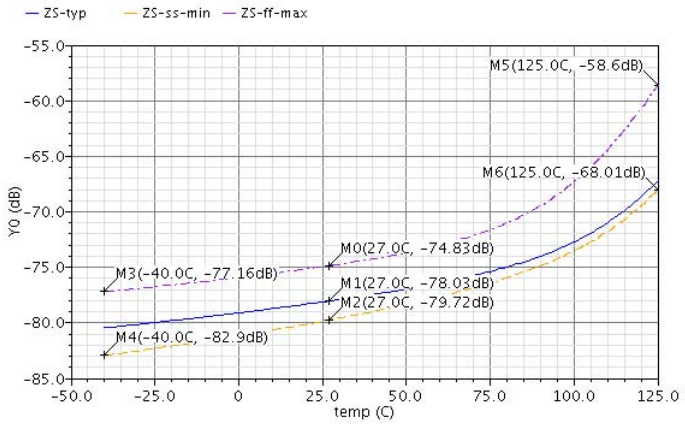


Figure 4.18: AC-DC characteristic - MOST and resistor corners - Impedance scaling at $f = 10kHz, I_{op,dc} = 20\mu A$

voltage by adjusting R_t or in this case the length of R_t: L_t. The R_t is found to be most suitable for trimming because of the sensitivity of the current transfer of the PMOST mirror to this resistance: it relates approximately $1/R_t$.

First a L_t sweep from for DC analysis is performed in order to evaluate the effect of L_t and thus R_t on the dc reference voltage level for the process corners. The result of this analysis is shown in Figure 4.19.

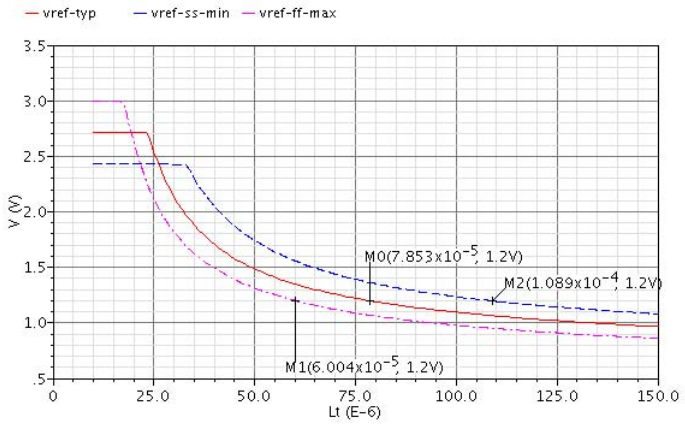


Figure 4.19: DC characteristic - Trimming of R_t - Reference voltage at $I_{op,ac} = 20\mu A$

From this plot the required trimming range can be found such that the reference voltage level can be calibrated to 1.2V at room temperature: from $60.04\mu m$ for 'ff-res_max' till $108.9\mu m$ for 'ss-res_min'.

The next step is to apply these trimming values and evaluate temperature dependence and dynamic performance. Again a temperature sweep is applied. The results are shown in Figures 4.20 and 4.21, and can now be compared to Figures 4.19 and 4.18 in order to evaluate the resistor trimming approach.

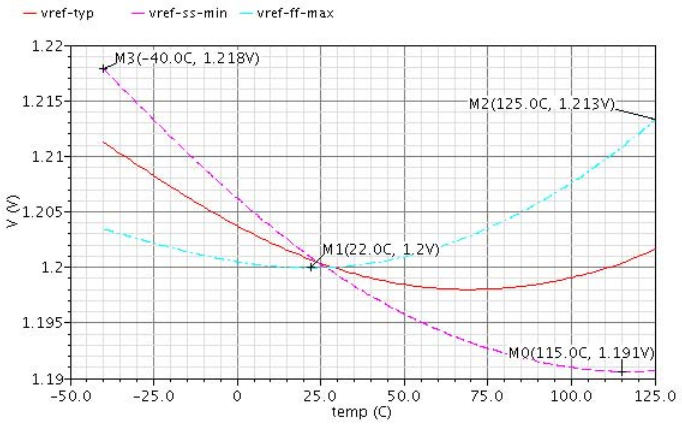


Figure 4.20: DC characteristic - Trimmed - Reference voltage at $I_{op,ac} = 20\mu A$

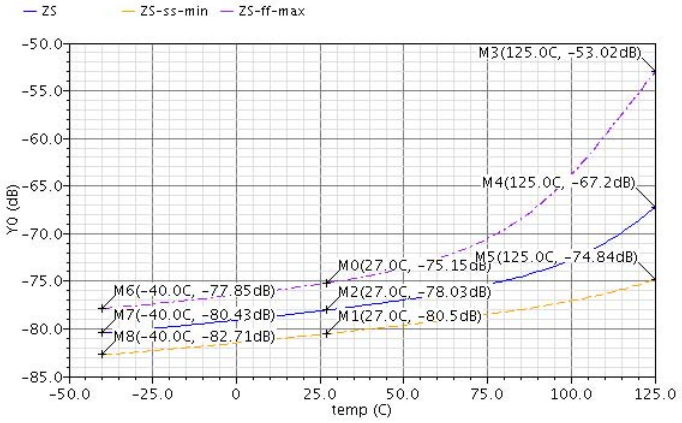


Figure 4.21: AC-DC characteristic - Trimmed - Impedance scaling at $f = 10kHz, I_{op,dc} = 20\mu A$

Note that, in this evaluation, trimming is emulated by scaling the resistor length. This is not a realistic method of trimming. A trimming network should be designed in order to estimate the performance after trimming more accurately. Such a network could be calibrated during production by for instance laser trimming or during the testing fase, by programming programmable cells. Another option is a self calibrating system as discussed in Chapter 2.

4.3 Evaluation

Although stability is ensured by the maximum phase shift constrain, capacitive loading can cause ringing effect. In order to suppress this effect C1 can be increased to shift the dominant pole, but this comes at the cost of bandwidth. The effect of transients on the circuit have been simulated and the use of an RC-filter has been evaluated.

The relatively 'high' noise contributions of the devices at the current mirror stages is a result of current noise generated by the source resistors and mirror devices combine with the high output impedance of the cascode stage. In order to achieve the noise specifications set by the requirements of Table 1.1, the device had to be scaled up significantly. These large devices have large parasitic capacitances, especially C_{gs} of M5 put a constrain on the bandwidth of the stabilizer. Although devices are big, the total chip area remains 'bond-pad limited'. For a system that achieves both high bandwidth an low noise with more die area efficiency, a multistage approach is advised. Bandwidth and low noise would then be achieved in separate stages. Both stabilizer stages can have the same concept as discussed in this thesis. However, such a design cannot be of the two-terminal (or shunt) type, a third terminal is required to separate the input from the output stage. The process spread that leads to inaccuracy, can be partially compensated by trimming of R_t.

The final dimensions of the components are included in Appendix B.

Chapter 5

Conclusions

The reference voltage stabilizer concept and the derived circuit presented in this thesis show performance characteristics in simulation that compare well to the low-voltage ($< 2V$) products currently on the market in terms of supply rejection, noise and operating current range. Because of these characteristics and the simple two terminal form factor a wide range of applications is foreseen.

This concept does not lean on the PTAT current properties of two current-density scaled p-n junctions (e.g. diode connected (parasitic) bipolar devices) like the bandgap reference does –which is most common in this market segment. However, the circuit implementation of this concept does manage to maintain enough temperature stability over the -40 to $125°C$ operating temperature range, by means of internal compensation, to maintain good supply rejection operation (impedance scaling at 10kHz of at least -53dB) and a near 1.2 Volt reference output level (maximum difference of $27mV$ over the entire temperature range). Mind that these figures are estimated for *worst case* scenarios, after calibration.

If a more typical scenario is considered, the performance figures become as follows: the input current range extends from $3.4\mu A$ untill $180mA$. That's over 4 orders of magnitude; the impedance scaling (the proposed figure-of-merit for power supply rejection by two-terminal devices) is -76dB at 10 kHz, meaning it has the highest bandwidth performance over a wide $20\mu A$ - $5mA$ operating current range; the low frequency impedance scaling is -121dB over the same current range; the low frequency noise is estimated to be less than $20\mu V_{p-p}$ at room temperature; the wide band spectral noise density is about $300nV/\sqrt{Hz}$; and the maximum voltage difference over the operating temperature range is typically 13mV.

The are a number of limitations that need consider while designing or applying the circuit: In order to establish good initial accuracy it is required to calibrate the circuit. Resistor trimming is expected to be a suitable method. Ringing is a concern for low operating currents with high capacitive loads. Therefore a certain minimum operating current, depending on the load, should be retained in order to circumvent to much ringing or instability.

So the design features are: very good supply rejection for low voltage applications; Competing noise performance; a very simple two terminal form factor that is makes easy to apply to different circuits as supply regulator or bias; it is all basic CMOS, nothing exotic, and therefore suitable for SoC integration;

and it is easily adjustable -trimming can also be used to achieve other than 1.2 V reference levels-.

The recommendations for further research and design can be summarized in three steps. First, trimming should to be implemented for initial accuracy needs be implemented, before proceeding with layout, fabrication and measurement of the current circuit design. Also, the self calibration concept discussed in Chapter 2 should be investigated. And finally, further research can be done to extend the same concept to a multistage design in order to separate the competing requirements on dimensioning for bandwidth or noise performance.

Appendix A

Market overview

Series references

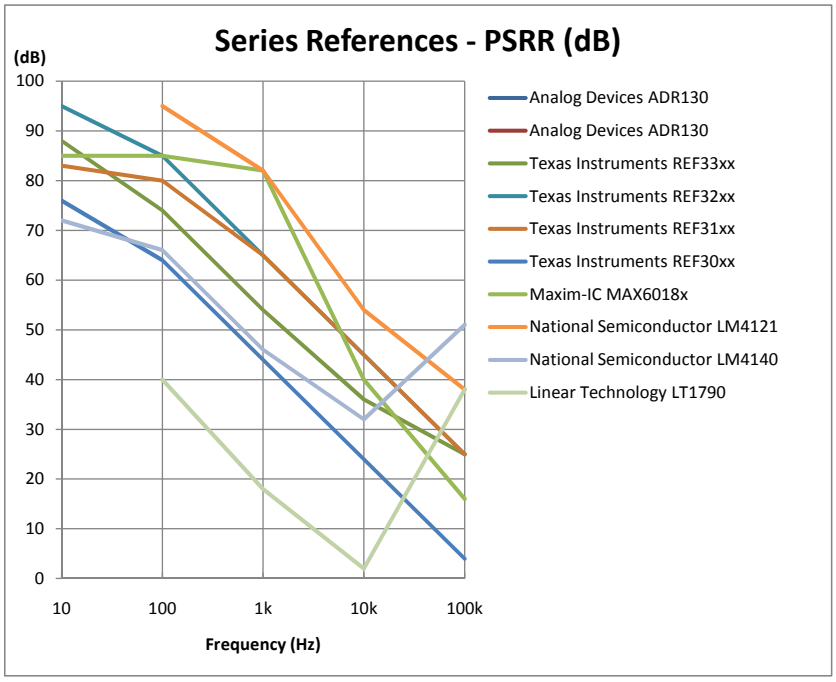


Figure A.1: Series references - Power Supply Ripple Rejection

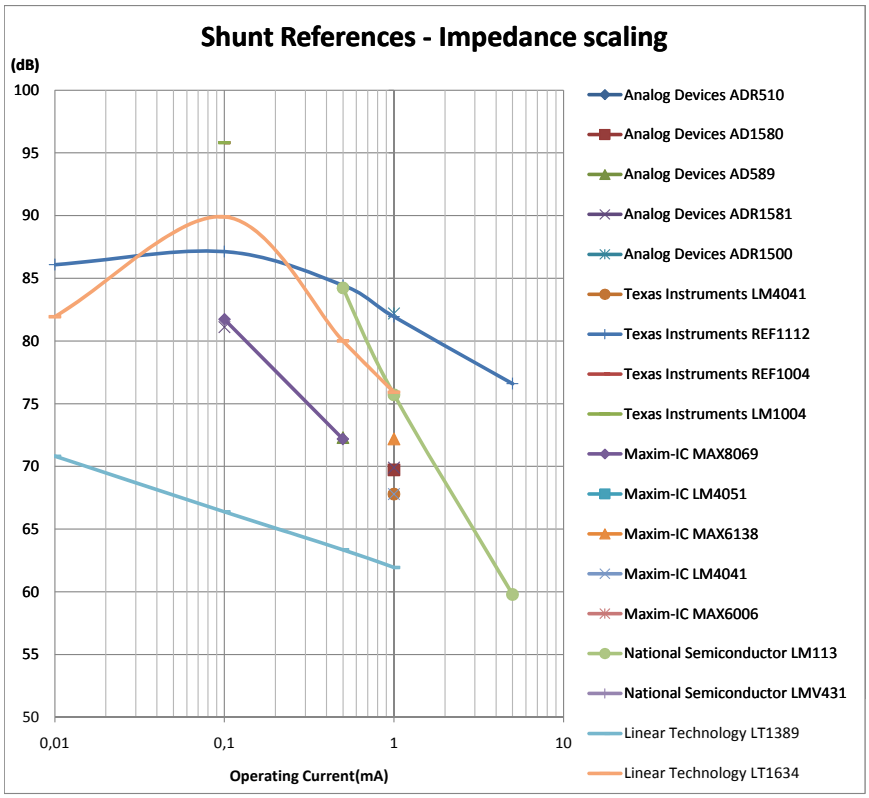


Figure A.2: Shunt references - Impedance scaling

Shunt references

Note 1

The impedance scaling factor is the ratio between the equivalent resistance and the dynamic output impedance at low input frequencies ($< 100Hz$). The equivalent resistance is the ohmic value that would be needed to achieve the same output voltage level with the operating current that attributes to the dynamic output impedance of the 'diode'). This can be calculated in [dB] by

$$ZS = 20 \cdot \log_{10} \frac{V_{out}/I_{op}}{Z_{out}} \tag{A.1}$$

With dynamic

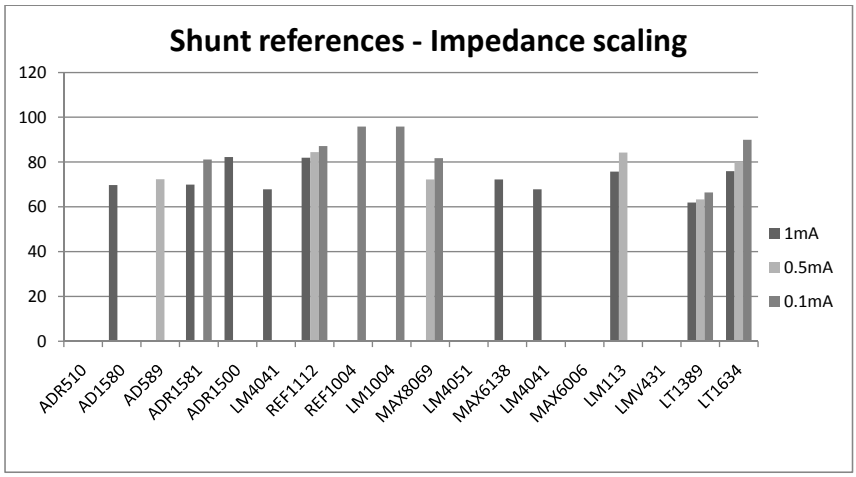


Figure A.3: Shunt references - Impedance scaling - Bar chart

Manufacturer	Part ID	Process	Datasheet	Vout	eN	VN	TCVo		Init error	Turn-on T	Vin,min	Vin,max	IQ	LNR	PSRR		Coutput	
				typ	typ(uVp-p)	typ(uVRMS)	typ(ppm/C)	max	max (V)	typ (us)	typ(V)	typ(V)	max(uA)	typ(ppm/V)	max	fc (Hz)	min(uF)	max(uF)
Analog Devices	ADR130-B grade	n/a	DS	0,5	3	(0.1uF Co) 172uVp-p	5	25	0,35%	80	2	18	175	10	40	n/a	0,1	10
Analog Devices	ADR130-B grade	n/a	DS	1	6	(0.1uF Co) 291uVp-p	5	25	0,35%	80	2	18	150	10	40	n/a	0,1	10
Texas Instruments	REF3312	n/a	DS	1,25	35		8	30	0,15%	20	1,8	5,5	8,5	30	50	10	0,1	10
Texas Instruments	REF3318	n/a	DS	1,8	50		8	30	0,15%	2000	2	5,5	8,5	30	50	10	0,1	10
Texas Instruments	REF3212	CMOS	DS	1,25	17	24	10,5	20	0,20%	2000	1,8	5,5	135	15	65	30	0	0
Texas Instruments	REF3112	CMOS	DS	1,25	14	24		10	20	0,20%	400	1,8	5,5	115	20	65	100	0	0
Texas Instruments	REF3012	CMOS	DS	1,25	14	42		35	75	0,20%	120	1,8	5,5	50	60	190	10	0	0
Texas Instruments	REF2912	CMOS	DS	1,25	14	42		35	75	2%	120	1,8	5,5	50	60	190	10	0	10
Maxim-IC	MAX6018A-EUR12	BiCMOS	DS	1,263	45	100		16	50	0,20%	200	1,8	5,5	5	50	400	1000	0,047	1
Maxim-IC	MAX6018A-EUR16	BiCMOS	DS	1,6	40	150		16	50	0,20%	200	1,8	5,5	6	40	250	1000	0,0001	1
Maxim-IC	MAX6018A-EUR18	BiCMOS	DS	1,8	45	160		16	50	0,20%	200		5,5	6	40	275	1000	0,0001	1
National Semiconductor	LM4121-1.2	n/a	DS	1,25	20	30	(-40/85C) 14		50	0,20%	8	1,8	14	275	7	120	10	0,022	1
National Semiconductor	LM4140xxx-1.0	n/a	DS	1,024	2,2	n/a	(0/70C) 3		n/a	0,10%	200	1,8	5,5	375	50	300	40	0,22	n/a
National Semiconductor	LM4140xxx-1.2	n/a	DS	1,25	2,2	n/a	(0/70C) 3		n/a	0,10%	200	1,8	5,5	375	50	300	40	0,22	n/a
Linear Technology	LT1790ACS6-1.25	Bipolar	DS	1,25	10	(10/1kHz) 14		5	10	0,05%	250	1,95	18	75	50	220	10	1	n/a

(a) Series references

Manufacturer	Part ID	Process	Datasheet	Vout	eN (uVp-p)	VN(uVRMS)	TCVo (ppm/C)		Init error (V)	Turn-on T	Iop		Cout	
				typ	typ	typ	typ	max	max(V)	typ (us)	min (uA)	max(mA)	min (nF)	
Analog Devices	ADR510A	n/a	DS	1	4	n/a	n/a	(-40/85C)85	0,35%	10	100	10	0	
Analog Devices	AD1580B	Bipolar	DS	1.225	5	20	n/a	(-40/85C)50	0,08%	5	50	10	0	
Analog Devices	AD589TH	Bipolar	DS	1.235	n/a	5	n/a	50	2,02%	25	50	5	0..1	
Analog Devices	ADR1581B	Bipolar	DS	1,25	4,5	20	n/a	(-40/85C)50	0,12%	5	60	10	0	
Analog Devices	ADR1500	Bipolar	DS	1,2875	5	20	170	(-40/85C)220	0,20%	5	50	10	0	
Texas Instruments	LM4041C12Q	n/a	DS	1.225	n/a	20	n/a	150	1,50%	5	80	12	0	
Texas Instruments	REF1112	n/a	DS	1,25	25	n/a	15	50	0,20%	~1000	1,2	5	10..100	
Texas Instruments	REF1004-1.2	n/a	DS	1.235	n/a	60	20	n/a	0,32%	~10000	10	20	0	
Texas Instruments	LM1004-12	Bipolar	DS	1.235	n/a	60	20	n/a	0,81%		10	n/a	0	
Maxim-IC	MAX8069ESA+	n/a	DS	1,22	n/a	20	n/a	25	0,41%		60	5	4700	
Maxim-IC	LM4051A	BiCMOS	DS	1.225	n/a	20	n/a	n/a	0,10%		60	12	0	
Maxim-IC	MAX6138_12	BiCMOS	DS	1,2205	n/a	20	4	(-40/85C)25	0,10%		60	12	0	
Maxim-IC	MAX6006A	BiCMOS	DS	1,25	30	n/a	n/a	30	0,20%	~10000	1	2	10	
National Semiconductor	LM113-1	Bipolar	DS	1.22	n/a	5	n/a	n/a	0,98%	5	500	20	0.2..100	
National Semiconductor	LMV431BI	Bipolar	DS	1.24	~10	n/a	39	130	1,53%	~2	100	15	0,1][10	
Linear Technology	LT1389ACS8	n/a	DS	1,25	25	n/a	4	(0/70C)10	0,12%	1000;200000	0,8	2	100	
Linear Technology	LT1634AIS8-1.25	n/a	DS	1,25	10	n/a	n/a	(-40/85C?)25	0,18%	400;20000	10	20	100	

(b) Shunt references

Table A.1: Specification overview

Appendix B

Circuit Dimensions

Component dimensions

Compontent	W (um)	L (um	Impedance	Folding
M1, M5	30	30		10
M2, M6	30	2		2
M3, M7	100	2		6
M4	70	18		4
M8	700	18		40
M9	20	2		10
M10	2	0.18		2
M11	700	0.18		10
M12	2	2		1
M13	100	2		6
M14	17.5	18		1
Rt	1	78.5	85kOhm	
Rs	1	60	65kOhm	
Rb	1	74	80kOhm	
C1	10	36	3pF	10

Figure B.1: Component dimensions

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