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Bandwidth extension and noise cancelling for TIAs

Two new common source TIA implementations

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Abstract

This thesis discusses two implementations for high-bandwidth low-noise transimpedance amplifiers. These techniques are designed for a common source TIA without using inductors in standard CMOS.

The two techniques proposed in this thesis are: noise cancelling and bandwidth extension. The noise cancelling technique uses the fact that at some point inside the feedback resistance a virtual ground for the input current is located, while at this node a part of the noise of the TIA is present. This node is used to cancel the noise of the TIA.

The second technique, the bandwidth extension, uses a controlled current source to increase the TIA bandwidth. This controlled current source both increases the loop gain without decreasing the transimpedance gain and decreasing the noise up to the TIA bandwidth.

Contents

Chapter 1

Introduction

Since the computer took its place in the modern society the need of faster computers and connectivity is only growing. The connection between computers became more and more important and the need for high speed links is growing to be able to meet the user demands. The large distance links nowadays are in the range of $1Tb/_S$, where high cost electronic and optical equipment is required. When these techniques would be applied to short distance links, for example fibre-in-home, the costs would not compete to the speed of this link. To make high speed links for the short range available the cost of the optical receiver systems must be less to make it attractive.

An optical receiver system consists of a photodiode, to convert signals in the optical domain into signal in the electrical domain, and an electrical circuit to reconstruct the transmitted data.
The chip and photodiode process are costly processes and therefore these optical receiver systems are still expensive nowadays; these processes are for example InGaAs (Indium Gallium Arsenide) or Germanium. To make these systems cheaper one could think of using a more standard process like CMOS; sub-micron CMOS is fast enough to compete with the expensive processes. Design for example the electrical front-end in a standard CMOS process and the diode in InGaAs. This means that the photodiode is off chip, this means an expensive photodiode process and assembly costs. But this is already cheaper then the original optical receiver system.

The solution proposed by S. Radovanovic [8] is to create an on chip photodiode, to get a more low cost solution. The development of such a photodiode on chip requires a new electrical circuit. This thesis describes such a electrical circuit for an on chip photodiode for high speed optical links.

1.1 System overview

This optical receiver system exists of two domains; an optical domain and an electrical front-end, where the design of the optical domain is out of the scope of this thesis. The characteristics of the optical sensor and optical standards are used to design the electrical front-end. The electrical front-end itself also exist of two domains; an analog front-end and digital processing. The domains and the sub-blocks of the system are shown in figure 1.1.

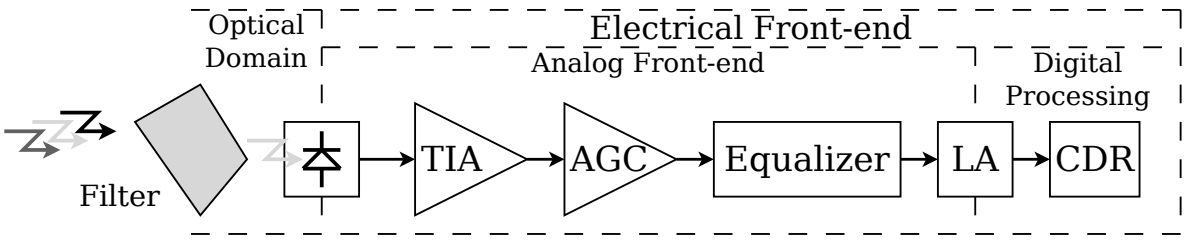


Figure 1.1: System overview of the optical receiver system

The incoming light contains information on several wavelengths, for example multiple data streams in different wavelengths. Since this is common in optical data transmission there is a filter on top of the photodiode, that enables the selection of one wavelength. The current from the photodiode is amplified and equalized to enable a large system bandwidth and thus large data rates. The limiting amplifier (LA) transforms the analog signal in a more digital like signal so it can be used in the clock and data recovering (CDR).

1.2 Research objectives

This thesis will mainly focus on the analog front-end of the optical receiver system as indicated in figure 1.1. The idea is to create a optical receiver system with a large bandwidth to achieve high data rates. The first research objective is to determine the maximum amount of input referred amplitude noise for the analog front-end, such that the bit error rate specified for the optical link is met. Since this bandwidth is several GHz, the integrated noise is the main concern. There is a trade-off between the bandwidth, optical power and the noise that can be tolerated to achieve the bit error rate specified.

The second and main research objective is the transimpedance amplifier (TIA), the TIA must meet the bandwidth and noise specified. The TIA will be designed without the use of inductors in standard 65nm CMOS. Two common TIA implementations are compared to noise behaviour and bandwidth. For the chosen TIA two enhancements are designed: noise cancelling and bandwidth extension. These features are used to meet the specifications of the optical link.

1.3 Outline of the report

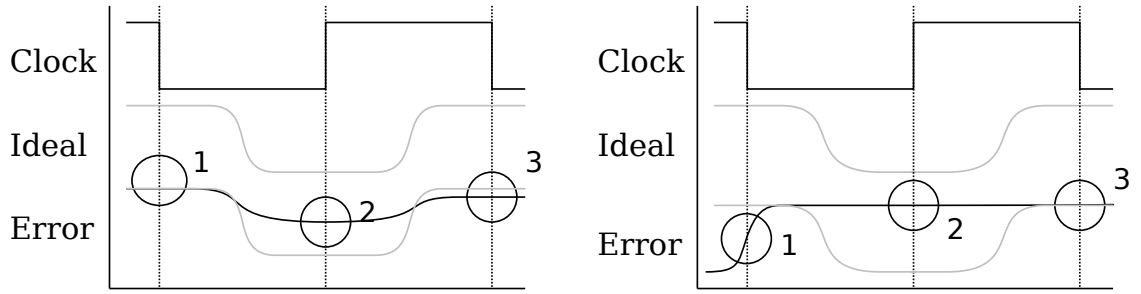
The TIA specifications are derived from the link specifications in chapter 2. Where two different TIA topologies are compared for noise in chapter 3. For the chosen TIA topology noise cancelling and bandwidth extension features are explained in chapter 4. The simulation results of the TIA enhancements are discussed in chapter 5.
The conclusion and recommendations are discussed in chapter 6.

Chapter 2

System noise analysis

This chapter presents a noise analysis to determine the system parameters that are used to design the analog front-end of the optical receiver system. The noise related specification for this system is the bit error rate (BER); according to the gigabit Ethernet standard the $BER = 10^{-12}$. To design the analog front-end the relation between the bit error rate and the amplitude noise is determined. With the amplitude noise the analog front-end can be designed to meet the BER.

The data information is coded in a low and high level voltages V_L and V_H respectively, if V_L is detected the information could be a 'zero' for example and a high level voltage could be a 'one'. A bit error is the detection of V_L instead of V_H for example.
In the clock and data recovery (CDR) the incoming data stream, information coded in V_L and V_H, is sampled by a clock generated by the CDR, this clock is usually recovered from the incoming data stream. The sampling moment of the clock differs in time with respect to the ideal moment in time. This is called timing jitter and can cause bit errors. The bit error rate is the description of the probability that a bit value is detected wrong.



(a) Noise behaviour in the analog front-end

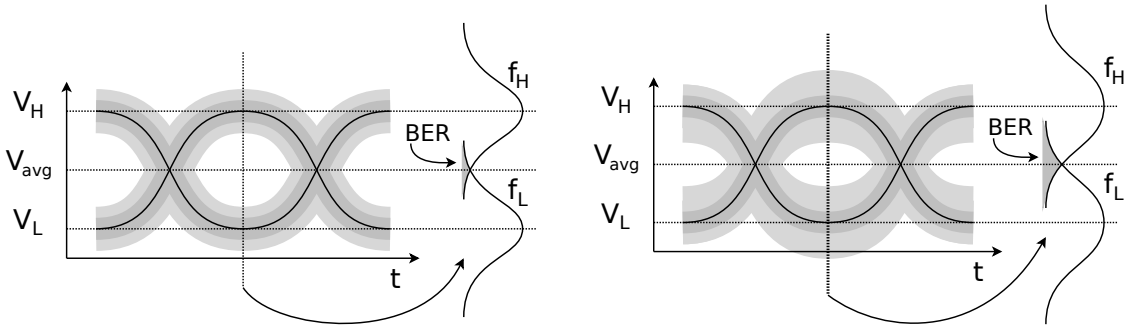
(b) Noise behaviour in the digital back-end

Figure 2.1: Overview of the bit error mechanisms

Amplitude noise in the analog front-end changes the voltage levels V_L and V_H, see figure 2.1(a). Situation 1 gives a voltage level that is not changed by the amplitude noise. In situation 2 the amplitude noise has raised the low voltage V_L, this could result in a wrong decision when situation 2 is amplified to a high voltage level V_H; a bit error occurs. The amplitude noise can also change the voltage level a bit, shown in situation 3.
The clock and data recovery experiences these signals with amplitude noise as signals with timing jitter. Two examples of bit errors that can occur in the digital back-end are shown in figure 2.1(b). Situation 3 is a situation where the data is sampled correct, and the information is valid. In situation 2 a bit error occurs, the information is coded V_L, but V_H is sampled. This error can occur because information got lost in the analog front-end or the clock-edge and data edge are shifted whole bit periods (period jitter). Situation 1 is a potential error, because the information is coded in V_H, but $\frac{V_H - V_L}{2}$ is sampled since this voltage level has no information value, the information is called meta-stable. This

situation is caused by clock and data edge variations in the order of half a bit period (edge-to-edge jitter), this can occur if the clock in no longer synchronized to the data stream.

A good insight in the bit error rate can be obtained with an eyediagram. An eyediagram is a graphical representation of the different bits in the data stream, the voltage level in time of all the bits are plotted in one bit period. In this way the amplitude difference caused by the amplitude noise is shown, large differences in the amplitude can cause bit errors, see situation 2 in figure 2.1(a). Two eyediagrams are shown in figure 2.2(a) and 2.2(b), figure 2.2(a) gives a situation where the amplitude noise causes less variation in the voltage level than the situation in figure 2.2(b). If there is more variation in the voltage level there is more chance a bit error occurs. And the chance that a bit error occurs is graphically seen as the eye opening.



(a) small BER (b) large BER

Figure 2.2: Eyediagram with gaussian amplitude noise on V_L and V_H

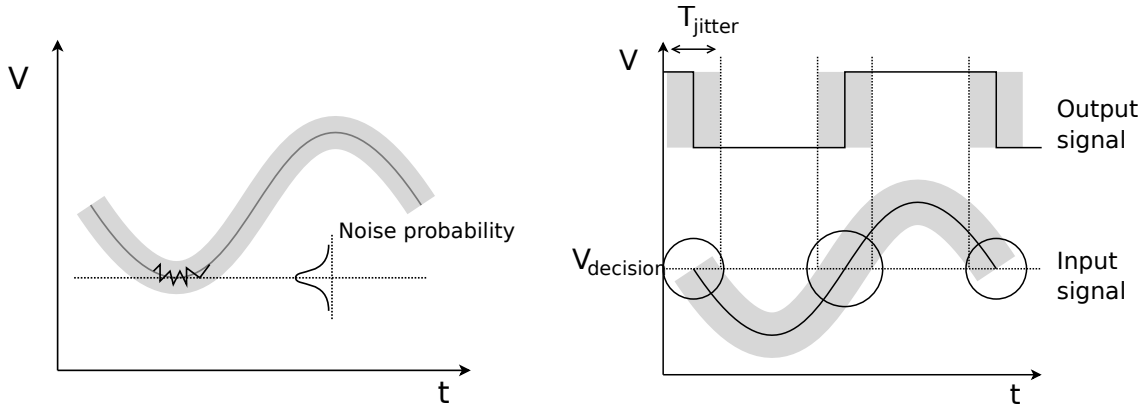
Noise calculation approach

The sample moment of the clock is not ideal, because of the clock timing jitter. This timing jitter gives an extra uncertainty in the sample time of the data. The mathematical derivation of the BER is done in the analog domain, to be able to model the timing jitter of the sample clock, this clock jitter is transformed into amplitude noise. Where it can be added to the amplitude noise of the analog front-end and thus be modelled in the BER equations.

The translation between jitter and noise is discussed first in section 2.1 to get the clock jitter transformed to the analog domain. The mathematical derivation of the BER is described in section 2.2.
Section 2.3 describe the noise introduced by the analog front-end. The noise and signal generated by the photodiode is discussed in section 2.4.
The derivation for the BER of the system is expressed in input referred current noise in section 2.5.

2.1 Noise-jitter transformation

The analog front-end of the optical receiver system adds white amplitude noise to the wanted signal, see figure 2.3(a). This white amplitude noise is represented as a Gaussian density function around the wanted signal.
The transformation from amplitude noise to timing jitter occurs in the limiting amplifier. The limiting amplifier is a kind of comparator that amplifies the signal to the voltage supply rails. The incoming signal is compared to a threshold voltage, thereby transforming the amplitude noise on the signal into timing jitter; a graphical representation is shown in figure 2.3(b).



(a) White noise represented as a Gaussian distribution on a signal

(b) White noise transformed into jitter

Figure 2.3: Noise and jitter representations

2.1.1 Mathematical description of the amplitude noise to timing jitter transformation

According to [10] amplitude noise to time jitter transformation takes place at the threshold of the comparator. The amplitude noise is transformed into timing jitter by the slope of the signal crossing the threshold. The slope is described as $\frac{\delta v}{\delta t}$, which transforms the amplitude noise (δv) to timing jitter (δt).
A signal with amplitude noise crossing the threshold of an comparator is graphically represented in figure 2.4.
The amplitude noise is presented as it's Gaussian density function on the vertical axis and the timing jitter density function is presented on the time axis.
[10] claims that the probability density function of timing jitter is the same as the probability density function of the amplitude noise. Multiplying a Gaussian function with a scalar resembles in a Gaussian function. The slope is a scalar and therefore the timing jitter is a Gaussian density function.

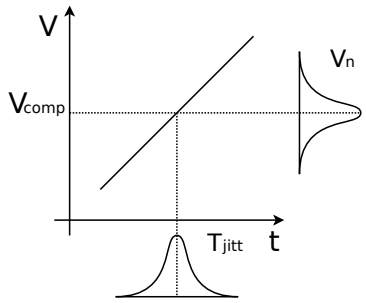


Figure 2.4: Transformation of voltage noise to timing jitter at a threshold [10]

[10] gives a relation between the Gaussian density function of the amplitude noise σ_{v_n} and the Gaussian density function of the timing jitter σ_{jitter}, see equation (2.1).

$$\sigma_{v_n}^2 = \sigma_{jitter}^2 \cdot \left| \frac{\delta v}{\delta t} \right|^2_{v=V_{comp}} \tag{2.1}$$

2.1.2 Mathematical description of the clock jitter and noise

The clock timing jitter can be cleaned with a circuit to reduce the jitter on the clock edges [9](p.576). This is represented as $\sigma_{clk} = \alpha \cdot \sigma_{jitter}$, where σ_{clk} is the standard deviation of the timing jitter on the clock edge and α the cleaning factor ($0 < \alpha < 1$). The influence of the clock jitter is added to the amplitude noise to obtain it's influence on the BER. The equivalent amplitude noise created by the clock timing jitter is $\sigma_{v_{n,clk}}$. A good estimation for $\alpha \approx 5\%$ [11].

$$\sigma_{jitter} = \sigma_{v_n} \cdot \left| \frac{\delta v}{\delta t} \right|^{-1}_{v=V_{comp}}$$

$$\sigma_{clk} = \alpha \cdot \sigma_{v_n} \cdot \left| \frac{\delta v}{\delta t} \right|^{-1}_{v=V_{comp}}$$

Now that the clock timing jitter caused by the amplitude noise is derived and the clock cleaning factor is added, the clock timing jitter is transformed to amplitude noise. The amplitude noise cause by the clock timing jitter is $\sigma_{v_{n,clk}}$.

$$\sigma_{v_{n,clk}} = \sigma_{clk} \cdot \left| \frac{\delta v}{\delta t} \right|_{v=V_{comp}} = \alpha \cdot \sigma_{v_n} \tag{2.2}$$

$\sigma_{v_{n,clk}}$ is assumed to be uncorrelated with the amplitude noise, because clock-edge and the data-edge are different in time. Recovering the clock signal adds delay to the clock line and therefore the timing jitter on the clock-edge and data-edge are uncorrelated. Data dependant jitter is usually low frequency jitter, and gives the time difference between large a number of bits. This low frequency jitter is filtered by the loop filter of the PLL and does not effect the data recovery.

The standard deviation of the Gaussian density function of the total amplitude noise $\sigma_{v_{n,tot}}$ is the product of the clock noise $\sigma_{v_{v,clk}}$ and the amplitude noise σ_{v_n}.
Note that the rms voltage noise is defined as $\sigma_{v_n} = \overline{v_n}$.

$$\sigma_{v_{n,tot}} = \sqrt{\sigma^2_{v_n} + \sigma^2_{v_{n,clk}}} = \sqrt{\sigma^2_{v_n} + \alpha^2 \cdot \sigma^2_{v_n}} = \sigma_{v_n} \cdot \sqrt{1+\alpha^2} = \overline{v_n} \cdot \sqrt{1+\alpha^2} \tag{2.3}$$

2.2 Mathematical description of the bit error rate

A bit error occurs if the high voltage level V_H, is decreased by the amplitude noise to a value below V_{avg} a bit error occurs. Note that the amplitude noise on the lower and higher voltage levels are uncorrelated and assumed to be of equal amplitude.[1] The amplitude noise caused by the clock jitter is also uncorrelated with the amplitude noise on the signal.
The stochastic process of the amplitude noise on the voltage levels V_L and V_H is called respectively X_L and X_H. An error occurs if $F_L(V_{avg}) = P(X_L \geq V_{avg})$ and $F_H(V_{avg}) = P(X_H \leq V_{avg})$, where the probability functions F_L and F_H are the amplitude noise probability distribution functions of respectively the low voltage and the high voltage levels. The bit error rate is defined as $BER = P_0 \cdot F_L(V_{avg}) + P_1 \cdot F_H(V_{avg})$, P_0 and P_1 are respectively the chance that a zero and an one occurs ($P_0 + P_1 = 1$).
To calculate the bit error rate the next definition is used:

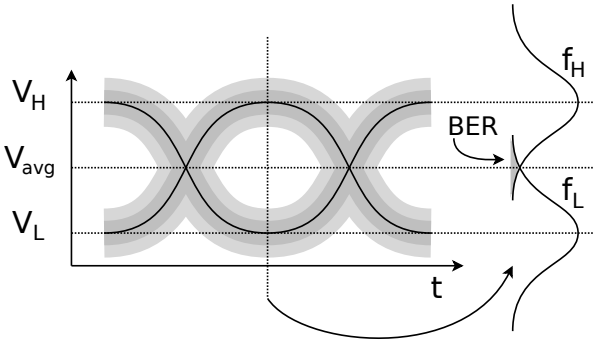


Figure 2.5: Overview of the bit error probability in the analog domain

$$F(z) = P(Z \geq z) = \int_z^{\infty} f_Z(x)\ \mathrm{d}x \tag{2.4}$$

Where $f_Z(x)$ is the probability density function of a stochastic process, in the case of white amplitude noise $f_Z(x)$ is given by:

[1] The amplitude noise on voltage levels V_H and V_L are not equal; noise on V_L has a smaller amplitude than noise on V_H. The amplitude noise is assumed equal to get the worst case scenario, the amplitude noise on V_H is taken.

$$f_Z(x) = \frac{1}{\sigma_Z\sqrt{2\pi}} \cdot e^{-\frac{(x-\mu_Z)^2}{2\sigma_Z^2}} \tag{2.5}$$

The mean values of the two density functions are ideally located at voltage levels V_L and V_H, this means $\mu_H = V_H$ and $\mu_L = V_L$. The mean value μ_Z can be shifted if the condition z also shifts, so the stochastic process F(z) can be rewritten to $P(Y \geq z - \mu_Z)$ where Y is the same process as Z but with $\mu_Y = 0$.
Choosing the following mean values result in equations for the stochastic processes:

$$\begin{aligned}
\mu_H &= V_{avg} - V_H \\
\mu_L &= V_L - V_{avg} \\
F_H(V_{avg}) &= P(X_H \leq V_{avg}) = P(X_H \geq -V_{avg}) \\
&= P(X_H \geq -V_{avg} - \mu_H) = P(X_H \geq 0) \\
F_L(V_{avg}) &= P(X_L \geq V_{avg} - \mu_L) = P(X_L \geq 0)
\end{aligned}$$

Since the amplitude on V_L and V_H is assumed equal and these two density functions are equal $F_L = F_H = F$: the mean value can be chosen equal for both density functions.

$$BER = P_0 \cdot F_L(0) + P_1 \cdot F_H(0) = (P_0 + P_1) \cdot F(0) = F(0)$$

The probability distribution function (2.4) is evaluated with the $Q(x)$ or erfc function.

$$Q(x) \equiv \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-\frac{y^2}{2}} \, \mathrm{d}y = \frac{1}{2} erfc\left(\frac{x}{\sqrt{2}}\right) \tag{2.6}$$

The $BER = F(0) = P(X \geq 0)$ rewritten into the Q-function form with $y = \dfrac{x-\mu}{\sigma}$:

$$P(X \geq 0) = \int_0^\infty \frac{1}{\sigma\sqrt{2\pi}} \cdot e^{-\frac{(x-\mu)^2}{2\sigma^2}} \, \mathrm{d}x$$

$$P(X \geq 0) = \frac{1}{\sigma} \cdot \frac{1}{\sqrt{2\pi}} \cdot \int_{0-\frac{\mu}{\sigma}}^{\infty-\frac{\mu}{\sigma}} e^{-\frac{y^2}{2}} \, \mathrm{d}y \cdot \sigma \tag{2.7}$$

$$P(X \geq 0) = \frac{1}{\sqrt{2\pi}} \cdot \int_{-\frac{\mu}{\sigma}}^{\infty} e^{-\frac{y^2}{2}} \, \mathrm{d}y \tag{2.8}$$

$$P(X \geq 0) = \frac{1}{2} erfc\left(-\frac{\mu}{\sigma\sqrt{2}}\right) \tag{2.9}$$

Substituting the above end results gives a general expression for the BER:

$$BER = \frac{1}{2} erfc\left(-\frac{V_{avg} - V_H}{\overline{v_n} \cdot \sqrt{2}\sqrt{1+\alpha^2}}\right) \tag{2.10}$$

Note that $\overline{v_n}$ is the maximum voltage noise that can be added to meet the BER that is specified.

2.3 Noise analysis of the analog front-end

According to the Friis formula for noise, the noise contribution of the following stages is negligible if the first stage has sufficient gain. The first stage in the optical receiver system is a transimpedance amplifier, typically this stage has enough gain to assume that the stages following the transimpedance amplifier do not contribute significantly to the noise.

The frequency characteristic of the diode has a low-pass behaviour, this means that the high frequency signal have a lower amplitude than the low frequency signals. The noise generated in the optical receiver is of equal amplitude for all frequencies, this means that the SNR is frequency dependant. For higher frequencies the SNR degrades because the input signal degrades. The frequency characteristic of the photodiode can be modelled with (2.11), where $0 < a < 1$. In this report the frequency characteristic is assumed low-pass with a cut-off frequency higher than the bandwidth of the optical receiver.

$$I_P(\omega) = \frac{I_{DC}}{\left(1 + j\frac{\omega}{\omega_0}\right)^a} \tag{2.11}$$

The gain of the transimpedance amplifier is the current to voltage gain:

$$R_{TIA} = \frac{V_{out_{pp}}}{I_{photo}} \tag{2.12}$$

2.4 Noise and signal analysis of the photodiode

This section discusses the current generated due to the incident light, the optical filtering and the noise of the photodiode.

2.4.1 Optical input power

The optical input power is defined in the gigabit Ethernet standard [1], by defining the optical modulation amplitude (OMA) and the extinction ratio (E_r) [7], see figure 2.6. The values from the standard are $OMA = -16dBm$ and $E_r = 6dB$. The wavelength used in this standard is 850nm.

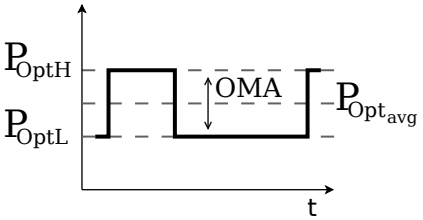


Figure 2.6: Overview of optical power definitions

$$OMA = P_{Opt_H} - P_{Opt_L} = 2\,P_{Opt_{AVG}}\frac{E_r - 1}{E_r + 1} \tag{2.13}$$

$$E_r = \frac{P_{Opt_H}}{P_{Opt_L}} \tag{2.14}$$

The optical power is calculated with the OMA: $P_{Opt_H} = 33.54\mu W$ and $P_{Opt_L} = 8.43\mu W$. The current generated by the diode is calculated for $\lambda = 850$nm:

$$I_{P_H} = \eta_{ext}\, q\frac{P_{Opt_H}\,\lambda}{h\,c} = 8.72\mu A \tag{2.15}$$

$$I_{P_L} = \eta_{ext}\, q\frac{P_{Opt_L}\,\lambda}{h\,c} = 2.19\mu A \tag{2.16}$$

The diode external efficiency $\eta_{ext} = 0.4 - 0.7$ for typical CMOS photodiodes, according to [8] (p.22). The diode external efficiency is assumed $\eta_{ext} \approx 0.4$ in this report.

2.4.2 Optical filter

The optical filter on top of the photodiode filters information channels, different information streams are send with different wavelengths. Due to spread and non-ideal optical filters on top of the photodiode, each photodiode receives power from both input channels. This results in crosstalk with a desired part and a smaller undesired part of the other channel. Assuming there are two information channels λ_1 and λ_2, with optical powers P_{λ_1} and P_{λ_2} respectively incident to the optical detectors (photodiode and filter). This crosstalk can be modelled using the matrix M that describes the optical power incident to each photodiode, see (2.17).

$$\begin{bmatrix} M_{11} & M_{21} \\ M_{12} & M_{22} \end{bmatrix} \cdot \begin{bmatrix} P_{\lambda_1} \\ P_{\lambda_2} \end{bmatrix} = \begin{bmatrix} P_{D_1} \\ P_{D_2} \end{bmatrix} \tag{2.17}$$

P_{D_1} and P_{D_2} are the optical powers incident on the photodiode 1 and 2 respectively.

2.4.3 Noise analysis of the Photodiode

The integrated photodiode converts the optical power into an electrical current, the relation for this conversion is (neglecting optical quantum noise):

$$I_{ph_1} = \eta_{ext}\, q \frac{P_{D_1}\, \lambda}{h\, c} = \eta_{ext}\, q \frac{(M_{11}\, P_{\lambda_1} + M_{12}\, P_{\lambda_2})\, \lambda}{h\, c} \tag{2.18}$$

where η_{ext} is the external quantum efficiency. The conversion process introduces shot noise, neglecting the optical quantum noise, the relation is:

$$\overline{i_{n_{ph_1}}} = \sqrt{2\, q\, I_{ph_1} BW} \tag{2.19}$$

where I_{ph_1} is the total electrical current produced by the photodiode and BW is the bandwidth of the optical receiver system. As can be seen in (2.18), the detector current contains information of the undesired channel λ_2, this is the noise introduced by the optical filter. So the total noise in channel 1 is described as:

$$\overline{i_{n_{diode}}} = \sqrt{\overline{i^2_{n_{ph_1}}} + \left(\eta_{ext}\, q \frac{M_{12} P_{\lambda_2}\, \lambda}{h\, c}\right)^2} \tag{2.20}$$

So the total amplitude noise from the photodiode and the filter referred to the input of the transimpedance amplifier is:

$$\overline{i_{n_{diode}}} = \sqrt{2\eta_{ext}\, q^2\, BW \frac{(M_{11} P_{\lambda_1} + M_{12} P_{\lambda_2})\, \lambda}{h\, c} + \left(\eta_{ext}\, q \frac{M_{12} P_{\lambda_2}\, \lambda}{h\, c}\right)^2} \tag{2.21}$$

2.5 Bit error rate to input referred current noise

The bit error rate is translated to the analog front-end noise performance; therefore the maximum input referred amplitude noise can be calculated that meets the bit error rate specified.

The BER equation (2.10) is rewritten into optical related parameters. And finally the bit error rate is expressed in terms of signal to noise ratio and input referred current noise.

$$BER = \frac{1}{2} erfc\left(-\frac{V_{avg} - V_H}{\overline{v_n} \cdot \sqrt{2}\sqrt{1+\alpha^2}}\right)$$

$\overline{v_n}$ is total voltage noise generated by the optical receiver system.

$$\begin{aligned} V_{avg} - V_H &= R_{TIA}(I_{avg} - I_{P_H}) \\ \overline{v_n} &= R_{TIA} \cdot \overline{i_n} \\ BER &= \frac{1}{2} erfc\left(\frac{I_{P_H} - I_{avg}}{\overline{i_n} \cdot \sqrt{2}\sqrt{1+\alpha^2}}\right) \end{aligned} \tag{2.22}$$

$\overline{i_n}$ corresponds to the total input referred current noise that the optical receiver system can generate for a given bit error rate. Using the relations for the current generation:

$$\begin{aligned} I_{P_H} &= \eta_{ext}\, q \frac{P_{Opt_H}\, \lambda}{h\, c} \\ I_{avg} &= \eta_{ext}\, q \frac{P_{Opt_{AVG}}\, \lambda}{h\, c} \end{aligned}$$

With (2.13) and (2.14) the relation can be converted to the Ethernet standard related parameters.

$$\begin{aligned} P_{Opt_{AVG}} &= \frac{OMA}{2} \frac{E_r + 1}{E_r - 1} \\ P_{Opt_H} &= OMA \frac{E_r}{E_r - 1} \\ P_{Opt_H} - P_{Opt_{AVG}} &= \frac{OMA}{2} \end{aligned}$$

$$\begin{aligned} BER &= \frac{1}{2} erfc\left(\frac{\eta_{ext}\, q\, \lambda}{h\, c} \frac{(P_{Opt_H} - P_{Opt_{AVG}})}{\overline{i_n} \cdot \sqrt{2}\sqrt{1+\alpha^2}}\right) \\ &= \frac{1}{2} erfc\left(\frac{\eta_{ext}\, q\, \lambda\, OMA}{2h\, c} \frac{1}{\overline{i_n} \cdot \sqrt{2}\sqrt{1+\alpha^2}}\right) \end{aligned} \tag{2.23}$$

The the total input referred current noise of the optical receiver system:

$$\begin{aligned} erfc^{-1}(2 \cdot BER) &= \frac{\eta_{ext}\, q\, \lambda\, OMA}{2h\, c} \frac{1}{\overline{i_n} \cdot \sqrt{2}\sqrt{1+\alpha^2}} \\ \overline{i_n} &= \frac{1}{erfc^{-1}(2 \cdot BER)} \frac{\eta_{ext}\, q\, \lambda\, OMA}{2h\, c} \frac{1}{\sqrt{2}\sqrt{1+\alpha^2}} \end{aligned} \tag{2.24}$$

The signal to noise ration in relation with the BER is given by:

$$\begin{aligned} \sqrt{2}\sqrt{1+\alpha^2} \cdot erfc^{-1}(2 \cdot BER) &= \frac{\eta_{ext}\, q\, \lambda\, OMA}{2h\, c} \frac{1}{\overline{i_n}} \\ \sqrt{2}\sqrt{1+\alpha^2} \cdot erfc^{-1}(2 \cdot BER) &= \frac{S_{rms}}{N_{rms}} \end{aligned} \tag{2.25}$$

The SNR of the system is determined with $BER = 10^{-12}$ and $\alpha = 0.05$:

$$\frac{S_{rms}}{N_{rms}} = 7.04 \tag{2.26}$$

The total input referred noise of the optical receiver system is given by:

$$\overline{i_{n_{total}}} = \sqrt{\overline{i^2_{n_{diode}}} + \overline{i^2_{n_{TIA}}} + \overline{i^2_{n_{\mathcal{E}}}}}$$

$\overline{i_{n_{\mathcal{E}}}}$ is the input referred noise generated by the optical receiver system except for the TIA and the photodiode. The noise of the optical receiver system related to the BER is given by:

$$\frac{1}{erfc^{-1}(2 \cdot BER)} \frac{\eta_{ext}\, q\, \lambda\, OMA}{2h\, c} \frac{1}{\sqrt{2}\sqrt{1+\alpha^2}} = \sqrt{\overline{i^2_{n_{diode}}} + \overline{i^2_{n_{TIA}}} + \overline{i^2_{n_{\mathcal{E}}}}} \tag{2.27}$$

The input referred current noise of the TIA is given by:

$$\overline{i^2_{n_{TIA}}} = \left(\frac{1}{erfc^{-1}(2 \cdot BER)} \frac{\eta_{ext}\, q\, \lambda\, OMA}{2h\, c} \frac{1}{\sqrt{2}\sqrt{1+\alpha^2}} \right)^2 - \overline{i^2_{n_{diode}}} - \overline{i^2_{n_{\mathcal{E}}}} \tag{2.28}$$

The TIA can be designed using (2.28), this gives the input referred current noise specification.

Chapter 3

TIA topologies

In this section two different TIA topologies are discussed, the discussion will mainly focus on the noise performance of the topology. But first the specifications are listed.

Opamp structures can not be used due to the high bandwidth required in the TIA: the unity gain bandwidth of the opamp is in the same order as the bandwidth of the TIA. High frequency transistor circuits like the common gate TIA and the common source TIA are discussed in this section.

3.1 Specifications

The photodiode capacitance is an important parameter, estimated at 500fF for the envisioned on-chip photodiode.

The input referred noise is calculated from the BER (2.28):

$$\left(\frac{1}{erfc^{-1}(2\cdot BER)}\frac{\eta_{ext}\,q\,\lambda\,OMA}{2h\,c}\frac{1}{\sqrt{2}\sqrt{1+\alpha^2}}\right)^2 = 2.38\cdot 10^{-13} \tag{2.28}$$

$$\overline{i^2_{n_{diode}}} = 1.26\cdot 10^{-14} \tag{2.21}$$

This gives the input referred current noise for the TIA and following stage of the optical receiver:

$$\sqrt{\overline{i^2_{n_{TIA}}} + \overline{i^2_{n_{\mathcal{E}}}}} = 474nA \tag{3.1}$$

The amount of input referred noise for the TIA is chosen 70% of the total for the TIA and following stage of the optical receiver, resulting in $\overline{i_{n_{TIA}}}$=397nA.
The photocurrent is given by $\frac{I_{P_H} - I_{P_L}}{2} = 3.265\mu$A, see equations (2.15) (2.16).

BW	5GHz
C_{in}	500fF
$\overline{i_{n_{TIA}}}$	397nA
photocurrent	3.263 μA

Table 3.1: TIA specifications

3.2 Common gate TIA

The common gate TIA is known for its low input impedance. A common gate TIA with the noise sources is shown in figure 3.1.

The noise currents of transistors N1 and P3 and the signal current are amplified to a voltage with the output impedance of mainly transistor P3. This means that the noise current of transistors N1 and P3 contribute almost without attenuation to the input referred noise current. The next equation gives insight in the noise behaviour of the circuit, to leave some noise budget for the next stages a factor ξ is introduced and chosen roughly 70%. The reference input referred input current noise $\overline{i_{n_{TIA}}} = 397nA$, see table 3.1.

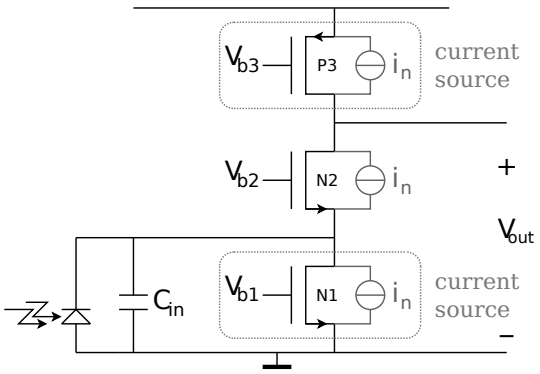


Figure 3.1: Common gate TIA with its noise sources

$$\begin{aligned}
\overline{i_{n_{TIA}}} &> \xi\sqrt{\overline{i_{n_1}^2} + \overline{i_{n_3}^2}} \\
&> \xi\sqrt{4 \cdot k \cdot T \cdot BW \cdot \gamma(g_{m1} + g_{m3})} \\
&> \xi\sqrt{4 \cdot k \cdot T \cdot BW \cdot \gamma}\sqrt{g_{m1} + g_{m3}} \\
\frac{\overline{i_{n_{TIA}}}}{\xi\sqrt{4 \cdot k \cdot T \cdot BW \cdot \gamma}} &> \sqrt{g_{m1} + g_{m3}} \\
2.85mS &> g_{m1} + g_{m3} \qquad (3.2)
\end{aligned}$$

To meet the bandwidth specification (BW=5GHz); $g_{m2} = \frac{1}{\omega_0 C_{in}} \approx \frac{1}{50}$S. The current needed for $g_{m2} \approx \frac{1}{50}$S results in a large $g_{m1} + g_{m3}$. A pre-design is made using ProMost to obtain the transistor specifications, which gives a good estimate of the feasibility of the common gate TIA. The design parameters for the transistors are shown in table 3.2.

Table 3.2: Pre-design of the common gate TIA

(a) Transistor N2

W	80μm
L	0.06μm
I_D	1.7mA
V_{DS}	250mV
V_{GT}	145mV
g_m	19.39mS

(b) Transistor N1

W	15μm
L	0.06μm
I_D	1.7mA
V_{DS}	400mV
V_{GT}	336mV
g_m	9.72mS

(c) Transistor P3

W	14μm
L	0.06μm
I_D	1.7mA
V_{DS}	550mV
V_{GT}	495mV
g_m	5.66mS

This pre-design gives the estimate that the noise specifications can not be met, the sum of the g_m values is 15mS. It can be concluded that the specifications, table 3.1, with the common gate TIA can not be met.

3.3 Common source TIA

The common source TIA has an advantage over the common gate TIA: only the noise of the feedback resistor contributes almost without attenuation to the input referred current noise. The input referred current noise caused by the noise of the transistors is attenuated by the transimpedance gain. A simple common source TIA is shown in figure 3.2.

The transimpedance gain is given by:

$$\frac{v_{out}}{i_{in}} = \frac{Z_L\left(R_f - \frac{1}{g_m}\right)}{\frac{1}{g_m} + Z_L}$$

Assuming that $Z_L >> \frac{1}{g_m}$ the equation can be simplified to:

$$\frac{v_{out}}{i_{in}} = R_f - \frac{1}{g_m} \tag{3.3}$$

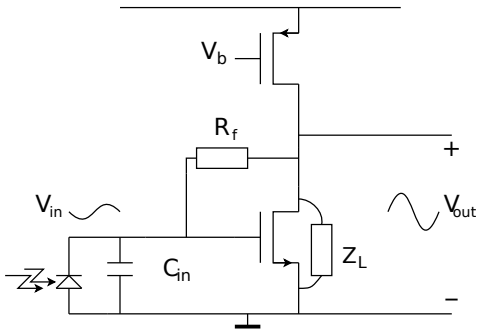


Figure 3.2: Common source TIA

The input impedance of this TIA (z_{in}) is given by the next equation and also assumes $Z_L >> R_f$:

$$z_{in} = \frac{Z_L + R_f}{g_m Z_L + 1} = \frac{1}{g_m} \tag{3.4}$$

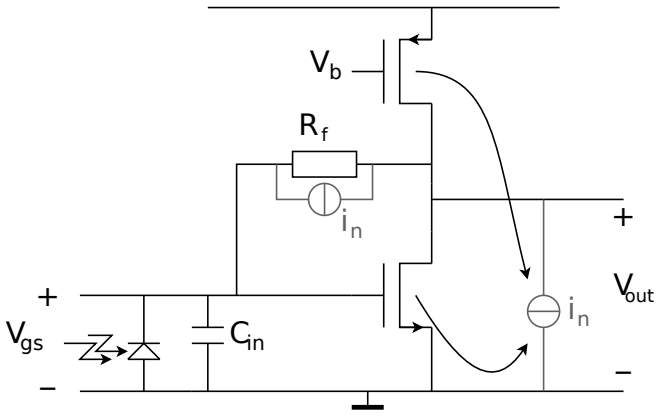


Figure 3.3: Noise sources of the common source TIA

The noise sources of the common source TIA are indicated in figure 3.3. Only the noise of the feedback resistance is directly added to the input referred noise, whereas the noise of the transistors, amplified by the output impedance, is attenuated by the transimpedance gain.

The input referred noise is caused by the transistors is given by $\overline{i_{n_{in}}} = \frac{\overline{i_{n_{MOST}}} \cdot Z_L}{R_f}$. The input referred noise caused by the feedback resistance is given by:

$$\overline{i_{n_{in}}} = \frac{4 \cdot k \cdot T \cdot BW}{R_f} \tag{3.5}$$

Choosing a large feedback resistance gives less input referred noise, but less bandwidth.

W	40μm
L	0.06μm
I_D	4.885mA
V_{DS}	700mV
V_{GT}	340mV
g_m	28.62mS

Table 3.3: Pre-design of the common source TIA transistor

A pre-design for the TIA is made, the bias transistor is replaced by a resistor. The width of the transistor is chosen in such a way that the gate capacitance is about 10% of C_{in}. The transistor parameters are listed in table 3.3.
For the resistance holds the following: $R_{out} = \dfrac{1.2 - V_{DS}}{I_D} = 102\Omega$.

The input referred noise of R_{out}, the transistor and R_f is solved for $\overline{i_{n_{TIA}}}$, see table 3.1:

$$\frac{\overline{i_{n_{MOST}}}^2 \cdot Z_L^2 + \overline{v_{n_{Rout}}}^2}{R_f^2} + \overline{i_{n_{Rf}}} = \overline{i_{n_{TIA}}} = 397nA \tag{3.6}$$

R_f is the unknown variable in this equation, solving for R_f gives the feedback resistance needed to obtain the specified noise current, $R_f = 667$.
The bandwidth of the TIA for the given R_f is calculated with (3.4) and the next equation:

$$f_{cut-off} = \frac{1}{2 \cdot \pi \cdot z_{in} \cdot C_{in}} \tag{3.7}$$

This pre-design gives a bandwidth of 1.34GHz, this is not sufficient.

3.4 Summary

Since the noise sources of the common gate TIA are input referred and the noise generated by the common gate TIA exceeds the specified noise excessively this TIA can not be used. The common source TIA could potentially meet the input current noise specified because the feedback resistance can be used to attenuate the input referred noise. However the bandwidth will suffer from choosing the feedback resistance large. According to the pre-design of the common source TIA, improvements on the design have to be made to meet the specifications.

Chapter 4

TIA realization

According to the pre-design of the common source TIA in the previous chapter, the bandwidth does not meet the specified bandwidth of 5GHz. This chapter discusses two techniques to improve the noise and bandwidth behaviour of the common source TIA.

In section 4.1 a noise cancelling mechanism is discussed, this decreases the noise and therefore the bandwidth can increase. A bandwidth extension technique is discussed in section 4.2, the idea is to increase the bandwidth without decreasing the signal to noise ratio.

4.1 Noise cancelling in a common source TIA

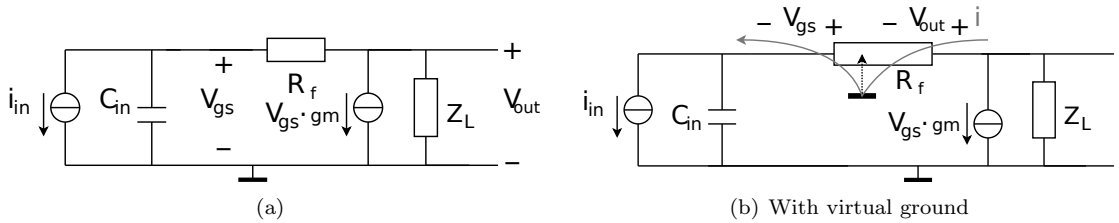
To cancel the noise of the common source TIA a node has to be found where only this noise is present. According to equations (3.3) and (3.4) for the transimpedance gain and input impedance; the feedback resistance can be divided into two functions.

$$\frac{v_{out}}{i_{in}} = R_f - \frac{1}{g_m} \tag{3.3}$$

$$z_{in} = \frac{Z_L + R_f}{g_m Z_L + 1} = \frac{1}{g_m} \tag{3.4}$$

The transimpedance gain $R_t = \frac{v_{out}}{i_{in}}$ and this can be written as:

$$\begin{aligned} R_t &= R_f - z_{in} \\ R_f &= z_{in} + R_t \end{aligned} \tag{4.1}$$



(a) (b) With virtual ground

Figure 4.1: Small signal model of figure 3.2

According to (4.1) the feedback resistance can virtually be split into two different resistances: the input impedance and the transimpedance gain. This means that there is a virtual ground node inside the feedback resistance that separates the input impedance and transimpedance gain. The frequency

transfer of the common source TIA without parasitic capacitances is derived with the small signal model shown in figure 4.1(a).

$$\frac{v_{out}}{i_{in}} = \frac{Z_L(g_m \cdot R_f - 1)}{g_m \cdot Z_L + 1 + j\omega C_{in}(R_f + Z_L)} \tag{4.2}$$

$$\begin{aligned} \omega_0 &= \frac{g_m \cdot Z_L + 1}{C_{in}(R_f + Z_L)} \\ &= \frac{Z_L + \frac{1}{g_m}}{\frac{C_{in}}{g_m}(R_f + Z_L)} \end{aligned} \tag{4.3}$$

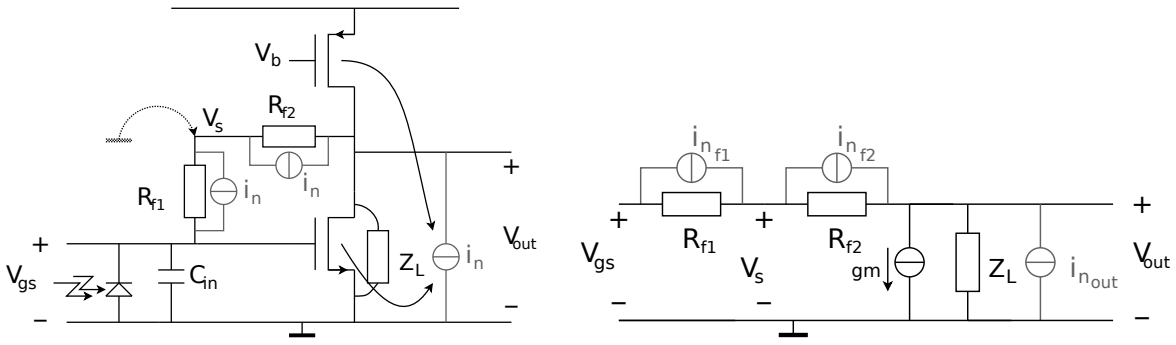
Using assumptions from section 3.3; ($Z_L >> \frac{1}{g_m}$ and $Z_L >> R_f$) together with equation (3.4); equation (4.3) changes to:

$$\begin{aligned} \omega_0 &\approx \frac{Z_L}{\frac{C_{in}}{g_m} Z_L} = \frac{g_m}{C_{in}} \\ &= \frac{1}{z_{in} \cdot C_{in}} \end{aligned} \tag{4.4}$$

The input impedance with the input capacitance creates a pole in the frequency transfer. Note that this can only be the case if the node inside R_f is virtual ground.
Secondly $\frac{v_{out}}{v_{gs}}$ are 180° out of phase:

$$\frac{v_{out}}{v_{gs}} = -\frac{Z_L(g_m \cdot R_f - 1)}{Z_L + R_f} \tag{4.5}$$

The phase difference is graphically shown in figure 4.1(b).
The feedback resistance divided into two resistors is shown in figure 4.2(a), where $z_{in} = R_{f1}$ and $R_t = R_{f2}$.



(a) Circuit with virtual ground

(b) Small signal model

Figure 4.2: Common source TIA with its noise sources

Calculating the noise transfer

The noise transfer of all the noise sources to v_s and v_{out} is calculated to obtain insight in the behaviour of the noise in the circuit. C_{in} is left out to obtain relations for the TIA itself.
The noise contribution of $\overline{i_{n_{f1}}}$ to v_s and v_{out}:

$$\begin{aligned} v_{out} &= v_s \\ v_{gs} &= v_{out} + \overline{i_{n_{f1}}} \cdot R_{f1} \\ v_{out} &= -g_m \cdot v_{gs} \cdot Z_L \\ v_{out} &= -g_m \cdot Z_L \cdot (v_{out} + \overline{i_{n_{f1}}} \cdot R_{f1}) \end{aligned} \tag{4.6}$$

This derivation result in:

$$\frac{v_{out}}{\overline{i_{n_{f1}}}} = \frac{-g_m \cdot Z_L \cdot R_{f1}}{1 + g_m \cdot Z_L} \tag{4.7}$$

$$\frac{v_s}{\overline{i_{n_{f1}}}} = \frac{-g_m \cdot Z_L \cdot R_{f1}}{1 + g_m \cdot Z_L} \tag{4.8}$$

For noise source $\overline{i_{n_{f2}}}$ the contribution is:

$$\begin{aligned} v_{gs} &= v_s \\ v_{gs} &= v_{out} + \overline{i_{n_{f2}}} \cdot R_{f2} \\ v_{out} &= -g_m \cdot v_{gs} \cdot Z_L \end{aligned} \tag{4.9}$$

This derivation result in:

$$\frac{v_{out}}{\overline{i_{n_{f2}}}} = \frac{-g_m \cdot Z_L \cdot R_{f2}}{1 + g_m \cdot Z_L} \tag{4.10}$$

$$\frac{v_s}{\overline{i_{n_{f2}}}} = \frac{R_{f2}}{1 + g_m \cdot Z_L} \tag{4.11}$$

The noise contribution of $\overline{i_{n_{out}}}$:

$$\begin{aligned} v_{out} &= v_s = v_{gs} \\ v_{out} &= (\overline{i_{n_{out}}} - g_m \cdot v_{gs}) Z_L \\ v_{out} &= (\overline{i_{n_{out}}} - g_m \cdot v_{out}) Z_L \end{aligned} \tag{4.12}$$

This derivation result in:

$$\frac{v_{out}}{\overline{i_{n_{out}}}} = \frac{1}{1 + g_m \cdot Z_L} \tag{4.13}$$

$$\frac{v_s}{\overline{i_{n_{out}}}} = \frac{1}{1 + g_m \cdot Z_L} \tag{4.14}$$

These noise transfers reveal a possibility to cancel noise of particular noise sources, using this virtual ground node. The noise contribution of $\overline{i_{n_{f1}}}$ and $\overline{i_{n_{out}}}$ can be cancelled by subtracting: $v_{out} - v_s$. The

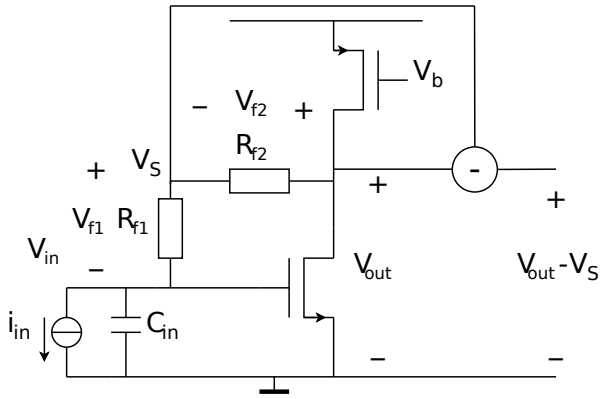


Figure 4.3: Noise cancelling TIA with schematic subtraction node

input signal at v_s is zero, because it is a virtual ground for i_{in}. The common source TIA with the sum point to cancel the noise is shown in figure 4.3.

For the noise source $\overline{i_{n_{f2}}}$ subtracting $v_{out} - v_s$ gives:

$$\frac{v_{out}}{\overline{i_{n_{f2}}}} - \frac{v_s}{\overline{i_{n_{f2}}}} = \frac{-g_m \cdot Z_L \cdot R_{f2}}{1 + g_m \cdot Z_L} - \frac{R_{f2}}{1 + g_m \cdot Z_L} = -R_{f2} \tag{4.15}$$

The input referred noise for the TIA, assuming the parasitic capacitances are zero, is given by:

$$\begin{aligned} \frac{v_{out} - v_s}{R_{f2}} &= \frac{-R_{f2} \cdot \overline{i^2_{n_{f2}}}}{R_{f2}} \\ &= \overline{i^2_{n_{f2}}} = \sqrt{\frac{4 \cdot k \cdot T \cdot BW}{R_{f2}}} \end{aligned} \tag{4.16}$$

According to this derivation only the current noise of the feedback resistance is input referred, the noise contribution of other noise sources can be cancelled using node v_s. The input referred noise can be decreased by increasing the R_{f2}.

4.1.1 The parasitic effects on the single stage TIA

The transimpedance amplifier with a number of its parasitics impedances is discussed in this section, see figure 4.4.

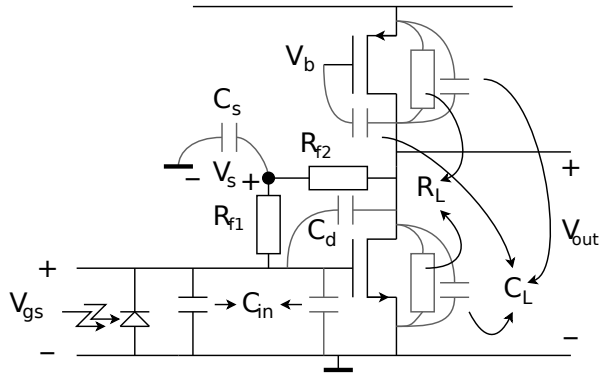


Figure 4.4: Single stage TIA with its parasitics

The voltage variations v_s caused by i_{in} must be zero, in this way the node v_s may be used to cancel noise on the output of the TIA. To achieve this virtual ground the relation for the feedback resistors is given by:

$$\begin{aligned} A = \frac{v_{out}}{v_{gs}} &= \frac{(g_m \cdot (R_{f1} + R_{f2}) - 1)\, Z_L}{R_{f1} + R_{f2} + Z_L} \\ R_{f1} &= \frac{R_{f1} + R_{f2}}{A + 1} \end{aligned} \tag{4.17}$$

Which results in:

$$\begin{aligned} R_{f1} &= \frac{R_{f2} + Z_L}{Z_L\, g_m} \\ Z_{in} = R_{f1} &= \frac{1}{\omega_0 \cdot C_{in}} \\ \frac{1}{\omega_0 \cdot C_{in}} &= \frac{R_{f2} + Z_L}{Z_L \cdot g_m} \end{aligned} \tag{4.18}$$

This equations gives the bandwidth trade-off for the TIA where R_{f1} is the input impedance for low frequencies and R_{f2} is the transimpedance gain. Z_L is the load impedance, given by $R_L//Z_{C_L}$; $Z_{C_L} = \frac{1}{j\,\omega\,C_L}$.

By rewriting and substituting R_{f2} into (4.18) a noise-bandwidth trade-off is obtained.

$$R_{f2} = \frac{4 \cdot k \cdot T}{\overline{i_n^2}} f_{cutt-off} = \zeta \cdot f_{cutt-off}$$

This results in:

$$\frac{1}{2 \cdot \pi \cdot f_{cutt-off} \cdot C_{in}} = \frac{\zeta \cdot f_{cutt-off} + Z_L}{Z_L \cdot g_m} \tag{4.19}$$

Where $\zeta = \frac{4 \cdot k \cdot T}{\overline{i_n^2}}$ and $\overline{i_n^2}$ is the noise contribution allowed by the TIA: $\overline{i_{n_{TIA}}}$, see table 3.1.
Equation (4.19) describes the effect of increasing the bandwidth of the receiver system; if $f_{cutt-off}$ increases, the left-hand side of (4.19) decreases while the right-hand side increases.

The assumption $Z_L >> R_{f2}$ made earlier, section 3.3, results in $Z_L >> \zeta \cdot f_{cutt-off}$ which simplifies the bandwidth-noise trade-off. However this assumption is not valid at 5GHz: the load capacitance at 5GHz can be in the same order as R_{f2}.

In order to meet the noise and bandwidth specification the following parameters can be increased: R_{f2} and $g_m \cdot Z_L$. Increasing R_{f2} decreases the noise and increases the transimpedance gain. Increasing $g_m \cdot Z_L$ keeps the right-hand side of (4.19) low enough to meet the bandwidth. In creasing the g_m and the output resistance of the transistor can be done with a large W and L, this however will end up with a too low unity gain frequency (FUG); the NMOS transistor has no gain left at high frequencies.

4.1.2 Single stage cascode TIA

The output impedance of the TIA has to be increased without decreasing the FUG.
Z_L can be increased by the using a cascode, the parasitic output impedance of the TIA is multiplied by $g_m \cdot Z_{out}$ of the cascode transistor. The cascoded circuit is shown in figure 4.5.

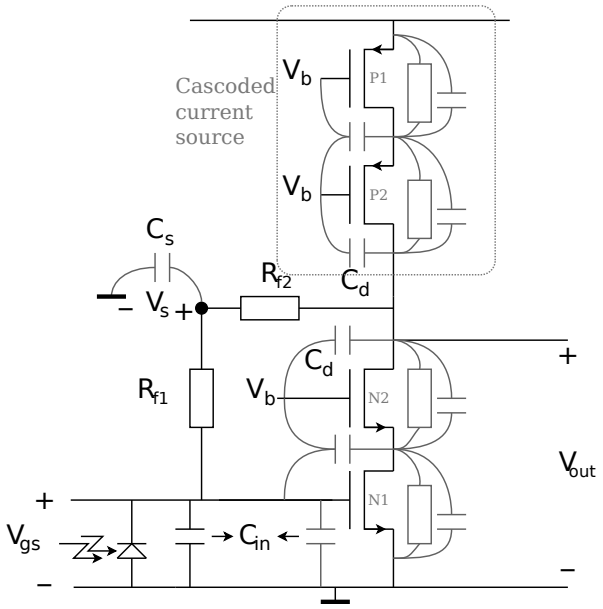


Figure 4.5: Single stage cascoded TIA with its parasitics

The output impedance of the cascoded stage is now increased to:

$$\begin{aligned} Z_L &= Z_{out_N} \,//\, Z_{out_P} \\ &= (Z_{out_{N1}} + Z_{out_{N2}} + Z_{out_{N1}} \cdot Z_{out_{N2}} \cdot g_{m_{N2}}) \,//\, (Z_{out_{P1}} + Z_{out_{P2}} + Z_{out_{P1}} \cdot Z_{out_{P2}} \cdot g_{m_{P2}}) \end{aligned} \quad (4.20)$$

The capacitance seen at the output of the TIA is dominated by the C_d capacitances of transistors M_2 and P_2.

Noise transfer

Eliminating the low load impedance reveals unwanted behaviour in the noise transfer from v_{out} to v_s, ideally $\frac{v_s}{v_{n_{out}}} = 1$. The simplified noise transfer $\frac{v_s}{v_{n_{out}}}$ is given by:

$$H_{n\,out \to s} = \frac{v_s}{v_{n_{out}}} = \frac{j\omega C_{in} R_{f1} + 1}{j\omega C_{in}(R_{f1} + R_{f2}) + 1} \quad (4.21)$$

The bandwidth of $\frac{v_s}{v_{n_{out}}}$ is lower than the system bandwidth, because R_{f2} is typically about 5-10 times larger than R_{f1}. This means that the noise at higher frequencies is not cancelled with $v_{out} - v_s$. The phase difference between v_{out} and v_s in the high frequency range causes the noise to add up, resulting in more noise than without the noise cancelling.

An option could be to equalize the noise at v_s to match the noise at v_{out}, but equalizing the noise at v_s will also cancel some of the input signal; for high frequencies the input signal is not zero at v_s.

4.1.3 Asymmetric feedback resistance

The bandwidth of the noise (4.21) and the system bandwidth can be brought together by choosing R_{f2} smaller. If R_{f2} is chosen small compared to R_{f1} the noise bandwidth and the system bandwidth would approximately be the same. But choosing R_{f2} small results in less gain and this results in more input referred noise. There is no use of changing the resistors; only the bandwidth or the noise will meet its specification.

What if R_{f2} would have a asymmetric value, from one side a high value and from the other side a low value. An asymmetric resistance is shown in figure 4.6, relations (4.22) and (4.23) give the resistance seen at each node.

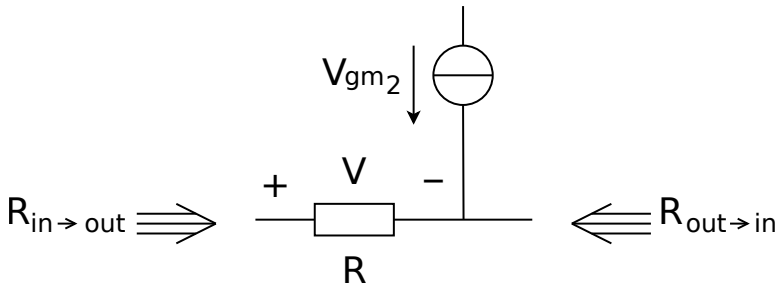


Figure 4.6: Asymmetric resistance model

$$R_{in\rightarrow out} = R \tag{4.22}$$

$$R_{out\rightarrow in} = \frac{R}{g_{m2} \cdot R + 1} \tag{4.23}$$

The resulting circuit with the asymmetric resistance is shown in figure 4.7.

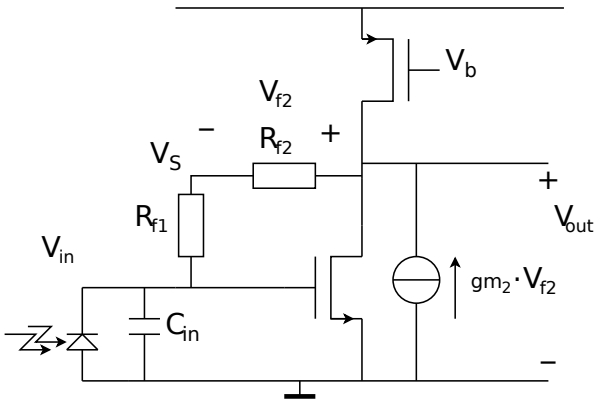


Figure 4.7: Asymmetric resistance in the common source TIA

This asymmetric resistance in the circuit decreases resistance R_{f2} and R_{f1} seen from the output to the input, this is calculated with the circuit in figure 4.8.

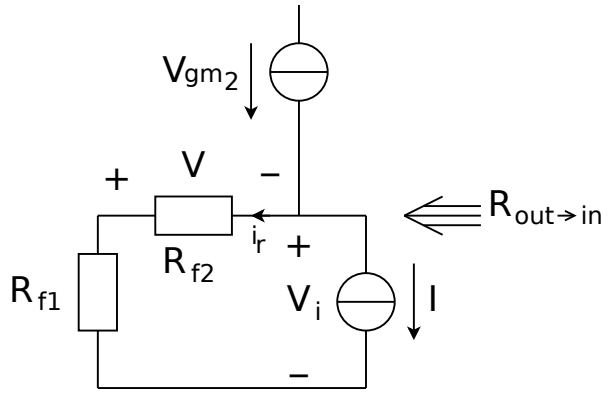


Figure 4.8: Effect of the asymmetric resistance on two resistors

$$
\begin{aligned}
R_{out\to in} &= -\frac{V_i}{I} \\
-I &= i_r \cdot R_{f2} \cdot g_{m2} + i_r \\
V_i &= i_r(R_{f1} + R_{f2}) \\
R_{out\to in} &= -\frac{V_i}{I} = \frac{R_{f1} + R_{f2}}{R_{f2} \cdot g_{m2} + 1} = \frac{R_{f1}}{R_{f2} \cdot g_{m2} + 1} + \frac{R_{f2}}{R_{f2} \cdot g_{m2} + 1}
\end{aligned} \tag{4.24}
$$

If only R_{f2} would be asymmetric $R_{out\to in} = R_{f1} + \frac{R_{f2}}{R_{f2} \cdot g_{m2} + 1}$ would be expected, but according to equation (4.24) R_{f1} decreases with the same factor as R_{f2}.
This means that the bandwidth of $H_{n_{out\to s}}$ is increased, but the TIA bandwidth is also increased; this is approximately given by: $\omega_0 = \frac{1}{C_{in} \cdot R_{f1}}$. Since R_{f1} is decreased with the same factor as R_{f2} the TIA bandwidth is increased with the same factor as $H_{n_{out\to s}}$. This still results in typically a 5-10 times larger TIA bandwidth compared to the bandwidth of $H_{n_{out\to s}}$. This noise cancelling is limited to the bandwidth of the noise transfer $H_{n_{out\to s}}$. Since the bandwidth of $H_{n_{out\to s}}$ does not meet the specified bandwidth of 5GHz, this noise cancelling mechanism can not be used.

4.2 Bandwidth extension in a common source TIA

Since the noise cancelling mechanism lags in bandwidth the asymmetric resistance is used to increase the bandwidth.
The effect of the asymmetric resistance, proposed in section 4.1.3, decreases the feedback resistance (4.24) seen from the output to the input. This effect is further investigated in the original TIA circuit, see figure 4.9.
To obtain insight in the influence of the voltage controlled current source the parasitic capacitances are assumed to be zero at this moment. This gives an estimate for the bandwidth, transimpedance gain and the loop gain.

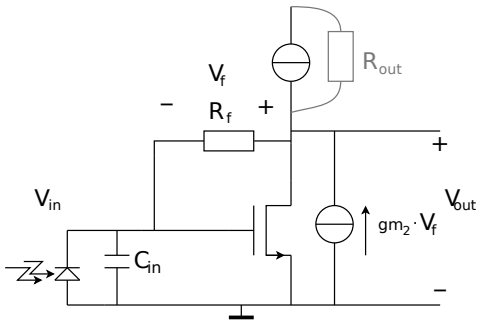


Figure 4.9: Common source TIA with steered current source

The estimated bandwidth is given by $\omega_0 = \frac{1}{z_{in} \cdot C_{in}}$ where z_{in} is given by (4.25). Where g_m is the VI gain of the of the TIA transistor.

$$z_{in} = \left. \frac{g_{m2} \cdot R_{out} \cdot R_f - R_{out} - R_f}{g_m \cdot R_{out} + 1} \right|_{C_{parasitic}=0} \tag{4.25}$$

The voltage controlled current source g_{m2} could be used to increase the bandwidth. The numerator of z_{in} can be set to zero by choosing g_{m2} according to:

$$g_{m2} = \frac{R_{out} + R_f}{R_{out} \cdot R_f} \tag{4.26}$$

The transimpedance gain with this g_{m2} is R_f, this can also be concluded from equation (4.1) a piece of R_f is the input impedance and the other part is the transimpedance gain. Since the input impedance is zero the transimpedance gain must be equal to R_f.

The loop gain of the TIA is given by the next equation:

$$A = \left. \frac{(-1 + g_m \cdot R_f + g_{m2} \cdot R_f) R_{out}}{-R_{out} - R_f + g_{m2} \cdot R_{out} \cdot R_f} \right|_{C_{parasitic}=0} \tag{4.27}$$

With this g_{m2} the loop gain A goes to infinity. The noise generated at the output node is cancelled because of the loop gain. Since the noise of the feedback resistance is directly input referred the noise of the feedback resistance is not cancelled by the infinite loop gain, choosing the feedback resistance large gives less input referred noise.

4.2.1 Parasitic effects on the bandwidth extension

The parasitic capacitances in the circuit are shown in figure 4.10, the light grey capacitances are the parasitics.

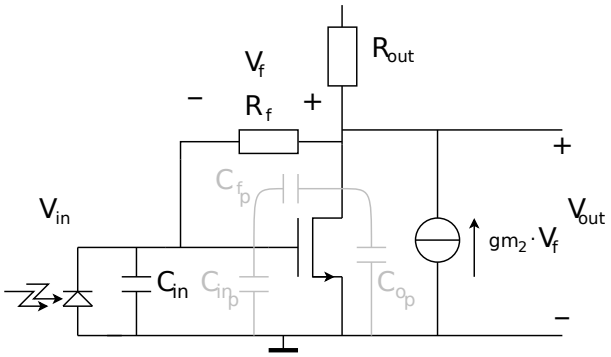


Figure 4.10: Parasitic capacitances of the common source TIA with bandwidth extension

The frequency behaviour of the TIA is estimated with a second order filter characteristic, with a zero and two poles.
The bandwidth is described as:

$$\omega_0 = \sqrt{\frac{gm \cdot R_{out} + 1}{R_{out} \cdot R_f(C_{in}C_l + C_{in}C_f + C_lC_f)}} \tag{4.28}$$

The voltage controlled current source (g_{m2}) is not present in the relation for the bandwidth, this is because the TIA is modelled as a second order filter. The g_{m2} in this model has effect on the Q-factor of the filter. The Q-factor determines the flatness of the frequency transfer and can therefore increase or decrease the bandwidth of the TIA, for large Q-factors the bandwidth is higher than for a lower Q-factor.

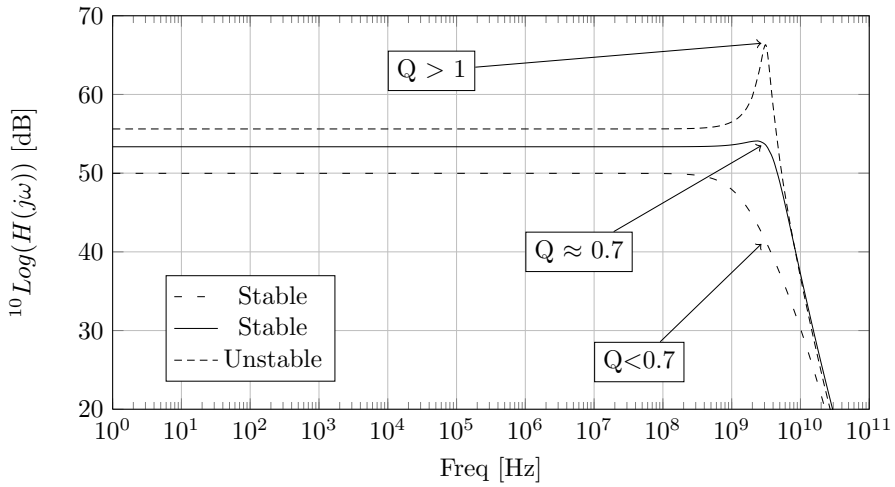


Figure 4.11: Frequency transfer for different Q factors

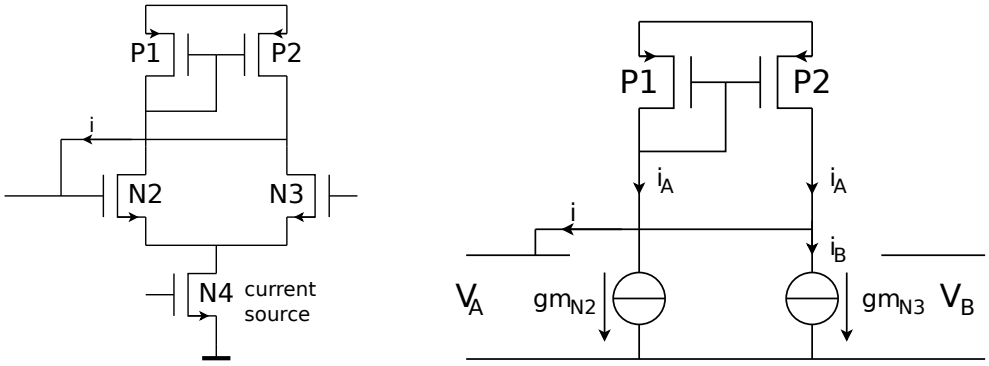
$$Q = \frac{\sqrt{R_{out} \cdot R_f(C_{in}C_l + C_{in}C_f + C_lC_f)(g_m \cdot R_{out} + 1)}}{R_{out} \cdot R_f\,(g_m \cdot C_f - g_{m2} \cdot C_{in}) + R_f\,(C_f + C_{in}) + R_{out}\,(C_{in} + C_l)} \tag{4.29}$$

The voltage controlled current source g_{m2} determines the stability of the circuit, the Q-factor is also a measure for the stability of the circuit. For a butterworth filter characteristic the Q-factor should be $\frac{1}{\sqrt{2}}$ to have a maximally flat frequency transfer. Three case with different Q-factors are shown in figure 4.11. Here can be seen that for high Q the bandwidth increases, but for too high Q-factors the TIA is oscillating. The gain and phase for the peak frequency ($Q > 1$) cause the TIA to oscillate.

The bandwidth can be influenced by three parameters: R_{out}, g_m and R_f. These parameters can be chosen freely in the design. The capacitances are parasitic behaviour and are therefore harder to change to the desired values. The output resistance of the TIA, R_{out} is chosen small to have a large bandwidth. g_m is chosen large but a too large g_m results adding significant capacitance to C_{in}. The feedback resistance is chosen with respect to the SNR and the bandwidth, a large R_f creates a large SNR, a small R_f creates a large bandwidth.

4.2.2 Design of the voltage controlled current source

The voltage controlled current source (g_{m2}) is implemented with a differential amplifier, taking the current output, the transistor implementation is shown in figure 4.12(a). The TIA circuit with g_{m2} is shown in figure 4.13.



(a) Transistor implementation

(b) Small signal model

Figure 4.12: Voltage controlled current source

The relations for g_{m2} are derived with the aid of the small signal model of the differential amplifier. A partial small signal model is shown in figure 4.12(b).

$$\begin{aligned} i_A &= v_A \cdot g_{m_{N2}} \\ i_B &= v_B \cdot g_{m_{N3}} \\ i &= i_A - i_B = v_A \cdot g_{m_{N2}} - v_B \cdot g_{m_{N3}} \\ i &= (v_A - v_B) \cdot g_{m2}|_{g_{m_{N2}}=g_{m_{N3}}=g_{m2}} \end{aligned} \tag{4.30}$$

The tail current source is used to tune g_{m2}.

The parasitics of the transistors influence the circuit behaviour, the output resistances of transistors N2 and N3 and of the current mirror decrease the g_m. g_{m2} is the effective VI gain of the differential amplifier and is given by (4.31). The output resistance in the branch of N3 also helps decreasing R_{out} of the TIA circuit, which is good for a high bandwidth. The parasitic capacitances added by the voltage controlled current source increase C_f and C_{out}, seen in figure 4.10.

$$g_{m2} = \frac{g_{m_{N2}} + g_{m_{N3}}}{2} \sum_{t=\{N2,N3,P1,P2\}} \frac{1}{\mu_t} \tag{4.31}$$

Where t is the transistor indication, N2 and N3 the input transistors and P1 and P2 the current mirror transistors.

4.3 Design of a common source TIA with bandwidth extension

The TIA is designed and simulated in a CMOS 65nm triple well process.
Designing the TIA is done in two steps: first the traditional common source TIA is designed and then the voltage controlled current source. The bias conditions of the traditional common source TIA are important for the voltage controlled current source. At last the two segments are added together and the biassing conditions are checked using a DC simulation. The transistors are designed using ProMost.

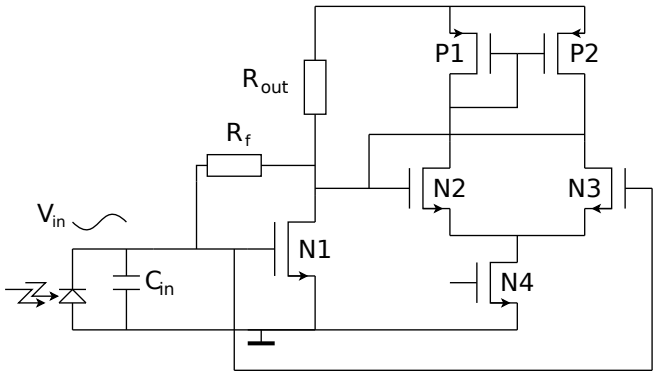


Figure 4.13: Transistor implementation of the common source TIA with bandwidth extension

4.3.1 Common source TIA

The DC voltage V_{OUT} is preferably as high as possible, in this way the input transistors N2 and N3 of the voltage controlled current source can have a sufficient V_{GT}, see figure 4.15(a). The V_{GS} of these transistors is limited by the voltage drop over the tail current source.
A high V_{OUT} also gives a high V_{GS} for the TIA transistor (N1) and this is undesired, because the current increases quadratically with V_{GS} where g_m increase linearly.
A good compromise is V_{OUT} = 700mV: for this value of V_{OUT} the current through the transistor is not unnecessarily high for the wanted g_m. Higher value for V_{OUT} give a large increase in current $I_D \propto V_{GT}^2$ but a smaller increase in $g_m \propto V_{GT}$. The V_{GS} is a bit lower, because of the dark current of the diode, this difference is about 5-10mV varying on the feedback resistor value. Transistor N1 is designed with W=40μm and L=60nm, L is chosen minimal length for a maximum g_m, W is chosen such that the gate capacitance is about 10% of the diode capacitance, $\approx$ 50fF. The resulting parameter values are listed in table 4.1, note that these results are with $R_{out} = 100\Omega$ and $R_f = 500\Omega$.

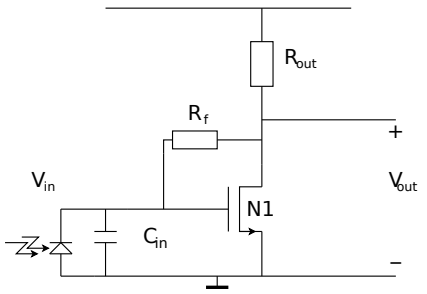


Figure 4.14: Traditional common source TIA

type	S_{V_T}
V_{GT}	341mV
V_{DS}	705mV
I_{DS}	4.94mA
W	40μm
L	60nm
Fold	40
g_m	28.7mS
r_{ds}	272 Ω

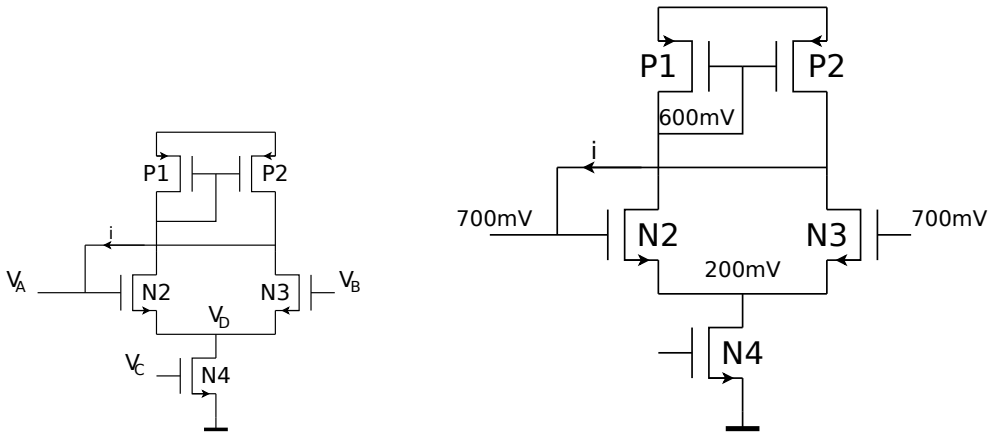
Table 4.1: Parameters of transistor N1

4.3.2 Voltage controlled current source

The VI gain of the voltage controlled current source is estimated with equation (4.26). Note that R_{out} in (4.26) is the parallel connection of R_{out} in the circuit and r_{ds_1} the output resistance of transistor N1. R_o is the parallel connection of the two resistors.

$$g_{m2} = \frac{R_o + R_f}{R_o \cdot R_f}$$
$$R_o = \frac{r_{ds_1} \cdot R_{out}}{r_{ds_1} + R_{out}}$$

$g_{m2} \approx 16$mS. The g_m of transistors N2 and N3 is estimated with equation (4.31) assuming $\mu \approx 6$ for the transistors. This gives $g_m \approx 24$mS for transistors N2 and N3. Note that this gives an approximation of the g_{m2} and this does not guarantee that the system is stable and at its maximum bandwidth.



(a) Node indication (b) Bias voltages

Figure 4.15: Voltage controlled current source

The voltages V_A and V_B of the voltage controlled current source are defined respectively by the voltages V_{OUT} and V_{GS} of the TIA. The transistor type chosen for the transistors N2 and N3 is a low V_T type, this enables a large g_m with a smaller V_{GS}. The V_{DS} of transistor N4 is chosen 200mV, to have a large V_{GS} for transistors N2 and N3 and enough voltage headroom to stay in the saturation region. The V_{DS} and V_{GS} value for transistor P1 is chosen 600mV.
The transistor parameters are listed in table 4.2.

Table 4.2: Transistor parameters for the voltage controlled current source

(a) N2&N3

type	L_{V_T}
V_{GT}	255mV
V_{DS}	500mV
I_{DS}	2.35mA
W	45μm
L	60nm
Fold	45
g_m	21.6mS
r_{ds}	323 Ω

(b) P1 & P2

type	L_{V_T}
V_{GT}	209mV
V_{DS}	500mV
I_{DS}	2.29mA
W	75μm
L	60nm
Fold	75
g_m	18.59mS
r_{ds}	363 Ω

(c) N4

type	S_{V_T}
V_{GT}	276mV
V_{DS}	200mV
I_{DS}	4.7mA
W	75μm
L	60nm
Fold	75
g_m	32.81mS
r_{ds}	97 Ω

4.3.3 DC simulations

The biassing conditions change when the entire circuit is simulated: the dark current of the photodiode gives an initial voltage over the feedback resistance, the voltage controlled current source therefore give a DC current that influences the bias conditions. The influence of the voltage controlled current source is not significantly on the bias conditions. The node voltages have changed, but the transistors are still in saturation.

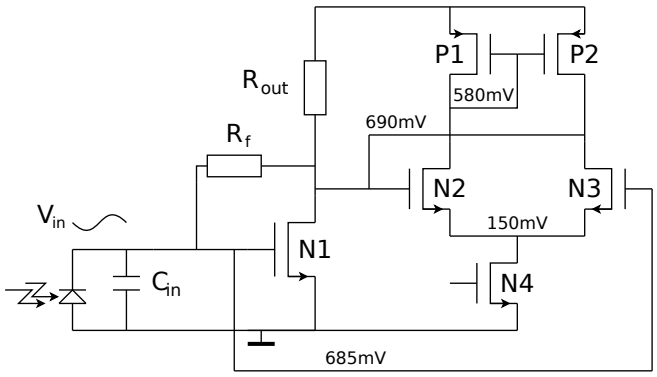


Figure 4.16: Bias conditions of the bandwidth extension TIA

With the tail current source the g_{m2} can be change significantly, with this tail current source the circuit can be tuned stable and with a maximum bandwidth. The updated transistor bias condition can be found in table 4.3.

	N1	N2	N3	N4	P1	P2
type	S_{V_T}	L_{V_T}	L_{V_T}	S_{V_T}	L_{V_T}	L_{V_T}
V_{GT}	325mV	284mV	293mV	342mV	238mV	230mV
V_{DS}	689mV	428mV	537mV	152mV	620mV	511mV
I_{DS}	4.45mA	2.96mA	3.29mA	6.25mA	2.96mA	2.64mA
W	40μm	45μm	45μm	75μm	75μm	75μm
L	60nm	60nm	60nm	60nm	60nm	60nm
Fold	40	45	45	75	75	75
g_m	27.44mS	24.45mS	26.18mS	32.19mS	21.68mS	20mS
r_{ds}	287 Ω	268 Ω	264 Ω	44 Ω	332 Ω	332 Ω

Table 4.3: Transistor parameters for the voltage controlled current source

Chapter 5

Simulation results

The simulation results of the noise cancelling TIA (section 4.1) and the bandwidth extension TIA (section 4.2) are given in this chapter. The simulation results of the noise cancelling TIA are given in section 5.1. The noise and frequency behaviour is shown and explained.
The simulation results of the bandwidth extension TIA are given in section 5.2. The -3dB bandwidth of the traditional common source TIA is compared to the bandwidth extension TIA.
Finally in section 5.3 the performance of a few published TIAs are compared to the bandwidth extension TIA.

5.1 Noise cancelling TIA

Simulations are done with the noise cancelling circuit shown in figure 4.3. The actual design of the common source TIA with noise cancelling is given in appendix A. These simulations are done with a TIA bandwidth of about 5GHz. The results for the noise cancelling TIA give insight in the signal and noise behaviour. The effect of v_s is discussed and explained by frequency responses.

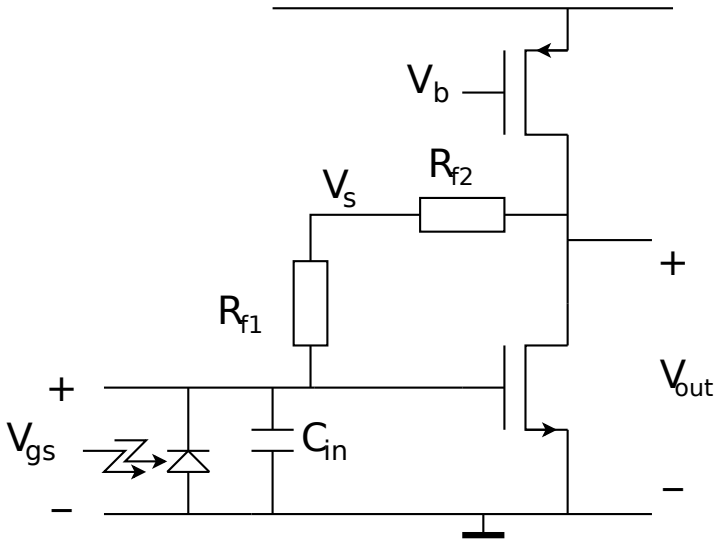


Figure 5.1: Frequency response of the noise cancelling TIA

5.1.1 Input signal

The frequency responses of $(v_{out} - v_s)/i_{in}$ and v_s/i_{in} are shown in figure 5.2. Note that v_s is a virtual ground for i_{in}, ideally the input signal would be zero.

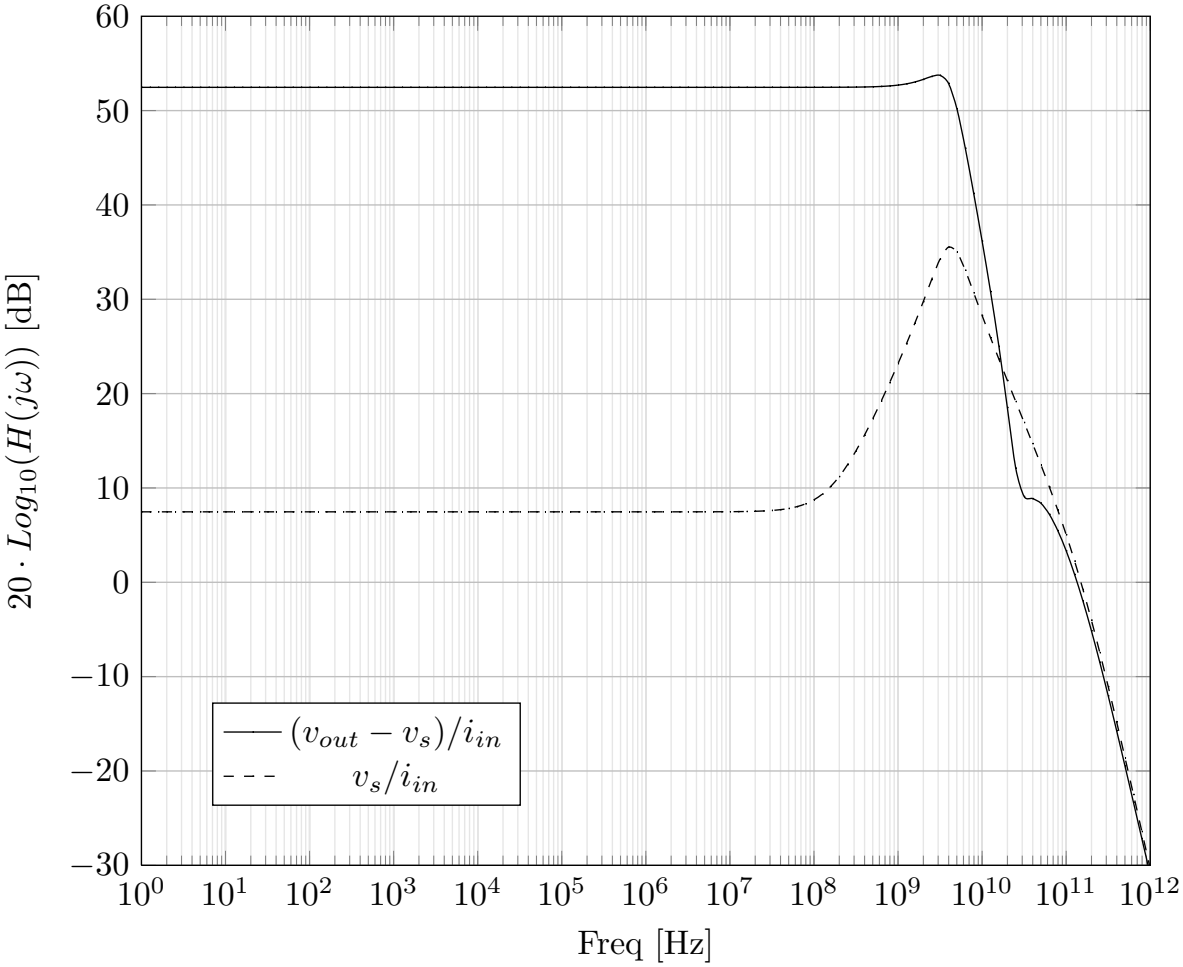


Figure 5.2: Frequency response of the noise cancelling TIA

The frequency transfer of v_s/i_{in} gives the virtual ground dependant on frequency, for low frequencies the difference of ≈45dB results in a good virtual ground. For higher frequencies the difference is decreased to≈20dB which results in a more worse virtual ground, the effect however is hardly recognizable in the frequency response of $(v_{out} - v_s)/i_{in}$.

5.1.2 Noise

Figure 5.3 gives the TIA frequency response and the frequency response for the noise $H_{n\,out\to s}$. $H_{n\,out\to s}$ given by equation (4.21) and the parameters listed in table A.1 give a calculated -3dB noise bandwidth of approximately 517MHz and -3dB TIA bandwidth of approximately 4.6GHz. These numbers are calculated with an approximation of the noise bandwidth and TIA bandwidth, the parasitic capacitance are not taken into account. The simulated bandwidths for the frequency responses are shown in figure 5.3.

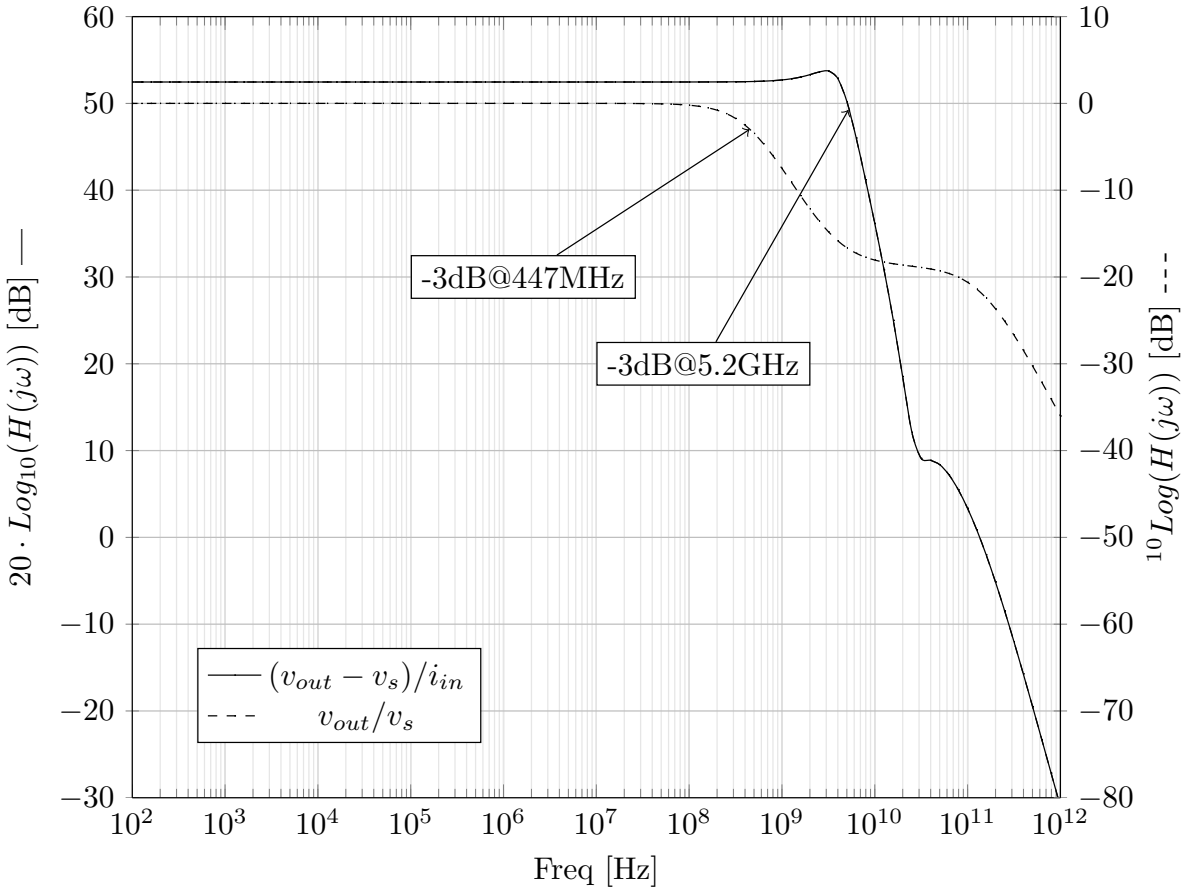


Figure 5.3: Frequency response of the noise cancelling TIA

Ideally for the noise cancelling to work the bandwidth of the noise should be equal or larger then the signal bandwidth.

Figure 5.4 gives the frequency response of the input referred noise density of the noise cancelling TIA and the traditional TIA.

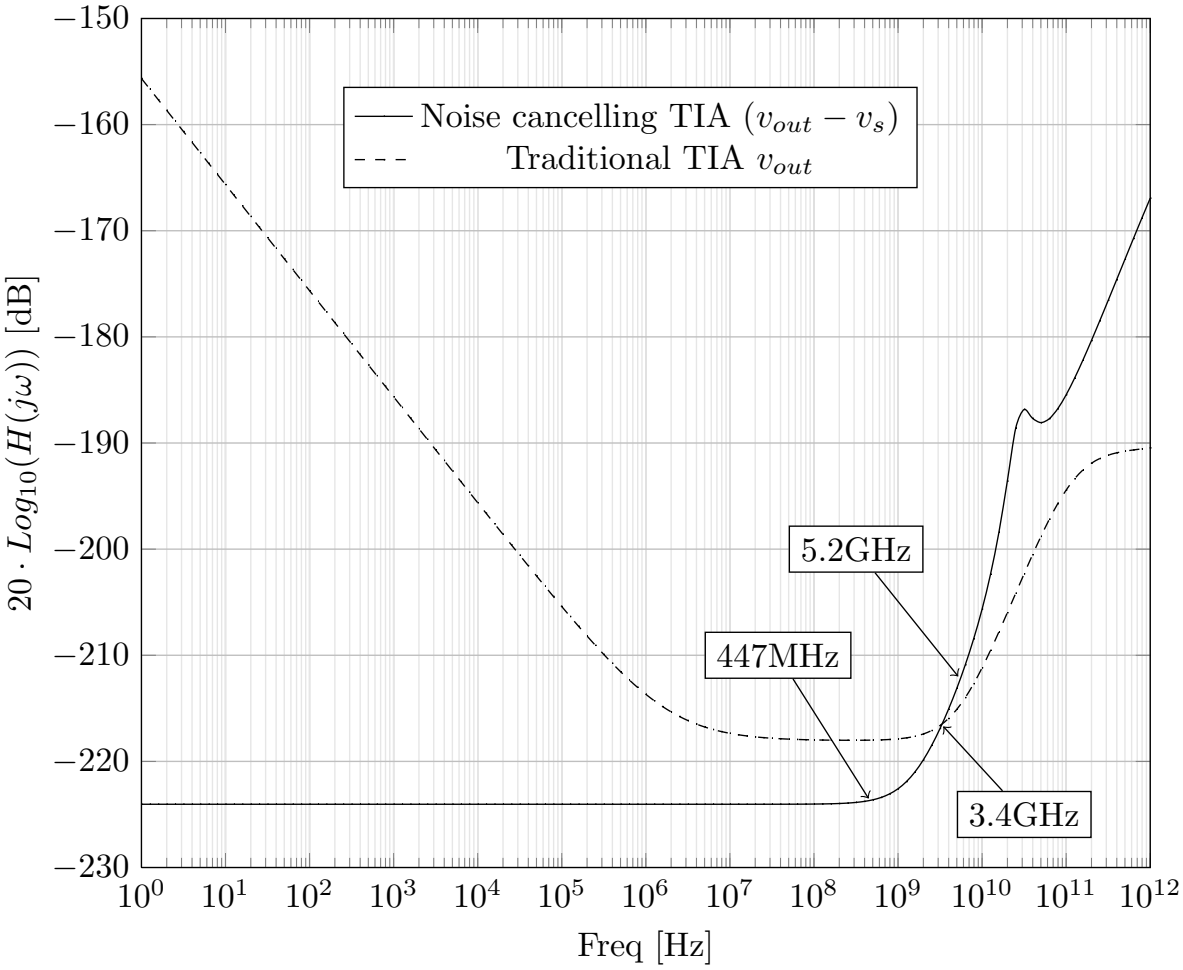


Figure 5.4: Frequency response of the input referred noise

This figure clearly shows the effect of the limited bandwidth for $H_{n_{out \to s}}$. For high frequencies the input referred noise density of the noise cancelling TIA increases. This increase in input referred noise density starts at the frequency where the noise transfer (4.21) has its -3dB point, 447MHz. The result of this increase at these high frequencies is a large integrated input referred noise current.
The input referred noise density of the traditional TIA crosses the input referred noise of the noise cancelling TIA at 3.4GHz. The -3dB bandwidth of 5.2GHz for the two TIAs is also given in the figure.

5.2 Bandwidth extension TIA

The simulation results of the bandwidth extension TIA are presented in this section; the cadence circuit is shown in appendix B. Bandwidth and noise behaviour of the bandwidth extension TIA is compared with the traditional common source TIA. Also mismatch and spread simulations are done for the bandwidth extension TIA.

5.2.1 Bandwidth

The -3dB bandwidth of the bandwidth extension TIA (with g_{m2}, figure 4.13) is compares with the traditional common source TIA (figure 3.2); the results are shown in figure 5.5. This comparison is based on equal transistor parameters for transistor N1 and with equal feedback resistances.

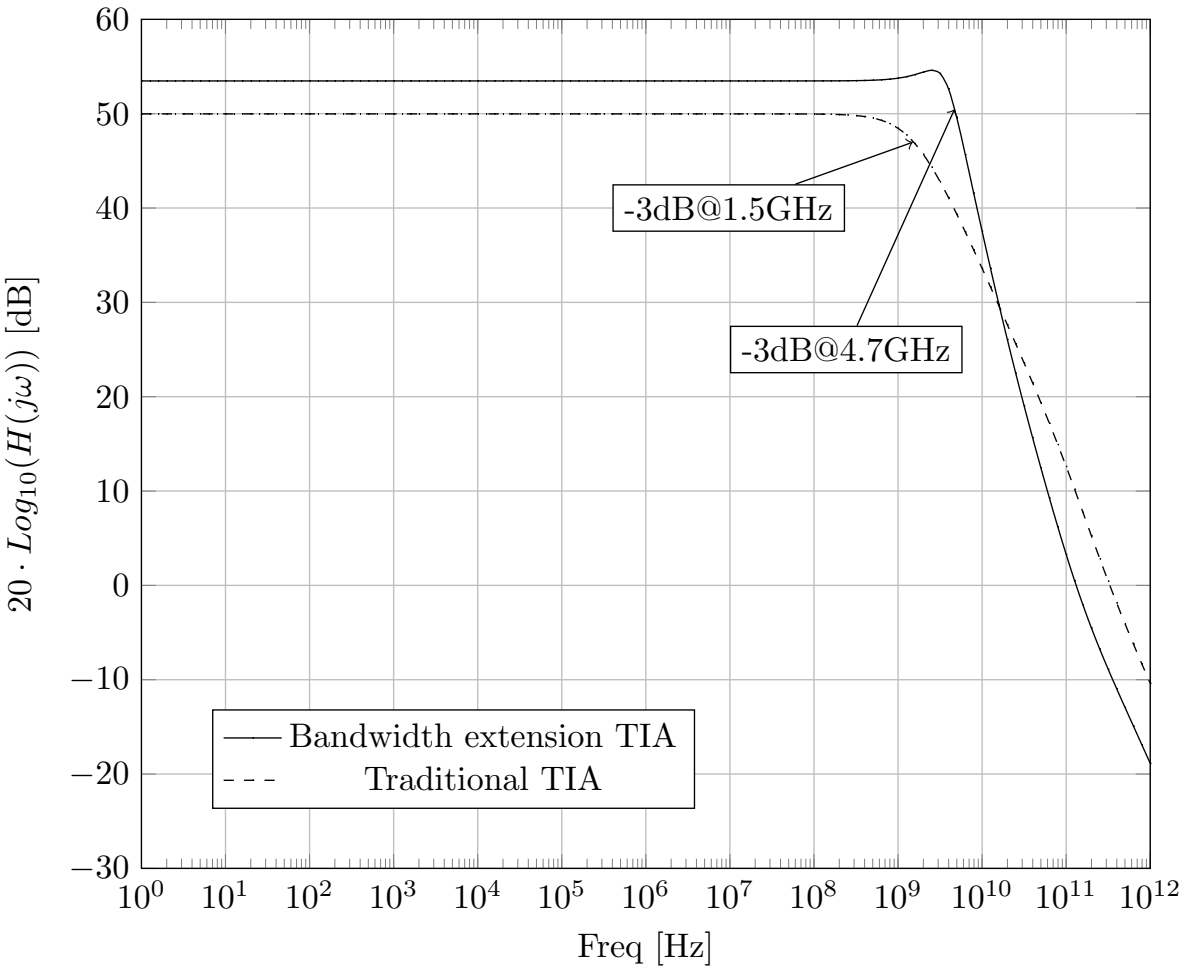


Figure 5.5: Frequency response of the traditional TIA and bandwidth extension TIA

The effect on the -3dB bandwidth is clearly visible, the bandwidth is extended by approximately a factor 3.

5.2.2 Noise

The noise performance of the TIAs is given by the integrated output noise of the system. The integrated noise of the TIAs is listed in table 5.1, the integrated noise of the traditional TIA is larger compared to the bandwidth extension TIA. The influence of g_{m2} is seen in the integrated noise, where the bandwidth extension TIA has a larger -3dB signal bandwidth and less integrated noise.
The output noise density of the TIAs is shown in figure 5.6. The output noise density of the traditional TIA compared to the bandwidth extension TIA is higher for frequencies larger than 11GHz, this causes the integrated noise to be larger for the traditional TIA. The output noise density of the bandwidth extension TIA is higher for frequencies below 11GHz because g_{m2} generates noise.

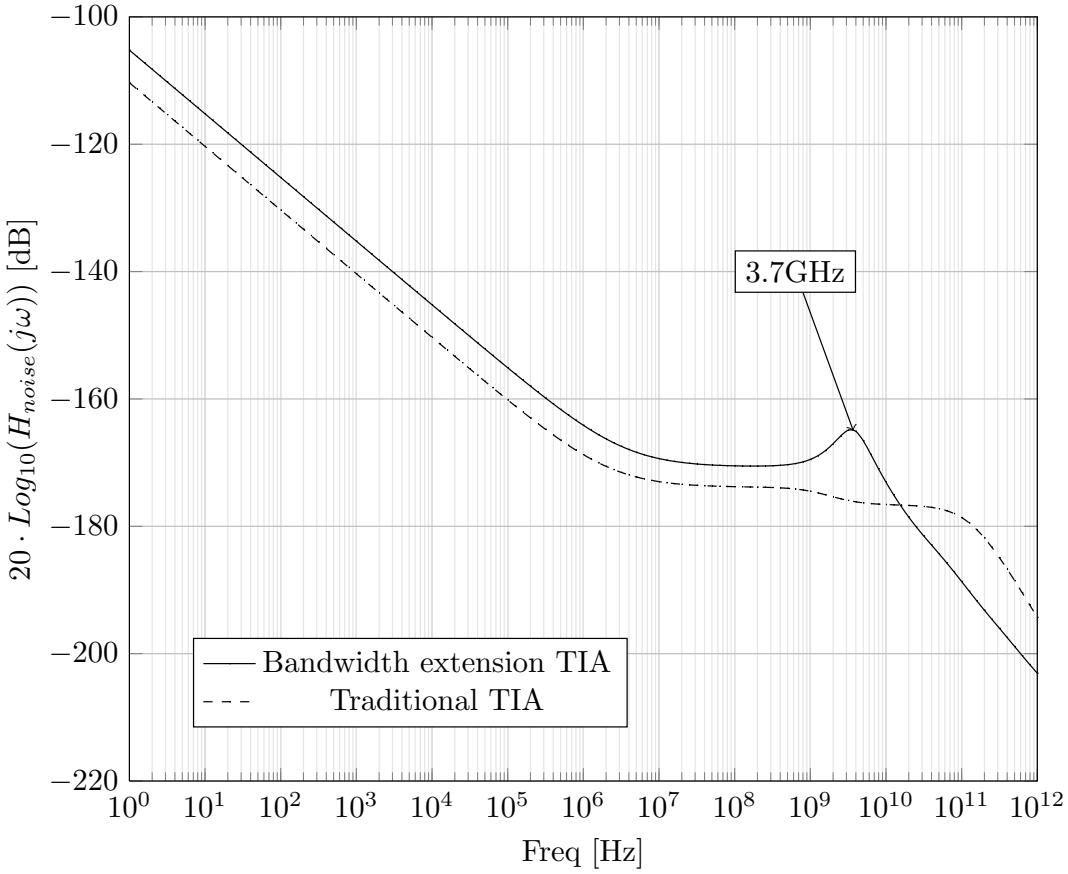


Figure 5.6: Output noise density of the traditional TIA and the bandwidth extension TIA

Table 5.1: Integrated output noise summary from 1Hz to 1THz

(a) Traditional TIA, figure 4.14

Transistor (T)	59.46 %
R_{out}	33.85 %
R_f	7.46 %
Total	$\overline{v_{n_{out}}} = 633\mu V$
Input referred	$\overline{i_{n_{out}}} = 2.25\mu A$

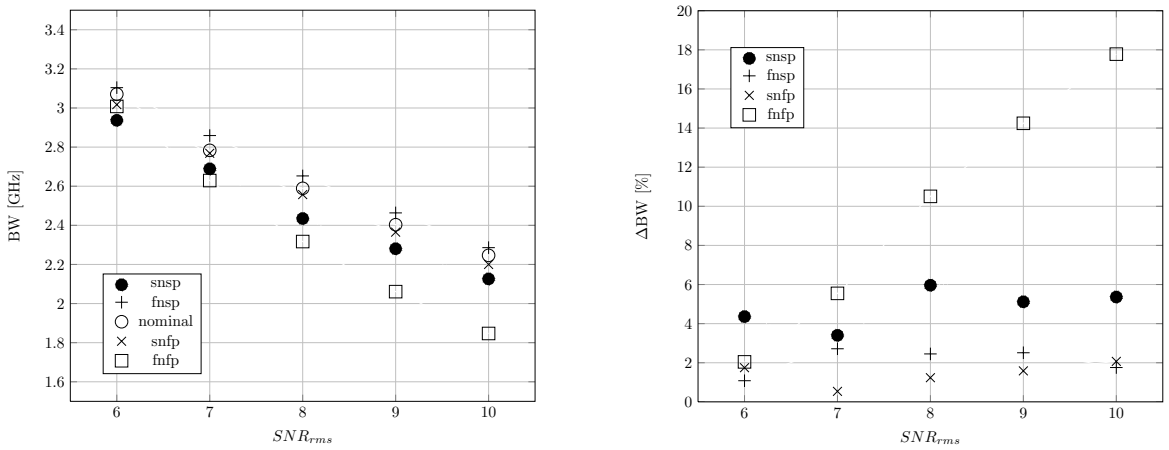
(b) Bandwidth extension TIA, figure 4.15(a) and 4.14

Transistor (T)	23.15 %
R_f	18.89 %
Transistor (2)	15.86 %
R_{out}	11.59 %
Transistor (B)	10.66 %
Transistor (A)	7.61 %
Transistor (1)	6.35 %
Total	$\overline{v_{n_{out}}} = 490\mu V$
Input referred	$\overline{v_{n_{out}}} = 1.1\mu A$

5.2.3 Mismatch and spread

Mismatch simulation using Monte Carlo (100 runs) give good results for the bandwidth extension TIA. The TIA is calibrated using g_{m2} in a stable position with a certain bandwidth, the results of the Monte Carlo simulation are that the fluctuations in bandwidth is limited to maximum 3%. The bias voltages of the TIA do not change significantly, roughly about 7mV compared to the nominal bias voltages.

The spread is simulated using 4 different process corners and the nominal setting. The TIA is simulated for 5 different signal-to-noise ratios sweeping the 4 different corner and the nominal setting. This gives a bandwidth of the TIA for a corner and a SNR, this bandwidth is plotted and gives this the influence of the corners for different SNR.
For each corner and SNR the TIA is calibrated using g_{m2}, the TIA is calibrated for a Q≈1. g_{m2} is calibrated using the bias voltage of the tail current source. This simulation gives knowledge of the tune ability of g_{m2} at the different corners. The simulation results are shown in figure 5.7(a).
The relative spread in bandwidth is shown in figure 5.7(b). The relative spread in bandwidth is calculated: $\Delta BW = \frac{BW_{corner} - BW_{nominal}}{BW_{nominal}}$ in percentage.



(a) Bandwidth for different SNR and corners

(b) Relative change in bandwidth compared to the nominal bandwidth

Figure 5.7: Spread simulation for different corners swept over SNR

The relative change in bandwidth for the corners fnsp and snfp stays within 3%. This means that the TIA can be tuned well for the corners. The snsp corner fluctuates more and tuning has less influence. The most worse corner is the fnfp for high SNR values, this corner is therefore hard to tune.
The relative change in bandwidth for the fnfp corner stays within about 18%, the other corners stay within the 6% change in bandwidth.

5.2.4 Constant SNR to Bandwidth relations

A common method for increasing the SNR in voltage-to-voltage and current-to-current amplifiers is W-scaling. However in TIAs W-scaling is more complex because the feedback resistance is not scalable with W. Normally the SNR increases with increasing W, in a TIA however if W increases the feedback resistance decreases and therefore the SNR of the TIA decreases.

In this section W-scaling of the transistors and the output resistance of the TIA (R_{out},figure 4.13) is performed to obtain the influence of W-scaling.
The influence is simulated by sweeping the W-scaling factor while maintaining a constant SNR (by scaling R_f). During the sweeping of the W-scaling factor the bandwidth extension TIA is constantly calibrated for a Q≈1. The Q factor is calibrated by changing g_{m2} this is done by changing: 1) the bias voltage of the tail current source 2) the width of the transistors (additionally to the W-scaling).

The results of the traditional TIA (W and R_f scaling) and bandwidth extension TIA (W, R_f and g_{m2} scaling) are seen in figure 5.8.

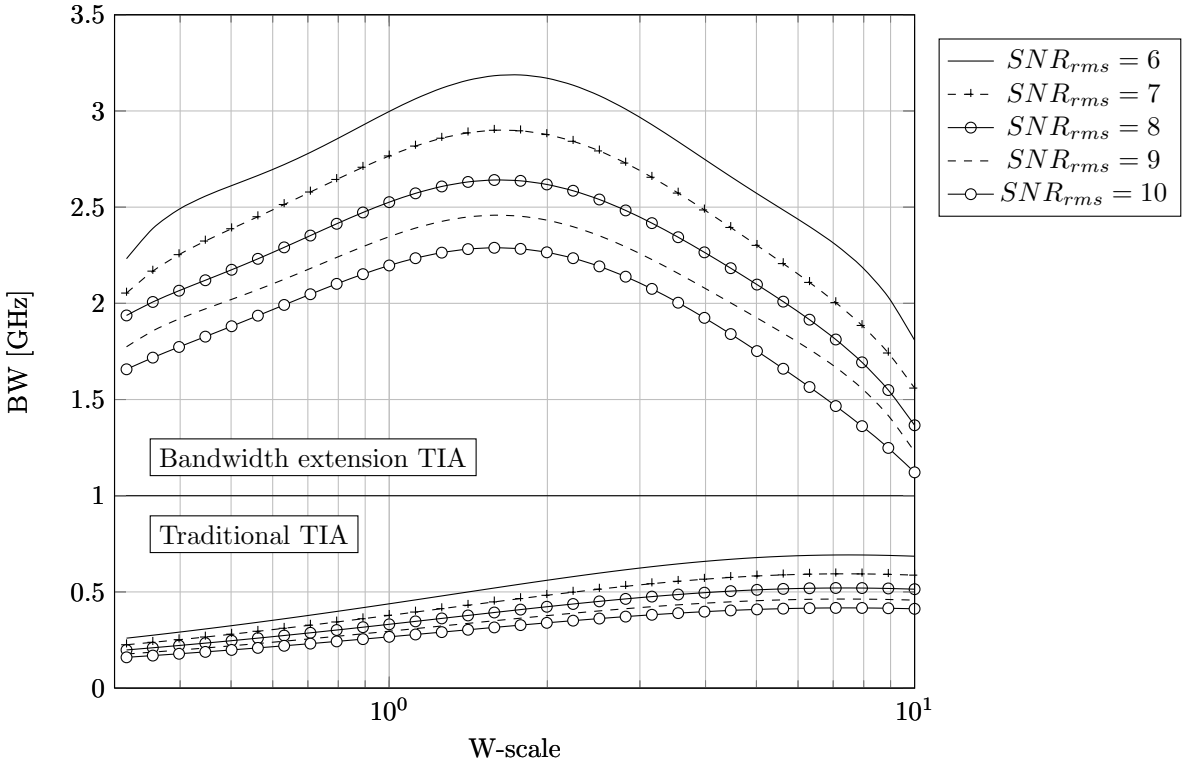


Figure 5.8: Bandwidth for the traditional and bandwidth extension TIA, for constant SNR ($L_T = 60nm$)

The bandwidth extension is clearly seen, the effect of the g_{m2} is significant. The maximum bandwidth for the bandwidth extension TIA is at the W-scaling factor of approximately 1.8, where the maximum bandwidth for the for the traditional TIA is at the W-scaling factor of approximately 8. The traditional TIA uses approximately 2 times more power then the bandwidth extension TIA at its maximum bandwidth. The ration between the maximum bandwidth of the bandwidth extension TIA and the traditional TIA are:

$$SNR_{rms} = 6 \rightarrow 4.5$$
$$SNR_{rms} = 7 \rightarrow 4.7$$
$$SNR_{rms} = 8 \rightarrow 5$$
$$SNR_{rms} = 9 \rightarrow 5.1$$
$$SNR_{rms} = 10 \rightarrow 5.3$$

If the length of transistor N1 is changed to L=100nm, for the traditional TIA and the bandwidth extension TIA. The influence of g_m of transistor N1 on the bandwidth is obtained.

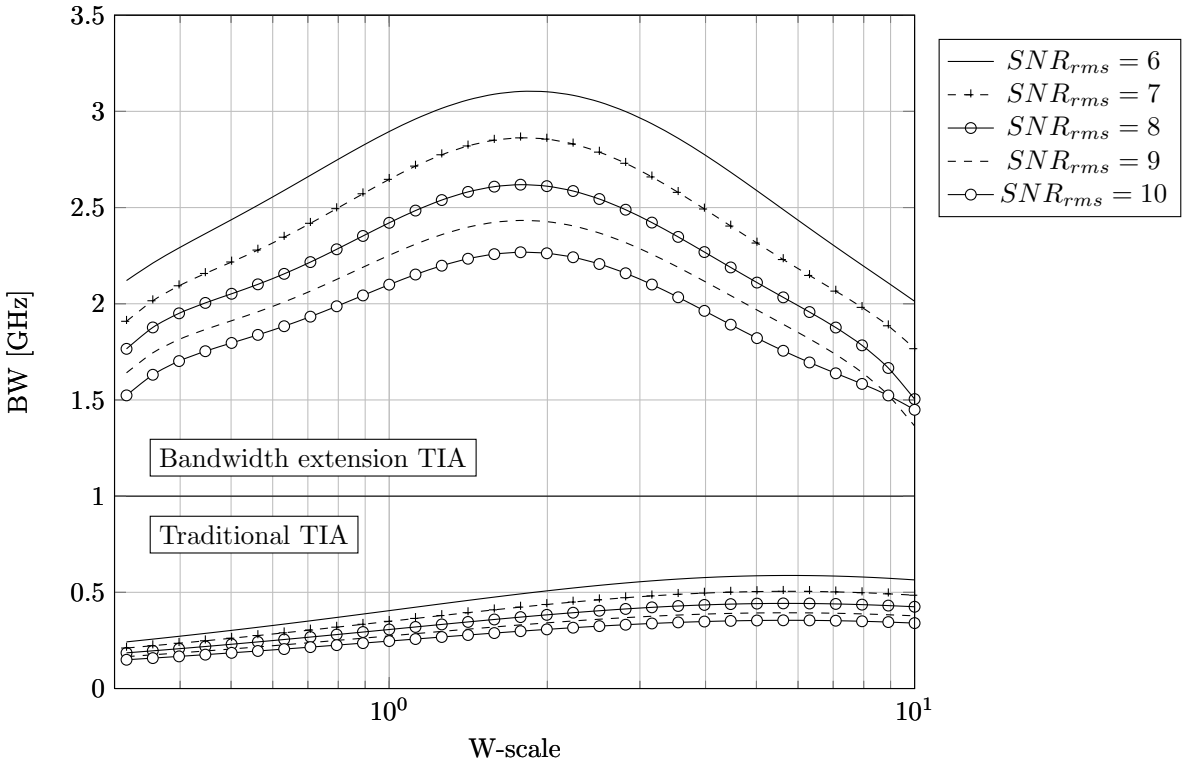


Figure 5.9: Bandwidth for the traditional and bandwidth extension TIA, for constant SNR ($L_T = 100nm$)

For the traditional TIA this change has a large influence, the bandwidth is decreased in the order of 200MHz, which is about 18% less bandwidth.
The bandwidth of the bandwidth extension TIA is also deceased in the order of 200MHz, which is about 4.5% less bandwidth.

Secondly the W-scaling factor at which the maximum bandwidth is located has changed, for the bandwidth extension TIA this is slightly larger and for the Traditional TIA this is much smaller.

5.3 Comparing TIAs

This section compares TIA that have already been published to the bandwidth extension TIA designed in this report. The benchmark it the bandwidth extension TIA simulated with the same C_{in} and input referred noise

Ref.	bandwidth (GHz)	Gain (dBΩ)	Noise (pA/$\sqrt{Hz}$)	C_{in} (fF)	Power (mW)	Technology
[3] [2]	21.6	46.7	30	200	39.9	65nm CMOS
benchmark	14.19	38.9	30	200	23	65nm CMOS
[6]	2.5	76	7 [3]	500	7.2	0.18μm CMOS
benchmark	2.5	60.4	7	500	35.3	65nm CMOS
[5]	13.4	52.8	28	220	2.2	80nm CMOS
benchmark	13.27	39	28	220	25.5	65nm CMOS
[2]	≈10	57	35	370	1.8	0.13μm CMOS
benchmark	13	35.8	35	370	35.5	65nm CMOS
[4]	3.5	60	20	250	16.5	0.5μm 3M1P CMOS
benchmark	9.84	44.4	20	250	23	65nm CMOS

Table 5.2: Bandwidth extension TIA comparison with already published TIAs

[2] includes 2 inductors

[3] <7pA/$\sqrt{Hz}$ (0.1-0.9GHz)

Chapter 6

Conclusion and recommendations

This thesis presents an analysis and extension to the well known common source TIA. The proposed techniques in this thesis increases the bandwidth while reducing noise. These techniques brought a new view on the common source TIA; where the noise-bandwidth trade-off is usually the bottleneck for high-bandwidth low-noise applications, these techniques enable to shift this bottleneck to higher frequencies and lower noise.

The noise cancelling TIA could be designed for extreme low noise within the noise bandwidth of the TIA. This TIA is therefore a good solution for low-noise and low-bandwidth applications.

The bandwidth extension TIA employs active (asymmetric) feedback that yields a larger bandwidth for a specified noise level. In comparison with the traditional common source TIA, the bandwidth extension TIA gives a factor 4 larger bandwidth.
The ability to tune the voltage controlled current source of the TIA has a lot of advantages. One of these is keeping the influence of spread within bounds. Also the TIA could be tuned to be stable and with a large bandwidth.

The bandwidth extension TIA presented in this thesis could be used in digital optical receiver systems designed in 65nm standard CMOS. This TIA is designed for data rates of 5.2Gb/s, with an $SNR_{rms} = 8$ ($BER = 10^{-12}$), for an input current $i_{rms} = 3.263\mu$A and a power consumption of 20mW.

6.1 Recommendations

The input capacitance and the parasitic capacitances at the output limit the TIA bandwidth. The output parasitic capacitance are not clearly known, since the designs in this thesis have not been verified with layout extraction simulations. The layout extraction could potentially reveal other parasitic influences that have effect on bandwidth and noise characteristics of the TIA.

Further research on parasitic capacitances is preferred. The TIA bandwidth can be enlarged by reducing and cancelling (parasitic) capacitances. The recommended node to investigate reduction and cancelling of parasitic capacitances is the output node of the TIA. Cancelling the input capacitance with an active circuit could add too much input referred noise. Cancelling parasitic capacitances at the output with an active circuit gives noise at the output which results in input referred noise attenuated by the transimpedance gain.

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Appendix A

Noise cancelling TIA design

The design of the noise cancelling TIA is given in this chapter, the bias conditions and the circuit parameters. Figure A.1 gives the bias conditions of the noise cancelling TIA and table A.1 gives the circuit parameters.

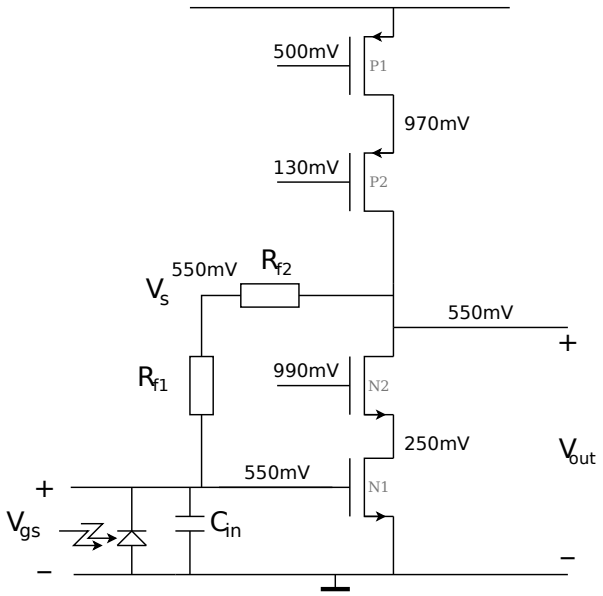

Figure A.1: Bias conditions of the single stage cascoded TIA with resistive feedback

The transistor parameters of the circuit:

Table A.1: Circuit parameters for the noise cancelling TIA

(a) Impedances

R_{f1}	53Ω
R_{f2}	420Ω
C_{in}	650fF

(b) Transistor parameters

	N1	N2	P1	P2
type	S_{V_T}	L_{V_T}	L_{V_T}	L_{V_T}
V_{GT}	325mV	284mV	238mV	230mV
V_{DS}	689mV	428mV	620mV	511mV
I_{DS}	4.45mA	2.96mA	2.96mA	2.64mA
W	40μm	45μm	75μm	75μm
L	60nm	60nm	60nm	60nm
Fold	40	45	75	75
g_m	27.44mS	24.45mS	21.68mS	20mS
r_{ds}	287 Ω	268 Ω	332 Ω	332 Ω

Appendix B

Bandwidth extension schematic

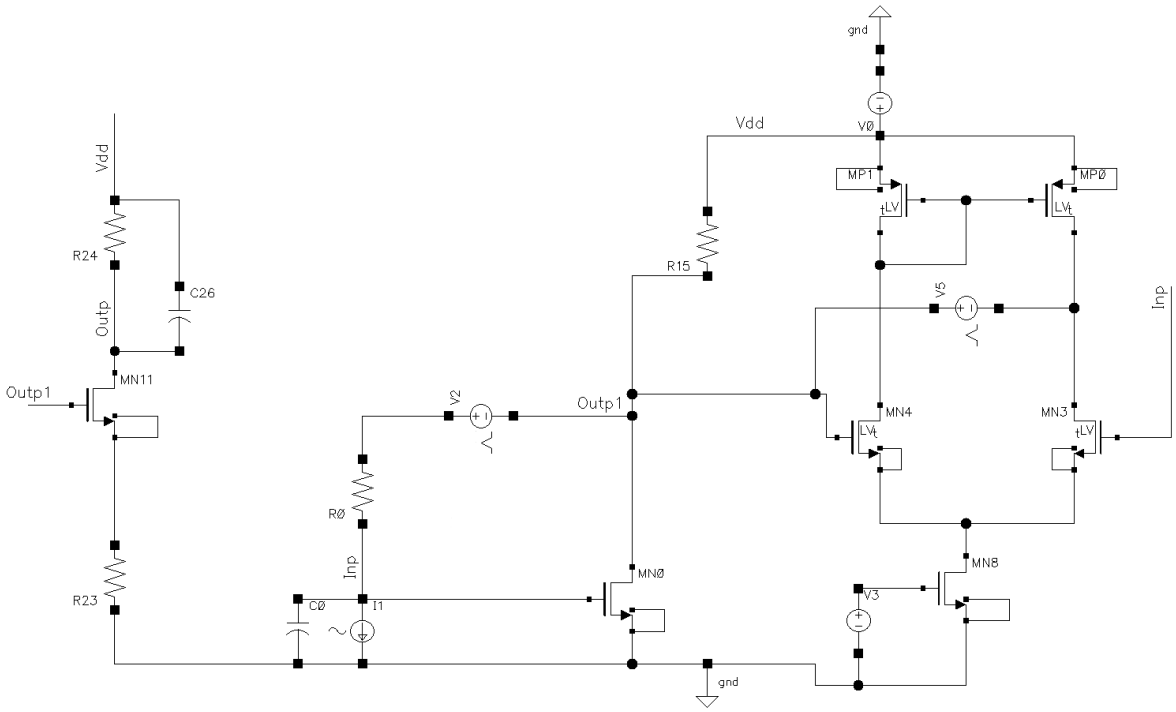

Figure B.1: Cadence circuit of the bandwidth extension TIA

The sources V2 and V5 are used to observe the transient stability, these source give a pulse within both the loops in the circuit.