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Feasibility study for a clock-controlled analog beamforming frontend

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MSc. Thesis

January 2010

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Abstract

In this work, a beamforming receiver system is presented that applies amplitude and phase adjustment by a passive mixer concept. A passive mixer is very linear and therefore suitable for canceling strong interference (nulling). In a concept proposed by Farzaneh et al. called 'A novel amplitude-phase weighting for analog microwave beamforming', amplitude and phase adjustment are realized by adjusting the pulse width and phase of a square wave LO (local oscillator) driving the mixer. This way of implementing amplitude and phase adjustment within a passive (switching) mixer relies on timing, which can perfectly exploit the benefits of CMOS technology: digital timing, very good switching capabilities and relatively low-costs.

In this work two important equations are derived: the first equation predicts the maximum possible null depth as a function of the number of bits with which the pulse width is controlled. The second equation predicts the maximum possible null depth as a function of the bandwidth of interferers, angular uncertainty of the interferers and the number of nulls that are working together.

Furthermore a beamforming circuit level design is proposed that is able to generate a LO clock at 1 GHz with variable phase and variable pulse width. With this LO clock, gains between 0.38 and 1 can be made together with phase shifts between 0 and 360 degrees. According to the derived equations and assuming that there are enough antenna elements, the system is expected to suppress interferers at least 20 dB. The system is able receive signals between 500 MHz and 1 GHz.

Contents

Chapter 1

Introduction

More and more applications use mobile radio communication: for example phones, wifi terminals, Bluetooth devices and mobile navigation devices. Therefore the multi-GHz band becomes more and more 'filled' with transmitters, each needing its own frequency band. The more transmitters in a limited bandwidth are present, the harder the filtering demands on the transmitter and receiver side become: power amplifiers in a transmitter generally suffer from spurious sidebands and harmonic distortion that has to be filtered in order not to interfere with other transmitters. Incoming signals in a receiver also have to be filtered to get rid of adjacent frequencies. A measure for the 'quality' of the received signal in a receiver is the signal-to-interferer ratio (SIR), which, for a fixed bandwidth, is directly proportional to the data capacity (bits per second). Better (higher-order) analog filters improve the SIR but they mostly work on a fixed frequency, which is undesirable for many applications like software defined radio and cognitive radio. In addition, high-order analog filters increase power consumption, circuit complexity, chip/pcb area and costs.

Another way to make more efficiently use of limited frequency space is to use beamforming[1]: multiple transmitters in the same area all can use the same frequency, but are mainly transmitting into the direction of the receiver and not into other directions. Therefore other receivers don't 'notice' the transmitter. The role of transmitters and receivers can be interchanged in this situation: receivers can 'listen' only into the direction of the transmitter, and ignore other transmitters. In other words: receivers can suppress ('null out') the other transmitters.

Beamforming has three main advantages over reception with a single antenna:

- Beamforming improves SIR because only the desired signal is strongly received and interferers can be suppressed on the receiver side. Applying

[1]Other terms referring to beamforming systems are 'synthetic aperture antennas', 'smart antennas' and 'phased array antennas'.

beamforming on both the transmitter and receiver side will improve SIR *even more*.

- Beamforming makes receivers more immune to *multipath fading*, the effect where reflections of waves (for example on buildings) interfere and (partly) cancel each other at the position of an antenna. This is because the receiver mainly looks into a single direction (directivity).

- Using beamforming increases the SNR (signal-to-noise ratio) because signals of different antennas in an array can be coherently added in amplitude, proportionally to their power squared, while noise (due to the antenna output impedance) is added in power. Another way to describe this advantage is by noting that multiple parallel antennas, each with an output impedance of say 50 Ohm, are equivalent to one antenna with a lower output impedance (so a lower noise figure).

In order to 'steer' the beam into a specific direction, every antenna element needs it's own *phase shift* and *amplification*. Nowadays only specialized, expensive technologies are suitable for implementing variable gain and delay circuits, which is why the use of beamforming is currently limited to military and some other specialized applications. To make beamforming available in consumer applications, it would be beneficial to implement it in low cost CMOS technologies. However amplifying and delaying signals in CMOS technology is difficult: variable-gain amplifiers are non-linear and typically consume significant power. Adjustable delays are generally implemented in CMOS by analog phase shifters which suffer from frequency-dependant gain, which digitally needs to be corrected. This needs exact knowledge of the circuit characteristics in the digital domain, which is often not available. And analog phase shifters use analog components that tend to consume high chip area. Therefore it is beneficial to look for other solutions that can be implemented in CMOS technology, preferably based on digital logic since digital power consumption scales with technology but analog power consumption doesn't.

1.1 Idea

In this thesis a different way of combining phase and amplitude weighting is exploited: every antenna signal is multiplied by a repeating pulse waveform (from a local oscillator, 'LO'), of which the *phase* and *pulse width* can be controlled (see Figure 1.1). By adjusting the pulse width of the LO, the amplitude of the downmixed signal can be adjusted. By adjusting the phase of the LO, the phase of the downmixed signal can be adjusted. In this way the system acts simultaneously as downmixer, multiplier and phase shifter. This idea was first offered by [4] although this group didn't aim to do implement it in CMOS. To our knowledge this is the first attempt to exploit this idea in CMOS technology.

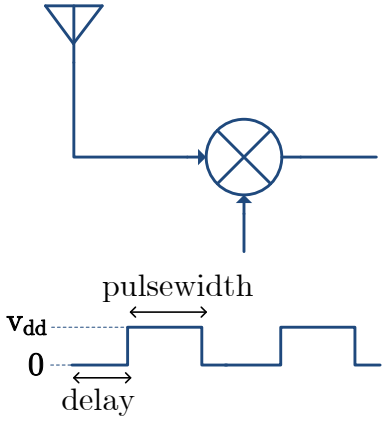


Figure 1.1: Idea used in this thesis to scale and delaying every antenna signal

The strong point of this idea is that only switches are needed to perform multiplication and phase shifting, combined with some electronics that generate the LO signal. Making very good switches is easy in CMOS technology. In addition, there is no precision electronics needed to amplify the signal with a particular gain. In stead, everything depends on timing. Timing can be highly accurate in CMOS when the digital possibilities of CMOS are exploited.

This thesis aims to find an answer to the following questions:

1. Given a system that applies amplitude weighting and phase adjustment through switching, with a certain number of phase and amplitude control bits and a given range of realizable phase- and amplitude values, what will be the nulling performance? This question will be answered in chapter 3.

2. What is a feasible implementation of this system in CMOS that applies amplitude weighting and phase adjustment through switching? This question will be answered in chapter 4.

Chapter 5 presents simulation results confirming the theory of nulling performance and feasibility of the implemented system in CMOS.

Chapter 2

Problem description and system level design

2.1 Problem description

Suppose a set of N antennas in a linear array to perform beamforming. Aim of this assignment is to demonstrate that it is possible to perform beamforming in CMOS technology by means of a downmixer with adjustable LO pulse width and phase (see Figure 1.1). Every antenna is attached to such a downmixing frontend. To demonstrate the principle we will design an implementation of the proposed system in 65nm. CMOS technology and evaluate it's effectiveness with respect to nulling.

In this section it suffices to regard an ideal mixer which multiplies the RF signal with a trapezoid-shaped periodic waveform (which is a decent approximation of a square wave with finite rise and fall times). One period of such a trapezoid-shaped waveform is shown in Figure 2.1.

Mathematically this trapezoid-shaped waveform can be written as a sum of

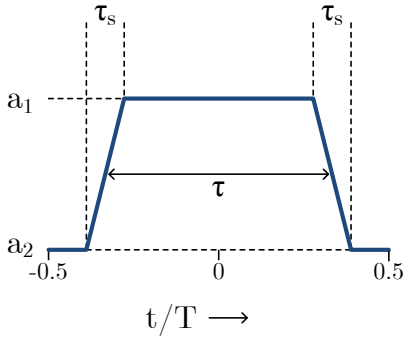


Figure 2.1: A trapezoid-shaped waveform $p(t)$. Note that the time axis is normalized to period T.

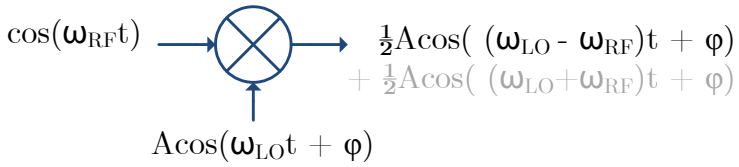


Figure 2.2: A mixer is transparent for amplitude (A) and phase (φ).

it's harmonics:

$$p(t) = \sum_{n=-\infty}^{\infty} c_n e^{\frac{j2\pi nt}{T}} \tag{2.1}$$

$$c_n = (a_1 - a_2)\frac{\sin(\pi n\tau)}{\pi n}\frac{\sin(\pi n\tau_s)}{\pi n\tau_s} \tag{2.2}$$

When the trapezoid-shaped waveform is delayed by τ_d (in seconds, so not normalized) we can write:

$$c_n = (a_1 - a_2)\frac{\sin(\pi n\tau)}{\pi n}\frac{\sin(\pi n\tau_s)}{\pi n\tau_s}e^{j\omega_{LO}\tau_d} \tag{2.3}$$

Here $\omega_{LO} = \frac{2\pi}{T}$.

We see that the amplitude of the first harmonic (c_1) scales with the sinusoid of the pulse width τ:

$$|c_1| \propto sin(\pi\tau) \tag{2.4}$$

c_1 has a maximum at $\frac{a_1-a_2}{\pi}$. The rising and falling edge time τ_s can be regarded small, in the order of 20 to 50 ps for CMOS 65 nm technology. For (infinitely) small τ_s the trapezoid-shaped waveform changes to a square waveform. It's Fourier coefficients change to:

$$c_n \approx (a_1 - a_2)\frac{\sin(\pi n\tau)}{\pi n}e^{j\omega_{LO}\tau_d} \tag{2.5}$$

We also see that for both the trapezoid-shaped wave and the square wave the phase of the first harmonic is directly proportional to the delay τ_d:

$$\angle c_1 \propto \omega_{LO}\tau_d \tag{2.6}$$

Because a mixer is 'phase-transparent' (see Figure 2.2), the phase of the output signal of the mixer also has this phase shift.

When multiplying a signal with a trapezoid we are effectively multiplying it with all the harmonics in the trapezoid. Because the amplitude and phase of the first harmonic can be adjusted, the phase and amplitude of the downmixed RF signal can be adjusted. We can use this principle to perform beamforming, although we have to take care that the higher harmonics don't ruin this nice result, and we have to propose a circuit that generates the trapezoid-shaped waveform.

2.2 System topologies

2.2.1 Superheterodyne vs. direct downconversion

Until now we have assumed that we mix down from RF to baseband in one step: in other words, we assumed a *direct downconversion receiver*. The most important disadvantage of direct downconversion is *local oscillator feedthrough*: due to capacitive coupling the LO signal is partly coupled to the RF port and mixed with itself, which generates a quasi DC component at the output.

Another way is to mix down in multiple steps: for example, first from RF to IF, and then from IF to baseband. This is called *superheterodyne receiving*. Local oscillator feedthrough is no problem in this topology because the input frequency band of all the mixers (at RF and IF) are not the same as the local oscillator frequencies. However, it needs generally very high-Q image rejection filters which cannot be integrated on chip. And nowadays the disadvantage of local oscillator feedthrough for direct downconversion can be partly compensated by means of digital signal processing [6]. In addition using direct downconversion has other advantages [9, 10]:

- Several standards such as GSM and UMTS can be implemented using a single receiver;
- The pre-mixing filter to suppress mirror frequencies can lower order and low-Q and can therefore be integrated on chip;
- The immunity to local oscillator harmonics is higher;
- The I and Q parts of the the quadrature paths don't have to be matched that good because the strength of the mirror frequencies is equally strong to the strength of the desired signal (as they originate from another transmitter which can be orders of magnitude stronger).

Considering these arguments, in this thesis we will assume a direct downconverter to be used.

2.2.2 Quadrature downconversion

When mixing 1 GHz down to 0 Hz with a LO of 1 GHz, both sidebands fall over each other and become inseparable. For AM this is no problem but for most other modulation schemes (like FM, QPSK) it is, because both sidebands contain independent information. Therefore a quadrature downconverter should be used (see Figure 2.3). By summing both the baseband I (BB_I) and baseband Q (BB_Q) signals the lower sideband can be recovered while by subtracting both I and Q signals the upper sideband can be recovered. Due to mismatch in the I and Q channel the separability of both sidebands in the quadrature downconverter is generally in the order of -20 to -40 dB. The low pass filters filter away the sum frequency (2 GHz).

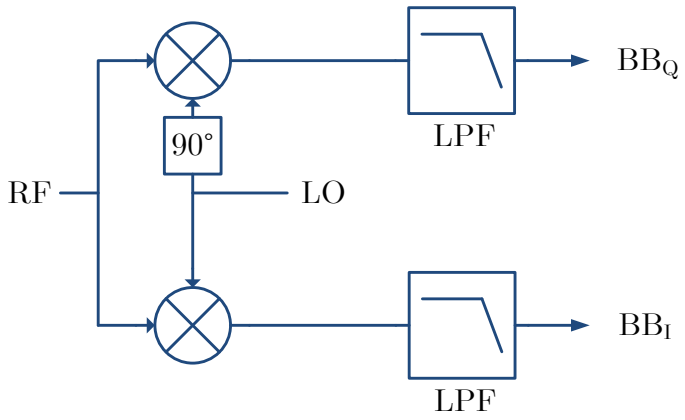


Figure 2.3: Quadrature downconverter

2.2.3 Mixer alternatives

For the mixer itself we can choose between an active Guilbert Mixer or a passive switching mixer.

Gilbert Mixer

A Gilbert Mixer [11] is an active mixer that, for small LO and RF signals, approximates an exact mathematical multiplier. It has the advantage that it can performing some amplification too. This can be very useful in receivers because a separate amplification stage can become superfluous. However, a Guilbert Mixer has a rather nonlinear transfer characteristic from the RF port to the output port. It therefore adds harmonic distortion and, more important, intermodulation distortion to the output. Intermodulation distortion is highly unwanted in receivers because it it is in-band distortion which is difficult to be filtered away once it is introduced.

Switching mixer

A passive switching mixer (Figure 2.4) is a mixer that alternately switches the RF input port to the output port, or ground to the output port[1]. It suffices to use only NMOSTs as switches since the amplitudes at RF side are generally small (at most about 200 mV peek-peek), so the switching circuit can be designed such that the switches always stay in strong inversion.

The LO port controls the switches, and should switch between two voltages ('on' and 'off'). Because the RF port is switched directly to the output port, the transfer characteristic of a passive switching mixer is very linear and (almost)

[1]At least 2 switches are needed. The switch to ground cannot be left out because otherwise the output would 'float' when the switch to the RF port is open, which makes the conversion gain from RF to output port less predictable

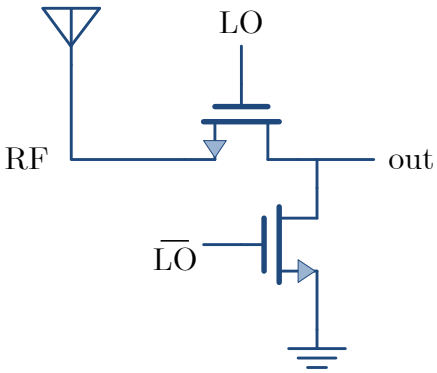


Figure 2.4: Switching mixer

immune to intermodulation distortion. A 2nd advantage of the passive switching mixer is it's very low flicker noise due to the lack of biasing [9].

Because CMOS technology can be used to produce almost perfect switches and because of the circuit simplicity, we choose for using a passive switching mixer.

2.2.4 LO harmonics

A drawback of any switching mixer is that it mathematically seen not only multiplies the RF signal with the LO clock, but also with multiples of the LO clock. A switching mixer with a LO frequency of 1 GHz generally mixes also with harmonics of the LO signal (at 2 GHz, 3 GHz etc.). These harmonics would mix down RF frequencies of 1.9 GHz, 2.1 GHz, 2.9 GHz, 3.1 GHz etc. to 100 MHz. In contrast with many mixing systems that use a LO clock with 50% duty cycle with only odd harmonics, our duty cycle cannot be fixed at 50% (because for our application the duty cycle should be adjustable). Therefore we will mix with both even and odd harmonics of the LO signal. Even when using a *balanced* mixer topology (as in Figure 2.5) the LO signal still contains odd harmonics. Nonetheless we prefer to use the balanced mixer topology because it has other advantages, such as a much more ideal conversion gain (in the sense that it follows the the sine-law of equation 2.4 much better).

To the problem of LO clock harmonics basically there exist the following solutions:

1. The RF frequencies of 1.9 GHz, 2.1 GHz, 2.9GHz, 3.1 GHz etc. partly can be filtered away from the RF signal prior to the mixer. This be done with analog filters but these filters usually work at a fixed frequency, which makes the receiver inflexible, and requires high-order filters.

2. In order to cancel the even harmonics, we should generate an LO signal that doesn't contain 2nd order components. Figure 2.6 shows two periods

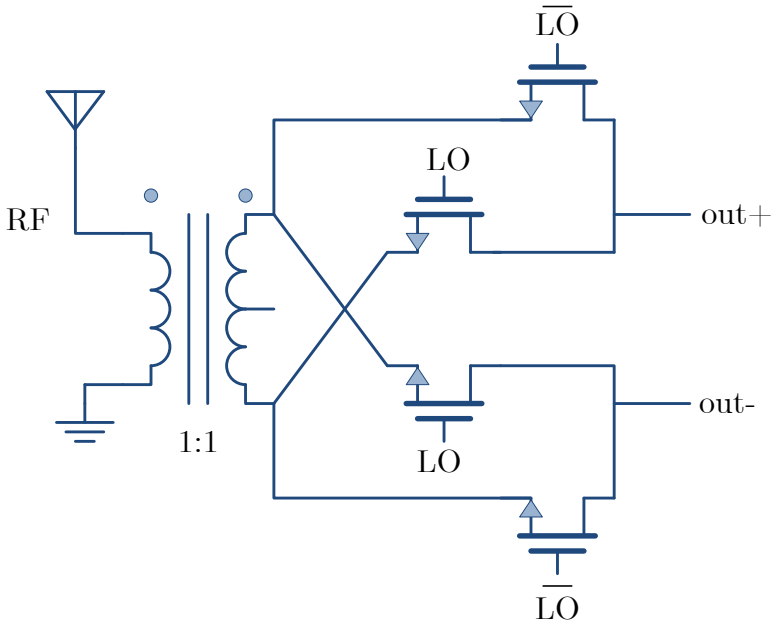


Figure 2.5: Balanced switching mixer. The transformer\'balun' is added to generate a differential antenna signal.

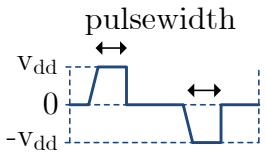


Figure 2.6: Example of a signal containing only odd harmonics.

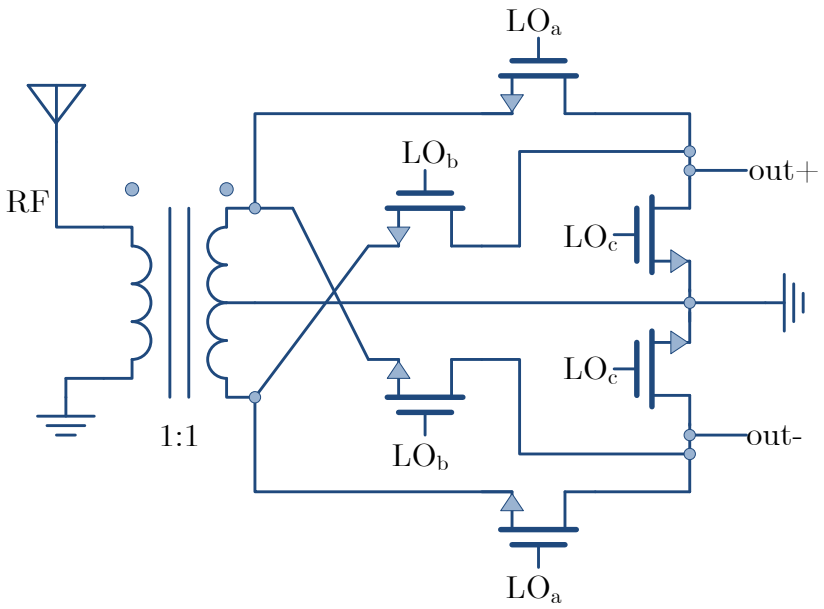


Figure 2.7: Modified balanced mixer for canceling even harmonics.

of such a signal. One can recognize such a signal for it's 2nd half which is a *vertically mirrored* version of the first half period. A way to implement such a mixer is by a slightly modified version of the 'normal' balanced mixer (see Figure 2.7). In this way the mixer output can be made positive, negative or zero. Figure 2.8 shows the waveforms that are needed to drive the switches of the modified balanced mixer. Only positive driving voltages are required so a negative power supply is not needed.

3. One can cancel additional odd LO harmonics, typically the 3th and 5th harmonic, by using a harmonic rejection mixer topology. This topology aims to approximate the sine wave more precisely than a square wave does, while keeping the benefits of using only switches in the mixer. This makes the generation of pulses somewhat more complicated. This falls outside the scope of this assignment but for reference one can take a look at [12, 14]. If one combines a harmonic rejection mixer with the previously mentioned way to reject even LO harmonics, the 7th harmonic is the first harmonic in the LO signal.

For the feasibility study described in this thesis, it suffices to use the balanced mixer from Figure 2.5. Note that this mixer has a maximum conversion gain of $\frac{2}{\pi}$. Therefore, for the mixer conversion gain as a function of pulse width pw in rad (where $pw = \pi$ means 50% duty cycle) we have:

$$\text{conversion gain} = \frac{2}{\pi}\sin(0.5pw) \tag{2.7}$$

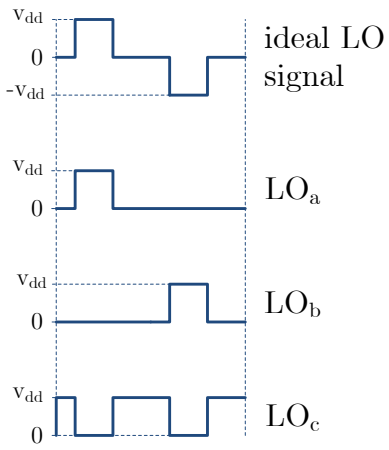


Figure 2.8: Waveforms for driving the modified balanced mixer switches.

2.2.5 Overview of the entire system

Figure 2.9 shows the entire proposed beamforming system with 3 antenna's. Suppose the system has to mix 1 GHz down to baseband (0 Hz) with a 1 GHz mixer. Then band-pass filter BPF1 filters the RF components around 2 GHz, 3 GHz etc. (partly) away, such that the LO harmonics don't convert these components to baseband, which would deteriorate our baseband signal. As said, further reduction of LO harmonics influence can be achieved by applying the modified balanced topology (which suppresses even harmonics), if necessary, combined with a harmonic rejection topology.

Low-pass filter LPF1 acts as an anti-aliasing filter for the ADC. The ADC itself[2] is chosen to be at the end of the chain. This way, less bits suffice because the beamforming part already has reduced strong interferers, limiting the necessary dynamic range.

The gain block performs multiple functions:

- It is used to amplify the antenna signal;
- It acts as a 50 Ohm load for the antennas;
- It shields the antennas for switching noise from the mixers (which otherwise would be transmitted back into the ether).

In Chapter 4 we will concentrate on the generation of the LO clocks that drive the switches.

[2]actually we have 2 ADC's because of the quadrature sum signal

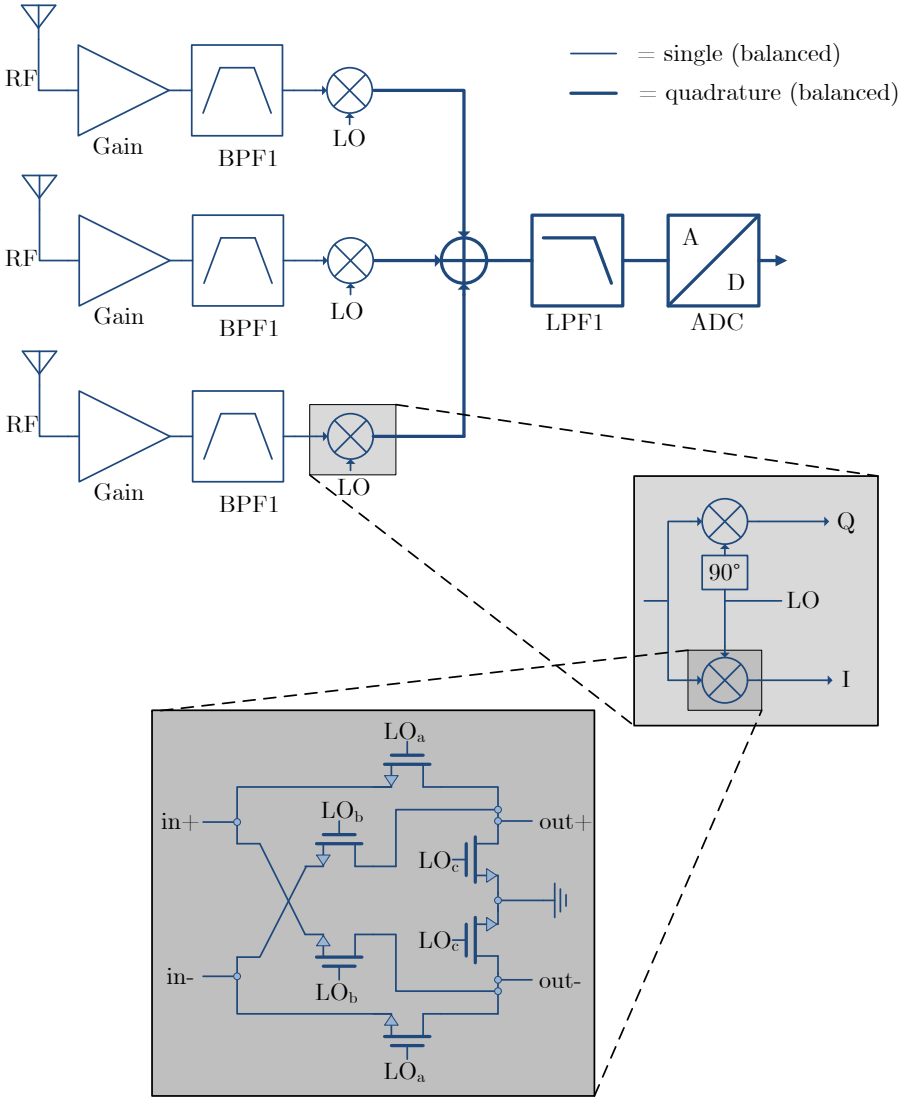


Figure 2.9: Entire beamforming system with 3 antenna's. All paths are differential.

Chapter 3

Optimal weights and nulling

3.1 Introduction to beamforming and problem description

3.1.1 Introduction to beamforming

In Figure 3.1 a linear array with 3 antenna's is shown. It is assumed that any signal arrives with the same strength and from the same direction at the three antennas, which is a reasonable assumption when the sources are relatively far away. Depending on the direction, a signal arrives earlier at some antennas then at other antennas. This fact is exploited in beamforming. To perform beamforming the signal received from the n-th antenna is shifted in phase by ϕ_2 and amplified by w_n. For now we ignore the mixing process because a mixer is transparent for phase and gain. Then all amplified and phase shifted signals are added up so they interfere with each other. They can amplify or cancel each other, depending on their frequency, the antenna spacing, w_n, ϕ_n and the direction of arrival called θ. This way the system gets a sensitivity that is a function of direction. For every value of ϕ_n and w_n the sensitivity of the system can be calculated as a function of direction and frequency of the arriving signal. In literature, this sensitivity function is called the *array factor* $F(\theta, f)$.

When we write the phase ϕ_n together with multiplication w_n as a complex weight factor $\bar{w}_n = w_n e^{j\phi_n}$, where f denotes the frequency at which we evaluate the array factor, it is straightforward to see that the array factor $F(\theta, f)$ can be written as

$$F(\theta, f) = \sum_{n=0}^{N-1} \bar{w}_n e^{j\kappa n d \sin\theta} \tag{3.1}$$

In this equation, d is the distance between 2 neighboring antenna elements (usually $\frac{\lambda}{2}$ for linear arrays). The wave number κ can be written in terms of wavelength λ ($\kappa = \frac{2\pi}{\lambda}$) or in terms of frequency f ($\kappa = \frac{2\pi f}{c}$ with c the phase velocity of the wave in air (the 'speed of light')). When f is not explicitly stated as a

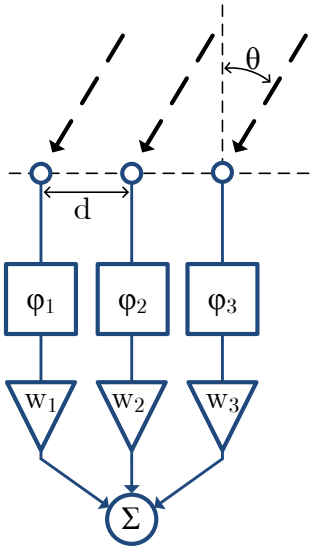


Figure 3.1: Three antennas in a linear array with distance d to each other. Every antenna signal is shifted in phase by by ϕ_n and amplified with w_n.

parameter of the array factor F, the nominal frequency of the array factor is assumed.

Figure 3.2 shows an example of an array factor of a 3-element linear array at $f = 1.1$ GHz and $d = \frac{\lambda}{2}$. The array factor shows that this system is very sensitive to signals from directions around -11 degrees, and not sensitive to signals from around 46 degrees. With the correct weights, in principle it is possible to create a 'null' in a certain direction. In a 'null' (described in terms of frequency and direction) the sensitivity is zero. The array factor to the 'back' (90 - 270 degrees) usually is not shown for a linear array because it is identical but mirrored with respect to the 'front' array factor, since for a linear array the antenna setup is symmetrically. That is:

$$F(\theta) = F(\pi - \theta) \tag{3.2}$$

Next to a linear array (line array) an often used setup is the *planar* array, which is a 2-dimensional antenna array. With this setup a beam can be steered in both horizontal and vertical directions. In addition, lots of other antenna configurations are possible.

This thesis only concentrates on the linear array.

3.1.2 Problem description

Because the rising and falling edge of the LO clock will have a finite slew rate (for CMOS 65 nm the minimum rising and falling times are in the order of 25 - 50 ps) there will be a limit on the minimum pulse width of the LO clock. That means that the weight factors will always have a minimum amplitude larger than

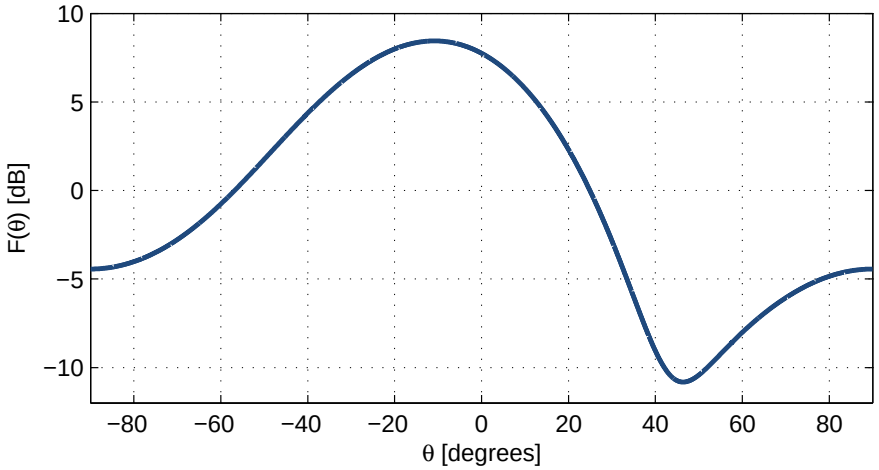


Figure 3.2: Array factor for a 3-element taper with complex weighting factors $\bar{w}_0 = 0.8, \bar{w}_1 = 1 + i, \bar{w}_2 = 0.2 + 0.4i$ and $d = \frac{\lambda}{2}$.

0, for example 0.2. A question that arises is:

- Will this effect of minimum pulse width influence the maximum Signal-to-Interferer Ratio (SIR) that can be reached with an otherwise ideal beamformer?

Because it is hard to find an answer on this question analytically we will try to find it later on by performing simulations (in Chapter 5).

When applying null-steering, interferers from particular directions can be suppressed. In this way, a maximum SIR is achieved. In practice a null is not exactly zero but suppresses only about some tens dB's. This has different reasons:

- The circuit elements that perform amplification and phase suffer from mismatch;
- The phase and amplification of every antenna signal is digitally controlled (in a finite number of quantization steps);
- Temperature fluctuations influence MOST characteristics, for example the threshold voltage (V_{th}). This gives varying system behavior;
- Every antenna array suffers from array geometry errors;
- Any interferer has a certain bandwidth over which it should be suppressed, while a null only suppresses maximally at a single frequency;
- When the position of an interferer is not known exactly (which is always the case), a certain *range of directions* should be suppressed.

- Any antenna array suffers from mutual coupling between the array elements which introduces non-ideal behaviour.

We will ignore circuit mismatch, temperature fluctuations, mutual coupling and array geometry errors, because of the following: circuit mismatch generally can be made insignificant by upscaling the circuit elements. Temperature fluctuations are assumed to have a relatively low influence on the array factor. Mutual coupling is a complicated field of research and depends largely on the shape of antennas and their spacing. Within this thesis, we will not dive into this, but it will significantly influence the nulling performance [13]. However, it is worth noting that mutual coupling can also be exploited for calibration and pattern prediction [2]. At last we assume that array geometry errors can be made insignificant by carefully manufacturing the antenna array.

This leaves us with phase and amplitude quantization steps due to limited timing resolution, position uncertainty and frequency bandwidth that influence the minimum possible null depth and maximum SIR. In most situations the position uncertainty and frequency bandwidth of the interferers cannot be changed so these are assumed to be given. Therefore, the questions that this chapter tries to answer are:

- How many bits do we need to control the timing resolution which which the LO clock can be synthesized, in order to get reasonable interferer suppression (some tens dB's)?
- When do position uncertainty and frequency bandwidth become the dominant source of error on null depth (over number of control bits)?

Because our system differs from most other beamforming systems in the fact that we have a sine-mapping between the quantized variable (pulsewidth) and the amplitude and by the fact that in our system only one parameter determines both phase and amplitude quantization (the timing resolution), in literature it's hard to find information that can help us to answer both questions. Therefore we find deduct expressions for the null depth in terms of timing resolution, position uncertainty and frequency bandwidth, which will be done in the next sections.

3.2 Nulling depth

3.2.1 Quantization of amplitude and phase

We call the moment at which the rising edge of the LO clock crosses $0.5V_{dd}$ the *rising edge*, and the moment at which the falling edge of the LO clock crosses $0.5V_{dd}$ the *falling edge*.

We define the phase shift as the middle between the rising edge and falling edge of the LO clock pulse, and we define 1 period to have length 2π (this simplifies our calculations; see Figure 3.3). The pulse width is the difference between the rising edge and the falling edge.

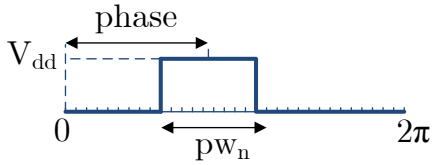


Figure 3.3: Example of one LO clock pulse. In this example, LO clock period is divided into 32 steps (5 bits quantization). The phase is $\frac{13.5}{32} \cdot 2\pi \approx 2.65$ rad and the gain is $\sin(0.5 \cdot \frac{9}{32} \cdot 2\pi) \approx 0.773$.

Between the pulse width pw_n (in rad, where 2π rad means 1 full period) and the equivalent amplitude gain w_n is the sine mapping[1]:

$$w_n = \sin(0.5 \cdot pw_n) \tag{3.3}$$

So for maximum amplitude of 1, the pulse width pw_n has to be π, which is half of the total LO clock period.

Because both phase and amplitude are made using discrete steps in time, the phase quantization errors and amplitude errors always exist together (in contrast with a 'classic' beamforming system that uses separate blocks for amplification and phase shifting). Only one parameter determines the phase and amplitude quantization error: the number of control bits n_{bits}. For 5 bits phase control, the clock period is divided into 32 equal intervals. The desired moments of the rising and falling edge of the LO clock pulse are rounded to their closest realizable value[2] (see Figure 3.3), resulting in a *quantization error* for the rising edge of the LO clock pulse called e_r and for the falling edge called e_f. Both are assumed to be uniformly divided on the interval $[-\frac{\pi}{2^{n_{bits}}}, \frac{\pi}{2^{n_{bits}}}]$.

It can be shown that phase quantization error and amplitude quantization error are statistically independent, in the sense that when the phase is rounded upwards, the amplitude still has an equal chance of being rounded upwards or downwards. Therefore we can treat them separately in the next paragraphs, and add up their effects on the null depth later on.

Note that for large amplitudes (close to 1) the amplitude quantization error goes to zero (due to the sine mapping). This can be seen in Figure 3.5.

In the next sections we will deduce formula's that indicate the nulling depth as a function of phase quantization, amplitude quantization and angular uncertainty and bandwidth of the interferer. In the next chapter (5) these formulas will be compared with simulations.

[1]The subscript n will later on be used to distinguish the different antenna elements from each other.

[2]There is another way of rounding: one could also choose to round the *pulse width* and the moment of the rising edge. That way of rounding causes smaller amplitude errors but larger phase errors, which, overall, would give *worse* performance. Therefore we choose to round the moment of the rising- and falling edge.

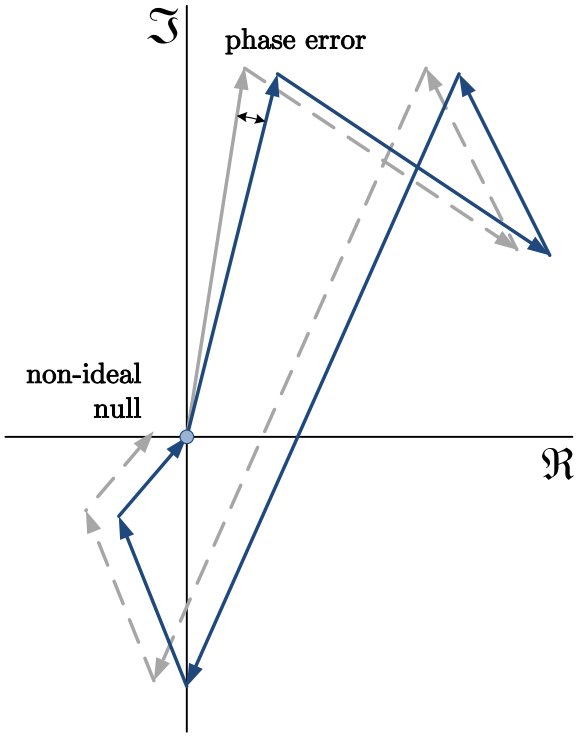


Figure 3.4: A phase error causes a nonzero null

3.2.2 Nulling depth as a function of phase quantization

Suppose that the digital phase quantization causes the biggest effect on non-zero nulls and ignore all other non-ideal effects that deteriorate nulling performance. Then, what is quantitatively the relationship between the number of phase quantization bits and the null depth? We will answer this question in this section.

The array factor (equation 3.1) can be expressed as a sum of complex numbers. Into the direction and at the frequency of a null, this sum ideally equals zero. This can be seen in Figure 3.4 where the cascade of all arrows (phasors in the complex plane) points to zero. Assume that for certain θ, without quantization we have a perfect null:

$$F(\theta) = \sum_{n=0}^{N-1} \bar{w}_n e^{j\kappa n d \sin\theta} = 0 \tag{3.4}$$

When we write $\bar{w}_n$ as $w_n e^{jb_n}$ we get

$$F(\theta) = \sum_{n=0}^{N-1} w_n e^{j(b_n + \kappa n d \sin\theta)} \tag{3.5}$$

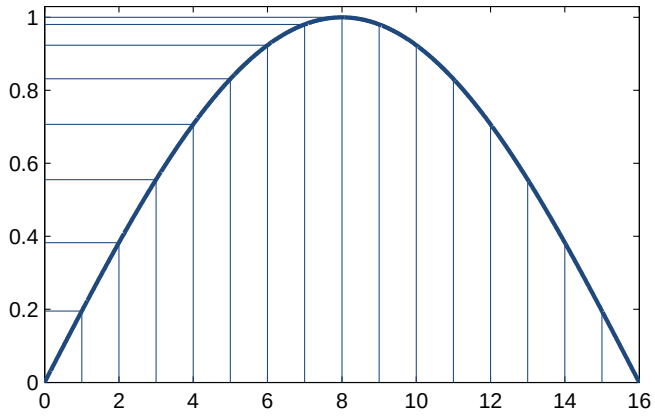


Figure 3.5: The sine mapping decreases amplitude quantization steps for amplitudes close to 1

When we apply Euler's formula we can separate the real and imaginary parts:

$$F(\theta) = \sum_{n=0}^{N-1} w_n \cos(b_n + \kappa n d \sin\theta) + j \sum_{n=0}^{N-1} w_n \sin(b_n + \kappa n d \sin\theta) \tag{3.6}$$

For the case of phase quantization, we we will show that for many antennas (large n) both the real and imaginary part of $F(\theta)$ can be approximated by a Gaussian distribution with a mean 0 and a variance σ^2. Therefore, $|F(\theta)|$ can be approximated by a Rayleigh[3] distribution with parameter σ. The expected value of this distribution will give an indication of the depth of a null.

Next we will derive an estimate for σ as a function of the number of quantization bits n_{bits}. Let's start with the real part of $F(\theta)$ and add a quantization error b_{nq} to the phase of the n-th weight factor b_n:

$$\Re(F(\theta)) = \sum_{n=0}^{N-1} w_n \cos(b_n + b_{nq} + \kappa n d \sin\theta) \tag{3.7}$$

This real part can be approximated by a 1st order Taylor Series approximation $\left(\cos(x+dx) \approx \cos(x) + \frac{d\cos(x)}{dx} dx\right)$ because b_{nq} is relatively small:

$$\begin{aligned} \Re(F(\theta)) &\approx \sum_{n=0}^{N-1} (w_n \cos(b_n + \kappa n d \sin\theta) - w_n \sin(b_n + \kappa n d \sin\theta) b_{nq}) \\ &\approx \sum_{n=0}^{N-1} w_n \cos(b_n + \kappa n d \sin\theta) - \sum_{n=0}^{N-1} w_n \sin(b_n + \kappa n d \sin\theta) b_{nq} \end{aligned} \tag{3.8}$$

[3]When two independent random variables have a Gaussian distribution with zero mean, the modulus of their sum is Rayleigh-distributed.

The first part can be recognized as the real part of *the array factor without quantization*, which equals 0. Therefore:

$$\begin{aligned} \Re(F(\theta)) &\approx \sum_{n=0}^{N-1} -w_n \sin(b_n + \kappa n d \sin\theta) b_{nq} \\ &\approx \sum_{n=0}^{N-1} -w_n \cdot \alpha \cdot b_{nq} \end{aligned} \tag{3.9}$$

where $\alpha = \sin(b_n + \kappa n d \sin\theta)$.

To find $Var(-w_n \cdot \alpha \cdot b_{nq})$, we first find the variances of w_n, α and b_{nq}:

The variance of w_n

For now, we leave $Var(w_n)$ and $E(w_n)$ as parameters.

The variance of α

When we assume that b_n (the phase of the nth weight factor) has an uniform distribution on $[-\pi, \pi]$, which is likely because for nulling b_n depends on the positions of the nulls and can be calculated using matrix inversion (see paragraph 5.1.1) but have no direct relation with each other. We also assume $\kappa n d \sin\theta$ to be independent of b_n. With these assumptions, $\alpha = \sin(b_n + \kappa n d \sin\theta)$ has a probability density function that is the derivative of arcsin:

$$f_\alpha(\alpha) = \begin{cases} \frac{1}{\pi\sqrt{1-\alpha^2}} & |\alpha| \leq w_n \\ 0 & \text{otherwise} \end{cases} \tag{3.10}$$

with

$$E(\alpha) = 0 \tag{3.11}$$

and

$$Var(\alpha) = 0.5 \tag{3.12}$$

The variance of b_{nq}

The *phase* of the LO clock pulse is the mean between the rising edge and falling edge of the LO clock pulse, and so is the phase quantization error b_{nq}:

$$b_{nq} = \frac{e_r + e_f}{2} \tag{3.13}$$

We assume that the quantization error of the rising and falling edge both are distributed uniformly on the interval $[-\frac{\pi}{2^{n_{bits}}}, \frac{\pi}{2^{n_{bits}}}]$ and are independent. There-

fore,

$$\begin{aligned} Var(b_{nq}) &= Var\left(\frac{e_r + e_f}{2}\right) \\ &= \frac{Var(e_r) + Var(e_f)}{4} \\ &= \frac{2}{4} \cdot \frac{(\frac{2\pi}{2^{n_{bits}}})^2}{12} \\ &= \frac{\pi^2}{6 \cdot 2^{2n_{bits}}}. \end{aligned} \tag{3.14}$$

And off course,

$$E\{b_{nq}\} = 0 \tag{3.15}$$

The expected null depth as a function of phase quantization

Now we can find an expression for $Var(-w_n \cdot \alpha \cdot b_{nq})$ in terms of $Var(w_n)$, $E(w_n)$, $Var(\alpha)$ etc. using the result of Appendix A for $Var(XYZ)$ where we take $X = b_{nq}$, $Y = \alpha$, $Z = w_n$, after simplifying:

$$Var(-w_n \cdot \alpha \cdot b_{nq}) = \frac{\pi^2}{2^{2n_{bits}}} \left(\frac{Var(w_n) + E(w_n)^2}{12}\right) \tag{3.16}$$

and because $E(XYZ) = E(X)E(Y)E(Z)$, we have

$$E(-w_n \cdot \alpha \cdot b_{nq}) = 0 \tag{3.17}$$

By the central limit theorem, a sum of M random variables, all with the same (arbitrary) probability density function with variance σ^2, gets a Gaussian distribution with variance $M\sigma^2$. In our case (formula 3.16), this means that for large N, the real part of the array factor $F(\theta)$ at a null becomes approximately Gaussian with variance σ_p^2 where

$$\begin{aligned} Var(\sum_{n=0}^{N-1} w_n \cdot \alpha \cdot b_{nq}) = \sigma_p^2 &= N \cdot Var(-w_n \cdot \alpha \cdot b_{nq}) \\ &= \frac{N\pi^2}{2^{2n_{bits}}} \left(\frac{Var(w_n) + E(w_n)^2}{12}\right) \end{aligned} \tag{3.18}$$

It's expectation is 0.

The same derivation can be done for the imaginary part of $F(\theta)$ and will give exactly the same result. Therefore we can conclude that the modulus of the array factor $F(\theta)$ in a null (the null 'depth') has the Rayleigh-distribution with *parameter* (not standard deviation) σ_p.

The expected value of a Rayleigh distribution with parameter σ is $\sigma\sqrt{\frac{\pi}{2}}$ and it's variance is $\frac{4-\pi}{2}\sigma^2$. This gives us a measure for the expected null 'depth' as

a function of the number of phase quantization bits n_{bits}:

$$\begin{aligned} E(|F(\theta)|) &= \sigma_p \sqrt{\frac{\pi}{2}} \\ &= \frac{\pi}{2^{n_{bits}}} \sqrt{\frac{N[Var(w_n) + E(w_n)^2]}{12}} \cdot \sqrt{\frac{\pi}{2}} \\ &= \frac{\pi}{2^{n_{bits}}} \sqrt{\frac{\pi N[Var(w_n) + E(w_n)^2]}{24}} \end{aligned} \tag{3.19}$$

When assumed that the largest element w_n from the array has a modulus that is normalized to 1, and when we assume that the other $N-1$ elements have a modulus that is uniformly distributed between 0 and 1, with some calculations it can be shown that

$$Var(w_n) = \frac{N^3 + 2N^2 - 6N + 3}{12N^3} \tag{3.20}$$

and that

$$E(w_n) = \frac{N+1}{2N} \tag{3.21}$$

Using this distribution for w_n, equation 3.19 reduces to:

$$E(|F(\theta)|) = \frac{\pi}{12 \cdot 2^{n_{bits}}} \sqrt{\pi \left(\frac{4N^3 + 8N^2 - 3N + 3}{2N^2} \right)} \tag{3.22}$$

In dB (ignoring the small term $-3N + 3$):

$$E(|F(\theta)|)_{dB} \approx 10 \log(2N + 4) - 6.02 \cdot n_{bits} - 6.67 \tag{3.23}$$

So for 9 antenna elements and 5 bits phase quantization, we can expect a null depth *due to phase quantization* of 0.068 which is about -23.3 dB.

3.2.3 Nulling depth as a function of amplitude quantization

To find an expression for the nulling depth as a function of amplitude quantization we follow the same approach as we did for the phase quantization: we find an expression for the variance of the real part and imaginary part of the array factor, and show that these parts are Gaussian. Then the modulus of the array factor is Rayleigh distributed and we can calculate it's expectation, which gives us the average depth of a null under influence of amplitude quantization.

To start, we take equation 3.7, remove the phase quantization component b_{nq} and add an amplitude quantization component w_{nq}:

$$\begin{aligned} \Re(F(\theta)) &= \sum_{n=0}^{N-1} (w_n + w_{nq}) \cos(b_n + \kappa n d \sin\theta) \\ &= \sum_{n=0}^{N-1} w_n \cos(b_n + \kappa n d \sin\theta) + \sum_{n=0}^{N-1} w_{nq} \cos(b_n + \kappa n d \sin\theta) \end{aligned} \tag{3.24}$$

Just as for phase quantization, the first part of this formula can be recognized as 0 (because it is the ideal array factor, without quantization). This leaves us:

$$\begin{aligned} \Re(F(\theta)) &= \sum_{n=0}^{N-1} w_{nq} \cos(b_n + \kappa n d \sin\theta) \\ &= \sum_{n=0}^{N-1} w_{nq} \cdot \beta \end{aligned} \tag{3.25}$$

where $\beta = \cos(b_n + \kappa n d \sin\theta)$.

The variance of β

The distribution of β is the same as the one of α (see section 3.2.2), assumed that b_n is uniformly distributed on $[0, 2\pi]$.

The variance of w_{nq}

The derivative of the sine mapping (equation 3.3) to the pulse width pw_n is:

$$\frac{dw_n}{dpw_n} = 0.5\cos(0.5pw_n) \tag{3.26}$$

For a small pulse width quantization error pw_{nq} (say, 2 bits pulse width quantization or more) we can use this derivative to get the amplitude quantization error w_{nq} corresponding to the pulse width quantization error:

$$w_{nq} \approx 0.5\cos(0.5pw_n) \cdot pw_{nq} \tag{3.27}$$

Substituting the inverse sine mapping ($pw_n = 2\arcsin w_n$) we get:

$$\begin{aligned} w_{nq} &\approx 0.5\cos(\arcsin w_n) pw_{nq} \\ &\approx 0.5 pw_{nq}\sqrt{1 - w_n^2} \end{aligned} \tag{3.28}$$

This result confirms our previous statement that for large w_n (close to 1) the amplitude quantization error goes to 0.

In order to get the variance of the amplitude quantization error w_{nq} (which is our goal in this paragraph) we use equation A.3 from Appendix A which gives the variance of a product of independent stochastic variables $Var(XY)$ in terms of the mean and variance of X and Y. We substitute $X = pw_{nq}$ and $Y = 0.5\sqrt{1 - w_n^2}$. To solve this equation, first we can calculate $E(Y)$, for which we need the probability density function of w_n. It's hard to say anything general over this distribution, because it depends on the application. For a rough approximation, we first assume that w_n is uniformly distributed on the interval

$[0, 1]$. In this case we have:

$$\begin{aligned} E(Y) = E\left(0.5\sqrt{1-w_n^2}\right) &= \int_0^1 0.5\sqrt{1-w_n^2}\, dw_n \\ &= \frac{\pi}{8} \end{aligned} \tag{3.29}$$

To calculate $Var(Y) = Var(0.5\sqrt{1-w_n^2})$, we need the probability density function of Y, $f(Y)$. To find this, we use the derivative of the cumulative distribution function of Y $(F(Y))$:

$$F(Y) = P(Y \leq w_n) = \begin{cases} 0 & w_n \leq 0 \\ 1 - \sqrt{1-4w_n^2} & 0 < w_n \leq 0.5 \\ 1 & \text{otherwise} \end{cases} \tag{3.30}$$

so

$$\begin{aligned} f(Y) &= \frac{dF(Y)}{dw_n} \\ &= \begin{cases} \frac{4Y}{\sqrt{1-4w_n^2}} & 0 \leq w_n \leq 0.5 \\ 0 & \text{otherwise} \end{cases} \end{aligned} \tag{3.31}$$

Now we can calculate $Var(Y)$:

$$\begin{aligned} Var(Y) &= \int (Y - E(Y))^2 f(Y) dy \\ &= \int_0^{0.5} \left(Y - \frac{\pi}{8}\right)^2 \cdot \frac{4Y}{\sqrt{1-4w_n^2}} dY \\ &= \frac{1}{6} - \frac{\pi^2}{64} \end{aligned} \tag{3.32}$$

Furthermore we know $E(X) = E(pw_{nq}) = 0$ and $Var(X) = Var(pw_{nq})$. Next we calculate $Var(XY)$:

$$\begin{aligned} Var(XY) &= Var(w_{nq}) \\ &= Var(X)Var(Y) + Var(X)E\{Y\}^2 \\ &\quad + Var(Y)E\{X\}^2 \\ &= Var(pw_{nq})\left(\frac{1}{6} - \frac{\pi^2}{64}\right) + Var(pw_{nq})\left(\frac{\pi}{8}\right)^2 \\ &= \frac{Var(pw_{nq})}{6} \end{aligned} \tag{3.33}$$

The variance of pw_{nq}

The LO pulse width is the difference between the rising edge of the LO clock pulse and the falling edge, and so is the pulse width quantization error pw_{nq}:

$$pw_{nq} = e_r - e_f \tag{3.34}$$

Again, when we assume that the quantization error of the rising edge and falling edge are distributed uniformly on the interval $[-\frac{\pi}{2^{n_{bits}}}, \frac{\pi}{2^{n_{bits}}}]$ we get:

$$\begin{aligned} Var(pw_{nq}) &= Var(e_r) + Var(e_f) \\ &= 2Var(e_r) \\ &= 2\frac{\left(\frac{2\pi}{2^{n_{bits}}}\right)^2}{12} \\ &= \frac{2}{3} \cdot \frac{\pi^2}{2^{2n_{bits}}} \end{aligned} \tag{3.35}$$

The expected null depth as a function of amplitude quantization

Substituting the result of equation 3.35 into in equation 3.33 yields:

$$Var(w_{nq}) = \frac{1}{9} \cdot \frac{\pi^2}{2^{2n_{bits}}} \tag{3.36}$$

Using Appendix A again, we know that

$$\begin{aligned} Var(-w_{nq} \cdot \beta) &= Var(-w_{nq})Var(\beta) + Var(-w_{nq})E(\beta)^2 \\ &\quad + Var(\beta)E(-w_{nq})^2 \\ &= \frac{1}{18} \cdot \frac{\pi^2}{2^{2n_{bits}}} \end{aligned} \tag{3.37}$$

The sum of many of these independent variables $w_{nq} \cdot \beta$ again is Gaussian, with variance σ_a^2 where

$$Var\left(\sum_{n=0}^{N-1} w_{nq} \cdot \beta\right) = \sigma_a^2 = \frac{N}{18} \cdot \frac{\pi^2}{2^{2n_{bits}}} \tag{3.38}$$

It's expectation is 0. Now we make one observation: we assumed that all all weight factors are scaled such that the largest weight factor equals 1. But this largest weight factor doesn't suffer from pulse width quantization because it's in the top of the sine mapping. Therefore, it doesn't contribute to the Gaussian shape and we have to use $N-1$ in stead of N in the expression of σ_a^2 [4]:

$$\sigma_a^2 = \frac{N-1}{18} \cdot \frac{\pi^2}{2^{2n_{bits}}} \tag{3.39}$$

[4] In fact, in many cases, 2 elements are equal to 1 because the moduli of the weight factors are often *symmetrical* (for example [0.7568 .9404 1.0000 1.0000 0.9404 0.7568]).

When we take the square root we get:

$$\sigma_a = \frac{\sqrt{N-1}}{3\sqrt{2}} \cdot \frac{\pi}{2^{n_{bits}}} \tag{3.40}$$

Again, the imaginary part gives the same result. Therefore, expectation of the null depth is the expectation of a Rayleigh distribtion with parameter σ_a:

$$\begin{aligned} E(|F(\theta)|) &= \sigma_a \sqrt{\frac{\pi}{2}} \\ &= \frac{\sqrt{N-1}}{3\sqrt{2}} \cdot \frac{\pi}{2^{n_{bits}}} \cdot \sqrt{\frac{\pi}{2}} \\ &= \frac{\sqrt{N-1}}{6} \cdot \frac{\pi\sqrt{\pi}}{2^{n_{bits}}} \end{aligned} \tag{3.41}$$

3.2.4 Nulling depth as a function of position uncertainty, bandwidth and number of nulls

Because the position of an interferer is not known exactly, a null should suppress the interferer over a certain *range of directions*, which we call the *direction uncertainty*. And because an interferer usually has a certain bandwidth, a null should also suppress over this whole bandwidth. When we talk about null depth, we mean the *largest, worst-case array factor over the mentioned bandwidth and direction uncertainty*. Adding more nulls together can give better suppression, or the same suppression but for a larger direction uncertainty or bandwidth. An example of the use of more nulls together can be seen in Figure 3.6.

In this section, an analytical expression is derived for the null suppression as a function of frequency bandwidth, direction uncertainty and the number of nulls. First we try to find an analytical expression for the null suppression for a single null. Next, we try to find an expression for the null depth using two nulls together. Finally, we try to deduce a formula for an arbitrary number of nulls. In this whole section, we assume that weight factors (amplitude and phase) have *no* quantization errors.

The relationship between frequency and direction

First we recall the array factor (equation 3.1) that gives the amplification of the antenna array for a signal from direction θ on frequency f:

$$\begin{aligned} F(\theta, f) &= \sum_{n=0}^{N-1} \bar{w}_n e^{j\kappa n d \sin\theta} \\ &= \sum_{n=0}^{N-1} \bar{w}_n e^{\left(\frac{j2\pi f n d}{c} \sin\theta\right)} \end{aligned} \tag{3.42}$$

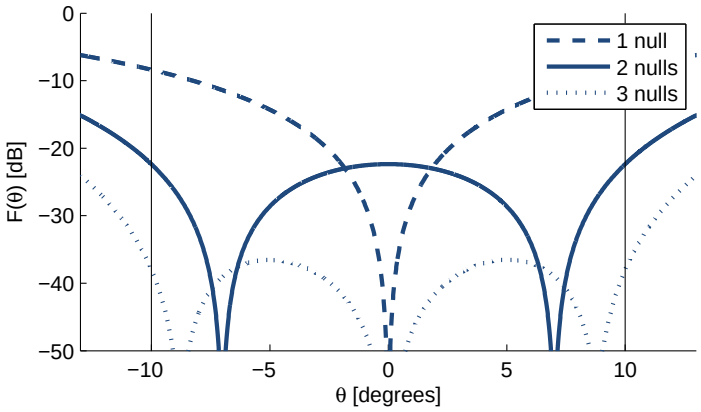


Figure 3.6: More nulls can combine to one deeper or broader null. In this example, 1 null suppresses (worst-case) only 8 dB from -10 degrees to 10 degrees. 2 nulls suppress (worst-case) 23 dB and 3 nulls together suppress (worst-case) 36 dB.

where $\kappa = \frac{2\pi f}{c}$ and c is the speed of light in air [ms]. θ is the direction [radians], d is the antenna spacing [meters].

A change in $F(\theta, f)$ due to a small change in frequency f can be compensated by a change in angle θ, without changing the array factor. This phenomenon is often referred to as 'beam squint'. In order to find this relation mathematically, lets write the product $\kappa \sin\theta$ as G:

$$G(f, \theta) = \frac{2\pi f \sin\theta}{c} \tag{3.43}$$

so

$$\frac{dG}{df} = \frac{2\pi \sin\theta}{c} \tag{3.44}$$

and

$$\frac{dG}{d\theta} = \frac{2\pi f \cos\theta}{c} \tag{3.45}$$

Therefore,

$$\frac{d\theta}{df} = \frac{\sin\theta}{f\cos\theta} = \frac{\tan\theta}{f} \tag{3.46}$$

so

$$\Delta\theta \approx \frac{\tan\theta}{f}\Delta f; \tag{3.47}$$

We will use this relation later on. It is interesting to note that at $\theta = \pm\frac{\pi}{2}$ rad, equation 3.46 goes to $\pm\infty$, which means that to these directions the array factor is insensitive for small changes in θ.

Null depth for 1 null

With N antenna elements we can make $N-1$ independent nulls (which becomes clear when writing the expression of the array factor as a N-th order polynomial, which has $N-1$ zeros). For antenna spacings larger than $\frac{1}{2}\lambda$ there can be more than $N-1$ nulls, but only $N-1$ can be independently placed.

We can draw the real and imaginary part of the array factor as a function of angle θ. On a small interval around a null, the real part and imaginary part can be approximated by straight lines that cross the horizontal axis where the array factor is 0 (at the null). Because in figures we mostly plot the modulus of the array factor, on linear scale we see a null as a 'v'-shape. On logarithmic scale this null goes to $-\infty$. On a small deviation $\Delta\theta$ (also in radians) from the direction of the zero, we can approximate the array factor by

$$F(\theta, f) \approx \frac{dF(\theta, f)}{d\theta}\Delta\theta \tag{3.48}$$

From equation 3.42 we know that the derivative of the array factor to θ is:

$$\frac{dF(\theta, f)}{d\theta} = \sum_{n=0}^{N-1} j\bar{w}_n \frac{2\pi f d}{c} n\cos(\theta) e^{j\kappa n d \sin\theta} \tag{3.49}$$

For N=2 this reduces to

$$\frac{dF(\theta, f)}{d\theta} = j\bar{w}_1 \frac{2\pi f d}{c}\cos(\theta) e^{j\kappa d \sin\theta} \tag{3.50}$$

Filling in this in equation 3.48 gives us an approximation of the array factor at a *small distance* $\Delta\theta$ from the null:

$$F(\Delta\theta) \approx j\bar{w}_1 \frac{2\pi f d}{c}\cos(\theta) e^{j\kappa d \sin\theta}\Delta\theta \tag{3.51}$$

The suppression[5] at this point is equal to the modulus of $F(\Delta\theta)$.

$$|F(\Delta\theta)| \approx w_1 \frac{2\pi f d}{c}|\cos(\theta)|\Delta\theta \tag{3.52}$$

Here w_1 is $|\bar{w}_1|$. When normalizing w_1=w_0 to 1, and when assuming half λ antenna spacing, we get:

$$|F(\Delta\theta)| \approx \pi|\cos(\theta)|\Delta\theta \tag{3.53}$$

This expression gives the worst-case null suppression over the range $\Delta\theta$. Of course, in this situation with 1 null, only at the edges of this interval the suppression is equal to equation 3.53 and everywhere in between it is better, but in order to make calculations not too complicated we stick to making calculations with the worst-case null suppression.

[5]When we talk about the *suppression*, we mean the modulus of the array factor $|F(\theta, f)|$. So when an array factor equals 0.2 for a certain θ and f, it has a suppression of 0.2.

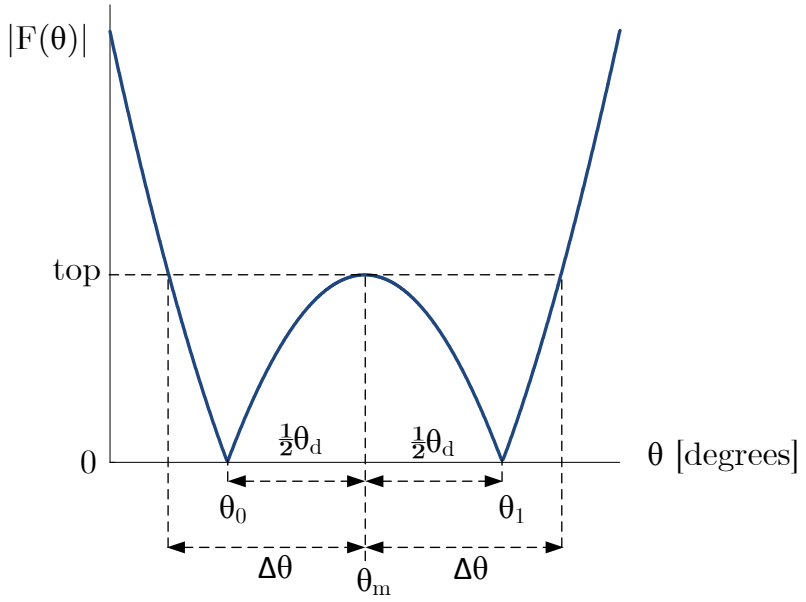


Figure 3.7: Definitions for the array factor with 2 closely spaced nulls

Null depth for 2 nulls

We will assume that for closely spaced nulls, the real and imaginary part of the array factor *near these nulls* can be written as a 2nd order polynomial in θ. Figure 3.7 shows the definitions that will be used. We define the null-depth as the top of the polynomial (see Figure 3.7) which, again, is a worst-case situation. Our aim is to find an expression of this null depth, again in terms of frequency f, θ_m and $\Delta\theta$ where θ_m is in the center between the two nulls. The place where these two nulls have to be placed, is determined by the angular uncertainty $\Delta\theta$, such that $F(\theta_m - \Delta\theta) = F(\theta_m + \Delta\theta) = F(\theta_m) = \text{top}$. We solve this problem as follows:

1. We find expressions for $\bar{w}_0$, $\bar{w}_1$ and $\bar{w}_2$ in terms of the null positions θ_0 and θ_1 (see Figure 3.7).

2. We substitute this expressions in the array factor so we get the array factor in terms of θ_0 and θ_1.

3. We want to evaluate this array factor at the 'top' (at θ_m) so we substitute $\theta = \theta_m$. Furthermore, we substitute $\theta_0 = \theta_m - 0.5\theta_d$ and $\theta_1 = \theta_m + 0.5\theta_d$ so we express 'top' in terms of θ_m and θ_d and we simplify the result.

4. We find an expression for direction uncertainty $\Delta\theta$ in terms of null spacing θ_d (review Figure 3.7 for their definitions) and inverse it (so we write θ_d in terms of $\Delta\theta$).

5. We substitute this expression for θ_d in the result of (3), which gives us the depth of the array factor for an angular uncertainly $\Delta\theta$.

Expressions for $\bar{w}_0$, $\bar{w}_1$ and $\bar{w}_2$ in terms of θ_0 and θ_1 Let's recall the array factor for 3 antenna elements at a fixed frequency f:

$$F(\theta) = \bar{w}_0 + \bar{w}_1 e^{j\kappa nd\sin\theta} + \bar{w}_2 e^{j\kappa nd\sin\theta} \tag{3.54}$$

We want $F(\theta_0) = 0$ and $F(\theta_1) = 0$, so we got:

$$\begin{aligned} 0 &= \bar{w}_0 + \bar{w}_1 e^{j\kappa nd\sin\theta_0} + \bar{w}_2 e^{j\kappa nd\sin\theta_0} && (3.55)\\ 0 &= \bar{w}_0 + \bar{w}_1 e^{j\kappa nd\sin\theta_1} + \bar{w}_2 e^{j\kappa nd\sin\theta_1} && (3.56)\end{aligned}$$

When we take (arbitrarily) $\bar{w}_0 = 1$ we have two (complex) linear equations with two unknown (complex) variables ($\bar{w}_1$ and $\bar{w}_2$). When we solve these we get:

$$\begin{aligned} \bar{w}_1 &= \frac{e^{2j\kappa d\sin\theta_0} - e^{2j\kappa d\sin\theta_1}}{e^{j\kappa d(2\sin\theta_1+\sin\theta_0)} - e^{j\kappa d(\sin\theta_1+2\sin\theta_0)}} && (3.57)\\ \bar{w}_2 &= \frac{e^{j\kappa d\sin\theta_0} - e^{j\kappa d\sin\theta_1}}{e^{j\kappa d(\sin\theta_1+2\sin\theta_0)} - e^{j\kappa d(2\sin\theta_1+\sin\theta_0)}} && (3.58)\end{aligned}$$

Substituting these expressions for $\bar{w}_0$, $\bar{w}_1$ and $\bar{w}_2$ in the array factor (equation 3.54) gives:

$$F(\theta) = 1 + \frac{-e^{j\kappa d(\sin\theta+2\sin\theta_0)} + e^{j\kappa d(\sin\theta+2\sin\theta_1)} - e^{j\kappa d(2\sin\theta+\sin\theta_1)} + e^{j\kappa d(2\sin\theta_1+\sin\theta_0)}}{e^{j\kappa d(\sin\theta_1+2\sin\theta_0)} - e^{j\kappa d(2\sin\theta_1+\sin\theta_0)}} \tag{3.59}$$

Substituting $\theta = \theta_m$, $\theta_0 = \theta_m - 0.5\theta_d$ and $\theta_1 = \theta_m + 0.5\theta_d$ gives:

$$\begin{aligned} F(\theta_m) = 1 &+ \frac{-e^{j\kappa d(\sin\theta_m+2\sin(\theta_m-0.5\theta_d))} + e^{j\kappa d(\sin\theta_m+2\sin(\theta_m+0.5\theta_d))}}{e^{j\kappa d(\sin(\theta_m+0.5\theta_d)+2\sin(\theta_m-0.5\theta_d))} - e^{j\kappa d(2\sin(\theta_m+0.5\theta_d)+\sin(\theta_m-0.5\theta_d))}} \\ &+ \frac{-e^{j\kappa d(2\sin\theta_m+\sin(\theta_m+0.5\theta_d))} + e^{j\kappa d(2\sin(\theta_m+0.5\theta_d)+\sin(\theta_m-0.5\theta_d))}}{e^{j\kappa d(\sin(\theta_m+0.5\theta_d)+2\sin(\theta_m-0.5\theta_d))} - e^{j\kappa d(2\sin(\theta_m+0.5\theta_d)+\sin(\theta_m-0.5\theta_d))}} \end{aligned} \tag{3.60}$$

Using $\sin(\theta_m \pm 0.5\theta_d) = \alpha \pm \beta$ with $\alpha = \sin\theta_m \cos 0.5\theta_d$ and $\beta = \cos\theta_m \sin 0.5\theta_d$ we get:

$$F(\theta_m) = 1 + \frac{-e^{j\kappa d(\sin\theta_m+2\alpha-2\beta)} + e^{j\kappa d(\sin\theta_m+2\alpha+2\beta)} - e^{j\kappa d(2\sin\theta_m+\alpha+\beta)} + e^{j\kappa d(2\sin\theta_m+\alpha-\beta)}}{e^{j\kappa d(3\alpha-\beta)} - e^{j\kappa d(3\alpha+\beta)}} \tag{3.61}$$

Next we use the rules $e^{-j\phi} - e^{j\phi} = -2j\sin\phi$ and $e^{j\phi} - e^{-j\phi} = 2j\sin\phi$. We substitute the expressions for α and β. Then we apply the rule $\cos(0.5\theta_d) \approx 1$ (assuming θ_d is small). Simplifying yields:

$$F(\theta_m) \approx -2 + 2\cos(\kappa d \cos\theta_m \sin(0.5\theta_d)) \tag{3.62}$$

For small θ_d, $\sin(0.5\theta_d) \approx 0.5\theta_d$, so we get:

$$F(\theta_m) \approx -2 + 2\cos(0.5\kappa d \cos(\theta_m)\theta_d) \tag{3.63}$$

Observe that θ_d is small and that $0.5\kappa d\cos(\theta_m)\theta_d$ is also small ($\kappa d = \pi$ for 0.5λ antenna spacing and cos(...) will never be larger than 1). Using $\cos(x) \approx 1 - \frac{x^2}{2}$ for small x, we get:

$$F(\theta_m) \approx (0.5\kappa d \cos(\theta_m)\theta_d)^2 \tag{3.64}$$

which gives the top of the array factor in terms of θ_m and θ_d. We would like to express this equation in terms of $\Delta\theta$ (refer again to Figure 3.7). Because we approximate the absolute of this part of the array factor by the absolute of a 2nd order polynomial in θ, we can see that $\Delta\theta = \sqrt{2}\frac{1}{2}\theta_d$[6]. Therefore, we see that the null depth with 2 nulls is:

$$\begin{aligned} |F(\theta_m)| &\approx \left(0.5\kappa d|\cos(\theta_m)\Delta\theta\sqrt{2}|\right)^2 \\ &= 0.5\left(\frac{2\pi f d}{c}|\cos\theta_m|\Delta\theta\right)^2 \end{aligned} \tag{3.65}$$

Figure 3.8 gives an example of the array factor for an interferer at 35 degrees with an angular uncertainty of 5 degrees ($\Delta\theta = 5 \cdot \frac{\pi}{180}$ radians). It's null depth is about -32 dB (≈ 0.025).

Null depth for N nulls

From the previous paragraph, we know that for 1 null, the best possible null depth will be

$$|F(\Delta\theta)|_{1 \text{ null}} \approx \frac{2\pi f d}{c}|\cos(\theta)|\Delta\theta \tag{3.66}$$

and for 2 nulls it will be

$$|F(\Delta\theta)|_{2 \text{ nulls}} \approx 0.5\left(\frac{2\pi f d}{c}|\cos\theta_m|\Delta\theta\right)^2 \tag{3.67}$$

As said, the latter equation assumes that the first weight factor has length 1.

[6] this also follows from writing $|F(\theta)|$ as a 2nd order polynomial $|a\theta^2 + b\theta + c|$, calculating the coefficients a, b and c with the values for the top and the zero crossings, and solving $a\theta^2 + b\theta + c = -top$

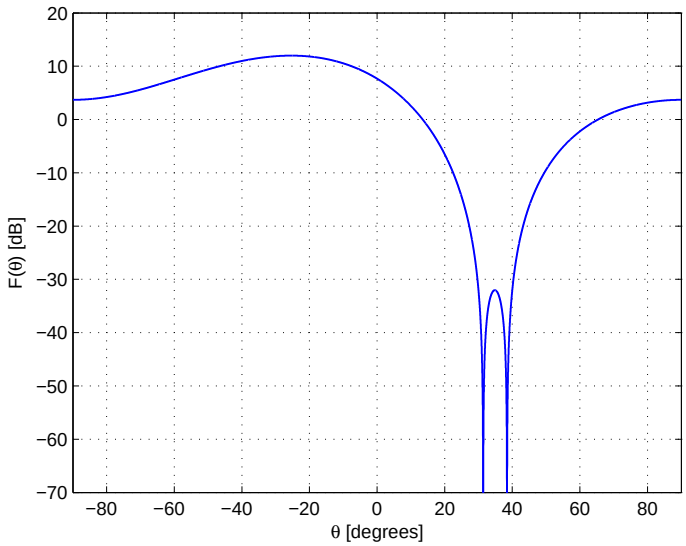


Figure 3.8: Array factor with 2 nulls at the most optimum places for minimum null depth into the direction of 35 degrees for an angular uncertainty of 10 degrees. $f = 1.1$ GHz and d=$\frac{1}{2}\lambda$. The weight factors are scaled such that the modulus of the first weight factor equals 1. In this example the weight factors are [0.222 + 0.975i, 1.975 - 0.000i, 0.222 - 0.975i].

Now, what will be the best possible null depth for an *arbitrary* number of nulls? Let's call the null depth for a number of nulls working together nd_b. Looking to equation 3.52 and 3.67, and assuming that *for every extra added null, the null depth will decrease with a fixed number of dBs*, nd_b should follow the relation $nd_b = c \cdot d^{N_{nulls}}$ with c and d constants. Later on, simulations will show that this assumption is correct. Using both deduced equations for $N_{nulls} = 1$ and $N_{nulls} = 2$ we find:

$$nd_b(N_{nulls}) = 2\left(0.5\kappa d|\cos\theta_m|\Delta\theta\right)^{N_{nulls}}, N_{nulls} \geq 1 \tag{3.68}$$

Until now, in our equations we have ignored the fact that a null should suppress over a certain *bandwidth* BW. From paragraph 3.2.4 we know that a small frequency deviation can be regarded as a direction deviation. Therefore we add equation 3.47 to $|\Delta\theta|$:

$$suppr(N_{nulls}) = 2\left(0.5\kappa d\left(|\cos\theta_m|\Delta\theta + |\sin\theta_m|\frac{0.5BW}{f}\right)\right)^{N_{nulls}} \tag{3.69}$$

Here BW is the bandwidth over which the null should suppress and f is the average frequency of the interferer. Note:

- κ also depends on f;

- The latter equation (3.69) is based on situations where the *the modulus of the first weight factor* is (arbitrarily) chosen to be 1 (which, off course, doesn't say anything about the modulus of the other $N-1$ weight factors). Simulations show that this formula almost perfectly fits the simulated suppression (see Chapter 5.5);

- For 1 antenna element the suppression is 0 dB by definition because 1 antenna cannot form nulls to suppress signals.

For the case where the weight factors are downsized such that the *largest weight factor* has size 1, equation 3.69 slightly changes: simulations (see next chapter) show that the suppression will be about 5.1 dB per null *better* (because of the smaller weight factors). This is equal to adding a factor of 1.8, as can be seen in equation 3.70:

$$\begin{aligned} nd_b(N_{nulls}) &= 1.8 \cdot 2 \left(\frac{1}{1.8} \cdot 0.5\kappa d \left(|\cos\theta_m|\Delta\theta + |\sin\theta_m| \frac{0.5BW}{f} \right) \right)^{N_{nulls}} \\ &= 3.6 \left(\frac{1}{3.6}\kappa d \left(|\cos\theta_m|\Delta\theta + |\sin\theta_m| \frac{0.5BW}{f} \right) \right)^{N_{nulls}}, N_{nulls} \geq 1 \end{aligned} \tag{3.70}$$

In dB we get:

$$\begin{aligned} nd_{b,dB}(N_{nulls}) &= 11.13 + N_{nulls} \cdot 20\log_{10} \left(\frac{1}{3.6}\kappa d \left(|\cos\theta_m|\Delta\theta + |\sin\theta_m| \frac{0.5BW}{f} \right) \right), \\ & N_{nulls} \geq 1 \end{aligned} \tag{3.71}$$

where N_{nulls} is the number of nulls, $\kappa = \frac{2\pi f}{c}$, d the antenna spacing (in meters), θ_m is the direction of the interferer (in radians), $\Delta\theta$ is the maximum angular uncertainty (in radians), f is the frequency of the interferer (in Hz) and BW is the bandwidth of the interferer (in Hz).

Figure 3.9 gives an example of null depths predicted by equation 3.71.

Note:

- This suppression formula assumes no amplitude or phase errors, no quantization, no mismatch or other sources of inaccuracies.

- For 0.5λ antenna spacing, $\kappa d = \pi$.

- This formula assumes nulls at the most optimum places.

- As said, this final formula has a *steepness* that is curve-fitted from simulations in which the array is optimized for nulls as deep as possible and normalized such that the largest weight factor has length 1. In real situations, an array is usually optimized for maximum SINR, which could give slightly different null depths than predicted with this formula.

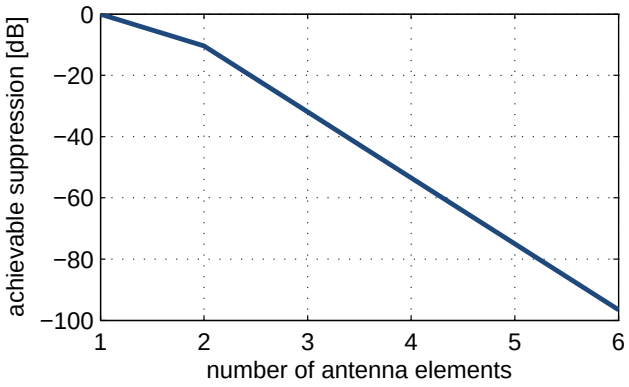


Figure 3.9: Null depth example calculated with equation 3.71 for different numbers of nulls working together. An angular uncertainty of 10 degrees is used with an interferer on -40 degrees at 1.1 GHz with a bandwidth of 100 MHz. The nominal array frequency is also 1.1 GHz and the antenna spacing is $\frac{1}{2}\lambda$. Note that number of nulls = number of antenna elements - 1.

When one has 4 antenna elements, one can make 3 nulls. With equation 3.71 we see that an interferer at 1.1 GHz with a bandwidth of 50 MHz from a direction of 50 degrees with angular uncertainty $\Delta\theta$ of 5 degrees, for 0.5λ antenna spacing, can be suppressed suppressed about 51 dB.

3.3 Demands on the number of quantization bits for nulling

We now have examined three important sources of errors that limit the reachable null depth:

- weight factor phase quantization
- weight factor amplitude quantization
- angular uncertainty and frequency bandwidth of the interferer

With the way of quantization as mentioned in paragraph 3.2.1 (where the position of the start- and stop-edge of the LO clock pulse are calculated and rounded to their nearest realizable value), it can be shown that the phase quantization error and amplitude quantization error are independent. Therefore, we can add their variances to get the total quantization effect. That is, we can add

equation 3.18 and equation 3.39:

$$\begin{aligned}
\sigma_{sum}^2 &= \sigma_p^2 + \sigma_a^2 \\
&= \frac{N\pi^2}{2^{2n_{bits}}}\left(\frac{Var(w_n) + E(w_n)^2}{12}\right) + \frac{N-1}{18}\cdot\frac{\pi^2}{2^{2n_{bits}}} \\
&= \frac{\pi^2}{2^{2n_{bits}}}\left(\frac{N(3Var(w_n) + 3E(w_n)^2 + 2) - 2}{36}\right)
\end{aligned} \tag{3.72}$$

Remember that σ_a is based on the assumption of uniformly divided weight factor lengths between 0 and 1 (with the largest weight factor having length 1). Without this assumption the entire probability density function of w_n would be left as a parameter which would make the result too complicated. σ_p is not yet based on this assumption. It has $Var(w_n)$ and $E(w_n)$ as parameters. If we apply the same assumption from σ_a on σ_p (using equation 3.21 and 3.20 for $Var(w_n)$ and $E(w_n)$) we get:

$$\begin{aligned}
\sigma_{sum}^2 &= \frac{N\pi^2}{2^{2n_{bits}}}\left(\frac{4N^3 + 8N^2 - 3N + 3}{144N^3}\right) + \frac{N-1}{18}\cdot\frac{\pi^2}{2^{2n_{bits}}} \\
&= \frac{\pi^2}{2^{2n_{bits}}}\left(\frac{12N^3 - 3N + 3}{144N^2}\right) \\
&\approx \frac{\pi^2}{2^{2n_{bits}}}\left(\frac{12N}{144}\right) \\
&= \frac{\pi^2 N}{12\cdot 2^{2n_{bits}}}
\end{aligned} \tag{3.73}$$

For the null depth as a function of both phase and amplitude quantization, which we call nd_q we now get:

$$\begin{aligned}
nd_q &\approx \sigma_{sum}\sqrt{\frac{\pi}{2}} \\
&= \frac{\pi}{2^{n_{bits}}}\sqrt{\frac{N}{12}}\cdot\sqrt{\frac{\pi}{2}} \\
&= \frac{\pi\sqrt{\pi N}}{2\sqrt{6}\cdot 2^{n_{bits}}}
\end{aligned} \tag{3.74}$$

Question: doesn't the position of the desired signal influence the nulling depth? In principle, there will always be a trade-off between nulling depth and signal strength. However, for enough degrees of freedom (= antenna elements) it becomes possible to simultaneously reach the (nearly) optimal interferer suppression and to meet the demands on (suppression of) the signal. Paragraph 5.1 goes further into the calculation of optimal weight factors.

In order to get a significant suppression (about 20 dB) with only 3 to 6 antenna elements, according to equation 3.74 we need at least $n_{bits} = 5$. Table 3.1 shows the necessary number of bits for different null suppressions.

	Null depth [dB]						
N	**-5**	**-10**	**-15**	**-20**	**-25**	**-30**	**-35**
3	1.8	2.6	3.5	4.3	5.1	6.0	6.8
4	2.0	2.8	3.7	4.5	5.3	6.2	7.0
6	2.3	3.1	4.0	4.8	5.6	6.5	7.3
8	2.5	3.3	4.2	5.0	5.8	6.7	7.5
11	2.7	3.6	4.4	5.2	6.1	6.9	7.7
15	3.0	3.8	4.6	5.5	6.3	7.1	8.0
20	3.2	4.0	4.8	5.7	6.5	7.3	8.2
30	3.5	4.3	5.1	6.0	6.8	7.6	8.5

Table 3.1: number of bits needed for desired null suppression

3.4 Summary

- An equation is derived (equation 3.74) that gives the maximum possible null depth as a function of timing resolution, indicated by a number of bits.
- An equation is derived (equation 3.70) that gives the maximum possible null depth as a function of bandwidth and range of angles over which the null should suppress, and as a function of the number of nulls working together.
- Assumed that the number of bits fully determines the null depth (because large angle ranges or large bandwidths always can be compensated by adding more nulls, while the number of bits puts a hard limit on the maximum null depth, which cannot be compensated), for null depths of at least -20 dB 5 bits timing resolution is needed.

Chapter 4

Circuit level design

Aim of this chapter is to present a circuit level design that generates a LO clock with a variable phase shift and pulse width. From the previous chapter we know that for nulling of about 20 dB we need at least 5 bits quantization to control the rising edge and falling edge. The circuit level design that is described in this chapter, uses 6 control bits to compensate for the loss in performance due to mismatch that will always be inevitable. With 6 bits, for a 1 GHz period the smallest time steps are 15.625 ps.

4.1 Topologies for clock-control circuits

A clock with variable pulse width and phase shift basically can be made on at least the following two ways: by using an Set-Reset latch (SR-latch, see Figure 4.1) or by taking the AND-function of two waves.

4.1.1 SR-topology and AND-topology

We want to synthesize a clock pulse with a specific phase and a specific pulse width using two pulses of which the pulse width doesn't matter, in combination with a SR-latch. The SET pulse makes the output of the SR-latch high and the RESET pulse makes the output back low.

In order for the SR-topology to generate a pulse of which the first harmonic is exactly a sine-function of the pulse width, it is very important that there is perfect symmetry between it's reaction on a change of the SET input and it's reaction on a changing of the RESET input. Perfect symmetry means: when the SET input goes high for example on moment 13 (between 0 and 64) and the RESET input goes high at moment 34, this should give *the same gain* as when the RESET input goes high at moment 13 and the SET input goes high at moment 34. In the first case a pulse of length 34 - 13 = 21 is generated while in the second case a pulse of length 64 - 21 = 43 is generated.

The problem with a standard SR-latch (as in Figure 4.2) is that, although it

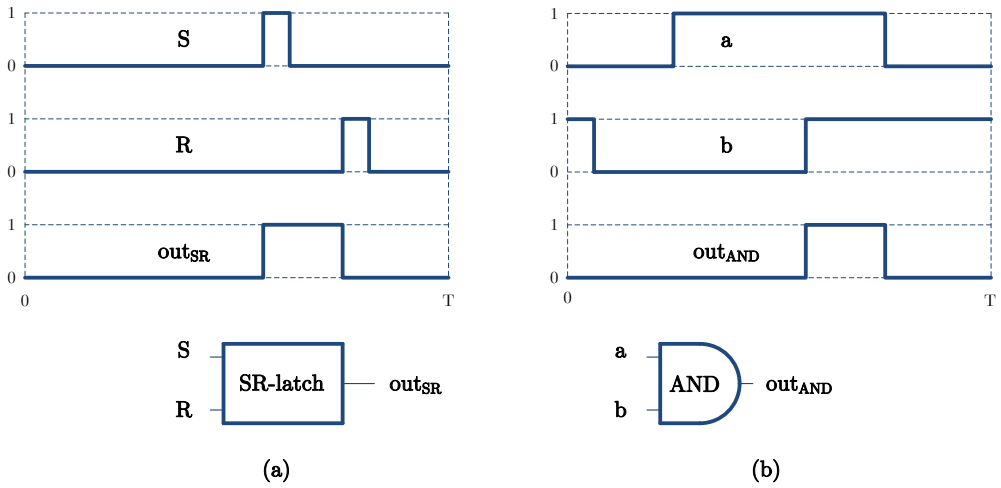


Figure 4.1: (a) pulse made by using an SR-latch, (b) pulse made by AND-function.

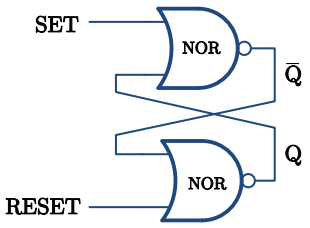


Figure 4.2: SR-latch with NORs.

seems perfectly symmetrical for the SET- and RESET input, it is not. This is because the SR-latch from Figure 4.2 is not edge-sensitive but level-sensitive, so it is sensitive for the pulse width of the SET and RESET pulses. For example, when both inputs are high[1], both outputs (Q and $\bar{Q}$) go to 0. So the SR-latch has 'RESET-priority' and therefore has no symmetrical behavior, resulting in a non-ideal sine mapping between amplitude and pulse width, like in Figure 4.3[2].

What we actually want is a latch that flips *both outputs* once both inputs are simultaneously high (which corresponds to edge-triggered behavior). A good candidate is the non-clocked JK-latch, that can easily be derived from the clocked JK-latch as in [7] (see Figure 4.4). This non-clocked JK-latch *switches* it's outputs when both inputs are high simultaneously, so functionally it behaves like an edge-triggered SR-latch. However the problem with these kind of structures

[1]Because the SET or RESET pulse have a certain pulse width, they will overlap when trying to switch the SR-latch on and off very fast in order to generate a short output pulse.

[2]Although we only need the first part of the sine-curve to make all gains between 0 and 1, a non-symmetrical sine mapping usually is also shifted in the x-axis, making the problems worse.

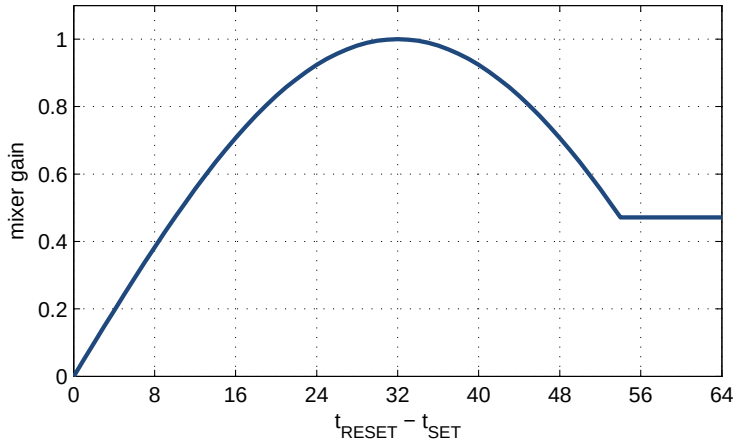


Figure 4.3: Distorted sine mapping between pulse width and amplitude due to RESET-priority of a SR-latch in combination with a nonzero pulse width of the SET and RESET pulses.

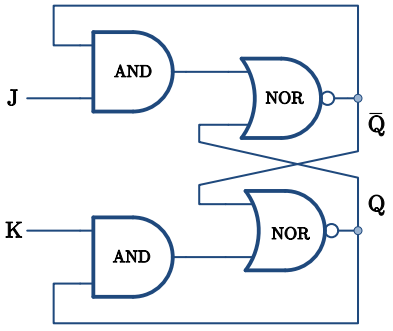


Figure 4.4: Edge-sensitive JK-latch.

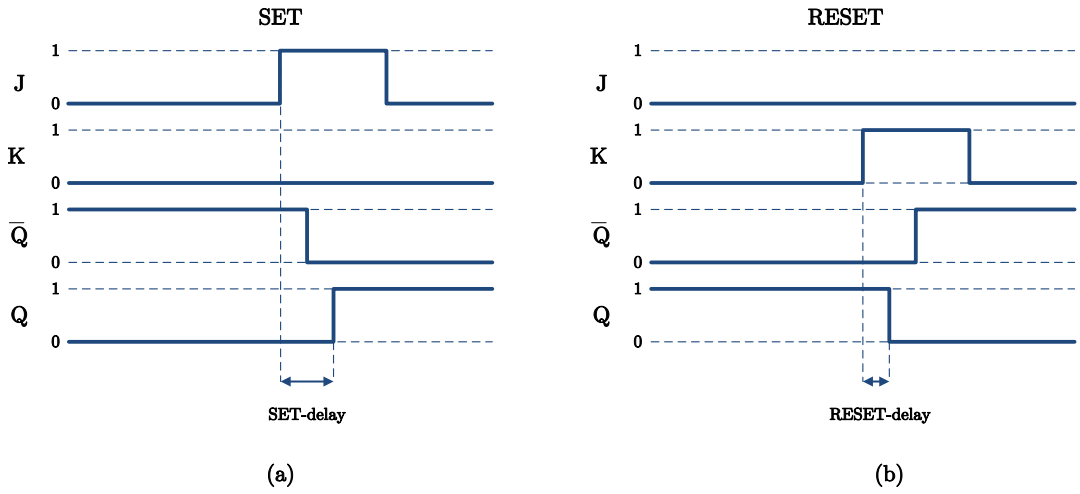


Figure 4.5: JK-latch, (a) long SET-delay (b) shorter RESET-delay.

is that they have a feedback loop from the output to an inner node (in Figure 4.4 both output NORs are crosscoupled). Because the NORs have some delay (in the order or 60 ps) this means that Q and $\bar{Q}$ are not always each others complement. For short periods of time they can be simultaneously 1 or 0. Therefore they cannot be used as complementary clocks to drive a balanced mixer. And when only one output, for example Q, is used to drive the mixer, the SET-delay is longer than the RESET-delay (see Figure 4.5), which again leads to asymmetry. Asymmetry for SET- or RESET-behavior leads to an unpredictable generated pulse width of the LO clock, causing a non-symmetrical, shifted, distorted and unpredictable sine mapping between the aimed pulse width and the resulting amplitude of the first harmonic.

Because it is so difficult to design a circuit that

1. can be set and reset;
2. has in all cases the same propagation delay for being set or being reset;
3. has two outputs Q and $\bar{Q}$ that are *always* complementary;
4. and behaves symmetrically for SET and RESET pulses so flips both outputs when SET and RESET are simultaneously high

we reject this SR-approach and we choose a design with the AND-approach, which can much easier be made very symmetric (see the results in section 5.7.2).

4.1.2 Switches

In order to keep the symmetry between a positive LO clock edge and a negative LO clock edge, we use a balanced passive switching mixer, which can be seen

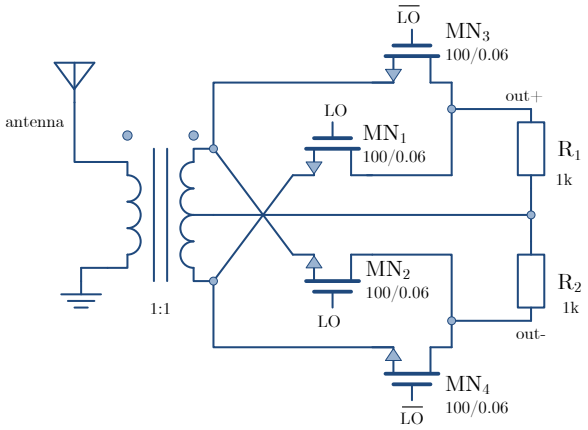


Figure 4.6: Passive balanced mixer.

in Figure 4.6. As said in section 2.2.3, it suffices to use only NMOSTS since we expect our antenna signal to be very low, so the NMOSTS always stay in strong inversion. The bulks of all four NMOSTs are connected to ground, which, however, is no problem because our previous assumption that the amplitude of the antenna signal never exceeds ± 100 mV means that the forward voltage of the bulk-source and bulk-drain junctions will never be exceeded.

A load of 1 kΩ is assumed for the stage following the mixer (which will be the beamformer summing point). For a low switching resistance (low losses and low noise) switches of 100 µm, which corresponds to Ron ≈ 5 Ω.

4.2 AND-design

For the AND-architecture it is important that pulse a and b have exactly 50% duty cycle (refer to Figure 4.1). When one of the pulses has a larger pulse width, there will be some overlap between a and b in all cases, which causes a minimum gain > 0 (refer to Figure 4.1b). When one of the pulses has a smaller pulse width, the maximum gain of the mixer cannot be reached.

4.2.1 Digital delay

For defining a variable moment in time, there are 2 solutions: analog delay (using some kind of current source charging a capacitor) or digital delay (using shift registers). For low jitter specifications, digital delay is preferred [5]. In addition, digital delay can easily be scaled in frequency, which makes our receiver easily adjustable to different signal frequencies. Therefore, as much delay as possible is done digitally.

Simulations show that shift registers up to at least 4 GHz can easily be made

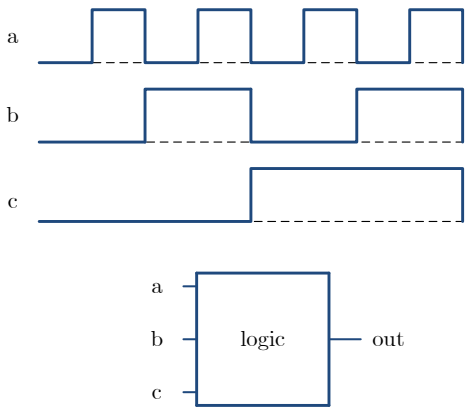


Figure 4.7: Generating a 1 GHz clock with 8 possible phases, using 3 clocks and some combinational logic.

in CMOS 65nm technology, which makes timing resolutions possible of 125 ps[3]. Because we want our system to generate a signal of 1 GHz with 6 bits resolution, every clock period of 1 ns has to be divided into $2^6 = 64$ steps of 15.625 ps. This cannot be done with only digital circuitry, so we make the first 3 bits digital (up to 125 ps) and the final 3 bits analog (up to 15.625 ps).

The digital delay can be made in two ways:

- With a clock of 4 GHz, 2 GHz and 1 GHz and some combinational logic (see Figure 4.7);
- With only a clock of 4 GHz, a signal of 1 GHz and a 8-bit shift registers (see Figure 4.8);

We choose the 2nd way because it is more easily to get a 50% duty cycle signal with this topology.

To make the shift register as fast as possible we use simple D-latches from Figure 4.9. Normally a D-latch uses a feedback (with a 2nd inverter) such that it really acts as a 'latch' and hold it's value when the transmission gate is open. But at a clock speed of 4 GHz the parasitic gate-source and gate-drain capacitances of MN2 and MP3 suffice to hold the D-latch value (1.2V or 0V).

The transmission gate is dimensioned such that the Ron of the PMOST is equal to the Ron of the NMOST.

Since the 1 GHz clock that enters the shift register is inverted at each D-latch, a 2nd, parallel shift register is added to generate the complementary signal of the first register, as can be seen in Figure 4.10. Dummy D-latches are added in front of the shift register to match the rising- and falling edges in the non-dummy D-latches. This is necessary because clock dividers that generate in and $\bar{in}$ have a different output impedance than the output impedances of the D-latches.

[3]Note that we can use both the positive and negative edge of a 4 GHz signal.

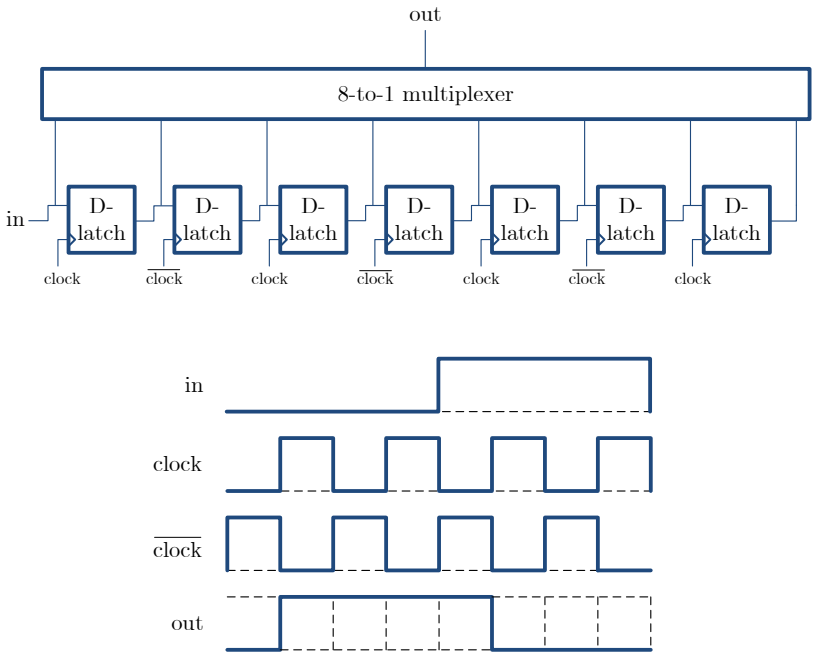


Figure 4.8: Generating a 1 GHz clock with 8 possible phases, using a shift register and a multiplexer. In this example, *out* is selected by the multiplexer to be connected to the output of the 5th D-latch.

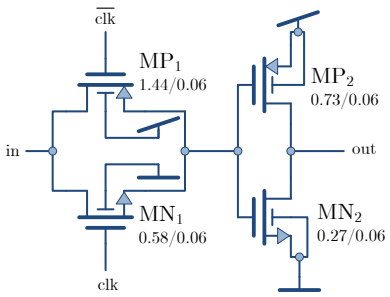


Figure 4.9: D-latch, build from a transmission gate with an inverter.

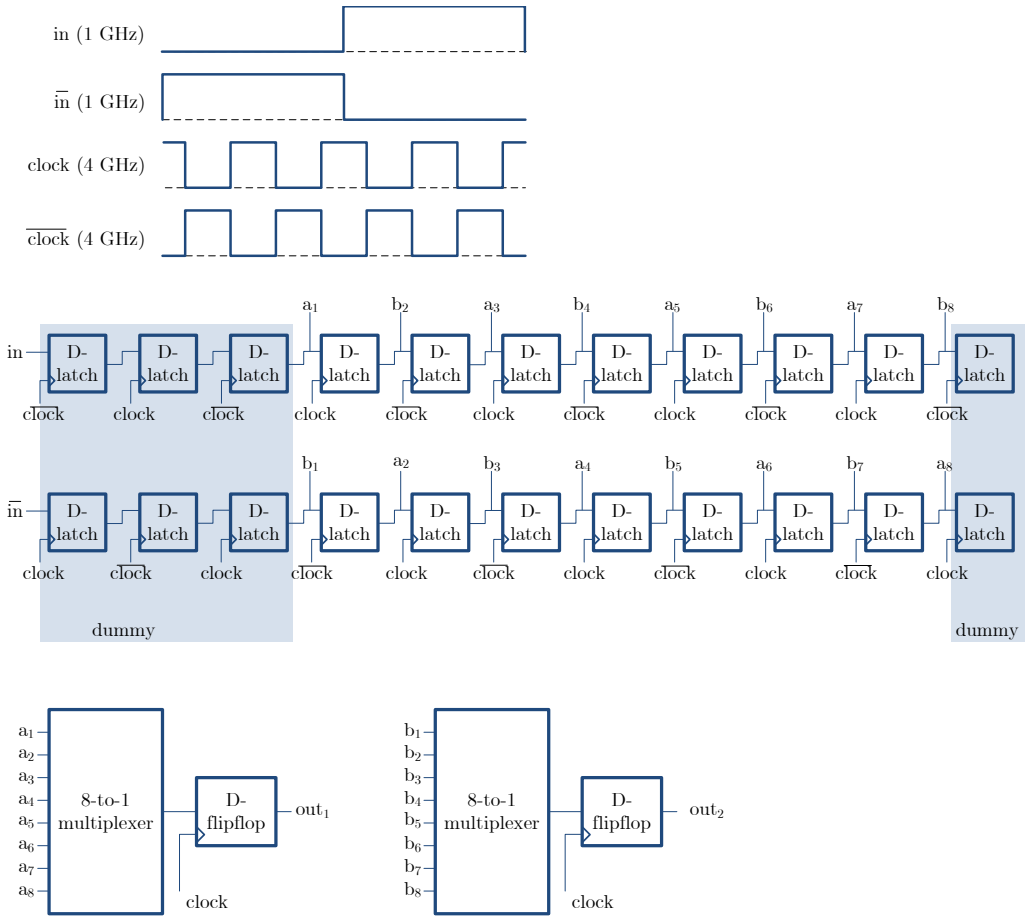


Figure 4.10: Balanced shift register with multiplexers. a_1 to a_8 are multi-phase components of in. b_1 to b_8 are multi-phase components of $\bar{in}$. Both multiplexers select one of these multi-phase components. The D-flipflops at the outputs of the multiplexers re-clock the selected multi-phase components to reduce jitter.

The dummy D-latches at the end of the shift register chain act as dummy loads.

Figure 4.12 shows the signals[4] $a_1 ... a_8$ and $b_1 ... b_8$, which are multi-phase versions of the 1 GHz clock. One out of these signals can be selected using a digitally controlled multiplexer (see Figure 4.11). The multiplexer is build from switches (transmission gates) and inverters. Between every transmission gate, an inverter with an NMOST of size 0.27/0.06 and a PMOST of size 0.73/0.06 is placed. Without these inverters the output of the multiplexer would have too slow rise- and fall times because it would have 3 transmission gates directly in series from input to output, giving a large output impedance. Even the capacitive load of the transmission gates itself would be too large without using the

[4]Note that for a_5 b_1 could be used, for a_6 b_2 etc., which could save us a total of 8 D-latches.

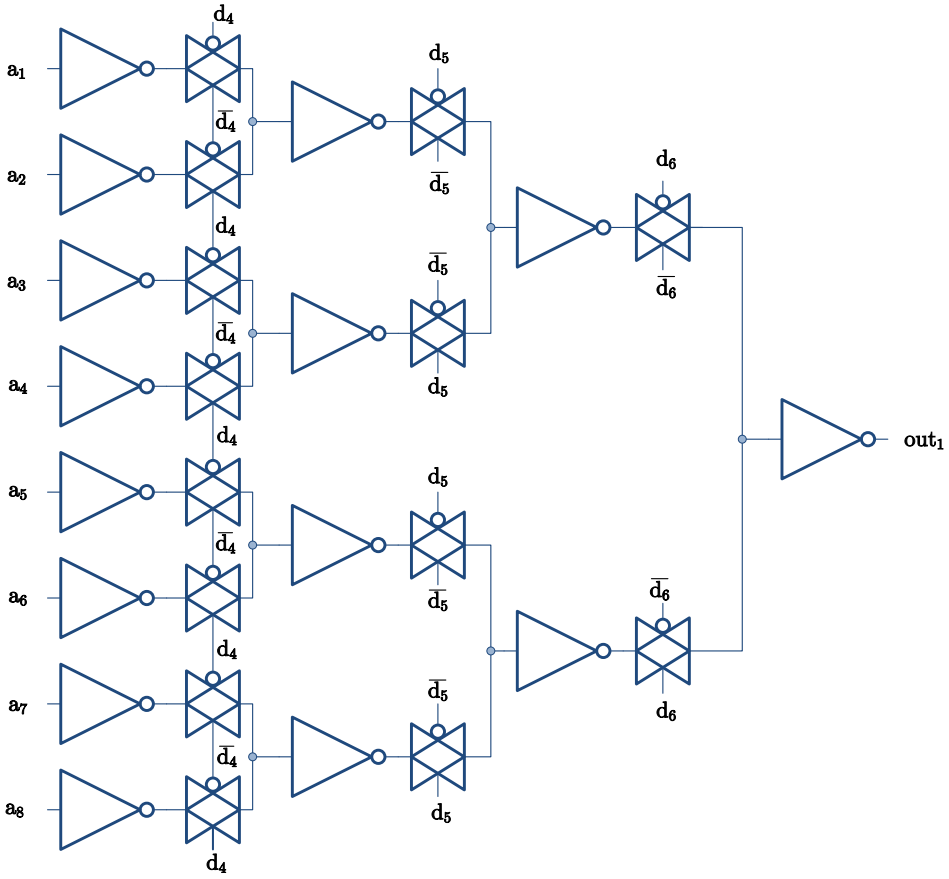


Figure 4.11: An 8-to-1 multiplexer build of transmission gates and inverters.

inverters.

Again, the transmission gates are designed to have equal Ron voltages for the NMOST and PMOST. For the digital control lines $d1+$, $d1-$, $d2+$, $d2-$, $d3+$ and $d3-$ also inverters are placed (which are not shown in Figure 4.11 but are shown in the schematic from Appendix B) for simulating a realistic output impedance for the digital control lines.

The 1 GHz signals (in and $\bar{in}$) are generated from the 4 GHz signal with standard digital clock divider (2 flipflops, each build from 2 D-latches).

After both multiplexers a D-flipflop is placed to clock the outgoing signals in order to get rid of jitter introduced in the multiplexers. These flipflops need to update their outputs 8 times per ns with a 4 GHz clock, which is why every flipflop consists of 2 parallel sub-flipflops (see Figure 4.13). During the negative clock level MX_1 samples the input D. Simultaneously, the previous sampled bit at INV_2 appears at the output out_1. During the positive clock level, MX_2 samples and INV_1 presents it's bit at the output.

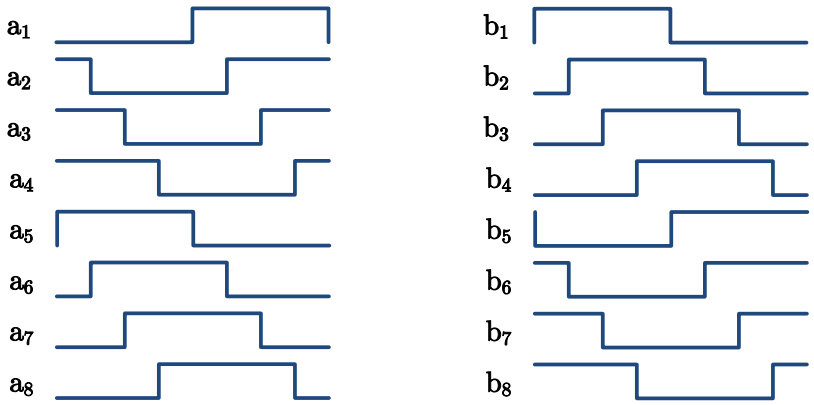


Figure 4.12: Signals $a_1 ... a_8$ and $b_1 ... b_8$.

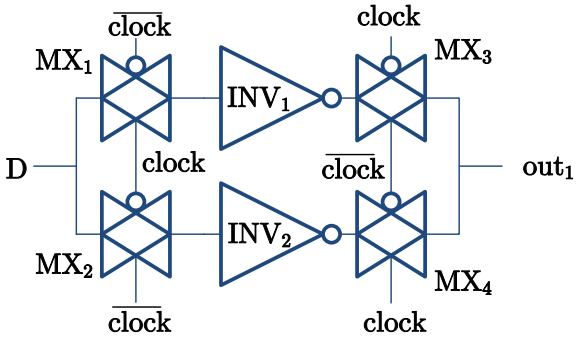


Figure 4.13: Flipflop consisting of two parallel sub-flipflops to double it's sampling speed.

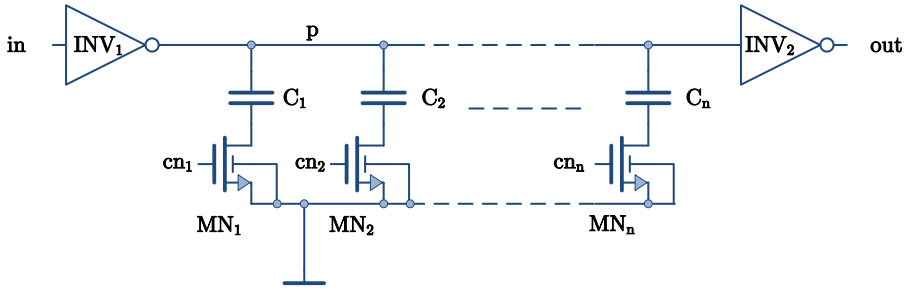


Figure 4.14: Shunt capacitor delay line. Control lines $cn_1 ... cn_n$ can be used to switch capacitors on and off.

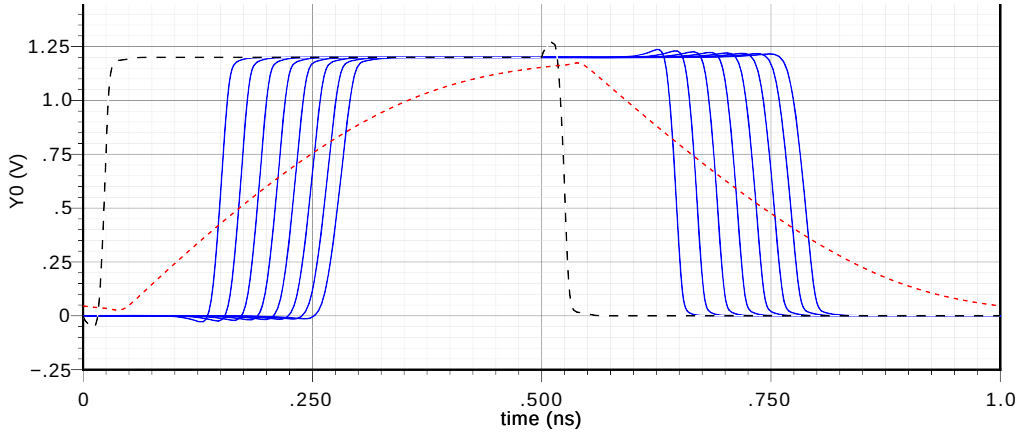


Figure 4.15: Example of the input (large black dashes), node p drawn for the largest delay (small red dashes) and the possible outputs (solid blue lines) of a shunt capacitor delay line.

4.2.2 Analog delay

The analog delay block needs to delay the 50% duty cycle signal with an incremental delay between 0 and 125 ps in steps of 15.625 ps (an inevitable constant 'offset' delay is no problem). Because these steps are this small, a DLL with current starved inverters cannot be used (every inverter would add a delay step of at least 25 ps). A good alternative is the shunt capacitor delay line [1]. It is shown in Figure 4.14. It basically consists of an inverter with some capacitors at it's output. Every capacitor can be switched on and off, changing the RC-delay from input to output. Figure 4.15 shows an example of the input and outputs of the delay line.

Ideally, delay increases linearly with the number of capacitors switched 'on'. In practice, some non-ideal factors make the difference between two delay steps dependent on the delay itself, resulting in non-equal delay steps (see Figure 4.16). These non-ideal factors are:

- The input capacitance of INV_2 is nonlinear over voltage. For practical values, as used in the final design[5] the influence of this varying impedance on the linearity of the delays is negligible.

- The 'on'-resistances of MN_1 to MN_n are non-zero. This resistance together with (dis)charging a capacitor gives a voltage drop that makes node p earlier crossing the 0.6V 'threshold' of INV_2. This effect is more strong for small delays where only 1 or 2 capacitors are 'on' because then the current through these capacitors is larger. Therefore, for small delays, the difference between two neighboring delays becomes smaller than for large delays. For the circuit dimensions as used in the final design, this is the dominant factor for nonlinearity. Making the NMOSTS MN_1 to MN_n larger is a solution, but only up to a certain amount, because this also makes the drain-source capacitances of the NMOSTS larger.

- When turned 'off', MN_1 to MN_n have a drain-source capacitance to ground. When these NMOSTS become too large, these parasitic drain-source capacitances also becomes large, and start to couple the capacitors $C_1, ..., C_n$ to ground, even when the NMOSTS are 'off'. This effect makes the 'offset' delay[6] larger. Larger offset delay results in the fact that node p has not enough time to entirely charge to vdd or discharge to ground for large delays (see figure 4.14 and Figure 4.15). So when the input of INV_1 switches, node p earlier crosses 0.6V and the output switches relatively too early, giving smaller delay steps when many capacitors are switched 'on'. To avoid this effect, MN_1 to MN_n may not become too large.

Mathematically it can be shown that the nonlinear output impedance of INV_1 has *no negative effect* on the above mentioned nonlinearity of the delay line, because it acts always in the same way, regardless of the number of capacitors that is switched 'on'.

Because we want the LO clock to be adjustable to frequencies between 500 MHz and 1 GHz, and because the delay steps do not scale with frequency, we need 16 delays steps of 15.625 ps in stead of 8 delay steps, such that even for 500 MHz we can provide enough analog steps of 15.625 ps to fill one digital step.

The sizes of the final inverter (INV_2 in figure 4.14) are chosen using 3 objectives:

- For DC the switching point of the inverter is exactly at 0.6 V;

- The inverter is small enough not to give extra unnecessary capacitance to node p;

- The inverter has a gain as large as possible (to act like a comparator).

[5] INV_1 is build with a 0.491/0.06 NMOST, a 1/0.06 PMOST, INV_2 is build with an 0.12/0.06 NMOST and a 0.4/0.06 NMOST, $C_1 = C_2 = ... = C_n = 7$fF, $MN_1 = MN_2 = ... = MN_n = 2/0.06$ NMOST

[6] The 'offset' delay is the delay of the delay block for all NMOSTS turned off.

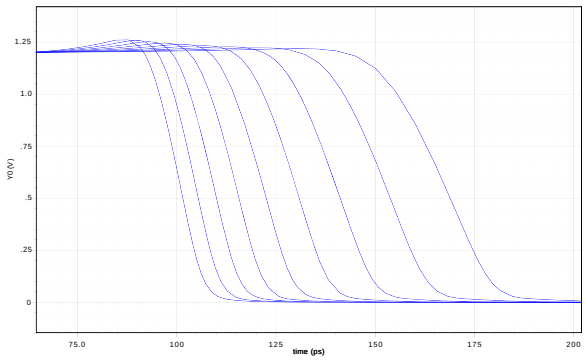


Figure 4.16: The output of a shunt capacitor delay line with nonlinear delay steps.

4.2.3 AND-gate and drivers

For the AND-gate the symmetrical NAND implementation of [3] is chosen, which, in contrast with a 'normal' CMOS NAND gate, is perfectly symmetric for input a and b. Figure 4.17 shows the used dimensions. The fact that a NAND in stead of an AND gate is used, is no problem because we need a complementary LO clock anyway, so the output of the NAND is used for the negative LO clock. To restrict the simulation time, a voltage controlled voltage source generates the positive LO clock, following exactly the exact rising and falling edges of the negative LO clock.

In order to drive the large switches of W = 100µm and L = 0.06µm (with large parasitic capacitances) some drivers are needed between the NAND-gate and the switches. For this purpose a chain of 6 inverters is used (both for the positive and the negative clock). Every inverter is about a factor e larger than the previous inverter, which is a common factor for minimizing the propagation delay.

4.2.4 Making the circuit symmetrically

Some important circuit dimensions (mainly transistor widths) are optimized using simulations. We will note them, in the order in which they are (and should be) optimized:

1. The NMOST of the final inverter of both driver stages is modified in order to make outputs of the driver stage ($clk+$ and $clk-$) cross each other at exactly 600 mV.

2. $wid0$, which is the width of the NMOST of the inverter that drives the analog delay block, is optimized such that (measured at the output of the delay block) the pulse width for 0 capacitors 'on' becomes the same as the pulse width for 7 capacitors 'on'. The pulse width itself, ideally 500 ps, is not important yet;

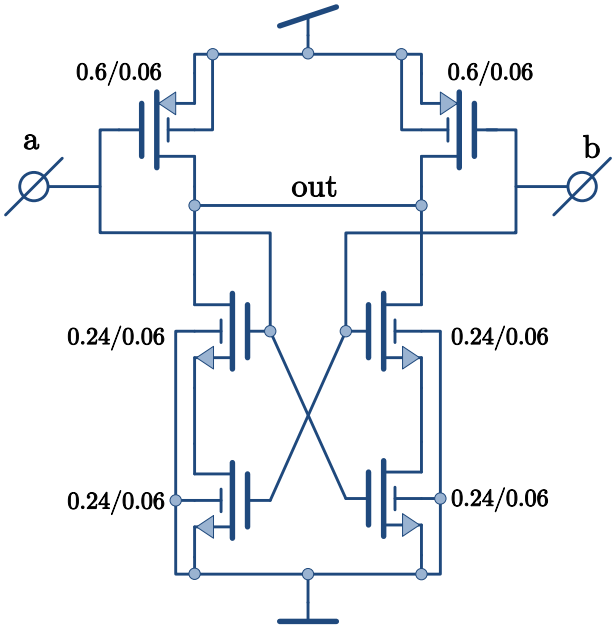


Figure 4.17: Symmetrical NAND gate.

3. An extra inverter is put in front of the delay block, of which the NMOST has width $wid2$. This variable is optimized such that the pulse width at the output of the delay block is exactly 500 ps, which is the same as matching the delay of the analog delay block for positive and negative edges.

4. *cap*, the capacitance in every stage of the analog delay block, is modified such that the phase of $d = 47$ and $d = 48$ differs exactly 15.625 ps (this step is the difference between 7 capacitors 'on' and 0 capacitors 'on' and is therefore the most difficult step). The delays are measured at $clk+$ and $clk-$ (at the switches).

Off course, mismatch will change these optimizations but with upscaling the circuit the changes due to mismatch can be made small enough. A good criterion for 'small enough' could be that in 99% of the manufactured chips, the rising and falling edges of the synthesized positive and negative clocks will never be more than 7 ps earlier or later than their nominal moments.

All optimized component values can be found in the schematics in Appendix B.

4.3 Summary

- A circuit is designed that generates two square waves, each having a 50% duty cycle. The phases of both square waves can be independently controlled over 360 degrees in 64 steps (6 bits timing accuracy). By taking

the AND-function of both square waves, a clock pulse is generated with adjustable phase and pulsewidth.

- The adjustable phase for both square waves is generated using a shift register as a digital delay, delaying in steps of $\frac{1}{8}$ of one clock period. With shunt capacitor delay lines the delay of both square waves can be further adjusted in steps of 15.625 ps. Enough capacitors are added for using the system to generate a clock pulse between 500 MHz and 1 GHz.
- The circuit is optimized for low jitter-sensitivity (using the re-clocking of time-discrete signals using 1 low-jitter clock) and for large symmetry with respect to the timing of rising and falling edges of the synthesized clock pulse.

Chapter 5

Simulations

In this chapter we will check the derived equations in the previous chapter for the nulling depth. We also treat some theory about the used approach of finding the optimal weight factors.

5.1 Calculation of optimal weight factors

5.1.1 Positioning nulls

A null is described by a particular direction at a particular frequency. When the desired direction and frequency of all nulls are known, the corresponding weight factors can be calculated. The positioning of nulls into certain directions (without caring about an 'desired signal' that does not have to be suppressed) all at the same fixed frequency f is very easy. Let's recall the array factor:

$$F(\theta) = \sum_{n=0}^{N-1} \bar{w}_n e^{j\kappa n d \sin\theta} \tag{5.1}$$

For a three-element array, the array factor reduces to

$$F(\theta) = \bar{w}_0 + \bar{w}_1 e^{j\kappa d \sin\theta} + \bar{w}_2 e^{2j\kappa d \sin\theta} \tag{5.2}$$

We can position 2 nulls, at θ_1 and κ_1 and at θ_2 and κ_2. Therefore we have two equations:

$$\begin{aligned} 0 &= \bar{w}_0 + \bar{w}_1 e^{j\kappa_1 d \sin\theta_1} + \bar{w}_2 e^{2j\kappa_1 d \sin\theta_1} \\ 0 &= \bar{w}_0 + \bar{w}_1 e^{j\kappa_2 d \sin\theta_2} + \bar{w}_2 e^{2j\kappa_2 d \sin\theta_2} \end{aligned} \tag{5.3}$$

In principle the whole 'shape' of the array factor is now determined. The third degree of freedom only determines the scale of this array factor, so we arbitrarily set some angle θ_3 at some frequency κ_3 to 1:

$$1 = \bar{w}_0 + \bar{w}_1 e^{j\kappa_3 d \sin\theta_3} + \bar{w}_2 e^{2j\kappa_3 d \sin\theta_3} \tag{5.4}$$

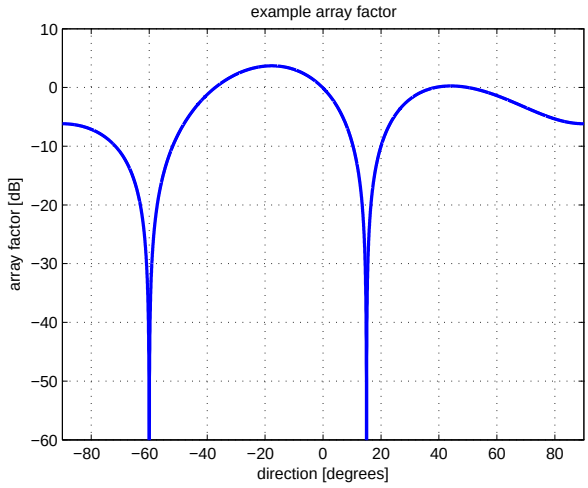


Figure 5.1: Example of an array factor with nulls at -60 degrees and 15 degrees.

Now we have a system of 3 (complex) linear equations with three (complex) unknowns (w_0, w_1 and w_2). Solving this system gives the 3 complex weight factors. For example, when we want nulls into the direction of -60 and 15 degrees at 1.1 GHz, and when we want the array factor into the direction of 50 degrees to be 1 (0 dB), for a linear array with $\frac{1}{2}\lambda$ spacing, we get the following complex weight factors: [-0.069 + 0.636i, 0.119 + 0.218i, 0.573 + 0.283i]. Figure 5.1 gives a plot of this array factor as a function of direction θ. The antenna spacing d is chosen to be $\frac{1}{2}\lambda$.

5.1.2 Finding optimum weight factors

Note that in the above example, we cannot move the top of the array factor from -20 degrees to 50 degrees, without changing the position of the nulls. We simply do not have enough degrees of freedom (antenna elements). One solutions is to add one or more antenna elements. Another solution is to look for an *optimum*, for example in the sense of maximum SIR or maximum SINR. When the desired signal is at 50 degrees, the array factor at this direction can be optimized at the cost of less 'deep' nulls. The next paragraphs treat this optimization process.

Criteria for optimum weight factors

Literature shows different criteria for optimal solutions [8]. The most common criteria are:

- minimizing the mean squared error between reference signal and output signal (a reference signal needs to be generated by the receiver circuitry);
- maximizing Signal-to-Interferer and Noise Ratio (SINR);

- minimizing the output noise variance (when the output noise variance is 0, only the signal of interest is received);
- maximizing the output energy while keeping the gain of the desired signal fixed

It has been shown ([8]) that all these criteria lead to the *same solution* for the weight factors (being only scaled versions of each other): the *Wiener solution.* This means that the choice of a particular criterion is not critical for performance. In signal processing, every *linear time-invariant* filter that optimizes a signal corrupted by additive noise for maximum signal-to-noise ratio in least square sense ends up with this Wiener solution.

How to find the Wiener solution?

The Wiener solution (for the optimum filter) can be calculated with the well-known Wiener-Hopf equation when the autocorrelation of a reference signal is known, together with the autocorrelation of the observed (noisy) signal and the cross correlation between the observed signal and the reference signal. The reference signal needs to be correlated with the desired signal. In most beamforming applications, statistical properties of the desired (reference) signal are known (for example, as some kind of pilot tone or pseudo-noise code) so the optimum weight factors can be calculated. This can be done using for example the Direct Sample Covariance Matrix Inversion, or the Least Mean Squares (LMS) method which uses the well-known steepest descent method to minimize a cost function ([8], pp. 43). When the weight factors are periodically re-calculated (in order to adjust to some changes in environment) we're dealing with *adaptive beamforming.*

Additional constraints

When a reference signal is *not* known, or when there are additional constraints to the weight factors, such as a minimum modulus of 0.3, the easiest and mostly used way to find an optimum solution is to iteratively minimize some cost function, for example $\frac{1}{SIR}$. Each of the criteria from paragraph 5.1.2 can be used as a cost function. This way the problem reduces to a mathematical optimization problem.

The Matlab Optimization Toolbox (version 3.1.2) that is used by us, offers 16 different optimization functions. In this work we have chosen to use *fmincon* from the Matlab Optimization Toolbox. This function is the only optimization function that is able to find "the minimum of a constrained nonlinear multivariable function". *Constrained* is necessary because our modula have to be inside the range [0, 1] (or [0.3, 1], or whatever smallest weight factor we want to simulate). *Nonlinear* is necessary because as a cost function $-10 \cdot \log_{10}(SIR(\vec{w}))$ is used, which is a nonlinear function of $\vec{w}$.

fmincon needs as it's first parameter the cost function, which is a function of the weight factors $\vec{w}$. The function tries to find the optimum values for $\vec{w}$ by minimizing the cost function, starting at the starting point indicated by parameter $\vec{w_0}$. In Matlab the vector $\vec{w}$ is implemented in the form [$modulus_0$, $phase_0$, $modulus_1$, $phase_1$, ...] (in stead of using complex values). This allows us to easily add constraints for $fmincon$, namely in the sense of an upper bound vector ub and a lower bound vector lb. The lower bounds for all modula can be set to 0.3 and the upper bounds are always chosen to be 1. The lower bounds of all phases are set to $-\pi$ and the upper bounds are set to π.

fmincon needs the gradient of the cost function. In the case that one provides this gradient in a sub-function to *fmincon*, *fmincon* will work very efficiently trying to find the optimum (using the method of preconditioned conjugate gradients, see Matlab help). In our case we cannot provide an explicit function for this gradient of the cost function, because we use the *max* function inside the cost function (see next paragraph). Therefore, *fmincon* uses a less-effective optimization routine (called Sequential Quadratic Programming) in which it estimates the gradient of the cost function by numerically estimating it's partial derivative into every search direction. For N antenna elements, we have a $2N$-dimensional search space (because for every antenna element we have 2 variables that have to be optimized: amplitude and phase). In this search space the global minimum of the cost function has to be found. It is not guaranteed that the final solution of *fmincon* is *the optimum* solution (which is the *global* minimum in the search space). It can also be a *local* minimum in the search space. A solution is to run *fmincon* multiple times, each time with a different starting condition $\vec{w}0$, and to pick the best solution.

The cost function calculates the SIR for the current $\vec{w}$. Therefore it first calculates the array factor that corresponds with $\vec{w}$. Next it evaluates this array factor into the direction and for the frequency of the desired signal. The square of this signal amplitude gives the signal power. Next, for every interferer, the direction uncertainty interval is calculated. For the k-th interferer with direction ϕ_k, frequency f_k, direction uncertainty $\Delta\theta$ and bandwidth BW_k we know (see 3.47 of the previous chapter) that this interferer is equal to different interferer with *no* bandwidth but with a direction uncertainty $\Delta\theta + \frac{1}{2}BW_k\frac{|\tan\theta|}{f}$. Therefore, for every interferer we evaluate the array factor on the whole interval $[\phi_k - \Delta\theta - \frac{1}{2}BW_k\frac{|\tan\theta|}{f}, \phi_k + \Delta\theta + \frac{1}{2}BW_k\frac{|\tan\theta|}{f}]$ around the k-th interferer. In order not to take too much sampling points in this interval (which would extend simulation time) we take $2N-1$ equally-spaced points in this interval. For an N-element linear array with $N-1$ nulls, we now are certain that we have enough sampling points in order not to sample exactly inside the nulls (which would estimate the signal suppression too optimistic). We take the largest (worst-case) suppression in this interval as the actual suppression of the k-th interferer, in order to compare it with the derived formulas for the worst-case null depth (see paragraph 3.2.4 in the previous chapter).

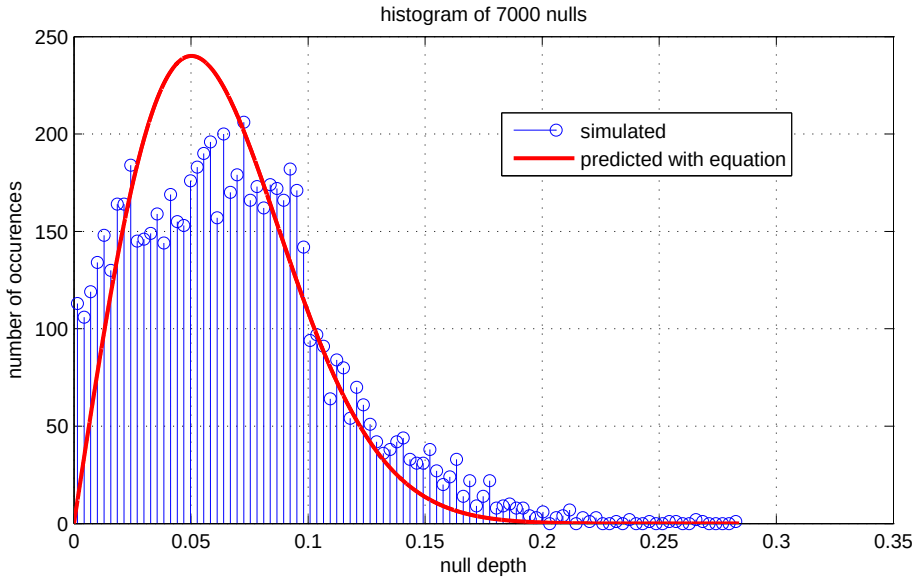


Figure 5.2: Histogram of simulated nulls and predicted nulls for an 8-element array with 5 bits quantization.

5.2 Simulating the amplitude quantization effect on null depth

To check the deduced formula for amplitude quantization, an 8-element array is simulated using 5 bits timing resolution. The weight factors for 7 nulls at arbitrary angles are calculated using the method of paragraph 5.1.1 and are quantized in *amplitude* (de phases are changed back to their ideal values). Next the the null depth is measured. This whole process is repeated 1000 runs, and a histogram from the null depth is plot for both simulated and predicted nulls (see Figure 5.2). Here the predicted shape is Rayleigh-distributed with an expectation given by equation 3.41. All nulling simulations are done using Matlab 7.5.0 together with the Optimization Toolbox. The simulated expectation of this histogram lies on 0.0677 and the predicted expectation lies on 0.0680. In the simulation, null depths close to 0 appear to show up more often than predicted. This effect becomes more obvious when going to less antenna elements. It is caused by the fact that almost 25% of the modula of the weight factors are 1 so do not suffer from (large) amplitude quantization errors. Therefore they can give very deep nulls. Why is 25% of w_n 1? This is because for an *even* number of antenna elements, the *modula* of the weight factors appear to be symmetrical, like: [0.13 0.48 0.82 1.00 1.00 0.82 0.48 0.13]. So with an *even* number of antenna elements there are always 2 largest weight factors scaled to 1. With an *odd* number of antenna elements there is sometimes 1 antenna element scaled to 1 (for example in the case [0.12 1.00 0.12]) and sometimes are 2 elements scaled

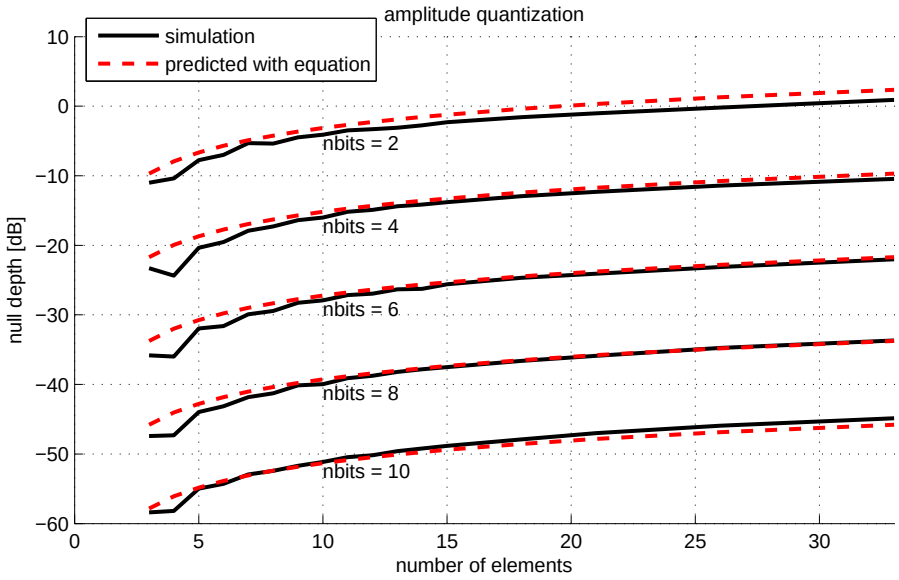


Figure 5.3: Null depth simulated applying only *amplitude quantization* for different numbers of bits and numbers of antenna elements.

to 1 (for example for [1.00 0.56 1.00]). In paragraph 3.2.3 there is corrected for only 1 antenna element that is scaled to 1 (taking into account even and odd numbers of antenna elements would make things unnecessary complicated).

The above simulation is repeated for an array with 3 to 33 antennas, and for 4 to 10 bits (in steps of 2 bits). The resulting expectations can be seen in Figure 5.3. Some remarks can be made:

- There is a 'dip' for $N = 4$ in the average simulated null depth, which is 2 - 3 dB better than predicted. This is because for $N = 4$ 2 out of 4 elements are 1 and do not suffer from amplitude quantization, while the deduced equation in paragraph 3.2.3 only corrects for 1 element that is 1. This effect also applies to $N = 6$, $N = 8$ etc. although less apparent.

5.3 Simulating the phase quantization effect on null depth

To check the deduced formula for phase quantization (equation 3.23) we use the same approach as for the amplitude quantization. The result of the null depths under influence of phase quantization can be seen in Figure 5.4. Some remarks can be made:

- Clearly the effect can be seen that for *even* numbers of antenna elements the nulling performance is slightly less good (less deep nulls) than for odd numbers of antenna elements. This is because for an even number of

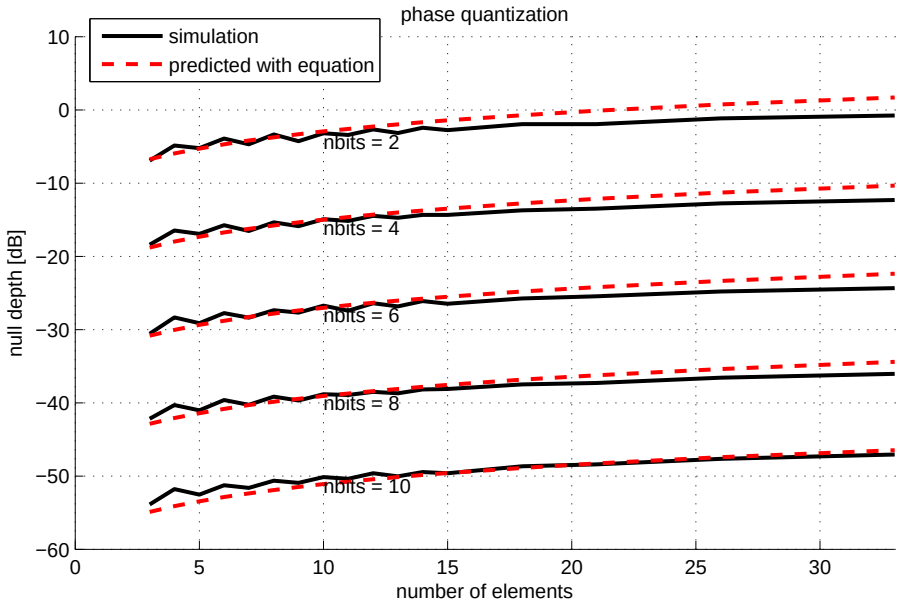


Figure 5.4: Null depth simulated applying only *phase quantization* for different numbers of bits and numbers of antenna elements.

antenna elements, always 2 weight factors have length 1 while for a odd numbers of antenna elements, sometimes 2 weight factors have length 1 but most of the time only 1 weight factor has length 1. The more weight factors have length 1, the larger the average length of the weight factors and the more influence phase quantization has. For large numbers of antenna elements, the difference between 1 of 2 'length-1' weight factors doesn't matter anymore. Therefore we see see the 'zigzag'-behavior only for small numbers of antenna elements.

- For large numbers of antenna elements (15 and more), the simulation gives better results than predicted by equation 3.23. This is due to the fact that for large numbers of antenna elements the part of weight factors that is *small* appears to be larger (and no longer uniformly divided between 0 and 1). And the smaller the weight factors, the less effect phase quantization has. When we use 3.19 to predict the phase quantization, which still has as parameters the variance and expectation of the weight factors, we get a better approximation, which can be seen in Figure 5.5.

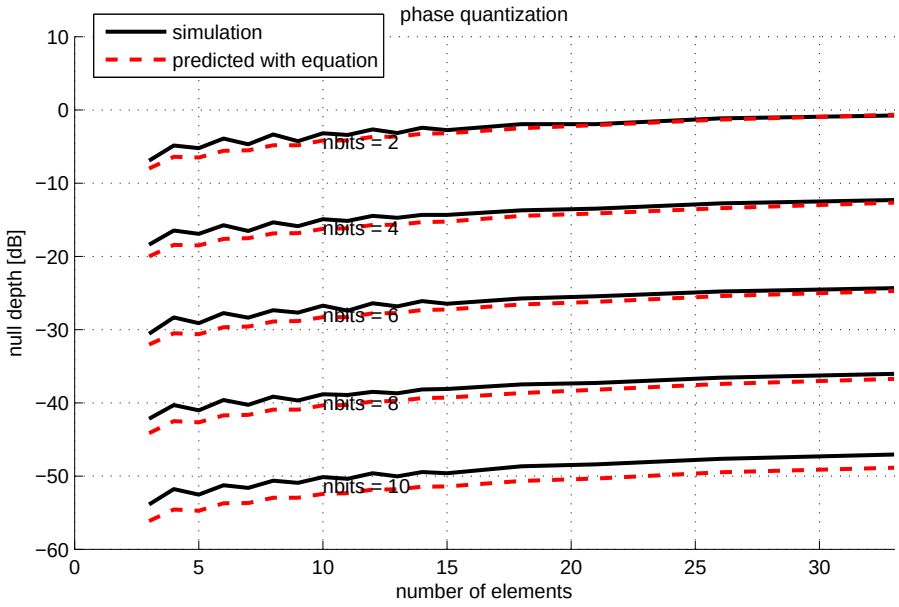


Figure 5.5: Null depth simulated applying only *phase quantization* where the prediction formula takes the variance and expectation of the weight factors into account.

5.4 Simulating of the combined phase and amplitude quantization effect on null depth

To check the deduced formula for both phase- and amplitude quantization (equation 3.74) we use the same approach as for the phase quantization. The result of this simulation can be seen in Figure 5.4. Note that this equation, again, assumes that the modulus of the weight factors is uniformly divided between 0 and 1. Again some remarks can be made:

- We again notice that for small numbers of antenna elements (below 8) the simulated null depth is slightly worse than predicted, which is due to the same reason that the simulated null depth due to phase quantization was slightly worse than predicted: for low numbers of antenna elements, 2 out of N antenna elements with length 1 form a relatively large part, and have a deteriorating effect on null depth.

- Overall the null depth due to both phase and amplitude quantization which is predicted by equation 3.74 shows a good match with the simulations (between $\pm$ 1.8 dB). Differences mainly originate from non-uniform distribution of the modula of the weight factors.

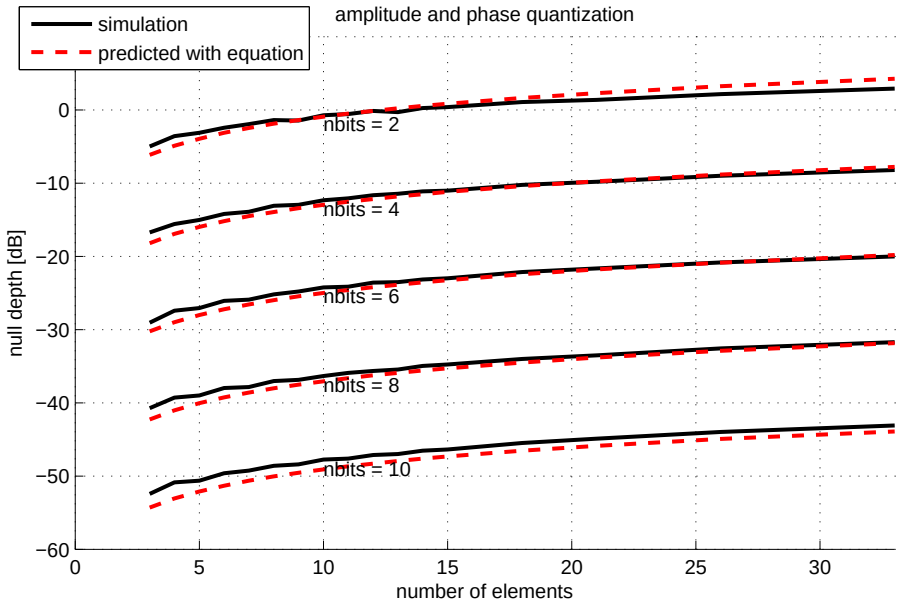


Figure 5.6: Null depth simulated applying both amplitude- and phase quantization.

5.5 Simulating the effect of multiple nulls on null depth

As mentioned before, when combining more nulls one can reach a deeper null. This null depth can be predicted with equation 3.69. To check this equation by simulations, for different numbers of nulls the null depth is simulated. The positions of the nulls are optimized using the procedure of section 5.1.2. An angular uncertainty of ±5 degrees is taken for an interferer on -40 degrees with a bandwidth of 100 MHz. The nominal array frequency is 1.1 GHz.

Figure 5.7 shows a plot of this simulation. The less-steep curve is valid for situations where the *first* weight factor has a modulus that is normalized to 1, because this convention is used to derive equation 3.69. The figure shows the corresponding prediction by equation 3.69, which almost perfectly fits the simulations.

The steeper curve is valid for situations where the *largest* weight factor is normalized to 1. To fit this simulation, equation 3.69 is adjusted with a *steepness-factor* of 1.8. Equation 3.69 now changes to:

$$\begin{aligned} suppr(N_{nulls}) &= 1.8 \cdot 2 \left(\frac{1}{1.8} \cdot 0.5\kappa d \left(|\cos\theta_m| \Delta\theta + |\sin\theta_m| \frac{0.5BW}{f} \right) \right)^{N_{nulls}} \\ &= 3.6 \left(\frac{1}{3.6} \kappa d \left(|\cos\theta_m| \Delta\theta + |\sin\theta_m| \frac{0.5BW}{f} \right) \right)^{N_{nulls}} \end{aligned} \quad (5.5)$$

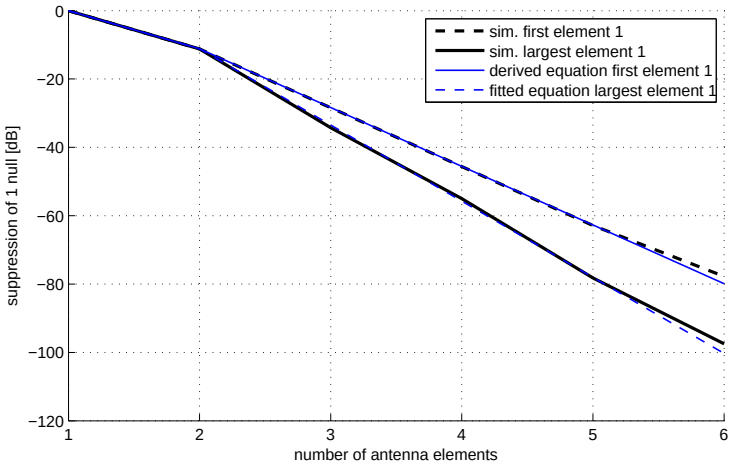


Figure 5.7: Null depth simulated for different numbers of nulls working together. No quantization effects or other unideal factors are assumed.

This formula is also tested for an interferer on different directions than -40 degrees, with similar results. In addition, the formula is tested for smaller and larger angular uncertainties and for different values of interferer bandwidth, also with similar results. In figure 5.7 for very large null depths (around -80 to -100 dB) the simulations give slightly smaller worse results than predicted. This is due to the optimization process that doesn't find infinite accurate null positions but stops when the gradient of the cost function is smaller than a certain (small) value. For very large suppressions this derivative also becomes very small so the algorithm stops earlier, at a slightly sub-optimal point.

Figure 5.8 shows an example of the array factor for the optimum solution of an interferer at 30 degrees with a bandwidth of 100 MHz and an angular uncertainty of ±5 degrees for 6 antenna elements (5 nulls):

5.6 Simulating the effect of minimum size of weight factors on null depth

We know that, because of finite rise and fall times of the LO clock pulse, the minimum gain w_{min} that we can make is larger than 0, for example 0.3. This means that only weight factors with a modulus between 0.3 and 1 can be made.

In order to find out if $w_{min} > 0$ has a negative effect on the SIR (in comparison with $w_{min} = 0$, we will:

1. sweep w_{min} from 0 to 1 in steps of 0.1;

2. for every value of w_{min}, run the optimization algorithm to find the optimum weight factors that are possible;

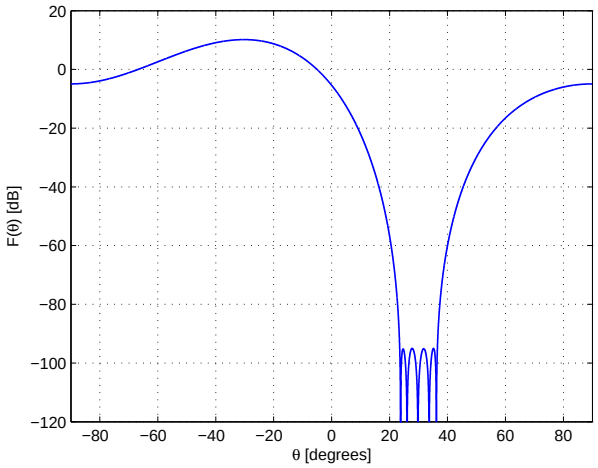


Figure 5.8: Example of array factor for 5 nulls working together to form a very deep null at 30 degrees over an angular range of 10 degrees for a frequency bandwidth of 100 MHz.

3. calculate the corresponding Signal-to-Interferer Ratio (SIR)[1].

We will repeat this procedure for multiple scenarios.

In theory, the following variables determine the maximum SIR for a given w_{min}:

- the angle uncertainty;
- the number of antenna elements N;
- the number of interferers;
- the positions and strengths of these interferers;
- the position and strength of the signal of interest;
- the antenna spacing
- the frequency of interferers

The bandwidth of the interferers can be calculated in terms of position and angle uncertainty of the interferers, therefore is not mentioned in this list. We assume that the *deterioration of SIR* for larger w_{min} is independent of the number of quantization bits (off course the SIR itself *is* dependent on the number of quantization bits). Table 5.1 lists the simulated scenario's, where for every scenario, one of the above mentioned variables is changed, relative to the previous

[1]Any antenna- and frontend noise is not taken into account because this would (for a given scenario) also limit the maximum achievable SINR, so we wouldn't know what part of the limitation in SINR would be due to the constraint w_{min} and what part due to the noise

scenario number	angle uncertainty [degrees]	number of antenna elements	strength signal of interest [dBmV]	position signal of interest [degrees]	strength interferers [dBmV]	position interferers [degrees]
1	10	2	10	-30	30	40
2	10	4	10	-30	30	40
3	20	4	10	-30	30	40
4	10	4	10	-30	30	40
					10	10
					20	75
5	10	4	10	-30	30	-20
					10	-45
					20	-75
6	10	4	10	-55	30	40
					10	10
					20	75
7	10	10	10	-30	30	40
					10	10
					20	75

Table 5.1: Settings for the different scenario's for testing the influence of w_{min}.

scenario. The angle uncertainties (20 degrees for the 3th scenario and 10 degrees for the other scenarios) are chosen quite large because smaller angle uncertainties would give very deep nulls, which makes it more difficult for the optimization algorithm to find the optimum. For the other variables (the number of antenna elements, signal strength etc.) real-world values are chosen. The change in antenna spacing is not simulated because it is equivalent to a change in frequency of interferers.

All signal strengths are given in dBmV, so with respect to 1 mV rms.

The optimum weight factors are approximated by the procedure described in 5.1.2, using the Matlab-function *fmincon*. For every scenario and every value for w_{min} the optimum weight factors are 25 times calculated, each time for different starting values for $\bar{w}$, and the best solution is picked out.

For every scenario, the SIR without and with beamforming are calculated. The difference, the SIR merit, is shown in Figure 5.9 as a function of w_{min}. All simulations are done for 1.1 GHz.

We make some notes:

- For scenario 1 to 6 there is (almost) no decrease in SIR for w_{min} up to 0.3.
- Scenario 1 has no decrease in SIR for large w_{min} because it consists of

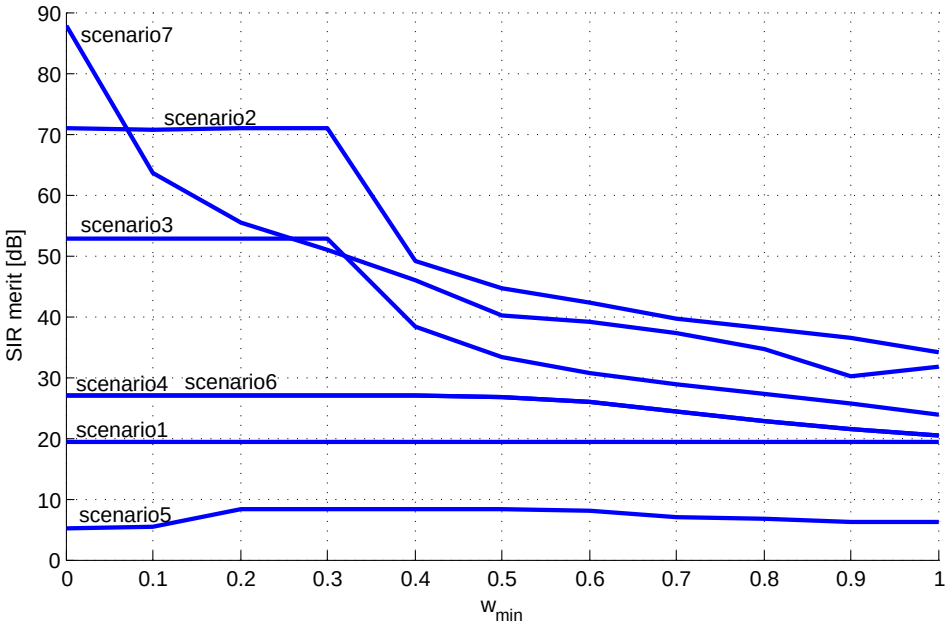


Figure 5.9: SIR merit as a function of w_{min}.

only 2 antenna elements, forming a null. Therefore both antenna elements have to cancel each other into the direction of the interferer so their weight factor modula are always 1.

- Scenario 4 and 6 give almost the same SIR merit, which makes sense because the only thing that differs is the position of the desired signal.

- Scenario 5 has it's interferers placed closely around the desired signal, which makes it harder to suppress the interferers while keeping a strong signal gain. Therefore scenario5 only gives a small improvement (of about 6-7 dB) in SIR. Increasing the number of antenna elements is in this situation a good solution.

- Scenario 7 shows a rapidly decreasing SIR merit for increasing w_{min}. It has on average 3 nulls per interferer, the same as scenario 2. Therefore it gives roughly SIR merits in the same order. For more than 5 antenna elements, the optimization routine finds it hard to find the 'best' solution. Therefore, the SIR merits for this scenario should not be trusted too much.

5.7 Circuit simulations

To demonstrate the working of the final circuit design described in Chapter 4 we do some circuit level simulations. We will show that:

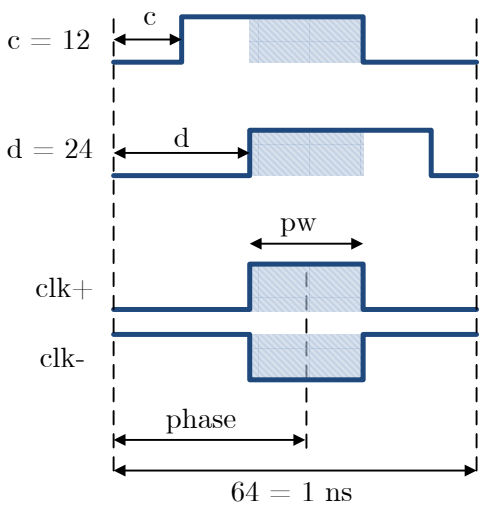


Figure 5.10: Code c and d indicate the delay of both inputs of the NAND gate. The output of the NAND gate gives the synthesized negative LO clock pulse $clk-$ from which $clk+$ is derived.

- the circuit can generate a pulse with a variable phase and variable pulse width;
- phase and conversion gain can be controlled independently;
- phase and conversion gain follow their predicted values.

For the simulations we use the Cadence Virtuoso Front to Back Design Environment version 5.10.41.500.5 including the Spectre Circuit Simulator. The schematic of the final circuit can be found in in Appendix B.

First we note that, although the system is designed to work for frequencies between 500 MHz and 1 GHz, we simulate it on 1 GHz only. Therefore, we don't use the 7th bit (that drives capacitors 8 to 15 inside the analog delay stage). The *delays* of both 50% duty cycle square waves at the inputs of the NAND gate are coded with integers c and d, where $c, d \in [0, 1, ..., 64]$ (see Figure 5.10). 0 corresponds with a delay of 0 ns and 64 corresponds with a delay of 1 full period (1 ns). When we choose $c = d$, both pulses have maximum overlap so a pulse with maximum pulse width is synthesized, giving the maximum possible conversion gain of $\frac{2}{\pi}$.

5.7.1 Constant pulse width, variable phase

First we keep the pulse width of the generated pulse constant at a value of $\frac{20}{64} \cdot 2\pi$. This corresponds to 313 ps and to a conversion gain of $\frac{2}{\pi} \sin\left(\frac{20\pi}{64}\right) \approx 0.530$ (see equation 2.7). We sweep the phase of the synthesized pulse from 0 to 2π. Therefore we substitute a new code x: $c = x$ and $d = x + 12$ and we sweep

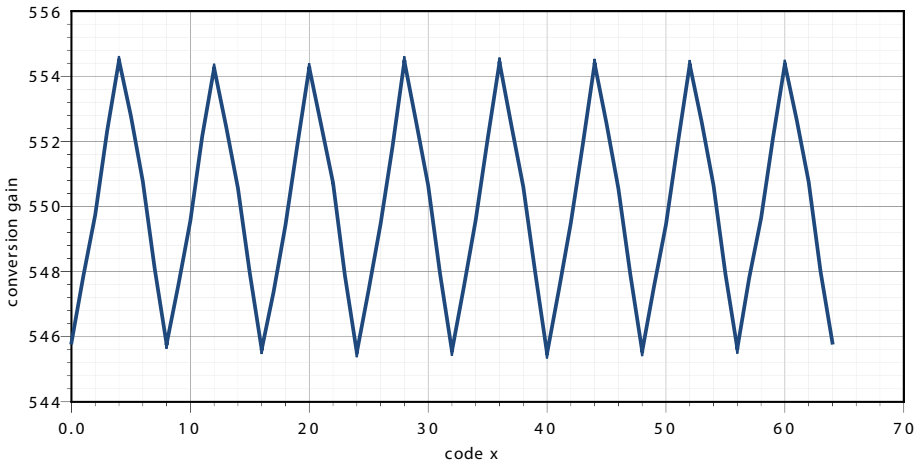


Figure 5.11: Gain of the mixer as a function of phase code, where the phase code is between 0 and 64. Code 0 corresponds to a phase of 0 degrees while code 64 corresponds with 2π degrees.

x from 0 to 64 (refer to Figure 5.10). The pulsewidth with code 20 is chosen because for this pulsewidth the variations in conversion gain are expected to be largest. This is because alternately the rising edge or falling edge will use half the delay of the analog delay block.

On the RF input of the mixer a 1.001 GHz signal is placed, which will be downconverted to 1 MHz. Theoretically the gain should be fixed at 0.530 because because the pulse width stays fixed (or at 0.530 - 1% because of the voltage drop over the switches). The realized gain between the mixers RF input and output is measured and plotted as a function of phase, using a parametric PSS + PAC sweep. The following settings are used: 27 degrees C, PSS Analysis 'Shooting', beat frequency '1 GHz', Number of harmonics '5', Accuracy 'Moderate', New Initial Value For Each Point 'yes', number of Sidebands '5'.

Figure 5.11 shows the resulting Mixer Gain as a function of the phase x. The simulated conversion gain is about 0.550 ± 0.005. The variance in de conversion gain Figure 5.11 (which is about $\pm$ 0.9%) is due to the fact that the analog delay block is still slightly nonlinear, as can be seen by Figure 5.12, where the time delay between for example x=15 and x=16 is slightly smaller than the time delay between x=16 and x=17. This repeats 8 times over the whole range from 0 to 64.

Using the derivative of the sine curve (equation 2.7) we know that at a pulse width of $\frac{20}{64} \cdot 2\pi$ rad 1 LSB step in pulse width corresponds with a conversion gain step of 0.018. So the variation in conversion gain is $\pm$ 28 % significantly of 1 LSB step. Figure 5.13 shows the derivative of the realized phase shift. On average it follows exactly the theoretical value of $\frac{360}{64} = 5.625$ degrees per code step. More interestingly is the deviation in the number of degrees per clock step,

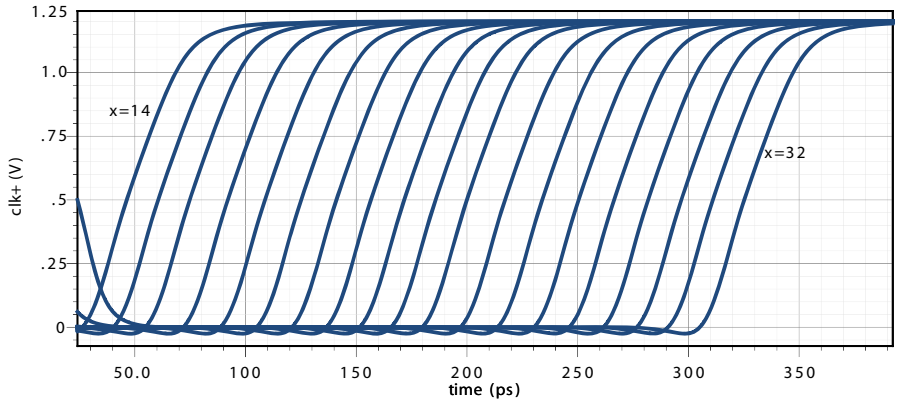


Figure 5.12: clk+ plotted for x=14 to x=32, showing slightly nonequal time steps

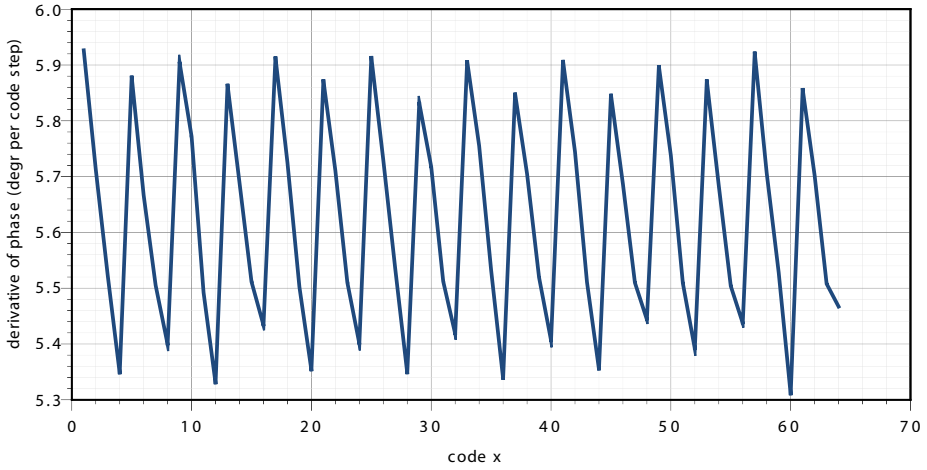


Figure 5.13: Derivative of the phase shift to code x, realized with the mixer as a function of x

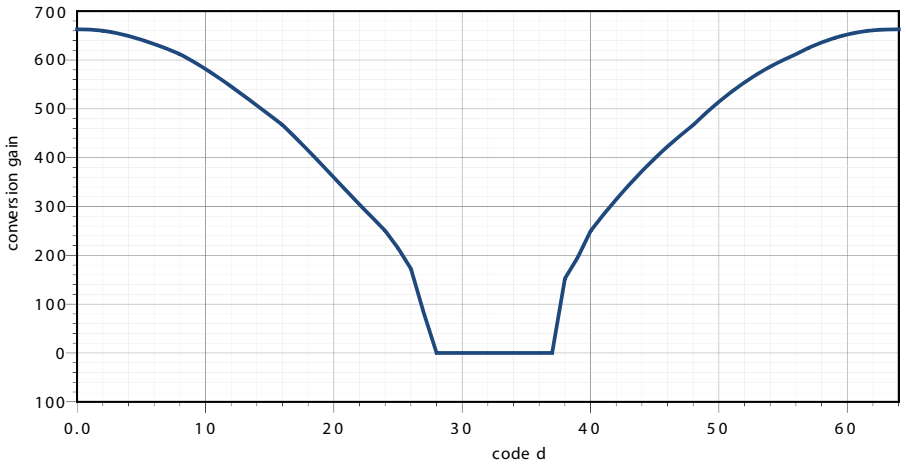


Figure 5.14: Gain of the mixer as a function of d where *pulse width* $= |32 - d|$

which can again be attributed to the slightly nonlinear analog delay stage. The maximum deviation of the steps is ± 5.2 % of 1 step for the simulated pulsewidth of $\frac{20}{64} \cdot 2\pi$ rad.

5.7.2 Constant phase, variable pulse width

The same simulation is done for keeping the rising edge constant (at $c = 0$) and sweeping the falling edge (d) from 0 to 64.

Figure 5.14 shows the resulting mixer gain as a function of d, measured on the mixer output with respect to the mixer input. It has it's maximum at $d = 0$ and $d = 64$ because the pulses from both branches then have maximum overlap. In order to compare this simulation with the sine-curve, we interchange the left and right halve. Figure 5.15 shows the ideal and simulated sine curves. Here the sine curve is scaled in amplitude to fit the simulated curve. For a pulse width of 8 or more ($|d - 32| \leq 8$) the mixer gain follows the expected sine curve within 12% of 1 LSB gain step. Gains between $\sin(\pi \cdot \frac{8}{64}) \approx 0.38$ and 1 (where the maximum gain is normalized to 1) can be made with this circuit. A pulse width of 8 corresponds with $\frac{8}{64} \cdot 1000$ ns $= 125$ ps.

The effect that the gain goes toe 0 for small pulse widths originates from the fact that small pulse widths are not able to propagate through inverter-chain that drives the switches (or are not able to be generated by the NAND gate at all). Measured on $clk+$ and $clk-$, 83ps is the smallest pulse width that comes through the inverter-chain that drives the switches.

5.7.3 Power consumption of the circuit

The power consumption of the entire designed circuit (as shown in Appendix B) is about 1.52 mA and appears to be almost independent on the shape of the

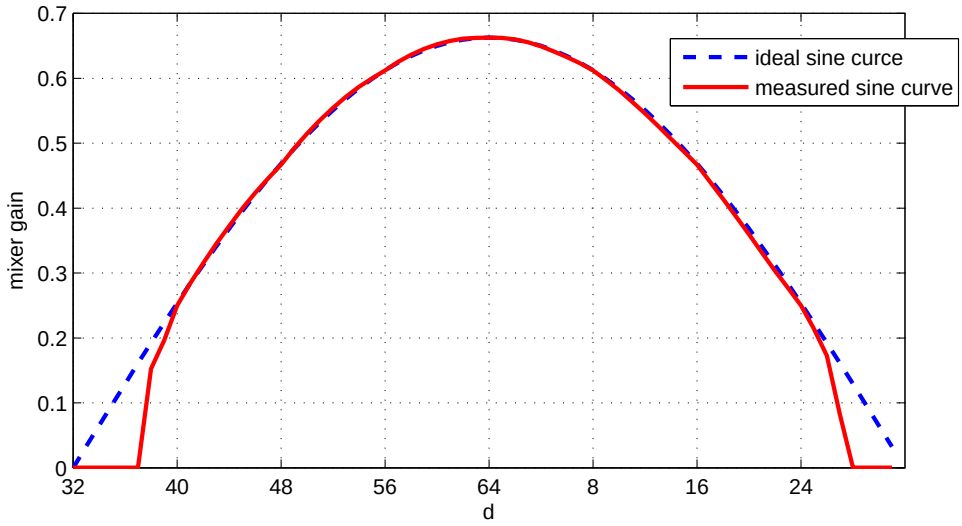


Figure 5.15: Gain of the mixer compared with an ideal sine curve

generated clock. It can be seen in Figure 5.16. The inverters that drive the switches are the most power consuming, because they drive the largest loads in the circuit.

5.7.4 Frequency of the LO clock

The designed system is able to synthesize a clock between 500 MHz and 1 GHz with 6 bits precision (at 500 MHz this becomes 7 bits precision). The inverters that drive the mixer are the bottleneck for speeding up the design, because they limit the minimum possible pulse width to about 80 - 125 ps[2]. The shift registers now runs at 4 GHz but can be speeded up to 8 GHz. The analog delay block also can be speeded up. A possible solution to the problem of the minimum pulse width through the inverters is proposed in Chapter 6.

5.8 Summary

- Equation 3.74 gives a good approximation of the expectation of the maximum null depth due to phase and amplitude quantization, for the case where the modula of the weight factors of all antenna elements are approximately uniformly distributed on the interval between 0 and 1.
- Equation 5.5 gives a good prediction of the maximum null due to the angular uncertainty and bandwidth of the interferers, for a given number of nulls working together.

[2]the smallest measured pulse width through the inverters is 83 ps but pulse widths of 125 ps or larger start to give a gain that follows the sine-curve accurately

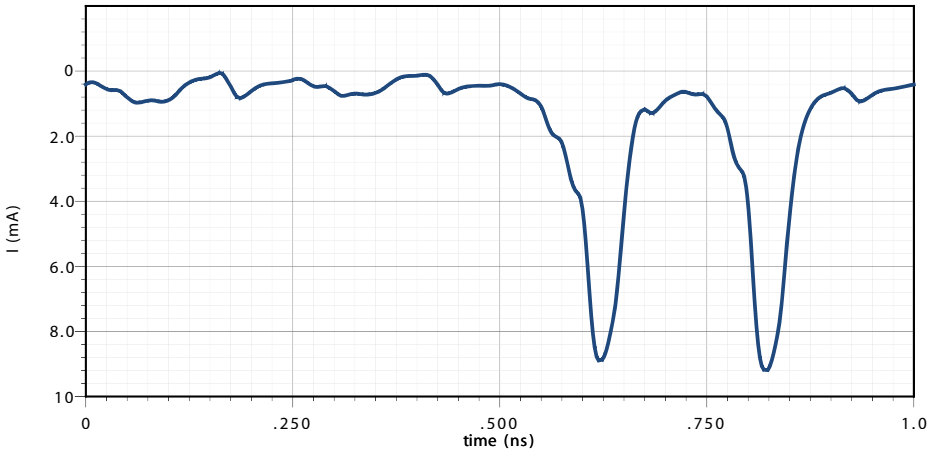


Figure 5.16: Current through the 1.2 V power supply during one clock period

- A constraint on the minimum of the weight factors (called w_{min}) certainly gives a negative effect on the maximum achievable SIR, but for $w_{min} \leq 0.3$ this effect appears to be very minimal, at least for 2-4 antenna elements. For 10 antenna elements there appears to be a significant decrease in SIR.
- The circuit designed in Chapter 4 can generate a pulse with a variable phase and variable pulse width. Phase and pulsewidth can be controlled independently.
- With the current circuit, the effect of phase on conversion gain is very low with ± 28% of 1 LSB phase step.
- The conversion gain follows the predicted sine curve within ± 12% of 1 LSB gain step for gains between 0.24 and $\frac{2}{\pi}$ (equivalent to gains between 0.38 and 1).

Chapter 6

Conclusions and recommendations

6.1 Conclusions

For a beamforming system that applies amplitude and phase adjustment by a passive mixer through adjustment of the pulse width and phase of the LO, the following conclusions can be drawn:

- The null depth is limited by the timing quantization with which the LO clock is synthesized. For a timing resolution of $\frac{1}{2^{n_{bits}}}$ of a LO clock period and under the assumption that the modula of the weight factors are uniformly distributed between 0 and 1, the maximum achievable null depth (compared to a single antenna) can be approximated with the equation

$$nd_q \approx \frac{\pi\sqrt{\pi N}}{2\sqrt{6}\cdot 2^{n_{bits}}} \tag{6.1}$$

  where N is the number of antenna elements.

  Note that although the null depth decreases for more antenna elements, the achievable SINR get better, because for more antenna elements higher gains can be reached into the direction of interest. In addition, with more antenna elements, there are more nulls available to be combined into one deeper null.

- The null depth is also limited by the angular uncertainty $\Delta\theta$ [rad] with which the direction of the interferer is known, by the bandwidth BW of the interferer [Hz] and by the number of nulls N_{nulls} that is 'working together'. The following equation describes this relation quantitatively:

$$nd_b \approx 3.6\left(\frac{1}{3.6}\kappa d\left(|\cos\theta_m|\Delta\theta + |\sin\theta_m|\frac{0.5BW}{f}\right)\right)^{N_{nulls}}, \quad N_{nulls} \geq 1 \tag{6.2}$$

Here $\kappa = \frac{2\pi f}{c}$, $c = 3 \cdot 10^8$, f is the frequency of the interferer [Hz], θ_m is the direction of the interferer [rad], $\Delta\theta$ is the angular uncertainty into one direction (where the total angular uncertainly is $2\Delta\theta$) and d is the antenna spacing [m].

Nulls can be made 'deeper' by adding more antenna elements, up to the depth determined by the timing resolution. Lower null depths are not possible, except by redesigning the circuit with better timing resolution.

- Based on equation 6.1, for null depths of -20dB and for 8 or less antennas, at least 5 bits timing quantization is needed ($n_{bits} = 5$).

- Simulations show that in cases where there is a constraint on the minimum of the modula of the weight factors (w_{min}), up to values of 0.3 (with respect to a maximum modulus of 1) this constraint seems to have low influence on the SIR merit[1]. A w_{min} larger than 0.3 leads to a significant decrease in SIR merit in most cases. This decrease in SIR merit is worse for situations with a lot of antenna elements and for large values of SIR merit. In all simulated cases, at least 50% of the SIR merit is left after imposing a constraint w_{min} of 0.4 or smaller.

A circuit for generating a LO clock with a variable phase and pulse width is designed in CMOS 65 nm technology, able to downconvert signals of 500 MHz to 1 GHz. The proposed circuit is able to make gains between 0.38 (at 1 GHz) and 1 and phase shifts between 0 and 360 degrees. The gain error is ±12% of 1 LSB gain step and the phase error is ±28% of 1 LSB phase step. Although theoretically 5 bits are enough for 20 dB null depth with 8 antenna elements or less, the circuit is designed with 6 bits at 1 GHz to (partly) compensate for amplitude and phase errors due to mismatch. The minimum gain is limited by the smallest pulse width that can be generated.

From these observations, the following conclusion can be drawn:

- Although simulations performed in this work indicate that gains down to 0.3 are necessary to maintain the null depth of -20 dB, these simulations are done for a limited number of scenarios and, in addition, a way to (almost) get rid of this constraint on the minimum gains is proposed in the next section. Therefore we conclude that a beamforming system based on mixers using LO clocks with variable phase and pulse width to implement amplitude and phase adjustment, able to suppress interferers at least 20 dB, seems feasible.

[1]The SIR merit is the *increase* in SIR after beamforming is applied, with respect to a single antenna where no beamforming is applied.

6.2 Recommendations and future work

Some recommendations can be made for improving nulling performance and clock speed of the proposed circuit:

- More thorough research is necessary to find a reliable quantitative indication of performance loss due to a constraint on the minimum of the modula of the weight factors (w_{min}). For example, more scenarios can be simulated, the reliability of the optimization algorithm for larger numbers of antenna elements can be improved and a mathematical investigation of this problem of performance loss can be considered.

- To be able to speed up the design *and* to get rid of the w_{min} constraint, a possible solution for the 'slow' inverter chains (limiting the minimum clock pulse width) is to perform the AND-function (see section 4.1) inside the mixer, using a cascade of 2 switches in stead of 1 switch. The AND-function is performed because the mixer will only pass the RF signal when both switches are 'on'. The benefit of this topology will be that the inverter chains only have to handle square waves with 50% duty cycle in stead of pulses with very small pulse widths.

- Although the proposed circuit is designed for low jitter and has 6 bits in stead of 5 bits (to compensate for the loss of performance due to mismatch) the circuit is not checked on jitter due to mismatch. Most digital parts of the circuit currently are (almost) minimum-size MOSTs, but these parts can be upscaled to meet the necessary mismatch requirements. We don't expect this to give a significant increase in power consumption because the only parts that dissipate by far the most power (the inverters driving the mixer switches) probably don't have to be upscaled because they already are large.

- In this work, a standard balanced mixer is used for simulations. But, in principle, any switching mixer can be used as long as it is linear enough for canceling strong interferers. A good candidate is the mixer described in [12], which is very linear and uses harmonic rejection.

Appendix A

Variance of products of stochastic variables

Note: $E\{X\}^2$ means $(E\{X\})^2$ Note: for independent random variables X and Y, $E(XY) = E(X)E(Y)$.

$$\begin{aligned} Var(XY) &= E\{XY - E(XY)\}^2 \\ &= E\{X^2Y^2 + E\{XY\}^2 - 2XY \cdot E\{XY\}\} \\ &= E\{X^2Y^2\} + (E\{X\}E\{Y\})^2 - 2E\{XY\}E\{XY\} \\ &= E\{X^2\}E\{Y^2\} + (E\{X\}E\{Y\})^2 - 2E\{XY\}E\{XY\} \end{aligned} \quad \text{(A.1)}$$

Now we try to find an expression of $E(Q^2)$ in terms of $Var(Q)$ and $E(Q)$, which we can use for equation A.1 to express $E\{X^2\}$ and $E\{Y^2\}$:

$$\begin{aligned} Var(Q) &= E\{(Q - E\{Q\})^2\} \\ &= E\{Q^2\} + E\{Q\}^2 - 2E\{QE\{Q\}\} \Rightarrow \\ E\{Q^2\} &= Var(Q) - E\{Q\}^2 + 2(E\{Q\})^2 \\ &= Var(Q) + E\{Q\}^2 \end{aligned} \quad \text{(A.2)}$$

Applying this rule on $E\{X^2\}$ and $E\{Y^2\}$ in equation A.1 yields:

$$\begin{aligned} Var(XY) &= (Var(X) + E\{X\}^2)(Var(Y) + E\{Y\}^2) + (E\{X\}E\{Y\})^2 - 2E\{XY\}E\{XY\} \\ &= Var(X)Var(Y) + Var(X)E\{Y\}^2 + Var(Y)E\{X\}^2 \end{aligned} \quad \text{(A.3)}$$

Using this result we can find $Var(XYZ)$, which is:

$$\begin{aligned} Var(XYZ) = {} & Var(X)Var(Y)Var(Z) + Var(X)E\{Y\}^2Var(Z) \\ & + Var(Y)E\{X\}^2Var(Z) + Var(X)Var(Y)E\{Z\}^2 \\ & + Var(X)E\{Y\}^2E\{Z\}^2 + Var(Y)E\{X\}^2E\{Z\}^2 \\ & + Var(Z)E\{X\}^2E\{Y\}^2 \end{aligned} \quad \text{(A.4)}$$

Appendix B

Schematic of the final clock generation circuit

parameter	value	short description
wid0	0.491 µm	width of MN7 in analog delay block for tweaking analog delay
wid2	0.280 µm	width of MP18 in analog delay block for tweaking analog delay
W2	2 µm	width of switches in analog delay
cap	7 fF	capacitance in analog delay
p	1 ns	period time of generated wave
c	0 ... 64	integer indicating delay of rising edge of synthesized clock
d	0 ... 64	integer indicating delay of falling edge of synthesized clock

Table B.1: Variables used in the final design

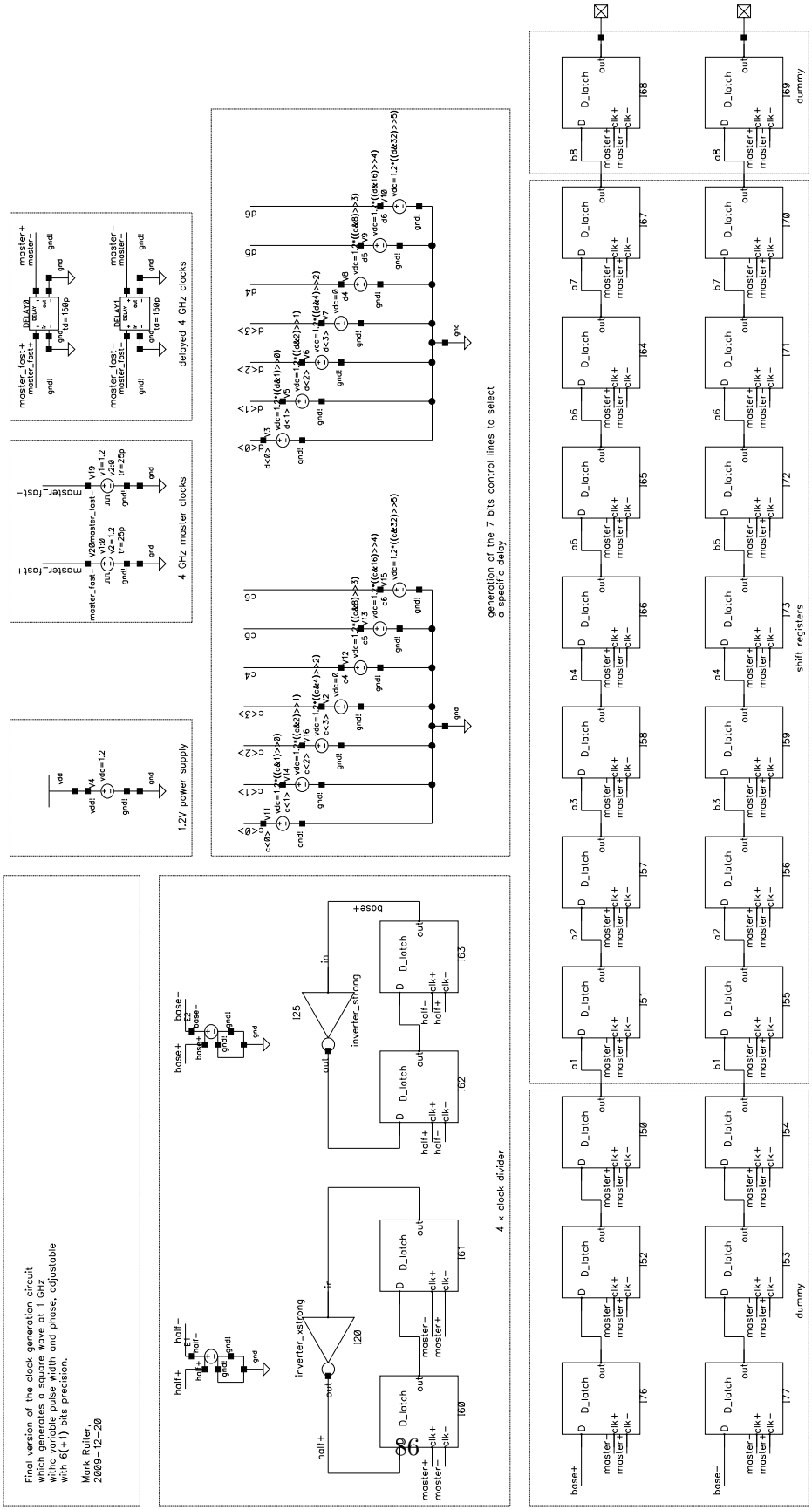


Figure B.1: Main schematic, part 1 of 2.

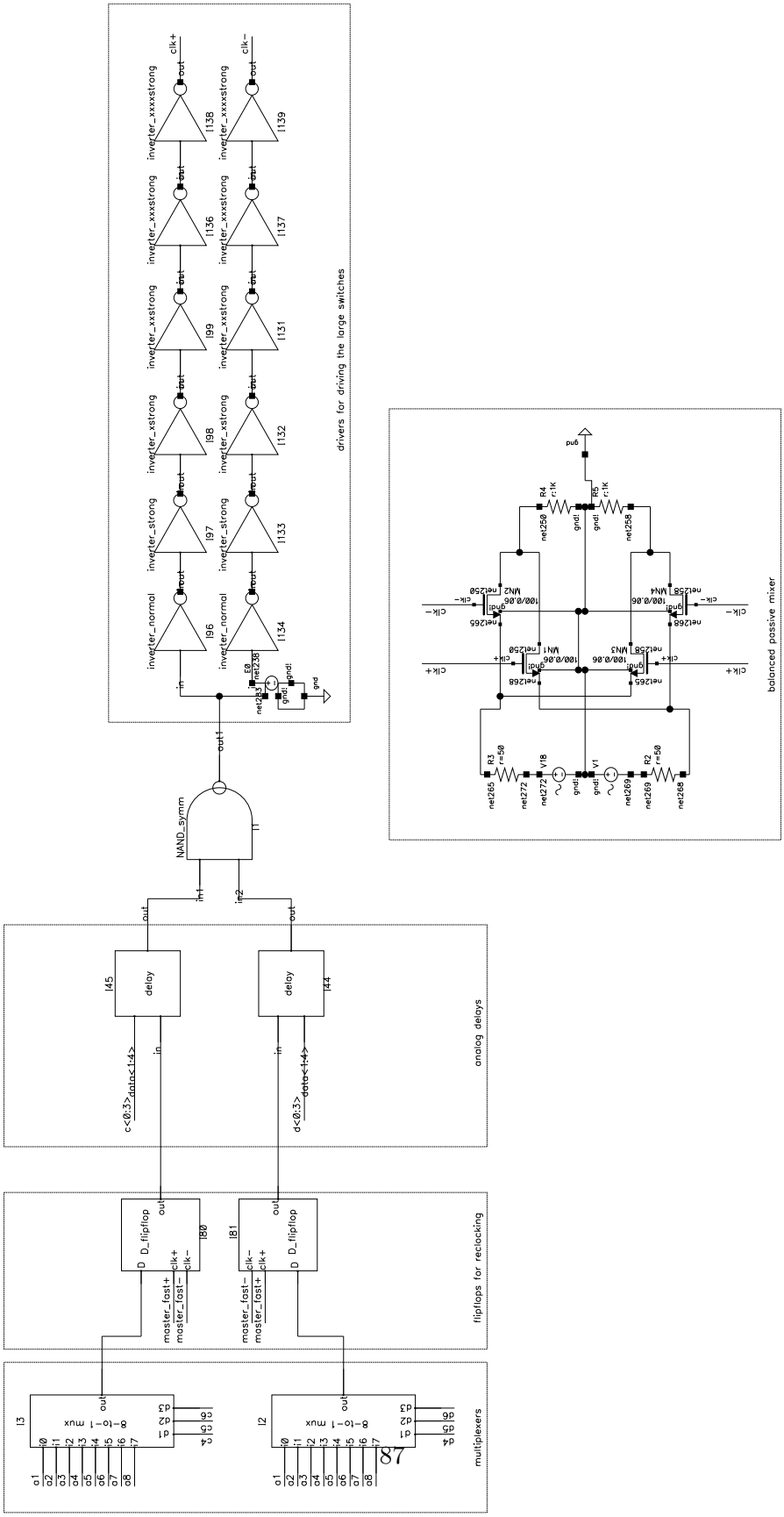
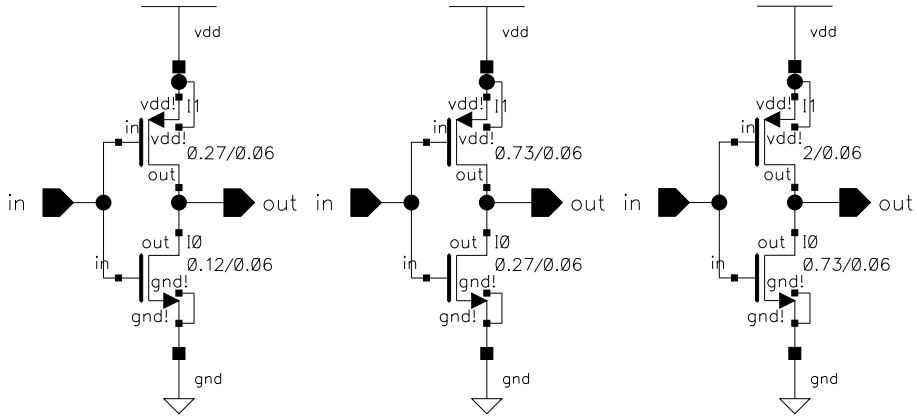
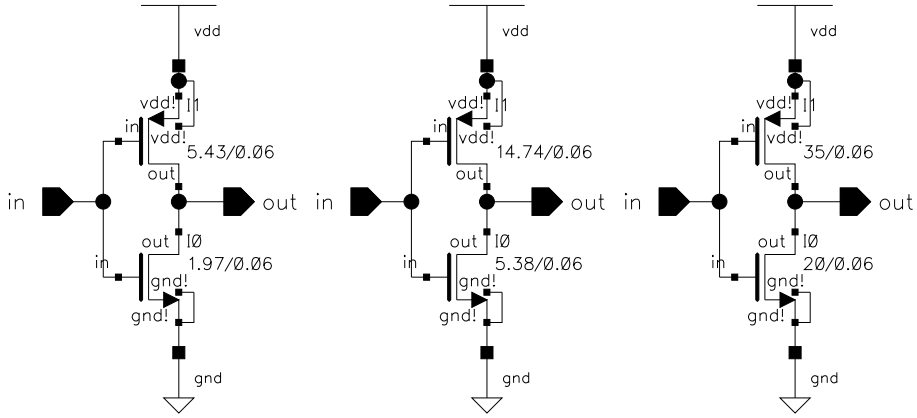


Figure B.2: Main schematic, part 2 of 2.



(a) inverter_normal (b) inverter_strong (c) inverter_xstrong



(d) inverter_xxstrong (e) inverter_xxxstrong (f) inverter_xxxxstrong

Figure B.3: Inverters

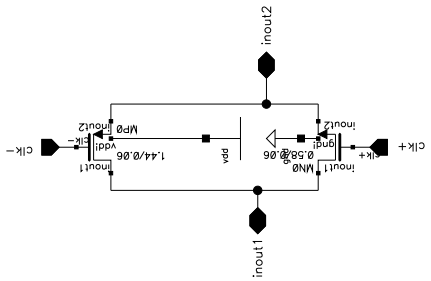


Figure B.4: transm_gate_strong

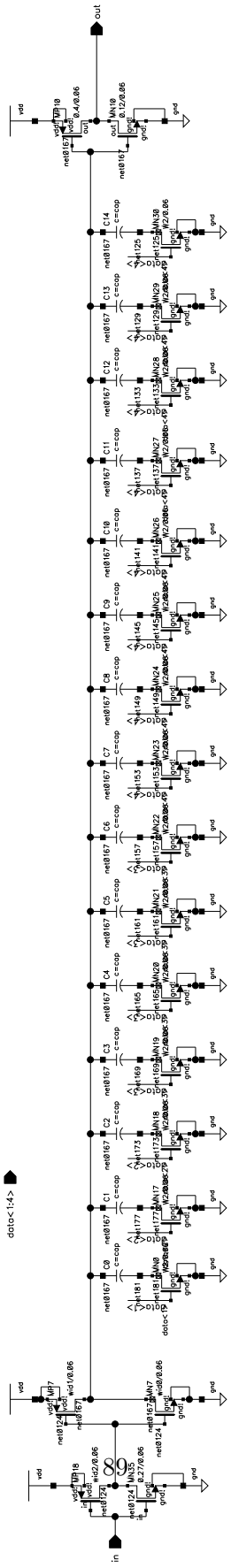


Figure B.5: delay

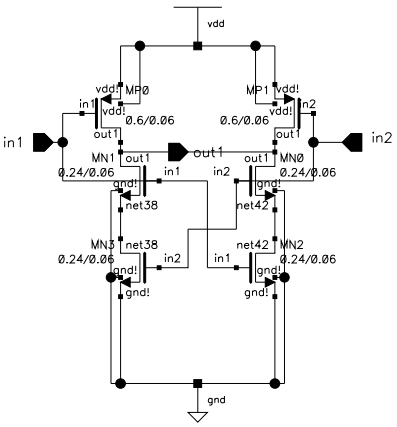


Figure B.6: NAND_symm

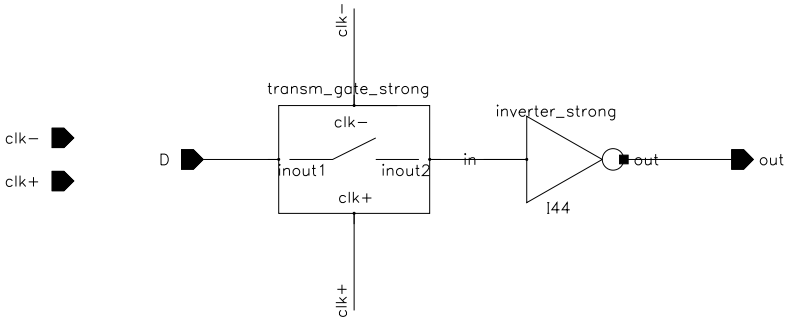


Figure B.7: D_latch

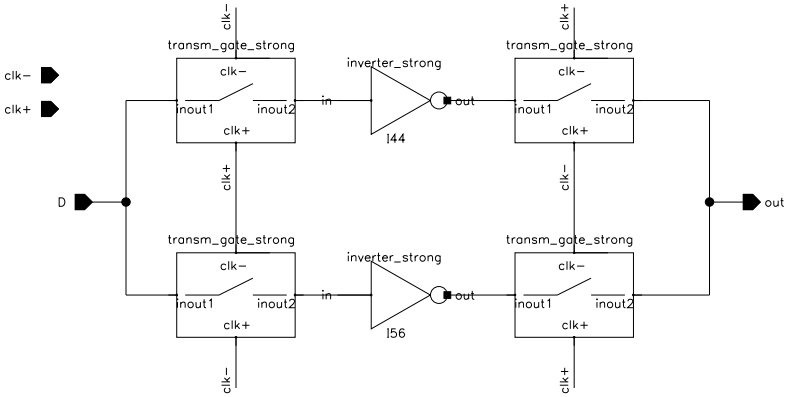


Figure B.8: D_flipflop

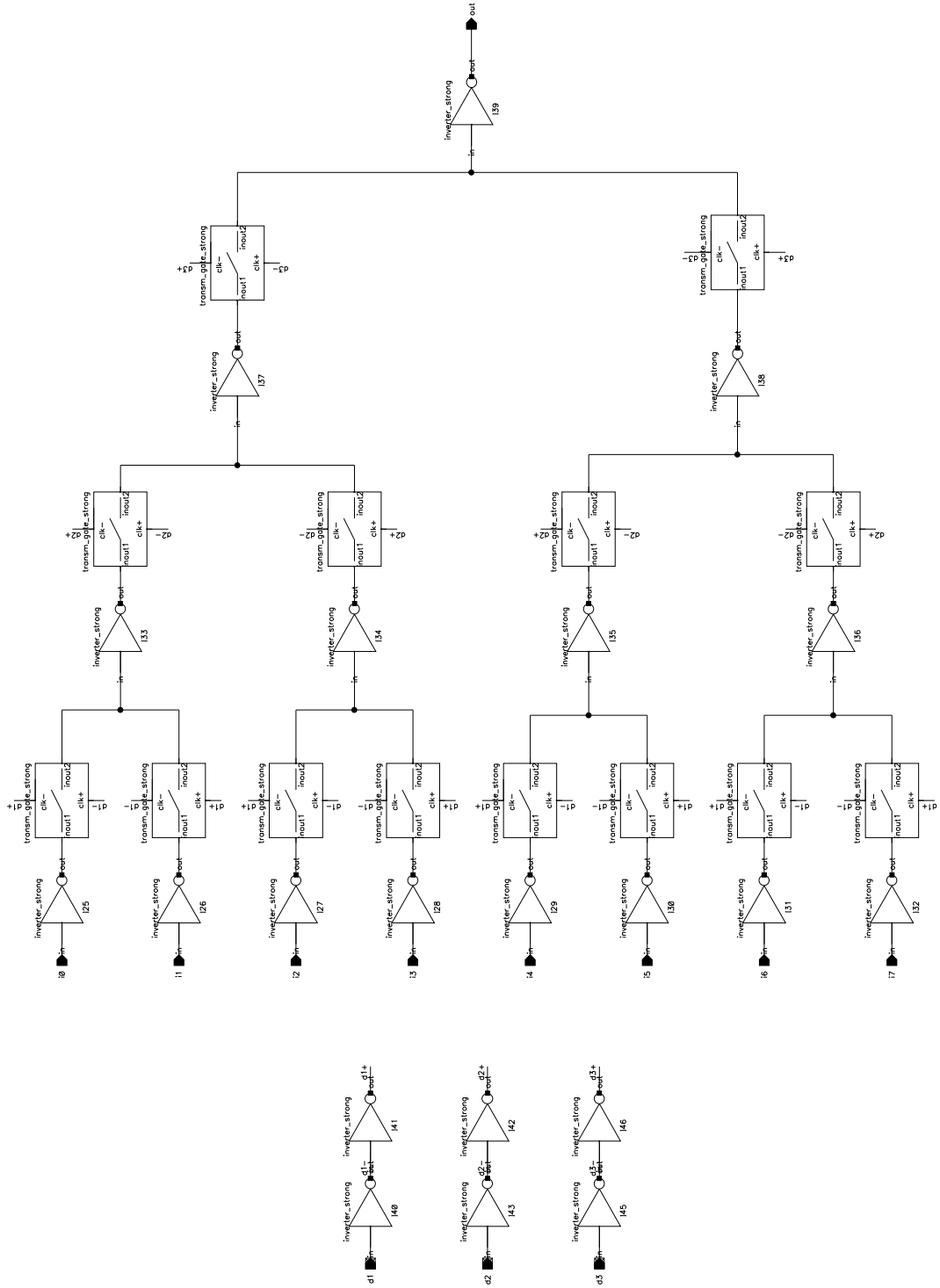


Figure B.9: 8-to-1 multiplexer

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