University of Twente
The Netherlands

Low series resistance structures for gate dielectrics with a high leakage current

by M.P.J. Tiggelman

Master Thesis

Report number: 068.031
July 19, 2005

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Prof.dr. J.Schmitz
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Abstract

Over the succession of chapters, this master thesis describes:

1. *the consequences of the gate oxide shrinkage on electrical device characterization,*

   A major issue concerns the large tunneling currents through the oxide and a relatively high value of the series resistance. Reciprocally, these parameters are related to the device performance.

2. *the approach to successfully handling these issues,*

3. *a solution that should allow an accurate characterization.*

   Radio frequency (RF) test structures are designed from which a capacitance-voltage (C-V) curve can be obtained. Electrical device parameters can be extracted from the intrinsic RF C-V curve by using a simulation model.

Contents

List of Acronyms

Al_2O_3	Aluminum oxide
C-V	Capacitance-voltage
CMOS	Complementary metal-oxide semiconductor
DUT	Device under test
EOT	Equivalent oxide thickness
GSG	Ground-signal-ground
HF	High frequency
ISS	Impedance standard substrate
LRL	Line-reflect-line
LRM	Line-reflective-match
LRRM	Line-reflect-reflect-match
MOS(FET)	Metal-oxide semiconductor field effect transistor
NMOS	Negative-channel metal-oxide semiconductor
NQS	Non-quasistatic effect
Q	Quality factor
QS	Quasistatic
RF	Radio frequency
SiO_2	Silicon dioxide
SMU	Standard measurement unit
SOLT	Short-open-load-thru
TiN	Titanium nitride
TRL	Thru-reflect-line
VNA	Vector network analyzer

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Introduction

Since the invention of the metal-oxide-semiconductor field effect transistor (MOSFET) and the integrated circuit (IC) in the 1960's, the pace in which technology is set to market is very high. Continuous development on IC's is often focused on increasing the functionality, the number of components per area, energy efficiency, reliability and speed, at a lower cost. Over time, technology advancements create opportunities for researchers to decrease device dimensions. The International Technology Roadmap for Semiconductors (ITRS) [1] outlines the milestones of the device nodes for the IC technology industry.

One of the device parameters is the equivalent oxide thickness (EOT) of the gate of a MOSFET. The EOT is used to compare the performance of high-κ and SiO_2 based gate oxides. If the capacitance value is constant, high-κ gate oxides are physically thicker than an SiO_2 layer, causing less gate leakage current. High-κ gate oxides form only a temporary solution of the gate leakage problem.

Accurate physical parameter extraction by electrical characterization can be obstructed by a large leakage current. A capacitance roll-off is visible in the capacitance-voltage (C-V) curve at low frequencies. The frequency has to be increased, to overcome this unwanted effect [2]. Performing measurements at microwave frequencies offers a solution. Measurements at these frequencies fall into the category of radio frequency (RF) measurements.

This research elaborates on the work of M.A. Negara [3], and indicates how a test structure could be made for leaky gate dielectrics, that should give a reliable assessment of the electrical parameters by following certain design rules.

The goal of this research is:

1. To examine once more if such feasible design can be made, coping with the restrictions of the equipment available at the MESA+ research

institute.

2. Designing the test structures.

3. Proving the validity of the device performance by RF C-V measurements after fabrication.

The upcoming chapters describe the progress of this research. The chapters discuss the gate leakage current, the theory behind RF C-V measurements, the design aspects and the experimental results respectively.

Chapter 1

Gate leakage current

The integrity of the gate oxide of a MOS structure is of crucial importance for the lifetime of a device and for it to function correctly. An electric field will be present in the oxide layer if a gate voltage is applied. Charge carriers will tunnel through the oxide and will cause a leakage current. If small or moderate voltages are used the gate current will be negligible. At high electric fields in the oxide, the gate current can become substantial. This will be clarified in section 1.1.

The electric field in the oxide [4]

$$E_{\text{ox}} = \frac{V_{\text{ox}}}{t_{\text{ox}}}, \tag{1.1}$$

with the potential across the oxide

$$V_{\text{ox}} = V_{\text{gate}} - V_{\text{fb}} - \phi_{\text{s}}, \tag{1.2}$$

with the flatband voltage V_{fb} and ϕ_{s} the silicon surface potential.

1.1 Equivalent Oxide Thickness (EOT)

The equivalent oxide thickness (EOT) is the thickness of an SiO_2 film that gives the same capacitance value as that obtained from the thickness of a high-κ dielectric. The relation between the SiO_2 thickness, a high-κ metal-oxide and the EOT is expressed by:

$$EOT = t_{\text{ox,high-}\kappa} \cdot \frac{\varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{high-}\kappa}} + t_{\text{inteface layer}} \;=\; t_{\text{ox,high-}\kappa} \cdot \frac{\varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{high-}\kappa}} + t_{\text{SiO}_2} \tag{1.3}$$

In this research, the high-κ dielectric Al_2O_3 is used as the gate oxide. An interface layer of e.g. SiO_2 can be present besides Al_2O_3. In the previous equation SiO_2 is used as the interface layer.

Due to scaling of MOS devices, the *EOT* reduces nearly every year. With a constant *EOT*, a high-κ oxide layer is thicker compared to an SiO_2 layer. The thicker layer makes it more difficult for charge carriers to tunnel through the oxide, so the leakage current will decrease. As already was pointed out, high-κ oxide materials are only a temporary solution to solve gate leakage problems.

The *updated* 'ITRS roadmap 2004' indicates the expected milestones for the *EOT* and the gate leakage current. The values for the years ahead are shown in table 1.1.

Year of production	**'05**	**'06**	**'07**	**'08**	**'09**
EOT for low operating power [nm]	1.4	1.3	1.2	1.1	1.0
Nominal J_{gate} [A/cm^2]	2.22	2.70	5.21	5.95	6.67
EOT for high operating power [nm]	1.1	1.0	0.9	0.8	0.8
Nominal J_{gate} [A/cm^2]	520	600	930	1100	1200

Table 1.1: The prediction of the updated ITRS roadmap 2004 for the *EOT* for low and high operating power for the next four years. The gate leakage current density J_{gate} is indicated when $T = 25$ °C.

In table 1.2 the thickness of the Al_2O_3 gate oxide is shown for the next four years, assuming that the gate oxide solely consists of Al_2O_3, and that the dielectric constants $\varepsilon_{Al_2O_3} = 9$ and $\varepsilon_{SiO_2} = 3.9$.

Year of production	**'05**	**'06**	**'07**	**'08**	**'09**
t_{ox} for low operating power [nm]	3.23	3.00	2.77	2.54	2.31
t_{ox} for high operating power [nm]	2.54	2.31	2.08	1.85	1.85

Table 1.2: The prediction of the updated ITRS roadmap 2004 for the t_{ox} of Al_2O_3 for low and high operating power for the next four years.

1.2 Tunneling mechanisms

Two tunneling mechanisms are investigated: Fowler-Nordheim (FN) and direct tunneling (see figure 1.1). Direct tunneling dominates at low gate voltages, while FN tunneling is significant at higher operating voltages. The band offsets of an Al_2O_3 gate oxide indicates that the tunneling current is primarily caused by electrons, since the conduction band offset is 2.8 eV and the valence band offset is 4.9 eV [5].

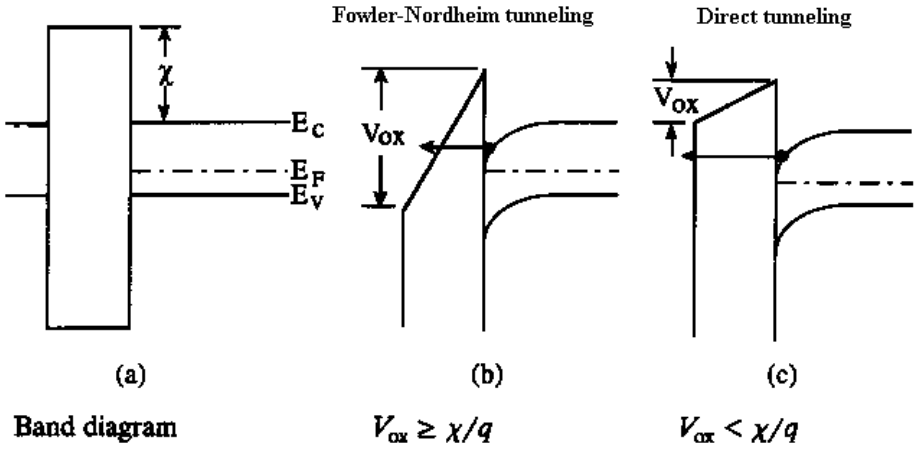

Figure 1.1: a) A banddiagram of a MOS structure with a p-type substrate, b) Fowler-Nordheim tunneling, and c) direct tunneling.

In this research only *p*-type substrates are used.

Direct tunneling

Direct tunneling means the flow of electrons goes directly from the silicon substrate through the Al_2O_3 to the positive charged electrode in inversion. In accumulation, the main current flow of electrons travel from the negatively charged electrode to the more positively charged silicon substrate. The direct current density is expressed by [6]

$$J_{\mathrm{DIR}} = \mathrm{A} \cdot E_{\mathrm{ox}}^2 \cdot \exp\left(\frac{-\mathrm{B}[1-(1-q \cdot V_{\mathrm{ox}}/\Phi_{\mathrm{b}})^{1.5}]}{E_{\mathrm{ox}}}\right) , \tag{1.4}$$

with

$$\mathrm{A} = 1.54 \cdot 10^{-6} \cdot (\frac{1}{\mathrm{m}^{*}\Phi_{\mathrm{b}}}) \tag{1.5}$$

and

$$\mathrm{B} = 6.83 \cdot 10^{7} \cdot (\mathrm{m}^{*})^{2} \cdot (\Phi_{\mathrm{b}})^{1.5}, \tag{1.6}$$

with the constant A in [A/V^2], constant B in [V/cm], the effective mass for an electron $\mathrm{m}^{*}(\mathrm{Al_2O_3}) = 0.23$ and the barrier height $\Phi_{\mathrm{b}}(\mathrm{Al_2O_3}) = 2.8$ eV [6].

Fowler-Nordheim tunneling

If a high electric field exists in the gate oxide, the tunneling of charge carriers through the oxide is facilitated. Electrons go through the silicon conduction band into the conduction band of the gate oxide, and will flow through the triangular shaped potential barrier. The FN tunneling current is described by:

$$J_{\mathrm{FN}} = \mathrm{A} \cdot E_{\mathrm{ox}}^{2} \cdot \exp(\frac{-\mathrm{B}}{E_{\mathrm{ox}}}) \tag{1.7}$$

Total gate current

According to Schroder [4] the total gate current density in the oxide is determined by adding both current densities

$$J_{\mathrm{GATE}} = J_{\mathrm{DIR}} + J_{\mathrm{FN}} \tag{1.8}$$

The total gate current, given as the sum of both tunneling mechanisms, is visualized for $\mathrm{Al_2O_3}$ in figure 1.2, for $t_{\mathrm{ox}} = 4$, 3 and 2 nm. The highest current density dominates except when $J_{\mathrm{DIR}} = J_{\mathrm{FN}}$.

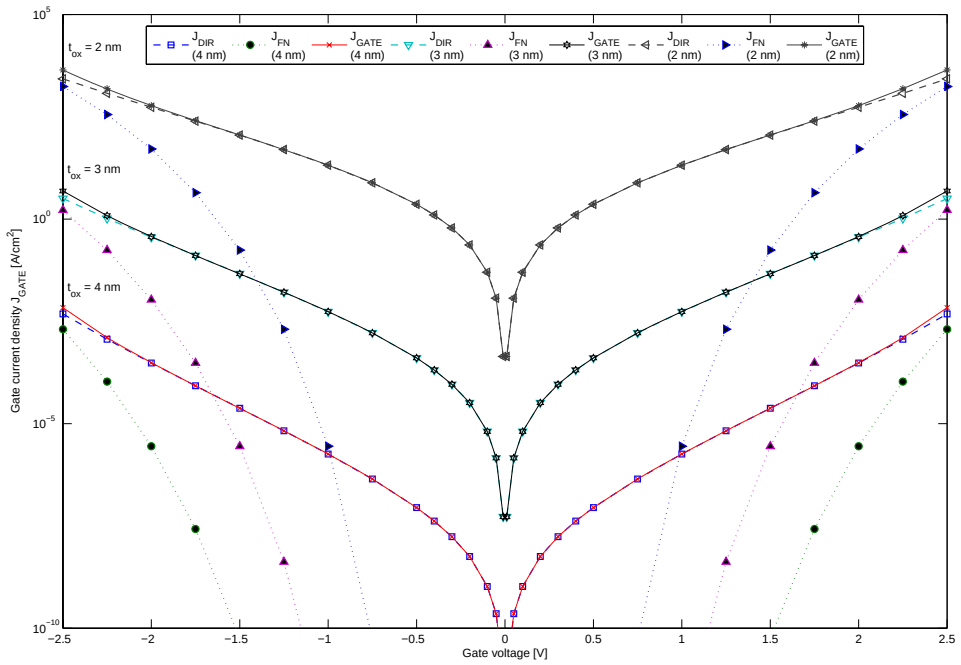

Figure 1.2: Model: Direct, FN and total gate tunneling current density vs. the gate voltage for Al_2O_3 with oxide thicknesses of t_{ox} = 4, 3 and 2 nm. The plot shows the direct tunneling dominates in the low voltage range.

The figure shows the exponential increase in gate leakage current for smaller dielectric thicknesses. To cope with high leakage currents, the measurement frequency has to be increased. RF test structures have been designed that should give a complete and accurate C-V curve.

Chapter 2

Theory RF C-V

In this chapter the theory of RF C-V measurements is discussed. It is divided in sections that discuss the scattering parameters, the measurement equipment, calibration techniques, the de-embedding technique and the three-element model.

Some of the equations in this report use physical constants or parameters that stay constant after calculation or assumptions. The constants are mentioned in table II in appendix B.

2.1 Scattering parameters

At RF frequencies the current and voltage laws of Kirchhoff are not always applicable anymore, when the frequencies are too high. Kirchoff does not take into account the influence of electrical and magnetic fields [7]. The boundary condition of using the laws of Kirchoff indicate that the wavelength λ must be much smaller then the size of the device. When a two-port environment is used the difficulty arises that accuracy is lost by the influence of the probe and the bidirectional path of waves. The use of scattering parameters or S-parameters offers the solution. These parameters can give the gain, loss and reflection by measuring the magnitude and phase of the transmitted, reflected and incident waves on the ports.

The S-parameter two-port scheme is visualized by figure 2.1.

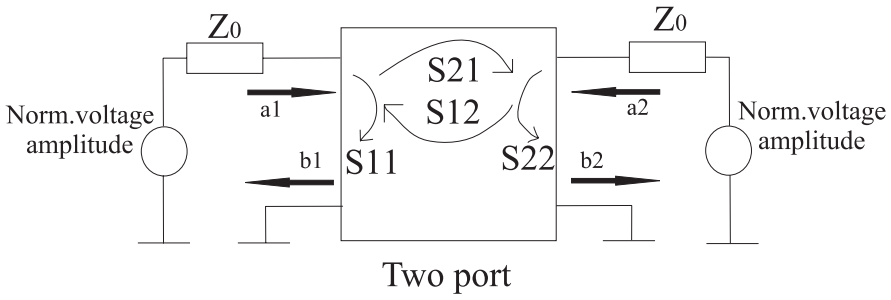

Figure 2.1: The S-parameter configuration.

The presence of a characteristic impedance (load) on both sides of the two-port system shows that the power of the traveling waves can also be seen as normalized voltages or currents.

Example for a normalized voltage with $Z_0 = 50\ \Omega$:

If the power P_{dB} is given in [dBm], the power P_{Watt} is given in [Watt] and the voltage V in [mV] , it shows for P_{dB} = -10 dBm:

$$P_{\mathrm{dB}} = 10 \cdot \log(P_{\mathrm{Watt}}\ [\mathrm{mW}]),\ \text{with} \tag{2.1}$$

$P_{\mathrm{Watt}} = 0.1$ mW gives

$$V = \sqrt{P_{\mathrm{Watt}}\ [\mathrm{mW}] \cdot Z_0},\ \text{so V}\ =\ 70.71\ \text{mV}. \tag{2.2}$$

The S-parameter matrix for the two-port:

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}.$$

The S-parameter definition in power terms:

$$\begin{pmatrix} |b_1|^2 \\ |b_2|^2 \end{pmatrix} = \begin{pmatrix} |S_{11}|^2 & |S_{12}|^2 \\ |S_{21}|^2 & |S_{22}|^2 \end{pmatrix} \cdot \begin{pmatrix} |a_1|^2 \\ |a_2|^2 \end{pmatrix}, \text{ with}$$

$|a_i|^2$ = the power wave travelling to the gate of the two-port,
$|b_i|^2$ = the power wave reflected back from the gate of the two-port gate,

and the power definition of the S-parameters

$|S_{11}|^2$ = the reflected power from port 1,
$|S_{12}|^2$ = the power transmitted from port 1 to port 2,
$|S_{21}|^2$ = the power transmitted from port 2 to port 1,
$|S_{22}|^2$ = the reflected power from port 2.

The impedance of the input :	$S_{11} = \frac{b_1}{a_1}\|_{a_2=0}$
The reverse complex transmission coefficient :	$S_{12} = \frac{b_1}{a_2}\|_{a_1=0}$
The forward complex transmission coefficient :	$S_{21} = \frac{b_2}{a_1}\|_{a_2=0}$
The impedance of the output :	$S_{22} = \frac{b_2}{\mathrm{a}_2}\|_{a_1=0}$

A nearly perfect load on one of the two ports allows $a_{\mathrm{x}} = 0$ with x = 1 or 2.

The S-parameters can easily be converted to Y, Z or H-matrixes to extract device parameters (see Appendix C). The S-parameters can be measured with a vector network analyzer (VNA) and displayed by means of a Smith diagram [8]. An example of a Smith Chart is given in figure 2.2.

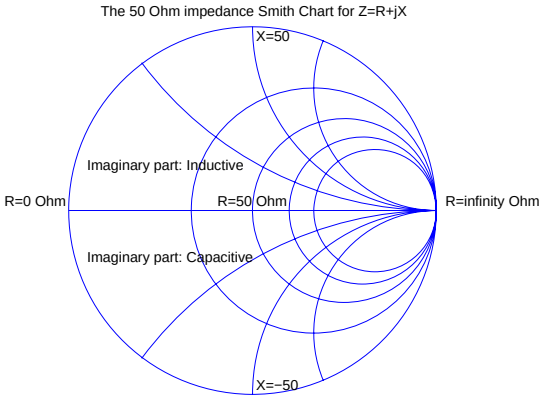

Figure 2.2: The 50 Ω impedance Smith Chart. The horizontal axis shows the real part and the circular shapes represent reactance values. The circular shape downwards represents the capacitive component and the circular shape upwards shows the inductive component.

2.2 RF *C-V* Measurement Equipment

The measurement equipment with a description:

1. HP 4145b Semiconductor Parameter Analyzer. A potential can be applied on the two-port and the current flow can be shown.
2. HP 8510c Vector Network Analyzer (VNA). The VNA extracts the *S*-parameters during a frequency sweep.
3. Agilent 8517b two-port *S*-parameter test set. The 8517b outputs the DC and RF voltage from respectively, the HP 4145b and the VNA, on the two-port.
4. Agilent Series Synthesized Sweeper. This signal generator controls the frequency with a coverage of 45 MHz to 50 GHz with 1 Hz resolution.
5. SUMMIT 9000 Analytical Probe Station. This wafer docking station includes the chuck, probes and light sources. Two different Ground-Signal-Ground (GSG) probes (type |Z| and 48131) have been used for the Adict wafer from Philips. Two identical Z-probes are used for the wafers fabricated in the cleanroom.

The measurement setup is given in figure 2.3.

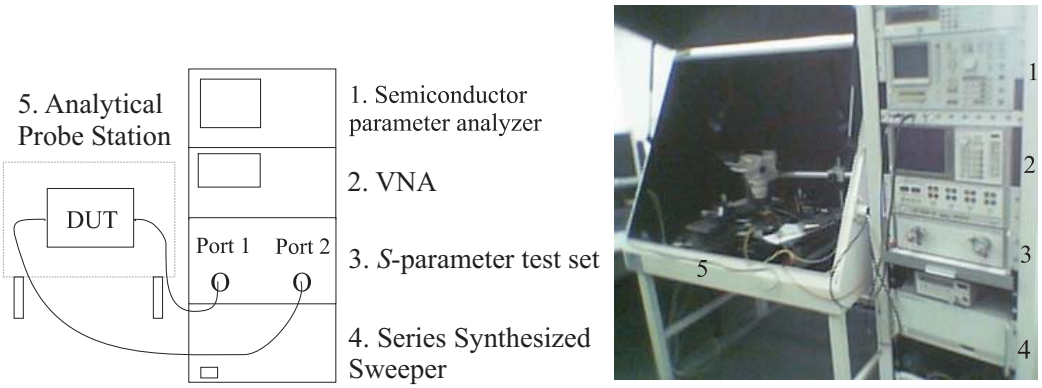

Figure 2.3: The measurement equipment.

The wafers and substrates:

- Wafer: 100 nm IMEC, Adict, PLI 1017#15, CMOS.
- A standard wafer and a low resistivity substrate.
- Calibration substrate from Picoprobe: Impedance Standard Substrate (ISS) Part# CS 5.
- Contact substrate.

The next section mentions the measurement precautions and the steps required before measuring on the actual DUT.

Measurement precautions

To make accurate measurements one has to give special attention to the measurement equipment.

Wafer and substrate placement

The wafer, the contact substrate and the calibration substrate are all placed on the same chuck and must be properly held by vacuum.

Probes

On-wafer*, the probes cannot be directly placed on the devices due too small dimensions. Bond pads are needed onto which the probes can make contact, so that an indirect contact can be made via interconnects to the DUT (see figure 2.4).

GSG probes are used for the measurements. The GSG configuration is electrically better than the Ground-Signal (GS) or Signal-Ground (SG) configurations, because in the two latter cases, field lines are coupled to the substrate on both sides of the signal line (see figure 2.5). The amount of coupling depends on the substrate thickness and on the pad spacing [9].

The probes must be clean. Dirt on the probes, like dust and metal parts, can disturb the measurements due to extra parasitics.

*In this report a difference is made between on-wafer and off-wafer. On-wafer means that the de-embedding structures and test structures are on the same wafer. Off-wafer points to the calibration or contact substrate that are separate samples.

To align the probes, a contact wafer is used to ensure good contact from all the tips of the probes on the contact substrate. Before starting the measurement make sure that the probes are in good contact with the bond pads, by looking at the amount of skate that is produced when placing the probes and verify on the VNA if a good contact is made.

Source Measurement Unit (SMU) connections

To connect the voltage and ground signals from the parameter analyzer to the probes, a connection has to be made to the VNA using coaxial cables. The VNA is successively connected to the S-parameter test set. In the S-parameter test set the DC gate voltage from the parameter analyzer and the RF power from the VNA are added by means of a bias T-connection that leads to the probes.

Settings VNA

The system should be calibrated by a calibration method that has a well-defined 50 Ω (like the SOLT calibration method in section 2.3). The system must be calibrated for the frequency range of interest, a sufficient amount of frequency points have to be used and the RF power has to be set.

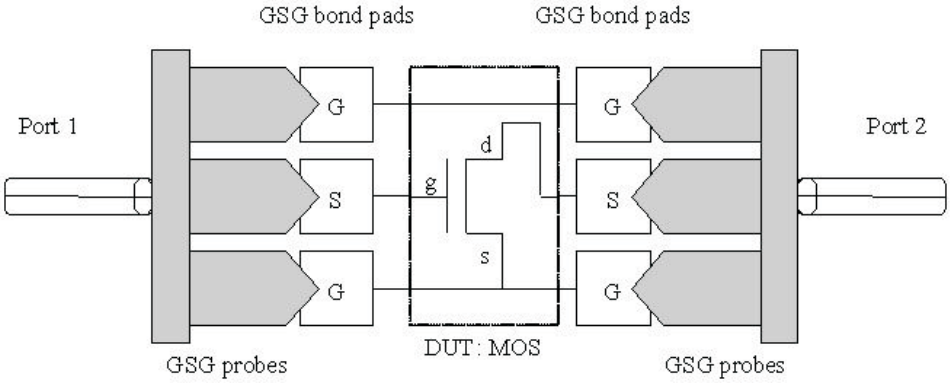

Figure 2.4: The GSG configuration with a MOSFET in between.

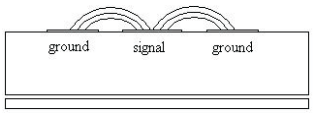

Figure 2.5: The fieldlines can be terminated on the ground lines.

Measuring in general

The intrinsic behavior of the device is of main interest. Two techniques are required to exclude parasitic effects between the measurement equipment and the DUT:

1) calibration
2) de-embedding

When the calibration has been performed, the parasitic elements of the measurement equipment, cables and probes have been removed. The S-parameters obtained from the calibration are memorized by the VNA and automatically subtracted from measurements to come, i.e. when measuring on de-embedding structures. The position of the reference plane is altered by means of calibration. This is a boundary region that defines were the measured system ends. The quality of the two-port calibration is mainly determined by the load termination.

The reference plane is at the probe tips after calibration and needs to be shifted from the probe tips to the DUT by means of de-embedding (see figure 2.6). De-embedding removes the parasitics caused by the bond pads and interconnects.

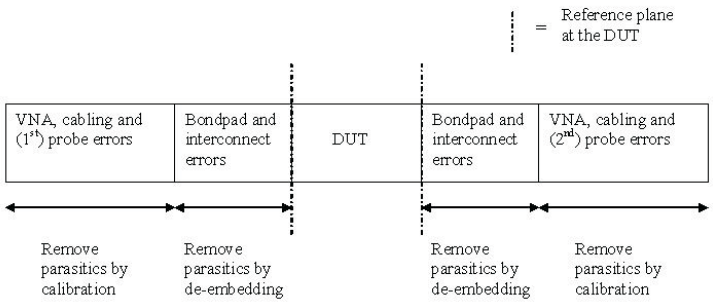

Figure 2.6: The reference planes after calibration and de-embedding.

2.3 Calibration

To make accurate measurements, with solely the effects of the DUT, a calibration must be performed followed by a de-embedding method. Different calibration techniques are used in the chip industry today. The accuracy of the calibration methods depends on how well the standards are known. A few of the calibration methods are listed in the next paragraph and are supported by the HP 8510c VNA. The off-wafer impedance standard substrate (ISS) is used for the calibration. The calibration standards on the ISS are durable, accurate, and the results show high repeatability. The bond pads are made of gold to ensure a low contact resistance.

For each method in general:

• The smaller the frequency range the more accurate the calibration.
• Placement of the probes is consistent within 5 µm due to phase changes [9]. Manual placement of the probes is not the most accurate way. Auto probes can offer better precision and repeatability. Manual probe placement gives an error of 15 % with 10 % spread, while automated calibration can give 5 % error with 0.3 % spread [10]. The calibration in this research is done manually.
• Verification of each standard is a must to ensure that the measurement results are consistent and as expected.
• Fixed GSG probes are used in this research.

In the following section a number of calibration techniques are listed, a suitable calibration method is chosen and an outline is given in order to interpret the calibration results. Several calibration methods that could be used are clarified.

Short-Open-Load-Thru (SOLT)

This calibration technique uses 4 calibration standards to correct for the parasitic effects: short, open, load and thru (see figure 2.7). The load resistance used is a well-defined 50 Ω impedance with < 0.25 % deviation on an ISS [9, 11]. It is difficult to fabricate 50 Ω load structures with high accuracy on-wafer, suitable for high frequencies. Consistency of the values for the parasitic inductances and capacitances, with just one reference plane, is difficult to obtain for frequencies above 20 GHz [12].

Line-Reflective-Match (LRM)

For this technique three standards are used: 1) a line or thru standard, 2) a reflect standard, for which no characterization is required and 3) two identical match (load) standards. The reference impedance is determined by highly accurate (trimmed) load resistors. The inductance caused by the match standard is determined internally by the VNA during calibration. The open and short standards do not have to be performed. This technique is more accurate over a broader frequency band and promises a better accuracy for the S-parameters compared to SOLT.

Line-Reflect-Reflect-Match (LRRM)

The standards used for LRRM: 1) the line or thru, 2) two different reflection standards (which do not require characterization) and 3) a matched load. Only one of the two ports has to be matched by a trimmed resistor. The deviations between the load reactances of the probes seen by the ports are not present, as with LRM. The LRM and LRRM load inductance corrections are only available in Cascade's VIVA calibration software (VNACAL and WINCAL). With LRRM, the line delay and DC resistance of one load standard must be known by the VNA.

Thru-Reflect-Line (TRL) or Line-Reflect-Line (LRL)

The standards for this type of calibration: 1) thru, 2) reflect and 3) one or more delay lines are used. The characteristic impedance is made by means of transmission lines instead of using trimmed resistors. The reference plane is set by the reflection standard and transmission line. When the measurement frequencies are low, the line length for the transmission line can become very long which is shown by the wavelength:

$$\lambda = \frac{c}{f} \tag{2.3}$$

The longer the lines, the more chance of loss. This can cause deviations in the characteristic impedance value. The reference plane is shifted, which causes inaccuracy. Hence, for low frequencies this method is not practical.

The choice for the off-wafer calibration method

Off-wafer, the choice of the calibration method mainly depends on the accuracy and the frequency range.

The HP8510c network analyzer can measure from $f = 45$ MHz until deep in the GHz range. In section 4.1 will be shown that the measurement frequency will not exceed $f = 1$ GHz. SOLT is the most common method for this small frequency range and is performed with the ISS wafer, which gives sufficient accuracy over the mentioned frequency range [13].

Interpreting the calibration

The SOLT calibration method is not an ideal one. The *short* represents an inductance, the *open* represents a capacitor, the *load* resistance deviates from its intended load value and the *thru* has a non-ideal delay time. Each standard has its own structure as is seen in figure 2.7.

SHORT

For a short all GSG-probe pads are shorted. The short standard is a reflection standard together with the open and load standards. The S-parameters for the reflection standard are S_{11} and S_{22}. The short measures the parasitic inductance coming from the measurement equipment. In a Smith Chart the first measurement point for both S-parameters is found at 0 Ω. For a rising frequency sweep, the marker will always move counter clock-wise in a circular shape along the Smith Chart (see figure 2.2).

OPEN

For an open calibration, the probes are placed on the pads. The open measures the parasitic capacitances of both ports. In the Smith Chart, the first measurement point starts at infinity (at the right end of the real axis).

LOAD

For a load, the probes are placed on a structure with two 100 Ω resistances in parallel, to minimize the inductance value.

THRU

For a thru, the probe pads of the GSG probes are connected to each other in parallel by three lines. The most important S-parameters of this transmission standard are S_{21} and S_{12}, respectively the forward and reverse transmission

coefficients, or forward and reverse delay [14].

After the calibration has been stored on the VNA, the impedance will be very close to 50 Ω in the middle of the impedance Smith Chart.

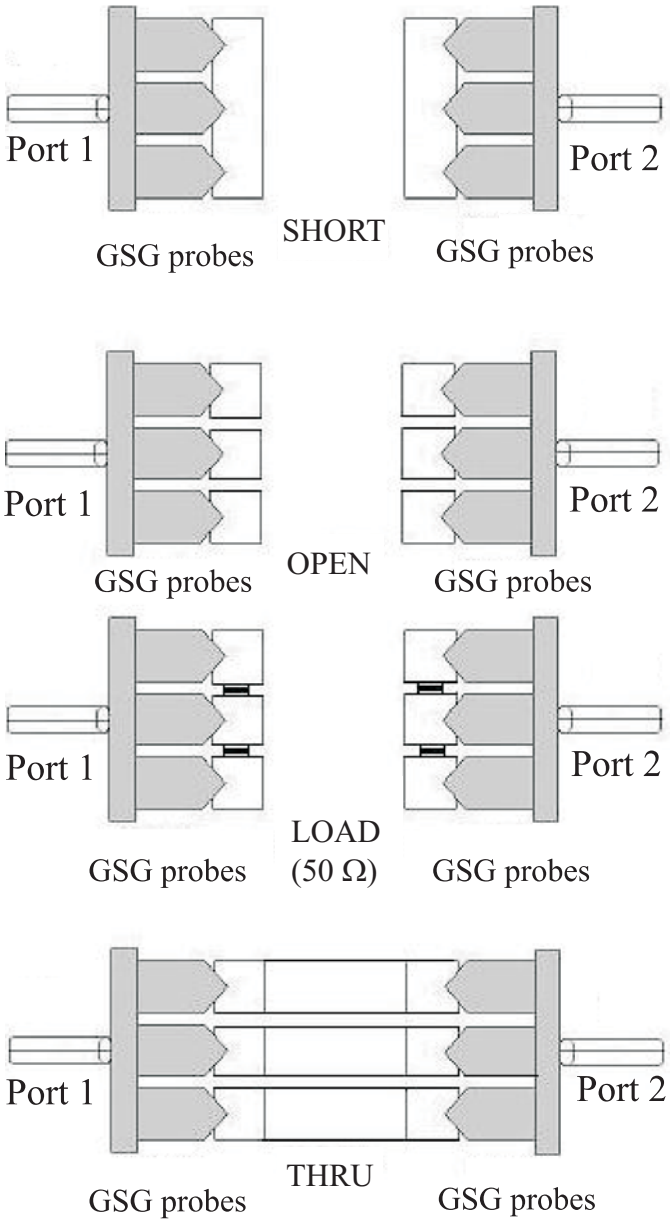

Figure 2.7: SOLT calibration.

2.4 De-embedding

After the calibration on the ISS the next step is de-embedding. De-embedding structures are made on-wafer to remove the parasitics caused by the bond pads and interconnects between the pads and the DUT. The parasitic effects are of great influence at microwave frequencies.

In this section the de-embedding is discussed in terms of design of the chosen de-embedding patterns, the equivalent circuit diagrams and calculation of the admittance (Y) parameters.

The de-embedding technique that is sufficiently accurate for f $<$ 30 GHz [15] is the well-known "open-short" de-embedding procedure [16]. More advanced methods can be found in [15, 17, 18, 19].

In this section the open-short de-embedding is discussed and the way in which the intrinsic device parameters are found is mentioned.

Open-short de-embedding

An 'open' de-embedding structure is added on-wafer to remove the pad capacitance and the interconnect line capacitances.

The 'short' de-embedding structure is required, because the contact resistance between the probes and contact pads must be taken into account. The contact pads of the off-wafer ISS are made of gold. However, the contacts pads on the test-structures on-wafer use aluminum for the layers. The difference in material gives an extra contact resistance. Also the resistive and reactance loss of the interconnect lines are removed.

Intrinsic device parameters

Three sets of S-parameters are obtained by performing measurements on the structure with the DUT (see figure 2.8a), the open de-embedding structure (see figure 2.8b) and short de-embedding structure (see figure 2.8c). All of which are saved and used in a later stage to make the conversion to Y- or Z-parameters.

To find the Y-parameters of the intrinsic DUT, the S-parameters have to be converted. Using the math of the open-short de-embedding technique, the

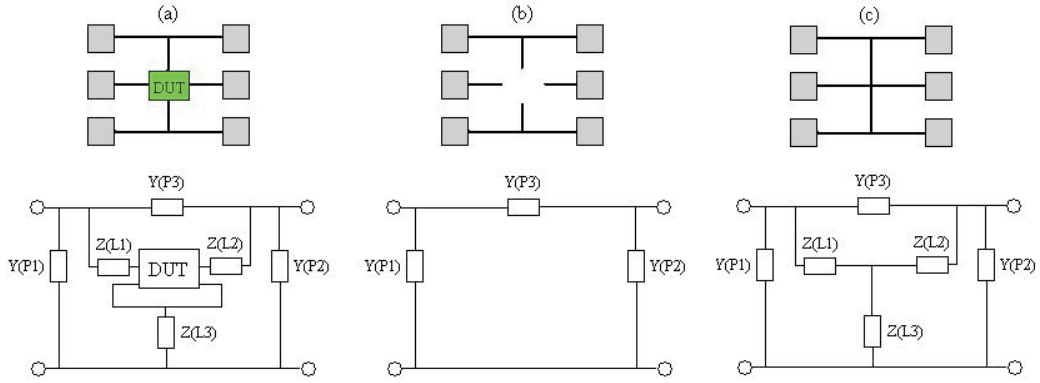

Figure 2.8: The structures of : a) the DUT, b) open de-embedding and c) short-de-embedding.

intrinsic admittance parameters follow from [16]

$$Y_{\text{intr}} = ((Y_{\text{DUT}} - Y_{\text{open}})^{-1} - (Y_{\text{short}} - Y_{\text{open}})^{-1})^{-1}. \tag{2.4}$$

After the de-embedding, the reference plane is shifted from the probe tips to the edge of the DUT.

The reading of the S-parameter data, the conversion to admittance parameters and calculation of the intrinsic Y-parameters have been implemented in the mathematical program Matlab.

2.5 Three-element model

Leaky MOS devices can be described by the three-element model in figure 2.9.

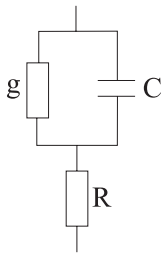

Figure 2.9: The three-element model.

The mathematical deductions from this model show partly the considerations that must be taken into account when designing test structures for devices with a high leakage current. The math that is presented is summoned and clarified.

Impedance

$$Z = \frac{1}{\mathrm{j}\omega C + g} + R \tag{2.5}$$

The impedance shows that at low frequencies the impedance is mainly determined by the influence of the capacitor. The series resistance dominates at RF frequencies.

Quality factor

The quality factor is a measure of the device performance.

The quality factor is expressed by:

$$Q = -\frac{Im(Z)}{Re(Z)} = \frac{\omega C}{g + R(\omega^2 C^2 + g^2)} \text{ , and} \tag{2.6}$$

simplified for low frequencies

$$Q \approx \frac{2\pi f C}{g} \text{ , and} \tag{2.7}$$

for high frequencies

$$Q \approx \frac{1}{2\pi f R C}. \tag{2.8}$$

The optimum Q is represented when the derivative of $Q(\omega) = 0$:

$$Q_{\mathrm{opt}} = \frac{1}{2\sqrt{gR(1+gR)}}. \tag{2.9}$$

If $Q_{\mathrm{opt}} \gg 1$:

$$g \cdot R \ll \frac{\sqrt{2}-1}{2} \approx 0.2, \text{ with } g = \frac{\mathrm{d}I}{\mathrm{d}V}. \tag{2.10}$$

On the spot, this shows that test structures for high leakage devices must have a low series resistance to make sure that $Q_{\text{opt}} \gg 1$.

One of the crucial demands for doing capacitance-voltage measurements is that the capacitance must be high enough ($C \geq 1$ pF) and the quality factor (Q) must be sufficient ($Q > 10$) to make solid statements on the device(s) in question [2].

In figure 2.10 different capacitance values, at different frequencies, show the influence on the quality factor. The plot indicates, that on the left side of the optimum Q, the differential conductance g dominates in determining the quality factor and on the right side the series resistance. The series resistance R, the differential conductance g and the capacitance C are all related to area. The structure contains a p^+-overlap region and the scalingfactor for device fabrication $\lambda = 2$ µm. More details can be found in chapter 3.

The series resistance R is determined in strong accumulation (see chapter 3), the capacitance

$$C = \frac{\varepsilon_0 \cdot \varepsilon_{Al_2O_3} \cdot W \cdot L}{t_{\text{ox}}}, \tag{2.11}$$

and the differential conductance g is determined from the 'gate tunneling current vs. the gate-voltage' plot (figure 1.2), by calculating the slope in strong accumulation at a fixed voltage ($V_{\text{gate}} = -2$ V).

Frequency

To prevent capacitive roll-off, the DUT must have a minimum operating frequency. The minimum and top frequency are set at $Q = 1$ and are expressed by

$$f_{\text{min}} = \frac{1 - \sqrt{1 - 4gR(1+gR)}}{4\pi RC} \approx \frac{g}{2\pi C}, \text{ and} \tag{2.12}$$

$$f_{\text{top}} = \frac{1 + \sqrt{1 - 4gR(1+gR)}}{4\pi RC} \approx \frac{1}{2\pi RC}. \tag{2.13}$$

The optimal quality factor Q_{opt} is set by the optimum frequency

$$f_{\text{opt}} = \frac{1}{2\pi RC}\sqrt{gR(1+gR)}. \tag{2.14}$$

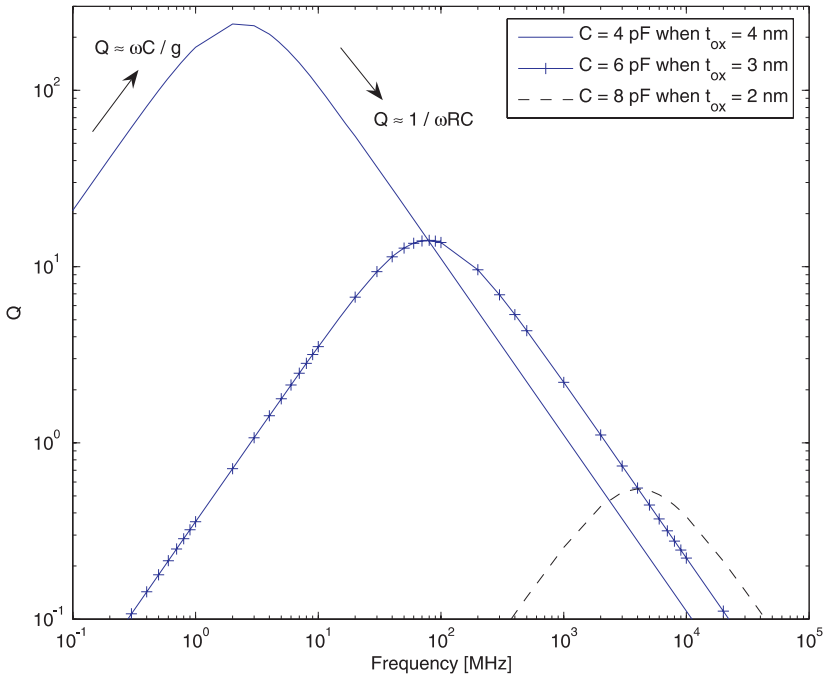

Figure 2.10: The influence of different oxide capacitances, at different frequencies, on the quality factor Q. A low resistivity substrate with 15-25 mΩ·cm is used for the calculations. The structure has a gate width W = 100 µm and gate length L = 2 µm. The three-element model is used with $R = 9$ Ω, $g(t_{ox} = 4\text{ nm}) = 4.8{\cdot}10^{-7}$ Ω^{-1}, $g(t_{ox} = 3\text{ nm}) = 1.4{\cdot}10^{-4}$ Ω^{-1}, $g(t_{ox} = 2\text{ nm}) = 6{\cdot}10^{-2}$ Ω^{-1}.

Parameter extraction by *S*-parameters

When the series resistance is very small, a few assumptions can be made that make it easier to find:

- R is assumed to be bias and frequency independent,
- $R \cdot C << 1$, and
- $R \cdot g << 1$.

The device capacitance and series resistance can be extracted from the conversion of the S-parameters to Y-parameters.

The complex Y_{11} is used to extract the parameters with

$$Y_{11} = \frac{\mathrm{j}\omega C + g}{1 + R(\mathrm{j}\omega C + g)} \ , \text{ so} \tag{2.15}$$

$$Re(Y_{11}) = \frac{g(1+gR) + \omega^2 C^2 R}{(1+gR)^2 + R^2\omega^2 C^2} \ \approx \ g + \omega^2 C^2 R \ , \text{ and} \tag{2.16}$$

$$Im(Y_{11}) = \frac{\omega C}{(1+gR)^2 + R^2\omega^2 C^2} \ \approx \ \omega C. \tag{2.17}$$

Then the device capacitance and the series resistance become:

$$C_{\mathrm{gg}} = \frac{Im(Y_{11})}{\omega}, \text{ and} \tag{2.18}$$

$$R = \frac{Re(Y_{11})}{Im(Y_{11})^2} \ , \text{ if } g \ \ll \ \omega^2 C^2 R. \tag{2.19}$$

Chapter 3

Design aspects

The specifications, considerations, calculations and the fabrication process all together affect the final test and de-embedding structures.

With the three-element model in mind, a few design considerations already have been mentioned that must be taken into account. More crucial design considerations are reported in this chapter . The series resistance calculation in accumulation and inversion are described, the best gate width for the test structures is determined, the possible influence of non-quasistatic effects are mentioned and a detailed layout of the test structures is given.

3.1 Design considerations

To design low series resistance structures the theoretical, measurement and device structure considerations are mentioned.

Theoretical considerations:

- The structure must satisfy equations 2.10 and 2.12 - 2.14.
- The device capacitance and quality factor must be large enough ($C \geq 1$ pF and $Q > 10$), see section 2.5.
- The influence of fringing fields coming from the gate must be checked. The percentage of fringing fields from the gate is defined by the ratio of the $t_{\mathrm{ox}}/L_{\mathrm{gate}}$ [20]. In this research the influence is negligible due to a long gate length.
- It must be clear how the intrinsic device capacitance is extracted and how the de-embedding is performed.

- The amount of doping in the silicon substrate is related to the series resistance contribution in accumulation. A higher doping gives a smaller series resistance contribution. Also the source is heavily doped to reduce the series resistance.
- The possible presence of the non-quasistatic effects must be checked.
- To minimize the threshold voltage shift, the channel must have a minimal length L_{min} [µm], indicated by Brews' law [21]:

$$L_{\min} = 0.4 \cdot [x_j \cdot t_{ox} \cdot (W_s + W_d)^2]^{1/3}, \tag{3.1}$$

  with the junction depth x_j [µm], the gate oxide thickness t_{ox} [Å], the depletion width of the source W_s [µm] and drain W_d [µm].

Device structure considerations:

- A small channel length is needed to reduce the series resistance of the channel in inversion. The photolithography equipment at MESA+ limits the dimension to about 1.5 µm. The smallest gate length that is used in this research is fixed in the calculations at $L = 2$ µm. The channel is relatively large, but there is an influence of short-channel effects e.g. threshold variations and mobility degradation. The threshold voltage gives variations dependent on the substrate doping, the temperature, the processing and the channel length. The mobility degradation depends on the electric field across the oxide.
- The diffusion regions must be as close to the gate as possible.
- A guard ring around the DUT prevents leakage effects to neighboring devices.
- The process flow and the available equipment form restrictions for the layout of the devices. The adjustment of the process flow for device fabrication in the MESA+ clean room is preferably simple and does not differ much from the current process flow development of MOS devices.
- The structures must not be unnecessary complex.
- A metal is used because of the lower sheet resistance compared to polysilicon.
- Multiple gate fingers are used to reduce the effective gate resistance*.

*At the moment a metal gate is used the gate resistivity is very small and thereby the effective gate resistance.

- The material and thickness of the metal layers are of importance. High conductivity material is preferred.

Measurement considerations:

- The calibration method must be accurate over the entire frequency range.
- The usage and type of probes have an influence on the design of the bond pads. The material and stiffness of the probes and the metal used for the bond pads determine how much landing and pressure is required for the probes to make good contact.

The test structure design in general

The layout of the test structures must be known to calculate the series resistance. The following design structure is formed:

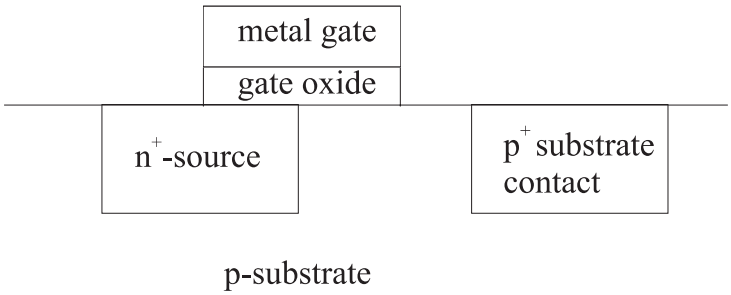

Figure 3.1: A sketch of the test structure *without* a gate overlap region for the substrate contact.

The test structure is a gated diode that resembles a MOSFET without a drain. The drain is left out to reduce the series resistance and dimensions of the test structure. The metal contacts are made of aluminum. To bring the device in accumulation and inversion, actually only a MOS capacitor is needed. The heavily doped source diffusion region is present to make it possible for the device to end up in inversion. The heavily doped substrate contact must be as close to the gate as possible to reduce the series resistance, as will appear from the mathematics in the next paragraph. Structures are made with and without a gate overlap region for the substrate contact. The substrate contact also gives the advantage of bringing the device faster in accumulation.

More (detailed) structures with dimensions and masks used for the process flow will be mentioned in section 3.2.

Determining the series resistance

There are different factors that contribute to the series resistance when going from inversion to accumulation. In inversion, the series resistance is mainly determined by the gate resistance and the channel resistance. In accumulation, the series resistance is dominated by the gate resistance and the p^+ substrate contact area.

Inversion region

The gate resistance is the same in inversion and accumulation and is given by [22]:

$$R_{\mathrm{g}} = (\frac{\rho_{\mathrm{Al}}}{t_{\mathrm{gate}}}) \cdot \frac{W_{\mathrm{finger}}}{\mathrm{N} \cdot L_{\mathrm{finger}}}, \tag{3.2}$$

with the thickness of the gate metal t_{gate} and the gate resistivity $\rho_{\mathrm{Al}} = 2.7{\cdot}10^{-6}$ $\Omega{\cdot}$cm [23].

The small signal channel resistance contribution is expressed by [24]

$$r_{\mathrm{channel}} = \frac{L}{\mu_{\mathrm{eff}} \cdot C_{\mathrm{ox}} \cdot W \cdot (V_{\mathrm{gs}} - V_{\mathrm{th}})}. \tag{3.3}$$

The assumption is used that the probes measure the resistance halfway through the channel between the gate and the source. Due to the distributed *R-C* network in the channel, the value of the total channel resistance is equally divided in the middle of the channel, so the channel resistance is divided by a factor of 4.

For the gate dielectric Al_2O_3 will be used. Comparing the conventional gate dielectric SiO_2 to Al_2O_3, a difference exists in the way the gate dielectric is formed. Silicon is thermally oxidixed to SiO_2 while Al_2O_3 is deposited on the silicon. Scattering phenomena reduce the channel mobility for the latter. Empirically, it is indicated in [25] that the channel mobility is reduced by a factor 2 with respect to a SiO_2 gate oxide.

The effective vertical electric field is needed to calculate the mobility. Both are found by using the equations in the BSIM v.3.3.0 MOSFET model [26].

The reference shows for an NMOS that, when V_{fb} = -0.8 V and the substrate surface potential Ψ is the opposite, the vertical electric field for SiO_2 will be:

$$E_{\mathrm{eff}} \approx \frac{1}{\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{Al_2O_3}}}} \cdot \frac{V_{\mathrm{gs}} + V_{\mathrm{th}}}{2 \cdot t_{\mathrm{ox}}} = \frac{V_{\mathrm{gs}} + V_{\mathrm{th}}}{6 \cdot t_{\mathrm{ox}}}. \tag{3.4}$$

The effective mobility for electrons $\mu_{\mathrm{eff,n}}$ for Al_2O_3 can now be found by:

$$\mu_{\mathrm{eff,\,n}} = \frac{1}{2} \cdot [\frac{\mu_0}{1 + (E_{\mathrm{eff}}/E_0)^{\nu}}], \tag{3.5}$$

with μ_0, E_0 and ν typical constants for electrons at the surface. The series resistance in inversion becomes:

$$R_{\mathrm{s,\,inv.}} = R_{\mathrm{gate}} + r_{\mathrm{channel}} = \frac{\rho}{t_{\mathrm{gate}}} \cdot \frac{W_{\mathrm{finger}}}{\mathrm{N} \cdot L_{\mathrm{finger}}} + \frac{L}{4 \cdot \mu_{\mathrm{eff}} \cdot C_{\mathrm{ox}} \cdot W \cdot (V_{\mathrm{gs}} - V_{\mathrm{th}})}. \tag{3.6}$$

Accumulation region

In accumulation, the series resistance is dominated by the gate resistance and by the areas of the substrate contacts. From the optimization of the layout of the test structure in section 3.2 follows the additive resistance caused by the substrate contact

$$R_{\mathrm{sub,\,contacts}} = R_{\mathrm{sub,\,contact_1}} \parallel R_{\mathrm{sub,\,contact_2}} = \frac{1}{2} \cdot R_{\mathrm{sub,\,contact_1}}, \text{with} \tag{3.7}$$

$$R_{\mathrm{sub,\,contact_1}} = R_{\mathrm{contact}} + R_{\mathrm{diff,\,area}}\ . \tag{3.8}$$

The original equation for the well resistance in [27] is transformed to the substrate diffusion area resistance $R_{\mathrm{diff,area}}$, so

$$R_{\mathrm{sub,\,contact}} = \frac{1}{2} \cdot [\ (\frac{\rho_{\mathrm{Al}}}{t_{\mathrm{contact}}}) \cdot \frac{W_{\mathrm{finger}}}{\mathrm{N} \cdot L_{\mathrm{finger}}} + \frac{R_{\mathrm{sub,\,sq}} \cdot L_{\mathrm{gate\text{-}sub.cont.}}}{2 \cdot W \cdot \mathrm{N}}\ ], \tag{3.9}$$

with the thickness of the contact t_{contact}. The $L_{\mathrm{gate\text{-}sub.cont.}}$ indicates the distance between the edge of the substrate contact and the edge of the gate

contact. *Without* a gate overlap region for the p^+ contact: $L_{\text{gate-sub.cont.}} = 6\lambda$ with λ the scaling parameter. *With* an overlap region the $L_{\text{gate-sub.cont.}}$ is redefined as the length in which the substrate will add a resistance value below the gate and is equal to the gate length λ. The substrate sheet resistance is [28]

$$R_{\text{sub, sq}} = \frac{\text{bulkresistivity}}{\text{junction depth } x_{\text{j}}}. \tag{3.10}$$

Three types of substrates used are summoned in table 3.1.

	bulk resistivity [Ω·cm]	junction depth x_{j} [µm]	sheet resistance [Ω/□]	N_{A} [cm^{-3}]
1	0.015 - 0.025	0.1585	$9.46{\cdot}10^2$ - $0.1585{\cdot}10^3$	$3.2{\cdot}10^{18}$
2	5 - 10	0.5711	$8.76{\cdot}10^4$ - $1.75{\cdot}10^5$	$1.8{\cdot}10^{15}$
3	± 0.13 (p-well)	0.2256	$5.08{\cdot}10^3$	$2.0{\cdot}10^{17}$

Table 3.1: Details of the substrates that will be used. Substrate 1 has a very low silicon resistivity, substrate 2 is a typical substrate and substrate 3 is a typical substrate with a *p*-well. The junction depth is determined by simulating the process flow in 'Silvaco'. The bulk resistivity of the *p*-well of the 3rd substrate is determined from [28].

Calculation of the parameters of interest

Only the gate width can vary for the calculation of the design parameters, since the gate length is fixed. Different gate widths have consequences for the parameters of interest, as could be made out from the equations in section 2.5.

For the first few process runs a gate oxide thickness of 4 nm is chosen.

Parameters in the inversion region

In inversion, the gate width is varied and the design parameters are examined. It is of importance that all of the design rules are considered before a final device size is chosen.

An important objective is a quality factor above 10, preferably in both inversion and accumulation. According to the data from table 3.2, with its

Inversion (all substrates)

W [µm]	R_{gate} [Ohm]	r_{ch} [Ohm]	R_{serie} [Ohm]	C [pF]	g [1/Ohm]	f_{min} [Hz]	f_{top} [Hz]	f_{opt} [Hz]	Q_{opt}	Q (f = 45 MHz)
10	6.75E-02	1.89E+02	7.56E+02	4.00E-01	3.36E-07	1.34E+05	2.10E+09	1.68E+07	6.27E+01	4.11E+01
20	1.35E-01	9.45E+01	3.78E+02	8.00E-01	6.72E-07	1.34E+05	2.10E+09	1.68E+07	6.27E+01	4.10E+01
40	2.70E-01	4.72E+01	1.89E+02	1.60E+00	1.34E-06	1.34E+05	2.09E+09	1.67E+07	6.26E+01	4.09E+01
60	4.05E-01	3.15E+01	1.26E+02	2.40E+00	2.02E-06	1.34E+05	2.08E+09	1.67E+07	6.24E+01	4.06E+01
80	5.40E-01	2.36E+01	9.50E+01	3.20E+00	2.69E-06	1.34E+05	2.06E+09	1.66E+07	6.20E+01	4.03E+01
100	6.75E-01	1.89E+01	7.63E+01	4.00E+00	3.36E-06	1.34E+05	2.03E+09	1.65E+07	6.17E+01	3.98E+01
150	1.01E+00	1.26E+01	5.14E+01	6.00E+00	5.04E-06	1.34E+05	1.95E+09	1.61E+07	6.04E+01	3.84E+01
200	1.35E+00	9.45E+00	3.91E+01	8.00E+00	6.72E-06	1.34E+05	1.84E+09	1.57E+07	5.87E+01	3.65E+01
300	2.03E+00	6.30E+00	2.72E+01	1.20E+01	1.01E-05	1.34E+05	1.59E+09	1.46E+07	5.46E+01	3.20E+01
500	3.38E+00	3.78E+00	1.85E+01	2.00E+01	1.68E-05	1.34E+05	1.11E+09	1.22E+07	4.56E+01	2.30E+01
700	4.73E+00	2.70E+00	1.55E+01	2.80E+01	2.35E-05	1.34E+05	7.65E+08	1.01E+07	3.78E+01	1.62E+01
1000	6.75E+00	1.89E+00	1.43E+01	4.00E+01	3.36E-05	1.34E+05	4.60E+08	7.85E+06	2.93E+01	9.93E+00
1500	1.01E+01	1.26E+00	1.52E+01	6.00E+01	5.04E-05	1.34E+05	2.33E+08	5.58E+06	2.09E+01	5.10E+00
2200	1.49E+01	8.59E-01	1.83E+01	8.80E+01	7.39E-05	1.34E+05	1.15E+08	3.93E+06	1.47E+01	2.54E+00
3000	2.03E+01	6.30E-01	2.28E+01	1.20E+02	1.01E-04	1.34E+05	6.34E+07	2.92E+06	1.09E+01	1.41E+00
5000	3.38E+01	3.78E-01	3.53E+01	2.00E+02	1.68E-04	1.35E+05	2.32E+07	1.77E+06	6.58E+00	5.17E-01
7000	4.73E+01	2.70E-01	4.83E+01	2.80E+02	2.35E-04	1.37E+05	1.18E+07	1.27E+06	4.70E+00	2.66E-01
10000	6.75E+01	1.89E-01	6.83E+01	4.00E+02	3.36E-04	1.40E+05	5.74E+06	8.97E+05	3.28E+00	1.31E-01

Table 3.2: The table shows the calculation of the parameters for different gate widths in inversion.

relating plots given in figure 3.2, this is possible with the HP8510c vector network analyzer (Q > 10 at f = 45 MHz).[†]

[†]The differential conductance g is obtained from an actual MOS capacitor measurement at V_g = -2 V, with an Al_2O_3 gate oxide thickness t_{ox} = 4 nm. The leakage current becomes I_{gate} = 1.68 A/cm^2 at this voltage.

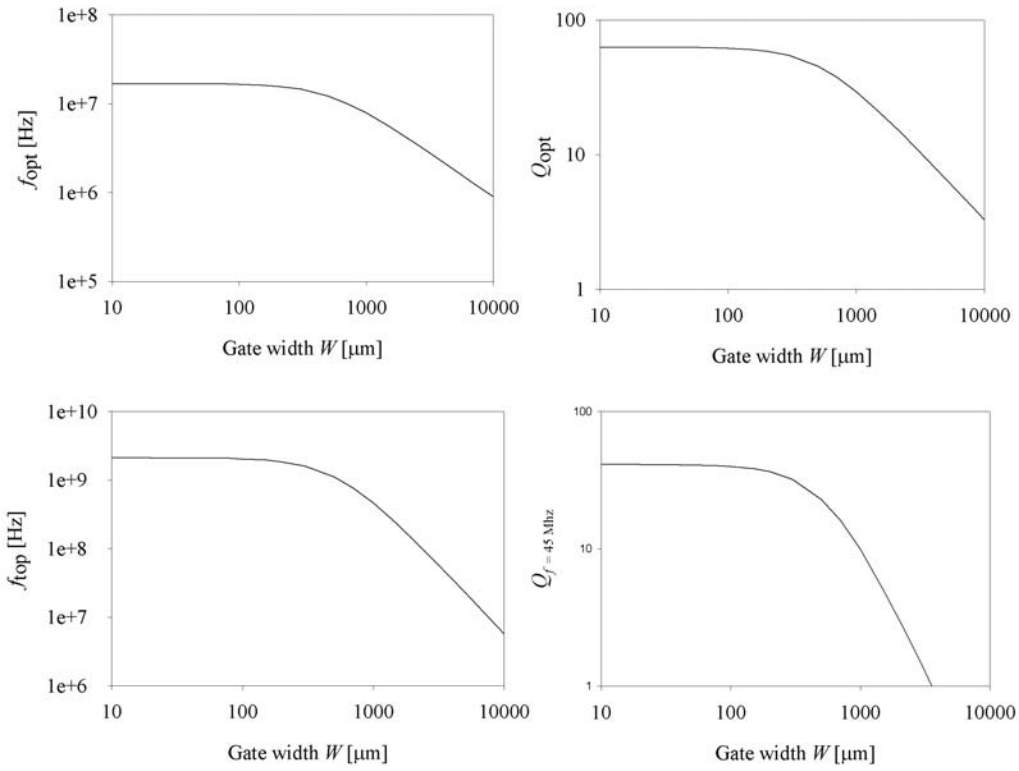

Figure 3.2: In the inversion region : the optimum frequency f_{opt}, the optimum quality factor Q_{opt}, the top frequency f_{top} and $Q_{\mathrm{f\,=\,45\ MHz}}$ vs. gate width W.

Since the series resistance and capacitance are determined in the accumulation region, this is the key area of concern.

Parameters in the accumulation region

In accumulation, the gate width is changed and the design parameters are examined (see tables 3.3 and 3.4). The consequences for the parameters of devices with and without a p^{+}-overlap region are clarified for all three substrates.

Low resistivity substrate without a p^+-overlap region under the gate

W [µm]	Rgate [Ohm]	Rsub1 [Ohm]	Rserie [Ohm]	Ctot [pF]	g [1/Ohm]	fmin [Hz]	ftop [Hz]	fopt [Hz]	Qopt	Q (f = 45 MHz)
10	6.75E-02	9.46E+02	4.73E+02	4.00E-01	3.36E-07	1.34E+05	8.41E+08	1.06E+07	3.97E+01	1.77E+01
20	1.35E-01	4.73E+02	2.37E+02	8.00E-01	6.72E-07	1.34E+05	8.40E+08	1.06E+07	3.96E+01	1.77E+01
40	2.70E-01	2.37E+02	1.19E+02	1.60E+00	1.34E-06	1.34E+05	8.39E+08	1.06E+07	3.96E+01	1.77E+01
60	4.05E-01	1.58E+02	7.93E+01	2.40E+00	2.02E-06	1.34E+05	8.37E+08	1.06E+07	3.96E+01	1.76E+01
80	5.40E-01	1.19E+02	5.97E+01	3.20E+00	2.69E-06	1.34E+05	8.33E+08	1.06E+07	3.95E+01	1.76E+01
100	6.75E-01	9.53E+01	4.80E+01	4.00E+00	3.36E-06	1.34E+05	8.29E+08	1.05E+07	3.94E+01	1.75E+01
150	1.01E+00	6.41E+01	3.26E+01	6.00E+00	5.04E-06	1.34E+05	8.15E+08	1.04E+07	3.90E+01	1.72E+01
200	1.35E+00	4.87E+01	2.50E+01	8.00E+00	6.72E-06	1.34E+05	7.95E+08	1.03E+07	3.86E+01	1.68E+01
300	2.03E+00	3.36E+01	1.78E+01	1.20E+01	1.01E-05	1.34E+05	7.45E+08	9.98E+06	3.73E+01	1.58E+01
500	3.38E+00	2.23E+01	1.28E+01	2.00E+01	1.68E-05	1.34E+05	6.20E+08	9.10E+06	3.40E+01	1.32E+01
700	4.73E+00	1.82E+01	1.15E+01	2.80E+01	2.35E-05	1.34E+05	4.95E+08	8.14E+06	3.04E+01	1.07E+01
1000	6.75E+00	1.62E+01	1.15E+01	4.00E+01	3.36E-05	1.34E+05	3.46E+08	6.81E+06	2.55E+01	7.53E+00
1500	1.01E+01	1.64E+01	1.33E+01	6.00E+01	5.04E-05	1.34E+05	2.00E+08	5.17E+06	1.93E+01	4.38E+00
2200	1.49E+01	1.92E+01	1.70E+01	8.80E+01	7.39E-05	1.34E+05	1.06E+08	3.77E+06	1.41E+01	2.35E+00
3000	2.03E+01	2.34E+01	2.18E+01	1.20E+02	1.01E-04	1.34E+05	6.06E+07	2.85E+06	1.06E+01	1.34E+00
5000	3.38E+01	3.56E+01	3.47E+01	2.00E+02	1.68E-04	1.35E+05	2.28E+07	1.76E+06	6.53E+00	5.09E-01
7000	4.73E+01	4.86E+01	4.79E+01	2.80E+02	2.35E-04	1.37E+05	1.17E+07	1.27E+06	4.68E+00	2.63E-01
10000	6.75E+01	6.84E+01	6.80E+01	4.00E+02	3.36E-04	1.40E+05	5.71E+06	8.95E+05	3.27E+00	1.30E-01

Typical substrate without a p+-overlap region under the gate

W [µm]	Rgate [Ohm]	Rsub2 [Ohm]	Rserie [Ohm]	Ctot [pF]	g [1/Ohm]	fmin [Hz]	ftop [Hz]	fopt [Hz]	Qopt	Q (f = 45 MHz)
10	6.75E-02	1.05E+05	5.25E+04	4.00E-01	3.36E-07	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
20	1.35E-01	5.25E+04	2.63E+04	8.00E-01	6.72E-07	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
40	2.70E-01	2.63E+04	1.31E+04	1.60E+00	1.34E-06	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
60	4.05E-01	1.75E+04	8.75E+03	2.40E+00	2.02E-06	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
80	5.40E-01	1.31E+04	6.56E+03	3.20E+00	2.69E-06	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
100	6.75E-01	1.05E+04	5.25E+03	4.00E+00	3.36E-06	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
150	1.01E+00	7.00E+03	3.50E+03	6.00E+00	5.04E-06	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
200	1.35E+00	5.25E+03	2.63E+03	8.00E+00	6.72E-06	1.39E+05	7.44E+06	1.02E+06	3.73E+00	1.68E-01
300	2.03E+00	3.50E+03	1.75E+03	1.20E+01	1.01E-05	1.39E+05	7.43E+06	1.01E+06	3.73E+00	1.68E-01
500	3.38E+00	2.10E+03	1.05E+03	2.00E+01	1.68E-05	1.39E+05	7.42E+06	1.01E+06	3.73E+00	1.68E-01
700	4.73E+00	1.50E+03	7.55E+02	2.80E+01	2.35E-05	1.39E+05	7.39E+06	1.01E+06	3.72E+00	1.67E-01
1000	6.75E+00	1.06E+03	5.32E+02	4.00E+01	3.36E-05	1.39E+05	7.34E+06	1.01E+06	3.71E+00	1.66E-01
1500	1.01E+01	7.10E+02	3.60E+02	6.00E+01	5.04E-05	1.39E+05	7.23E+06	1.00E+06	3.68E+00	1.64E-01
2200	1.49E+01	4.92E+02	2.53E+02	8.80E+01	7.39E-05	1.39E+05	7.00E+06	9.86E+05	3.62E+00	1.58E-01
3000	2.03E+01	3.70E+02	1.95E+02	1.20E+02	1.01E-04	1.39E+05	6.65E+06	9.62E+05	3.53E+00	1.51E-01
5000	3.38E+01	2.44E+02	1.39E+02	2.00E+02	1.68E-04	1.40E+05	5.60E+06	8.86E+05	3.24E+00	1.27E-01
7000	4.73E+01	1.97E+02	1.22E+02	2.80E+02	2.35E-04	1.42E+05	4.51E+06	8.00E+05	2.91E+00	1.03E-01
10000	6.75E+01	1.73E+02	1.20E+02	4.00E+02	3.36E-04	1.45E+05	3.17E+06	6.79E+05	2.44E+00	7.37E-02

Typical substrate with a p-well and without a p+-overlap region under the gate

W [µm]	Rgate [Ohm]	Rsub3 [Ohm]	Rserie [Ohm]	Ctot [pF]	g [1/Ohm]	fmin [Hz]	ftop [Hz]	fopt [Hz]	Qopt	Q (f = 45 MHz)
10	6.75E-02	3.05E+03	1.52E+03	4.00E-01	3.36E-07	1.34E+05	2.61E+08	5.91E+06	2.21E+01	5.70E+00
20	1.35E-01	1.52E+03	7.62E+02	8.00E-01	6.72E-07	1.34E+05	2.61E+08	5.91E+06	2.21E+01	5.70E+00
40	2.70E-01	7.62E+02	3.81E+02	1.60E+00	1.34E-06	1.34E+05	2.61E+08	5.91E+06	2.21E+01	5.70E+00
60	4.05E-01	5.08E+02	2.54E+02	2.40E+00	2.02E-06	1.34E+05	2.61E+08	5.90E+06	2.21E+01	5.69E+00
80	5.40E-01	3.82E+02	1.91E+02	3.20E+00	2.69E-06	1.34E+05	2.60E+08	5.90E+06	2.21E+01	5.69E+00
100	6.75E-01	3.05E+02	1.53E+02	4.00E+00	3.36E-06	1.34E+05	2.60E+08	5.90E+06	2.20E+01	5.68E+00
150	1.01E+00	2.04E+02	1.03E+02	6.00E+00	5.04E-06	1.34E+05	2.58E+08	5.88E+06	2.20E+01	5.65E+00
200	1.35E+00	1.54E+02	7.76E+01	8.00E+00	6.72E-06	1.34E+05	2.56E+08	5.86E+06	2.19E+01	5.61E+00
300	2.03E+00	1.04E+02	5.28E+01	1.20E+01	1.01E-05	1.34E+05	2.51E+08	5.80E+06	2.17E+01	5.49E+00
500	3.38E+00	6.43E+01	3.39E+01	2.00E+01	1.68E-05	1.34E+05	2.35E+08	5.61E+06	2.10E+01	5.14E+00
700	4.73E+00	4.83E+01	2.65E+01	2.80E+01	2.35E-05	1.34E+05	2.14E+08	5.36E+06	2.00E+01	4.70E+00
1000	6.75E+00	3.72E+01	2.20E+01	4.00E+01	3.36E-05	1.34E+05	1.81E+08	4.92E+06	1.84E+01	3.97E+00
1500	1.01E+01	3.04E+01	2.03E+01	6.00E+01	5.04E-05	1.34E+05	1.31E+08	4.18E+06	1.56E+01	2.88E+00
2200	1.49E+01	2.87E+01	2.18E+01	8.80E+01	7.39E-05	1.34E+05	8.29E+07	3.33E+06	1.25E+01	1.84E+00
3000	2.03E+01	3.04E+01	2.53E+01	1.20E+02	1.01E-04	1.34E+05	5.22E+07	2.65E+06	9.88E+00	1.16E+00
5000	3.38E+01	3.98E+01	3.68E+01	2.00E+02	1.68E-04	1.35E+05	2.15E+07	1.71E+06	6.34E+00	4.80E-01
7000	4.73E+01	5.16E+01	4.94E+01	2.80E+02	2.35E-04	1.37E+05	1.14E+07	1.25E+06	4.61E+00	2.55E-01
10000	6.75E+01	7.05E+01	6.90E+01	4.00E+02	3.36E-04	1.40E+05	5.62E+06	8.88E+05	3.25E+00	1.28E-01

Table 3.3: The calculation of the parameters in accumulation for different gate widths with a p^+-overlap region, whereby $L_{\text{gate-sub.cont.}}(\text{with overlap}) = \lambda = 2$ µm.

Low resistivity substrate with a p+-overlap under the gate

W [µm]	Rgate [Ohm]	Rsub1 [Ohm]	Rserie [Ohm]	Ctot [pF]	g [1/Ohm]	fmin [Hz]	ftop [Hz]	fopt [Hz]	Qopt	Q (f = 45 MHz)
10	6.75E-02	1.58E+02	7.89E+01	4.00E-01	3.36E-07	1.34E+05	5.04E+09	2.60E+07	9.71E+01	8.41E+01
20	1.35E-01	7.90E+01	3.96E+01	8.00E-01	6.72E-07	1.34E+05	5.03E+09	2.59E+07	9.70E+01	8.39E+01
40	2.70E-01	3.97E+01	2.00E+01	1.60E+00	1.34E-06	1.34E+05	4.98E+09	2.58E+07	9.65E+01	8.33E+01
60	4.05E-01	2.67E+01	1.35E+01	2.40E+00	2.02E-06	1.34E+05	4.90E+09	2.56E+07	9.57E+01	8.22E+01
80	5.40E-01	2.03E+01	1.04E+01	3.20E+00	2.69E-06	1.34E+05	4.78E+09	2.53E+07	9.46E+01	8.08E+01
100	6.75E-01	1.64E+01	8.56E+00	4.00E+00	3.36E-06	1.34E+05	4.65E+09	2.49E+07	9.32E+01	7.90E+01
150	1.01E+00	1.15E+01	6.27E+00	6.00E+00	5.04E-06	1.34E+05	4.23E+09	2.38E+07	8.89E+01	7.35E+01
200	1.35E+00	9.24E+00	5.29E+00	8.00E+00	6.72E-06	1.34E+05	3.76E+09	2.24E+07	8.38E+01	6.69E+01
300	2.03E+00	7.28E+00	4.65E+00	1.20E+01	1.01E-05	1.34E+05	2.85E+09	1.95E+07	7.30E+01	5.33E+01
500	3.38E+00	6.53E+00	4.95E+00	2.00E+01	1.68E-05	1.34E+05	1.61E+09	1.47E+07	5.48E+01	3.23E+01
700	4.73E+00	6.98E+00	5.85E+00	2.80E+01	2.35E-05	1.34E+05	9.71E+08	1.14E+07	4.26E+01	2.03E+01
1000	6.75E+00	8.33E+00	7.54E+00	4.00E+01	3.36E-05	1.34E+05	5.28E+08	8.40E+06	3.14E+01	1.13E+01
1500	1.01E+01	1.12E+01	1.07E+01	6.00E+01	5.04E-05	1.34E+05	2.49E+08	5.77E+06	2.16E+01	5.44E+00
2200	1.49E+01	1.56E+01	1.52E+01	8.80E+01	7.39E-05	1.34E+05	1.19E+08	3.99E+06	1.49E+01	2.62E+00
3000	2.03E+01	2.08E+01	2.05E+01	1.20E+02	1.01E-04	1.34E+05	6.45E+07	2.94E+06	1.10E+01	1.43E+00
5000	3.38E+01	3.41E+01	3.39E+01	2.00E+02	1.68E-04	1.35E+05	2.33E+07	1.78E+06	6.61E+00	5.21E-01
7000	4.73E+01	4.75E+01	4.74E+01	2.80E+02	2.35E-04	1.37E+05	1.19E+07	1.27E+06	4.71E+00	2.66E-01
10000	6.75E+01	6.77E+01	6.76E+01	4.00E+02	3.36E-04	1.40E+05	5.75E+06	8.97E+05	3.28E+00	1.31E-01

Typical substrate with a p^+-overlap under the gate

W [µm]	Rgate [Ohm]	Rsub2 [Ohm]	Rserie [Ohm]	Ctot [pF]	g [1/Ohm]	fmin [Hz]	ftop [Hz]	fopt [Hz]	Qopt	Q (f = 45 MHz)
10	6.75E-02	1.75E+04	8.75E+03	4.00E-01	3.36E-07	1.34E+05	4.53E+07	2.47E+06	9.21E+00	1.01E+00
20	1.35E-01	8.75E+03	4.38E+03	8.00E-01	6.72E-07	1.34E+05	4.53E+07	2.47E+06	9.21E+00	1.01E+00
40	2.70E-01	4.38E+03	2.19E+03	1.60E+00	1.34E-06	1.34E+05	4.53E+07	2.47E+06	9.21E+00	1.01E+00
60	4.05E-01	2.92E+03	1.46E+03	2.40E+00	2.02E-06	1.34E+05	4.53E+07	2.47E+06	9.21E+00	1.01E+00
80	5.40E-01	2.19E+03	1.09E+03	3.20E+00	2.69E-06	1.34E+05	4.53E+07	2.47E+06	9.21E+00	1.01E+00
100	6.75E-01	1.75E+03	8.76E+02	4.00E+00	3.36E-06	1.34E+05	4.53E+07	2.47E+06	9.20E+00	1.01E+00
150	1.01E+00	1.17E+03	5.84E+02	6.00E+00	5.04E-06	1.34E+05	4.53E+07	2.47E+06	9.20E+00	1.01E+00
200	1.35E+00	8.76E+02	4.39E+02	8.00E+00	6.72E-06	1.34E+05	4.52E+07	2.47E+06	9.19E+00	1.00E+00
300	2.03E+00	5.85E+02	2.94E+02	1.20E+01	1.01E-05	1.34E+05	4.50E+07	2.46E+06	9.18E+00	1.00E+00
500	3.38E+00	3.53E+02	1.78E+02	2.00E+01	1.68E-05	1.34E+05	4.45E+07	2.45E+06	9.12E+00	9.88E-01
700	4.73E+00	2.55E+02	1.30E+02	2.80E+01	2.35E-05	1.35E+05	4.37E+07	2.42E+06	9.04E+00	9.71E-01
1000	6.75E+00	1.82E+02	9.43E+01	4.00E+01	3.36E-05	1.35E+05	4.21E+07	2.38E+06	8.87E+00	9.36E-01
1500	1.01E+01	1.27E+02	6.85E+01	6.00E+01	5.04E-05	1.35E+05	3.86E+07	2.28E+06	8.50E+00	8.59E-01
2200	1.49E+01	9.44E+01	5.46E+01	8.80E+01	7.39E-05	1.35E+05	3.30E+07	2.11E+06	7.85E+00	7.34E-01
3000	2.03E+01	7.86E+01	4.94E+01	1.20E+02	1.01E-04	1.35E+05	2.67E+07	1.90E+06	7.07E+00	5.95E-01
5000	3.38E+01	6.88E+01	5.13E+01	2.00E+02	1.68E-04	1.36E+05	1.54E+07	1.45E+06	5.37E+00	3.45E-01
7000	4.73E+01	7.23E+01	5.98E+01	2.80E+02	2.35E-04	1.38E+05	9.38E+06	1.14E+06	4.19E+00	2.11E-01
10000	6.75E+01	8.50E+01	7.63E+01	4.00E+02	3.36E-04	1.41E+05	5.08E+06	8.46E+05	3.08E+00	1.16E-01

Typical substrate with a p-well and a p+-overlap under the gate

W [µm]	Rgate [Ohm]	Rsub3 [Ohm]	Rserie [Ohm]	Ctot [pF]	g [1/Ohm]	fmin [Hz]	ftop [Hz]	fopt [Hz]	Qopt	Q (f = 45 MHz)
10	6.75E-02	5.08E+02	2.54E+02	4.00E-01	3.36E-07	1.34E+05	1.57E+09	1.45E+07	5.41E+01	3.15E+01
20	1.35E-01	2.54E+02	1.27E+02	8.00E-01	6.72E-07	1.34E+05	1.56E+09	1.45E+07	5.41E+01	3.15E+01
40	2.70E-01	1.27E+02	6.38E+01	1.60E+00	1.34E-06	1.34E+05	1.56E+09	1.44E+07	5.40E+01	3.14E+01
60	4.05E-01	8.51E+01	4.27E+01	2.40E+00	2.02E-06	1.34E+05	1.55E+09	1.44E+07	5.39E+01	3.13E+01
80	5.40E-01	6.40E+01	3.23E+01	3.20E+00	2.69E-06	1.34E+05	1.54E+09	1.44E+07	5.37E+01	3.11E+01
100	6.75E-01	5.15E+01	2.61E+01	4.00E+00	3.36E-06	1.34E+05	1.53E+09	1.43E+07	5.34E+01	3.08E+01
150	1.01E+00	3.49E+01	1.79E+01	6.00E+00	5.04E-06	1.34E+05	1.48E+09	1.41E+07	5.26E+01	2.99E+01
200	1.35E+00	2.68E+01	1.41E+01	8.00E+00	6.72E-06	1.34E+05	1.42E+09	1.38E+07	5.15E+01	2.88E+01
300	2.03E+00	1.90E+01	1.05E+01	1.20E+01	1.01E-05	1.34E+05	1.26E+09	1.30E+07	4.86E+01	2.59E+01
500	3.38E+00	1.35E+01	8.46E+00	2.00E+01	1.68E-05	1.34E+05	9.41E+08	1.12E+07	4.19E+01	1.97E+01
700	4.73E+00	1.20E+01	8.35E+00	2.80E+01	2.35E-05	1.34E+05	6.80E+08	9.54E+06	3.57E+01	1.45E+01
1000	6.75E+00	1.18E+01	9.29E+00	4.00E+01	3.36E-05	1.34E+05	4.28E+08	7.57E+06	2.83E+01	9.26E+00
1500	1.01E+01	1.35E+01	1.18E+01	6.00E+01	5.04E-05	1.34E+05	2.24E+08	5.48E+06	2.05E+01	4.91E+00
2200	1.49E+01	1.72E+01	1.60E+01	8.80E+01	7.39E-05	1.34E+05	1.13E+08	3.89E+06	1.45E+01	2.49E+00
3000	2.03E+01	2.19E+01	2.11E+01	1.20E+02	1.01E-04	1.34E+05	6.27E+07	2.90E+06	1.08E+01	1.39E+00
5000	3.38E+01	3.48E+01	3.43E+01	2.00E+02	1.68E-04	1.35E+05	2.31E+07	1.77E+06	6.57E+00	5.15E-01
7000	4.73E+01	4.80E+01	4.76E+01	2.80E+02	2.35E-04	1.37E+05	1.18E+07	1.27E+06	4.70E+00	2.65E-01
10000	6.75E+01	6.80E+01	6.78E+01	4.00E+02	3.36E-04	1.40E+05	5.73E+06	8.96E+05	3.28E+00	1.30E-01

Table 3.4: The calculation of the parameters in accumulation for different gate widths without a p^+ overlap region, whereby $L_{\text{gate-sub.cont.}}(\text{no overlap}) = 6\lambda = 12$ µm.

Discussion about the dimensions of the test structure

The quality factor in accumulation is inferior *without* a p^+-overlap region below the gate. The best results are expected from the low resistivity substrate, followed by a typical substrate with a p-well and a typical substrate (without a p-well). A $Q > 10$ can be obtained at RF frequencies in accumulation and inversion, so an accurate and reliable electrical parameter extraction can follow in both regions. According to the calculations in accumulation, the typical substrate does not satisfy the test structure requirements.

The data in inversion (see also figure 3.2) and accumulation indicate a suitable gate width to choose. The choice was made to work with a teststructure of $W = 100$ µm with a fixed gate length $L = 2$ µm.

Non-quasistatic effects

The quasistatic (QS) model is used when the operating frequency is low, so the device is able to respond fast enough to follow the small-signal input signal. The charge present in the channel below the gate has no time dependency and is in a steady-state. If the opposite occurs, a channel propagation delay will be present and there is a distributed effect of the channel resistance. This is also known as the non-quasistatic (NQS) effect. The channel resistance is determined by adding two types of resistances : 1) the static dc channel resistance and 2) the excess-diffusion channel resistance. The latter is caused by the distributed nature of the channel, when high frequencies are applied and long channels are used [29]. Successively, the effective unit-area gate capacitance ($C_{\mathrm{gg,unit}}$) value will be lowered for devices with long channel lengths as the frequency increases. At relatively low RF frequencies the NQS effects can be ignored. The NQS effect is observed when the channel length is longer than 0.35 µm at frequencies above 1 GHz [30]. The longer the channel and the higher the frequency, the more drastic the NQS effect will be. The frequency after which the NQS effect must be taken into account, is close to the cut-off frequency f_{t} [31].

The NQS frequency is given by :

$$f_{\mathrm{NQS}} = \frac{\mathrm{n} \cdot \mu_{\mathrm{eff}} \cdot (V_{\mathrm{g}} - V_{\mathrm{th}})}{2 \cdot \pi \cdot L_{\mathrm{eff}}^2}, \tag{3.11}$$

where n is a fitting parameter that determines the accuracy of the simulation.

For an accurate result, the fitting parameter must be small and the operating frequency must be well below the f_{NQS} to be able to neglect the NQS effect. A factor of ten is used. The ratio between the instantaneous inversion charge and the inversion charge at low frequency is given by X. Two examples are given just to illustrate the effects of accuracy for the ratio X and the phase ϕ [°]. Respectively, an accurate and less accurate example from [31]. The fitting parameter n is extracted from the reference.

Example 1 :

With X $>$ 99% and $\phi < 1^{\mathrm{o}}$ the value of n < 0.032.

This gives: $f_{\mathrm{NQS}} = 0.5276$ [GHz] $\cdot$ n $= 16.9$ MHz.

Example 2 :

With X $>$ 90% and $\phi < 10^{\mathrm{o}}$ the value of n < 0.3.

This gives: $f_{\mathrm{NQS}} = 0.5276$ [GHz] $\cdot$ n $= 158.3$ MHz.

The NQS effects seems an issue in both examples. Two things can be done to minimize the chance of NQS effects: 1) decrease the (effective) length of the channel by putting the diffusion region(s) closer together, 2) increase the oxide thickness, to increase the mobility, assuming the oxide voltage stays the same. In this research only the first case is an option.

3.2 Layout of the test structures

In this section the optimization of the test structure with a low-series resistance (figure 3.1) is discussed.

An extra substrate contact is placed in parallel to halve the resistance caused by the substrate contact. This causes the gate to be split up in 2 gate fingers of 50 µm in width. A folded structure is formed. The symmetrical structure enables the use of the original open-short de-embedding as in figure 2.8 at relatively low radio frequencies.

The test and de-embedding structures have been created according to design

rules for GHz probing [32, 33]. The structures are scaled with a scaling parameter λ. The design rules will be shown in figure 3.3.

The wafer will contain different RF C-V structures that have small differences in:

- gate width W: 50, 100, 150 µm.
- gate length L: 1.0, 1.6, 1.8, 2.0, 2.2, 2.4, 4.0 µm.
- ground planes: standard and wide planes.
- scaling parameter λ: 1.4, 2.0 and 5.0 µm

Furthermore, RF C-V structures are designed with the substrate contact placed below the gate (overlap) and just beside the gate. Van der Pauw structures are designed to measure the sheet resistivity and structures are designed to measure the contact resistance.

The interconnect lines of the open de-embedding structures end at the active area of the device. At the next revision the interconnect lines have to be extended to the contact holes to reduce the influence of the inductance.

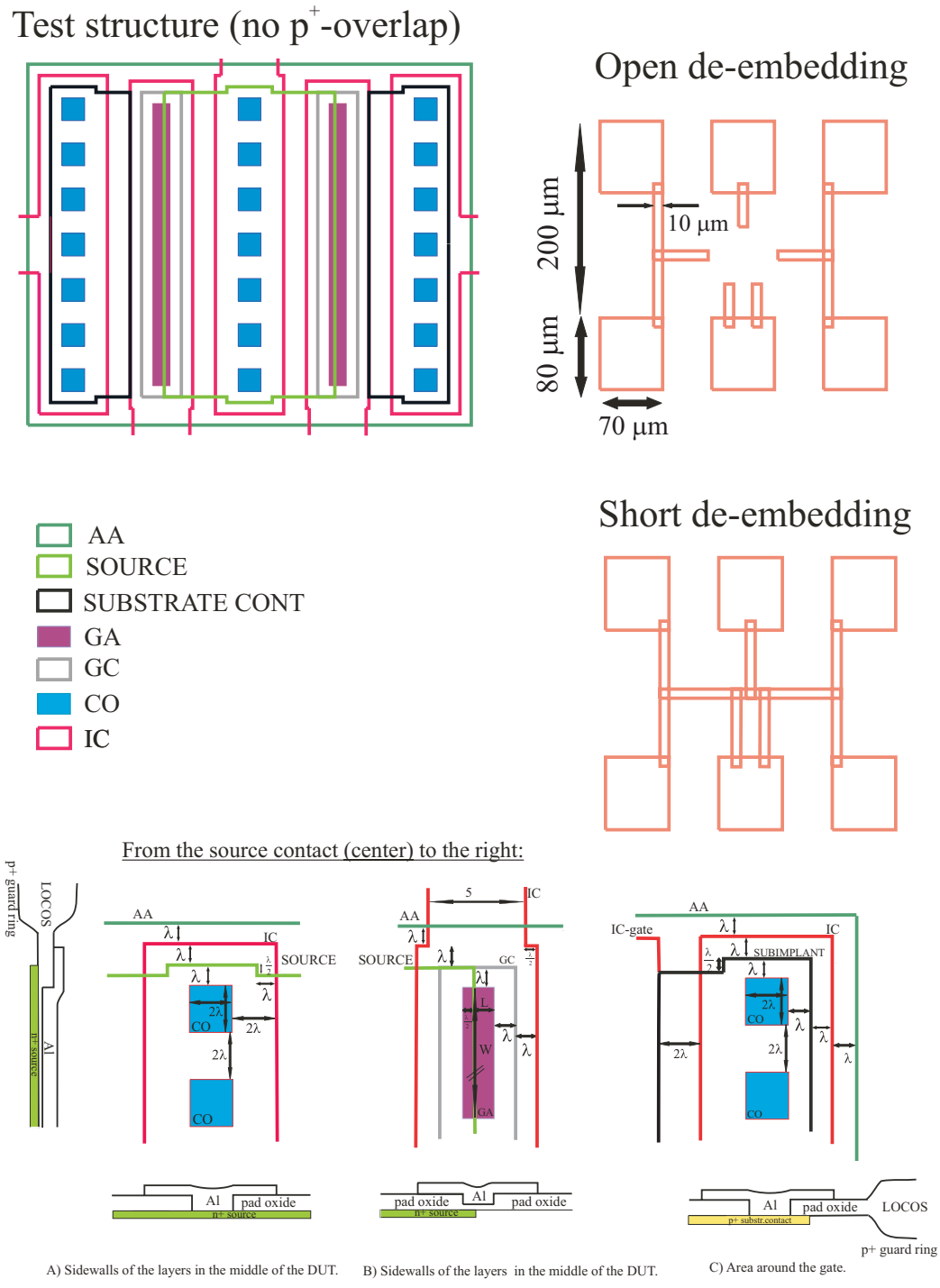

Figure 3.3: Test structures without a gate overlap region for the substrate contacts and the de-embedding structures together with the layout rules.

Chapter 4

Experimental results

Previous work [3] indicates in general how radio frequency (RF) test structures can be created for devices with leaky gate dielectrics. The test structures must satisfy design rules in such a way that the structures can give a reliable extraction of device parameters from the RF measurements.

The goal in this research is to design test structures, fabricate them and perform RF characterization. Therefore previous statements are reviewed in the following sections to see how much agreement can be reached.

In this chapter the RF measurements are presented and in the last paragraph an outlook is given of the dimensions of the final test structure.

4.1 Verification of previous work

To learn and practise performing RF measurements, an Adict wafer from Philips is used. This wafer contains several test structures that are appropriate for RF C-V measurements.

The measurement results have been attained on a device with a gate length $L = 0.5$ µm, gate width $W = 20$ µm and N = 2 gate fingers. The frequency range is divided in 201 steps. The RF power is set to -10 dBm.

The results of the measurements are respectively:

1. $Re(Y_{11})$ and $Im(Y_{11})$ vs. frequency with a fixed V_g = -2 V,
2. $Re(Y_{11})$ vs. frequency with different values for V_g in or close to the inversion region,

3. Q vs. frequency with different values for V_g in or close to the inversion region, and

4. a C-V measurement that covers the accumulation, depletion and inversion regions with different frequencies.

A SOLT calibration must be completed before the device measurements and de-embedding procedure can start. The 1st measurement is done to prove the validity of equations 2.16 and 2.17 by S-parameter measurements on the 'Adict' wafer. Figure 4.1 confirms that the real part of Y_{11} is quadratically

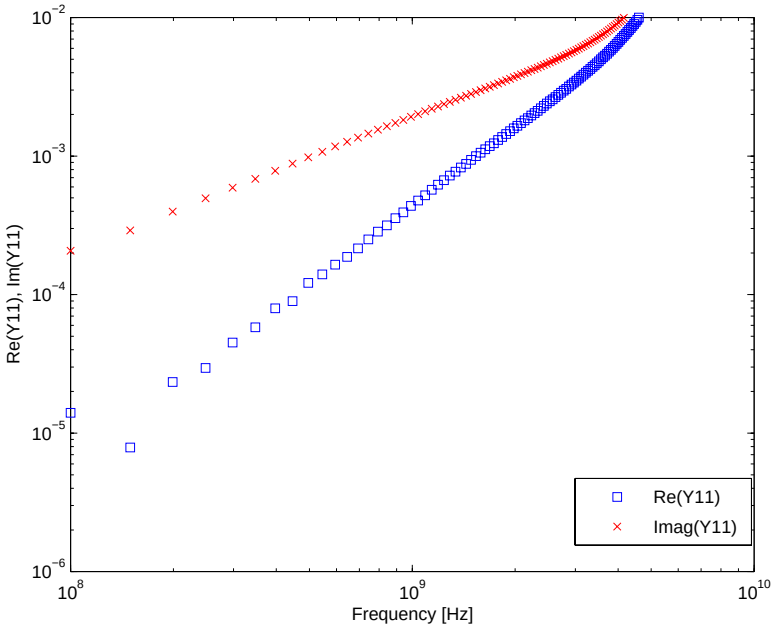

Figure 4.1: The real and imaginary part of Y_{11} vs. frequency with V_g = -2 V.

dependent on the frequency, whereas the imaginary part shows a linear relation. Both show a frequency dependency in accordance with [2, 22].

The 2nd measurement shows the influence of the gate voltage from 0.7 V to 1.9 V and the frequency on the gate leakage (see figure 4.2). An increase in gate voltage gives a higher leakage current. The leakage current shows a large effect on the $Re(Y_{11})$ at low frequencies (see equation 2.16). At higher frequencies the series resistance gives the highest contribution to $Re(Y_{11})$.

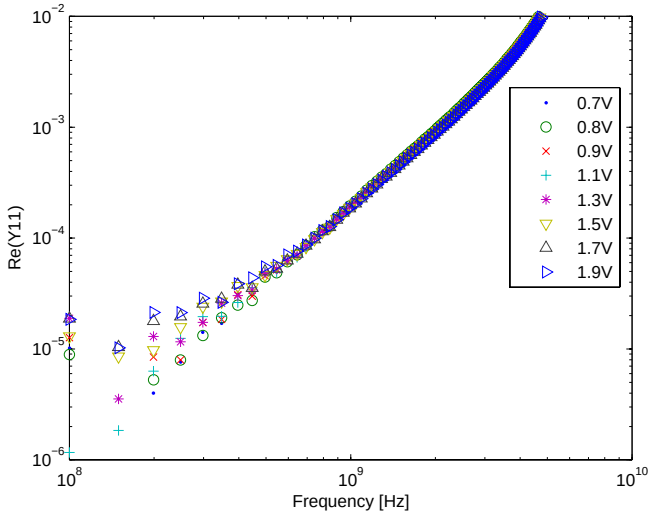

Figure 4.2: The real part of Y_{11} vs. frequency for different V_g.

The 3rd measurement result follows out of the 2nd measurement. The higher the leakage current, the lower the quality factor (see equation 2.7) at low frequencies.

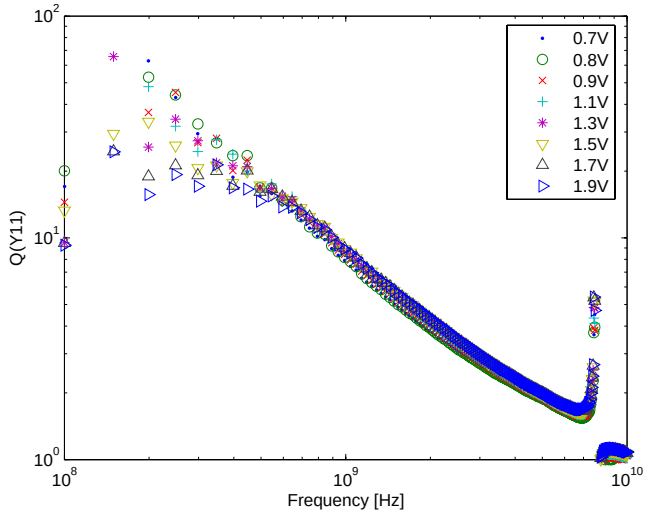

Figure 4.3: The quality factor of Y_{11} vs. frequency with different V_g.

At higher frequencies, equation 2.8 confirms that an increase in frequency

lowers the quality factor (see figure 4.3). The peak at $f = 8$ GHz was found in all measurements. This unwanted effect is not caused by a disturbance in the air i.e. by radar. It is possible that because of the usage of two different probes an oscillation occurs due to cavities.

The 4$^{\text{th}}$ measurement represents the RF C-V measurement at $f = 500$ MHz, 750 MHz, 850 MHz, 1 GHz and 2 GHz. The voltage is varied from -2.5 V to 2.5 V (see figure 4.4).

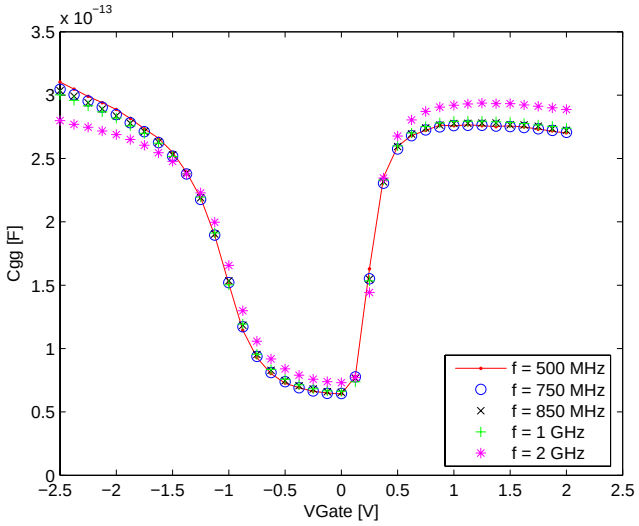

Figure 4.4: The RF C-V curve for different frequencies with $C_{\text{gg}} = \frac{Im(Y_{11})}{\omega}$.

The results in accumulation are in accordance with previous results by Schmitz et al. [2]. The overall results are identical as in [3]. The level drop of the device capacitance in accumulation at high frequencies is due to the series resistance. In inversion at $f = 2$ GHz the capacitance is higher than at lower frequencies. A different capacitance extraction method [34] was checked to try to overcome this effect. This method gives more accurate results, when the parasitic resistance of the gate, well, source/drain are 'large'. In contrast to the C_{gg} extraction method by means of Y-parameters, this method uses Z-parameters (see appendix C). Both methods were not able to remove the effect. The comparison of both capacitance extraction methods can be found in appendix D.

The intrinsic capacitance can be found by subtracting two RF C-V measurements of devices with the same design structure, but with different gate

lengths [2]. With the QM CV model from the Berkeley group [35], a fit with the intrinsic RF C-V curve can be created by altering the doping concentration and oxide thickness. The final oxide thickness is found by subtracting 0.2 nm of the fitting parameter of the oxide thickness to compensate for the accumulation charge centroid in the gate [36]. This parameter extraction model is implemented in Matlab code.

4.2 C-V measurement results

Considering the performance of different structures on-wafer, in addition to performing RF C-V measurements, several other measurements are performed.

On the first (typical) wafer, various device characteristics were checked: the threshold voltage of diodes (V_{th} = -0.66 V), the threshold voltage of an NMOS (V_{th} = 0.7 V), leakage current measurements (where breakdown occurs at an electric field $E_{\text{breakdown}} \approx 8$ MV/cm) and high frequency (HF) C-V measurements on a MOS capacitor.

HF C-V measurement

A HF C-V measurement on a MOS capacitor gives valuable information about the device characteristics.

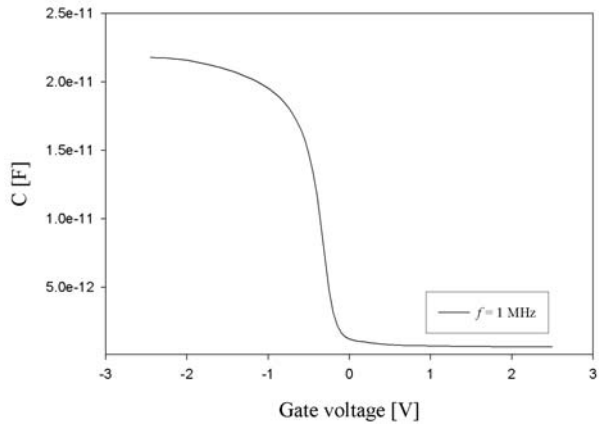

Figure 4.5: HF C-Vmeasurement on a MOS capacitor with W = 154 µm, L = 9 µm and $t_{\text{ox}} \approx 4.76$ nm.

Some of the gathered information of the parameters can be compared with the data obtained from the RF C-V measurement. The calculated parameters of this MOS capacitor can be found in the table below:

Calculated parameters	**Value**
Series resistance R in strong accumulation [Ω]	1720
Oxide capacitance C_{ox} [F]	$2.32{\cdot}10^{-11}$
Inversion capacitance C_{inv} [F]	$6.46{\cdot}10^{-13}$
Depletion capacitance C_{dep} [F]	$6.64{\cdot}10^{-13}$
Depletion width W_{dep} [nm]	216
Substrate doping N_{sub} [cm^{-3}]	$1.99{\cdot}10^{16}$
Debye length L_{d} [nm]	28.9
Flatband capacitance C_{fb} [F]	$4.09{\cdot}10^{-12}$
Flatband voltage V_{fb} [V]	-0.225
Gate oxide thickness t_{ox} [nm]	4.758
Equivalent oxide thickness EOT [nm]	2.062
Bulk potential V_{bulk} [V]	0.377
Work function ϕ_{ms} [V]	-0.39
Interface state concentration N_{ss} [cm^{-2}]	$1.74{\cdot}10^{12}$

Table 4.1: Calculated parameters of the MOS capacitor with W = 154 µm, L = 9 µm, $\kappa_{\mathrm{Al_2O_3}} = 9$ and $\phi_{\mathrm{TiN}} = 4.7$ V.

RF C-V measurements

Differently shaped RF C-V structures have been made and are investigated. The structures differ in area, groundplanes and the presence of a p^+-overlap region under the gate. One of the main objectives was to extract the oxide capacitance C_{ox} and the series resistance R in accumulation. On the low resistivity substrate a number of successful RF C-V measurements in accumulation have been obtained.

Results of structures with small groundplanes and a p^+-overlap region

The results of the 1st device with $W = 100$ µm, $L = 2.2$ µm, *small groundplanes* and a *p^+-overlap region* under the gate, are shown in figure 4.6 and in figure 4.7. The 2nd device only differs in the gate length L = 4 µm (see

figure 4.8 and figure 4.9)*. Enough information is available to determine the intrinsic device C-V curve from both RF C-V curves (see figure 4.10).

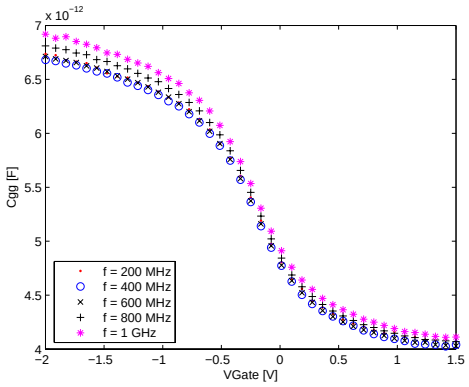

Figure 4.6: The device capacitance C_{gg} vs. the gate voltage V_g of the first RF C-V teststructure with $W = 100$ µm and $L = 2.2$ µm.

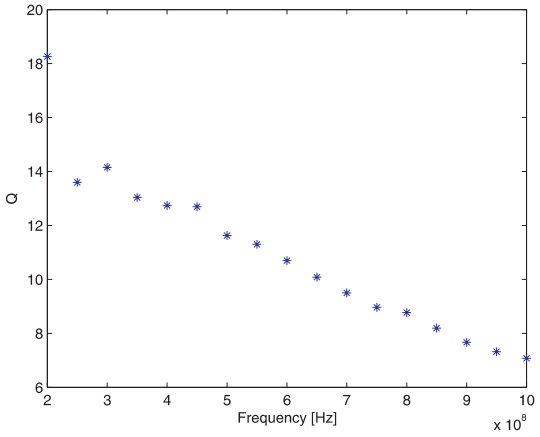

Figure 4.7: The quality factor Q vs. the frequency f of the first RF C-V teststructure.

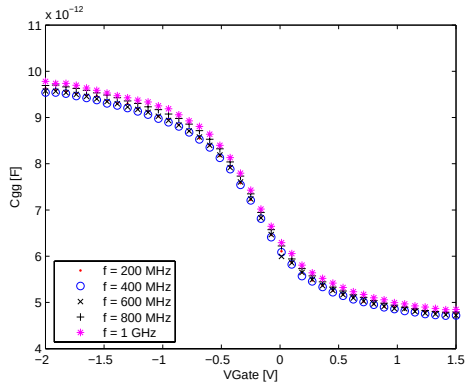

Figure 4.8: The device capacitance C_{gg} vs. the gate voltage V_g of the second RF C-V teststructure with $W = 100$ µm and $L = 4$ µm.

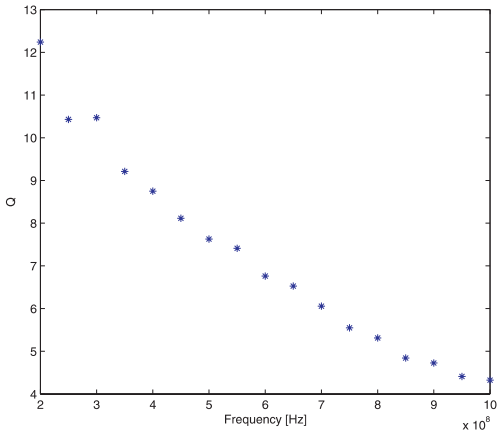

Figure 4.9: The quality factor Q vs. the frequency f of the second RF C-V teststructure.

*Likewise with the wafer of Philips, the extraction method of G. Sasse [34] is tested.

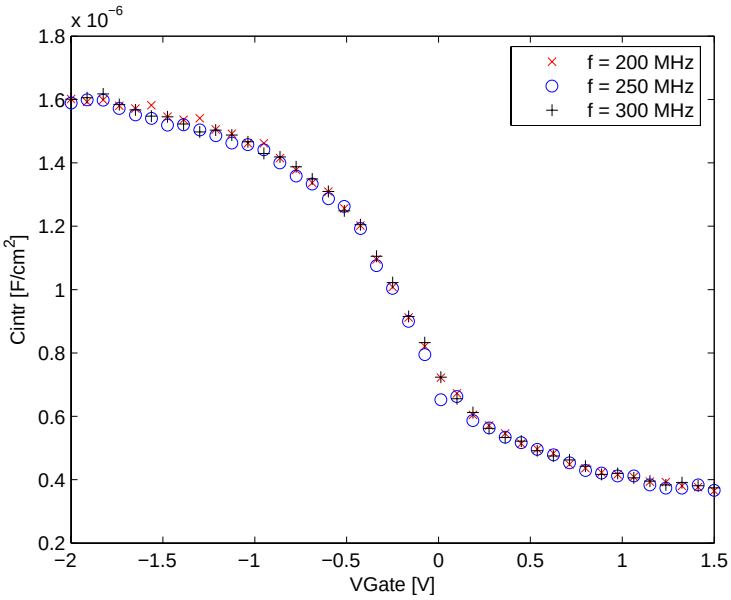

Figure 4.10: Intrinsic RF C-V curve for devices with a p^+-overlap region under the gate, small ground planes and for frequencies that indicate $Q > 10$.

Discussion of the measurement results

Both devices show a good quality factor ($Q > 10$) in accumulation. The RF C-V intrinsic plot in figure 4.10 shows the frequencies with the most optimal Q. At the end of the frequency range ($Q < 10$) the previous two $C_{\mathrm{gg}} - V$ figures show a frequency dependency.

The device does not end up in inversion at the right part of the x-axis in the C-V plot. This non-ideal situation can be caused if the source is (partly) depleted. The electron charge carriers in the source would decrease, which makes it more difficult for the device to end up in inversion. The width of the depletion layer of the p-n junction is calculated [37] to check if this is the problem. The depletion width in the substrate:

$$x_{\mathrm{p}} = \sqrt{\frac{2 \cdot \kappa_{\mathrm{Si}} \cdot \varepsilon_0}{q} \cdot \phi_{\mathrm{bi}} \cdot \frac{N_{\mathrm{D}}}{N_{\mathrm{A}}(N_{\mathrm{A}} + N_{\mathrm{D}})}} \tag{4.1}$$

and the depletion width in the source:

$$x_{\mathrm{n}} = \sqrt{\frac{2 \cdot \kappa_{\mathrm{Si}} \cdot \varepsilon_0}{q} \cdot \phi_{\mathrm{bi}} \cdot \frac{N_{\mathrm{A}}}{N_{\mathrm{D}}(N_{\mathrm{A}} + N_{\mathrm{D}})}}, \tag{4.2}$$

with the built-in potential ϕ_{bi} in the p-n junction:

$$\phi_{\mathrm{bi}} = \frac{kT}{q} \cdot \frac{N_{\mathrm{d}} \cdot N_{\mathrm{a}}}{n_{\mathrm{i}}^2} \tag{4.3}$$

The bandgap $\Delta E(N)$ of this low resistivity silicon substrate shrinks by -40.2 meV due to the dependency of the doping. For the calculations above the intrinsic concentration $n_{\mathrm{i}} = 1.93{\cdot}10^{10}$ cm^{-3}, the donor doping N_{d} in the source $= 1.6{\cdot}10^{20}$ cm^{-3}, the acceptor doping N_{a} in the substrate $= 3.2{\cdot}10^{18}$ cm^{-3} and the built-in potential $\phi_{\mathrm{bi}} = 1.08$ eV.

The total depletion width becomes:

$$x_{\mathrm{d}} = x_{\mathrm{p}} + x_{\mathrm{n}} = 2.1 \cdot 10^{-2} + 4.14 \cdot 10^{-3} = 2.51 \cdot 10^{-2}\ \mu\mathrm{m} \tag{4.4}$$

According to Silvaco simulation results the depletion width in the source x_{n} is much smaller than the p-n junction depth $x_{\mathrm{j}} = 1.585 \cdot 10^{-1}$ µm.

To verify if the device is scaled correctly, the minimum channel length is tested with the scaling law of Brews (see equation 3.1). Only the source gives a contribution in Brews' law, because no drain exists. When $t_{\mathrm{ox}} = 45$ Å, the junction depth $x_{\mathrm{j}} = 0.1585$ µm and $W_{\mathrm{s}} = 2.51{\cdot}10^{-2}$ µm. The minimum channel length $L_{\mathrm{min}} = 0.06$ µm. The requirement of the minimum channel length is meet.

To find out more information about the device, energy diagrams must be made. These diagrams are used to detect space charges, electric fields, built-in voltages and currents within the device structure.

In accumulation, some useful device characteristics can be obtained from the intrinsic RF C-V plot. The oxide thickness can be calculated with equation 2.11. The gate oxide thickness $t_{\mathrm{ox}} = 4.98$ nm, when the assumption is used that the dielectric constant $\kappa_{\mathrm{Al_2O_3}} = 9$. The value of the thickness on

this low resistivity silicon wafer is very close to the oxide thickness of the HF C-V measurement *on a standard silicon wafer*.

A realistic value for κ is of importance to accurately determine the oxide thickness. The height of the exact value of κ can differ for Al_2O_3. Values of κ that range from 8 - 11 are reported in [38, 39]. In [6] differences in κ are explained by the presence of an interface layer, quantum mechanical effects, the Al_2O_3 film density and chemical composition. Figure 4.11 describes the consequences of various κ's on the gate oxide thickness.

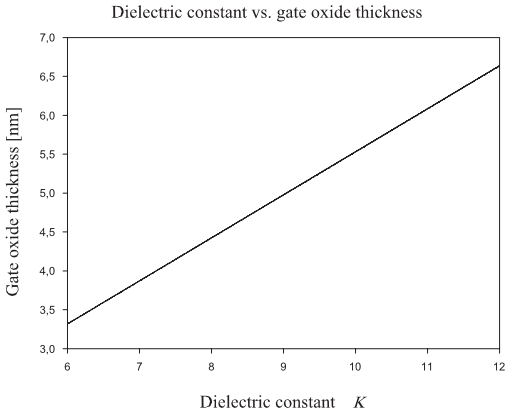

Figure 4.11: The dielectric constant vs. the gate oxide thickness, when $C_{\text{intr}} = 1.6{\cdot}10^{-6}$ [F/cm^2].

The expected oxide thickness is about $t_{\text{ox}} = 4.5$ nm for the process runs so far. This means $\kappa_{Al_2O_3} \approx 8.14$.

Series resistance

The series resistance R of both devices are smaller than 10 Ω. According to the theory in chapter 3 the resistance is a little bit lower then expected. This observation has a positive effect on the quality factor, when frequencies exceed the optimal frequency Q_{opt}.

Leakage current through the gate oxide

The differential conductance g is compared by looking at results obtained from the theory (see figure 2.10), measurement results on MOS capacitors

and results from the low resistance RF C-V structures. The difference in strong accumulation at V_g = -2 V is given in table 4.2.

	differential conductance g [Ω^{-1}]	**source**
Theory	$4.8 \cdot 10^{-7}$	figure 2.10
MOS capacitor	$2.3 \cdot 10^{-5}$	HF C-V measurement
Low R structures	$1.8 \cdot 10^{-4}$-$5.3 \cdot 10^{-4}$ ($200 \leq f$ [MHz] ≤ 400)	equation 2.16 & figure 4.12

Table 4.2: Differential conductances according to the theory and two different measurements.

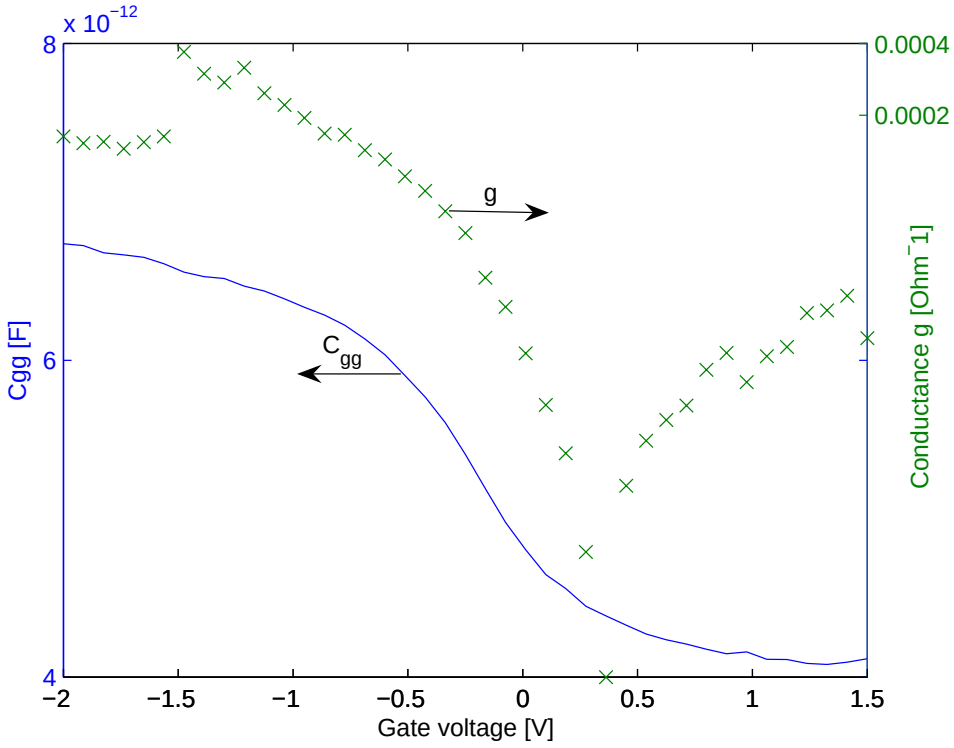

Figure 4.12: The measured device capacitance and conductance of the 1st teststructure with overlap, small groundplanes and f = 200 MHz.

The prediction of the differential conductance of a 4 nm Al_2O_3 oxide layer, without an interface layer, is much lower compared to the results of both measurements. The measurements were not performed on the same wafer. Progressing knowledge on the development of the recipe of the process flow

reveals why the leakage current could be very high. Until now two steps are being refined.

The first step is related to the deposition of the gate metal. The gate metal consists of aluminum and titaniumnitride (TiN). The aluminum is deposited on top of TiN. To free aluminum particles, from an aluminum target, argon ions in a plasma are accelerated to the aluminum target. The energy of the argon ions on impact determines the amount of sputtered aluminum atoms. The sputtered atoms end up on the TiN layer, forming an aluminum layer. The amount of energy involved in a sputtering process can degrade the quality of the oxide. The energy of the argon atoms should probably be decreased to reduce the charge in the aluminum. The oxide will contain less damage.

The second step involves the growth temperature of the gate oxide by atomic layer deposition (ALD). A thermocouple measures the temperature inside the growth chamber of the ALD system. The thermocouple does not measure the actual temperature of the wafer. The temperature is controlled by two resistive heating elements inside the reactor. The first heating element is situated directly below the wafer and gets the same power, but has a different power-density. The second heating element is located in the cover of the deposition reactor. The oxide is supposed to be deposited at 300 °C. If the temperature of the wafer ends up above 350 °C, while the temperature of the thermocouple indicates 300 °C, the layer-by-layer growth rate by ALD drops significantly.

Results of structures with large groundplanes and a p^+-overlap region

The results of the 1st device with $W = 100$ µm, $L = 2$ µm, *large groundplanes* and a p^+*-overlap region* under the gate, are shown in figure 4.13 and 4.14. The 2nd device only differs in the gate length L = 2.4 µm (see figure 4.15 and figure 4.16). In appendix E the extraction method of G. Sasse [34] is tested. To find the intrinsic device C-V curve, both curves have to normalized to area and subtracted from another (see figure 4.17).

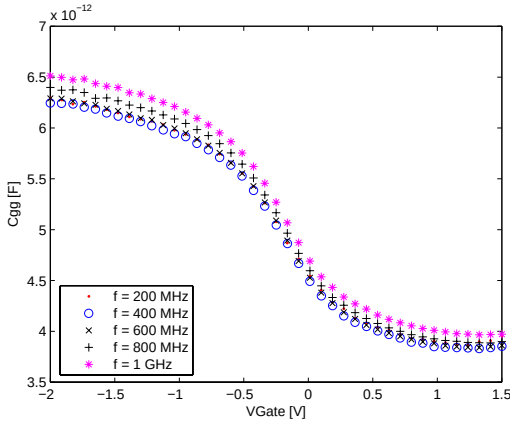

Figure 4.13: The device capacitance C_{gg} vs. the gate voltage V_{g} of the first RF C-V teststructure with $W = 100$ µm and $L = 2$ µm.

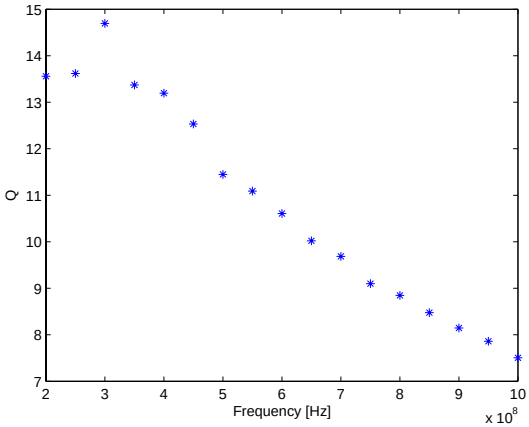

Figure 4.14: The quality factor Q vs. the frequency f of the first RF C-V teststructure.

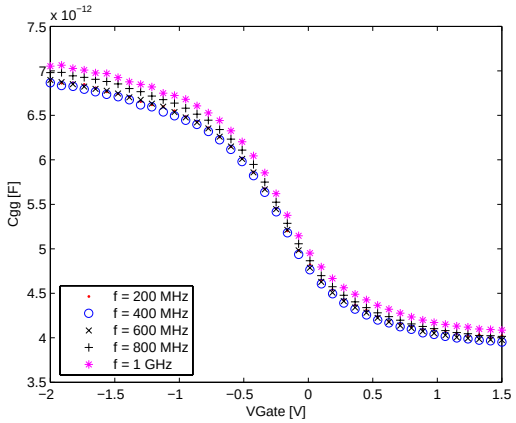

Figure 4.15: The device capacitance C_{gg} vs. the gate voltage V_{g} of the second RF C-V teststructure with $W = 100$ µm and $L = 2.4$ µm.

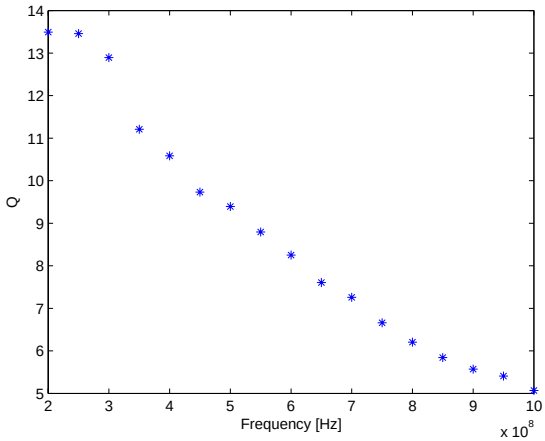

Figure 4.16: The quality factor Q vs. the frequency f of the second RF C-V teststructure.

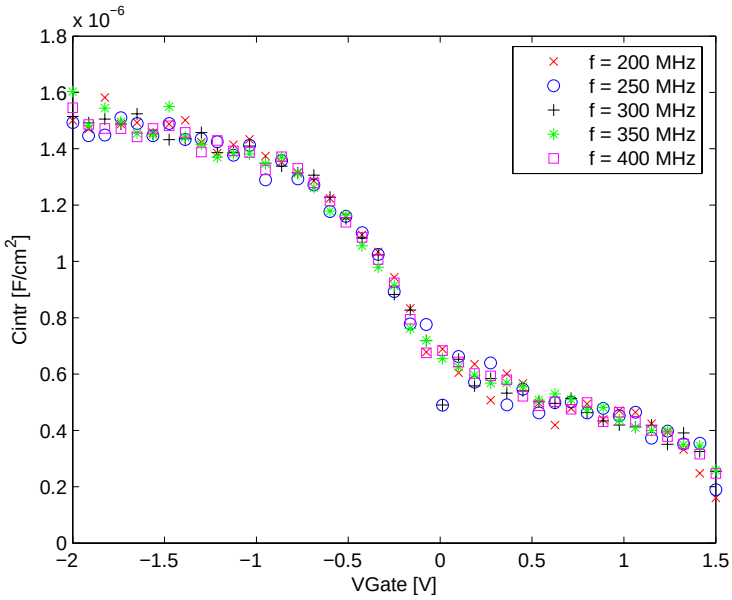

Figure 4.17: Intrinsic RF C-V curve for devices with a p^+-overlap region under the gate, large ground planes and with frequencies that show $Q > 10$.

Discussion of the measurement results

In accumulation, both devices can satisfy the requirement of the quality factor if 200 MHz $< f <$ 400 MHz. The average value of the $C_{\text{intr}} = 1.55{\cdot}10^{-6}$ F/cm^2, so the gate oxide thickness $t_{\text{ox}} \approx 5.14$ nm. According to figure 4.11 the dielectric constant $\kappa \approx 9$. In strong accumulation, the intrinsic capacitance differs with frequency, which makes it more difficult to extract just one intrinsic capacitance. For example: If $f = 350$ MHz, the oxide thickness is exactly the same as previously obtained from figure 4.10, for structures with a p^+-*overlap* and *small groundplanes*. A little deviation can give $\Delta t_{\text{ox}} = 0.2$ nm in this case. The fluctuations are possibly attributed to the large capacitance value caused by the large groundplanes, compared to the capacitance of the device.

As far as the series resistance and the leakage current is concerned, the series resistance R of both devices are also smaller than 12 Ω. This observation has a positive effect on the quality factor, when frequencies exceed the optimal frequency Q_{opt}. In figure 4.18 the differential conductance $g = 3{\cdot}10^{-4}$ Ω^{-1} at f = 200 MHz. Compared to the expected theoretical value, this value is rather high.

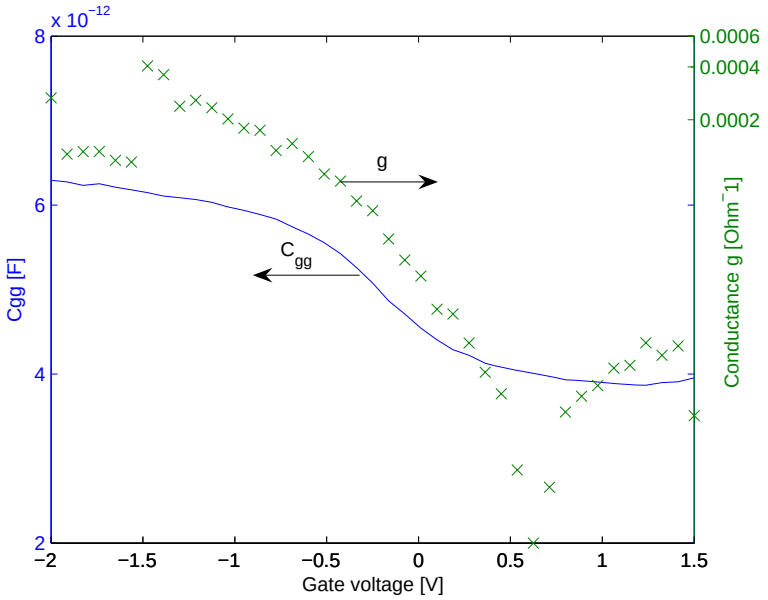

Figure 4.18: The C_{gg} and g of the 1st teststructure with overlap, large groundplanes and $f = 200$ MHz.

Results of structures with small groundplanes and without a p^+-overlap region

Two structures are tested with small groundplanes, without an overlap region, $W = 100$ µm and lengths of $L = 2.2$ µm and $L = 4$ µm. The RF C-V measurement results are plotted in figure 4.19 - 4.22. The number of frequency steps is divided in two to minimize the stress on the devices. The selected frequency range will show the most promising results for these structures. Keep in mind that the figures of the quality factor for both structures have to be carefully compared to the previously found results in this section.

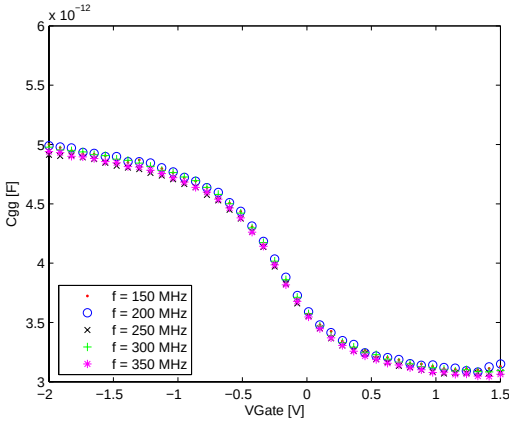

Figure 4.19: The device capacitance C_{gg} vs. the gate voltage V_g of the first RF C-V teststructure with $W = 100$ µm and $L = 2.2$ µm.

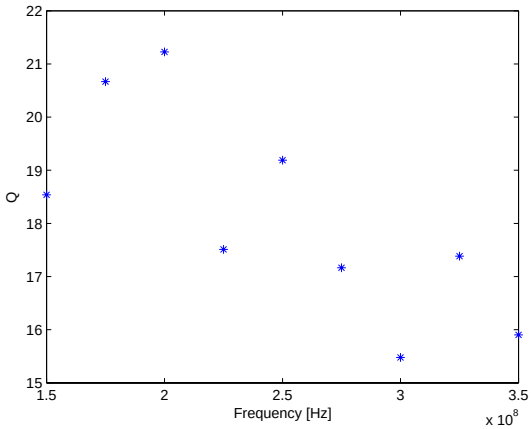

Figure 4.20: The quality factor Q vs. the frequency f of the 1st RF C-V teststructure.

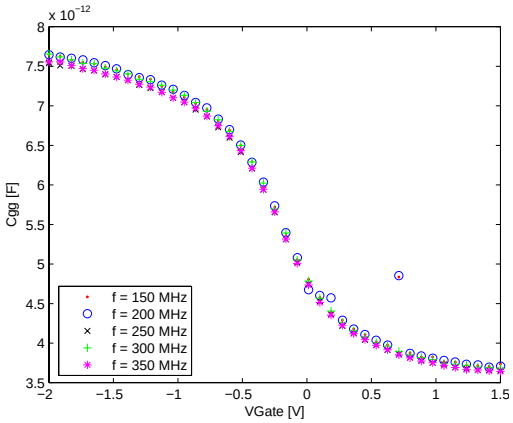

Figure 4.21: The device capacitance C_{gg} vs. the gate voltage V_g of the second RF C-V teststructure with $W = 100$ µm and $L = 4$ µm.

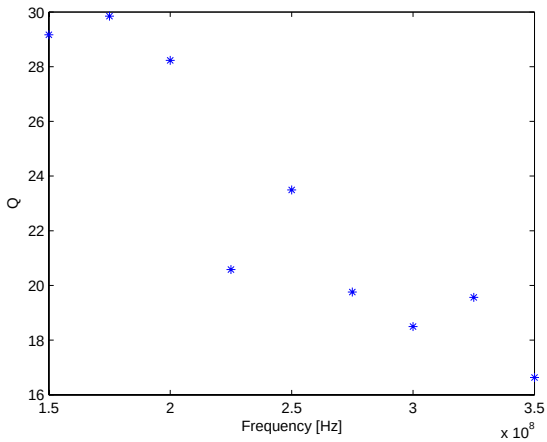

Figure 4.22: The quality factor Q vs. the frequency f of the 2nd RF C-V teststructure.

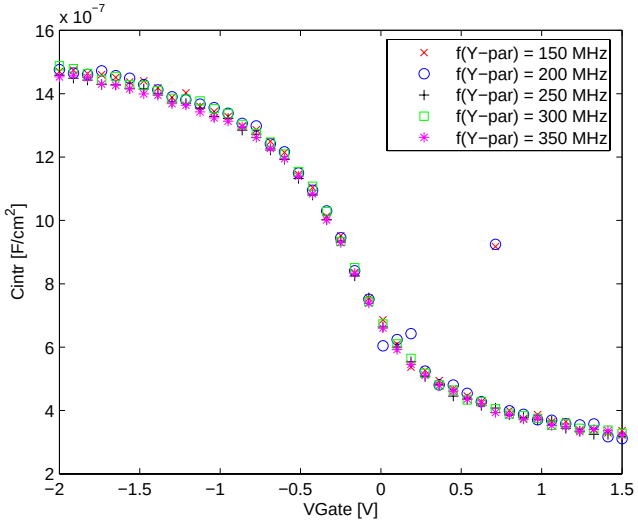

Figure 4.23: Intrinsic RF C-V curve for devices without a p^+-overlap region, small ground planes and with frequencies that show $Q > 10$.

In figure 4.23 the measurement points at $f = 150$ MHz and $f = 200$MHz, between $V_g = 0$ V and $V_g = 0.75$ V are measurement errors.

Discussion of the measurement results

The intrinsic capacitance $C_{intr} \approx 1.47 \cdot 10^{-6}$ F/cm^2, so the gate oxide thickness $t_{ox} = 5.42$ nm. According to figure 4.11, the dielectric constant $\kappa = 9.7$. In strong accumulation, the series resistance $R < 20\ \Omega$ for both devices. The differential conductance $g = 0.3 \cdot 10^{-4}\ \Omega^{-1}$.

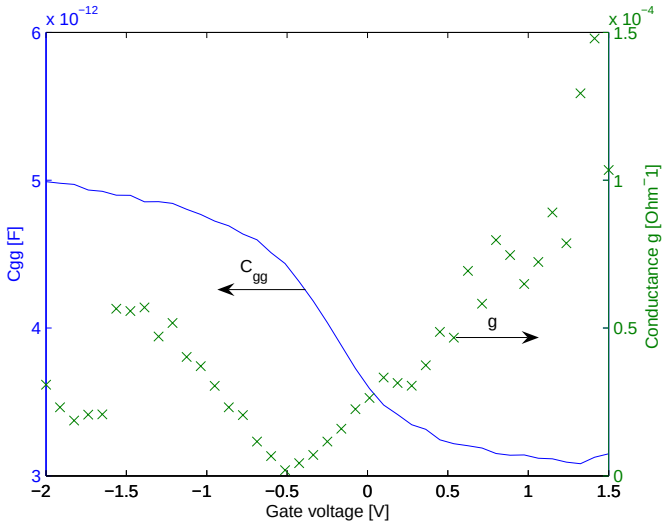

Figure 4.24: The C_{gg} and g of the 1$^{\mathrm{st}}$ teststructure without overlap, small groundplanes and $f = 200$ MHz.

Energybands of the low resistance RF C-V teststructures

Energy band diagrams are used to achieve a better understanding about the current flow through the gate oxide. In this section the energy band diagrams of the RF C-V teststructures in accumulation and inversion on a p-type substrate are discussed. The conduction band offset of the Al_2O_3 gate oxide is 2.8 eV, the valence band offset is 4.9 eV and the bandgap is 8.8 eV. Comparing the band offsets with those of SiO_2 the conductance band offset is 3.5 eV, the valence band offset is 4.4 eV and the bandgap is 9 eV [5]. The Al_2O_3 has a lower conduction band offset, a higher valence band offset and the bandgap approximately the same. Since the effective mass and barrier height of electrons is lower compared to holes, injection of electrons into the oxide is more likely to occur.

Energy band diagram in strong accumulation

A negative potential is applied on the gate, if a device operates in strong accumulation. The main leakage current will flow from the metal conduction

band to lower energy levels in the p-substrate and holes are attracted towards the Si-Al_2O_3 interface.

Energy band diagram in strong inversion

A positive potential is applied on the gate, if a device is in strong inversion. A leakage current of electrons goes from the substrate to the gate. The electrons that form a channel, are coming from the substrate and the n^+ source. The electrons are mainly coming from the heavily doped n^+-source.

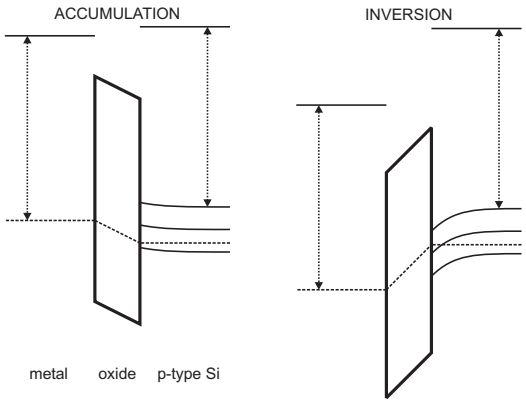

Figure 4.25: Energy diagrams of the structures in accumulation and inversion.

Chapter 5

Conclusions

Different innovative RF C-V test structures are presented for material research. The low series resistance RF C-V structures have been fabricated. Measurements performed on the low resistivity substrate indicate that the test structure requirements are satisfied. The measured series resistance values for the structures with an overlap region are very close to the calculated theoretical values. However, the differential conductance across the 4 nm thin Al_2O_3 gate oxide is 1000 times higher than expected for both structures. A low yield of the devices at relatively low electric fields, across the gate oxide, drastically decreased the number of successful measurements. Remarks are made about the gathered results.

Electrical device characteristics were obtained in accumulation for all types of low resistance RF C-V structures. The structures with a p^+-overlap region and small groundplanes show the most unambiguous and promising RF C-V measurement results. The influence of larger groundplanes decreases the precision with which the intrinsic capacitance value in accumulation can be determined. It is possible that the large groundplanes have a much larger capacitance value than the device capacitance, which causes the fluctuations.

The high amount of acceptor doping in the substrate prevents a full C-V curve, due to the relatively large shift in threshold voltage, and the limitation of the electric field across the oxide. A typical substrate with a lower doped p^+-well, will decrease the amount of shift and give better results in inversion.

More measurements have to be performed on wafers fabricated with the refined process flow, to verify whether the structures are capable of giving accurate device characterization results for smaller gate oxide thicknesses.

Acknowledgements

In my second year at the University of Twente I had too decide where I would perform my IOO assignment. Looking at the courses that I had attended, it was a logical step to choose for the chair of semiconductor components. After the IOO assignment, I started my master assignment at the same group, with a lot of pleasure.

During this assignment I was stimulated by a number of people. Special thanks goes out to my committee of supervisors. I would like to thank Radko Bankras, for his time spend on me and in giving just that extra push, once in a while. Likewise, Jurriaan Schmitz stimulated me, in different ways. His ideas and tips were more than welcome. The comments of Jisk Holleman were also very appreciated.

I would also like to thank Henk de Vries and Guido Sasse for their useful comments on performing RF C-V measurements and the design of test structures. Furthermore, I would like to thank all the people of the semiconductor components group for creating a fine and informal working atmosphere. I enjoyed the time spend on floor 3!

Furthermore, I would like to thank my parents and my sister for their continuous support during my college years.

Appendix A

List of symbols

χ	Electron affinity [eV]
λ	Wavelength [m]
λ	Scaling parameter [m]
ω	Corner frequency [rad/sec]
ϕ_{ms}	Workfunction of the metal-semiconductor [eV]
ϕ_{TiN}	Workfunction of TiN [eV]
ϕ_{bi}	Built-in potential [eV]
ϕ	Phase [°]
Φ_{b}	Barrier height [eV]
m^*	Effective electron mass
$\Delta E_{\mathrm{g}}(N)$	Bandgap shrinkage of the substrate [eV]
ε_0	Permittivity of free space [F/m]
$\varepsilon_{\mathrm{Si}}$	Permittivity of silicon [F/m]
$\varepsilon_{\mathrm{SiO_2}}$	Permittivity of SiO_2 [F/m]
$\varepsilon_{\mathrm{Al_2O_3}}$ or $\kappa_{\mathrm{Al_2O_3}}$	Relative dielectric constant of Al_2O_3
ϕ_{s}	Silicon surface potential [V]
μ_0	Constant mobility parameter [cm^2/V·s]
$\mu_{\mathrm{eff,n}}$	Effective mobility for electrons [cm^2/V·s]
a_1 or a_2	$V_{\text{towards port 1}}$ [V] or $V_{\text{towards port 2}}$ [V]
A	Constant for calculating the direct and FN current density [A/V^2]
AA	Alignment area mask
Al	Aluminum
b_1 or b_2	$V_{\text{reflected at port 1}}$ or $V_{\text{reflected at port 2}}$
B	Constant for calculating the direct and FN current density [V/cm]
c	Speed of light [m/s]
C	Capacitance [F]

C_{dep}	Depletion capacitance [F]
C_{fb}	Flatband capacitance [F]
C_{gg}	Device capacitance [F]
C_{inv}	Inversion capacitance [F]
C_{ox}	Oxide capacitance [F/cm^2]
CO	(Mask for the) contacts
$E_{\text{breakdown}}$	Electric breakdown field [MV/cm]
E_{eff}	Vertical electric field [MV/cm]
E_{g}	Bandgap of the silicon substrate [eV]
E_0	Constant vertical electric field parameter [MV/cm]
E_{ox}	Oxide electric field [V/cm]
f_{t}	Cut-off frequency [Hz]
f_{min}	Minimal frequency [Hz] at which $Q > 1$
f_{opt}	Optimal frequency [Hz] at which Q is optimal
f_{NQS}	Non-quasistatic frequency [Hz]
f_{top}	Maximum frequency [Hz] at which the $Q = 1$
g	Differential conductance [Ω^{-1}]
GA	Gate area (mask)
GC	Gate contact (mask)
IC	Interconnect (mask)
H	Transfer function
I_{gate}	Gate leakage current per area [A/cm^2]
$Im(..)$	Imaginary value [Ω]
$L_{\text{gate-sub.cont.}}$ (without overlap)	Length from the gate to the substrate contact [m]
$L_{\text{gate-sub.cont.}}$ (with overlap)	Length in which the sub. adds a R below the gate [m]
L_{gate}	Length of the gate [m]
L_{finger}	Gate finger length [m]
L_{min}	Minimal channel length [µm]
J_{DIR}	Direct tunneling current density [A/cm^2]
J_{FN}	Fowler-Nordheim tunneling current density [A/cm^2]
J_{GATE}	Gate tunneling current density [A/cm^2]
LOCOS	Local oxidation of silicon
L_{d}	Debye length [µm]
n	Fitting parameter
n_{i}	Intrinsic concentration [cm_2]
n^+	Heavily doped area with electrons
N	Number of gate fingers
N_{a}	Acceptor doping concentration [cm^{-3}]
N_{d}	Donor doping concentration [cm^{-3}]
N_{ss}	Interface state concentration [cm^{-2}]
N_{sub}	Substrate doping concentration [cm^{-3}]

p	Doped area with holes as majority carriers
p^+	Heavily doped area with holes as majority carriers
P_{Watt}	Power [Watt]
P_{dB}	Power [dB]
Q	Quality factor
Q_{opt}	Optimum quality factor
R	Series resistance [Ω]
R_{channel}	Channel resistance [Ω]
$R_{\text{diff,area}}$	R added by the substrate contact (diffusion)area [Ω]
R_{g}	Gate resistance [Ω]
$R_{\text{s,inv}}$	Series resistance when the DUT is in inversion [Ω]
$R_{\text{sub,contact}}$	Substrate contact resistance [Ω]
$R_{\text{sub,sq}}$	Substrate resistivity [Ω/□]
$Re(..)$	Real value [Ω]
S	S-parameter matrix
t_{contact}	Contact thickness [m]
$t_{\text{interface layer}}$	Thickness of the interface layer [nm]
t_{ox}	Gate oxide thickness [m]
T	Temperature [°C]
V_{bulk}	Bulk voltage [V]
V_{fb}	Flatband voltage [V]
V_{gs}	Gate-source voltage [V]
V_{ox}	Potential across the oxide [V]
V_{th}	Threshold voltage [V]
W	Gate width [m]
W_{d}	Depletion width of the drain [µm]
W_{dep}	Depletion width [µm]
W_{s}	Depletion width of the source [µm]
W_{finger}	Gate finger width [m]
x_{d}	Depletion depth [µm]
x_{n}	Depletion depth in the n-part of the pn junction [µm]
x_{j}	Junction depth [µm]
x_{p}	Depletion depth in the p-part of the pn junction [µm]
X (ratio)	Instantaneous inversion charge/the inv.charge at a low frequency
Y	Admittance [Ω^{-1}]
Z	Impedance [Ω]
Z_0	Characteristic impedance [Ω]

Appendix B

Constants

Name	**Constants**	**Value**
Gate resistivity	ρ_{Al} [Ω·m]	$2.70 \cdot 10^{-8}$
Number of gate fingers	N	2
Length of the gate	L [µm]	2
Thickness gate	t_{gate} [nm]	500
Gate voltage	V_{gs} [V]	2
Flatband voltage	V_{fb} [V]	-0.8
Substrate surface potential	Ψ [V]	0.8
Oxide capacitance	C_{ox} [F/cm^2]	$2 \cdot 10^{-6}$
Dielectric constant of Al_2O_3	$\varepsilon_{\mathrm{Al_2O_3}}$	9
Permittivity of Si	$\varepsilon_{\mathrm{Si}}$ [F/m]	$1.036 \cdot 10^{-10}$
Permittivity of SiO_2	$\varepsilon_{\mathrm{SiO2}}$ [F/m]	$3.451 \cdot 10^{-11}$
Permittivity of Al_2O_3	$\varepsilon_{\mathrm{Al_2O_3}}$ [F/m]	$7.969 \cdot 10^{-11}$
Mobility constant for electrons at the surface	μ_0 [cm^2/V·s]	670
Effective mobility	μ_{eff} [cm^2/V·s]	102
Vertical electric field constant for electrons at the surface	E_0 [MV/cm]	$6.70 \cdot 10^{-1}$
Effective vertical electric field	E_{eff} [MV/cm]	1.125
Constant mobility factor for electrons at the surface	ν	1.6
Scaling parameter	λ [m]	$2 \cdot 10^{-6}$
Oxide thickness	t_{ox} [nm]	4.5
Substrate acceptor doping: low resistivity substrate	N_{a} [cm^{-3}]	$3.2 \cdot 10^{18}$
typical substrate		$2.0 \cdot 10^{17}$
typical substrate with p-well		$1.8 \cdot 10^{15}$
Donor doping concentration of the source	N_{d} [cm^{-3}]	$1.6 \cdot 10^{20}$
Junction depth: low resistivity substrate	x_{d} [µm]	0.1585
typical substrate		0.5711
typical substrate with p-well		0.2559

Table I: The constants.

Appendix C

S-parameter conversion

S- to Y-parameter conversion

$$Y_{11} = \frac{(1 + S_{22})(1 - S_{11}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

$$Y_{12} = \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

$$Y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

$$Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

S- to Z-parameter conversion

$$Z_{11} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$$

$$Z_{12} = \frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$$

$$Z_{21} = \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$$

$$Z_{22} = \frac{(1 + S_{22})(1 - S_{11}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$$

S- to H-parameter conversion

$$H_{11} = \frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$H_{12} = \frac{2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$H_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$H_{22} = \frac{(1 - S_{22})(1 - S_{11}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

Appendix D

Two RF C-V gate-capacitance extraction methods

From the Adict wafer from Philips:

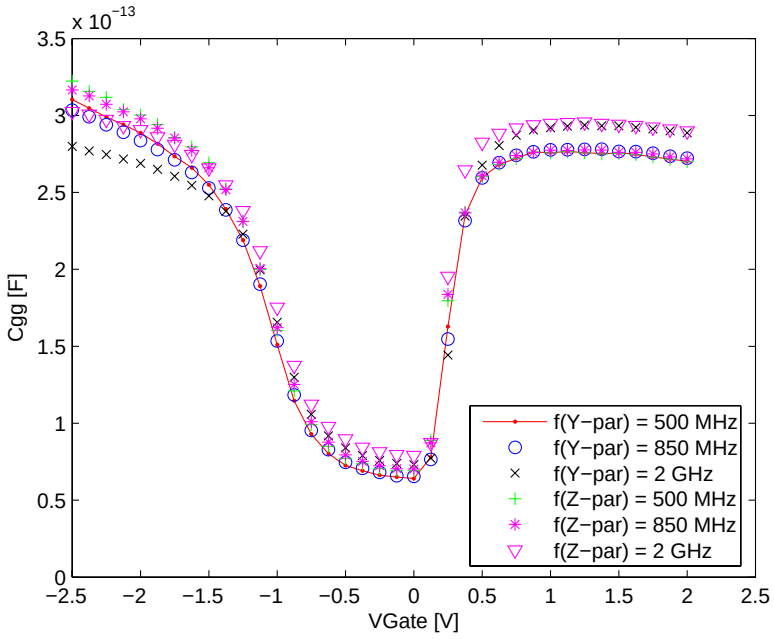

Figure I: The Y- and Z-parameter C_{gg} methods for RF C-V measurements with $C_{\mathrm{gg}} = \frac{Im(Y_{11})}{\omega}$ and $C_{\mathrm{gg}} = Im(\frac{1}{Z_{11}-Z_{12}}) \cdot \frac{1}{\omega}$.

The Y_{11}-parameter C_{gg} extraction method shows the best results for the Adict wafer.

Appendix E

C_{gg} using Z-parameters

For low R structures with a *p^+-overlap and small groundplanes*:

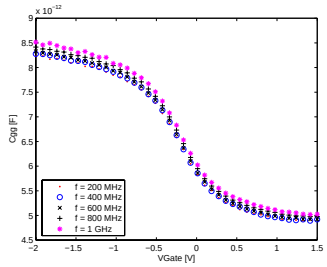

Figure II: First device: $W = 100$ µm and $L = 2.2$ µm.

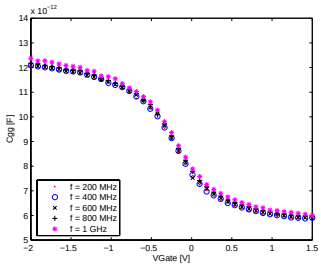

Figure IIa: Second device: $W = 100$ µm and $L = 4$ µm.

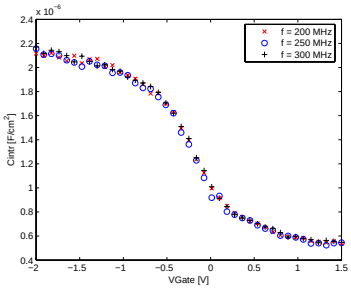

Figure IIb: The intrinsic device capacitance C_{intr} extraction for frequencies with $Q > 10$. The gate oxide thickness $t_{\text{ox}} \approx 3.7$ nm.

The thickness is rather low compared to the results of the Y-parameter C_{gg} extraction method and the expected values.

For low R structures with a *p^+-overlap and large groundplanes*:

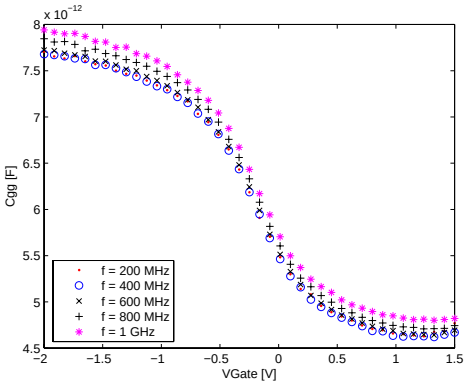

Figure III: First device:
$W = 100$ µm and $L = 2.2$ µm.

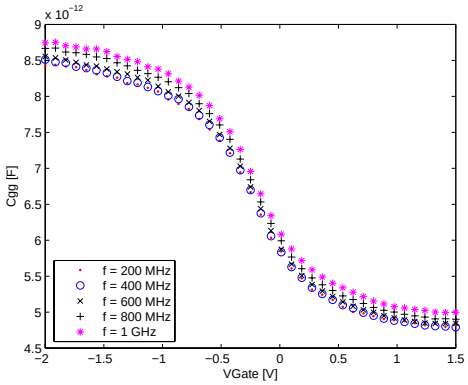

Figure IIIa: Second device:
$W = 100$ µm and $L = 2.4$ µm.

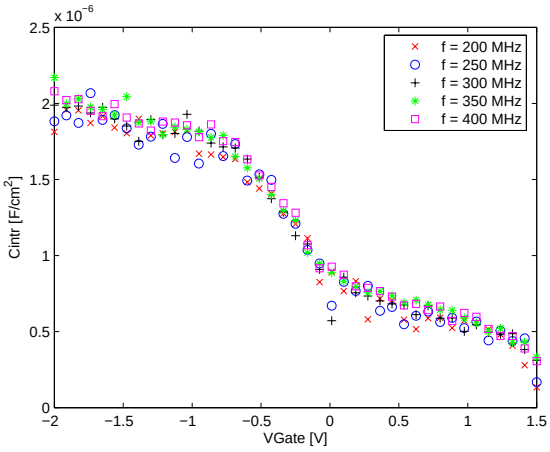

Figure IIIb: The intrinsic device capacitance from the RF C-V measurements for frequencies with $Q > 10$. The gate oxide thickness $t_{\text{ox}} \approx 4.0$ nm.

The thickness is rather low compared to the results of the Y-parameter C_{gg} extraction method and the expected values.

For low R structures without a p^+-*overlap and small groundplanes*:

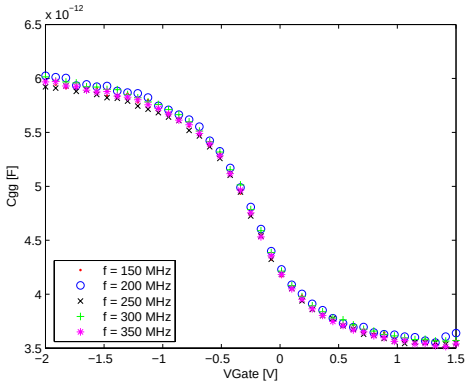

Figure IV: First device:
$W = 100$ µm and $L = 2.2$ µm.

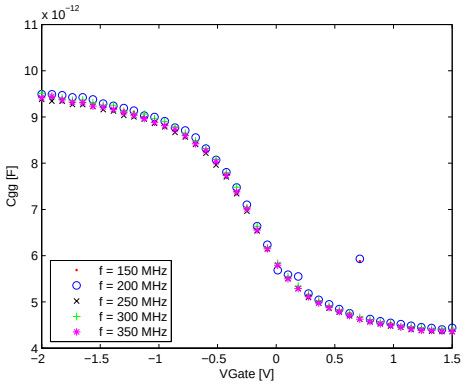

Figure IVa: Second device:
$W = 100$ µm and $L = 4$ µm.

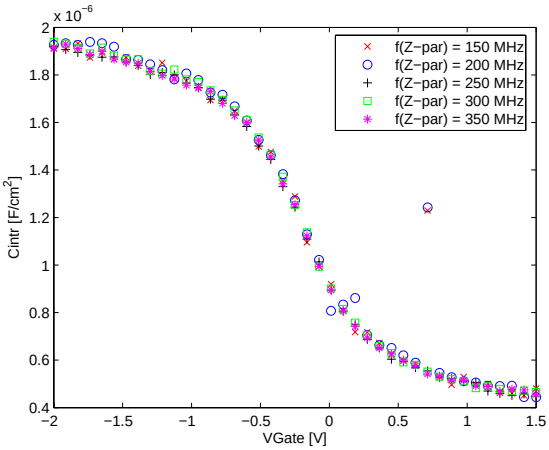

Figure IVb: The intrinsic device capacitance from the RF C-V measurements for frequencies with $Q > 10$. The gate oxide thickness $t_{\text{ox}} \approx 4.1$ nm.

The thickness is rather low compared to the results of the Y-parameter C_{gg} extraction method and the expected values.

Appendix F

Process flow

0. Starting material

wafer	size	doping	orientation	resistivity (Ω·cm)	dope (cm^{-3})
OSP	100 mm	B (p-Si)	<100>	5 - 10	10^{15}
OSP	100 mm	B (p-Si)	<100>	0.015 - 0.025	10^{17}

Lot number:

	wafer number
01	
02	
03	
04	
05 (dummy)	

◯ Comments:

1. Standard wafer cleaning (process time: 30 min)

	step	time
1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	boiling HNO_3 69% 110 °C	10 min
5	rinsing DI water	until conductivity < 0.1 μS
6	1% HF dip	until hydrophobic
7	rinsing DI water	until conductivity < 0.1 μS
8	spin dry	

◯ Comments:

2. Cleaning of oxidation furnace (process time: 120 min) **WITHOUT WAFERS**

Furnace: Tempress 6 furnace stack (right top [D1] gate oxidation)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	process time (min)
800 - 850	10	O_2	4	5
850 - 1100	10	O_2 / $C_2H_3Cl_3$ (C_{33})	4	25
1100	-	O_2 / $C_2H_3Cl_3$ (C_{33})	4	35
1100 - 800	-7.5	N_2	4	40

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	55	00	-	jump prog step 55
cleaning	55	9	00	20	147	O_2 850 °C paddle in
	56	4	01	03	147	O_2 wait temp
	57	9	1.	00	12567	C_{33} temp 1100 °C 1 hour
	58	9	10	00	1	O_2 temp 800 °C 10 min
	59	1	00	00		end program

◯ Comments:

3. Growth of 25 nm pad oxide (process time: 90 min)

Furnace: Tempress 6 furnace stack (right top [D1] gate oxidation)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	process time (min)
800 - 950	10	O_2 / $C_2H_3Cl_3$ (C_{33})	4	15
950	-	O_2	4	44
950	-	N_2	4	20
950 - 800	-7.5	N_2	4	20

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	02	00	-	jump prog step 02
gate ox. 25 nm	02	9	05	00	137	O_2 5 min 800 °C paddle out
	03	9	05	00	1237	O_2 + C_{33} 5 min 800 °C paddle out
	04	4	01	03	127	wait temp and paddle in
	05	9	00	10	12457	set temp 950 °C
	06	4	01	03	12457	wait temp 950 °C
	07	9	44	00	1457	44 min O_2 950 °C
	08	9	20	00	457	20 min N_2 950 °C
	09	3	60	00	-	jump step 60 800 °C
standard downramp 800 °C	60	9	00	20	7	N_2 set temp 800 °C
	61	4	01	01	7	wait temp 800 °C
	62	9	00	02	78	set output 8
	63	4	12	1°2	37	end program

◯ Comments:

4. Ellipsometry of pad oxide (process time: 10 min)

mode	angle Ψ (°)	angle Δ (°)	period (nm)	refractive index	thickness (nm)
float					
fixed	↑	↑	284.28	1.457	

◯ Comments:

5. Flush LPCVD Si_3N_4 (process time: 120 min) **WITHOUT WAFERS**

Furnace: CMOS LPCVD (F1) Recipe: N2 (FLUSH)

SiH_2Cl_2 (sccm)	NH_3 (sccm)	pressure (mTorr)	temperature (°C)	time (hours)
0	25	600	850	2

◯ Comments:

6. LPCVD of 50 nm Si_3N_4 (process time: 60 min) **WAFERS IN CENTER**

Furnace: CMOS LPCVD (F1) Recipe: N3 (NITRTEST)

SiH_2Cl_2 (sccm)	NH_3 (sccm)	pressure (mTorr)	temperature (°C)	dep. rate (nm/min)	dep. time (min:sec)
22	66	200	800	5	10:55

◯ Comments: check recipe: fixed 01:00, variable 09:55

7. Ellipsometry of Si_3N_4 (process time: 10 min)

Si_3N_4 on blanked wafer:

mode	angle Ψ (°)	angle Δ (°)	period (nm)	refractive index	thickness (nm)
float					
fixed	↑	↑	178.33	2.008	

Si_3N_4 on pad oxide:

mode	angle Ψ (°)	angle Δ (°)	period (nm)	refractive index	thickness (nm)
float					
fixed	↑	↑	178.33	2.008	

◯ Comments:

8. Standard wafer cleaning (process time: 30 min)

◯ Comments: does not include HF etching

9. Photolithography of active area (mask AA) (process time: 30 min)

Equipment: BLE Gamma 60 + EVG 620 aligner

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
6000 rpm 20 s	1	3.6	1	45	NO

◯ Comments:

10. Plasma etching of Si_3N_4 (process time: 5 min)

chart speed	600 mm/h
channel span	1 V
gain	10^7

Reactor: Plasmatherm 400
Phase 1 (descum)

O_2 (sccm)	pressure (μbar)	power (W)	matching network	time (s)
20	106	100	30/100	20

Phase 2 (etching Si_3N_4)

CF_4 / O_2 (sccm)	pressure (μbar)	power (W)	matching network	rate (nm/min)	time (min)	overetch (s)
44	106	100	30/100	50	1	30

◯ Comments: + 1 min. after rotation of wafers

11. Resist removal (process time: 90 min)

Reactor: Tepla 300 Recipe: 15 preheat + full strip

step	gas 1 O_2 (ml/min)	gas 2 N_2 (ml/min)	power (W)	time (min:sec)
1	0	500	0	01:00
2	0	500	1000	10:00
3	700	0	1000	60:00
4	0	500	0	01:00

◯ Comments:

12. Standard wafer cleaning (process time: 30 min)

◯ Comments:

13. Cleaning of oxidation furnace (process time: 120 min) **WITHOUT WAFERS**

Furnace: Tempress 6 furnace stack (right bottom [D3] wet oxidation)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	process time (min)
800 - 850	10	O_2	4	5
850 - 1100	10	O_2 / $C_2H_3Cl_3$ (C_{33})	4	25
1100	-	O_2 / $C_2H_3Cl_3$ (C_{33})	4	35
1100 - 800	-7.5	N_2	4	40

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	55	00	-	jump prog step 55
cleaning	55	9	00	20	147	O_2 850 °C paddle in
	56	4	01	03	147	O_2 wait temp
	57	9	1.	00	12567	C_{33} temp 1100 °C 1 hour
	58	9	10	00	1	O_2 temp 800 °C 10 min
	59	1	00	00		end program

◯ Comments:

14. Growth of 700 nm LOCOS field oxide (process time: 4.5 hours)

Furnace: Tempress 6 furnace stack (right bottom [D3] wet oxidation)

temperature cycle (°C)	ramp (°C/min)	ambient	ambient temp (°C) tamson set-point	process time (min)
800 - 1050	10	N_2/H_2O	85	25
1050	-	N_2/H_2O	85	200
1050 - 800	-7.5	N_2/H_2O	85	35

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	02	00	-	jump prog step
wet oxidation 700 nm	02	9	3.	00	37	tamson heat up time 3 hours
	03	4	01	03	7	N_2 wet 800 °C paddle in
	04	9	00	10	467	set temp 1050 °C
	05	4	01	03	467	wait temp 1050 °C
	06	9	3.	20	467	3 h 20 min N_2 wet 1050 °C
	07	3	60	00	-	jump step 60 ramp 800 °C
standard downramp 800 (°C)	60	9	00	20	7	N_2 wet 800 °C
	61	4	01	01	7	wait temp 800 °C
	62	9	00	02	78	set output 8
	63	4	12	1°2	37	end program

◯ Comments:

15. Ellipsometry of field oxide (process time: 10 min)

mode	angle Ψ (°)	angle Δ (°)	period (nm)	refractive index	thickness (nm)
float					
fixed	↑	↑	284.28	1.457	

◯ Comments:

16. Removal of oxidized Si_3N_4 (process time: 15 s)

SiO_2 etch	etch rate	etch time (s)
HF / NH_4F 1:6	80 nm/min	15

◯ Comments:

17. Removal of Si_3N_4 (process time: 20 min) **QUARTZ RACK**

Si_3N_4 etch	etch rate	temperature	etch time (min)	overetch (min)
H_3PO_4 85%	3.5 nm/min	180 °C	15	5

◯ Comments:

18. Standard wafer cleaning (process time: 30 min)

◯ Comments:

19. Photolithography of stopper implantation mask (SI = AA) (process time: 30 min)

Equipment: Convac recipe 9 (3.3 μm) + EVG 620 aligner

resist spin HDMS + 907/35	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	5	7.5	NO	70	15

◯ Comments: not required for p-well

20. Stopper implantation

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	I fil. (A)	p tot. (mbar)	mass magnet (amu)	2^{nd} magnet (A)
B^+	$1.5 \cdot 10^{12}$	0.800	350			11 (10.81)	11.15

◯ Comments:

21. P-well implantation

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	I fil. (A)	p tot. (mbar)	mass magnet (amu)	2^{nd} magnet (A)
B^+	$1.5 \cdot 10^{13}$	8.00	350			11 (10.81)	10.20
B^+	$4.0 \cdot 10^{12}$	2.13	110			11 (10.81)	6.09
B^+	$2.0 \cdot 10^{12}$	1.07	40			11 (10.81)	3.54

◯ Comments:

22. Resist removal (process time: 30 min) **NO LIFT-OFF WITH HNO_3**

Reactor: Tepla 300 Recipe: 15 preheat + full strip

step	gas 1 O_2 (ml/min)	gas 2 N_2 (ml/min)	power (W)	time (min:sec)
1	0	500	0	01:00
2	0	500	1000	10:00
3	700	0	1000	120:00
4	0	500	0	01:00

◯ Comments:

23. Standard wafer cleaning (process time: 30 min)

◯ Comments:

24. Photolithography of implantation mask (mask SD) (process time: 30 min)

Recipe: BLE Gamma 60 / Convac + Karl-Suss aligner

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
3000 rpm 20 s	1	6.0	1	45	**30**

◯ Comments:

25. Implantation of S/D regions

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	I fil. (A)	p tot. (mbar)	mass magnet (amu)	2^{nd} magnet (A)
As^+	$2 \cdot 10^{15}$	1067	100			75 (74.92)	15.5
P^+	$5 \cdot 10^{13}$	27	70			31 (30.97)	8.0

◯ Comments:

26. Removal of implantation mask (process time: 10 min)

Reactor: Tepla 300 Recipe: 15 preheat + full strip

step	gas 1 O_2 (ml/min)	gas 2 N_2 (ml/min)	power (W)	time (min:sec)
1	0	500	0	01:00
2	0	500	1000	10:00
3	700	0	1000	120:00
4	0	500	0	01:00

◯ Comments:

27. Standard wafer cleaning (process time: 30 min)

◯ Comments:

28. Photolithography of implantation mask (mask SC) (process time: 30 min)

Recipe: BLE Gamma 60 / Convac + Karl-Suss aligner

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
3000 rpm 20 s	1	6.0	1	45	**30**

◯ Comments:

29. Implantation of substrate contact regions

implant	dose (cm^{-2})	implantation value (μC)	acceleration (kV)	I fil. (A)	p tot. (mbar)	mass magnet (amu)	2^{nd} magnet (A)
BF_2^+	$2.0 \cdot 10^{15}$	1067	70			49 (48.81)	10.66

◯ Comments:

30. Removal of implantation mask (process time: 10 min)

Reactor: Tepla 300 Recipe: 15 preheat + full strip

step	gas 1 O_2 (ml/min)	gas 2 N_2 (ml/min)	power (W)	time (min:sec)
1	0	500	0	01:00
2	0	500	1000	10:00
3	700	0	1000	120:00
4	0	500	0	01:00

◯ Comments:

31. Standard wafer cleaning (process time: 30 min)

◯ Comments:

32. Cleaning of annealing furnace (process time: 120 min) **WITHOUT WAFERS**

Furnace: Tempress 6 furnace stack (right middle [D2] anneal)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	process time (min)
800 - 850	10	O_2	4	5
850 - 1100	10	O_2 / $C_2H_3Cl_3$ (C_{33})	4	25
1100	-	O_2 / $C_2H_3Cl_3$ (C_{33})	4	35
1100 - 800	-7.5	N_2	4	40

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	55	00	-	jump prog step 55
cleaning	55	9	00	20	147	O_2 850 °C paddle in
	56	4	01	03	147	O_2 wait temp
	57	9	1.	00	12567	C_{33} temp 1100 °C 1 hour
	58	9	10	00	1	O_2 temp 800 °C 10 min
	59	1	00	00		end program

◯ Comments:

33. Anneal of implantation damage / dopant activation (process time: 120 min)

Furnace: Tempress 6 furnace stack (right middle [D2])

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	process time (min)
550	-	N_2	4	60
800 - 900	10	N_2	4	10
900	-	N_2	4	29
900	-	O_2	4	1
900 - 800	-7.5	N_2	4	15

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	22	00	-	jump prog step 22
surface state anneal	22	9	00	10	345	N_2 set temp 550 °C paddle out
	23	4	01	01	345	N_2 wait temp 550 °C
	24	4	01	03	45	N_2 wait paddle in
	25	9	1.	00	45	N_2 1 hour 550 °C
	26	9	00	10	37	N_2 set temp 800 °C paddle out
	27	4	01	01	37	N_2 wait temp 800 °C
	28	4	01	03	7	N_2 wait paddle in
	29	9	00	10	57	N_2 set temp 900 °C
	30	4	01	03	57	N_2 wait temp 900 °C
	31	9	29	00	57	N_2 29 min 900 °C
	32	9	01	00	157	O_2 1 min 900 °C
	33	3	60	00	-	N_2 jump step 60 ramp 800 °C

◯ Comments: cooldown to 550 °C requires extra time

34. Standard wafer cleaning (process time: 30 min)

◯ Comments:

35. Photolithography of gate area (mask GA) (process time: 30 min)

Equipment: BLE Gamma 60 / Convac + Karl-Suss aligner

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	6.0	1	45	15

◯ Comments:

36. Etching of sacrificial oxide (process time: 10 min) **LIGHT OFF**

	SiO_2 etch	etch rate (nm/min)	etch time (s)
1	HF / NH_4F 1:6	80 nm/min	15
2	0.3% HF + 0.37% HCl	slow	until reference area hydrophobic

◯ Comments: step 2 4:30 min + 1:00 min overetch

37. Resist removal and cleaning (process time: 30 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	boiling HNO_3 69% 110 °C	10 min
5	rinsing DI water	until conductivity < 0.1 μS
6	spin dry	

◯ Comments:

38. Protective resist layer (process time: 20 min) **OPTIONAL**

resist spin HDMS + 907/17	postbake 120 °C (min)
4000 rpm 20 s	15

◯ Comments:

39. Wafer sawing (process time: 15 min) **OPTIONAL**

die size (mm^2)
$15 \cdot 15$

◯ Comments:

40. Resist removal (process time: 30 min) **OPTIONAL**

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	boiling HNO_3 69% 110 °C	10 min
5	rinsing DI water	until conductivity < 0.1 μS
6	spin dry	

◯ Comments:

41. Etch native oxide / grow chemical oxide (process time: 30 min)

	solution	time (min)
a	0.3% HF + 0.37% HCl	until reference area hydrophobic
b	1% HF	until reference area hydrophobic
c	boiling HNO_3 69% 110 °C	10
d	96% H_2SO_4 + 31% H_2O_2 (4:1) 90 °C	10

◯ Comments: option a.

42. ALD of AlO layer

◯ Comments:

43. ALD of TiN layer

◯ Comments:

44. Photolithography of gate cover (mask GC) (process time: 30 min)

Equipment: BLE Gamma 60 / Convac + Karl-Suss aligner

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	6.0	1	45	15

◯ Comments:

45. Etching of gate cover (process time: 2 min)

TiN etchant	etch rate (nm/min)	etch time
1% HF		15 s
H_2O_2		10 min

◯ Comments:

46. Resist removal and cleaning (process time: 15 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	spin dry	

No boiling HNO_3.

◯ Comments:

47. Photolithography of contact holes (mask CO) (process time: 30 min)

Equipment: BLE Gamma 60 / Convac + Karl-Suss aligner

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	6.0	1	45	15

◯ Comments:

48. Etching contact holes (gate oxide + pad oxide) (process time: 2 min) **LIGHT OFF**

SiO_2 etch	etch rate (nm/min)	etch time (min)
1 % HF		7 - 8

◯ Comments:

49. Resist removal (process time: 15 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	spin dry	

◯ Comments:

50. Metallization (process time: 60 min)

Ar flow (sccm)	pressure (mTorr)	power (W)	V_{DC} (V)	sputter rate (nm/min)	sputter time (min)	estimated thickness (nm)
210	10.0	7000	425		1:15	1000

◯ Comments:

51. Wafer cleaning (process time: 15 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	spin dry	

Boiling HNO_3 will remove the aluminum.

◯ Comments:

52. Photolithography of interconnect (mask IN) (process time: 30 min)

Equipment: BLE Gamma 60 / Convac + Karl-Suss aligner

resist spin HDMS + 907/17	prebake 95 °C (min)	exposure time (s)	after exp. 120 °C (min)	develop. OPD 4262 (s)	postbake 120 °C (min)
4000 rpm 20 s	1	6.0	1	45	15

◯ Comments:

53. Etching of interconnect (process time: 2 min)

Al etchant	temperature (°C)	etch rate (nm/min)	etch time (s)
phosphoric acid H_3PO_4 (+ CH_3COOH + HNO_3)	45 - 50	500	until clear pattern

◯ Comments:

54. Resist removal and cleaning (process time: 15 min)

1	fuming HNO_3 100% beaker 1	5 min
2	fuming HNO_3 100% beaker 2	5 min
3	rinsing DI water	until conductivity < 0.1 μS
4	spin dry	

Boiling HNO_3 will remove the aluminum.

◯ Comments:

55. Metallization of backside (process time: 60 min)

Ar flow (sccm)	pressure (mTorr)	power (W)	V_{DC} (V)	sputter rate (nm/min)	sputter time (min)	estimated thickness (nm)
210	10.0	7000	425		1:15	1000

◯ Comments:

56. Cleaning of sintering furnace (process time: 120 min) **WITHOUT WAFERS**

Furnace: Tempress 6 furnace stack (left middle [C2] sintering)

temperature cycle (°C)	ramp (°C/min)	ambient	gas flow (slm)	process time (min)
800 - 850	10	O_2	4	5
850 - 1100	10	O_2 / $C_2H_3Cl_3$ (C_{33})	4	25
1100	-	O_2 / $C_2H_3Cl_3$ (C_{33})	4	35
1100 - 800	-7.5	N_2	4	40

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	55	00	-	jump prog step 55
cleaning	55	9	00	20	147	O_2 850 °C paddle in
	56	4	01	03	147	O_2 wait temp
	57	9	1.	00	12567	C_{33} temp 1100 °C 1 hour
	58	9	10	00	1	O_2 temp 800 °C 10 min
	59	1	00	00		end program

◯ Comments: no tube cleaning available

57. Sintering (process time: 15 min) **OPTIONAL**

Furnace: Tempress 6 furnace stack (left middle [C2] sintering)

temperature	ambient	process time
400 °C	N_2 + H_2O	10 min

Omron seq.	step	opcode	data1	data2	output	comments
start	01	3	06	00	-	jump prog. step 6
aluminum sintering	06	9	05	00	3	5 min paddle out
	07	4	01	03	-	wait temp 400 °C and paddle in
	08	9	10	00	-	10 min Al sintering
	09	3	63	00	-	jump step 63
end program	63	4	12	1°2	3	paddle out

◯ Comments:

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