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Automatic Gain Control ADC based on signal statistics for a cognitive radio cross-correlation spectrum analyzer

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Abstract

For integration purposes of a cross-correlation spectrum analyzer for cognitive radio, the use of low-resolution ADCs is investigated. In radio astronomy cross-correlation is exploited intensively together with low resolution ADCs and therefore a 2-bit ADC concept originating from ASTRON is analyzed and implemented. This ADC has automatic gain control and offset canceling based on estimates of the cumulative distribution function of the input signal. The ADC is worked out at system level and simulated to verify its correctness. The comparator is a critical component in the ADC and it is implemented on circuit level in a 90 nm CMOS process. Performance dependencies on both system level and circuit level are analyzed. The ADC allows a SFDR of the spectrum analyzer of 60 dB when the measurement time is 0.2 seconds, the sample frequency is 1536 MHz and the resolution bandwidth is 6 MHz. In practical cases this SFDR is lowered to 55 dB. The implemented comparator allows a SFDR of 54 dB. The AGC mechanism causes input signal dependency which degrades performance. The required measurement time to achieve substantial SFDR results in less efficient spectrum estimation than when higher resolution ADCs are used.

Contents

Chapter 1

Introduction

More and more electronic devices use wireless communication to send or receive data. Cellphones, WLAN connected devices, wireless digital television and blue-tooth connected devices all communicate by sending and receiving electro-magnetic signals. The signals sent and received by these devices occupy a part of the electro-magnetic spectrum. More wireless communication means more spectrum occupation. Due to the traditional fixed spectrum assignment policy many parts of the spectrum are reserved for a specific type of user, but are used only for about 15% to 85% of the time [1]. The utilization not only varies in time, but also per geographic location. Thus spectrum is used inefficiently. Because of the increasing use of wireless communications, available parts in the spectrum are getting scarce. To utilize the electro-magnetic spectrum more efficiently, a new networking paradigm is emerging: Cognitive Radio. Certain licensed parts of the spectrum may now be used by unlicensed users as long as the licensed user is not interfered with. In order to determine whether a part in the spectrum is used or not, the electronic device must sense the spectrum very accurate. Then it must adapt its transmission parameters in order to use the spectrum. The sensing of the spectrum is required by current cognitive radio standards to be very accurately. This requirement results in many design challenges.

1.1 Cognitive Radio

Cognitive radio was first introduced by Mitola [2] in 1998 and in the following decade FCC, Ofcom and IEEE started developing regulations and standards for cognitive radio. A cognitive radio device senses the spectrum, detects licensed users and adjust its transmission and reception parameters accordingly. Sensing and detecting are often referred to as one task: *spectrum sensing*.

Spectrum holes The main goal of spectrum sensing is to find spectrum holes. A spectrum hole is the absence of a primary user signal at a certain frequency, at a certain place on a certain moment. When a cognitive radio device communicates, it must sense the spectrum frequently (e.g. every second), detect spectrum holes and 'jump' to another spectrum hole when it's current hole is no longer available. This is illustrated in Figure 1.1.

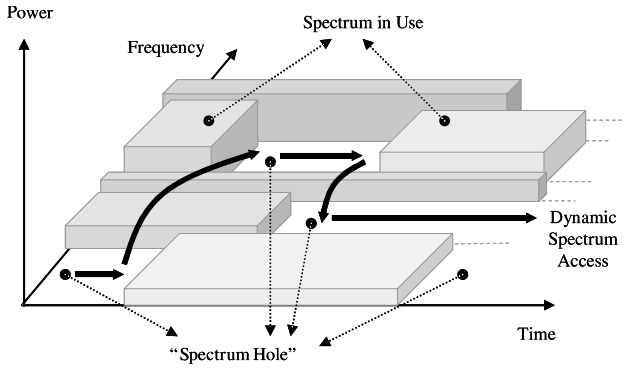

Figure 1.1: A cognitive device jumps from spectrum hole to spectrum hole [1].

Another dimension in which a spectrum hole can be defined is direction. With the use of beam-forming techniques the direction of an incoming signal can be determined and direction from which no signal is received can be used. This type of spectrum sensing is not addressed in this thesis.

The chance of rightfully identifying a spectrum spot as occupied and the chance of wrongfully identifying a spot as occupied are referred to as *probability of detection* and *probability of false alarm*. Required probabilities of a cognitive radio system are defined by cognitive radio standards.

Types of spectrum sensing Different methods of estimating the spectrum are proposed in literature. For some methods multiple nodes share their spectrum sensing information and for some methods the spectrum occupancy is predicted, based on their previous observations. There are methods which require prior knowledge of the signal characteristics to detect primary users [1], [3], but the most straight forward method only senses the power density in the electro-magnetic spectrum. This method is referred to as *energy detection spectrum sensing*, which is a form of blind spectrum sensing.

A CMOS integrated cognitive radio sub-system Since cognitive radio is used in wireless communicating devices, most of these devices will be battery powered. A cognitive radio sub-system must therefore be power and chip area efficient and will be integrated as a part of a system on chip. When the sub-system is used in relatively cheap devices which are produced in large numbers it is most likely realized as an integrated circuit on a chip fabricated in CMOS technology. So, in this theses implementation in CMOS is aimed for.

1.2 Spectrum analyzers

In this thesis the focus is on energy detection spectrum sensing. A spectrum analyzer estimates the spectral power distribution after the electro-magnetic signal is picked-up by the antenna. Many different spectrum analyzers exist: expensive high performance spectrum analyzers are found in electrical laboratories, but cheaper hand-held spectrum analyzers are also available. More

expensive spectrum analyzers perform better in terms of for instance, linearity or amplitude accuracy. In general: the higher the price, the better the performance .

Figure 1.2: Different spectrum analyzers

Spectrum analyzers can also be categorized by type. Over the last few decades different types of spectrum analyzers have emerged, each having its advantages and disadvantages. The Fast Fourier Transform (FFT) analyzers which have a digital back-end are of interest for integration on chip. This spectrum analyzer first converts the input signal to a suitable format [1], then the signal is converted to the digital domain. In the digital domain the spectrum is obtained by a Fast-Fourier-transform.

Power consumption and chip area are important cost factors but for cognitive radio sensitivity is also very important. This sensitivity is limited by a device's Spurious Free Dynamic Range (SFDR), which is a measure for the pollution of the estimated spectrum due to non-linearity and noise of the spectrum analyzer. This is elaborated in Section 2.1. Cost and sensitivity trade off against each other and finding a cheap solution with acceptable sensitivity is one of the motivations for this thesis.

1.3 Previous work

The work in this thesis is carried out in the context of the research project *Ad-hoc Dynamic Radio-spectrum Exploitation via Multi-phase Radio (AD-REM)*. For this project a cross-correlation spectrum analyzer is designed and prototyped. In this thesis a part of this spectrum analyzer is zoomed in to. Because there are similarities between the spectrum analyzer and techniques applied in radio astronomy, an ADC concept of ASTRON is described. ASTRON is Netherlands Institute for Radio Astronomy.

1.3.1 Cross-correlation spectrum analyzer

As a way to more accurately sense the spectrum, a new type of spectrum analyzer is proposed in recent work [4], [5], [6]. The key requirement SFDR is increased by adding the factor *measurement time* to its trade-off between noise and non-linearity. This spectrum analyzer uses two analog front-ends and cross-correlation to increase SFDR. The spectrum analyzer is elaborated

[1] Downmixed to intermediate frequencies and properly scaled.

in Section 2.3. As part of this recent work a prototype of the spectrum analyzer is realized to proof the concept.

1.3.2 Radio Astronomy

Traditionally, cross-correlation is exploited intensively in radio astronomy: the output of multiple antennas is converted to the digital domain and cross-correlated to detect signals which are buried in noise. In these applications low-resolution ADCs are used, like 1, 1.5 or 2 bits [7]. For these applications the performance degradation when using a low-resolution ADC is minimal, because of specific signal characteristics.

1.4 Project description

In order to integrate the cross-correlation spectrum analyzer on-chip for the use in low-power wireless communicating devices, a potentially cheap Analog to Digital Converter (ADC) is required. The cost is expressed in power consumption and chip area. The problem statement is as follows:

- *For integration purposes of a cross-correlation spectrum analyzer for energy detection spectrum sensing for the use in cognitive radio, a low cost on-chip ADC is required.*

To reduce the cost of an ADC, its resolution can be decreased. In radio astronomy systems low resolution ADCs have been used frequently. Because of the characteristics of the input signals, the decrease in system performance due to the lower resolution of the ADC is acceptable. The input signal has a nearly white spectrum and a Gaussian amplitude distribution. Because these systems also use cross-correlation in their spectral analysis, the question arose whether a low resolution ADC applied in a cognitive radio spectrum analyzer would also lead to a feasable system with an acceptable decrease in system performance.

The research question is defined as follows:

- *Is a low resolution ADC suitable for the use in a cross-correlation spectrum analyzer for cognitive radio?*

To this end a 2-bit ADC concept originating from ASTRON is investigated [7], [8]. Apart from the low-resolution, it has offset canceling and Automatic Gain Control (AGC). These two features contribute to maximization of system performance. The offset canceling and AGC is achieved by variable decision levels of the ADC. The decision levels determine the output code of a sample. The value of the decision levels are based on the Cumulative Distribution Function (CDF) of the input signal. The ADC is therefore referred to as *CDF-based AGC ADC*. The relation between the input CDF and the reference levels is illustrated in Figure 1.3. The probabilities at the y-axis ($[p_n, p_0, p_p]$) are set by a system controller, through the cumulative distribution function of the input signal the ADC's decision levels are set.

To investigate the suitability of low resolution ADCs in general and the *CDF-based AGC ADC* specifically, the following sub-questions are defined:

1. How does spectrum analyzer performance depend on the ADC resolution?

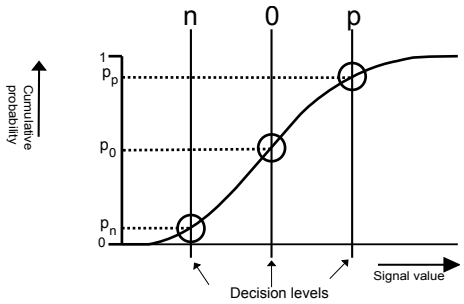

Figure 1.3: CDF-based AGC ADC principle: decision levels depend on system settings and input CDF

2. Is a *CDF-based AGC ADC* suitable as a low resolution ADC in cross-correlation spectrum analyzer for cognitive radio?

3. What is at circuit level the critical component in the CDF-based AGC ADC and how does system performance depend on circuit level behavior?

4. What performance is achievable and what are the costs?

The ADC concept is revisited and an architecture is proposed which balances sensitivity, measurement time, power consumption and complexity.

The achievable SFDR is decreased by the limited resolution, but this is compensated to a certain extent by utilizing the cross-correlation spectrum analyzer and using the measurement time allowed by the current cognitive radio draft standards.

1.5 Thesis outline

The second chapter describes the cross-correlation spectrum analyzer and theory on how it breaks the SFDR trade-off. The third chapter addresses sampling and quantization and the effect on performance of a cross-correlation spectrum analyzer. It describes different ways of using dither to increase system performance and one dithering scheme is described extensively for a 2-bit quantizer.

Chapter four describes the cognitive radio standard used, it discribes theoretical system performance and the CDF based AGC ADC concept is analyzed and implemented on system level. Implementation choices are described and the concept is validated by system level simulations.

In chapter five the comparator of the ADC is identified as the most critical component and this component is implemented at circuit level. Non-ideal properties are identified and their effect on performance are investigated.

In the last chapter conclusions are presented and elaborated. Then recommendations are presented.

Chapter 2

Integrated cross-correlation spectrum analyzer

The task of an energy detection spectrum analyzer for the use in a cognitive radio application is to find spectrum holes. The performance of the spectrum analyzer determines the chance of successfully finding spectrum holes. When strong narrow-band signals are present at the input of a spectrum analyzer, the performance of the spectrum analyzer is limited by its SFDR. The SFDR is increased by the cross-correlation spectrum analyzer with respect to traditional spectrum analyzers. This chapter provides insight in the increased performance of the cross-correlation spectrum analyzer with respect to traditional spectrum analyzers. The mechanism used by the spectrum analyzer is introduced and the spectrum analyzer itself is described. First the SFDR trade-off is described and the conventional equation for SFDR is extended with the variable measurement time. Then cross-correlation is described, starting from a mathematical point of view and ending with an estimator which can be easily implemented digitally. Then the cross-correlation spectrum analyzer is described. The role of the ADC and the dependency of its cost on word-size is described.

2.1 The SFDR trade-off

A big challenge in cognitive radio spectrum sensing is that the power of very small signals should be measured while the overall signal can also contain strong narrow band signals. This problem can be characterized in terms of the SFDR. SFDR is a performance measure of an analog system. It gives the ratio between the strongest and the weakest signal that can be detected at the same time [9]. The SFDR results from the trade-off between linearity and noise. This trade-off can be extended by the factor *measurement time* by lowering the noise by cross-correlation [4], [5].

The SFDR of a system depends on noise power and non-linearity. The noise power added by a system is expressed as the noise factor, which is the ratio of input Signal to Noise Ratio (SNR) and output SNR. For most systems the *noise figure* is specified, which is the *noise factor* expressed in dB. The non-linearity is expressed as Input referred third order Intercept Point (IIP3), which is a measure for distortion in a system.

Spurious Free Dynamic Range For an analog front-end the Dynamic Range (DR) is defined as the ratio between the noise floor and the maximum input signal. However, due to non-linearity the maximum attainable dynamic range can be limited by distortion components. When the strongest distortion component power is equal to the noise floor, the ratio between input signal and the input referred strongest harmonic is the SFDR. Figure 2.1 illustrates the SFDR for an arbitrary spectrum analyzer.

The noise in Figure 2.1 is white and the magnitude of the noise depends on the bandwidth in which the noise power is expressed, for instance $\frac{V^2}{kHz}$. In that case the resolution bandwidth is $1kHz$.

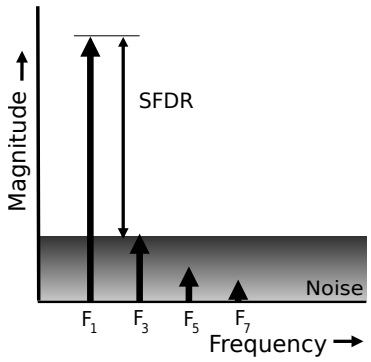

Figure 2.1: Spurious free dynamic range

If the IIP3 approximation is acceptable and if the noise floor is white, then the SFDR is expressed as [10]:

$$SFDR = \frac{2}{3}\left(IIP3 - P_{noisefloor} - 10 \cdot \log_{10}(RBW) + 174\right)[dB] \tag{2.1}$$

Where RBW is the resolution bandwidth and $P_{noisefloor}$ is the power of the noise floor per Hertz. If it is possible to reduce the noise and keep the IIP3 unchanged, this trade-off is broken and yields higher SFDR. This is possible with cross-correlation.

Noise factor The noise factor (F) expresses the amount of noise added by a system:

$$F = \frac{SNR_{output}}{SNR_{input}} \tag{2.2}$$

When subsystems are cascaded, where block i is followed by block $i+1$, contributions to the total system noise depends on the gain of the other blocks. The contribution of the subsystems to the noise factor of the total system is calculated as follows:

$$F_{total} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_{a,1}} + .. + \frac{F_m - 1}{G_{a,1} \cdot G_{a,2}..G_{a,m-1}} \tag{2.3}$$

Where $G_{a,i}$ are available power gains: the input and output impedances are matched. For unmatched sub-blocks the formula gets more complicated [11, , pg. 45] but the following effect remains: Noise added in early stages contribute more to total system noise factor, when the gain of the sub-blocks is > 1.

Input referred third order intercept point Most integrated circuits in analog front-ends are differentially implemented, such that second order distortion is canceled out. For these cases the third harmonic is in general the largest distortion component. The linearity of a circuit is therefore often expressed in the IIP3, which is the theoretical intercept point of the input referred first harmonic power and the input referred power of the strongest distortion component. The strongest distortion component is either the third harmonic of a single pure sine wave, or the component of a 2-tone test which falls in the measured bandwidth. For narrow-band systems, for the strongest distortion component the strongest distortion component is introduced by aplying two frequencies such that the

When the non-linearity of a system is modeled as:

$$y(t) = \alpha_0 + \alpha_1 \cdot x(t) + \alpha_2 \cdot x^2(t) + \alpha_3 \cdot x^3(t)... \tag{2.4}$$

so when $x(t) = A \cdot cos(t)$ this results in the equation: [11]

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A \frac{3\alpha_3 A^2}{4}\right) cos(\omega t) + \frac{\alpha_2 A^2}{2} cos(2\omega t) + \frac{\alpha_3 A^3}{4} cos(2\omega t) \tag{2.5}$$

Because of differential circuitry the even order terms disappear. Because of small values of A, higher powers of A then n for term n can be neglected.

Then the IIP3 is the input power of $x(t)$ for which holds:

$$var(x(t)) = \frac{\alpha_3}{4 \cdot \alpha_1} var(x^3(t)) \tag{2.6}$$

This approach uses harmonic distortion components to determine IIP3. For small band systems an approach based on intermodulation of two sine waves can be used [11].

Real interception of the first and third harmonic does not happen in practice due to limited gain at large input signal powers. The gain is limited when other non-linear effects dominate such that Equation 2.4 is not valid anymore, for example saturation or compression.

When subsystems are cascaded its contribution to the total system noise depends on the gain of the other sub-blocks. A approximation of the total system IIP3 is [11, pg. 24] :

$$\frac{1}{IIP3_{\text{total}}} = \frac{1}{IIP3_1} + \frac{G_{a,1}}{IIP3_2} + ... + \frac{G_{a,1} \cdot G_{a,2}..G_{a,m-1}}{IIP3_m} \tag{2.7}$$

$$\tag{2.8}$$

Where $IIP3_{\#}$ denote the ratio of first and third signal harmonic powers at a linear scale. Although Equation 2.7 is an approximation the following effect remains: Non-linearity added in later stages contribute more to total system non-linearity, when the gain of the sub-blocks is > 1. The effect is the opposite of the effect of the noise figure in cascaded stages, which is the reason for the SFDR trade-off.

The trade-off The trade-off between non-linearity and noise in a system consisting of cascaded subsystem can be influenced by choosing the location of the gain. This can be seen in Equations 2.7 and 2.3. When more gain is located in later stages the noise is increased and IIP3 is reduced.

This trade-off between noise and linearity is broken when a cross-correlation front-end is used. Such an analog front-end is described in [4]. This front-end consists of two parallel paths, where the uncorrelated noise floor introduced in both paths is reduced by cross-correlating the two output signals.

When a cross-correlation front-end is used, the SFDR also depends on measurement time. If the amount of correlated noise in the front-end is small compared to the amount of uncorrelated noise, then 2.1 changes to:

$$SFDR \approx \frac{2}{3}\left(IIP3 - P_{noisefloor} - 10 \cdot \log_{10}(RBW) + 174 + 10 \cdot \log_{10}(\sqrt{T_m \cdot RBW})\right) \tag{2.9}$$

Where T_m is the measurement time in seconds. When for instance an RBW of 1 kHz is required and the measurement time is 2 ms, the last term in Equation 2.9 adds 1.5 dB to the SFDR. Figure 2.2 illustrates the lowered noise floor by using the cross-correlation front-end.

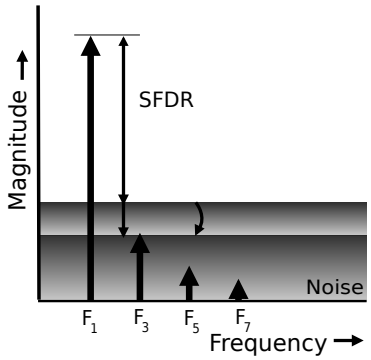

Figure 2.2: Spurious free dynamic range improvement by the cross-correlation front-end

2.2 Cross-correlation

Cross-correlation of two signals gives information on their similarity. Cross-correlation is a statistical property, which in practice often can only be estimated. Time-averaged statistics are then used instead of 'true' ensemble averages (which are obtained from different realizations).
First the statistical definition of cross-correlation is given, then the continuous time cross-correlation function is presented, which is easily transformed to the frequency domain. The discrete-time and discrete-frequency cross-correlation functions are presented and one cross-correlation estimator is introduced. This cross-correlation estimator is a function to be implemented digitally. Although an analog implementation is a possible choice, only digital correlation estimator

issues are addressed because an analog implementation would introduce more correlated noise sources. Finally, spectral averaging is addressed as a way to actually benefit from the cross-correlation estimation.

2.2.1 Statistical representation

The cross-correlation ρ_{XY} of two signals X and Y is the normalized version of the cross-covariance [5]:

$$\rho_{XY}(t,\tau) = \frac{E\left[\left(X^*(t) - \mu_{X^*(t)}\right) \cdot \left(Y(t+\tau) - \mu_{Y(t+\tau)}\right)\right]}{\sigma_X(t) \cdot \sigma_Y(t+\tau)}. \tag{2.10}$$

Where $*$ denotes the complex conjugate. The scaling factor $\sigma_X(t) \cdot \sigma_Y(t+\tau)$ is often not known or assumed 1, making the cross-covariance and cross-correlation equal. In this document the term cross-correlation is used for both metrics. The cross-correlation function becomes the auto-correlation function when $Y = X$ in Equation 2.10.

Joint ergodicity of input signals The input signals X and Y are assumed to be jointly ergodic, which means [12]:

1. The signals are wide sense stationary, i.e. their first and second order moments are time invariant.
2. Ensemble average and time average are equal: the first and second order moments along the time dimension are equal to the first and second order moments across the space of different realizations.

2.2.2 Continuous time and frequency representation

Because of the assumed ergodicity of the input signals the result of Equation 2.10 can also be obtained by the following time dependent function:

$$\gamma_{XY}(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-\infty}^{\infty} x^*(t) \cdot y(t+\tau) dt \tag{2.11}$$

An important property of the cross-correlation function is that its Fourier transform yields the cross-power spectrum:

$$\Gamma_{XY}(f) = F\left(\gamma_{XY}(\tau)\right) \tag{2.12}$$

$$\Gamma_{XY}(f) = \int_{-\infty}^{\infty} \gamma_{XY}(\tau) e^{-j2\cdot\pi f\tau} d\tau \tag{2.13}$$

$$\tag{2.14}$$

Convolution and cross-correlation are very similar:

$$x(t) * y(t) = \int_{-\infty}^{\infty} x(\tau) \cdot y(\tau - t) d\tau \tag{2.15}$$

$$x(t) \star y(t) = \int_{-\infty}^{\infty} x^*(\tau) \cdot y(\tau + t) d\tau \tag{2.16}$$

$$x(t) \star y(t) = x^*(-t) * y(t) \tag{2.17}$$

Where $\star$ denotes the cross-correlation operation and $*$ denotes convolution. Because convolution in the time domain is multiplication in frequency domain, the cross power spectrum of signals x and y is:

$$\Gamma_{XY}(f) = X^*(f) \cdot Y(f) \tag{2.18}$$

where $X(f)$ and $Y(f)$ are the spectra of x and y respectively, obtained via the Fourier transform:

$$X(f) = F(x(t)) \tag{2.19}$$
$$Y(f) = F(y(t)) \tag{2.20}$$

2.2.3 Discrete-time and -frequency representation

A discrete-time version of the above described cross-correlation function exists. The input signal is sampled with frequency f_s. The estimated cross-correlation function then becomes:

$$r_{XY}(n) = \lim_{M\to\infty} \frac{1}{2 \cdot (M+1)} \sum_{m=-M}^{M} x^*(m) \cdot y(m+n) \tag{2.21}$$

$$\tag{2.22}$$

Analogous to the continuous time case, the discrete-time cross-correlation function can be converted to the frequency domain by the discrete-time Fourier Transform:

$$R_{XY}(f) = F\left(r_{XY}(n)\right) \tag{2.23}$$
$$R_{XY}(f) = \sum_{n=-\infty}^{\infty} r_{XY}(n) \cdot e^{-j2\pi \frac{f}{f_s} n} \tag{2.24}$$

When the result of this transform is estimated by a digital system, a discrete-frequency representation is required. This is obtained by applying a discrete Fourier transform (DFT):

$$R_{XY}(k) = DFT\left(r_{XY}(n)\right) \tag{2.25}$$
$$R_{XY}(k) = \sum_{n=0}^{N-1} r_{XY}(n) \cdot e^{-j\frac{2\pi}{N} nk} \tag{2.26}$$

Again analogous to the continuous case, the cross-power spectrum can also be obtained by the product of the conjugate spectrum of $x(n)$ and the spectrum of $y(n)$:

$$R_{XY}(k) = X^*(k) \cdot Y(k) \tag{2.27}$$

For a practical implementation this function has to be estimated. There are different estimators of the discrete cross-correlation function found in literature [12], of which two are widely used: the biased estimator and the unbiased estimator [5]. The unbiased estimator yields larger mean-square error. The biased estimator is focused on and is described in Section 2.2.4. Under plausible assumptions both estimators give comparable performance, so choosing one or the other is does not make a difference. For detailed information, see [5].

2.2.4 Estimation of the discrete-time and -frequency cross-correlation function

The estimator for cross-correlation is described in discrete-time and discrete-frequency domain in following paragraphs.

Time domain cross-correlation estimator When the summing interval of Equation 2.21 is reduced to a realistic value, a biased estimator appears. When samples are available for $0 < n < N-1$ and all other samples are set zero, the summation interval reduces to $0 < n < N-1$:

$$c_{XY}(k) = \frac{1}{N} \sum_{n=0}^{N-1} (x^*(n) \cdot y(n+k)) \tag{2.28}$$

$$\tag{2.29}$$

The estimator gives output values for $(-N+1) < k < (N-1)$. For large $|k|$ a relatively small number of products is available. The estimation is then less accurate because the factor $\frac{1}{N}$ does not correspond to the number of available products. This error is referred to as the estimator bias and is described in [5]. When N is large with respect to k, the bias is small and as N goes to infinity the bias converges to zero. The estimated cross-power spectrum is now obtained by Discrete Fourier transforming c_{XY}:

$$C_{XY} = DFT(c_{XY}) \tag{2.30}$$

Obtaining the cross-power spectrum by correlation prior to Fourier transformation is referred to as XF correlation.

Frequency domain cross-correlation estimator The frequency domain version of the estimator calculates the spectra of parts of signal $x(m)$ and $y(m)$ and multiplies them:

$$X(f) = \sum_{n=-\infty}^{\infty} x(n) \cdot e^{-j\frac{2\pi}{N}nf} \tag{2.31}$$

$$Y(f) = \sum_{n=-\infty}^{\infty} y(n) \cdot e^{-j\frac{2\pi}{N}nf} \tag{2.32}$$

$$C_{XY} = X^*(f) \cdot Y(f) \tag{2.33}$$

Obtaining the cross-power spectrum by discrete Fourier transformation prior to correlation is referred to as FX correlation.

2.2.5 Auto-correlation, Cross-correlation and spectrum estimation

In traditional spectrum analyzers the Power Spectral Density (PSD) is a result of auto-correlation and is equal to the cross-correlation front end when no uncorrelated components are present in the input signals. When two signals $x(t), y(t)$ are composed of correlated components $s(t)$ and uncorrelated

components $u_1(t), u_2(t)$, their cross-correlation function is:

$$\gamma_{XY}(t) = \lim_{T\to\infty} \frac{1}{2T} \int_{-\infty}^{\infty} x^*(\tau) \cdot y(t+\tau) d\tau \quad (2.34)$$

$$= \lim_{T\to\infty} \frac{1}{2T} \int_{-\infty}^{\infty} (s(\tau) + u_1(\tau))^* \cdot (s(t+\tau) + u_2(t+\tau)) d\tau \quad (2.35)$$

$$= \gamma_{ss}(t) + \gamma_{su_2}(t) + \gamma_{u_1 s}(t) + \gamma_{u_1 u_2}(t) \quad (2.36)$$

$$= \gamma_{ss}(t) \quad (2.37)$$

And thus the resulting power spectrum converges to the power spectrum of $s(t)$.

When multiple spectra of the cross-correlation front-end are averaged, the correlated components of the two input signals converge to their actual values and the uncorrelated components of the input signals converge to zero.

Power spectrum variance Due to randomness of noise and limited measurement time, the noise floor in an estimated spectrum is not the same in different measurements. For Gaussian distributed noise the distribution of the noise PSD components is also Gaussian. To express the noise floor, the standard deviation of the power spectrum components is used.

$$Noisefloor = \sigma_{PSD_n} = \sqrt{var(PSD_n)} \quad (2.38)$$

where PSD_n denotes the PSD of the noise. In order to estimate the noise floor in auto- and cross-power spectra, the mean and standard deviation of the signal's PSD must be estimated.

For the variance of the cross-power estimator in Equation 2.33, the variance of the estimated cross-power spectrum converges to the squared cross-power spectrum of signals x and y [5]. In other words, as the measurement time increases, the variance per Hertz does not decrease:

$$\lim_{N\to\infty} var(C_{XY}(f)) = |\Gamma_{XY}(f)|^2 \quad (2.39)$$

As the variance of the signal does not converge to zero, the estimation output does not converge to the value being estimated. The variance per resolution bandwidth remains constant: The estimator is *inconsistent*. To get a consistent cross-power spectrum estimator, spectral averaging is applied.

Spectral averaging Spectral averaging is applied to the output of the cross-correlation estimation to reduce the variance per resolution bandwidth such that it results in a consistent estimation. There are several methods of spectral averaging, the method described below is the Bartlett-method (also used for the cross-correlation spectrum analyzer of the previous work). The Bartlett-method splits a measurement in L sequences of length K and averages the spectra of those sequences.

$$C_{XY}(f) = \frac{1}{L} \cdot \sum_{l=0}^{L} (X_l(f) \cdot Y_l^*(f)) \quad (2.40)$$

For the true cross-power spectrum, the spectral variance reduces when the measurement time is increased and the cross-power spectrum will converge to the power spectrum of its correlated signal components:

$$var(\Gamma_{XY}) = \frac{1}{L} var\left(\Gamma_{ss} + \Gamma_{su_2} + \Gamma_{u_1 s} + \Gamma_{u_1 u_2}\right) \tag{2.41}$$

The noise floor standard deviation thus decreases by the square root of the relative increase in measurement time.

$$\sigma(\Gamma_{XY}) = \sqrt{\frac{1}{L}} \sqrt{\sigma(\Gamma_{ss}) + \sigma(\Gamma_{su_2} + \Gamma_{u_1 s} + \Gamma_{u_1 u_2})} \tag{2.42}$$

The reduction of spectral variance of the cross-power spectrum is approximately equal to the reduction of spectral variance of the estimated spectrum:

$$\sigma(C_{XY}) \approx \sqrt{\frac{1}{L}} \sqrt{\sigma(C_{ss}) + \sigma(C_{su_2} + C_{u_1 s} + C_{u_1 u_2})} \tag{2.43}$$

because:

$$\Gamma_{XY} \approx C_{XY} \tag{2.44}$$

When a cross-spectrum is averaged, its components converge to their actual values: the variance is reduced. For an uncorrelated signal, the cross-spectrum power is 0, so according to Equation 2.42 the uncorrelated components decrease by $\sqrt{\frac{1}{L}}$. So as a rule of thumb, the standard deviation of the noise floor in a power spectrum decreases by 1.5 dB per doubling of measurement time. This in contrast to auto-correlation, where the mean of the noise floor is non-zero and the absolute noise floor converges to that mean. Figure 2.3 depicts a block diagram of a cross-correlation spectrum averaging front-end.

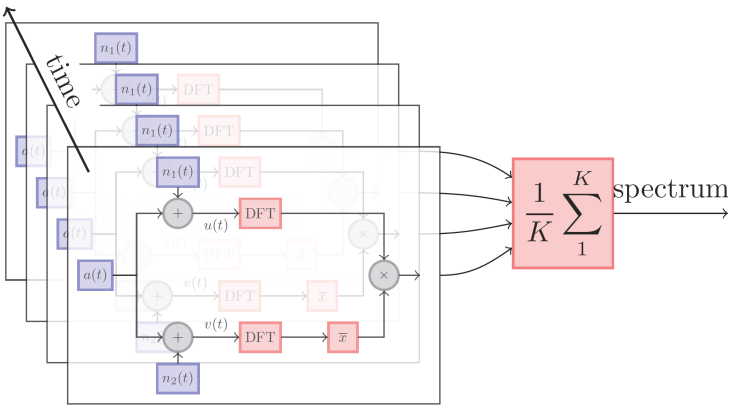

Figure 2.3: Block diagram of the operation of a cross-correlation spectrum averaging front-end. [4]

Auto-correlation and Cross-correlation spectrum For autocorrelation, X and Y in Equation 2.42 are equal. This results in a sequence of absolute real

values. The expected value is non-zero and thus the noise floor converges to a non-zero value. Figure 2.4 illustrates the convergence of an auto-correlation spectrum to its expected value. For cross-correlation, X and Y in Equation 2.42 are unequal. This results in a sequence of complex values. The expected value is zero if the noise signals are fully uncorrelated and the noise floor converges to zero. Figure 2.4 illustrates the convergence of a cross-correlation spectrum to its expected value.

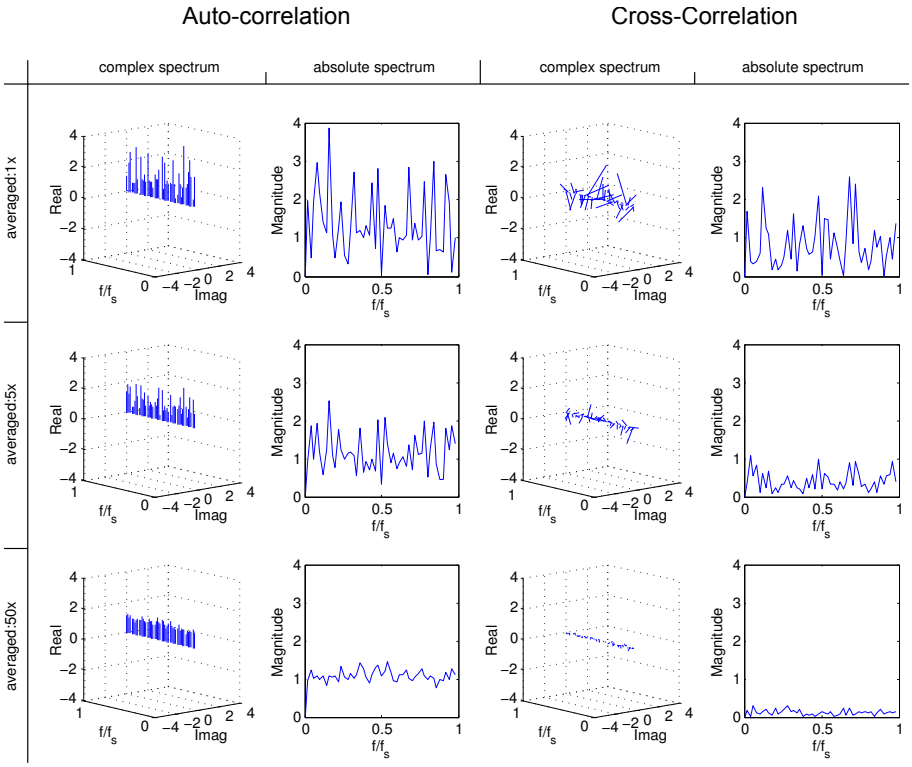

Figure 2.4: Convergence of power spectra when spectrum averaging is applied.

2.3 Cross-correlation spectrum analyzer

This section describes the specific front-end which is used in the previous work [4] and on which assumptions and system calculations are based. First an FFT spectrum analyzer is described and then the cross-correlation spectrum analyzer is described. The latter can be seen as an extension to the FFT spectrum analyzer.

2.3.1 FFT spectrum analyzer

The FFT spectrum analyzer obtains spectrum information by Fast-Fourier-Transforming the input signal. The input signal is first filtered, amplified and down-mixed before it is converted to the digital domain where the FFT is calculated. Figure 2.5 shows a block diagram of this front-end. (In this figure the noise floor is a bit exaggerated to emphasize the benefit of the cross-correlation spectrum analyzer in following figures).

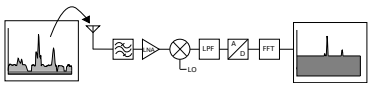

Figure 2.5: Typical analog front-end

By choosing the mixing frequency, the Intermediate Frequency (IF) band can be selected. A number of possible ranges are identified, each having their advantages. In the following sections zero-IF range is elaborated, as it is used in previous work and allows the largest bandwidth to be converted to the digital domain.

2.3.2 Cross-correlation spectrum analyzer

The cross-correlation spectrum analyzer consists of two FFT spectrum analyzers placed in parallel. The FFT outputs are cross-correlated and averaged. It consists of a passive splitter to divide the signal power over the two signal paths. Because of the noise-linearity trade-off described in section 2.1 the signals are not amplified by Low Noise Amplfiefiers (LNA) but attenuated in both paths. Both signals are then down-mixed to zero-IF and converted to the digital domain by the ADCs. The digital section consists of two Fast Fourier Transform blocks, one of the results is conjugated and the two spectra are multiplied element-wise. Multiple spectra are then averaged. Figure 2.6 shows a simple representation of the spectrum analyzer. The increased noise floor, due to the lack of LNAs, will be reduced when the output signals are cross-correlated. The theory from section 2.2 can be applied to this front-end. The effect of uncorrelated noise sources such as thermal noise from the mixer, ADC and attenuators is reduced in the power spectrum. The noise added by the attenuators is partially correlated [6], so the correlated noise originates from the antenna, the passive splitter and attenuator.

In Figure 2.6 the uncorrelated noise power is represented by the gradient-filled areas and is reduced in the final spectrum. The correlated noise power is represented by the solid-filled gray area and is not reduced.

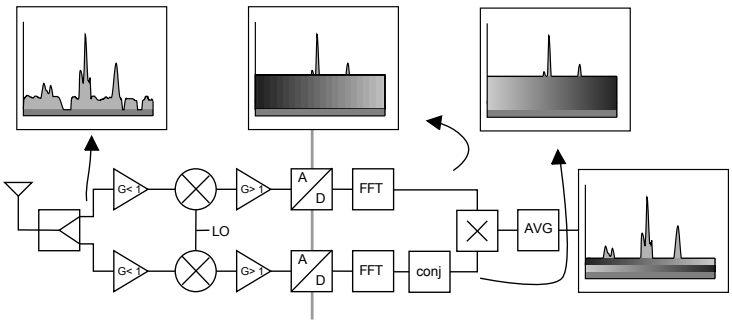

Figure 2.6: Cross-correlation spectrum analyser

The signal is down-mixed to zero-if, such that both negative and positive frequencies contain information. By using quadrature mixing the negative frequencies can be distinguished from the positive frequencies. Each path of the front-end thus consists of an I and a Q path resulting in four ADCs for the total front-end. Figure 2.7 shows the spectrum analyzer with quadrature mixing. Although not shown in the figure, the analog part of the front-end is

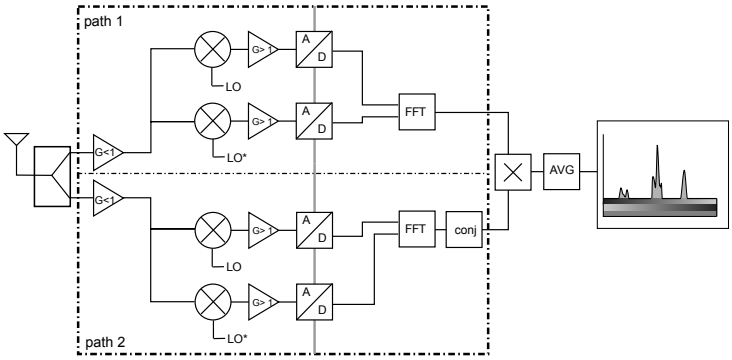

Figure 2.7: Quadrature mixing FX cross-correlation spectrum analyzer (LO* denotes the 90 degrees shifted oscillator signal phase)

differential.

2.3.2.1 Gain location

Cross-correlation reduces the uncorrelated noise in the signal spectrum, so the input signal is attenuated just after the signal has been split into two paths to increase linearity. The splitting itself also attenuates the power by 6 dB per path [4]. Because the power of the incoming signal is not exactly known, a variable attenuator is required to scale the signal properly and have maximal benefit of the cross-correlation and spectrum averaging. The attenuator described in this section is based on the splitter described in [4] with adjustable resistor values as described in [5].
The passive splitter divides the power of the incoming signal over the input impedances of the mixers. It also attenuates the signal. By choosing resistor

values of the passive splitter, the attenuation can be set. Figure 2.8 shows the differential passive splitter.

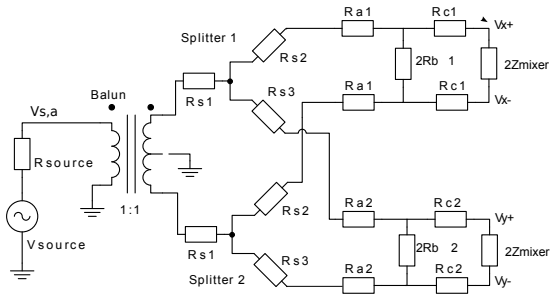

Figure 2.8: Passive splitter [6]

The splitter (R_{s_1} to R_{s_3}) together with the attenuator $R_{a_i}, R_{b_i}, R_{c_i}$ allows to attenuate the signal and control the system IF bandwidth [5].

The attenuation of the signal before the mixer reduces the amount of distortion produced by the mixer. For proper conversion to the digital domain, the signal must be scaled to fit the ADC input range. The signal is thus amplified before the ADC conversion.

2.3.2.2 XF and FX correlation spectrum analyzer

As described in Section 2.2.4 the cross-power spectrum can be estimated in two ways: using an FX- or an XF cross-correlation spectrum analyzer. Until this paragraph the front-end illustrations show spectrum analyzers where the signal is transformed to a discrete spectrum prior to the cross-correlation. Figure 2.9 shows the XF correlation spectrum analyzer.

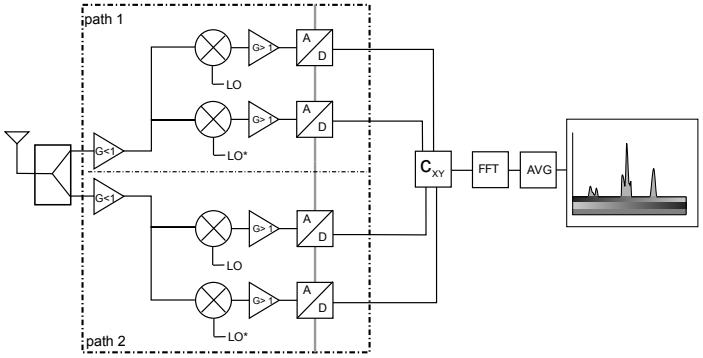

Figure 2.9: Quadrature mixing XF cross-correlation spectrum analyzer (LO* denotes the 90 degrees shifted oscillator signal phase)

2.3.2.3 Cost of the ADC and digital back-end

The cost of a spectrum analyzer is partially determined by the ADCs and the digital back-end. The cost in this context is power consumption and required

silicon area. Following paragraphs discuss the dependency of cost on digital signal resolution.

ADC The cost of an ADC depends on topology, sample frequency and resolution. When the resolution is lowered the number of comparisons per conversion is reduced and thus the power per conversion is reduced. Reduction of resolution decreases complexity in a way which depends on the topology of the ADC. A flash ADC for instance consists of a comparator for each , the number of comparators is reduced and therefore the amount of silicon area is reduced.

Digital back-end For the digital back-end, a higher sampling frequency leads to more dynamic power consumption, because parasitic capacitances are charged and discharged more often [13]. Higher resolution leads to more digital logic and thus to more parasitic capacitances and more silicon area. When the dependency of cost on resolution is considered, the digital implementation becomes important. For the cross-correlation spectrum analyzer the dependence of cost on resolution may be different for a FX or a XF correlation. When the XF correlator is used, the digital signals are correlated just after the analog to digital conversion. The signal resolution is determined by the resolution of the ADC. When the output of the correlator is transformed to a discrete spectrum, the signal resolution is determined by the desired sensitivity of the spectrum analyzer. For a lower resolution, the reduction of cost is clearly located in the XF correlator.

When the FX correlator is used, the lower resolution also leads to cost reduction. The FFT modules have low resolution input signals and high resolution output signals. The resolution of internal nodes will increase as the signal travels trough the FFT module. The exact reduction of cost is less obvious than in the XF correlator case. Also, to compare the cost the time-domain correlator cost must be compared to the frequency-domain correlator. More information on both and other correlators can be found in [5] and [14]

2.4 Summary and conclusions

Summary The cross-correlation spectrum analyzer increases the SFDR by adding the factor measurement-time to the trade-off between noise and linearity. Cross-correlation is a statistical property which can be estimated in discrete-time and discrete-frequency domain. The latter is done by the cross-correlation spectrum analyzer. This spectrum analyzer attenuates the input signal to reduce non-linearity introduced by the mixer. After the mixer the signal is amplified to meet the ADC input range before conversion to the digital domain. In the digital domain the spectrum estimate is calculated. The power and silicon-area cost of the digital processing largely depend on the input signal word-size.

Conclusions Cross-correlation is an effective way to increase the SFDR of a spectrum analyzer when the noise power per spectrum bin limits SFDR. Noise power added in the parallel paths of a cross-correlation spectrum analyzer is reduced at the cost of measurement time. The mixer in the analog front-end introduces distortion, which is reduced when the signal is attenuated prior to

entering the mixer. At the output of the mixer, an amplifier is required to scale the signal for proper AD conversion Reduction of ADC resolution will clearly reduce the digital complexity in the case of the XF correlator. For an FX correlator it is less straight-forward to determine the complexity reduction .

Chapter 3

Low resolution analog to digital conversion

In the previous chapter the concept of cross-correlation estimation and the cross-correlation spectrum analyzer are introduced. When the cross-correlation spectrum analyzer is integrated on chip, a low-cost ADC is preferred. The cost of ADCs can be reduced considerably by reducing the resolution. A low-resolution ADC will consume less power and occupy less chip area in contrast to higher resolution ADCs. Quantization is a non-linear function. The IIP3 of a quantizer largely depends on its resolution. Reduction of ADC resolution results in increase of the non-linearity. When the resolution is decreased too much, the SFDR of the spectrum analyzer is degraded to an unacceptable level. A possible counter measure to the non-linearity is to deliberately add noise to the input signal (dithering the input signal). The effect of lowering the resolution of an ADC is described by first describing the effect of quantization in general. Then the effects of low-resolution quantization and dithering are described. Different dithering approaches exist, of which one is described more extensively, as it is implemented on system level for this thesis (see Chapter 4).

3.1 Analog to digital conversion

Converting a signal from the analog domain to the digital domain consists of two orthogonal operations: quantization and sampling. Figure 3.1 shows the two operations. The order in which they are executed does not affect the result.

3.1.1 Sampling

Sampling converts a continuous-time signal to a discrete-time signal. At a single moment per period, the input signal is represented by a dirac pulse with a strength proportional to the input signal at that moment. In the ideal case these moments are spaced uniformly. When the Nyquist criterion is satisfied [15], the original signal can be reconstructed from the sampled signal and no information is lost.

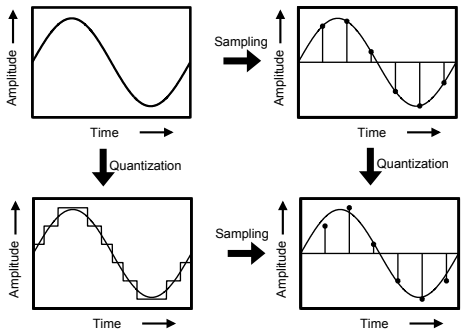

Figure 3.1: Analog to digital conversion: Sampling and Quantization

3.1.2 Quantization

A digital signal is described by a finite set of values. A quantizer rounds the analog signal to the nearest digital representation. In practice this means that the input signal is compared to *decision levels* to determine the digitized output. The possible quantizer output values are referred to as *quantization values*. The space between two decision levels is called the Least Significant Bit (LSB). Figure 3.2 illustrates the naming conventions. Quantization approaches exist where the decision levels are not located at equal distance, but for this thesis only quantizers with uniformly spaced decision levels are described. This type of quantization is referred to as *uniform quantization*.

There are two types of quantizers: *midtread* and *midrise* quantizers. Figure 3.3 shows a part of the transfer function of a midtread and a midrise quantizer.

The description in following sections apply to a quantizer of type midrise, which is used in this thesis because the midrise quantizer is symmetrical around zero. (the formulas have obvious analogs for midtread quantizers and all conclusions are also valid).

The symbolic representation of a quantizer is shown in Figure 3.4. The output of a midrise quantizer is given in Equation 3.1. In this equation the rounding is realized by applying the floor operator to the normalized input and adding a half LSB after scaling the result to an LSB:

$$y = Q(w) = \Delta \cdot \left\lfloor \frac{w}{\Delta} \right\rfloor + \frac{\Delta}{2} \tag{3.1}$$

where

- w: the input signal to the quantizer
- $Q(w)$: The quantization operation on input signal w
- Δ: The spacing between decision levels: an LSB

And the following is defined:

- $q = Q(w) - w$: The quantization error.

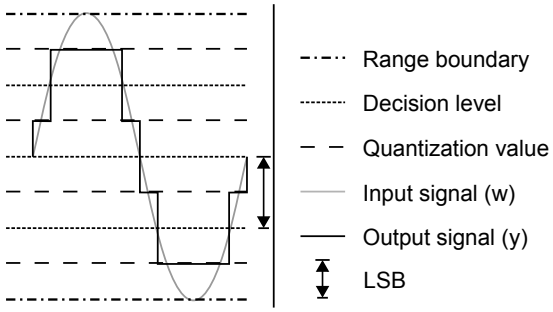

Figure 3.2: Quantizer naming conventions

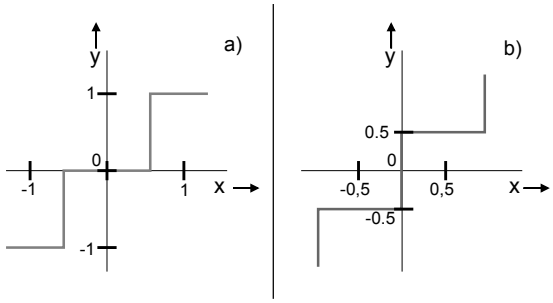

Figure 3.3: a) Midtread quantizer transfer function. b) Midrise quantizer transfer function.

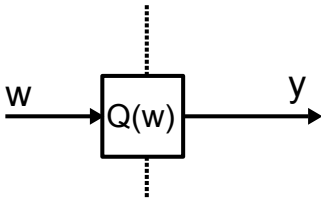

Figure 3.4: Quantizer symbol

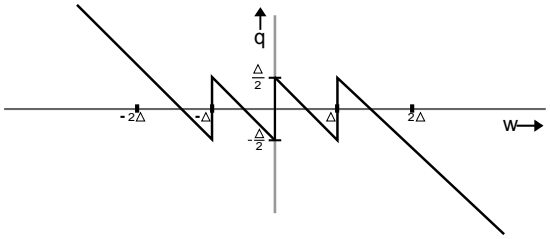

Figure 3.5: Quantization error signal of a two bit midrise quantizer

3.1.2.1 Quantization error

The quantization error q is the difference between the quantizer input and output. Figure 3.5 shows the quantization error as a function of the quantizer input w of a 2-bit quantizer. When the input signal is outside the input range of the ADC, the error signal is referred to as clipping error. This type of error is not addressed in this thesis, but conditions are obtained such that the influence is limited when the error is unavoidable. Detailed analysis of this type of error is found in [16].

Distortion Each input signal value has one quantization error value associated with it: i.e. for a given input signal, the quantization error is a deterministic signal. As a result the quantization error signal is correlated with the input signal. This correlation is inversely propertional to the resolution of the quantizer. When the input signal is periodic, the quantization error signal is periodic and will give distortion components in the output signal spectrum. In the spectrum of the distorted signal, harmonic distortion and inter-modulation products appear.

For instance when the input to the quantizer is a sine wave with frequency f, the output spectrum will contain frequency components at multiples of f. Figure 3.6 shows the quantization of a sine wave, the quantization error has distinct frequency components with higher frequencies.

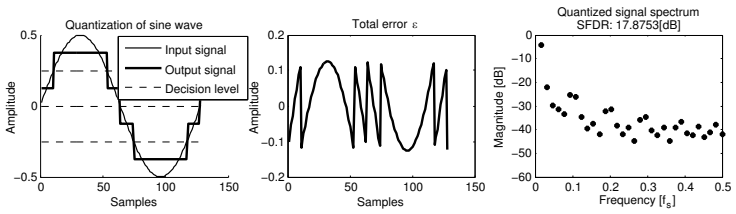

Figure 3.6: 2-bit Quantization of a sine wave and the quantization error.

For a uniform quantizer, based on a full scale sine wave input, the SFDR is [17]:

$$SFDR \approx 8.07 \cdot D + 3.29 \tag{3.2}$$

where b is the number of bits of the quantizer.

3.1.3 Models of quantization

There are different ways to look at quantization. A simplistic view is the classical model of quantization, which linearizes the quantization operation [18]. Another vies is to analyze the effect of non-linearity. Blachman describes an approach to calculate distortion components [19]. In practical situations noise is present which improves the SFDR. This improvement in SFDR is exploited when the signal is dithered. Dithering is deliberately adding a noise signal to the input signal to control distortion components.

3.1.3.1 Classical model of quantization

The classical model of quantization [18] approximates the effects of quantization by assuming that the quantization noise is uncorrelated with the input signal, has a white spectrum and is uniformly distributed. The result of quantization is then easily described by white noise added to the input signal. The power of the quantization error is [20] a function of its Probability Distribution Function (PDF) ($p_q(q)$):

$$p_q(q) = \frac{1}{\Delta},\ for\ \frac{-\Delta}{2} < q < \frac{\Delta}{2} \tag{3.3}$$

$$\tag{3.4}$$

such that the power is:

$$E(q^2) = \int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} q^2 \cdot p_q(q)dt = \frac{\Delta^2}{12} \tag{3.5}$$

3.1.3.2 Spectrum of quantized signals

The exact magnitude and phase of distortion components can be calculated with the method described in [19]. The quantization error for a single sine wave input is expressed by its Fourier series [19]. The mathematical derivations are found in [19] for a midtread quantizer. The modification to this derivation for a midrise quantizer can be found in Appendix A. The result is:

$$w = A \cdot sin(\theta(t)) \tag{3.6}$$

$$q(w) = \sum_{p=1,3,5,7,\ldots}^{\infty} \left(\sum_{n=1}^{\infty} \frac{2}{\pi n} J_p(2\pi \cdot n \cdot A) sin(p \cdot \theta(t)) \right) \tag{3.7}$$

where $J_p(2\pi \cdot n \cdot A)$ is the Bessel function of the first kind.

When the input signal is a sum of multiple sine waves, the number of distortion components increases exponentially. As an example, the Fourier series for two sine waves is obtained by extending the approach of [19]:

$$w = A_1 \cdot \sin(\theta_1(t)) + A_2 \cdot \sin(\theta_2(t)) \tag{3.8}$$

$$\begin{aligned} q(w) = imag\{ \sum_{p=-\infty}^{\infty} \sum_{q=-\infty}^{\infty} \Bigg(\sum_{n=1}^{\infty} \frac{1}{n\pi} J_p(2\pi \cdot n \cdot A_1) \cdot e^{i\ p\ \theta_1} \cdot \\ J_q(2\pi \cdot n \cdot A_2) \cdot e^{i\ q\ \theta_2} \Bigg) \} \end{aligned} \tag{3.9}$$

If the input signal remains within the quantizer input range, the expected quantization error power cannot exceed $\left(\frac{\Delta}{2}\right)^2$, as the error has a maximum value of $\frac{\Delta}{2}$. The number of distortion components in the spectrum increases exponentially with respect to the number of sinusoids at the input, so the power per distortion component decreases: adding more frequency components reduces the average power per distortion frequency component. When white noise is added this effect is maximally utilized, because it contains an infinite

number of sinusoids. How well the power of the quantization error is distributed across the spectrum depends on the amount of power of the white noise and whether it is statistically independent of the input signal. As a conclusion, adding white noise to the signal is an effective way to decrease distortion components and thus increase linearity. Adding a signal to reduce distortion components is known as *dithering*.

3.2 Dither

Quantization of a signal is a non-linear process which adds undesired distortion and inter-modulation components to the signal. Dithering is a process applied to the signal *before* the non-linear operation to control these undesired components. In many applications dithering adds a random signal to an input signal.

For energy detection spectrum sensing the power and spectral distribution of the dither signal and quantization noise must be known, such that signal power can be distinguished from the noise power. This is achieved when the ADC generates an error with a white spectrum. The noise floor of the output signal is then also white. This is achieved by dithering the input to the quantizer.

This section discusses different dithering schemes. Each scheme has its advantages and disadvantages and its suitability depends on the application it is used in. First dithering is explained intuitively.

3.2.0.3 Dither, intuitive approach

Without dithering, an input value can result in only one error value, so when the input signal is periodic the quantization error signal is periodic. The periodicity would not be present when an input value could result in any quantization error with equal probability. This is achieved with proper dithering. Figure 3.7 shows that the periodicity of the error signal is not present when a sine wave is dithered with uniform distributed dither with a range of 1 LSB. With this kind of dither each quantization error value is equally probable.

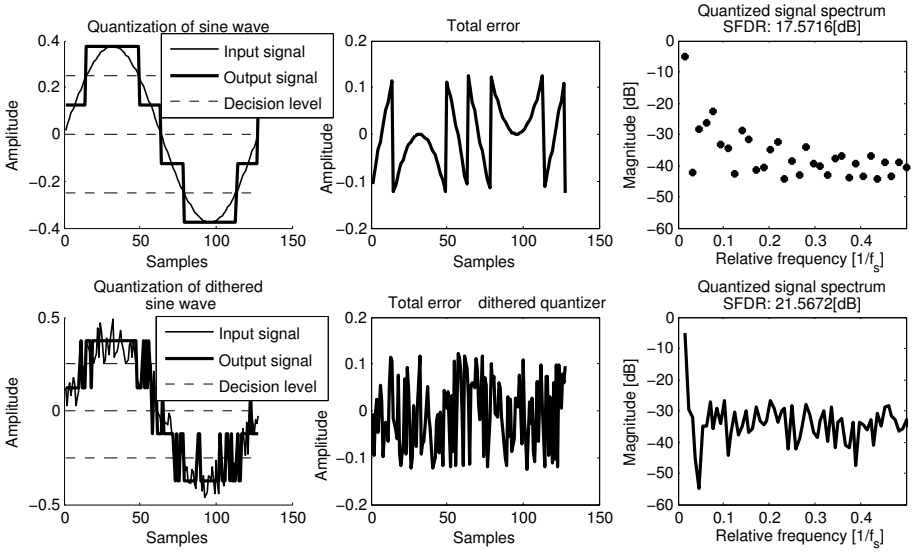

Figure 3.7: Quantized undithered and dithered sine wave with an amplitude of $\frac{3}{4}$ full scale, the error signal and spectrum. The spectrum of the undithered signal only contains odd harmonics of the fundamental frequency, the spectrum of the dithered signal also has frequencies at even harmonic frequencies.

3.2.1 Dithering schemes

Many different dithering schemes can be found in literature [18], [21], [22], [23]. The most important differences between the schemes are:

1. Subtractive or non-subtractive dither
2. Type of dither signal PDF
3. Bandwidth of the dither signal

The advantages and disadvantages of these differences are described. At the end of this section the approach is selected which fits the goals of this thesis best.

3.2.1.1 Subtractive or non-subtractive dither

Adding dither to the input signal decreases distortion components, but the quantized signal also contains the dither signal. Figure 3.13 shows the block diagram of a non-subtractive dithered quantizer.

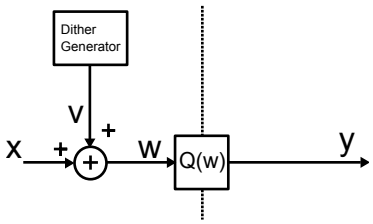

Figure 3.8: Dithered quantizer

In subtractive dithering the dither signal power is removed from the quantizer output signal by subtracting a digital version of the dither signal from the quantizer output signal. In [24] the concept of subtractive dither is introduced. In this paper digital images are dithered and quantized before they are transmitted over a channel with limited capacity, then after reception the dither is subtracted. This way the bandwidth of the transmitted signal can be reduced while the distortion in the image is acceptable. Figure 3.9 shows a subtractive dithered quantizer.

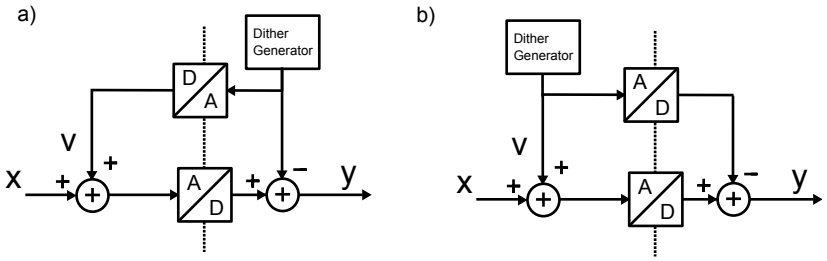

Figure 3.9: Subtractive dither quantizer. The dither source can be in: a) digital or b) analog domain.

For a spectrum analyzer subtractive dithering leads to an increase of digital resolution just after the quantization, so the benefit from resolution reduction of the ADC is decreased when the dither is subtracted. I.e. the resolution reduction leads to only little complexity reduction as the digital processing complexity is not reduced. The ADC resolution is reduced, but not the digital word resolution. However, because the ADC resolution is lowered, this may still be a interesting option. Comparing non-subtractive dithering to subtractive dithering; the latter results in less noise power, but the first achieves more complexity reduction.

3.2.1.2 Type of dither signal

Most natural noise sources produce signals with an amplitude which has a Gaussian distributed PDF. For instance, the voltage and current amplitude of the thermal noise of a resistor is Gaussian distributed. However, dither signals with other specific PDFs lead to a higher SFDR.

Gaussian distributed noise In [17] the effect of Gaussian distributed noise is analyzed. Adding a Gaussian distributed noise signal increases the SFDR, Equation 3.2 is extended to:

$$SFDR \approx 8.07 \cdot D + 3.29 + 171.5 \cdot \sigma_{LSB}^2 \tag{3.10}$$

where σ_{LSB}^2 is the power of the noise in LSB^2. This might look very promising, however two performance limiting effects are introduced when increasing Gaussian distributed dither signal power:

1. The noise floor is raised.
2. Signal values falling outside the quantizer input range introduce clipping distortion.

The clipping distortion problem is reduced by attenuating the input signal, but the noise floor becomes more dominant and the SFDR is reduced. Figure 3.10 shows the dithered quantizer with attenuated input signal.

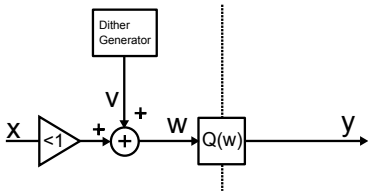

Figure 3.10: Dithered quantizer with attenuated input signal.

In [17] the allowed probability of a value being clipped is coarsely estimated. According to this estimation, for an 8-bit quantizer, the probability of clipped values must be less than 0.13 % to have no discernible distortion. For lower resolutions, for example 2 bits, the resulting distortion and required attenuation results in unacceptable SFDR values. The estimation of [17] does not correctly approximate the allowed clipping for a 2-bit quantizer when the target SFDR is 60 dB. This is concluded from simulation results. Time domain simulations

in MATLAB show the relation between Gaussian distributed noise power and required attenuation of the input signal to allow a certain SFDR. The result of this simulation is shown in Figure 3.11. The SFDR is obtained for an amount of noise power and a certain amplitude of the sine wave input. The amount of noise power results from equation 3.10:

$$\sigma_{LSB}^2 = \frac{SFDR_{target} - 3.29 - 8.07 \cdot D}{171.5} \tag{3.11}$$

For a SFDR of 60 dB the input signal must be attenuated by 20 dB, relative to a full scale sine wave. The amount of dither power is roughly equal to the dithering alternatives of next paragraphs, thus the resulting dither and quantization noise floor is roughly equal. However, the 20 dB attenuation makes this dithering option not attractive.

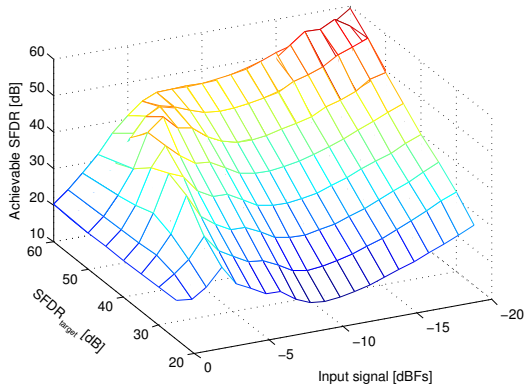

Figure 3.11: Achievable SFDR for Gaussian distributed dither and signal attenuation. MATLAB code snippet can be found in Appendix C.2.

Non-Gaussian distributed noise Dither signals with other distributions lead to less required signal attenuation and a fixed amount of noise power. Finding a signals with specific distributions in the analog domain is not trivial, therefore the dither signal is generated in the digital domain and then converted to the analog domain by a Digital to Analog Converter (DAC), this is illustrated in Figure 3.9.b. Section 3.3 elaborates these types of dither signals extensively, the required signal attenuation is 2.5 dB or 6 dB depending on the exact dither signal.

3.2.1.3 Bandwidth of the dither signal

A dither signal can have a bandwidth which is a fraction of the measurement bandwidth. This is referred to as band-limited dither or narrow-band dither. When the used dither signal has a bandwidth equal to the measurement bandwidth, this is referred to as wide-band dithering. When the dither signal band is only a part of the measured band, the other part of the band does not suffer from higher noise power levels. This might sound promising, but generation of band-limited dither with a specific non-Gaussian PDF is difficult or may be

impossible. The signal must be for instance uniformly distributed (see section 3.3.1.2 for more details). When a white signal with a uniform PDF is filtered, the resulting PDF becomes more Gaussian like. This can be explained by the fact that filtering is summing time delayed versions of the same white signal, which is adding multiple independent signals with a uniform distribution. The creation of band-limited dither signals with specific PDF requirements is considered out of scope of this thesis and is not further investigated.

Figure 3.12 illustrates the principle of subtractive, non-subtractive and band-limited dithering: non-subtractive dither increases SFDR, but it is limited by the increased noise floor. Subtractive dither results in a lower noise floor. In the case of band-limited dither a part of the spectrum is dedicated for the dither signal power.

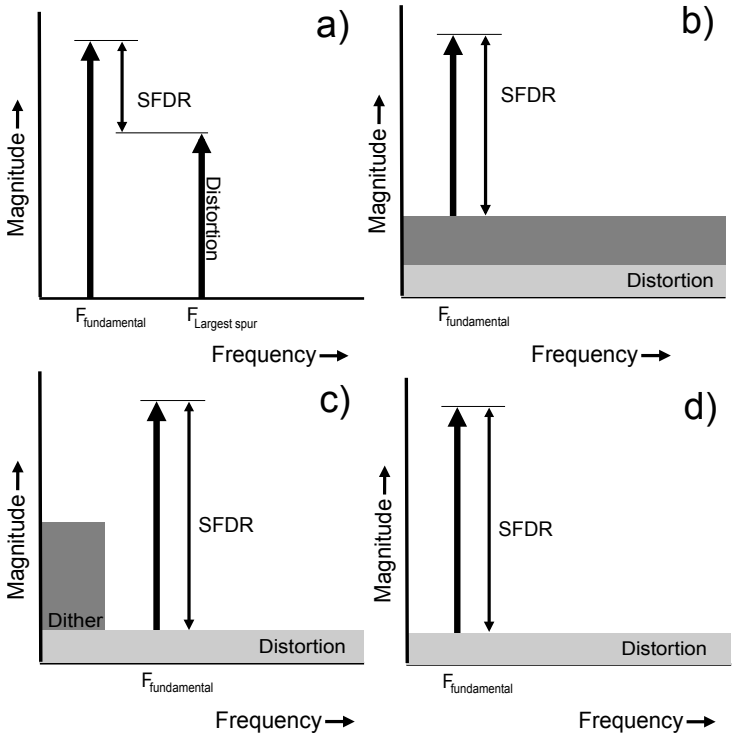

Figure 3.12: Dithering schemes and effect on SFDR: a) no dither. b) non-subtractive dither. c) band-limited dither. d) subtractive dither.

3.2.1.4 Dithering for an energy detection spectrum analyzer

The use of a Gaussian distributed dither signal results in a relatively high dither noise floor and thus a limited maximum input signal (compared to the quantizer full scale). A high SFDR then requires a longer measurement time or a smaller resolution bandwidth of the spectrum analyzer. The resolution bandwidth and a maximum measurement time is often defined per application, such that the achievable SFDR is acceptable. Dither signals with other proba-

bility distributions allow higher SFDR with less measurement time relative to the resolution bandwidth. I.e. these dither signals are more effective.

Subtractive dithering counteracts the complexity reduction of lowering the quantizer resolution to some extent and is therefore not chosen as an option for the energy detection spectrum analyzer.

Band-limited dithering requires a large part of the measured bandwidth and gives exceptional requirements for the dither signal PDF. Therefore non-subtractive wide-band dithering is the best option for the cross-correlation spectrum analyzer and is described in next sections.

3.3 Non-subtractive dithered 2-bit Quantizer

This section describes the most effective fundamentals for making a proper choice of which dither signal is used. Because the intuive approach as described in 3.2.0.3 does not reveal all relations of the dither signal and the total error spectrum, a mathematical approach found in literature is summarized. Requirements for the dither to render the quantization noise floor white are described.

Rectangular PDF and triangular PDF dither are described and rectangular PDF dither is described more intensively. Digital generation of these dither signals is described and the effect of quantizer non-linearity in a digital dithered quantizer is described. To this end the concept *equivalent quantizer* is introduced which provides a clear view on the SFDR of a dithered quantizer.

A non-subtractive dithered quantizer For a non-subtractive dithered quantizer the following signals are defined.

- x: the input signal of the system
- v: the dither signal
- $w \triangleq x + v$: the input signal to the quantizer
- $Q(w)$: The quantization operation on input signal w
- $y = Q(w)$: the output signal of the system
- $\epsilon \triangleq y - x$ is the *total error* of a quantizing system.
- $q \triangleq Q(w) - w$ is the quantization error.

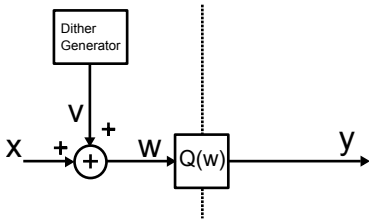

Figure 3.13: Dithered quantizer

By adding dither (v) to the input signal (x) of a quantizer, the system input is unequal to the quantizer input(w): $x \neq w$. As a result the quantization error ($q = y - w$) is unequal to the total error ($\epsilon = y - x$). The latter is called the *total error* and is the error in the resulting spectrum estimate. It should have a white spectrum in order to maximize the SFDR.

3.3.1 Dither signal statistics

The ultimate goal of dithering is to make the total error signal independent of the input signal. For a non-subtractive dither this is not possible, as will become clear in this section. However, certain moments of the error signal can be made independent of the input signal. In an energy detection spectrum analyzer, the task of dithering is to generate a total error with a white spectrum. Via the 'independence of moments theory' spectral whiteness can be assured for a certain type of dither. First the condition for moment independence is described and then the condition for spectral whiteness is given.

3.3.1.1 Independence of total error moments

The m^{th} moment is the expected value of ϵ^m [20]:

$$E[\epsilon^m] = \int_{-\infty}^{\infty} \epsilon^m \cdot p_\epsilon \, d\epsilon \tag{3.12}$$

Where p_ϵ is the PDF of ϵ. The m^{th} moment of the total error ϵ is made independent of the input signal by adding a dither signal which is the sum of m or more independent uniformly distributed random signals with a range of one LSB, which follows from the next description (summarized from [18]). The characteristic function of a signal is the inverse Fourier transform of the PDF of the signal. In [18] a requirement for the dither signal statistics is given such that it renders specific moments of the error signal independent of the input signal. When the characteristic function of the dither signal is P_v, then the m^{th} moment of the total error signal is independent if [18]: [1]

$$G_v^{(m)}\left(\frac{k}{\Delta}\right) = 0, \forall k \in \mathbb{Z}_0 \tag{3.13}$$

where

$$G_v^{(m)}(u) = \frac{d^m}{du^m}\left(\mathrm{sinc}_\Delta(u) \cdot P_v(u)\right) \tag{3.14}$$

$$\mathrm{sinc}_\Delta(u) \triangleq \frac{sin(\pi\Delta u)}{\pi\Delta u} \tag{3.15}$$

and $\mathbb{Z}_0$ is the set of all integers except 0. This condition thus defines a requirement for P_v. This requirement is fulfilled when Equation 3.13 is fulfilled [18]:

$$P_v(u) = \mathrm{sinc}_\Delta^m(u) \tag{3.16}$$

[1] the m^{th} power of x is denoted by x^m, the m^{th} derivative is denoted by $x^{(m)}$

Because then

$$G_v = \text{sinc}_\Delta^{m+1}(u) = \left(\frac{sin(\pi\Delta u)}{\pi\Delta u}\right)^{m+1} \tag{3.17}$$

and in the m^{th} derivative of this function each term contains the product with $sin(\pi\Delta u)$, which is 0 for $(u = \frac{k}{\Delta}, \forall k \in \mathbb{Z})$. So then $G_v^{(m)}\left(\frac{k}{\Delta}\right) = 0$ for all nonzero integers.

When Equation 3.13 is satisfied for m, the m_{th} moment is [18]:

$$E(\epsilon^m) = \left(\frac{j}{2\pi}\right)^m G_v^{(m)}(0) \tag{3.18}$$

Which is zero for $m \geq 1$ and $G_v = \text{sinc}_\Delta^2(u)$.

From characteristic function to dither signal p_v is obtained by Fourier transforming (F) P_v [20], [18]:

$$\begin{aligned} p_v &= F(P_v) && (3.19)\\ &= F(\text{sinc}_\Delta(u)^m) && (3.20)\\ &= \left[\star \prod_{l=0}^{m-1}\right] F(\text{sinc}_\Delta(u)) && (3.21)\\ &= \left[\star \prod_{l=0}^{m-1}\right] \Pi_\Delta && (3.22) \end{aligned}$$

where $\star \prod_{l=0}^{m-1}$ denotes the convolution of m statistically independent functions. The Fourier transform of the sinc_Δ function is the Π function, which is:

$$\Pi_\Delta(\omega) = \begin{cases} \frac{1}{\Delta}, & \text{if} -\frac{\Delta}{2} < \omega \leq \frac{\Delta}{2} \\ 0, & \text{otherwise} \end{cases} \tag{3.23}$$

Summation of independent signals results in convolution of their PDFs, thus for the m^{th} moment of ϵ to be independent of x, v should be the sum of m statistically independent uniform distributed signals with a range of $[-\frac{\Delta}{2}, \frac{\Delta}{2}]$.

Complete independence of the total error signal on the input signal is only achieved when an infinite number of uniform distributed functions are added, which results in a Gaussian distributed function with infinite power.

3.3.1.2 Rectangular and Triangular dither

When $m = 1$ and $m = 2$ in Equation 3.22 the resulting dither signals are referred to as *rectangular* and *triangular* PDF dither respectively. Rectangular PDF dither renders the first moment of the total error signal independent of the input signal, but not the second moment, i.e. the total error power depends on the input signal. When triangular PDF dither is applied, also the second moment of the total error signal is independent of the input signal, i.e. the total error power is constant. This is illustrated in Figure 3.14. In this figure the PDF of w is given for two values of x, for both dither functions. It can be seen that the total error power in the case of the rectangular dither depends on the input signal.

Spectral whiteness and noise uncertainty In [18] is proven that the total error spectrum is white, when triangular PDF dither is used ($m = 2$). However, simulation results show that for rectangular dither ($m = 1$) the spectrum is also white for an input signal which is the sum of any number of sinusoids. Figure 3.15 shows the whiteness of the total error spectrum. All simulation ran for this thesis with rectangular PDF dither confirms that the resulting total error spectrum is white.

Error power dependence of rectangular dithered signals When rectangular PDF dither is applied, the total error power depends on the input signal, but never exceeds $\frac{\Delta^2}{4}$. However, when the mean and power of the input signal is controlled, the total error power can be lowered to below $\frac{\Delta^2}{6}$.Figure 3.16 shows the total error power of a dithered quantized sine wave and a Gaussian distributed signal as function of its mean and power. This is concluded from analysis of [18] (elaborated in Appendix B.2) and simulation. The power of other signals in an energy detection spectrum analyzer are expected to also result in a total error power below $\frac{\Delta^2}{6}$,

Using rectangular dither has an advantage and disadvantage. Whether the performance is better for rectangular or triangular dither, requires more research. Using rectangular PDF dither results in a noise floor uncertainty, causing a SNR wall [25]. This has a negative effect on the probability of detection and probability of false alarm [26]. When mean and power of the input signal are controlled, the exact degradation of these probabilities depends on the input signal. As is elaborated in section 4.3, a rectangular PDF dither results in a larger ADC input range compared to triangular PDF dither. The lower noise power and large ADC input range are advantages of rectangular dither, but the noise uncertainty is a disadvantage. Knowledge on the type of input signal is required to calculate the theoretical performance of a energy detection spectrum analyzer. This calculation is not done in this thesis.

In following chapters the effects of digital dithering is elaborated. The effects on system non-linearities is elaborated using rectangular PDF dither. Most reasonings can be applied to triangular dither as well. System level simulations prove that the theoretical performance is a good estimate of the system level simulation performance for both types of dither.

3.3.1.3 Spectra of Dithered signals

Proper dithering gives a spectrum of a (low-resolution) quantized signal with a raised noise floor, but without distortion components. It causes the expected value of an output signal to become equal to the input signal. This is true in the time and in the frequency domain.

Time domain According to Equation 3.18 the first moment of ϵ is 0, for a dither signal which is the sum of one or more normal distributed signals:

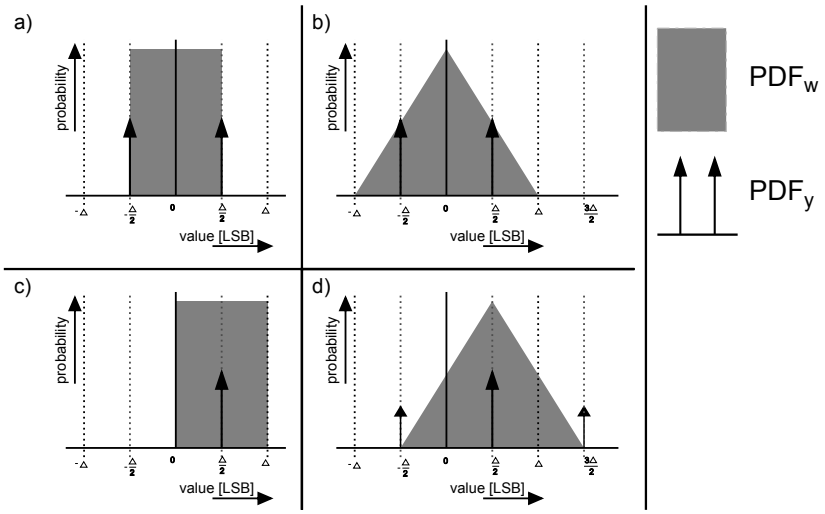

Figure 3.14: Illustration of dependency of total error power on input signal. For rectangular dither the total error power depends on the input signal.

a) Rectangular PDF dither, $x = 0$: maximal total error power: Whatever the dither value is, $\epsilon^2 = |y - x|^2$ is always $\frac{\Delta^2}{4}$.

b) Triangular PDF dither, $x = 0$: The total error power for any dither value is $\frac{\Delta^2}{4}$

c) Rectangular PDF dither, $x = \frac{\Delta}{2}$. Minimal total error power: Whatever the dither value is, $y = x$. The total error is 0.

d) Triangular PDF dither, $x = \frac{\Delta}{2}$. Still the total error power is equal to $\frac{\Delta^2}{4}$

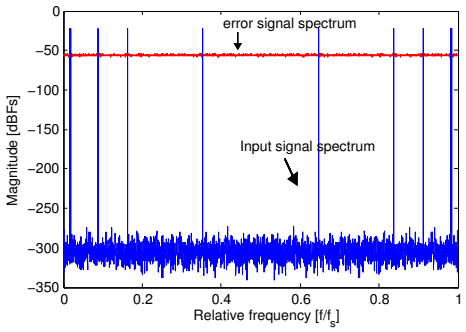

Figure 3.15: Spectra of rectangular dithered signal, consisting of five sinusoids. The signal and total error spectrum are shown.

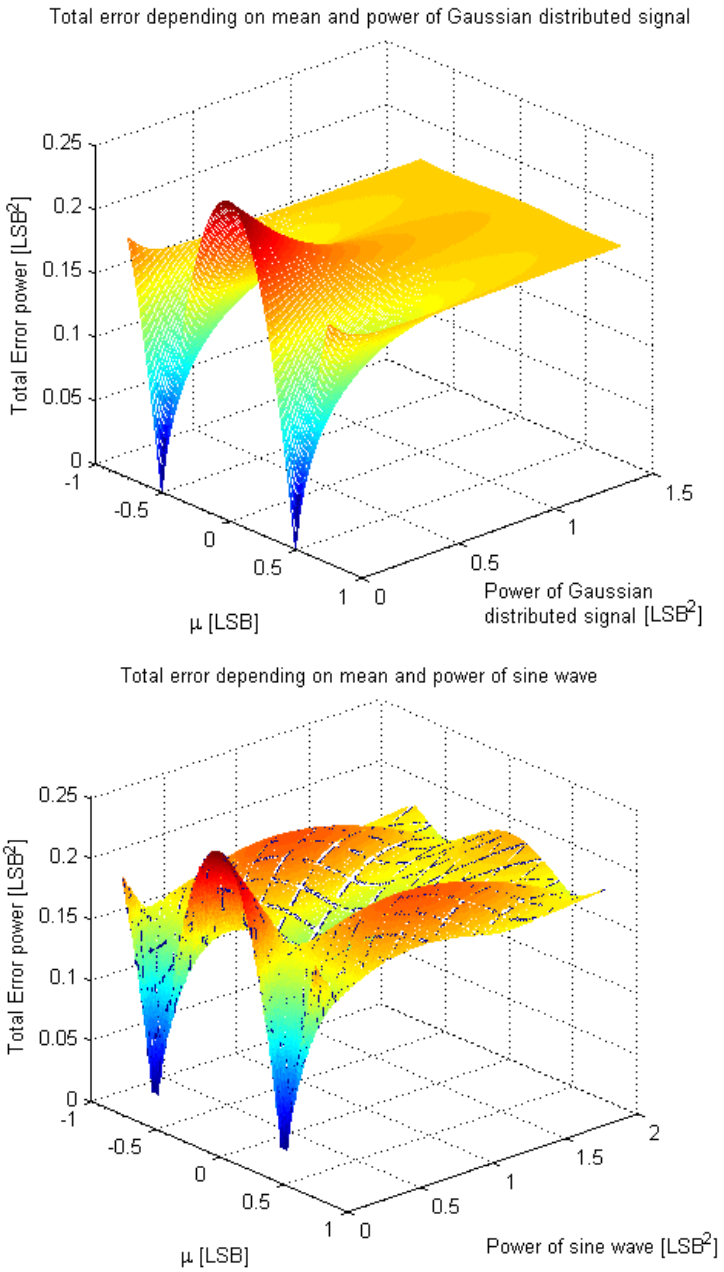

Figure 3.16: Total error depending on mean (μ) and power of Gaussian distributed signal (top) and sine wave (bottom) when dithered with a rectangular dither signal.

$$v = \left[\star \prod_{l=0}^{m-1} \right] \Pi_\Delta$$

$$\begin{aligned} E(\epsilon) &= 0 \\ E(y) &= E(Q(w)) \\ &= E(Q(w+x)) \\ &= E(\epsilon + x) \\ &= E(\epsilon) + E(x) \end{aligned}$$

$$E(y) = E(x) \tag{3.24}$$

Figure 3.17 illustrates the conclusion of 3.24 for rectangular dither ($v = \Pi_\Delta$). It shows the expected statistical output of three arbitrary values. The input values (x) are represented by black dots and for that value the value range of the quantizer input (w) is indicated by the black lines connected to the dot. The probabilities of the output values corresponding to x are shown by the circles on the quantization value lines. Suppose that x is a static value, w then produces two possible output values. The occurrence of both output values translate to $E(y)$.

Frequency domain To prove the equal expected values for the frequency domain, the expected values are written as the ensemble average. $y^{(s)}$ represents sample s of y taken from ensemble S.

$$E(y) = \lim_{S\to\infty} \frac{1}{S} \sum_{s=1}^{S} y^{(s)} \tag{3.25}$$

$$\tag{3.26}$$

The expected value of a frequency component is:

$$E(Y) = \lim_{S\to\infty} \frac{1}{S} \sum_{s=1}^{S} F(y_s) \tag{3.27}$$

$$\tag{3.28}$$

Filling in the Fourier transform, and rewriting the expression:

$$E(Y(f)) = \lim_{S\to\infty} \frac{1}{S} \sum_{s=1}^{S} \int_{-\infty}^{\infty} y_s(\tau) e^{-j\cdot 2\pi\cdot f\cdot \tau} d\tau \tag{3.29}$$

$$= \int_{-\infty}^{\infty} \left[\lim_{S\to\infty} \frac{1}{S} \sum_{s=1}^{S} y_s(\tau) \right] e^{-j\cdot 2\pi\cdot f\cdot \tau} d\tau \tag{3.30}$$

The term between square brackets is the expected value of y, which is equal to the expected value of x, thus:

$$E(Y(f)) = \int_{-\infty}^{\infty} \left[\lim_{S\to\infty} \frac{1}{S} \sum_{s=1}^{S} x_s(\tau) \right] e^{-j\cdot 2\pi\cdot f\cdot \tau} d\tau \tag{3.31}$$

$$= \lim_{S\to\infty} \frac{1}{S} \sum_{s=1}^{S} \int_{-\infty}^{\infty} x_s(\tau) e^{-j\cdot 2\pi\cdot f\cdot \tau} d\tau \tag{3.32}$$

$$= E(X(f)) \tag{3.33}$$

The same can be done for the Discrete Fourier Transform (DFT), such that:

$$E(Y(k)) = E(X(k)) \tag{3.34}$$

In a practical system, the frequency components $Y(k)$ are calculated from the values $y(n)$. The output resolution of $Y(k)$ is much higher than $y(n)$, but is limited. $Y(k)$ is then an estimate of $y(n)$: the estimated frequency component strength approximates the actual component strength.

$$Y(k) \approx X(k) \tag{3.35}$$

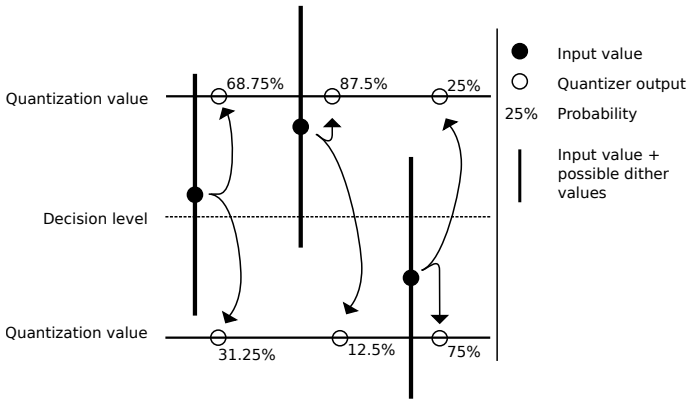

Figure 3.17: Statistical representation of three arbitrary values

3.3.2 Digitally generated dither

As described in the previous section, the condition of a dither signal to render the quantization error spectrum white is that the dither signal is the sum of one or more independent uniform distributed random signal with range of 1 LSB.

In the following sections the achievements of dither and non-linearity effects are discribed for rectangular PDF dither. On some points also triangular PDF dither is addressed. The exact achievements for triangular dither must can be derived using this approach. The effects of non-linearity are expected to hold the same relations with rectangular dither.

In the previous section the uniform distribution is assumed to be a continuous function. When the dither signal is generated in the digital domain, its

distribution function is discrete: the signal can assume only a finite number of values. Figure 3.18 shows the discrete and continuous PDF of a rectangular dither signal.

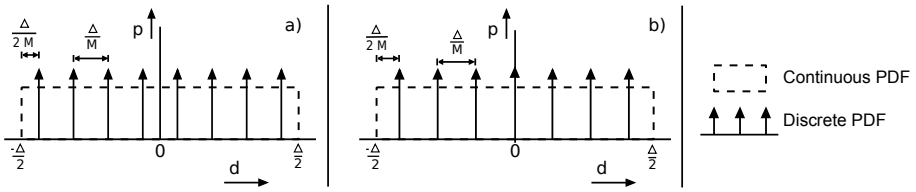

Figure 3.18: Continuous and discrete rectangular PDF dither. a) eight discrete dither values (M = 8), b) seven discrete dither values (M = 7).

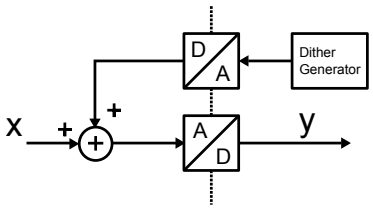

Figure 3.19: Digitally dithered quantizer

The digital dither must be converted to the analog domain such that it can be added to the analog signal before AD conversion. A basic digitally dithered quantizer system is shown in Figure 3.19.

3.3.2.1 Achievements of digital dithering

When the dither signal is digital, the starting situation differs from the continuous case discussed in section 3.3.1.3. The expected total error (ϵ) may be unequal to zero. Because the dither signal can only have a finite number of values, so can the expected value of y.

Figure 3.20 illustrates how an input signal is converted to an expected output value of the dithered quantizer. The granularity of the digital dither is very low in this figure for clear illustration. The black dots represent arbitrary input values, the horizontal bars connected to the dot represent the possible values for w, given x. In this figure the range of the dither is 1 LSB, but due to the low number of discrete values, the maximum value is clearly less than $\frac{1}{2}$ LSB. The cause of this difference is shown in Figure 3.18: the outer most dither values are $\frac{\Delta}{2M}$ spaced from the corresponding continuous PDF range. A very important point is that the dither range is exactly 1 LSB. If this is not exactly the case, distortion is introduced.

When digital dither is applied there is a range for the input signal which produces the same value of $E(y)$. In Figure 3.20 this is indicated by the gray areas. The possible values of $E(y)$ is the combination of the possible dither values and the quantizer decision levels.

The fact that the input signal may vary, without a change of $E(y)$ can be translated to a totally different quantizer with the same number of output values as possible values of $E(y)$. For this totally different quantizer, the input signal may also vary in the same range, without a change of output signal.

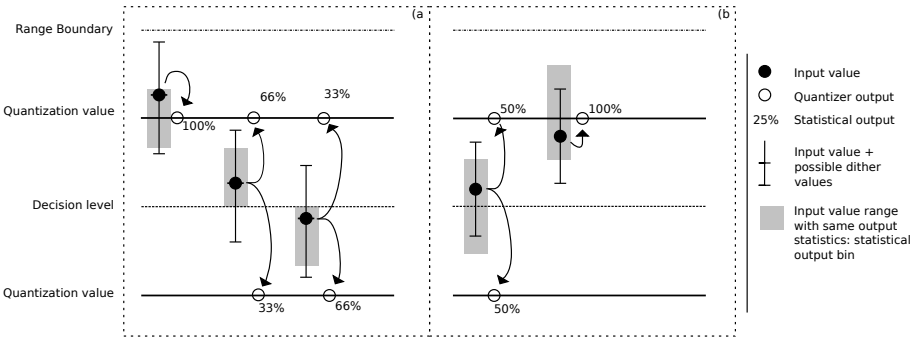

Figure 3.20: Effect of: a) 3 valued dither signals. b) 2 valued dither signals.

To continue this reasoning, this totally different quantizer is referred to as *equivalent quantizer*. The relations for an equivalent quantizer and the dithered quantizer depend on the type of dither used. In following section the equivalent quantizer is described for rectangular PDF dither.

3.3.2.2 Rectangular PDF dither equivalent quantizer

The digitally dithered quantizer can be represented by an undithered quantizer with a number of possible output values equal to the number of possible values for $E(y)$. This equivalent quantizer yields the same non-linearity, but the noise floor of the dithered quantizer is higher due to the dither. The equivalent quantizer concept is used to analyze the effects of non-linearity in a dithered quantizer.

$$SFDR_{eq} \approx SFDR_{dithered\ 2-bit}$$
$$SNR_{eq} > SNR_{dithered\ 2-bit}$$

Figure 3.21 illustrates the resemblance of the dithered quantizer and the equivalent quantizer. The output of this *equivalent quantizer* is denoted as y_{eq} and the operation of the equivalent quantizer is denoted as $Q_{eq}(x)$. Supposing that the input signal to both quantizers is a static value, the relations of expected values between the equivalent quantizer and the dithered quantizer are:

$$E(y) = E(Q(x + v_{digital})) \tag{3.36}$$
$$\approx E(Q_{eq}(x)) \tag{3.37}$$
$$\approx E(y_{eq}) \tag{3.38}$$

and thus:

$$E(Y) \approx E(Y_{eq}) \tag{3.39}$$

This holds under the constraint that $x + v$ fall inside the quantizer input range.

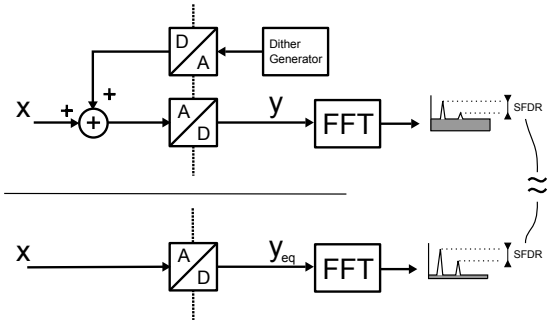

Figure 3.21: Equivalent quantizer resulting in equal distortion component magnitude

Rectangular PDF dither When the dither signal can assume M values, v_d is the PDF of the dither signal:

$$v_d(x) = \sum_{c=0}^{M-1} \frac{1}{M} \delta \left(x - (\frac{-\Delta}{2} + \frac{\Delta}{2 \cdot M} + \frac{c \cdot \Delta}{M}) \right) \tag{3.40}$$

and d_{D-bit} is the set of decision levels for a D-bit quantizer:

$$d_{D-bit}(x) = \sum_{d=0}^{2^D-1} \left(\frac{1}{2^D - 1} \delta \left(x - \frac{2^D - 1}{2} \cdot \Delta + d \cdot \Delta \right) \right) \tag{3.41}$$

The set of possible values for $E(y)$ is separated by a set of equivalent quantizer decision levels which are defined as the convolution of v_d and d_{2-bit}:

$$d_{E(y)} = v_d * d_{2-bit} \tag{3.42}$$

So while y can only assume 2^D values, the number of expected values of y is increased by the digital dither. This effect is illustrated in Figure 3.22. For this type of dither, the maximum input signal range is equal to the range of the convolution result. As will become clear, for other dither signals, the convolution result will contain values which are out of the allowed input signal range and therefore not used. For a D-bit quantizer and a rectangular PDF dither signal with M discrete values, the number of quantizer decision levels are:

$$(2^D - 1) \cdot M \tag{3.43}$$

and the number of possible values of $E(y)$ is:

$$(2^D - 1) \cdot M + 1 \tag{3.44}$$

The use of the concept of the equivalent quantizer is illustrated by simulation for rectangular PDF dither. A spectrum plot of a dithered quantizer and its equivalent undithered quantizer is shown in Figure B.3.

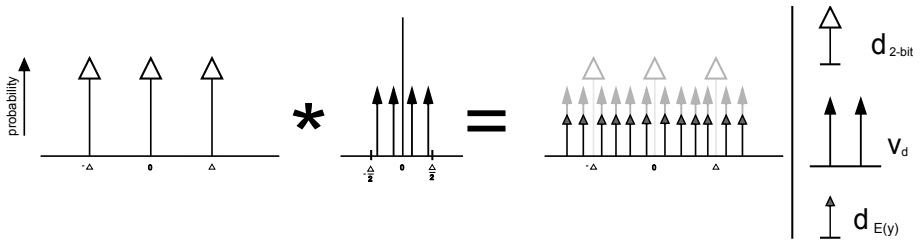

Figure 3.22: Convolution of rectangular dither PDF and quantizer decision levels result in decision level distribution.

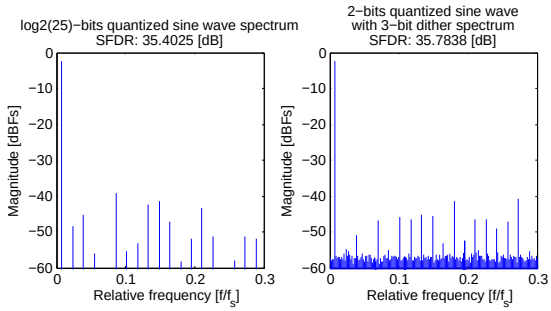

Figure 3.23: Spectra of a log(25)-bits equivalent quantizer and the 3-bit rectangular dithered 2-bit quantizer: they have approximately the same SFDR. (MATLAB code in appendix C.3)

Triangular PDF dither. For triangular dither a similar relations exist. These are worked out to certain extend and are listed in appendix B.4, but due to time limitations correctness cannot be guaranteed. Simulation show that the equivalent quantizer SFDR approximates the SFDR of the dithered quantizer.

Theoretical SFDR The theoretically achievable SFDR of a rectangular dithered quantizer can be expressed by modifying 3.2. The resolution of the equivalent quantizer is the $\log_2$ of the number of quantization values (Equation 3.44):

$$(2^D - 1) \cdot M + 1$$

The SFDR of a dithered D-bit quantizer, with M different dither values has a maximum value of:

$$SFDR \approx 8.07 \cdot log_2((2^D - 1) \cdot M + 1)) + 3.29 \tag{3.45}$$

3.3.3 Non-linearity

Until now the non-linear behavior of a (dithered) quantizer is discussed when all components are assumed ideal. In practice other non-linearities will also be present. The dithered quantizer consists of a dither DAC and a quantizer.

The effect of non-linearity for both sub-systems are discussed in this section. Because of the variable decision levels of the targeted ADC concept, the non-linearity of the quantizer is discussed in more detail. The non-linearity effects are analyzed by looking using the equivalent quantizer concept. The analysis is done for rectangular dither, because of time constraints. The relations identified in next sections are not directly applicible to triangular dither.

Errors of the output values of the dither DAC and errors of the decision values of the 2-bit quantizer can be translated to multiple errors in the decision values of the equivalent quantizer. When rectangular PDF dither is used, in the ideal case, each equivalent quantizer decision level is determined by a single 2-bit quantizer decision level and a single dither DAC output value. Although in this section the low-resolution quantizer is assumed to be 2-bit quantizer, the line of reasoning is valid for quantizers with a other resolutions as well.

3.3.3.1 Dither DAC non-linearity

The dither DAC error results in errors for multiple decision levels of the equivalent quantizer. Equation 3.42 shows that the dither range affects the equivalent quantizer output for each 2-bit quantizer decision level. For example, when one possible dither DAC output value is higher than intended, the equivalent quantizer has 3 decision levels which are higher than expected.So the non-linearity of the dither DAC has a repetitive effect on the non-linearity of the dithered quantizer. Figure 3.24 illustrates this repetitiveness for a 2-bit quantizer and a 3-bit digital dither signal. It shows the Integral Non-Linearity (INL) of the equivalent quantizer (and thus also the possible expected output values of the dithered quantizer).

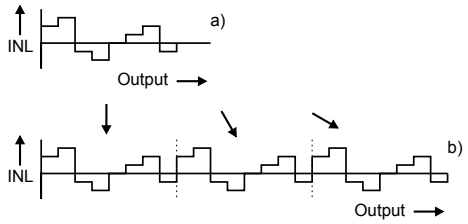

Figure 3.24: Repetitive INL due to INL of dither DAC and quantizer. a) INL of the dither DAC. b) INL of equivalent quantizer.

3.3.3.2 Quantizer non-linearity

When a 2-bit quantizer decision level deviates from its intended value, this results in multiple decision levels of the equivalent quantizer to deviate from their intended values. For the dithered quantizer this means that all expected values of the output depending on the deviating 2-bit quantizer decision level deviate by the same amount, this can be concluded from Equation 3.42.

Figure 3.25 illustrates the INL for a 2-bit quantizer and a 3-bit digital dither signal where the lower decision level has a higher value than intended.

Any change in the decision levels can always be translated to an increase of the lower decision level value and scaling of the signal for a 2-bit quantizer. Therefore only the case of an increase of lower decision level value is considered.

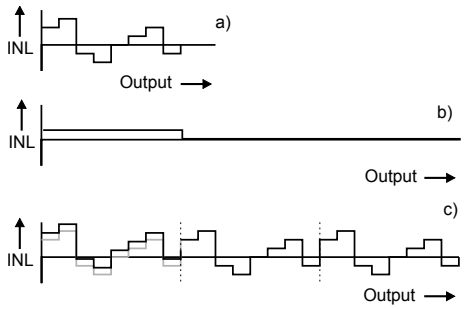

Figure 3.25: Repetitive INL due to INL of dither DAC. a) INL of the dither DAC. b) INL of the 2-bit quantizer. c) Statistical INL of the dithered quantizer.

The effects of this error are analyzed in next paragraphs by looking at the effects on the equivalent quantizer.

Equivalent quantizer with decision level error. An error in decision levels add distortion to the quantized signal. In order to calculate the added distortion caused by an error in the lower decision level, the concept of the equivalent quantizer is used. The function of the equivalent quantizer is denoted as $EQ()$. A decision level error of the 2-bit quantizer (Q) changes the ranges for which the input value has the same output value: the quantizer transfer function is changed. The change in the equivalent quantizer input signal ranges is illustrated in Figure 3.26. The gray areas represent ranges of the input signal which produce equal output values. In this figure the output values defined by the lower decision level of the 2-bit quantizer are shifted by the same amount as this decision level is changed. Thus when a sine wave is input to the equivalent quantizer (EQ), the output signal is distorted because of the changed quantizer function.

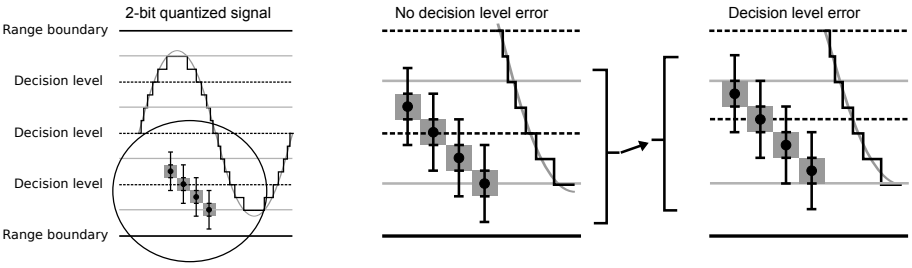

Figure 3.26: Decision level error effect on input signal ranges (gray areas), which lead to an output value

To analyze the effect of non-linearity, the ideal equivalent quantizer is compared to the equivalent quantizer with an error (caused by the error in the 2-bit quantizer decision level). To distinguish between the ideal equivalent quantizer and the one with the error, the following transfer functions are defined:

- EQ: the ideal quantization function of the equivalent quantizer.
- EQ_e: the equivalent quantizer adjusted for the decision level error.

SFDR degradation In this paragraph an expression is presented, by which the SFDR can be found of the 2-bit dithered quantizer with an error in a decision level.

The SFDR of EQ_e can be calculated by applying a sine wave to the input and Fourier transforming the output signal. A nice description of the output signal depending on the decision level error is not easy to find. A description for frequency components of a sine wave quantized by EQ is available in literature [18]. To find a nice expression for the SFDR of the equivalent quantizer, the equivalent quantizer non-linearity error signal is defined:

- $e_{EQ}(x) = EQ(x) - EQ_e(x)$: The equivalent quantizer error due to decision level error.

The error signal value as a function of an input sine wave is given in Equation 3.46. The derivation is given in Appendix B.3.1. This expression allows to calculate the added distortion due to a decision level eror.

$$e_{EQ}(\sin(2\pi \cdot t)) = \begin{cases} 1 & \text{if } [b(c,M)] > \sin(2\pi \cdot t) > [b(c,M) + (1-\alpha)\Delta], \\ & \quad \forall c \in \{\frac{M}{2}, \frac{M}{2}+1, ...(\frac{3 \cdot M}{2}-1)\} \\ 0, & \text{otherwise} \end{cases} \tag{3.46}$$

In this expression $b(c, M)$ is decision level c and $(1-\alpha)\Delta$ is the shift of this decision level due to the error in the 2-bit quantizer decision level.

$$b(c,M) = -\left[\frac{\Delta \cdot c}{2^M} \cdot \frac{4\Delta}{A_\Delta}\right] \tag{3.47}$$

Where 2^M is the number of dither values, α is the decision level error in LSB and A_Δ is the amplitude of the input sine wave in LSBs. For rectangular dither this is $\frac{3}{2}$. Figure 3.27 shows how $e_{EQ}(\sin(2\pi \cdot t))$ relates to $\sin(2\pi \cdot t)$.

The frequency components of the sine wave quantized by EQ are expressed by Blachman's approach [19] and the frequency components of the error e_{EQ} presented. When this is summed, the total spectrum is obtained and the SFDR is calculated.

The magnitude of frequency components of $EQ(sin(2\pi \cdot t))$ [18]:

$$EQ(p) = \Delta\left(A_\Delta \cdot \delta(p-1) + 2 \cdot \sum_{n=1}^{\infty} \frac{(-1)^n}{\pi n} J_p(2\pi \cdot n \cdot A_\Delta)\right) \tag{3.48}$$

For p is positive and odd. The magnitude of frequency components of $e_{EQ}(sin(2\pi \cdot t))$ are calculated by applying the Fourier transform to $e_{EQ}(sin(2\pi \cdot t))$:

$$F(e_{EQ}(sin(2\pi \cdot t)))(p) = \begin{array}{l} \sum_{c=1}^{M}\left[\int_{\pi+B(c,M)}^{\pi+A(c,M)} \Delta \cdot e^{-i \cdot p \cdot t} dt\right] + \\ \sum_{c=1}^{M}\left[\int_{2\pi-A(c,M)}^{2\pi-B(c,M)} \Delta \cdot e^{-i \cdot p \cdot t} dt\right] \end{array} \tag{3.49}$$

Where the integration borders are $b(c, M)$ scaled by the sine wave amplitude and input to the *arcsin* function:

$$A(c,M) = sin^{-1}(b(c,M)) \tag{3.50}$$

$$B(c,M) = sin^{-1}(b(c,M) + (1-\alpha)\Delta) \tag{3.51}$$

This approach is only valid when α is smaller than an equivalent quantizer LSB, i.e. when the equivalent quantizer is monotonic.

The method of finding SFDR degradation is verified by calculating the frequency components of the error signal and constructing a time-domain signal. The result is shown in Figure 3.27.

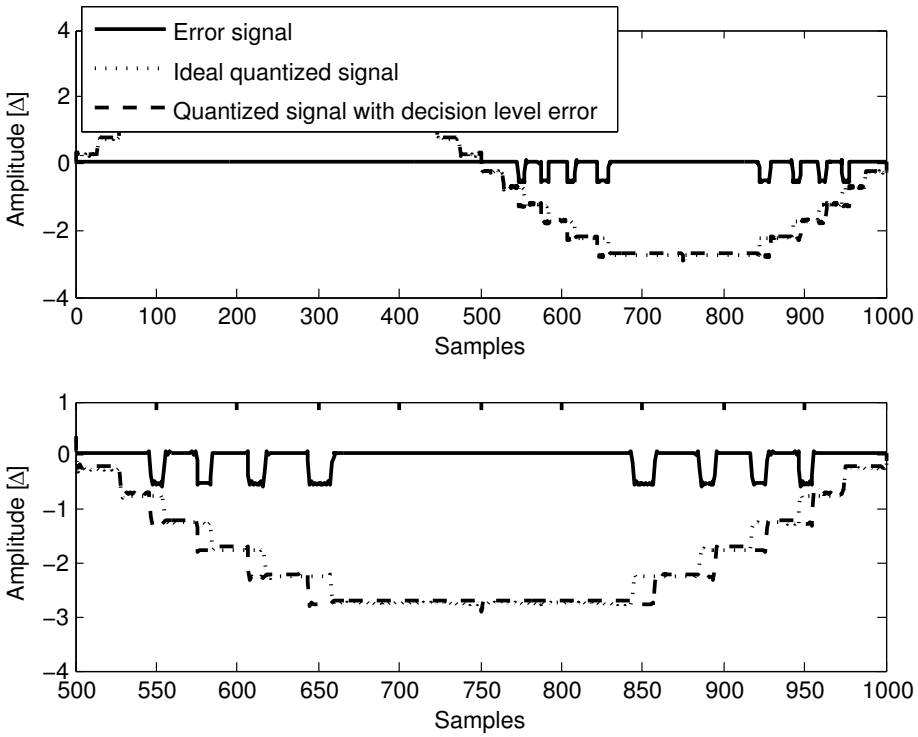

Figure 3.27: Time domain representation of decision level variation. Obtained by calculating the frequency components of e_{EQ_e}, when $D = 2$ and $\alpha = 0.8$. MATLAB code in Appendix C.4

With the equations presented above, the SFDR depending on the 2-bit quantizer decision level error (α) can be calculated. This is done in MATLAB and the SFDR are shown in Figure 3.28. The figure shows three signals:

1. The theoretical upper limit of the SFDR for the dithered quantizers (Equation 3.45). The SFDR values obtained are 0.5 to 1.1 dB below the theoretical performance (which is in accordance with [17]).

2. The frequency domain approach result, as described in this section.

3. Time domain simulation results. The lower decision level of an ideal 2-bit quantizer is adjuste by α. A rectangular PDF dithered sine wave is then quantized.

The figure shows the SFDR as a function of α for $D = 4, 5, 6$, the x-axis range is one LSB for each plot. It can be seen that the frequency domain approach simulation result follows the same trend as the time-domain simulation, although the first one is a bit optimistic. The value of α at which the SFDR

starts decreasing is roughly equal. The error of α becomes noticeable when the error is bigger than $\frac{1}{3}$ an LSB of the equivalent quantizer.

From these results a certain allowed decision level deviation is found. For instance, when the targeted SFDR is 60 dB for instance, a dither resolution of 6 bits is required and that the the decision level error error may not exceed half a dither signal LSB.

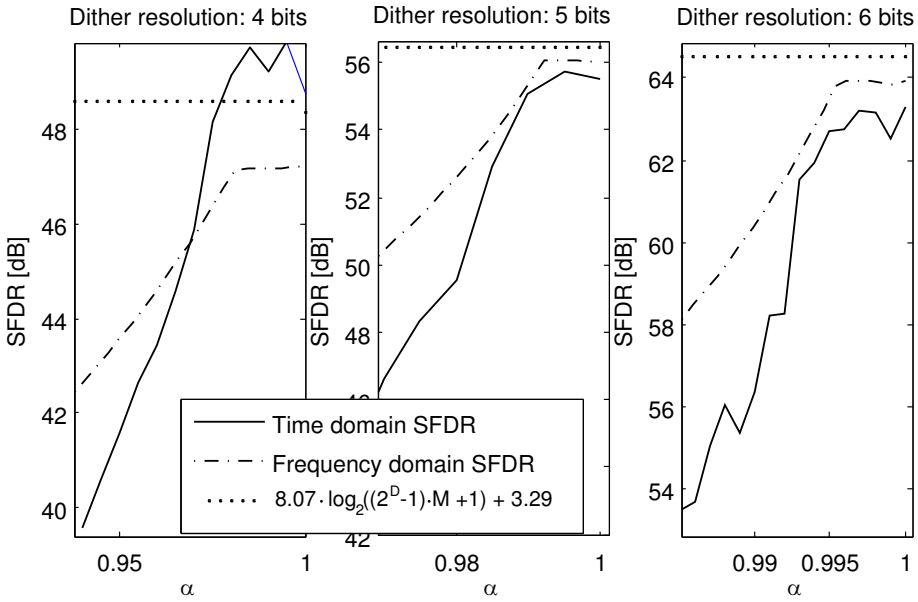

Figure 3.28: SFDR as a function of α. The x-axis range is 1 LSB.

3.3.4 Random number generators

A dither signal is a signal with random values. True random values are non-deterministic, which is difficult to generate by a digital system because operations of a digital system tend to be deterministic. A pseudo-random number generator can be used for dithering purposes. The output of this generator is deterministic, but its statistical properties can be sufficient to be used as a random number generator. The output will cycle through all its possible values in a pseudo-random order.

Many pseudo random generators consists of a Linear Feedback Shift Register (LFSR). A LFSR generates linear recursive sequences: they cycle through $2^n - 1$ output values, where n is the number of registers used for the LFSR. The two most well known types of LFSR are the Fibonacci and Galois generator [27], both types are shown in Figure 3.29. In this figure the states of the switches are denoted by g_m.

The Galois generator can operate faster, because it has less logic gates in the feedback loop. The generators will output all possible values if the values for g_m are chosen properly [28].

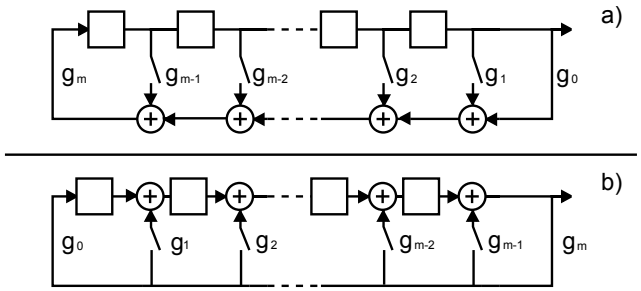

Figure 3.29: Linear shift feedback registers. a) the Fibonacci generator. b) the Galois generator

3.4 Summary and conclusions

Summary Analog to digital conversion involves sampling and quantization. Quantization is a non-linear operation and introduces distortion. The magnitude of the distortion components in the spectrum depend on quantizer resolution. Adding dither to the input signal of a quantizer reduces the distortion components.

Non-subtractive dithering increases the noise floor in the measured spectrum, but does not consume bandwidth as with band-limited dither or increase digital complexity as with subtractive dither. A mathematical approach is introduced which allows the derivation of the expected performance of a 2-bit dithered quantizer. For dithering with a signal with a rectangular or triangular PDF, the total error of the dithered quantizer has a white spectrum which allows highest SFDR. The concept of the equivalent quantizer is introduced, which gives insight in the achievable performance of a dithered quantizer. Also the the effects of non-linearity of the quantizer can be investigated using the equivalent quantizer concept.

Non-linearity introduced by error in the quantizer decision levels leads to degradation in SFDR. An approach to find the SFDR based on the equivalent quantizer concept, for a decision level error, is presented. A maximum allowed deviation of the decision level for a certain SFDR is found. In this analysis, the effects of rectangular PDF dither are examined. Rectangular dither results in a varying noise floor and thus some noise uncertainty. However, the noise floor is lower than when triangular dither is applied and rectangular dither allows larger input signal swing. Generation of digital dither can be done by using a linear feedback shift register, which produces a pseudo-random digital signal.

Conclusions Different dithering schemes are discussed and one is most suitable for an energy detection spectrum analyzer: non-subtractive wide-band dithering with rectangular or triangular dither PDF. This dithering scheme allows low-resolution digital processing and does not consume measurement bandwidth, but it raises the noise floor.

Triangular dither results in a higher noise floor in the measured spectrum than rectangular dither. However, rectangular dither results in a dependency between signal and added noise power. When the mean and power of the input signal is controlled, the variation of noise floor power is limited to a small range.

Whether this noise uncertainty dominates the achievable system performance depends on the total system it is used in. The noise uncertainty introduced by rectangular dithering is assumed to be acceptable for this thesis. The equivalent quantizer concept is an effective tool to analyze the performance of a digitally dithered quantizer.

Chapter 4

System level design

Chapter 2 described the cross-correlation spectrum analyzer and how it increases the SFDR compared to traditional spectrum analyzers. Then Chapter 3 described sampling and quantization and zoomed in to a 2-bit quantizer and described dithering as a countermeasure for distortion.

The goal of this chapter is to introduce the revisited ADC concept, originating from ASTRON, and to investigate the suitability for the use in a cognitive radio energy detection spectrum analyzer. The performance dependency of the spectrum analyzer on ADC characteristics are investigated.

This chapter describes the system level design and simulation results of a digitally dithered 2-bit ADC with automatic gain control and offset canceling for the use in this cross-correlation spectrum analyzer. Uncorrelated dither is added in both signal paths and the dither and quantization noise floor is lowered by utilizing the cross-correlation spectrum analyzer. Thereby a higher SFDR is achieved than for a traditional spectrum analyzer with a dithered 2-bit ADC.

In the following sections, first system level choices and calculations are presented. Based on the expected performance of the ADC, a SFDR of 60 dB is expected to be achieved after cross-correlation, for a resolution bandwidth of 6 MHz . The ADC concept is introduced, then an abstract view on the loop is presented and an implementable block diagram is presented. Specifications and settings are derived for the ADC sub-blocks. The ADC concept is implemented in SIMULINK, the simulation results are shown and discussed. Also some expectation for a CDF-based AGC ADC with a higher resolution are discussed.

4.1 Cognitive radio standard

The ADC concept described in this chapter is designed for the use in a cognitive radio system. In this section relevant numbers from one cognitive radio standard are presented.

FCC, Ofcom and IEEE are working on standards for cognitive radio. The standards differ a little and therefore the IEEE 802.22 standard is used for system calculations. Depending on geographic location, the DTV band is divided into channels with three different widths [29].

1. DTV band: 54MHz – 862MHz

2. Channel width: $6, 7$ or 8 MHz.

3. Sensitivity limit: $-116dBm$ in a $6MHz$ wide channel

4. Back-off time: $2s$: When the used channel becomes occupied, the system has this time to switch to another channel.

Solutions proposed in literature, where the goal is to meet the sensitivity limit requirement of $-116dBm/6MHz$ often use knowledge on the signal, such as pilot tones or other cyclostationary properties [30]. The spectrum analyzer of this thesis is designed as being a part of a cognitive radio system where possibly also other spectrum sensing techniques are applied. In this case, the energy detection spectrum analyzer gives a first coarse estimation of the spectrum. Then a more advanced spectrum sensing mechanism determines if one of the potential channels are free.

4.2 Spectrum analyzer front-end

The cross-correlation spectrum analyzer consists of an analog front-end and a digital back-end, separated by the ADCs. In order to derive specifications and requirements of the ADC, the characteristics of the analog front-end must be defined. First two concepts for the analog front-end are discussed

4.2.1 Analog front-end concepts

In many analog front-ends, the signal picked up by the antenna is mixed down to the IF band. This is done because the bandwidth of the signal of interest lies beyond the bandwidth of the ADC and digital back-end, or because such the bandwidth leads to large power consumption.

In previous work [4], the cross-correlation spectrum analyzer consists of a quadrature mixer concept. The advantage of quadrature mixing is that negative frequencies can be distinguished from positive frequencies, because of the complex input signal representation.

The frequency range of the DTV band is relatively low: it starts at 54 MHz and stops at 862 MHz. When quadrature mixing is used, the sample frequency is reduced but at the cost of another mixer, anti alias filter and ADC.

Choosing for a zero-IF quadrature mixer concept instead of a mixer-less concept is justified when the power consumption reduction outweighs the cost of additional hardware, for equal performance. Because in previous work a zero-IF mixer concept is used and because a mixer-less concept might be a good solution, both cases are addressed in this section.

4.2.2 Expression of signal power

The input signal power received at the antenna is expressed in Watt. When the signal is amplified using automatic gain control, the ratio between analog input signal power and output signal power is variable. Therefore, the output signal power is expressed in a different unit than the input signal power. The input signal is often expressed relative to one milliwatt. The output signal will be expressed in decibels relative to a full scale (complex) sine wave (dBFs).

The output signal is referred to a complex sine wave or a non-complex sine wave, depending on the system discussed.

Power expressed relative to a full scale sine wave When a full scale real signal is expressed in dBFs, the amplitude is half full scale and its power is:

$$P = \frac{\left(\frac{FS}{2}\right)^2}{2} \tag{4.1}$$

$$= \frac{1}{8} \cdot FS^2 \tag{4.2}$$

where FS denotes full scale. The power of a full scale sine wave is then:

$$10 \cdot \log_{10} \frac{\frac{1}{8} \cdot FS^2}{\frac{1}{8} \cdot FS^2} = 0[dBFs] \tag{4.3}$$

Relative to a full scale complex sine wave When a full scale complex sine wave is converted to the digital domain, both its real and imaginary parts are converted by separate ADCs. The amplitude of the real and imaginary part are then half the input range of the ADC. The power of a full scale complex sinusoid is thus:

$$P_{\text{real}} + P_{\text{imaginary}} = \frac{\left(\frac{FS}{2}\right)^2}{2} + \frac{\left(\frac{FS}{2}\right)^2}{2} \tag{4.4}$$

$$= \frac{1}{4} \cdot FS^2 \tag{4.5}$$

The power in decibels of a full scale complex sine wave is then:

$$10 cdot \log_{10} \frac{\frac{1}{4} \cdot FS^2}{\frac{1}{4} \cdot FS^2} = 0[dBFs] \tag{4.6}$$

4.3 Theoretical system performance

This section presents the system calculations for the two front-ends in mind.

4.3.1 Choices and calculations

First the choices are presented on which the theoretical performance calculations are based.

Choices

1. Maximum frequency.
    - *In case of zero-IF mixer concept:* If the spectrum analyzer consist of a quadrature mixing zero-IF front-end (in accordance with previous work), then the DTV band is down-mixed to around $0HZ$, For instance with an oscillator frequency of $460MHz$. The maximum frequency is then approximately $405MHz$.

- *In case of mixer-less concept:* The maximum frequency is defined by the cognitive radio standard: $862MHz$

2. *Sample frequency and resolution bandwidth:* The channel bandwidths for DTV vary per country and the channels are not uniformly distributed over the DTV band. However, for the validation of the ADC concept, the resolution bandwidth is chosen to be 6 MHz.

   When the signal is down-mixed to around 0 Hz, the IF bandwidth ranges from $-\frac{862-54}{2}$ to $\frac{862-54}{2}$. The minimal sample frequency is:

   $$862 - 54 = 808MHz \tag{4.7}$$

   Because the anti-aliasing filter requires some bandwidth, the sample frequency is chosen higher. The sample frequency is chosen based on the resolution bandwidth of $6MHz$ and taking into account convenient FFT implementation (i.e. the number of channels is a power of two). The sample frequency for a zero-IF mixer concept is then:

   $$f_s = 1536MHz \tag{4.8}$$

   When the mixer-less concept is used, the frequency is doubled:

   $$f_s = 2 \cdot 1536 = 3072MHz \tag{4.9}$$

   The number of channels in one spectrum is then:

   $$\#_{channels} = 2^{\lceil log_2(\frac{862-54}{6})\rceil} = 256 \tag{4.10}$$

3. *Analog front-end gain* The zero-IF front-end used in previous work [4] consists of a passive splitter to divide the signal power over the two parallel front-ends. In [5] a variable attenuator is described as part of a cross-correlation spectrum analyzer. The front-end in mind, for which the CDF-based AGC ADC is worked out, consists of this variable attenuator. The attenuation is tunable in steps of 6 dB.

4. *ADC concept:* The analog to digital conversion is done by a dithered 2-bit CDF-based AGC ADC. This is the revisited ADC concept from ASTRON. It includes automatic gain control and offset canceling. The offset canceling suits the zero-if mixer concept, because this concept introduces offset when input signal frequency components are close to the mixer local oscillator frequency. The input signal is properly scaled by the automatic gain control. The ADC uses dithering to remove distortion components when strong narrow-band signals are input to the spectrum analyzer.

5. *Dither signal:* The dither added to both parallel input signals are statistically independent complex valued signals with a rectangular or triangular PDF. The noise floor is now raised by quantization noise and dither noise. Uncorrelated dither signals are added to both signal paths such that the quantization and dither noise floor is lowered by cross-correlation.

6. *SFDR determination:* The theoretical SFDR is based on a zero mean sine wave with amplitude $\frac{3}{4}$ (rectangular PDF dither) and $\frac{1}{2}$ (triangular PDF dither) of the input range of the quantizer, depending on the type of dither used. For the calculation no other noise than dither and quantization noise is present.

system calculations

1. *Noise and distortion (in case of no dither):* For a 2-bit ADC the power of the quantization noise power, when assumed white, is:

$$q(w)^2_{white} = \frac{\Delta^2}{12} \tag{4.11}$$

The resulting noise floor is then:

$$NoiseFloor_q = 10 \cdot \log_{10}(\frac{\Delta^2}{12}) - 10 \cdot log_{10}(\#_{channels}) \tag{4.12}$$

The worst case SFDR of a 2-bit quantizer is, according to equation 3.2:

$$\text{SFDR}_{wc} = 8.07 \cdot 2 + 3.29 = 19.43[dB] \tag{4.13}$$

2. *Noise and Distortion (in case of dither)* Rectangular dither and triangular dither power respectively:

$$v_r^2 = \frac{\Delta^2}{12} \tag{4.14}$$

$$v_t^2 = \frac{\Delta^2}{6} \tag{4.15}$$

When added to the input signal of the quantizer, the noise floor is dominated by the quantization noise power and dither power (total error power, see 3.2). For the rectangular PDF, dither this depends on the input signal. Although this is subject to recommended further research, the total error power is approximately $\frac{\Delta}{12} + \frac{\Delta}{12}$ when the input signal is properly scaled, thus:

$$NoiseFloor_{\epsilon_r} = 10 \cdot \log_{10}(\frac{\Delta^2}{12} + \frac{\Delta^2}{12}) - 10 \cdot \log_{10}(\#_{channels}) \tag{4.16}$$

$$NoiseFloor_{\epsilon_t} = 10 \cdot \log_{10}(\frac{\Delta^2}{12} + \frac{\Delta^2}{6}) - 10 \cdot \log_{10}(\#_{channels}) \tag{4.17}$$

3. *SFDR (in case of dither):* For rectangular PDF dither, the input sine wave is scaled by $\frac{3}{4}$ and for the triangular PDF dither it is scaled by $\frac{1}{2}$. When proper dithering is applied, the distortion components are reduced

to below the noise floor. The SFDR in both cases then is:

$$\text{SFDR}_r = 20 \cdot \log_{10}(\frac{3}{4}) - NoiseFloor_{\epsilon_r} \tag{4.18}$$

$$= 20 \cdot \log_{10}(\frac{3}{4}) - 10 \cdot \log_{10}(\frac{\Delta^2}{12} + \frac{\Delta^2}{12}) - 10 \cdot \log_{10}(\#_{channels}) \tag{4.19}$$

$$\text{SFDR}_t = 20 \cdot \log_{10}(\frac{1}{2}) - NoiseFloor_{\epsilon_t} \tag{4.20}$$

$$= 20 \cdot \log_{10}(\frac{1}{2}) - 10 \cdot \log_{10}(\frac{\Delta^2}{12} + \frac{\Delta^2}{6}) - 10 \cdot \log_{10}(\#_{channels}) \tag{4.21}$$

4. *Cross-correlation* Thus the increase in SFDR due to cross correlation is (equation 2.9):

$$I = 10 \cdot log_{10}(\sqrt{T_m \cdot RBW}) \tag{4.22}$$

$$\tag{4.23}$$

5. *SFDR (in case of dither and cross-correlation)* Which gives a theoretical achievable SFDR for rectangular PDF dither and triangular PDF dither of:

$$\text{SFDR}_r = 20 \cdot \log_{10}(\frac{3}{4}) - 10 \cdot \log_{10}(\frac{\Delta^2}{12} + \frac{\Delta^2}{12}) - 10 \cdot \log_{10}(\#_{channels}) + 10 \cdot log_{10}(\sqrt{T_m \cdot RBW}) \tag{4.24}$$

$$\tag{4.25}$$

$$\text{SFDR}_t = 20 \cdot \log_{10}(\frac{1}{2}) - 10 \cdot \log_{10}(\frac{\Delta^2}{12} + \frac{\Delta^2}{6}) - 10 \cdot \log_{10}(\#_{channels}) + 10 \cdot log_{10}(\sqrt{T_m \cdot RBW}) \tag{4.26}$$

Table 4.6 shows the achievable SFDR values based on the calculations presented above, for a measurement time of 0.2 seconds. In general: the smaller the Resolution Bandwidth (RBW), the higher the SFDR, but the measurement of a spectrum takes more time and thus the cross-correlation effect is smaller. Based on these numbers, the ADC concept is worked out for a resolution bandwidth of 6 MHz. A margin for the SFDR is used for the noise uncertainty due to limited measurement time: the targeted SFDR for the ADC concept is 60 dB when rectangular dither is used.

The utilization of the cross-correlation allows a significant increase in SFDR for a 2-bit ADC.

4.4 The ADC concept

The ADC concept originates from ASTRON [8], where it was implemented with discrete components. In this section the concept is revisited and designed for on-chip integration. The ADC is referred to as *CDF-based AGC ADC*.

RBW	Number of channels	SFDR, no XC [dB] (Rect,Triang)	SFDR, XC [dB] (Rect,Triang)	XC Gain [dB]
200 kHz	7680	47.1, 41.9	69.6, 64.3	23
6 MHz	256	32.4, 27.1	62.7, 57.4	30.4
7 MHz	220	31.7, 26.4	62.33, 57.0	30.7
8 MHz	192	31.1, 25.8	62.0, 56.8	31

Table 4.1: Achievable SFDRs for different resolution bandwidths

4.4.1 The use in radio astronomy

In radio astronomy knowledge on the input signal to the ADC is available, as opposed to cognitive radio. In radio astronomy the input signal is Gaussian distributed and white over the entire measured band. In cognitive radio the input signal can be Gaussian distributed with a bandwidth which is a fraction of the measured band. This is the reason that dithering is not required in these radio astronomy applications. The input signal provides the dithering effect itself: the quantization noise is white because the input signal is white. Not only is the quantization noise white, but also clipping distortion is white.

This difference in input signals is the reason why the ADC concept for cognitive radio yields different results than for radio astronomy. System settings derived in the *decision probability rules* section (Section 4.4.6) are different than system settings in [8], [7].

4.4.2 Introduction to the ADC concept

The CDF-based AGC ADC is a 2-bit ADC with automatic gain control and offset canceling. When a signal is digitized, the amplitude ratio between the analog and digital signal is determined by the ADC. To achieve variable gain there are two possibilities. The first is amplifying the input signal by a variable gain block prior to AD conversion. The second is adjusting the full-scale range of the ADC. The CDF-based AGC ADC is based on a flash ADC and has a variable full-scale range. The full-scale range is adjusted based on estimations of the CDF of the input signal. A CDF of a signal is a function ($CDF(x)$) that will give the probability that the signal is less than or equal to x. The CDF of a signal thus also provides information on its amplitude. When the CDF is estimated, this amplitude information is estimated and the full-scale range of the ADC is adjusted accordingly.

The expected input signal to a cognitive radio system is a strong narrow-band signal (e.g. FM signals), a combination of a few strong narrow-band signals (e.g. Multiple FM signals) or Gaussian distributed signals (e.g. OFDM signals). The CDF of sinusoidal or Gaussian distributed signals are known. For signals with known CDFs, the relation between decision level probability and amount of clipped distortion is known. Clipping distortion is present when input signal samples fall outside the ADC input range. Because instantaneous values of a Gaussian distributed signal can have any value theoretically, there is always some clipping distortion. The ADC must make sure that the amount of clipping distortion is small enough such that it does not degrade the targeted SFDR. Thus the decision levels of the ADC are set such that maximal SFDR

is achieved.

A signal consisting of multiple sinusoids can have many different CDFs because of phase differences between the sinusoids. The CDF then must be predicted or estimated, such that the amount of distortion is limited to acceptable levels. This issue will be elaborated in section 4.4.6.

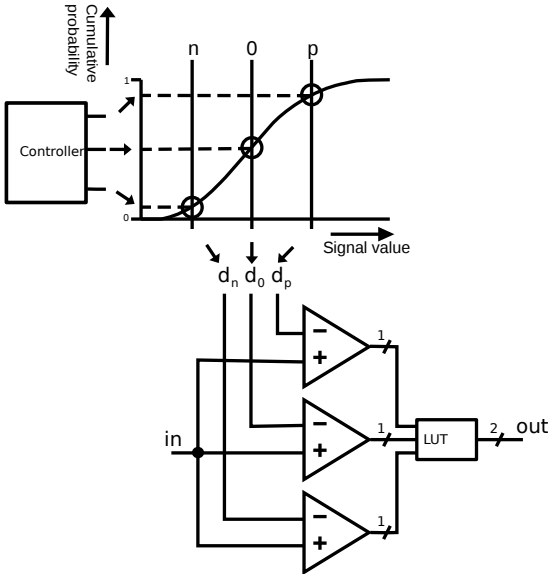

Figure 4.1: Flash ADC with decision levels set through the input signal CDF.

Figure 4.1 shows the concept of the ADC. Three comparators convert the analog signal to a digital signal, like a flash ADC. The reference level of each ADC is determined through the input signal CDF. The probabilities are determined by a digital subsystem, referred to as the system-controller. Each decision level corresponds to a certain probability that the input signal is higher than that decision level, as shown in Equation 4.27. This equation reveals a kind of loop, as d_{out} is proportional to a function of d_{in} and d_{out} determines d_{in}.

$$d_{out} \propto p_x(x > d_{in}) \tag{4.27}$$

Assumptions The ADC acts on estimations of the CDF of the input signal. A starting point of the energy detection spectrum analyzer for cognitive radio is that it has no information on the input signal. However to say something about the expected behavior of any ADC, some assumptions have to be made. For the system level design of the CDF based AGC ADC, the following assumptions are made:

1. The PDF of the input signal is symmetric around the mean of the signal. This is a necessary condition to have uniform quantization.

2. The input signal statistics are constant during the measurement of one spectrum. When this is not the case, the estimated spectrum is ambiguous because signals with different statistics are averaged.

During system design it turned out that the first assumption is not valid for certain signals. This problem is addressed in section 4.4.8.

Automatic gain control and offset canceling The desired decision level *probabilities* are predefined by the system. The decision level *values* then result via the CDF of the input signal. The three decision levels are denoted as $[d_n, d_0, d_p]$. When the input signal has less pwoer, the range of its CDF is smaller and the decision levels are changed accordingly. Also when an offset is added to the signal, its CDF changes and so do the decision levels. This is illustrated in Figure 4.2.

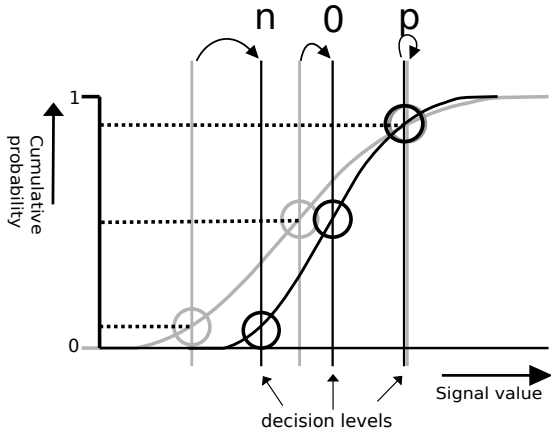

Figure 4.2: Reference levels are adapted to CDF changes: a positive offset is introduced and the amplitude is decreased.

From CDF estimate to decision level loop For three decision levels, three points in the CDF are estimated. Each probability can be estimated by counting the number of input values that are higher than the corresponding decision levels in a certain interval. Another representation of the probabilities is obtained when this counter signal is low pass filtered.

The result of the low pass filtered counter signal is compared to a reference set by the controller. The decision level is then adapted accordingly. When the results of the quantization are then fed-back to the decision level a *decision level loop* is created.

4.4.3 Power estimation

To give any meaning to the resulting spectrum, a power reference is needed. The value of an LSB is equal to the distance between two adjacent decision levels, so each ADC defines an LSB in twofold. In the proposed implementation in the following sections the value of an LSB is available in the digital domain. Figure 4.3 illustrates the two LSBs known to the system. The two definitions of an LSB are expected to be equal and their average is used as the power reference. The spectrum analyzer consists of multiple ADCs (two for direct-conversion and four for quadrature-conversion), so there are multiple power references available, which can again be averaged.

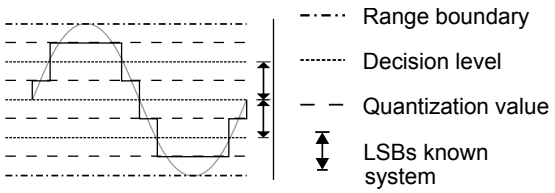

Figure 4.3: Quantizer LSBs known to system

4.4.4 Decision level loop

As became clear from Equation 4.27, each decision level is determined by a feedback loop. A single ADC consists of three decision levels and thus three decision level loops. Each loop sets that decision level independently. The input signal and the desired decision level probability are inputs to this loop. In the following sections, first an abstract view is presented on the decision level loop and then an implementable block diagram of the loop is presented.

4.4.4.1 Abstract view

When looking at the decision level loop by looking at Equation 4.27 and Figure 4.2, only two signal expressions are of interest: *decision level values*(d) and emphthe probability of a signal being less then or equal to d ($p_x(x > d)$) . Those units are related to the CDF of the input signal, so in the abstract view only those units are considered. Figure 4.4 shows the abstract decision level loop.

A decision level loop has three tasks:

1. Compare the input to the decision level.
2. Estimate the probability that the input signal is higher than the decision level: estimate $p_x(x > d)$.
3. Adapt the decision level value.

The comparison results in an estimation of the probability that the input signal is larger than the decision level. This probability is denoted as p_d. p_{ref} is the reference probability (which is the desired probability for p_d) and is set by the system controller. The difference between these two probabilities is the error probability Δp, and must converge to zero. To let the error converge to zero, Δp is integrated before it is converted to a decision level. The integration also filters out the high frequencies of Δp, which bears relevance when the implementation is concerned.

4.4.4.2 Decision level loop blocks

The abstract blocks of Figure 4.4 are filled in with realistic functions, such that an implementable version of the decision level loop emerges. This decision level loop is shown in Figure 4.5. The following choices are made:

1. The signal ($w(t)$) entering a decision level loop is a voltage, so the decision level ($d(t)$) is also a voltage.

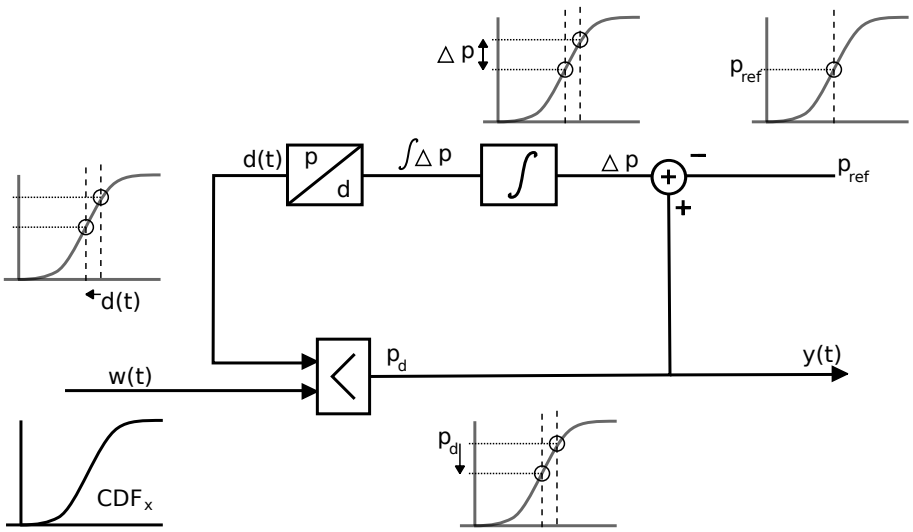

Figure 4.4: Abstract representation of CDF-based decision level loop. (The compare function is in this abstract representation not a comparator.) The input signal is compared to $d(t)$, which results in a probability p_d, this probability differs from the reference probability p_{ref}. The difference is integrated ($\int \Delta p$) and converted to a decision level ($d(t)$). Because the difference is integrated, p_d converges to p_{ref}, as is indicated by the small CDF plots.

2. The comparison block is a clocked comparator, the clock frequency equals the sample frequency of the total ADC. The output of this comparator ($p_d(t)$) is combined with other comparator outputs and results in the digital output signal of the total ADC.

3. The output of the comparator ($p_d(t)$) is low-pass filtered which results in a higher-resolution digital signal ($\overline{p_d}(t)$).

4. The difference between ($\overline{p_d}(t)$) and the reference probability (p_{ref}) is the probability error (Δp) and is obtained by subtracting those digital signals. The result is integrated by a digital integrator. The digital integrator is followed by a gain block to control the dynamics of the loop.

5. The decision level is converted from the digital domain to the analog domain by a DAC.

Figure 4.5 shows the implementable decision level loop block diagram.

The resolution of $\overline{(}p_d(t))$, p_{ref} and Δp and the DAC are derived when the total ADC is addressed (Section 4.4.5).

4.4.4.3 Frequency behavior

The low-pass filter and integrator limit the bandwidth of the decision level. Because the filter and integrator are part of the feedback, the loop itself is a high-pass filter. Figure 4.6 shows the effect of the decision level loop in the frequency domain: the low-frequency components of the input signal are filtered out and the reference probability signal is added.

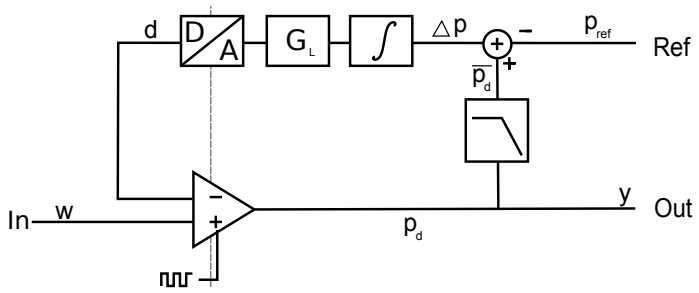

Figure 4.5: Decision level loop with realistic function blocks.

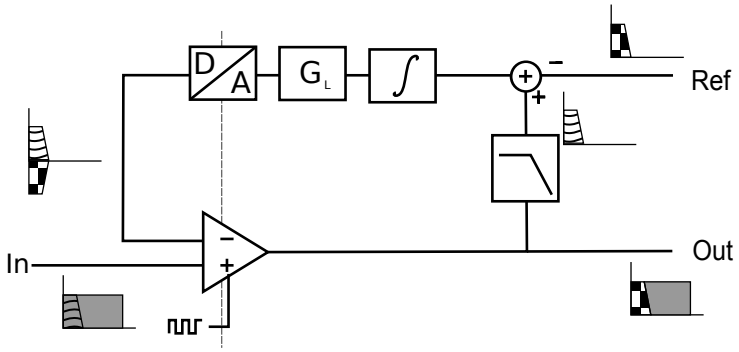

Figure 4.6: Decision level loop effect in frequency domain. The low-frequency content of the input signal is filtered out and the reference signal is added. The reference signal sets the decision level. The small spectra illustrate how frequency content is subtracted and added.

Bandwidth settling time trade-off The low pass filter and integrator enable the offset canceling of the input signal and comparator, because all offsets can be translated to low-frequency components in the input signal. The consequence is that the resulting spectrum is not estimated for frequencies around zero Hertz. When this waste of bandwidth has to be reduced, the filter cut-off frequency must be lowered. As a result the time for the loop to settle will increase. Thus a trade-off exists between loop settling time and waste of bandwidth.

4.4.4.4 Decision level loop transfer function

In order to determine the loop characteristics, the transfer function is linearized. A transfer function from w to d is presented, such that the frequency components in d can be defined. To linearize the loop, the comparator is replaced by a summing point and gain G_c, the integrator has no upper limit and the DAC resolution is assumed to be infinite.

Figure 4.7 shows the linearized decision level loop. In this figure the addition of noise by the comparator is denoted by q_c. For the determination of the transfer characteristics the noise is neglected.

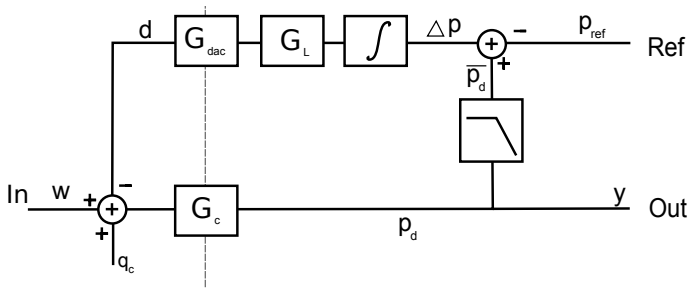

Figure 4.7: Linearized decision level loop

The loop consists of the following functions:

$$d = G_l \cdot G_{dac} \cdot \int \Delta p \tag{4.28}$$

$$\Delta p = \overline{p_d} - p_{ref} \tag{4.29}$$

$$\overline{p_d} = H_{lpf}(p_d) \tag{4.30}$$

$$p_d = G_c \cdot (w - d) \tag{4.31}$$

The transfer function of w to d is:

$$\frac{d}{w}(s) = \frac{G_{dac}G_lG_c \cdot H_{lpf}}{s + G_{dac}G_lG_c \cdot H_{lpf}} \tag{4.32}$$

$$\tag{4.33}$$

The frequency behavior of the loop can now be defined by choosing H_{lpf} and G_l.

The transfer function of w to y has a high-pass characteristic:

$$\frac{y}{w} = \frac{s \cdot G_c}{s + G_{dac}G_l \cdot H_{lpf}} \tag{4.34}$$

$$\tag{4.35}$$

Loop settings The loop filter is determined by defining the filter order, stop-band and stop band attenuation and phase margin. The stop-band depends on the mixer concept used. For the mixer-less concept, frequencies higher than 54 MHz must be attenuated properly. For a zero-IF mixer concept the channel mixed to around 0 Hz cannot be measured by the spectrum analyzer. To have minimal waste of sensed spectrum, the oscillator frequency is located in the middle of this channel. The filter stop band starts at half the channel bandwidth ($\frac{RBW}{2} = 3MHz$).

Because the theoretically achievable SFDR is 62.7 dBFs, The maximum gain of the loop in the stop-band is $-62.7dB$. The phase margin is set to 60 degrees to have just a little overshoot and acceptable settling time. For the design a settling time of maximal 1% of the measurement is considered to be sufficient. For a measurement time of 0.2 seconds, the maximal settling time is 1 ms. This allows a first order filter and instability issues are not introduced by the linear behavior of the loop.

The first order loop filter is of the form:

$$H_{lpf} = \frac{1}{s\tau + 1} \tag{4.36}$$

The transfer function of w to d becomes:

$$\frac{\Delta d}{\Delta w} = \frac{G_{dac}G_lG_c}{s^2\tau + s + G_{dac}G_lG_c} \tag{4.37}$$

Values for $G_{dac}G_lG_c$ and τ such that the requirement are satisfied are:

- $G_{dac}G_lG_c = 3 \cdot 10^5$
- $\tau = \frac{1}{6 \cdot 10^5}$

For the implementation the filter is converted to a digital filter by the bilinear transformation, resulting in a second order digital filter of the form:

$$H(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{a_0 + a_1 \cdot z^{(} - 1) + a_2 \cdot z^{-2}} \tag{4.38}$$

where

$$[a_0, a1] = [1.000, -1.9996, 0.9996] \tag{4.39}$$

$$[b_0, b_1] = [0.1907, 0.3814, 0.1907] \cdot 10^{-}7 \tag{4.40}$$

4.4.4.5 Non-linear effects

The linearization in the previous section excludes some important behavior of the loop which is now addressed:

- The comparator was linearized as a summing point and gain. However, the comparator introduces variable gain. The gain depends on the voltage difference at the input. As a result, large variations in the input signal CDF have longer settling times than according to the linear model and the loop has become potentially unstable. The longer settling times become visible in simulation, but in those simulations the loop does not become unstable. To avoid large overshoots due to this non-linearity, a margin must be used for setting the gain. Because the attenuator in the analog front-end can be set by steps of 6 dB, the margin of the gain must be at least a factor 2.

- The digital integrator can saturate. The effects are the same as for the comparator. When the integrator saturates, the settling time will become even larger than when only the comparator saturates.

Analysis of the non-linear behavior of the loop is required to be able to assure that the loop does not become unstable. This analysis is not done for this thesis and is listed as a recommendation in section 6.

4.4.5 Total ADC

When multiple decision level loops are placed in parallel and each loop has different reference probabilities, a multi-bit ADC is created. This section deals with a 2-bits ADC mainly, based on the observations, expectations and conclusions are drawn about the possibility of ADCs with higher resolutions.

A single 2-bit ADC consists of three decision level loops. Figure 4.8 shows the block-diagram of a total ADC. Each loop has its own reference probability, denoted as $p_{ref}[p, 0, n]$ for the high, middle and low decision levels respectively.

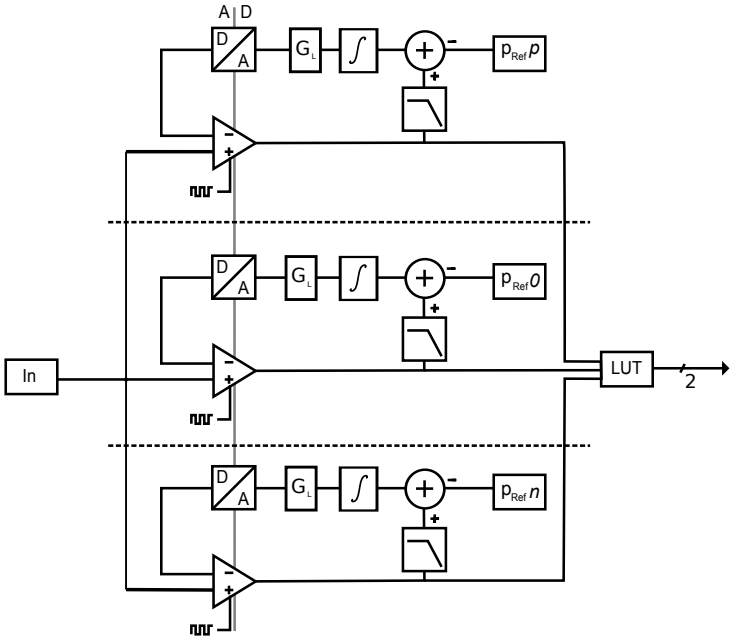

Figure 4.8: Total ADC consisting of three decision level loops

The output of the three loops must be converted to the desired representation, for instance 2's complement. This can be done by a small Look-up Table (LUT).

When dither is added to the ADC, the block diagram is changed. The dither can be added in multiple ways, as is elaborated in next section.

4.4.5.1 Implementation choices

When the decision level loops are implemented, the dither and decision level resolution must be defined. For the total ADC the way dither is added to the input signal must be defined.

Dither resolution As described in Section 3.3.3, the required dither resolution depends on the required SFDR and quantizer resolution. When an SFDR of at least 60 dB is required, the dither should be 6 bits (see section 3.3.3). For ideal decision levels and a rectangular PDF dither signal, the theoretical

SFDR is:

$$SFDR_r = 8.07 \cdot (2 + 6 + \log_2(\frac{3}{4})) + 3.29 = 64.5[dB] \tag{4.41}$$

and for a triangular PDF dither signal:

$$SFDR_t = 8.07 \cdot (2 + 6 + \log_2(\frac{2}{4})) + 3.29 = 59.8[dB] \tag{4.42}$$

For these expressions it is assumed that the noise does not limit the SFDR.

The sample frequency of the dither DAC must be equal to the sample frequency of the comparator. If the sample frequency is lower, there is a correlation between time-separated dither values. The dither signal statistics do not fulfill the requirements as described in section 3.3.1. The spectrum of the analog dither signal is then not white anymore and neither is the spectrum of the quantization error: distortion is present.

Decision level DAC According to the results of Section 3.3.3 the decision level may have a maximal error of $\frac{1}{3}$ dither LSB for rectangular dither, otherwise a SFDR of 60 dB cannot be guaranteed. For triangular dither it is assumed that the same holds (this is subject to recommended future research). Thus the precision of the decision level must be better than $\frac{1}{3}$ of a dither LSB. The resolution of the dither DAC is 6 bits, and the quantizer consists of 2^2 quantization values, thus the decision level DAC resultion must be $6 + 2 = 8$ bits.

The output bandwidth of the decision level DAC must accommodate the loop bandwidth and is 3 MHz for a front-end with a zero-IF mixer concept and 54 MHz for a mixer-less concept.

Dither DAC implementation Dither is added to the input signal of the ADC. The digital dither signal must have the same bandwidth as the total measurement. Because of the variable decision levels, the value of an LSB is variable and the dither must be scaled accordingly. Thus the dither must be scaled before it is added to the signal. There are two options:

1. The dither signal (v) is added to the digital decision level signal (d) before the decision level DACs. The dither signal is then converted to the analog domain for each decision level. Figure 4.9 shows the block diagram of this solution. The dither signal is thus added to the feedback signal for each comparator. When the dither is added in the digital domain before the decision level DAC, the decision level DAC requirements are increased. The bandwidth of the decision level signal is significantly lower than the bandwidth of the dither signal. So when the dither signal is added to the decision level prior to DA conversion, the DA converted signal bandwidth is equal to the dither bandwidth. Also the resolution of the DAC is increased, because the dither value is scaled to the decision level spacing. The required resolution of the DAC then depends on the lowest expected value of an LSB. Because of the increased requirements,. the power consumption and silicon area of this DAC are increased. Because the dither is added to all three decision level loops in the ADC, the power consumption and silicon area is increased in threefold.

2. A single dedicated dither DAC is added to the ADC. The dither signal is then added to the input signal before it enters the ADC. Figure 4.10 shows the block diagram of this solution. In this case a fourth DAC is added to the ADC, but only this fourth DAC must have the high bandwidth requirements for the dither signal.

The best option is the second, because it costs only one extra DAC with bandwidth requirements. The first option introduces three DACs with higher bandwidth and resolution requirements.

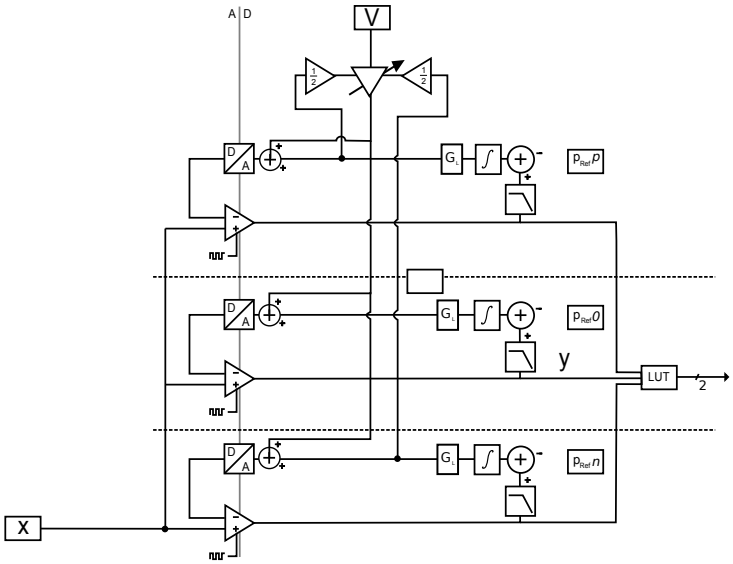

Figure 4.9: Total ADC with scaled dither added in the digital domain.

Another advantage of the second option is that dither scaling can be done in the analog domain. The proposed solution is connecting the reference of the dither DAC to the difference of the upper and lower decision level. This is illustrated in Figure 4.11.

Stability Adding and scaling of the dither solution might be identified as a potential stability problem. The dither amplitude is a function of the value of an LSB and the value of an LSB is influenced partially by the dither signal. When the value of an LSB increases, the dither signal amplitude increases and the value of an LSB increases again. However the dither solution is not unstable for rectangular and triangular dither. For rectangular PDF dither the maximum amplitude is a half LSB and for triangular dither the maximum amplitude is one LSB. The probability that the amplitude of the input signal exceeds an LSB by the dither only is 0. So the gain of this loop is smaller than 1: the loop is stable.

4.4.6 Decision probability rules

The decision probabilities are set by the system controller. For different type of signals, different rules must be applied for optimal performance. When an

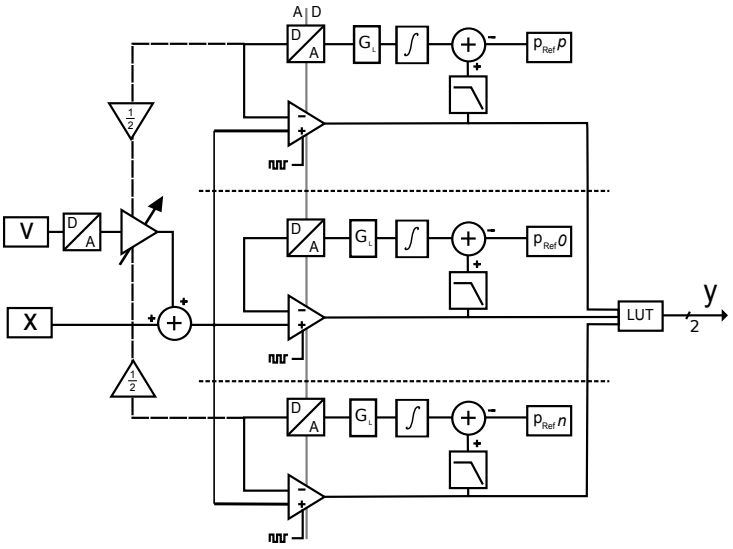

Figure 4.10: Total ADC with scaled dither added to the input signal

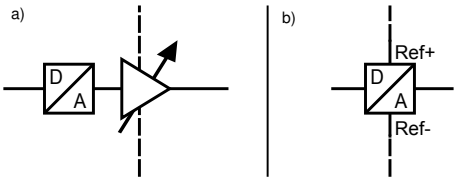

Figure 4.11: Scaling the dither while converting to analog domain. b) is the proposed implementation of a)

optimal rule for a specific signal type is applied, the SFDR is largest. For a sine wave for instance, the decision level rules are optimal when the dithered signal ampltitude exactly spans the input range.

In practice when the ADC is used in the spectrum analyzer, the most conservative decision probability rules must be applied. Only in that case it can be guaranteed that distortion components for any type of input signal are below the noise floor.

For a sine wave, this conservative setting results in a raised noise floor and thus SFDR is degraded. However, for analyzing the behavior of the ADC, the optimal rule per signal type can be applied.

This section describes optimal decision probability rules for a sinusoidal signal and Gaussian distributed signal. Finding optimal decision level rules for other types of signals is a bit more complicated and is briefly addressed (finding optimal decision rules for these signals is expected to be quite a study and is considered out of scope of this thesis):

Decision level rules for a sine wave as input The PDF of a sine wave:

$$p_x(x) = \frac{1}{\pi \cdot \sqrt{A^2 - x^2}} \tag{4.43}$$

$$\tag{4.44}$$

where A is set to $\frac{3}{2}LSB$ for rectangular dither and $1LSB$ for triangular dither. For rectangular dither:

$$p_v = \Pi_{LSB} \tag{4.45}$$

$$p_{w_r} = p_x * p_v \tag{4.46}$$

and for triangular dither:

$$p_v = \Pi_{LSB} * \Pi_{LSB} \tag{4.47}$$

$$p_{w_t} = p_x * p_v \tag{4.48}$$

Non-linearity is minimized when all the possible input values are within the ADC range. The null-decision level must correspond to a probability of 0.5, because of PDF symmetry. The positive decision probability must correspond to half the maximum input value, the negative decision level must correspond to half the minimum input value.

The optimal decision are, for rectangular dither:

$$p_w^{-1}([\frac{1}{2}, 0, -\frac{1}{2}]) = [0.2542, 0.5, 0.7457] \tag{4.49}$$

The optimal decision are, for triangular dither:

$$p_w^{-1}([\frac{1}{2}, 0, -\frac{1}{2}]) = [0.1250, 0.5, 0.8750] \tag{4.50}$$

These results are verified by simulation.

The MATLAB snippet for obtaining these rules can be found in Appendix C.5.1.

Decision level rule for a Gaussian distributed signal A Gaussian distributed signal can have any value theoretically. In practice the input signal range will be bounded, but a decision level rule for which all the possible input values fall into the ADC range results in a lot of attenuation.

For this decision level rule the percentage of samples falling outside the ADC range is chosen such that the SFDR is not degraded to below 40, 50 and 60 dB.

A relation between distortion and signal power is determined by simulation. Figure 4.12 shows the relation between the power of a Gaussian distributed signal and the maximum power of a clipping error frequency component. The input signal is shown in Figure 4.13. The simulation is repeated for various input signal bandwidths with different locations in the spectrum, yielding approximately the same result. The MATLAB code is listed in Appendix C.5.2.1.

The PDF of the input signal:

$$p_x = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{4.51}$$

$$p_w = p_x * p_w \tag{4.52}$$

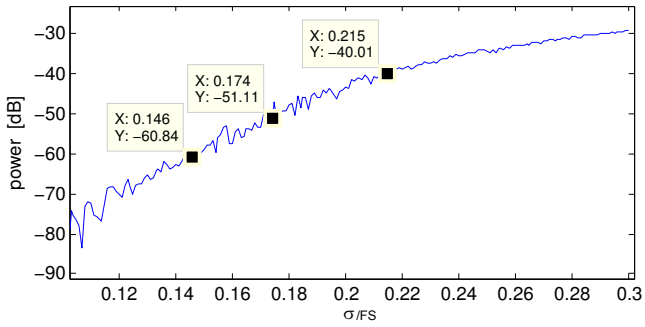

Figure 4.12: clipping error maximum frequency component power per signal input power

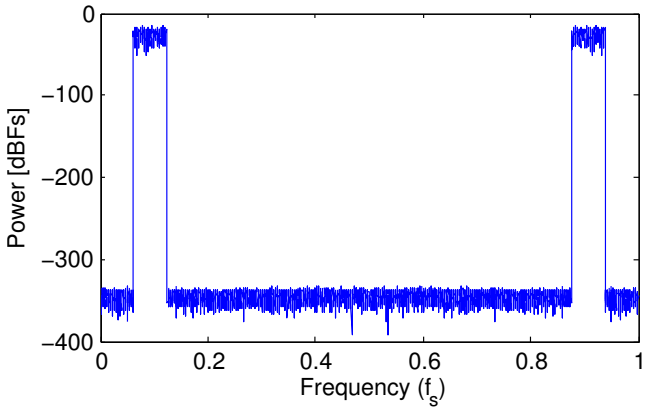

Figure 4.13: Gaussian distributed band-limited input signal.

The input signal power allowed is:

$$\sigma^{(40dB)} = 0.215[\frac{1}{FS}] \tag{4.53}$$

$$\sigma^{(50dB)} = 0.174[\frac{1}{FS}] \tag{4.54}$$

$$\sigma^{(60dB)} = 0.146[\frac{1}{FS}] \tag{4.55}$$

This gives the following decision level probabilities (MATLAB code of obtaining these number is found in Appendix C.5.2.2):

$$p_{ref}^{(40dB)} = p_w^{-1}([\frac{1}{2}, 0, -\frac{1}{2}]) = [0.1354, 0.5, 0.8646] \tag{4.56}$$

$$p_{ref}^{(50dB)} = p_w^{-1}([\frac{1}{2}, 0, -\frac{1}{2}]) = [0.0925, 0.5, 0.9075] \tag{4.57}$$

$$p_{ref}^{(60dB)} = p_w^{-1}([\frac{1}{2}, 0, -\frac{1}{2}]) = [0.0626, 0.5, 0.9374] \tag{4.58}$$

These decision probabilities differ from the probabilities used in astronomy applications [8], [7] for reasons explained in section 4.4.1. In those applications

the optimal decision level probabilities are:

$$\Delta = 0.91 \cdot \sigma \tag{4.59}$$

$$p_{ref}^{(radioastronomy)} = CDF^{-1}(-0.91, 0, 0.91) \tag{4.60}$$

$$= [0.1814, 0.5, 0.8186] \tag{4.61}$$

4.4.7 Uncorrelated quantization and dither noise

The performance of the 2-bit AD conversion is increased by utilizing the cross-correlation spectrum analyzer: the quantization and dither noise in the spectrum is decreased. To achieve this reduction, uncorrelated dither is added to both parallel signal paths and the dither and quantization noise floor is lowered by cross-correlation and spectral averaging.

In case of an analog front-end with a zero-IF mixer concept, generation of two uncorrelated complex dither signals is done by four dither generators (a,b,c,d):

$$v_1 = v_a + i \cdot v_b \tag{4.62}$$

$$v_2 = v_c + i \cdot v_d \tag{4.63}$$

For a mixer-less concept two dither signals are required, as the dither signals are not complex.

For each dither signal a dither DAC is required and the signal is scaled to the LSB of that ADC. Figure 4.14 shows the block schematic of the analog to digital conversion for a zero-IF mixer concept.

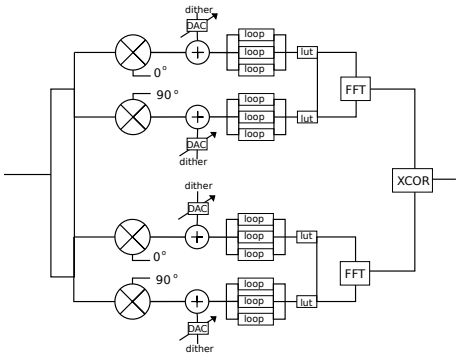

Figure 4.14: ADCs in a total system in case of an FX correlator. Decision level feedback to dither DAC, attenuator and averaging not drawn. For each ADC one dither DAC is introduced.

4.4.8 Input signal dependency

During system level design, dependencies of the system performance on the input signal have been found. Because not all characteristics of the input signal are known, the exact impact on system performance is not presented

and further research on this topic is listed as a recommendation in chapter 6. The following paragraphs elaborate these dependencies

Dependency due to sampling When the input signal PDF is symmetrical around its mean, the PDF of the sampled version is not exactly symmetrical in most cases. In Figure 4.15 this is illustrated for a sine wave. This results in distortion when the signal is quantized by the CDF based AGC ADC, because the decision levels will not be spaced with equal distances. The estimated PDF becomes more symmetrical when the input signal frequency is lower, thus the decision level spacing difference reduces when signal frequency is reduced.

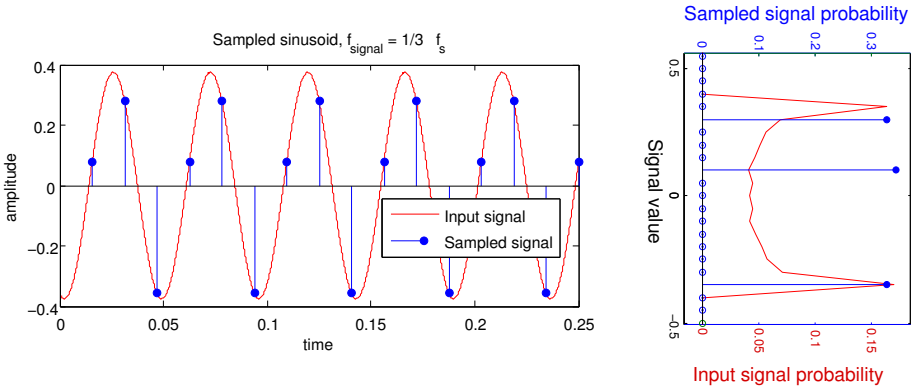

Figure 4.15: A sampled sine wave and its non-symmetrical PDF of a sampled sine wave.

For a sine wave, the unequal spacing of the decision levels depends on its frequency and phase related to the sample frequency and phase. Figure 4.15 shows a case where the effect is very clearly visible. The frequency is $\frac{1}{3}$ of the sample frequency.

In case of the CDF-based AGC ADC the PDF of a sine wave is estimated by observing a number of samples in the time domain. Because of the problem described above, the estimated PDF of a sine wave can vary periodically in time. The period of this variation is the common period of the sine wave and the sample frequency. Figure 4.16 illustrates this variation of the PDF over time.

Dependency in case of sum of several sine waves Another dependency of the performance of the ADC on the input signal becomes visible when the input signal is the sum of small number of sine waves. Such a signal can result in non-symmetrical PDFs as is illustrated in Figure 4.17. The asymmetry is present when the initial phases of the sine waves differ.

The chance that such a signal is picked up in practice may be very small, such that it can be considered not a problem. This requires further research.

Solutions Some potential solutions are shortly discussed:

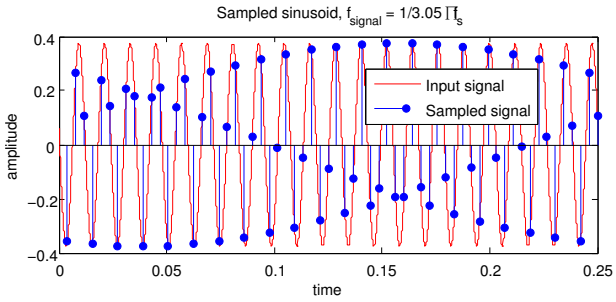

Figure 4.16: Sampling of a sine wave: illustration of variation in short interval estimated PDF. When this PDF is estimated for example from 0 to 0.1 seconds and from 0.1 to 0.2 seconds, the resulting PDFs will be different.

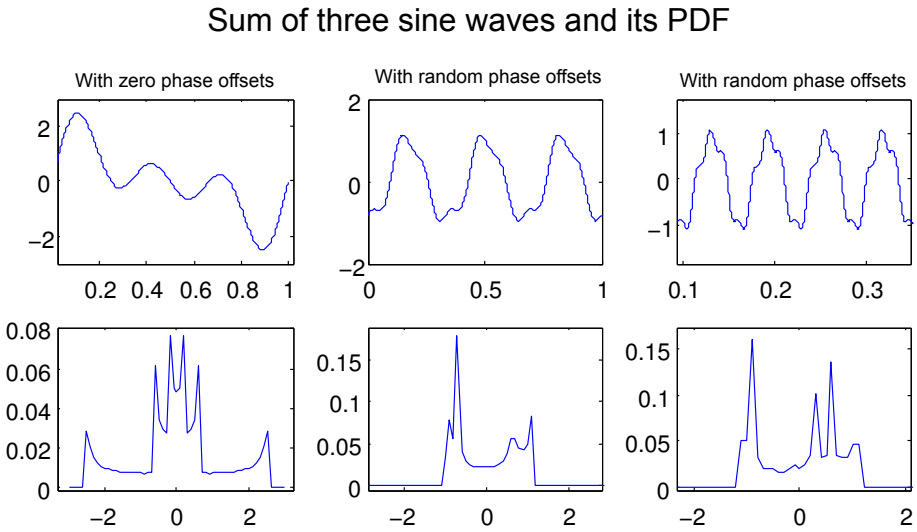

Figure 4.17: Sums of multiple sine waves with different frequency and phase offset result in symmetrical or asymmetrical PDFs. The three signals are the sum of three sinusoids only with different phase differences.

- *Increasing the oversample factor.* The PDF of a sine wave resulting from an estimation becomes more symmetrical when the sample frequency is higher. The variation in the PDF estimates also is reduced.

- *Detect unequally spaced decision levels.* When an input signal results in unequally spaced decision levels, the system controller can detect it and disregard the estimated spectrum.

4.4.9 Multi-bit CDF based AGC ADC

Until now only a 2-bit ADC is considered. In this context, a multi-bit ADC is an ADC with more than 2 bits. An ADC with a larger resolution is easily constructed when more decision level loops are placed in parallel. Decision levels closer to the range boundaries of the ADC will become a problem. The

probability that the input signal crosses that decision level will become smaller as the ADC resolution increases. The time required to properly estimate those points in the CDF is thus increased as the probabilities move closer to 0 or 1.

Suitability of such a multi-bit CDF based AGC ADC depends on system requirements. To have insight in a multi-bit ADC, additional research is required on this topic.

4.4.10 Applicability of the CDF-based AGC ADC

Theoretically the dithered CDF-based AGC ADC allows a SFDR of 60 dB when a pure sine wave is input to the spectrum analyzer. However, this performance requires knowledge about the signal received, which is in contradiction with the design goals: the energy detection spectrum analyzer must sense the spectrum without having knowledge on the input signal.

Three problems arise when the ADC is used in an energy detection spectrum analyzer for cognitive radio.

- The decision level probabilities for optimal performance differ per type of input signal. In practice the most conservative settings must be used, which are the probabilities for Gaussian distributed noise. When a sine wave is input to spectrum analyzer, the signal will not be full scale and the SFDR is degraded by 5 dB (which is obtained from simulation), so the achievable SFDR is 55 dB.

- Signal frequency component phase differences. When the input signal to the ADC consists of one or a few pure sine waves, the phase difference between the sine waves may introduce non-symmetrical PDFs, which degrade the SFDR seriously. It may be that signals picked up by an antenna prove to have symmetrical PDFs, but this is then knowledge about the input signal, which is in contradiction with the design goals. The impact on performance when real signals picked up by an antenna is subject to future research and is listed as a recommendation in Chapter 6.

- Sine wave and sample clock phase differences. For a sine wave with a frequency close to the sample frequency, the estimation of a symmetrical PDF can result in a non-symmetrical PDF. If this is the case, decision levels are spaced non-uniformly and SFDR is degraded seriously.This problem is reduced when the input signal is oversampled. The exact impact of oversampling is listed as a recommendation in Chapter 6.

The SFDR degradation because of non-ideal decision levels may be acceptable but the need for oversampling and the knowledge required about signals picked up by an antenna make this ADC less attractive for the use in an energy detection spectrum analyzer.

4.5 Simulation

The theoretical performance of the proposed CDF-based AGC ADC is verified by system level simulations. An ADC and zero-IF mixer front-end are simulated to verify that the ADC can work for energy detection spectrum sensing in

cognitive radio. The results in the frequency domain are presented as spectra of complex valued signals.

The expected behavior and performance of the ADC are verified by simulation using SIMULINK and MATLAB. The decision level loop is built out of SIMULINK blocks. Input signals are generated in MATLAB and imported in SIMULINK, output signals are exported to and analyzed in MATLAB.

This section consists of two subsections:

1. Functional simulations. The expected function of the ADC is verified. The settling of the ADC is shown and discussed and estimated spectra of different input signals are discussed.

2. Non-linearity simulations. Because the comparator is worked out at system level in Chapter 5, three sources of additional non-linearity are modeled at system level: comparator offset, comparator hysteresis and comparator noise. Maximum allowed values for these non-linearities are found as they are expected to be present at the circuit level.

4.5.1 Functional simulations

Following paragraphs show and discuss the simulation results. The time domain simulation results are shown for a single ADC, as each ADC in the cross-correlation front-end behaves the same. The spectra presented are based on a zero-IF mixer concept front-end. I and Q signals are AD converted and thus is the frequency range $[-\frac{1}{2}f_s, \frac{1}{2}f_s]$.

In the following paragraphs three cases are discussed:

1. A sine wave is the input signal, the dither signal has a rectangular PDF and the probabilities are set to the optimal values for a sine wave. In practice, for the cognitive radio energy detection spectrum analyzer these setting cannot be used, because it is not known whether the signal is a sine wave or not.

2. A sine wave is the input signal, the dither signal has a triangular PDF and the probabilities are set to the optimal values for a sine wave.

3. A sine wave is the input signal, the probabilities are set to the optimal values for a Gaussian distributed signal. With these settings unacceptable clipping is avoided for sinusoidal or Gaussian distributes signals. Because these are the most conservative settings, in practice these setting must be used.

4. A Gaussian distributed signal is the input signal.

4.5.1.1 Sine wave input, Rectangular dither, optimal sine wave probability rules applied

To investigate the SFDR of the loop, a sine wave is used as input signal to the total ADC. The probability levels for this sine wave are set to the optimal values for a sine wave.

Figure 4.24, 4.19 and 4.20 show the result of simulation in SIMULINK. The SFDR in Figure 4.20 is 60.1 dB. The frequency component with strength

-62.66 dB limits the SFDR. The achieved SFDR is thus 2.5dB lower than the theoretical SFDR of 62.7 dB.

The settings used for the simulation are shown in Table 4.2. As the decision levels climb to their intended levels, the dither signal scales accordingly. The output signal also changes according to the decision levels. The settling time is about $3.6 \cdot 10^4$ samples: $23.4\mu s$ for a sample frequency of $1536MHz$. This is only 0.12% of the measurement time.

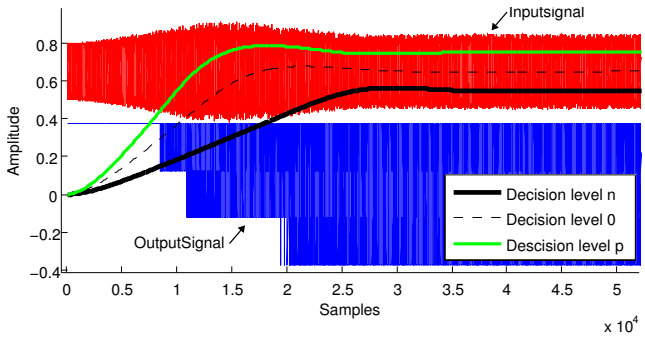

Figure 4.18: Settling of the ADC, settings used shown in Table 4.2. The input signal shown is the input signal at each comparator.

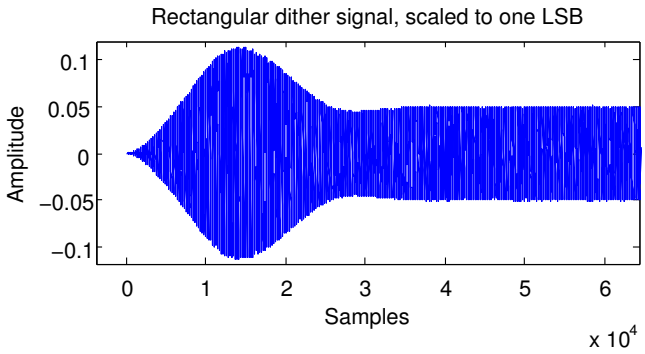

Figure 4.19: Scaled rectangular dither signal, settings used shown in Table 4.2

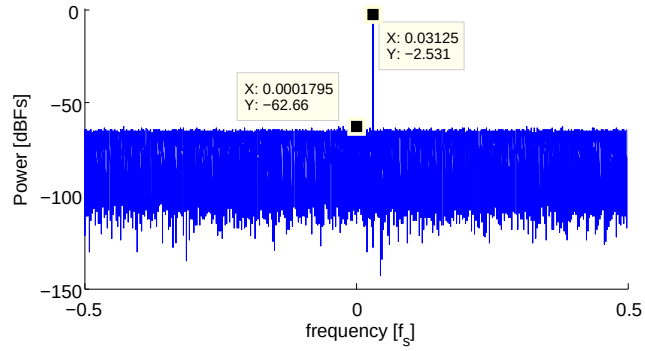

Figure 4.20: Spectrum of quantized sine wave, settings used shown in Table 4.2

Observations The non-linearity effects as discussed in Section 4.4.4.5 can be seen in this simulation. The simulation shows a CDF step response. This is because the initial state of the loop does not corresponds with the CDF of the input signal. The effects which can be seen are elaborated:

- The comparator output is limited,so the maximum slope of a decision level is limited. The gain of the comparator of the lower decision level is smaller, because the target decision level voltage is closer to the low output voltage of the comparator.

- The dither signal amplitude has more relative overshoot than either of the decision levels. The upper decision level increases faster than the lower, such that the difference signal has more overshoot.

Spectrum averaged XC result, long measurement time Figure 4.21 shows the simulation result of the full measurement time of 0.2 seconds. The SFDR is 58.2 dB.

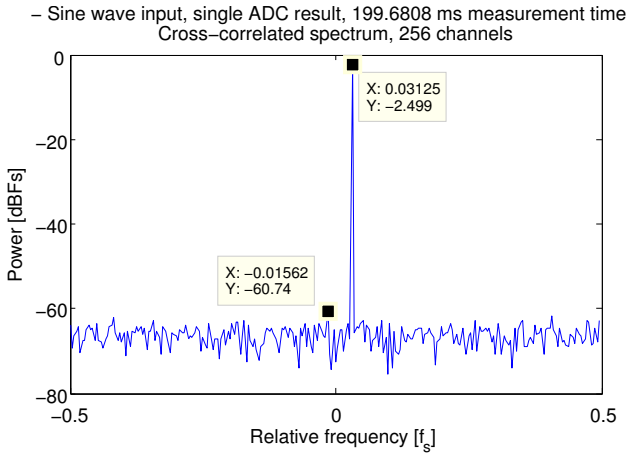

Figure 4.21: Total IF front-end simulation, spectrum (when settled), settings used shown in Table 4.2

4.5.1.2 Sine wave input, triangular dither, optimal probability rules applied

When triangular dither is used, the result is as expected: the noise floor is higher and the settling time is longer. Figure 4.22 shows the settling of one ADC. When the system would be implemented and the positive voltage is 1 volt, then for this input signal, dither signal and loop settings, the input signal to the ADC would clip. The dither is amplified such that the sum of the input signal and the dither leads to values outside the range of supply voltage. Figure 4.23 shows simulation results when the clipping is modeled. Nothing has changed, because the input signal is above the upper decision level, whether it is being clipped or not: the ADC output does not change.

Setting	**Value**
Input signal Sample clock	1.536 GHz
Input signal type	Sine wave
Input signal frequency	48 MHz
Input signal offset	0.65
Input signal amplitude	0.15
Dither signal	Rectangular
p_n	0.75
p_0	0.5
p_p	0.25
H_{lpf}	$\frac{1}{s \cdot 6 \cdot 10^{-5}+1}$
G_l	$3 \cdot 10^5$

Table 4.2: Simulation settings for ADC simulation

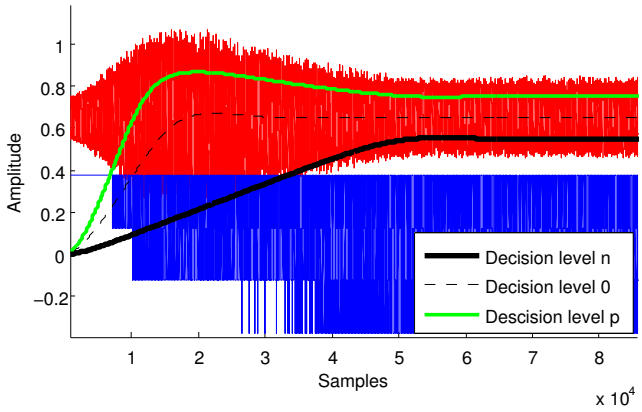

Figure 4.22: Settling of the ADC, settings used shown in Table 4.3

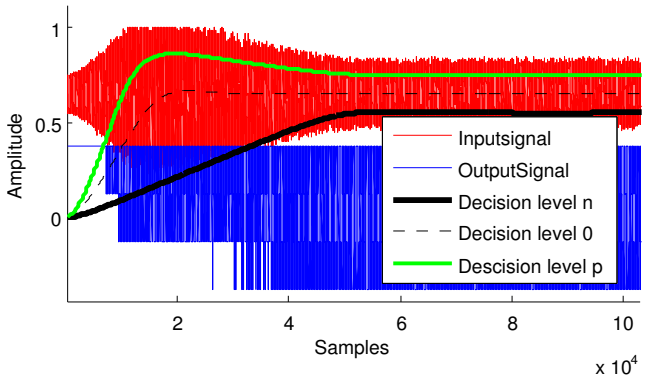

Figure 4.23: Clipping of input signal while settling. 4.3

Setting	Value
Input signal Sample clock	1.536 GHz
Input signal type	Sine wave
Input signal frequency	48 MHz
Input signal offset	0.65
Input signal amplitude	0.15
Dither signal	Triangular
p_n	0.875
p_0	0.5
p_p	0.125
H_{lpf}	$\frac{1}{s \cdot 6 \cdot 10^{-5}+1}$
G_l	$3 \cdot 10^5$

Table 4.3: Simulation settings for ADC simulation

4.5.1.3 Sine wave input, optimal Gaussian distribution probability rules applied

When the probability are set to the optimal probabilities for a Gaussian distributed signal, the power of the sine wave is reduced by 5.2 dB and the settling time has increased to

Setting	Value
Input signal Sample clock	1.536 GHz
Input signal type	Sine wave
Input signal frequency	48 MHz
Input signal offset	0.65
Input signal amplitude	0.1
p_n	0..09374
p_0	0.5
p_p	0.0626
H_{lpf}	$\frac{1}{s \cdot 6 \cdot 10^{-5}+1}$
G_l	$3 \cdot 10^5$

Table 4.4: Simulation settings for ADC simulation

4.5.1.4 Gaussian distributed signal input

The simulation results in case of sinusoidal signals at the input show a smaller resolution bandwidth then the intended 6 MHz. This is done to show that no harmonic distortion components appear in the spectrum, while limiting the simulation time. For a Gaussian distributed signal, this cannot be done because due to the wide input signal bandwidth, the distortion components are a lot more distributed across the spectrum.

Figure 4.27 shows the result of simulations in SIMULINK. The decision levels are set for no distortion components above -60 dBFs (obtained in Section 4.4.6).

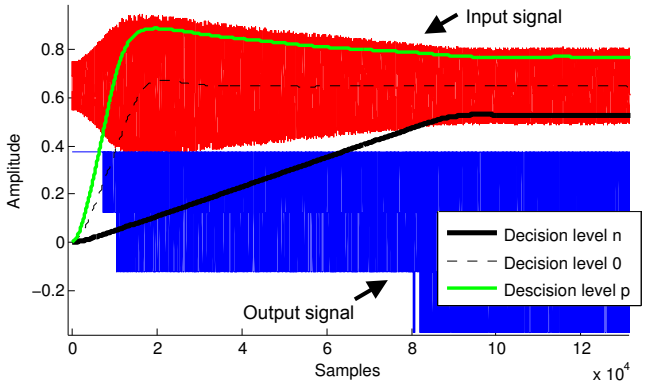

Figure 4.24: Total ADC simulation, settings used shown in Table 4.4

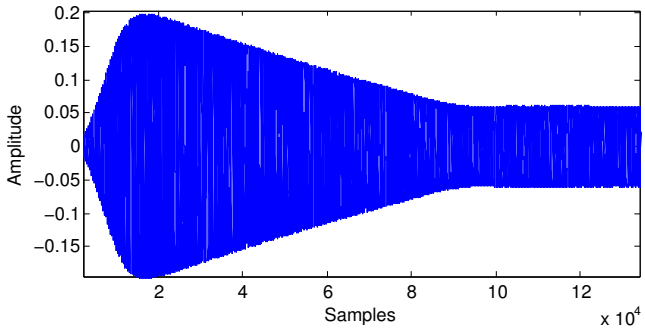

Figure 4.25: Scaled dither signal, settings used shown in Table 4.4

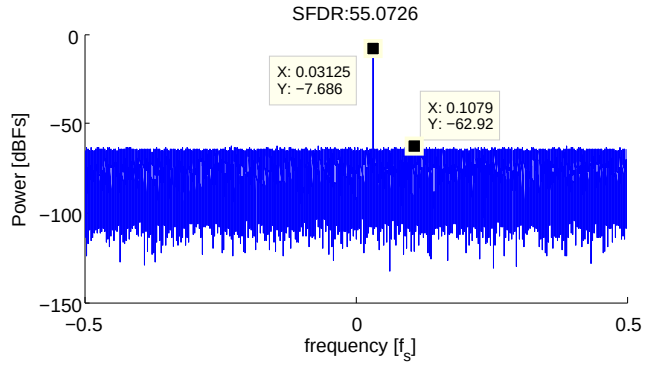

Figure 4.26: Spectrum when ADC is settled, The fundamental tone now has a amplitude of -7.7 dBFs. Settings used shown in Table 4.4

The settling time in this case is about $6 \cdot 10^4$ samples: $39\mu s$ for a sample frequency of $1536MHz$.

The settings used for the simulation are shown in Table 4.5. The settling time per decision level is different than in the case of a sine wave, resulting in more overshoot of the dither signal amplitude.

The spectrum of this short measurement time simulation is not shown, because it does not give a lot of information. In the case of a Gaussian distributed signal, reducing the resolution bandwidth does not provide more information.

In the following paragraph, the resulting spectrum is presented when the measurement time is increased.

Setting	**Value**
Input signal Sample clock	1.536 GHz
Input signal type	Gaussian distributed
Input signal frequency	64-96 MHz
Input signal offset	0.65
Input signal power	0.0466
p_n	0.9374
p_0	0.5
p_p	0.0626
H_{lpf}	$\frac{1}{s \cdot 6 \cdot 10^{-5}+1}$
G_l	$3 \cdot 10^5$

Table 4.5: Simulation settings for ADC simulation

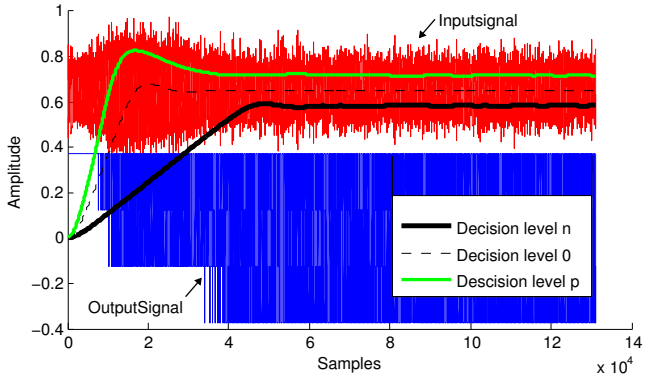

Figure 4.27: Gaussian distributed signal, settling behavior. Settings shown in Table 4.5.

Spectrum averaged XC result, long measurement time Figure 4.28 shows the result of a simulation of the full measurement time of 0.18 seconds. It is clearly seen that the resulting spectrum noise floor is non-white. The strongest distortion components are located at -3 times the fundamental tone frequencies. The non-whiteness of the noise floor is because of the clipping noise which is present. It is interesting to note that the distortion components

at -3 times the fundamental tones decrease when measurement time increases. The clipping distortion of the parallel paths is thus partially uncorrelated.

In the spectrum, spectral leakage is clearly visible. This effect can be reduced by applying a tapering window. Unfortunately this technique decreases resolution bandwidth [5]. Choosing a suitable window is subject to future research.

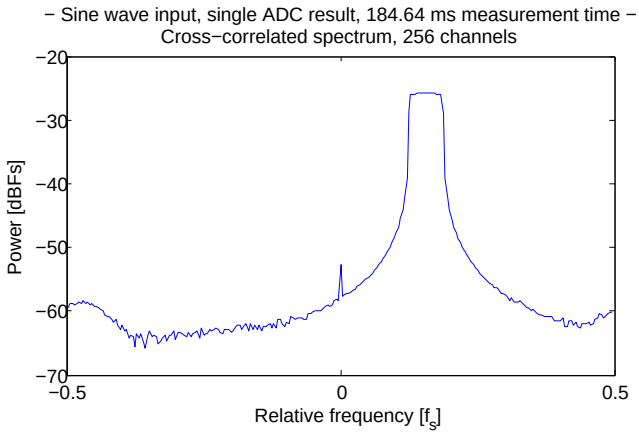

Figure 4.28: Total IF front-end simulation, spectrum (when settled), settings used shown in Table 4.5.

4.5.2 Modeling of non-linearities

Because the circuit level design in the next chapter zooms in to the comparator, three non-linearity effects are investigated at system level: comparator offset, comparator hysteresis and comparator noise. Offset is a problem when the dither is scaled to the decision levels. When the offset differs between decision levels, the dither is not scaled properly which leads to distortion.Hysteresis is a memory effect, the outcome of a comparison between two values depends on the previous values. This effect introduces additional distortion components and thus decreases the SFDR of the system.

4.5.2.1 Comparator offset

An ideal comparator gives a high output value when the voltage at the positive terminal is higher than the voltage at the negative terminal. When a comparator suffers from offset, the output of the comparator is high when the voltage at the positive terminal is at least the offset voltage higher than the voltage at the negative terminal

The CDF-based AGC ADC has offset canceling for each of the decision levels. When the offset of a comparator is canceled, the decision levels will differ in value with respect to the intended value. The dither signal is scaled to the upper and lower decision levels. If the offset for those decision levels are equal, the offset is canceled as well:

$$LSB = \frac{(d_p + v_o) - (d_n + v_o)}{2} = \frac{(d_p) - (d_n)}{2} \tag{4.64}$$

Where d_p and d_n denote the input voltages at negative terminals of the upper and lower comparator of the ADC. v_o denotes the offset voltage. When the upper and lower decision levels have different offsets, the dither range deviates by half the difference in offset:

$$LSB = \frac{(d_p + v_{op}) - (d_n + v_{on})}{2} = \frac{(d_p) - (d_n)}{2} + \frac{v_{op} - v_{on}}{2} \tag{4.65}$$

where v_{op} and v_{on} denote the offset voltages for the upper and lower comparators respectively. In this case the dither range is not equal to one LSB and will cause additional distortion.

It may seem a plausible countermeasure to increase the dither signal range such that the range of the dither is larger than decision level spacing in any case. However, the conditions for independent moments and spectral whiteness of Section 3.3 are not satisfied.

Also simulation results show that the added distortion is not reduced by this countermeasure: would there be no offset in the system, increasing the dither range not only leads to more noise but also to additional distortion.

Allowed offsets Offsets are canceled without SFDR degradation when each comparator in the ADC has equal offsets. So only offset-mismatch is looked at: comparator offset relative to the other comparator offsets. In case of offset-mismatch, the dither signal is not scaled properly to an LSB. Allowed offset values are obtained by simulation.

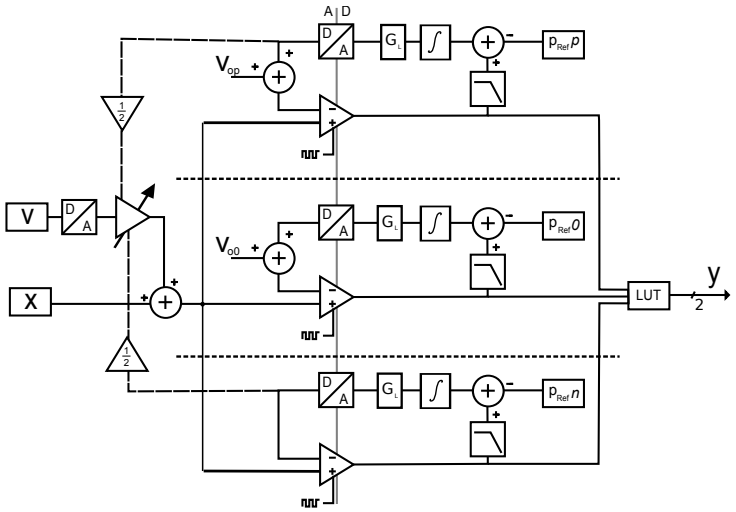

Figure 4.29: Total ADC with offsets added to upper and middle comparator.

Three comparators give two relative offsets. In this case the offset of the lower comparator is fixed and the other two are varied. The comparator offsets are denoted by $[v_on, v_o0, v_op]$ and $v_on = 0$. For a SFDR of 60 dB the allowed offsets are found by simulation. Figure 4.29 shows the simulation set up. The offset is swept and the maximum allowed value is found for which the distortion components in the resulting spectra are below 60 [dBFs].

1. $v_o(0) = v_o(p)$ and $v_o(0,p) > 0$: The resulting dither amplitude is too large. Allowed offset: $v_o(0,p) < 1mV$
2. $v_o(0) = v_o(p)$ and $v_o(0,p) < 0$: The resulting dither amplitude is too small. Allowed offset: $v_{o(0,p)} > -0.7mV$

These numbers are a starting point for circuit level design optimization.

4.5.2.2 Comparator hysteresis

Hysteresis is defined as the maximum difference in the values of a code transition, when the transition level is approached by a changing input signal from either side of the transition [21]. Hysteresis is non-linear effect, so distortion components in the spectrum are expected. In many applications hysteresis is deliberately added to a comparator to get stable output signals: when the difference voltage at the comparator is very small, the noise in the signal causes an fast alternating output. For the CDF-based AGC ADC the essential information is contained in the statistics of the fast alternating comparator output. Therefore, the hysteresis must be as small as possible.

Hysteresis is subdivided in dynamic and static hysteresis effects. Dynamic hysteresis is the non-linearity which depends on input signal frequency. Static hysteresis is caused by memory effects which exist at circuit level. Allowed static hysteresis values are obtained by system level modeling of the hysteresis effects. In this case only static hysteresis effects are modeled, because dynamic hysteresis effects depend on the exact implementation of the comparator. Static hysteresis is modeled as:

$$w_h(n) = w(n) + h \cdot 2 \cdot (w_h(n-1) - \frac{1}{2}) \tag{4.66}$$

$w(n)$ is the original comparator input sample at moment n, w_h is the changed input sample due to the hysteresis and h is the allowed hysteresis. The output is thus w_h compared to the decision level. Figure 4.30 shows the modeling of the hysteresis effect.

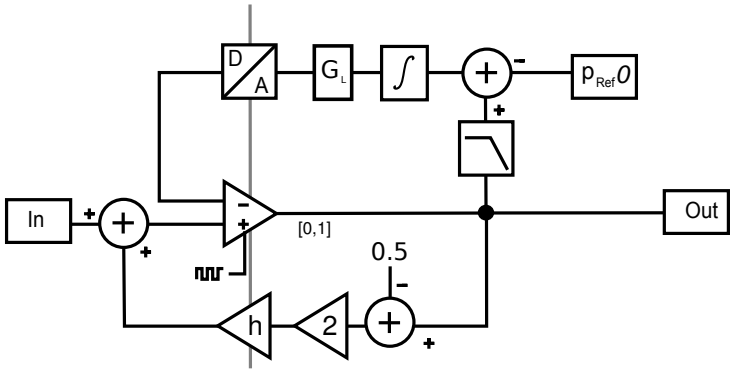

Figure 4.30: Model of decision level loop with comparator with hysteresis effect.

The allowed value for h is determined by simulation. A SFDR of at least 60 dB is achieved when:

- $h < 0.3[mV]$

Thus when a comparison results in a high output of the comparator and the next comparison will results in a low output, the input signal difference must be larger than h for this next comparison. This value h is used as a starting point for circuit level optimizations.

4.5.2.3 Comparator noise

Noise added by the comparator may lead to additional clipping distortion and may degrade the SFDR. For the case of a sine wave with optimal decision level rules, the allowed amount of noise is obtained by simulation. For each comparator in the an ADC, statistically independent random Gaussian distributed noise is added. When the input signal is smaller, the noise of the comparators is relatively larger, thus the smaller the input signal amplitude, the smaller the allowed noise is: this is the traditional noise and linearity trade-off. Table 4.6 shows the allowed noise levels for optimal sine wave probability settings.

Input amplitude [V]	**Allowed noise σ [mV]**
0.15	1.6
0.1	0.9
0.075	0.3
0.05	0.1

Table 4.6: Allowed noise per input sine wave amplitude, for optimal sine wave probility settings.

For a Gaussian distributed signal, the noise added by the comparator can be translated to increased amplitude of the input signal. The allowed noise can than be obtained

4.6 Summary and conclusion

Summary The system level implementation of the CDF-based AGC ADC is described in this chapter. System choices are made and the theoretical performance is calculated. The CDF-based AGC ADC concept is introduced and its automatic gain control and offset canceling mechanism is described.

Dither is added to the input signal to reduce distortion components in the spectrum at the cost of a higher noise floor. Because the values of an LSB are variable for the ADC, the dither is scaled to the value of an LSB.

Optimal settings for the ADC are derived for different signal types. Because the energy detection spectrum analyzer does not have knowledge about the input signal, in practice the most conservative setting must be applied for any type of signal.

The theoretical performance is achieved when optimal settings for a sine wave are used. However, because conservative settings must be used in practice, the practical performance will be less.

The correct functioning of the ADC is verified by simulation. The theoretical SFDR is achieved when a sine wave is input to the system and when the

corresponding optimal settings are used. With the most conservative settings, the SFDR is decreased by 5.2 dB.

During this verification, the assumption of the input signal having a symmetrical PDF appeared to be a problem. When several strong narrow-band signals are present in the input signal, the PDF becomes non-symmetrical. Also the frequency and phase of narrow-band input signals related to the sample frequency and phase influence the performance. For sinusoidal signals with frequencies close to the sample frequency, the sampled version of the signal has a non-symmetrical or slowly varying non-symmetrical PDF.

The performance of the ADC thus depends on the input signal. For larger oversample factors this dependency reduces and the practical performance approximates the theoretical performance (for equal system settings).

When the practical performance is reduced by the non-uniform decision level spacing, this can be detected by a system controller. Thus, when the measurement is corrupted due to this effect, it is known by the system controller and the spectrum can be disregarded, although this is not acceptable in a cognitive radio application.

The ADC is simulated to verify the expected behavior of the ADC and to see if the theoretical SFDR can be achieved. The dither signals added to the (quadrature mixing) cross-correlation IF front-end are two statistically independent (complex) uniform distributed random signals. This allows the cross-correlation to reduce the dither and quantization noise floor. Thus a higher SFDR is possible than would be possible for a conventional dithered ADC with the same dither resolution, quantization resolution and resolution bandwidth.

Because the comparator is analyzed on circuit level, hysteresis and offset are modeled at system level, as they are expected circuit level non-linearities. This way maximum allowed values are obtained.

With this system level design, the performance dependencies at system level are investigated and circuit level components, such as the comparator, can be implemented on circuit level.

Conclusions When the resolution of the ADCs for a cognitive radio spectrum analyser is lowered, several problems are introduced. The ADC proposed in this chapter is able to tackle those problems, but other problems appear.

The problem of distortion due to the low resolution is reduced by adding dither to the input signal. The result is that the measurement noise floor is raised. This problem is reduced by utilizing the cross-correlation concept, thus the measurement noise floor is lowered by increasing measurement time. To do this two statistically independent dither signals with specific PDFs are required, which must be generated in the digital domain. The dither signal must be added to the analog input signal, thus additional hardware is required to convert this digital signal to the analog domain.

Another problem is, to achieve maximal SFDR, signal clipping must be avoided or limited to acceptable values. The CDF-based AGC ADC solves this problem by the AGC and offset canceling. These features are realized by adjustable ADC decision levels based on the CDF estimate of the input signal. This approach introduces new problems. Due to the coarse estimation of CDF, different signals cannot be distinguished. Thus in practice, the most

conservative ADC settings must be used, which decreases the sensitivity of the spectrum analyzer. An assumption was made that input signal PDFs are symmetrical, but the estimate of a symmetrical PDF can be non-symmetrical. This is the case for input signals with frequencies close to half the sample frequeny. The assumption may be not realistic as the PDF of a sum of a few strong sinusoids can be non-symmetrical.

Digitally dithering a 2-bit ADC is an effective way to increase its SFDR. When decision levels are varried to create AGC and offset canceling, the dither can be scaled accordingly to approximate the theoretical allowed performance. The utilization of the cross-correlation concept and statistically independent digitally generated dither effectively increases the SFDR of the dithered ADC at the cost of measurement time.

The AGC and offset canceling realization of the CDF-based AGC ADC, introduces problems which counteract the design goals of the energy detection spectrum analyzer. Because of the dependency of performance on the input signal, the CDF-based AGC and offset canceling is not considered to be a good choice for a cognitive radio energy detection spectrum analyzer. The scaled dithering and cross-correlation utilization can be applied to 2-bit ADCs with other AGC mechanism, such as in [7].

Chapter 5

Circuit level design

The previous chapters described the system level design and the theory required to make proper design choices. To have insight in the impact of implementing the ADC components on circuit level, the most critical component is selected and implemented. The comparator is implemented in Cadence using UMC090 MOSFETs. This is a 90 nm process with 1v supply voltage MOSFETs, the models used are BSIM4 models. The first part of this chapter describes the comparator, how it works and the expected causes for performance degradation. The second part presents ADC simulation results with ideal components except for the comparator. The comparator is worked out for a sample frequency of 1.536 MHz.

5.1 Critical ADC component

The ADC consists of the following blocks in the analog domain:

1. Comparator, sample frequency: 1536 MHz
2. Dither DAC, resolution: 6 bits, frequency: 1536 MHz
3. Decision level DAC, 8 bits, frequency: 3 MHz

DACs with requirements compaale to the dither DAC are found in literature and is considered to be not critical, Table 5.3 gives an overview of some DAC characteristics from literature. The decision level DAC has a relative low output frequency and is even less critical. The comparator is more critical. In system level design, the influence of offset, hysteresis and common-mode dependency became clear. To get a view on the influences of an implemented comparator on the system performance by these factors, a comparator is selected and implemented on circuit level. The selected comparator is previously implemented for the use for long on-chip wires and the specifications are in the same range as the target comparator.

The comparator may not have too much hysteresis, which adds distortion to the measured spectrum of the energy detection spectrum analyzer. When its offset is too large the effect of dither is reduced and distortion components appear. Also power estimation becomes a problem when the offset depends on the input common mode voltage.

Reference	**Resolution**	sample rate	Power	process	year
[31]	6 Bits	1.25 GHz	6 mW	1.8 V, 0.18 um	2008
[32]	6 Bits	2.7 GHz	28 mW	1.2V, 0.13 um	2006
[33]	6 Bits	5.4 GHz	20 mW	1.5V, 0.13 um	2005
[34]	6 Bits	1 GHz	7.5 mW	1.5 V,0.13 um	2005

Table 5.1: CMOS DAC characteristics from literature.

5.2 The comparator

The selected comparator is the *double tail voltage sense amplifier* by D. Schinkel et. al.[35]. The implementation described in [35] allows a sample frequency of up to 3 GHz, fabricated in a 1.2V 90nm CMOS process. The comparator was designed for being a part of a low-swing on-chip data transceiver, with input signals biased around $1.1V$. The operating characteristics thus differ from the ones in this thesis.

5.2.1 The circuit

Figure 5.2 shows the comparator used in the circuit level modeling. It is a clocked comparator, each half period it is reset and the next half period it compares the input signals. The parasitic capacitances play a crucial role in the way the comparator functions. Therefore figure 5.2 shows the comparator with parasitic capacitances connected to the internal nodes and the negative supply rail.

Both phases are described in next paragraphs.

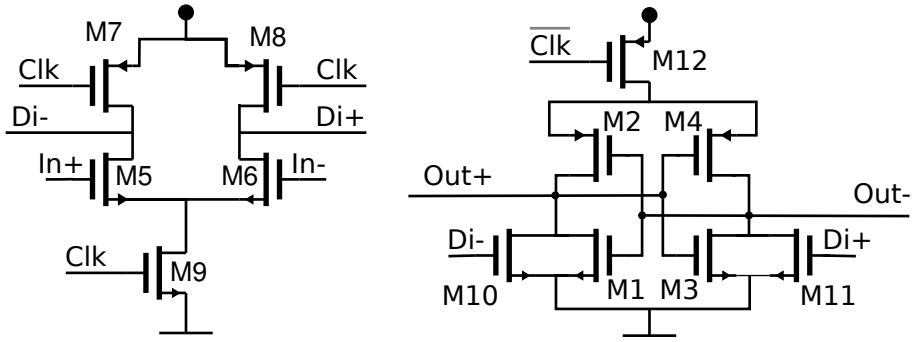

Figure 5.1: Double tail voltage sense amplifier [35], consisting of an input stage (left) and a latch (right).

Reset phase. When the Clk signal is low, nodes $Di-$ and $Di+$ are connected to the positive supply rail and C_{Di-} and C_{Di-} are charged. As a result $M10$ and $M11$ start conducting and will discharge C_{Out-} and C_{Out+}. $M12$ and $M9$ are not conducting during reset.

Compare phase. Nodes $Di-$ and $Di+$ are 'high' and nodes $Out+$ and $Out-$ are 'low'. At the rising edge of the Clk signal, $M9$ starts to conduct and the

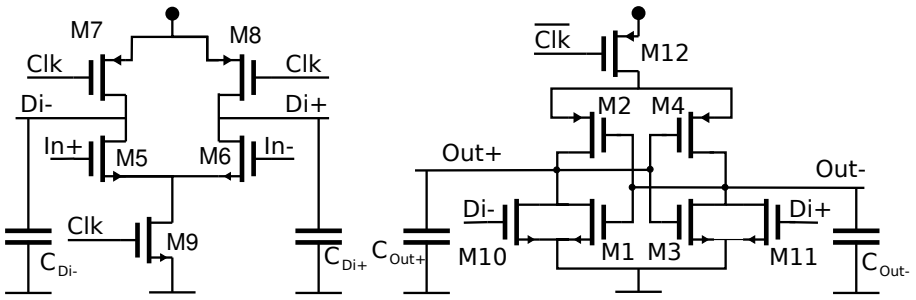

Figure 5.2: Comparator with parasitic capacitances.

voltages on $In+$ and $In-$ will make $M5$ and for $M6$ conduct. As a result nodes $Di-$ and $Di+$ are discharged to the negative supply rail with a rate depending on the input voltages.

The resulting voltage difference on nodes $Di-$ and $Di+$ cause different currents through $M10$ and $M11$. One of the output nodes will discharge faster and the positive feedback of the latch amplifies this difference such that one output node will be pulled to the negative supply rail and one to the positive supply rail.

Figure 5.3 shows the Di and output nodes of the comparator.

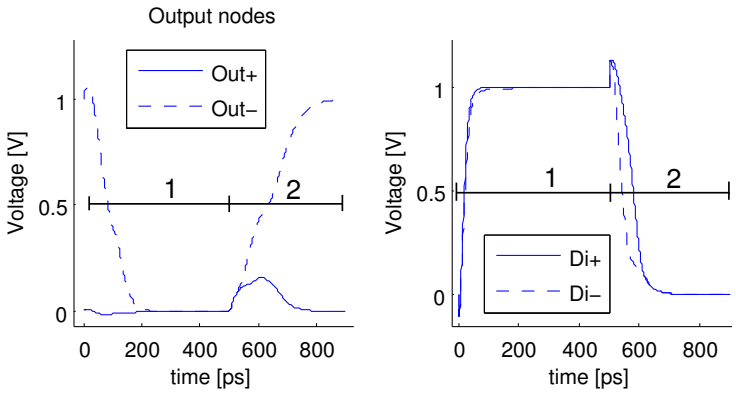

Figure 5.3: Internal and output nodes of comparator for a voltage difference of 150 mV. 1) reset phase. 2) compare phase

5.2.2 Input signal properties

Because the input MOSFETs are N type devices, the input signal is biased such that the input MOSFETs are in strong inversion. The input signal swing....

5.2.3 Block diagram

To have insight in the behavior of the comparator during the compare phase, a block diagram is derived, which shown in Figure 5.4. This block diagram shows the location of gain and the integrations. When the differential paths are

assumed to be perfectly symmetrical, the comparator behavior can be depicted as shown in Figure 5.5 (this block diagram is also presented by D. Schinkel on a poster at ICD). The gain blocks do not have a fixed gain, thus the block diagram does not represent a linear model of the comparator.

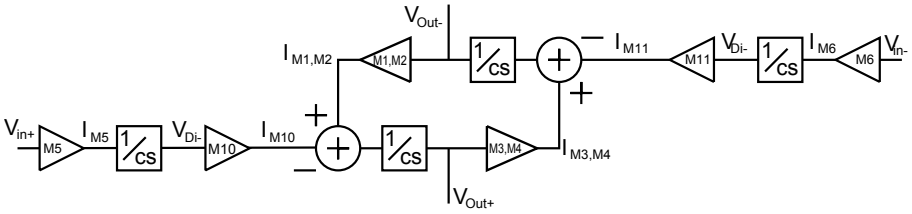

Figure 5.4: Block diagram representation of comparator

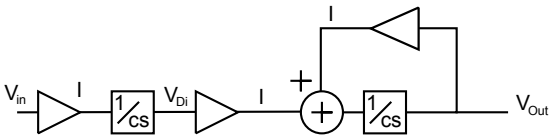

Figure 5.5: Block diagram representation of comparator, assuming perfect symmetry between parallel branches.

5.2.4 Dimensioning the comparator

To aim at minimal silicon area, the components of the comparator are initially sized with the minimal values allowed by the process. The necessary adjustments are made for proper operation. For convenient description the comparator components are grouped:

1. Latch: M1, M2, M3, M4
2. Input stage: M5, M6
3. Input stage reset MOSFETs: M7, M8
4. Input stage tail MOSFET: M9.
5. Intermediate stage: M10, M11
6. Latch top MOSFET: M12

Following paragraphs describe the considerations which are taken into account when the comparator is dimensioned.

Compare phase Component sizes influence the behavior of the comparator in the compare phase. The following list important aspects when the comparator components are dimensioned.

1 Wider MOSFETs increase power consumption due to larger currents and large parasitic capacitances which need to be charged and discharged.

2 For the comparator the input signal is integrated and the integration saturates at some point, so that the input MOSFETs (M5, M6) gain should not be too large. Would the gain be too large, the integration at the Di nodes saturate and the voltage difference on these nodes is reduced quickly. As a result, the voltage difference due to the integration at the output nodes is then limited. Because of the large input signal swing, the saturation point in time depends on the common mode voltage. For worst case, the saturation moment must be controlled such that it is within the compare phase time.

3 The latch (M1, M2, M3, M4) gain should not be too large with respect to the gain of the intermediate MOSFETs (M10, M11). Then the comparator decision would be influenced by the voltages at the imperfectly discharged output nodes too much, i.e. hysteresis is increased. The intermediate stage gain trades-off to the latch gain. Larger intermediate phase gain reduces hysteresis, but it takes longer for the latch to determine the output voltages.

4 The Di node integration must saturate at the end of the compare phase time, because at the end of the phase one output must be high and therefore the intermediate MOSFETs (M10,M11) must not conduct.

5 To reduce the common mode dependency, the $\frac{W}{L}$ of the input stage tail MOSFET (M9) can be decreased such that the MOSFET will act as a degeneration load to the common-source input phase. The gain of the input stages is then reduced.

6 To let the inverters of the latch (M1, M2, M3, M4) operate properly, in the compare phase the PMOS source voltages must be equal to the positive supply rail. M12 must be wide enough to supply the current which is conducted by the latch PMOSs. M12 must be approximately two times wider than M2 and M4.

Reset phase In the reset phase all comparator nodes are set to a specific value: all parasitic capacitances are (dis)charged. When this is not properly done, hysteresis is present. The Di nodes and output nodes are (dis)charged:

7 The Di nodes are charged such that the voltage is equal to the positive supply rail at the end of the reset phase. At the start of the reset phase both nodes will be approximately equal to the negative supply rail. Therefore, the Di nodes will not cause much hysteresis.

8 The output nodes are discharged. One of the nodes is approximately equal to the positive supply rail. When the output nodes are discharged in the reset phase, improper discharging will cause hysteresis.

9 The discharge current is limited by the intermediate phase MOSFETs (M10, M11). Di is their gate-source voltage, so when Di are not charged fast enough, the output nodes are discharged even worse.

5.2.4.1 Sizes

Based on the above performance dependencies, the following adjustments are made to the minimal sized MOSFETs:

1. LATCH PMOSs are sized 3 times wider than the latch NMOSs, to compensate for the electron and hole mobility difference.

2. The Latch top PMOS is size 2 times wider than the latch PMOSs, such that the source voltage is largely independent of the currents.

3. The input phase tail NMOS is made longer, such that it acts as a degeneration impedance. Figure 5.6 shows the effect of a longer input phase tail NMOS. Not only the dependency of offset due to mismatch on common mode voltage is reduced, but also the absolute offset is reduced.

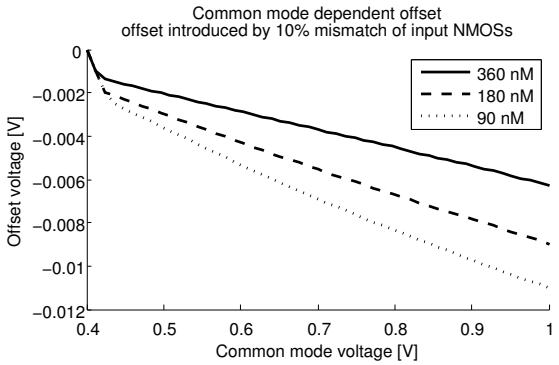

Figure 5.6: Illustration of common mode dependent offset. The offset is introduced by increasing the length of M5 by 10%. In the plot the three lines correspond to the three lengths of the input phase tail NMOS (M9).

Table 5.2 lists the component sizes.

Component	**Width [nm]**	**Length [nm]**
M1	120	90
M2	360	90
M3	120	90
M4	360	90
M5	120	90
M6	120	90
M7	120	90
M8	120	90
M9	120	360
M10	120	90
M11	120	90
M12	720	90

Table 5.2: Comparator MOSFET Sizes

5.2.5 Comparator simulation

Offset, hysteresis and metastability, are investigated by simulation. The comparator is implemented with components sized as listed in Table 5.2. Each of the differential outputs is connected to an inverter to include capacitative load. The inverters are then connected to an ideal differential-to-single-ended block followed by an ideal flip-flop to get a valid digital signal. Figure 5.7 shows the simulation set up for the comparator.

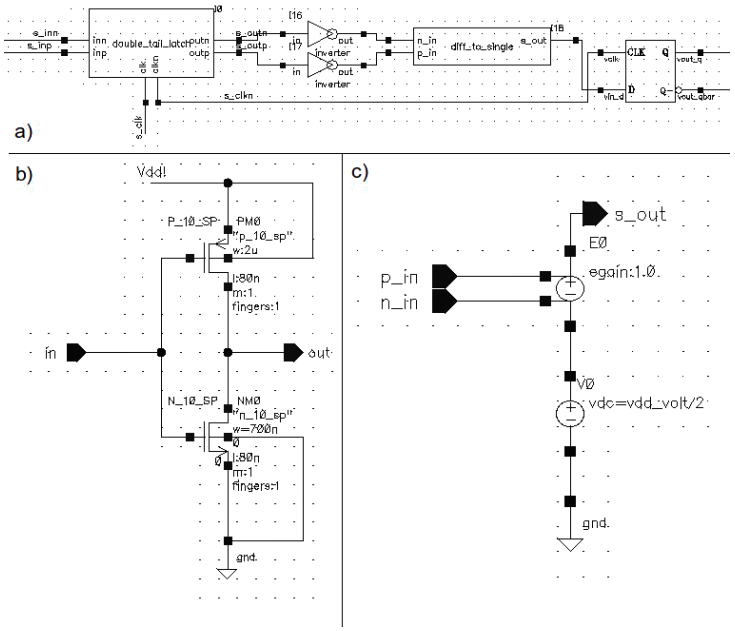

Figure 5.7: a) Simulation of the comparator. b) Inverter to take into account capacitative load. c) Ideal differential to single ended conversion.

5.2.6 Non-ideal properties

The comparator is a non-linear component. Conceptually it is non-linear which is modeled at system level, but a real comparator has other non ideal properties which introduce additional non-linearities. The sources of non-linearity described and investigated in this section are:

1. Noise
2. Offset
3. Hysteresis
4. Metastability
5. Voltage slope dependency
6. Clock feed-trough

5.2.6.1 Noise

Noise is added to each node by the components of the comparator. The input signal to the comparator is dithered and the system it is used in extracts its information from output signal statistics, so noise may seem to be not problem. However, with the optimal probability rules for a sine wave and a sine wave amplitude of 150 mV, clipping may occur which results in distortion. On the system level a maximum input referred standard deviation for zero-mean Gaussian distributed noise is derived for this case, which is 1.6 mV. This value is worst case, because for practically more relevant settings the allowed noise is larger. So worst case, the comparator noise must not exceed this value.

The analysis of noise in a clocked comparator is not as straightforward as the usual steady-state analysis for amplifiers [36]. In [37] the effect of noise is analyzed for a latched comparator. The comparator operation is described by identifying 3 phases and for each phase the noise effects are calculated. To know the noise of the double tail voltage sense amplifier, a similar analysis is required. For this thesis such an analysis does not fit in the time budget and is listed in the recommendation section in Chapter 6. A standard deviation of the input referred noise of 1 mV is presented in [37], although device dimensions are not presented. The comparator is comparable to the double tail voltage sense amplifier. Both comparators are designed for the use in an integrated ADC realized in a 90 nM process.

5.2.6.2 Offset

Offsets in the comparator are canceled by the ADC, but the dither signal is improperly scaled when the offsets of the comparators in the ADC differ too much.

The comparator is fully differential, thus offsets are only present because of component mismatch. In the case of mismatch one of the differential branches will be slightly different than the other. The resulting offset will be depending on the common mode voltage of the input signal. Thus the worst case offset must be controlled to be within the allowed value.

Investigation by simulation The dependency of the offsets on common mode is investigated by the circuit shown in Figure 5.8;

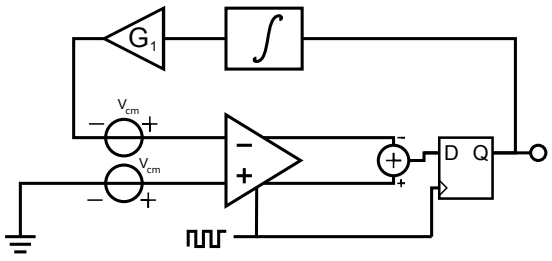

Figure 5.8: Test-bench for investigating offset

The allowed offset difference is $0.7mV$. Based on process spread information, the latch PMOS area can be increased and proper precautions can be

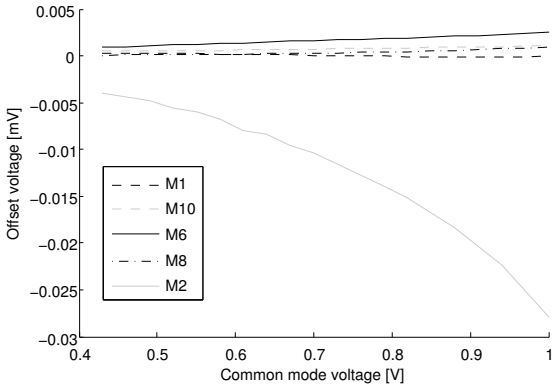

Figure 5.9: Common mode dependent offset for 5nM difference in MOSFET length for components shown in figure 5.2.

taken during layout [38], such that the expected mismatch does not degrade SFDR too much.

5.2.6.3 Hysteresis

Hysteresis is present when the reset transistors do not fully discharge the parasitic capacitances of the Di and output nodes. The C_{Di} parasitic capacitances are both discharged in the compare phase and charged in the reset phase. Therefore there will be hardly any difference voltage at these nodes at the end of the compare phase, when the capacitances are not fully charged in the reset phase. So the contribution to hysteresis is considered negligible.

The output nodes have opposite voltages after the compare phase. When the capacitor is not fully discharged, one output node will have charge left at the start of the compare phase. Therefore the output node parasitic capacitances are dominant in determining the hysteresis. It is thus important that the load capacitance of the comparator is taken into account when hysteresis dependency is analyzed.

Investigation by simulation In reset the intermediate phase MOSFETs (M10, M11) will reset the output nodes. So the input phase reset transistors (M7, M8) must pull the Di nodes high fast enough such that the intermediate transistors pull the output nodes low fast enough. The minimal sized transistors appear to be sufficient for the comparator. Figure 5.10 shows the behavior of the comparator for very large common mode and little differential mode input signal. One clock period the input voltage difference is 200 mV and the next period it is only 1 mV. For this worst case input signal, the output nodes are reset properly. The difference voltage at the output nodes is smaller than $1uV$. The hysteresis effect is thus obscured by noise and assumed to be not of any influence.

5.2.6.4 Metastability

The problem of metastability for a comparator is that for very small input voltage differences, the output does not reach a valid logic output voltage in

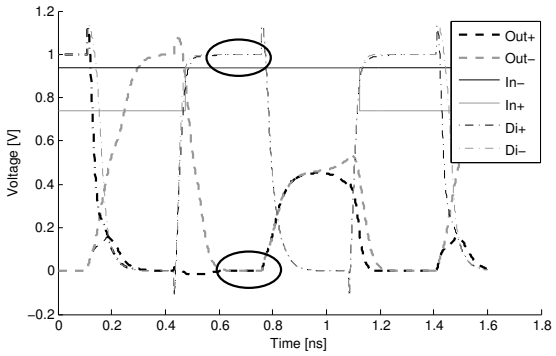

Figure 5.10: Static hysteresis is obscured by noise and not degrading the performance below toleration. The Di and output nodes are reset properly as indicated by the ellipses. The voltage difference is $< 1uV$ at the end of the reset stage.

the time available. The range in which the input signal does not lead to a valid logic output is referred to as the *dead-zone*.

When the comparator compares a difference voltage in the dead-zone, one of the differential output nodes will not reach a logic '1', because the latch is not able to pull one of the outputs high in the available time. The available time is half a sample clock period. When the input voltage difference is within the dead-zone, noise in the circuit will cause the logic signal to assume a valid value [13].

To have a logic output value, the differential output is converted to a single ended output. When the differential-to-single-ended block is not symmetrical, i.e. it tends to output more logic '1's than '0's when the input is in the dead-zone, an offset is created. So either the dead-zone must be small, or the differential-to-single-ended block must be very symmetrical.

Investigation by simulation In order to limit the dead-zone, it must be defined: in this case a dead-zone is defined as the range of the input signal difference for which either of the outputs is not at 80% of the expected output value. Thus, when the difference is a very small negative value in the dead zone, the negative output voltage is below 0.8 V.

The dead-zone of the comparator can be visualized by determining the offset when only looking at one of the differential outputs. The simulation flip-flop threshold is then set to 0.8 V.

Figure 5.11 shows the dead-zone of the input signal as a function of the common mode voltage. When the input voltage difference is greater than $30uV$ over the whole range, the comparator will produce a valid logic output value.

Also, the dead-zone will be obscured by noise. Because the σ of the noise may not exceed $0.7mV$, the dead-zone must be also less than $0.7mV$. As is clear from Figure 5.11, the comparator dead-zone is small enough.

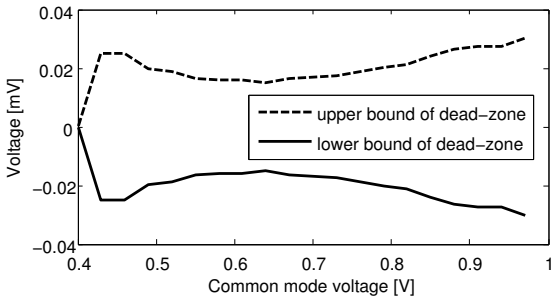

Figure 5.11: Dead-zone: range in which the comparator output is not between 0.2 and 0.8 of supply voltage of 1V.

5.2.6.5 Input voltage slope dependency

The voltage slope of the input signal will influence the performance of the comparator for two reasons:

- Parasitic capacitances of the input MOSFETs cause crosstalk between gate and drain.
- The Di node capacitances are discharged and as a result the input MOSFETs cycle through different operating regions. The non-linear transconductance of the input MOSFETs cause different integration results at the parasitic capacitances of the Di nodes for different signal slopes.

A countermeasure to dynamic hysteresis is placing a track-and-hold circuit before the comparator. An ideal track-and-hold holds the input to the comparator constant during the compare phase. The voltage slope is then zero and above effects are circumvented. Section 5.3.2 elaborates on track-and-hold circuits.

5.2.6.6 Clock feed-through

Because of the parasitic capacitances between the clocking MOSFETs, the steep edges of the clock signal will result in added voltages to internal nodes. Because of the differential nature of the comparator this will not degrade comparator performance. However, due to mismatch between M7 and M8, the clock feed-trough will lead to offsets.

Investigation by simulation The clock feed-trough is clearly seen in figure 5.10 and 5.3. The Di nodes and output nodes voltage rise above the positive supply voltage during the clock edges. The effect on offset is shown in Figure 5.9.

5.3 Simulation of multiple ADCs

The sources of distortion in the comparator are investigated in previous section. In this section the simulation results are presented of the ADCs in a zero-IF front-end. Because of extremely long simulation time, the performance of the

ADC is evaluated for a single sine wave as input up to a SFDR of 58 dB. The output is directly Fourier transformed without cross-correlation or spectral averaging. When cross-correlation and spectral averaging are included in the simulation, a measurement time of 0.2 seconds would take more than a year to simulate with the settings used and the simulation hardware available.

5.3.1 Simulation set up

The circuit level simulation in spectre are the analog equivalent of the system level simulations. To focus on the comparator, the decision level DACs and dither DACs are omitted and the low pass filter and integrator are constructed from ideal analog components. Figure 5.12 shows the analog implementation of the decision level loop in spectre. The performance of the loop is equal to the system level design in MATLAB when an ideal comparator was used, this is verified by simulation.

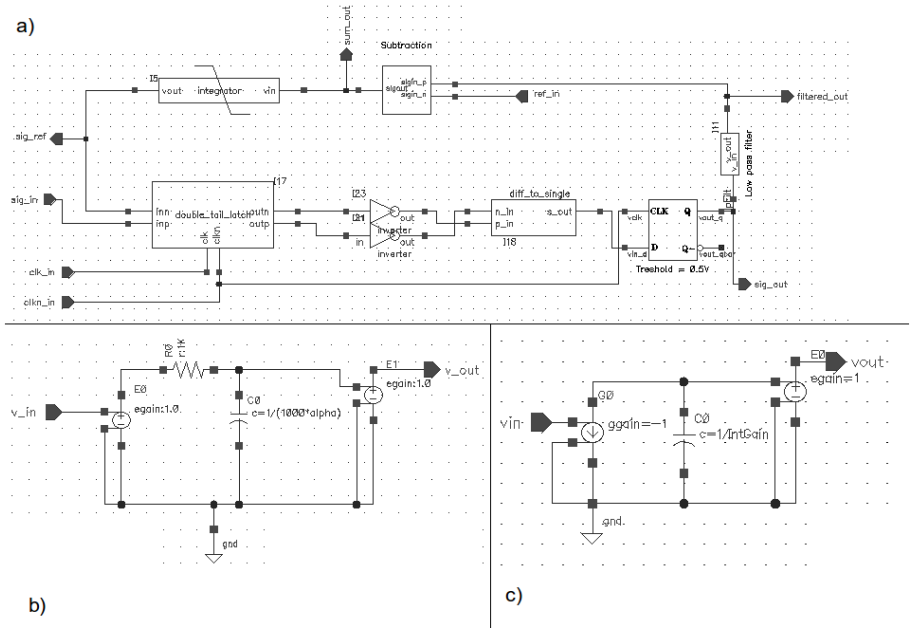

Figure 5.12: a) Single decision level loop. b) Ideal low pass filter. c) Ideal analog integrator

For the simulation a complex sine wave is generated by MATLAB. Also four statistically independent dither signals are generated with maximum amplitude of 0.5. The results of the simulation are processed in MATLAB after the simulation.

5.3.2 Spectra

In the following paragraphs, the resulting spectra are shown when different track and hold circuits are used. First an ideal track and hold is used, to show how well the comparator performs when the voltage slope effects are reduced.

The then spectra is shown for when no track and hold circuit is used to show what the effects are. The simplest form of a track and hold is then implemented to see how much this improves the ADC.

Because of long measurement times, the measurement is stopped when it become visible that the SFDR was limited, thus the noise floor in the spectra are not below 62.5 dBFs.

First a spectrum is obtained when the signal is directly connected to the ADC. The SFDR appears to be limited to 46.5 dB. Then an ideal track and hold is placed before each ADC. The SFDR is then increased to 54.14 dB, but still not the target SFDR of 60 dB.

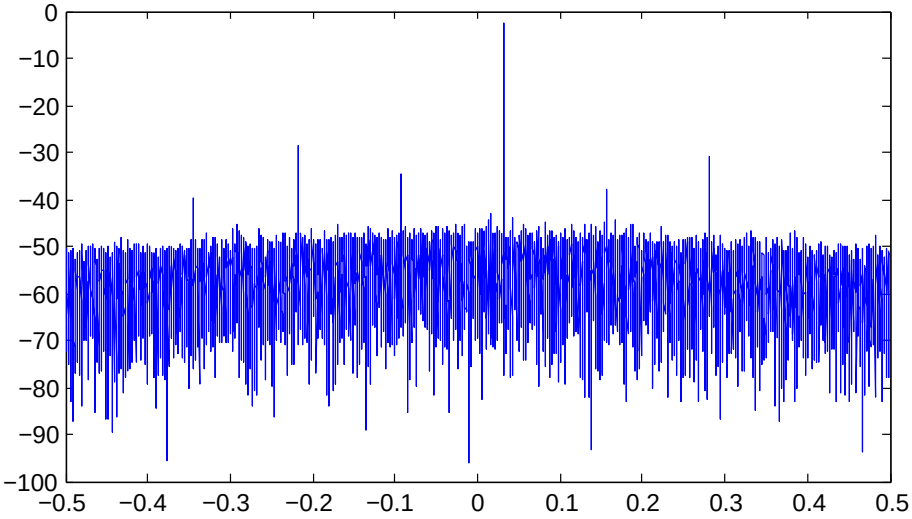

Figure 5.13: Spectrum when no track and hold is used.

No track and hold Strength of distortion components seriously increase when to track and hold is used. Figure 5.13 shows the resulting spectrum. This confirms that the performance of a comparator depends on the voltage slope of the input signal. The conclusion is that the comparator still has non-linear behavior which degrades the SFDR. The approach to optimize the comparator for this SFDR is too optimistic and must be revisited. Because of time constraints, this work is listen as recommendation in Chapter 6.

Ideal sample and hold When the ideal sample and hold is used, the resulting spectrum is expected to have a SFDR of at least 60 dB. The resulting spectrum however shows that the SFDR is not achieved. A spurious peak is present of 56.74 dB which limits the SFDR to 54.14 dB. Figure 5.14 shows the spectrum in case of the ideal sample and hold.

5.4 Power consumption

The power consumption of the CDF based AGC ADC is estimated and compared to the power consumption estimation of a 8-bit ADC. Also for both the

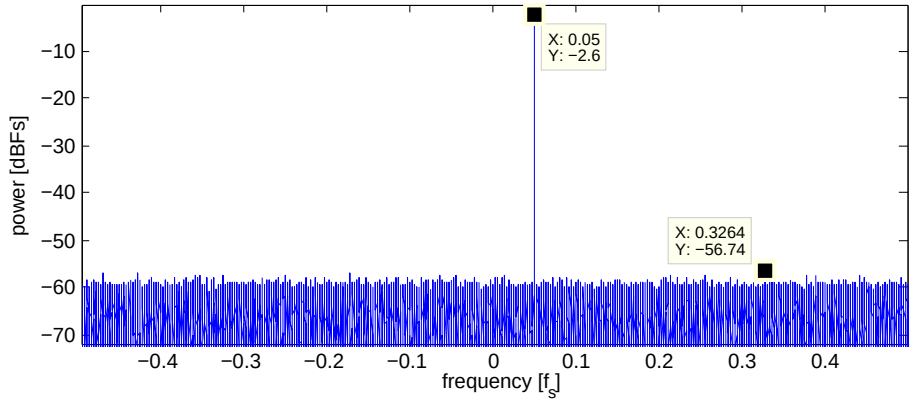

Figure 5.14: Ideal sample and hold

XF and XF correlators a coarse power consumption estimate is calculated in order to draw a conclusion on the efficiency of a cross-correlation spectrum analyzer with CDF-based AGC ADCs.

The energy consumption depends on the measurement time of both ADCs. Because for the CDF based AGC ADC the noise floor is expected to be dominated by quantization noise and dither noise, 0.2 seconds is needed to obtain a spectrum estimate with a SFDR of about 60 dB. For an 8-bit ADC the noise floor is determined by the analog front-end components, which determines the required measurement time.

5.4.1 This design

Comparator Circuit level simulations show that the power consumption per comparator, at a frequency of 1.536 MHz, 1 volt supply voltage in a 90 nm process is:

$$E = 58fJ/conversion \tag{5.1}$$

Per ADC the comparators consume:

$$P = 58 \cdot 10^{-15} \cdot 3 \cdot 1.536 \cdot 10^{9} = 265\mu W \tag{5.2}$$

DACs The power consumption of the DACs is very coarsely estimated by linearly scaling the power consumption of DACs from literature to the sample frequency, resolution and to process size and scaling quadratically to supply voltage [13]:

$$P_{Dither\ DAC} = P \cdot \frac{1.536}{f} \cdot \left(\frac{0.09}{p}\right) \cdot \left(\frac{1.0}{v}\right)^2 \tag{5.3}$$

$$P_{Decision\ level\ DAC} = P \cdot \frac{0.003}{f} \cdot \left(\frac{0.09}{p}\right) \cdot 2^{8-6} \cdot \left(\frac{1.0}{v}\right)^2 \tag{5.4}$$

where f, p and v are the reference design sample frequency in GHz, process resolution in μm and process voltage in volt respectively.

Table 5.3 shows the DACs from literature with scaled power consumption. From this data the power consumption of the dither DAC is approximated to be 2 mW and the decision level DAC is 0.2 mW.

Ref.	Resolution	sample rate	Power	process	year	scaled power (f = 3 MHz, f = 1536 MHz)
[31]	6 Bits	1.25 GHz	6 mW	1.8 V, 0.18 um	2008	0.009, 1.14
[32]	6 Bits	2.7 GHz	28 mW	1.2V, 0.13 um	2006	0.060, 7.66
[33]	6 Bits	5.4 GHz	20 mW	1.5V, 0.13 um	2005	0.014, 1.75
[34]	6 Bits	1 GHz	7.5 mW	1.5 V,0.13 um	2005	0.028, 3.54

Table 5.3: CMOS DAC characteristics from literature.

Total ADC power consumption A total ADC contains 1 dither DAC, 3 decision level DACs and three comparators. Such an ADC would consume approximately:

$$2 \cdot 10^{-3} + 3 \cdot (265 + 0.2) \cdot 10^{-6} = 2.77mW \tag{5.5}$$

5.4.2 Reference ADC

ADC A high resolution ADC yielding an SFDR of 60 dB must have 8 bits (Equation 3.2). The power consumption of an 8 bit ADC with a sample frequency of 1536 MHz is estimated by comparison to ADC from literature. To find an approximate power consumption of a 8-bit ADC with a sample frequency of 1536 MHz, the power numbers are scaled to frequency (based on [13] and [39]):

$$P_{ADC} = P \cdot \frac{1.536}{f} \cdot \left(\frac{0.09}{p}\right) \cdot 2^{8-b} \cdot \left(\frac{1.0}{v}\right)^2 \tag{5.6}$$

Table 5.4 shows three reference ADCs and the scaled power consumption. Based on these scaled powers, the power consumption of an 8-bit ADC is estimated to be at least 200 mW.

Ref.	Resolution	Sample rate	Power	Process	Year	Scaled power
[40]	6 Bits	1.6 GHz	350 mW	1.8 V, 0.18 um	2006	207 mW
[41]	8 Bits	0.25 GHz	150 mW	1.8 V, 0.18 um	2004	142 mW
[42]	8 Bits	1.25 GHz	207 mW	1.0 V, 0.09 um	2008	254 mW

Table 5.4: CMOS ADC specifications from literature.

5.4.2.1 Correlator power consumption

XF correlator To find an approximate power consumption of the XF correlator, the implementation data and approach of [5] is used. The dynamic power consumption of the XF correlator dominates the overall power consumption. The approach scales the power consumption of two implementations with

different dimensions. The difference between the two implementations is the number of correlator stages. The two implementations operate at 100 MHz, have a resolution of 8 bits and 257 or 7 correlation stages.

The XF correlator in this design operates at 1536 MHz, has a resolution of 2 bits and requires 257 correlation stages. The estimated power consumption then is (a term is added for different voltage supply, with respect to [5]):

$$P_{dyn,1} \approx 0.108 \cdot \frac{1536}{100} \cdot \left(\frac{2}{10}\right)^2 \cdot \frac{257}{257} \cdot \left(\frac{1.0}{1.2}\right)^2 = 0.072[W] \tag{5.7}$$

$$P_{dyn,2} \approx 0.0024 \cdot \frac{1536}{100} \cdot \left(\frac{2}{10}\right)^2 \cdot \frac{257}{7} \left(\frac{1.0}{1.2}\right)^2 = 0.058[W] \tag{5.8}$$

Thus averaged the approximate power consumption is:

$$P = \frac{P_{dyn,1} + P_{dyn,2}}{2} \approx 65[mW] \tag{5.9}$$

FX Correlator As concluded in [5], the power consumption of an FX correlator is a factor 13 lower than that of an XF correlator. Thus to approximate the power consumption of the FX correlator, Equation 5.7 (from [5]) is adjusted:

$$P_{dyn,1} \approx \frac{0.108}{13} \cdot \frac{1536}{100} \cdot \left(\frac{8}{8}\right)^2 \cdot \frac{257}{257} \cdot \left(\frac{1.0}{1.2}\right)^2 = 0.0882[W] \tag{5.10}$$

$$P_{dyn,2} \approx \frac{0.0024}{13} \cdot \frac{1536}{100} \cdot \left(\frac{8}{8}\right)^2 \cdot \frac{255}{7} \cdot \left(\frac{1.0}{1.2}\right)^2 = 0.0715[W] \tag{5.11}$$

Averaged, the approximate power consumption is:

$$P = \frac{P_{dyn,1} + P_{dyn,2}}{2} \approx 80[mW] \tag{5.12}$$

5.4.3 Energy consumption

Per ADC solution, the measurement time defines the energy consumed per spectrum estimate. The estimated power consumption of the CDF-based AGC ADC is rougly 70 times less, thus it can measure 70 times longer than the 8-bit ADC to consume the same amount of energy. However, the correlator following the ADC also consumes a substantial amount of energy. Thus for equal energy consumption, the measurement time of the CDF-based AGC ADC is about eight times longer. The dither and quantization noise floor can thus be lowered by 4.5 dB Equation 4.22), achieving a SFDR of approximately 37 dB (see Table 4.6). An 8-bit ADC is assumed to achieve a much higher SFDR in one measurement.

This indicates that the CDF based AGC ADC it is less energy efficient than an undithered high-resolution ADC.

5.5 Summary and conclusion

Summary In this section the double tail voltage sense amplifier is introduced. This comparator is implemented in the UMC090 process. The expected non ideal properties of the comparator are described. Offset, hysteresis,

metastability and clock feed-through are investigated by simulation. It has been verified per non ideal property that the comparator does not introduce an unacceptable amount of distortion due to these properties. The second part of this chapter presents quadrature ADC simulation results. Because of long simulation times, the SFDR is limited by the noise floor to 58 dB. The correctness of the simulation set up is verified by simulation with ideal comparators. The results of simulations of two quadrature connected ADCs with implemented comparators with and without an ideal track and hold circuit are presented. The track and hold circuits are added to reduce the input voltage slope dependency of the comparator, i.e. to idealize the sample function. A coarse estimation of the power consumption of the CDF-based AGC ADC is made and compared to the estimated power consumption of a 8-bit ADC. Because of relative long measurement time of the CDF-based AGC ADC it is less energy efficient than a solution with high-resolution ADC.

Conclusions Different non-ideal properties are investigated, but the non-linearity of the comparator is dominated by voltage slope dependency. An effective solution is adding a track-and-hold circuit. Still the SFDR of the ADC is limited by the comparator. Offset, hysteresis, metastability or other non-ideal properties cause this performance limit. The approach presented in this chapter is not sufficient for dimensioning the comparator such that the dithered CDF-based AGC ADC results in the target SFDR of 60 dB. More research is required to determine the source of the performance degradation. Based on power consumption estimations, using the CDF-based AGC ADC for spectrum estimation is less efficient than using high resolution ADCs.

Chapter 6

Summary and Conclusions

For integration of an energy detection cross-correlation spectrum analyzer for the use in cognitive radio, a low cost ADC solution is investigated. In radio astronomy, cross-correlation is a technique exploited intensively, often together with low-resolution AD conversion.

In this thesis an ADC concept from radio astronomy is explored for the use in cognitive radio application. The concept is referred to as the CDF-based AGC ADC, because it contains Automatic Gain Control (AGC) by adjusting ADC decision levels based on estimates of the input signal Cumulative Distribution Function (CDF).

6.1 Summary

The work carried out is summarized by addressing the subquestion of this thesis. The subquestions for this thesis are:

1. How does the performance of a spectrum analyzer depend on the resolution of its ADCs?
2. Is a CDF-based AGC ADC suitable as a low resolution ADC in cross-correlation spectrum analyzer for cognitive radio?
3. What is at circuit level the critical analog component in the CDF-based AGC ADC and how does system performance depend on circuit level behavior?
4. What performance is achievable and what are the costs?

Reflection on sub questions

1. *How does the spectrum analyzer performance depend on the ADC resolution?*
   When distortion components dominate the SFDR of the spectrum analyzer, the SFDR reduces by approximately 8 dB per reduced bit [17]:

   $$SFDR \approx 8.07 \cdot D + 3.29$$

   Where D is the number of bits of the quantizer. When digital dither is applied in a cross-correlation spectrum analyzer and the dither signal

fulfills the requirements of rectangular dither (Section 3.3), the reduction of distortion components is expressed by Equation 3.45, which is:

$$SFDR \approx 8.07 \cdot \log_2\left((2^D - 1) \cdot M + 1\right) + 3.29$$

Where M is the number of dither values. Thus the SFDR of a spectrum analyzer can be reduced when the ADC resolution is reduced, but this is compensated to certain extent when dither is added.

As a tool to address performance and non-linearity issues of a digitally dithered quantizer, the rectangular PDF dithered equivalent quantizer concept is introduced in Section 3.3.2.2. This concept provides insight in the performance dependencies of rectangular PDF digitally dithered quantizers. For triangular PDF dither similar relations can be found. This is partially done, but the correctness was not fully verified due to time limitation. This work can be found in appendix B.4,

When noise dominates the SFDR, possibly due to dither and quantization noise, cross-correlation can be utilized to lower the noise floor and increase SFDR (see section 4.3). This utilization of cross-correlation is an effective solution to SFDR limitations when using dithered quantizers.

The use of rectangular PDF dither results in variation in the noise floor, which is minimized by the AGC and offset canceling. In the case of triangular PDF the noise floor does not vary, but it is in any case higher or equal to the noise floor when rectangular PDF dither is used.

2. *Is a CDF-based AGC ADC suitable as a low resolution ADC in cross-correlation spectrum analyzer for cognitive radio?*
The performance of the CDF-based AGC ADC depends on the input signal (Section 4.4.8). Therefore, the CDF-based AGC ADC is not very suitable as a low resolution ADC in a cross-correlation spectrum analyzer for cognitive radio. An energy detection spectrum analyzer must correctly sense the spectrum regardless of the type of input signal. How much the performance is degraded in practical situations requires more research.

   When the resolution of the ADCs for a cognitive radio spectrum analyzer is lowered, several problems are introduced. The CDF-based AGC ADC tackles those problems, but other problems are introduced.

   Problems

   a) Resolution reduction increases distortion components
   b) Dithering raises the noise floor
   c) Signal clipping introduces distortion components
   d) Highest SFDR is achieved when signal specific settings are used
   e) A signal with a non-symmetrical PDF results in non-uniform quantization
   f) Assumption on symmetry of PDF is questionable

   The problem of increased distortion components is reduced by applying proper dither and utilizing the cross-correlation concept. Signal clipping

must be avoided or limited such that the intended SFDR is achieved. The CDF-based AGC ADC solves this problem by the AGC and offset canceling. These features are realized by adjustable ADC decision levels based on the CDF estimate of the input signal (section 4.4.2). However, this approach introduces new problems. Maximal performance is achieved when optimal system settings are applied. Optimal system settings differ per type of input signal. Because the energy detection spectrum analyzer has no knowledge on the input signal, only the most conservative settings can be used, which result in less SFDR.

An assumption is made that the PDF of an input signal is symmetrical, but the estimate of a symmetrical PDF can be non-symmetrical. Also, the assumption may be non-realistic, as the PDF of a sum of a few strong sinusoids can be non-symmetrical (Section 4.4.8).

Dithering and cross-correlation utilization is an effective way to increase SFDR of a low resolution quantizer. In case of non-white spectra, it should be applied to 2-bit ADCs with other AGC mechanisms, such as a signal power-based AGC ADC (for instance as in [7]).

3. *What is at circuit level the critical analog component in the CDF-based AGC ADC and how does system performance depend on circuit level behavior?*
The comparator is considered the critical component at circuit level. DAC implementations with required specifications exist and are found in literature (Chapter 5). A comparator is implemented at circuit level in a 90 nm technology. The non-linearity of the comparator is dominated by voltage slope dependency (or referred to as $\frac{dV}{dt}$ dependency). An effective solution is adding a track-and-hold circuit. Still the SFDR of the ADC is limited by the comparator. Offset, hysteresis, metastability or other non-ideal properties cause this performance limit (Section 5.1). More research is required to determine the exact source of the performance degradation.

4. *What performance is achievable and what are the costs?*

Performance Theoretically a SFDR of 62.7 dB can be achieved for a resolution bandwidth of 6 MHz, sampling at 1536 MHz and measuring for 0.2 seconds (Section 4.3). Simulations show that a SFDR of 60.1 is achieved, which is lower than the theoretical value because of noise uncertainty due to limited measurement time (Section 4.5). However, these numbers are based on system settings which require knowledge on the input signal and can therefore not be used in practice. When practical relevant settings are used the SFDR is reduced by 5.2 dB (Section 4.5). After circuit level integration of the comparators the achievable SFDR with optimal system settings is reduced to 54.14 dB (Section 5.3.2). For practical relevant settings SFDR is reduced more. Because of limited time, the comparator is not fully optimized on circuit level and a track-and-hold circuit still must be designed.

Power consumption In Section 5.4 a coarse estimation is made on the expected power consumption of the CDF-based AGC ADC operating at 1536 MHz. The estimation is based on scaled performance of DACs found in literature. This estimation indicates that a large part of the power is consumed by the dither DAC. Incorporating a low-power DAC is subject to future research. The power consumption estimation of the CDF-based AGC ADC is compared to a power consumption estimation of an 8-bit ADC, based on scaled performance of ADCs found in literature. Because of the long measurement time of the CDF-based AGC ADC and because of the relative high expected power consumption of the dither DAC, it is more power efficient to use a higher resolution ADC.

6.2 Conclusions

The research question for this thesis was:

- *Is a low resolution ADC suitable for the use in a cross-correlation spectrum analyzer for cognitive radio?*

With respect to the research question, the following is concluded:

1. Low-resolution quantization is not very suitable for an energy-detection cross-correlation spectrum analyzer. In order to achieve reasonable SFDR, a high speed DAC is required because of the PDF requirements of the dither signal. The power consumption of this DAC, in combination with long measurement time leads to large energy consumption per spectrum estimation.

With respect to the work carried out in general, the following is concluded:

2 The CDF-based automatic gain control and offset canceling mechanism is not very suitable for a spectrum analyzer for cognitive radio. The performance of the CDF-based AGC ADC depends on the type of input signal and an energy detection spectrum analyzer does not have knowledge on the input signal. The performance which is aimed at cannot be guaranteed.

3 When the input signal is digitized by a low resolution ADC, dithering must be applied in the case of cognitive radio. In order to achieve reasonable SFDR with a low-resolution ADC, digitally dithering the input signal and utilizing cross-correlation is effective.

4 The equivalent quantizer concept is an effective tool to investigate the performance of digitally dithered quantizers.

5 When AGC is realized by adjusting the ADC's decision levels, the ADC can be properly dithered by scaling the dither amplitude to the decision levels.

6.3 Recommendations

For the analysis and implementation of the CDF-based AGC ADC choices are made to limit the time-span of the work. When the remaining alternatives are worked out, this may introduce new insights or better performing ADCs. Also some performance dependencies are not investigated thoroughly, because of time limitation. More research on this topics may lead to better characterization of the ADC concept.

Recommended research is listed as research questions for future work:

1. What is the performance limitation of the noise uncertainty introduced by using rectangular PDF dither. When does the noise certainty of triangular dither lead to a higher performance.

2. How does the performance of the ADC depend on decision level errors when triangular PDF dither is used. For this thesis this is only worked out for rectangular PDF dither.

3. Can the decision level loop of the CDF-based AGC ADC become unstable. What is the dependency of loop stability on system parameters.

4. To what extend is the input signal dependency of the CDF-based AGC ADC a problem when used in a cognitive radio energy detection spectrum analyzer. And how does the dependency relate to oversampling?

5. What is the expected power consumption of the CDF-based AGC ADC, when all analog components are worked out at circuit level. And what will the contribution of the digital processing.

6. What dominates the performance degradation in the comparator, when voltage slope dependency is excluded by applying an ideal track-and-hold?

7. What track-and-hold circuit is required to reduce voltage slope dependency of the comparators to acceptable levels.

8. What is the effect of noise in the comparator and how does it relate to settings of the CDF-based AGC ADC.

Appendix A

Quantization error in frequency domain

This chapter gives the mathematical derivation of distortion component strength for a uniform midrise quantizer, based on Blachmans derivation [19] for a midtread and midrise quantizer.

A.1 Midrise quantizer

- the quantizer starcase function now is described by:

$$y(t) = x + \sum_{n=1}^{\infty} \frac{1}{\pi n} sin(2n\pi x) \tag{A.1}$$

$$= x + im\{\sum_{n=1}^{\infty} \frac{1}{\pi n} e^{2n\pi x}\} \tag{A.2}$$

- The Jacobi-Anger expansion is used:

$$e^{i \cdot z \cdot sin\theta} = \sum_{p=-\infty}^{\infty} J_p(z) e^{i\ p\ \theta} \tag{A.3}$$

- the spectral components of the error are:

$$q(t) = im\{\sum_{n=1}^{\infty} \frac{1}{\pi n} \left(\sum_{p=-\infty}^{\infty} J_p(2\pi \cdot n \cdot A) e^{i \cdot p \cdot \theta(t)}) \right)\} \tag{A.4}$$

- Because the quantization staircase is odd, only odd harmonics are present, so p is odd. Also negative and positive harmonics are added, such that when rewriting the equation:

$$q(t) = \sum_{p=1,3,5,\ldots}^{\infty} \left(\sum_{n=1}^{\infty} \frac{1}{\pi n} J_p(2\pi \cdot n \cdot A) sin(p \cdot \theta(t)) \right) \tag{A.5}$$

A.2 Midtread quantizer

- the quantizer starcase function now is described by:

$$y(t) = x + \sum_{n=1}^{\infty} \frac{(-1)^n}{\pi n} sin(2n\pi x) \tag{A.6}$$

$$= x + im\{\sum_{n=1}^{\infty} \frac{(-1^n)}{\pi n} e^{2n\pi x}\} \tag{A.7}$$

- The Jacobi-Anger expansion is used:

$$e^{i \cdot z \cdot sin\theta} = \sum_{p=-\infty}^{\infty} J_p(z) e^{i\ p\ \theta} \tag{A.8}$$

- the spectral components of the error are:

$$q(t) = im\{\sum_{n=1}^{\infty} \frac{(-1)^n}{\pi n} \left(\sum_{p=-\infty}^{\infty} J_p(2\pi \cdot n \cdot A) e^{i \cdot p \cdot \theta(t)}) \right)\} \tag{A.9}$$

- Because the quantization staircase is odd, only odd harmonics are present, so p is odd. Also negative and positive harmonics are added, such that when rewriting the equation:

$$q(t) = \sum_{p=1,3,5,\ldots}^{\infty} \left(\sum_{n=1}^{\infty} \frac{(-1)^n}{\pi n} J_p(2\pi \cdot n \cdot A) sin(p \cdot \theta(t)) \right) \tag{A.10}$$

Appendix B

Dither

B.1 Characteristic function

Via the characteristic function statistical properties of a signal can be obtained easily. The characteristic function for a probability distribution of variable z is the expected value of the function $e^{j\omega z}$ and is denoted by $P(\omega)$. ω can have any real value.

$$P(\omega) = E(e^{j\omega z}) = \int_{-\infty}^{\infty} p_z e^{j\omega z} dz \tag{B.1}$$

The characteristic function is the inverse Fourier transform of the probability distribution of z, all properties of ordinary Fourier transforms are also valid.

Although the physical meaning of the characteristic function may not be evident, it is very useful in deriving properties of stochastic processes. The characteristic function allows to get the moments of the stochastic variable. The derivatives of the characteristic function:

$$\frac{dP(\omega)}{d\omega} = \int_{-\infty}^{\infty} (jz) e^{j\omega z} p(z) dz \tag{B.2}$$

The derivative of $P(\omega)$ is easily obtained by deriving $e^{j\omega z}$ expressed as its series expansion. After the m^{th} derivation for $\omega = 0$, the m^{th} order moment appears:

$$P(\omega) = E(e^{j\omega z}) \tag{B.3}$$

$$= E(1 + j\omega z + \frac{-1 \cdot \omega^2 z^2}{2!} + \frac{-j \cdot \omega^3 z^3}{3!}) \tag{B.4}$$

$$\tag{B.5}$$

Then taking the m^{th} derivative:

$$\frac{d^m P(\omega)}{d^m \omega} = E\left(\frac{d^m}{d^m \omega}(1 + j\omega z + \frac{-1 \cdot \omega^2 z^2}{2!} + \frac{-j \cdot \omega^3 z^3}{3!})\right) \tag{B.6}$$

$$= E(z^m) \tag{B.7}$$

And thus for differentiating $P(\omega)$ k times, the moment k can be obtained by taking the absolute value of $P(\omega)$ for $\omega = 0$

When $\omega = 0$, $\frac{dP(\omega)}{d\omega} = jE(z)$. For higher derivatives this gives higher moments. in General:

$$\frac{d^n P(\omega)}{d\omega^n} = j^n E(z^n) \tag{B.8}$$

B.2 Total error moment dependence on input signal

In this section the following variables are used:

- x: input signal
- v: dither signal
- w: quantizer input
- y: output signal
- ϵ Total error $(y - x)$

B.2.1 Properties of the total error

B.2.1.1 Conditional PDF of ϵ

The dependence of the total error on the system input can be analyzed in terms of its PDF as a function of a specified input value, this function is referred to as the conditional PDF:

$$p_{w|x}(w, x) = p_v(w - x) \tag{B.9}$$

Where $p_{w|x}(w, x)$ is the probability that the input to the quantizer is w when the input to the system is x. Because $w = x + v$ this is equal to the probability $p_v(v) = p_v(w - x)$. For a given value of x, the PDF of ϵ is a series of delta functions, because the error is equal to $-x + k \cdot \Delta$ where k is an integer and represent all the quantization values. The conditional PDF of $\epsilon|x$ is:

$$p_{\epsilon|x}(\epsilon, x) = \sum_{k=-\infty}^{\infty} \delta(\epsilon + x - \frac{\Delta}{2} - k\Delta) \cdot \int_{k\Delta}^{k\Delta+\Delta} p_v(w - x)dw \tag{B.10}$$

This relation is illustrated in Figure B.1. In this figure an arbitrary PDF of v is centered around the value of x. The area per quantization value is integrated and represented by a dirac pulse at the value of the corresponding total error values ϵ.

B.2.1.2 Unconditional PDF of ϵ

The integral in function B.10 can be written as the product of a dirac pulse and a convolution of $p_v(w - x)$ and a shifted rectangular function $\Delta\Pi_\Delta$.

$$\delta(\epsilon + x - \frac{\Delta}{2} - k\Delta) \cdot \int_{k\Delta}^{k\Delta+\Delta} p_v(\epsilon)dw = \delta(\epsilon + x - \frac{\Delta}{2} - k\Delta) \cdot [\Delta\Pi_\Delta * p_v](\epsilon) \tag{B.11}$$

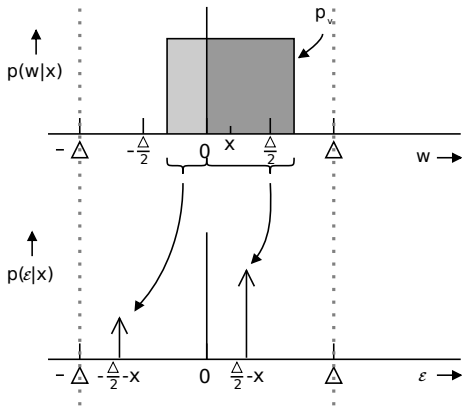

Figure B.1: Illustration of obtaining $p_{\epsilon|x}(\epsilon, x)$ from $p_v(w - x)$

this gives for $p_{e|x}(e, x)$:

$$p_{\epsilon|x}(\epsilon, x) = [\Delta \cdot \Pi_\Delta * p_v](\epsilon) W_\Delta(\epsilon + x) \tag{B.12}$$

where

$$W_\Delta(\epsilon) \triangleq \sum_{k=-\infty}^{\infty} \delta(\epsilon - k\Delta - \frac{\Delta}{2})$$

Given the value of x, the PDF of ϵ is a series of dirac pulses: because x is known the possible error values are known. When x is unknown, the possible error values are unknown. Obtaining the conditional PDF of e from the unconditional PDF of e is integrating the product of $p_{\epsilon|x}$ and p_x:

$$\begin{aligned} p_\epsilon(\epsilon) &= \int_{-\infty}^{\infty} p_{\epsilon|x}(\epsilon, x) p_x(x) dx && \text{(B.13)} \\ &= \int_{-\infty}^{\infty} ([\Delta \cdot \Pi_\Delta * p_v](\epsilon) W_\Delta(\epsilon + x)) \cdot p_x(x) dx && \text{(B.14)} \\ &= ([\Delta \cdot \Pi_\Delta * p_v](\epsilon)) \int_{-\infty}^{\infty} W_\Delta(\epsilon + x) \cdot p_x(x) dx && \text{(B.15)} \\ &= [\Delta \Pi_\Delta * p_v](\epsilon) [W_\Delta * p_x](-\epsilon) && \text{(B.16)} \end{aligned}$$

Characteristic function of ϵ The Fourier transform of a rectangle is a sinc function. The width of the rectangle Δ is inversely proportional to the frequency axis scaling of the *sinc* function.

The characteristic function of the total error is obtained by Fourier transforming the PDF of the total error :

$$\begin{aligned} P_\epsilon(u) &= [sinc(u) P_v(u)] * [\mathcal{F}(W_\Delta) \cdot P_x(-u)] && \text{(B.17)} \\ & && \text{(B.18)} \end{aligned}$$

The series of dirac pulses results is known as a *dirac-comb* and has the property that its fourier transform is again a dirac-comb:

$$\mathcal{F}(\sum_{k=-\infty}^{\infty}\delta(\epsilon - k\Delta - \frac{\Delta}{2})) = \frac{1}{\Delta}\sum_{k=-\infty}^{\infty}\delta(u - \frac{k}{\Delta})\cdot e^{-i\cdot\frac{\Delta}{2}u} \tag{B.19}$$

The the convolution of equation B.17 becomes:

$$P_\epsilon(u) = [sinc(u)P_v(u)] * [\frac{1}{\Delta}\sum_{k=-\infty}^{\infty}\delta(u - \frac{k}{\Delta})P_x(-u)e^{-i\frac{\Delta}{2}u}] \tag{B.20}$$

$$= \sum_{k=-\infty}^{\infty}\frac{1}{\Delta}[sinc(u)P_v(u)] * [\delta(u - \frac{k}{\Delta})P_x(-u)e^{-i\frac{\Delta}{2}u}] \tag{B.21}$$

The second argument of the convolution is a series of dirac pulses and thus the convolution becomes a sum of products:

$$P_\epsilon(u) = \sum_{k=-\infty}^{\infty}\frac{1}{\Delta}sinc(u - \frac{k}{\Delta})P_v(u - \frac{k}{\Delta})\cdot e^{-i\frac{\Delta}{2}\frac{k}{\Delta}}P_x(-\frac{k}{\Delta}) \tag{B.22}$$

Condition for independent moments The derivation of conditions for independent moments is found in [18]. The description in this section is more elaborate and illustrated. In Equation B.22 only P_v can be chosen. In [18] a condition for independence of moments is given. For this condition the a part of Equation B.22 si denoted by $G_v(u)$:

$$G_v(u) \triangleq sinc(u)P_v(u) \tag{B.23}$$

Then the m^th moment is independent of x when:

$$G_v^{(m)}\left(\frac{k}{\Delta}\right) = 0 \forall k \in Z_0 \tag{B.24}$$

If this condition is satisfied for the first and second moment, the total error depend on the moments of the dither signal:

$$E[\epsilon] = E[v] \tag{B.25}$$

$$E[\epsilon^2] = E[v^2] + \frac{\Delta^2}{12} \tag{B.26}$$

where $\frac{\Delta^2}{12}$ is the quantization error power.

B.3 Decision level variation

B.3.1 Error function integration intervals.

This section describes the integration intervals to calculate the error funcion of a equivalent quantizer (EQ) and a decision level error adjusted equivalent quantizer (EQ_e). The error is:

$$e_{EQ_e}(x) = EQ(x) - EQ_e(x) \tag{B.27}$$

The frequency components of $e_{EQ_e}(x)$ when $x = \frac{3\Delta}{2} sin(2\pi \cdot t)$ determine the degradation ion SFDR for a 2-bit quantized full-scale rectangular PDF dithered sine wave.

In this derivation only an increase in the lower decision level of a 2-bit ADC is considered. This number of decision levels of the equivalent quantizer affected by this error is $\frac{1}{3}$ of $3 \cdot M$.

The integration intervals starts at the decision level of EQ and stops at the decision level of EQ_e or vice versa (depending on the quadrant of the sine wave it applies to). The number of integration thus is $2M$.

In this derivation M is even and the quantizer is of type midrise, the resulting equivalent quantizer is of type midtread.

Because the input signal is a sine wave, the integration ranges are found by determining the signal values related to the decision levels. The phase is obtained by applying the arcsin operation and gives the integration ranges.

An LSB of the equivalent quantizer is:

$$\Delta_{EQ} = \frac{\Delta_{2-bit}}{2^M} \tag{B.28}$$

d denotes the equivalent quantizer decision levels affected. c is positive for decision levels above zero and negative for decision levels below zero. Thus the decision levels affected are defined by: $c = [-\frac{2^M}{2}, -\frac{2^M}{2} - 1, ... - (\frac{3 \cdot 2^M}{2} + 1)]$. Relative to full scale the decision levels are located at:

$$b_{FS}(c, M) = -\frac{c \cdot \Delta_{2-bit}}{2^M} \tag{B.29}$$

The decision levels are scaled to unitary scale in order to apply the arcsin operation. Because the amplitude of a sine wave is half full scale and the sine wave amplitude is $\frac{3}{4}$:

$$b(c, M) = \frac{c \cdot \Delta_{2-bit}}{2^M} \cdot \frac{8}{3} \tag{B.30}$$

The error of a 2-bit quantizer is denoted by α:

$$e_{declevel} = declevel_{EQ_e} - \alpha \cdot declevel_{EQ} \tag{B.31}$$

The shift of decision levels of EQ_e relates to the error (α) of 2-bit quantizer decision level as:

$$(1 - \alpha) \cdot \Delta_{2-bit} \tag{B.32}$$

And thus the integration range is :

$$e_{EQ}(x) = \begin{cases} 1 & \text{if } [b(c, M)] > x > [b(c, M) + (1 - \alpha)\Delta_{2-bit}], \quad \forall c \in \{1, 2, .., 2^D\} \\ 0, & \text{otherwise} \end{cases} \tag{B.33}$$

In this expression $b(c, M)$ is decision level c and $(1 - \alpha)\Delta$ is the shift of this decision level due to the error in the 2-bit quantizer decision level.

B.4 Triangular dither equivlent quantizer

This section discribes the approach of section 3.3.2.2 applied to triangular dither. Because of time constraints the correctness of the approach cannot be guaranteed, although it certainly points to the right direction.

For triangular PDF dither, v_d is now:

$$v_d(x) = \sum_{c=0}^{M-1} \frac{2}{M} \cdot \left(1 - |\frac{2c}{M}|\right) \cdot \delta \left(x - (-\Delta + \frac{\Delta}{M} + \frac{2 \cdot c \cdot \Delta}{M})\right) \tag{B.34}$$

When v_d is convoluted, the resulting decision level distribution is only valid for the range of the input signal where no clipping occurs. This means that some decision levels resulting from the convolution are not part of the set of decision levels.

$$d_{E(y)} = \begin{cases} v_d * d_{2-bit}, & \text{when } -\Delta < E(y) < \Delta \ \} \\ 0, \text{ otherwise} \end{cases} \tag{B.35}$$

This is illustrated in Figure B.2. The number of decision levels are:

$$(2^D - 2) \cdot M \tag{B.36}$$

and the number of possible values of $E(y)$ is:

$$\#E(y) = (2^D - 2) \cdot M + 1 \tag{B.37}$$

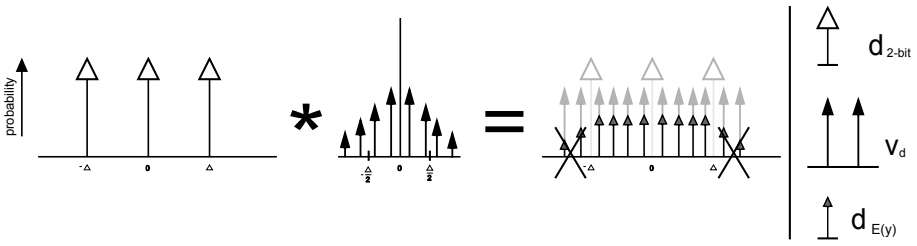

Figure B.2: Convolution of triangular dither PDF and quantizer decision levels result in decision level distribution.

The use of the concept of the equivalent quantizer is illustrated by simulation for triangular PDF dither. A spectrum plot of a dithered quantizer and its equivalent undithered quantizer is shown in Figure B.3.

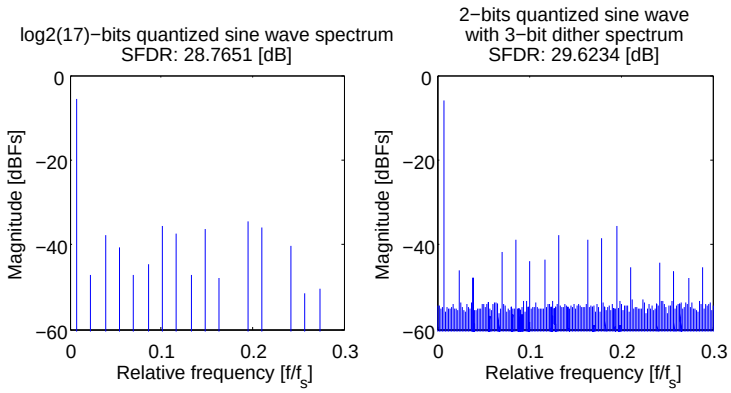

Figure B.3: Spectra of a log(17)-bits equivalent quantizer and the 3-bit triangular dithered 2-bit quantizer: they have approximately the same SFDR. (MATLAB code in appendix C.3)

Appendix C

MATLAB code snippets

C.1 General MATLAB scripts

C.1.1 Time domain - Uniform quantizer

The following lists the MATLAB code for time domain ADC simulation.

Listing C.1: Time domain - Uniform quantizer

```
Fullscale = 1;                  % ADC input range
ADCbits = 2;                    % Resolution in bits
% Quantization levels (can be more than 2^4, to exclude clipping effects)
Qlevels = 4;
LSB = Fullscale / 2^ADCbits;    %
% set of quantization levels
book = (-(Qlevels-1)/2 * LSB): LSB:((Qlevels-1)/2 * LSB);
% set of decision levels
partition = (-(Qlevels-2)/2 * LSB): LSB:((Qlevels-2)/2 * LSB);
% quantization of signal x
[index,y] = quantiz(x,partition,book);
```

C.1.2 Ideal band-pass filtered Gaussian distributed noise generation

Creation of ideal band-pass filtered gaussian distributed noise:

Listing C.2: Create bandpass Gaussian distributed noise

```
%settings for input signal
channels = 2;           %channels occupied with Gaussian noise
choffset = 9;           %first channel to start at...

windo = [zeros(1,floor(NrOfSamples/targetRBW)*choffset),...
         ones(1, ceil(NrOfSamples/targetRBW)*channels), ...
         zeros(1, floor(NrOfSamples/targetRBW)*(targetRBW-(channels+choffset...
             )))];
windo = [windo, zeros(1,NrOfSamples - length(windo))];

%create signal
sig = randn(1,NrOfSamples);
sig = real(ifft(windo.*fft(sig)));
sig = (sig./sqrt(mean(sig.^2)))*(1/max(Steps));
```

C.2 Gaussian distributed noise and SFDR

The following lists the MATLAB code for looking at distortion components due to clipping. The code can be iterated over s and p to get the dependency

of SFDR on signal and noise power. The code snippet for the ADC is found in Appendix C.1.1.

Listing C.3: Gaussian distributed noise and SFDR

```
% time
time = [0:1:NrOfSamples-1]*Period;

 % create input signal
 PsigdBFs = p;
 Psig = 10^(PsigdBFs/10);
 x = sqrt(Psig)* (Fullscale/2)*sin(time* 2 * pi * frequency);

  SFDRtarget = s;
  Pnoise = ((SFDRtarget-8.07*b-3.29)/171.5)*(LSB^2);
  Pnoisedb = 10*log10(Pnoise*8)    %in dBFs

  %averaging to lower the noise floor
  avgMax = 2^14;
  fftz = zeros(1,NrOfSamples);
  for avg = 1:1:avgMax
   %create dither signal
   v = sqrt(Pnoise)*randn(1,NrOfSamples);
   %create quantizer input
   w = x+v;
   %do conversion
   [index,z] = quantiz(x,partition,book);
   %averaging
   fftz = fftz + (fft(z)/avgMax);
   end;
```

C.3 Equivalent quantizer

The following lists the MATLAB code to show that the SFDR of a dithered system is approximately equal to it's equivalent quantizer.

Listing C.4: equivalent quantizer concept proof

```
%time domain simulation to prove statistical resolution
% A.J. van Heusden, 07-2011
close all;clear;

%Simulation settings
NrOfSamples = 2^19;
period = 1e-9;
time =[0:1:NrOfSamples-1]*period;


D = 2;
M=2^4;
%quantizer settings
Fullscale = 1;
%ADCbits = log2((2^D -1)*M+1);
ADCbits = log2((2^D -2)*M+1); %triangular dith

%ADCbits = 5;
Qlevels = 2^(ADCbits);
LSB = Fullscale / 2^ADCbits;
%book = (-(Qlevels-1)/2 * LSB): LSB:((Qlevels-1)/2 * LSB);
%partition = (-(Qlevels-2)/2 * LSB): LSB:((Qlevels-2)/2 * LSB);
book = (-(Qlevels-2)/2 * LSB): LSB:((Qlevels-1)/2 * LSB);
partition = (-(Qlevels-3)/2 * LSB): LSB:((Qlevels-2)/2 * LSB);

%scale = 3/4;
scale = 1/2
x = Fullscale/2 * scale * sin(time*2*pi*(31.25e6/4));

% equivalent quantizer
[index,y1] = quantiz(x,partition,book);


%quantizer settings: 2-bit Quantizer
FullscaleQ = 1;
ADCbitsQ = 2;
Qlevels = 2^ADCbitsQ;
LSBQ = Fullscale / 2^ADCbitsQ;
bookQ = (-(Qlevels-1)/2 * LSBQ): LSBQ:((Qlevels-1)/2 * LSBQ);
partitionQ = (-(Qlevels-2)/2 * LSBQ): LSBQ:((Qlevels-2)/2 * LSBQ);
```

```
%quantizer settings: dither
FullscaleD = 1/2^ADCbitsQ;
ADCbitsD = log2(M);
Qlevels = 2^(ADCbitsD);
LSB = Fullscale / 2^ADCbits;
bookD = (-(Qlevels-1)/2 * LSB): LSB:((Qlevels-1)/2 * LSB);
partitionD = (-(Qlevels-2)/2 * LSB): LSB:((Qlevels-2)/2 * LSB);
%dither signal:
%v = LSBQ*(rand(1,NrOfSamples)-0.5);
v = LSBQ*(rand(1,NrOfSamples)-0.5) + LSBQ*(rand(1,NrOfSamples)-0.5); %...
    triangular dith
%quantize dither signal:
[index,vq] = quantiz(v,partitionD,bookD);


%quantize 2-bit
[index,y2] = quantiz((x+vq),partitionQ,bookQ);

%get FFT in dBFs
plotffty1 = 20*log10(abs(fft(y1)/NrOfSamples *(2/Fullscale)*2));
plotffty2 = 20*log10(abs(fft(y2)/NrOfSamples *(2/Fullscale)*2));

%calculate SFDRs:
fftc = plotffty1(1:NrOfSamples/2); [maxy1, loc] = max(fftc); fftc(loc) = ...
    -300;
SFDRy1 = maxy1 - max(fftc);
fftc = plotffty2(1:NrOfSamples/2); [maxy2, loc] = max(fftc); fftc(loc) = ...
    -300;
SFDRy2 = maxy2 - max(fftc);

xax = [0:1:NrOfSamples-1]/NrOfSamples;
subplot(1,2,1);
plot(xax,plotffty1);
xlabel('Relative frequency [f/f_s]');ylabel('Magnitude [dBFs]');
title({['log2(' num2str(2^ADCbits) ')-bits quantized sine wave spectrum'];['...
    SFDR: ' num2str(SFDRy1) ' [dB]']});
axis([0 0.3 -60 0]);
subplot(1,2,2);
plot(xax,plotffty2);
xlabel('Relative frequency [f/f_s]');ylabel('Magnitude [dBFs]');
title({[num2str(ADCbitsQ) '-bits quantized sine wave'];['with 3-bit dither ...
    spectrum'];['SFDR: ' num2str(SFDRy2) ' [dB]']});
axis([0 0.3 -60 0]);
```

C.4 Decision level variation

The following code shows the method of calculating the frequency components of the equivalent quantizer error function

Listing C.5: Decision level variation error signal

```
% To show the dependence of an undithered quantizer SFDR on variations in
% its decision levels.
% A.J. van Heusden, 08-2011

%cycle through Mr: number of harmonics
for m = Mr
    ideal = 0;
    sumr = 0;

    %blachman implementation for m is odd (Nr is fourier terms)
     if(mod(m,2) ~= 0)
        ideal = i*imag(  sum((2./(-i*pi.*Nr)).*besselj((m),Nr*2*pi*A*2^D/LSB...
            ))));
    else
        ideal = 0;
    end;

    %calculate added error:
    added = 0;
    %cycle through decision levels
    for d = 2^D/2:1:(3*2^D/2 - 1)
        %Amp is amplitude in LSB
        A = -2*(2*LSB/Amp) * (d)*(LSB/2^D);
        B = orig + LSB*(1-alpha);

        %written out integration:
        added = added + (3*Amp/(4*LSB)) * (1/(-i*2*pi*m)) * (...
              - exp(-i*m*(2*pi-asin(A))) + exp(-i*m*(2*pi-asin(B))) + ...
```

```
            +exp(-i*(m)*(pi+asin(A))) - exp(-i*(m)*(pi+asin(B)))      );
    end
    Eideal = [Eideal ideal];
    Eadded = [Eadded added];
end;

Eideal = Eideal*LSB*2; %scale the output
Eideal(1) = Eideal(1)+i*A*2^D*2; % add fundamental
```

C.5 Decision level rules

C.5.1 Decision level rule, sine wave

The following lists the MATLAB code to obtain optimal decision levels for sinusoidal inputs.

Listing C.6: Obtain decision level probabilities

```
%this calculates the disicion levels for a pure sine as input
%set dither type, otherwise dither is rectangular
dither = 'triang';

LSB = 0.25;  %LSB definition

if(sum(dither == 'triang'))
    A = LSB*1; %signal amplitude
else
    A = LSB*1.5; %signal amplitude
end

step = LSB/10000; %nummerical approximation accurateness
xSine = [-A:step:A]; % value axis for sine PDF

h1 = (A*2)./(pi.*sqrt((A)^2 - xSine.^2)) / length(xSine);
%correct the infinite values
h1(length(h1)) = 0; h1(1) = 0;
h1(1) = (1-sum(h1))/2;
h1(length(h1)) = (1-sum(h1));

%create the dither PDF
xPDF = [-1*LSB+step : step:1*LSB];
h2 =  (((xPDF > (-LSB/2)) + (xPDF < (LSB/2)))-1);
if(sum(dither == 'triang'))
    %create triangular PDF
    h2 = conv(h2,h2);
end
h2 = h2/sum(h2);
h2 = h2(length(h2)/4: 3*length(h2)/4); %chop off zeros

%create total PDF
h3 = conv(h1,h2);
%get the values
d_min = sum(h3(1:(length(h3)/4)))
d_nul = sum(h3(1:2*(length(h3)/4)))
d_max = sum(h3(1:3*(length(h3)/4)))
check = sum(h3(1:4*(length(h3)/4)))
```

C.5.2 Band-pass Gaus clipping distortion vs. SFDR

C.5.2.1 Maximum allowed sigma

Listing C.7: Clipping distortion of bandlimited Gaussian distributed signal

```
%this calculates the disicion levels for a Gaussian distributed signal with
%a certain sigma
%A.J. van Heusden, 08-11

%settings:
LSB = 0.25;
step = 1/1000;
fsRange = 16;
xGaus = [-(fsRange/2)+step : step:(fsRange/2)]; %16sigma..
%set the sigma:
%sigma = %0.215;
%sigma = 0.174;
```

```
sigma = 0.146;
%create input signal PDF
h1 = 1/(2*pi*sigma^2) * exp( -((xGaus).^2./(2*sigma^2)));
h1 =h1./sum(h1);
%create dither PDF
h2 =  (((xGaus > (-LSB/2)) + (xGaus < (LSB/2)))-1);
h2 = h2/sum(h2);
%convolute and chop off the unused parts
h3 = conv(h1,h2);
h3 = h3(length(h3)/4: 3*length(h3)/4);
%obtain the probabilities
d_min = sum(h3(1:((length(h3)/2)-(LSB/step)-1)))
d_nul = sum(h3(1:(length(h3)/2)-1))
d_max = sum(h3(1:(length(h3)/2+(LSB/step)-1)))
check = sum(h3(1:4*(length(h3)/4)))
```

C.5.2.2 Decision levels

The following lists the snippet for determination of decision levels for a certain sigma

Listing C.8: Calculation of decision level probabilities

```
%this calculates the disicion levels for a Gaussian distributed signal with
%a certain sigma
%A.J. van Heusden, 08-11

%settings:
LSB = 0.25;
step = 1/1000;
fsRange = 16;
xGaus = [-(fsRange/2)+step : step:(fsRange/2)]; %16sigma..
%set the sigma:
%sigma = %0.215;
%sigma = 0.174;
sigma = 0.146;
%create input signal PDF
h1 = 1/(2*pi*sigma^2) * exp( -((xGaus).^2./(2*sigma^2)));
h1 =h1./sum(h1);
%create dither PDF
h2 =  (((xGaus > (-LSB/2)) + (xGaus < (LSB/2)))-1);
h2 = h2/sum(h2);
%convolute and chop off the unused parts
h3 = conv(h1,h2);
h3 = h3(length(h3)/4: 3*length(h3)/4);
%obtain the probabilities
d_min = sum(h3(1:((length(h3)/2)-(LSB/step)-1)))
d_nul = sum(h3(1:(length(h3)/2)-1))
d_max = sum(h3(1:(length(h3)/2+(LSB/step)-1)))
check = sum(h3(1:4*(length(h3)/4)))
```

Bibliography

[1] Ian F. Akyildiz, Won-Yeol Lee, Mehmet C. Vuran, and Shantidev Mohanty. Next generation/dynamic spectrum access/cognitive radio wireless networks: A survey. *Elsevier*, May 2006.

[2] III Mitola, J. and Jr. Maguire, G.Q. Cognitive radio: making software radios more personal. *Personal Communications, IEEE*, 6(4):13 –18, August 1999. ISSN 1070-9916. doi: 10.1109/98.788210.

[3] T. Yucek and H. Arslan. A survey of spectrum sensing algorithms for cognitive radio applications. *Communications Surveys Tutorials, IEEE*, 11(1):116 –130, 2009. ISSN 1553-877X. doi: 10.1109/SURV.2009.090109.

[4] M.S. Oude Alink, E.A.M. Klumperink, M.C.M. Soer, A.B.J. Kokkeler, and B. Nauta. A 50mhz-to-1.5ghz cross-correlation cmos spectrum analyzer for cognitive radio with 89db sfdr in 1mhz rbw. In *New Frontiers in Dynamic Spectrum, 2010 IEEE Symposium on*, pages 1 –6, 2010. doi: 10.1109/DYSPAN.2010.5457887.

[5] M.S. Oude Alink. Increasing the spurious free dynamic range of an integrated spectrum analyser. Master's thesis, University of Twente, Nov 2008.

[6] A.R. Smeenge. Improving cross-correlation spectrum sensing using two antennas. Master's thesis, University of Twente, Oct 2010.

[7] M. G. M. Stegers. Design and realization of a 2-bit a/d converter with power dependent reference levels for astronomical use. Master's thesis, University of Twente, Sept. 1996.

[8] A.B.J. Kokkeler. Level regulation in he dzb a/d converter (note 624). Technical report.

[9] T.H. Lee. *The design of CMOS radio-frequency integrated circuits*. Cambridge University Press, 2004. ISBN 9780521835398. URL http://books.google.com/books?id=io1hL48OqBsC.

[10] Roland Minihold Christoph Rauscher, Volker Janssen. *Fundamentals of Spectrum Analysis*. Rohde & Schwarz GmbH & Co. KG, 2001.

[11] Behzad Razavi. *RF microelectronics*. Prentice-Hall, Inc., Upper Saddle River, NJ, USA, 1998. ISBN 0-13-887571-5.

[12] S.V. Vaseghi. *Advanced digital signal processing and noise reduction*. John Wiley, 2000. ISBN 9780471626923.

[13] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. *Digital integrated circuits- A design perspective*. Prentice Hall, 2ed edition, 2004.

[14] John Bunton. Ska correlator advances. *Experimental Astronomy*, 17:251–259, 2004. ISSN 0922-6435. 10.1007/s10686-005-5661-5.

[15] M. Pelgrom. *Analog-to-Digital Conversion*. Springer, 2010. ISBN 9789048188871.

[16] J.H. Van Vleck and D. Middleton. The spectrum of clipped noise. *Proceedings of the IEEE*, 54(1), jan. 1966.

[17] M.S. Oude Alink, A.B.J. Kokkeler, E. Klumperink, K.C. Rovers, G. Smit, and B. Nauta. Spurious-free dynamic range of a uniform quantizer. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 56(6):434 –438, 2009. ISSN 1549-7747. doi: 10.1109/TCSII.2009.2020929.

[18] R.A. Wannamaker, S.P. Lipshitz, J. Vanderkooy, and J.N. Wright. A theory of nonsubtractive dither. *Signal Processing, IEEE Transactions on*, 48(2):499 –516, February 2000. ISSN 1053-587X. doi: 10.1109/78.823976.

[19] N. Blachman. The intermodulation and distortion due to quantization of sinusoids. *Acoustics, Speech and Signal Processing, IEEE Transactions on*, 33(6):1417 – 1426, December 1985. ISSN 0096-3518. doi: 10.1109/TASSP.1985.1164729.

[20] B Widrow, I Kollar, and Mc Liu. Statistical theory of quantization. *Ieee Transactions On Instrumentation And Measurement*, 45(2):353–361, 1996.

[21] J.M.D. Pereira, A.C. Serra, and P.S. Girao. Dithered adc systems in the presence of hysteresis errors. In *Instrumentation and Measurement Technology Conference, 1999. IMTC/99. Proceedings of the 16th IEEE*, volume 3, pages 1648 –1652 vol.3, 1999. doi: 10.1109/IMTC.1999.776103.

[22] L. Schuchman. Dither signals and their effect on quantization noise. *Communication Technology, IEEE Transactions on*, 12(4):162 –165, 1964. ISSN 0018-9332. doi: 10.1109/TCOM.1964.1088973.

[23] R.M. Gray and Jr. Stockham, T.G. Dithered quantizers. *Information Theory, IEEE Transactions on*, 39(3):805 –812, May 1993. ISSN 0018-9448. doi: 10.1109/18.256489.

[24] L. Roberts. Picture coding using pseudo-random noise. *Information Theory, IRE Transactions on*, 8(2):145 –154, 1962. ISSN 0096-1000. doi: 10.1109/TIT.1962.1057702.

[25] R. Tandra and A. Sahai. Snr walls for signal detection. *Selected Topics in Signal Processing, IEEE Journal of*, 2(1):4 –17, 2008. ISSN 1932-4553. doi: 10.1109/JSTSP.2007.914879.

[26] Rahul Tandra, Shridhar Mubaraq Mishra, and Anant Sahai. What is a spectrum hole and what does it take to recognize one? *Proceedings of the IEEE*, 97(5):824–848, 2009.

[27] Mark Goresky, Andrew M. Klapper, Associate Member, and Associate Member. Fibonacci and galois representations of feedback-with-carry shift registers. *IEEE Trans. Inform. Theory*, 48:2826–2836, 2002.

[28] Mark Goresky and Andrew Klapper. Fibonacci and galois representations of feedback with carry shift registers. *IEEE Trans. Inform. Theory*, 48:2826–2836, 2000.

[29] C. Stevenson, G. Chouinard, Zhongding Lei, Wendong Hu, S. Shellhammer, and W. Caldwell. Ieee 802.22: The first cognitive radio wireless regional area network standard. *Communications Magazine, IEEE*, 47(1):130 –138, january 2009. ISSN 0163-6804. doi: 10.1109/MCOM.2009.4752688.

[30] F.-X. Socheleau, P. Ciblat, and S. Houcke. Ofdm system identification for cognitive radio based on pilot-induced cyclostationarity. In *Wireless Communications and Networking Conference, 2009. WCNC 2009. IEEE*, pages 1 –6, april 2009. doi: 10.1109/WCNC.2009.4917840.

[31] Jae-Jin Jung, Kwang-Hyun Baek, Shin-Il Lim, Suki Kim, and Sung-Mo Kang. Design of a 6 bit 1.25 gs/s dac for wpan. In *ISCAS*, pages 2262–2265, 2008.

[32] Jae-Jin Jung, Bong-Hyuck Park, Sang-Seong Choi, Shin-Il Lim, and Suki Kim. A 6-bit 2.704gsps dac for ds-cdma uwb. In *APCCAS*, pages 347–350, 2006.

[33] Shen Wang, Dong Sam Ha, and S.S. Choi. Design of a 6-bit 5.4-gsamples/s cmos d/a converter for ds-cdma uwb transceivers. In *Ultra-Wideband, 2005. ICU 2005. 2005 IEEE International Conference on*, pages 333 – 338, sept. 2005. doi: 10.1109/ICU.2005.1570009.

[34] S. Spiridon and F. Op't Eynde. A 6 bit resolution, 1 gsamples/sec digital to analog converter. In *Semiconductor Conference, 2005. CAS 2005 Proceedings. 2005 International*, volume 2, pages 455 –458 vol. 2, oct. 2005. doi: 10.1109/SMICND.2005.1558825.

[35] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta. A double-tail latch-type voltage sense amplifier with 18ps setup+hold time. In *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pages 314 –605, 2007. doi: 10.1109/ISSCC.2007.373420.

[36] Todd Sepke, Peter Holloway, Charles G. Sodini, and Hae-Seung Lee. Noise analysis for comparator-based circuits. *Trans. Cir. Sys. Part I*, 56:541–553, March 2009. ISSN 1549-8328. doi: 10.1109/TCSI.2008.2002547. URL http://portal.acm.org/citation.cfm?id=1657444.1657448.

[37] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas. Noise analysis of regenerative comparators for reconfigurable adc architectures. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 55(6):1441 –1454, july 2008. ISSN 1549-8328. doi: 10.1109/TCSI.2008.917991.

[38] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, Inc., New York, NY, USA, 1 edition, 2001. ISBN 0072380322, 9780072380323.

[39] Zhaohui Huang and Peixin Zhong. An architectural power estimator for analog-to-digital converters.

[40] Chien-Kai Hung, Jian-Feng Shiu, I-Ching Chen, and Hsin-Shu Chen. A 6-bit 1.6 gsps flash adc in 0.18-um cmos with reversed-reference dummy. In *Solid-State Circuits Conference, 2006. ASSCC 2006. IEEE Asian*, pages 335 –338, nov. 2006. doi: 10.1109/ASSCC.2006.357919.

[41] Ja-Hyun Koo, Yun-Jeong Kim, Sin-Hu Kim, Won-Joo Yun, Shin-Il Lim, and Suki Kim. An 8-bit 250msps cmos pipelined adc using open-loop architecture. In *Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-Pacific Conference on*, pages 94 – 97, aug. 2004. doi: 10.1109/APASIC.2004.1349416.

[42] Hairong Yu and M.-C.F. Chang. A 1-v 1.25-gs/s 8-bit self-calibrated flash adc in 90-nm digital cmos. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 55(7):668 –672, july 2008. ISSN 1549-7747. doi: 10.1109/TCSII.2008.921596.