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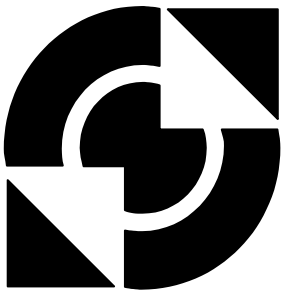

# Continuous Classes of Power Amplifiers

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**Abstract**

In wireless systems a trend towards integration of all building blocks of transmitter and receiver into mainstream CMOS is going on. The Power Amplifier is one of the most difficult blocks to integrate; a relative high power block to integrate in a process with relative low quality factors and nonlinear components. In this report an RF model is presented that can be used for designing a PA using nonlinear components. With this developed model calculations are done that show that it is possible to influence the output phase by varying the input signal and by varying the X reactance. It is also shown that there is a trade off between the input signal amplitude and the PA efficiency. Simulations with varying input signal and varying X reactance show that it is possible to control both the output power and output phase of a Class-E PA.

# Contents

# Chapter 1

# Introduction

In the last decade tremendous growth has occurred in wireless communications systems. In all these wireless systems an RF Power Amplifier (PA) is present. In currently available systems these PAs are generally realized in dedicated and therefore expensive technologies. This blocks cheap integration of a PA into a device. One method to reduce costs and increase integration flexibility is to include the PA into the mainstream technology: CMOS. Mainstream CMOS is however designed for high speed, low power digital applications. From this it can already be concluded that is becomes very difficult to implement a high power PA in mainstream CMOS. There are many classes of power amplifiers, a PA class with theoretically a very high efficiency is the Class-E PA. So it seems to be logical to implement this class of PA in CMOS, but because of the CMOS technology properties it is not possible to implement an *ideal* Class-E PA in CMOS.
In this project the Class-E PA is investigated from a non standard point of view; if it is not possible to implement an *ideal* Class-E PA in CMOS, it may be possible to implement a Class-E lookalike PA in CMOS which does not have the theoretical 100% efficiency, but a slightly lower efficiency and higher flexibility. The PA operation is then not Class-E anymore, but probably a mix of Class-E and other classes. The higher flexibility makes it maybe possible to switch realtime between the different classes of PAs; preferably resulting in a continuous class PA! With this continuous class PA the PA performance (for example efficiency and linearity) can be adjusted realtime.
In chapter 2 the goals of the project are presented. A definition of the continuous class PA is given in chapter 3. In chapter 4 a PA modeling method is presented and a PA model is derived using this method. With the developed model simulations are done, they are presented in chapter 5. Finally in chapters 6 and 7 conclusions are drawn and recommendations for further research are given.
This work was done as final part of the master Electrical Engineering at the University of Twente.

In order to increase the readability of this document, complex modeling issues and derivation details are shown in boxes like this. It is advised to read these boxes only after having a solid knowledge of the used modeling method.

# Chapter 2

# Assignment (re)definition

In this chapter the original assignment is given and redefined.

## 2.1 Original assignment

*"The task of the student in this assignment is to understand the work that has been carried out in our group in this subject. These are 5 publications.*

*After having a solid knowledge about the concept the design phase will start. The load network of the PAs can be designed either using smd components or dedicated technologies such as PASSI. By using an already available transistor in 65nm technology in our group the student will implement the new class of PA for a certain application such as Bluetooth or Wireless LAN etc.*

*Use of simulations is essential in the design process. Cadence, ADS and some EM simulators will be highly needed. After the design is finished, the load network will be send for fabrication which generally takes 2-3 months. This time can be utilized by the student to compose the main parts of the thesis."*

The main goal of the original project was to design a PA for e.g. Bluetooth or Wireless LAN. To be able to design a PA at this relative high frequency it is necessary that accurate models are used during the design process. The already available [5] model did not include all the effects that come up in mainstream CMOS technologies. Therefore it was decided that one of the main tasks was the development of a good model for RF frequencies. Before a model can be made it is important to specify the effects that should be modeled, therefore the very broad goal of implementing a PA into CMOS should be redefined into a much more specific goal.

## 2.2 New PA design options

Designing a PA in CMOS is very challenging because of the CMOS properties, the two main challenges are:

1. Efficiency
2. Flexibility

### 2.2.1 Efficiency

In mainstream CMOS it is impossible to implement an *ideal* PA. In the PA there are a lot of components that introduce power loss, see figure 2.1. Depending

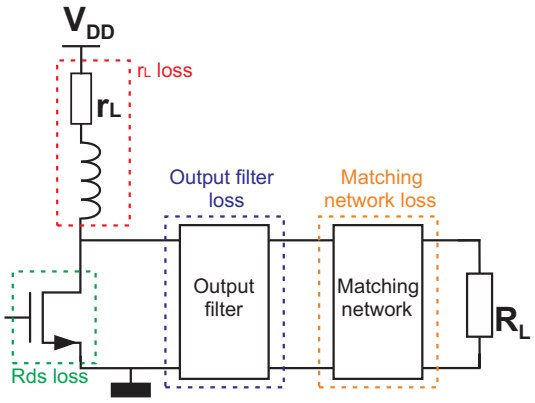



Figure 2.1: Overview of losses inside PA

on the implementation some components will contribute more to the power loss than other components. Probably there is a trade off between the total power loss in external components and loss in switching components.

### 2.2.2 Flexibility

A PA is one of the most complicated building blocks of a wireless system; it is very expensive to design a good PA. Nowadays for each application another PA is designed, a lot of development costs are needed to design all these different PAs. It would be nice if a more flexible PA could be designed, which is capable of working in different applications.
Different applications means different frequencies, output power, modulation techniques, etc. Recently by B.Verhoef, PA frequency and output power control was investigated [4]. The implementation of different modulation techniques and the PA voltage harmonic contents are not investigated in detail yet.
To drive a PA generally an analog pre-driver is used. In most applications the data to transmit is available in the digital domain, with a DAC this is converted to the analog domain to drive the pre-driver. All these intermediate steps limits the flexibility of the whole PA. One possibility of decreasing the number of intermediate blocks is the inclusion of a DAC directly in the PA, see figure 2.2.

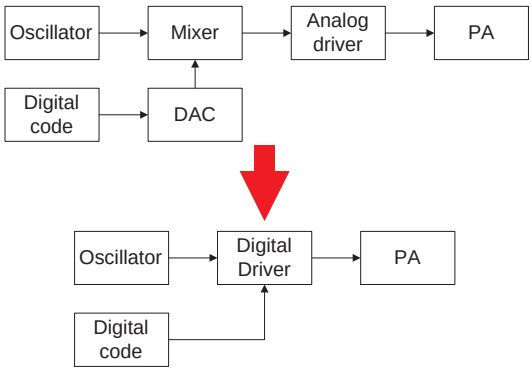



Figure 2.2: DAC inclusion into PA

## 2.3 Conclusion

A PA design aiming at the optimalization of the efficiency probably results in an optimal PA with respect to efficiency, but the resulting PA is still designed for one specific application, it is not very flexible. The resulting PA cannot be used for different applications. It is more interesting to increase the flexibility of a PA. To get a flexible PA a couple of specifications should be controllable:

- Frequency (done by B.Verhoef [4])
- Output Power (done by B.Verhoef [4])
- Modulation techniques (this work)
- Spectrum of output signal (not done yet)

On way of making the PA more flexible is the use of a digital pre-diver, see figure 2.2. The digital pre-driver uses a fixed clock frequency; there is no phase information in the pre-driver clock. Therefore another way of modulating the output signal should be used. In this project the possibilities of DAC integration and possible modulation techniques are investigated. As a result of this the work is more a feasibility study instead of a real optimal design.

# Chapter 3

# Continuous Class PA; Definition

## 3.1 PA analysis

Before a definition of a continuous class PA can be given it is important to understand the existing classes of PAs. In this section the different classes are discussed briefly. A general PA circuit is shown in figure 3.1, the type of transistor, harmonic filtering and output matching network depends on the target application and type of PA. Basically almost all the PA classes use the same

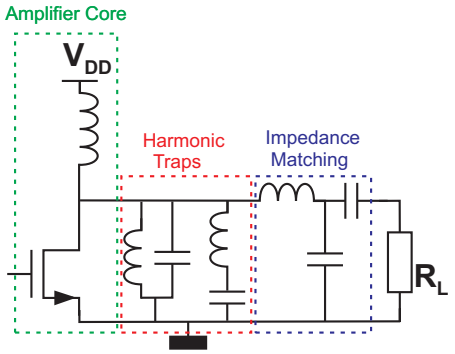



Figure 3.1: A basic PA topology

circuit, see figure 3.1, the main difference between the classes is the transistor conduction angle, the input signal waveform and the output filter configuration. In figure 3.2 an overview of the conduction angle and the input signals of the different classes of PAs are shown.

## 3.2 Continuous Class PA

As can be seen in figure 3.2 one difference between the Class-E and the other classes is the input signal waveform; a square wave in Class-E, sinusoidal in the other classes. In modern CMOS the bandwidth is however limited, especially

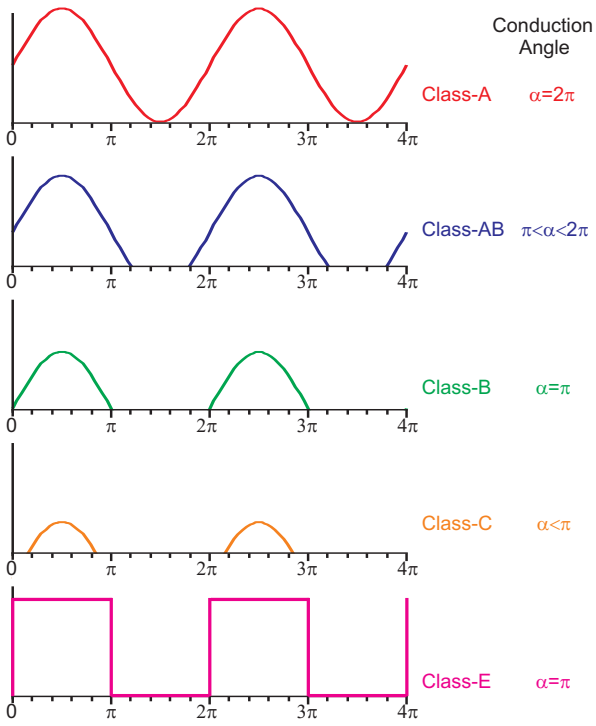



Figure 3.2: Conduction angle and input signal for different PA classes

at high frequencies the square wave Class-E input signal is therefore not ideal anymore. From this becomes clear that the difference between the different classes is very small, especially at RF in (mainstream) CMOS.

### 3.2.1 Definition continuous class PA

From the combination of all these PA classes a new class of PAs is defined:

**"A continuous class PA is a flexible power amplifier which adapts its specifications realtime"**

As a result of this realtime specifications adjustment option, the PA can be used for various applications. These realtime adjustments in specifications can be forced for example by tuning some PA components or the input signal.

One way of modeling the continuous class PA is by adding some "non Class-E effects" to an existing Class-E model. As initial Class-E model the analytical model of M.Acar [8] is chosen, because of the high flexibility of the model. Most of the "non Class-E effects" follow directly from the limitations of the mainstream CMOS. Therefore in the rest of this report the focus is on adding these effects to the existing Class-E model.

## 3.3 Design conditions

The PA should be very flexible; it should be a "building block" that can be placed on every chip. It is therefore important that the PA is designed in a mainstream CMOS process. The newest available process is CMOS 65 from Crolles. The PA is designed for an operating frequency around the 2.4GHz band. Typical output power levels at this frequency are 100mW to 200mW. In this work an output power of 100mW is chosen. To make this possible thick-oxide transistors are used for the PA, this allows the usage of a higher supply voltage compared with thin-oxide. In modern processes quality factors up to 11 are possible [9], but quality factors of 5 are also used. In this work the quality factor of the on-chip inductor is varied between 5 and 11. The quality factor of the on chip capacitors is assumed to be infinite. The output filter components are considered to be off-chip, the quality factor off the off-chip components are assumed to be infinite.
A summary of the design conditions is given below:

- Mainstream CMOS 65
- Operating frequency: 2.4GHz
- Thick-oxide transistor in PA (length = 0.28$\mu$m)
- Output power: 100mW
- PA $V_{DD}$: 1V
- Quality factor on-chip inductor: 5 & 11
- Quality factor on-chip capacitor: $\infty$
- Quality factor off-chip components: $\infty$

# Chapter 4

# PA modeling

## 4.1 Introduction

Recently a new analytical modeling method for Class-E PAs was presented by M.Acar [5]. This method is based on design equations, that make it possible to design a Class-E PA by only specifying the supply voltage, frequency and output power of the PA. The modeling method and the developed model described in this report are based on this theory.
The basic Class-E circuit is shown in figure 4.1.

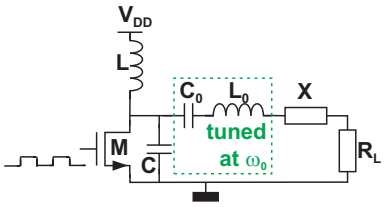



Figure 4.1: Basic Class-E circuit

The implementation into mainstream CMOS can give difficulties when modeling the circuit:

- Transistor: the transistor in a typical new CMOS process cannot be approximated with a switch and an $R_{on}$ anymore, because of the huge (non-linear) capacitors surrounding the transistor. Therefore a new way of transistor modeling needs to be found.

- Output filter ($L_0$ and $C_0$): the $L_0$ and $C_0$ combination acts as a filter to ensure a sinusoidal current trough the load $R_{load}$. $R_{load}$ however puts an upper limit to the loaded quality factor of the filter. This limited loaded quality factor results in a distorted output current, resulting in unwanted out of band signals.

- Pre-driver & Input signal: the circuit needed to drive the transistor has a limited bandwidth. Because of this limited bandwidth the signal at the gate of the transistor is not an ideal square wave.

To predict the circuit behavior at high frequencies it is important that the items listed above are included in a model, but this increases the complexity of the model. It is therefore important to make appropriate simplifications. Before discussing the advanced model in more detail first a general Class-E PA modeling method is described in paragraph 4.2. In paragraph 4.3 the points listed above are discussed. In [3] and [6] some variations on the typical Class-E conditions are presented; a summary of this is given in paragraph 4.4. The more advanced model is presented in paragraphs 4.5 to 4.8. In paragraph 4.9 the developed model is verified with simulations. Some general remarks about the model are discussed in paragraphs 4.10 to 4.11. Finally in paragraph 4.12 some modeling conclusions are drawn.

## 4.2 General Class-E modeling method

An overview of the modeling method [5] is shown in figure 4.2. To explain the used method the design set of the simple model of figure 4.3 will be derived in the following paragraphs using the steps of the flowchart.

### 4.2.1 Simplified model

For this discussion a simple Class-E model [5] is used. First of all a simplified model of the Class-E circuit should be made; the result is shown in figure 4.3. The transistor is modeled as a switch with a finite $R_{on}$. The switch is driven by a square wave. In time interval $0 < t < \pi/\omega$ (time interval 1) the switch is closed, and in interval $\pi/\omega < t < 2\pi/\omega$ (time interval 2) the switch is opened. The quality factor of the output filter (loaded quality factor) is assumed to be infinite, so the load current is sinusoidal: $I_R(t) = I_{R0}\sin(\omega t + \varphi)$. For the inductor an infinite quality factor is assumed. Reactance $X$ can be capacitive as well as inductive.

### 4.2.2 Differential equations

With these assumptions 2 differential equations can be formulated, one with closed switch, and one for the opened switch. In the time interval 1 the switch is closed, the resulting KCL at the drain node of the transistor can be written as:

$$I_{L_1}(t) - I_{S_1}(t) - I_{C_1}(t) + I_R(t) = 0 \tag{4.1}$$

This can be rewritten into:

$$C\frac{d^2V_{C_1}(t)}{dt^2} + \frac{1}{R_{on}}\frac{dV_{C_1}(t)}{dt} + \frac{V_{C_1}(t)}{L} - \frac{V_{DD}}{L} - \omega I_{R0}\cos(\omega t + \varphi) = 0 \tag{4.2}$$

In time interval 2 the switch is opened, so $I_{S_2}(t)$ is zero; from this the KCL in this time interval follows:

$$I_{L_2}(t) - I_{C_2}(t) + I_R(t) = 0 \tag{4.3}$$

This can be rewritten into:

$$C\frac{d^2V_{C_2}(t)}{dt^2} + \frac{V_{C_2}(t)}{L} - \frac{V_{DD}}{L} - \omega I_{R0}\cos(\omega t + \varphi) = 0 \tag{4.4}$$

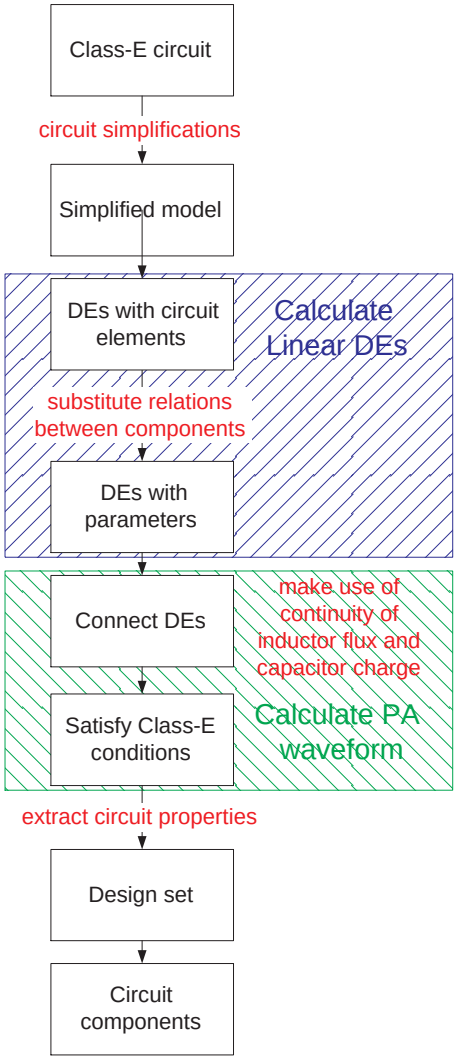



Figure 4.2: Modeling flowchart

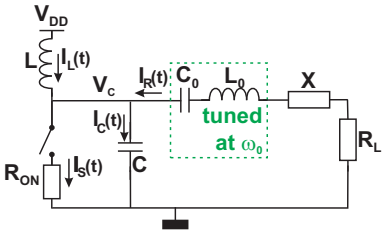



Figure 4.3: Simple Class-E model ($I_R$= sinusoidal)

**Parameters**

The two differential equations (4.2) and (4.4) describe the Class-E model in terms of component values. These two equations can be rewritten into differential equations that only contain the relations between the circuit components; for this three parameters are defined:

$$q = \frac{1}{\omega\sqrt{LC}} \tag{4.5}$$

$$\beta = R_{on}C \tag{4.6}$$

$$p = \frac{\omega L I_{R0}}{V_{DD}} \tag{4.7}$$

With the parameters defined in (4.5) to (4.7) the differential equations (4.2) and (4.4) can be rewritten into (4.8) and (4.9) respectively:

$$\frac{1}{q^2\omega^2}\frac{d^2V_{C_1}(t)}{dt^2} + \frac{1}{q^2\omega^2\beta}\frac{dV_{C_1}(t)}{dt} + V_{C_1}(t) - V_{DD} - p\,V_{DD}\cos(\omega t + \varphi) = 0 \tag{4.8}$$

$$\frac{1}{q^2\omega^2}\frac{d^2V_{C_2}(t)}{dt^2} + V_{C_2}(t) - V_{DD} - p\,V_{DD}\cos(\omega t + \varphi) = 0 \tag{4.9}$$

If the differential equations (4.8) and (4.9) are solved with respect to $V_C(t)$ expressions for $V_{C_1}(t)$ and $V_{C_2}(t)$ are obtained:

$$\begin{aligned} V_{C_1}(t) = {} & e^{\frac{(-1+\sqrt{1-4\,q^2\omega^2\beta^2})t}{2\beta}} Const2_1 + e^{\frac{(1+\sqrt{1-4\,q^2\omega^2\beta^2})t}{2\beta}} Const1_1 \\ & + \frac{p\,q^2\omega^2\beta^2(q-1)(q+1)\cos(\omega\,t+\varphi)}{1+\beta^2(q-1)^2(q+1)^2\omega^2} \\ & + \frac{p\sin(\omega\,t+\varphi)\omega\,\beta\,q^2}{1+\beta^2(q-1)^2(q+1)^2\omega^2} + V_{DD} \end{aligned} \tag{4.10}$$

$$\begin{aligned} V_{C_2}(t) = {} & \sin(q\,\omega\,t)\,Const2_2 + \cos(q\,\omega\,t)\,Const1_2 \\ & + \frac{V_{DD}\,(q^2-1+p\,q^2\cos(\omega\,t+\varphi))}{q^2-1} \end{aligned} \tag{4.11}$$

As can be seen in (4.10) and (4.11) for each solution there are two unknown constants; these constants can be solved by using circuit properties (initial conditions). When these constants are solved, the Class-E model is described without explicitly specifying component values! From this the strong point of this modeling method becomes clear: the waveform of the Class-E PA is known without specifying any component value!

### 4.2.3 Calculate PA waveform

**Connect DEs**

Both (4.10) and (4.11) describe the model in a different time interval, see figure 4.4. As can be seen in the figure at time instances $T_0$, $T_1$ and $T_2$ there is a switch between descriptions. To explain this switching in more detail first the behavior at time instance $T_1$ will be discussed. Time instance $T_1$ can be split

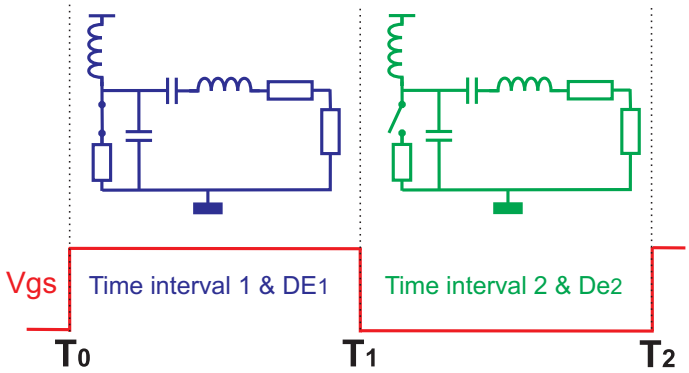



Figure 4.4: Overview time interval switching

into two time instances: $T_1^-$ and $T_1^+$.
From the continuity of the capacitor charge and inductor flux it follows that:

$$Q_C(T_1^-) = Q_C(T_1^+) \tag{4.12}$$
$$\Phi_L(T_1^-) = \Phi_L(T_1^+) \tag{4.13}$$

These two relations should be rewritten in terms of $V_C$, $q$, $\beta$, $p$ and $\varphi$. For (4.12) this is simple:

$$\begin{aligned} Q_C(T_1^-) &= Q_C(T_1^+) \\ V_{C_1}(T_1^-)\,C &= V_{C_2}(T_1^+)\,C \\ V_{C_1}(T_1^-) &= V_{C_2}(T_1^+) \end{aligned} \tag{4.14}$$

For (4.13) it is not so straightforward, because the inductor current is by definition equal to:

$$\begin{aligned} \Phi_L(T_1^-) &= \Phi_L(T_1^+) \\ I_L(T_1^-)\,L &= I_L(T_1^+)\,L \\ \int_{-\infty}^{T_1^-}(V_{DD} - V_C(t))dt &= \int_{-\infty}^{T_1^+}(V_{DD} - V_C(t))dt \\ \int_{-\infty}^{T_1^-}(V_{DD} - V_C(t))dt &= \int_{-\infty}^{T_1^-}(V_{DD} - V_C(t))dt \\ V_C(t) &= V_C(t) \end{aligned} \tag{4.15}$$

This relation cannot be used, because it does not result in an extra initial condition. Therefore the $I_L$ should be described in another way. One possibility is the use of the KCLs at $T_1^-$ and $T_1^+$ (see (4.1) and (4.3) respectively). Using

these KCLs relation (4.13) can be rewritten into:

$$\begin{aligned}
\Phi_L(T_1^-) &= \Phi_L(T_1^+) \\
I_L(T_1^-)\,L &= I_L(T_1^+)\,L \\
I_{S_1}(T_1^-) + I_{C_1}(T_1^-) - I_R(T_1^-) &= I_{C_2}(T_1^+) - I_R(T_1^+) \\
I_{S_1}(T_1^-) + I_{C_1}(T_1^-) &= I_{C_2}(T_1^+) \qquad (4.16) \\
\frac{1}{R_{on}}\,V_{C_1}(T_1^-) + C\left(\frac{dV_{C_1}(t)}{dt}, \{t = T_1^-\}\right) &= C\left(\frac{dV_{C_2}(t)}{dt}, \{t = T_1^+\}\right) \\
\frac{1}{\beta}\,V_{C_1}(T_1^-) + \left(\frac{dV_{C_1}(t)}{dt}, \{t = T_1^-\}\right) &= \left(\frac{dV_{C_2}(t)}{dt}, \{t = T_1^+\}\right) \qquad (4.17)
\end{aligned}$$

Both (4.12) and (4.13) are now expressed in terms of $V_C$ and $\beta$. With these two relations it is now possible to solve $Const1_1$ and $Const2_1$ of (4.10). The constants in (4.11) can be solved using the same method at time instances $T_2^-$ and $T_0^+$.

**Satisfy Class-E conditions**

In both time intervals 1 and 2, $V_C(t)$ is described in terms of $q$, $\beta$, $p$ and $\varphi$. By adding the typical (ideal) Class-E conditions (see (4.18) and (4.19)) two of these four parameters can be solved (for example $p$ and $\varphi$; $V_C(t)$ is then described in terms of $q$ and $\beta$).

$$V_C(2\pi/\omega) = 0 \qquad (4.18)$$

$$\left(\frac{dV_C(t)}{dt}, \{t = 2\pi/\omega\}\right) = 0 \qquad (4.19)$$

### 4.2.4 Design set derivation

Using the design set developed by M.Acar [5] it is possible to calculate the circuit component values. The design set definition is given in (4.20) to (4.23).

$$K_L = \frac{\omega L}{R} \qquad (4.20)$$

$$K_C = \omega C R \qquad (4.21)$$

$$K_P = \frac{P_{OUT} R}{V_{DD}^2} \qquad (4.22)$$

$$K_X = \frac{X}{R} \qquad (4.23)$$

In this paragraph the derivation of the design set $K$ is presented.

$K_L$: follows from the principle of power conservation:

$$P_{R_{load}} + P_{switch} = P_{DC} \qquad (4.24)$$

From this the $K_L$ can be derived:

$$K_L = \frac{\omega\,L}{R}\,\frac{P_{R_{load}}}{P_{DC} - P_{switch}} \qquad (4.25)$$

$K_C$: follows from the definition of $q$ and $K_L$:

$$K_C = \frac{1}{q^2 K_L} \tag{4.26}$$

$K_P$: To calculate $K_P$ the $P_{OUT}$ should be calculated. This can be done with help of the assumption of an infinite loaded quality factor (sinusoidal current through $R_{load}$):

$$P_{OUT} = P_{R_{load}} = I_R^2 \frac{R_{load}}{2} \tag{4.27}$$

By using the definitions of $p$ and $q$, $K_P$ can be expressed as:

$$K_P = \frac{p^2}{2K_L^2} \tag{4.28}$$

$K_X$: can be derived using two fundamental quadrature Fourier components of $V_C(t)$.

$$V_R = \int_0^{\frac{\pi}{\omega}} \frac{V_{C_1}(t)}{\pi} \sin(\omega t + \varphi)\, dt + \int_{\frac{\pi}{\omega}}^{\frac{2\pi}{\omega}} \frac{V_{C_2}(t)}{\pi} \sin(\omega t + \varphi)\, dt \tag{4.29}$$

$$V_X = \int_0^{\frac{\pi}{\omega}} \frac{V_{C_1}(t)}{\pi} \cos(\omega t + \varphi)\, dt + \int_{\frac{\pi}{\omega}}^{\frac{2\pi}{\omega}} \frac{V_{C_2}(t)}{\pi} \cos(\omega t + \varphi)\, dt \tag{4.30}$$

$$K_X = V_X / V_R \tag{4.31}$$

### 4.2.5 Circuit components

In figure 4.5 the relations between the design set and the component values are shown. From the figure can be seen that when for example $V_{DD}$, $P_{OUT}$ and $\omega$ are specified all the component values can be calculated.

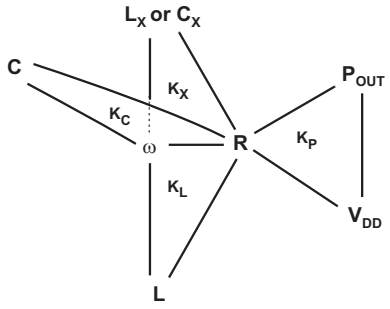



Figure 4.5: Relation between design set and components

### 4.2.6 Modeling method conclusions

In this paragraph a modeling method using a design set is described; the whole analysis for this simple model was already done by M.Acar [5]. From his simulations and experience it was concluded that this simple model is not sufficiently accurate for good RF modeling, therefore a more advanced model is developed using the same method. This advanced model is described in paragraphs 4.5 to 4.8, but first some of the modeling difficulties mentioned in the introduction of this chapter will be discussed.

## 4.3 Modeling difficulties

### 4.3.1 Transistor modeling

In modern CMOS processes the $C_{GS}$ and $C_{GD}$ are relatively large compared to $C_{DS}$. Especially the $C_{GD}$ will play a dominant role at high frequencies. It is therefore important that this capacitor is modeled in a proper way. The $C_{GS}$ is also relatively large and each period this capacitor is charged and discharged, but the Class-E waveform is not directly influenced by this capacitor; the Power Added Efficiency (PAE) is however influenced. As stated in paragraph 2.3, the goal of this project is to investigate the possibilities of phase modulation; not primarily the PAE optimization. Therefore only $C_{GD}$ and $C_{DS}$ are included in the developed model, see figure 4.6 for the used equivalent transistor circuit. In figure 4.6 the equivalent transistor circuit is given, but it is not possible

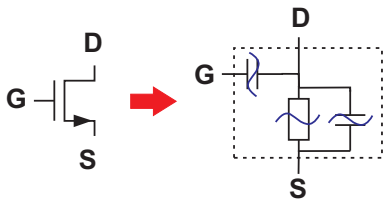



Figure 4.6: Used transistor model

to give values to the components, because of the unknown transistor width. It is therefore important that the transistor can be described without explicit specifying the transistor width. From the physical transistor model can be extracted that:

$$R_{DS}\,W = constant(V_{GS}, V_{DS}) \tag{4.32}$$

$$\frac{C_{DS}}{W} = constant(V_{GS}, V_{DS}) \tag{4.33}$$

$$\frac{C_{GD}}{W} = constant(V_{GS}, V_{DS}) \tag{4.34}$$

From these three relations some combinations of width independent transistor properties can be formulated:

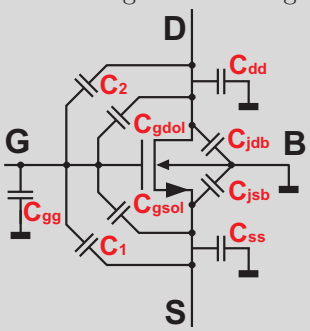
$$\beta = R_{DS}(C_{DS} + C_{GD}) = constant(V_{GS}, V_{DS}) \tag{4.35}$$

$$gdtot = \frac{C_{GD}}{C_{GD} + C_{DS}} = constant(V_{GS}, V_{DS}) \tag{4.36}$$

$$dstot = \frac{C_{DS}}{C_{GD} + C_{DS}} = constant(V_{GS}, V_{DS}) \tag{4.37}$$

### Physical transistor capacitors

For the transistor model a DC model is used. In the PA the transistor is however used at RF frequencies. The use of a DC model can be justified by the assumption that the transit frequency (fT) of the transistor is high enough to be able to neglect non-quasi static effects in the model. An overview of the physical capacitors of a transistor is given in the figure below.




In the PA circuit the source of the transistor is grounded, from this follows:

$$C_{DS} = C_{dd} + C_{jdb} \tag{4.38}$$
$$C_{GD} = C_{gdol} + C_2 \tag{4.39}$$
$$C_{GS} = C_{gg} + C_{gsol} + C_1 \tag{4.40}$$

In this work only the $C_{DS}$ and $C_{GD}$ are included.
In a real transistor some extra effects are present, for example the change in drain charge due to a changing gate voltage. This effect is not modeled in this work.

### $C_{gs}$ modeling issues

In this work the $C_{GS}$ is not included in the model because this capacitor does not influence the PA waveform directly, but it does influence the PAE. The inclusion of $C_{GS}$ in the model is not simple; it requires a more advanced loaded quality factor model, as is explained in paragraph 4.3.3.
A couple of effects should be kept in mind before it can be decided whether $C_{GS}$ should be included in a model:

- $R_{out}$ pre-driver
- $C_{GS}$ tuning out
- Differential Class-E

If the digital input method is used, see paragraph 4.10 for more details, the pre-driver is probably made of inverters. The $R_{out}$ of these inverters in combination with $C_{GS}$ forms a low pass filter. The lower $R_{out}$ the higher the resulting filter cut-off frequency. If the cut-off frequency is high enough the $C_{GS}$ does not influence the PA waveform directly, but it affects the PAE.

The energy consumed by $C_{GS}$ can be reduced by placing an inductor in series with the gate of the transistor. An disadvantage of this technique is the very small bandwidth of the circuit. So this probably is not possible in combination with the digital pre-driver.

Another possibility to reduce the energy consumption of $C_{GS}$ is the use of a differential PA topology with cross-coupled feedback to the input. This technique is also not easy to implement in the digital PA.

### 4.3.2 Input signal modeling

In the simplified Class-E model the input signal is a square wave, so the input signal can be described with 2 samples. In a practical situation the input signal never is a real square wave (because of the limited bandwidth of the pre-driver), so it should be nice if the input signal can be described more accurately. This is recently done by M.Acar [9], by sampling the input signal: Consider for example the input signal given in figure 4.7 (A square wave with only the first and third harmonic). In the traditional way this input signal is approximated with 2 input samples, as can be seen in the figure this approximation is far from perfect. If this input signal is sampled for example 10 times per period, the approximation of the input signal is obviously better. Another advantage of this technique is that it is even possible to investigate the effect of non-square wave input signals.

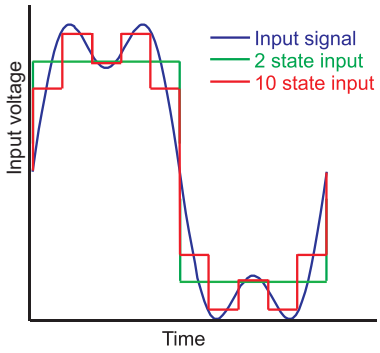



Figure 4.7: Example input signal sampling

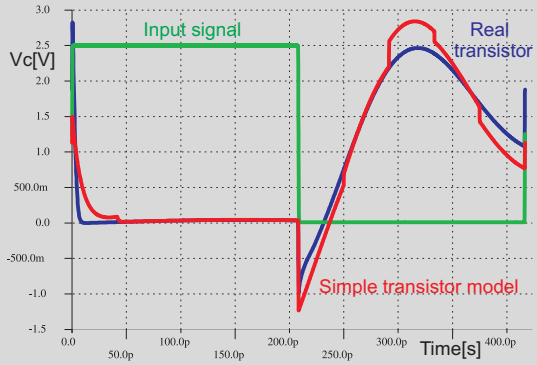
#### Sampled input

In the case of only 2 input samples the model is subdivided into 2 time intervals, as is done in the simple model of paragraph 4.2. So there are 2 differential equations needed to describe the model. The situation of more input samples is basically the same as the 2 sample input, only a couple of samples (time intervals) are added. In this project there is chosen to sample the input signal at 10 times the fundamental frequency. So instead of 2 differential equations there are now 10 differential equations.

The transistor is modeled with nonlinear components, see figure 4.6. As is explained in paragraph 4.8 these nonlinear components are linearized around an operating point. Therefore the model uses states; in each state a new operating point is calculated. To make the linearization accurate it is important that enough states are used in the model.
The input signal is sampled at 10 times the fundamental frequency. Each input sample results in other nonlinear transistor components. So at least 10 states should be used in the model.

### Optimal number of states

In the figure below results of a calculation and simulation with relative high $\alpha$ are shown, see (4.41) for a definition of $\alpha$. As can be seen in the figure the drain voltage (Vc) is high at the beginning of the period. Due to the high Vgs (VN(SG)), $R_{DS}$ is low at the beginning of the period. As a result of this the drain voltage should drop rapidly, as is shown in the simulation result, this is not the case with the calculation result. This high voltage results in an inaccurate transistor operating point determination in the first state (see paragraph 4.8.3 for a detailed description).




In the figure above 10 equidistantly placed states are used for the calculation; from this figure it becomes clear that this is not always sufficient to get a good transistor linearization. From the simulation result it can be seen that the time intervals should be divided into at least 10 intervals to get a good approximation, so at least 100 states are needed to get a good transistor approximation.

### Optimal number of input samples

When keeping the digital driver technique (see paragraph 4.10 for more details) in mind it becomes clear that the input sample frequency cannot be too high. In case of the 10 input samples used in this project the resulting digital clock frequency is 10 times the fundamental frequency; the PA should operate at 2.4GHz, so the resulting digital clock should be 24GHz. When the digital part is designed very accurate this is feasible in CMOS 65, but the power consumption will be high. To reduce the power consumption of the digital part it could be considered to reduce the number of input samples. Because of the more proof-of-concept character of this work no attention is paid to this power consumption; the number of input samples is kept 10.

**Solvability in Maple**

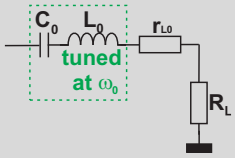
As stated above at least 100 states should be used to get a good transistor approximation. From this follows that there also appear 100 DEs that should be connected. Unfortunately Maple is not always capable of connecting such high number of DEs. It is possible to tune the number of "Digits" that Maple uses, but this doesn't result in a reliable Maple script. It is expected that the use of another mathematical program, for example a Fortran or C code implementation, is able to solve this issue.

### 4.3.3 Loaded quality factor modeling

In the simple model it is assumed that the output current is sinusoidal. From M.Acar's experience it was concluded that for a loaded quality factor of 5 or lower the output current can not be approximated with a sinusoidal current anymore. In this project the main goal is to investigate the possibilities of phase and amplitude modulation and not primarily the output spectrum optimalization. In this work therefore a loaded quality factor of 10 is used in the simulations; in the calculations this is approximated with a sinusoidal output current, because otherwise the model becomes too complicated.

**Efficiency**

It is clear that changing the loaded quality factor results in a changing linearity of the total PA. If the loaded quality factor decreases and the linearity should remain unchanged, it is clear that the PA waveform should also change (should contain less harmonics). This probably results in a lower PA efficiency. Besides this second order dependency there is a more direct relation between the loaded quality factor and the loss in the output filter. Assume the output filter of the figure below.




The quality factor of the capacitor is assumed infinite; the quality factor of the inductor ($q_L$) is assumed to be finite:

$$q_L = \frac{\omega L_0}{r_{L_0}}$$

The loaded quality factor is defined as [1]:

$$Q_L = \frac{\omega L_0}{R_{Load}}$$

These 2 relations can be rewritten into:

$$r_{L_0} = \frac{R_{Load} Q_L}{q_L}$$

From this it can be seen that the series resistor $r_{L_0}$ (due to limited inductor quality) decreases when $Q_L$ decreases and $R_{load}$ is kept constant, resulting in less power loss in the output filter. At the same time the efficiency of the PA decreases, from this becomes clear that there is trade off between the power loss in de PA and the power loss in the output filter.

**Overview solvability of different DEs**

The loaded quality factor is a result of $R_{load}$ in combination with the output filter ($L_0$ and $C_0$). In a real implementation $R_{load}$ is transformed with a matching network. This matching network probably has a frequency dependent characteristic. From this it follows that the loaded quality factor is also influenced by the matching network. To predict the linearity of a PA correctly the loaded quality factor must properly be included in the calculations. This results in higher order differential equations. The inclusion of $C_{GS}$ in the model also increases the DE order. Not all combinations of transistor modeling and loaded quality factor modeling can be done in the same model, because of the resulting DEs. In the table an overview of the solvability of the different combinations is given.

| Transistor | Loaded Quality factor | Resulting DE | Solvable? |
|---|---|---|---|
| $R_{DS}$ & $C_{DS}$ | $\infty$ | 2nd order + sin | yes |
| | finite + matching | $\geq$4th order | yes |
| $R_{DS}$ & $C_{DS}$ & $C_{GD}$ | $\infty$ | 2nd order + sin | yes |
| | finite + matching | $\geq$4th order | yes |
| $R_{DS}$ & $C_{DS}$ & $C_{GD}$ & $C_{GS}$ | $\infty$ | 3nd order + sin | **no** |
| | finite + matching | $\geq$5th order | **yes** |

From the table it can be seen that it is not possible to make a model that includes the $C_{GS}$ and an infinity loaded quality factor. So for good transistor modeling it is needed to also include the loaded quality factor into the model.

## 4.4 Class-E: Classic, $V_{ariable}$ $V_{oltage}$ and $V_{ariable}$ $S_{lope}$

In the classical Class-E operation the switch closes at the moment where both the capacitor voltage and voltage slope are zero. This ensures that there are no power losses at the switching moment. An alternative for these classical boundary conditions is to allow non zero capacitor voltage and voltage slope at the switching moment; resulting in two new PA subclasses: Class-$E_{V_{ariable}V_{oltage}}$ and Class-$E_{V_{ariable}S_{lope}}$. Recently it is shown that both Class-$E_{VV}$ and Class-$E_{VS}$ boundary conditions have some advantages compared with the classical Class-E [3] [6]. In figure 4.8 typical waveforms of Class-$E_{VV}$ and Class-$E_{VS}$ are shown.

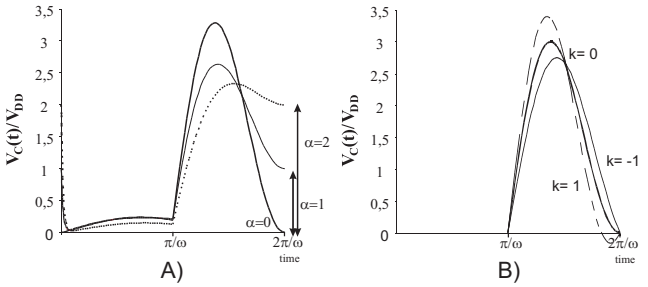



Figure 4.8: PA voltages A) Class-$E_{VV}$ B) Class-$E_{VS}$

To describe the nonzero voltage at the switching moment an extra parameter ($\alpha$) is defined for the Class-$E_{VV}$:

$$V_C(2\pi/\omega) = \alpha\, V_{DD} \tag{4.41}$$

For the Class-$E_{VS}$ also an extra parameter ($k$) is defined to describe the nonzero voltage slope at the switching moment:

$$\left(\frac{dV_C(t)}{dt}, \{t = 2\pi/\omega\}\right) = k\,\omega\, V_{DD} \tag{4.42}$$

It is also possible to combine both Class-$E_{VV}$ and Class-$E_{VS}$ boundary conditions. Especially if for example linearity optimizations of the PA are considered, it is important that the model offers the possibility to implement these new boundary conditions.

## 4.5 Advanced model; Overview

In the following paragraphs an advanced Class-E PA model is presented. The model includes the nonlinear effects of the transistor ($R_{ds}$, $C_{ds}$ and $C_{gd}$); it can be divided into two main blocks, see figure 4.9:

1. A linear model, like the one described in paragraph 4.2.
2. An iterative algorithm encapsulating the linear model. This algorithm calculates the "operating point" of the linear model.

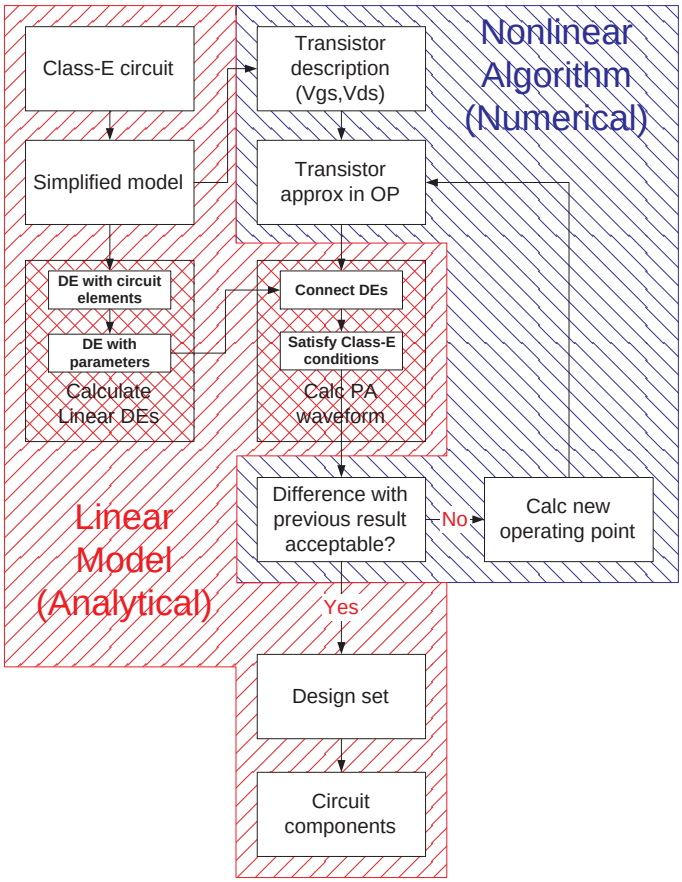



Figure 4.9: Overview nonlinear modeling method

The model description is also done in 2 parts, in paragraph 4.7 the derivation of the linear design set is described; in paragraph 4.8 the algorithm is presented. But before going into mathematical details in paragraph 4.6 a summary of the used method and a preview of the results is given.

## 4.6 Advanced model; Summary

In the paragraphs 4.5 to 4.8 the model is described with mathematics. In this section a summary of the used method and a preview of the results is given.

### 4.6.1 Used Method

First of all the Class-E circuit is modeled, resulting in a model with nonlinear (ideal) components, see figure 4.10. The values of these nonlinear components

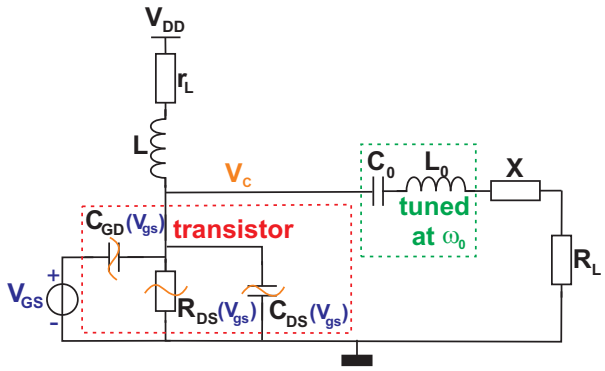



Figure 4.10: Class-E model with nonlinear components

are dependent on the voltage across the components. Because of the varying PA voltage during a period, the voltage across the nonlinear components is also varying, resulting in varying component values during a period. To model this component variation the PA waveform is sampled, in each time interval (state) the nonlinear components are linearized, resulting in piece-wise linear components. In state the minimal and maximal PA voltage is calculated. These voltages are used for the linearization of the components in each state, see figure 4.11 for an example. In figure 4.11 on the right side a PA voltage is shown. The

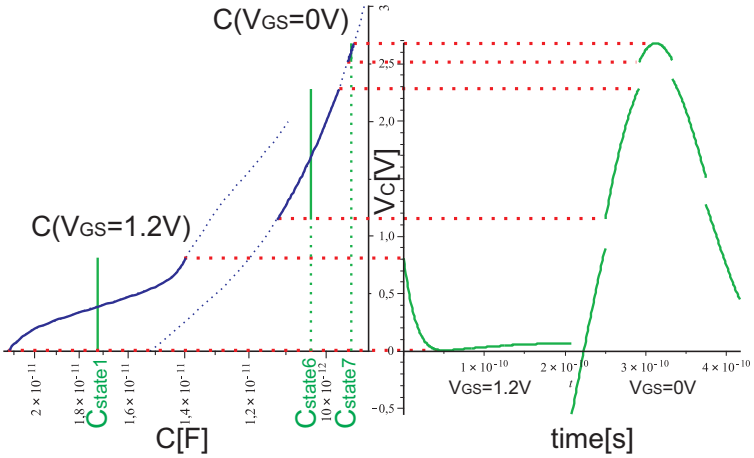



Figure 4.11: Component linearization example

used input voltage is a square wave; in the first half of the period $V_{GS} = 1.2$V, in the second half $V_{GS} = 0$V. On the left a nonlinear capacitor is shown for both

$V_{GS} = 1.2$V and $V_{GS} = 0$V. From the figure becomes clear that the linearized capacitor is different in each state. At the switching moments between the states, the capacitor values changes, resulting in a discontinuity in PA voltage.

### 4.6.2 Preview results

As stated above the nonlinear effects of the transistor ($R_{ds}$, $C_{ds}$ and $C_{gd}$) are linearized in each state, resulting in different components in each state. This results in a discontinuity in the PA voltage. With help of the linearized components it is possible to calculate a PA voltage. The PA voltage of the corresponding real circuit should be approximately the same, except for the discontinuities, these are of course not present in the real circuit. In figure 4.12 the PA voltages resulting from both calculation and simulation are shown. There is a good matching between the calculation and simulation, as expected the PA voltage of the real circuit does not have discontinuities.

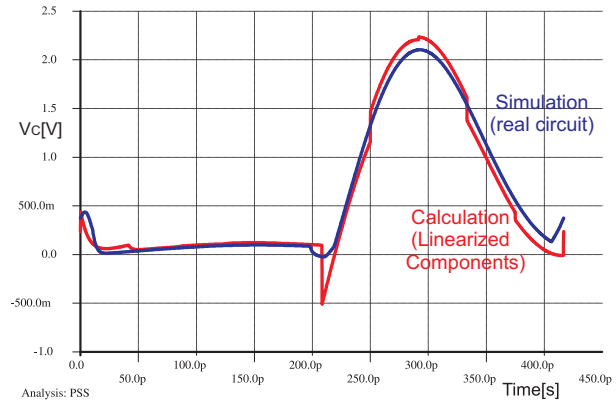



Figure 4.12: PA voltage resulting from calculation and simulation

## 4.7 Advanced model; Linear part

In this paragraph the linear part of the advanced model is derived, this is done in the same way as for the simple model (see paragraph 4.2). Each step in the flowchart of figure 4.9 will be explained here. The explanation of the used method is kept compact, because it is the same as is described in paragraph 4.2.

### 4.7.1 Class-E model

Paragraph 4.3 explains the details of the used transistor model, number of input samples, number of states and loaded quality factor. The capacitor in parallel to the transistor is assumed to be only formed by the output capacitor of the transistor. For the inductor a finite quality factor is assumed. The resulting Class-E model is shown in figure 4.13.

The inductor is modeled with an ideal inductor in series with an ideal resistor. In reality there is also a (nonlinear) capacitor parallel to these inductor and resistor. This capacitor is not included in the model, but it is possible to include the capacitor in the model, without increasing the order of the DEs. Effectively this capacitor is in parallel with the $C_{DS}$ of the transistor.

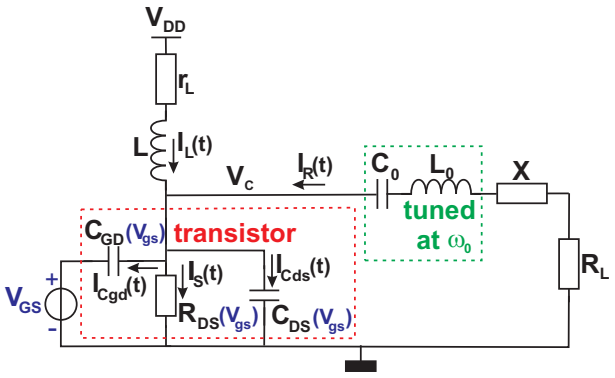



Figure 4.13: Advanced Class-E model ($I_R$= sinusoidal)

As can be seen in the figure, linear components are used for the transistor instead of the nonlinear components shown in figure 4.6. The approximation of the nonlinear effects is discussed in detail in paragraph 4.8.

### 4.7.2 Differential equations

In the model 10 states are used, so the model can be described with 10 differential equations. All these equations have the same form, only the component values ($R_{DS}$, $C_{DS}$ and $C_{GD}$) are different in each equation. The KCL at the drain node of the transistor can be written as:

$$I_{L_n}(t) - I_{S_n}(t) - I_{Cds_n}(t) - I_{Cgd_n}(t) + I_R(t) = 0 \tag{4.43}$$

With $n = 1...10$

This can be rewritten into:

$$\left(C_{GD_n}+C_{DS_n}\right)\frac{d^2V_{C_n}(t)}{dt^2}+\left(\frac{1}{R_{DS_n}}+\frac{\left(C_{GD_n}+C_{DS_n}\right)r_L}{L}\right)\frac{dV_{C_n}(t)}{dt}$$
$$+\left(\frac{r_L}{R_{DS_n}}+\frac{1}{L}\right)V_{C_n}(t)-\frac{V_{DD}}{L}-\omega I_{R0}\cos(\omega t+\varphi)$$
$$-\left(\frac{I_{R0}\,r_L}{L}\right)\sin(\omega t+\varphi)=0 \tag{4.44}$$

With $n = 1...10$

**Parameters**

Differential equation (4.44) describes the model in terms of component values. This DE should be rewritten into a differential equation containing only parameters, like is done in paragraph 4.2.2. The parameters of the simple model cannot be used directly because of the complex transistor model. The new parameters are based on the parameters of the simple model (relations (4.5) to (4.7)), the only difference is the substitution of $C = (C_{DS_n} + C_{GD_n})$. Because $R_{DS}$, $C_{DS}$ and $C_{GD}$ are different in each state parameters $q$ and $\beta$ are also different in each state. The advanced model also includes the finite quality factor of the inductor, therefore an extra parameter ($q_l$) is added which describes the quality factor of the inductor:

$$q_n = \frac{1}{\omega\sqrt{L(C_{DS_n}+C_{GD_n})}} \equiv q_{initial}\sqrt{\frac{C_{DS_1}+C_{GD_1}}{C_{DS_n}+C_{GD_n}}} \tag{4.45}$$

$$q_{initial} = \frac{1}{\omega\sqrt{L(C_{DS_1}+C_{GD_1})}} \tag{4.46}$$

$$\beta_n = R_{DS_n}(C_{DS_n}+C_{GD_n}) \tag{4.47}$$

$$p = \frac{\omega L I_{R0}}{V_{dd}} \tag{4.48}$$

$$q_L = \frac{\omega\, L}{r_L} \tag{4.49}$$

To be able to compare the different PAs with different component values, and thus different parameter values, an extra parameter ($q_{initial}$) is added to the definition of $q$ in (4.45). This extra parameter is used as a normalization for each time interval.

The algorithm, see paragraph 4.8, uses iterations to approximate the nonlinear transistor. In each iteration the PA waveform is calculated with the new transistor approximation. So in each iteration $R_{DS}$, $C_{DS}$ and $C_{GD}$ are changed compared to the previous iteration. From this it follows that the parameters $q_n$ and $\beta_n$ are also different in each iteration. To be able to compare the result of different PAs, parameter $q_{initial}$ should be normalized:

$$q_{initial} = \frac{q_{iteration_n}}{\sqrt{\frac{C_{DS_{1_1}}+C_{GD_{1_1}}}{C_{GD_{iteration_n}}+C_{GD_{iteration_n}}}}} \tag{4.50}$$

The $q$ specified in simulation results is in fact the normalized $q_{initial}$.

With these parameters (4.44) can be rewritten into:

$$\begin{aligned}
&\frac{1}{q_n^2\,\omega^2}\frac{d^2V_{C_n}(t)}{dt^2}+\left(\frac{1}{q_n^2\,\omega^2\,\beta_n}+\frac{1}{q_n^2\,\omega\,q_L}\right)\frac{dV_{C_n}(t)}{dt}\\
&+\left(\frac{1}{q_n^2\,\omega^2\,\beta_n\,q_L}\right)V_{C_n}(t)-V_{DD}\\
&-p\,V_{DD}\cos(\omega t+\varphi)-\frac{p\,V_{DD}\sin(\omega t+\varphi)}{q_L}=0
\end{aligned}\tag{4.51}$$

This differential equation can be solved with respect to $V_{C_n}(t)$, but the solution is too complex to show here. In the solution two constants appear like in (4.10). These two constants can be solved using the initial conditions of the circuit.

### 4.7.3 Calculate PA waveform

First of all the DEs are connected to form a periodic solution, like in paragraph 4.2.3, then Class-E conditions (4.41) and (4.42) are forced to define the PA waveform.

#### Connect DEs

For each $n = 1...9$ there is a switching moment $T_n$ and for $n = 10$ the moments $T_{10}$ and $T_0$ are shared like in paragraph 4.2.3. At each switching moment the (total) capacitor charge and the inductor flux are continuous, but because of the switching $V_{GS}$ extra charge is injected or extracted from the circuit. The two relations that describe these effects are derived in appendix A, the results are shown here.
The equation that follows from the continuous capacitor charge and charge injection effect is:

$$\begin{aligned} V_{C_{n+1}}(T_n^+)\Big(C_{gd_{n+1}} + C_{ds_{n+1}}\Big) &= V_{C_n}(T_n^-)\Big(C_{gd_n} + C_{ds_n}\Big) \\ &\quad - V_{gs_n} C_{gd_n} + V_{gs_{n+1}} C_{gd_{n+1}} \end{aligned} \tag{4.52}$$

This relation can be rewritten into a relation that is normalized to the transistor width:

$$\begin{aligned} V_{C_{n+1}}(T_n^+) &= V_{C_n}(T_n^-)\,\Delta tot_n\Big(gdtot_n + dstot_n\Big) \\ &\quad - V_{gs_n}\,\Delta tot_n\, gdtot_n + V_{gs_{n+1}}\, gdtot_{n+1} \end{aligned} \tag{4.53}$$

With:

$$\Delta tot_n = \frac{C_{GD_n} + C_{DS_n}}{C_{GD_{n+1}} + C_{DS_{n+1}}}$$

$$gdtot_n = \frac{C_{GD_n}}{C_{GD_n} + C_{DS_n}} \tag{4.54}$$

$$dstot_n = \frac{C_{DS_n}}{C_{GD_n} + C_{DS_n}} \tag{4.55}$$

Both (4.55) and (4.54) are derived from (4.36) and (4.37), with the addition of the different states.

With the continuity of the inductor flux at the switching moment it follows that:

$$\begin{aligned} &\frac{1}{\beta_n} V_{C_n}(T_n^-) + \left(\frac{dV_{C_n}(t)}{dt}\{t = T_n^-\}\right) = \\ &\frac{1}{\Delta tot_n}\left(\frac{1}{\beta_{n+1}} V_{C_{n+1}}(T_n^+) + \left(\frac{dV_{C_{n+1}}(t)}{dt}\{t = T_n^+\}\right)\right) \end{aligned} \tag{4.56}$$

With the two relations given in (4.53) and (4.56) the 2 constants in each differential equation can be solved, so the PA periodic voltage can be expressed as a function of $q$, $\beta$, $p$ and $\varphi$.

**Satisfy Class-E conditions**

The periodic PA voltage can be calculated now, but until now there is no Class-E operation specified in the model. The Class-E conditions are specified at the end of the period ($T_{10}^-$). The typical Class-E conditions (4.18) and (4.19) are extended to make Class-E$_{VV}$ and Class-E$_{VS}$ operation possible, see paragraph 4.4. The resulting relations are:

$$V_{C_{10}}(2\pi/\omega) = \alpha V_{DD} \tag{4.57}$$

$$\left(\frac{dV_{C_{10}}(t)}{dt}, \{t = 2\pi/\omega\}\right) = \omega k\, V_{DD} \tag{4.58}$$

### 4.7.4 Design set derivation

The design set definition is the same as used in the simple model, so (4.20) to (4.23) are also used in the advanced model. There are however some changes in the derivation of the design set:

$K_L$: follows from the principle of power conservation. In the model the quality factor of the inductor is assumed to be finite, so there is power loss in the inductor ($P_{r_L}$). The addition of $C_{gd}$ created an extra power path from the pre-driver to the drain of the transistor, the power delivered by the pre-driver is -$P_{V_{gs}}$.

$$P_{R_{load}} + P_{switch} + P_{r_L} = P_{DC} - P_{V_{gs}} \tag{4.59}$$

From this $K_L$ can be derived:

$$K_L = \frac{\omega\, L}{R}\, \frac{P_{R_{load}}}{P_{DC} - P_{switch} - P_{r_L} - P_{V_{gs}}} \tag{4.60}$$

With:

$$P_{R_{load}} = \frac{p^2\, V_{DD}^2\, R_{load}}{2\,\omega^2\, L^2} \tag{4.61}$$

$$P_{DC} = \frac{1}{10} \sum_{n=1}^{10} \left( \frac{V_{DD}}{\beta_n\, \omega^2\, L\, q_n^2\, (T_n - T_{n-1})} \int_{T_{n-1}}^{T_n} V_{C_n}(t) dt \right) \tag{4.62}$$

$$P_{switch} = \frac{1}{10} \sum_{n=1}^{10} \left( \frac{1}{\beta_n\, \omega^2\, L\, q_n^2\, (T_n - T_{n-1})} \int_{T_{n-1}}^{T_n} V_{C_n}^2(t) dt \right)$$

$$P_{V_{gs}} = \frac{1}{10} \sum_{n=1}^{10} \left( \frac{1 - dstot_n}{\omega^2\, L\, q_n^2\, (T_n - T_{n-1})} \int_{T_{n-1}}^{T_n} \frac{dV_{C_n}(t)}{dt} dt \right) \tag{4.63}$$

$$P_{r_L} = \frac{1}{10} \sum_{n=1}^{10} \left( \frac{\omega\, L}{q_L\, (T_n - T_{n-1})} \int_{T_{n-1}}^{T_n} I_{L_n}^2(t) dt \right)$$

$$I_{L_n}(t) = \frac{1}{\omega^2\, L\, q_n^2} \left( \frac{dV_{C_n}(t)}{dt} + \frac{V_{C_n}(t)}{\beta_n} - p\, V_{DD}\, \omega\, q_n^2\, \sin(\omega\, t + \varphi) \right)$$

$K_C$: follows from the definition of $q_n$ and $K_L$, but because of the switching $q_n$, $K_C$ is also different in each time interval:

$$K_{C_n} = \frac{1}{q_n^2 K_L} \tag{4.64}$$

$K_P$: $K_P$ can be calculated in the same way as is done in the simple model:

$$K_P = \frac{p^2}{2K_L^2} \tag{4.65}$$

$K_X$: can be derived using two fundamental quadrature Fourier components of $V_C(t)$.

$$K_X = V_X / V_R \tag{4.66}$$

With:

$$V_R = \sum_{n=1}^{10} \left( \int_{T_{n-1}}^{T_n} \frac{V_{C_n}(t)}{\pi} \sin(\omega t + \varphi)\, dt \right)$$
$$V_X = \sum_{n=1}^{10} \left( \int_{T_{n-1}}^{T_n} \frac{V_{C_n}(t)}{\pi} \cos(\omega t + \varphi)\, dt \right)$$

### 4.7.5 Circuit components

The translation from design set to component values is the same as for the simple model, see paragraph 4.2.5. The advanced model approximates the PA behavior with a real transistor, so the transistor width should be calculated. In the simple model the capacitor in parallel with the transistor follows from the design set, see figure 4.5. As is stated in paragraph 4.7.1 this capacitor is only formed by the output capacitor $C_{DS}$ of the transistor. In the advanced model $C_{GD}$ is also included, effectively this capacitor is in parallel with $C_{DS}$. So the capacitor that follows from the design set should be equal to $C_{DS}+C_{GD}$. Combining this with relations (4.33) and (4.34) results in the transistor width, see figure 4.14

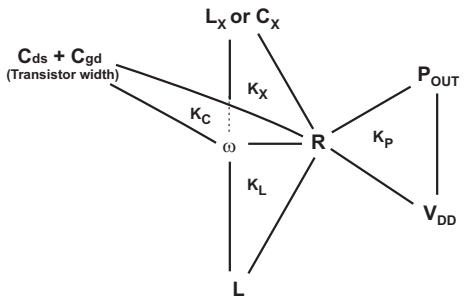



Figure 4.14: Relation between design set and components for the advanced model

## 4.8 Advanced model; Nonlinear algorithm

The nonlinear algorithm is a skin that encapsulates the linear model, see figure 4.9. Each step in the flowchart of figure 4.9 will be explained here.

### 4.8.1 Transistor description

For each operating point of the transistor the three components $R_{DS}$, $C_{DS}$ and $C_{GD}$ are extracted from a (Pstar) device model. These components are rewritten into width-independent parameters (4.35) to (4.37). For each value of $V_{gs}$ these three parameters can be plotted as function of $V_{ds}$ (= $V_C$), in figure 4.15 an example for $\beta$ (defined in 4.47) is shown.

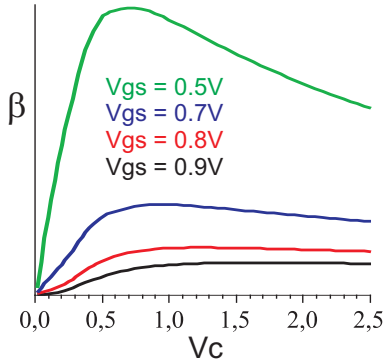



Figure 4.15: $\beta$ curves for different values of $V_{gs}$

### 4.8.2 Calculate new Operating Point

To linearize the transistor components in each interval the operating point in each interval must be calculated. The operating point is defined as the minimal voltage during one time interval ($V_{OPmin_n}$) to the maximal voltage during the time interval ($V_{OPmax_n}$):

$$V_{OPmin_n} = min\Big(V_{C_n}(t)\{t = T_{n-1}...T_n\}\Big) \tag{4.67}$$

$$V_{OPmax_n} = max\Big(V_{C_n}(t)\{t = T_{n-1}...T_n\}\Big) \tag{4.68}$$

To calculate the operating point of each interval $V_C(t)$ should be known. In the first iteration of the algorithm the $V_C(t)$ is not known, therefore the operating point of the first iteration is chosen to be from 0V ($V_{OPmin_n}$= 0) to 2V ($V_{OPmax_n}$= 2) (just a random number, it does not influence the final result). After the first iteration the $V_C(t)$ is known. From this the operating point ($V_{OPmin_n}$ and $V_{OPmax_n}$) can be calculated.

### 4.8.3 Transistor approximation in Operating Point

As can be seen in figure 4.15 the transistor parameters are described as function of $V_C$. The transistor parameters in the operating point are calculated by taking the mean parameter value between ($V_{OPmin_n}$) and ($V_{OPmax_n}$):

$$\beta_{iteration+1_n} = \frac{\int_{V_{OPmin_{iteration_n}}}^{V_{OPmax_{iteration_n}}} \beta(V_{GS_n}, V_C)\, dV_C}{V_{OPmax_{iteration_n}} - V_{OPmin_{iteration_n}}} \tag{4.69}$$

$$gdtot_{iteration+1_n} = \frac{\int_{V_{OPmin_{iteration_n}}}^{V_{OPmax_{iteration_n}}} gdtot(V_{GS_n}, V_C)\, dV_C}{V_{OPmax_{iteration_n}} - V_{OPmin_{iteration_n}}} \tag{4.70}$$

$$dstot_{iteration+1_n} = \frac{\int_{V_{OPmin_{iteration_n}}}^{V_{OPmax_{iteration_n}}} dstot(V_{GS_n}, V_C)\, dV_C}{V_{OPmax_{iteration_n}} - V_{OPmin_{iteration_n}}} \tag{4.71}$$

The definitions of $\beta(V_{GS_n}, V_C)$, $gdtot(V_{GS_n}, V_C)$ and $dstot(V_{GS_n}, V_C)$ are given in (4.35) to (4.37).

An example of the resulting linearized (piecewise constant) transistor description is given in figure 4.16.

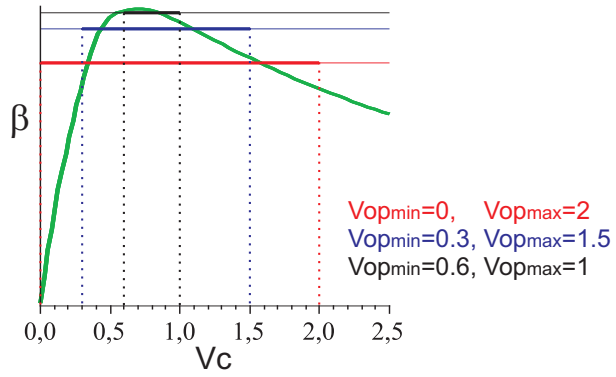



Figure 4.16: $\beta$ approximation in succeeding iterations @ $V_{gs} = 0.5$V

### 4.8.4 Difference acceptable

With the linearized transistor description (4.69) to (4.71) it is possible to calculate the PA periodic waveform; this is described in detail in paragraphs 4.2.3 and 4.7.3. After each iteration a PA waveform is available, with this result it is possible to calculate the operating point for the next iteration. Because of the converging character of the algorithm the difference between the results of the succeeding iterations becomes smaller after each iteration. When the difference between the different iterations is small enough the final PA voltage is used to determine the design set, see paragraphs 4.2.4 and 4.7.4 for a detailed description. Finally with the derived design set the component values are calculated using the methods described in paragraphs 4.2.5 and 4.7.5.

## 4.9 Model verification; Maple vs Pstar

In this section the advanced model is compared with simulations. The used settings for this comparison are: Square wave input of 2.5V @ 2.4GHz, $\alpha = 0$, $k = 0$ and $q = 1.1$. In table 4.1 an overview of the difference between the Maple calculations and Pstar simulations is given.

Table 4.1: Overview calculation and simulation models

| | Maple | Pstar simple transistor model | Pstar real transistor |
|---|---|---|---|
| | Calculation | Simulation | |
| Ql | $\infty$ | 10 | 10 |
| Input signal | discrete | discrete | continues |
| PA waveform | discontinues | discontinues | continues |

First of all in paragraph 4.9.1 the Maple calculations are compared with Pstar simulations where the simple transistor model is used. Then the maple calculations are compared with the real transistor simulations, see paragraph 4.9.2. Finally in paragraph 4.9.3 an overview of the models is given.

### 4.9.1 Maple vs Pstar; Simple transistor model

The only difference between the maple calculations and the pstar simulations where the simple transistor model is used is the loaded quality factor; in maple $Q_L = \infty$, in pstar $Q_L$ is varied between 5 and 100. The results of both maple and pstar are shown in figure 4.17. The waveforms in the figure contains big discontinuities, this is due to the switching between the different states of the algorithm. From figure 4.17 can be seen that the pstar simulation with $Q_L = 100$ has the best fit with the maple calculations. This high loaded quality factor is physical not possible therefore for further simulations a $Q_L$ of 10 is used. Even the value of 10 is quite difficult to implement in a real PA. In a more advanced model it should be considered to include the $Q_L$ in the maple calculations to be able to model lower loaded quality factors.

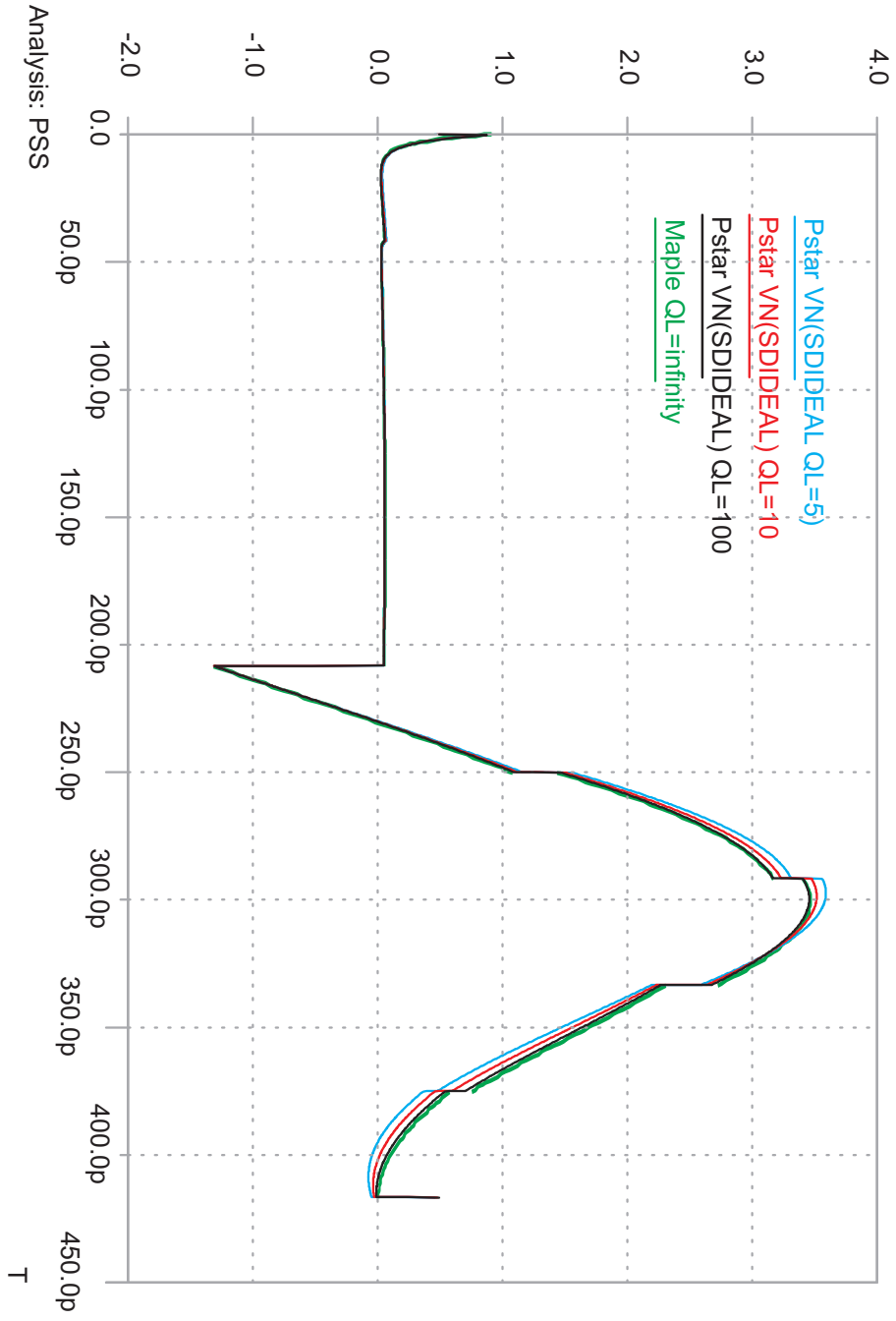
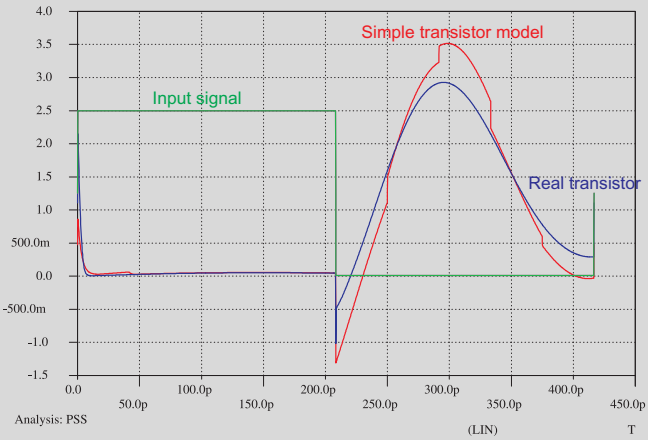



Figure 4.17: Maple and Pstar (simple transistor model) results with different QL

### 4.9.2 Maple vs Pstar; Real transistor

In the figure below two Pstar simulation results are shown, one with the simple transistor model and one with the real transistor.




As can be seen in the figure the waveforms of both simulations are approximately the same. In both simulations an infinite switching speed is assumed, for the simple transistor model this is correct, but because of the limited bandwidth of the pre-driver in reality this is not possible. Therefore the rest of simulations are done with a slow switching $V_{gs}$, see figure 4.18.

In figure 4.18 the results of the simple transistor model and of the real transistor are shown. Because of the limited bandwidth of the pre-driver the input signal for the real transistor simulations has increased rise and fall times. As can be seen in the figure the waveforms of both simulations are approximately the same. So the waveform matching between the calculations and simulations with the real transistor is good. In paragraph 4.9.3 a more detailed comparison is given.

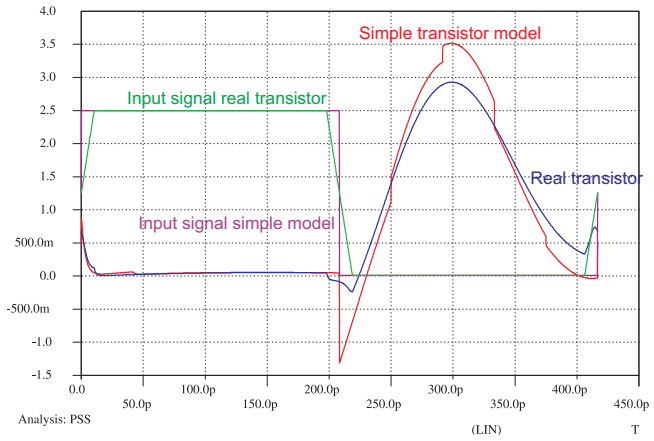



Figure 4.18: Model results; slow switching input voltage

### 4.9.3 Maple vs Pstar; Overview

In this work the $C_{GS}$ and the limited quality factor of the output filter are not included in the model, the efficiency shown in the results is therefore not the PAE. The used definition of the efficiency in this work is:

$$efficiency = \frac{P_{R_{load}}}{P_{DC} - P_{V_{gs}}} \tag{4.72}$$

The definitions of $P_{R_{load}}$, $P_{DC}$ and $P_{V_{gs}}$ are given in (4.61), (4.62) and (4.63) respectively.

In figures 4.19, 4.20 and 4.21 the Maple calculations are compared with Pstar simulations with the real transistor. The used settings for this comparison are: Square wave input of 2.5V @ 2.4GHz, QL=10, $\alpha = -0.8...0.4$. For each value of $\alpha$ the $k$ and $q$ are chosen such that the maximal efficiency was achieved.

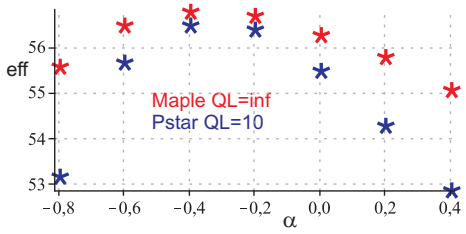



Figure 4.19: Efficiency comparison

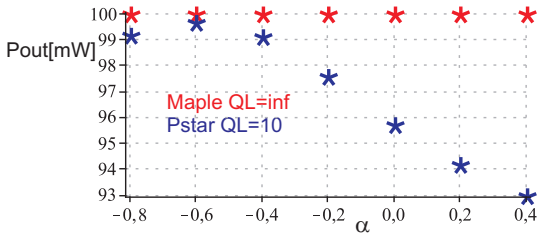



Figure 4.20: Output power comparison

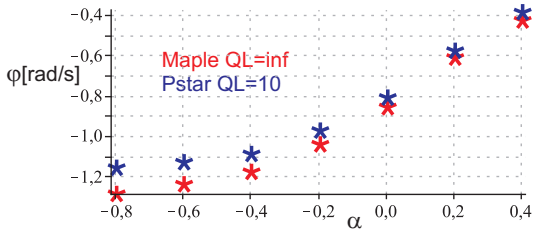


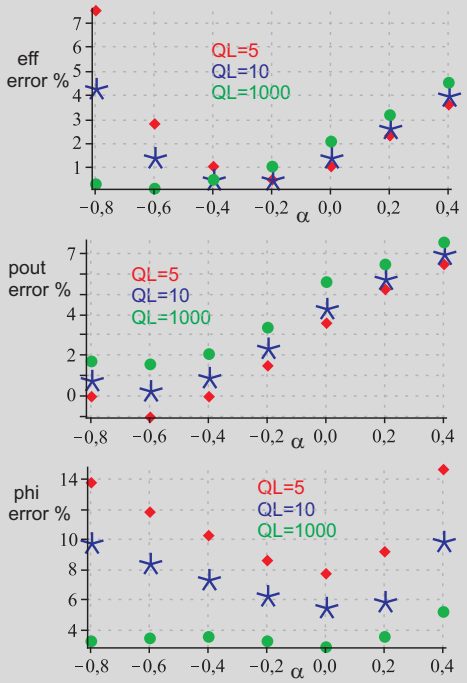

Figure 4.21: Output phase comparison

In the range from $\alpha = -0.8...0.4$ the difference between the calculated and simulated efficiency is maximal 4.3%. The maximal difference between the output

power and output phase is 7% and 10% respectively. The big difference between calculations and simulations for the output phase are due to the loaded quality factor approximation. If in Pstar the same simulations are done with a QL=1000, the maximal error decreases to 5.2%.

**Loaded quality factor**

The same simulations are done with other loaded quality factors; QL=5, QL=10 and QL=1000. In the three figures below the results are shown. In the figures the difference between the error compared to the Maple calculations are shown for different loaded quality factors.



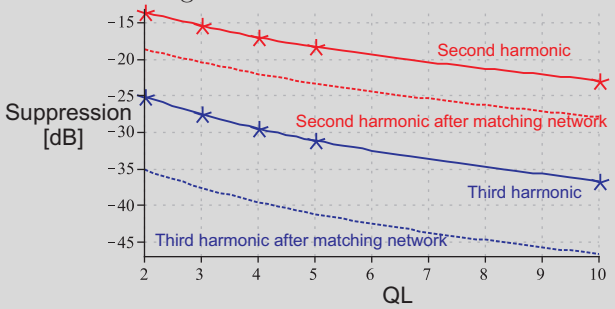

In the first figure the error in the efficiency is shown. It can be seen that the error is slightly higher in the case of QL=5.

In results of the output power matching are shown in the second figure. As can be seen there is almost no difference between the different loaded quality factors.

In the third picture the error in output phase is shown. From this becomes clear that the loaded quality factor does influence the error; a higher loaded quality factor results in less error. In the case of QL=5 the error between the calculations and simulations is maximal 14%, this high error is not acceptable when doing output phase simulations.

**Output spectrum**

The output spectrum of the PA is determined by looking at the suppression of the second and third harmonics. Typical applications require an out of band suppression of 40dB to 50dB; both second and third harmonic should be suppressed 40dB to 50dB. The required output impedance is 50Ω, a matching network is needed to achieve this. This matching network acts as a filter; if a simple LC network is used as matching network the second harmonic is suppressed approximately 5dB, the third harmonic approximately 10dB [10].
To check the output spectrum of the PA as function of the loaded quality factor, simulations are done with QL=2...10. The other settings are: Square wave input of 2.5V @ 2.4GHz, $\alpha = -0.4$, $k = -1.8$, $q = 0.74$ and ql=5. In the figure below an overview of the results is given.




To suppress the third harmonic 40dB, a loaded quality factor of at least 4 is needed. The second harmonic is suppressed at least 23dB @QL<4, this is not enough. The remaining 17dB can be suppressed by using an differential PA.

## 4.10 Analog vs digital input

Till now the PA is modeled with analog input signals, it is however also possible to apply digital input words to the PA, see figure 4.22. The most critical transistor parameter is the $R_{DS}$ during the "on" state (high $V_{gs}$ in combination with low $V_{ds}$) in this state the transistor operates in triode. In this section a comparison between both techniques is given.
The $C_{GD}$ and $C_{DS}$ are considered to be independent of the input signal, from this follows that the total transistor width should be equal in both analog and digital cases. In the analog case a transistor of width $W_{analog}$ is driven with a $V_{gt_{analog}}$. In the digital case a part of the total transistor, with width $W_{digital_{on}}$, is driven with $V_{gt_{digital}}$. The other part, with width $W_{digital_{off}}$, is switched off.

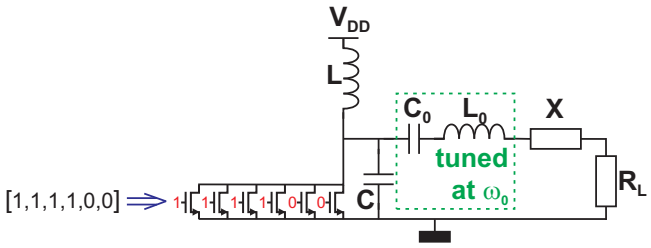



Figure 4.22: Class-E circuit with digital input

### 4.10.1 Analog input

Consider the circuit of figure 4.1, with analog $V_{gt}$. $R_{DS}$ can be expressed as:

$$R_{DS_{analog}} = \frac{1}{\mu_n C_{ox} \frac{W_{analog}}{L} V_{gt_{analog}}} \tag{4.73}$$

### 4.10.2 Digital input

In figure 4.22 a circuit is shown with digital "word" input. $R_{DS}$ can be described with the same relation as in the analog case:

$$R_{DS_{digital}} = \frac{1}{\mu_n C_{ox} \frac{W_{digital_{on}}}{L} V_{gt_{digital_{on}}}} \tag{4.74}$$

From relations 4.73 and 4.74 follows that $R_{DS}$ in both the analog and digital case is equal when:

$$W_{digital_{on}} = \frac{W_{analog}\, V_{gt_{analog}}}{V_{gt_{digital_{on}}}} \tag{4.75}$$

From the constant $C_{GD}$ and $C_{DS}$ follows:

$$W_{digital_{off}} = W_{analog} - W_{digital_{on}} \tag{4.76}$$

In the derivation above it is shown that an "analog" transistor is equivalent to a word of "digital" transistors turned on, parallel to a word of "digital" transistors turned off.

### 4.10.3 Conclusion

It is shown that an "analog" transistor can be replaced with "digital" transistors. In the current model an analog input is used to demonstrate several effects. To translate this situation to a digital input it is only needed to determinate a analog to digital mapping function. In this work this is not done because of the more "proof of concept" character.

## 4.11 General discussion

### 4.11.1 Cascode and Cgd

In this chapter a way of PA modeling with one transistor is described. The use of only one transistor upper limits the supply voltage. One possibility to increase the total PA efficiency is to increase the supply voltage, this is not possible in the single transistor PA (because of the limited breakdown voltage). If the single transistor is replaced by a cascode configuration it is possible to increase the supply voltage. Another advantage of the use of a cascode configuration is the increased isolation between input and output.
To prevent the breakdown of the two transistors it is important that the PA voltage is equally divided over both transistors.

### 4.11.2 Why add extra C?

In this work the capacitor parallel to the transistor is assumed to be only formed by the output capacitance of the transistor. In a Class-E PA often an extra capacitor is added parallel to the transistor. This is done to increase the linearity of the total capacitor (for most calculation methods a linear capacitor is required [2]). With the modeling method described in this report it is possible to do the Class-E calculations with nonlinear components, so the extra capacitor in parallel to the transistor is not needed anymore! As a result of this it is possible to increase the efficiency of the PA.

The transistor width of the PA is very large; a complex layout is needed to connect to this transistor. This layout results in extra capacitance parallel to the transistor. It is possible to include this extra capacitance without increasing the model complexity.

### 4.11.3 Antenna impedance measurement

An antenna usually has an input impedance of 50Ω. Due to the environment of the antenna this input impedance will change continue, resulting in a mistuned PA. Changing the antenna impedance is effectively the same as changing the X component in the PA. As will be mentioned in paragraph 5.3, due to a changing X component the PA voltage waveform also changes. By measuring the PA waveform realtime it is possible to calculated the antenna impedance realtime. This makes it possible to optimize the PA efficiency for the antenna impedance realtime.

## 4.12 Modeling conclusions

In this chapter a semi analytical method of PA modeling using nonlinear components was presented. With this model it is possible to predict the PA performance of PAs using nonideal components. This model makes it possible to use a more advanced inductor model, without increasing the complexity of the calculations, see paragraph 4.7.1. Using this new model it is possible to design a PA in mainstream CMOS technologies.

The $C_{GD}$ of the transistor is included in the model, to the best of the author's knowledge, analysis of the $C_{GD}$ have not been presented in literature. With this new model it is possible to investigate the influence of the input signal on the PA waveform, and a better prediction of the pre-driver power specification can be given.

The $C_{GS}$ is not included in the model. If the efficiency, or pre-driver specifications should be calculated very accurately it is needed to include $C_{GS}$ (and of course $R_{out}$ of the pre-driver) in the model. The resulting differential equation will become third order. This third order differential equation is not solvable in combination with an infinite loaded quality factor, see paragraph 4.3.3; it is only solvable in combination with a finite loaded quality factor. A model that takes both $C_{GS}$ and loaded quality factor into account is based on a fifth order differential equation; this DE is solvable.

When an infinite loaded quality factor is assumed the calculations, in the simulation at least a loaded quality factor of 10 should be used, because otherwise the difference between the calculations and the simulations is to big. For efficiency reasons however a lower loaded quality factor is wanted; the lower limit is approximately 5. This low quality factor cannot be approximated with an infinite loaded quality factor. A PA with a loaded quality factor lower than 10 can only be modeled with an more advanced model; using fourth order differential equations, see paragraph 4.3.3.

The developed model can be used in combination with non-square wave input signals. This input signal can be "traditional" analog or digital (switch more or less transistors on).

In the model the transistor is approximated with 10 states per period. Due to this limited number the voltage swing per state is relatively high, resulting in mismatch between the transistor model and the real transistor. Increasing the number of states per period will reduce this problem; the calculation time will increase however. Currently Maple is not able to handle a high number of states; implementation in another mathematical program, for example a Fortran or C code implementation, will probably solve this issue.

# Chapter 5

# Design route & Simulation results

All the calculations and simulations in this chapter are done with the circuit shown in figure 5.1, the X reactance can be either capacitive or inductive. For the pre-diver there are two possibilities; thin-oxide or thick-oxide transistors. A

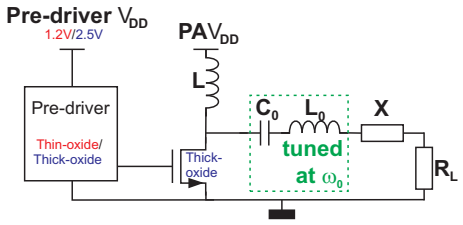



Figure 5.1: Circuit overview

summary of the design conditions described in paragraph 3.3 is given below:

- Mainstream CMOS 65
- Operating frequency: 2.4GHz
- Thick-oxide transistor in PA (length = 0.28$\mu$m)
- Output power: 100mW
- PA $V_{DD}$: 1V
- Quality factor inductor (L): 5 & 11
- Quality factor capacitor ($C_0$): $\infty$
- Quality factor inductor ($L_0$): $\infty$

As stated in paragraph 2.3, the main goal of the project is the investigation of modulation possibilities. Before the calculations on the phase modulation can be done first a type of pre-driver should be chosen, this is described in paragraph 5.1. The modulation possibilities are described in paragraphs 5.2 to 5.6.

## 5.1 Pre-driver implementation

There are two ways of implementing the Class-E pre-driver; thick-oxide and thin-oxide transistors, see figure 5.1. When thin-oxide transistors are used in the pre-driver, the pre-driver supply voltage is 1.2V; the PA transistor is driven by a 1.2V square wave input signal. With thick-oxide transistors the pre-driver supply voltage is 2.5V, resulting in 2.5V square wave PA input signal.
To decide whether thin or thick-oxide should be used calculations with both 1.2V and 2.5V square wave input signals are done. For both pre-diver implementations the optimal PA, with respect to efficiency, is calculated. Based on these calculations is decided wether thin-oxide or thick-oxide transistors are used in the pre-driver.

### 5.1.1 Optimal point determination

The efficiency of a PA (with fixed specifications like output power and frequency) depends on the three parameters $\alpha$, $k$ and $q$. To determine the optimal PA with respect to efficiency extensive calculations are done. The three parameters $\alpha$, $k$ and $q$ are varied to determine the optimal parameter values. The calculations are done for two values of the inductor quality factor: ql=5 and ql=11. A graphical representation of the efficiency as function of the three parameters $\alpha$, $k$ and $q$ is not possible; it results in a four dimensional plot. Therefore for each value of $\alpha$ the corresponding optimal values of $k$ and $q$ are calculated; resulting in a plot where the optimal efficiency is plotted as function of $\alpha$.

#### 2.5V square wave

In figure 5.2 the optimal PA efficiency, with ql=5, is shown as function of $\alpha$. As can be seen in the figure the maximum efficiency is at $\alpha = -0.4$; the corresponding values for $k$ and $q$ are -1.8 and 0.74 respectively. In figure 5.3 the efficiency is shown with ql=11. The maximal efficiency is at $\alpha = -0.6$, $k = -1.7$ and $q = 0.82$.

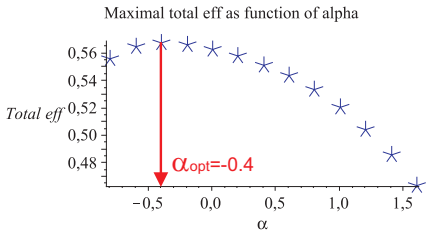



Figure 5.2: Efficiency as function of $\alpha$ @ 2.5V, ql=5

As can be seen in figures 5.2 and 5.3 the maximal efficiency is 56.8% and 74.0% for ql=5 and ql=11 respectively. For both inductor quality factors the maximal efficiency is reached for negative $\alpha$, this means that the PA voltage at the end of the period is negative. In a real transistor there is a junction between the drain and bulk; if the drain voltage is lower then approx 0.6V this junction starts

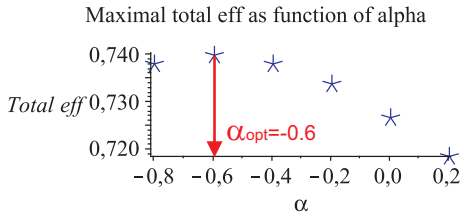



Figure 5.3: Efficiency as function of $\alpha$ @ 2.5V, ql=11

to conduct current, resulting in a decreased efficiency which is not taken into account in the previous shown calculation results. Especially when high supply voltages are used the negative $\alpha$ can become a problem. It is important that the product $\alpha V_{DD}$ is high enough ($> -0.6V$) to prevent the drain-bulk junction from conducting current.

### 1.2V square wave

In figure 5.4 the PA efficiency, with ql=5, is shown as function of $\alpha$. The maximum efficiency is at $\alpha = 0.48$, $k = -1$ and $q = 0.83$. For ql=11 the maximum is located at $\alpha = 0.2$, $k = -1.2$ and $q = 0.85$, see figure 5.5. The

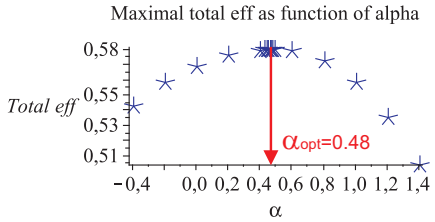



Figure 5.4: Efficiency as function of $\alpha$ @ 1.2V, ql=5

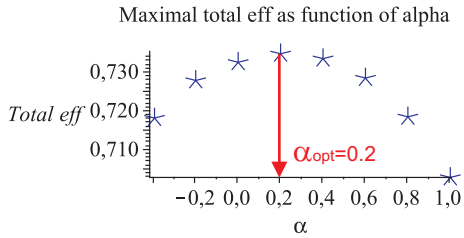



Figure 5.5: Efficiency as function of $\alpha$ @ 1.2V, ql=11

maximal efficiency is 58.0% and 73.4% for ql=5 and ql=11 respectively.

### 5.1.2 Conclusion

From the calculations it can be concluded that there is almost no difference between the 1.2V and 2.5V optimal efficiencies. In the efficiency calculations however the power consumption of $C_{GS}$ is not included, see (4.72) for the used efficiency definition. The power needed to charge and discharge $C_{GS}$ is proportional to:

$$P_{C_{gs}} \propto C_{GS} V^2 f \tag{5.1}$$

The transistor $C_{GS}$ is proportional to the transistor width, from this follows:

$$P_{C_{gs}} \propto W V^2 f \tag{5.2}$$

To make a comparison between the different PAs possible a $P_{C_{gs}}$ power factor is defined (the frequency is constant for all PAs, so this is not taken into account):

$$P_{gs_{factor}} = W[mm] V^2 \tag{5.3}$$

In table 5.1 a summary of the simulations is given, in the table the resulting transistor width and a term proportional with the power consumption of $C_{GS}$ are also shown.

Table 5.1: Overview efficiency @ 1.2V & 2.5V square wave @ ql=5 & ql=11

| simulation | efficiency | Transistor width [$\mu$m] | $P_{gs_{factor}}$ |
|---|---|---|---|
| 2.5V, ql=5 | 56.8% | 13764 | 86.0 |
| 1.2V, ql=5 | 58.0% | 15074 | 21.7 |
| 2.5V, ql=11 | 74.0% | 8763 | 54.7 |
| 1.2V, ql=11 | 73.4% | 11312 | 16.2 |

From table 5.1 can be concluded that in the case of 1.2V input signal $C_{GS}$ consumes less power than with a 2.5V input signal. Based on the reduced $C_{GS}$ power consumption is chosen for the 1.2V input signal, so the pre-driver should be made with thin-oxide transistors. An extra advantage of thin-oxide above thick-oxide is the higher bandwidth of the thin-oxide transistors.

### 5.1.3 Inductor quality factor

The optimal point determination is also done with an unrealistic high value of ql=20, for both 1.2V and 2.5V square wave input signals. The results are shown in the table below:

| simulation | efficiency | Transistor width [$\mu$m] | $P_{gs_{factor}}$ |
|---|---|---|---|
| 2.5V, ql=5 | 56.8% | 13764 | 86.0 |
| 2.5V, ql=11 | 74.0% | 8763 | 54.7 |
| 2.5V, ql=20 | 82.5% | 7659 | 47.8 |
| 1.2V, ql=5 | 58.0% | 15074 | 21.7 |
| 1.2V, ql=11 | 73.4% | 11312 | 16.2 |
| 1.2V, ql=20 | 80.9 % | 10246 | 14.7 |

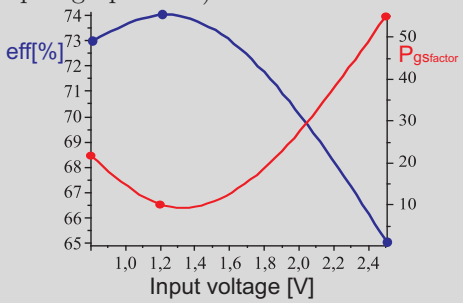
From the table it can be seen that a higher inductor quality factor results in a higher optimal efficiency. Another interesting effect is that increasing the quality factor reduces the transistor width, which results in a lower power consumption of the $C_{GS}$.

### 5.1.4 Reduced input voltage

From the calculations follows that reducing the input voltage from 2.5V to 1.2V results in a higher efficiency. To check this trend a calculation with 0.8V input signal is done; the results are shown below:

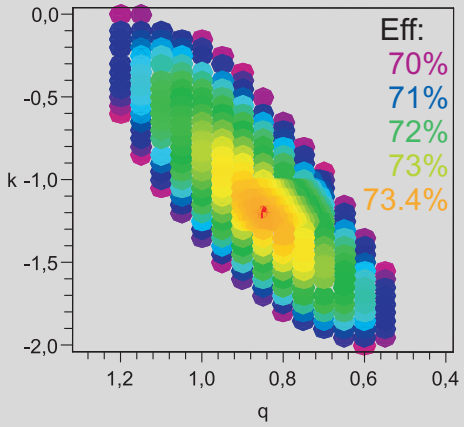
| simulation | efficiency | Transistor width [$\mu$m] | $P_{gs_{factor}}$ |
|---|---|---|---|
| 2.5V, ql=11 | 74.0% | 8763 | 54.7 |
| 1.2V, ql=11 | 73.4% | 11312 | 16.2 |
| 0.8V, ql=11 | 65.0 % | 40835 | 26.1 |

From the results can be seen that a input voltage of 0.8V results in a lower efficiency and a higher power consumption of $C_{GS}$. The figure below shows the efficiency and $P_{gs_{factor}}$ as function of the input voltage. It can be seen that there is a trade off between the PA efficiency and the $C_{GS}$ power consumption; there is an optimal input voltage (which is dependent of the inductor quality factor as is shown in paragraph 5.1.3).



### 5.1.5 Sub optimal parameters

From figure 5.5 it can be concluded that the maximal efficiency is reached at $\alpha = 0.2$ (for this specific situation). Due to component variations a PA implementation will never be exactly the same as in the calculations. So the parameters will be slightly different from the calculated values. From figure 5.5 can already be concluded that variations in $\alpha$ results in almost the same PA efficiency; in the range $\alpha = 0...0.4$ the efficiency only changes 0.3%. In the figure below the efficiency is shown for different values of $k$ and $q$ at a fixed $\alpha = 0.2$.




As can be seen in the figure there is a large range of $q$ and $k$ which results in almost the same efficiency. From this can be concluded that the efficiency is relative independent of parameter variations.

## 5.2 Tuning point; Overview

Due to the DAC integration into the PA, see figure 2.2, there is no analog phase information in the pre-diver clock anymore. The output phase should be controlled in another way. In the ideal case the output phase can be varied between 0 and 360 degrees, while keeping the output power and the efficiency constant. The output phase of a PA is determined by the whole circuit; varying one or more components results in another output phase, PA efficiency and output power. In the next paragraphs the relation between varying component values, the output phase and other PA specifications are discussed.

In a PA circuit the number of tuning possibilities are limited; it is not possible to tune for example inductors without using dedicated (MEMS) processes. In figure 5.6 possible tuning points of a typical Class-E circuit are shown.

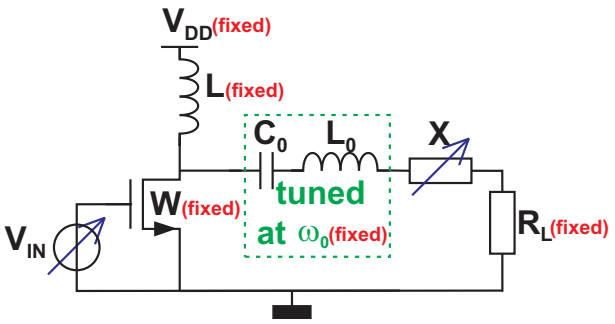



Figure 5.6: Overview tuning points Class-E circuit

The output phase of the PA should be varied while keeping the following parameters and components constant:

- Inductor values
- Transistor width
- $R_{load}$ & Output power
- Supply voltage
- Frequency (and thus $C_0$ and $L_0$)

As can be seen in figure 5.6 there are only two possibilities left that can be used as tuning input:

- Varying reactance X (only when capacitor).
- Varying input signal.

The output phase ($\varphi_{OUT}$) of the PA is determined by the phase of the PA waveform ($\varphi_{PA}$) and the ratio between the impedance of the X reactance and the load resistance ($\varphi_X$). The output phase can be influenced by changing the phase of the PA waveform and or the ratio between the X reactance and the load resistance. This can be done by either changing the X reactance or the input signal.

### 5.2.1 Calculation method

Using the model described in chapter 4 a PA realization is calculated, resulting in a PA waveform, $p$ and $\varphi$. From this $p$ and the specified output power, $R_{load}$ is calculated. The X reactance is calculated from the PA waveform, using the fourier components of the PA waveform. In the differential equation describing the circuit (4.44) the X reactance is not included; only the current through the X reactance is specified. Due to this modeling method it is not possible to calculate a PA voltage that belongs to a specified X reactance. So it is not possible to calculate output phase variations due to X reactance variations.

### 5.2.2 Conclusion

With the developed model it is not possible to reverse calculate the PA output phase variations that correspondents to X reactance variations. The main problem is the assumption of the sinusoidal output current, as a result of this assumption the X reactance is not included in the differential equations describing the PA voltage. These calculations will become possible if a more advanced model is made using fifth order differential equations to describe the PA.

It is however possible to do simulations with varying X reactance and input signals while the circuit is kept the same. In sections 5.3 and 5.4 the result of these simulations are shown.

## 5.3 Tuning point; Varying reactance X

In this section the influence of a varying X reactance on the output phase is investigated. In paragraph 5.1.2 it was concluded that a pre-driver with thin-oxide transistors results in the highest efficiency; the input signal is a square wave of 1.2V. From the simulations in paragraph 5.1.1 follows that for ql=11 the maximum efficiency is located at $\alpha = 0.2$, $k = -1.2$ and $q = 0.85$. The corresponding PA circuit is used for the rest of the simulations in this paragraph, see figure 5.7 for an overview of the circuit.

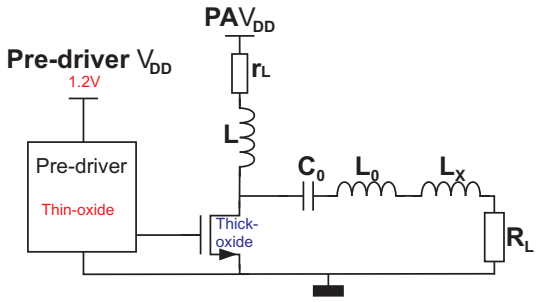



Figure 5.7: Circuit used for simulations

The used component values are:

- L = 0.578nH
- $r_L$ = 0.792Ω (ql=11)
- Transistor width = 11312.4$\mu$m
- Transistor length = 0.28$\mu$m (thick-oxide)
- $C_0$ = 1.30pF
- $L_0$ = 3.37nH
- Initial value $L_x$ = 0.323nH
- $R_L$ = 5.08Ω

A summary of the other settings are:

- PA $V_{DD}$ = 1V
- Pre-driver $V_{DD}$ = 1.2V (thin oxide pre-driver)
- $\alpha = 0.2$
- $k$ = -1.2
- $q = 0.85$
- $QL = 10$
- Input signal: 1.2V square wave (thin oxide pre-driver)

The $L_x$ is varied from 0.194nH to 0.453nH (initial value of $L_X$ ±20%), the results are shown in figures 5.8 and 5.9. In these simulations inductor $L_X$ is varied, which is very difficult in integrated PA realizations. It is however possible to use a constant inductor with a tunable capacitor in series.

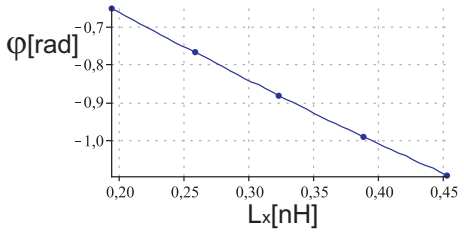



Figure 5.8: Output phase as function of $L_x$

In figure 5.8 the PA output phase is shown as function of $L_x$. It can be seen that there is a linear relation between $L_x$ and the output phase. The whole range can be used for output phase tuning.

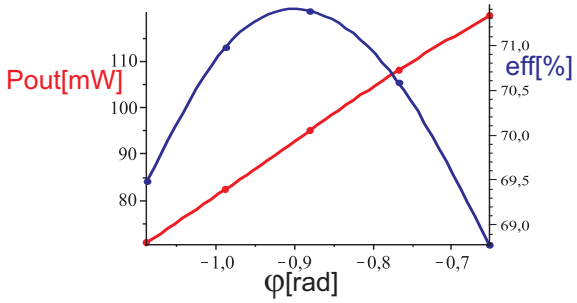



Figure 5.9: Output power & efficiency as function output phase while varying the X reactance

Figure 5.9 shows the output power and the PA efficiency as function of the output phase. The efficiency decreases when the output phase deviates more from its initial value (-0.88rad). The useful range with respect to the efficiency is limited to approximately -1.1rad to -0.7rad; the efficiency drop is maximal 3% in this range. As can be seen in figure the output power is far from constant over the useful range; it varies from 70mW to 115mW.
The output phase range -1.1rad to -0.7rad correspondents with $L_x$ = 0.22nH to 0.45nH. The maximal achievable phase variation due to a varying $L_x$ is approximately 0.4rad (22.9 degrees).

### 5.3.1 Conclusion

From the simulations it follows that the maximal achievable phase shift due to a varying $L_x$ is approximately 0.4rad (22.9 degrees). The output power is however not constant. As can be seen in figure 5.9 results more phase shift in more output power.

## 5.4 Tuning point; Input waveform variations

Till now all the simulations where done with square wave input signals. In this section the input waveform shape (not phase) is varied. As starting point again the maximal efficiency parameters $\alpha = 0.2$, $k = -1.2$ and $q = 0.85$ are used. In the used model the input signal is approximated with 10 samples. The input signal is varied by changing the input samples, for these variations extra parameters ($\gamma_1$, $\gamma_2$, $\gamma_3$) are defined, see figure 5.10.

$$S_1 \& S_5 = V_{amp}\,\gamma_1 \tag{5.4}$$
$$S_2 \& S_4 = V_{amp}\,\gamma_2 \tag{5.5}$$
$$S_3 = V_{amp}\,\gamma_3 \tag{5.6}$$
$$S_6 \& S_{10} = V_{amp}(1-\gamma_1) \tag{5.7}$$
$$S_8 \& S_9 = V_{amp}(1-\gamma_2) \tag{5.8}$$
$$S_7 = V_{amp}(1-\gamma_3) \tag{5.9}$$

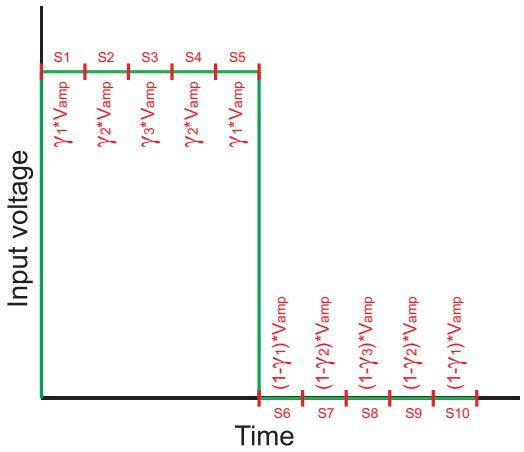



Figure 5.10: Overview $\gamma$ definitions

To investigate the possibilities of this technique first the input signal is varied in a quite large range. For each input signal an optimal PA (with respect to efficiency) is calculated, resulting in different PA realizations with different component values. From the results of these calculations some "linear regions" are extracted; in these regions the phase change technique can be used. This operating area determination is done in paragraph 5.4.1. In paragraph 5.4.2 the results of the operating area determination are discussed.

### 5.4.1 Operating area determination

In this work only the parameter $\gamma_1$ is varied between 0 and 1; the resulting PA voltage and the corresponding PA circuit is calculated; the phase of the input signal and the $V_{amp}$ are kept constant. The calculations are done with a quality factor of 5 and 11. First of all an "operating area" for the phase changing is extracted.

#### Output phase

In figure 5.11 the output phase as function of $\gamma_1$ is shown. As can be seen in the figure the output phase can be influenced by varying the input signal. If the resulting output phase for both ql=5 an ql=11 are compared it can be seen that for $\gamma_1 = 0.75...1$ the phase change is almost independent of ql.

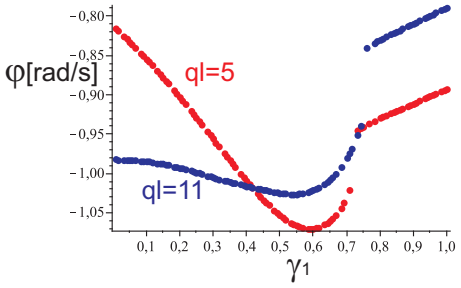



Figure 5.11: Output phase as function of $\gamma_1$

In the figures 5.11 to 5.14 some PA properties as function of $\gamma_1$ are shown. In all these results there are big discontinuities. These discontinuities are caused by the converging character of the algorithm; due to the limited number of states in the model the transistor approximation is not sufficient accurate at these values of $\gamma_1$. Increasing the number of states in the model probably solves this effect.

#### Efficiency

It is important that the efficiency is relatively constant in the tuning range. In figure 5.12 the efficiency is shown as function of $\gamma_1$. As can be seen in the figure, the range $\gamma_1 = 0.75...1$ is the most interesting range with respect to efficiency; the efficiency stays almost constant in the whole range (even slightly higher). From efficiency point of view follows that the range $\gamma_1 = 0...0.75$ cannot be used for output phase changing; the resulting efficiency is too low.

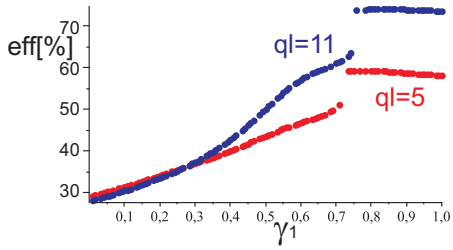



Figure 5.12: Efficiency as function of $\gamma_1$

### Component values

It follows from both the phase and efficiency calculations that the range $\gamma_1$ = 0.75...1 is suitable for phase modulation, by varying the input signal. It is however also necessary that the component values are relatively constant in this range. Therefore in figures 5.13 and 5.14 the inductor value and the transistor width are shown as function of $\gamma_1$. From the figures it can be seen that in the

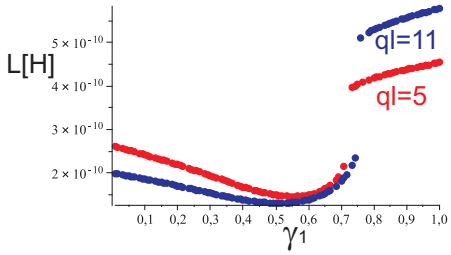



Figure 5.13: Inductor value as function of $\gamma_1$

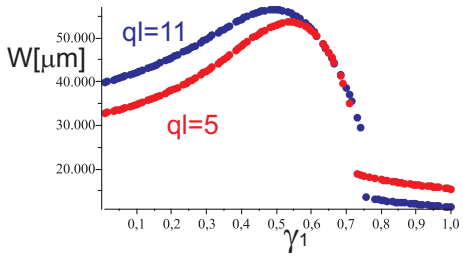



Figure 5.14: Transistor width as function of $\gamma_1$

range $\gamma_1$ = 0.75...1 the change in component values is relative small. From this can be concluded that the range $\gamma_1$ = 0.75...1 is a kind op “operating area” for the input varying technique.

### 5.4.2 Operating area

From the figures 5.11 to 5.14 it can be seen that the change in PA performance and PA circuit is relatively low in the range $\gamma_1 = 0.75...1$. The midpoint of this range is used for further simulations; the resulting PA circuit with $\gamma_1 = 0.875$ is used as initial circuit.

### 5.4.3 Simulations

It is not possible to calculate the exact phase change as function of the varying input signal, it is however possible to do circuit simulations. For these simulations the circuit that results from $\gamma_1 = 0.875$ is used, see figure 5.7. The used component values are:

- L = 0.553nH
- $r_L$ = 0.758Ω (ql=11)
- Transistor width = 12121.8$\mu$m
- Transistor length = 0.28$\mu$m
- $C_0$ = 1.48pF
- $L_0$ = 2.98nH
- $L_X$ = 0.319nH
- $R_L$ = 4.49Ω

A summary of the other settings are:

- $V_{DD}$ = 1V
- $\alpha = 0.2$
- $k$ = -1.2
- $q = 0.85$
- $QL = 10$
- $V_{amp}$ = 1.2V

Using this circuit the $\gamma_1$ is varied, the results are shown in figures 5.15 and 5.16.

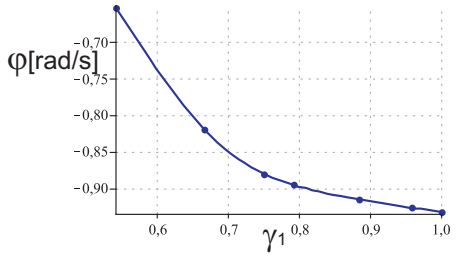



Figure 5.15: Output phase as function of $\gamma_1$

Figure 5.15 shows that the output phase can be influenced by varying $\gamma_1$. In the range $\gamma_1 = 0.65...1$ the relation between $\gamma_1$ and the output phase is approximately linear.

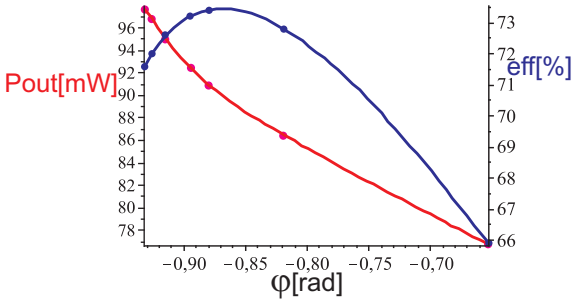



Figure 5.16: Output power & efficiency as function output phase while varying $\gamma_1$

In the range $\gamma_1 = 0.65...1$ the output phase can be influence in a controlled way. Figure 5.16 shows the output power and efficiency as function the output phase: the efficiency is relatively constant in the range -0.95rad to -0.75rad. In the whole range the maximal efficiency decrease is 3%. It can be seen that the output power is less than the wanted 100mW output power. In the range -0.95rad to -0.75rad the output power varies between 98mW to 82mW. The maximal achievable phase variation due to a varying $\gamma_1 = 0.65...1$ is approx 0.2rad (11.5 degrees).

### 5.4.4 Conclusion

Simulations are done around the calculated operating point. In the range $\gamma_1 = 0.65...1$ a phase variation of approximately 0.14rad (11.5 degrees) is achievable. The output power is however not constant in the whole range. As can be seen in figure 5.16 results more phase shift in less output power.

## 5.5 Tuning point; Conclusion

The developed model cannot be used for reverse calculating the PA voltage while specifying component values. By including the X reactance in the used differential equations the PA voltage can be calculated. Due to the model limitations it is not possible to prove mathematically that either the varying X reactance or the varying input voltage can be used for phase modulation.

From the calculations with varying input signals can be concluded that it is possible to influence the output phase by varying the input signal. Due to model limitations it is however not possible to calculate the exact phase change.

Simulations are done with varying input signals. In the range $\gamma_1 = 0.65...1$ a phase variation of approximately 8.0 degrees is achievable. In the whole range the PA efficiency is relative constant (maximal 3% decrease), the output power increases from 86mW to 98mW.

By tuning the X reactance the output phase can be influenced approximately 22.9 degrees. Over the whole tuning range the efficiency is relative constant (maximal 3% decrease), the output power decreases from 115mW to 75mW.

By tuning the X reactance the output phase can be influenced. The output phase can also be influenced by varying the input signal. In figure 5.17 the output power is shown as function of the output phase; both varying input signal and varying X reactance effects are shown in one figure. From the figure can

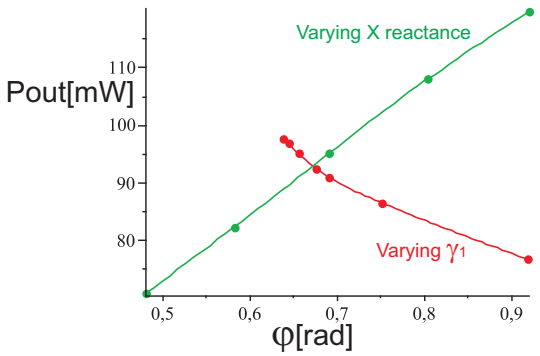



Figure 5.17: Output power as function output phase while varying $\gamma_1$ and the X reactance

be seen that if both techniques are combined it may be possible to influence the output phase while keeping the output power constant. It is however also possible to keep the output phase constant while varying the output power. So if both techniques are combine it is possible to control both the output power and output phase, with a small penalty in efficiency.

## 5.6 Extra tuning possibilities

The total required phase change is from 0 to 360 degrees, the variations in both input signal and X reactance does not results in enough output phase variation; maximal 20 degrees is possible. There are two possibilities to increase the tuning range:

- Vary both input signal and X reactance over a bigger range. This will result more variations in the output phase. The total efficiency however decreases.
- Change the phase of the input signal. The input signal is updated 10 times per period, so there are 10 input samples. The "phase" of the input signal can be changed by delaying the input signal for example by one sample.

This last technique is discussed in more detail in the next paragraph.

### 5.6.1 Input phase variations

With use of the digital pre-driver it is possible to control the amplitude of each sample of the input signal, see paragraphs 4.10 and 7.3.1. By delaying the input waveform for example with 1 sample it is possible to change the output phase, see figure 5.18. The input signal is described with 10 samples, so it is possible

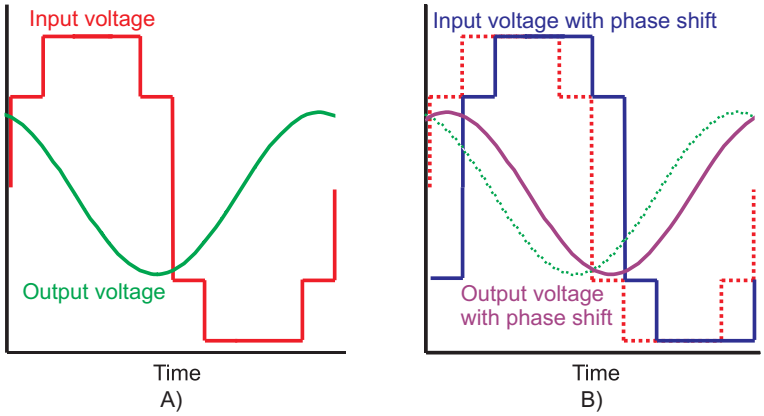



Figure 5.18: Overview input phase variations; A) original phase, B) new phase

to change the PA output phase in steps of $\frac{360}{10} = 36$ degrees with this technique.

### 5.6.2 Total phase variations

By varying the X reactance and the input signal waveform a phase variation of approximately 20 degrees can be archived. By changing the input signal phase a phase variation of 36 degrees can be archived. By combining both techniques the output phase tuning range can be increased, see figure 5.19. In the figure it can be seen that not the whole output phase range is covered with the used variation techniques; there are some blind spots. There are several possibilities for increasing the tuning range:

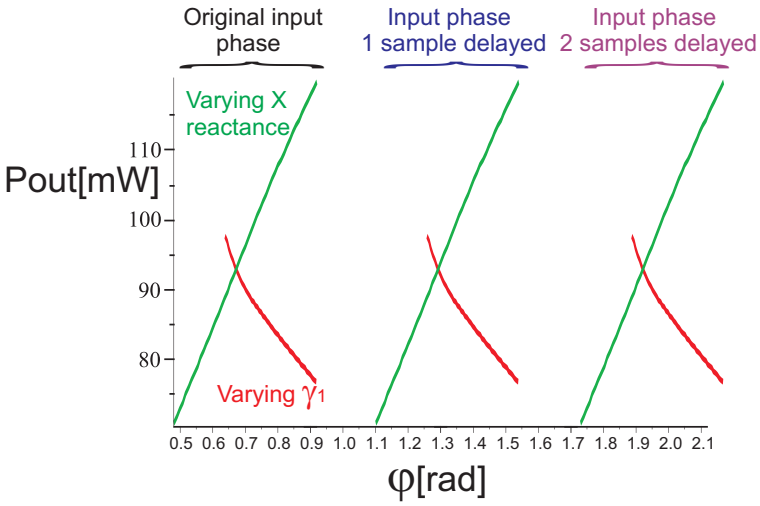



Figure 5.19: Output power as function output phase while varying $\gamma_1$, X reactance and the input signal phase

- Vary both input signal and X reactance over a bigger range. This will result more variations in the output phase for each input phase. The maximal decrease in efficiency will be more then 3%.
- Increase the sampling rate of the input signal. Increasing the sampling rate results in a higher speed digital pre-driver, resulting in a less efficient pre-driver.
- Use time multiplexing techniques. With this method a kind of PWM modulation is used for the input signal. It is however not clear if this technique can be used; the Class-E PA circuit should act as a low pass filter with respect to the input phase. See paragraph 7.2 for more details.

## 5.7 Conclusion

Both the output power and output phase can be controlled by varying he input signal and the X reactance. Both effects are shown with help of simulations; the developed model is not able to confirm the results. From the simulation results can be extracted that it is possible to vary the phase at a constant output power or varying the output power at a constant phase. It is however almost impossible to find these solutions using (iterative) simulations; a more advanced model should be developed to calculate these solutions. In this new model the X reactance should be included in the differential equations describing the circuit; resulting in fourth order differential equations.

# Chapter 6

# Conclusions

Using one PA for several applications requires a PA which is able to adapt its specifications to satisfy the different standards. The specifications that should be controllable are; frequency, output power, modulation techniques and output spectrum. Both the frequency and output power can be controlled by only tuning capacitors [4]. In this report it is shown that both output phase and output power can be controlled by varying the input signal and the X reactance.

The developed model can be used to design a PA with nonlinear components. The PA transistor is modeled as a combination of nonlinear capacitors and a nonlinear resistor. The equivalent component values can be extracted from any process; it is very simple to compare the performance of different (CMOS) processes. This model makes it possible to use a more advanced inductor model, without increasing the complexity of the calculations, see paragraph 4.7.1. With this model it is possible to design a PA with nonlinear components without doing extensive simulations, only a couple of calculations are needed to find the optimal efficiency.

A pre-driver implemented with thin-oxide transistors is preferred above a thick-oxide transistors. The efficiencies of both implementations are equal, but the needed power to drive the PA transistor is lower in the thin-oxide case. Another advantage of the thin-oxide pre-driver is the higher bandwidth. From the calculations also follows that in case of thick-oxide transistors increasing the supply voltage results in less efficiency. This is due to a negative drain voltage at the end of the period resulting in a conducting drain-bulk junction, see paragraph 5.1.1.

A higher inductor quality factor results in a higher efficiency and in a smaller transistor, so increasing the inductor quality factor increases the efficiency and decreases the power needed to drive the PA transistor.

The output phase and output power can be controlled by varying the input signal shape and the X reactance; a phase shift of 20 degrees can be achieved very simple. An additional phase shift of 36 degrees (360 degrees divided by the number of digital input samples) can made by changing the phase of the input signal. Combining both techniques it is possible to control both output power

and output phase over almost the whole range. There are however some bind spots in the tuning range, there are several possibilities to remove these blind spots, see paragraphs 5.6.2 and 7.2.

# Chapter 7

# Recommendations

One of the main goals of the project was to make a PA that is able to adapt its specifications realtime. The specifications that should be controllable are:

- Frequency (done by B.Verhoef [4])
- Output Power (done by B.Verhoef [4])
- Modulation techniques (this work)
- spectrum of output signal (not done yet)

Both frequency and power control where investigated by B.Verhoef [4]. Output power and output phase control is described in this report, but not all important specifications are described. In the next section an overview of the items not described in this work are given. The PA output spectrum control is not investigated during the project; a couple of interesting linearity issues are described in this chapter.

## 7.1 Modulation techniques

### 7.1.1 Amplitude vs phase modulation

In most modern applications both the amplitude and phase modulation are used. In this work only the phase modulation was investigated; it is assumed that the amplitude modulation can be done by varying the output power, some alternative possibilities for amplitude modulation are:

- Supply voltage modulation (EER)
- Input signal variation
- Switch more or less PAs in parallel

The items listed above are not investigated in the project.

### 7.1.2 Phase modulation calculations

To design a PA that is able to change its output phase a model should be developed that is able to calculate the PA waveform given the component values. The developed model cannot be used for this. The model can be expanded for these calculations by including the X reactance in the differential equations describing the PA voltage (see paragraph 5.3). The resulting differential equations that describe the PA circuit are fourth order, it is not clear if the modeling method described in this work can be used to find the PA realization; the sinusoidal current assumption cannot be used anymore.

### 7.1.3 Modulation bandwidth

To transmit data a certain bandwidth is needed; switching between the different output phases should be done fast enough. This switching speed is not investigated in this project. The switching speed is dependent of the quality factor of the PA circuit, a lower quality factor results in a higher switching speed (higher bandwidth) but also in a decreased efficiency. This trade off between bandwidth and efficiency should be investigated in more detail. Therefore PSS (or transient) simulations covering several periods should be done.

## 7.2 Blind spot removal

From figure 5.19 can be seen that there are some blind spots in the tuning range, one possible way of removing these blind spots is the use of PWM modulation of the phase of the input signal, see paragraph 5.6.2. This PWM technique should be investigated in more detail.

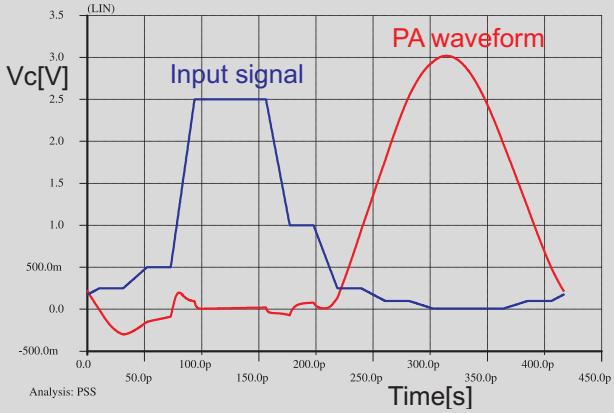
## 7.3 Output spectrum

In this work the loaded quality factor is not included in the model, as a result of this it is not possible to do calculations which include the output spectrum. In the model the assumption of a sinusoidal output current is used, if the loaded quality factor is included in the model this assumption cannot be used anymore, therefore another calculation method should be used.

### 7.3.1 Advanced $\gamma$ definition

The parameters ($\gamma_1$, $\gamma_2$, $\gamma_3$) as defined in paragraph 5.4 can only be used in combination with a symmetric input signal. When output spectrum optimalization of a PA is important probably asymmetric input signals will be used. For these simulations another parameter definition should be used, for example for each input sample one $\gamma_n$.

Some simulations to check the output spectrum are already done. One "lucky shot" is shown below; the input signal is changed to a more "sinusoidal" wave. The other setting are: $\alpha = -0.4$, $k = -1.8$, $q = 0.74$, ql=5 and QL=10.




The PA output spectrum is determined by looking at the suppression of the second and third harmonics, the results are shown in the table below. As reference the simulation of paragraph 4.9.3 is shown.

| Simulation | Suppression | | Efficiency |
|---|---|---|---|
| | Second harm. | Third harm. | |
| square wave (reference) | 22.9dB | 36.6dB | 56.8% |
| "lucky shot" | 17.8dB | 44.2dB | 31.0% |

From the simulation results it can be seen that it is possible to increase the linearity of the PA (especially third harmonic suppression) at cost of the efficiency. The result that is shown here is just a random simulation to show that it is possible to influence the linearity. From this again the power of the used modeling method can be seen; if the model is extended with the loaded quality factor it is possible to investigate the trade off between the output spectrum and efficiency without doing extensive simulations.

### 7.3.2 Efficiency

The minimum loaded quality factor that is needed to satisfy the out of band specifications is dependent of the PA linearity. As is shown in paragraph 4.3.3 the efficiency is also dependent of the loaded quality factor. So the linearity of the PA influences the total PA efficiency. Calculations that include these effects can only be done when the loaded quality factor is included in the model. This trade off between PA linearity and PA efficiency should be investigated in more detail.

## 7.4 General discussion

During the project some general points are not taken into account, these are described here.

### 7.4.1 Reduce number of input samples

To reduce the power consumption of the digital pre-driver the "oversampling frequency" of the digital input can be decreased. This reduces the number of possible input waveforms, so the phase modulation can be done less accurately, see paragraph 7.2. However if the quality factor of the PA circuit is high enough it is possible to use time multiplexed input signals to make more accurate phase modulation possible, this should be investigated in more detail, see paragraph 7.2.

### 7.4.2 Transistor breakdown

In this work the transistor breakdown is not taken into account, in future models this should be taken into account. There are several possibilities that can influence the breakdown process:

- Use cascode transistor configuration.
- Detect defect transistors and disable them, like is shown in [7]

### 7.4.3 Inductor layout

The huge transistor dimensions results in large interconnects between the transistor and the on-chip inductor, this limits the inductor quality factor. A new type of on-chip inductor layout that reduces the interconnect length should be developed.

### 7.4.4 Inductor quality factor

As expected results a higher quality factor of the inductor in a higher PA efficiency, but also in less stringent pre-driver specifications. So for both the PA and the pre-driver a higher quality factor is beneficial. Therefore the possibilities of high quality factor inductors should be investigated, for example flip-chip implementations.

# Bibliography


[1] N. O. Sokal and A. D. Sokal, "lass E, a new class of high efficiency tuned single-ended switching power amplifiers" *IEEE J. Solid-State Circuits,* vol. SC-10, pp. 168176, June 1975.

[2] H.Sekiya, Y.Arifuku, H.Hase, J.Lu, T.Yahagi, "Investigation of Class E Amplifier with Nonlinear Capacitance for Any Output Q and Finite DC-Feed Inductance", *IEICE TRANS. FUNDAMENTALS,* VOL.E89A, NO.4 APRIL 2006

[3] M.Acar, A.J.Annema, B.Nauta, "Generalized analytical design equations for variable slope class-e power amplifiers" *Proceedings of 13th IEEE International Conference on Electronics, Circuits and Systems,* 10-13-2006, Nice, France. pp. 431-434. IEEE Computer Society Press. ISBN 1-4244-0395-2.

[4] B.Verhoef, "A new tuning and power control mechanism for class-e power amplifiers" *ICD - University of Twente*, Report nr: 067.3188.

[5] M.Acar, A.J.Annema, B.Nauta, " Analytical Design Equations for Class-E Power Amplifiers with Finite DC-Feed Inductance and Switch On-Resistance" *IEEE International Symposium on Circuits and Systems 2007,* 27-30 May 2007, New Orleans, LA. pp. 2818-2821. ISBN 1-4244-0921-7.

[6] M.Acar, A.J.Annema, B.Nauta, "Variable-Voltage Class-E Power Amplifiers" *The IEEE MTT-S International Microwave Symposium 2007 (IMS 2007),* 03-08-June 2007, Hawaii, Honolulu. pp. 1095-1098.

[7] M.Acar, A.J.Annema, B.Nauta, "Digital Detection of Oxide Breakdown and Life-Time Extension in Submicron CMOS Technology" *International Solid-State Circuits Conference (ISSCC 2008, IEEE)*,February 3-7, 2008.

[8] M.Acar, A.J.Annema, B.Nauta, "Analytical Design Equations for Class-E Power Amplifiers" *Theory of Circuits and Systems-I(IEEE, TCAS-I)*, to be published December 2008.

[9] Personal communication with M.Acar.

[10] Personal communication with R.Shrestha.

# Appendix A

# Connection DEs advanced model

## A.1 Connecting DEs; Constant charge

To explain the charge injection effect in more detail the Class-E model of figure 4.13 is simplified to the circuit shown in figure A.1 at the switching moments.

Consider the time point $T_n$; At time $T_n^-$ the total charge on the system is

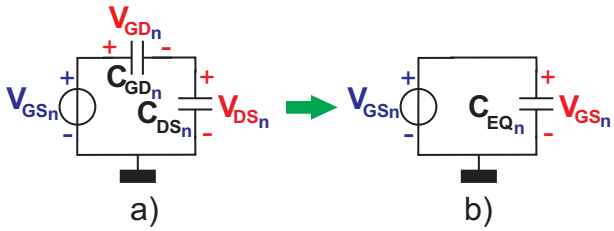



Figure A.1: Circuit simplification for charge injection effect

$V_{gs_n}(T_n^-)C_{EQ_n}$. At time $T_n^+$ the total charge on the system is $V_{GS_{n+1}}(T_n^+)C_{EQ_{n+1}}$. From this follows the total charge change at the switching moment:

$$\Delta Q_{eq_n} = V_{GS_{n+1}}(T_n^+)C_{EQ_{n+1}} - V_{gs_n}(T_n^-)C_{EQ_n} = Q_{eq_{n+1}}(T_n^+) - Q_{eq_n}(T_n^-) \tag{A.1}$$

The capacitors $C_{GD_n}$ and $C_{DS_n}$ are connected in series, so the charge change due to a change in $V_{GS}$ is equal for both capacitors:

$$\Delta Q_{eq_n} = \Delta Q_{gd_n} + \Delta Q_{ds_n} = 2\Delta Q_{gd_n} = 2\Delta Q_{ds_n} \tag{A.2}$$

From this follows:

$$\Delta Q_{eq_n} = 2\,Q_{ds_{n+1}}(T_n^+) - 2\,Q_{ds_n}(T_n^-) \tag{A.3}$$

From the combination of relation A.1 and A.3 follows:

$$Q_{eq_{n+1}}(T_n^+) = Q_{eq_n}(T_n^-) + 2\,Q_{ds_{n+1}}(T_n^+) - 2\,Q_{ds_n}(T_n^-) \tag{A.4}$$

This can be rewritten into:

$$Q_{gd_{n+1}}(T_n^+) - Q_{ds_{n+1}}(T_n^+) = Q_{gd_n}(T_n^-) - Q_{ds_n}(T_n^-) \tag{A.5}$$

Finally this results in:

$$\begin{aligned} V_{C_{n+1}}(T_n^+) &= V_{C_n}(T_n^-)\,\Delta tot_n\Big(gdtot_n + dstot_n\Big) \\ &\quad -V_{gs_n}\,\Delta tot_n\,gdtot_n + V_{gs_{n+1}}\,gdtot_{n+1} \end{aligned} \tag{A.6}$$

With:

$$\begin{aligned} \Delta tot_n &= \frac{C_{GD_n} + C_{DS_n}}{C_{GD_{n+1}} + C_{DS_{n+1}}} \\ gdtot_n &= \frac{C_{GD_n}}{C_{GD_n} + C_{DS_n}} \\ dstot_n &= \frac{C_{DS_n}}{C_{GD_n} + C_{DS_n}} \end{aligned}$$

The relation shown in A.6 is one of the two relations that describes the initial condition problem. The second relation will be derived in the next section.

## A.2 Connecting DEs; Constant inductor flux

From the continuity of flux at the switching moments follows (see relation 4.16):

$$I_{S_n}(T_n^-) + I_{C_{ds_n}}(T_n^-) + I_{C_{gd_n}}(T_n^-) = I_{S_{n+1}}(T_n^+) + I_{C_{ds_{n+1}}}(T_n^+) + I_{C_{gd_{n+1}}}(T_n^+) \tag{A.7}$$

Substituting the currents gives:

$$\begin{aligned} &\frac{1}{R_{DS_n}}\,V_{C_n}(T_n^-) + \left(C_{GD_n}\left(\frac{dV_{C_n}(t)}{dt}\right) + C_{DS_n}\left(\frac{d\big(V_{C_n}(t) - V_{GS_n}\big)}{dt}\right), \{t = T_n^-\}\right) = \\ &\frac{1}{R_{DS_{n+1}}}\,V_{C_{n+1}}(T_n^+) + \left(C_{GD_{n+1}}\left(\frac{dV_{C_{n+1}}(t)}{dt}\right) + C_{DS_{n+1}}\left(\frac{d\big(V_{C_{n+1}}(t) - V_{GS_{n+1}}\big)}{dt}\right), \{t = T_n^+\}\right) \end{aligned}$$

During one time interval $V_{GS}$ is constant, so $\frac{dV_{GS}}{dt} = 0$, this results in:

$$\begin{aligned} &\frac{1}{\beta_n}\,V_{C_n}(T_n^-) + \left(\frac{dV_{C_n}(t)}{dt}\,\{t = T_n^-\}\right) = \\ &\frac{1}{\Delta tot_n}\left(\frac{1}{\beta_{n+1}}\,V_{C_{n+1}}(T_n^+) + \left(\frac{dV_{C_{n+1}}(t)}{dt}\,\{t = T_n^+\}\right)\right) \end{aligned} \tag{A.8}$$

With this relation is it possible to solve the second initial condition constant.