
# MICROWAVE POWER AMPLIFIER DESIGN USING STACK TOPOLOGY

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# 1. INTRODUCTION

Power amplifiers for radar applications require a relatively wide bandwidth (for example from 8.0 -12 GHz) and need to deliver as much output power as possible. Therefore these amplifiers are designed to the limit of what is offered by the used processing technology. The main limit is the voltage breakdown of the transistors. For typical GaAs processing technologies this gate-drain voltage breakdown limit is around 16 to 20 V, and typical drain bias voltage is around 8 V.

In standard class- AB amplifier designs the voltage swing at the output of the transistors is around 2 times the drain bias. Therefore the maximum drain bias is around half of the breakdown voltage limit (with some correction for the knee region and extra margin for reliability). This maximum drain bias (together with the maximum current) defines the maximum output power.

Given a fixed technology and transistor size the current cannot be increased. The only way to increase the output power any further is to increase the voltage swing. One way of doing this is to use a cascode transistor: the combination of a common gate transistor (either as two separate transistors or as one dual gate transistor). This approach is often used in low voltage CMOS technology, where the bias voltage is limited to only 1.1 V

This approach is also often used in very high frequency designs, where the gain offered by the cascode is higher than that of a single common source transistor. A cascode configuration also offers more bandwidth and is therefore often applied in very wide band distributed amplifiers.

In this thesis following study questions will be investigated.

- For what applications are cascodes currently used, and why? (What is the theory behind cascodes?)
- Can cascode transistors be used to increase the output power of microwave power amplifiers in the range of S- band (2 to 4 GHz)?
- Are cascode devices useful for other operating classes, such as Class-E, Class-F, etc., where higher drain voltage peaks can occur?
- Can a microwave power amplifier with cascodes offer more bandwidth (while delivering at least the same output power and efficiency) than standard power amplifiers (using only common source devices)?
- What specific modeling is required for cascodes (especially for the common-gate device)?
- What implementation of cascodes is most useful: 2 separate devices (common source + common gate, or a dual-gate device)?
- Demonstrate the use of cascodes by designing a microwave integrated power amplifier in GaAs technology

To be able to answer the above described research questions, literature information will be provided together with simulation results in ADS. Following design goals will be achieved with employing aforementioned cascode concept at S band.

## 1.1 GOAL OF DESIGN

Increase the output power of microwave power amplifiers and/or increase the maximum Power Added Efficiency,

For:

• Microwave (>2 GHz) integrated power amplifiers (MMICs)

• In GaAs technology ( 0.5um pHEMT, TNO model)

Target specifications

For S-band Bandwidth: 2.9 – 3.5 GHz

We start with background information about the power amplifiers for radars.

## 1.2 ACTIVE DEVICE TECHNOLOGIES IN POWER AMPLIFIERS FOR RADAR APPLICATIONS

There are several active device technologies that are mostly used in radar applications. Most important technologies that are used are based on GaAs, LDMOS and GaN which is the new generation amplifier technology.

### LDMOS-based Amplifiers

LDMOS is an enhanced MOSFET structure especially suited for high power applications. It is used from point-to-multipoint communications to Radar. The most pervasive application is in cell phone base-stations. [5]

These technologies are best known to operate with supply voltages of 28V with recent improvements allowing 50V operation

LDMOS technology works well up to around 3.5 GHz. The intrinsic parasitic capacitance characteristics of LDMOS limit the frequency and bandwidth performance as well as its power-handling capabilities. [4] Therefore these types of technologies are less attractive for high frequency radar applications.

## GaAs-based Amplifiers:

In today radar systems GaAs is the one of the most used technology. GaAs-based amplifiers provide high-efficiency and that operate in microwave and millimeter frequency ranges operating from supply voltages ranging from 5V to 28V. [28]

Higher power radar applications require devices with higher power density. For these kinds of applications GaAs device has power density limitation. Therefore power combining is indispensable for those applications. GaN has better physical properties than GaAs in the sense of bandgap and power density which omit these limitations of GaAs.

## GaN- based Amplifiers

As mentioned before GaN technology has a very high power density which is about ten times higher than the GaAs devices [32]. This higher density results in a smaller transistor die with higher output. Compared to silicon LDMOS FETs and GaAs MESFETs of similar output power, GaN HEMTs have smaller parasitic capacitances. [28]

The wide bandgap character of GaN results in a higher breakdown voltage and allow for a supply voltage up to 1000 volt. It is the best candidate for the next-generation power amplifiers for radar applications today. But the cost is the main drawback of these type amplifiers. The majority of GaN HEMTs are produced on silicon carbide substrates, which are both costly and limited in size.

Figure 1.1 summaries the above mentioned PA technologies

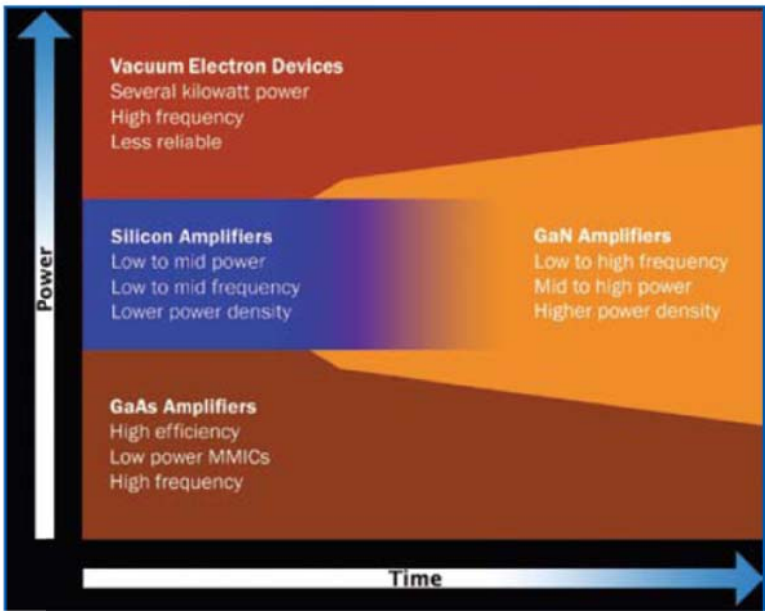



**Figure 1.1:** Radar Amplifier Technology Adaptation Projection [4]

In de table 1.1 we see the comparison of material properties of GaN with other semiconductor materials for RF and microwave applications.

| Material ⇒ Properties ⇓ | Si | GaAs | InP | SiC | GaN |
|---|---|---|---|---|---|
| Bandgap (eV) | 1.1 | 1.4 | 1.3 | 3.2 | 3.4 |
| Saturation Velocity (cm/s) | $1.0 \cdot 10^7$ | $2.1 \cdot 10^7$ | $2.3 \cdot 10^7$ | $2.0 \cdot 10^7$ | $2.7 \cdot 10^7$ |
| Thermal Conductivity (W/cmK) | 1.3 | 0.46 | 0.7 | 4.9 | 1.7 |
| Breakdown Field (V/cm) | $0.3 \cdot 10^6$ | $0.4 \cdot 10^6$ | $0.7 \cdot 10^6$ | $2.0 \cdot 10^6$ | $2.7 \cdot 10^6$ |
| Electron Mobility ($cm^2/Vs$) | 1350 | 8500 | 5400 | 800 | 1500 |

Table 1.1: Semiconductor materials for RF and microwave applications [29]

Because of the good power performance of GaAs PHEMT compared to the other device technologies at high frequencies we will design our PAs with using this as active device.

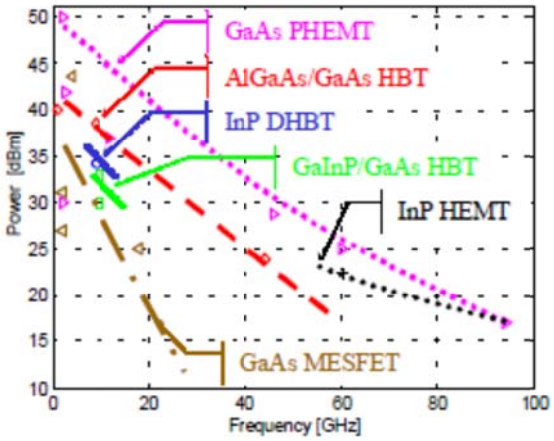



**Figure 1.2**: Power performance of HEMTs, MESFETs and HBTs as a function of frequency.[33]

## 1.3 ORGANIZATION OF THESIS

The goal of this thesis is, to increase the output power and/or increase the maximum power added efficiency (PAE) of a microwave power amplifier in GaAs technology.

Introduction and power amplifiers for radar applications are described above in chapter 1

The thesis is organized as follows:

Chapter 2 presents the specification for the high power amplifier (HPA) design and selected operating HPA operating class.

Chapter 3 deals with explanation of the functioning, use and advantages of cascode structure.

Chapter 4 discusses the design issues. Unit cell (cascode) performance and bias point selection, output matching, input matching, total performance of the whole circuit and layout is presented in this chapter.

Chapter 5 represents the designed PA with design kit components and the layout

Chapter 6 gives conclusions and recommendations

# 2. OVERVIEW OF POWER AMPLIFIERS

Power amplifiers can be categorized into two major groups [5]: Linear PAs and Nonlinear PAs. Linear PAs are able to generate output power proportional to the input power with a negligible amount of harmonic power generated. On the contrary, non-linear Pas operate near the cut-off region with a significant amount of harmonics generated besides the fundamental signal. The input and output power are no longer proportionally related.

Furthermore, amplifiers can also be classified into 2 categories: biasing class and switching class. In biasing class, amplifiers such as Class A,B, AB and C amplifiers are classified based on their quiescent point (bias point) or output Current Conduction Angle (CCA) θ. θ is defined as the fraction of RF input drive signal where non-zero current is flowing through the device [5].

In this thesis we will investigate the benefits of stacked topology with circuits both in linear and non linear characteristics. This will provide us a good comparison opportunity whether we can make use of power efficiency enhancement using switch mode power amplifiers for MMIC power amplifiers at high frequencies. In this way we will try to increase the output power about 2 times more than a common source stage and at the same time keeping a relative high PAE.

For linear PA design case the circuit will be biased in class AB mode according to reason that will be explained in the coming section. In non linear case we will use a class E switch mode power amplifier because of the reasons which are also be explained in the coming sections.

## 2.1 POWER AMPLIFIERS WORKING AS A CURRENT SOURCE

In PAs working as a current source, different bias points result in different conduction angles, and therefore different classes of operation with each having own pros and cons. Here we will briefly describe each class of operation. The detailed analysis and derivation of the linear power amplifiers are fully discussed elsewhere (see e.g. [7], [8])

Efficiency for linear PA can be given in general form as follows [9].

For the voltage and current we have (see fig 4.1),

$$v_{in} = v_b + V_{in} \cdot \cos \omega t , \quad (2.1)$$

$$i = I_q + I \cdot \cos\theta ; \text{ For } -\theta < \omega t < \theta ; \text{ otherwise } i=0, \quad (2.2)$$

in which $V_b$ is the bias voltage, $I_q$ is the quiescent current, θ is the half of the conduction angle, and Vin and I are amplitude of the input voltage and the output current respectively Since θ is the half of the conduction angle, it can be determined at the moment when current is equal to zero, as shown in (2.3)

$$I_q + I \cdot \cos\theta = 0 \Rightarrow \cos\theta = -\frac{I_q}{I} \Rightarrow i = I(\cos\omega t - \cos\omega t) = 0 \quad (2.3)$$

In order to determine the efficiency for each class of operation, first the DC component of the current and the fundamental component of it should be calculated using (2.4) and (2.5),

$$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta)d\omega t = \frac{I}{\pi}(\sin\theta - \theta\cos\theta) \quad (2.4)$$

$$I_1 = \frac{1}{2\pi}\int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta)\cos\omega t d\omega t = \frac{I}{\pi}(\theta - \sin\theta\cos\theta) \quad (2.5)$$

Knowing that the efficiency is the ratio of power at the fundamental to the power at DC, and assuming an ideal condition of zero saturation voltage (voltage peak factor (Vin/Vcc) is equal to 1, in which Vcc is the DC supply voltage), we have,

$$\eta = \frac{P_1}{P_0} = \frac{1}{2}\cdot\frac{I_1}{I_0} = \frac{1}{2}\cdot\frac{(\theta - \sin\theta\cos\theta)}{(\sin\theta - \theta\cos\theta)} \quad (2.6)$$

$$P_0 = \frac{V_0^2}{2R}$$

Depending on the conduction angle, efficiency and linearity of each class is determined. More details on different classes of operation of this category will be provided in the following sections.

### *2.1.1. CLASS A AMPLIFIER*

A Class A amplifier is a linear amplifier, which has conduction angle of 360°. The 360° conduction angle means that the transistor in this class is turned on and conducts over the entire sinusoidal cycle. Most of the small-signal amplifiers are designed in this class because of its simplicity and the best linearity among all classes of amplifiers. Because of the 360° conduction angle of Class A, these amplifiers have the lowest efficiency and are only suitable for low-power applications. The transfer characteristic of a Class A amplifier and its corresponding voltage and current waveforms are shown in Fig.2.1

The class A amplifier is cheap, because it only requires a single active device. It is biased in the active linear region and amplifies the signal over the entire input cycle. Fig. 2.1 shows how a class A amplifier operates. Its performance is good in terms of linearity (it contains no harmonics at the output), but undesirable in terms of efficiency. In other words, it is very inefficient because it is always conducting even when there is no input signal. According to (2.6) it can obtain a maximum efficiency of 50% ($\theta=\pi$).

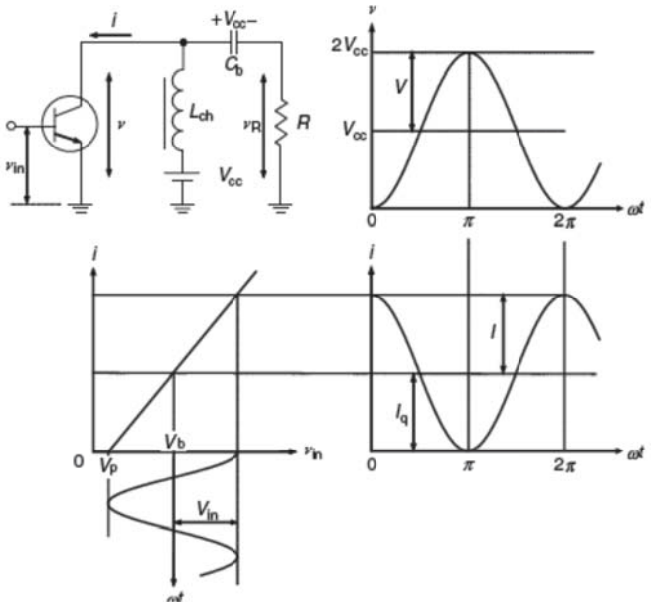



**Figure 2.1:** Voltage and current waveforms in Class-A operation.

### *2.1.2. CLASS B AMPLIFIER*

Unlike class A, a class B amplifier amplifies only half of the cycle of the input signal. Its operation is shown in Fig. 2.2. Turning off the amplifier for half of the cycle reduces power dissipation, but on the other hand, increases the harmonic content of the output signal as it is not purely sinusoidal anymore. Therefore, class B is more efficient than class A but less linear. Using (2.6) with θ=90° (half the cycle) shows that a maximum efficiency of 78.5% is obtainable for a class B power amplifier.

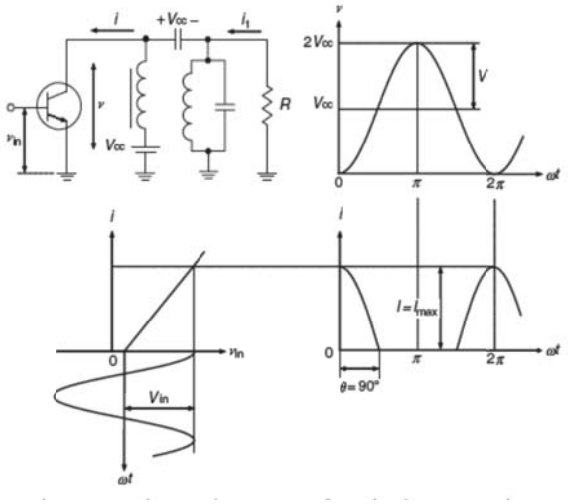



**Figure 2.2**: Class B operation

### *2.1.3 CLASS C POWER AMPLIFIERS*

A class C amplifier conducts even less than half of the cycle of the input signal (θ is less than 90°), which makes it more efficient than class B. But it should be noted that the advantage of high efficiency comes with the disadvantage of high distortion at the output.

### *2.1.4 CLASS AB POWER AMPLIFIERS*

The class AB amplifier is a classical compromise, which has higher efficiency than class A, but inevitably increased nonlinearity [8]. In other words, the class AB amplifier is biased somewhere between class A and class B (which means less than full cycle but more than half a cycle conduction). Therefore, the ideal efficiency will be between 50% and 78.5% (feasible PAE 40-50%), and the linearity will be better than a class B, but worse than a class A amplifier.

Since in our design, efficiency and output power is more important than the linearity; our choice for biasing will be in class AB mode.

Following section will analyzes the switch mode power amplifiers. Among different class of switch mode power amplifiers class E type power amplifiers gain more attention since class E power amplifiers can better tolerate real circuit variation[10] and also it has a relative simple configuration compared to the other switching modes PAs. Therefore our attention will be focused mainly on this class of amplifiers.

## 2.2 SWITCH MODE POWER AMPLIFIERS

In this category, power amplifiers are designed so that the transistor acts as an RF switch, rather than as a voltage-controlled current source. In other words, the output networks provide non-overlapping waveforms. Furthermore, efficiency of this category is improved, because of operation in the saturation region at the cost of more complex load networks (which means at lower powers, switching mode power amplifiers will have poor efficiency). On the other hand, linearity is sacrificed due to operation in a strongly nonlinear region, which results in nonlinear voltage and current waveforms.

In the following sections we will look at two different switch mode power amplifier types. We first start with a short introduction about class F PAs and after that deal with class E power amplifier theory and some class E PAs with alternative load networks.

### 2.2.1 CLASS F POWER AMPLIFIERS

Class F power amplifiers are analyzed in the frequency domain. In other words, canceling the overlap between current and voltage is done in the frequency domain using harmonic terminations. Ideal current and voltage waveforms of a class F power amplifier are shown in Fig.2.3

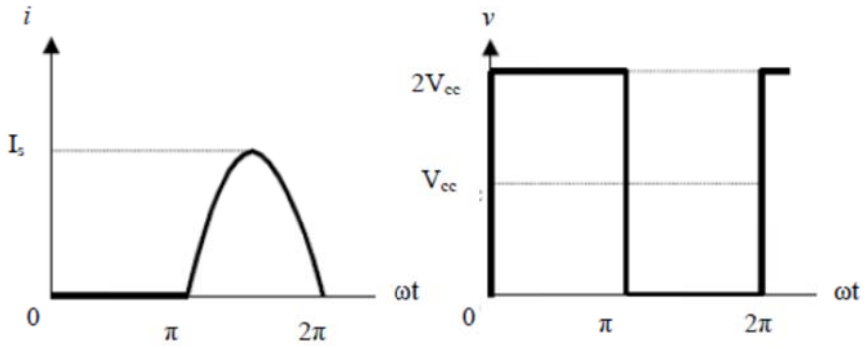



**Figure 2.3** Ideal current and voltage waveforms of class F power amplifier

As shown in Fig. 2.3, the current waveform is half-sinusoidal and the voltage has a square-wave shape. The current contains the even harmonics, while voltage consists of odd harmonics. It results in non overlapping harmonics and reduction of the power loss due to harmonics. Theoretically, an ideal efficiency of 100% is predicted.

### 2.2.2 CLASS E POWER AMPLIFIERS

As mentioned in 2.1.4 , between the switching mode amplifiers class E type power amplifiers gain more attention since class E power amplifiers can better tolerate real circuit variation[10].

In the Class E power amplifier, the transistor operates as an on-off switch and the shapes of the current and voltage waveforms provide a condition where the high current and high voltages do not overlap simultaneously, to minimize the power dissipation and maximize the power amplifier efficiency. Such an operation mode can be realized for the tuned power amplifier by an appropriate choice of the values of the reactive elements in its load network [11].

There are different class E power amplifiers configurations available namely; Class E with shunt capacitance, even harmonic Class E, parallel-circuit Class E, and Class E with quarter wave transmission line. Here we will shortly deal with these configurations and in the

following sections, we will also provide the ADS simulation results of Class E with quarter wave transmission line in order to compare the performance of this SMPA with the linear PA.

### 2.2.2.1 Class E with shunt capacitance

The basic circuit of a class E power amplifier with a shunt capacitance is shown in Figure 2.4 where the load network consists of a capacitance *C* shunting the transistor, a series inductance *L*, a series fundamentally tuned $L_0C_0$ circuit and a load resistance *R*. The collector of the transistor is connected to the supply voltage by RF choke having high reactance at the fundamental frequency. Such a simplified load network represents a first-order Class E mode as their electrical behavior in time domain can be analytically described by the first-order differential equations. (See for more details [12]).

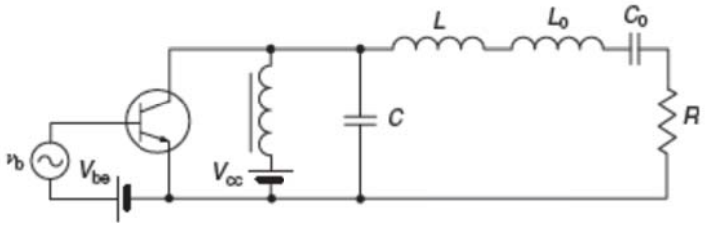



**Figure 2.4** Basic circuits of Class-E power amplifier with shunt capacitance. [9]

### 2.2.2.2 Even harmonic Class E

The second-order Class E load network implies the finite value of DC feed inductance rather than ideal RF choke with infinite reactance at any harmonic components. For even harmonic Class E, the DC feed inductance is restricted to values that satisfy an even harmonic resonance condition and it is assumed that the fundamental voltage across the switch and output voltage across the load have a phase difference of π/2. Generally, even harmonic resonance condition means that the parallel inductance *L* and shunt capacitance *C* can be tuned on any even harmonic component:

$$2n = \frac{1}{\omega\sqrt{LC}} \quad \text{Where n =1, 2, 3, …} \qquad (2.7)$$

The load network of the even harmonic Class E is shown in Figure 2.5 where the series capacitance $C_x$ is needed to compensate the required phase shift. In Figure 2.6, the normalized collector voltage (a) and current (b) waveforms for idealized optimum even harmonic Class E

mode are plotted. Although the collector voltage waveform of even harmonic Class E is very similar to the collector voltage waveform of Class E with shunt capacitance, the behavior of the current waveform is substantially different. So, for the even harmonic Class E configuration, the collector current reaches its peak value, which is four times greater than the DC current, at the end of the conduction interval. Consequently, in the case of the sinusoidal driving signal it is impossible to provide the maximum collector current when the input base current is smoothly reducing to zero. [12]

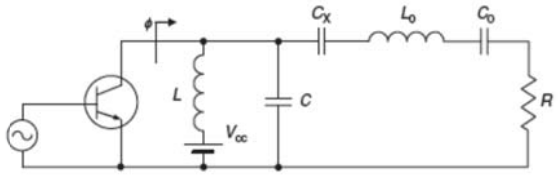



**Figure 2.5** Equivalent circuit of the even-harmonic Class-E power amplifier. [9]

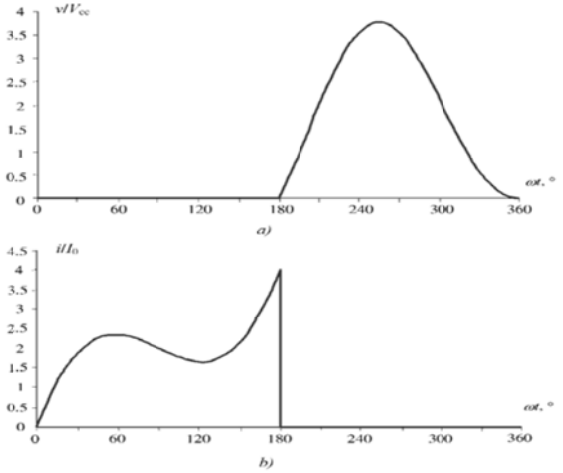



**Figure 2.6** Normalized collector voltage (a) and current (b) waveforms for idealized optimum even harmonic Class E. [12]

### 2.2.2.3 Parallel-circuit Class E

The load network of a parallel-circuit Class E amplifier is shown in Figure 2.7. The series circuit is tuned to the fundamental frequency and the required phase shift to realize idealized voltage and current waveforms is provided by the proper choice of the three parallel circuit parameters, a parallel inductance *L*, a shunt capacitance *C* and a load resistance *R*. In the parallel-circuit Class E mode, no additional series phase-shifting elements are required. In Figure 2.8, the normalized collector voltage (a) and current (b) waveforms for idealized optimum conditions are shown. For the parallel-circuit Class E mode, the optimum load resistance *R*, parallel inductance *L* and parallel capacitance *C* can be obtained, with the high $Q_L$ assumption for the series $L_0C_0$ circuit [12]:

$$R = 1.365\frac{V_{cc}^2}{P_{out}} \qquad L = 0.732\frac{R}{\omega} \qquad C = \frac{0.685}{\omega R} \tag{2.8}$$

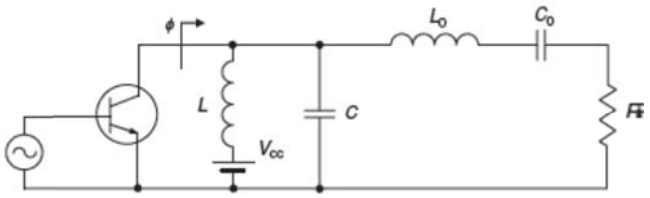



**Figure 2.7**: Equivalent circuit of the parallel-circuit Class E power amplifier. [9]

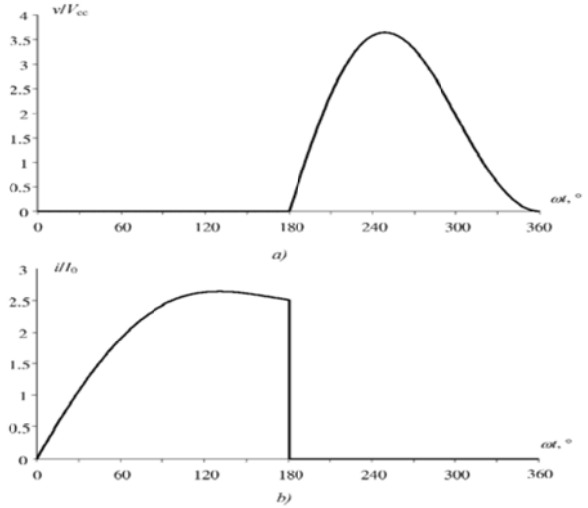



**Figure 2.8:** Normalized collector voltage (a), and current waveforms (b) For an idealized optimum parallel circuit Class E. [12]

### 2.2.2.4 Class E with quarter wave transmission line

The idealized Class E load network with a shunt capacitance where a quarter wave transmission line is connected between the series inductance and fundamentally tuned series $L_0C_0$ circuit is shown in Figure 2.9. In Figure 2.10, the normalized collector voltage (a) and current (b) waveforms for an idealized optimum Class E mode with a quarter wave transmission line are shown. The series inductance *L*, shunt capacitance *C* and load resistance *R* with high $Q_L$ assumption for series $L_0C_0$ circuit can be obtained from

$$R = 0.465\frac{V^2_{cc}}{P_{out}} \qquad L = 1.349\frac{R}{\omega} \qquad C = \frac{0.2725}{\omega R} \qquad (2.9)$$

Class E mode with a quarter wave transmission line shows different impedance properties at even and odd harmonics. At odd harmonics, the optimum impedances can be established by the shunt capacitance as it is required for all harmonics in Class E with a shunt capacitance. At even harmonics, the optimum impedances are realized using a parallel LC circuit. Thus, the frequency properties of a grounded quarter wave transmission line, with its open circuit conditions at odd harmonics and short circuit conditions at even harmonics, allow Class E with a quarter wave transmission line to combine simultaneously the harmonic impedance conditions typical for both Class E with a shunt capacitance and Class E with a parallel circuit. [12]

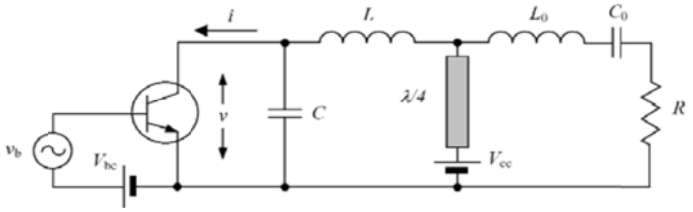



**Figure 2.9:** Equivalent circuit of Class E power amplifier with quarter wave transmission line [12].

The theoretical results obtained for Class E mode with a quarter wave transmission line show (see [9] for detail mathematical derivation of these results) that it is enough to use a very simple load network to realize the optimum impedance conditions even for four harmonics. In this case, the shunt capacitance *C* and series inductance *L* provide optimum inductive impedance at the fundamental and the quarter wave transmission line realizes the reduction of even harmonics. Then, an open circuit condition is required for the third harmonic component. Consequently, when the ideal series $L_0C_0$ circuit in figure 2.9 is replaced by the output matching circuit, the optimum impedance conditions for Class-E load network with a quarter-wave transmission line can be practically fully realized by simply providing an open-circuit condition at the third-harmonic component. (See figure 2.10)

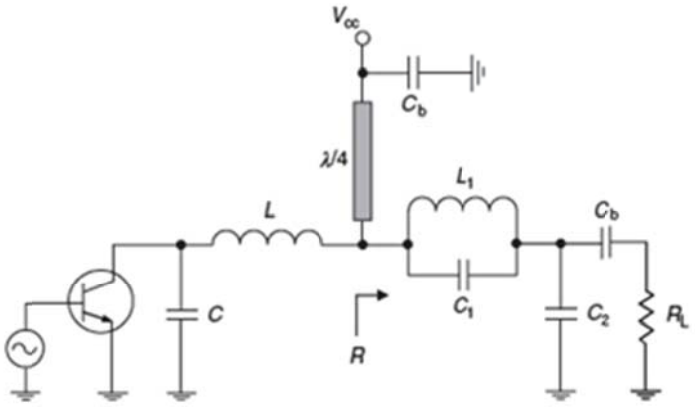



**Figure 2.10** Schematic of quarter-wave-line Class-E power amplifier with lumped matching circuit. [9]

The parameters of the matching-circuit elements can be calculated according to the following equations that are given in 2.10. Here the parallel resonant $L_1C_1$ circuit tuned to the third harmonic component is used and $C_b$ represents the blocking or bypass capacitor. Since the reactance of the parallel third harmonic tank circuit is inductive at the fundamental frequency, it is enough to use the shunt capacitance $C_2$ composing the L-type low-pass matching circuit to provide the required impedance matching of the optimum Class-E load resistance $R$ with the standard load impedance of $R_L = 50\Omega$. In this case, it is assumed that $R < R_L$, which is normally the case for high-power or low-voltage power amplifiers.

$$
\begin{aligned}
L &= 1.349\frac{R}{\omega} & Q_L &= \sqrt{\frac{R_L}{R}-1} \\
C &= \frac{0.2725}{\omega R} & C_2 &= \frac{Q_L}{\omega_0 R_L} \\
R &= 0.465\frac{V_{dd}^2}{P_{out}} & L_1 &= \frac{8}{9}\frac{Q_L R}{\omega_0} \\
 & & C_1 &= \frac{1}{9\omega_0^{\,2} L_1}
\end{aligned}
\qquad (2.10)
$$

Thus with this type of class E PA, one can achieve a good harmonic termination with relative simple circuit. Because of this reason we will investigate our cascode PA structure performance with this type of switch mode PA.

## 2.3 DISADVANTAGES OF SWITCH MODE PAS

It is also important to note that switch mode amplifiers are not suited for microwave application where broadband width is required since the design procedure of these class of operations is based on considering a single fundamental frequency, which makes it narrowband and unsuitable for broadband power amplifiers. Another drawback of switch mode PAs is that although switch mode PAs achieves much higher efficiencies they generate strong nonlinearities.

A large output capacitance and switch on resistance (Ron) are also limiting factors at high frequencies. At very high frequencies (at $\mu$-wave range) this can cause deviation from the ideal drain/collector voltage- current waveform for switch mode PAs which in turns result in an overlapping of both signal quantity. This will have then, of course, deleterious effect on the efficiency.

However there are some papers have been published with promising results at S band with switch mode PAs. In [6] PAE of greater than 70% over 3.0-3.7 GHz is obtained for 15.0 dBm input power drive, and a peak PAE of more than 90% is obtained at around 3.25 GHz when the amplifier is driven by only 12.0 dBm of input power. Over 10% bandwidth in S-Band, an inverse class-F amplifier exhibits [13] more than 60% drain efficiency and 10W output power. Also in [14] and [15] peak PAE performances close to 80% have been published for class-F and inverse class-F GaN power amplifiers operating at around 2GHz. We have to also stress out here that these designs are not all of them MMIC applications. A more general conclusion will be given after comparing the performance results of class AB PA with switch mode class E PA.

In the coming sections we will compare the performance of both, linear and switch mode PAs through simulation results. In this way we want to conclude that despite of those aforementioned disadvantages of switch mode PAs, whether we can still achieve an acceptable relative broadband characteristic and enough output power and PAE for S band system with the aid of stacked- switch mode PA.

# 3. CASCODE ARCHITECTURE

The cascode configuration is formed by a cascade of a common source (CS) stage driving a common gate (CG). (See figure 3.1) The cascode configuration is usually used for low-noise amplifier applications when a mixer is the next stage [B.Razavi et.al]. Then the load will be capacitive which will limit the frequency response of the LNA due to Miller effect. Also it is frequently used in wideband amplifiers because of high reverse isolation and high gain characteristic of the cascode configuration.

## 3.1 POSSIBLE CASCODE CONFIGURATIONS

There are two types of cascode arrangement possible one with a combination of two single gate devices (as CS+CG) and a dual gate device. (See fig 3.1)

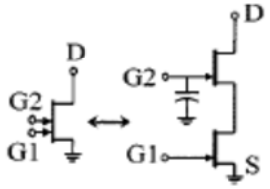



**Figure 3.1** Schematic diagram of dual-gate FETs and CS. /CG pair

A dual-gate device is electrically equivalent to a common-source (CS) / common-gate (CG) cascode pair, *but occupies less die area.* [17]. Dual-gate FET differs in modeling than CS/CG pair as it is a three port device and only two-port S-parameters are measured using vector network analyzer which needs a more complex modeling techniques which in turn causes accuracy problems [18]

The cascode cell (dual gate and/or CS+CG combination) has some advantages over the simpler CS stage:

- The output to input feedback capacitance is reduced; therefore, the Miller effect capacitance is smaller thereby allowing wider bandwidths.
- The output impedance is higher. Not only is the reverse isolation is very high, but the cascode cell is less sensitive to change in $r_{ds}$ (drain source resistance).
- Another possible advantage of the cascode configuration is higher voltage swings at the output before FET breakdown is reached.
- The effective Gds (output conductance) of the dual gate device is less dependent on input voltage Vgs than the single gate device, resulting in better linearity performance than single gate device.
- A dual gate device has much lower Gds (higher Rds), lower loss hence higher efficiency could be obtained.
- Dual gate device has higher maximum stable gain (MSG) than single gate device. [17, 18]

The disadvantages associated with dual gate device:

- Number of gates per device is twice of a single gate one, hence higher yield is required during the processing, this practically becomes an issue
- A dual Gate device has higher knee voltage Vknee than the single gate one.
- Due to the complexity, it is difficult to get an accurate nonlinear model for the dual gate device. [17,18]

Following argument explains the lower feedback of the cascode configuration. For better understanding of this argument, definition of Miller effect has to be given first. The Miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the capacitance between the input and output terminals. The additional input capacitance due the Miller effect is given by [2]

$$C_m = (1 - A_v) \cdot C_{gd} \qquad (3.1)$$

Loaded with the input impedance $\frac{1}{g_m}$ of the common gate circuit, the small signal gain, Av, of the common source stage with transconductance $g_m$ exhibits a low value of -1 since $Av \approx -g_m \cdot R_L$.

According to Eq. (3.1) we get

$$C_m = (1 - A_v) \cdot C_{gd} = 2 \cdot C_{gd} \qquad (3.2)$$

In comparison to the common source circuit this result in a much smaller Miller capacitance than the one for the common source circuit. Consequently, the low pass characteristic associated with the input capacitance is less pronounced yielding higher cutoff frequencies for the voltage, current and power gain. [3] .The nearly unilateral nature of cascode cell helps improving the stability as well.

As it can be seen from the figure 3.1 an additional capacitor is added on the gate of the 2nd transistor. Next section will highlight the reason of this configuration.

## 3.2 WHY AN ADDITIONAL CAPACITOR MUST BE ADDED ON THE GATE OF THE SECOND TRANSISTOR?

The capacitor at the gate of the common gate transistor enables to equalize the output impedances of both transistors within the cascode cell. [16] And also reduce the voltage swing between the gate and drain of the stacked FET's below the breakdown voltage limit. [30]

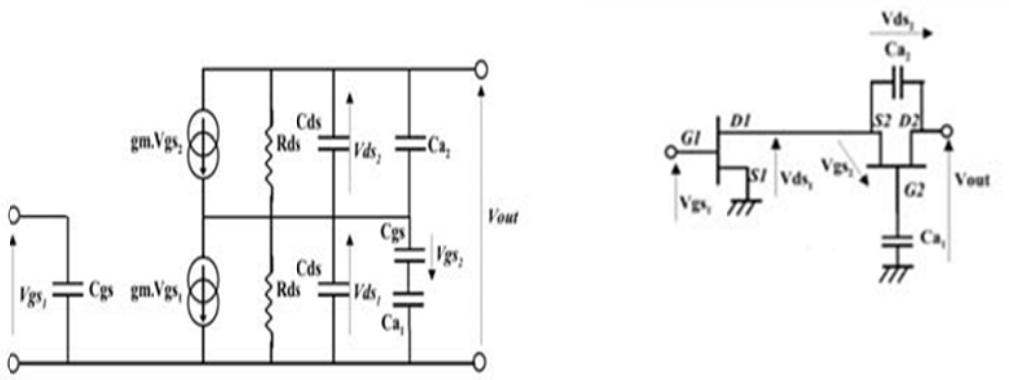



**Figure 3.2:** Schematic of balanced cascode cell with the additive capacitors: *Ca*1 and *Ca*2. [16]

On the other hand, the addition of a Ca2 capacitor between the drain and the source of the 2nd transistor makes it possible to obtain twice the output conductance of a single common source transistor. It enables to equalize the output impedances of both transistors within the cascode cell by considering that Ca2 meets the following requirement [16]:

$$Ca2 = \frac{Cgs*Ca1}{Cgs+Ca1} \qquad (3.3)$$

However during the simulation it is observed that adding this additional capacitor Ca2 cause stability problems. This is due to the fact that adding of Ca2 generates negative resistance at the drain. Therefore in our design Ca2 is removed.

To get more output power, the voltage swing across the top transistor and the bottom one should be the same. Thus both have nearly the same load line. This equal voltage swing across the both transistor is achieved by means of the gate capacitor Ca1.

The output power of the balanced cascode configuration $Pout_{cas}$ is twice that of a common source device $Pout_{CS}$ is derived as follows in [16] (See also figure 3.2).

$$Pout_{cas} = \frac{1}{2}.\Re[(Vds_1 + Vds_2).(gm.\frac{1}{2}.(Vgs_1 + Vgs_2) + \frac{Vds_1 + Vds_2}{2Z})] \quad (3.4)$$

In optimum power case:

$$Vg2 = \frac{1}{2}.V_{dd} + Vg_1 \qquad (3.5)$$

$$Vgs_1 = Vgs_2 = Vgs_{opt} \tag{3.6}$$

$$Vds_1 = Vds_2 = Vgs_{opt}$$

And the total impedance at the output is:

$$Z = (\frac{1}{R_{ds}} + j.\omega.C_{ds})^{-1} \tag{3.7}$$

So that:

$$Pout_{cas} = \frac{1}{2}.\Re[\left(2.Vds_{opt}\right).(gm.Vgs_{opt} + \frac{Vds_{opt}}{2Z})] \tag{3.8}$$

$$= 2.Pout_{tr\_cs} \tag{3.8}$$

In [31] the authors provide mathematical analysis of calculation of the gate capacitance value for N-cell stacked FET. We will do the same analysis for the 2 cell stacked FET.

For the sake of simplicity Rg, Rd, Rs, Rgs, and Cgd is ignored in figure 3.5 since their effect are small and can be removed in the analysis.

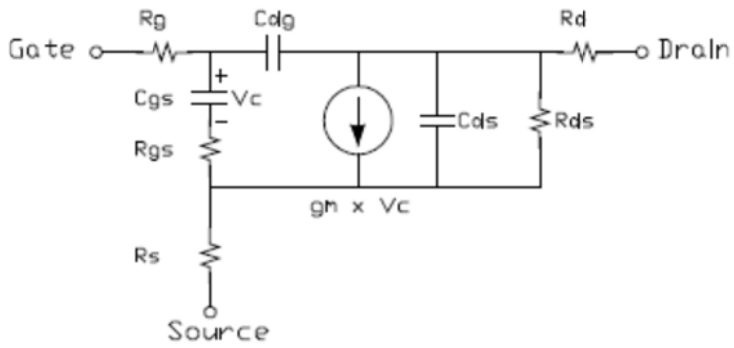



Figure 3.4: Intrinsic Small-Signal FET Equivalent Circuit

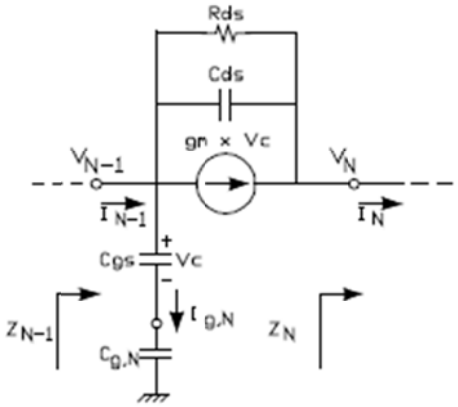



Figure 3.5: Small-Signal Equivalent Circuit of a 2-Cell stacked FET

In order to achieve maximum power the voltage swing across the device terminals, the current source, gmVc, and the intrinsic elements in each device should be the same for each device. Based on this approach, the following conditions must be fulfilled:

$$V_{N+1} - V_N = V_m \qquad (3.9)$$

Vm is the voltage swing across drain and source of each device, Hence

$$V_N = N.V_m \qquad (3.10)$$

For equal devices currents Vc is a constant:

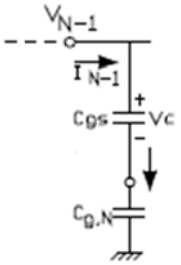



Figure 3.6 : Cgs and Cg form a capacitive divider

Figure 3.6 shows a capacitive divider, hence

$$V_c = \frac{C_{g,N}}{C_{g,N} + C_{gs}}.V_m(N-1) \qquad (3.11)$$

Simplifying this result gives eq (3.12)

$$V_c = V_{gs,N} = \frac{(N-1)V_m}{1+\frac{C_{gs}}{C_{g,N}}} \qquad (3.12)$$

Since Vc is constant the current sources in all cells have the same magnitude Im

$$I_m = g_m V_c = g_m . \frac{(N-1)V_m}{1+\frac{C_{gs}}{C_{g,N}}} \qquad (3.13)$$

If we assume that $Y_{opt}$ is optimum admittance needed at the drain terminal of a common source single FET, then we get:

$$Y_{opt} = (I_m - j\omega C_{ds} V_m)/V_m \qquad (3.14)$$

From (3.13) and (3.14)

$$Y_{opt} + j\omega C_{ds} = g_m . \frac{(N-1)}{1+\frac{C_{gs}}{C_{g,N}}} \qquad (3.15)$$

Hence

$$C_{g,N} = \frac{C_{gs}}{g_m (N-1)/(Y_{opt} + j\omega C_{ds}) - 1} \qquad (3.16)$$

And for 2 cell stacked structure this will be equal to:

$$C_{g,2} = \frac{C_{gs}}{g_m / (Y_{opt} + j\omega C_{ds}) - 1} \qquad (3.17)$$

Since for the microwave transistors $Y_{opt}$ can be approximated by a shunt resistor and a shunt negative capacitor which can be defined as follows:

$$Y_{opt} = G_{opt} - j\omega C_{opt} \tag{3.18}$$

Assuming Copt =Cds and from (3.16 and 3.18)

$$C_{g,N} = \frac{C_{gs}}{g_m(N-1)/(G_{opt} - j\omega C_{opt} + j\omega C_{ds}) - 1}$$

$$\cong \frac{C_{gs}}{g_m(N-1)/G_{opt} - 1} \tag{3.19}$$

The mathematical analysis above show us why the stacked topology gives more output power compared to a common source stage and the following analysis after that establishes the relation of gate capacitance with other circuit parameters.

The more accurate value for the gate capacitance will be found through performing simulation which also take account of ignored parasitic.

# 4. PERFORMANCE ANALYSIS OF STACKED MMIC POWER AMPLIFIER IN GaAs TECHNOLOGY USING ADS

In order to demonstrate whether stacked FET can be used to increase the output power of microwave power amplifiers in the range of S- band, we will design a linear power amplifier and a switch mode PA in ADS. These will give us also an opportunity whether we can make use of efficiency benefit of switch mode power amplifiers (SMPA) with enough bandwidth for radar systems.

## 4.1 LINEAR PA DESIGN TO VERIFY THE STACKED STRUCTURE CONCEPT FOR S BAND SYSTEM

To show that the output power will be doubled as mentioned in [16] when it is designed in stacked topology, we start with a power amplifier that is biased in class AB mode for optimum tradeoff between power and PAE (see fig 4.1).

### *4.1.1 LINEAR SINGLE GATE DESIGN*

One of the first steps in designing a power amplifier is that you guarantee the stability of the power amplifier. The following section highlights this issue.

- STABILITY ISSIUES

Stability is an important consideration when designing an amplifier. In order to fulfill to have a two-port be stable for all combinations of passive impedance terminations; conditions, which is called Rollet's stability criterion, in eq (4.1) has to be satisfied. Two relations must be fulfilled to have a necessary and sufficient criterion for unconditionally stability.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} > 1, \qquad (4.1)$$
$$\Delta = S_{11}S_{22} - S_{12}S_{21} < 1$$

Here K is called Rollet stability factor and $\Delta$ is being the determinant of the S parameter matrix of the two-port.

Another useful criterion that combines the S parameters in a test involving only a single parameter, $\mu$, defined as [19]

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta S_{11}^*|+|S_{12}S_{21}|} > 1 \qquad (4.2)$$

Where $\Delta$ is again the determinant of the S-parameter matrix

Thus, if $\mu$>1, the device is unconditionally stable. In addition, larger values of $\mu$ imply greater stability. In contrast, the Rollett factor itself cannot give secure prediction about unconditional stability. An additional auxiliary condition such as |Δ| < 1 is necessary and sufficient for unconditional stability of a two-port (see eq. 4.1).

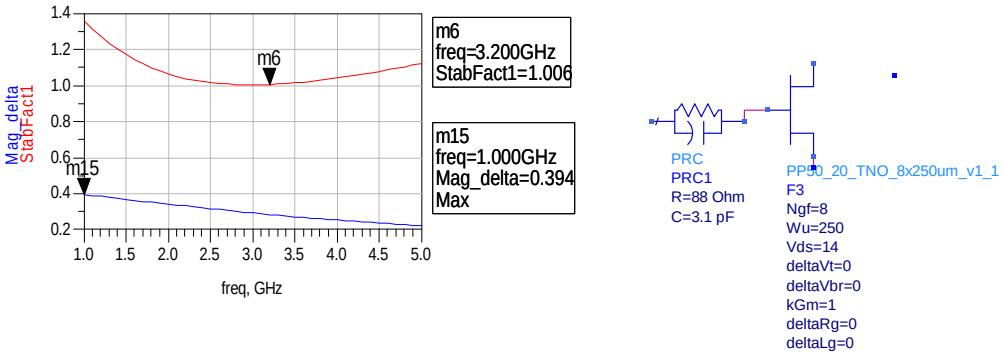


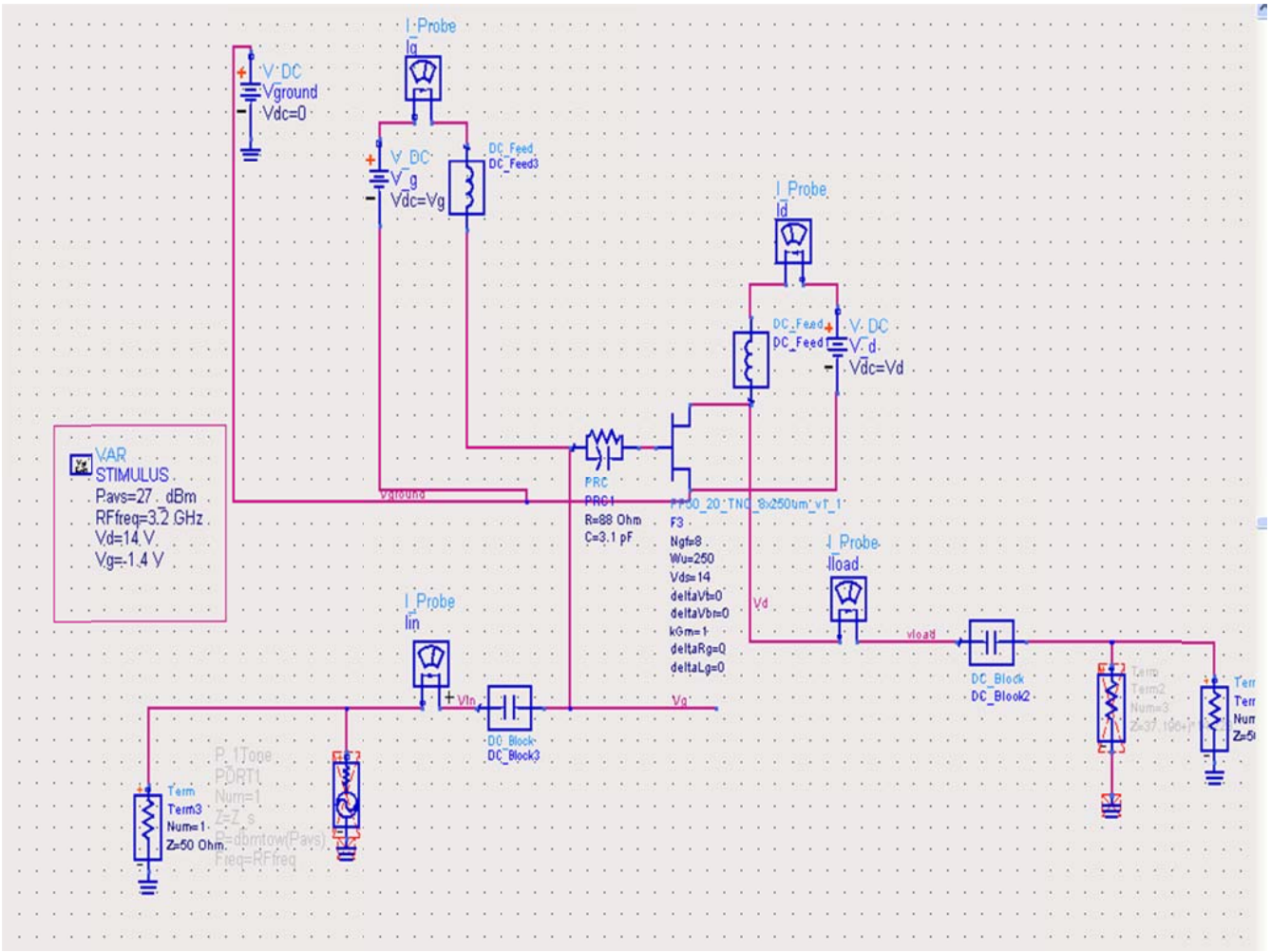

**Figure 4.1:** verification of unconditional stabilization according to Rollet stability criteria K (stabFact1)>1 and $\Delta(Mag\_delta) < 1$

Rollet's criterion in our circuit is achieved by adding a parallel RC combination at the gate of our active device. The values of these components are chosen such that at low frequencies the circuit shows a relative high resistance in order to suppress the unwanted oscillation, because of high small signal gain at those frequencies. Further, the values are optimized with the tuning tool in ADS. The result is given in fig 4.1.

In the coming section load pull analysis will be performed in order to determine the optimum load. The circuit will be biased in AB mode, operating at 3.2 GHz with an input drive level of 27 dBm.

**LOAD PULL ANALYISIS AND BIAS POINT SELECTION**

At the first stage we perform load pull analysis in ADS to find the optimum load. It is observed from the smith chart in figure 5.2 that Z=36,108+j13.415 results optimum between power added efficiency (PAE) and output power.



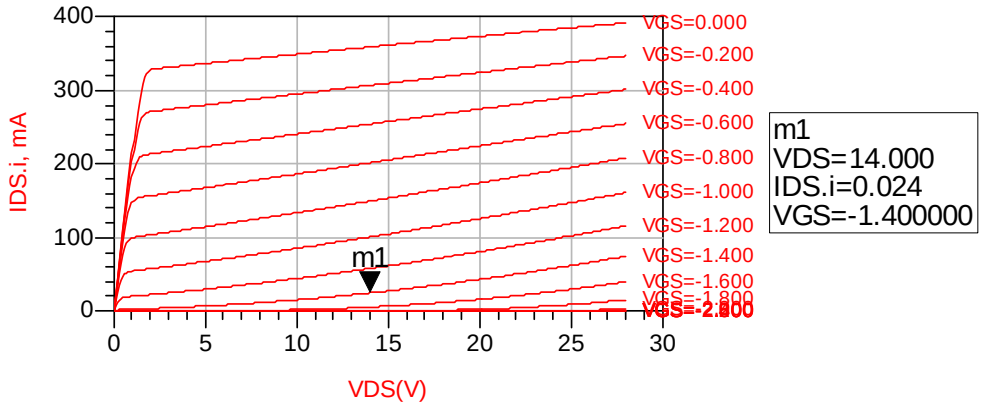



**Figure4.2:** Setup for load pull analysis and bias point selection

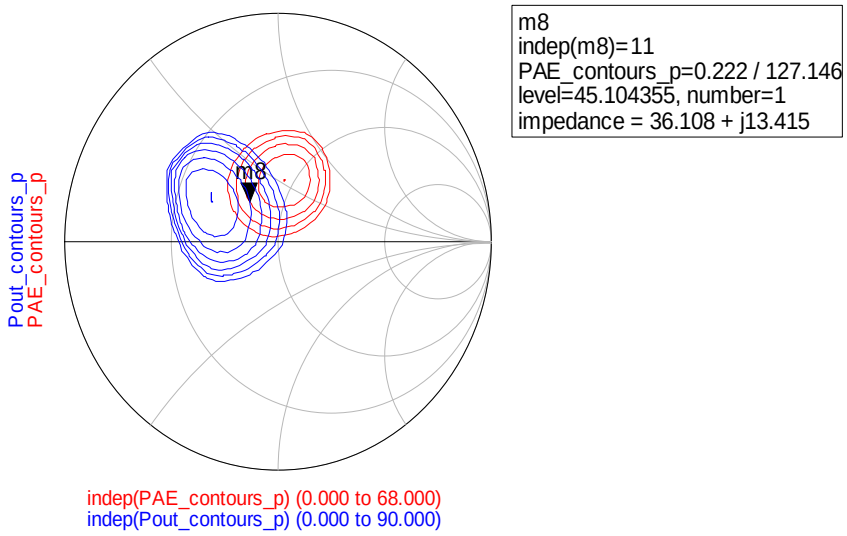



**Figure 4.3:** Load pull analysis for determining the optimum load

- PERFORMANCE PARAMETERS FOR COMMON SOURCE PA

In the figures below following results are achieved at 3.2 GHz with 27dBm input drive signal.

Output Power = 32.38 dBm
Power added efficiency=52.23 %
Power Gain=11.18dB
Optimum Load= 36.1+j13.4 Ohm

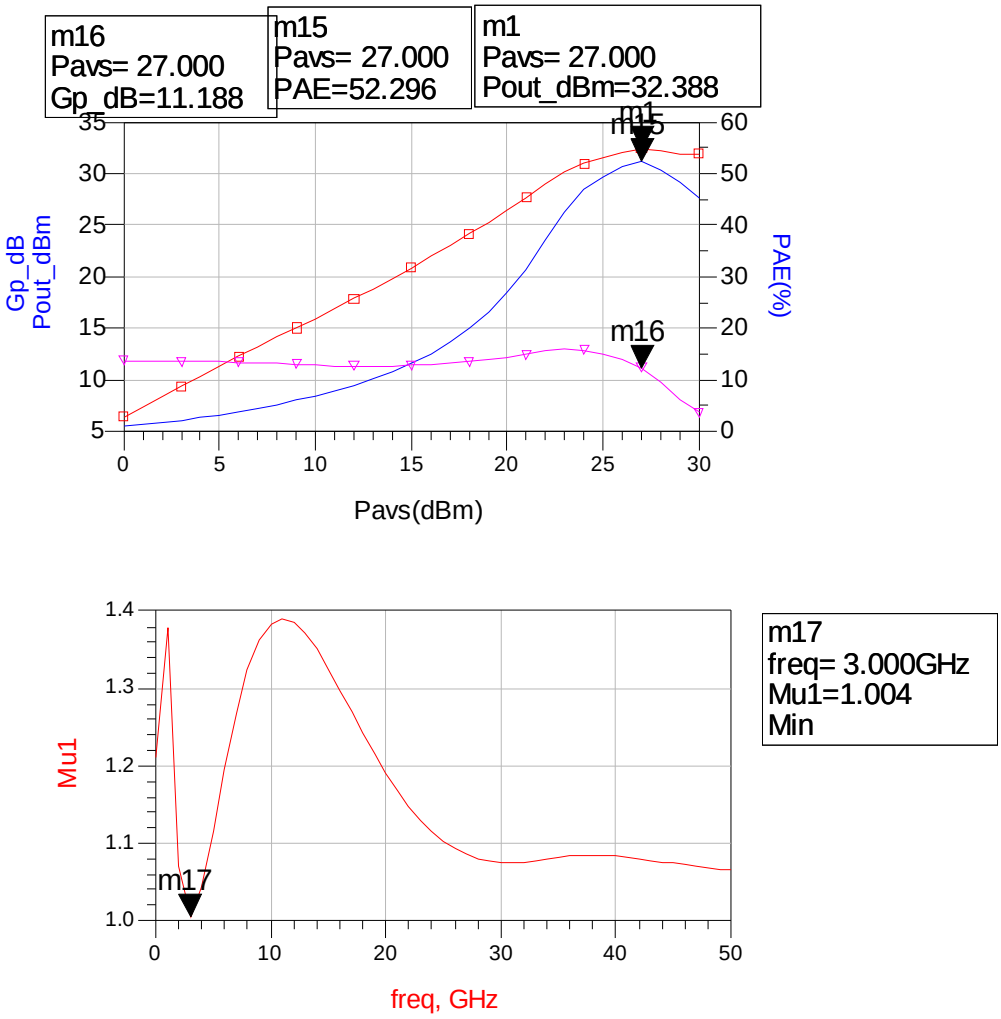



**Figure 4.4**: Performance results of unmatched common source PA

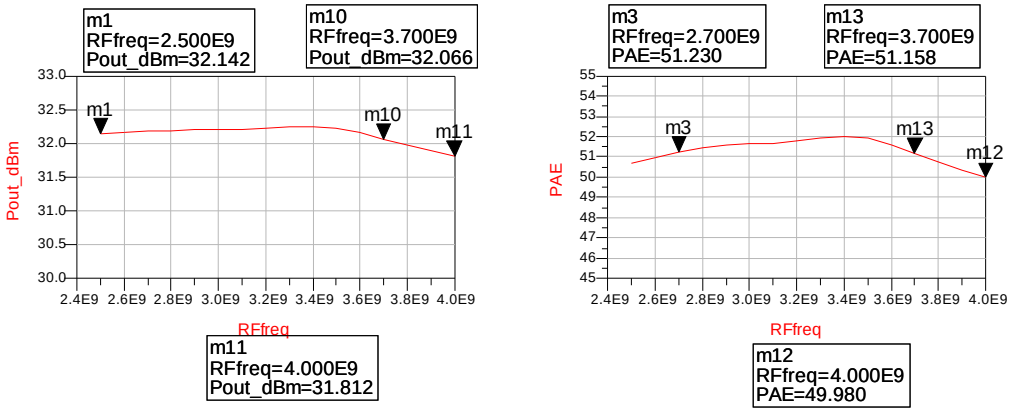



**Figure 4.5:** Frequency (in GHz) characteristic of Pout and PAE for the common source stage PA

### *4.1.1 STACKED CONFIGURATION BIASED IN CLASS AB-MODE*

As for the single stage, after determining the DC bias condition, the next step was determining the optimum load to be presented to output of transistor. For the cascode configuration we have found Zopt= 57.149+j*38.147

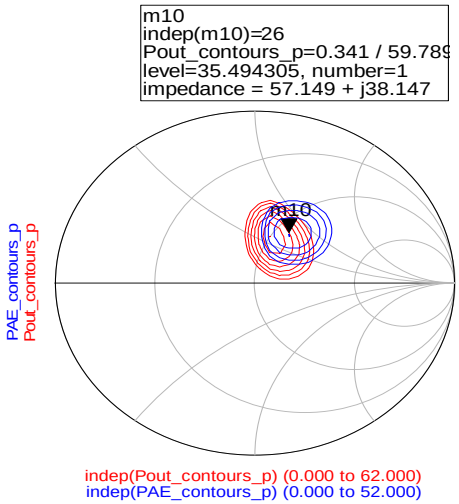



**Figure 4.6:** Load Pull analysis result of stacked configuration

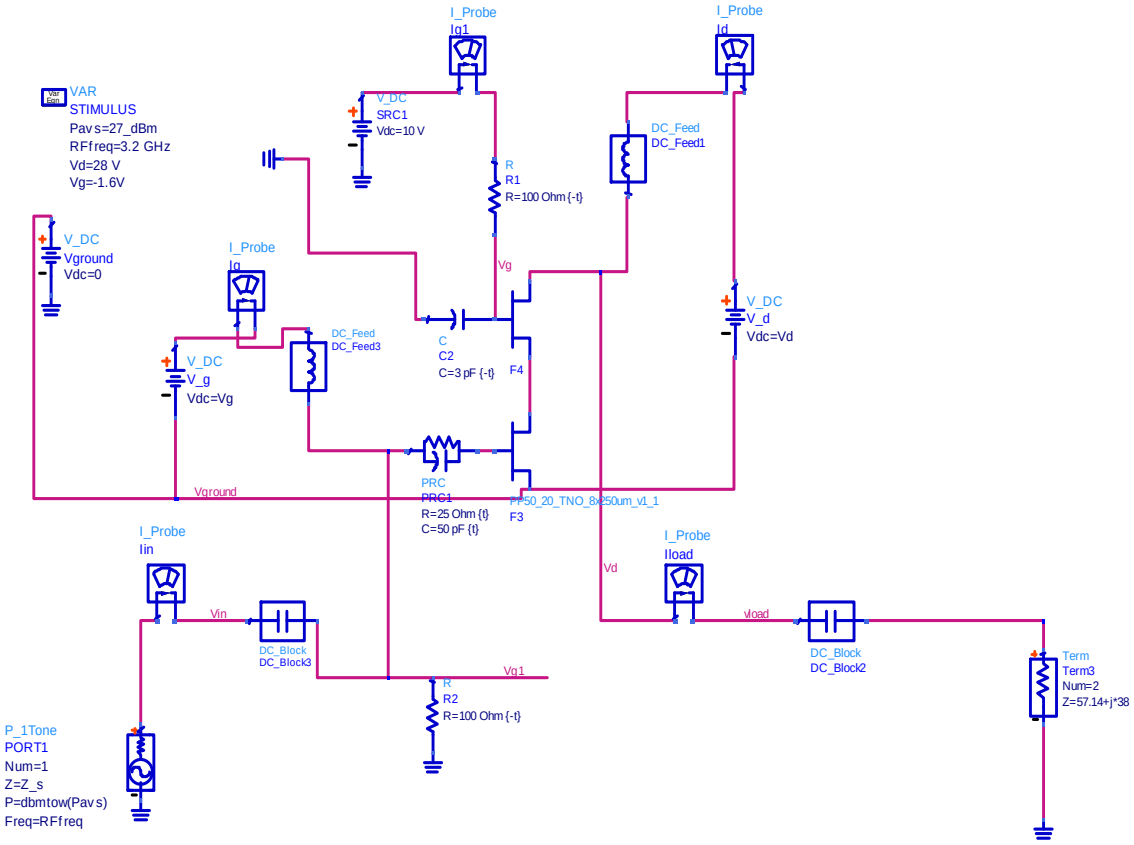



**Figure 4.7:** Unmatched stacked class AB PA

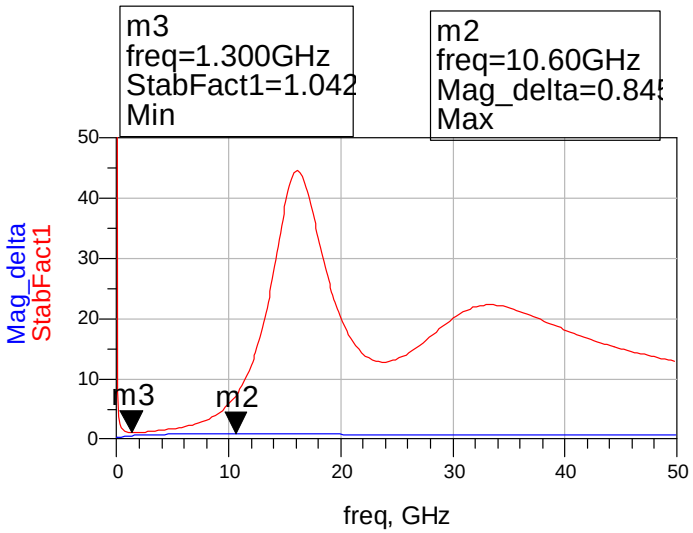



**Figure 4.8:** Unconditional stability, K>1 and Δ< 1 is satisfied

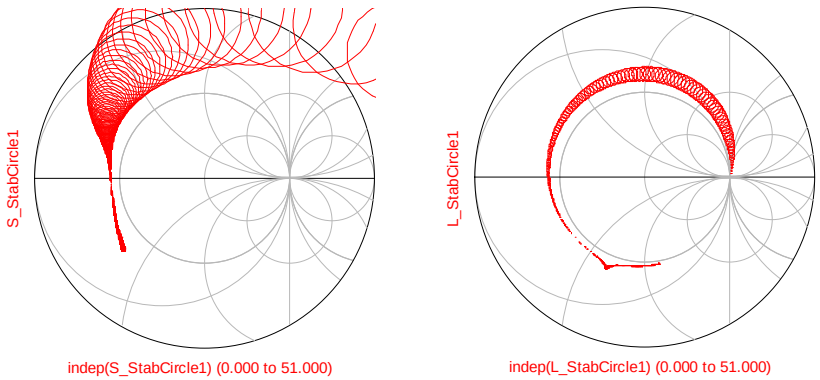



**Figure 4.9:** Source and Load stability Circles

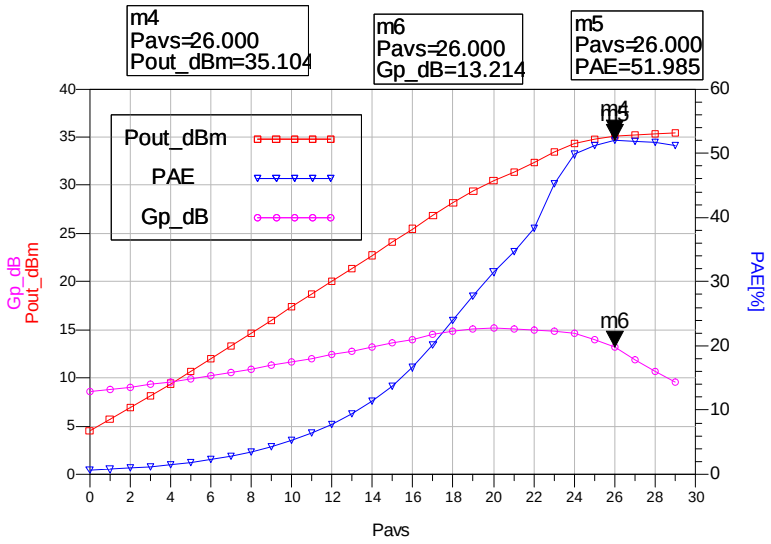



**Figure 4.10:** Power performance of the stacked amplifier @ 3.2GHz and $V_{DD}$=28[V]

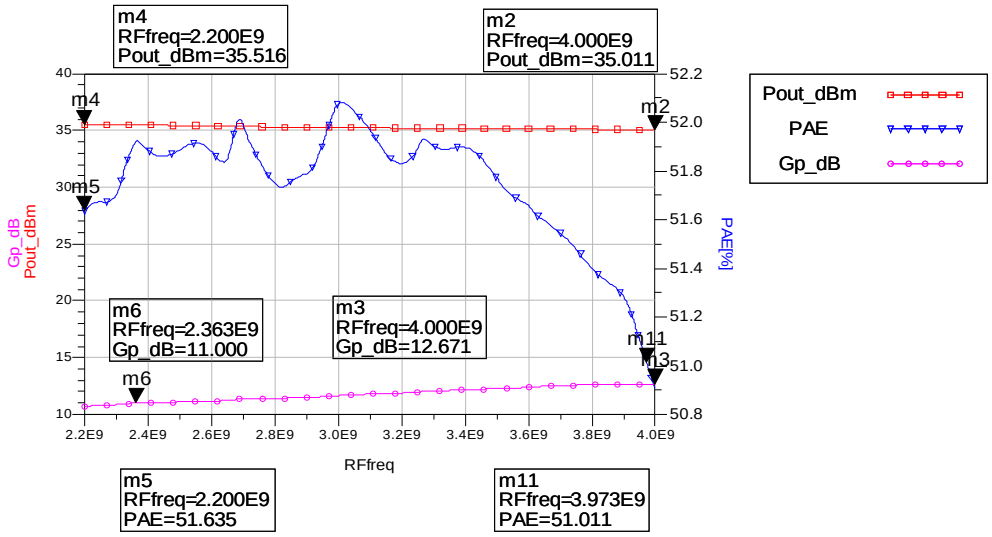



**Figure 4.11:** PAE, Pout and Power gain versus Frequency of the cascode stage amplifier @ S band

### *4.1.2 PERFORMANCE OF DESIGNED UNMATCHED CLASS AB PA*

The performance comparison of common source stage 'linear' PA with stacked PA is given in table 4.1

The output power is increased almost 2 times in stacked topology compared to the common source stage as expected from the literature information. Other important points are the increased output power bandwidth and PAE bandwidth (about 20% increasing) along with increased power gain in stacked topology.

| | Common Source Stage | Stacked structure |
|---|---|---|
| | | |
| Output Power[dBm]@P1dB | 32.4 | 35.1 |
| Power added efficiency[%] | 51 | 51 |
| Power Gain[dB] | 11.2 | 13.2 |
| Pout Bandwidth[%] | 37.5 | 56.3 |
| PAE Bandwidth[%] | 31.3 | 55.4 |

Table 4.1: Performance summary of common source 'linear' PA and Stacked PA

In the next section we will deal with the same analysis but this time we will do it for a switch mode PA.

## 4.2 SWITCH MODE DESIGN AS AN ALTERNATIVE APPROACH TO LINEAR DESIGN IN ORDER TO IMPROVE THE EFFICIENCY

Switching-mode power amplifiers (SMPA) use active transistors as switches. That is, the active device is ideally fully on (short-circuit) or fully off (open-circuit). The theoretical efficiency of the SMPA's is 100%. However this is in practice never the case. Especially in the high frequency range, optimum drain current and voltage waveforms deviate substantially from the ideal non-overlapping situation.

We will perform some simulations with a class E power amplifier with quarter wave transmission line configuration. The reason of chosen configuration is explained in section 4.2.2.4. But it could be also done in other kind of configuration of class E PA.

### *4.2.1 SINGLE STAGE CLASS –E @3.2 GHZ*

As to aim to increase the PAE along with output power using stack structure, we designed a class E PA with quarter wave transmission line which is given below in the figure 4.12

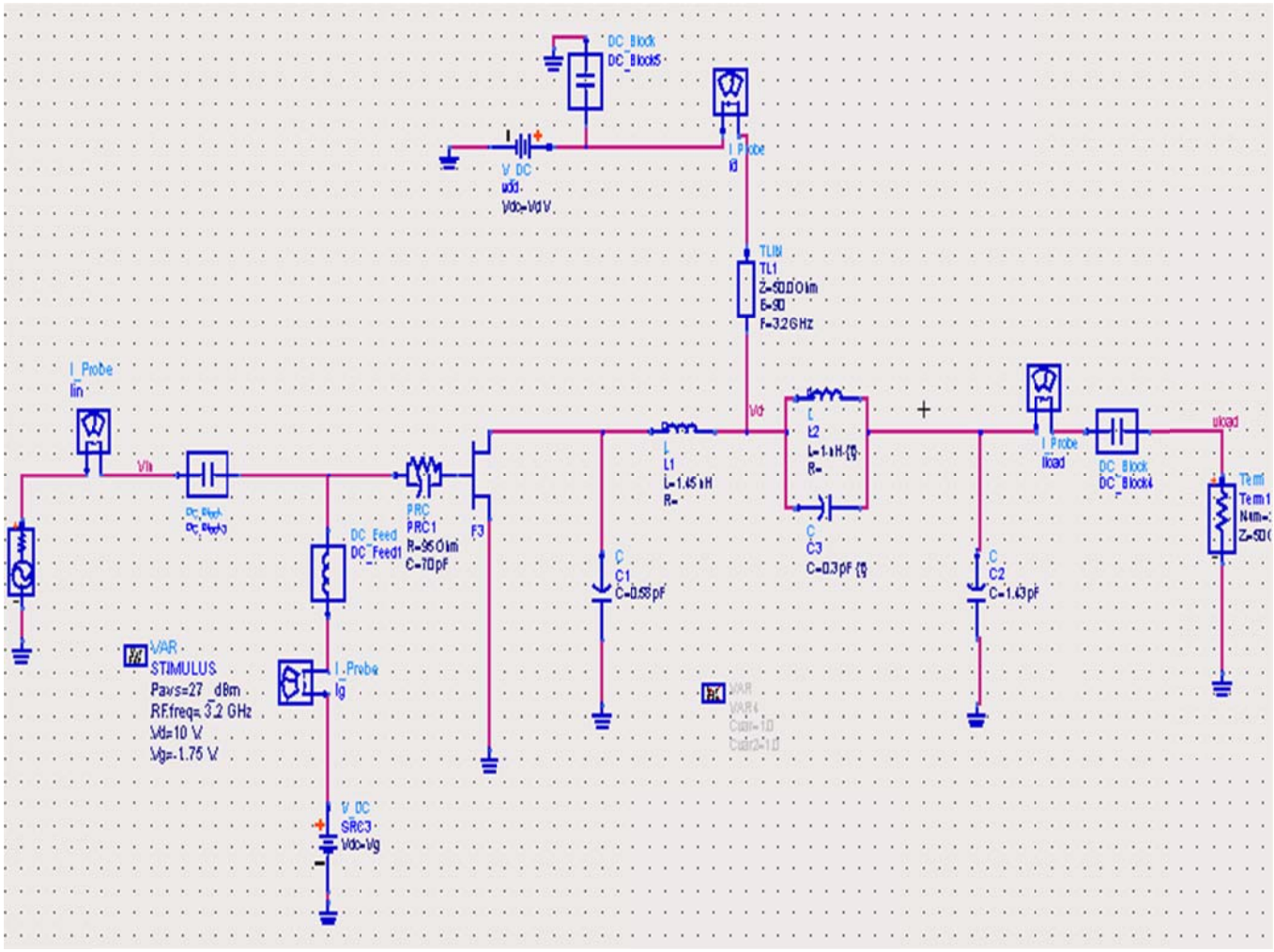



**Figure 4.12:** Single stage class E power amplifier with quarter wave transmission line

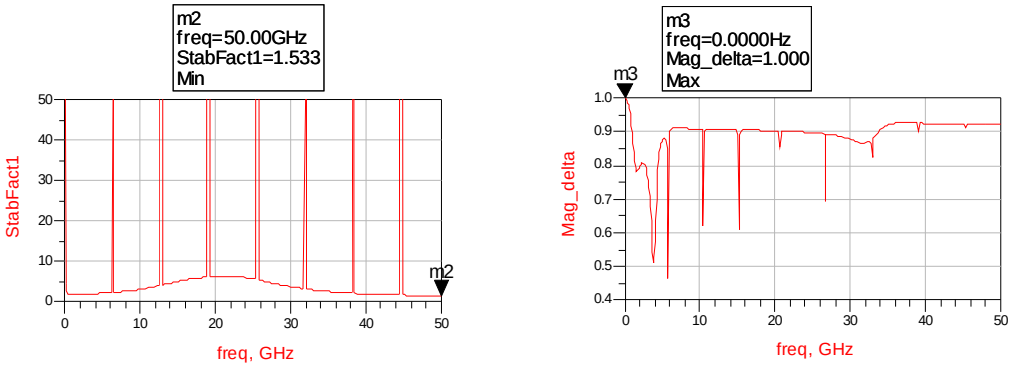



**Figure 4.13:** Unconditional stability verification

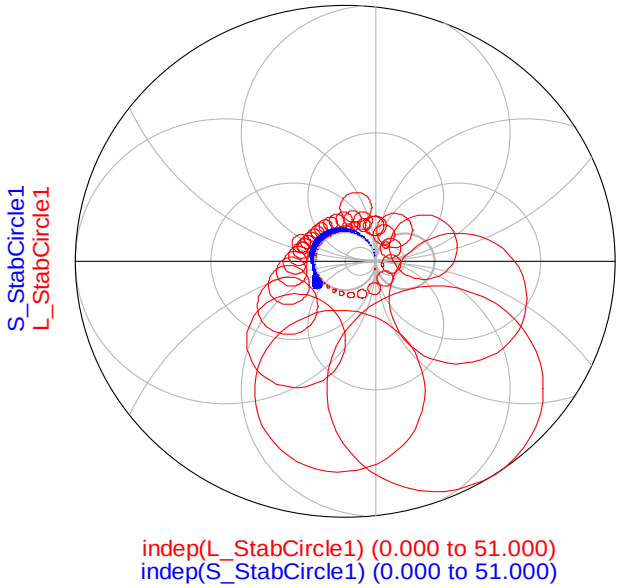



**Figure 4.14:** Load and Source stability Circles

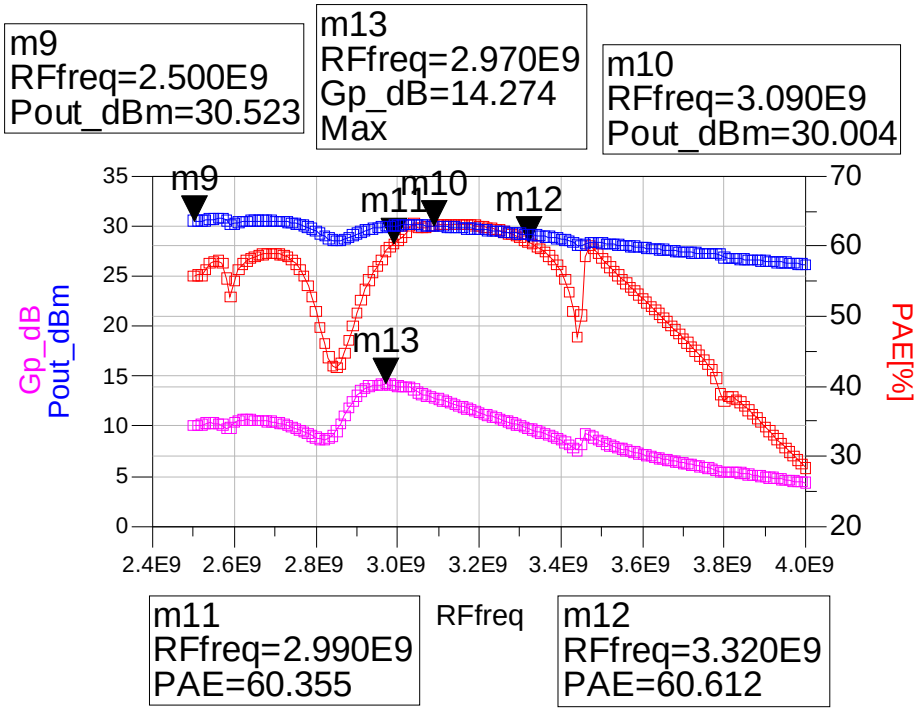



**Figure 4.15:** Simulated PAE, Pout, and Power Gain vs. frequency bias (Vd=10 [V], Vg=-1.75[V]

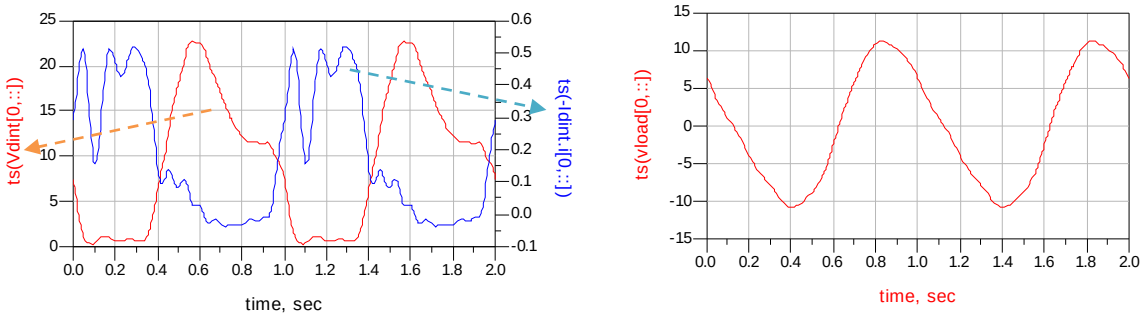



**Figure 4.16:** Drain Voltage and current vs. time and load signal vs. time

As it can be seen from the figures 4.13 and 4.14 unconditional stability is satisfied( Rollett stability criteria has been fulfilled). Also from figure 4.16 we observe that the optimum class E condition is not satisfied but further improvement of this condition would make the bandwidths for output power and PAE much narrower which would be also an unwanted situation moreover the aim of this project is not to desing a best perfomed PA at S band but

to show the benefits of cascode structure at high frequencies.So it is decided to satisfy with this result and go further with cascode configuration of this class E PA.

### *4.2.2 STACKED SWITCH MODE DESIGN*

Below the stacked version of the previous class E PA is given. This circuit will be used to compare the performance of single stage with cascode version of the SMPA.

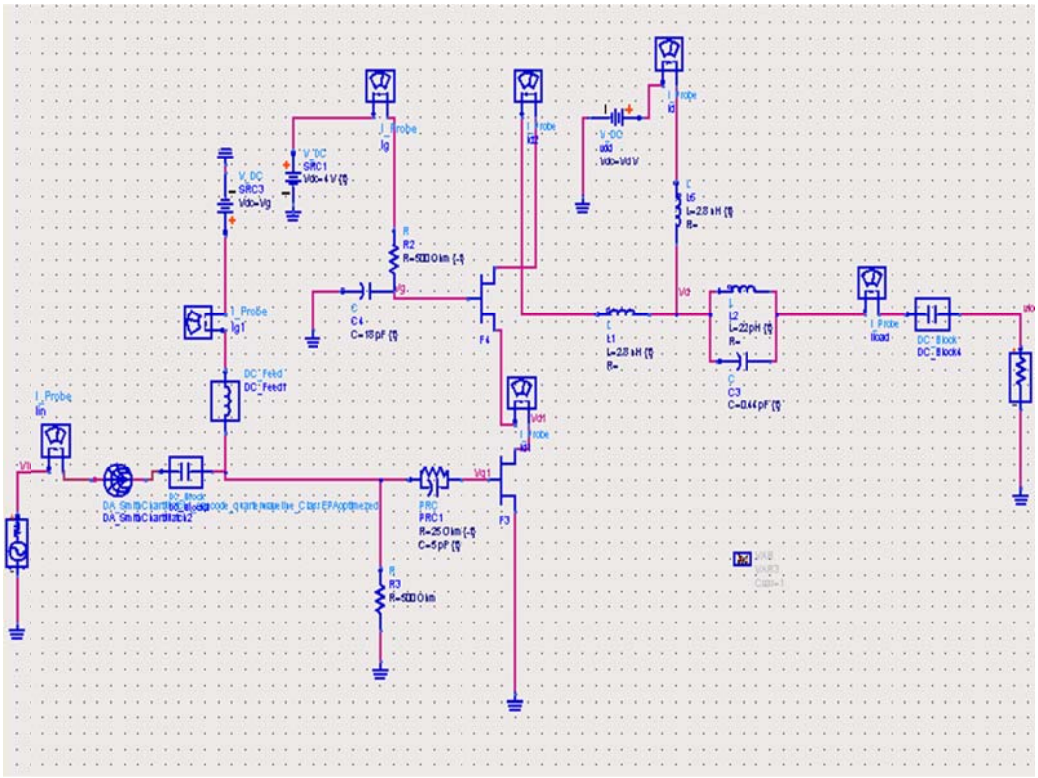


**Figure 4.17:** Stacked Switch mode PA

In figure 4.18 the load and source stability circles along with Rollet's criterion given. We see in these figures that the unconditional stability is satisfied.

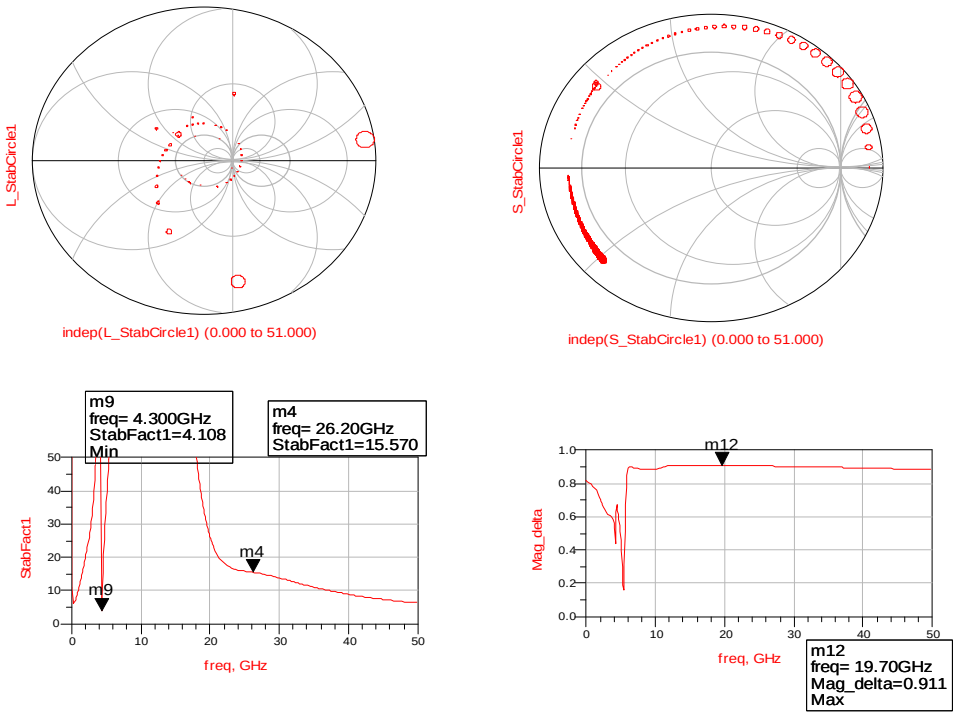



**Figure 4.18**: Unconditional stability verification; above the load and source stability circles beneath that the K factor and Δ are given

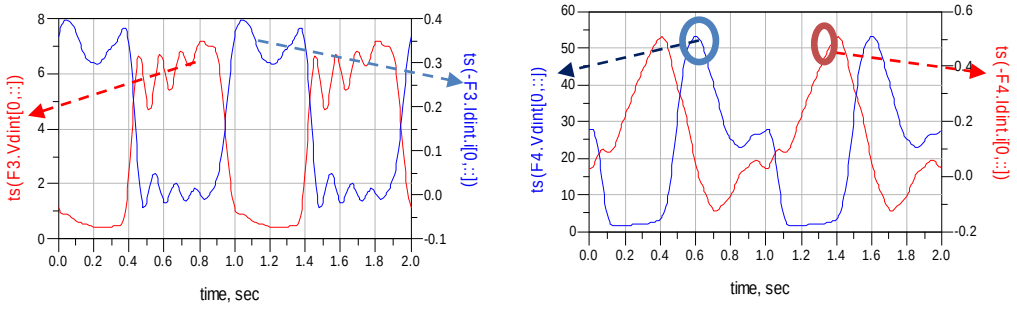



**Figure 4.19**: Drain current and Voltage waveforms of bottom and top transistors

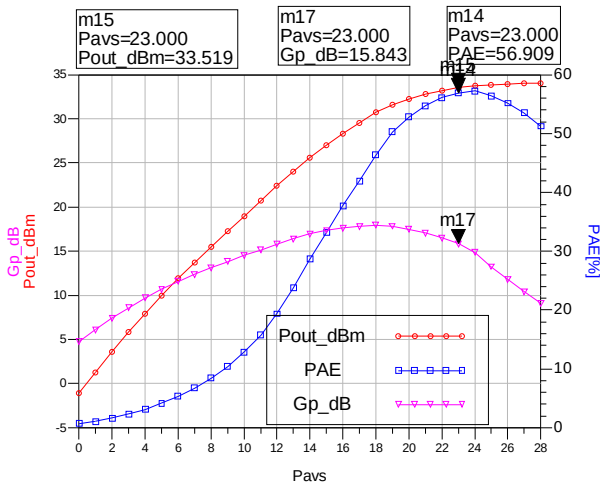



**Figure 4.20**: PAE, Power Gain and PAE vs. Pavs

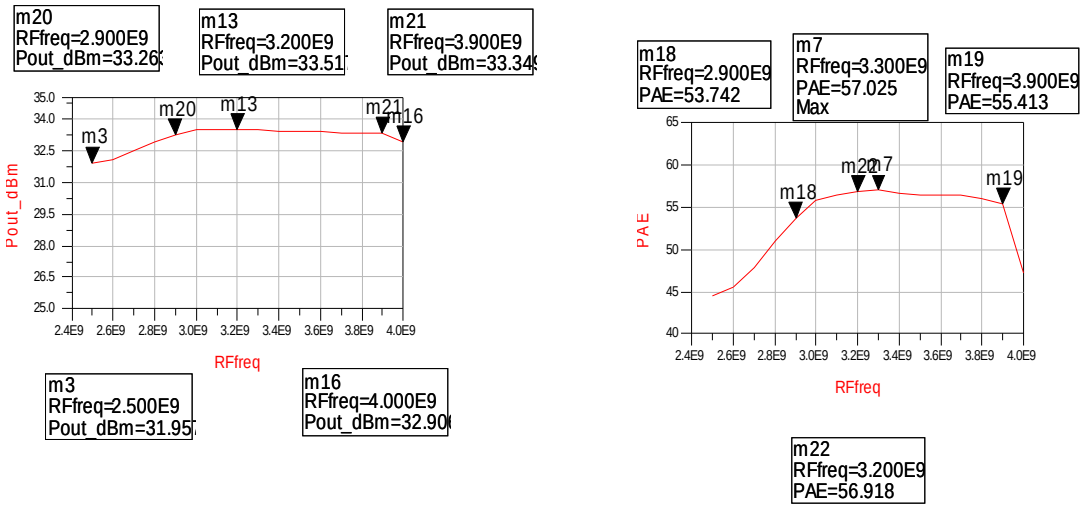



**Figure 4.21**: Pout and PAE vs. frequency( in GHz) characteristic

### 4.2.3 *PERFORMANCE SUMMARY OF DESIGNED SWITCH MODE PA*

In table 4.2 the performance comparison of single stage SMPA with stacked version given. We see here again an increase in the bandwidth and the output power for the stacked topology. Also the power gain is greater for the stacked configuration as it was the case for linear PA.

| | **Single Stage** | **Cascode Stage** |
|---|---|---|
| | | |
| Output Power[dBm]@P1dB | 30.5 | 33.3 |
| Power added efficiency[%] | 60 | 55 |
| Power Gain[dB] | 14.3 | 15.8 |
| Pout Bandwidth[%] | 15.6 | 31.2 |
| PAE Bandwidth[%] | 9.7 | 31.2 |

Table 4.2: Performance summary of single stage SMPA with stacked SMPA

The increase in bandwidth for PAE is pretty high but this is due to the fact that we have used here class E power amplifier with quarter wave transmission line that possess 4 harmonic termination which makes the output characteristics more selective for single stage SMPA. We do not expect that much increasing in the bandwidth for other kinds of class E PAs but still the increasing would be about 2 times more for stacked topology compared to the single stage.

Another important observation is that the switch mode PAs do not perform very well in the sense of PAE and output power when we compare it with 'linear' PAs at S band. This is because of the difficulties in achieving the optimum class E conditions at high frequencies. The maximum output power that is achieved with SMPA is almost 2 dBm less than linear PA but it also provides 3dB more output power when using stacked structure compared to single stage version as it was for the linear PA.

In the figure below we see the improvement in the bandwidth characteristic for the SMPA

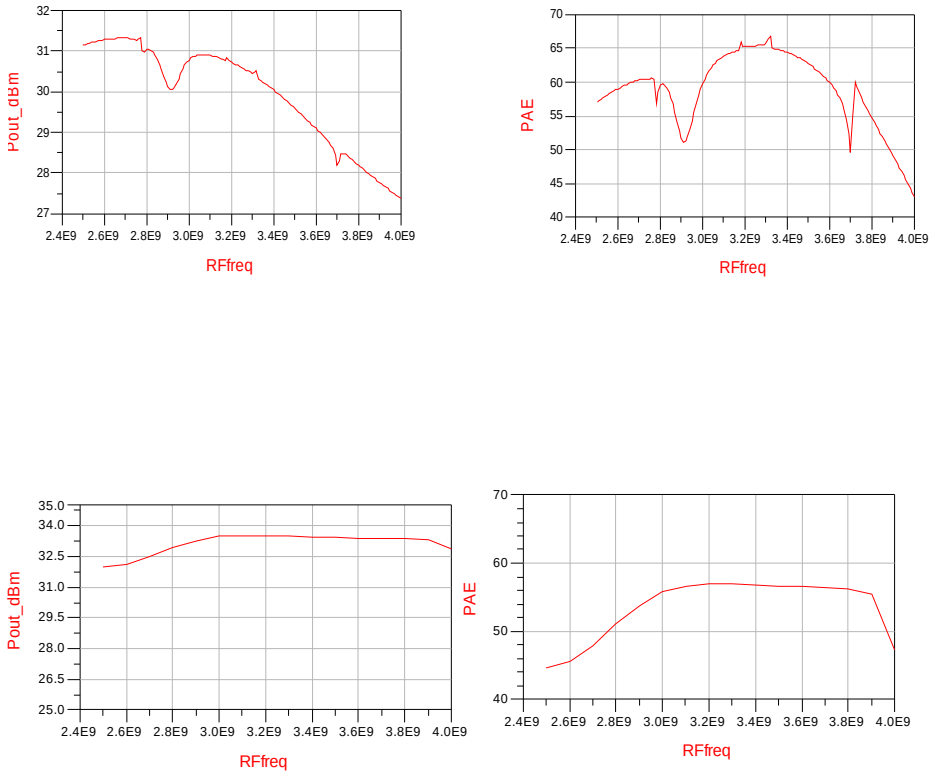



**Figure 4.22:** Improvement in the bandwidth characteristic for the SMPA: first two belong to the single stage SMPA and below that the cascode stage SMPA frequency characteristic.

Having finishing the comparison of unmatched circuit performances, it is now time to design the impedance matching circuits for the PAs in order to have a more realistic performance merits.

## 4.3 IMPEDANCE MATCHING NETWORK DESIGN FOR LINEAR POWER AMPLIFIER

Matching networks provide a transformation of impedance to a desired value to maximize the power dissipated by a load. The input impedance of the transistor is highly nonlinear, i.e., dependent on the operating point. Thus, the device operating under large-signal conditions

(and especially in switched-mode PAs), will exhibit dynamically varying input impedance. Therefore it is one of most important steps in the design of a PA.
As explained in section 4.2.3 the performance of SMPA at S band is worse than the linear counterpart. Therefore we will focus on the 'linear' PA and design the input and output matching networks for this PA.

### *4.3.1 INPUT/OUTPUT MATCHING CIRCUIT DESIGN FOR COMMON SOURCE STAGE PA*

After connecting the load network we will determine the large-signal input impedance $Z_{in}$ at the $f_0$ of 3.2 GHz. We then design a lowpass impedance transformation network that transforms 50ohm $Z_{source}$ into $Z_{in}^*$ at $f_0$=3.2 GHz

Through load Pull analysis the optimum output power was determined for a load impedance of $Z_{Lopt}$=36,108+j13.415 for the common source class AB PA. So we first design an output network match circuit that will transform 50 Ohms to the optimal load impedance.

---

***Output matching circuit Design for common source stage PA***

---

In the figure below, the conceptual design schematic of a PA given with matching circuits at the output and input of the circuit.

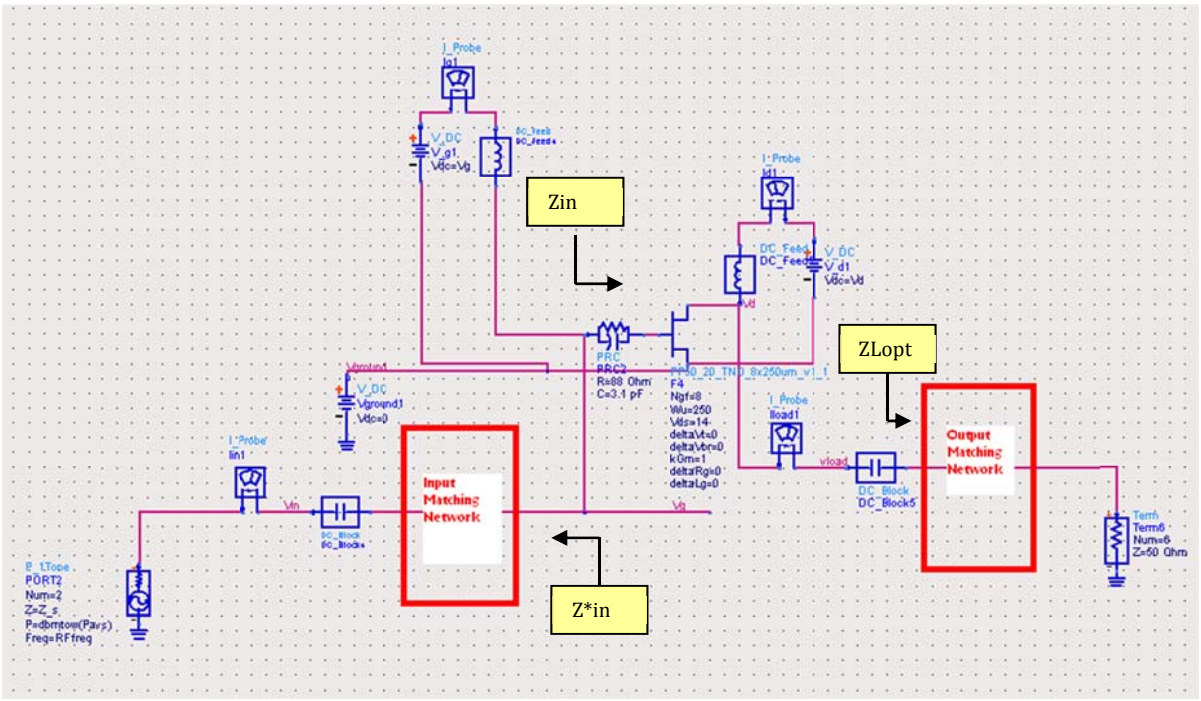



**Figure 4.23:** PA with input/output matching networks

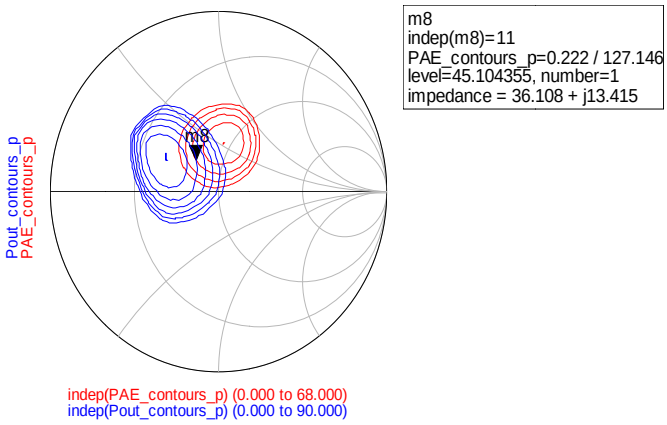



**Figure 4.24**: Load pull analysis for determining the optimum load

The first step is finding the optimum impedance as explained several times. According the load pull analysis this is equal to Zopt= 36.108+j13.415 in our case for the common source linear PA.

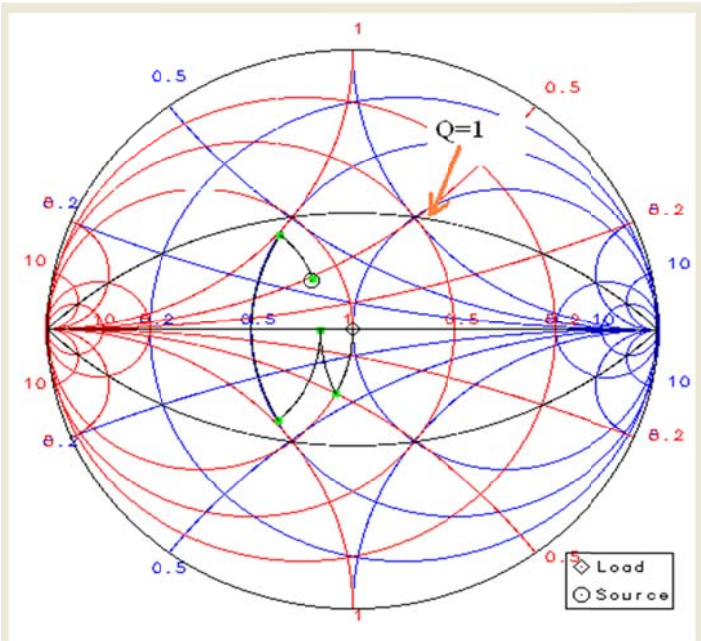



**Figure 4.25:** Smith Chart based output matching circuit design result

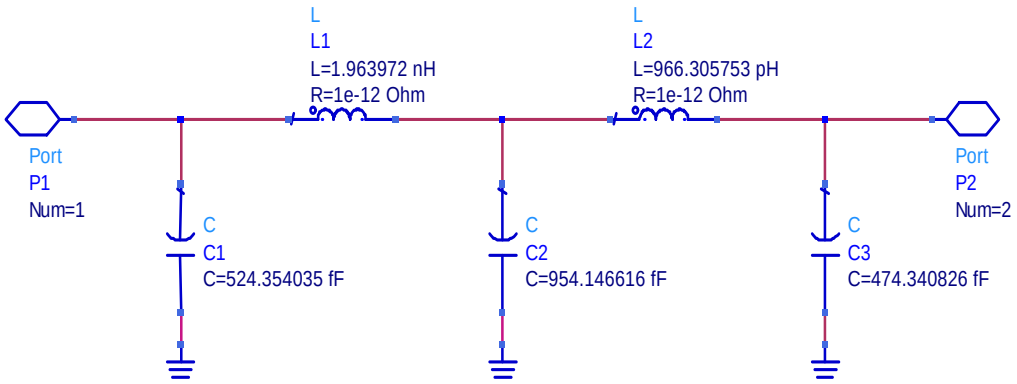



**Figure 4.26:** Output matching network

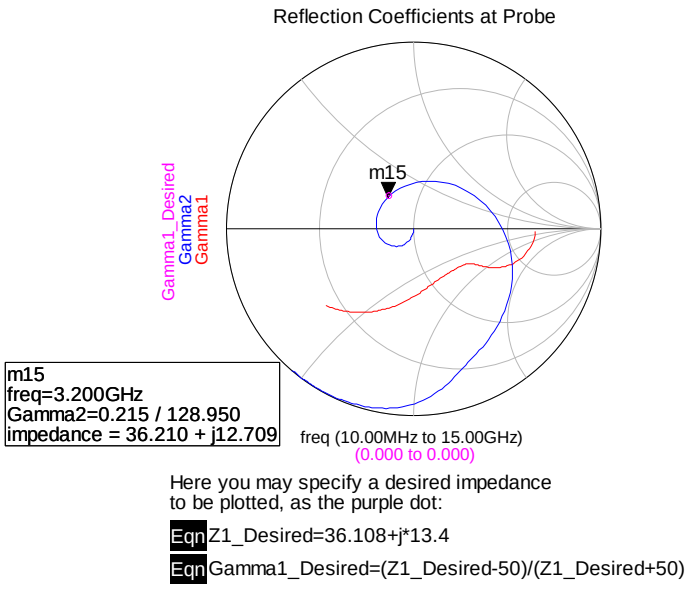



**Figure 4.27:** Output match verification

The data display in figure 4.27 shows that the desired impedance is achieved. Furthermore to satisfy the broadband matching characteristic multi section filter is designed through 'staying' within the border of the quality factor (Q=1) circle when transforming the load impedance to the optimum impedance.

---

***INPUT MATCHING CIRCUIT DESIGN FOR COMMON SOURCE STAGE PA***

---

After having designed the output matching network, we determined the large signal input impedance. The simulated impedance value is given in the figure 4.28 which is equal to 4.04+j28.73 [Ω]

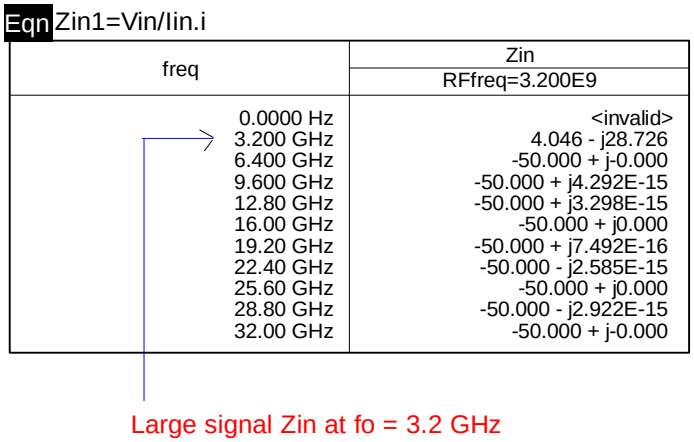



**Figure 4.28**: Large signal Zin at fo

We then conjugate match the input in order to get the maximum power transfer. Design procedure and results are given

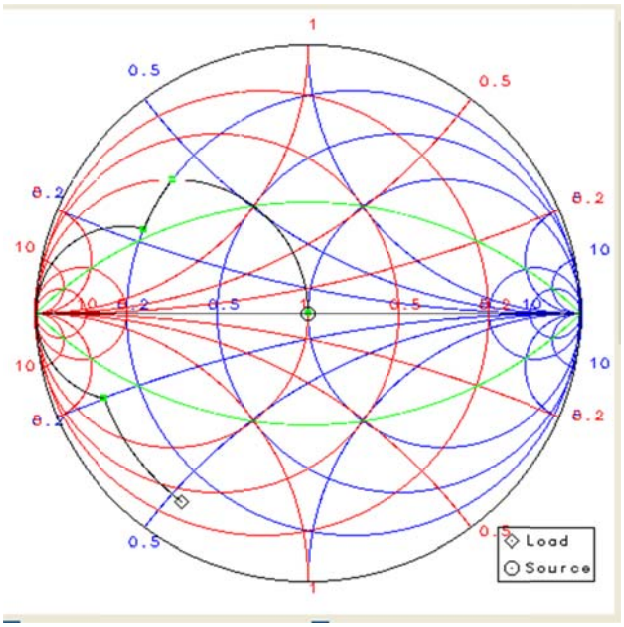



**Figure 4.29:** Smith Chart based input matching circuit design result

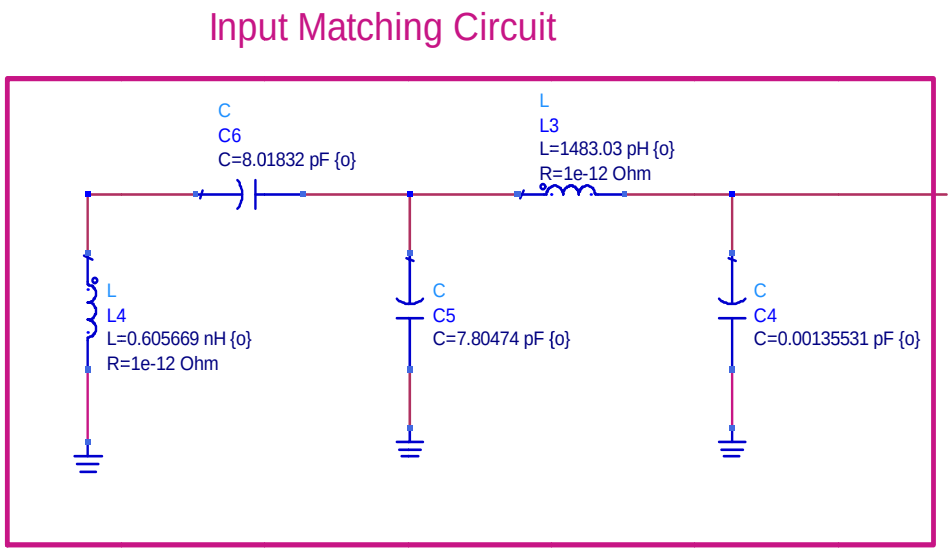



**Figure 4.30:** Input matching circuit

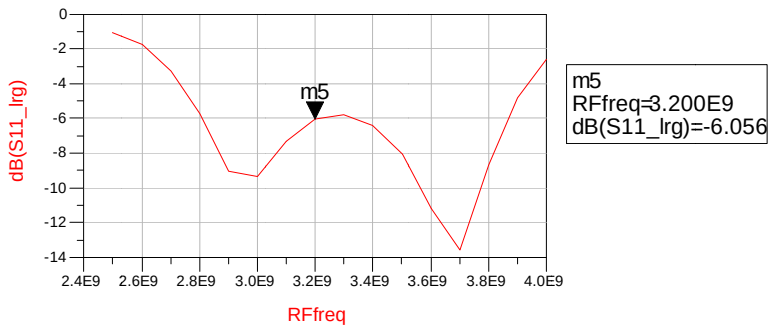



**Figure 4.31:** Large signal S11 parameter

The large signal S11 can be further improved through optimizing the input matching circuit so that it gives -10 dB but we will satisfy with this result here. Since our aim is not to design best performed PA.

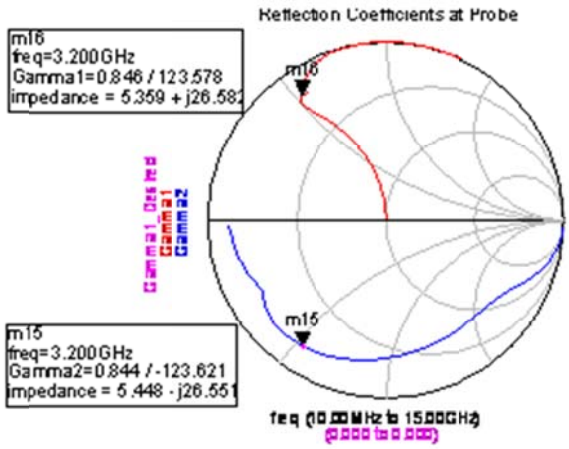



**Figure 4.32:** Input match verification

We see from the figure 4.32 that source impedance presented to the input of the device is close to the complex conjugate of the device's input impedance at 3.2GHz operating frequency.

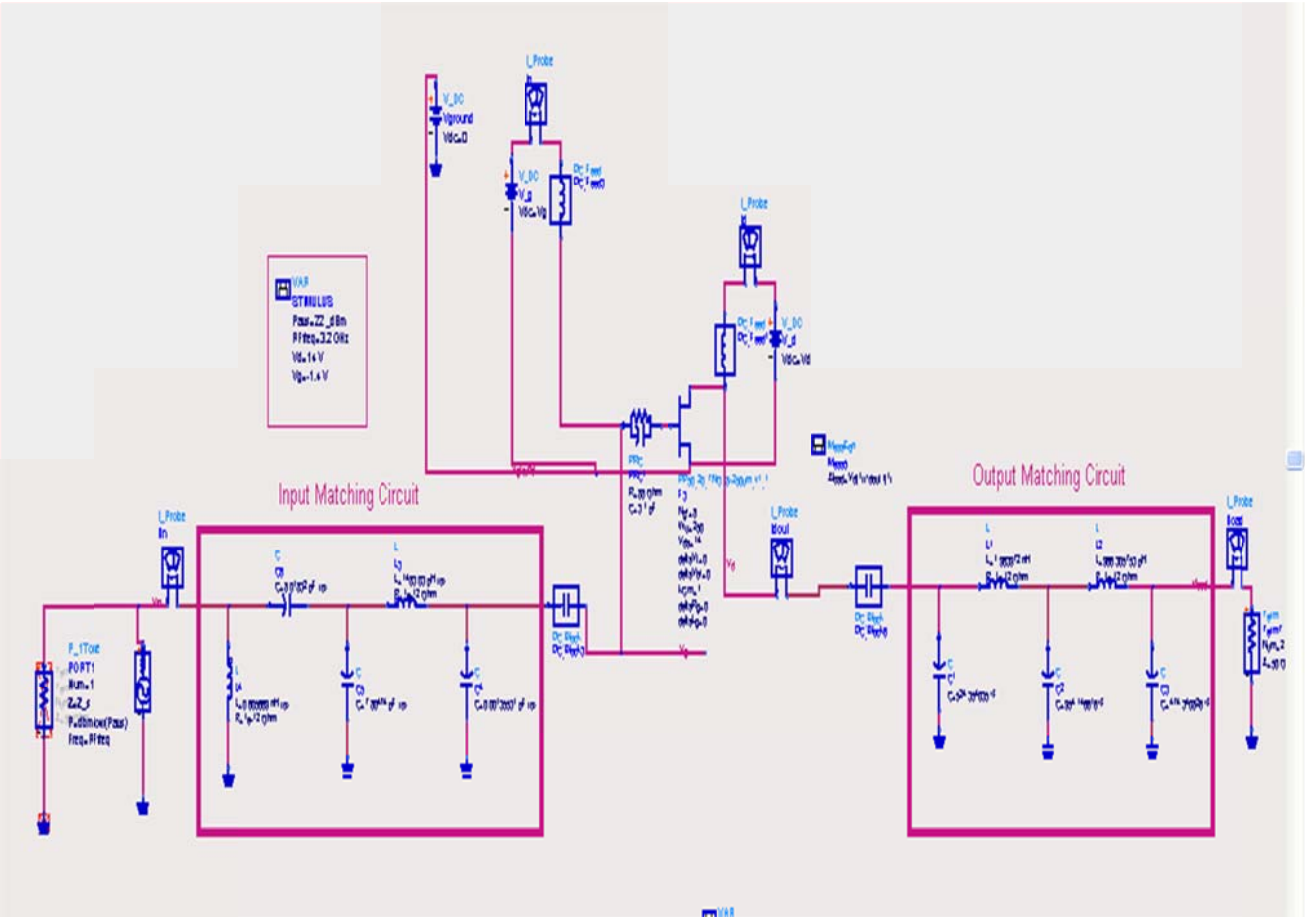



**Figure 4.33:** Designed common source matched circuit

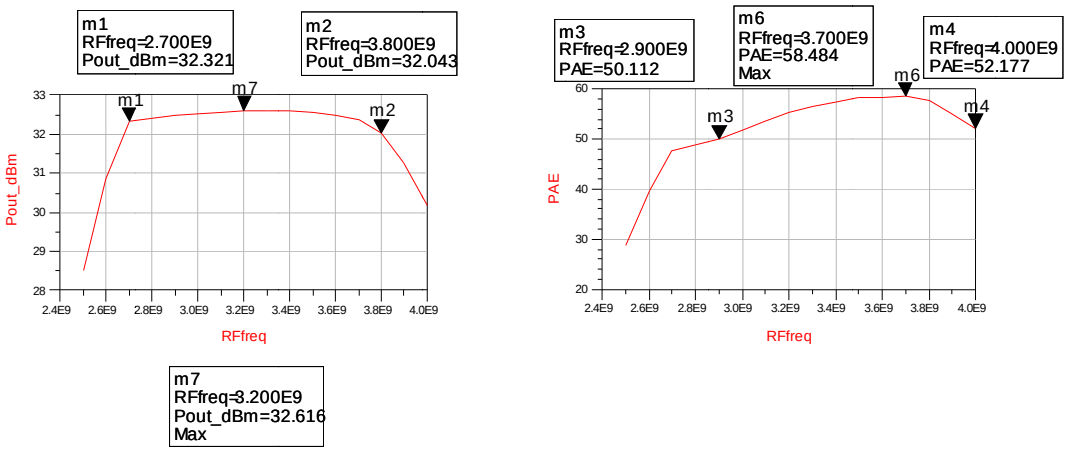



**Figure 4.34:** Pout and PAE vs. frequency for Pavs=22dBm, Vd=14Vand Vg=-1.4

We start again with determining the optimal load impedance (57.15+j38.15 Ohms) which is present to the output of the device.

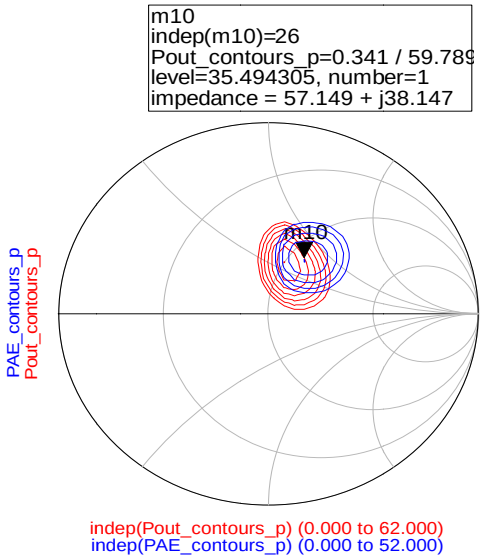



**Figure 4.35:** Load pull result for cascode stage

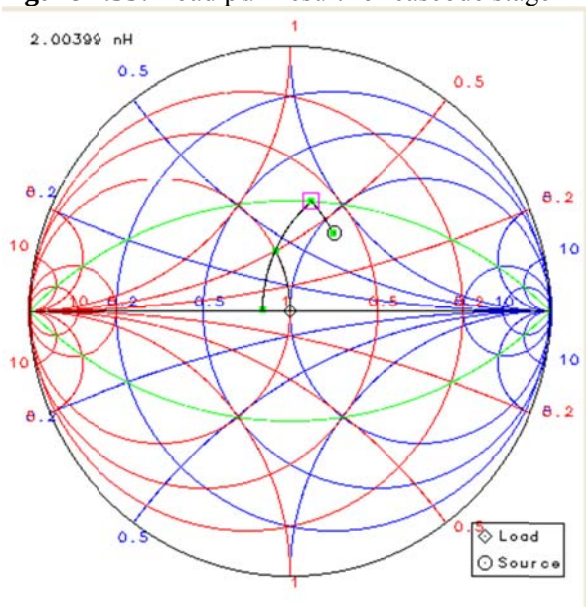



**Figure 4.36:** Smith Chart based output matching circuit design result

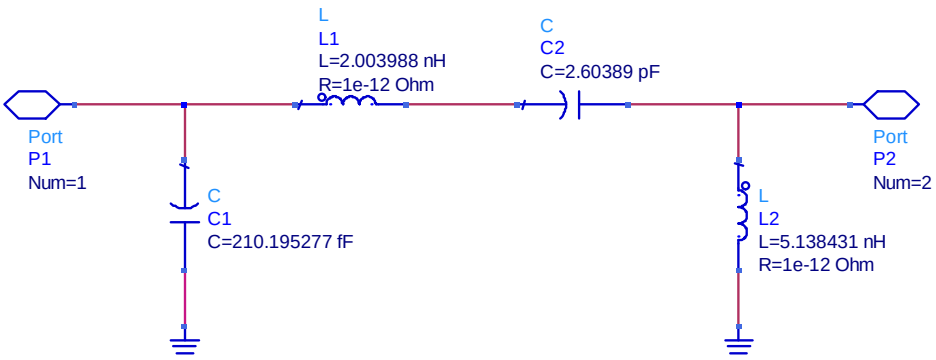



**Figure 4.37:** Output Matching Network for stacked linear PA

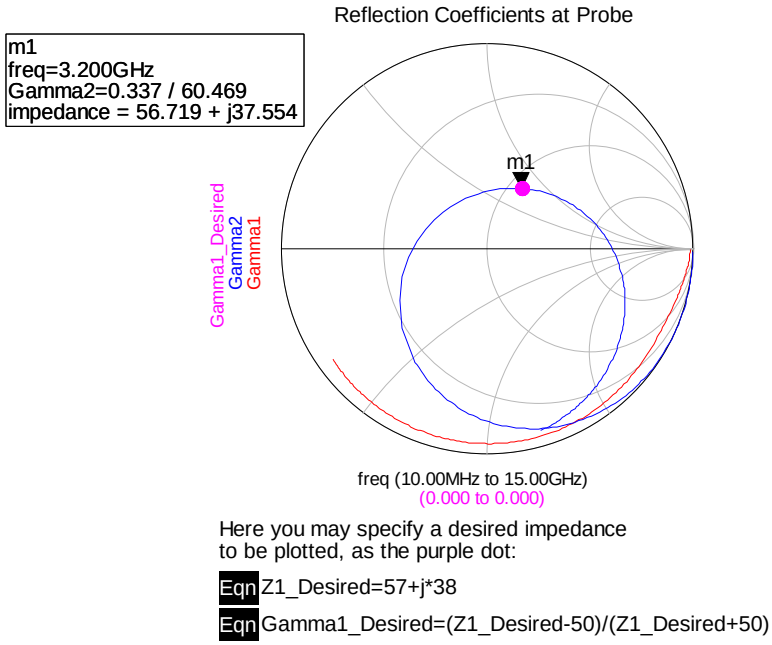



**Figure 4.38:** Output Match verification

The design procedure is the same as we for the common source stage. Also we see from the figure 4.38 that our output matching circuit is matched very well with a broadband characteristic. Next step is determining the large signal Zin and conjugately match the input according to this impedance value.

## *Input Matching Network Design for Stacked Class AB PA*

The design steps of input matching circuit are given below. We follow exactly the same procedure for designing the input matching circuit as we done for the common source stage.

| freq | Zin<br>RFfreq=3.200E9 |
|---|---|
| 0.0000 Hz | <invalid> |
| 3.200 GHz | 5.733 - j14.842 |
| 6.400 GHz | -50.000 + j-0.000 |
| 9.600 GHz | -50.000 + j0.000 |
| 12.80 GHz | -50.000 + j-0.000 |
| 16.00 GHz | -50.000 + j0.000 |
| 19.20 GHz | -50.000 + j-0.000 |
| 22.40 GHz | -50.000 + j3.445E-15 |
| 25.60 GHz | -50.000 + j-0.000 |

Large signal
Zin @f0=3.2 GHz

**Figure 4.39:** Large signal Zin @ 3.2GHz

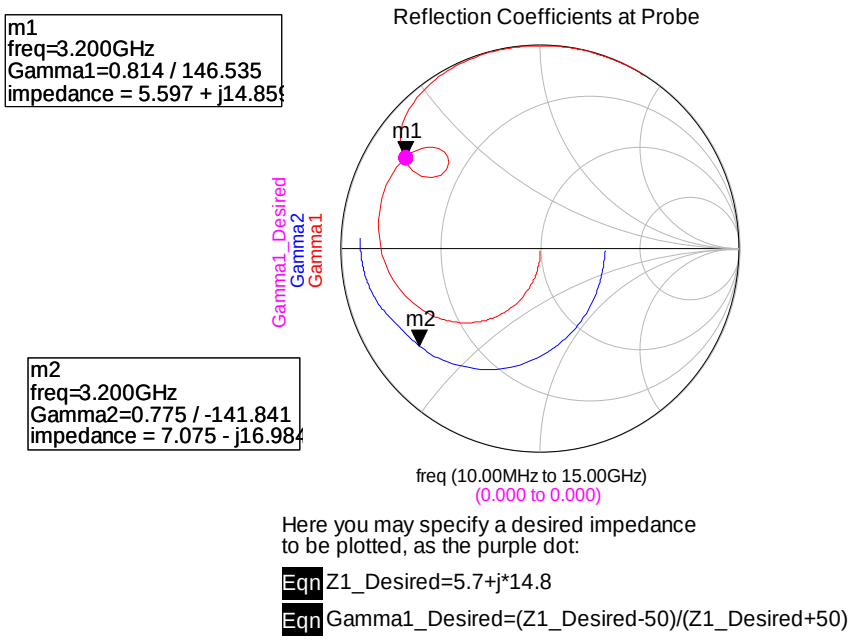



**Figure 4.40:** Input Match verification

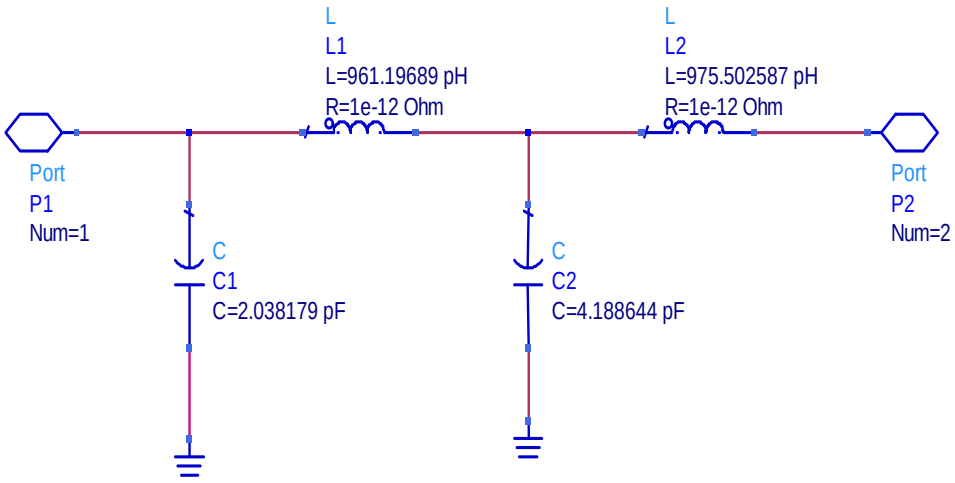



**Figure 4.41:** Designed input Matching network for stacked PA

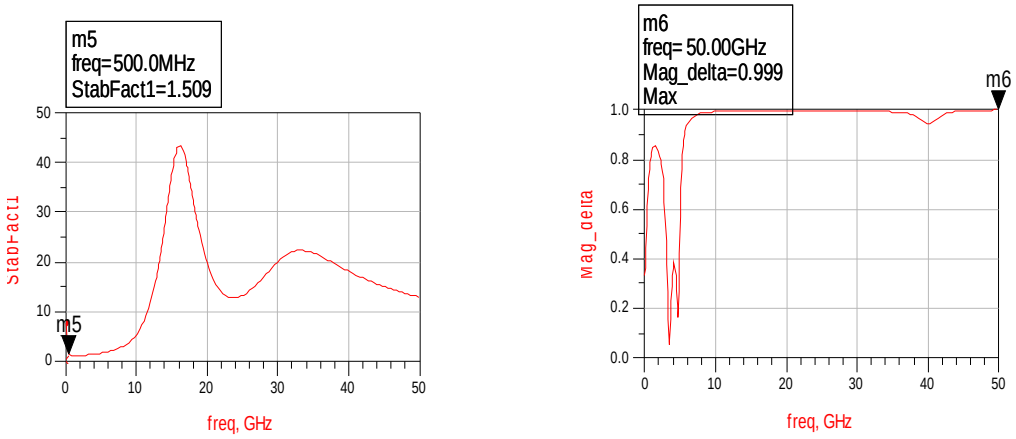



**Figure 4.42:** Unconditional stability verification of the designed stacked PA

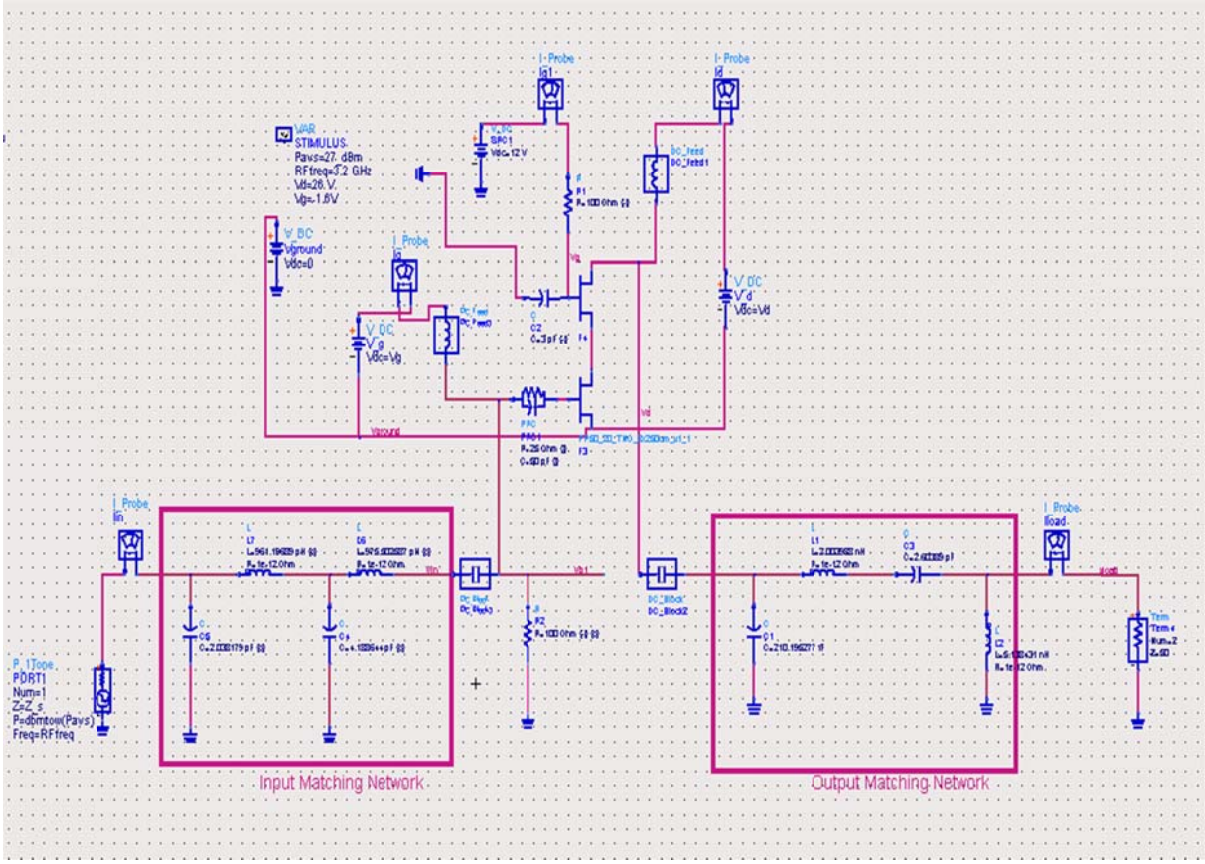



**Figure 4.43:** Designed matched version of stacked class AB PA

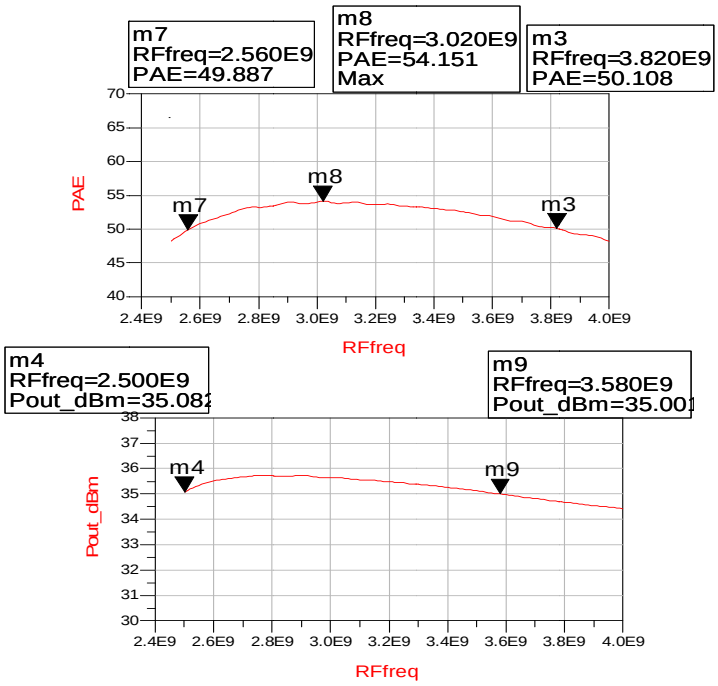



**Figure 4.44:** PAE vs. Freq and Pout vs. Freq

# 5. CIRCUIT SCHEMATIC OF THE DESIGNED CASCODE 'LINEAR' PA WITH NON-IDEAL COMPONENTS

Below we see the input/output matching circuits of the designed PA. And in figure 5.4 the whole circuit is given. The values are not good to see but it is included just for the completeness.

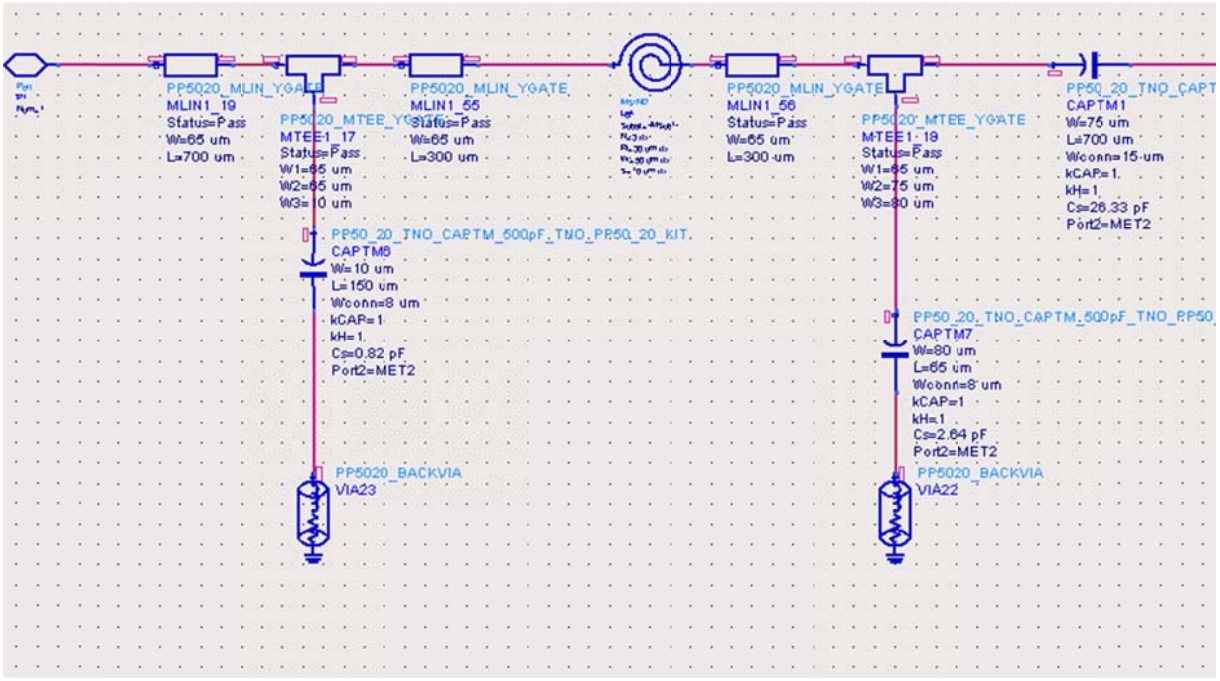



**Figure 5.1:** Input match circuit

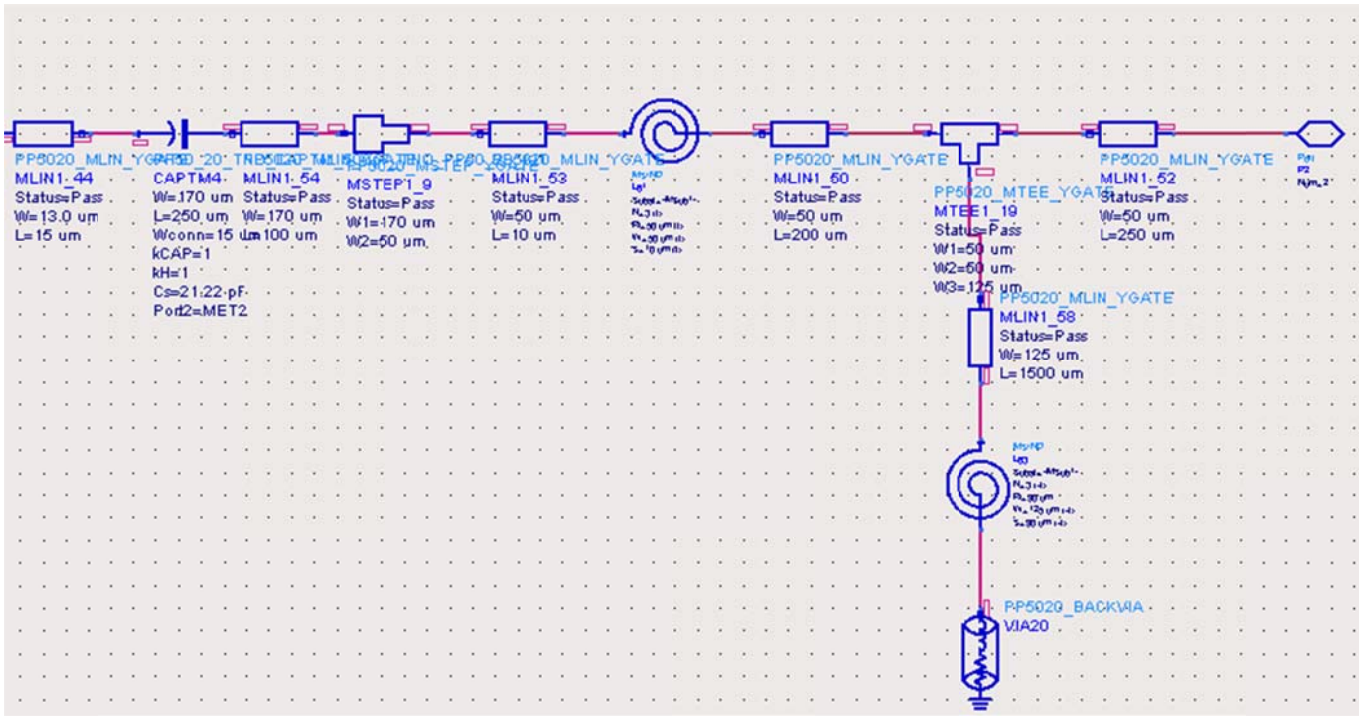



Figure 5.2: Output match circuit

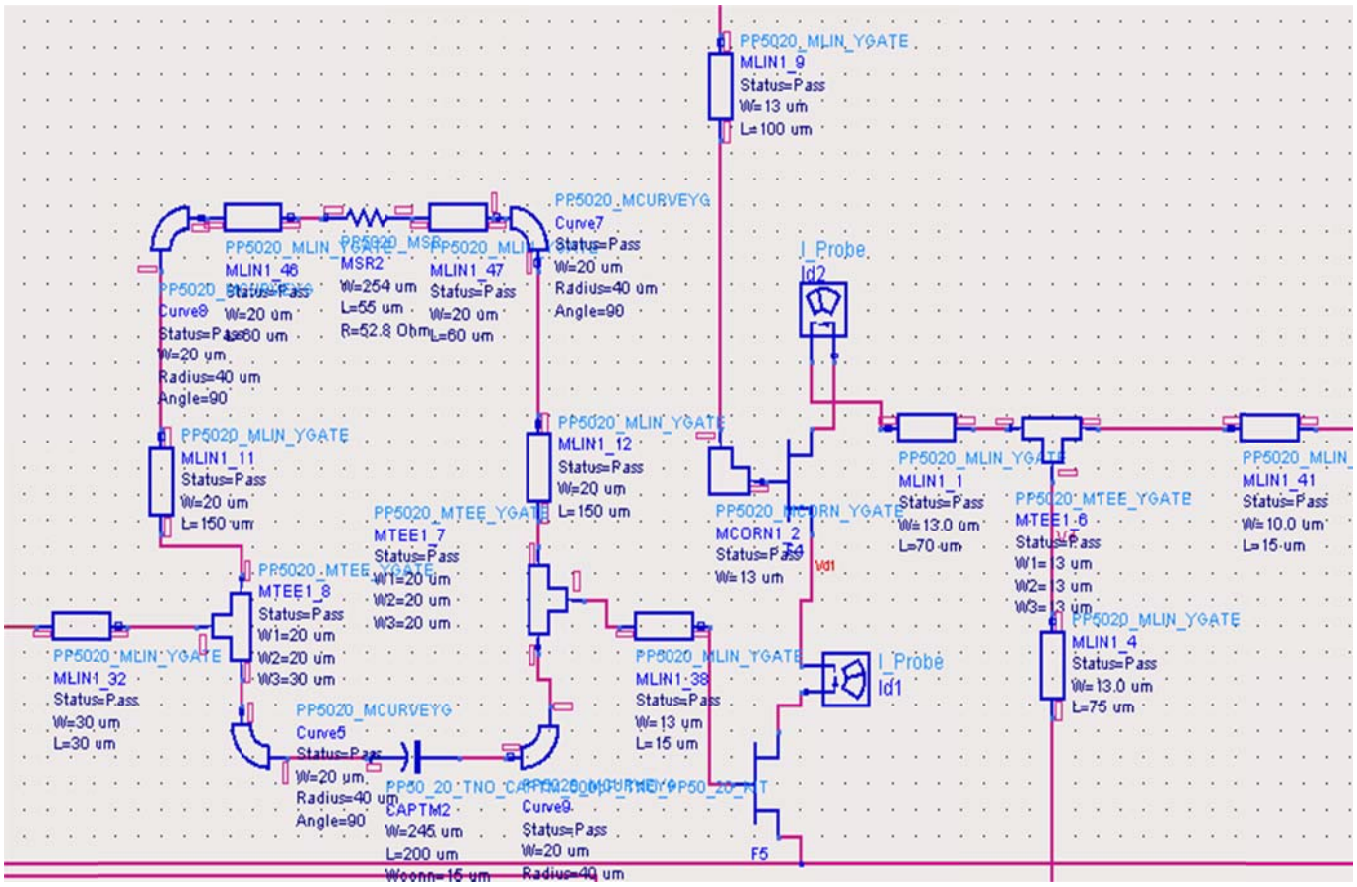



Figure 5.3: Active devices with RC stabilization circuit

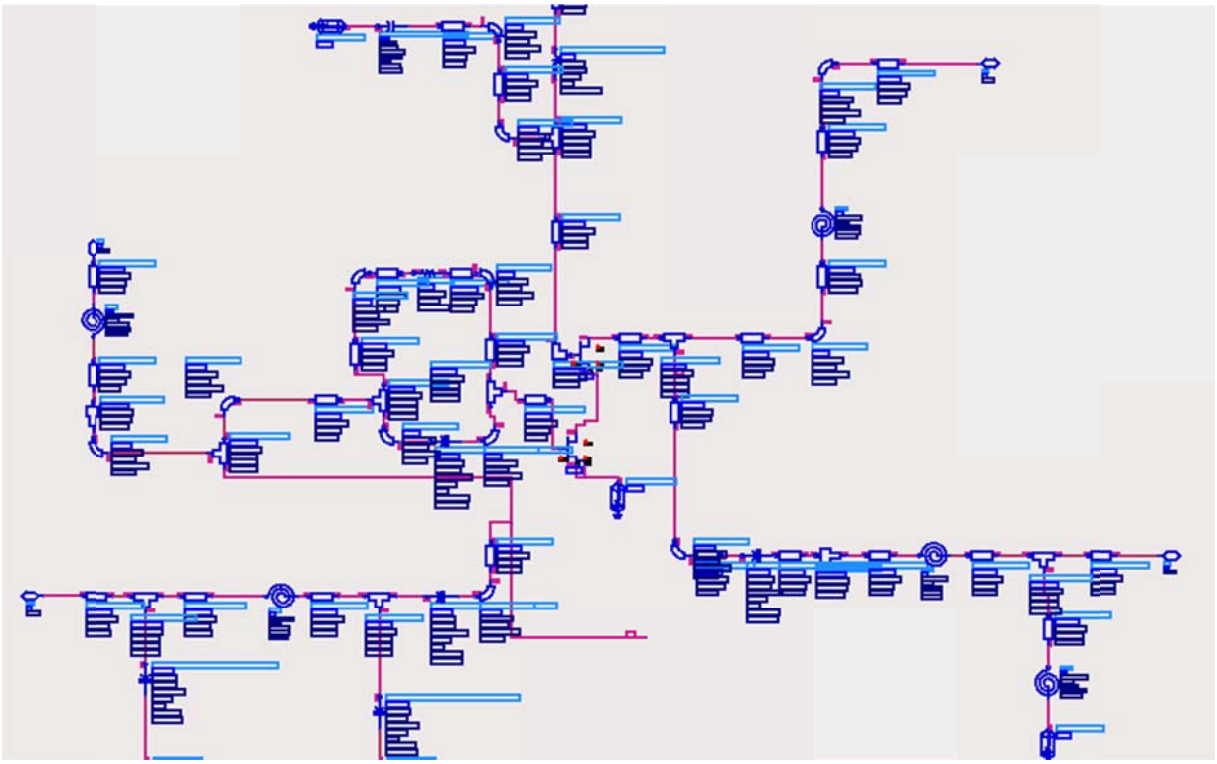
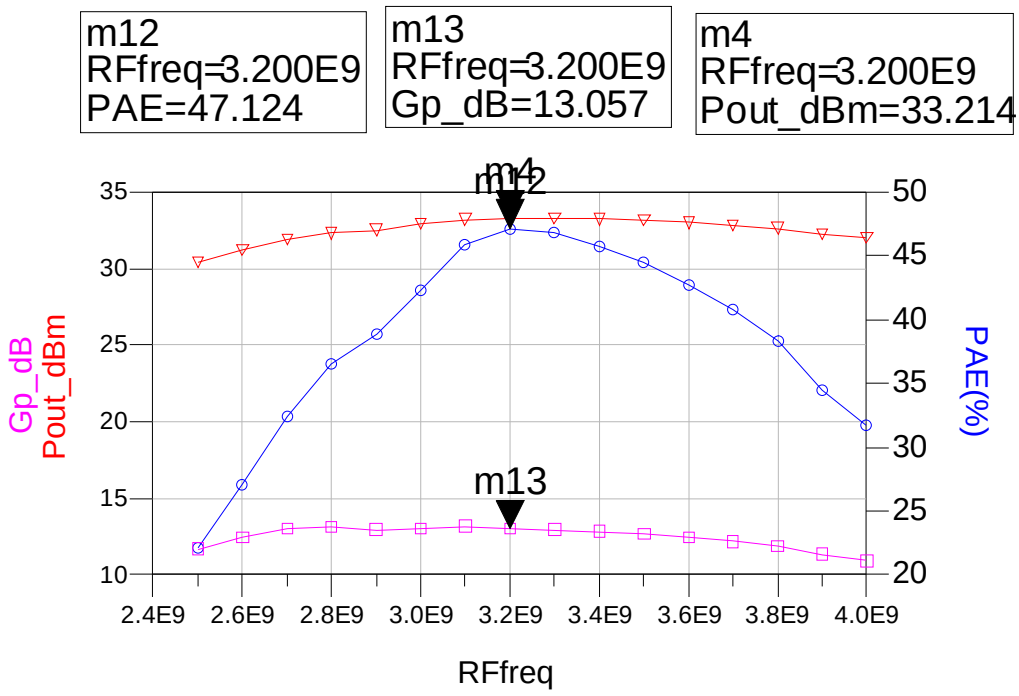
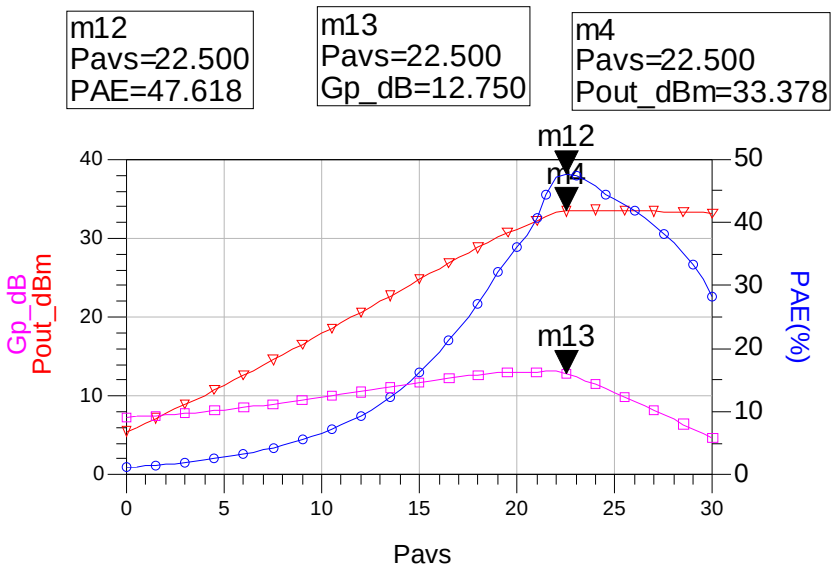


**Figure 5.4:** The whole circuit

## 5.1 PERFORMANCE OF THE PA WITH NON IDEAL COMPONENTS

In figure 5.5 the performance merits of the designed PA given .



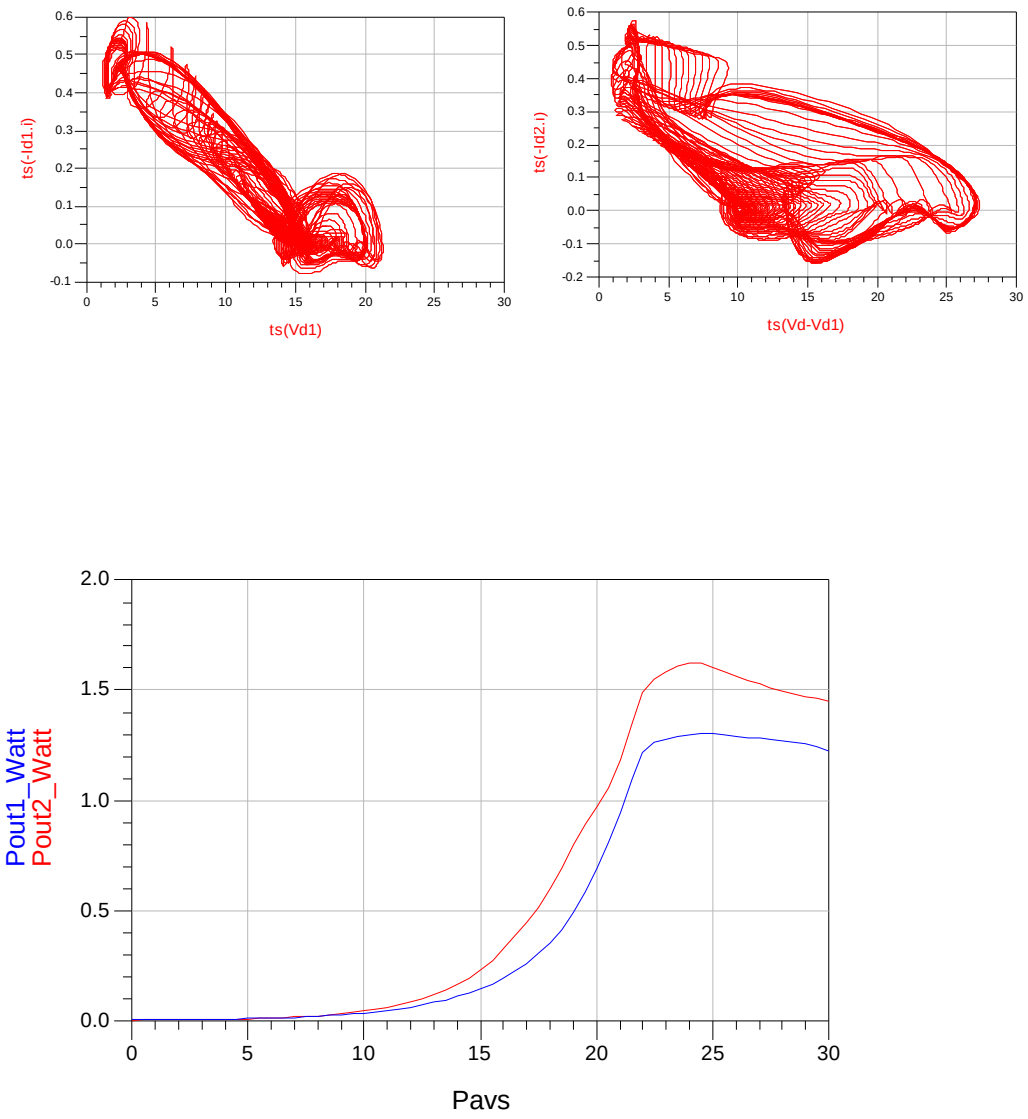



**Figure 5.5:** Pout, PAE and Power Gain vs. freq of the cascode PA with non ideal components for Vd=24 V, Vg =-1.58V and Pavs=22 dBm and load lines of both transistors.

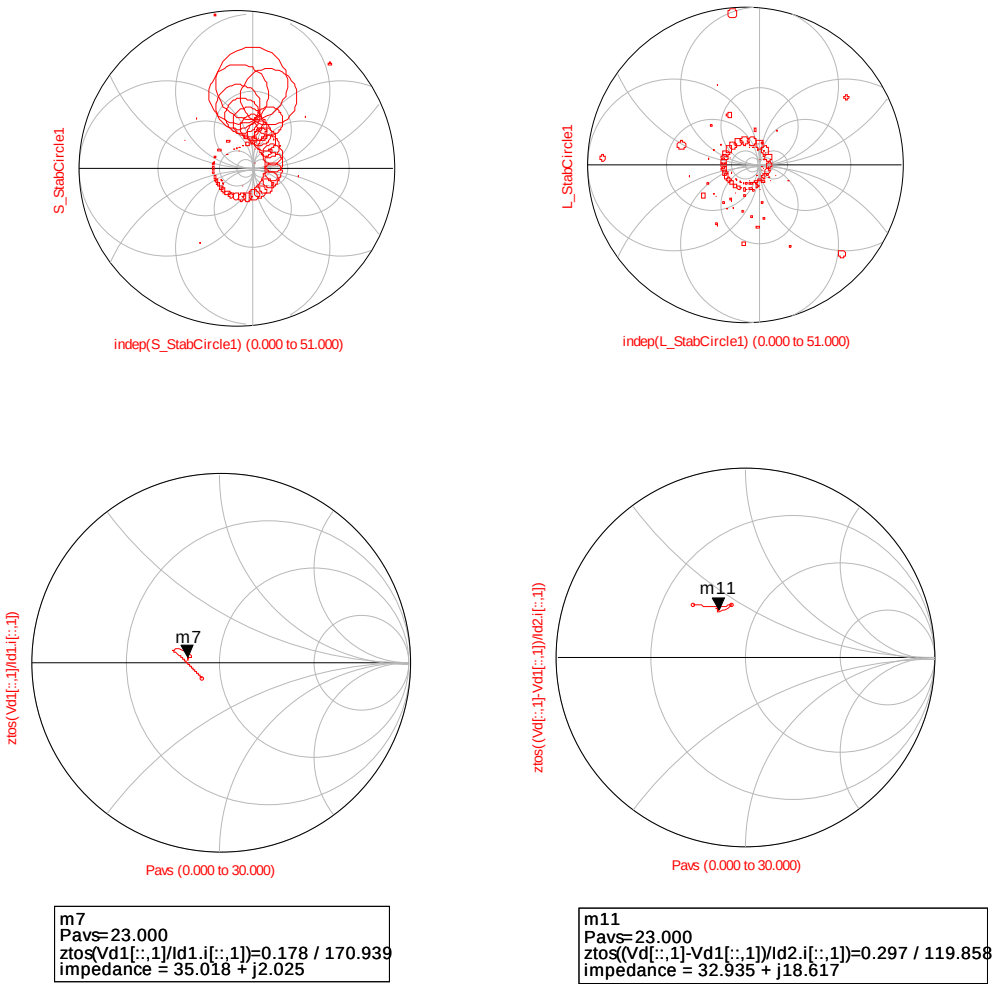



**Figure 5.6:** Source and Load stability circles above and impedances seen from the drain of the both transistors given in the plots below.

The designed PA shows a 47% peak PAE and 10 % bandwidth over S band with PAE of 43% and about 33.3 dBm peak output power.

## 5.2 LAYOUT OF THE CASCODE POWER AMPLIFIER

The complete schematic of the designed **P**A is given in the figure below.

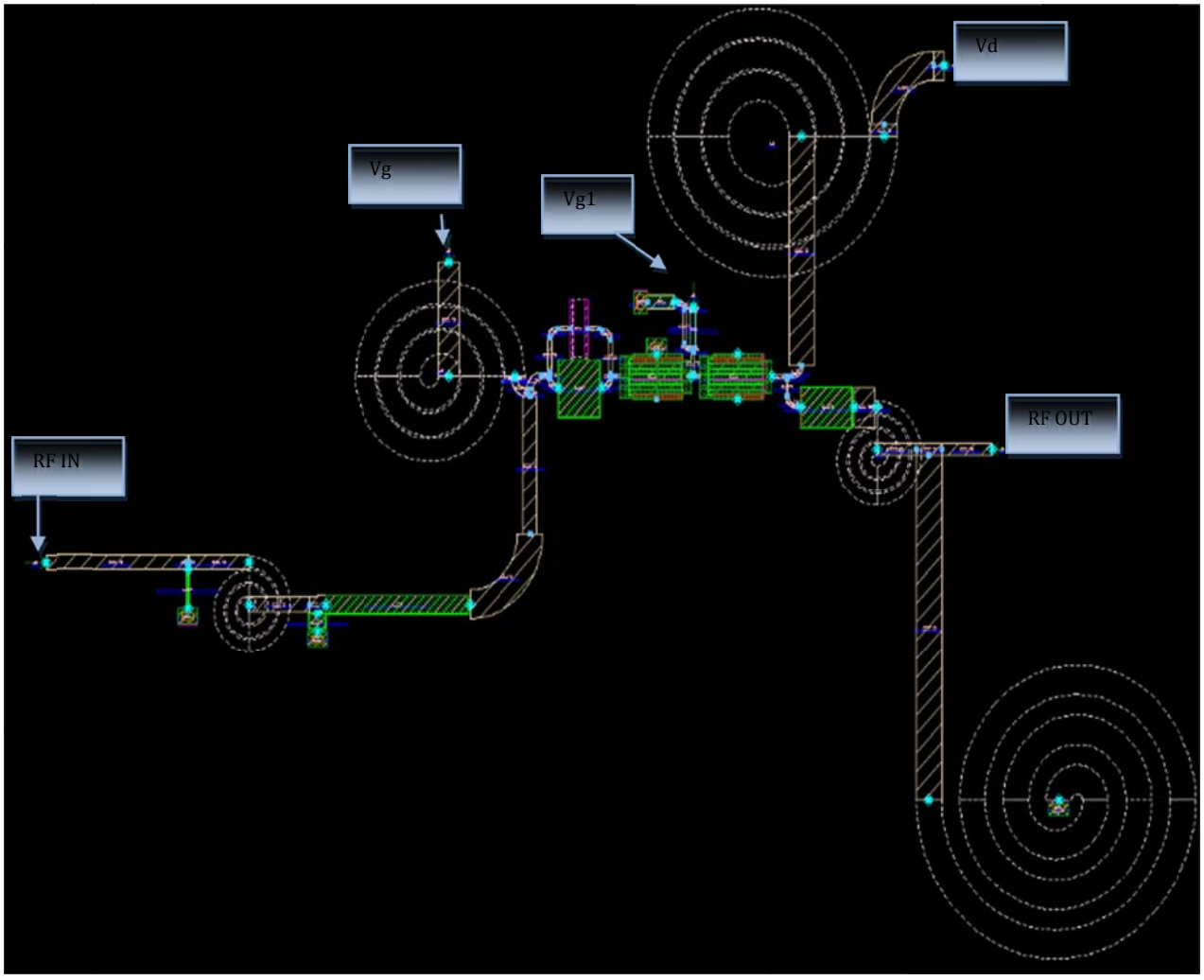



FIGURE 5.7: THE LAYOUT OF THE WHOLE CIRCUIT

# 6 CONCLUSIONS AND RECOMMENDATIONS

In this project we have investigated the benefits of the stacked configuration in the power amplifiers for radar systems at microwave frequencies; more specifically at S band with a centre frequency of 3.25 GHz. Therefore we have first designed a common source stage amplifier and compared the performance of this amplifier with the stacked version of that amplifier. Besides that we have also designed a switch mode PA in order to see the performance of this kind of amplifier at the high frequency range; especially with the aim of increasing the PAE along with the output power using it in a stacked configuration.

It is known from the literature study that the stacked configuration provides us a 3dB more output power compared to the common source stage PA. But there is not so much information available about the benefits of stacked configuration in the sense of PAE, influence on the bandwidth characteristics, robustness of the stacked configuration on the load impedance variation etc. Therefore in this work it is also tried to find answers to these questions.

The important point in using of the stacked structure is the addition of a capacitor between the gate of the FET and ground. This capacitor plays an important role in adjusting the impedance level seen by the drain of active device. This impedance adjustment is important since the optimum power from the active device is delivered only when the output of the device is matched to the optimum impedance. [22].

An additional capacitor is also used between the drain source terminals of the top transistor to make it possible to obtain twice the output conductance of a single common source transistor. [16]. However during the simulations it is observed that using this capacitor cause difficulties in achieving the unconditional stability condition. It is also pointed out in [16] that in most cases this capacitor could not be integrated because of its low value.

Having dealt with these issues, it is time to summarize results of this thesis:

- We have shown in this work that the stacked structure provides 3 [dB] (2 times) more output power for both types of PAs (for the linear PA and for the SMPA) than the single stage versions at S band frequency range.
    - The common source PA that is biased in class AB mode gives 32.4 dBm Pout with a bandwidth (BW) of 37.5% while the stacked version of this PA gives 35 dBm Pout with a 56.3% BW.
    - The single stage SMPA gives 30.5 dBm Pout with a 15.6 % BW while the stacked version of this SMPA provides 33.5 dBm Pout with 31.2% BW.
- The Power added Efficiency (PAE) of the switch mode PA (SMPA) is better than that of the ‘linear’ PA but the achieved bandwidth @S band with SMPA is less than the linear version.

- The PAE for the single stage 'linear' PA is 51% with a 31.3% BW which is also 51% for the stacked configuration of this PA with a BW of 55.4 %
- The PAE for the single stage SMPA is 60% with a 9,7% BW and 55% for the stacked stage SMPA with a BW of 31.2 %

- Power gains are also increasing in stacked configuration compared to the single stage.

  - The power gain for the single stage linear common source PA is 11.2 dB which is 13.2 dB for the stacked stage
  - The power gain for the single stage SMPA is 14.3 dB while it is 15.8 dB for the stacked version.

  For a clearer overview of these results see the tables 5.1.2 and 5.2.3

- Stacked configuration results in a higher output impedance which minimizes the losses of output matching circuit.

  - Zopt_single=36.108+j13.4 [Ohms] for the common source stage while it's Zopt_cascode= 57.15+j38.15 [Ohms] for the linear stacked PA.

In this project we have used 0.5um GaAs pHEMT technology. However if the cost is not primary concern, GaN technology would probably result in a much better performance in the sense of output power, PAE and gain than the GaAs technology.

There are several papers which are show the superiority of GaN technology comparing with the first generation semiconductor Si, Ge and second generation compound semiconductor GaAs, InP. In order to compare GaAs and GaN technology performance we will provide here two different designs from the literature.

In [26] the GaN Monolithic Class E Power Amplifier that is measured under three pulsed drain voltages at 7.5 GHz gives the following results (67%, 36.8 dBm @ 20 V), (64%, 37.8 dBm @ 25 V) and (58%, 38.3 dBm @ 30 V). Also the load possesses a broadband class-E performance showing a nearly frequency independent response over 6.0-12.0 GHz. So in this design one octave bandwidth is achieved with a high PAE along with a high output power thanks to GaN technology.

The S band HPA which is designed for radar application by SELEX Sistemi Integrati S.p.A. Engineering Division (Rome Italy) has the following properties: In the frequency bandwidth 2.4-3.6GHz, the HPA biased at Vd=10V delivers an output power of 20W @ 4dB of gain compression, with an associated PAE of circa 28% in 0.5μm GaAs PHEMT technology.

If we now compare these two designs, we see that in [27] very poor PAE is achieved at S band. Also to achieve 20 Watt Pout they had to use more active devices in parallel. The HPA in [26] which uses GaN technology shows a PAE of 67 % and 36.8 dBm output power at the operating frequency 7.5 GHz. It is shown in that work that the (min. & max.) values for PAE and power over 7.0 -11.0 GHz at 30 V drain bias are: (43%-57%) and (37.0-37.9 dBm) respectively.

As a comparison of our cascode PA with a similar work, we can give the result which is performed by Amin K Ezzeddine and Ho.C Huang [22] because their circuit operates also at the same frequency range. So this would give a bit fair comparison.

Their circuit operates at 3.5 GHz. The P1dB is 31.5 dBm with a PAE of 42% at 1 dB compression. There is no bandwidth information available in their work.

Our PA shows a 47% peak PAE and 10 % bandwidth over S band with PAE of 42% and about 33 dBm peak output power. The operating frequency is 3.2 GHz

This comparison shows us that our circuit has some better performance merits but actually a fair comparison is not possible because each design has different design specifications.

An important conclusion might be that using a switch mode PA along with GaN technology can offer us a high PAE with a high output power in compare to the linear mode PAs in other technologies than GaN. We have to also note here that the work in [26] which is performed through Raytheon Space & Airborne Systems uses a different load network than the classical ones which is stated in that paper. And it's entirely not explained; probably because of the confidentiality. So with the load networks for class E PAs, that are covered in the literature it is almost impossible to achieve such a high bandwidths with such a high PAE at S and X bands. In the future works this kind of better performed load networks for class E PAs can be investigated first. Using the better output power performance of cascode stage this would result in a best performed PA at high frequencies.

As a final word we can say that using cascode configuration in a SMPA or harmonic termination applied to a linear PA in GaN technology will result best performance parameters for a HPA.

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