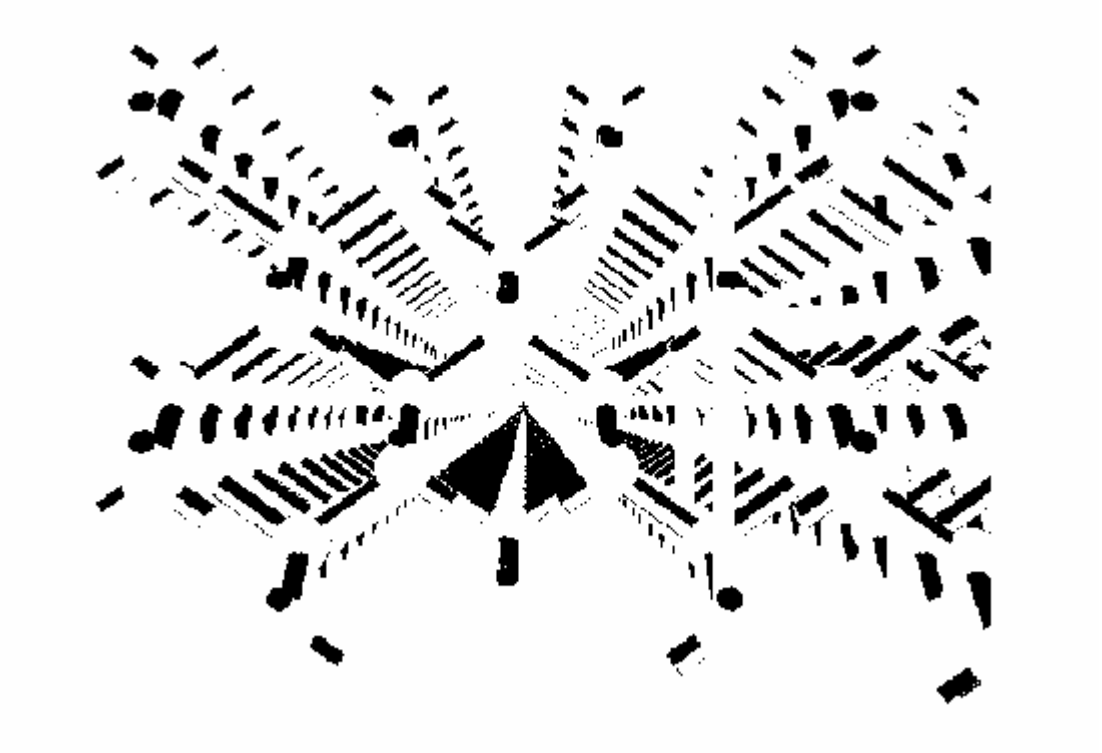
Dislocation engineered silicon Light Emitting Diode



2005
M.Sc. thesis: 068.043/2005
Bob Schippers

University of Twente
Department of Electrical Engineering,
Mathematics & Computer Science (EEMCS)
Semiconductor Components Group (SC)

P.O. Box 217
7500 AE Enschede
The Netherlands

Thesis committee: **T. Hoang**
Dr. A.Y. Kovalgin
Prof. Dr. J. Schmitz

University of Twente
The Netherlands

Abstract

Since the 60's silicon rapidly became the dominant material due to its superior oxide quality in combination with CMOS-technology. The silicon fraction of the semiconductor market is around 95% with the remainder dominated by III–V semiconductors. Two drawbacks of silicon compared to some other *III–V semiconductors* are its indirect band gap and low electron mobility.

Despite silicon's indirect band gap there have been great efforts over the past decade to obtain technologically viable and efficient light emission from silicon with operating wavelengths in the range of 0.45−1.6μm (2.8−0.7eV) to cover both full color displays and fiber optics operating wavelengths of 1.3 and 1.55μm.

The driving force behind silicon optics is the interconnect problem in computer chips. The electronics and computing sectors have been driven by the exponential growth in processor power and speed. This growth has been achieved by the systematic shrinking down of the transistor dimensions enabling more and more transistors to be formed in the same area of silicon thus increasing the speed and power of the chip. As the transistors need to be connected together essentially by wires referred to as metallization, there is a time delay associated with electron transport in the metallization and this time does not scale.

The solution to this interconnect problem is the replacement of at least some of the metal interconnects with optical interconnect.

Given the huge tool up costs in the microelectronics industry new approaches are closely compatible with silicon Ultra Large Scale Integration (ULSI) technology. The key technology for the fabrication of silicon chips is ion implantation. Dislocation engineering is based upon ion implantation and annealing to engineer defects at approximately the implantation depth that are supposed to enhance light emission out of silicon.

Diode sets have been prepared for different implants and anneals to engineer respectively depth of the defects with respect to the light emitting surface area and defect density/ defect radius. By proper choice of the annealing budget the dominant defect is a so called dislocation loop.

Diode sets DILED1 and DILED2 have been fabricated by boron implantation with energies in the range 40 − 100keV, annealing temperatures in the range 850 − 1100°C and doses in the range 1×10^{15} – 1.6×10^{15}cm^{-2} to compensate for decreasing peak concentration with increasing implant energy. Diode set DIFLED has been fabricated by single, double or no silicon implants in boron diffused junction with energies in the range 0 − 450keV, annealing temperature of 950°C and each dose equal to 1×10^{15}cm^{-2}.

DILED1, DILED2 and DIFLED I-V characteristics have been measured and light intensity measurements have been performed in the wavelength range 950 − 1300nm. Electrical parameters that have been derived and compared to estimated values are: *photo current*, *saturation current*, *thermal voltage equivalent*, *ideality factor*, *junction voltage* and *bulk resistance*. The electrical parameters have been compared to find a correlation with optical parameters *peak intensity* and *standard deviation in peak intensity* but no trends were observed.

The maximum peak intensity was situated around 1154nm and belonged to diodes annealed at 1100°C originating from diode set DILED2. This maximum peak intensity was weakly dependent upon the energy range 40 − 70keV. The average deviation in peak intensity was 4.2%. This maximum peak intensity has been compared to that of a DIFLED "no silicon implant in boron diffused junction" diode that served as reference. Main conclusion: dislocation loops do not seem to enhance light intensity.

Acknowledgement

When people are about to finish a certain period in their lifes they start reflecting. The same holds for me. Looking back it became clear to me that solid state phyics always was my first and only love. It started in the final year of high school when my teacher of science at that time described the behavior of a bipolar transistor. That intuitive way of thinking, fascinating. That world of thought fiscinates and at the same time suites me until this day on.

After some flirts with other chairs at the faculty of electrical engineering, I returned to my first and only love. The chair of Semiconductor components (SC) headed by Prof. J. Schmitz turned out to be a good choice. Due to the freedom I have been given, I was able to go into details whenever I felt it was necessary. Especially chapter *3.4 The dominant defects introduced by the implantation process: {311} Rod-like defects, Frank faulted loops and perfect prismatic loops*, was my pet project.

Special thanks to

Tu Hoang, Dr. Alexey Kovalgin and Prof. Jurriaan Schmitz, members of this thesis committee, for giving me a lot of freedom;
Ludmilla Fedina of the Institute of Semiconductor Physics, Novosibirsk, Russia, for her endless efforts trying to answer my questions put by email and sharing her profound knowledge of silicon defects;
Jisk holleman for giving me insights, concerning I-V characteristics that putted me on the right track while analyzing the electrical measurements.

Enschede, July 14 2005

Bob Schippers

Table of Contents

Dislocation engineered silicon Light Emitting Diode

Part I – Literature report

University of Twente
The Netherlands

1 Introduction

Silicon dominates the current semiconductor market because of its widespread use in microelectronics.

"The electronics market is currently worth around 1500 billion dollars per annum with an underlying growth of around 7% per annum. The semiconductor contribution to this is around 20% or around 300 billion dollars per annum predicted to increase to around 40% by 2010.

Figure 1-1: A dazzling amount of money circulates in the semiconductor industry.

The silicon fraction of the semiconductor market is around 95% with the remainder dominated by III–V semiconductors. The III–V sector although much smaller is crucial because it provides devices of superior performance and additional functionality than Silicon for several key device areas, for example laser diodes for optical communication systems[7]."

Since the 60's silicon rapidly became the dominant material due to its superior oxide quality in combination with CMOS-technology. Because MOS-transistors are surface devices, the conducting channel is formed at the interface between the Si and the SiO_2 gate oxide, this oxide needs to be high quality.

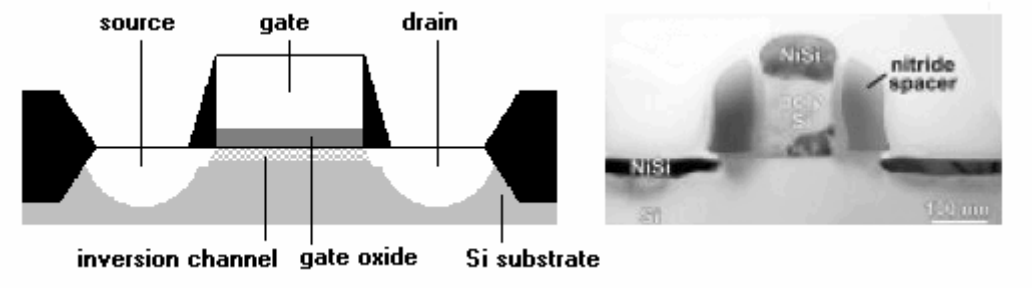


Figure 1-2: CMOS-transistor schematic and TEM.

Two drawbacks of silicon compared to some other *III–V semiconductors* are its indirect band gap and low electron mobility. Consequently only optical emitters and **H**igh **E**lectron **M**obility **T**ransistor**s** (HEMTs) or **M**odulation **D**oped **F**ield **E**ffect **T**ransistor**s** (MODFETs) based transistors are based upon *III–V semiconductors*, all other devices are silicon based. This specific group of transistors is used in microwave satellite amplifier circuits.

"There have been great efforts over the past decade to obtain useful, that is, technologically viable and efficient, light emission from silicon both in the visible and infrared regions of the spectrum. In the visible regions, porous silicon and other quantized systems, such as silicon/silicon dioxide super lattices and silicon nano precipitates in silicon dioxide, have been the main emphasis. In the infrared region, systems such as erbium in silicon, silicon/ germanium and, more recently, iron disilicide offer potential routes. No approach has so far been applied commercially. The reasons for this are a combination of the lack of genuine or perceived compatibility with conventional ULSI technology[1]."

The driving force behind silicon optics is the interconnect problem in computer chips. The electronics and computing sectors have been driven by the exponential growth in processor power and speed. This growth has been achieved by the systematic shrinking down of the transistor dimensions enabling more and more transistors to be formed in the same area of silicon thus increasing the speed and power of the chip. As the transistors need to be connected together essentially by wires referred to as metallization, there is a time delay associated with electron transport in the metallization and this time does not scale. Thus as the length scale of the devices decreases, electrons will spend increasingly more of their time in the connections between components. Consequently a limit to classical scaling is reached within the next decade when computer chips will stop getting faster.

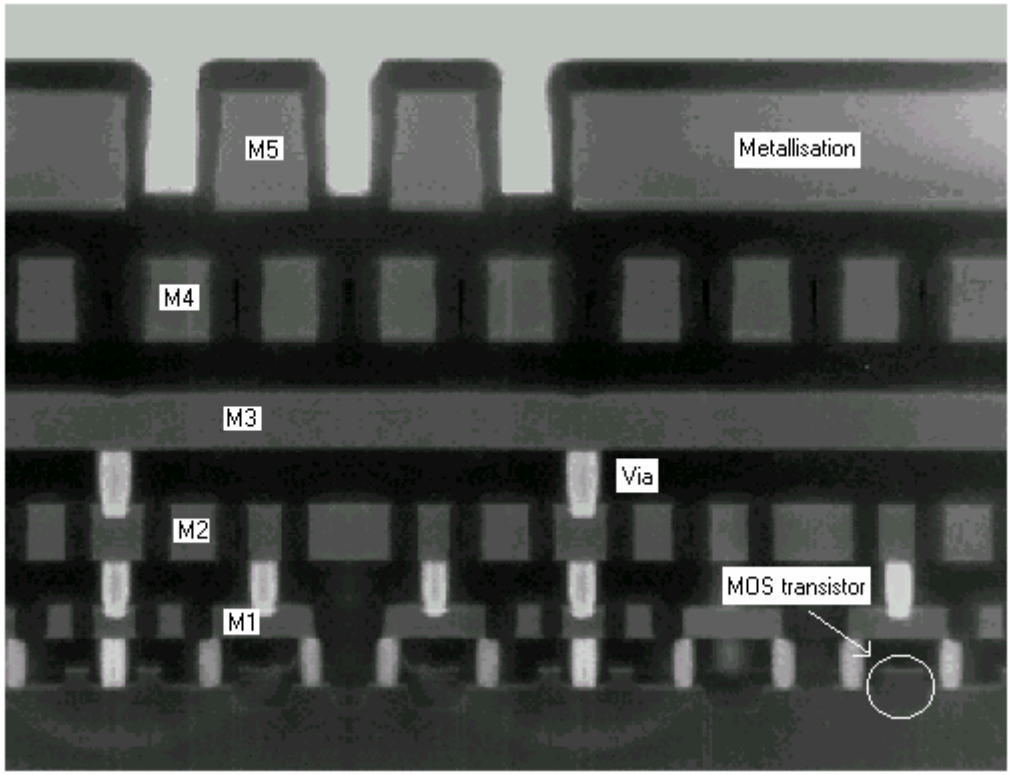


Figure 1-3: Bulk of metallization to connect MOS-transistors.

“For the year 2010 an electrical interconnect pitch of 140nm and a total length of interconnects per chip of 20 km are predicted, which would lead to a power dissipation of more than 60% of the total power consumption of the chip by the interconnects only[40x].”

The solution to this interconnect problem is the replacement of at least some of the metal interconnects with optical data transfer on chip. The development of optical pin outs and inter chip and inter board optical connections are also seen to be required for use in optical communication technologies such as fiber optics or displays. “Operating wavelengths in the range of 0.45–1.6μm (2.8–0.7eV) are needed to cover both full color displays and fiber optics operating wavelengths of 1.3 and 1.55μm[18].

“Given the huge tool up costs in the microelectronics industry, for example fabrication facilities are currently 2–3 billion dollars to set up, the industry is very conservative about new processes and materials. It is therefore a requirement that new approaches are closely compatible with silicon ultra large scale integration (ULSI) technology. The key technology for the fabrication of silicon chips is ion implantation[7].”

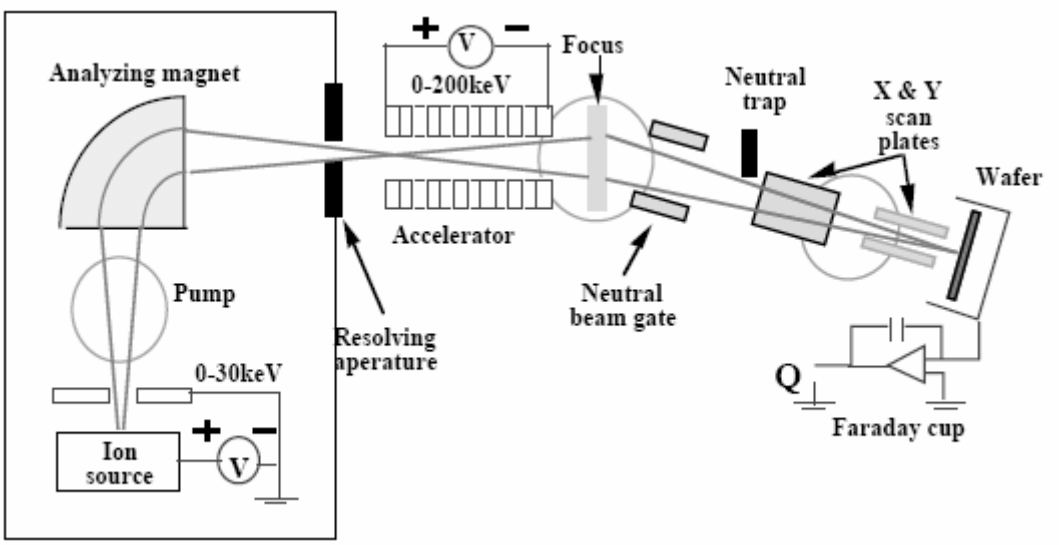


Figure 1-4: Ion implantation schematic.

The major advantage of ion implantation is that it provides a very precise means to introduce a specific dose or number of ions into the substrate. Therefore efficient silicon optical emitters made by ion implantation are preferred.

"One objective of designing an LED must be to achieve a high efficiency. Moreover, the radiation has to have a geometry that allows the optical fibers to collect as much of the optical power as possible, in order to maximize the coupling efficiency. A third objective is to design an LED in which the light output can be directly modulated at high rates with an information-carrying signal by the forward current. Finally, its construction must ensure a rapid discharge of heat from the p-n junction, since the light output drops as the junction temperature rises[34]."

This master thesis at the Semiconductor Components group contributes to the HELIOS project at the University of Twente, the Netherlands. Aim of this project is to obtain **H**igh **E**fficiency **LI**ght Emission **O**ut of **S**ilicon.[1]

In this "literature report", we report on **L**ight **E**mitting **D**iodes made by ion implantation, so called dislocation engineered. Such a device would also form the basis for the development of an injection laser based on the same principles but with the incorporation of an optical cavity. This master thesis describes how dislocation engineering could increase the (quantum) efficiency.

[1] http://sc.el.utwente.nl/tdr/Projects/HELIOS/

2 Silicon as indirect band gap material and poor quantum efficiency

So aim of this project is to develop efficient silicon **L**ight **E**mitting **D**iodes made by ion implantation, so called dislocation engineered.

2.1 Indirect band gap material

An LED is basically a junction diode that operates in forward bias. “From the edge of the depletion layer electrons will diffuse inward to the metal contact of the p-region while they will slowly recombine with the plentiful holes that are available. At a distance of L_n, the diffusion length of electrons, most of them will have disappeared and an equal number of holes must come from the contact to supply the holes that have recombined with the incoming electrons[34].” Holes go *mutatis mutandis* the same way. The only difference is the diffusion length of holes L_p. The diffusion length of holes is approximately 3 times as low as that of electrons.

The amount of recombination decays exponentially from the edges of the depletion layer to the contacts. Therefore most of the surface-emitting LEDs have a thin highly doped n-layer on top with a lowly doped p-layer below[35]. In that way generated photons are generated not far from the surface and have a high chance of being ejected from the substrate. Besides surface emitters also edge-emitters exist.

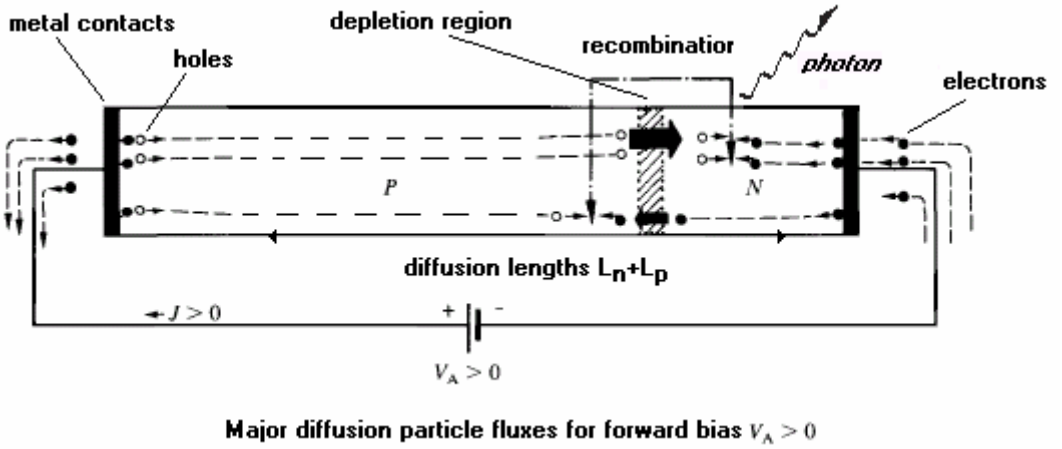


Figure 2-1: Junction diode under forward bias (notice the difference in diffusion lengths).

When the metal contacts are placed to close to the edge of the depletion layer, electrons and holes do not have the ‘space’ to recombine in the silicon. Instead some will recombine at the metal contacts. Metals do not exhibit a band gap, and therefore this recombination event will never produce a photon.

“A forward current is passed through a junction diode leads to energy dissipation in the device. This dissipation appears in two forms. The first is Joule heating (the common Ohmic loss, which is not very large in heavily doped neutral regions), which is phonon excitation in the crystal lattice (lattice vibrations) due to collisions of accelerated charge carriers. The second and more important is dissipation due to recombination of carriers in the neutral regions where diffusion takes place (and in the depletion region). The latter form of dissipation can lead to photon generation: carriers recombine crossing the band gap possibly releasing energy in the form of a photon[34].” Thus not every recombination event in silicon delivers a photon.

The amount of generated photons is very poor for silicon, because silicon is an indirect band gap material. Most group IV semiconductors including germanium (Ge) and silicon carbide (SiC) are indirect band gap semiconductors. Indirect band gap semiconductors do not exclusively have indirect band gaps, figure 2-2[36].

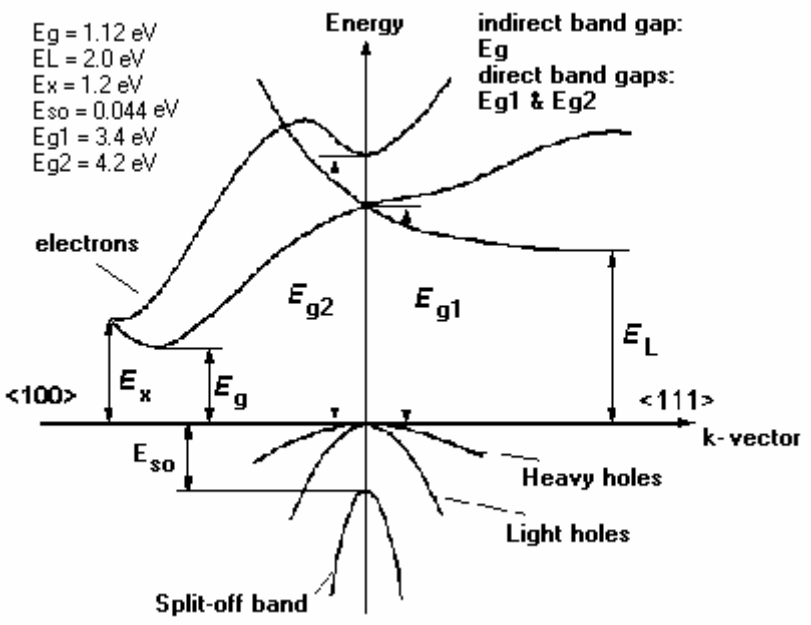


Figure 2-2: Silicon band structure shows indirect band gap.

However "in semiconductor physics, an indirect band gap is a band gap in which the minimum energy in the conduction band is shifted by a k-vector, which is determined by the material's crystal structure. Semiconductors with an indirect band gap are inefficient at emitting light. This is because any electrons present in the conduction band quickly settle into the energy minimum of that band. Electrons in this minimum require some source of momentum allowing them to overcome the offset and fall into the valence band. Photons have very little momentum compared to this energy offset – hence, the momentum "kick" of a photon being emitted would normally not be enough to dislodge the electron from the conduction band. Since the electron cannot rejoin the valence band by radiative recombination, conduction band electrons typically last quite some time before recombining through less efficient means[37]."

An emitted photon is like a bullet leaving a gun. The velocity of the gun being the momentum won't change. A phonon-assisted momentum "kick" could supply the needed k-vector momentum for photon generation. However energy transfer E_{phonon} comes along with the momentum "kick". Setting up a phonon costs energy, while absorption of a phonon results in energy gain. "It is understood that the transition assisted by phonon emission is more probable due to a negligible amount of phonons suitable for absorption at room temperature[18]."

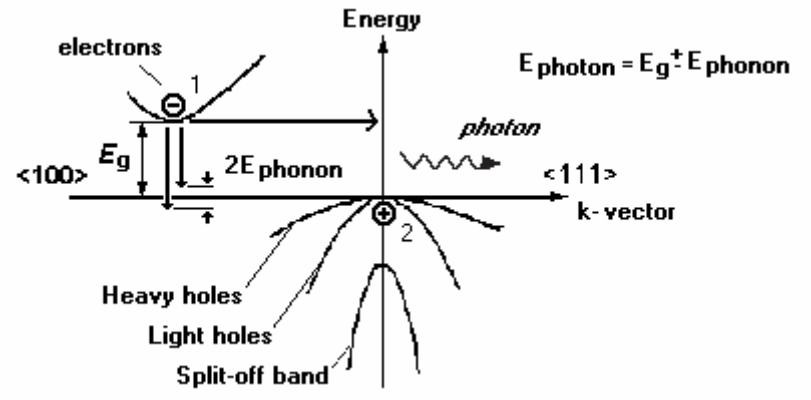


Figure 2-3: Low quantum efficiency and phonon assisted momentum kick.

Both a photon and phonon interaction at the same time is unlikely and hence the (quantum) efficiency of indirect band gap semiconductors will be low[2]. Most of the energy release will not be in the form of a photon. Less efficient means like setting up a phonon dominate. An electron loses bits of energy each time it collides resulting in heat until the electron is no longer excited. An electron that is no longer excited does not have sufficient energy to move free through the material taking part in the conduction. In stead it is a valence electron again possibly taking part in the covalent binding process to keep the material together. The electron recombines with a hole. A hole is an available electron site.

Perfect pure and defect free semiconductors, like semiconductors tabulated in the periodic table of elements, do not permit an electron to reside in the band gap. An electron can only *cross* the band gap when it has energy exceeding the band gap energy. However impurities or defects introduce extra *energy bands* called traps or states, in the band gap.

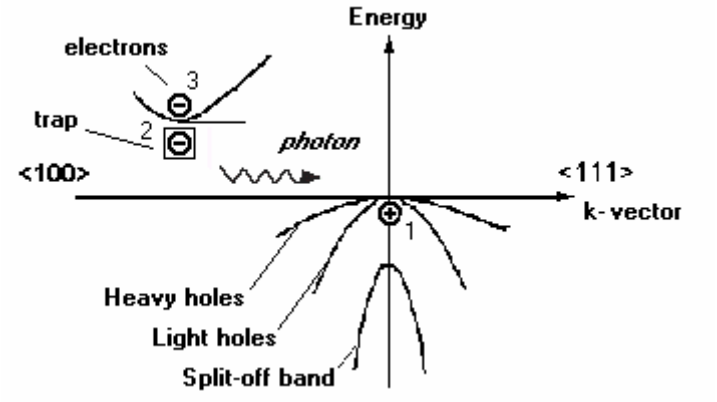


Figure 2-4: Introduction extra energy bands (traps).

Later on we will see that defects called dislocation loops, that are introduced by the implantation process, also introduce energy bands (1D-energy bands). These energy bands help increase the quantum efficiency.

Just as an electron can reside in the valence band or the conduction band, it can also stay in these extra energy bands. An electron does no longer need the band gap energy in order to cross the band gap. It can use these extra energy bands as stepping-stones. Suppose that states are positioned at 1/3 below the conduction band then the largest energy an electron needs is 2/3 of the band gap energy. Therefore the chance that electrons can leave the valence band increases. Both the transition electron band–energy band and energy band–valence band can result in photon emission. Such an emitted photon would result in less energy than the band gap energy! Again phonon and photon action at the same time is required.

2.2 Quantum efficiency

Quantum efficiency is defined as the average number of primary electron hole pairs per incident photon. Primary carriers are generated directly by the incident photon. There is a distinction between the internal quantum efficiency and external quantum efficiency. The internal quantum efficiency is a theoretical value for the average number of *primary* generated carriers per absorbed photon. An electron generated by a photon might have enough energy to generate a second carrier. The internal gain *G* grasps this concept. The external quantum efficiency is the measured value for the number of *primary* generated carriers that are collected at the contacts, per incident photon originating from an external light source. So no internal gain is assumed (G=1). Suppose P_0 is the incident optical power in Watts, and I_{photo} is the resulting photo current at the contacts in Ampère, then external quantum efficiency η is defined as[35]:

[2] Appendix A – Silicon as optical-detector. Despite of the fact that Silicon is regarded fundamentally unsuitable as optical emitter, it is still used as a photo-detector!

Equation [2-1]

$$\eta = \frac{No.\_of\ \_electron\_hole\_pairs\_generated\ \&\ collected}{No\_of\ \_incident\_photons} = \frac{\frac{I_{photo}}{e}}{\frac{P_0}{h\upsilon}}[-]$$

Both carriers and photons are influenced by the material boundaries. For example interface trapping of carriers and reflection of light diminish the external quantum efficiency. In general the external quantum efficiency is lower than the internal quantum efficiency. Methods mentioned in the introduction like *porous silicon, silicon/silicon dioxide super lattices, silicon nano precipitates in silicon dioxide, erbium in silicon, silicon/ germanium and iron disilicide* aim to increase the external quantum efficiency by increasing the internal quantum efficiency. However the external efficiency can also be increased on its own e.g. by process technology like cleaner processes to reduce the amount of surface defects, and proper design[3]. An example of proper design originates from the solar industry. Solar cells are provided with textured surfaces and mirroring metal layers at the backside[9].

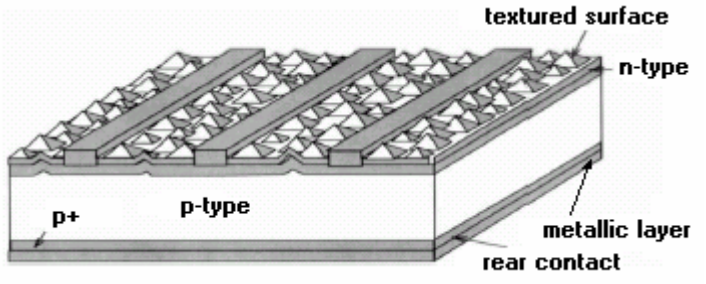


Figure 2-5: Textured surface and mirroring metal layers increase quantum efficiency.

Because carrier recombination or generation and reflection are dependent upon photon energy or wavelength, quantum efficiency is also wavelength dependent.

In articles when quantum efficiency is mentioned it is often the external quantum efficiency. The external quantum efficiency of silicon has been estimated 10^{-6} (about 10^{-4}%)[18] i.e. in the best case scenario 1 million (1,000,000) electrons recombine with as many holes to generate 1 external photon which contributes to the emitted light. Therefore high current values would be required to produce light out of silicon. Conventional LEDs have external efficiencies of 1%, although the internal efficiencies range from 50-80%[35]. Therefore by saying "aim of this project is to develop an efficient silicon **L**ight **E**mitting **D**iode", we mean a silicon LED with high external quantum efficiency in the order of 1%. All quantum efficiencies reported in literature at the moment of writing, concerning "silicon **L**ight **E**mitting **D**iode made by ion implantation", are in the order of 0.1%[1,5,6,7].

As mentioned in the introduction, dislocation engineering is not the only way to increase the external quantum efficiency. However we prefer this method based upon ion implantation.

[3] Thorsten Trupke et. al. even claim "very efficient light emission from bulk crystalline Silicon" [42] by using commercially available float-zone wafers and textured surfaces.

3 Increasing the quantum efficiency by dislocation engineering

In this main section we explain how dislocation loops can be engineered, how dislocation loops look like and how the introduction of these loops in junction diodes should increase the quantum efficiency.

3.1 The implantation process and creating excess interstitials

The ion implantation process creates a lot of damage to the silicon substrate. At the same time an excess of interstitials equal to the implant dose is implanted into the substrate. Let us see how this works.

3.1.1 The silicon substrate as starting material

The **L**ight **E**mitting **D**iodes are formed using a silicon wafer as substrate. How does this silicon substrate look like?

Silicon is a crystalline material, meaning that the atoms form regular atomic arrangements. Regions of regular atomic arrangement are called crystals or grains. Each crystal consists of a Unit cell that periodically repeats itself in all directions. The resulting grid is often called matrix.

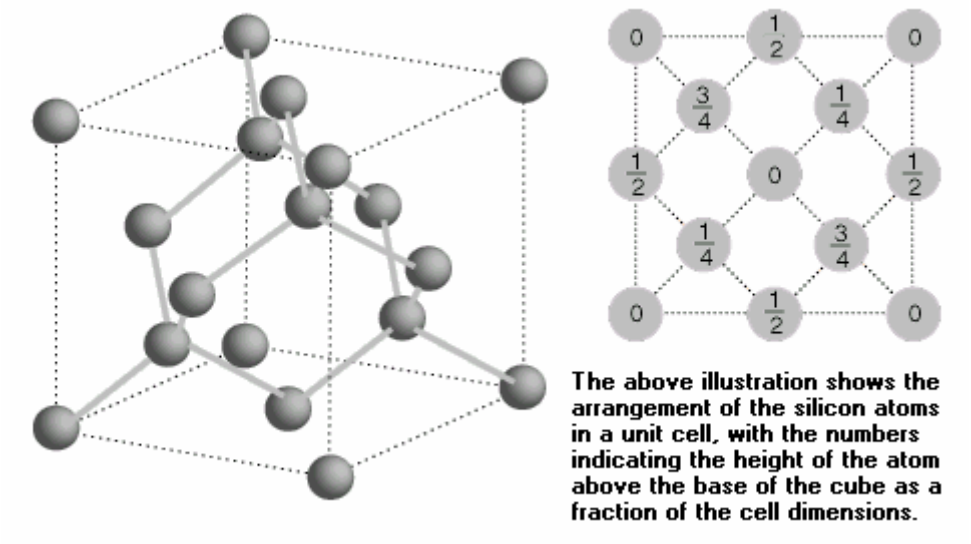


Figure 3-1: Silicon Unit cell and lattice.

The regular atomic arrangement is called lattice. Each atom resides at its lattice site at 0K.

The forces holding the silicon atoms together to form the lattice are covalent or shared electron bonds. Meaning for silicon that individual atoms prefer to bond with their four nearest neighbors. In a single crystal each individual atom is able to bond with its four nearest neighbors due to the regular atomic arrangement.

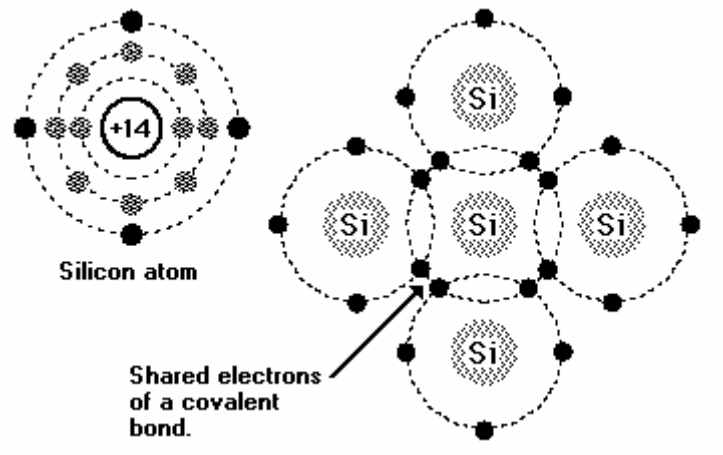


Figure 3-2: Covalent bonding with 4 nearest neighbors.

Single crystalline silicon is used nowadays in the electronics industry i.e. the region of regular atomic arrangement encloses the total wafer. The figure 3-3 depicts how a simple cubic unit cell, repeated itself in all dimensions. To be clear this is not the actual Unit cell of silicon. However such an abstract mental picture can be useful later on to get some feeling for the ion implantation process and how dislocation loops look like.

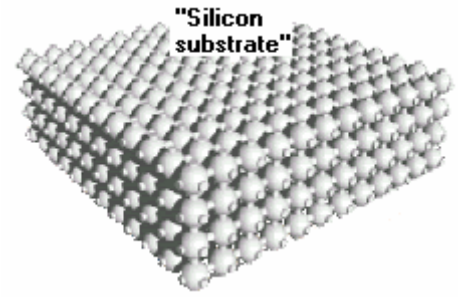


Figure 3-3: Model of silicon substrate.

For example, dislocation loops we will discuss later on are intersected extra planes with a loop shape. A plane is a cross-section in a particular direction and consists of the atoms that lie on that plane.

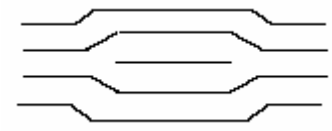


Figure 3-4: Extrinsic dislocation loop revealing inserted extra plane.

The wafer or substrate is single crystalline material. Because the region of regular atomic arrangement encloses the total silicon substrate, boundaries are avoided. In polycrystalline material the individual grains are separated by grain boundaries.

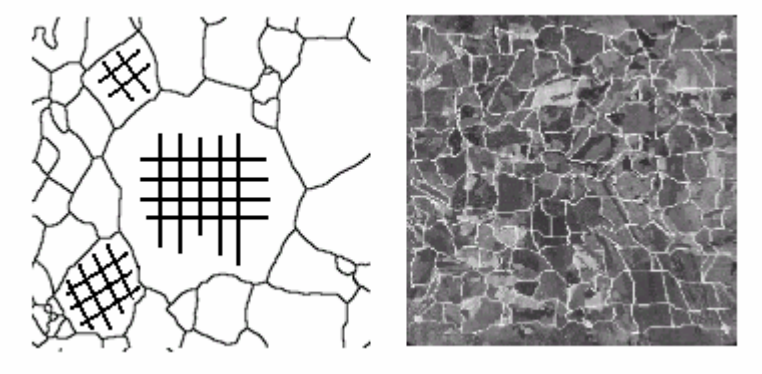


Figure 3-5: Grain boundaries destroy regular atomic arrangement.

Grain boundaries are less densely and regularly packed compared to single crystals. Because the regular atomic arrangement is interrupted at the grain boundaries, not each individual atom is able to bond with its four nearest neighbors. The resulting dangling bonds introduce defects. Those have a significant effect on device properties. By following special procedures single crystals wafers are produced with diameters up to 300mm and a typical thickness of 775μm. From this point in text when we speak of silicon we mean single crystal silicon.

The introduction of dislocation loops also interrupts the regular atomic arrangement. The result is again dangling bonds.

3.1.2 Diode junction formation

As mentioned earlier, an LED is a forwarded junction diode. The junction diode can be introduced into the silicon starting substrate by performing a separate diffusion step. Recall that most of the surface-emitting LEDs have a thin highly doped n-layer on top with a lowly doped p-layer below. In that way generated photons are generated not far from the surface and have a high chance of being ejected from the substrate.

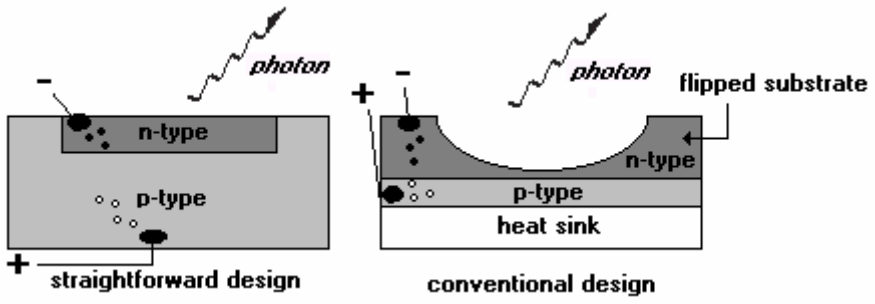


Figure 3-6: N-type silicon on top of p-type silicon.

A straight forward design results in n-type dopant and p-type silicon substrate. However as indicated in the introduction, conventional LED construction must ensure a rapid discharge of heat from the p-n junction, since the light output drops as the junction temperature rises. Therefore in conventional LED design, the silicon substrate is n-type and the dopant is p-type. The n-type substrate is fitted upside down on the heat sink i.e. the substrate is flipped. And finally a hole has been etched away in the substrate at the light output side, so that the light only has to travel through a thin n-type layer[35].

The dopant can also be introduced along with the dislocation loops by ion implantation. However we prefer to separate the introduction of the junction diode and dislocation loops, to not unnecessarily complicate the design process.

3.1.3 The implantation process and damage accumulation

The dislocation loops are introduced into the silicon substrate by ion implantation. The implantation process is not treated in detail, because it is such a common process in IC-processing. Our summary is extracted from reference 33.

The implantation process consists of the acceleration of ions, targeting them at the silicon substrate, and implanting them in it. Channeling occurs often in crystalline silicon.

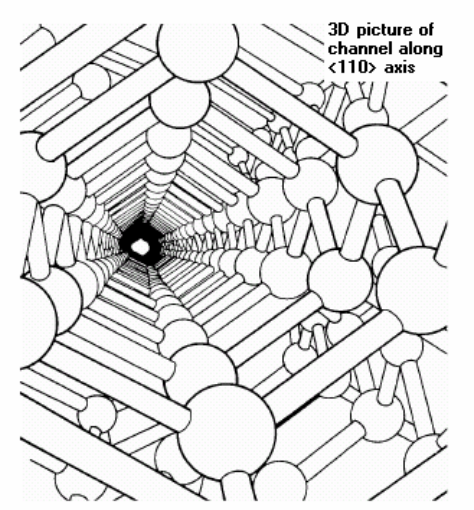


Figure 3-7: Artist impression of channel.

The small-angle scattering events from the atoms that line the walls of the channel results in ions that are steered quite a long distance along the channel before coming to rest from the electronic drag or from a sharp nuclear collision that causes the ion to exit the channel. Due to scattering events each implanted ion follows a random trajectory.

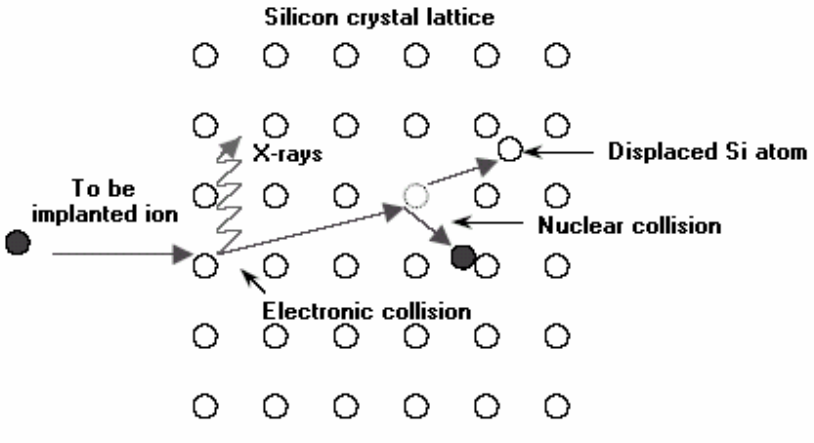


Figure 3-8: Scattering events.

Since the total number of ions implanted is usually greater than $10^{12}cm^{-2}$, the distribution can be described statistically and is often modeled by a symmetric Gaussian distribution. The distribution in projected range is:

Equation [3-1]

$$n(x) = n_p e^{\left(\frac{-(x-R_p)^2}{2(\sigma_p)^2}\right)} [cm^{-2}]$$

R_p is the average projected range normal to the surface, σ_p is the standard deviation about that range, and $n(R_p)$ is the peak concentration where the Gaussian is centered. Besides a distribution in projected range, a distribution in lateral range, called lateral straggle $\sigma_\perp$ exists. However we only concern our self with the distribution in projected range.

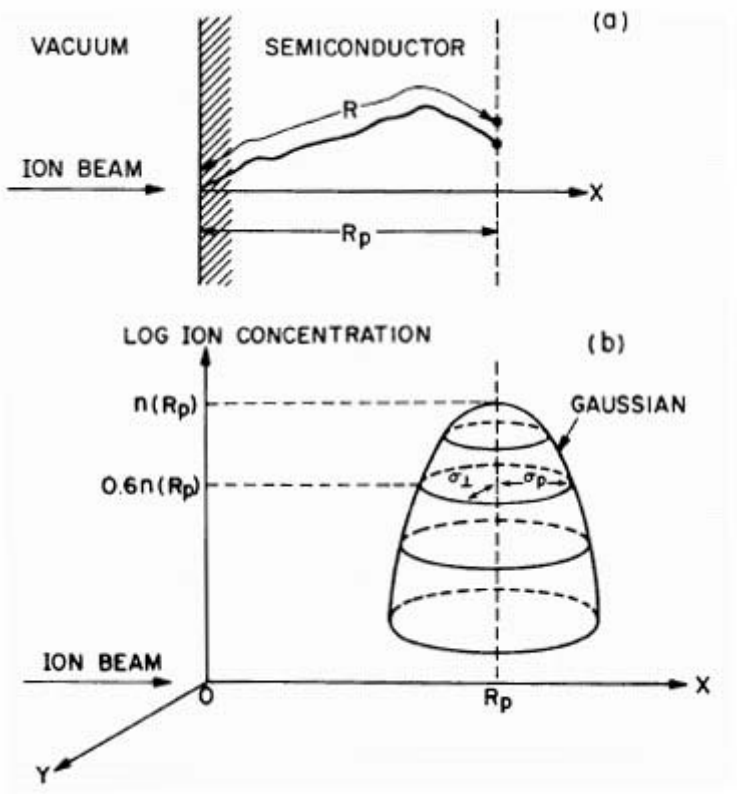


Figure 3-9: Projected range, peak concentration and standard deviation.

Note that the actual distribution profile in projected range can deviate from the Gaussian profile. For example the effect of channeling on the implant profile is to cause a tail that continues much further than expected. Also lighter ions do have the tendency to back scatter of silicon atoms and fill in the front side of the distribution. Therefore less simple models exist taking into account all kind of aspects.

A convenient relationship between dose, peak concentration and standard deviation about that peak concentration, can simply be derived by integrating equation 3-2:

Equation [3-2]

$$Q = \int_{-\infty}^{\infty} n(x)\partial x = \sqrt{2\pi}\sigma_p n_p [cm^{-2}]$$

With known dose and implantation energy, the standard deviation and projected range can be found in look-up tables (Appendix B – look-up table projected range and standard deviation most common dopants in silicon). With help of equation 3-2 the peak concentration can be calculated.

Later on we will see that if the implant concentration is within 10% of the silicon concentration, the silicon is regarded as amorphous. Amorphous material lost all its regular atomic arrangement due to the ion bombardment.

3.1.4 Dose, damage and defect production

The scattering events that an implanted ion encounters can be divided into nuclear collisions and electronic stopping. Sharp nuclear collisions result in displacements of silicon atoms from the lattice sites. An atom or ion that does not reside at a lattice site, whether it is the displaced silicon atom or the implanted ion, is called interstitial. A silicon atom displaced from its own lattice site is called self-interstitial. The vacant lattice site is called vacancy. The lattice positions are such that the free energy is minimized[39].

When an interstitial is injected into the lattice, considerable energy is expended and the lattice becomes strained. Therefore the energy which is required to move the interstitial is low and they can easily migrate to energy sinks. Sinks can include the surface, interfaces or other vacancies or interstitials. Also impurity ions/atoms both in lattice and interstitial positions can act as a sink for lattice defects and can promote defect clustering processes. Interstitial positions are matrix places between lattice sites[39].

If the nuclear collision does not separate the self-interstitial and vacancy for enough, they will immediately recombine again. However when an amount of energy, called the displacement energy is put into the nuclear collision, a stable self-interstitial-vacancy pair is formed. Such a pair is called Frenkel-pair[12].

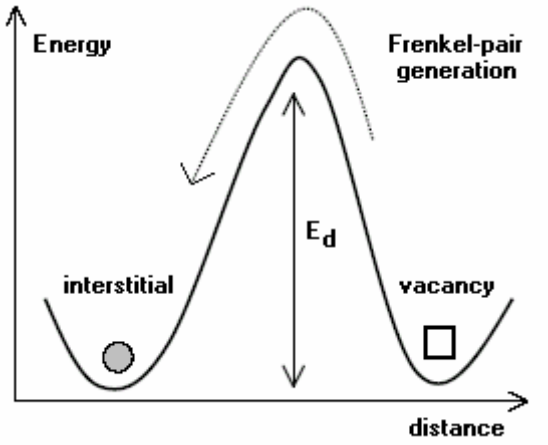


Figure 3-10: Displacement energy and Frenkel-pair generation.

For silicon the displacement energy is approximately 15eV. The implant energy E_n is often in the range of kilo electron volts (1–1000keV), therefore a large number of displacements will be caused. A sequence of displacements is called cascade. An estimate for the number of displaced atoms is given by the Kinchin-Pease-formula[33]:

Equation [3-3]

$$d = \frac{E_n}{2E_d}$$

Thus per implanted ion, depending upon the implantation energy, a large amount of Frenkel-pairs is generated. A large amount of interstitials and vacancies are injected into the matrix. When interstitials or vacancies encounter each other they form clusters. Cluster formation reduces the amount of dangling bonds and is therefore energetically favored. So the resulting lattice defects are primarily small interstitial and vacancy

clusters, dopant-defect complexes and some isolated interstitials and vacancies. The recombination of a vacancy and interstitial restores the lattice-order.

The question now is how this primary damage introduced by 1 implanted ion accumulates when other ions are implanted. Some of the defects generated can recombine with defects from other cascades.

3.1.5 The implantation dose and realization of an amorphous layer

Physically, the dense damage cascades from heavy species like arsenic allow for more efficient recombination than the more dispersed damage distribution from a light ion like boron. Overlapping cascades locally increase the amount of displaced atoms until amorphous pockets arise. If the dose is high enough the primary damage builds up until eventually an amorphous state is reached[33].

Table 3-1: Damage versus implant dose[39].

Dose (cm^{-2})	*Implant conc.*	*Cascade processes*	*Structural effects*
10^{8}	Trace (ppb)	Individual tracks	Discrete defects, stable or mobile
10^{12}	Trace (ppm)	Overlapping tracks	Complex clusters, amorphous zones or extended defects
10^{15}	~1 at. %	Complete overlap (~1dpa)	Dynamic annealing or amorphisation, complex structures
10^{18}	~50 at. %	Composition changes and sputtering	Chemical driving forces: alloying, compound formation and precipitation.

The threshold for amorphous layer production is the total vacancy concentration above which the substrate is assumed to be amorphous. It is expressed as a percentage of the silicon atom concentration[33]. The silicon atom concentration is 5 $10^{22}cm^{-3}$. Usually this threshold is assumed to be 10%. Remember from figure 3-9 that the peak concentration n_p exceeds this threshold first.

3.1.6 Amorphous layer evolution dependence upon ion mass and implant energy

Whether an amorphous layer is formed is almost exclusively dictated by the implant dose. However the subsequent evolution of the amorphous layer depends upon the implanted atom/ion mass and implantation energy.

For heavy ions like arsenic, whose stopping may be dominated by nuclear collisions, the damage profile is relatively flat over the whole projected range up to R_p i.e. from surface to projected range atoms have been displaced. Lighter ions like boron have an appreciable component of electronic stopping at higher energies. Electronic stopping does not result in displacement of atoms. Therefore the damage accumulation is concentrated near R_p i.e. atoms are only displaced near R_p. For lighter ions then, the amorphous region will form first at the peak of the damage density profile near R_p and expand on both sides of this depth as the implant dose is increased. A buried amorphous layer first forms, and it may take a considerably higher implant dose before a continuous amorphous layer extending down from the surface forms (surface amorphous layer)[33].

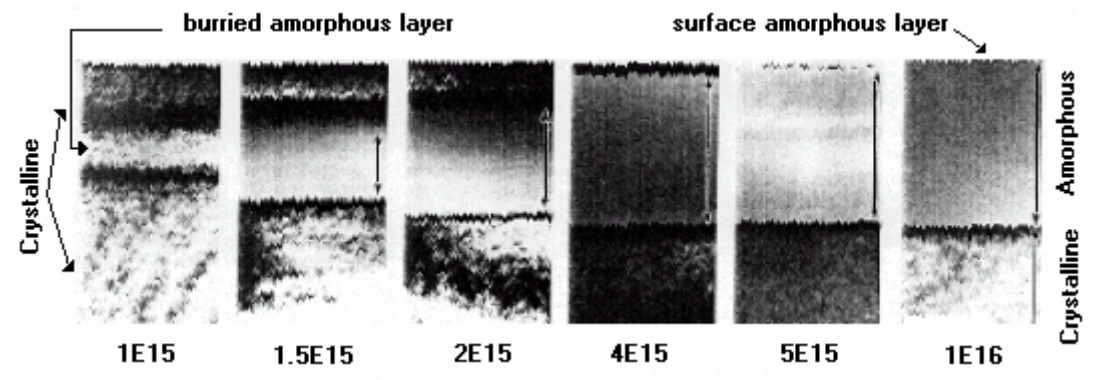


Figure 3-11: Evolution of amorphous layer.

In general simply up scaling up a low-dose implant does not give the same profile as a high-dose implant. As the crystal is damaged by the implanted ions, channels are less evident to subsequent incoming ions. Relatively speaking, higher implanted doses are less prone to channeling effects. Producing an amorphous layer before the actual ion implantation, called pre-amorphization, eliminates the effect of channeling[33].

It is also worth mentioning that it is easier to form an amorphous layer at low temperatures (liquid nitrogen) rather than at room temperature or higher. This observation is easily explained by the larger fraction of ions that recombine within a cascade at higher implant temperatures. If the implant is performed at liquid nitrogen temperatures rather than room temperature, a lower implant dose can be used to form the same amorphous layer. Because of this, the amount or dose of damage in the tail of the damage distribution beyond the a/c interface is much less for the liquid nitrogen temperature implant. Also the a/c interface is sharper[33].

3.2 The implantation dose and nucleation of dominant defects

During the ion implantation, various levels of damage can be done to the lattice. The resulting defects depend almost entirely upon the implantation dose (implantation energy 40–200keV)[21]. For silicon implants in silicon these levels of damage can be divided into five regimes:

Table 3-2: Damage regimes versus implant dose.

	Implanted silicon dose [cm^{-2}]		amorphous implant	Depth of defect formation	Defect
A	$<5\times10^{12}$	1×10^{11}–2×10^{13}	No	–	Nanometer-size Interstitial clusters
B	5×10^{12}–1×10^{14}	2×10^{13}–1×10^{14}	No	–	**I**ntermediate **D**efect **C**onfigurations = rod-like defects and {113} stacking faults
C	2×10^{14}–1×10^{15}		No	Projected range R_p	Category I: **I**ntermediate **D**efect **C**onfigurations, Frank stacking faults and perfect prismatic dislocation loops
D	$>1\times10^{15}$		Yes	End of Range (EOR) region	Category II: **I**ntermediate **D**efect **C**onfigurations, Faulted loops and perfect prismatic dislocation loops
E	$>2\times10^{15}$		Yes	–	Dislocation networks

(a) "At silicon implantation doses below $5\times10^{12}cm^{-2}$, no {113} defects are observed. This could indicate that the interstitial clusters formed from the implantation damage, are too small to be detected by **T**ransmission **E**lectron **M**icroscopy. Alternatively, this threshold dose could reflect a nucleation barrier for the formation and growth of {311} defects[40]". "Recently, Crowern and co-workers have been able to extract information on I-cluster dissociation by monitoring its effect on TED[10]" "Ultra fast TED occurs at relatively low temperature

(700°C) and for times from 15s up to 40 minutes after low-dose implants (1×10^{11}–2×10^{13} Si/cm^2)[10]". Also, "tight-binding calculations of I-agglomeration revealed that the structure of an I-cluster alternative to the {311} defect structure may exist when few interstitials agglomerate. The formation energy per I is lower than that necessary for the formation of the (110) chain, which is the building block of the {311} defect, when the number of interstitials is lower than 10.[10]"

(b) The point defects left over after recombination of vacancies and interstitials will be dominantly interstitial clusters. The point defects coalescence into what has been termed **I**ntermediate **D**efect **C**onfigurations (**IDCs**). They include rod like defects as well as {113} stacking faults (also called {311} rod-like defects)[2].

"For doses in between 5×10^{12} and 1×10^{14}cm^{-2}, {311} defects are the only visible defects[40]". After using both **D**eep **L**evel **T**ransient **S**pectroscopy (DLTS) measurements and **P**hoto**l**uminescence (PL), Libertino points out "the strong reduction in the defect concentration at 5×10^{13}cm^{-2}, about one order of magnitude, can be attributed to the formation of extended {311} defects, obtained at fluences above 2×10^{13}cm^{-2}…[10]".

Intermediate **D**efect **C**onfigurations are part of category I damage, but not exclusively. Category 1 damage forms when the implantation damage is insufficient to produce an amorphous layer. Like the name "intermediate" suggest, these defects might transform into more stable defects e.g. extrinsic Frank stacking faults loops and perfect prismatic dislocation loops, if the implant dose and subsequent thermal budget is right. The interstitials left over after high temperature anneals, will coalescence into loops. These loops are extra planes consisting of self-interstitials.

"Extended defects or dislocation loops will result if the dose or peak concentration is above a critical concentration. For doses below 2×10^{14}cm^{-2} no dislocation loops were observed. This corresponds to a critical peak concentration of ~1.6×10^{19}cm^{-3}. This critical concentration is independent of the species and wafer orientation[2]". The category 1 defects form at the projected range R_p.

This critical peak concentration is related to the (electrical) solid solubility of silicon. Implanted ions are not yet part of the crystal structure. Annealing provides energy to bond with 4 silicon atoms in the re-crystallizing structure, thereby occupying a lattice site. The implanted ion is said to become electrically active. At the same time a self-interstitial is created giving up its lattice site. At some depth like the projected range or later on discussed end-of-range region, the concentration of implanted ions first exceeds the electrical solid solubility. The electrical solid solubility reflects the amount of foreign atoms that can be incorporated on lattice sites by ejecting a self-interstitial. When the electrical solid solubility is exceeded implanted ions start to occupy interstitial sites i.e. matrix space between lattice sites, and start forming neutral clusters. When even the solid solubility is exceeded a separate phase is formed e.g. an extra plane. The extra planes provide new available space in the form of (lattice) sites. The self-interstitials created by ion implantation gather to occupy these extra planes. These extra planes often have the shape of *loops*[33].

(c) A typical category I dose regime for silicon implants is 2×10^{14}–1×10^{15}cm^{-2}. Above a threshold dose of 2×10^{14}cm^{-2}, {113} defects break up[22]. After dissolution of {113} defects an excess of interstitials provide the formation of extrinsic Frank stacking fault loops (also called Frank loops or faulted loops) and perfect prismatic dislocations loops (often called perfect loops). Since these dislocations are more stable than {113} defects, significantly stronger annealing steps are needed to fully dissolve this dislocation damage.

It is not possible to produce category I extended defects by room temperature or lower temperature for implantation with heavier ions such as arsenic. Category I damage forms when the implantation damage is insufficient to produce an amorphous layer. The production of an amorphous layer takes place at an implant dose of 5×10^{13}cm^{-2} for implants with implantation energy below 200keV. So an amorphous layer forms first and therefore category II defects, that forms when the damage is sufficient to produce an amorphous layer, is produced prior to exceeding the critical peak concentration necessary for category 1 defect formation[2].

Figure 3-12[3] depicts the dependence of category I damage and category II damage upon ion mass. 92.23 Percent of silicon found in nature has an ion mass of 28 and 100% of arsenic found in nature has an ion mass of 75.

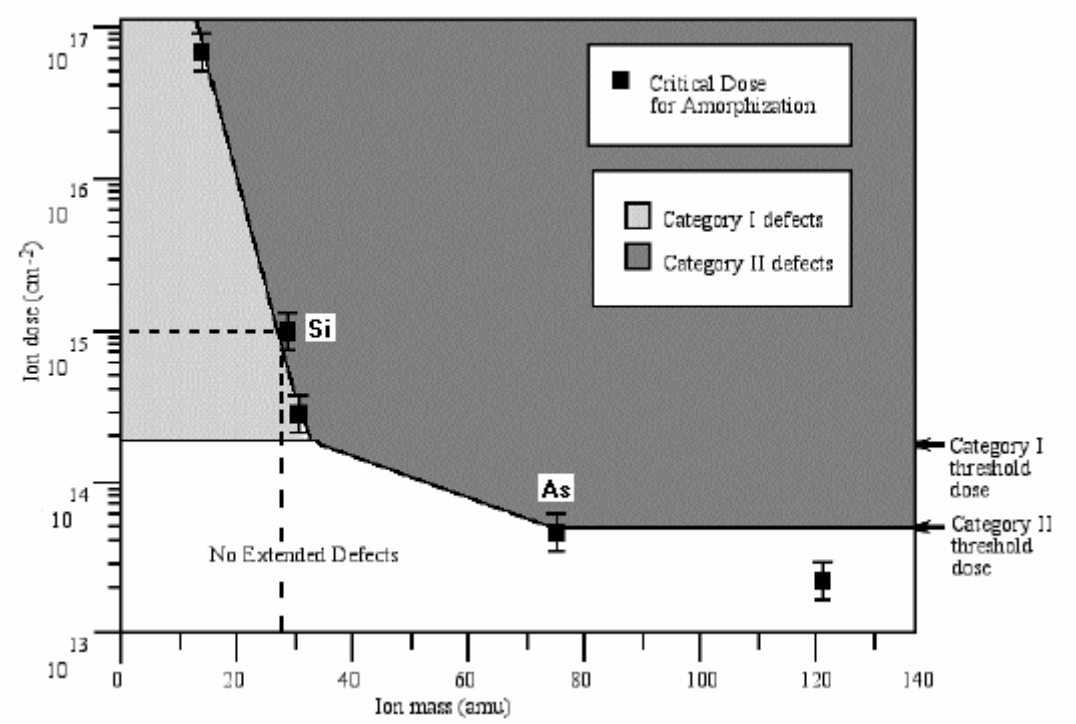


Figure 3-12: Category I and II damage for varying ion mass and implant dose.

(d) For silicon the implantation dose should exceed $1\times10^{15}cm^{-2}$ to produce category II defects[22]. Category II damage forms when the implantation damage is sufficient to produce an amorphous layer.

Let us start with an example that illustrates the influence of the proximity of the surface upon category II defects nucleation.

IMEL-NCSR "demokritos"[15] reports in her Bi-annual report 2001-2002 that the proximity of the silicon surface to the dislocation loop band (on the order of 5 nm), causes the dissolution of category II defects even from the early stage of the oxidation process. Extended defects were absent after dry oxidation of nitrogen implanted silicon (3keV, $1\times10^{15}cm^{-2}$) at 800°C for 60 minutes.

All defects, whether it are {311} rod-like defects, Frank stacking faults or perfect loops, consist of interstitials due to the nature of the implantation process. The surface loss of interstitials is too high when the surface is to close to the defect region. Consequently defects dissolve before they nucleate. We assume that surface loss is negligible.

The implantation process gives rise to large amounts of displaced atoms or interstitials, even after recombination of interstitials and vacancies. As has been mentioned briefly, interstitials can easily move to energy sinks for example an interface. After producing an amorphous layer, the amorphous-crystalline interface forms such an energy sink. Consequently after producing an amorphous layer there is a region, super saturated with interstitials or becomes so upon annealing, just beyond the amorphous-crystalline (a/c) interface: the **E**nd-**O**f-**R**ange (**EOR**) region, figure 3-12[21].

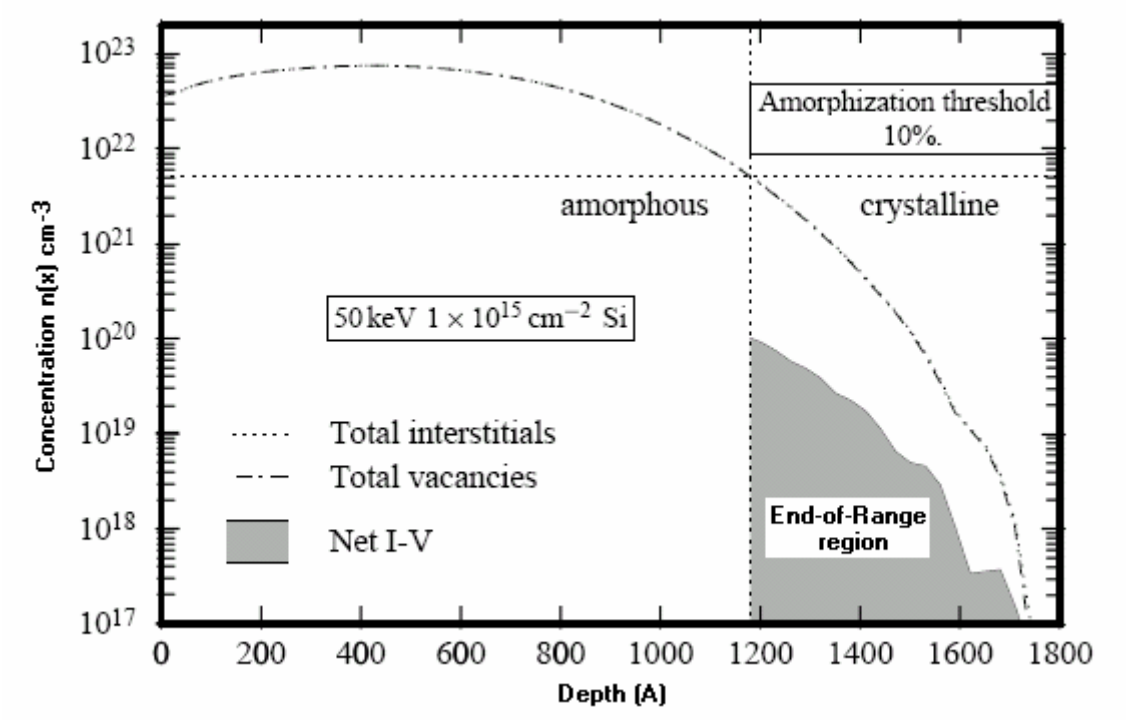


Figure 3-13: End-of-range region and depth of a/c interface.

"The area under the damage density distribution beyond the a/c interface does not increase with higher dose due to the increase in thickness of the amorphous layer with dose[2]".

Due to the presence of large amounts of interstitials in this region it becomes stretched. However the **S**olid **P**hase **E**pitaxy (**SPE**) re-grown silicon is not stretched. Therefore, high stress exists at the amorphous-crystalline interface. To relieve stress, interstitials just beyond the amorphous-crystalline interface form dislocation loops[2].

Upon annealing, type II (end of range) dislocation loops e.g. faulted or perfect are observed to form. The formation of extrinsic dislocation loops in the category 2 region is energetically favorable to the formation of a large cluster of interstitials like {113} stacking faults. The reduction in strain energy associated with the formation of an extra plane is larger. The evolution of category 2 damage from point defects to extrinsic dislocation loops during annealing, is believed to occur via intermediate defect configurations such as {113} stacking faults[2].

Thus, once again, due to the stress, clusters like {113} stacking faults, are less preferred than category II loops. Remember that category I loops form in the absence of an amorphous layer and resulting stress. Therefore the ratio {113} stacking faults to category I loops will be lower than the ratio {113} stacking faults to category II loops.

(e) if the concentration of atoms bound by the extrinsic dislocation loops exceeds the concentration of atoms in a mono layer of the {111} plane of silicon (~1.4×10^{15}cm^{-2}), then dislocation network formation becomes possible upon annealing via dislocation-dislocation interaction[2].

After dissolution of {113} defects an excess of interstitials provide the formation of Frank- and perfect loops. However, some of these interstitials diffuse into the bulk or surface. Therefore the dose necessary for dislocation network formation has been estimated 2×10^{15}cm^{-2} which is higher than ~1.4×10^{15}cm^{-2}.

In the dose regime above 1.4×10^{15}cm^{-2} some remarkable aspects concerning the roll of pre-amorphization have been mentioned. First of all Jones et. al.[2] carried out the following experiment:

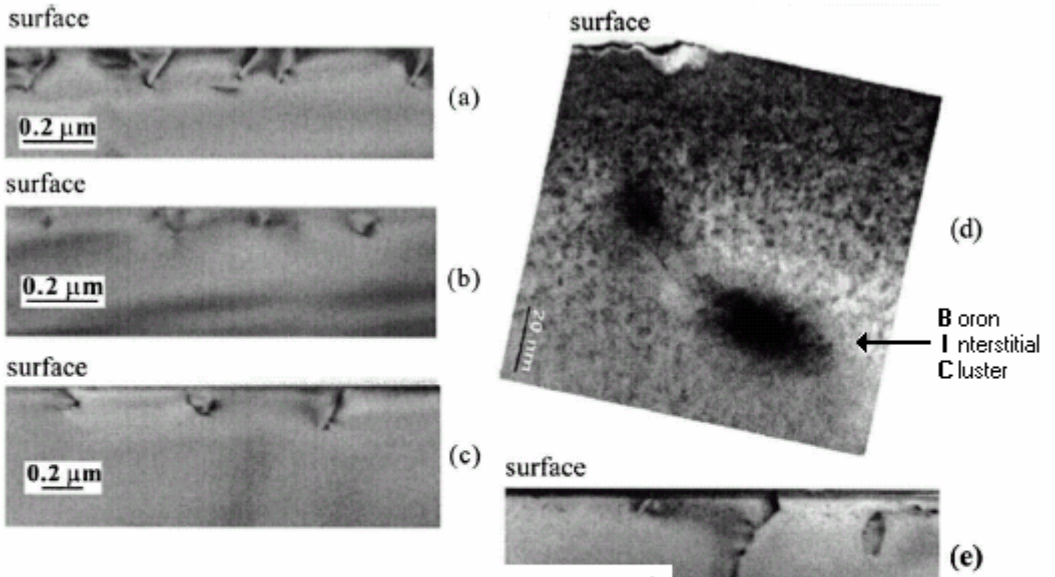
Table 3-3: Roll of pre-amorphization from Jones experiment.

Jones Experiment	Pre-amorphization implant		Implant	
	Energy	Dose	Energy	Dose
	E	Q	E	Q
Sample	keV	cm^{-2}	keV	cm^{-2}
1	–	–	50	1×10^{16}
2	70	5×10^{15}	30	5×10^{15}
3	30	5×10^{15}	70	5×10^{15}

After re-growth of the amorphous layer at 550°C, the samples were annealed at 900°C for 16h. When compared with sample 1, the concentration of atoms bound by the dislocation loops is observed to be smaller for sample 2. However the concentration of atoms bound by the dislocation loops is observed to be larger for sample 3.

Thus a low energy pre-amorphization implant followed by a higher energy implant introducing the same dose as a single implant, results in a larger concentration of atoms bound by the dislocation loops.

An interesting situation exists when a pre-amorphization implant with silicon atoms is followed by a high dose boron implant. At boron implants exceeding $1\times10^{16}cm^{-2}$, the boron concentration reaches the thermal equilibrium solubility limit ($1.53\times10^{20}cm^{-3}$) at 1050°C[14]. Hence the boron clusters can not be dissolved during the long time anneal. "Observations by Cowern *et al.* [9, 10], suggest that in systems where B is present in large doses, excess interstitials help boron atoms to form boron clusters and are themselves incorporated into these clusters (so-called **B**oron **I**nterstitial **C**lusters, **BICs**)[21]". Sun *et al.* suspect that the dark spots depicted in figure 3-14[14] are the BICs, however they were not able to prove it. The origin of the contrast of these dark spots is attributed to high strain in an area of locally high density of Si-B interstitial clusters, Si interstitials, or it is induced by the strain field around extended defects (like dislocation loops)[14].



XTEM images of the silicon *pn* diodes prepared by B^+ implantation at 25 keV with different doses of 2.0×10^{13} (a), 1.0×10^{15} (b), 4.0×10^{15} (c), and 1×10^{16} cm^{-2} (e). The extended defects in image (a) of the reference sample are produced by preamorphization via Si^+ implantation at 50 keV with a dose of 1.5×10^{15} cm^{-2}. (d) is a close-up view of strained clusters formed at the end of an extended defect taken from the same sample as in (c). All analyzed samples were annealed at 1050 °C for 20 minutes.

Figure 3-14: Boron interstitial clusters?

Later on more about how the introduced dislocation loops and “doping spikes” help increasing the quantum efficiency. Because increasing the quantum efficiency is what we try to achieve. For now we can mention that both dislocation loops and doping spikes act as blocking potential, thereby hindering the motion of carriers across the junction, figure 3-15[14].

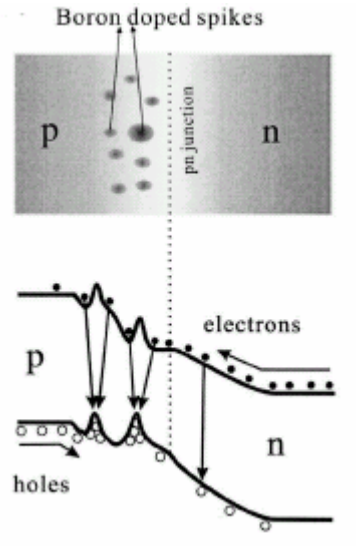


Figure 3-15: Boron interstitial clusters act as transition barrier for carriers.

The carriers are confined to the region where the blocking potentials are situated.

We chose to introduce the dopant and dislocation loops in 2 separate steps. Dislocation loops are introduced by silicon ion implantation after the junction has already been formed by in diffusing. Advantage is better control, however the disadvantage is the lack of “doping spikes” that help block the carriers and consequently improve the quantum efficiency.

3.3 Annealing and evolution of dominant defects

The right dose provides the nucleation of different types of defects during annealing. The evolution of these defect nuclei depends on the thermal budget. Annealing takes place in an inert ambient unless stated otherwise.

The evolution of both category I and category II damage from point defects to respectively category I and category II loops upon annealing, is believed to occur via intermediate defect configurations such as {113} stacking faults. The implant damage is removed during a typical re-crystallization temperature of 550°C.

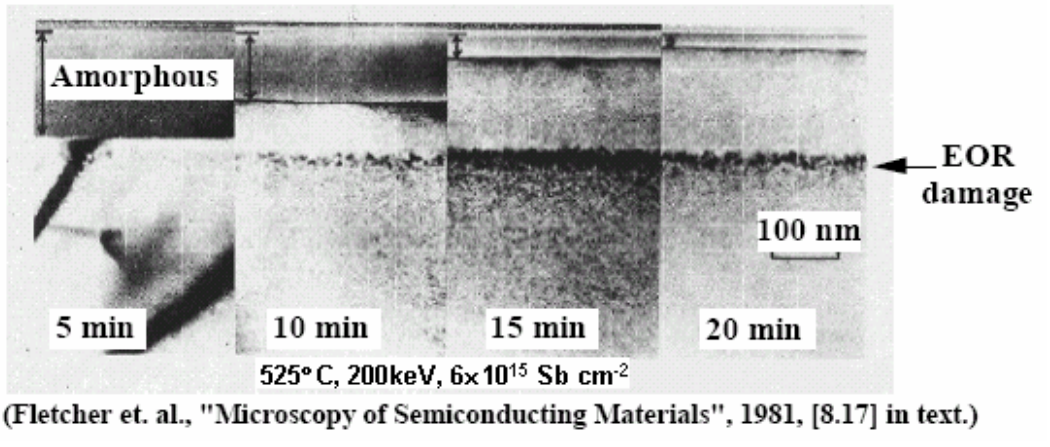


Figure 3-16: Solid phase epitaxy re-growth of silicon (notice EOR damage remains).

What remains is the category I *or* category II damage. For different thermal budgets, different defects will evolve. Eventually for sufficient high thermal budgets all defects dissolve.

Table 3-4: Regimes during thermal annealing.

Annealing Temperature	regime		{311} Rod-like defect and loop activity
°C	{311} Rod-like	loops	
<700	Growth	Growth	{311} Rod-like defects nucleate and grow by capturing interstitials. {311} defects form the nuclei of perfect loops.
700–800	Dissolution	Growth	{311] Rod-like defects dissolve by releasing interstitials. Perfect loops continue to grow by capturing interstitials. Frank loops nucleate and start growing.
800–900	–	Coarsening	Both perfect loops and Frank loops enter Oswald rippening process: average loop radius increases while average loop density decreases. The total amount of interstitials bound by the loops stays almost constant
900–1000	–	Coarsening/ Dissolution	Oswald rippening process continuous and at the same time some loops dissolve by releasing interstitials. The total amount of interstitials bound by the loops decreases.
>1000	–	Dissolution	All loops dissolve by releasing interstitials.

The first defects that start evolving (besides the nanometer-sized Interstitial clusters) are the {311] defects. It is shown that {311} rod-like defects have three stages of micro-structural evolution[3]:

- Accumulation of point defects to form circular interstitial clusters;
- Growth of these circular clusters along the <110> direction;
- Dissolution into the silicon matrix.

Intermediate **D**efect **C**onfigurations were estimated to be ~20A^2. {311} Defects start breaking up for temperatures over 700°C i.e. they dissolve into the silicon matrix. During this dissolution process interstitials are gradually lost from the damage region through diffusion into the bulk and to the surface, the latter most likely being the dominant loss mechanism. The rate at which this decay occurs is determined by the average binding energy of interstitials at {311} defects (1.3eV), the proximity of the surface, and the initial interstitial concentration as it is set by the implant dose.

The dissolution of {113} defects provides an excess of interstitials that allows the formation of category I *or* category II loops, depending on the exact implant dose. Dislocation loops nucleate, upon annealing, from primary defects residing in the crystalline silicon near the amorphous/ crystalline interface. A certain critical dose (2×10^{14}cm^{-2}) must be used in order to form stable loops [24]. Otherwise dislocations cannot exceed critical dimensions for stable growth due to lack of point defects from the implant. In this case, unstable loops nucleate but dissolve upon annealing[19]. For a thermodynamic explanation of dislocation nucleation, the reader is referred to the model proposed by Tan[30].

For the following information we should point out to references 22, 23 or 25, unless stated other wise.

For the 2×10^{14}cm^{-2} dose, which is below the amorphization threshold, the dominant defect at 700°C is the {311} defect with a much smaller concentration of type I loops. The total trapped interstitial concentration was around 7×10^{13}cm^{-2} for 700°C 1 hour anneals. The formation of category I loops does not result in complete trapping of interstitials released by {311} defects. The {311} defects begin dissolving after several hours at 700°C. The type I loops show some growth during the {311} dissolution. The ratio total amount of interstitials: {311} defect: type I loops is 6:4:2. Thus quantitatively less than half of the released interstitials appear to be trapped by the type I loops.

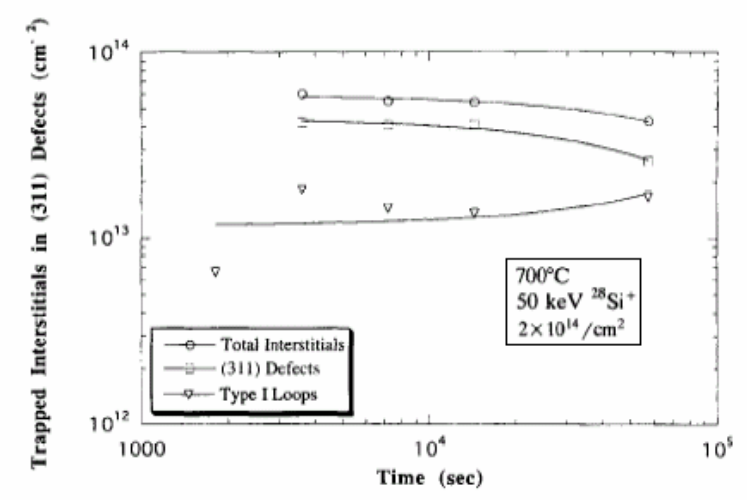


Figure 3-17: Ratio {113} defects to category I loops (2:1).

For the $1\times10^{15}cm^{-2}$ sample amorphization occurs and both type II (end of range) loops i.e. extrinsic Frank stacking fault and perfect prismatic loops, and {311} defects are observed for 700°C anneals. The total number of trapped interstitials for 700°C 1 hour anneals is also around $7\times10^{13}cm^{-2}$. The ratio, total amount of interstitials: {311} defect: type II loops is 7:2:5. Thus the ratio of {311} defects to loops has switched such that the dominant defect is the type II loop. Upon annealing, the {311} defects again show a reduced dissolution rate and the type II loops are in the growth regime. Increasing the anneal temperature to 800°C results in further growth of the type II loops and all of the {311} defects have either dissolved or unfaulted.

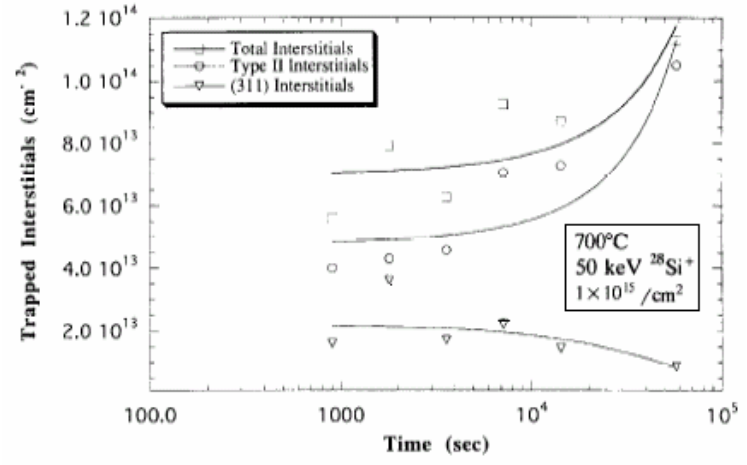


Figure 3-18: Ratio {113} defects to category II loops (2:5).

The light emission has been assigned to the category I and category II loops. The total amount of trapped interstitials is for both category I and category II loops the same. However the ratio {113} defects to category I loops (2:1) is much smaller than the ratio {113} defects to category II loops (2:5). Or in other words, a higher percentage of the implant dose directly results in loops for an amorphous implant. At 800°C most {311} defects dissolved. During their dissolution the injected interstitials provide the nucleation and growth of Frank loops and further growth of perfect loops. However interstitials are lost during the dissolution process. These interstitials don't end up in loops. For amorphous implants a higher percentage of the implant dose directly results in loops, and these interstitials can't get lost during {311} dissolution. Therefore from this point in text we examine category II loops.

According to the +1 model, the amount of introduced extra interstitials equals the implant dose. However interstitials are lost from the damage region during {311} cluster formation and loop formation through diffusion into the bulk and to the surface.

Figure 3-19[2] depicts the amount of interstitials bounded by the category II loops as function of the implant dose. In is interesting to see that the amount of atoms bound by the dislocation loops is larger for heavier implant species.

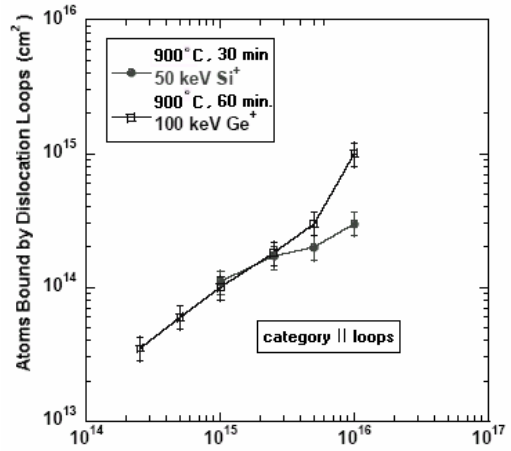
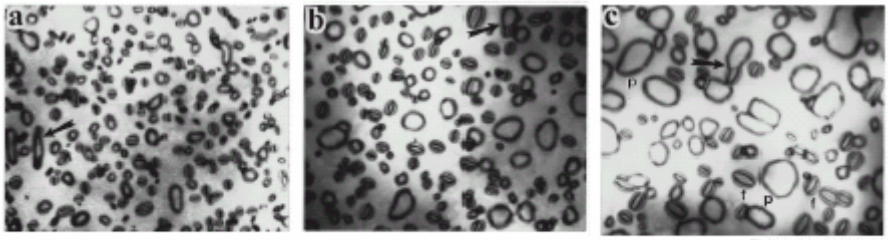


Figure 3-19: Bound interstitials versus implant dose (increase for heavier species).

During annealing, a coarsening process known as Ostwald ripening takes place, resulting in the growth of large loops at the expense of smaller ones, figure 3-20.



TEM symmetrical bright-field images of Si-implanted silicon taken along the [001] Si direction show the ripening growth of extrinsic dislocation loops after furnace annealed at 850 °C for (a) 5, (b) 60, and (c) 960 min.

Figure 3-20: Oswald rippening process (f= Frank loop, p= perfect loop).

Therefore during the Oswald rippening process, the total amount of interstitials bounded or trapped by the loops remains almost constant. Bonafos et al. give a thorough analysis of this process[31].

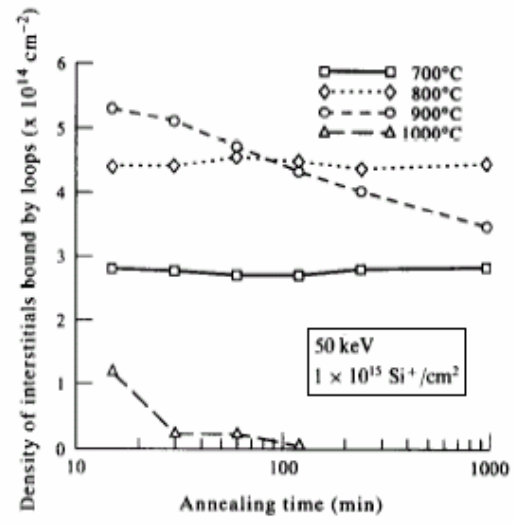


Figure 3-21: Density of interstitials bound by category II loops (constant during coarsening regime).

The loop growth rate is approximately constant for each annealing temperature (700−1000°C).

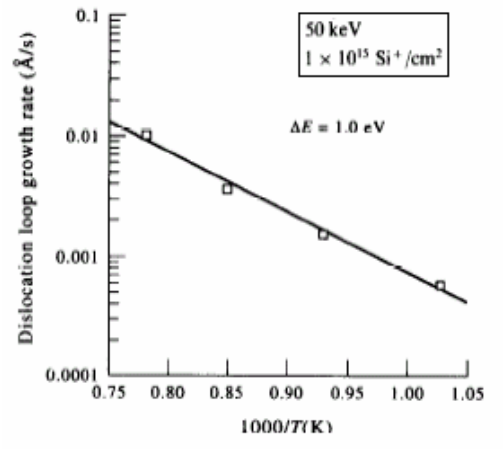


Figure 3-22: Category II loop growth rate (almost constant versus temperature).

The loop growth is governed by the bulk-diffusion mechanism. According to bulk diffusion mechanism, the radii of growing loops are proportional to the annealing time. This implies an uniformly increasing average loop radii. In addition, the loop growth rates increase with the increase of annealing temperature. At lower temperatures (700°C, 800°C) this growth appears to be much slower than that at high temperatures (900°C, 1000°C). The average loop radius for 1000°C anneal is much larger than that of the other temperatures. In general, secondary defects become large enough to observe via transmission electron microscopy (TEM) during post implantation annealing at temperatures exceeding 700°C.

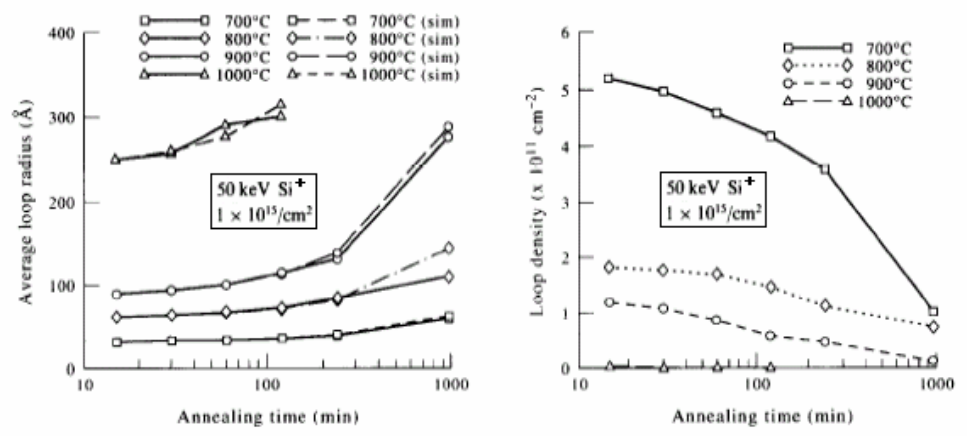


Figure 3-23: Loop radius increases and loop density decreases during Oswald rippening.

In the mean time the total loop density is decreasing (larger loops grow at the expense of smaller loops) which makes the density of interstitial bound by the loops stay constant for low temperature annealing and decrease after annealing at high temperatures (i.e. ≥900°C). For 700°C and 800°C annealing, the loops remain in the coarsening regime (for annealing times up to 16 hours) and the density of the interstitials bound by the loops is constant during the annealing process. For 900°C annealing, after 30 minutes the interstitial density decreases and the loops change from the coarsening regime to the dissolution regime. After only 15 minutes annealing at 1000°C, the loop dissolution process starts and the interstitial density reaches a very small value (< 3×10^{12}cm^{-2}) after 2 hours. For annealing times greater than 2 hours at 1000°C, very few loops remain and they evolve into stacking faults.

“The stress is found to be strongly sensitive to the size and distribution of the loops. It has been researched that the change in the magnitude of this strain with time is negligible for the low temperature anneals (<900°C). However, at higher temperatures (1000°C) there is a sharp drop in magnitude for long anneals.

It appears that the magnitude of the strain is sensitive only to the anneal temperature for temperatures below 900°C. At elevated temperatures (>900°C), it is a strong function of both the annealing time and temperature"[18].

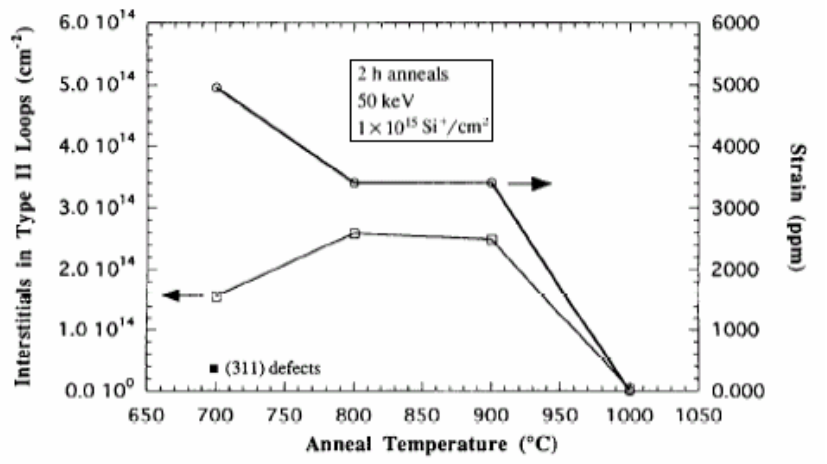


Figure 3-24: Strain almost constant during Oswald rippening (decrease during dissolution).

Pan et. al. divides the category II loops into Frank loops and perfect to show both density and mean loop radius of both type of loops.

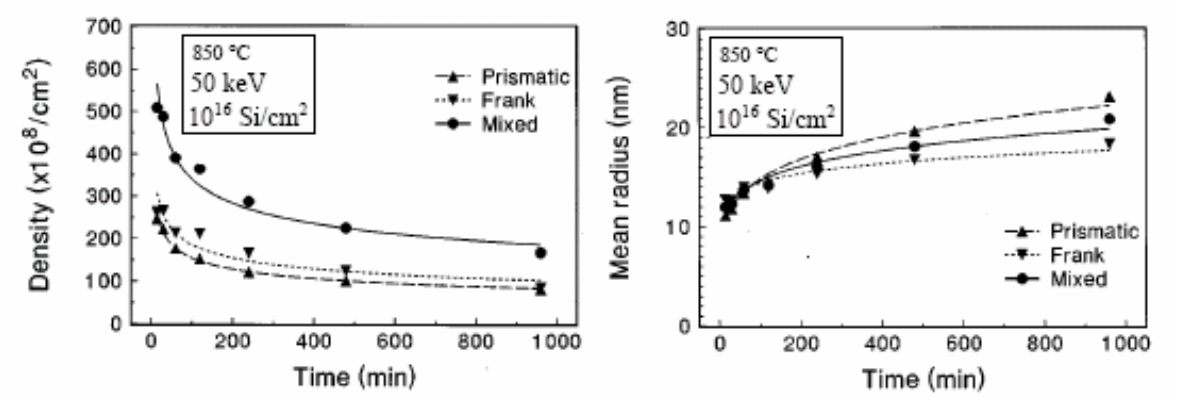


Figure 3-25: Frank curves follow perfect loop curves (evidence of no unfaulting of Frank loops).

Both dislocation loops grow simultaneously with anneal time. In addition, the density-time curve for the Frank loops closely follows the density and mean radius curves for the prismatic loops. This suggests that the increase of interstitials for prismatic loops and the decrease of interstitials for Frank loops with annealing time is a preferred ripening of prismatic loops rather than an unfaulting effect of Frank loops.

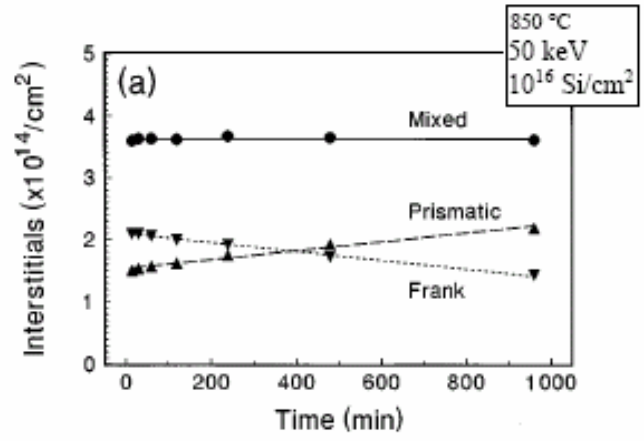


Figure 3-26: Domination Frank loop (less strain energy) and perfect loop (preferred rippening).

In addition Pan et. al reveal the damage distribution profiles of both Frank loops and perfect loops.

"A study of **E**nd-**O**f-**R**ange (**EOR**) dislocation loops in silicon implanted with 50keV $1\times10^{16}cm^{-2}$ was carried out by using transmission electron microscopy. The size distribution profile of faulted Frank dislocation loops could be well fitted by a normal Gaussian probability function and that of perfect prismatic dislocation loops by a log-normal Gaussian probability function"

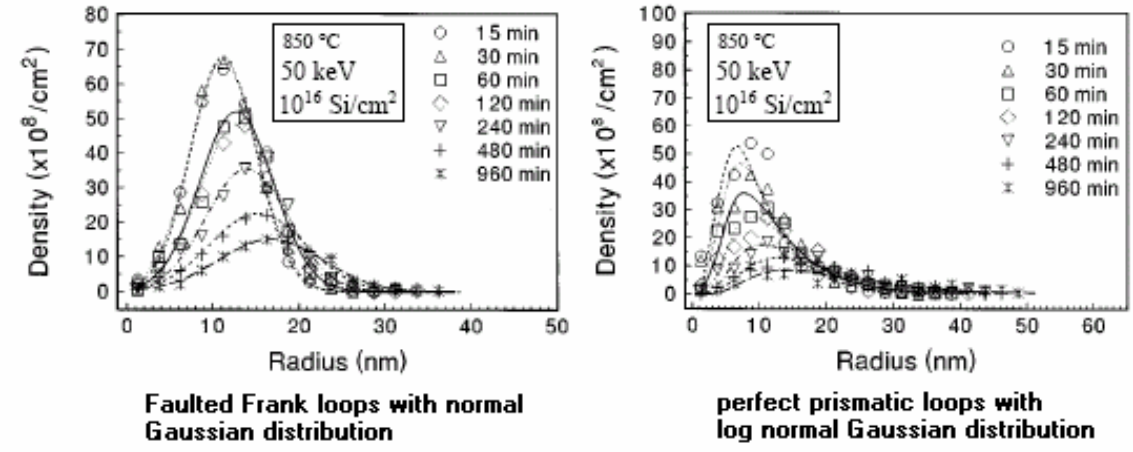


Figure 3-27: Difference in distribution function (notice the tail for perfect loops).

Authors assign optimum light emission to annealing temperatures varying between 975–1100°C, with an average of 1050°C and annealing times around 20 minutes, at least for boron implants. Due to the coarsening the average loop radius is much larger and the density is much lower after 1000°C anneal than for lower temperature anneals. Some "rare authors" assign the light emission to the perfect prismatic loops, because for a silicon implant the radius of perfect loops is largest. According to reference 4, the average loop radius, which is an indicator of how large the loops are, is important in relating the spread of the strain in the lattice. The larger the loop, the larger is the length of the strained lattice. The larger strained lattice contributes to the improved potential barrier, which is the reason for the increased intensity.

Kase and Liebert[17] et. al. support this relation, loop size-light intensity, although they approach it from a slightly different angle. They keep the thermal budget the same, but performed boron implants at different implant temperatures: liquid nitrogen temperature (NT), -60°C and room temperature (RT), and established density and size of the loops and resulting leakage current. The leakage current is related to the amount of recombination that takes place.

Table 3-5: Variation of implant temperature (notice highest recombination for RT implant).

Implant temperature	Density (cm^{-2})	Size (nm)
LN	$2\text{–}5\times10^{8}$	50–150
−60 °C	5×10^{10}	20–50
RT	3×10^{9}	> 100

Implant temperature	1000 °C annealing		800 °C annealing	
	−5 V	−1.5 V	−5 V	−1.5 V
RT	1.26	0.508	3.55	1.21
−60 °C	0.710	0.299	2.95	0.822
LN	0.812	0.492	2.71	0.884

B^+ implanted at RT, −60 °C, and LN temperature. Implantation condition is B^+ at 35 keV with 1×10^{15} cm^{-2}. Annealing conditions are 1000 and 800 °C for 10 min. The leakage current was measured at −5 and −1.5 V.

They conclude “the higher concentration of loops at -60°C than at RT does not correlate with J_R. On the contrary, J_R at LN temperature is not reduced. We cannot explain this at this time, but we assume that the large dislocation loop in Fig. 1 (c) may be concerned with large J_R.”

Reference 3 reveals that “Meng et al. investigated the interaction between oxidation induced point defects i.e. injected interstitials during oxidation, and dislocation loops.”

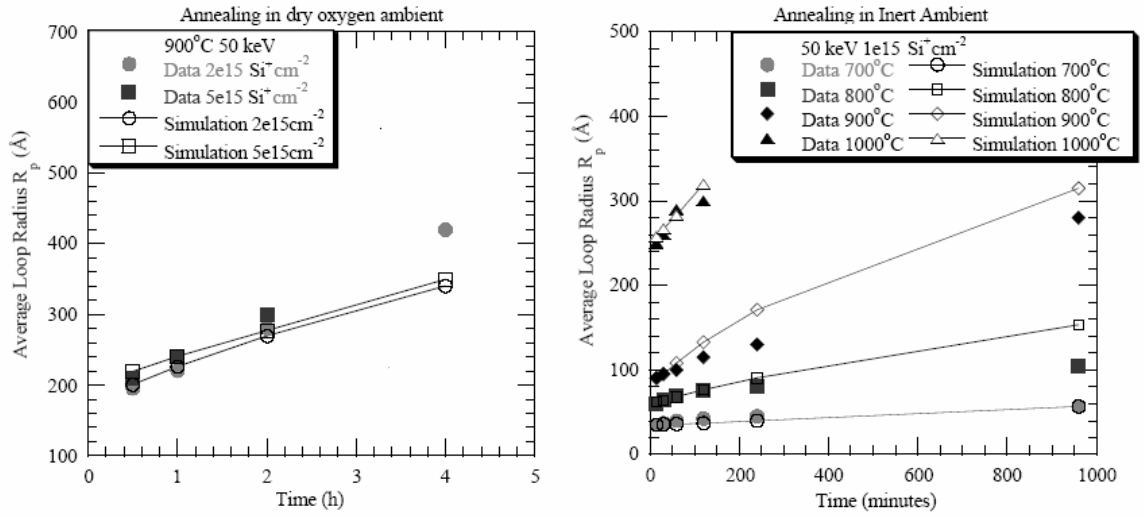


Figure 3-28: Dry oxygen and inert annealing ambient (notice increased loop radius for oxygen).

Annealing in a dry oxygen ambient results in 2.5(!) times larger average loop radius in comparison with annealing in an inert ambient for 1×10^{15}cm^{-2} implant dose. When the recombination rate correlates with average loop radius, then performing the annealing step in an oxidizing environment might not be a bad idea for implant doses around 1×10^{15}cm^{-2}. Figure 3-28 reveals us that the average loop radius is almost independent of implant dose for annealing in dry oxygen ambient. Figure 3-19 shows us that the amount of interstitials bounded by the loops is directly proportional to the implant dose. Therefore an implant dose that exceeds around 3×10^{15}cm^{-2} must be followed by an inert anneal.

However Sobolev[6] et. al. argues that the optimum light intensity on average happens for annealing budgets (~1050°C for 20 minutes) that must result in the dissolution of loops. Therefore the remaining implant damage after Solid Phase Epitaxy re-growth and dissolution of the loops is responsible for the light emission, not the loops themselves: “The dislocation loops are found to dominate after annealing at 1000°C, as in paper [1], but they do not produce the maximum quantum efficiency. The maximum η_{int} and τ_p are observed after annealing at 1100°C, when the extended defects are not introduced…The influence of extended defects on the band-to-band luminescence is most likely to be related to the gettering of radiation-induced non-radiative recombination centers and/ or the introduction of new recombination centers.”

η_{int} Is the internal quantum efficiency, and τ_p is the minority carrier lifetime.

3.4 The dominant defects introduced by the implantation process: {311} Rod-like defects, Frank faulted loops and perfect prismatic loops

This information became available through extensive mail correspondence with the first author of references 27 and 28, L. Fedina.

The defects mentioned in table 2 are all extrinsic defects, meaning interstitial type of defects. This in contrast to intrinsic defects that means vacancy type of defect. From a statistical point of view, these interstitial clusters must be dominated by self-interstitials i.e. silicon atoms. Only due to the large amount of Frenkel-pairs generated before an implanted ion comes to rest (typically 1000 atoms for low energy implant).

Therefore some authors like L. Fedina, believe the term "extrinsic" is a wrong one because both self-interstitial atoms and vacancies are native point defects i.e. intrinsic in nature. This mistake historically came from the situation when the nature of interstitial type Frank loops could not be determined exactly. They thought that this defect was introduced by agglomeration of foreign atoms meaning of extrinsic in nature. However, the term "extrinsic" is still in use nowadays in literature, but it means only "interstitial". In addition, it has been shown that rod-like defects do not *exclusively* consist of self-interstitials.

The defects should be separated not only as "extrinsic" and "intrinsic", but rather as "gliding" defects and “prismatic” defects.

3.4.1 Gliding dislocations

Gliding dislocations like 30° and 90°-partial Shockley (a/6<112>) or 60° (a/2<110>)- dislocations are always "intrinsic". They can never be "extrinsic", and they never include vacancy aggregation. Gliding defects form without any movement of point defects. This dislocation is introduced to relieve the local strains of the crystal: by plastic deformation e.g. during hetero-epitaxial growth of films on foreign substrates (silicon on Germanium)

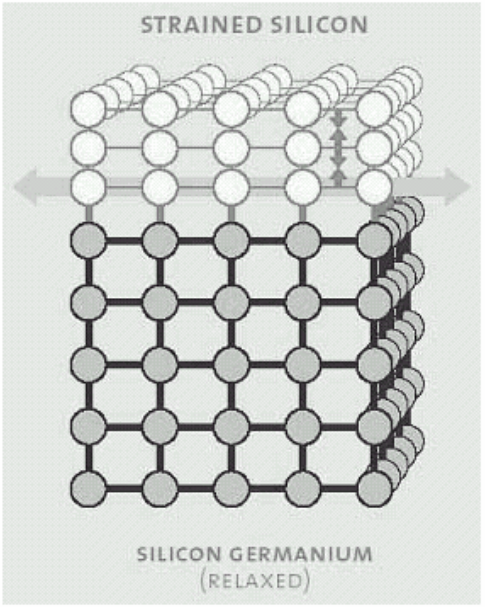


Figure 3-29: Lattice mismatch result in gliding dislocations.

or to accommodate the "prismatic" defect in the lattice. A 60° gliding dislocation is split into a 30° and 90°-partial Shockley gliding dislocation when the strain of the core of 60° dislocation is high.

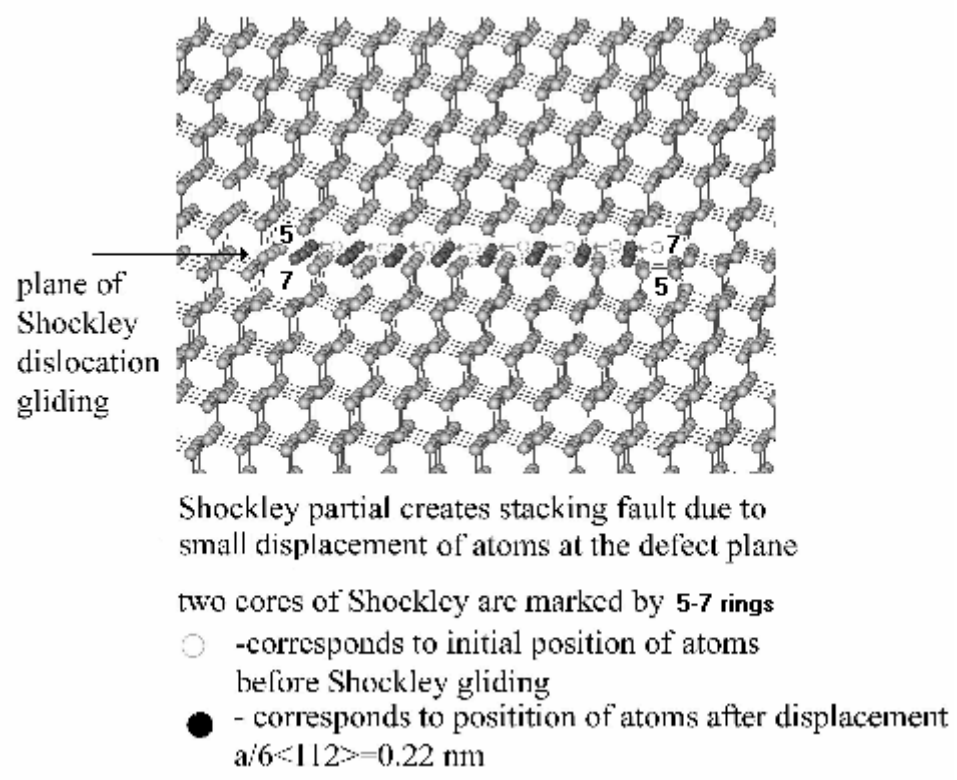


Figure 3-30: Shockley gliding is small displacement of host atoms.

Gliding of dislocation is bond switching followed with small displacement of host atoms within the vector of lattice translation. This Burgers vector always shows the direction of displacement of the crystal. The Burgers vector of gliding dislocations is always lying on the defect plane. Thus no additional extra layer is created after gliding. The displacement-angle is the angle between the defect plane and the Burgess-vector.

3.4.2 Prismatic dislocations

"prismatic" dislocations form during aggregation of point defects e.g. due to the implantation process. Aggregation of (self) interstitials results in “extrinsic” prismatic dislocation loops and aggregation of vacancies results in “intrinsic” prismatic dislocation loops.

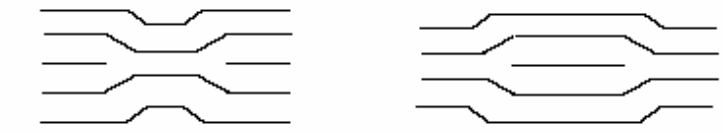


Figure 3-31: Intrinsic and extrinsic character of dislocation loops.

The term "prismatic" comes from the fact that the Burgers vector never lies on the defect plane. The displacement angle is 90° with respect to a Frank defect plane (a/3<111>) or 60° with respect to a perfect prismatic dislocation loop plane (a/2<110>). Prismatic defects exist mainly in the shape of LOOPS corresponding to the shape of a certain plane inserted to or cut from the lattice for respectively “extrinsic” or “intrinsic” dislocations.

3.4.3 {311} Rod-like defects

Figure 3-32: {311} Type defects for the weak beam dark field imaging condition[19].

It is believed that interstitials form chains along <110> direction and these chains come together to form a {113} plane. This defect can get very long (about 1μm) in the <110> direction, hence is given the name “rod-like” defects[21].

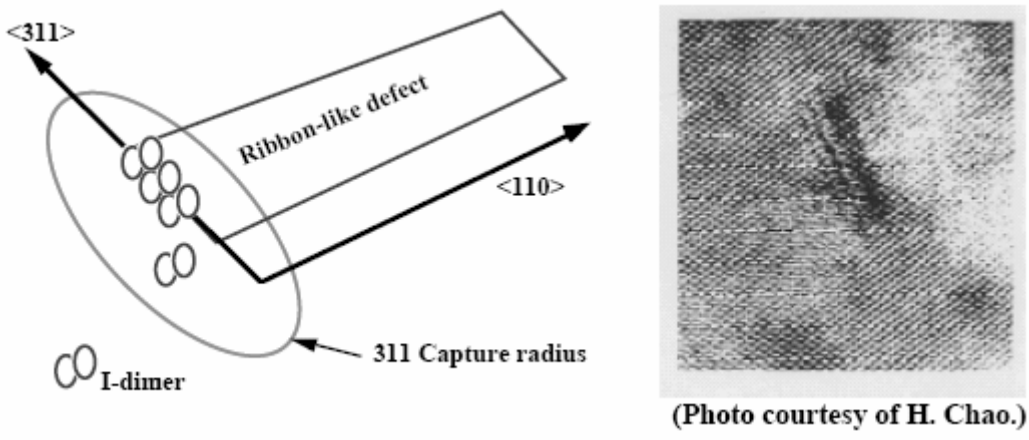


Figure 3-33: Formation of long interstitial chains on <311> plane in <110> direction[33].

These “rod-like” defects are {113}-stacking faults. The {113}-plane consists of interstitials chains. The formation of chains from interstitials is still unknown. Each interstitial on the {311} plane occupies a lattice site. It is a “virtual” extra plane because the density of interstitials at the {311} plane is not enough to create a full extra plane. Therefore the chains are broken up in segments by 8-rings. 8-Rings are empty sites. If additional interstitials are inserted into the 8-rings, the {311} defect immediately transforms to the perfect prismatic loop. The “virtual extra {311} plane lies between 2 {113} lattice planes. At each side the chains are bonded to the lattice planes by 5-7-ring configuration.

There is a final equilibrium structure that is Takeda's structure[29].

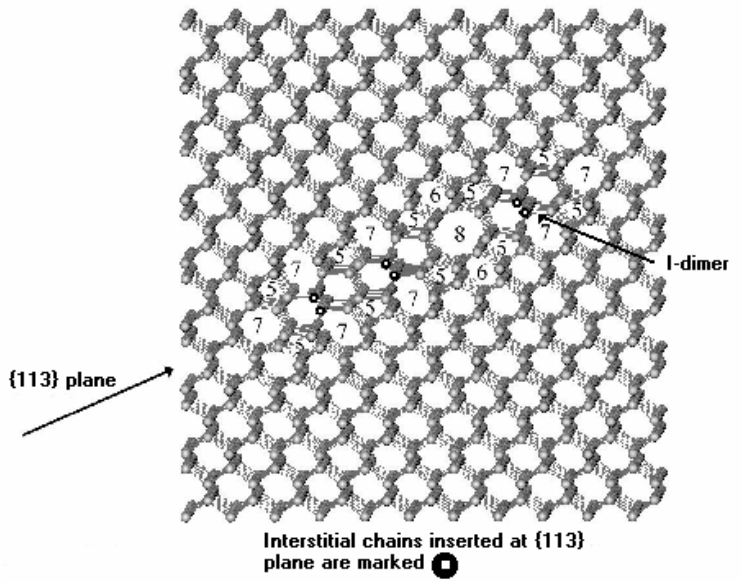


Figure 3-34: Cross-section of {311} rod-like defect (I-dimers = interstitial chains that form extra "virtual" plane, and 5-7 rings surround extra plane to relieve stress).

5-7-Ring defects are associated with strain relaxation. The distance between the "virtual" extra {113} plane and the 2 {113} lattice planes it lies between equals the burgess vector. The burgess vector is a/25<116>=0.14nm. In contrast to dislocation loops, these I-dimers chains are surrounded by a distorted crystal structure. The recent claim of G.Z. Pan et al. that " {113} defects other than dislocation loops result in strong silicon light emissions." [33], might be linked to this distortion of the crystal structure.

The final structure of complex point defect clusters mainly depends on 2 aspects:

- The competition in point defect recombination rate at the cluster i.e. restoration of covalent bonds with corresponding bond lengths and bond angles. The recombination rate depends mainly on the temperature;
- The rate of additional point defect arrival at the cluster. Point defect arrival depends mainly on the local point defect super saturation.

High super saturation of point defects is needed for {113} defect to grow in <110> direction. A high density of nuclei strongly decreases the super saturation and inhibits the growth.

The type of point defect super saturation differs in the proximity of an energy sink. For example near the surface vacancy super saturation dominates and due to this lots of vacancy type clusters are created. Far away from the surface interstitial super saturation dominates and lots of interstitial type clusters are created. Due to the ion implantation process lots of interstitials are available to form interstitial type of defects. Therefore these interstitial type of defects dominate throughout the substrate. Under those circumstances vacancy clusters act as interstitial traps. The resulting interstitial clusters transform into {113} defect of the interstitial type.

3.4.4 Frank faulted loops

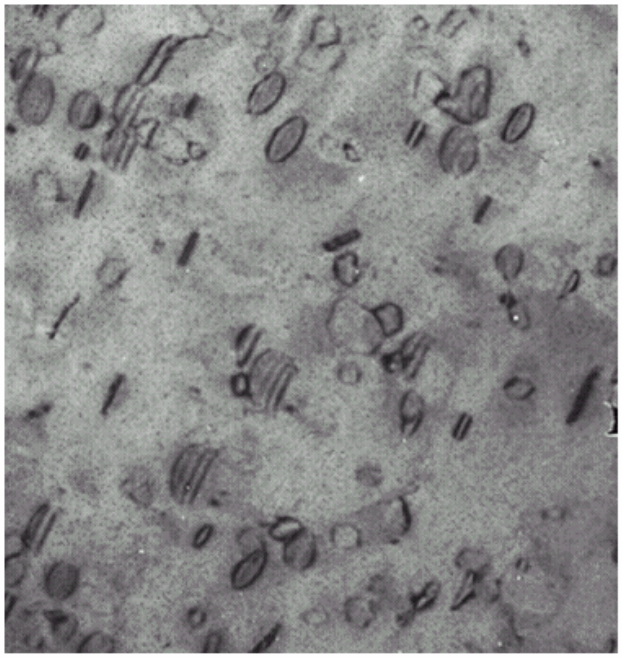


Figure 3-35: Frank stacking fault loops (notice these loops look like lips).

A full extra plane is inserted between 2 {111} layers[27].

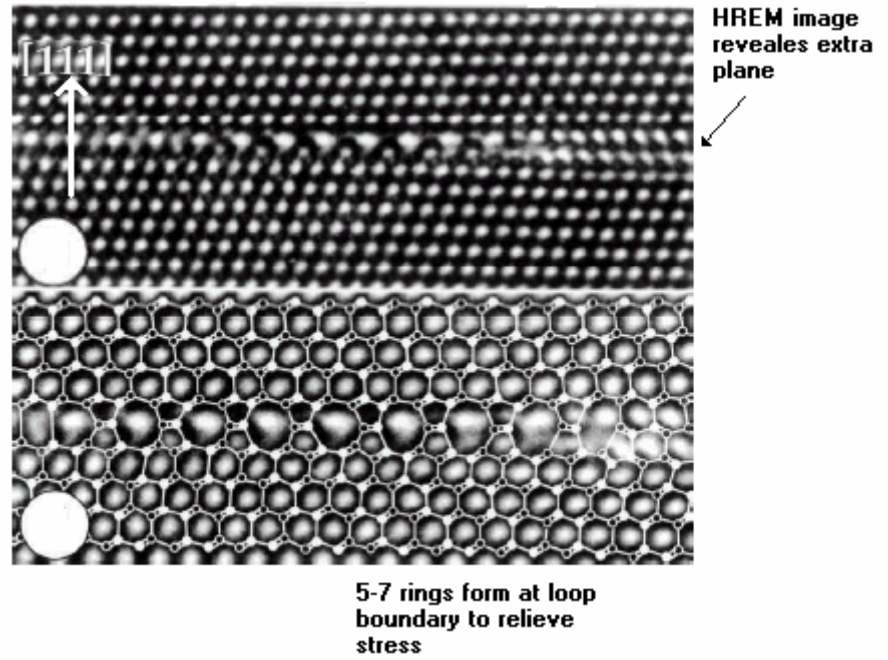


Figure 3-36: Extra Frank stacking fault plane (under HREM conditions) introduces many 5-7 rings near dislocation loop boundary to relieve stress.

The full extra plane is inserted in twin position, graphically illustrated by figure 3-37. To be clear, this figure does not reflect the situation in the HREM.

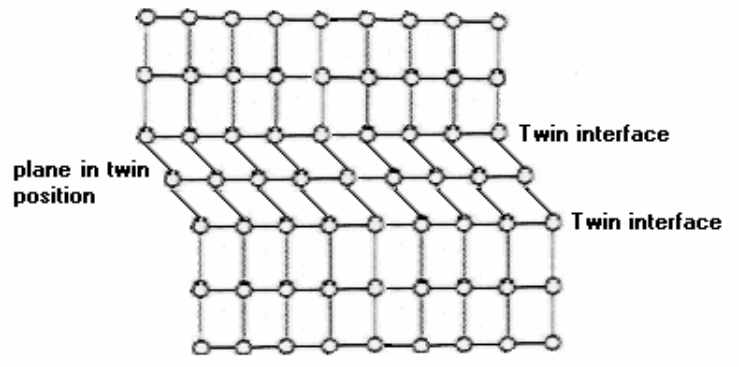


Figure 3-37: Principle of twin layer[12].

Dark spots in the HREM image correspond to projection of atomic chains in the [110] direction, and white spots are the channels along the [110] direction in the silicon lattice. The dark spots located at the extra plane are rotated (according to their twin position) with respect to dark spots far from the defect. Another layer of rotated dark spots is placed at the top of the extra plane. From the HREM it is clear that the interstitials that form the extra plane do not occupy lattice positions. Thus the Frank faulted loop (also called Frank stacking fault) is accompanied by a stacking fault, hence its name.

The extra plane bonds with the twin interface from one side (accompanied by Shockley gliding) and from the other side by an additional stacking fault in the form of Shockley gliding (creating the second twin interface). The Burgess vector of this extra plane is a/3<111>=0.314nm and equals the distance between the extra {111} plane in the center of the Frank stacking fault and the {111} lattice planes it lies between.

5-7-Rings are created only at the loop boundary (the core) with a thickness of about 0.3nm. In figure 3-36 many 5-7-rings are depicted. The HREM condition helps to reveal 5-7-rings by stress relaxation. However for Frank stacking faults under “normal” conditions just one 5-7-ring exists at each side of the loop boundary. At this loop boundary the strain is highest. 5-7-Ring defects are associated with strain relaxation. The energy of the core decreases due to a smaller Burgers vector of 5-7-ring defects a/5<111>= 0.191nm compared to the center of the loops, a/3<111>=0.314nm. Strain energy is proportional to the square of the Burgers vector.

3.4.5 Perfect prismatic loops

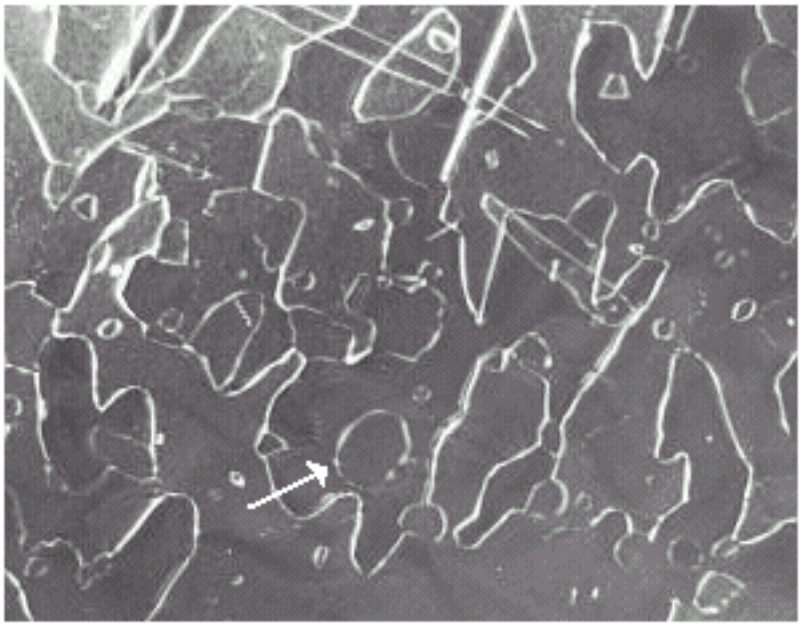


Figure 3-38: Dislocation network (notice absence of lip shape for perfect loops, also notice rim at loop boundary caused by 5-7-rings to relieve stress).

A full extra lattice plane is shifted between 2 {111} planes, but not in twin position. Therefore each interstitial on the {111} plane occupies a lattice site. Therefore this defect is not accompanied by a stacking fault. The distance between the extra plane and the 2 lattice planes is equal to the distance between 2 {111} lattice planes in a defect free region, a/2<111>=0.384nm. Therefore this defect is called perfect. No stacking faults are introduced, figure 3-39[29].

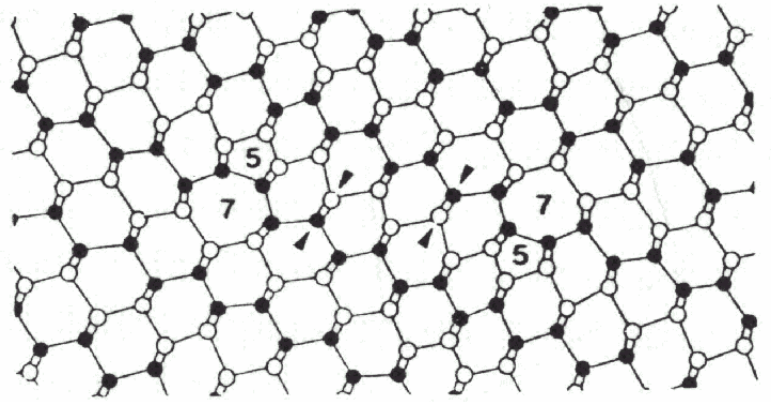


Figure 3-39: Perfect insertion of extra plane (notice in this model only one 5-7 ring accommodates the loop boundary).

What is remarkable is that the burgess vector associated with a perfect plane (0.384nm), is larger than the burgess vector associated with a Frank stacking fault (0.314nm). Because strain energy is proportional to the square of the Burgers vector, the strain energy associated with perfect loops is larger. Therefore in the early stage of the annealing process Frank loops dominate. Later on perfect loops dominate, because of the preferred ripening of prismatic loops in comparison to Frank loops.

The center of the plane bonds with the {111} lattice planes in a perfect way. However at the loop boundary (the core) again a 5-7-ring configuration with a thickness of about 0.3nm to relax the strain.

Perfect loops form by transformation of {311} rod-like defects. Frank loops do not. {311} Defects have 8 rings (empty sites) in their extra “virtual” lattice plane. The reason for this is that the density of interstitials is too low to form a full extra plane. When the implant dose is increased ($>1\times10^{14}cm^{-2}$) not only {311} defects form, but also perfect loops. Interstitials migrate to the {311} defects that act as nuclei for perfect loops. Then the interstitials are inserted into the 8 rings. After insertion the {311} defect immediately transform into perfect loops.

3.5 Dislocation loops and their influence on light emission properties

3.5.1 Dislocation introduced stepping stones and transition barriers to increase the quantum efficiency

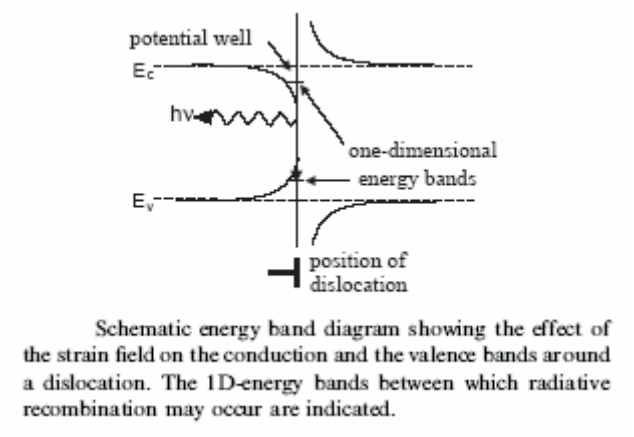
Both dislocation loops and doping spikes act as blocking potential, thereby hindering the motion of carriers across the junction. The carriers are confined to the region where the blocking potentials are situated, thereby increasing the probability of recombination and hence the quantum efficiency.

Rebane[16] et. al. report:
“Bound states for electrons and holes at dislocations in semiconductors can originate from three main factors:

- Long range strain and electric fields of the dislocations;
- Dangling bonds; (authors note: for example laBusch[8])
- Impurities and intrinsic defects in the vicinity of the dislocation. (Authors note: for example Sun[14]).

In principle, different experimental techniques exist to distinguish between the three types of dislocation states, [1] but the results are not always conclusive.

Dislocation bound states arising from the long range strain and electric fields of the dislocations form a set of one-dimensional (1D) dislocation bands split off from the valence- and conduction band edges.



Schematic energy band diagram showing the effect of the strain field on the conduction and the valence bands around a dislocation. The 1D-energy bands between which radiative recombination may occur are indicated.

Figure 3-40: Formation of 1D dislocation energy bands that act as stepping stones.

This set of 1D-dislocation bands is responsible for a wide range of the dislocation-related phenomena such as dislocation photoluminescence and cathode luminescence [1..6], dislocation light absorption below the intrinsic absorption edge [7..8]; dislocation conductivity and microwave conductivity [9..11].

Theoretical calculations of the energy positions of the 1D-dislocation bands can be divided in two groups. The first group consists of quantum chemical calculations, which take into account the discrete atomic structure of the crystal. At present the results of these calculations are contradictory and strongly depend on the approximations made and the parameters chosen. [12..18].

The second group consists of the variational calculations made in the continuous media approach, [19..27] which is based on empirical effective-mass and deformation approximations. Both these approximations fail in the vicinity of the dislocation core. But the approach seems to be justified for shallow 1D-dislocation bands arising from the dislocation strain field because the characteristic size of the resulting wave functions is larger than the dislocation core and therefore the core should not affect these states strongly.

Previous theoretical calculations of the structure and the energy positions of the 1D-dislocations bands in the continuous medium approximation were mainly restricted to the case of electron bound states with the few exceptions [19-21,27] where the hole bound states were also considered. This is because of the fact that valence band in cubic semiconductors has a complex structure and consists of sub-bands of light and heavy holes and thus the variational calculations of hole binding energies become very complicated and their accuracy is rather low."

V. Kveder[44] et. al. report "…considerable reduction of nonradiative carrier recombination at dislocations due to impurities and core defects by impurity gettering and hydrogen passivation, respectively…"

An example of a long range strain calculation in appendix C, thanks to M. Lourenco[7] who pointed out one of the many possible paths to do so. What is most important from this example is that the band gap of semiconductors is stress or pressure dependent. In the case of silicon, the band gap decreases with increasing pressure and increases under negative pressure. The pressure is maximal at the dislocation loop boundary and then drops proportional to the distance to the loop boundary.

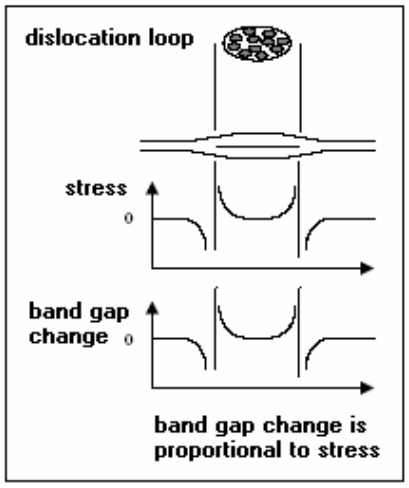


Figure 3-41: Dislocation loop induced stress bends the silicon band gap.

The observed light emitted from boron implanted dislocation engineered LEDs is in the wavelength range around 1150 nm (1.05eV–1.07eV) [1,5,6,7]. The band gap of silicon is approximately 1.12eV. Notice that the photon energy is indeed lower than the band gap energy.

So if the band gap changes it would be in the order of 50meV. Rebanne[16] et. al. theoretically predict the difference in energy between the 1D-bands and the valence- and conduction band edges to be in the range 37–50meV. The combination band gap change and band split off introduces the earlier mentioned extra energy band that act as "stepping-stones". Only difference is that due to the strain and resulting band bending, these stepping-stones are located outside the band gap.

Sobolev[6] stated that the remaining defects after SPE re-growth of the silicon and dissolution of the loops might be responsible for the light emission, and not the loops themselves. Then no strain is present. In the absence of strain no band bending occurs, but stepping stones are still present. Recall that these extra energy bands are introduced by defects. Consequently the stepping-stones will lie in the band gap and still act as generation or recombination centers.

The extra energy bands, stepping-stones, enhance the generation rate for photo-luminescence, and recombination rate for electro-luminescence and photo-luminescence.

Electro-luminescence involves the injection of excited electrons into the silicon substrate by passing an injection current. Photo-luminescence involves the generation of excited electrons that are already present in the silicon substrate. These electrons get the needed energy to cross the band gap in the form of light.

For photo-luminescence the "nearly excited" electrons with energy below the band gap, can cross the band gap by using the stepping-stones. The generation rate increases. Like the generation rate also the recombination rate will increase. For electro-luminescence the excited electrons are directly injected into the conduction band. These excited electrons recombine at a higher rate. The increase in recombination results in an increase in quantum efficiency.

We already mentioned that dislocation loops and "doping spikes" also help increase the quantum efficiency by hindering the motion of carriers that cross the junction (assuming that dislocation loops are present at 1050°C, 20 min. annealing). The changes in the band gap form transition barriers.

Therefore we conclude that clean dislocation loops i.e. free of dangling bonds, intrinsic defects and not decorated by impurities, act twofold:

- Electron and hole motion is hindered in the vicinity of the dislocation loop array that acts as transition barrier. Both carriers spent more time in the vicinity of the dislocation loop array;
- In the vicinity of the dislocation loop array the recombination rate is increased. The 1D-dislocation energy bands resulting from band bending act as stepping-stones.

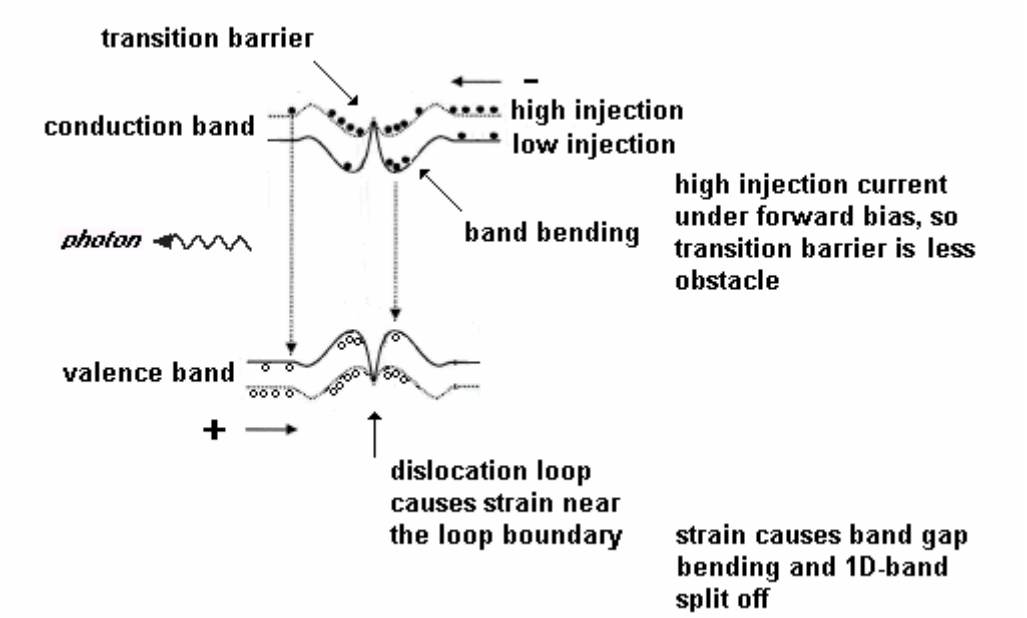


Figure 3-42: Both transition barrier and stepping stones help increase the quantum efficiency.

3.5.2 Placement of dislocation loops within the junction diode

The stepping-stones are confined to a region near the dislocation loops. We pass an injection current through the junction diode. Therefore at first guess, the dislocation loops should be situated where the amount of "nearly recombining" electrons is highest. This amount of "nearly recombining" electrons is highest at the edge of the depletion region. At the edge of the depletion region the recombination rate is already highest.

This observation is consistent with literature concerning dislocation related light emitting diodes[7] and junction diode theory[34] that describes that the amount of recombination decays exponentially from the edges of the depletion layer to the contacts.

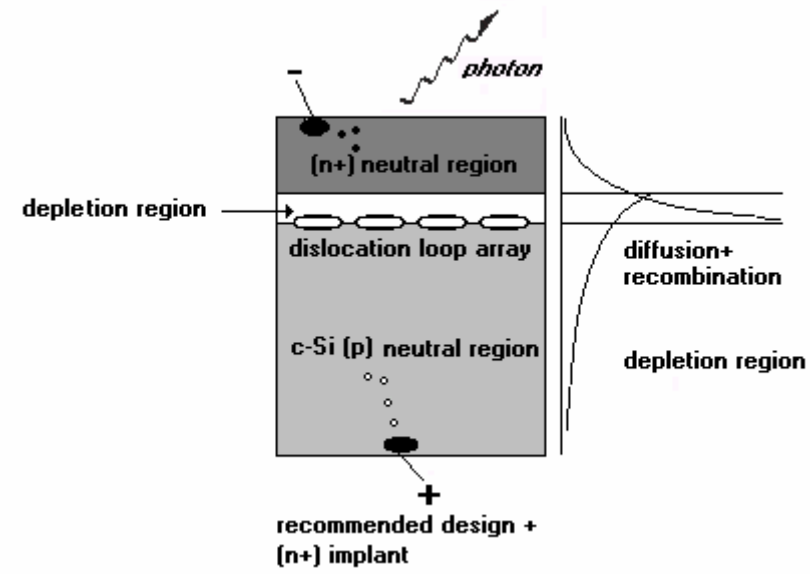


Figure 3-43: Loop array introduced where recombination is maximal (notice thin n-type region on top).

3.5.3 Dislocation engineered Light Emitting Diodes from literature

Because the LED is still in its development phase, instead of taken in production, authors use a “straight forward design”: Ohmic contacts were formed by vacuum evaporation of Al and AuSb eutectic on the p-type region and n-type substrate, respectively, and sintered for 360°C for 2 minutes. The contacts were then protected with black wax and subsequently the samples were mesa etched ($25H_2O$:1HF:$25HNO_3$) to isolate the p-n junction[7]”.

For convenience we again show figure 3-6[35].

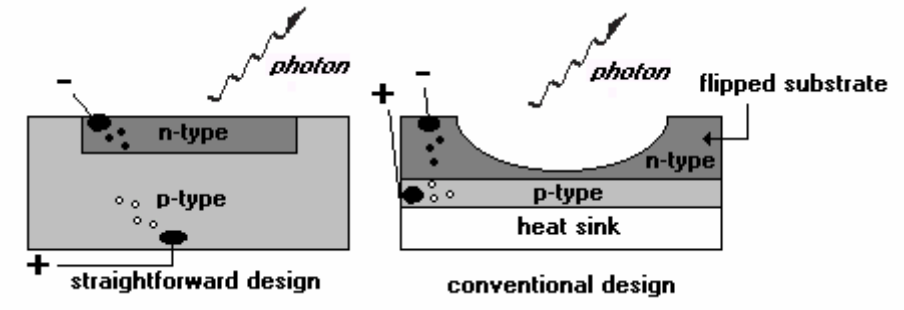


Figure 3-44: N-type silicon on top of p-type silicon.

Most authors[1,5,6,7] use boron implants (30–40keV, $1\times10^{15}cm^{-2}$) to form both the junction and dislocation loops in the n-type silicon substrate (2–7Ωcm). Low energy implants are used to reduce the etching time to isolate the p-n junction.

The exact position of the dislocation loops with respect to the edges of the depletion region seems to be irrelevant.

According to Lourenco: “Although the strongest EL was obtained from devices fabricated by a 30keV boron implantation, no specific trend on the EL integrated intensity as a function of implant energy was observed, thus suggesting that the electroluminescence is weakly dependent upon the energy range…” [41]

The dose has been chosen such that it produces an amorphous implant.

Sobolev[6] et. al. varies the background doping, using 2 sets of implants:

Table 3-6: Low substrate doping preferred.

Influence of substrate doping	boron implantation Energy	boron implantation dose	phosphor substrate dose
	E	Q	Q
Sample	keV	cm^{-2}	cm^{-2}
1	40	1×10^{15}	1×10^{13}
2	40	1×10^{15}	1×10^{16}

The light properties for sample 1 ($1\times10^{13}cm^{-2}$) give better results than for sample 2 ($1\times10^{16}cm^{-2}$). Thus low background doping is preferred.

Yes sufficient high boron implants (>$1\times10^{16}cm^{-2}$) will result in boron-Interstitial-Clusters[14], thereby enhancing the quantum efficiency. However besides that used implant doses are below $1\times10^{16}cm^{-2}$, the question remains…wouldn’t phosphor-implants also form clusters? For both boron and phosphor form respectively boron-interstitial-pairs and phosphor-interstitial-pairs during **T**ransient **E**nhanced **D**iffusion[11].

There seems to be no obvious reason to combine boron implants with straightforward design. Most of the conventional surface-emitting LEDs have a thin highly doped n-layer on top with a lowly doped p-layer below. The combination straightforward design and n-type implant e.g. phosphor, would be more obvious.

Because the diffusion length of holes is 3 times lower than that of electrons, the n-type region can be 3 times as thin as the p-type region. With the n-type region on top, photons will have a much higher probability to escape from the sample, thereby increasing the external quantum efficiency[35].

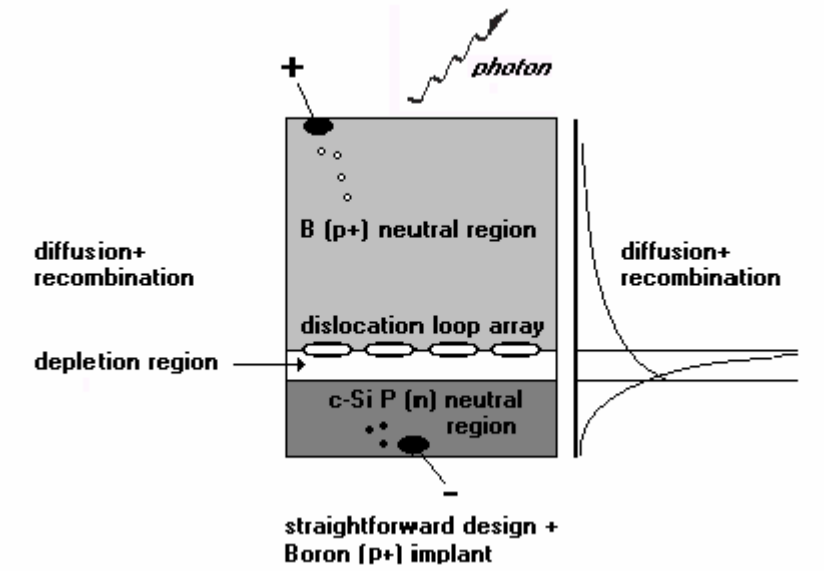


Figure 3-45: Thick p-type region on top reduces chances of photons to escape.

4 Conclusions and Recommendations

Boron implants (30–40keV, $1\times10^{15}cm^{-2}$) are used to form both the junction and dislocation loops in the n-type silicon substrate (2–7Ωcm). The maximum quantum efficiency is about 0.1% and is achieved for thermal budgets 975–1100°C, 20 min. The observed light emitted from boron implanted dislocation engineered LEDs is in the wavelength range around 1150nm (1.05eV–1.07eV).

We want to achieve optimum result for dislocation engineered LEDs for which the dislocation loop array has been formed by a separate silicon implant.

For such an LED we recommend:

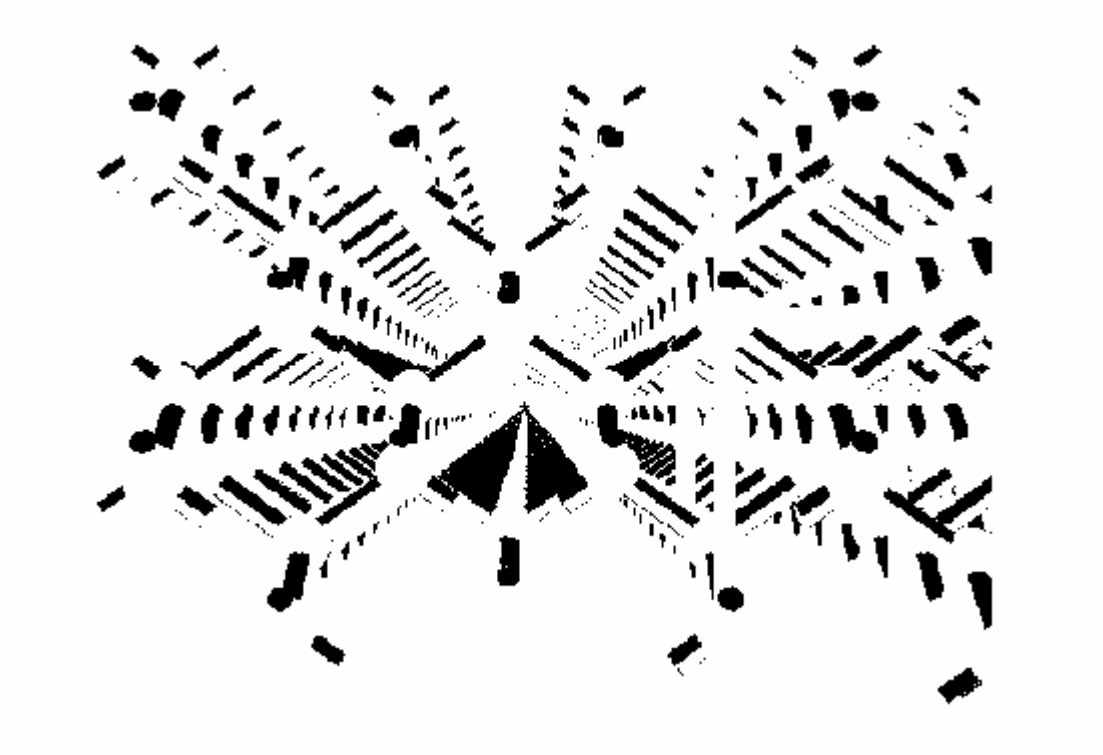
- Use low substrate doping;
- Perform the implants in a p-type silicon substrate resulting in n-type material on top for a straightforward LED design or perform the implants in a n-type silicon substrate in combination with a flipped substrate conventional LED design;
- Use low energy pre-amorphization implants followed by high energy implants to introduce the dislocation loop array;
- Do not perform the implants below room temperature;
- Use an amorphous implant ($>1\times10^{15}cm^{-2}$) resulting in category II (End Of Range) loops. For the upper limit no exact data has been found. The substrate is sputtered for doses near $1\times10^{18}cm^{-2}$;
- Perform an anneal in a dry oxygen ambient for implant doses around 1×10^{15}. Anneal in an inert ambient for implant doses exceeding $3\times10^{15}cm^{-2}$;
- Use thermal budgets around 1050°C for 20 minutes for conventional anneals;
- Make a TEM to prove whether dislocation loops did dissolve for the optimum annealing budget.

When we no longer restrict ourselves to a separate silicon implant, then additional suggestions are:

- Perform the (pre-amorphization) implant with heavy species like Germanium. The amount of interstitials bound by the end-of-range loops is higher for higher dose implants and the amorphous-crystalline interface is sharper;
- Maybe performing the implants at slightly elevated temperatures helps;
- Maybe the advantage of doping-spikes out weights the advantage of introducing the dopant and dislocation loops in two separate steps. Use n-type implants in combination with straightforward design. P-type implant in combination with conventional design.

Dislocation engineered silicon Light Emitting Diode

Part II – Measurement report



University of Twente
The Netherlands

5 Introduction

Different sets of dislocation loop engineered silicon light emitting diodes have been prepared by standard wafer processing techniques: DILED1, DILED2 and DIFLED.

General purposes of these sets are:

- DILED1: light intensity versus annealing temperature;
- DILED2: light intensity versus boron implant energy;
- DIFLED: light intensity for single, double or no silicon implants in boron diffused junction.

Extracted electrical parameters in the I-V diode characteristics will be compared to the different light intensity characteristics to find a correlation.

The references 33, 34 and 46 have been used as general references throughout the chapters. Specific references are indicated in the text.

6 Important junction diode characteristics

At this point it is examined what junction diode parameters can be extracted from measurement results, and an estimate will be given for the parameters to be extracted.

Besides junction diodes Schottky diodes exist. From this point in text with diode we mean junction diode.

6.1 On the extraction of electrical parameters

An ideal junction diode is completely described by a Schockley-equation also called ideal-diode-equation:

Equation [6-1]

$$I_D = I_0\left(\left[\exp\left(\frac{V_A}{V_{th}}\right)-1\right]\right)[A], V_{th} = \frac{kT}{mq}[V]$$

with V_{th} the thermal voltage equivalent, m the ideality-factor (or emission coefficient) and I_0 the saturation current (or reverse leakage current).

From this point in text we call this Schockley-equation ideal-diode-equation.

Some approximations have been made to derive the ideal-diode-equation:

- Both generation and recombination in the depletion region are negligible;
- The so-called low-level injection assumption stipulates that even after biasing, the minority concentrations at either side of the depletion region continue to remain much smaller than the majority concentrations there, and thus leave the latter essentially undisturbed compared to the unbiased case;
- Zero electric field in the regions at either side of the depletion region, across these regions, so that the voltage applied externally across the terminals is transmitted entirely to the edges of the depletion region itself. The bulk resistance is negligible.

Thus once the thermal voltage equivalent V_{th} or the ideality factor m, and the saturation current I_0 is known, the complete ideal junction diode can be described.

We plan to extract these parameters and 3 additional parameter: junction voltage, bulk resistance and photo current, to describe a non-ideal (practical) diode:

- Photo current $I_{v=0}$
- Saturation current I_0
- Thermal voltage equivalent V_{th}
- Ideality factor m
- Junction voltage V_j
- Bulk resistance R_{BULK}

6.1.1 Parameter extraction in the reverse bias regime

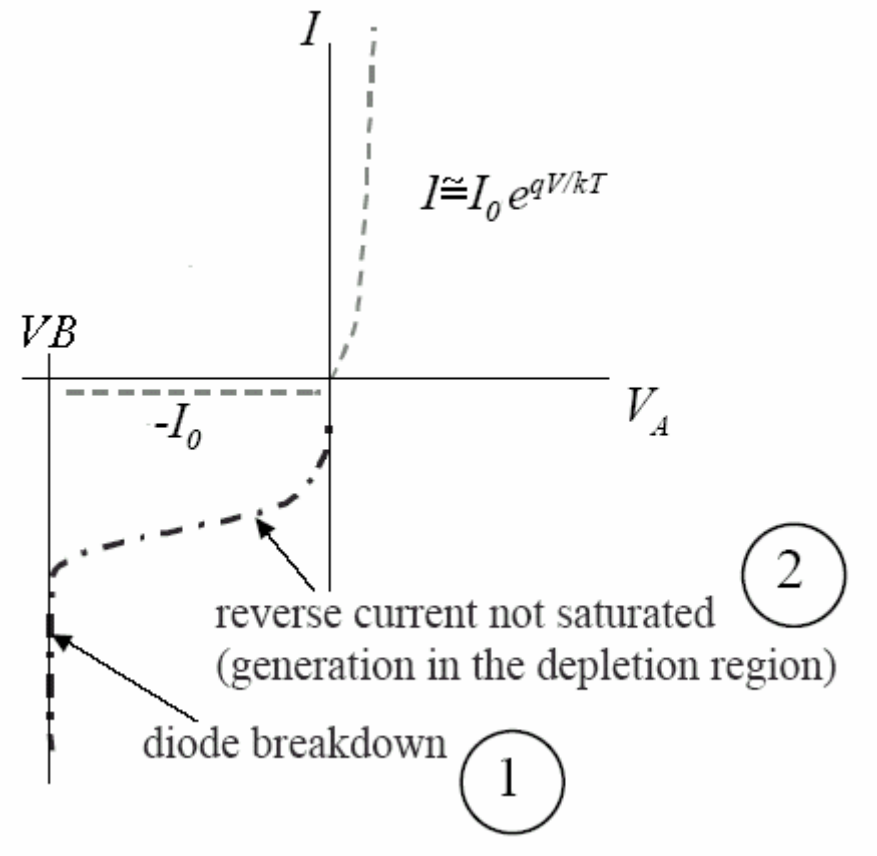


Figure 6-1: Reverse bias regime.

Figure 6-1 depicts ideal diode behavior. However a real diode no longer obeys the ideal-diode-equation when either:

- Generation and recombination in the depletion region can't be neglected;
- High-injection occurs;
- Series resistances like bulk resistance can't be neglected.

2 Effects are noticeable in the reverse bias regime.

(1) Diode breakdown (generation in the depletion region)

Diode breakdown could be either Zener breakdown or Avalanche breakdown. The former occurs in heavily doped junctions, the latter in lightly doped junctions.

Zener breakdown:
In heavily doped junctions the electric field within the depletion region is fairly strong, and increasing it further will give it enough strength to strip electrons away from their covalent bonds and thus creating electron-hole pairs. The field itself then sweeps these newly freed charges out of the depletion region, thus sustaining much higher currents than in the case of thermal generation alone.

Avalanche breakdown:
In lightly doped junctions the electric field is not strong enough to break covalent bonds directly. However, with the wider depletion layer now available, the field has more space to accelerate any free electrons that happen to be within the depletion region. Given sufficient kinetic energy, these electrons will free new

electron-hole pairs as they collide with the atoms of the crystal lattice. These secondary electrons can in turn free additional carriers.

In our measurement results diode breakdown has not been observed.

(2) Reverse current not saturated (generation in the depletion region)

Thermal generation of electron-hole pairs takes place in the depletion region. The field itself then sweeps these newly freed charges out of the depletion region. On their way out little recombination takes place because in this intrinsic region few carriers are available to recombine with. **P**-**I**-**N** photo diodes use this effect by placing a fairly large **I**ntrinsic region between a **P**-region and a **N**-region. Eventually many freed charges will reach the neutral regions to contribute to the total current at the contacts.

Indeed with increasing reverse bias V_A the depletion layer width W increases significantly. Equation 6-2 shows the depletion layer width as function of applied reverse voltage:

Equation [6-2]

$$W = W_0\sqrt{1-\frac{V_A}{\phi_0}}[m], W_0 = \sqrt{\frac{2\varepsilon_{Si}\phi_0}{q}\frac{N_A+N_D}{N_A N_D}}\left[m\right]$$

The ideal-diode-equation can be written down in different form. Equation 6-3 shows the ideal-diode-equation including thermal generation in the depletion for reverse bias:

Equation [6-3]

$$i_D = 2A\frac{eW}{\tau}n_i\left(\exp\left(\frac{V_A}{2V_{th}}\right)-1\right)\left[A\right]$$

The carrier lifetime within the junction $\tau_0=\tau_{n,p}$ are assumed constant and equal throughout the depletion region.

Together both equations reveal the quadratic relationship between the reverse current I_R and applied voltage V_A in the reverse bias regime. Often an additional offset is noticeable in the measurement results for applied voltage is zero, $V_A=0$, due to imperfect light shielding of the probe station chamber.

Because generation in the depletion region is often not negligible, saturation current I_0 is not extracted in the reverse regime. Therefore the saturation current I_0 is extracted in the forward regime. It is not uncommon that the actual measured reverse current is decades higher than the saturation current. A common value for a measured saturation current would be in the order of femto Ampères.

6.1.2 Parameter extraction in the forward bias regime

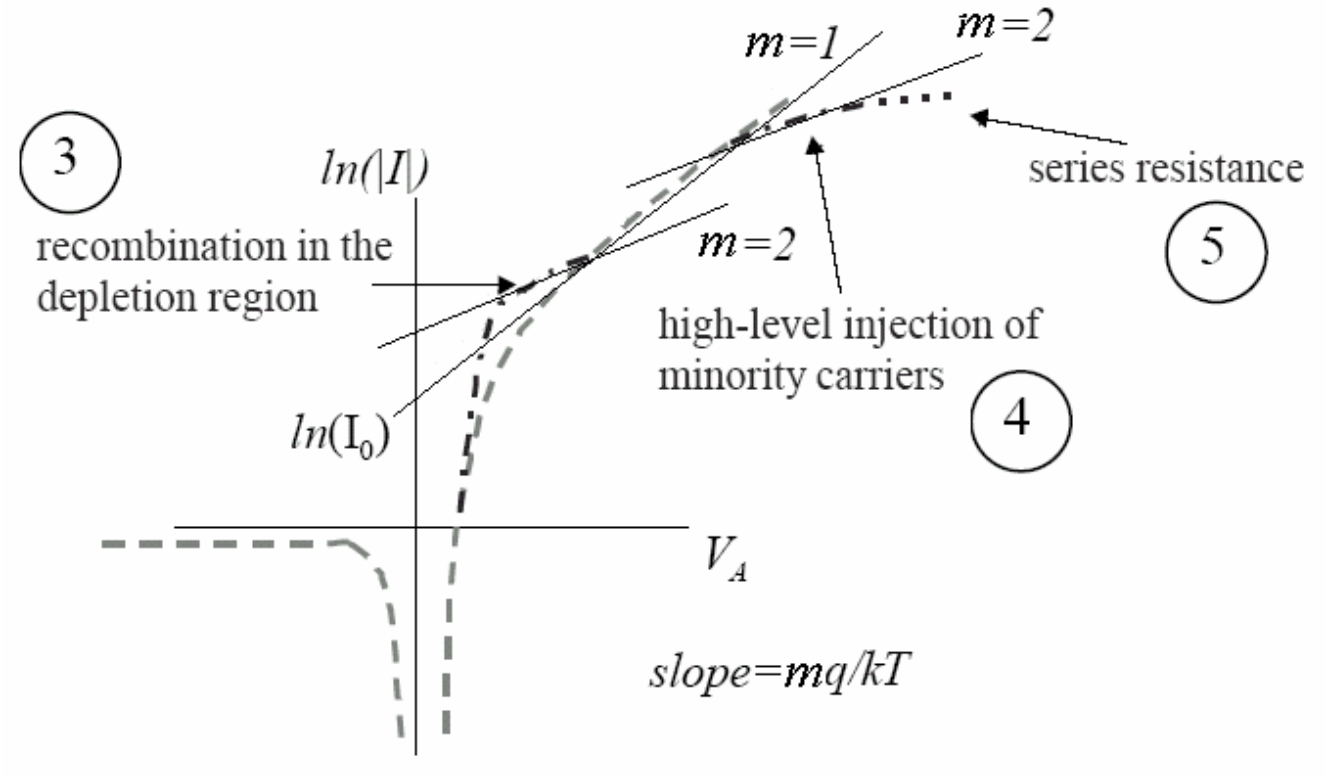


Figure 6-2: Gummel plot of forward bias regime

For $V_A >> V_{th}$ ($V_A > 4V_{th}$) the ideal-diode-equation equation can be approximated, equation 6-4:

Equation [6-4]

$$i_D = I_0\left(\exp\left(\frac{V_A}{V_{th}}\right)\right)[A], V_{th} = \frac{kT}{mq}[V]$$

Rewriting equation 6-4 gives the expression for the inverted thermal voltage equivalent, equation 6-5:

Equation [6-5]

$$\frac{1}{V_{th}} = \frac{Ln(I) - Ln(I_0)}{V_A}\left[V^{-1}\right]$$

The I-V characteristic plotted on a semi-logarithmic scale called Gummel plot, reveals a straight line with a slope equal to 25.2mv, equation 6-6:

Equation [6-6]

$$slope = \frac{1}{V_{th}} = \frac{mq}{kT} \cong \frac{1}{25.2}[mV]$$

For an ideal diode *m* equals 1. Once a nearly ideal thermal voltage equivalent of 25.2mV has been found, it is easy to find the saturation current for this nearly ideal diode. Extrapolate the slope towards $V_A = 0$, and take the exponential of the found current value on the y-axis. In this way the generation currents in the reverse current

originating from the depletion region are excluded. This derived saturation current in the forward bias regime belongs to a nearly ideal junction diode. Consequently the saturation current only consists of minority drift currents originating from the neutral regions.

From figure 6-2 it is clear that plot-sections that can be described by the ideal-diode-equation coexist with plot-sections that can not be described by the ideal-diode-equation.

(3) Recombination in the depletion region:

This loss to recombination in the depletion region occurs regardless of the operating point on the I-V characteristic, but its effects is noticeable only at the low-end where the forward current is comparable to or even smaller than that due to loss.

This recombination in the depletion region can be accounted for by adding an extra term in the ideal-diode-equation, equation 6-7:

Equation [6-7]

$$i_D = 2A\frac{eW}{\tau_0}n_i\left(\exp\left(\frac{eV_A}{2kT}\right)-1\right)[A]$$

This equation equals equation 6-3. Only difference is that the depletion layer width *W* in the forward regime, is assumed to be no longer a function of applied bias V_A. Thus equation 6-2 does not apply for equation 6-7.

Addition of equation 6-7 causes the slope in the Gummel plot to become twice as small compared to the nearly ideal case.

(4) High-level injection of minority carriers

“The high injection tends to change the charge neutrality of the neutral regions. At the p-side a negative charge will build up that will enhance the electric field across the junction. The applied forward voltage does not allow that. As a consequence the majority concentration increases to compensate for the high injection of minorities. In fact, majority and minority concentrations are nearly equal…and we have a situation as in the depletion region where both carrier concentrations differ from their equilibrium values.”

This high injection effect can be accounted for by re-modeling the ideal-diode-equation to include high injection effect, equation 6-8:

Equation [6-8]

$$i_D = \frac{I}{1+\sqrt{\frac{I}{I_{kf}}}}[A]$$

The knee current I_{kf} is the current at which this high injection effect sets in. The slope will be twice as small compared to the nearly ideal case.

(5) Series resistance

The reciprocal slope of the diode curve at a given operating current I_D in the forward bias regime is called *dynamic resistance*, equation 6-9:

Equation [6-9]

$$r_d = \left.\frac{dv_D}{di_D}\right|_{I_D} [\Omega]$$

Substitution of the ideal-diode-equation in equation 6-9 results in the resistance for an ideal diode, see equation 6-10:

Equation [6-10]

$$r_d = \left.\frac{dv_D}{di_D}\right|_{I_D} = \frac{V_{th}}{I_D}[\Omega]$$

Note that the actual resistance between the contacts is neglected. When this bulk resistance is no longer negligible, part of the applied voltage drop will be across the bulk, equation 6-11:

Equation [6-11]

$$V_{BULK} = V_A - V_j [V]$$

Junction voltage V_j is the actual voltage across the depletion region and V_A is the applied voltage at the contacts.

Suppose that for a certain bias V_A this junction diode is ideal so it can be described by the ideal-diode-equation. When the only non-negligible effect is the bulk resistance, then the voltage drop across the bulk would be, equation 6-12:

Equation [6-12]

$$V_{BULK} = V_A - V_{th} \exp\left(\frac{i_D}{I_0}\right)[V]$$

However “it is difficult to distinguish at first hand the effects of series resistance and high injection as both bend the Gummel plot at high currents. Plot on a linear scale, however, a series resistance will give a straight line, while a high injection rises exponentially.”

When both the current through the junction as well as the voltage across the contacts is known, then the bulk resistance can be estimated, equation 6-13:

Equation [6-13]

$$R_{BULK} = \frac{V_{BULK}}{I} = \frac{V_A - V_{th} \exp\left(\frac{i_D}{I_0}\right)}{I}[\Omega]$$

6.1.3 Estimating electrical parameters

Thermal voltage equivalent & ideality factor

For an ideal junction diode with ideality-factor m=1, V_{th}=25.2mV.

Saturation current

The saturation current is expressed by equation 6-14:

Equation [6-14]

$$I_0 = Aqn_i^2\left(\frac{1}{N_A}\frac{D_n}{L_n}+\frac{1}{N_D}\frac{D_p}{L_p}\right)[A]$$

Some parameters are readily known:

- Cross-section junction area A=100μm^2
- Elementary charge q=1.6$\times$10^{-19}C
- Intrinsic carrier concentration of silicon at room temperature n_i=1.45$\times$10^{10}cm^{-3}
- Electron diffusivity (or diffusion constant) D_n=36cm^{2}s^{-1} [6]
- Hole diffusivity D_p=36cm^{2}s^{-1} [6]

Other parameters should be derived:

- Electron diffusion length L_n [cm]
- Hole diffusion length L_p [cm]
- Acceptor concentration N_A [cm^{-3}]
- Donor concentration N_D [cm^{-3}]

With the electron and hole majority carrier lifetimes τ_n and τ_p known, the electron and hole diffusivity can be calculated, equation 6-15:

Equation [6-15]

$$\tau = \tau_n = \tau_p = 1.0\times10^{-7}[s]$$
$$L_n = \sqrt{D_n\tau_n} = 1.9\times10^{-3}[cm]$$
$$L_p = \sqrt{D_p\tau_p} = 1.1\times10^{-3}[cm]$$

The calculation of the acceptor and donor concentrations is somewhat more complicated, and differs for DILED1, DILED2 and DIFLED devices.

For DILED1 this peak concentration varies with implant energy. Higher implant energies result in lower peak concentrations. A boron dose of 1.0$\times$10^{15}cm^{-2} is implanted. Implant dose, peak concentration and the standard deviation are related according to equation 6-16:

Equation [6-16]

$$Q = \int_{-\infty}^{\infty} N(x)\partial x = \sqrt{2\pi}\Delta R_p N_p[cm^{-2}]$$

The implant profile is Gaussian, figure 6-3. Therefore the acceptor concentration N_A varies with distance x. We assume that the peak concentration N_p represents the acceptor concentration.

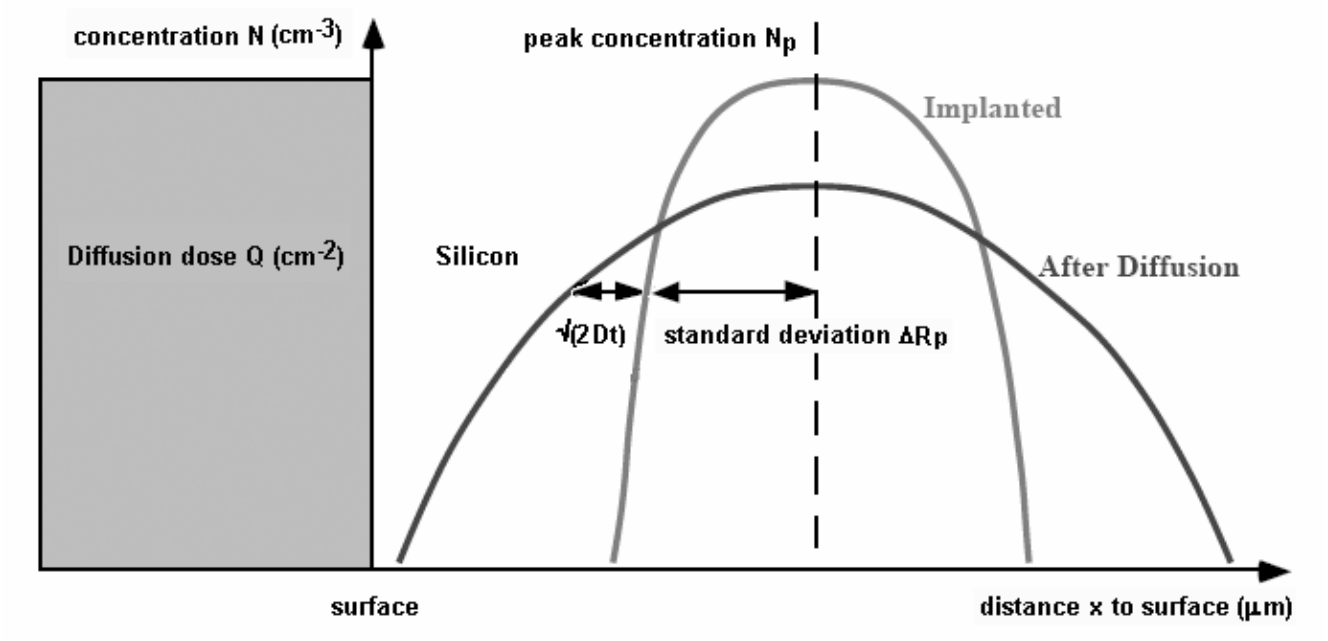


Figure 6-3: Implantation profile.

From the literature report, *Appendix A — Look-up table projected range and standard deviation most common dopants in silicon*, the standard deviation is known.

The calculated acceptor concentrations are tabulated in table 6-1:

Table 6-1: Standard concentration and acceptor concentration.

Acceptor concentration	Standard deviation	Acceptor concentration
	ΔR_p	N_A
	cm	cm^{-3}
40keV	5.62×10^{-6}	7.1×10^{19}
70keV	7.36×10^{-6}	5.4×10^{19}
100keV	8.57×10^{-6}	4.7×10^{19}

For DILED2 devices the peak concentration is approximately $1\times10^{20}cm^{-3}$. The implant dose has been adjusted in order to get a peak concentration that is independent of implant energy. If we assume again that the acceptor concentration equals this peak concentration, we know N_A.

For DIFLED devices the junction has been formed by boron diffusion. The diffusion source at the interface is infinite if silicon is heated in the presence of a gas containing the dopant. The DIFLED diffusion source is finite.

After wafer cleaning, 50nm boron doped SILOX layer is deposited. That is a p-type layer containing SiO_2+B_2O_3. Subsequently a 250nm SiO_2 layer is deposited followed by lithography to define the diffusion source and etching of the diffusion source. Finally resist is removed and boron is diffused in for 10 minutes in nitrogen ambient and 20 minutes in oxygen ambient at 950°C.

The thermal budget has been chosen such that the junction depth and sheet resistance of the LEDs light emitting surface area are equal for DILED1, DILED2 and DIFLED devices.

The finite diffusion source and resulting junction are depicted in figure 6-4:

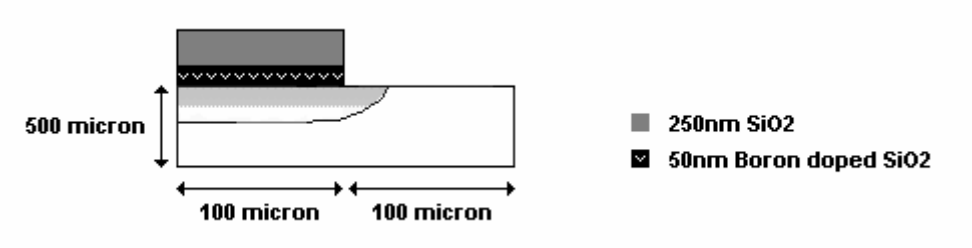


Figure 6-4: Finite boron diffusion source.

For the special condition that the source of dopants at the interface is finite with a value of Q [cm^{-2}], dose and concentration are related according to equation 6-17:

Equation [6-17]

$$N(x,t) = \frac{Q}{\sqrt{\pi D_N t}} \exp\left[-\left(\frac{x}{2\sqrt{D_N t}} \right)^2 \right] \left[cm^{-3} \right]$$

In a diffusion profile, the peak concentration is at the diffusion source, figure 6-5. Thus x being the distance to the diffusion source is zero.

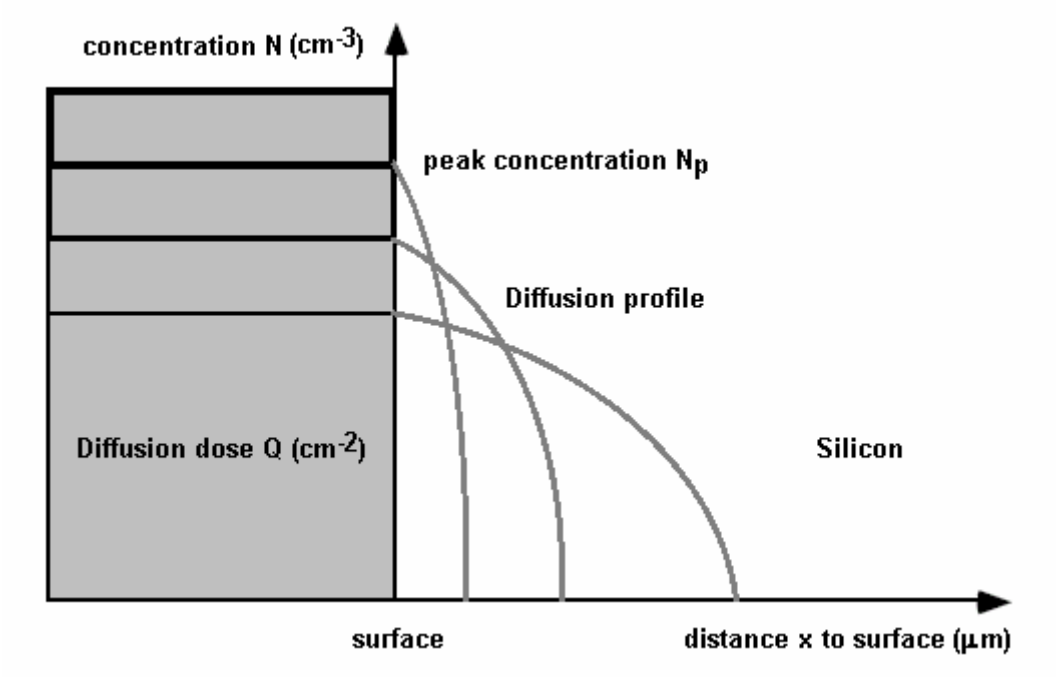


Figure 6-5: Diffusion profile for finite diffusion source.

Q again is the dose in cm^{-2}, D_N is the diffusion constant and t is the diffusion time in seconds.

A diffusion profile in silicon originating from a finite diffusion source is Gaussian. At the characteristic distance of $2\sqrt{(D_N t)}$ [cm] the dopant concentration is equal to e^{-1} times the surface concentration.

The junction has been formed by diffusion of boron for 10 minutes in nitrogen ambient and 20 minutes in oxygen ambient at 950°C. At this temperature the diffusion constant D_N for boron in silicon is approximately $7 \times 10^{-14} cm^2 s^{-1}$.

Subsequently silicon is implanted at room temperature with a dose of $1\times10^{15}cm^{-2}$ for each implantation. silicon is implanted 0, 1 or 2 times to form respectively 0, 1 or 2 dislocation loop arrays. After a first implant annealing took place in nitrogen ambient at 950°C for 20 minutes. After a second implant annealing took place in nitrogen ambient at 950°C for 30 minutes. Even if zero dislocation loop arrays were introduced, both anneals took place.

Thus the thermal budget is approximately: 950°C for 1.5 hours. Note that diffusion constants are elevated when a high number of interstitials are present. This phenomenon is called **T**ransient **E**nhanced **D**iffusion (**TED**). According to equation 6-17, the peak concentration is $3\times10^{19}cm^{-3}$.

Because the wafer resistivity ρ is between 1 and 10 Ωcm, the donor concentration N_D is between 4×10^{15} and $3\times10^{14}cm^{-3}$.

Table 6-2 summarizes the calculated saturation currents:

Table 6-2: Calculated saturation current for 2 different wafer resistivities.

Saturation current	Saturation current	
	I_0	
	A	
	Resistivity ρ =1	Resistivity ρ =10
DILED1 40keV	9.2×10^{-17}	1.2×10^{-15}
DILED1 70keV	9.2×10^{-17}	1.2×10^{-15}
DILED1 100keV	9.2×10^{-17}	1.2×10^{-15}
DILED2	9×10^{-17}	1×10^{-15}
DIFLED	9×10^{-17}	1×10^{-15}

Junction voltage

From the Schokley-equation it is clear that there is no specific voltage at which the current turns on. However the built-in potential ϕ_{bi} is often referred to as the “turn-on” voltage, equation 6-18:

Equation [6-18]

$$\phi_{bi} = V_{th} Ln\left(\frac{N_D N_A}{n_i^{\,2}}\right)[V]$$

With V^{th}=25.2mV, the “turn-on” voltage must be somewhere in between:

Equation [6-19]

$$\phi_{bi}\left[\rho = 10, \rho = 1\right] = \left[0.53, 0.60\right][V]$$

For bias values that “turn-on” the junction diode, the junction voltage V_j must be passed the built-in voltage ϕ_{bi}.

Bulk resistance

The wafer resistance gives an estimation of the bulk resistance R_{BULK}, equation 6-20:

Equation [6-20]

$$R_{WAFER} = \frac{V}{I} = \frac{\rho_{Si}}{2\Pi r}[\Omega]$$

The potential *V* is measured at a distance *r* from a probe carrying a current *I* in a material with resistivity ρ. Probes are positioned at the backside contact and topside contact. The topside contact is connected to the actual junction diode. The distance *r* between the probes equals the wafer thickness, approximately 500μm.

The estimated wafer resistance is:

Equation [6-21]

$$R_{WAFER}\left[\rho=1,\rho=10\right]=\left[3.18,31.8\right]\left[\Omega\right]$$

Until now the resistance formed by the Ohmic contacts is neglected. This resistance scales with the contact area. Typical values for good Ohmic contacts on silicon have specific resistances of $10^{-7}\Omega cm^2$. Our smallest contact area is 100^2-92^2=1536μm^2. Therefore the estimation for the contact resistance is, equation 6-22:

Equation [6-22]

$$R_{CONTACT}=\frac{\rho_c}{A}=\frac{10^{-7}}{1536\times10^{-8}}=6.51m\Omega$$

Thus in our case the resistance formed by the Ohmic contacts can be neglected when comparing them to the wafer resistance.

When the bulk resistance is much smaller than the dynamic resistance of the diode, the first one can be neglected. Combining equation 6-10 and 6-20 provides us the information for what operating current I_D, bulk resistance can be neglected, equation 6-23:

Equation [6-23]

$$R_{WAFER}<<r_d\rightarrow\frac{\rho_{Si}}{2\Pi r}<<\frac{V_{th}}{I_D}\left[\Omega\right]$$

Equation 6-24 shows for what current values bulk resistance can be neglected:

Equation [6-24]

$$I_D\left[\rho=10,\rho=1\right]<<\left[0.792,7.92\right]\left[mA\right]$$

For much smaller operating currents I_D than the values in equation 6-24, bulk resistance can be neglected.

6.2 On the extraction of optical parameters

Average peak intensity

To extract the average maximum light intensity, background (offset) correction has been performed. The background has been corrected for each of the 5 measurements, with different position of the fiber, performed upon a single device. After background correction the background is zero. Equation 6-25 shows the average peak in light intensity:

Equation [6-25]

$$\overline{I}_{PEAK}=\frac{1}{N}\sum_{i=1}^{N}\left(I_i-I_{i\_offset}\right)\left[a.u.\right]$$

Standard deviation in peak intensity

Measurements for different positions of the fiber showed some spread in light intensity values. The deviation in light intensity (with respect to the background-corrected average) has been calculated by taking a Root-Mean-Square value[47], equation 6-26:

Equation [6-26]

$$I_{PEAK-DEVIATION} = \sqrt{\frac{\sum_{i=1}^{N}\left(I_i - \overline{I}_{PEAK}\right)^2}{N-1}}\left[a.u.\right]$$

7 Process flow of Light Emitting Diodes

The original DILED1 “Light intensity versus annealing temperature” batch has been fabricated by Dr. P. Le Ming. This batch has been reproduced by T. Hoang, member of the thesis committee. In addition T. Hoang fabricated the DILED2 “Light intensity versus implant energy” batch and DIFLED “Light intensity for single, double and or no silicon implant in boron diffused junction” batch.

7.1 DILED1 “Light intensity versus annealing temperature” devices

The final DILED1 device structure is depicted in figure 7-1:

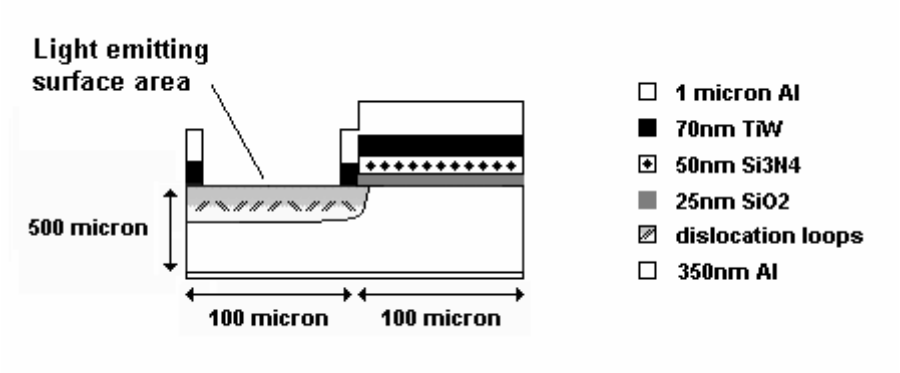


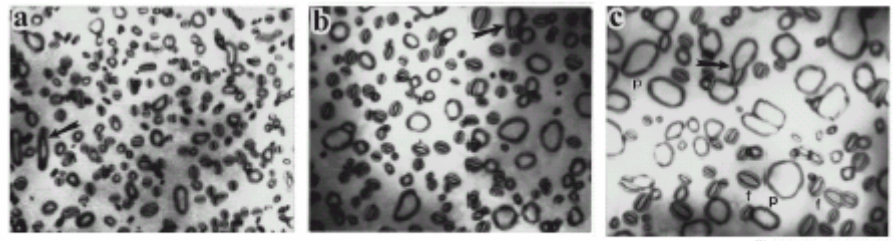
Figure 7-1: DILED1 cross-section.

A boron implant at room temperature has formed the junction. Implant energies vary between 40, 70 and 100keV. The implant dose of $1\times10^{15}cm^{-2}$ is exactly the same for all implant energies and annealing temperatures.

The following information originates from *part I – Literature report, 3.2 The implantation dose and nucleation of dominant defects.*

During ion implantation, various levels of damage can be done to the lattice. Among the defects are Nanometer-size Interstitial clusters, **I**ntermediate **D**efect **C**onfigurations (rod-like defects and {113} stacking faults), Frank stacking faults and perfect prismatic dislocation loops. What defects are present after implantation, depends almost entirely upon the implantation dose (implantation energy 40 – 200keV[15]). The implant dose of $1\times10^{15}cm^{-2}$ would allow the nucleation and evolution of dislocation loops during annealing.

Whether dislocation loops nucleate and in what stadium of evolution they are, depends on the annealing budget. Figure 7-2 shows a picture of evolving dislocation loops while annealing:



TEM symmetrical bright-field images of Si-implanted silicon taken along the [001] Si direction show the ripening growth of extrinsic dislocation loops after furnace annealed at 850 °C for (a) 5, (b) 60, and (c) 960 min.

Figure 7-2: Evolving dislocation loops while annealing.

The annealing budget for the DILED1 devices: annealing at 850, 900, 950, 1000 or 1050°C for 20 minutes in an inert N_2 ambient. The content of the table 3-4 originating from *part I – Literature report, 3.3 Annealing and evolution of dominant defects,* summarizes the different annealing regimes.

The general opinion is that dislocations that are engineered right, enhance light intensity. The way dislocation loops influence light intensity is by introducing stain/stress near the loop boundary, figure 7-3.

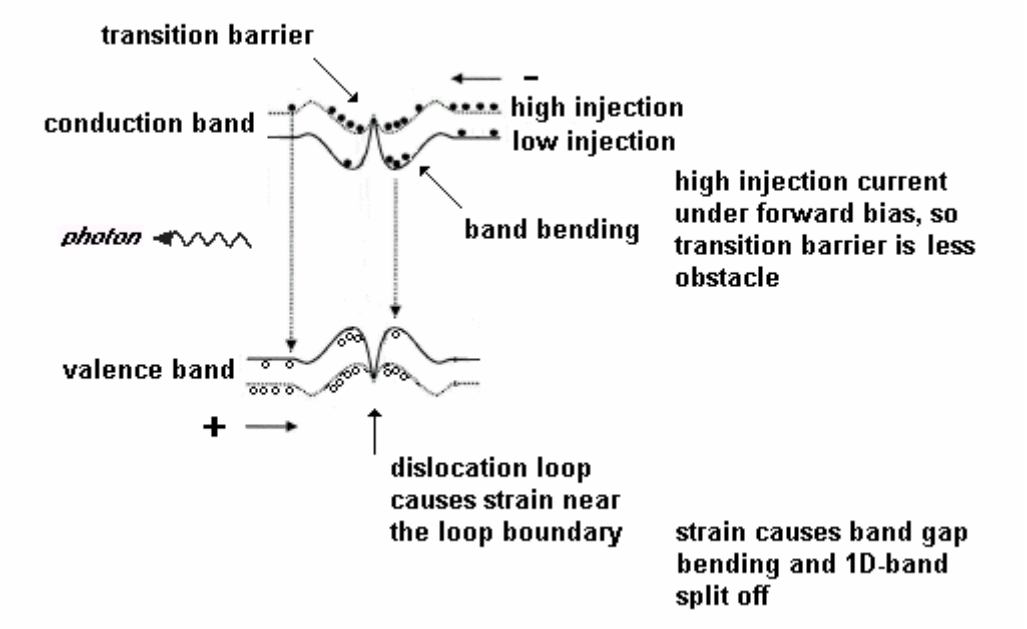


Figure 7-3: Stain/ stress near loop boundary free of dangling bonds, intrinsic defects and impurity decoration.

This stress changes the band gap energy. And the changed band gap energy is supposed to enhance the electron-hole pair generation and recombination rate. Just a fraction of the recombining electron-hole pairs emits a photon. This fraction seems fixed. However with an increasing amount of recombining electron-hole pairs, the amount of emitted photons increases as well. Light intensity is enhanced.

At the edges of the depletion region the recombination rate is highest, figure 7-4. No matter whether dislocation loops are introduced. It is just a property of the junction diode. Therefore the dislocation loops are positioned near the edges[4].

[4] Thorsten Trupke[42] and co-workers obtained "very efficient light emission from bulk crystalline Silicon" by using highly purified floatzone wafers and a textured surface. The surface was textured with inverted pyramid structure, passivated with thermally grown oxides and annealed with Aluminum (Al anneal). The title suggests that light emission is not restricted to the junction region. One can speculate that highly purified bulk Silicon is responsible for the light emission. Maybe the textured surface itself is responsible…

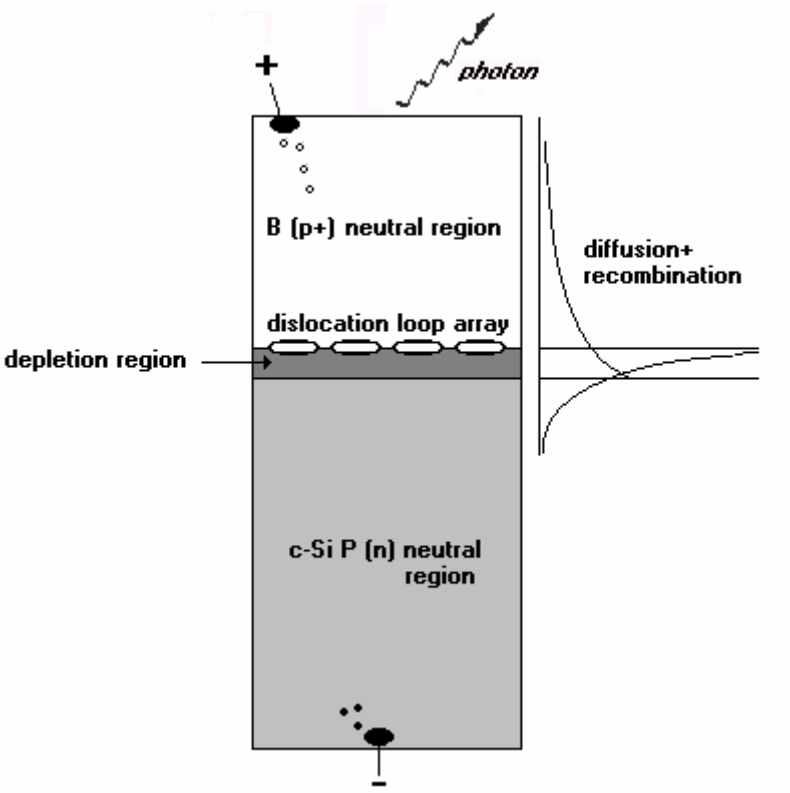


Figure 7-4: Position of dislocations at the edge of the depletion region.

The annealing temperature has been varied to introduce dislocation loops that are in different stadium of their evolution process, but why is the implantation energy varied? To take a short cut, together with the junction dislocation loops are introduced. The dislocation loops are situated around the implanted peak concentration N_p, figure 7-5:

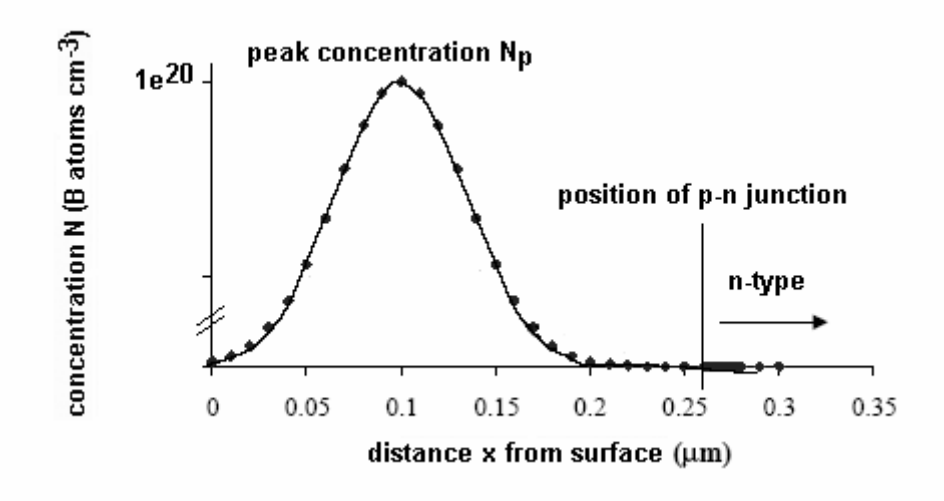


Figure 7-5: Position dislocation loops with respect to the implant profile.

The position of the dislocation loops and the position of the edges of the depletion region can't be varied independently. Both are dictated by implanting boron at a certain depth. Therefore for each implant the spacing between the dislocation loop array and edge of the depletion region is fixed.

The standard deviation ΔR_p for the projected range increases with implant energy and in addition the peak concentration decreases, figure 7-6.

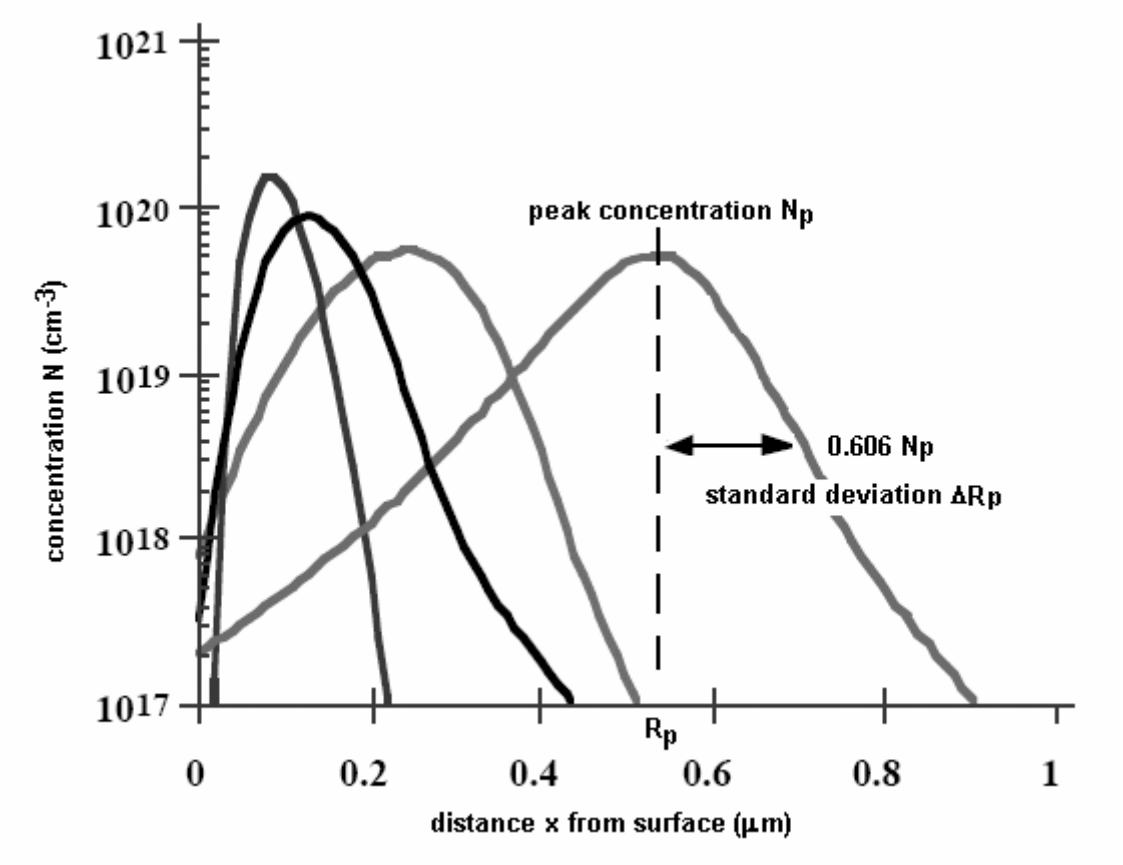


Figure 7-6: Decreasing peak concentration and increasing standard deviation with increasing implant energy.

Meaning that the spacing between the dislocation loop array and edge of the depletion region slightly increases for higher implant energies.

Of course, both the dislocation loop array and edges of the depletion region are situated further from the light emitting surface for increasing implant energies.

Table 7-1 summarizes which parameters have been varied:

Table 7-1: DILED1 parameter variation.

DILED1	Implant Energy	Annealing temperature
	E	T
	keV	°C
W2	40	850
W3	40	900
W4	40	950
WW1	40	1000
W5	40	1050
393	70	1050
187	100	1050

Note that WW1 was part of an other batch. The process parameters for DILED1 resemble process parameters of authors[45,7,1,6] that achieved similar type of dislocation engineered silicon LED's prepared by boron implantation.

Summarizing DILED1 process flow:

- The junction has been formed by a boron implant;
- Together with the junction, dislocation loops are introduced by choosing the implant dose and annealing budget according to theory;
- For each implant the spacing between the dislocation loop array and edge of the depletion region is fixed;
- The peak concentration reflects the position of the dislocation loop array, and the standard deviation reflects the spacing between the dislocation loop array and edge of the depletion region. Both are a function of implant energy.

7.2 DILED2 "Light intensity versus boron implant energy" devices

The final DILED2 device structure equals that of DILED1 devices. The DILED2 device structure has been depicted in figure 7-7:

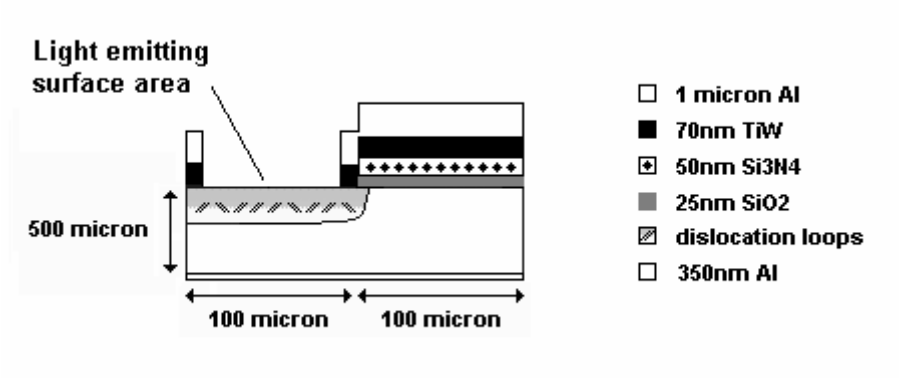


Figure 7-7: DILED2 cross-section.

For DILED2 devices the implant energy has been varied between 40, 50 and 70keV. The implant dose has been adjusted[1,2] to respectively $1.2x10^{15}$, $1.37x10^{15}$ and $1.6x10^{15}cm^{-2}$ to maintain a peak implant concentration of $\sim 1x10^{20}cm^{-3}$. When dose and standard deviation are known, the peak concentration can be calculated. For convenience equation 7-1 is shown again:

Equation [7-1]

$$Q = \int_{-\infty}^{\infty} N(x)\partial x = \sqrt{2\pi}\Delta R_p N_p [cm^{-2}]$$

Appendix B contains the standard deviation for most common dopants in silicon.

The peak implant concentration of $\sim 1x10^{20}cm^{-3}$ corresponds to a critical peak concentration exceeding $\sim 1.6\times10^{19}cm^{-3}$. Below this concentration no dislocation loops are formed, figure 7-8. This critical peak concentration is independent of the species and wafer orientation.[2]

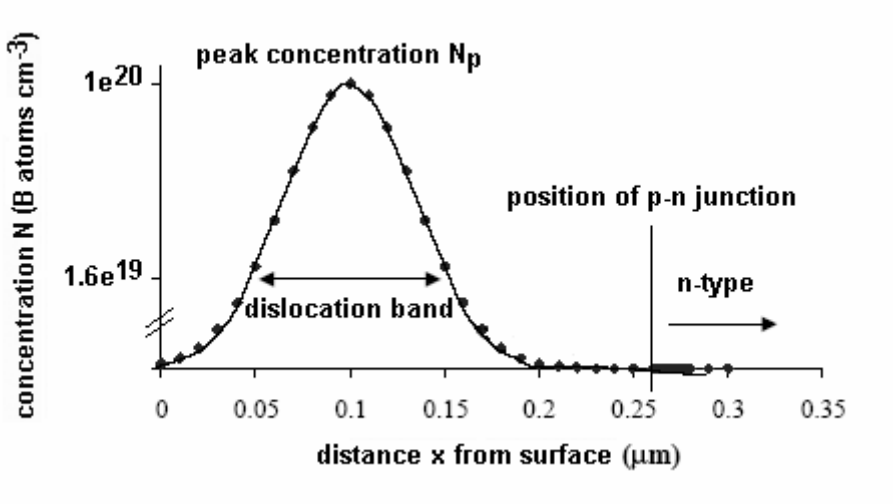


Figure 7-8: Dislocation loops for concentrations exceeding $1.6x10^{19}cm^{-3}$.

Annealing took place in an inert N_2 ambient for 20 minutes. The annealing temperatures have been chosen in accordance to Lourenco's[7,45] and Sobolev's[6] findings, who achieved maximum light intensities at respectively 975°C and 1100°C. It is interesting to note that the general opinion is that at 1100°C dislocation loops have disappeared.

Table 7-2 summarizes which parameters have been varied:

Table 7-2: DILED2 parameter variation.

DILED2	Implant Energy	Annealing temperature	Implant dose
	E	T	Q
	keV	°C	cm^{-2}
13322-3+4	40	950	$1.2x10^{15}$
13322-2	50	950	$1.37x10^{15}$
13322-1	70	950	$1.6x10^{15}$
13579-3+4	40	1100	$1.2x10^{15}$
13579-2	50	1100	$1.37x10^{15}$
13579-1	70	1100	$1.6x10^{15}$

For example 13322-3+4 indicates DILED2 devices that are found in quadrants 3 and 4 of wafer 13322.

The wafer map depicted in figure 7-9 shows to what section the quadrants 1 to 4 correspond:

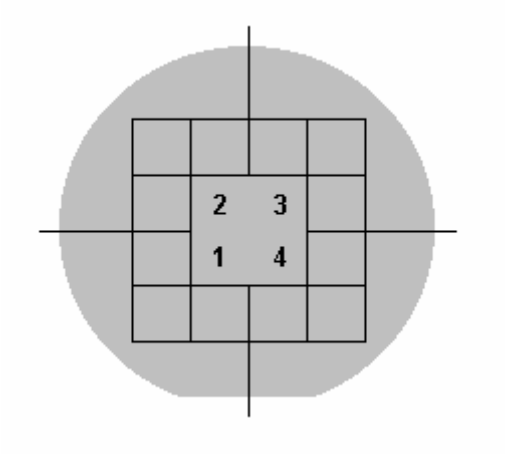


Figure 7-9: Quadrants on wafer map.

Summarizing DILED2 process flow:

- The junction has been formed by a boron implant;
- Together with the junction, dislocation loops are introduced. The annealing budget has been chosen according to Lourencos and Sobolevs findings to obtain maximum light intensities;
- For each implant the spacing between the dislocation loop array and edge of the depletion region is fixed;
- The peak concentration reflects the position of the dislocation loop array, and the standard deviation reflects the spacing between the dislocation loop array and edge of the depletion region. Both are a function of implant energy;
- The implant dose has been adjusted[1] to maintain a peak implant concentration of $1x10^{20}cm^{-3}$. The peak concentration is no longer a function of implant energy. The standard deviation still is a function of implant energy.

7.3 DIFLED "Light intensity for single, double or no silicon implant in boron diffused junction" devices

The final DIFLED device structure has been depicted in figure 7-10:

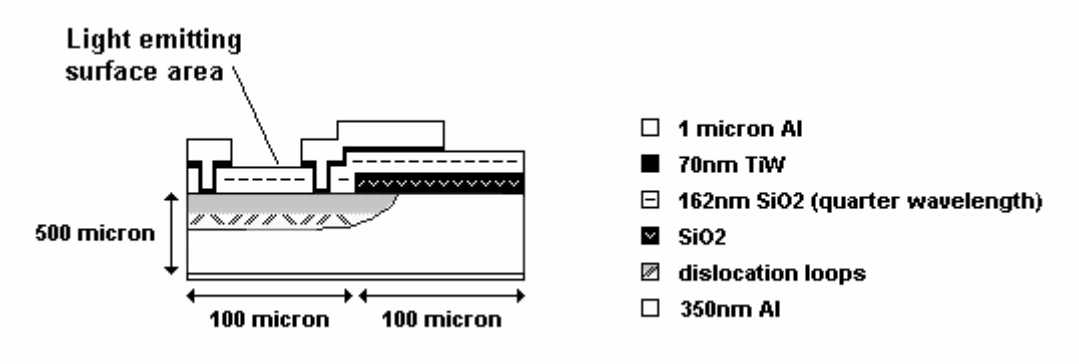


Figure 7-10: DIFLED cross-section.

The junction has been formed by diffusion of boron for 20 minutes in oxygen ambient and 10 minutes in nitrogen ambient. Diffusion reduces lattice damage, a property of the implantation process.

Subsequently silicon is implanted at room temperature with a dose of $1\times10^{15}cm^{-2}$ for each implantation. silicon is implanted 0, 1 or 2 times to form respectively 0, 1 or 2 dislocation loop arrays. After a first implant annealing took place in nitrogen ambient at 950°C for 20 minutes. After a second implant annealing took place in nitrogen ambient at 950°C for 30 minutes. Even if zero dislocation loop arrays were introduced, both anneals took place.

Thus the junction and dislocation loops are introduced separately. The junction dictates the position of the edges of the depletion region. And the dislocation loops are situated around the implanted peak concentration. The position of the dislocation loop array and the position of the edges of the depletion region can now be varied independently. Therefore for each implant the spacing between the dislocation loop array and edge of the depletion region is no longer fixed.

Adjusting the implant energy, varied the spacing between the dislocation loop arrays and edges of the depletion region.

Normally, recombination rates at either side of the junction are different. By introducing dislocation loops at one side, the opposite side, both sides, or not at all, the recombination rate is changed. This change in recombination rate reflects itself in the light intensity.

Table 7-3 summarizes which parameters have been varied:

Table 7-3: DIFLED parameter variation.

DIFLED	Implant Energy 1	Implant Energy 2
	E	E
	keV	keV
3202-1	450	X
3202-2	200	X
3203-3	450	200
3202-4	X	X
3310-1	360	X
3310-2	260	X
3310-3	360	260
3310-4	X	X

For example 3202-1 indicates DIFLED devices that are found in quadrants 1 of wafer 3202.

The wafer map depicted in figure 7-11 shows to what section the quadrants 1 to 4 correspond:

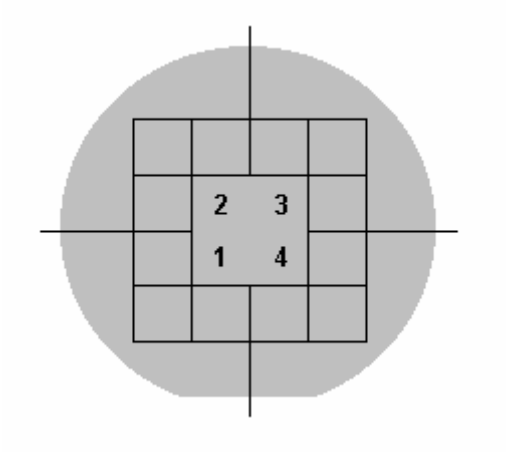


Figure 7-11: Quadrants on wafer map

Summarizing DIFLED process flow:

- The junction has been formed by diffusion of boron;
- 0, 1 or 2 Dislocation loop arrays were introduced by a silicon implant. Each dislocation loop array is supposed to enhance the total electron-hole generation and recombination rate near the edges of the depletion region;
- For each implant the spacing between the dislocation loop array and edge of the depletion region is no longer fixed. It was controlled by varying the implant energy.

8 Measuring Light Emitting Diodes

The measurements are divided in 2 parts:

- Electrical dc measurements to obtain common I-V diode characteristics;
- Optical measurements to obtain light intensity versus wavelength characteristics.

Only the measurement procedure will be explained. Encountered difficulties while measuring are in *Appendix E – Encountered difficulties while measuring*. Most important is that the results from 260keV DIFLED devices (3310-2) and 40keV & 1000°C DILED1 devices (B1WW1) should be discarded.

8.1 Electrical "I-V Characteristics" measurements

The electrical measurements have been performed on a probe station connected by a Hewlett Packard E5250A Low Leakage Switch Mainframe to an Agilent precision Semiconductor Parameter Analyzer.

The voltage has been ramped from –15V up to V_{max}. This voltage V_{max} has been selected such that the resulting diode current was at least 100mA.

For each type of device within DILED1, DILED2 or DIFLED, measurements have been performed at least 5 times in order to get 5 "smooth" I-V diode characteristics. These characteristics corresponding to 5 different devices on a wafer.

8.2 Optical "Light intensity versus wavelength" measurements

For optical measurements an additional optical fiber probe was part of the probe station. The fiber probe has been positioned on top of the LED's light emitting surface area to collect the light from the top side, figure 8-1. Light emitted at the edges has not been collected.

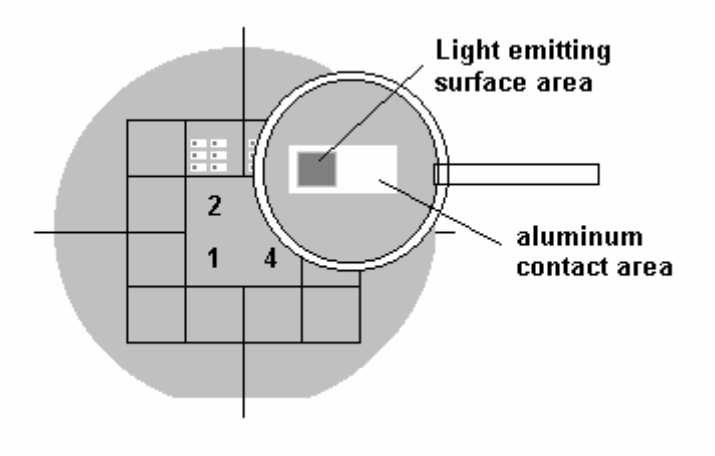


Figure 8-1: DILED1, DILED2 & DIFLED top view.

Figure 8-2 shows the light emission from the light emitting area:

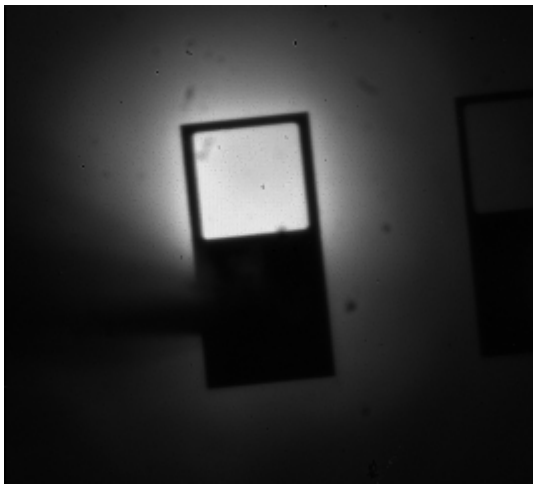


Figure 8-2: Photo by InGaAs camera of device under a 50mA forward bias (permission T. Hoang).

The actual measurement of the emitted light took place by the Spectro 320 – the Universal Spectrum Analyzer, spectrometer.

The operating software was a non-commercial version called SpecWin. The parameter settings in Specwin are in *Appendix F – Specwin software settings*.

The current has been fixed at 100mA.

For each type of device within DILED1, DILED2 or DIFLED, 10 measurements have been performed divided over 2 devices to get Light intensity versus wavelength plots. 5 Measurements with different position of the fiber probe for device1 and 5 measurements with different positions of the fiber probe for device2.

It was not possible to extract absolute light intensity values e.g. calibrated values. The reason for this is simple: the calibration process is too time-consuming. A calibration cycle would result in a (different) light intensity correction for each wavelength. However the maximum light intensity occurs at a fixed wavelength. Thus for each device the non-calibration-error is the same. Therefore individual devices can be compared with each other.

9 Presentation & Discussion measurement results

The electrical and optical results are presented and discussed.

9.1 Electrical parameters

"Electrical" parameters are derived from the I-V measurement characteristics. All electrical parameters are tabulated in *Appendix G – Measurement results, electrical parameters*.

9.1.1 DILED1

The derived parameters are:

- Photo current $I_{v=0}$
- Saturation current I_0
- Thermal voltage equivalent V_{th}
- Ideality factor m
- Junction voltage V_j
- Bulk resistance R_{BULK}

These parameters have been estimated in *6.1.3 Estimating junction parameters*, except for the photo current. For convenience the results are summarized:

- The saturation current between 9×10^{-17} and 1×10^{-15}A;
- The thermal voltage equivalent is 25.2mV;
- The ideality factor for an ideal diode is 1;
- The junction voltage must exceed the built-in voltage (also called onset voltage) of around 0.6V;
- The wafer resistance gives an estimation of the bulk resistance: 3.18 – 31.8Ω.

The derived parameters have been compared with the estimated values.

In general the extracted diode parameters give a good indication for DILED1.

DILED1 parameters, table 9-1:

Table 9-1: DILED1 electrical parameters.

DILED1	Photo current	Saturation current	Thermal voltage equivalent	Ideality factor	Junction voltage	Bulk resistance
	$I_{V=0}$	I_0	V_{th}	m	V_j	R_{BULK}
	pA	fA	mV	-	mV	Ω
850°C & 40keV	-0.749	1.15	26.0	1.03	835	13.3
900°C & 40keV	-0.816	0.941	25.7	1.02	830	11.4
950°C & 40keV	-1.97	1.04	25.8	1.02	831	13.3
1000°C & 40keV	X	X	X	X	X	X
1050°C & 40keV	-0.162	1.71	26.2	1.04	831	7.49
1050°C & 70keV	-0.179	4.22	26.8	1.06	825	17.7
1050°C & 100keV	-0.0766	3.12	26.4	1.05	821	36.8

The DILED1 parameters have been compared to find a correlation with optical parameters, but no trends were observed.

First we will present and discuss the forward characteristics.

For DILED1 the bulk-resistance R_{BULK} seems okay, because it is in the estimated range. However the DILED1 current versus forward voltage characteristics show a-linear behavior, especially the deeper 70 and 100keV implants, figure 9-1. Therefore not only bulk resistance influences this forward current.

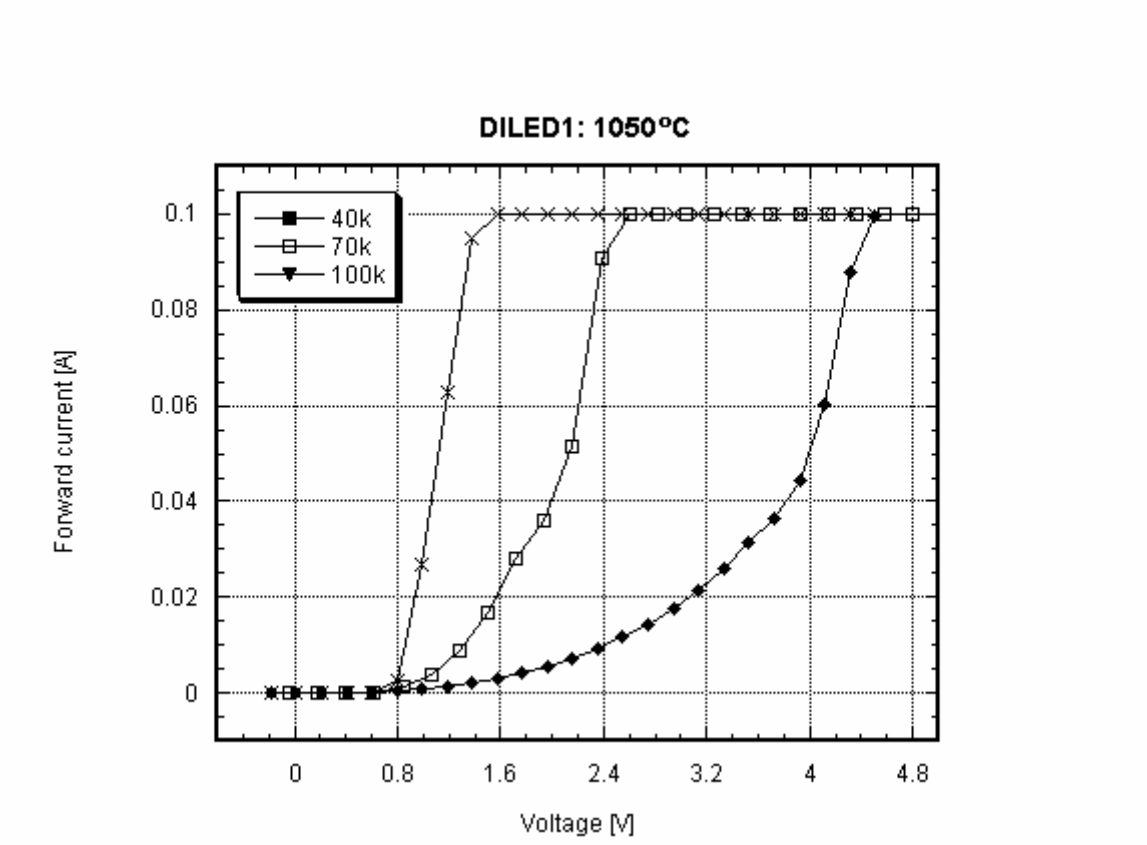


Figure 9-1: Increasing a-linearity with increasing implant energy.

In *6.1.2 Parameter extraction in the forward bias regime*, several mechanisms were described that cause junction behavior to deviate from ideal junction behavior. To derive the Ideal-diode-equation, 3 assumptions have been made:

- Negligible generation and recombination in the depletion region;
- No high-level injection;
- Negligible bulk resistance.

Only 1 mechanism causes linear behavior…bulk resistance. Both junction voltage V_j and bulk-resistance R_{BULK} were calculated assuming that only bulk resistance influenced the I-V characteristics in the forward regime. Because of the a-linearity in the forward I-V characteristics, the tabulated bulk resistance values are not correct values[5]. Although the exact values are not known, still a common known trend is visible:

[5] With recombination in the depletion region and high level injection included in the ideal-diode equation, it becomes very difficult, if not impossible, to rewrite the resulting diode equation in order to have voltage as function of current, see also 6.1.2 Parameter extraction in the forward bias regime.

Bulk resistance increases with increasing implant energy when the dose is not adjusted to compensate for the decreasing peak concentration with increasing implant energy, figure 9-2.

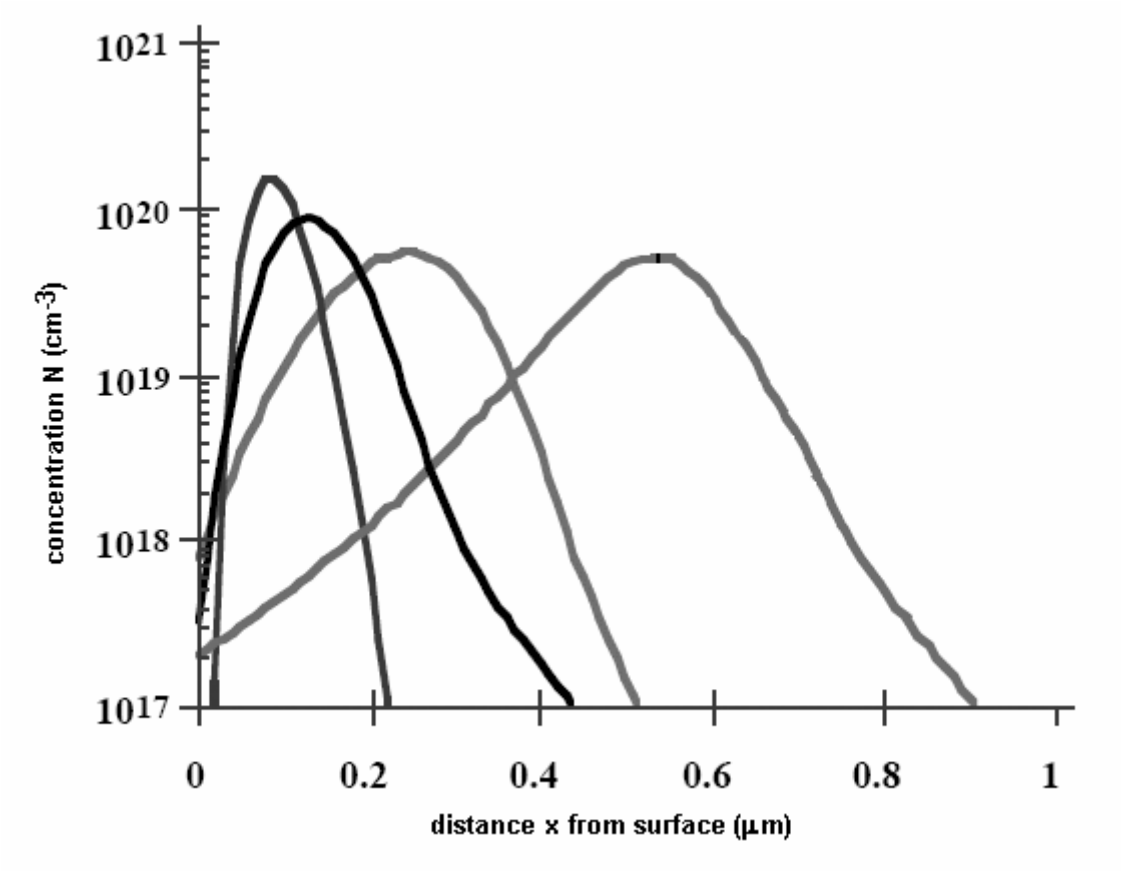


Figure 9-2: Increasing bulk resistance for increasing implant energy.

Not only the deeper 70 and 100keV DILED1 characteristics show a-linear behavior, but also the shallower 40keV implants, figure 9-3.

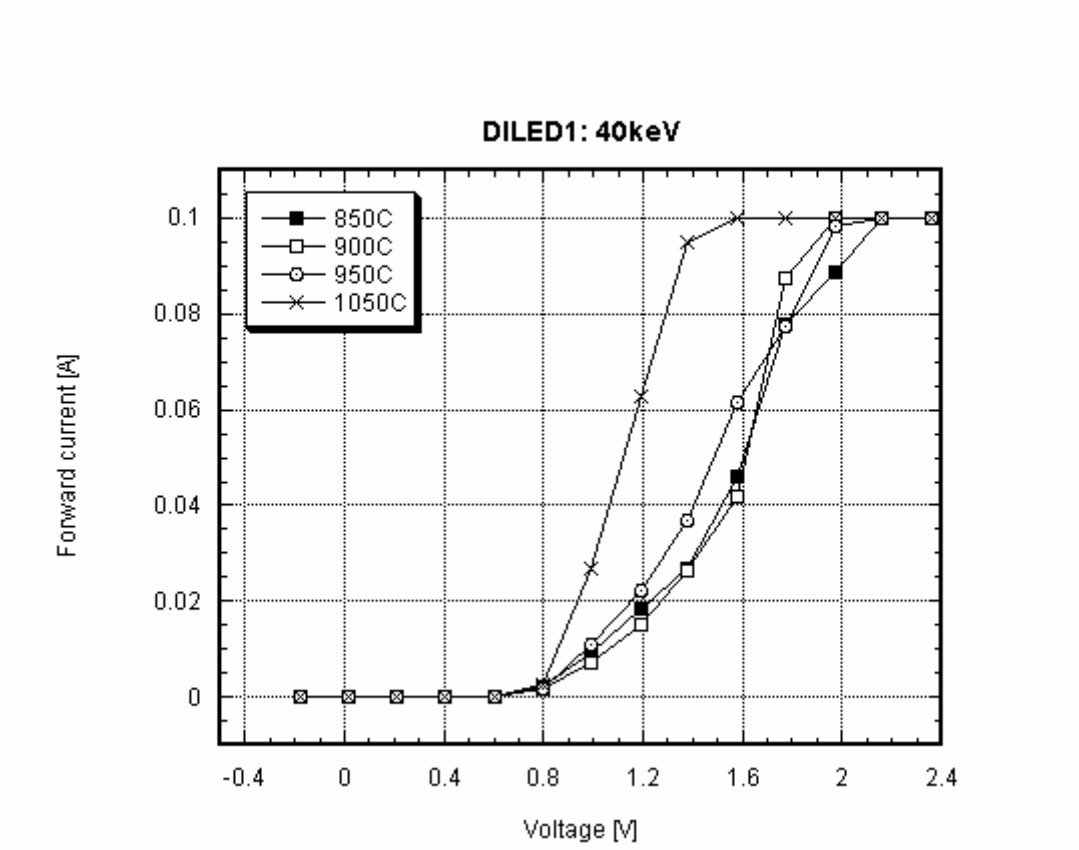


Figure 9-3: A-linearity throughout complete batch.

The total DILED1 batch consisted of 7 wafers, one wafer for each type of DILED1 device. Therefore throughout the complete batch, a-linearity in the I-V characteristics can be detected.

In chapter 8 *Measuring Light Emitting Diodes*, it was briefly mentioned that "Encountered difficulties while measuring are in appendix C". One such difficulty was that 50% of the DILED1 70keV & 1050°C type of devices and 100% of the 100keV & 1050°C type of devices required a breakdown in order to get contact with the underlying silicon.

There are 2 situations that require a breakdown:

- The 50nm Si_3N_4 layer has been plasma etched successfully to open the light emitting surface area. But the 25nm SiO_2 layer has been wet etched partially, figure 9-4;

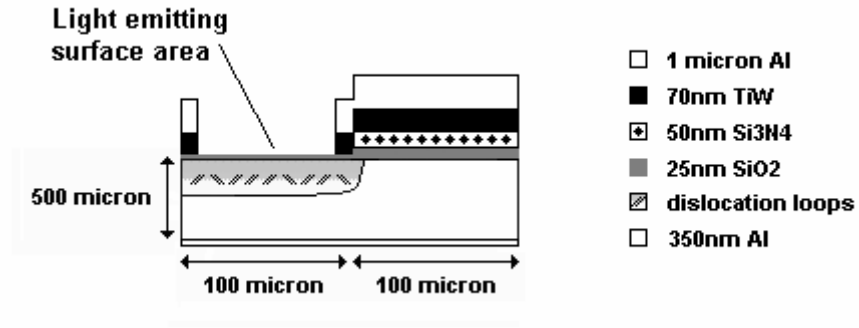


Figure 9-4: DILED1 70 & 100keV cross-section with SiO_2 film on light emitting surface area.

- The 50nm Si_3N_4 layer has **not** been plasma etched successfully. Consequently the underlying SiO_2 layer has not been wet etched during the SiO_2 etching process step in order to open the light emitting surface area, figure 9-5.

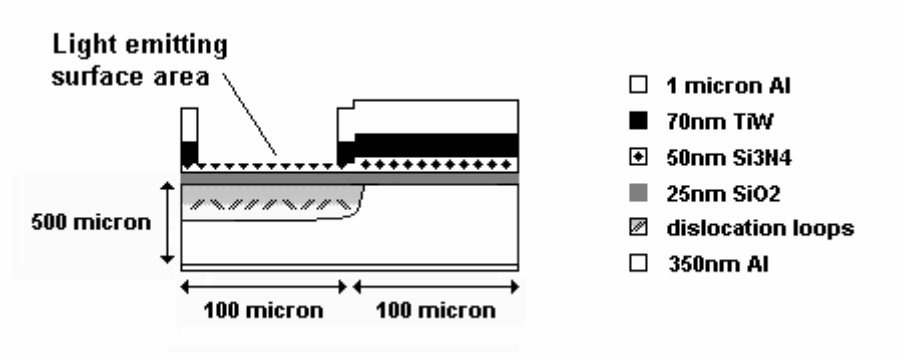


Figure 9-5: DILED1 70 & 100keV cross-section with SiO_2 and Si_3N_4 film on light emitting surface area.

Some properties of SiO_2 Si_3N_4 have been tabulated in table 9-2:

Table 9-2: Properties of SiO_2 and Si_3N_4.

Breakdown material	Dielectric strength	Breakdown voltage	Resistivity	Resistance
	$E_{BREAKDOWN}$	$V_{BREAKDOWN}$	ρ	R
	Vcm^{-1}	V	Ωcm^{-1}	Ω
25nm of SiO_2	$\sim 10^7$	~25V	10^{14}	2.5×10^8
50nm of Si_3N_4	$\sim 10^7$	~50V	$>10^{14}$	$>5\times10^8$

The measured breakdown voltage was between 5.5 – 7V, that is equivalent to 5.5 – 7nm material between the top contact and the underlying silicon. At first sight that would mean, an estimated 5.5 – 7nm SiO_2 has not been etched away.

In a nutshell, a break down is a forced local conduction of the dielectric material due to the applied high electric field. Carriers are forced to take part in this local conduction. Thermal runaway accompanies this conduction eventually leading to the local melting of the dielectric material and its surroundings, figure 9-6.

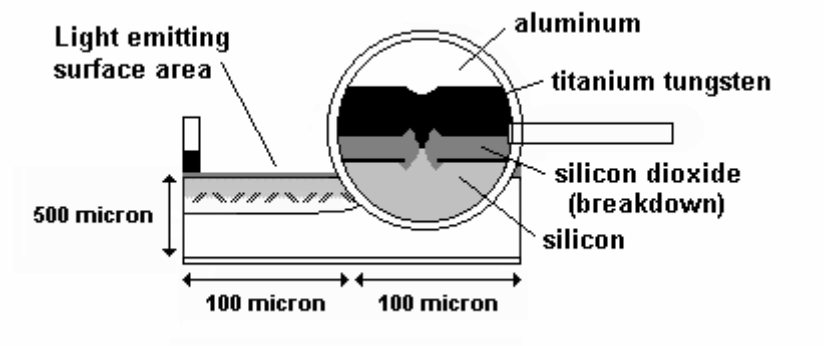


Figure 9-6: SiO_2 breakdown.

After a break down, dielectric material locally no longer obstructs the current path between the topside contact and the underlying silicon. It is needless to say that the resulting contact is poor of quality. Also the contact area is significantly reduced:

A qualitative and quantitative analysis will show that the a-linearity in the I-V characteristics of the 70 and 100keV devices is related to this poor quality reduced contact area after dielectric breakdown.

Qualitative analysis

For convenience figure 9-7 is shown again:

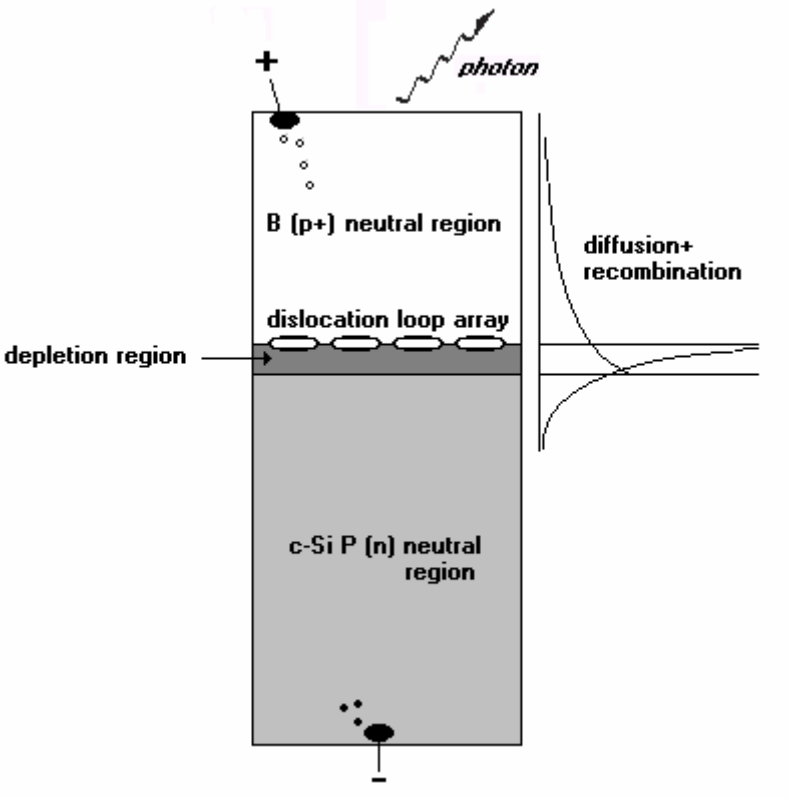


Figure 9-7: Position of dislocations at the edge of the depletion region.

Electrons and holes go *mutatis mutandis* the same way.

Electrons are injected at the negative backside contact. These majority carriers drift to the edge of the depletion region at the n-type neutral side. There they cross the depletion region to become minority carriers and diffuse into the p+ type neutral region. While they diffuse into the p+ type neutral region they recombine with the plentiful holes that are available. An equal number of holes must come from the positive contact to supply the holes that have recombined with the incoming electrons.

However due to the reduced quality and area of the positive contact, electrons are injected faster than holes can be supplied. From chapter *6.1.2 Parameter extraction in the forward bias regime* it was mentioned that "The high injection tends to change the charge neutrality of the neutral regions. At the p-side a negative charge will build up that will enhance the electric field across the junction. The applied forward voltage does not allow that. As a consequence the majority hole concentration increases to compensate for the high injection of electron minorities. In fact, majority and minority concentrations are nearly equal…and we have a situation as in the depletion region where both carrier concentrations differ from their equilibrium values."

The a-linearity increases for increasing implant energy. Thus the high injection effect becomes more prominent for increasing implant energy. A possible explanation for the increased a-linearity with increasing implant energy:

For increasing implant energy the overall boron concentration in the p+ neutral region decreases, figure 20. The boron dose is smeared out over a larger volume due to the increased implant depth. A decreased boron concentration means an increased bulk resistance. The increase in resistance makes it even more difficult for holes to be injected into the p+ type neutral region. High injection effect becomes more prominent.

Quantitative analysis

The high injection effect is represented by equation 9-1. Equation 9-1 equals equation 6-8 from *2.1 On the extraction of electrical parameters*.

Equation [9-1]

$$i_D = \frac{I}{1+\sqrt{\frac{I}{I_{kf}}}}[A]$$

The knee current I_{kf} is the current at which this high injection effect sets in. The I-V characteristic on a linear scale will roughly show quadratic behavior.

Until this far the forward characteristics have been presented and discussed. Now the reverse current characteristics will be presented and discussed, figures 9-8 and 9-9:

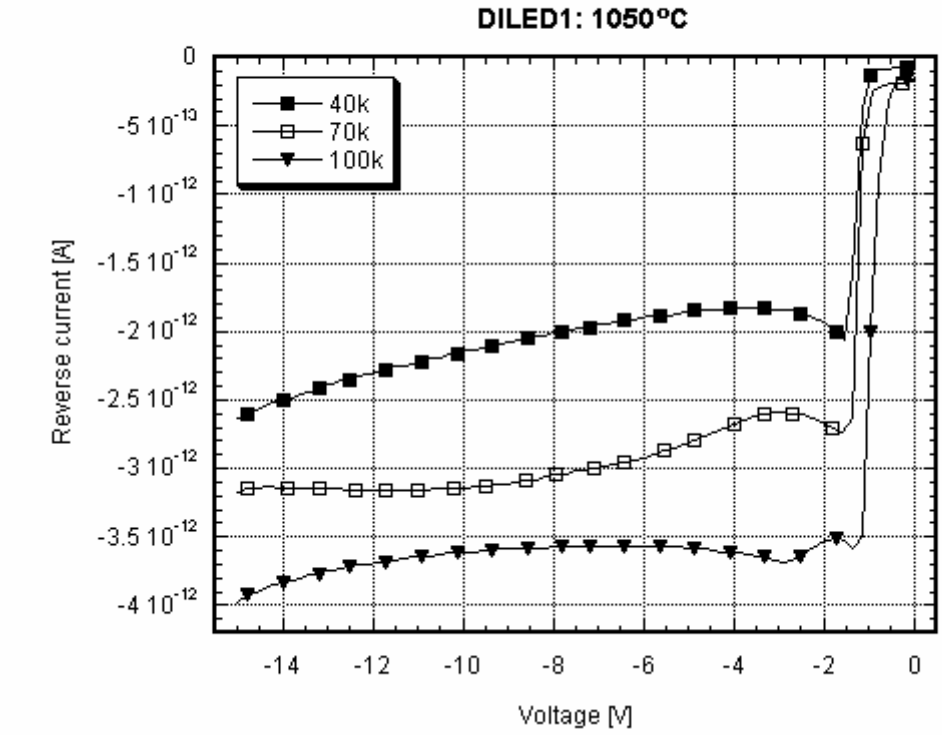


Figure 9-8: Increasing reverse current with increasing implant energy.

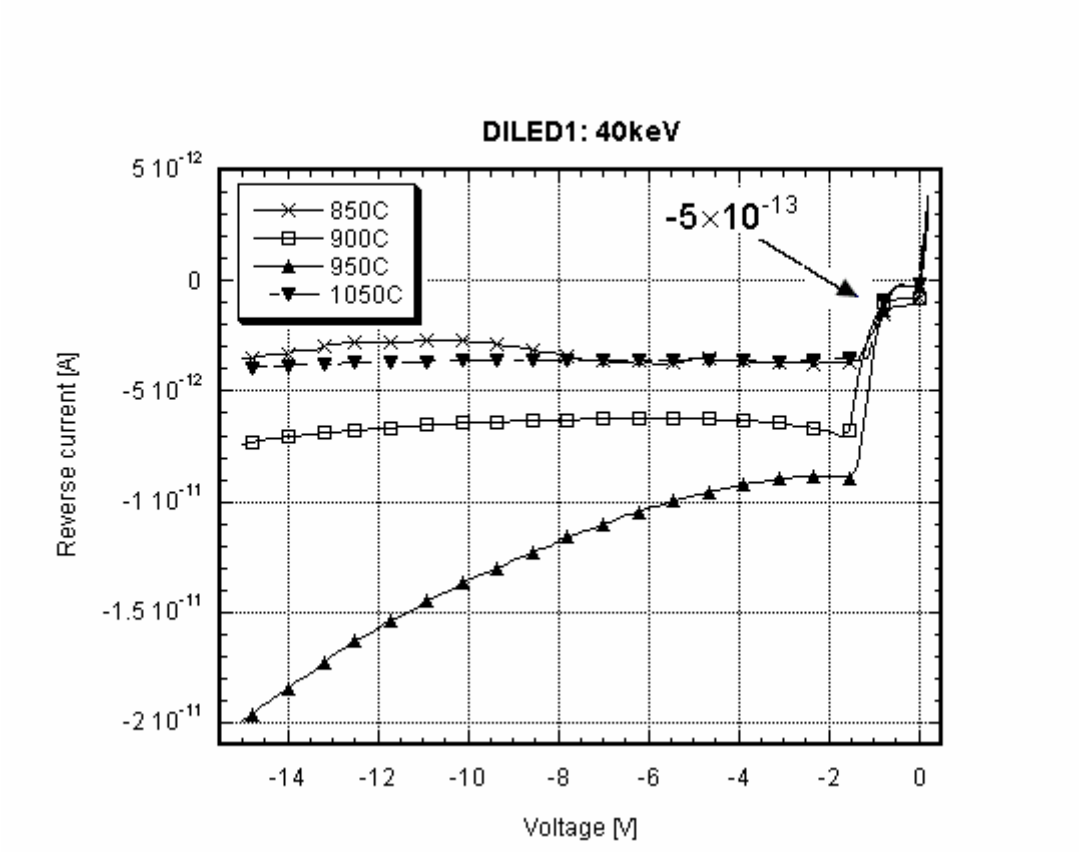


Figure 9-9: No direct relation between reverse current and annealing temperature.

Figure 9-8 shows that an increase in implant energy results in an increase in reverse current, when the peak concentration is not adjusted for different implant energies.

Figure 9-9 shows that, no direct relation between reverse current and annealing temperature exists.

For an ideal diode the negative reverse current is constant and equals the saturation current. Due to generation in the depletion region this behavior is absent in figure 9-9. Instead behavior like that has been depicted in figure 6-1, *6.1 On the extraction of electrical parameters*, can be observed. Notice the offset for a zero volt bias due to imperfect shielding of the probe station chamber. Notice also the inverted square-root behavior in reverse current. This behavior is linked to an increasing generation in the depletion region with increasing depletion layer width for increasing negative bias.

Summarizing DILED1 electrical results:

- The extracted diode parameters give a good indication for DILED1. The bulk resistance values are not correct values due to assumptions that have been made while deriving them. However one known trend is visible: bulk resistance is proportional to implant energy;
- The DILED1 parameters have been compared to find a correlation with optical parameters, but no trends were observed;
- The DILED1 current versus forward voltage characteristics show a-linear behavior, especially the deeper implants 70 and 100keV. The latter two have been assigned to high injection effect;
- The a-linearity becomes more prominent for higher implant energies, probably due to an increase in bulk resistance;
- The reverse current is proportional to implant energy;
- There is no direct relation between reverse current and annealing temperature.

9.1.2 DILED2

The derived parameters are:

- Photo current $I_{v=0}$
- Saturation current I_0
- Thermal voltage equivalent V_{th}
- Ideality factor m
- Junction voltage V_j
- Bulk resistance R_{BULK}

These parameters have been estimated in *6.1.3 Estimating junction parameters*, except for the photo current. For convenience the results are summarized:

- The saturation current between 9×10^{-17} and 1×10^{-15}A;
- The thermal voltage equivalent is 25.2mV;
- The ideality factor for an ideal diode is 1;
- The junction voltage must exceed the built-in voltage (also called onset voltage) of around 0.6V;
- The wafer resistance gives an estimation of the bulk resistance: 3.18 – 31.8Ω.

The derived parameters have been compared with the estimated values.

In general the extracted diode parameters give a good indication for DILED2.

DILED2 parameters, table 9-3:

Table 9-3: DILED2 electrical parameters.

DILED2	Photo current	Saturation current	Thermal voltage equivalent	Ideality factor	Junction voltage	Bulk resistance
	$I_{Va=0}$	I_0	V_{th}	m	V_j	R_{BULK}
	pA	fA	mV	-	mV	Ω
40keV & 950°C & $1.2x10^{15}$ cm^{-2}	-1.39	1.15	25.5	1.01	818	36.8
50keV & 950°C & $1.37x10^{15}$ cm^{-2}	-0.904	1.27	25.7	1.02	822	36.8
70keV & 950°C & $1.6x10^{15}$ cm^{-2}	-1.20	1.27	25.7	1.02	822	36.8
40keV & 1100°C & $1.2x10^{15}$ cm^{-2}	-1.98	7.35	27.5	1.09	832	36.7
50keV & 1100°C & $1.37x10^{15}$ cm^{-2}	-0.822	3.45	26.5	1.05	821	36.8
70keV & 1100°C & $1.6x10^{15}$ cm^{-2}	-0.713	2.56	26.2	1.04	820	34.9

The DILED2 parameters have been compared to find a correlation with optical parameters, but no trends were observed

Figures 9-10 and 9-11 are the I-V characteristics that represent DILED2.

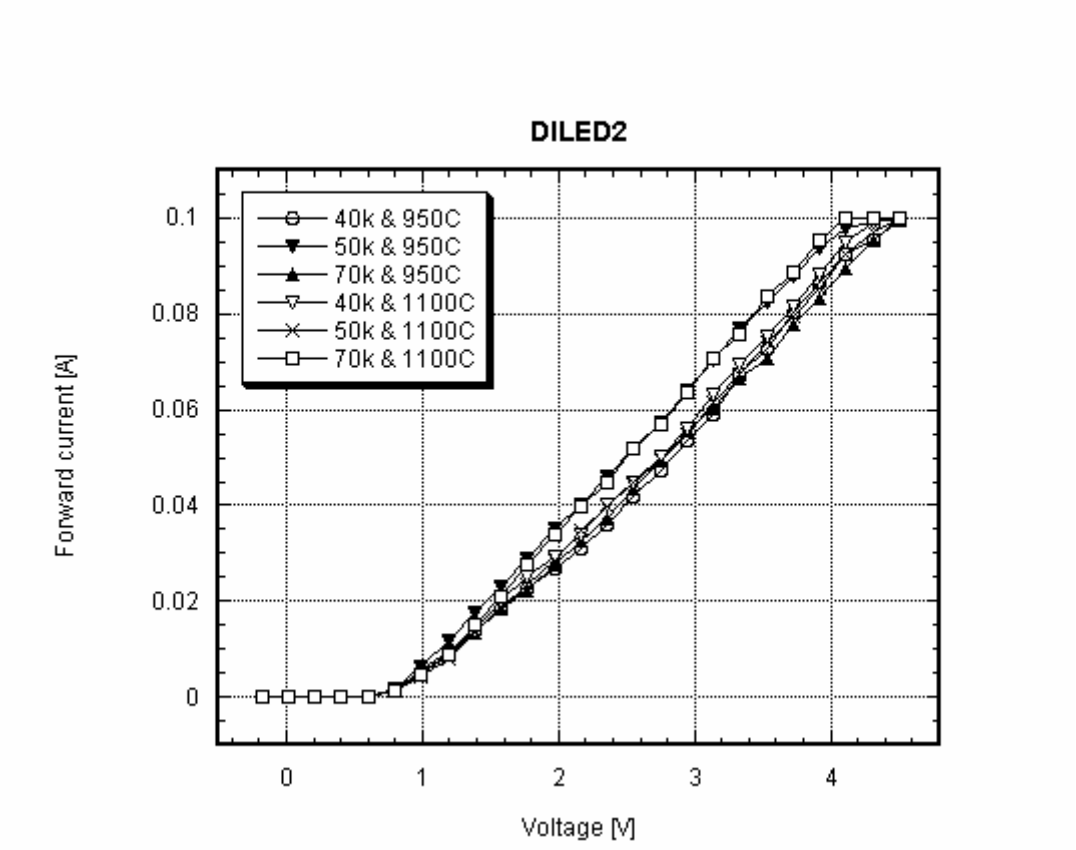


Figure 9-10: Absence of a-linearity.

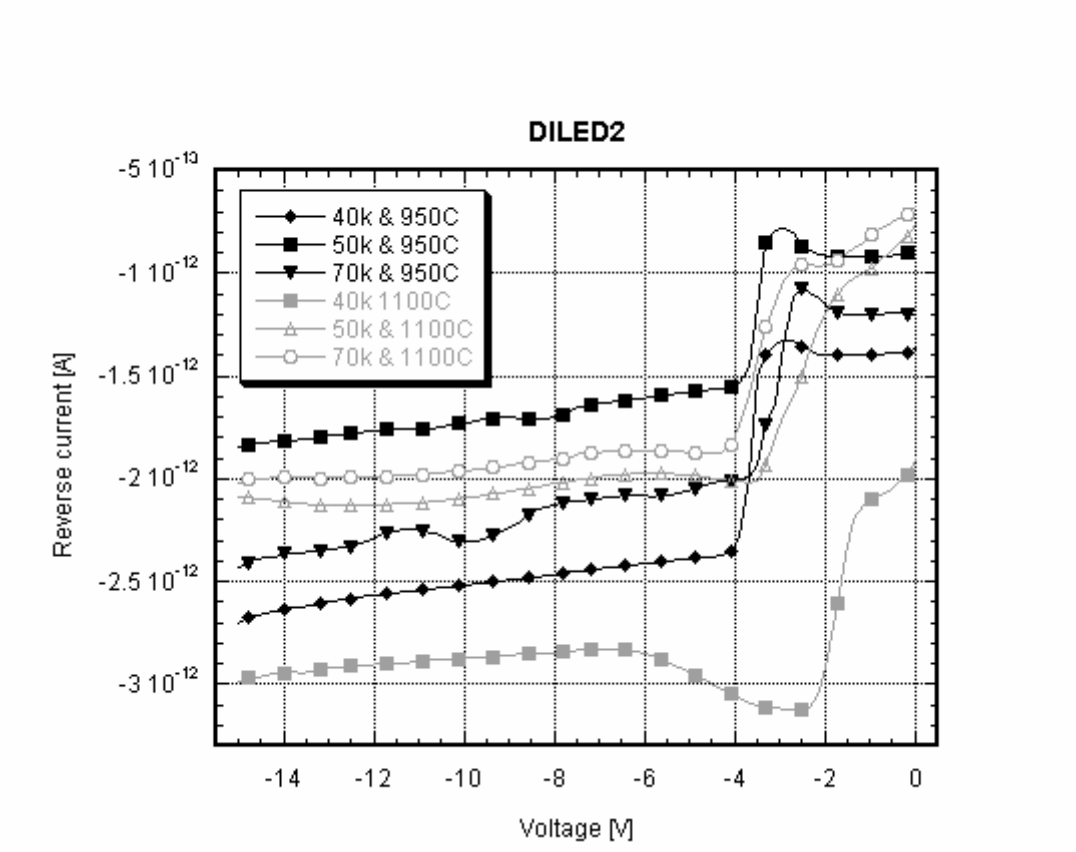


Figure 9-11: No direct relation between reverse current and both implant energy & annealing temperature.

From the table 9-3 and forward characteristic figure 9-10 the first thing that becomes clear is that due to the adjustment of the peak concentration, bulk resistance is no longer proportional to implant energy.

From figure 9-10 it is clear that the DILED2 forward characteristics show no a-linear behavior. The absence of a-linearity seems consistent with the analysis in *9.1.1 DILED1*, because DILED2 devices required no breakdown.

Figure 9-11 reveals 2 things. First of all there is no relation between reverse current and implant energy. Second of all there is no relation between reverse current and annealing temperature.

The analysis for the reverse bias regime of DILED2 devices is comparable to that of DILED1 devices, chapter *9.1.1 DILED1*.

Summarizing DILED2 electrical results:

- The extracted diode parameters give a good indication for DILED2;
- The DILED2 parameters have been compared to find a correlation with optical parameters, but no trends were observed;
- Due to the adjustment of the peak concentration bulk resistance is not proportional to implant energy;
- The DILED2 current versus forward voltage characteristics shows no a-linear behavior;
- The reverse current is not proportional to implant energy;
- There is no direct relation between reverse current and annealing temperature.

9.1.3 DIFLED

The derived parameters are:

- Photo current $I_{v=0}$
- Saturation current I_0
- Thermal voltage equivalent V_{th}
- Ideality factor m
- Junction voltage V_j
- Bulk resistance R_{BULK}

These parameters have been estimated in *6.1.3 Estimating junction parameters*, except for the photo current. For convenience the results are summarized:

- The saturation current between 9×10^{-17} and 1×10^{-15}A;
- The thermal voltage equivalent is 25.2mV;
- The ideality factor for an ideal diode is 1;
- The junction voltage must exceed the built-in voltage (also called onset voltage) of around 0.6V;
- The wafer resistance gives an estimation of the bulk resistance: 3.18 – 31.8Ω.

The DIFLED results deviate a lot from the estimated values, see table 9-4:

Table 9-4: DIFLED electrical parameters.

DIFLED	Photo current	Saturation current	Thermal voltage equivalent	Ideality factor	Junction voltage	Bulk resistance
	$I_{Va=0}$	I_0	V_{th}	m	V_j	R_{BULK}
	pA	pA	mV	-	mV	Ω
450keV	-19.8	37.8	39.9	1.58	866	52.5
200keV	-0.461	0.0127	28.1	1.12	834	52.9
200+450keV	-4.12	5.11	35.9	1.42	851	57.1
No	-0.281	0.0015	25.7	1.02	825	48.6
360keV	-1.33	0.566	32.8	1.30	849	67.1
260keV	X	X	X	X	X	X
360+260keV	-1.58	0.0513	30.3	1.20	857	79.0
No	-0.443	0.0015	25.7	1.02	825	59.2

The DIFLED parameters have been compared to find a correlation with optical parameters, but no trends were observed.

From table 9-4 it is clear that for single implants there is no relation between bulk resistance R_{BULK} and implant energy. Not so remarkable because DIFLED junctions have been formed by diffusion instead of implantation.

Due to the high implant energies, all DILFLED parameters are elevated compared to their estimated values. The smallest silicon implant of 200keV through a 3.5μm masking photo resist layer, equals the largest DILED1 boron implant of 100keV (standard implant tables).

Prove for the impact that the high energies have, are the large reverse currents, figure 9-12. DILED1 and DILED2 devices have reverse currents in the order of 10^{-12}A.

Reverse characteristics figure 9-13 also reveals that for single implants reverse current is proportional to implant energy.

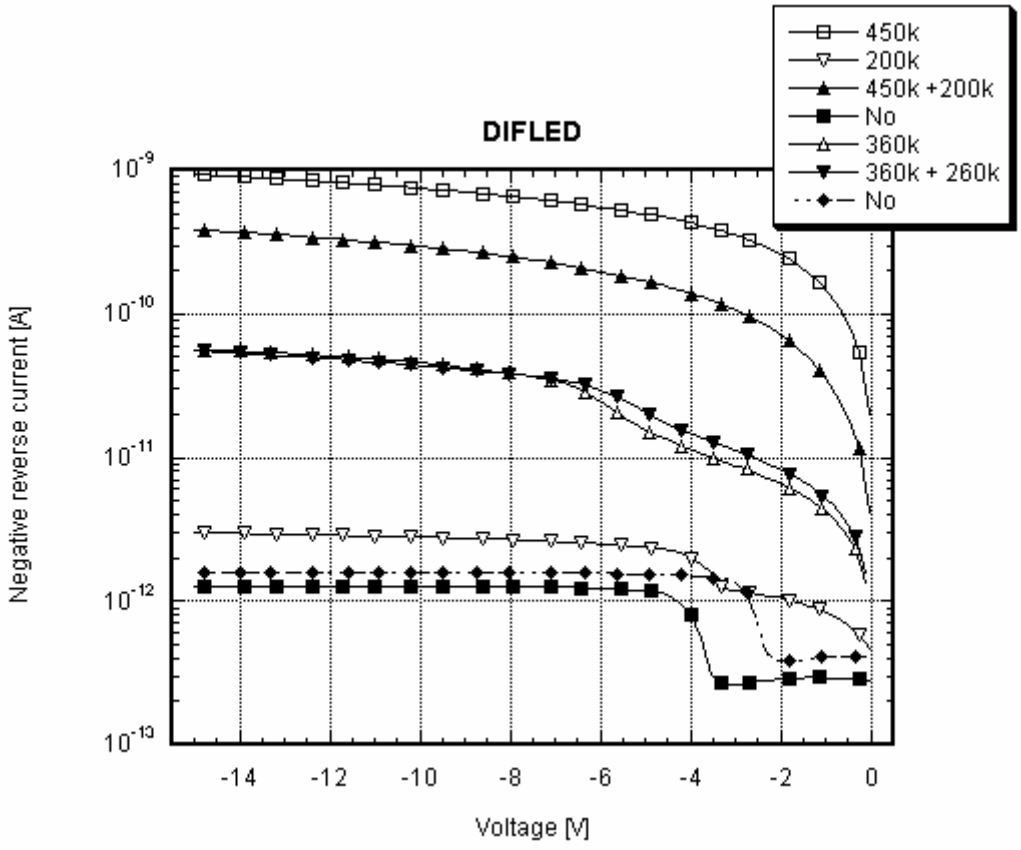


Figure 9-12: Large DIFLED reverse currents compared to DILED1 and DILED2 reverse currents.

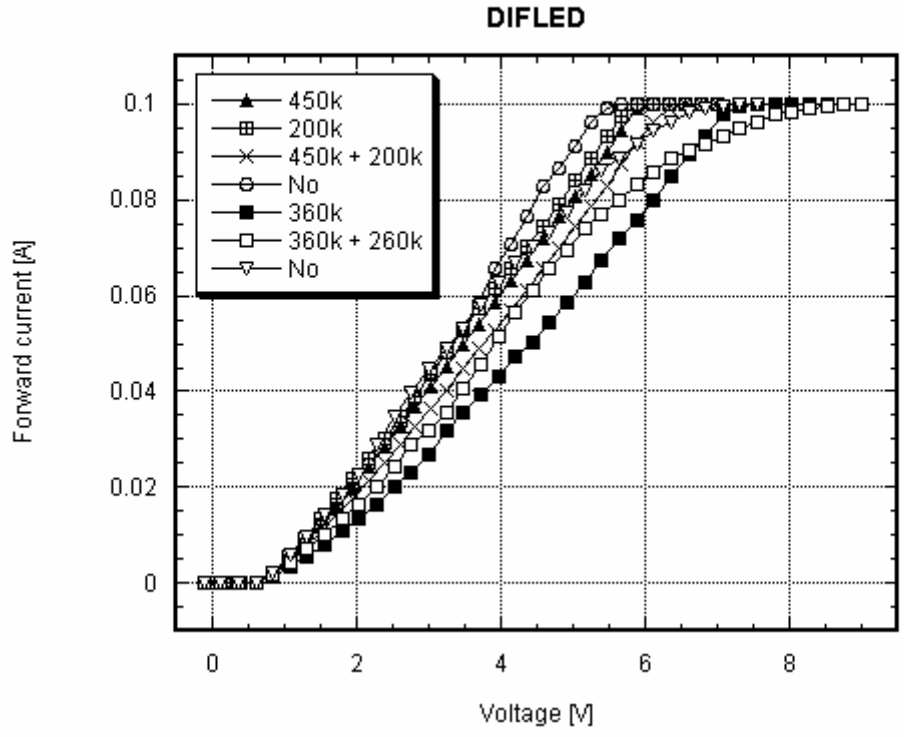


Figure 9-13: DIFLED absence of a-linearity.

Figure 9-13 shows that that all forward characteristics lack a-linearity. That seems consistent with the analysis in *9.1.1 DILED1,* because DIFLED devices required no breakdown and therefore high injection effect is absent.

The analysis for the reverse bias regime of DIFLED devices is comparable to that of DILED1 devices, chapter *9.1.1 DILED1*.

Summarizing DIFLED electrical results:

- All extracted diode parameters are increased, probably due to the high implant energies. Prove for the effect that high implant energies have upon the I-V characteristics are the high revere currents;
- The DIFLED parameters have been compared to find a correlation with optical parameters, but no trends were observed;
- The DIFLED current versus forward voltage characteristics show no a-linear behavior;
- For single implants reverse current is proportional to implant energy.

9.2 Optical parameters

Before drawing conclusions some remarks have to be made:

- All data points have error-bars. Only a few are visible, particularly for large light intensity values. The average deviation in percentage is 4.2%;
- All optical data is based upon the tables in *Appendix G – Measurement results, optical parameters*;
- There was a DILED1 batch, a DILED2 batch and DIFLED batch.

9.2.1 Light intensity versus annealing temperature

Figure 9-14 shows light intensity as function of annealing temperature:

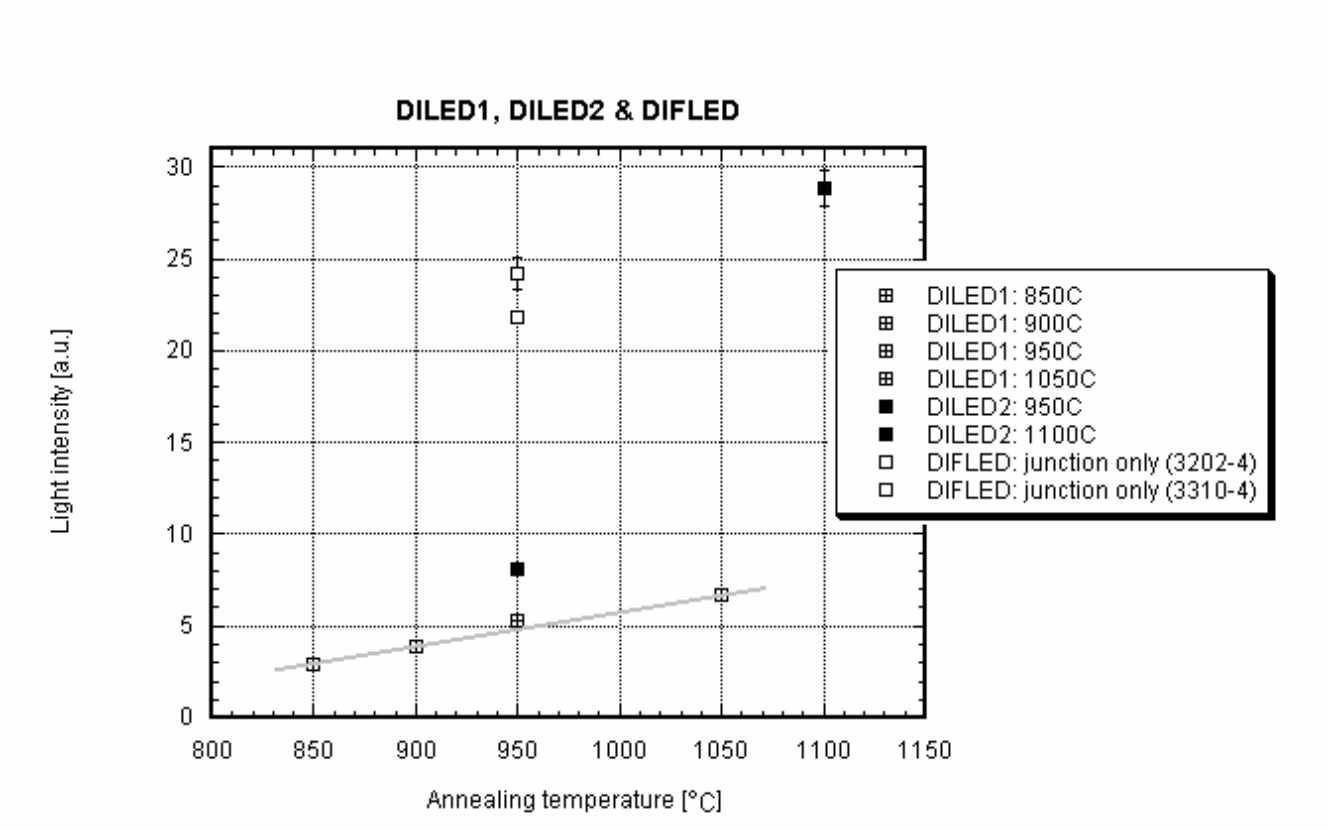


Figure 9-14: Light intensity as function of annealing temperature.

From figure 9-14, 5 things become clear:

- For DILED1 annealed at 850°C light intensity is 2.93(a.u.). For 850 – 1050°C light intensity of DILED1 increases with a factor of ~2.3. Thus the change in light intensity is ~0.6 per 50°C;
- At 950°C light intensity of DILED1 is 5.3 (a.u.) and the light intensity of DILED2 8.1(a.u.). Light intensity differs by a factor 1.5. The implant dose of DILED1 is 1.0 x $10^{15}cm^{-3}$. The implant dose of DILED2 is 1.2x $10^{15}cm^{-3}$;
- Within the annealing temperature range of 850 – 1100°C, light intensity is maximum for devices annealed at 1100°C. For a 40keV DILED2 annealed at 1100°C light intensity is maximum with a value of 28.8(a.u.);
- The change in light intensity from 1050 to 1100°C is far more than the change in light intensity between 850 – 1050°C. Light intensity increases with a factor estimated between 4.3 and 6.9 per 50°C;
- At 950°C "DIFLED: junction only" light intensity is much higher than both DILED1 and DILED2 light intensity. Light intensity of DILED1 is 5.29(a.u.). Light intensity of DILED2 is 8.11(a.u.). Light intensity of "DIFLED: junction only (3202-4)" is 21.8(a.u.) and light intensity of "DIFLED: junction only (3310-4)" is 24.2(a.u.).

(1) For DILED1 annealed at 850°C light intensity is 2.93(a.u.). For 850 – 1050°C light intensity of DILED1 increases with a factor of ~2.3. Thus the change in light intensity is ~0.6 per 50°C.

According to theory the dislocation loop density is approximately constant between 850 – 1050°. Some small loops disappear when they are eaten by bigger loops and at the same time interstitials are lost by dislocation loops.

(2) At 950°C light intensity of DILED1 is 5.3(a.u.) and the light intensity of DILED2 is 8.1(a.u.). Light intensity differs by a factor 1.5. The implant dose of DILED1 is 1.0x$10^{15}cm^{-3}$. The implant dose of DILED2 is 1.2x $10^{15}cm^{-3}$.

Light intensity differs by a factor 1.5. Note that DILED1 and DILED2 devices belonged to different batches.

According to K. S. Jones[2] et. al. the amount of interstials gettered by dislocation loops is proportional to the implant dose, figure 9-15:

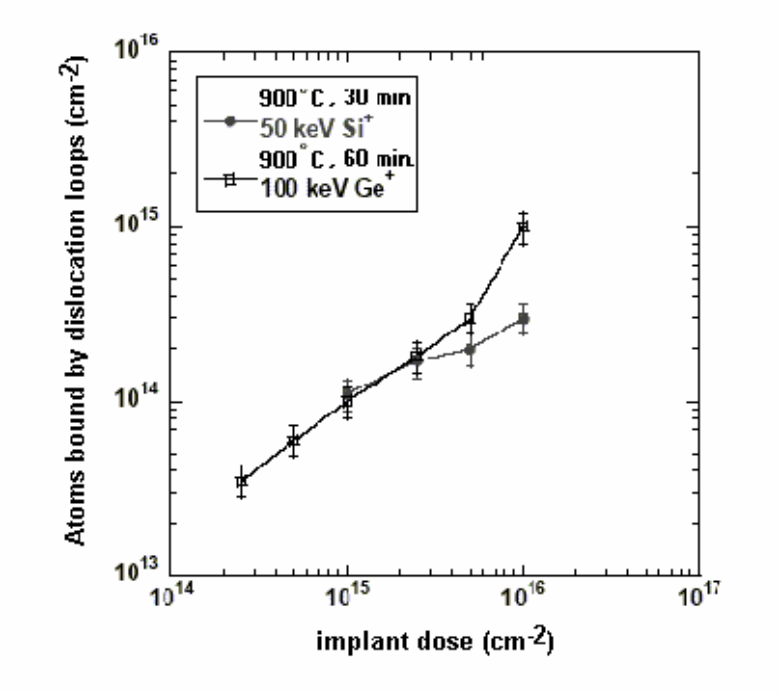


Figure 9-15: Bound interstitials versus implant dose (increase for heavier species).

Sun[14] et. al. showed that electro-luminescence is proportional to implant dose, figure 9-16. This group prepared silicon p-n diodes by b+ implantation at 25keV followed by an anneal at 1050°C for 20 minutes.

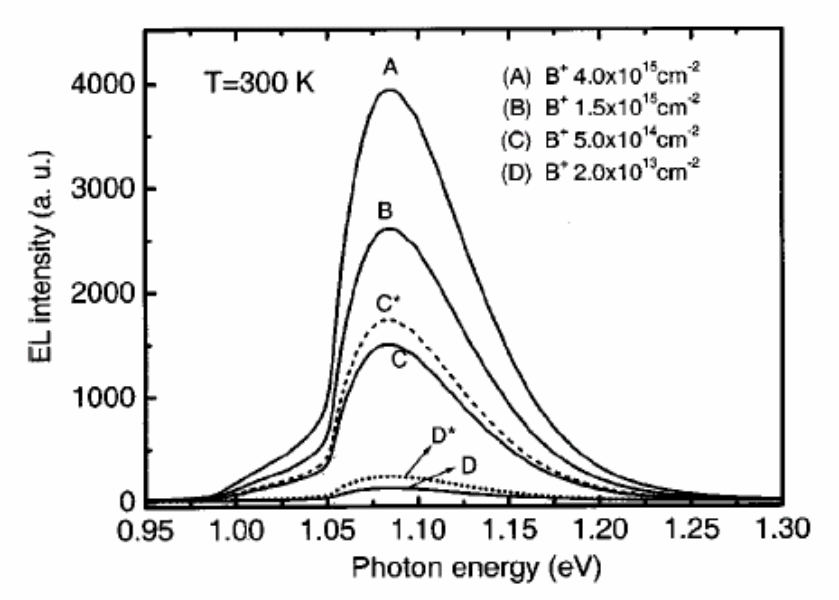


Figure 9-16: EL intensity for increasing boron implant doses.

(3) Within the annealing temperature range of 850 – 1100°C, light intensity is maximum for devices annealed at 1100°C. For a 40keV DILED2 annealed at 1100°C light intensity is maximum with a value of 28.8(a.u.).

Sobolevs[6] who annealed up to 1200°C reports: "The efficiency increases monotonically with temperature, achieves its maximum value ~0.4% after annealing at 1100°C and decreases after T_{ann} = 1200°C. This value is much larger than η_{int} at room temperature for all other types of LED's based on c-Si…"

η_{int} Is the internal quantum efficiency.

In this article Sobolev[11] et. al. argue that this optimum light intensity occurs for annealing budgets that must result in the dissolution of loops. Therefore the remaining implant damage after Solid Phase Epitaxy re-growth and dissolution of the loops might be responsible for the light emission, not the loops themselves.

(4) The change in light intensity from 1050 to 1100°C is far more than the change in light intensity between 850 – 1050°C. Light intensity increases with a factor estimated between 2.7 and 4.3 per 50°C.

The dose adjustment for the DILED2 1100°C devices is this time $1.6x10^{15}cm^{-3}$. We can't ignore the fact that light intensity is proportional to implant dose. Therefore it is impossible to mention the exact change in light intensity from 1050 to 1100°C. Let's look at two extreme cases:

✓ The difference in implant dose is ignored, because light intensity is not related to implant dose: then from 1050 – 1100°C light intensity increases with a factor ~4.3. Thus the change in light intensity is 4.3 per 50°C;

✓ The difference in implant dose is not ignored. In fact we believe that light intensity is directly proportional to implant dose: then from 1050 – 1100°C light intensity increases with a factor ~4.3*1.6 is ~6.9. In figure 32 the 1050°C point is shifted down to adjust the dose to $1.0x10^{15}cm^{-3}$ or the 1100°C point is shifted up to adjust the dose to $1.6x10^{15}cm^{-3}$. Thus the overall change in light intensity is ~6.9 per 50°C.

(5) At 950°C "DIFLED: junction only" light intensity is much higher than both DILED1 and DILED2 light intensity. Light intensity of DILED1 is 5.29(a.u.). Light intensity of DILED2 is 8.11(a.u.). Light intensity of "DIFLED: junction only (3202-4)" is 21.8(a.u.) and light intensity of "DIFLED: junction only (3310-4)" is 24.2(a.u.).

From literature it is not at all clear whether light intensity is really enhanced by dislocation engineering. For a certain annealing temperature light intensity shows a maximum in a temperature range 700 – 1200°C, but is it really enhanced?

The "DIFLED: junction only" devices were used as reference LED's. The junction formation by diffusion reduces the amount of damage to the lattice that comes along with implantation. Less Frenkel-pairs are generated to support the formation of dislocation loops. Therefore the density of dislocation loops is reduced.

The information concerning dislocation loop densities became available through extensive mail correspondence with the first author of references 27 and 28 in "part I, Literature report", L. Fedina.

Figure 9-17 is a plan-view TEM image of a p-n junction in silicon created by thermal diffusion of boron atoms to a depth of about 2μm. To reach the bulk boron concentration of about 1x20 cm^{-3} at a depth of 1,5 – 2μm, annealing temperatures of 1150°C for 1 – 2hours are necessary. The diffusion constant complicates calculating in advance the exact dose necessary to obtain a peak concentration of 1x20 cm^{-3}.

The dark lines represent a dislocation network.

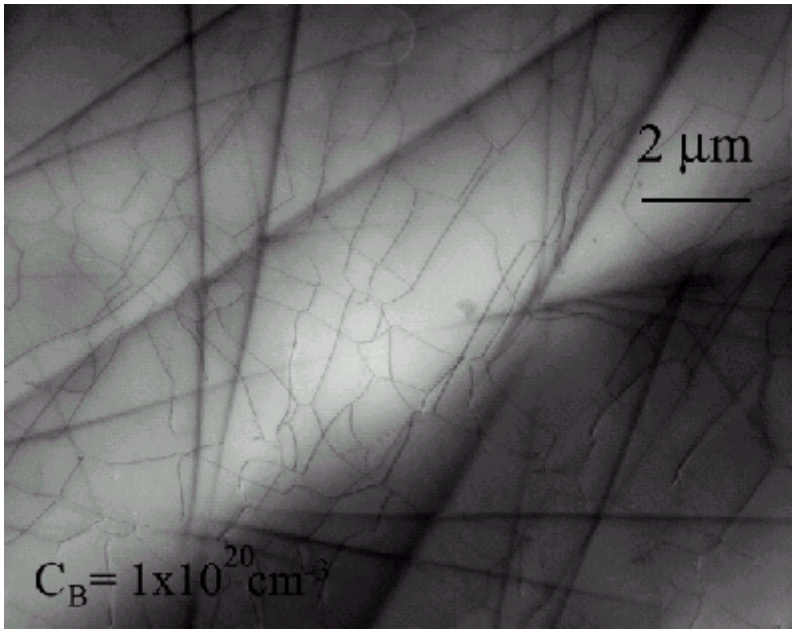


Figure 9-17: Dislocation network in thermally diffused silicon p-n junction.

The concentration of boron atoms measured by **S**econdary **I**on **M**ass **S**pectrometry (**SIMS**) is 1x10E20cm^{-3}. The density of dislocations is about 2x10^8cm^{-2}.The local dislocation density varies between 2x10^7 and 10^9cm^{-2}.

While implantation of 1×10^{15}cm^{-2} boron atoms followed by a 1000°C anneal introduces dislocation loop densities varying between 1×10^9 – 1×10^{10}cm^{-2}. Thus the "DIFLED: junction only" loop density is on average 100 times smaller.

1st and 5th points suggest that light intensity is inversely proportional to dislocation loop density.

.

9.2.2 Light intensity versus implant energy

Figure 9-18 shows light intensity as function of implant energy:

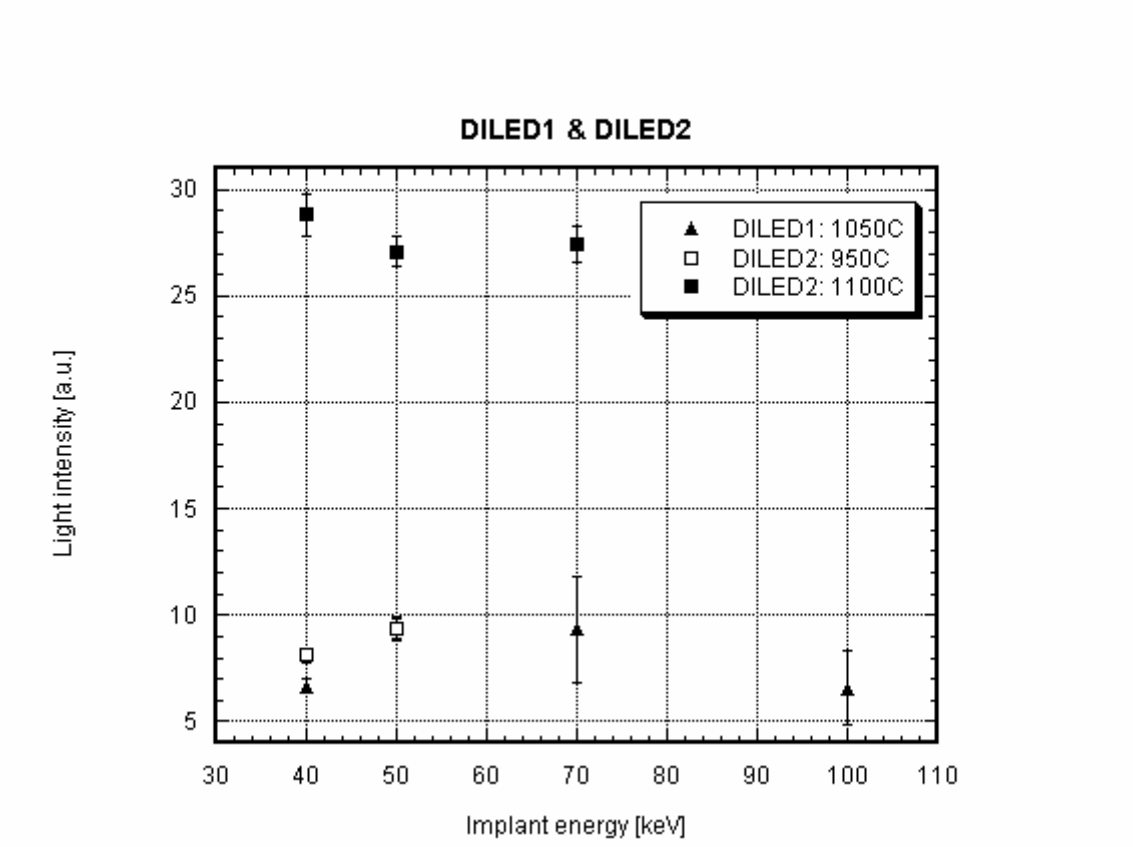


Figure 9-18: Light intensity as function of implant energy.

From figure 9-18 two things are worth mentioning:

- Light intensity is weakly dependent upon the energy range 40 to 100keV;
- The error bars of the 70 and 100keV data indicate a peak deviation of respectively 26.9 and 26.7%. With an average peak deviation of 4.2%, these peak deviation are 6.3 times larger than normal. A separate section *9.2.4 Light intensity for DILED1 70 and 100keV devices*, will be dedicated to 70 and 100keV DILED1 devices.

(1) Lourenco[45] et al. conducted partially identical measurements, table 9-5:

Table 9-5: Range of implant energies as has been used by Lourenco.

Implant Energy	Implant dose	Annealing temperature	Annealing time
E	Q	T	t
keV	boron atoms cm^{-2}	°C	minutes
20	7.6×10^{14}	950	20
30	1×10^{15}	950	20
40	1.2×10^{11}	950	20
50	1.37×10^{11}	950	20
70	1.6×10^{11}	950	20

This group concluded:

"Although the strongest EL was obtained from devices fabricated by a 30keV boron implantation, no specific trend on the EL integrated intensity as a function of implant energy was observed, thus suggesting that the electroluminescence is weakly dependent upon the energy range…"

Due to the large spread in light intensity values for the DILED1 70 and 100keV data it is impossible to draw a conclusion that stands on its own.

9.2.3 Light intensity for single, double or no silicon implants in boron diffused junction

Figure 9-19 shows light intensity for single, double or no implantation:

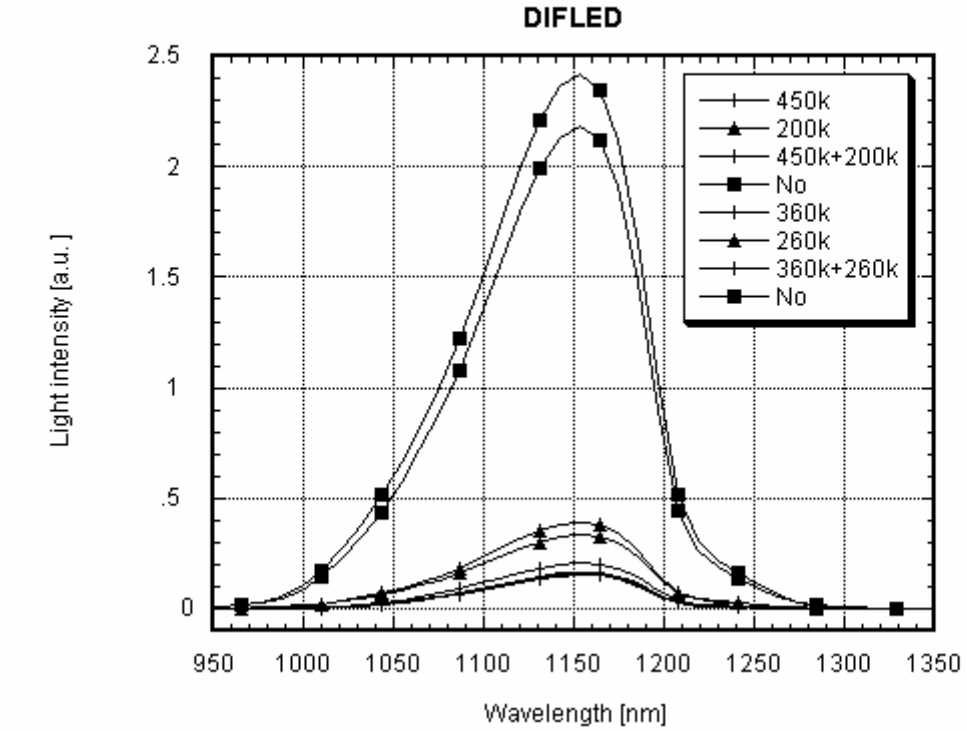


Figure 9-19: Light intensity as function of single, double or no silicon implants in boron diffused junction.

Three light intensity groups are distinguishable in figure 9-19:

- Double implants and deep single implant (450k, 450 & 200k, 360k, 360 & 260k);
- Shallow single implants (200k, 260k);
- No implants (boron diffusion).

(1) Double implants and deep single implant (450k, 450 & 200k, 360k, 360 & 260k)

The common factor for both implants is the deep implant. This deep implant depth exceeds the depletion layer edge nearest to the surface. The dislocation loop arrays are produced in the n-type region.

(2) Shallow single implants (200k, 260k);

The resulting dislocation loop arrays are situated at the edge of the depletion layer in the p-type region.

(3) No implants.

See 9.2.1 Light intensity versus annealing temperature, point 5.

9.2.4 Light intensity for DILED1 70 & 100keV devices

In *9.1.1 DILED1* the forward I-V characteristics were presented and discussed. It was concluded that due to incomplete etching of the SiO_2 or Si_3N_4 layers these characteristics showed a-linear behavior. The a-linearity was assigned to high injection effect. A quick calculation showed that after etching, a dielectric layer in the order of 5 – 7nm on top of the silicon surface should have remained.

In *9.2.2 Light intensity versus implant energy* we noticed that the error bars of the 70 and 100keV optical data indicated a peak deviation of respectively 26.9 and 26.7%. With an average peak deviation of 4.2%, these peak deviations are 6.3 times larger than normal.

Thus the electrical results pointed in the direction of a remaining estimated 5 – 7nm SiO_2 after wet etching. However in this section it shown that that conclusion might not be so obvious with respect to the optical results.

Figures 9-20 and 9-21 show the deviation in peak intensity for the 70 and 100keV devices:

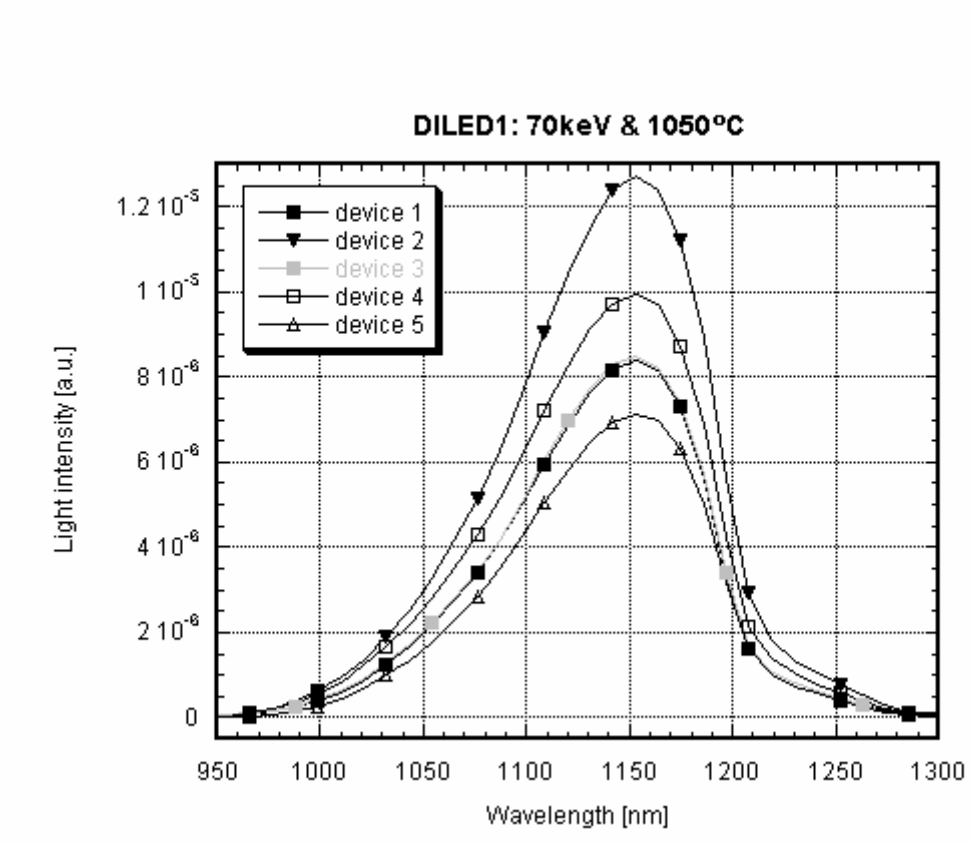


Figure 9-20: Standard deviation peak intensity for 70keV DILED1 devices

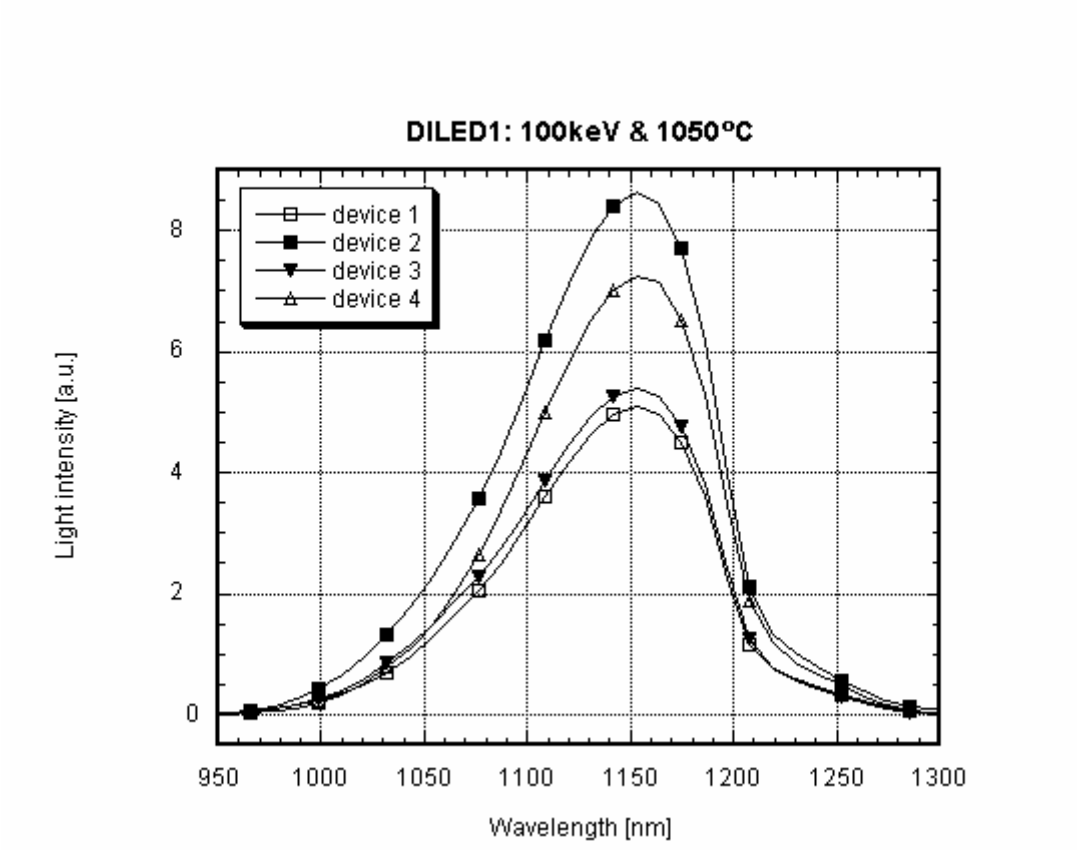


Figure 9-21: Standard deviation peak intensity for 100keV DILED1 devices.

Groups of neighboring devices have been measured, figure 9-22. Thus there is a huge spread in light intensity even for neighboring devices! Notice that some light intensity curves are almost identical, both for the 70 and 100keV devices.

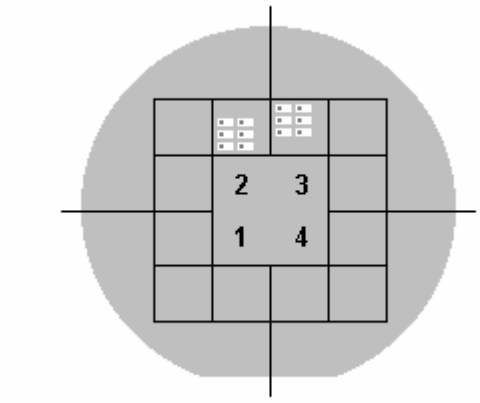


Figure 9-22: Measured groups of neighboring devices.

In *9.1.1 DILED1* it was stated that there are 2 situations that required a breakdown:

- The 50nm Si_3N_4 layer has been plasma etched successfully to open the light emitting surface area. But the 25nm SiO_2 layer has been wet etched partially;
- The 50nm Si_3N_4 layer has **not** been plasma etched successfully. Consequently the underlying SiO_2 layer has not been wet etched during the SiO_2 etching process step in order to open the light emitting surface area.

Light is generated in silicon (hopefully near the dislocation loops). It is collected at the front side i.e. at the Si/SiO_2 interface. At this interface a fraction of the incoming light is reflected, figure 9-23.

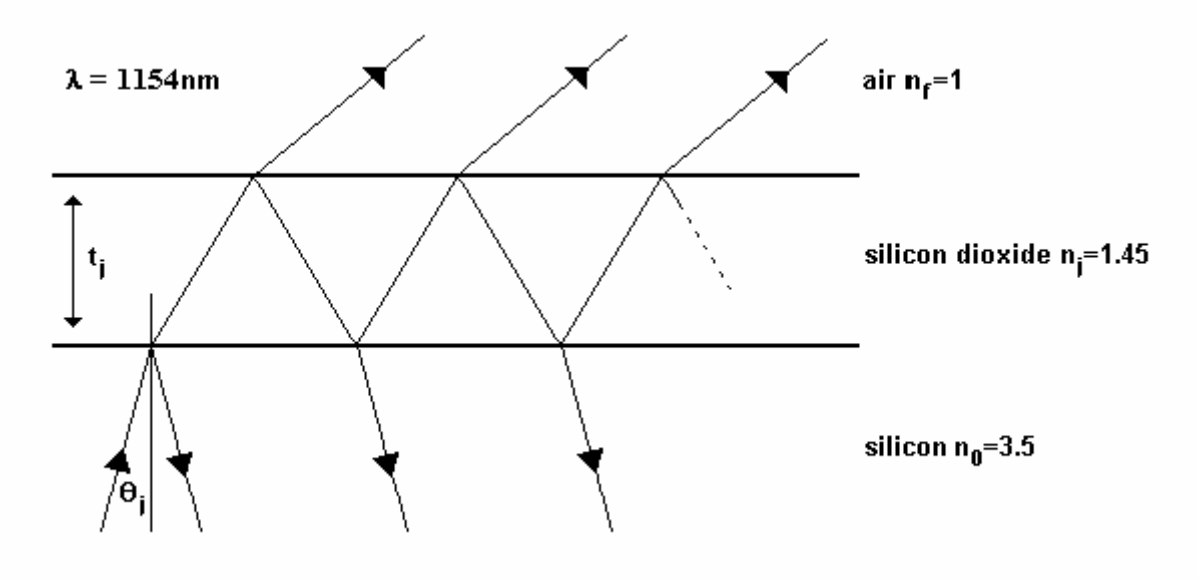


Figure 9-23: Multiple reflections at interfaces.

This reflected fraction depends upon the thickness of the oxide layer. For a quarter-wavelength thickness reflections are minimized. For zero thickness reflection is maximized. This maximum equals the reflection at the Si/vacuum interface. For multiple layers, as is the case when the Si_3N_4 layer has not been etched completely, reflections occur at each interface.

The text below concerning the derivation of an expression for reflectivity is a summary of *chapter 8.6 Multiple-layer Thin film from Contemporary optics for scientists & engineers*.[48]

In 1937 Rouard discovered that a multi layer-film could be analyzed by representing each layer by a 2×2 matrix M_j which has the form:

Equation [9-2]

$$M_j = \begin{pmatrix} \cos(\delta_j) & \dfrac{i\sin(\delta_j)}{n_j} \\ in_j \sin(\delta_j) & \cos(\delta_j) \end{pmatrix}$$

The phase shift has been defined as:

Equation [9-3]

$$\delta_j = \frac{2\Pi}{\lambda} n_j t_j \cos(\theta_j)[rad]$$

θ_j is the angle of incidence with respect to a plane perpendicular to the interface. The thickness of a layer is t_j [m] and the refractive index at a certain wavelength λ [m] is n_j.

The effect of a combination of layers is the product of the matrices representing each layer. Special matrices are:

The media that contain the light source is represented by:

Equation [9-4]

$$\begin{pmatrix} n_0 & -1 \\ n_0 & 1 \end{pmatrix},$$

and the final layer of interest to calculate the overall reflectivity *R* is represented by:

Equation [9-5]

$$\begin{pmatrix} 1 \\ n_f \end{pmatrix}$$

The reflectivity of the thin film combination is given by:

Equation [9-6]

$$R = \left|\frac{a}{b}\right|^2 [-]$$

where *a* and *b* are obtained from:

Equation [9-7]

$$\begin{pmatrix} a \\ b \end{pmatrix} = \begin{pmatrix} n_0 & -1 \\ n_0 & 1 \end{pmatrix} \begin{pmatrix} \cos(\delta_j) & \frac{i\sin(\delta_j)}{n_j} \\ in_j \sin(\delta_j) & \cos(\delta_j) \end{pmatrix} \begin{pmatrix} 1 \\ n_f \end{pmatrix}$$

By using the expression for the reflectivity of a thin film combination, equation 9-6, the effect of both the incomplete etch of the SiO_2 layer and SiO_2/Si_3N_4 multiple layers is examined. Is it possible that due to reflections, light intensity changes by a factor of 26.8% within a layer thickness…?

Table 9-6 summarizes the refractive indices necessary for the calculation of the reflectivity:

Table 9-6: Refractive indices at 1154nm wavelength[44].

Refractive index at 1154nm	Refractive index
	n
	–
silicon	3.5
silicon dioxide	1.45
silicon nitride	2.0
air	1

Figure 9-24 shows the effect of variations in the SiO_2 layer thickness and angle of incidence upon the calculated reflectivity:

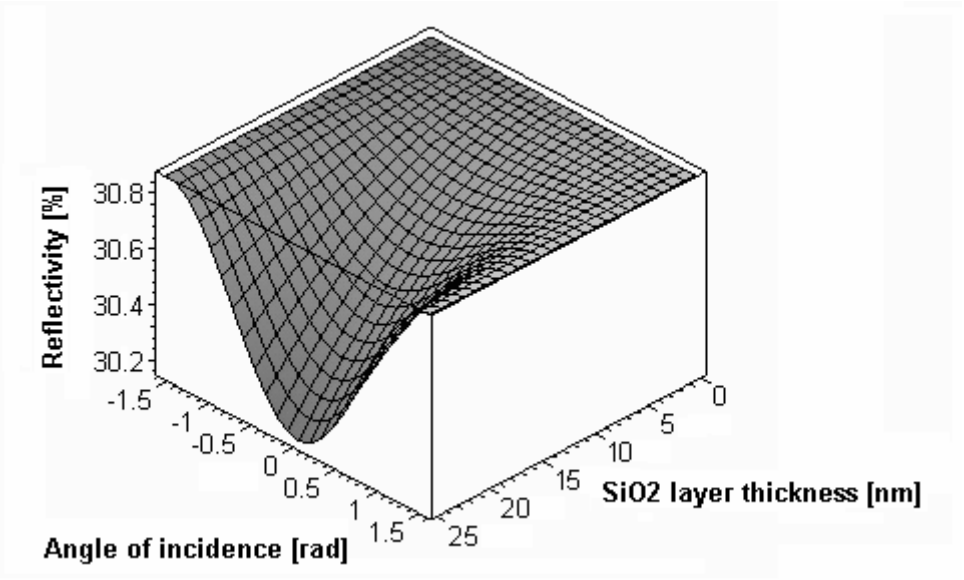


Figure 9-24: Reflectivity at Si/SiO_2 interface as function of angle of incidence and SiO_2 layer thickness.

It is clear that within a SiO_2 layer thickness reflections are not responsible for the high deviation in peak intensity.

Figure 9-25 shows the effect of variations in layer thickness of the SiO_2 and Si_3N_4 layer upon the calculated reflectivity:

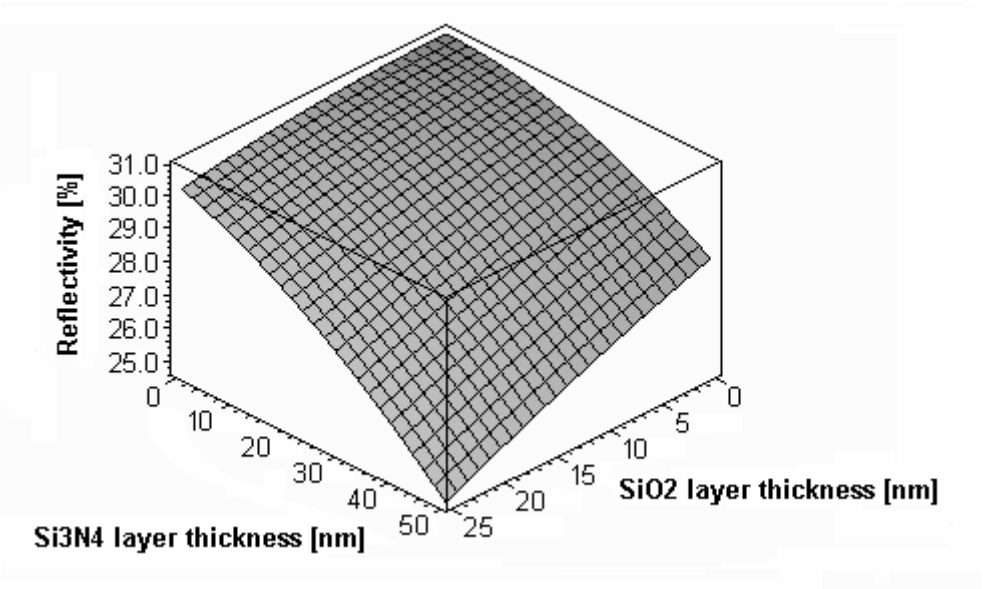


Figure 9-25: Reflectivity at Si/SiO_2 and SiO_2/Si_3N_4 interface as function of SiO_2 and Si_3N_4 layer thicknesses.

The reflectivity of the SiO_2/ Si_3N_4 multiple layer system changes between a maximum of 30.8 and a minimum of 24.7. That makes the overall change in reflectivity 19.8%.

In *9.1.1 DILED1* a quick calculation showed that after etching a dielectric layer in the order of 5 – 7nm should have remained on top of the silicon surface. The overall change in layer thickness of the SiO_2/Si_3N_4 system is 75nm for the reflectivity to change with 19.8%. Are both observations compatible? One possible explanation has to do with the drawbacks of plasma etching…trenching, figure 9-26.

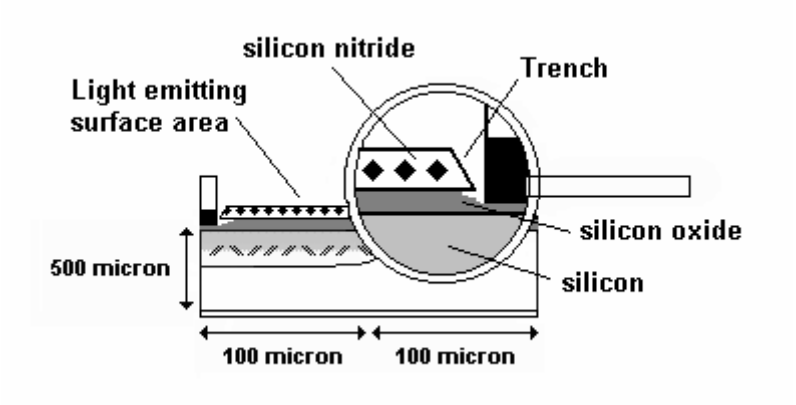


Figure 9-26: Trenching reduces dielectric material below topside contact.

The calculated change in reflectivity of 19.8% is a theoretical value under perfect conditions i.e. defect free interfaces, no pollution, the refractive index is independent of layer structure, composition, current density etc.

An additional explanation for the gap between the calculated reflectivity and measured reflectivity could be photo resist pollution in the form of a film (fragments) that covered the Si_3N_4 layer after definition of the light emitting surface area.

At this point it is impossible to tell whether the SiO_2/ Si_3N_4 system is really responsible for the change in reflectivity. A pessimist would say that the calculated change of 19.8% does not equal the measured change of 26.8%. An optimist would believe it could have been 26.8% under perfect circumstances. One thing is clear…reflections at the Si/SiO_2 interface alone can't cause deviations in peak intensity of 26.9 and 26.7% for respectively DILED1 70 and 100keV devices.

In *9.1.1 DILED1* it was briefly mentioned that 50% of the 70keV DILED1 devices required a breakdown, the other 50% did not. All 100keV DILED1 devices required a breakdown. Additional measurements of the 70keV DILED1 devices could provide more information about the change in light intensity for devices that require a breakdown with respect to devices that do not require a breakdown.

Summarizing:

- Reflections at the Si/SiO_2 interface alone can't cause deviations in peak intensity of 26.9 and 26.7% for respectively DILED1 70 and 100keV devices.

10 Achievements, Conclusions & Recommendations

10.1 Achievements

For DILED1, DILED2 and DIFLED I-V characteristics have been measured. Electrical parameters have been derived and compared to estimate values, except the photo current.

- Photo current $I_{v=0}$
- The saturation current I_0 between: 9×10^{-17} and 1×10^{-15}A;
- The thermal voltage equivalent V_{th}: 25.2mV;
- The ideality factor m: 1;
- The junction voltage V_j: exceeds the built-in voltage (also called onset voltage) of ~0.6V;
- Bulk resistance R_{BULK}: in the order of the wafer resistance of 3.18 – 31.8Ω.

Summary DILED1

- The extracted diode parameters give a good indication for DILED1. The bulk resistance values are not correct values due to assumptions that have been made while deriving them. However one known trend is visible: bulk resistance is proportional to implant energy;
- The DILED1 parameters have been compared to find a correlation with optical parameters;
- The DILED1 current versus forward voltage characteristics show a-linear behavior, especially the deeper implants 70 and 100keV. The latter two have been assigned to high injection effect;
- The a-linearity becomes more prominent for higher implant energies, probably due to an increase in bulk resistance;
- The reverse current is proportional to implant energy;
- There is no direct relation between reverse current and annealing temperature.

Summary DILED2

- The extracted diode parameters give a good indication for DILED2;
- The DILED2 parameters have been compared to find a correlation with optical parameters;
- Due to the adjustment of the peak concentration bulk resistance is not proportional to implant energy;
- The DILED2 current versus forward voltage characteristics shows no a-linear behavior;
- The reverse current is not proportional to implant energy;
- There is no direct relation between reverse current and annealing temperature.

Summary DIFLED

- All extracted diode parameters are increased, probably due to the high implant energies. Prove for the effect that high implant energies have upon the I-V characteristics are the high revere currents;
- The DIFLED parameters have been compared to find a correlation with optical parameters;
- The DIFLED current versus forward voltage characteristics show no a-linear behavior;
- For single implants reverse current is proportional to implant energy.

For DILED1, DILED2 and DIFLED light intensity measurements have been performed in the wavelength range 950 – 1300nm. Optical parameters have been derived:

- ✓ Peak intensity I_{PEAK}
- ✓ Standard deviation in peak intensity $I_{PEAK\text{-}DEVIATION}$

10.2 Conclusions

- The electrical parameters have been compared to find a correlation with optical parameters, but no trends were observed

.

- Light intensity versus annealing temperature:

✓ For DILED1 annealed at 850°C light intensity is 2.93(a.u.). For 850 – 1050°C light intensity of DILED1 increases with a factor of ~2.3. Thus the change in light intensity is ~0.6 per 50°C;
✓ At 950°C light intensity of DILED1 is 5.3(a.u.) and the light intensity of DILED2 8.1(a.u.). Light intensity differs by a factor 1.5. The implant dose of DILED1 is 1.0 x $10^{15}cm^{-3}$. The implant dose of DILED2 is 1.2x $10^{15}cm^{-3}$;
✓ The change in light intensity from 1050 to 1100°C is far more than the change in light intensity between 850 – 1050°C. Light intensity increases with a factor estimated between 4.3 and 6.9 per 50°C;
✓ Within the annealing temperature range of 850 – 1100°C, light intensity is maximum for devices annealed at 1100°C. For a 40keV DILED2 annealed at 1100°C light intensity is maximum with a value of 28.8(a.u.);
✓ At 950°C "DIFLED: junction only" light intensity is much higher than both DILED1 and DILED2 light intensity. Light intensity of DILED1 is 5.29(a.u.). Light intensity of DILED2 is 8.11(a.u.). Light intensity of "DIFLED: junction only (3202-4)" is 21.8(a.u.) and light intensity of "DIFLED: junction only (3310-4)" is 24.2(a.u.).

- Light intensity versus boron implant energy:

✓ Light intensity is weakly dependent upon the energy range 40 to 100keV;
✓ The error bars of the 70 and 100keV data indicate a peak deviation of respectively 26.9 and 26.7%. With an average peak deviation of 4.2%, these peak deviation are 6.3 times larger than normal.

- Light intensity for single, double or no silicon implantation (junction only):

✓ Three light intensity groups are distinguishable:
(1) Double implants and deep single implant (450k, 450 & 200k, 360k, 360 & 260k);
(2) Shallow single implants (200k, 260k);
(3) No implants (boron diffusion).

- Light intensity for DILED1 70 & 100keV devices

✓ Reflections at the Si/SiO_2 interface alone can't cause deviations in peak intensity of 26.9 and 26.7% for respectively DILED1 70 and 100keV devices.

Main conclusion: dislocation loops do not seem to enhance light intensity.

10.3 Recommendations

In this section 2 recommendation are given with respect to dislocation loop engineered devices[6].

Recommendation 1

Perform a step to getter aluminum to reduce the non-radiative emission that competes with silicon band-to-band luminescence. Maybe even change the DILED1, DILED2 and DIFLED layout in order to do so.

This information became available through extensive mail correspondence with the first author of references 27 and 28 in "part I, Literature report", L. Fedina.

Strains introduced by clean dislocations e.g. free of dangling bonds and impurities, seems to provide a main contribution to enhanced band-to-band **E**lectro-**L**uminescence (**EL**). Note that {113] defects compete with band-to band EL providing another peak at 1230-1380nm[10]. 60°-Gliding dislocation is also competing with band-to-band luminescence providing a peak at 1150nm. Note that with exception of the dominant band-to-band peak (called D1 line), these peaks are observed at temperatures below room temperature.

In reality dislocation loops are decorated with impurities. Probably, high temperature annealing decreases the concentration of non-radiative centers at the dislocation, thus leading to the increase of radiative band-to-band luminescence. This effect is known as gettering of impurities.[42, 44] Some defects increase silicon band-to-band luminescence and others decrease silicon band-to-band luminescence. This is a matter of investigations as well as the nature of dislocation related luminescence (D1-D4 bands). Aluminum competes with band-to-band luminescence[42]. Rare earth atoms, Erbium as the most prominent example enhances the band-to-band luminescence[50].

Recommendation 2

First introduce the dislocation loop array by performing a low energy silicon pre-amorphization implant. For amorphization the silicon dose should exceed $1\times10^{15}cm^{-2}$. Then form the junction by a high energy boron implantation of a dose exceeding $1\times10^{16}cm^{-2}$.

In the dose regime above $1.4\times10^{15}cm^{-2}$ some remarkable aspects concerning the roll of pre-amorphization have been mentioned. First of all Jones et. al. carried out the following experiment, table 10-1:

Table 10-1: Roll of pre-amorphization from Jones experiment[2].

Jones Experiment	Pre-amorphization implant		Implant	
	Energy	Dose	Energy	Dose
	E	Q	E	Q
Sample	keV	cm^{-2}	keV	cm^{-2}
1	–	–	50	1×10^{16}
2	70	5×10^{15}	30	5×10^{15}
3	30	5×10^{15}	70	5×10^{15}

After re-growth of the amorphous layer at 550°C, the samples were annealed at 900°C for 16h. When compared with sample 1, the concentration of atoms bound by the dislocation loops is observed to be smaller for sample 2. However the concentration of atoms bound by the dislocation loops is observed to be larger for sample 3.

[6] Recently G.Z. Pan[43] and co-workers stated in an article titled "{113} Defect-Engineered Silicon Light-Emitting-Diodes", IEEE, 0-7803-8684-1/04, 2004, that {113} cluster engineered devices have a light intensity that is 25 times higher than for dislocation loop engineered devices. Of course it would be possible to present a list of recommendations concerning {311} clusters, but the emphasize in this master thesis is on dislocation loops.

Thus a low energy pre-amorphization implant followed by a higher energy implant introducing the same dose as a single implant, results in a larger concentration of atoms bound by the dislocation loops.

An interesting situation exists when a pre-amorphization implant with silicon atoms is followed by a high dose boron implant. Sun[16] prepared silicon p-n diodes by silicon pre-amorphization at 50keV followed by different boron doses at 25keV. The diodes are annealed at 1050°C for 20 minutes, figure 10-1.

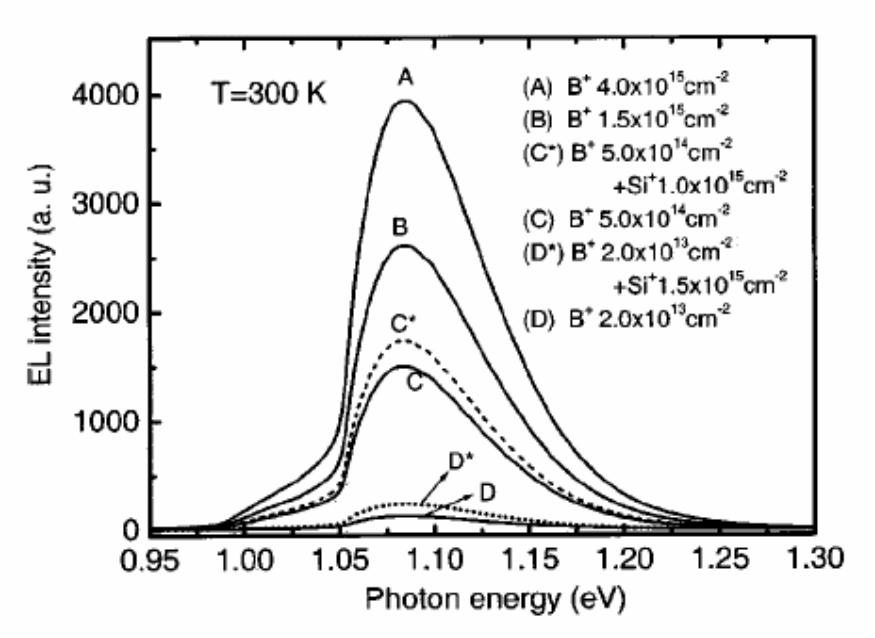


Figure 10-1: Roll of silicon pre-amorphization and increasing boron implant doses.

At boron implants exceeding $1\times10^{16}cm^{-2}$, the boron concentration reaches the thermal equilibrium solubility limit ($1.53\times10^{20}cm^{-3}$ at 1050°C)[14]. Hence the boron clusters can not be dissolved during the long time anneal.

"Observations by Cowern *et al.* [9, 10], suggest that in systems where B is present in large doses, excess interstitials help boron atoms to form boron clusters and are themselves incorporated into these clusters (so-called **B**oron **I**nterstitial **C**lusters, BICs)[14]", figure 10-2.

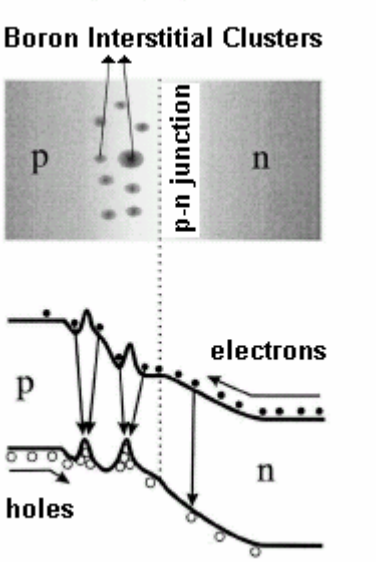


Figure 10-2: Boron Interstitial Clusters act as blocking potential.

Both dislocation loops and **B**oron **I**nterstitial **C**lusters act as blocking potential, thereby hindering the motion of carriers across the junction. The carriers are confined to the region where the blocking potentials are situated.

11 References

[1] Wai Lek Ng, M. A. Lourenco, R. M. Gwilliam, S. Ledain, G. Shao, and K. P. Homewood, "An efficient room-temperature Silicon-based light emitting diode", *Nature*, Vol. **410**, pp.192-194, 2001.

[2] K. S. Jones, S. Prussin, and E. R. Weber, "A systematic analysis of defects in ion-implanted Silicon" *Applied Physics A*, Vol. **45** (1), pp. 1-34, 1988.

[3] I. Avci, "Modeling the nucleation and evolution of dislocation loops in Silicon during annealing and the effects of mechanical stress on dislocation loops", Ph. D dissertation, University of Florida, 2001.

[4] S. Chaudry, "Analysis and modeling of stress related effects in scaled Silicon technology", PhD. Thesis, University of Florida, 1996.

[5] D. J. Stowe, S.A. Galloway, S. Senkader, Kanad Mallik, R. J. Falster, P. R. Wilshaw, "Near-band gap luminescence at room temperature from dislocations in Silicon", PHYSICA B-CONDENSED MATTER, Vol. **340**, pp. 710-713, 2003.

[6] N. A. Sobolev, A. M. Emel'yanov, E. I. Shek, V.I. Vdovin, "Extended structural defects and their influence on the electroluminescence in efficient Si light-emitting diodes", PHYSICA B-CONDENSED MATTER, **340**, pp. 1031-1035, 2003.

[7] M. A. Lourenco, M. S. A. Siddiqui, G. Shao, R. M. Gwilliam, K. P. Homewood, "Ion beam fabricated Silicon light emitting diodes", PHYSICA STATUS SOLIDI A-APPLIED RESEARCH, Vol. **201** (2), pp. 239-244, 2004.

[8] R. Labusch, "The true potentials and transition barriers at dislocations", JOURNAL OF PHYSICS-CONDENSED MATTER, Vol. **14** (48), pp. 12801-12811, 2002.

[9] Martin A. Green, "Photovoltaic principles", PHYSICA E, Vol. **14** (1-2), pp. 11-17, 2002.

[10] Sebastian Libertino and Salvatore Coffa, "Formation, evolution, and annihilation of interstitial clusters in ion implanted Si", PHYSICAL REVIEW B, Vol. **63** (19), Art. No. 195206, 2001.

[11] P. M. Fahey, P. B. Griffin, and J. D. Plummer, "Point defects and Dopant Diffusion in Silicon", Reviews of modern Physics, vol. **61**, p.289, 1989.

[12] Leonid V. Zhigilei, "Crystal defects", Lecture, University of Virginia, Department of Materials Science and Engineering.

[14] J. M. Sun, T. Dekorsy, W. Skorupa, B. Schmidt, A. Mücklich, and M. Helm, "Below-band-gap electroluminescence related to doping spikes in Boron-implanted Silicon pn-diodes", Physical Review B, Vol. **70**, Art. No. 155316, 2004.

[15] IMEL NCSR "Demokritos"–Center of excellence in micro, nanotechnologies and microsystems, Bi-annual report 2001-2002.
www.imel.demokritos.gr/

[16] Y. T. Rebane and J. W. Steeds, "Hole bound states in the deformation field of screw dislocations in cubic semiconductors", Physical Review B, Vol. **48** (20), Art. No. 14963, 1993.

[17] Masataka Kase, Yoshio Kikuchi, Mami Kimura, and Haruhisa Mori, "Defects produced in Si p^+n diodes by B^+ implantation at liquid nitrogen temperature or -60°C", JOURNAL OF APPLIED PHYSICS, Vol. **75** (7), pp. 3358-3364, 1994.

[18] Le Minh Phuong, "Silicon Light Emitting Devices for Integrated Applications", Ph. D dissertation, University of Twente, 2003.

[19] Andres Felipe Gutierrez, "defect evolution from low energy germanium implants in Silicon", Ph. D dissertation, University of Florida, 2001.

[20] J. S. Williams, “Ion implantation of semiconductors”, Materials Science and Engineering A, Vol. **253** (1-2), pp. 8-15, 1998.

[21] Alp H. Gencer, “Modeling and simulation of transient enhanced diffusion based on interaction of point and extended defects”, Ph. D dissertation, Boston University, 1999.

[22] K. S. Jones, J. Liu and L. Zhang, V. Krishnamoorthy, R. T. Dehoff, “Studies of the interactions between (311) defects and type and II dislocation loops in Si+ implanted Silicon”, Nuclear Instruments and Methods in Physics Research B, Vol. **106**, pp. 227-232,
1995

[23] J. Liu, M. E. Law and K. S. Jones, “EVOLUTION OF DISLOCATION LOOPS IN SILICON IN AN INERT AMBIENT-I”, Solid-State Electronics, Vol. ***38***. (7), pp. 1305-1312, 1995

[24] S. Chaudhry, J. Liu, K. S. Jones and M. E. Law, “EVOLUTION OF DISLOCATION LOOPS IN SILICON IN AN INERT AMBIENT- II”, *Solid-State Electronics,* Vol. ***38****. (7), pp. 1313-1319, 1995.*

[25] G. Z. Pan and K. N. Tu, “Size-distribution and annealing behavior of end-of-range dislocation loops in Silicon-implanted Silicon”, Journal of applied Physics, Vol. **81** (1), 1997.

[26] G. Z. Pan and K. N. Tu, “Transmission electron microscopy on {113} rodlike defects and {111} dislocation loops in Silicon-implanted Silicon”, Journal of applied Physics, Vol. **82** (2), 1997.

[27] L. Fedina , A. Gutakovskii, A. Aseev, J. VanLanduyt and J. Vanhellemont, “On the mechanism of {111}-defect formation in Silicon studied by *in situ* electron irradiation in a high resolution electron microscope”, PHILOSOPHICAL MAGAZINE A, VOL. **77** (2), pp. 423-435, 1998.

[28] L. Fedina , A. Gutakovskii, A. Aseev, J. VanLanduyt and J. Vanhellemont, “Extended Defects Formation in Si Crystals by Clustering of Intrinsic Point Defects Studied by in-situ Electron Irradiation in an HREM**”,** physica status solidi A, Vol. **171,** 147-157, 1999.

[29] S. Takeda, M. Kohyama, and K. Ibe, “Interstitial Defects on {113} in Si and Ge: Line Defect Configuration Incorporated with a Self-Interstitial Atom Chain”, Philosophical Magazine A, Vol. 70 (2), p. 287, 1994.

[30] T. Y. Tan, “*Atomic Modeling of Homogeneous Nucleation of Dislocations from Condensation of Point Defects in Silicon”*, *Philosophical Magazine A*, Vol. **44**, pp.101-125, 1981.

[31] C. Bonafos, D. Mathiot and A. Claverie, “Oswald rippening of end-of-range defects in Silicon”, Journal of Applied Physics, Vol. **83**(6): pp. 3008-3017, 1998.

[32] J. P. Hirth and J. Lothe, *Theory of dislocations*, ISBN McGraw-Hill, 1968.

[33] Plummer, Deal, Griffin, “Silicon VLSI Technology-Fundamentals, Practice and Modeling”, ISBN 0-13-085037-3, Prentice Hall, 2000.

[34] Mouthaan, “Semiconductor Devices Explained-using active simulation”, ISBN 0-471-98854-5, John Wiley & Sons, 1999.

[35] Wim van Etten en Jan van der Plaats, “Principles of optical fiber communications”, ISBN 9036515092, Twente University Press, 2000.

[36] Ioffe Physico-Technical Institute, Physical properties of semiconductors, Silicon, band structure.
http://www.ioffe.rssi.ru/SVA/NSM/Semicond/Si/index.html

[37] Science daily, Encyclopedia, Indirect band gap.
http://www.sciencedaily.com/encyclopedia/indirect_bandgap

[38] Steve Roberts, “Microplasticity”, Lecture, University of Oxford, Oxford Materials: Strong Solids Group, 2004.

Dislocation animations and videos:
(http://users.ox.ac.uk/~roberts/sgrgroup/lectures/microplast/microplast_vids.htm)

[39] Julie Bellingham, "SIMS Depth Profiling of Ultra-low Energy Ion Implanted Silicon using Sub-keV Ion Beams", Ph. D dissertation, University of Warwick, 2003.

Chapter 2 – Challenges facing the production and analysis of modern implanted materials.
www.triv.org.uk/~jules/Chapter2.pdf

[40] P. A. Stolk, H.-J. Gossmann, D. J. Eaglesham, D. C. Jacobson, C. S. Rafferty, G. H. Gilmer, M. Jaraı´z and J. M. Poate, "Physical mechanisms of transient enhanced dopant diffusion in ion-implanted Silicon", Journal of Applied Physics, Vol. **81** (9), 1997.

[41] M. A. Lourenco, M. S. A. Siddiqui, G. Shao, R. M. Gwilliam, G. Shao, K. P. Homewood, "Efficient Silicon light emitting diodes made by dislocation engineering", PHYSICA E, Vol. 16, pp. 376-381, 2003.

[42] Thorsten Trupke, Jianhua Zhao, Aihua Wang, Richard Corkish, and Martin A. Green, "Very efficient light emission from bulk crystalline Silicon", APPLIED PHYSICS LETTERS, Vol. 82 (18), 2003.

[43] G.Z. Pan, R.P. Ostroumov, Y.G. Lian, K.N. Tu and K.L. Wang, "{113} Defect-Engineered Silicon Light-Emitting-Diodes", IEEE, 0-7803-8684-1/04, 2004.

[44] V. Kveder, M. Badylevich, E. Steinman, A. Izotov, M. Seibt and W. Schrőter, "Room-temperature Silicon light-emitting diodes based on dislocation luminescence", APPLIED PHYSICS LETTERS, Vol. 84 (12), 2004.

[45] M. A. Lourenco, M. S. A. Siddiqui, G. Shao, R. M. Gwilliam, G. Shao, K. P. Homewood, "Efficient Silicon light emitting diodes made by dislocation engineering", PHYSICA E, Vol. 16, pp. 376-381, 2003.

[46] Sedra, Adel S., and Smith, Kenneth C.: *Microelectronics*, 4th Ed, Oxford University Press, 1997.

Online material:
Sergio Franco, "The *pn* Junction – THEORY AND PRACTICE", San Francisco State University, 2004.
online.sfsu.edu/~sfranco/Notes/pnJunction.pdf

[47] H. Vos, "Algemene practicum handleiding elektrotechniek (APH) cursus 1998/1999", University of Twente, No. 196, pp. 33-38, 1998.

[48] Allen Nussbaum, Richard Arlan Philips, "Contemporary optics for scientists & engineers", Prentice-Hall, 0-13-170183-5, 1976.

[49] Edward D. Palik, "Handbook of optical constants of solids 2", Boston Academic press, 0-12-544422-2, 1985 and 1991.

[50] C. Buchal, S. Wang, F. Lu R. Carrius, S. Coffa,"Ion implantation of rare earth ions for light emitters", NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH SECTION B-BEAM INTERACTIONS WITH MATERIALS AND ATOMS 190: 40-46 MAY 2002.

Articles that might be interesting in the future:

[51x] T. Dekorsy, J.M. Sun, W. Skorupa, B. Schmidt, A. Mücklich, and M. Helm, "Light emitting Silicon pn diodes", APPLIED PHYSICS A-MATERIALS SCIENCE & PROCESSING, Vol. **78** (4), pp. 471-475, 2004.

[52x] J.M. Sun, T. Dekorsy, W. Skorupa, B. Schmidt, A. Mücklich, and M. Helm, "Origin of anomalous temperature dependence and high efficiency of Silicon light-emitting diodes", APPLIED PHYSICS LETTERS, Vol. **83** (19), pp. 3885-3887, 2003.

[53x] J.M. Sun, T. Dekorsy, W. Skorupa, B. Schmidt, A. Mücklich, and M. Helm, "Bound-excition-induced current bistability in a Silicon light emitting diode", Applied Physics Letters, Vol. **82** (17), pp. 2823-2825, 2003.

[54x] P. Etchegoin, J. Kircher, M. Cardona, “Elasto-optical constants of Si”, PHYSICAL REVIEW B, Vol. **47** (16), pp. 10292-10303, 1993.

Appendices

Appendix A – Silicon as optical absorber

When an electron crossed the band gap it eventually resides in the conduction band minimum. The excitation to the conduction band implies current conduction is possible. The photo-detector is a junction operating in reverse bias i.e. every generated electron-hole pair is ripped apart by the electric field across the junction. The electrons and holes are collected at external contacts.

Due to the indirect nature of the band gap, transitions from valence band maximum to conduction band minimum are rare. Again a phonon assisted k-vector momentum "kick" is needed. A large part of the photon energy will be wasted before a phonon and photon event occurs at the same time. The remaining energy is insufficient to cross the band gap.

However silicon *does* absorb light "this only occurs for photons with significantly more energy than the band gap. This is why pure silicon appears dark gray and opaque, rather than clear[37]".

Figure A.1: gray/opaque glow of Silicon.

"Because of its small band gap in relation to energy of light in the visible spectrum (and mostly because of its low price!), it is still used as a photo-detector. The surplus of light energy is absorbed by the lattice and there will be enough phonon energy to facilitate transitions from the valence to conduction band; the quantum efficiency (…) of silicon is still high[34]".

Appendix B – Look-up table projected range and standard deviation most common dopants in Silicon

	Phos		As		Sb		Boron	
Energy (keV)	Range (μm)	Std Dev (μm)	Range (μm)	Std Dev (μm)	Range (μm)	Std Dev (μm)	Range (μm)	Std Dev (μm)
10	0.0199	0.0064	0.0084	0.0043	0.0121	0.0058	0.0473	0.0249
20	0.0342	0.0125	0.0156	0.0075	0.0219	0.0100	0.0826	0.0384
30	0.0473	0.0179	0.0226	0.0102	0.0306	0.0133	0.114	0.0483
40	0.0598	0.0229	0.0294	0.0128	0.0385	0.0162	0.143	0.0562
50	0.0717	0.0275	0.0362	0.0152	0.0459	0.0187	0.171	0.0628
60	0.0833	0.0317	0.0429	0.0176	0.0528	0.0209	0.198	0.0685
70	0.0947	0.0356	0.0495	0.0198	0.0594	0.0229	0.223	0.0736
80	0.105	0.0393	0.0561	0.0220	0.0656	0.0248	0.248	0.0780
90	0.116	0.0428	0.0626	0.0241	0.0716	0.0265	0.272	0.0821
100	0.127	0.0461	0.0692	0.0261	0.0773	0.0280	0.296	0.0857
120	0.148	0.0522	0.0821	0.0301	0.0883	0.0309	0.341	0.0922
140	0.169	0.0579	0.0950	0.0339	0.0985	0.0334	0.385	0.0978
160	0.189	0.0630	0.107	0.0375	0.108	0.0357	0.428	0.102
180	0.210	0.0678	0.120	0.0411	0.117	0.0378	0.469	0.107
200	0.229	0.0723	0.133	0.0446	0.126	0.0397	0.509	0.110

Appendix C – Example of band gap change calculation

We must mention that M. Lourenco did not perform any calculations, her role was restricted to draw attention to the screw dislocation as starting point of a long range strain calculation.

The deformation field of a screw dislocation is calculated (sheet 1: 14). By setting the slip angle θ=0°, the displacement is in the x-z plane. This displacement reflects the dislocation boundary i.e. the interface between the extra lattice and its surroundings. For loops that are perfect round we can give an estimate for the length of the dislocation boundary (reflected by radius r). From figure 3-23 we derive that for a 50keV, 1×10^{15}cm^{-2} Si+ implant annealed at 1000°C, the average loop radius is 25nm. Thus the loop boundary is 50π nm. The loop boundary exhibits a height equal to the displacement i.e. the Burgess vector, along the total boundary. Therefore a too small radius does not reflect a loop boundary anymore. The smallest radius that reflects a screw dislocation correct is 1nm according to reference 38. For smaller radii elastic theory breaks down.

In her article M. Lourenco mentions some figures: maximum stress (25-50GPa), poissons ratio υ (0.42) and Young modulus G (113GPa). Through mail correspondence with L. Fedina we were able to find out that 5-7 ring configuration (b = a/5<111>=0.191 nm) form the dislocation boundary of a dislocation loop. Now we are able to calculate the stress in the y-z direction i.e. in the plane perpendicular to the loop boundary. By setting the slip angle θ=0°, the stress is calculated at the loop boundary and reflects the maximum stress:

Equation [C-1]

$$\sigma_{yz} = \frac{Gb}{2\pi}\frac{x}{x^2+y^2} = \frac{Gb}{2\pi}\frac{\cos\theta}{r} = \frac{113\times0.191}{2\pi}\frac{1}{50\pi} = 0.022\left[GPa\right]$$

It is clear that our stress estimation is significantly lower. Also notice that smaller loop boundaries result in larger stress? Large loops (boundaries) give rise to long range stress and therefore large loops are preferred. This formula does not reflect that.

By keeping *x* fixed, we notice that the stress field is inversely proportional to the distance to the loop boundary y. According to Lourenco “this stress field decays inversely with distance and reaches a maximum stress of 25 to 50 GPa”.

The band gaps of semiconductors are pressure dependent and, in the case of Silicon, the band gap decreases with increasing pressure and increases under negative pressure. Through mail correspondence with Lourenco we were told that the pressure-coefficient of silicon is -0.18meV per kilo bar. This equals -0.18×10^{-11}eV per Pascal. Therefore the band gap change, based upon our first approximation, is:

Equation [C-2]

$$\Delta E_{gap} = \alpha_{pressure}\sigma_{yz} = -0.18\times10^{-11}\times0.022\times10^{9} = 0.04\left[meV\right]$$

Lourenco estimates the total band gap change from 0.325 to 0.75eV, a significant fraction of the band gap itself which is 1.1eV.

Elasticity - recap

Displacement vector:

$$\mathbf{u} = [u_x, u_y, u_z]$$

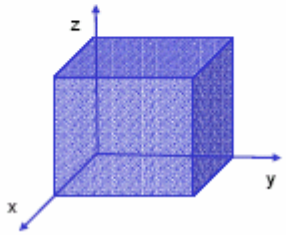
Strain tensor:

$$\varepsilon_{xx} = \frac{\partial u_x}{\partial x}$$

$$\varepsilon_{xy} = \frac{1}{2}\left(\frac{\partial u_x}{\partial y} + \frac{\partial u_y}{\partial x}\right) \quad etc.$$

Dilatation, Δ:

$$\Delta = \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}$$



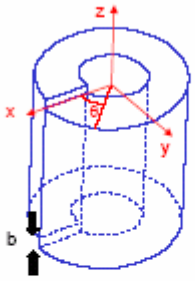
Stress tensor:

$$\sigma_{xx} = 2G\varepsilon_{xx} + \lambda\Delta$$
$$\sigma_{yy} = 2G\varepsilon_{yy} + \lambda\Delta$$
$$\sigma_{zz} = 2G\varepsilon_{zz} + \lambda\Delta$$
$$\sigma_{xy} = 2G\varepsilon_{xy}$$
$$\sigma_{xz} = 2G\varepsilon_{xz}$$
$$\sigma_{yz} = 2G\varepsilon_{yz}$$
$$\lambda = \frac{2G\nu}{(1-2\nu)}$$

Elastic energy:

$$dE_{el} = \tfrac{1}{2}dV \sum_{i=x,y,z} \sum_{j=x,y,z} \sigma_{ij}\varepsilon_{ij}$$

Strain field of straight screw dislocation



"Recipe" :
- take a hollow cylinder, axis along z:
- cut on a plane parallel to the z-axis;
-displace the free surfaces by **b** in the z-direction.

By inspection: $u_x = u_y = 0$

$$u_z = \frac{b\theta}{2\pi}$$
$$= \frac{b}{2\pi}\tan^{-1}\left(\frac{y}{x}\right)$$

$$\varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_{zz} = \varepsilon_{xy} = \varepsilon_{yx} = 0$$

$$\varepsilon_{xz} = \tfrac{1}{2}\frac{\partial u_z}{\partial x} = \frac{b}{4\pi}\frac{\partial}{\partial x}\tan^{-1}\left(\frac{y}{x}\right)$$
$$= -\frac{b}{4\pi}\frac{1}{1+\left(\frac{y}{x}\right)^2}\frac{y}{x^2}$$
$$= -\frac{b}{4\pi}\frac{y}{x^2+y^2} = -\frac{b}{4\pi}\frac{\sin\theta}{r}$$

$$\varepsilon_{yz} = \tfrac{1}{2}\frac{\partial u_z}{\partial y} = \frac{b}{4\pi}\frac{\partial}{\partial y}\tan^{-1}\left(\frac{y}{x}\right)$$
$$= \frac{b}{4\pi}\frac{1}{1+\left(\frac{y}{x}\right)^2}\frac{1}{x}$$
$$= \frac{b}{4\pi}\frac{x}{x^2+y^2} = \frac{b}{4\pi}\frac{\cos\theta}{r}$$

Stress field of straight screw dislocation

$$\varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_{zz} = \varepsilon_{xy} = \varepsilon_{yx} = 0$$

$$\varepsilon_{xz} = -\frac{b}{4\pi}\frac{y}{x^2+y^2} = -\frac{b}{4\pi}\frac{\sin\theta}{r}$$

$$\varepsilon_{yz} = \frac{b}{4\pi}\frac{x}{x^2+y^2} = \frac{b}{4\pi}\frac{\cos\theta}{r}$$

$$\sigma_{xx} = \sigma_{yy} = \sigma_{zz} = \sigma_{xy} = \sigma_{yx} = 0$$

$$\Delta = 0$$

$$\sigma_{xz} = 2G\varepsilon_{xz} = -\frac{Gb}{2\pi}\frac{y}{x^2+y^2} = -\frac{Gb}{2\pi}\frac{\sin\theta}{r}$$

$$\sigma_{yz} = 2G\varepsilon_{yz} = \frac{Gb}{2\pi}\frac{x}{x^2+y^2} = \frac{Gb}{2\pi}\frac{\cos\theta}{r}$$

In Polar coordinates:

(either by direct inspection, or by transforming the strains and stresses from Cartesian co-ordinates)

$$\varepsilon_{\theta z} = \varepsilon_{z\theta} = \frac{b}{4\pi r}$$

$$\sigma_{\theta z} = \sigma_{z\theta} = \frac{Gb}{2\pi r}$$

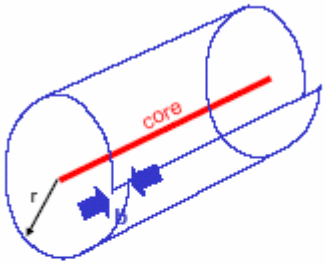
All other components of the stress tensor are zero.

Note:

- Stress and strain fields are pure shear
- Fields have radial symmetry
- Stresses and strains are proportional to 1/r:
  - extend to infinity
  - tend to infinite values as r⇒0

Infinite stresses cannot exist in real materials: the dislocation core radius r_0 is that within which our assumption of linear elastic behaviour breaks down. Typically $r_0 \approx 1$ nm.

Strain energy of a screw dislocation



In the shell shown,

$$\varepsilon_{\theta z} = \varepsilon_{z\theta} = \frac{b}{4\pi r}$$

$$\sigma_{\theta z} = \sigma_{z\theta} = \frac{Gb}{2\pi r}$$

All other stresses and strains are zero.

Elastic energy per unit volume = $\frac{1}{2}(\varepsilon_{\theta z}\sigma_{\theta z} + \varepsilon_{z\theta}\sigma_{z\theta}) = \frac{Gb^2}{8\pi r^2}$

Volume of shell, thickness δr = $2\pi r.\delta r$

Elastic energy of shell = $\frac{Gb^2}{4\pi r}\delta r$

Total elastic energy $= \int_{r_0}^{R} \frac{Gb^2}{4\pi r} dr$

$$= \frac{Gb^2}{4\pi}\ln\left(\frac{R}{r_0}\right)$$

per unit length of dislocation line

Appendix D – Process flow

DILED Device with dislocation loops formed by B implantation

Phase 0 Standard processing steps

0.1 Standard Wafer cleaning

process parameters cleaning: (total process time ≈ ½ hr)

step 1

beaker 1 fuming HNO_3 [min]
5

step 2

beaker 2 fuming HNO_3 [min]
5

step 3

rinsing DI water until resistance greater than [MΩ]
10

step 4

HNO_3 65% [min]
10

step 5

rinsing DI water [MΩ]
>10

Phase 1 Active Areas

1.1 Wafer cleaning

standard cleaning

1.2 Growth of 25 nm pad oxide

O-Rbov-S: 02-09 (total process time ≈ 1½ hr)

Process parameters:

temperature cycle [°C]	ramp up/down [°C/min]	ambient	process time [min]	gas flow [slm]
800-950	10	O_2/HCl	15	4
950		O_2	30	4
950		N_2	20	4
950-800	-7.5	N_2	20	4

1.3 Deposition of 50 nm LPCVD Si_3N_4

O-Lbov-N1 (total process time ≈ 1 hr)

process parameters:

gas flow SiH_2Cl_2 [sccm]	gas flow NH_3 [sccm]	total pressure [mTorr]	deposition temperature [°C]	growth rate [nm/min]	deposition time [min]
30	90	300	800	6.7	7.5

1.4 Definition of active area (AA-msk)

process parameters:

resist	thickness [µm]	pre-bake (95°C) [sec]	exposure time [sec]	exposure offset [µm]	after exp. bake (120°C) [sec]	post-bake (120°C) [min]
S1813	1.6	60			60	no

1.5 Plasma etching of Si_3N_4

process parameters 2-phase-etch: (total process time ≈ 2 min)

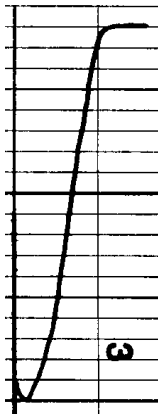
phase 1: descum

gas flow O_2 [sccm]	pressure [µbar]	power [Watt]	ardel plate	V_{dc} [Volt]	matching network	etch time [sec]
44	106	100	no	?	30/100	20

phase 2: plasma etching of Si_3N_4

gas flow CF_4/O_2 [sccm]	pressure [µbar]	power [Watt]	ardel plate	V_{dc} [Volt]	etch rate Si_3N_4 [nm/min]	projected thickness [nm]	etch time [min]	overetch time [sec]	matching network
44	106	100	no	190	50	50	1	30	30/100

use process wafer for end-point-detection



Phase 2 Junction implantation

2.1 P-well Implantation

process parameters:

implantation species	dose/cm^2	implantation value [µC]	acceleration voltage [kV]	mass magnet [amu]	2^{nd} magnet [A]
B^+	1.0 10^{15}	533.4	Xx	11	

Xx=40,70,100

2.2 Resist removal and cleaning

standard cleaning

2.3 Formation of loops

O-Rmid-S: 02-05 (total process time ≈ 1 h 20 min)

process parameters:

temperature cycle [°C]	ramp up/down [°C/min]	ambient	process time [min]	gas flow [slm]
800-1050	10	O_2/HCl	25	4
1050		N2	Wait for peddle	
1050		N_2	19	4
1050		O_2	1	4
1050		N_2	Paddle out	4
1050-800	7.5	N_2	34	4

Phase 3 Gettering

3.1 Cover front side with resist for implantation back side

process parameters:

resist	thickness [µm]	post-bake (100°C) [min]
S1818	1.8	30

3.2 Implantation of Phosphorous back side

process parameters:

implantation species	dose/cm^2	implantation value [µC]	acceleration voltage [kV]	mass magnet [amu]	2^{nd} magnet [A]
P^+	$8.0\ 10^{15}$	4267	100	31	10

3.3 Wafer cleaning

standard cleaning

3.4 Gettering

O-Rmid-S: 34-42 (total process time ≈ 3½ hr)

process parameters:

temperature cycle [°C]	ramp up/down [°C/min]	ambient	process time [min]	gas flow [slm]
800-900	10	N_2	10	4
900		N_2	10	4
900-600	-2	N_2	150	4

Phase 4 Metallization

4.1 Removal of pad oxide (in the dark etching)

Etching time: ≈ 1 min

process parameters:

SiO_2 etch	etch rate SiO_2 (20°C) [nm/min]	etch time [min]	projected thickness [nm]
1 % HF	50	1	2.5

4 .2 Deposition of 70 nm TiW and 1 µm Al

Recipe Nordiko: 5 (process time each wafer 30 min)

process parameters 2-phase-sputtering:

phase 1: sputtering 70 nm TiW

gas flow Ar [sccm]	pressure [µbar]	power [Watt]	V_{dc} [Volt]	sputter rate [nm/min]	projected thickness [nm]	sputter time [min]
?	?	?	?	75	70	1

phase 2: sputtering 1 µm Al

gas flow Ar [sccm]	pressure [µbar]	power [Watt]	V_{dc} [Volt]	sputter rate [nm/min]	projected thickness [µm]	sputter time [min]
?	?	?	?	75	1	10

4 .3 Definition of interconnect

process parameters:

resist	thickness [µm]	pre-bake (95°C) [sec]	exposure time [sec]	exposure offset [µm]	after exp. bake (120°C) [sec]	post-bake (120°C) [min]
907/17	1.3	60	4.8		60	15

4 .4 Etch of Aluminum

1. Option 1: Plasma etching

Floppy: "Aluminium" (total process time ≈ 1 hr)

process parameters 3-phase-etch:

phase 1 (process step 5):

gas flow Cl_2 [sccm]	gas flow BCl_3 [sccm]	pressure [mTorr]	power [Watt]	V_{dc} [Volt]	etch time [min]
1.3	19.8	40	160	230	2

phase 2 (process step 7):

gas flow Cl_2 [sccm]	gas flow BCl_3 [sccm]	pressure [mTorr]	power [Watt]	V_{dc} [Volt]	etch rate Al [nm/min]	projected thickness [µm]	etch time until Al disappeared [min]
8.6	34.4	25	130	218	?	1	≈ 15

phase 3 (process step 9): overetch

gas flow Cl_2 [sccm]	gas flow BCl_3 [sccm]	pressure [mTorr]	power [Watt]	V_{dc} [Volt]	overetch time [min]
1.3	19.7	40	257	350	4

Option 2: Wet etching of Aluminum

process parameters 2-phase-etch

phase 1 (etch of Al)

fuming H_3PO_4	etch rate Al [nm/min]	process time [min]
55^0C		

phase 2 (etch of TiW)

H_2O_2 30%	etch rate Al [nm/min]	process time [min]
23^0C	~10	7

4 .5 Removal of resist

process parameters:

fuming HNO_3	process time [min]

100 %	10

4 .6 Sintering of the Aluminium

O-lmid-S: ?-? (total process time ≈ ½ hr)

process parameters:

temperature [°C]	ambient	process time [min]	gas flow [slm]
400	wet N_2	10	4

Phase 5 Backside Metallization

5.1 Cover front side with resist for sputtering back side

process parameters:

resist	thickness [µm]	post-bake (100°C) [min]
S1818	1.8	30

5 .2 Deposition of 350 nm Al

Recipe Nordiko: 5 (process time each wafer 10 min)

gas flow Ar [sccm]	pressure [µbar]	power [Watt]	V_{dc} [Volt]	sputter rate [nm/min]	projected thickness [µm]	sputter time [min]
?	?	?	?	75	1	5

5.3 Removal of resist

process parameters:

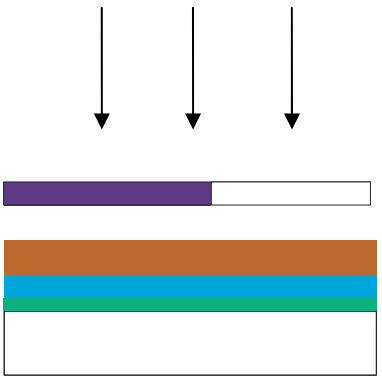
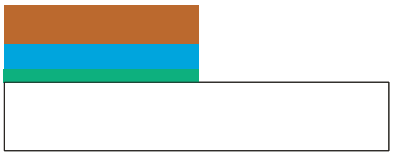
fuming HNO_3	process time [min]
100 %	10

PROCESS FLOW

DiFLED with two processes of Si implantation

Starting material is a standard <100> 4” n-Si wafer with Resistivity: 5-10Ωcm

1. Wafer cleaning Equipment: Ultra Clean Line, CR125C Standard wafer cleaning: a. Beaker 1 - fuming HNO_3, 5 min. b. Beaker 2 - fuming HNO_3, 5 min.	

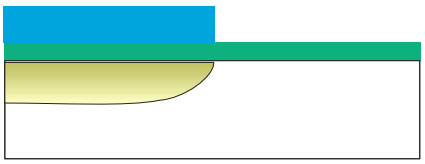
c. Rinse in DI water, QDR until 1/R<0.1 μS d. Boiling HNO_3 69%, 10 min. e. Rinse in DI water, QDR until 1/R<0.1 μS f. Spin dry Removal of native oxide: 1% HF, until hydrophobic	
2. Deposit a layer of Boron doped Silox. That is a p-type layer containing 50 nm SiO_2 + B_2O_3.	
3. Deposit a SiO_2 layer. Deposition of 250 nm SiO_2. In total the Silox layer thickness will be ~ 300 nm	
4. Lithography: definition diffusion source (mask 1) Equipment: Semi automated resist spinner CR117B Karl Süss Mask Aligner MA55, CR119B Developer, CR112B a. Apply primer b. Spin on photo-resist (type 907.17, program 6) c. RPM=4000, time=20 s, resist thickness=1.50m d. Soft bake: 60 sec, 95 °C e. Align mask f. Expose to UV-light (vacuum contact, 5.5 sec, separation distance) g. After-exposure bake (1 min, 120 °C) h. Develop (50 s) i. Check the features j. Post bake 15 min, 120 °C.	
5. Etch diffusion source. BHF (65 nm/min) ~ 5 min (until hydrophobic) Check with microscope.	
6. Removal of resist Equipment: Ultra Clean Line, CR125C Standard wafer cleaning: a. beaker 1 - fuming HNO_3, 5 min. b. beaker 2 - fuming HNO_3, 5 min. c. rinse in DI water, QDR until 1/R<0.1 μS d. boiling HNO_3 69%, 10 min. e. rinse in DI water, QDR until 1/R<0.1 μS f. spin dry	

7. Boron-drive-in 1050^{0}C (also to oxidize Silicon surface)

O-Rbov-S: 11-17 (total process time ≈ 2 hr)

process parameters:

temperature cycle [°C]	ramp up/down [°C/min]	ambient	process time [min]	gas flow [slm]
800-950	10	N_2	15	4
950		N_2	10	4
950		O_2	20	4
950-800	-7.5	N_2	18	4



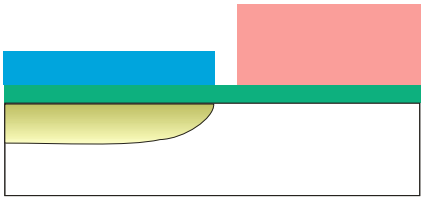
Should make sure the annealing time and temperature!!!!

8. Lithography: Remove Silox layer (Mask 3)
Masking for high energy Implantation

Equipment: Semi automated resist spinner CR117B
Karl Süss Mask Aligner MA55, CR119B
Developer, CR112B

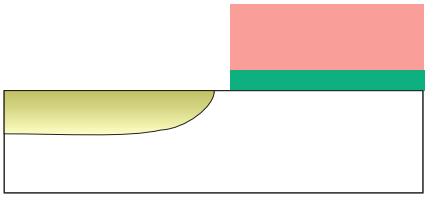
a. Apply primer
b. Spin on photo-resist (type 907.17, program 9)
   RPM=3000, time=20 s, resist thickness =3.5 μm
c. Soft bake: 180 sec, 60 °C
   5 min at 95 ^{0}C
   5 min cooling down to 21 ^{0}C
d. Align mask
e. Expose to UV-light (vacuum contact, **30 sec**, separation distance)
f. After-exposure bake (15 min, 21 °C)
g. Develop (45 s)
h. Check the features

Post bake 15 min, 120 °C



9. Etch Silox layer

BHF (65 nm/min) ~ 5 min (until hydrophobic)
Check with microscope



10. Silicon Implantation
(forming dislocation loops outside the Juction)

Process parameters:

implantation species	dose/cm^2	implantation value [μC]	acceleration voltage [kV]	mass magnet [amu]	2nd magnet [A]
Si^+	**1.0x10^{15}**	533.4	450 360	28	

Projected range for 360 keV ~ 0.589 micro
Junction depth ~ 1.472 micro

11. Removal of resist

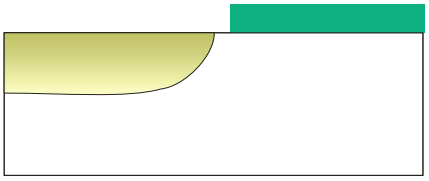
Oxygen Plasma etching

Equipment: Ultra Clean Line, CR125C
Standard wafer cleaning:

a. beaker 1 - fuming HNO_3, 5 min.
b. beaker 2 - fuming HNO_3, 5 min.
c. rinse in DI water, QDR until 1/R<0.1 μS
d. boiling HNO_3 69%, 10 min.
e. rinse in DI water, QDR until 1/R<0.1 μS
f. spin dry

Removal of native oxide: 1% HF, ~ 1 min

g. rinse in DI water, QDR until 1/R<0.1 μS
h. boiling HNO_3 69%, 10 min.
i. rinse in DI water, QDR until 1/R<0.1 μS
j. spin dry



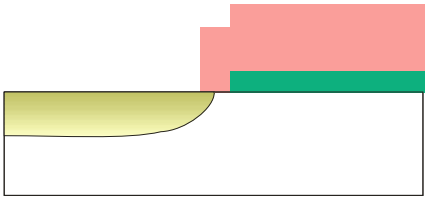
12. forming of dislocation loops outside the junction

O-Rmid-S: 02-05 (total process time ≈ 45 min)
process parameters:

temperature cycle [°C]	ramp up/down [°C/min]	ambient	process time [min]	gas flow [slm]
800-900	10	O_2/HCl	10	4
900		N2	Wait for peddle	
900		N_2	19	4
900		O_2	1	4
900		N_2	Paddle out	4
900-800	7.5	N_2	14	4

13. Lithography: Masking for low energy Implantation (mask 2)

The same step 8



14. Silicon Implantation
(forming dislocation loops inside the juction)

Process parameters:

implantation species	dose/cm^2	implantation value [μC]	acceleration voltage [kV]	mass magnet [amu]	2nd magnet [A]
Si^+	**1.0x10^{15}**	533.4	260 200	28	

Projected range for 260keV ~ 0.418 micro
Junction depth ~ 1.135 micro

15. Removal of resist

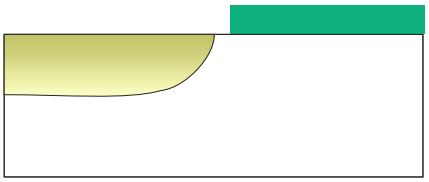
Oxygen Plasma etching

Equipment: Ultra Clean Line, CR125C
Standard wafer cleaning:

k. beaker 1 - fuming HNO_3, 5 min.
l. beaker 2 - fuming HNO_3, 5 min.
m. rinse in DI water, QDR until 1/R<0.1 μS
n. boiling HNO_3 69%, 10 min.
o. rinse in DI water, QDR until 1/R<0.1 μS
p. spin dry

Removal of native oxide: 1% HF, ~ 1 min

q. rinse in DI water, QDR until 1/R<0.1 μS
r. boiling HNO_3 69%, 10 min.
s. rinse in DI water, QDR until 1/R<0.1 μS
t. spin dry



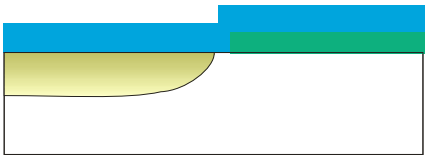
16. forming of dislocation loops inside the junction

O-Rmid-S: 02-05 (total process time ≈ 45 min)
process parameters:

temperature cycle [°C]	ramp up/down [°C/min]	ambient	process time [min]	gas flow [slm]
800-900	10	O_2/HCl	10	4
900		N2	Wait for peddle	
900		N_2	19	4
900		O_2	1	4
900		N_2	Paddle out	4
900-800	7.5	N_2	14	4

17. Deposit undoped Silox layer: Optimize optical characteristics

(SiO2 thickness ~ wavelength/4*n_{ox} = 162 nm)

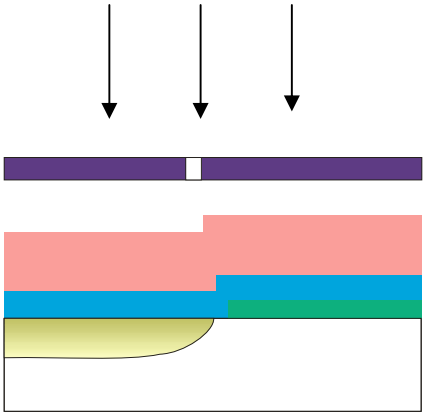


18. Contact opening lithography (mask 4)

Equipment: Semi automated resist spinner CR117B
Karl Süss Mask Aligner MA55, CR119B
Developer, CR112B

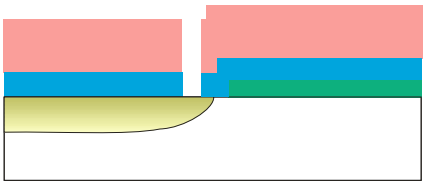
a. Apply primer
b. Spin on photo-resist (type 907.17, program 6)
c. RPM=4000, time=20 s, resist thickness=1.5μm
d. Soft bake: 60 sec, 95 °C
e. Align mask
f. Expose to UV-light (vacuum contact, 5 sec)
g. After-exposure bake (1 min, 120 °C)
h. Develop (50 s)
i. Check the features

Post bake 15 min, 120 °C.



19. Contact opening to P region

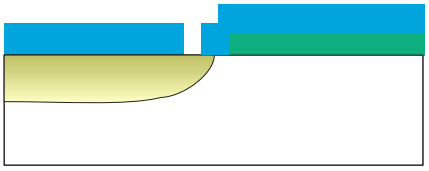
BHF (80 nm/min) -



20. Removal of resist

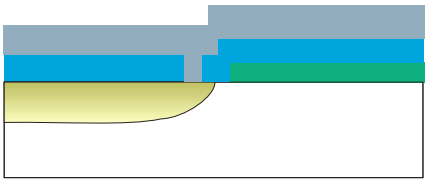
Equipment: Ultra Clean Line, CR125C
Standard wafer cleaning:

a. beaker 1 - fuming HNO_3, 5 min.
b. beaker 2 - fuming HNO_3, 5 min.
c. rinse in DI water, QDR until 1/R<0.1 μS
d. boiling HNO_3 69%, 10 min.
e. rinse in DI water, QDR until 1/R<0.1 μS
f. spin dry



21. Deposition of 70 nm TiW and 1 μm Al

1μm Al sputtering (Oxford)

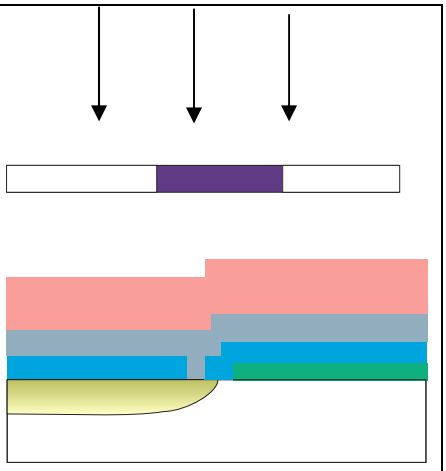


22. Aluminum lithography (mask 3)

Equipment: Semi automated resist spinner CR117B
Karl Süss Mask Aligner MA45, CR119B
Developer, CR112B

a. Apply primer
b. Spin on photo-resist (type 907.17, program 6)
c. RPM=4000, time=20 s, resist thickness=1.5μm
d. Soft bake: 60 sec, 95 °C
e. Align mask
f. Expose to UV-light (vacuum contact, 5 sec)
g. After-exposure bake (1 min, 120 °C)
h. Develop (50 s)
i. Check the features

Post bake 15 min, 120 °C.



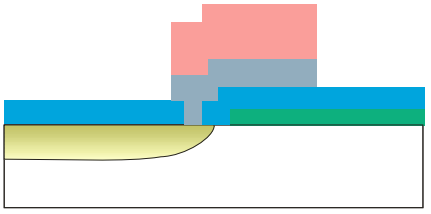
23. Al and TiW etch

Etch 1 micro Al

fuming H_3PO_4	etch rate Al [nm/min]	process time [min]
55^0C		

Etch 70 nm TiW

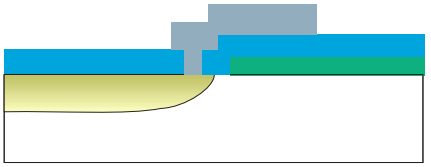
H_2O_2 30%	etch rate Al [nm/min]	process time [min]
23^0C	~10	7



24. Removal of resist

Equipment: Ultra Clean Line, CR125C
Standard wafer cleaning:

a. beaker 1 - fuming HNO_3, 5 min.
b. beaker 2 - fuming HNO_3, 5 min.
c. rinse in DI water, QDR until 1/R<0.1 μS
d. spin dry



25. Cover front side with resist for sputtering back side

process parameters:

resist	thickness [μm]	post-bake (100°C) [min]
S1818	1.8	30

26. Deposition of 350 nm Al from backside

Recipe Nordiko: 5 (process time each wafer 10 min)

gas flow Ar [sccm]	pressure [μbar]	power [Watt]	V_{dc} [Volt]	sputter rate [nm/min]	projected thickness [μm]	sputter time [min]
?	?	?	?	75	1	5

<table>
<tr>
<td>27. Removal of resist
process parameters:
<table><tr><th>fuming HNO_3</th><th>process time [min]</th></tr><tr><td>100 %</td><td>10</td></tr></table></td>
<td></td>
</tr>
<tr>
<td>22. PMA (sintering of the Al)</td>
<td></td>
</tr>
</table>

Appendix E – Encountered difficulties while measuring

A general encountered problem was a different background value (“offset”) in light intensity each time the Spectro 320 - the Universal Spectrum Analyzer, spectrometer was switched on. The measured light intensity values are corrected for this change in offset.

Figure below depicts 2 different background values for the same DILED device when the Universal Spectrum Analyzer was switched off and on again:

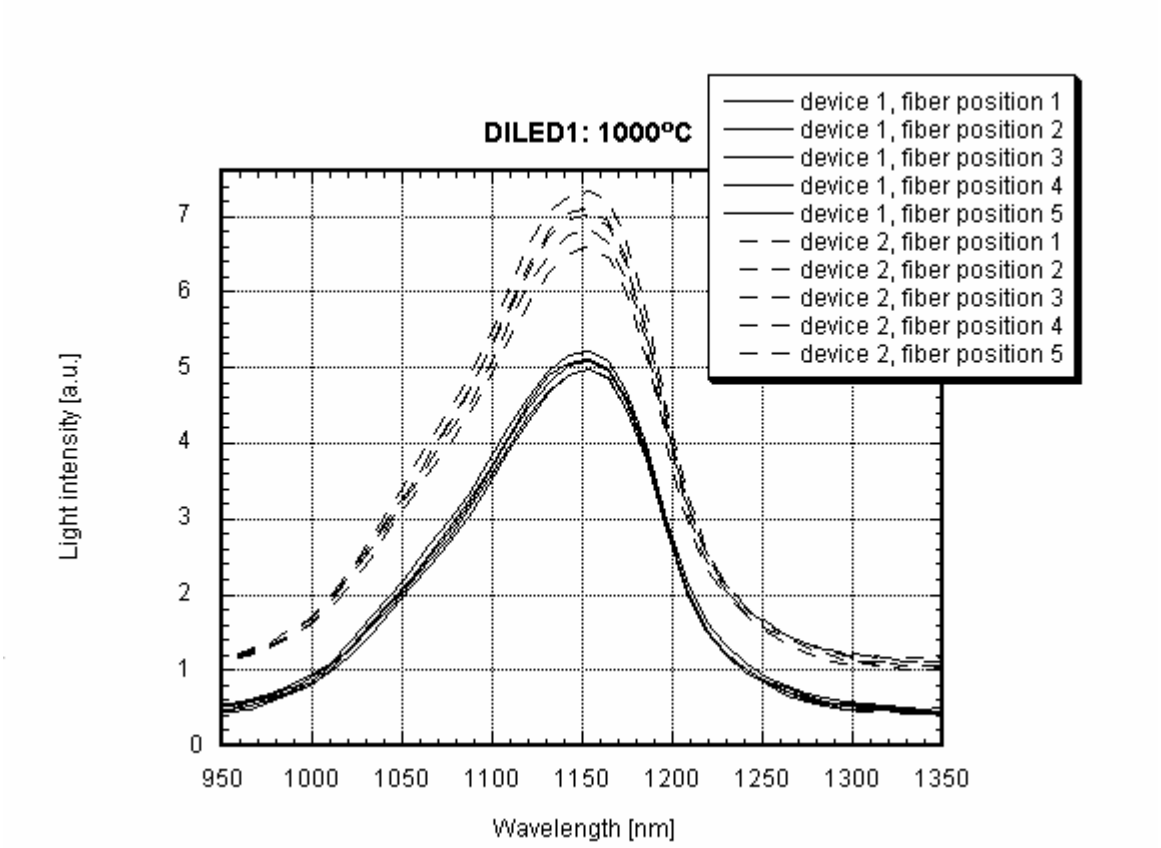


Figure C-1: Different background level each time spectrometer was switched on.

A more specific problem has to do with device type 40keV & 1000°C (B1WW1). It turned out that this type of device belonged to another batch then the rest of the DILED1 devices. The obtained maximum light intensity deviated significantly from a clear trend in maximum light intensity versus annealing temperature. Therefore the 40keV & 1000°C (B1WW1) results have been discarded.

Figure below shows the deviation of the 40keV & 1000°C type of device from a clear trend:

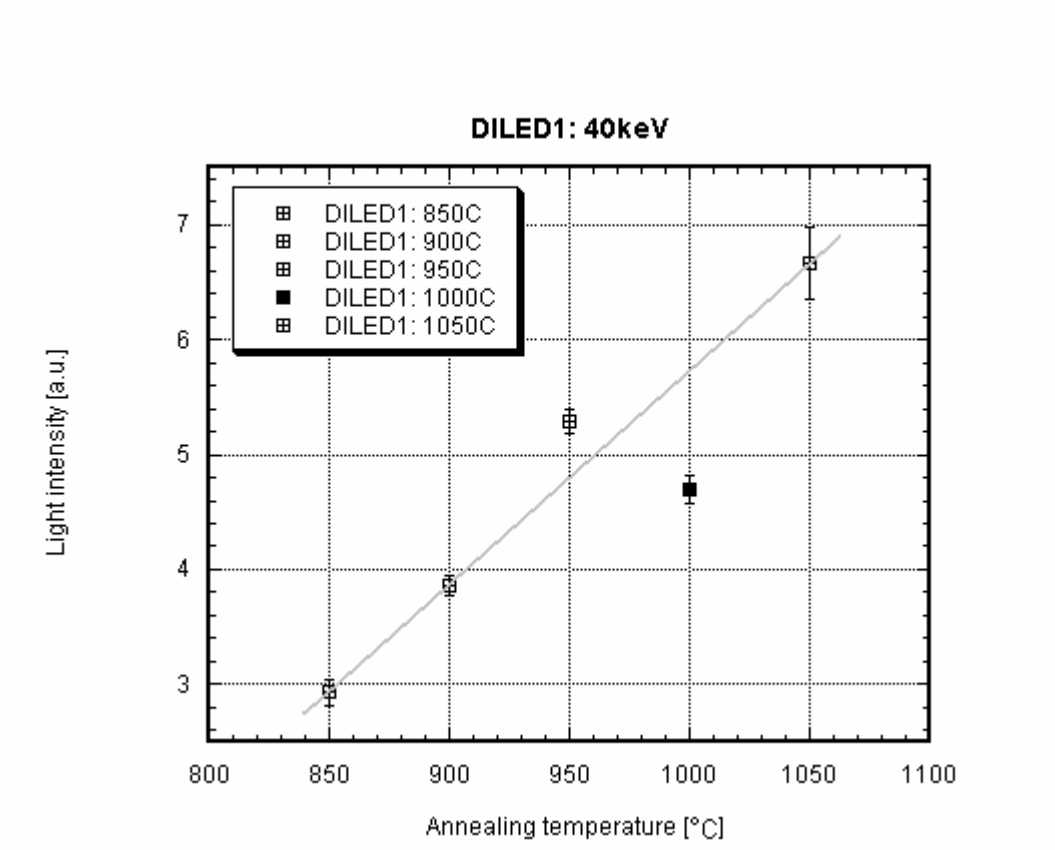


Figure C-2: DILED1 1000°C originating from a different batch was rejected.

Device types 70keV & 1050°C (B2) and 100keV & 1050°C (B3) within the first set DILED1 showed some difficulties measuring the I-V diode characteristics, because dielectric material e.g. SiO_2 or Si_3N_4 had not been etched completely away.

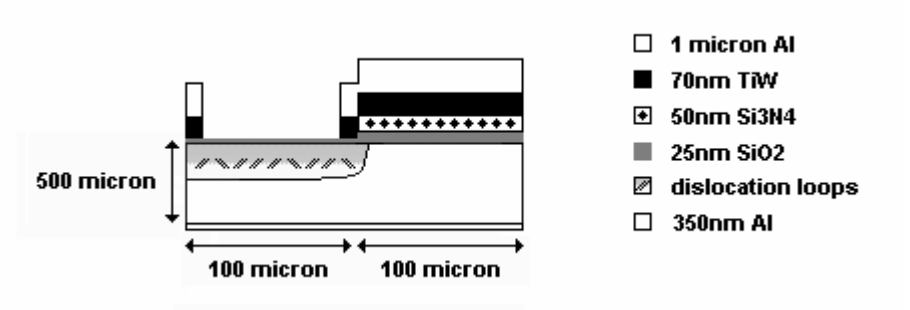


Figure C-3: DILED1 70 & 100keV cross-section with SiO_2 film on light emitting surface area.

It turned out that 50% of the 70keV & 1050°C (393) devices required an breakdown to get good contact with the actual junction diode. 100% of the 100keV & 1050°C (187) type of devices required such a breakdown.

Device type 260keV (3310-2) within the third set DIFLED showed some difficulties pumping 100mA through it within an applied voltage range of 20V. The upper limit of the equipment is 20W.

Figure below shows extraordinary high Ohmic resistance. These difficulties have been assigned to photo resist not rinsed of the aluminum contact area. Fortunately some devices just allowed pumping 100mA at 20V:

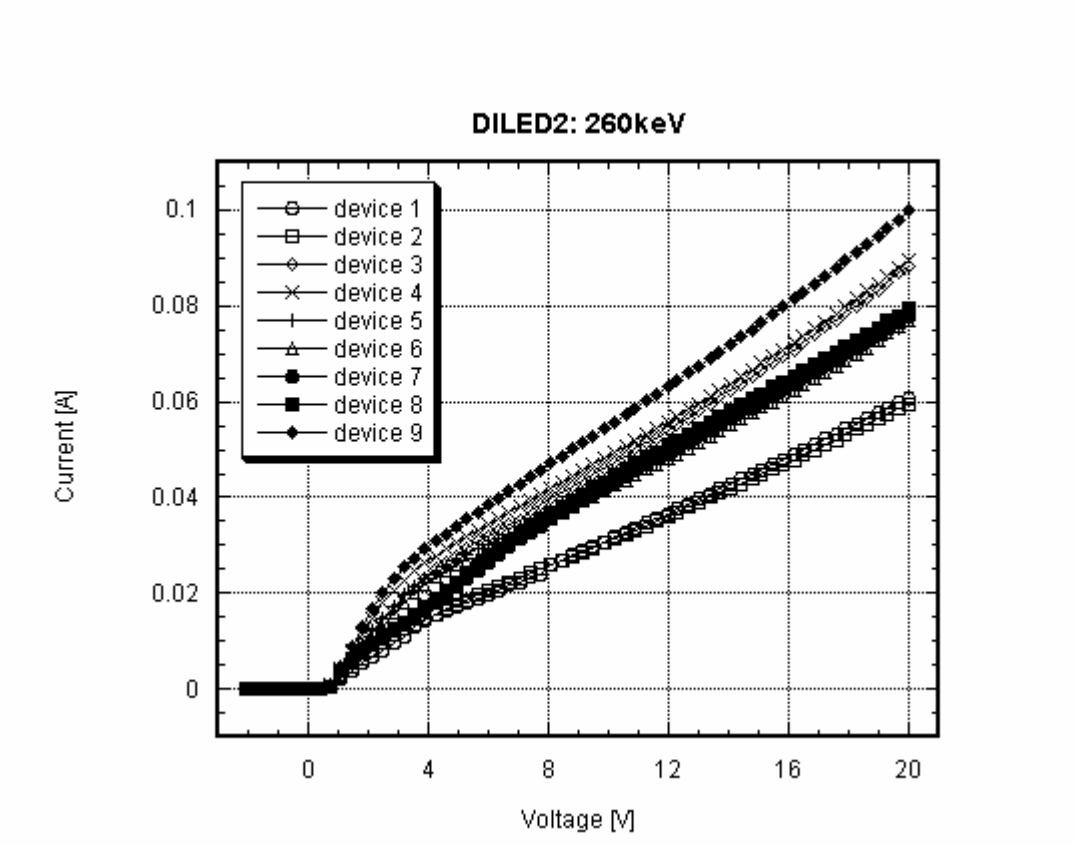
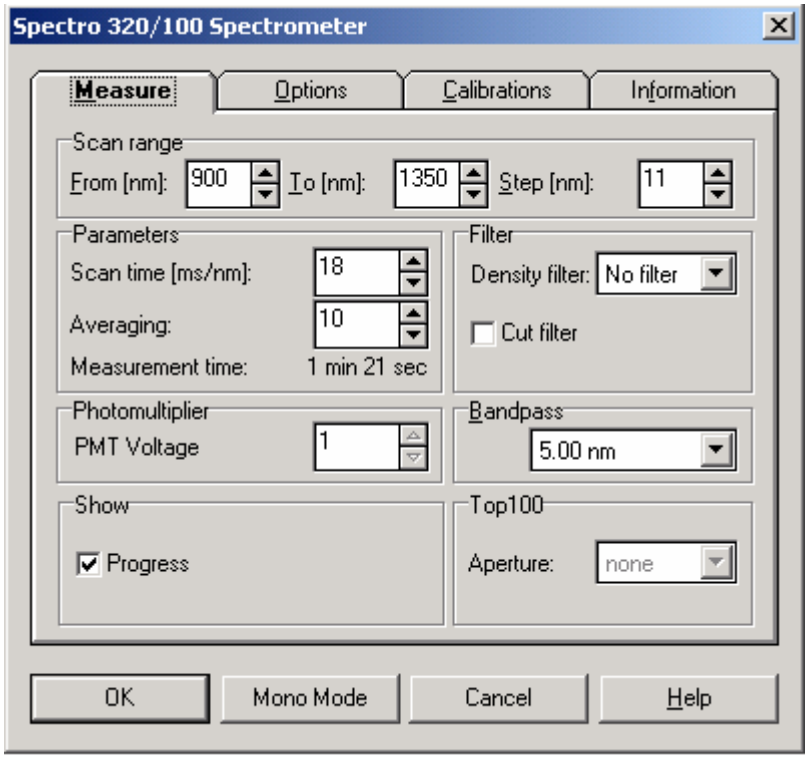


Figure C-4: Photo resist on topside contact increases resistance.

Appendix F – Specwin software settings



Appendix G – Measurement results

Electrical parameters

DILED1	100mA voltage	Photo current	Saturation current	Thermal voltage equivalent	Ideality factor	Junction voltage	Bulk resistance
	$V_{I=100mA}$	$I_{V=0}$	I_0	V_{th}	m	V_j	R_{BULK}
	V	pA	fA	mV	-	mV	Ω
850°C 40keV	2.16	-0.749	1.15	26.0	1.03	835	13.3
900°C 40keV	1.97	-0.816	0.941	25.7	1.02	830	11.4
950°C 40keV	2.16	-1.97	1.04	25.8	1.02	831	13.3
1000°C 40keV	X	X	X	X	X	X	X
1050°C 40keV	1.58	-0.162	1.71	26.2	1.04	831	7.49
1050°C 70keV	2.60	-0.179	4.22	26.8	1.06	825	17.7
1050°C 100keV	4.50	-0.0766	3.12	26.4	1.05	821	36.8

DILED2	100mA voltage	Photo current	Saturation current	Thermal voltage equivalent	Ideality factor	Junction voltage	Bulk resistance
	V_{100mA}	$I_{Va=0}$	I_0	V_{th}	m	V_j	R_{BULK}
	V	pA	fA	mV	-	mV	Ω
40keV 950°C $1.2x10^{15}$ cm^{-2}	4.50	-1.39	1.15	25.5	1.01	818	36.8
50keV 950°C $1.37x10^{15}$ cm^{-2}	4.50	-0.904	1.27	25.7	1.02	822	36.8
70keV 950°C $1.6x10^{15}$ cm^{-2}	4.50	-1.20	1.27	25.7	1.02	822	36.8
40keV 1100°C $1.2x10^{15}$ cm^{-2}	4.50	-1.98	7.35	27.5	1.09	832	36.7
50keV 1100°C $1.37x10^{15}$ cm^{-2}	4.50	-0.822	3.45	26.5	1.05	821	36.8
70keV 1100°C & $1.6x10^{15}$ cm^{-2}	4.31	-0.713	2.56	26.2	1.04	820	34.9

DIFLED	100mA voltage	Photo current	Saturation current	Thermal voltage equivalent	Ideality factor	Junction voltage	Bulk resistance
	V_{100mA}	$I_{Va=0}$	I_0	V_{th}	m	V_j	R_{BULK}
	V	pA	pA	mV	-	mV	Ω
450keV	6.12	-19.8	37.8	39.9	1.58	866	52.5
200keV	6.12	-0.461	0.0127	28.1	1.12	834	52.9
200+450keV	6.56	-4.12	5.11	35.9	1.42	851	57.1
No	5.68	-0.281	0.0015	25.7	1.02	825	48.6
360keV	7.56	-1.33	0.566	32.8	1.30	849	67.1
260keV	X	X	X	X	X	X	X
360+260keV	8.76	-1.58	0.0513	30.3	1.20	857	79.0
No	6.78	-0.443	0.0015	25.7	1.02	825	59.2

Optical parameters

DILED1	Average peak intensity	Standard deviation peak intensity
	I_{PEAK}	$I_{PEAK-DEVIATION}$
	a.u.	%
850°C 40keV	2.93	3.75
900°C 40keV	3.86	2.10
950°C 40keV	5.29	2.07
1050°C 40keV	6.67	4.75
1050°C 70keV	9.33	26.9
1050°C 100k	6.59	26.7

DILED2	Average peak intensity	Standard deviation peak intensity
	I_{PEAK}	$I_{PEAK-DEVIATION}$
	a.u.	%
40keV 950°C $1.2x10^{15}$ cm^{-2}	8.11	3.99
50keV 950°C $1.37x10^{15}$ cm^{-2}	9.38	4.84
70keV 950°C $1.6x10^{15}$ cm^{-2}	9.65	6.24
40keV 1100°C $1.2x10^{15}$ cm^{-2}	28.8	3.99
50keV 1100°C $1.37x10^{15}$ cm^{-2}	27.1	2.66
70keV 1100°C $1.6x10^{15}$ cm^{-2}	27.4	3.03

DIFLED	Average peak intensity	Standard deviation peak intensity
	I_{PEAK}	$I_{PEAK-DEVIATION}$
	a.u.	%
450keV	1.60	8.94
200keV	3.90	6.42
200+450k	1.54	12.8
No	21.8	1.35
360keV	2.08	6.51
260keV	3.36	1.28
260+360k	1.67	5.61
No	24.2	3.74

Appendix H – Silvaco Virtual Wafer Fab simulations of dislocation engineered silicon Light Emitting Diodes

In publications 3 mechanisms have been proposed that should explain light emission behavior of silicon Light Emitting Diodes as function of annealing temperature. It should be mentioned that these proposals are not well substantiated i.e. they are not convincingly confirmed or rejected over the total temperature range of 700–1200°C.

- Proposal by Lourenco

Light intensity as function of annealing temperature is directly proportional to recombination rate as function of annealing temperature.

- Proposal by Sobolev

Light intensity as function of annealing temperature is directly proportional to minority carrier lifetime as function

of annealing temperature.

The third proposal is most difficult to underline either by experiment or simulation. People in this particular field do not reject this idea, but have not been able to confirm or reject it.

- Proposal by dislocation engineering scientific community

Light intensity as function of annealing temperature is directly proportional to the number of impurities e.g.

Aluminum, decorating the dislocation loops as function of temperature.

These proposals are worth examining. This simulation script was part of a first effort to run a reliable simulation. However until now the results have been below “master thesis” standard.

Athena script

```
# START STRUCTURE SPECIFICATION

go athena

# THIS MESH WILL BE DISCARDED IN DEVEDIT (it serves to create a structure in
ATHENA)

# LED dimension (width)
line x loc=0.00 spac=0.5
line x loc=4.00 spac=0.5
line x loc=50.00 spac=5
line x loc=96 spac=0.5
line x loc=100 spac=0.5
line x loc=200 spac=25

# LED dimension (depth)
line y loc=0.0 spac=0.02
line y loc=0.25 spac=0.1
line y loc=0.9 spac=0.02
line y loc=3.0 spac=1
line y loc=500 spac=100

# Measurements show dominant bulk resistance, y-scaling not possible
# intense mesh at junction depth: ~0.5
# vacancies levels return to normal at etch of depletion region (within 2 micron).
Thus interstitial diffusion not included in model.
```

```
# 1.1 Starting material after wafer cleaning
init silicon phosphor resistivity=10 orientation=100

# 1.2 Growth of 25nm pad oxide (oxidation: method compress or viscous)

method viscous
diffus temp=800 t.final=950 time=15 dryo2
diffus temp=950 time=31 dryo2
diffus temp=950 time=20 nitrogen
diffus temp=950 t.final=800 time=20 nitrogen

# diffusion process inaccurate-> make sure padoxide = 25nm
extract name="padoxide" thickness material="SiO~2" mat.occno=1 x.val=0.5

# 1.3 Depostion of 50nm LPCVD Si3N4

deposit nitride thick=0.05 divisions=5 dy=0.01

# 1.4 Definition of active area (resist layer acts as implant mask)
deposit photoresist thick=1.6 divisions=5 dy=0.32

# Etching of photoresist
etch photoresist left p1.x=100

# 1.5 Plasma etching of Si3N4
etch nitride left p1.x=100 p1.y=-1.5 p2.x=100 p2.y=0.5

# 2.1 P-well implantation through pad oxide for shallow junction formation
# energy for resp. B1, B2 and B3 = 40,70,100

implant boron dose=1.0e15 energy=40 tilt=0 rotation=0 crystal

# Introduction of dislocation loops between indicated boron  concentrations.
Dislocation loops act as interstitial sink. Fact  indicates No. of interstitials
generated for each implanted boron species that is trapped by dislocation loops)

# cluster min.clus & max.clus from "literature report"
# method I.Loop.Sink
# cluster min.clus=1.6e19 max.clus=7.8e20
# clust.fact=10 boron

# 2.2 Resist removal and cleaning
etch photoresist all

# 2.3 Formation of loops by temperature step (diffusion)
annealing cycle for B2 & B3:

diffus temp=800 t.final=850 time=5 dryo2
diffus temp=850 time=19 nitrogen
diffus temp=850 time=1 dryo2
diffus temp=850 t.final=800 time=6.6 nitrogen

# annealing cycles for B1: 850,900,950,1000,1050 for 19 minutes in nitrogen

# 4.1 Removal of pad oxide
etch oxide left p1.x=100 p1.y=-1.5 p2.x=100 p2.y=0.5

# 4.2 Deposition of 70nm TiW and 1micron Al

deposit titanium thick=0.07 divisions=5 dy=0.014
```

```
deposit aluminum thick=1.00 dy=0.2

# 4.3-4.5 Definition of interconnect and etch of aluminium
(overlapp metal contact-photo diode emission area = 8%)

etch aluminum start x=4 y=-1.5
etch continue x=96 y=-1.5
etch continue x=96 y=0.5
etch done x=4 y=0.5

etch titanium start x=4 y=-1.5
etch continue x=96 y=-1.5
etch continue x=96 y=0.5
etch done x=4 y=0.5

electrode name=anode x=98
electrode name=anode x=0

# 4.6 Sintering of Aluminum (temperature step for chemical bonding to get Ohmic
contact - minimum temp = 474.85 for impurity diffusion)
diffus time=10 temp=400 f.h2o=2.0 f.n2=2.0

# 5.1-5.3 Backside metallization (virtual deposition of 350nm Al)
electr  backside name=cathode

structure outf=DILED40k850.str
save outfile=DILED40k850.str

# Extract junction depth in Athena
extract name="Junctiondepth" xj material="Silicon" mat.occno=1 x.val=50.0 \
        junc.occno=1 datafile="junction depth"

# END STRUCTURE SPECIFICATION

# Including ATLAS output in the structure file enables remeshing for these outputs
(These outputs show up in Refine on Quantities option in Devedit)

go atlas

# MATERIALS MODELS SPECIFICATION

# Specifying contact characteristics
# current or voltage controlled (default voltage):
# Specifying material properties

material taup0=2.e-6 taun0=2.e-6

# minority carrier lifetimes taup & taun from silicon photo diode examples

# Specifying interface properties

# Specifying physical models

# bipolar models are: conmob fldmob bgn consrh auger
models bipolar bbt.std print
impact selb

# output included in *.str file (NOTE: only last active output statement shows up
in structure file)
```

```
# output u.radiative recomb taurn e.velocity ex.velocity ey.velocity e.mobility
taurp h.velocity hx.velocity hy.velocity h.mobility con.band val.band

# NUMERICAL METHOD SELECTION
method newton trap maxtrap=10

# SOLUTION SPECIFICATION

# Voltage ramping to generate VI diode curve
# contact name=anode
# solve init
# log outf=I_anode.log
# solve vanode=0.0015 vstep=0.2 vfinal=4.5 name=anode
# tonyplot I_anode.log

# Switch to current controlled to force 100mA
 contact name=anode current
 solve init
# log outf=V_anode.log
 solve ianode=0.000887
# tonyplot V_anode.log

# RESULT ANALYSIS
save outfile=DILED40k850.str
tonyplot DILED40k850.str

# MANUAL REMESHING BY DEVEDIT (result Devedit remeshing is remeshDILED40k850.str,
This file is loaded into file remeshDILED40k850.in)

quit
```

Atlas script

```
go atlas

# LOADING remeshDILED40k850.str
mesh infile=remeshDILED40k850.str

# MATERIALS MODELS SPECIFICATION

# Specifying contact characteristics
# current or voltage controlled (default voltage):
# Specifying material properties
material taup0=2.e-6 taun0=2.e-6

# minority carrier lifetimes taup & taun from silicon photo diode examples

# Specifying interface properties

# Specifying physical models

# bipolar models are: conmob fldmob bgn consrh auger
models bipolar bbt.std print
impact selb

# output included in *.str file (NOTE: only last active output statement shows up
in structure file)

output u.radiative recomb taurn e.velocity ex.velocity ey.velocity e.mobility
taurp h.velocity hx.velocity hy.velocity h.mobility con.band val.band
```

```
# NUMERICAL METHOD SELECTION
method newton trap maxtrap=10

# SOLUTION SPECIFICATION

# Voltage ramping to generate VI diode curve
# contact name=anode
# solve init
# log outf=I_anode.log
# solve vanode=0.0015 vstep=0.2 vfinal=4.5 name=anode
# tonyplot I_anode.log

# Switch to current controlled to force 100mA
 contact name=anode current
 solve init
# log outf=V_anode.log
 solve ianode=0.000887
# tonyplot V_anode.log

# DILED40k850C: 0.0887A at 1.97V with ~11% deviation
# The calculated voltage on the electrode with current boundary conditions is
stored as the internal bias

# RESULT ANALYSIS
save outfile=DILED40k850.str
tonyplot DILED40k850.str

quit
```