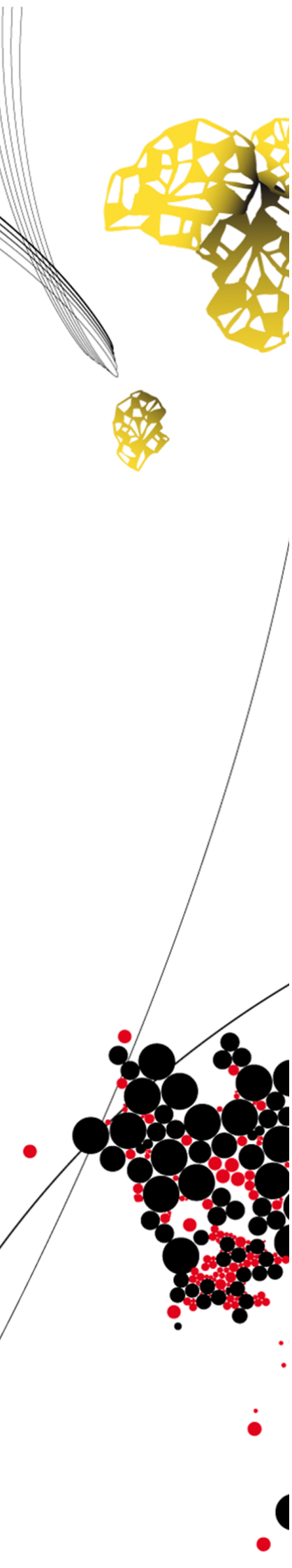

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An interference-robust wideband low-noise amplifier with balanced outputs

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MSc. Thesis
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Abstract

This thesis presents a noise-canceling LNA based on a complementary common-gate common-source combination. It provides active balun functionality with a single-ended input that is power matched to the antenna and a differential current output driving a passive mixer. By allowing class AB operation for both outputs, the LNA achieves a high compression point and its outputs remain balanced under interference, while consuming relatively little power. The inductorless design can be fully integrated in a CMOS integrated circuit process and achieves more than a decade of bandwidth.

Contents

1 Introduction

Traditional receivers are designed for a single standard with channel selection and demodulation done in hardware. In a software defined radio (SDR) a wideband analog-to-digital converter (ADC) captures all channels and the desired channel is extracted and demodulated in software [1]. The flexibility of software allows a single receiver to support multiple wireless standards, provided that the analog front-end covers the relevant RF-bands. This requires a wideband low-noise amplifier. The downside of receiving multiple standard concurrently is that it requires a stronger interference robustness. Communication standards set levels to the minimum received wanted signal and maximum received interferer levels. When multiple standards are received simultaneously, low received powers from one standard are combined with high interferer levels from other standards. [2]

A typical SDR analog front-end consists of

- a wideband low-noise amplifier (LNA) amplifying the signal so that the noise contribution of following blocks is reduced
- a quadrature mixer that down-converts the desired band to zero-IF
- an intermediate frequency (IF) filter that removes signals falling outside the bandwidth of the ADC
- an IF-amplifier that amplifies the signal to a level suitable for analog to digital conversion

This gives the block schematic shown in Fig. 1.1. To reduce cost and size all these functions are preferably all performed on one CMOS chip with the least possible ammount of external components. One of those components is the balun, which converts the single-ended signal from the antenna to the balanced differential signal preferred on chip. Traditionally a balun is an electrical transformer, but the 3D nature of a transformer makes it difficult to integrate in a planar IC-process. More suited for integration are so-called 'active baluns' [3–10], different from passive devices, active devices however produce noise. They can have gain and thereby reduce the noise contribution of later stages, but this gives a proportional reduction of the overall linearity. For this reason balun and LNA a preferably combined by making the unbalanced-to-balanced conversion an integral part of the low-noise amplifier, giving a so-called balun-LNA.

1.1 Aim of the project

In [11] an interference-robust front-end for SDR was presented, using a topology similar to Fig. 1.2 except it still needs an off-chip balun. The goal of this thesis is to obtain an integrated class AB LNA for such an interference-robust, wideband receiver front-end which does not require a balun.

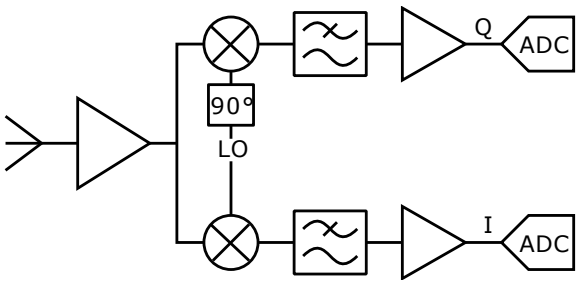


Fig. 1.1: Generic block schematic of an SDR receiver front-end

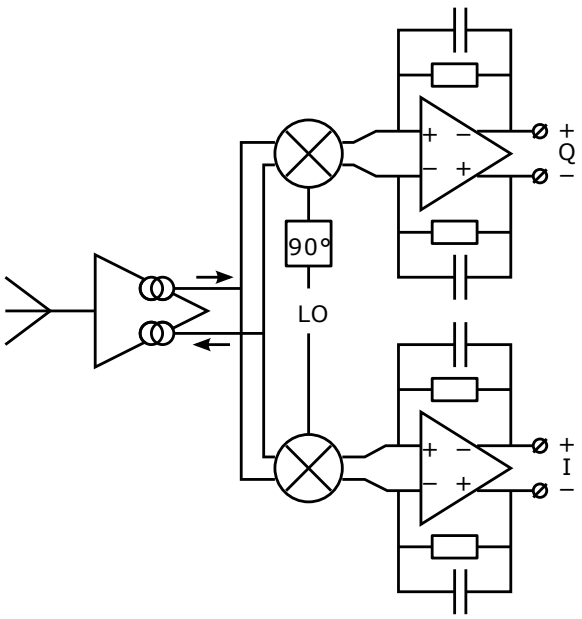


Fig. 1.2: Front-end topology used in this thesis

Class AB operation is wanted because strong interferer handling capabilities should not come at the direct cost of a high power consumption. Since the LNA should directly interface with the antenna the input is single ended and the input impedance must be matched to the antenna impedance. The on-chip connections are all differential, rejecting the interference which is mostly common-mode when the chip is properly layed out.

The output of the LNA is a current which drives a passive current-switching mixer, which in its turn feeds a transimpedance amplifier (TIA). The TIA consists of an operational transconductance amplifier (OTA) with an RC feedback network giving some first-order filtering. The ouputs of the TIA are the in-phase (I) and quadrature (Q) signals in the voltage domain that can be demodulated in the digital domain after analog-to-digital conversion. This topology needs no voltage gain at RF and thereby avoids a direct trade-off between supply voltage (which is very limited in modern CMOS processes) and maximally allowed input swing.

Because they operate in anti-phase, the transcondances of the output transistors in the LNA may change in opposite direction in the presence of a strong interferer. This means that the output becomes unbalanced. This effect is demonstrated in chapter 8 using a previously published LNA with differential outputs. An increase in imbalance leads to an increase in second-order distortion as explained in section 2.3. This thesis aims for an LNA design in which the balance is robust to interference,

Next to this aim the following requirements should be met:

- The RF band covered should include the UHF television band (470 - 870 MHz) and the various mobile telecommunication bands such as UMTS (2.0 - 2.15 GHz). For this reason the RF band runs from 400 MHz to 2.5 GHz.
- For wideband applications there is a big chance some strong interferer (TV, GSM) is present in the RF band, and this single interferer may potentially block all other signals. Hence the front-end must have a high compression point of at least 0 dBm. At an impedance level of 50Ω this means an input voltage of 632 mVpp and an input current of 12.6 mApp.
- To avoid reflection at the input which can adversely affect the frequency characteristics the input of the receiver must be matched to the antenna. The antenna is modeled as a simple 50 Ω resistor in this report and the input reflection coefficient (S_{11}) should be less than -10 dB.

- Interferers in the RF band may create intermodulation products in the LNA and mixer that interfere with the signal to be received. The goal is a third-order intercept point (IIP3) of at least 12 dBm.

1.2 Outline of the report

In chapter 2 the mixer and IF-amplifier are briefly described. In chapter 3 a new LNA topology is proposed and discussed qualitatively. Next its performance is analyzed, starting with the two essential properties of an LNA in chapter 4: gain and noise. Since it has to be a wideband LNA the frequency response and matching are described chapters 5 and 6 respectively, which concludes the linear analysis. Then the effects of common-mode and differential-mode nonlinearity are described in chapter 7. The theory described therein is applied to a previously published design to show its limitations in chapter 8. The nonlinearity (including balance) of the proposed LNA are described from two perspectives, a small-signal approximation using a the first three terms of a Taylor Series in chapter 9 and using a large-signal model in chapter 10. Based on the analysis in the previous chapters and the trade-offs found therein, chapter 11 gives a design procedure that allows the competing effects to be brought together in such a way that the requirements of section 1.1 are satisfied. This design strategy is applied to a 0.14 µm CMOS process in chapter 12. This implementation is simulated with Spectre, results of which are found in chapter 13. A look back to the key findings is given in chapter 14. Chapter 15 discusses some points for future research and concludes this report.

2 Mixer and IF-amplifier

The receiver front-end consists of an LNA, a mixer and an IF amplifier. The LNA is the main subject of this thesis and will be treated in detail in the following chapters. Of the other two blocks the operation is described with an emphasis on those properties important for the design of the LNA.

2.1 Operation

The current-switching mixer schematic is shown in Fig. 2.1. In Fig. 2.2 the idealized waveforms of the currents and voltages at the numbered wires are sketched for an (unrealistic[1]) RF to IF ratio of 3. To characterize its response to an unbalanced input signal the inputs are decomposed in common-mode and differential current, which are applied separately. The input signal comes from current sources I1 and I2, in Fig. 2.2a these are fully differential (wanted situation) and in Fig. 2.2b they are fully common-mode. Signals 3-10 show the pulses driving the switches, waveforms 11-18 show the input currents (1,2) chopped at the moment given by pulse trains 3-10. These are combined to form currents 19-22 which for differential inputs contains a component at the frequency difference between RF and LO, the wanted IF signal. This frequency is not present when a common-mode input is applied. This IF component is sketched as 23-26, which is also the output voltage of the TIA. Ideally the mixer thus fully rejects any common-mode component in the LNA output.

2.2 Imbalance in the mixer output

The previous section assumed a perfect 25% dutycyle for all phases, if these are however not exactly equal then an imbalance in the output current may arise. When the effective duty cycle, i.e. including the effects of mismatch, of the switches M3 to M6 is δ_3 to δ_6 then the amplitude of the output currents may be approximated[2] as:

$$i_{19} \propto i_1 \cdot \delta_3 - i_2 \cdot \delta_4$$

$$i_{20} \propto i_2 \cdot \delta_5 - i_1 \cdot \delta_6$$

In which the minus sign comes from the fact that the pulses at nodes 3 and 5 are in antiphase with those at 4 and 6. Imbalance corresponds to a common-mode component, which is

$$i_{19} + i_{20} \propto i_1 \cdot (\delta_3 - \delta_6) + i_2 \cdot (\delta_4 - \delta_5)$$

First of all this shows that if the duty cycles are equal there is no output imbalance, regardless of input balance. Secondly when the switches are identical, hence $\delta_3 = \delta_5$ and $\delta_4 = \delta_6$, there is no imbalance in the output current if the input current is balanced, even when the LO phases are unequal. The imbalance in the output of the mixer thus is a product of the imbalance of the LO and the LNA.

[1] Realistically this ratio is in the order of a hundred, which means that for one IF cycle the RF input has gone though 100 cycles, but this is very inconvenient to draw

[2] Two approximations are used: 1. It is assumed that the phase relation between the LO phases is maintained. 2. The fundamental component in the pulse wave is approximated as being proportional to the duty cycle, in reality the relation is sinusoidal.

2.3 Second-order intermodulation in the mixer

In wideband down conversion mixers two types of second-order intermodulation products are generated:

- A wideband second-order intermodulation product, which is due to intermodulation before down conversion. When the interfering tones are at frequencies f_1 and f_2 and the local oscillator (LO) frequency is f_{LO} this IM2 is located at $(f_1 - f_2) - f_{LO}$ at the output of the mixer. This product is called 'wideband' because to fall inside the zero-IF band the two-tone spacing of the interferers must be (slightly) bigger than the local oscillater frequency
- A narrowband second-order intermodulation product which is due to the intermodulation after down conversion. When the interfering tones are again f_1 and f_2 and the LO at f_{LO} this IM2 is located at $(f_1 - f_{LO}) - (f_2 - f_{LO}) = f_1 - f_2$ at the output of the mixer. This type of non-linearity mainly originates from the non-linear current splitting between two MOSFETs around the switching moment. [12] This product is called 'narrowband' because to fall inside the zero-IF band the two-tone spacing must be small.

After down conversion the balance is strongly depended on the duty cycle of the local oscillator as explained in the previous section. When the duty-cycle is exactly 25% for each phase the output currents at each terminal are equal but in anti-phase. As a result when each switching MOSFET is identical the second-order intermodulation component is common-mode and rejected by the differential IF amplifier.

The situation is different for the wideband intermodulation product, here the balance of the input current, i.e. the output of the LNA, matters. When there is an imbalance of ΔA in the output, which means that one normalized output current is $(1 + \Delta)$ and the other $(1 - \Delta)$, an incomplete cancellation of the quadratic term occurs:

$$(A + \Delta A)^2 - (A - \Delta A)^2 = 4\Delta A^2$$

In words: the wideband second-order intermodulation product is proportional to the imbalance of the output current of the LNA. To illustrate the effect of imbalance of intermodulation, the WB-IIP2 was obtained by simulating the mixer described above with

- Input tones at 1.05 GHz and 1.56 GHz and the LO at 500 MHz, which gives a WB-IM2 at 10 MHz
- A nominal source and drain voltage of 900 mV (half supply for this technology)
- Gate widths of 75 µm, drawn lengths of 0.16 µm (the minimum allowed by technology) and a DC gate voltage of 1.8 V. This means the switches operate in on-overlap with a drain source resistance of 23 Ω at the commutation moment.
- An LO swing of 800 mVpp with rise and fall times of 75 ps. This gives an on-resistance of 11.8 Ω.
- A two time current gain and 250 Ω single ended output resistance for the LNA.
- A load impedance of 10 Ω modeling the virtual-ground node of the IF amplifier

Fig. 2.3 shows the result of increasing imbalance, from an insignificant product the wideband second-order intermodulation product produced by the mixer may become the dominant source of second-order intermodulation. The IIP2 decreases by 6 dB for every doubling of the imbalance, which confirms that the wideband second-order intermodulation generated by the mixer is proportional to the output imbalance of the LNA.

2.4 TIA

With two inputs and two outputs there are four transfer functions describing the OTA, of which those three that involve a common-mode signal are ideally zero and the differential in to differential out transconductance is the wanted behavior. The common-mode output is normally set to a DC level by internal feedback in the OTA.

The differential input current to the TIA is split in three parts

1. the frequency components generated by the switching mixer and the interferers that fall well outside the IF band flow through a shunt capacitor
2. the interferers close to the IF band flow through a feedback capacitor into the OTA
3. the signal current flows through a resistor into the OTA

For linearity and power consumption it is beneficial to remove as much as possible the interferers before the OTA, i.e. using a big shunt capacitance, but this is likely to degrade the stability of the circuit.

Because the OTA ideally does not respond to common-mode input signals the common-mode input impedance of the TIA is much higher than the differential input impedance. To provide a low impedance path for common-mode components falling well outside of the IF band the shunt capacitance is connected to ground and not between the input terminals.

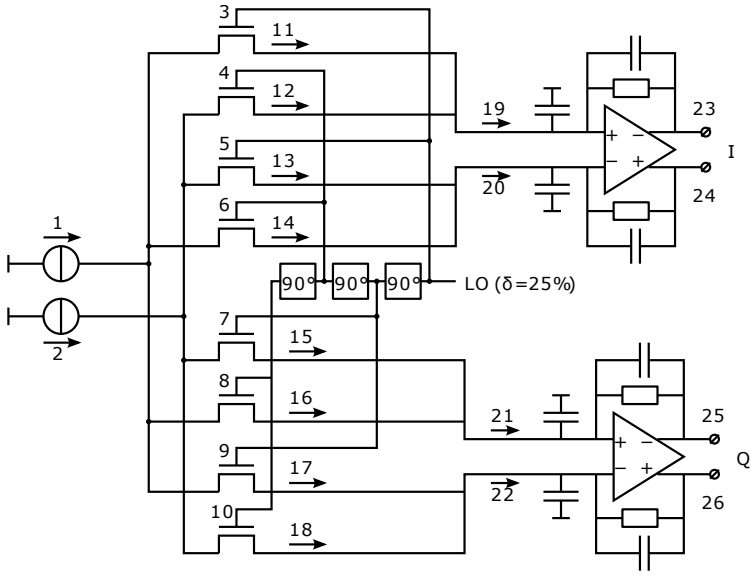
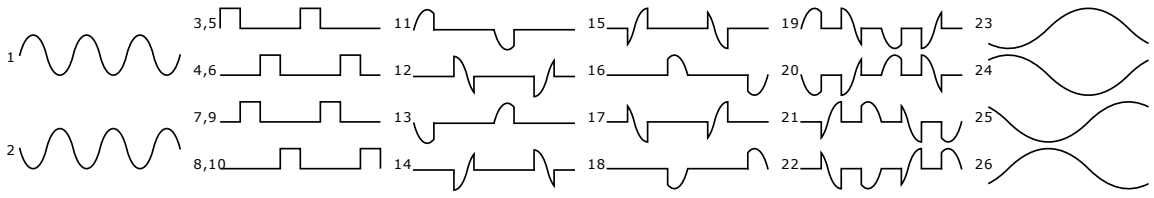
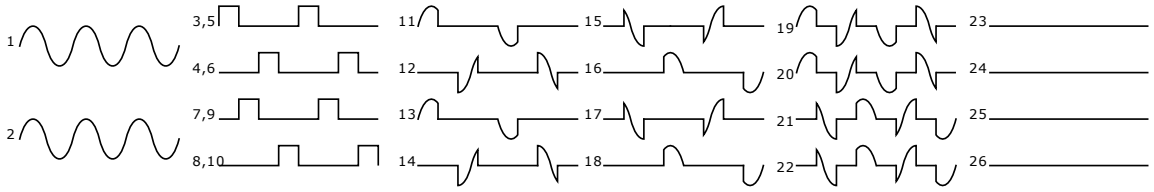


Fig. 2.1: Mixer and IF-TIA



(a) For differential input



(b) For common-mode input

Fig. 2.2: Ideal waveforms in mixer and IF-TIA

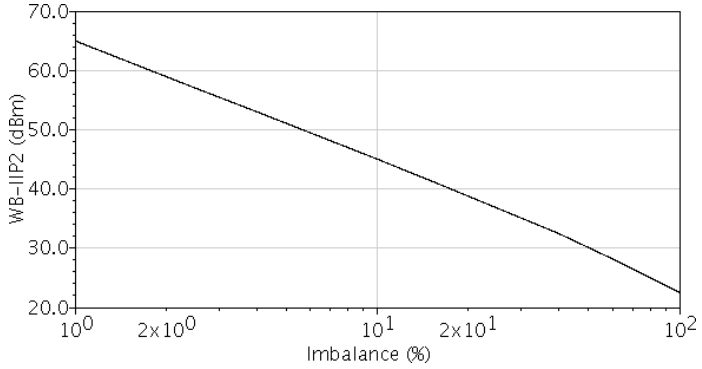


Fig. 2.3: Simulated WB-IIP2 as function of LNA output imbalance

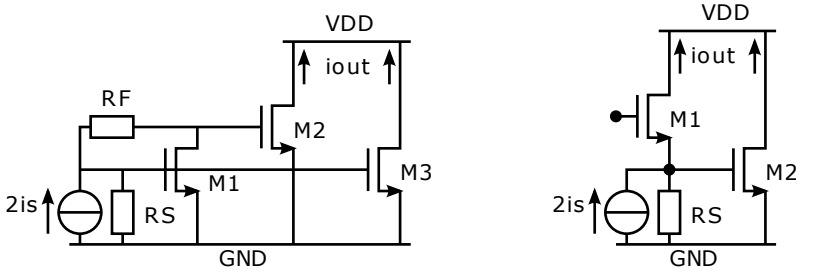
3 LNA topology

To make a class AB amplifier with current outputs PMOS transistors have to be used. The modest frequency requirements does not preclude the use of PMOS as amplifying element (transconductor) in a recent CMOS process and is a more optimal use of power than using it as a constant current source.

Noise canceling is a technique which breaks the traditional power consumption vs. noise trade-off arising when the input of an LNA has to be wideband matched. The noise generated by the matching device is feedforwarded via a second amplifying element such that at the output the noise adds up destructively. Fig. 3.1 shows the two noise canceling circuits from [13] that essentially have differential current outputs.

The circuit in Fig. 3.1a is unsuitable for large input swings since to avoid significant noise contribution by R_F the voltage gain $g_{m1} \cdot R_F$ must be several times. This proportionally lowers the IIP3 and compression point caused by M2. The one in Fig. 3.1b is however very suited since it has no voltage gain internally and can be converted into a class AB design by simply adding a complementary PMOS circuit on top, as shown in Fig. 3.2. This circuit is chosen as the LNA design in this report for the following reasons:

- The noise of the common-gate stage is canceled, giving a low noise figure.
- For square law-devices the circuit is linear, giving a high IIP2 and IIP3 and a well maintained balance under interference.
- The drain current is reused, giving doubled transconductance for the same quiescent current.
- The output current is not limited by a biasing current, giving a high compression point.



(a) Common-source with shunt-feedback [13, fig 6.5h]

(b) Common-gate and common-source combination [13, fig 6.5e]

Fig. 3.1: Noise canceling LNA's

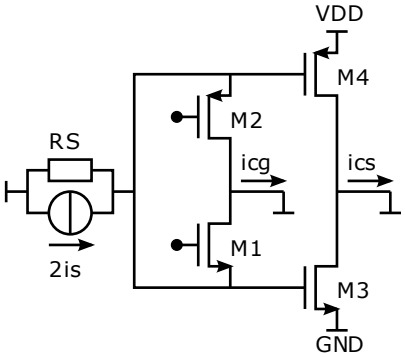
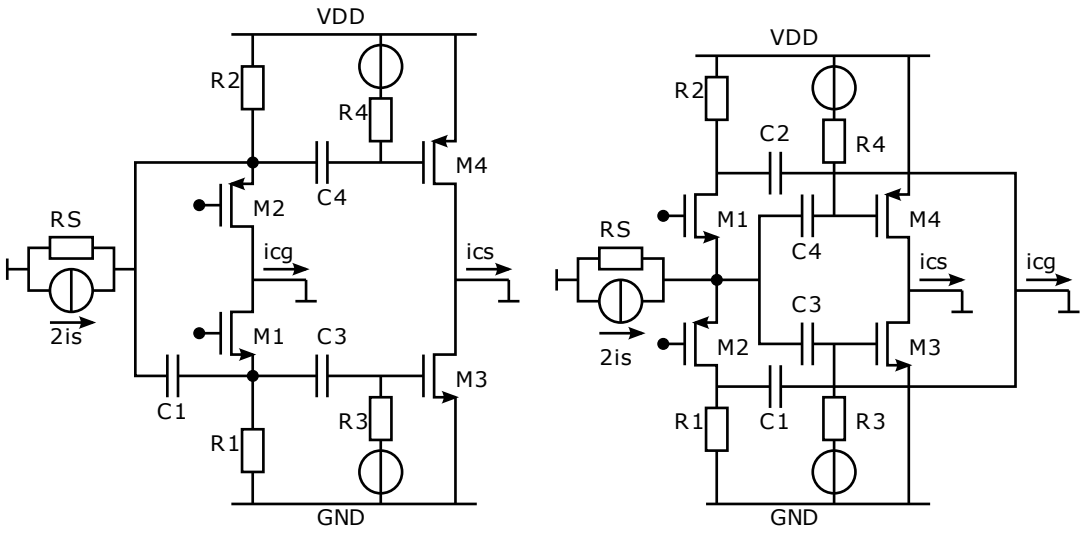


Fig. 3.2: Simplified schematic of the LNA proposed in this report



(a) Variant I (b) Variant II

Fig. 3.3: Schematics of the LNA designs with biasing circuits for M1 and M2 omitted

Since the NMOS M1 needs a positive drain source voltage and the PMOS M2 a negative, either the sources (variant I, Fig. 11.1a) or the drains (variant II, Fig. 11.1b) need to be AC-coupled. In variant I the capacitance is chosen to couple to the NMOS because these have less gate-source capacitance, which gives less attenuation as coupling to the PMOS.

The resistors R1 and R2 are used to set the drain currents of M1 and M2 respectively. Resistors rather than saturated MOSFETs are used since their overdrives would have to be low and hence their noise contribution big. For a narrow band receiver inductors could be used as current source. For wideband receivers integrated inductors are however problematic. The relatively low frequency of 400 MHz means it would occupy a lot valuable chip area. The highest frequency of 2.5 GHz means that it should have little associated parallel capacitance. [14, section 5.14].

AC-coupling the common-gate to the common-source stage gives another degree of design freedom with respect to DC coupling. In the case of DC coupling the gate-source voltage is rather high in the case of variant I ($V_{GS3} + V_{GS4} = V_{DD}$) and rather low in the case of variant II ($V_{GS3} + V_{GS4} = V_{DD} - V_{DS1} - V_{DS2}$).

In the subsequent chapters these two variants are analyzed and compared in detail. Two practical properties can already be seen by inspection:

- The capacitor in variant I is at the input and may be off-chip, requiring one extra connection. Doing so for variant II would require 3 extra connections which is more costly.
- In the case of variant II the gates of the common-gate stage are very close to the supply rails, requiring additional circuitry to use replica biasing.

Throughout the analysis some assumptions will be used.

- It is assumed that the intrinsic voltage gain is much greater than unity.
$$g_m \cdot r_o \gg 1$$
- The transconductances of the MOSFETs are assumed to be similar to the characteristic conductance of the antenna.
$$g_m \sim \frac{1}{R_S}$$
- The load impedance (the impedance at the virtual ground node of the baseband-amplifier plus the series resistance of the mixer) is assumed to be lower than the antenna impedance.
$$R_S > R_L$$

In effect these assumptions mean that the drain-source resistance (r_o) may be neglected, and the MOSFETs may be modeled as a (non-linear) transconductor. Furthermore the bulks are always connected to the supply lines and the backgate effect (g_{mb}) is incorporated into g_m and not written down explicitly.

4 Noise and gain

In this chapter the noise figure and current gain are derived assuming that the circuit is frequency independent, i.e. the coupling capacitors are treated as shorts and the parasitic capacitances as opens. The resistors R3 and R4 are assumed to be so big that their effect, both in terms of noise contribution and attenuation, may be neglected. Furthermore it is assumed that thermal noise dominates over other types of noise and all devices are at the same temperature.

4.1 Variant I

The input referred current noise power spectral density generated by R1 and R2 is

$$i^2_{n,in,R1,2} = 4kT\frac{1}{R_1 \parallel R_2} \tag{4.1}$$

The output referred current noise power spectral density generated by M1 and M2 is

$$i^2_{n,out,M1,2} = 4kT(\gamma_1 g_{m1} + \gamma_2 g_{m2})\left(\frac{1-(g_{m3}+g_{m4})(R_S \parallel R_1 \parallel R_2)}{1+(g_{m1}+g_{m2})(R_S \parallel R_1 \parallel R_2)}\right)^2 \tag{4.2}$$

In which the second term in the numerator is the contribution via the feedforward path. For $g_{m3}+g_{m4} = \frac{1}{R_S \| R_1 \| R_2}$ the contrinution by M1 and M2 is zero, but then the output is unbalanced.
The output referred current noise power spectral density generated by M3 and M4 is

$$i^2_{n,out,M3,4} = 4kT(\gamma_3 g_{m3} + \gamma_4 g_{m4}) \tag{4.3}$$

The output referred noise in (4.2) and (4.3) can be referred to the input by dividing it by the current gain from the signal source ($2i_s$) to the output which is

$$\frac{i_{out}}{2i_s} = \left(\frac{1}{g_{m1}+g_{m2}} \parallel R_1 \parallel R_2 \parallel R_S\right)(g_{m1}+g_{m2}+g_{m3}+g_{m4}) \tag{4.4}$$

For readability the transconductances are combined, a symmetrical design is assumed and the (biasing dependent) noise excess factors are approximated by one value

$g_{m1}+g_{m2} = g_{m,CG} \qquad g_{m3}+g_{m4} = g_{m,CS} \qquad R_1 = R_2 = R_{1,2} \qquad \gamma = \gamma_1 = \gamma_2 = \gamma_3 = \gamma_4$

Adding all input referred noise contributions and normalizing to $4kT\frac{1}{R_S}$ gives the spot noise factor.

$$F = 1 + \frac{2R_S}{R_{1,2}} + \gamma R_S \frac{g_{m,CG}\left(\frac{1-g_{m,CS}\cdot(R_S \| \frac{1}{2}R_{1,2})}{1+g_{m,CG}\cdot(R_S \| \frac{1}{2}R_{1,2})}\right)^2 + g_{m,CS}}{\left[\left(R_S \parallel \frac{1}{g_{m,CG}} \parallel \frac{1}{2}R_{1,2}\right)\cdot(g_{m,CG}+g_{m,CS})\right]^2} \tag{4.5}$$

The current gain is

$$A_i = \frac{i_{out}}{i_s} = 2\frac{(g_{m,CG}+g_{m,CS})\cdot R_S \parallel R_{1,2}}{1+g_{m,CG}\cdot R_S \parallel R_{1,2}} \tag{4.6}$$

Matching requires that $\frac{1}{g_{m,CG}} \parallel R_1 \parallel R_2 = R_S$, from which the transconductance of the common-gate stage can be solved

$$g_{m,CG} = \frac{1}{R_S} - \frac{2}{R_{1,2}} \tag{4.7}$$

To have a balanced output the transconductance of both stages must be equal

$$g_{m,CS} = g_{m,CG} \tag{4.8}$$

Substitution of (4.7) and (4.8) in (4.5) and (4.6) gives

$$F = 1 + \frac{2R_S}{R_{1,2}} + \gamma\frac{\left(\frac{2R_S}{R_{1,2}}\right)^2 + 1}{1-\frac{2R_S}{R_{1,2}}} \tag{4.9}$$

and

$$A_i = \frac{i_{out}}{i_s} = 2 - 4\frac{R_S}{R_{1,2}} \tag{4.10}$$

These equations show that when the biasing resistors (R1 and R2) downward approach two times the characteristic impedance the gain goes to zero and the noise factor goes to infinity. At this point the biasing resistors provide the matching to the antenna alone and the transconductance has become zero. To the other side, when the biasing resistors become very big (current source behavior) the gain is two times (6 dB) and the noise factor is $1 + \gamma$, which for a typical value of $\gamma = 1$ corresponds to a noise figure of 3 dB. At this point the common-source stage is the only noise contributor.

4.2 Variant II

The output referred current noise power spectral density generated by R1 and R2 is

$$i^2_{n,out,R1,2} = 4kT\frac{1}{R_1 \parallel R_2} \cdot \left(\frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_L}\right)^2 \tag{4.11}$$

The output referred current noise power spectral density generated by M1 and M2 is

$$i^2_{n,out,M1,2} = 4kT(\gamma_1 g_{m1} + \gamma_2 g_{m2}) \left(\frac{\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_L}\right) - (g_{m3} + g_{m4})R_S}{1 + (g_{m1} + g_{m2})R_S}\right)^2 \tag{4.12}$$

The output referred current noise power spectral density generated by M3 and M4 is

$$i^2_{n,out,M3,4} = 4kT(\gamma_3 g_{m3} + \gamma_4 g_{m4}) \tag{4.13}$$

The current gain from the signal source ($2i_s$) to the output is

$$A_i = \frac{i_{out}}{2i_s} = \left(\frac{1}{g_{m1} + g_{m2}} \parallel R_S\right) \cdot \left[(g_{m1} + g_{m2}) \cdot \left(\frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_L}\right) + g_{m3} + g_{m4}\right] \tag{4.14}$$

Dividing (4.11), (4.12) and (4.13) by (4.14) and adding them gives the total input referred noise. Again combining the transconductances for readability, assuming a symmetrical design, approximating the noise excess factors by one value and normalizing to $4kT\frac{1}{R_S}$, the spot noise factor is

$$F = 1 + \frac{\gamma g_{m,CG}\left(\frac{\frac{R_{1,2}}{R_{1,2}+2R_L} - g_{m,CS}R_S}{1+g_{m,CG}R_S}\right)^2 + \gamma g_{m,CS} + \frac{2}{R_{1,2}+2R_L}}{\left(\frac{g_{m,CG} \cdot \frac{R_{1,2}}{R_{1,2}+2R_L} + g_{m,CS}}{1+g_{m,CG}R_S}\right)^2 R_S} \tag{4.15}$$

The current gain is

$$A_i = \frac{i_{out}}{i_s} = 2\frac{(g_{m,CG} \cdot \frac{R_{12}}{R_{12}+2R_L} + g_{m,CS})R_S}{1 + g_{m,CG}R_S} \tag{4.16}$$

Matching requires that

$$g_{m,CG} = \frac{1}{R_S} \tag{4.17}$$

To have a balanced output the transconductance of the common-gate stage must bigger than that of the common-source stage to compensate for the current division due to the lower output impedance of the common-gate stage.

$$g_{m,CS} = g_{m,CG} \cdot \frac{R_{1,2}}{R_{1,2} + 2R_L} \tag{4.18}$$

Substitution of (4.17) and (4.18) in (4.15) and (4.16) gives

$$F = 1 + \frac{(\gamma R_{1,2} + 2R_S)(R_{1,2} + 2R_L)}{R^2_{1,2}} \tag{4.19}$$

and

$$A_i = \frac{i_{out}}{i_s} = 2\frac{R_{1,2}}{R_{1,2} + 2R_L} \tag{4.20}$$

These equations show that the gain goes to zero and the noise figure goes to infinity when the biasing resistors go to zero. At this point the drain current of M1 and M2 flows directly to the supplies, and to maintain the balance the transconductance of the common-source stage is zero. To the other side, when the biasing resistors become very big the gain is two times (6 dB) and the noise factor is $1 + \gamma$, which for a typical value of $\gamma = 1$ corresponds to a noise figure of 3 dB. At this point all noise is generated by the common-source stage.

4.3 Numerical example and comparison

In Fig. 4.1 the spot noise figures in (4.9) and (4.19) and the gains in (4.10) and (4.20) are plotted for $\gamma = 1$, $R_S = 50\Omega$ and $R_L = 25\Omega$ (single ended) as a function of $R_{1,2}$. Variant II has a lower noise figure for two reasons:

1. The noise generated by R1 and R2 is present only in one output of variant II. In variant I the noise is introduced at the input and is therefor present in both outputs.
2. In variant I the resistors are at the input and cause attenuation of the signal, in variant II they are at the output attenuating both signal and LNA noise.

The gain is higher for variant II for two reasons:

1. In variant I a part of the input signal is lost via R1 and R2 while in variant II only part of one output is lost.
2. The single ended impedance at the virtual ground node of the IF-TIA plus the series resistance of the mixer will be lower than the characteristic impedance of the antenna, giving a smaller loss via R1 and R2 due to the current division.

4.4 Effect of capacitive attenuation

The effect of the coupling capacitances and their parasitic plate-to-ground capacitances have not been taken into account in subsections 4.1 and 4.2. But they not only limit the bandwidth (see chapter 5), they also cause attenuation. This reduces the gain and for variant I, since the attenuation is at the input and hence only the signal is attenuated, the noise figure is increased. Since the capacitive attenuation in variant II takes place at the output the signal and noise are attenuated by the same proportion, leaving the noise figure unaffected.

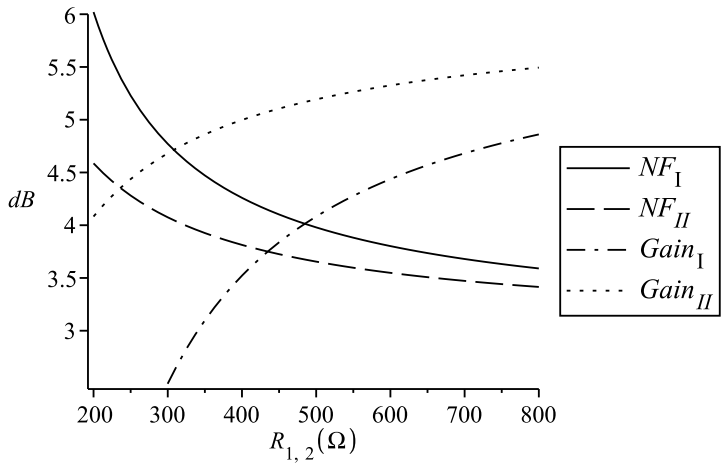


Fig. 4.1: Calculated noise figure and current gain as function of biasing resistor

5 Bandwidth

In this section the frequency response will be modeled, calculating the lower cut-off frequency f_L due to the AC-coupling and the upper cut-off frequency f_H due to the parasitic capacitances. The parasitic plate to ground capacitances of coupling capacitor C_X are denoted as C_{Xa} and C_{Xb}, these normally have different values. The MOSFET capacitances are grouped together as:

$$C_{M1} = c_{sg1} + c_{sd1} + c_{bg1} + c_{bd1} \qquad C_{M2} = c_{sg2} + c_{sd2} + c_{bg2} + c_{bd2}$$

$$C_{M3} = c_{gs3} + c_{gd3} + c_{gb3} \qquad C_{M4} = c_{gs4} + c_{gd4} + c_{gb4}$$

The capacitive transfer from source to drain, gate to drain and vice versa are ignored, i.e. when analyzing the time constants at the input the output is assumed grounded and vice versa. This over estimates the effect of the drain-source capacitance and under estimates the effect of the drain-gate capacitance. Also the time constants of the coupling capacitor and biasing resistors at the common-source stage are assumed have negligible effect on the bandwidth, i.e.

$$C_3 \cdot R_3 \gg \frac{1}{2\pi f_L} \qquad C_4 \cdot R_4 \gg \frac{1}{2\pi f_L}$$

When calculating the lower cut-off frequency the parasitic capacitors are ignored. And when calculating the upper cut-off frequency the coupling capacitors are treated as shorts.

5.1 Variant I

In variant I the AC-coupling capacitors directly impact on the bandwidth, the lower frequency is determined by their value and the upper frequency is limited by their associated parasitics. Fig. 5.1 shows the impedances determining the frequency response.

Assuming a matched and symmetric design, the transconductances and biasing resistors can be related to the antenna impedance as

$$\frac{1}{g_{m1}} \parallel R_1 = \frac{1}{g_{m2}} \parallel R_2 = 2R_S \tag{5.1}$$

Treating the parasitics as open circuits, the transimpedance from input to the NMOS side is

$$Z_N = \frac{v_{s1,g3}}{2i_s} = \frac{2}{3} R_S \frac{j\omega 2R_S C_1}{1 + j\omega \frac{8}{3} R_S C_1} \tag{5.2}$$

And the transimpedance to the PMOS side is

$$Z_P = \frac{v_{s2,g4}}{2i_s} = \frac{2}{3} R_S \frac{1 + j\omega 2R_S C_1}{1 + j\omega \frac{8}{3} R_S C_1} \tag{5.3}$$

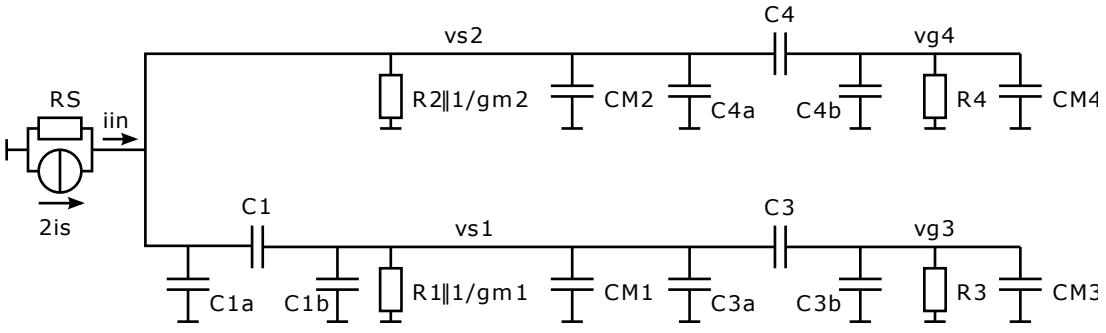


Fig. 5.1: Impedances for variant I determining the frequency behavior

The overall transimpedance, which for balanced outputs is a $2/g_m$ times scaled copy of the output currents, is the sum of these

$$Z_N + Z_P = \frac{2}{3} R_S \frac{1 + j\omega 4 R_S C_1}{1 + j\omega \frac{8}{3} R_S C_1} \tag{5.4}$$

For low frequencies the NMOS side becomes uncoupled, this makes the transimpedance in (5.2) go to zero, but also makes the transimpedance in (5.3) go up by 50%. These two effects combined give a transimpedance in (5.4) that decreases with frequency by one third. For high frequencies (5.2) and (5.3) are half the antenna impedance.

Nominally (5.4) is thus equal to the antenna impedance. Solving $|Z_N + Z_P| = \alpha R_S$ at ω_L for C_1 gives the minimum coupling capacitance to obtain an attenuation of α at ω_L.

$$C_1 = \frac{\frac{1}{8}\sqrt{9\alpha^2 - 4}}{\sqrt{1 - \alpha^2}\omega R_S} \tag{5.5}$$

The upper frequency is limited by the parasitic capacitances to ground and may be estimated by calculating the dominant RC-time constant, which is

$$\tau_H = c_{par} \cdot \frac{1}{2} R_S \tag{5.6}$$

In which c_{par} is the sum of all parasitic capacitances

$$c_{par} = C_{1a} + C_{1b} + C_{M1} + C_{M2} + C_{3a} + C_{3b} + C_{4a} + C_{4b} + C_{M3} + C_{M4} \tag{5.7}$$

For an attenuation of α at ω_H the maximum sum of parasitic capacitances is

$$c_{par} = \frac{2\sqrt{1 - \alpha^2}}{R_S \cdot \omega_H} \tag{5.8}$$

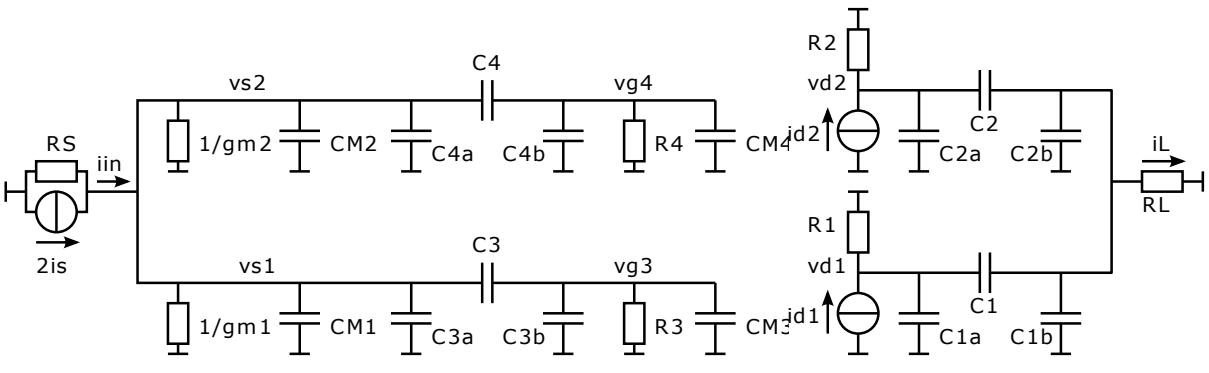
5.2 Variant II

Due to the big impedance difference between the output impedance of the LNA and the input impedance of the mixer plus IF-amplifier, the AC coupling does not directly impact the bandwidth for variant II but lowers the compression point. Fig. 5.2a shows the impedances at the input and Fig. 5.2b at the output. The lower corner-frequency is mostly determined by the series combination of the coupling capacitances and the output impedance of the LNA. The transfer function from the common-gate output to the input of the next stage, modeled as R_L is, treating all parasitics as opens is

$$H_{CG} = \frac{i_L}{i_{d1} + i_{d2}} = \frac{j\omega R_{1,2} C_{1,2}}{1 + j\omega (R_{1,2} + R_L) C_{1,2}} \tag{5.9}$$

The output of the common-source stage is DC coupled, so its transfer function is simply

$$H_{CS} = \frac{i_L}{i_{d3} + i_{d4}} = 1 \tag{5.10}$$



(a) Input (b) Output

Fig. 5.2: Impedances for variant II determining the frequency behavior

When the outputs are nominally balanced the normalized overall transfer function from the drains to the input of the next stage is the average of (5.9) and (5.10)

$$H = \frac{1}{2}(H_{CG} + H_{CS}) = \frac{1}{2}\frac{1 + j\omega(2R_{1,2} + R_L)C_{1,2}}{1 + j\omega(R_{1,2} + R_L)C_{1,2}} \tag{5.11}$$

Solving $|H| = \alpha$ for $C_{1,2}$ at ω_L gives the minimum coupling capacitance to obtain an attenuation of α at ω_L

$$C_{1,2} = \frac{1}{\omega_L}\sqrt{\frac{4\alpha^2 - 1}{[(1-\alpha)\cdot(2R_{1,2} + R_L) - R_L]\cdot[(1+\alpha)\cdot(2R_{1,2} + R_L) + R_L]}} \tag{5.12}$$

Using this resulting capacitance would however reduce the compression point for frequencies already well above f_L since the impedance seen at the drains of M1 and M2 would start rising with decreasing frequency. This results in increasing voltage gain from source to drain and hence to keep the transistors saturated less input power would be allowed. The voltage at the drain of M1 due to the drain currents of M1 and M2 is

$$v_{d1} = i_{d1} \cdot R_1 \parallel \left[\frac{1}{j\omega C_1} + (R_2 + \frac{1}{j\omega C_2}) \parallel R_L\right] \tag{5.13}$$

$$+ i_{d2}\frac{R_2}{R_2 + \frac{1}{j\omega C_2} + R_L \parallel (\frac{1}{j\omega C_1} + R_1)} \cdot \frac{R_L}{R_L + \frac{1}{j\omega C_1} + R_1} \cdot R_1 \tag{5.14}$$

Assuming a symmetrical design, the effective impedance seen at the drains of the common-gate transistors is

$$Z_{d,CG} = \frac{v_{d1,2}}{i_{d1} + i_{d2}} = \frac{R_{1,2}}{2}\frac{1 + j\omega(2R_L + R_{1,2})C_{1,2} - \omega^2 2R_L R_{1,2} C_{1,2}^2}{1 + j\omega 2(R_L + R_{1,2})C_{1,2} - \omega^2 R_{1,2}(2R_L + R_{1,2})C_{1,2}^2} \tag{5.15}$$

For very low frequencies all the drain current of M1 flows through R1 and all the drain current of M2 flows through R2. Since each drain current is half the output current this gives a voltage drop of $\frac{1}{2} i_{CG} \cdot R_{1,2}$, dividing by i_{CG} then gives the same value as (5.15) at $\omega = 0$.

For very high frequencies the coupling capacitors may be treated as shorts and the drain currents of M1 and M2 and the resistors R1 and R2 are in parallel, giving a voltage at the drains of $i_{CG} \cdot R_1 \parallel R_2 \parallel R_L$. Dividing this by i_{CG} gives the same value as (5.15) at $\omega = \infty$.

If the maximum input voltage is $V_{CP,in}$ and the maximum voltage swing for which the MOSFETS stay saturated is $V_{d,CG,max}$, the minimum coupling capacitance could be found by solving $|Z_{d,CG}|V_{CP,in} = R_S \cdot V_{d,CG,max}$ with $\omega = 2\pi f_L$ for $C_{1,2}$. Doing so symbolically would yield an unwieldy result, if however the allowed impedance is closer to R_L than to $R_{1,2}$, then (5.15) can be approximated as

$$Z_{d,CG} \approx \frac{1}{j\omega 2C_{1,2}} + R_L \tag{5.16}$$

In this case all current will flow through RL, C1 and C2, not through R1 and R2. Because the circuit is assumed to be symmetric the drain currents may be added and the capacitors are in parallel, making the impedance seen at the drains of the common-gate stage a series connection of a capacitor with value $C_1 + C_2$ and resistor RL

Solving $|Z_{d,CG}|V_{CP,in} = R_S \cdot V_{d,CG,max}$ for $C_{1,2}$ at ω_L using (5.16) yields a simple expression for the minimum coupling capacitance

$$C_{1,2} = \frac{\omega_L}{2\sqrt{R_S^2 \cdot \left(\frac{v_{d,CG,max}}{V_{CP,in}}\right)^2 - R_L^2}} \tag{5.17}$$

The upper frequency is determined by two time constants: one at the input (5.18) and one at the common-gate output (5.19).

$$\tau_{inp} = \frac{1}{2}R_S \cdot (C_{M1} + C_{M2} + C_{3a} + C_{3b} + C_{4a} + C_{4b} + C_{M3} + C_{M4}) \tag{5.18}$$

$$\tau_{outp,CG} = R_L \parallel \frac{1}{2}R_{1,2} \cdot (C_{1a} + C_{1b} + C_{2a} + C_{2b}) \tag{5.19}$$

In which it has been assumed that if the parasitics are treated as opens the input is matched. The time constant in (5.19) is present in only one path to the output. The normalized transfer functions to each output are

$$H_{CG} = \frac{1}{(1 + j\omega\tau_{inp})(1 + j\omega\tau_{outp,CG})} \qquad H_{CS} = -\frac{1}{1 + j\omega\tau_{inp}} \tag{5.20}$$

Assuming a nominally balanced output the normalized differential output is the normalized difference of these

$$H = \frac{1}{2}(H_{CG} - H_{CS}) = \frac{2 + j\omega\tau_{outp}}{(1 + j\omega\tau_{inp})(1 + j\omega\tau_{outp,CG})} \tag{5.21}$$

5.3 Numerical example and comparison

For a -1dB point ($\alpha = 0.89$) at 400 MHz the coupling capacitor given by (5.5) for variant I is 4 pF. Allowing for 250 mV amplitude at the drains of M1 and M2 in variant II, choosing the compression point at 0 dBm and assuming a 25 Ω single-ended load, (5.17) also gives approximately 4 pF.

Using these values and $R_S = 50\Omega$ the normalized frequency response for variant I, the normalized frequency response for variant II and the voltage gain from source to drain for variant II are plotted in Fig. 5.3 for low frequencies. This clearly shows that although the corner frequency is much lower than 400 MHz for variant II, the voltage swing at the drains for these frequencies is still too big and keeps declining even way beyond 400 MHz.

For a -1dB point at 2.5 GHz (5.7) limits the total parasitic capacitance to 1.3 pF

Because the load resistance (R_L) is half the antenna impedance (R_S) and the plate-to-ground capacitors for variant II ($C_{1a}, C_{1b}, C_{2a} and C_{2b}$) add up to twice the value of those of variant I ($C1a, C1b$), they cause a time constant (5.6) for variant II that is twice that of variant I (5.20). This time constant in variant II is however only present in the path to one output branch, while in variant I it is present in both. As a result the the upper frequency limit will be similar for both variants for these example numbers.

A big difference between both variants is that the outputs of variant I remain balanced over the whole frequency band while in variant II the bandwidth of the common-source stage is bigger than that of the common-gate stage. The balance of variant II thus degrades for frequencies away from the center of the band when designed for maximum bandwidth. Alternatively the common-source stage could also be capacitively coupled, limiting its bandwidth the same way as that of the common-gate stage. This improves the balance over frequency at the expense of bandwidth.

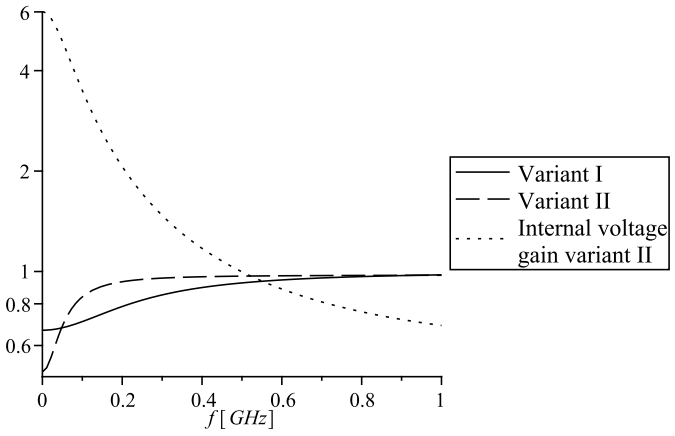


Fig. 5.3: Calculated normalized frequency response due to AC-coupling

6 Input matching

To avoid reflection on the interconnection between the antenna and the LNA, which translates to filtering behavior, the input impedance of the LNA (Z_{in}) should be matched to that of the antenna. The antenna in this report is modeled as a simple 50Ω resistor (R_S). A measure for the quality of the matching is the input reflection coefficient

$$S_{11} = \frac{Z_{in} - Z_S}{Z_{in} + Z_S}$$

which ideally is zero.

6.1 Variant I

Assuming that the input is perfectly matched if the coupling capacitances were shorts and the parasitics opens and treating C_3 and C_4 as shorts, the input impedance of variant I is

$$Z_{in} = \left(\frac{1}{j\omega C_1} + 2R_S \parallel \frac{1}{j\omega C_{par,N}} \right) \parallel 2R_S \parallel \frac{1}{j\omega C_{par,P}} \tag{6.1}$$

$$= 2R_S \frac{1 + j\omega 2R_S(C_1 + C_{par,N})}{1 + j\omega 2R_S(2C_1 + C_{par,N} + C_{par,P}) - \omega^2 4R_S^2 C_{par,P}(2C_1 + C_{par,N})} \tag{6.2}$$

in which

$$C_{par,N} = C_{1b} + C_{M1} + C_{3a} + C_{3b} + C_{M3} \qquad C_{par,P} = C_{1a} + C_{M2} + C_{4a} + C_{4b} + C_{M4}$$

This gives a reflection coefficient of

$$S_{11} = \frac{1 + j\omega 2R_S(C_{par,N} - C_{par,P}) + \omega^2 4R_S^2 C_{par,P}(2C_1 + C_{par,N})}{3 + j\omega 2R_S(4C_1 + 3C_{par,N} + C_{par,P}) - \omega^2 4R_S^2 C_{par,P}(2C_1 + C_{par,N})} \tag{6.3}$$

6.2 Variant II

Again assuming that the input is perfectly matched if the coupling capacitances were shorts and the parasitics opens and treating C_3 and C_4 as shorts, the input impedance of variant II is

$$Z_{in} = R_S \parallel \frac{1}{j\omega C_{par}} = \frac{R_S}{1 + j\omega R_S C_{par}} \tag{6.4}$$

in which

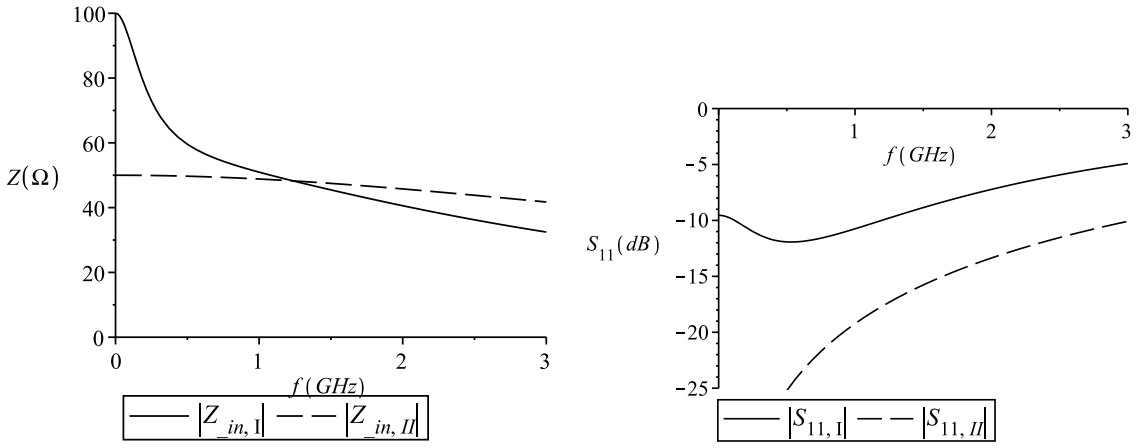
$$C_{par} = C_{M1} + C_{M2} + C_{3a} + C_{3b} + C_{4a} + C_{4b} + C_{M3} + C_{M4}$$

This gives a reflection coefficient of

$$S_{11} = \frac{-j\omega R_S C_{par}}{2 + j\omega R_S C_{par}} \tag{6.5}$$

6.3 Numerical example and comparison

Fig. 6.1a shows the input impedances and Fig. 6.1b the reflection coefficient for $R_S = 50\Omega$, $C_1 = 4\text{pF}$, $c_{par,N} = 0.6\text{pF}$, $c_{par,P} = 0.7\text{pF}$ (together the 1.3 pF maximally allowed for bandwidth considerations) and $c_{par} = 0.7\text{pF}$ (the difference corresponds to 15% parasitic plate-to-ground capacitance of the coupling capacitor). This shows that the input matching requirement sets a much stricter limit to the amount of parasitic capacitance allowed for variant I than the bandwidth requirement. Furthermore it shows that the AC coupling at the input itself does not cause matching problems.

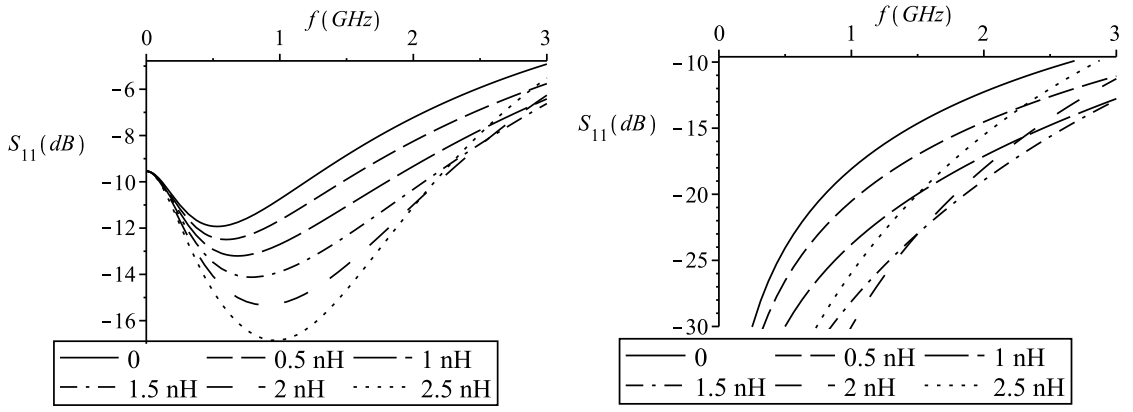


(a) Input impedance (b) Input reflection coefficient

Fig. 6.1: Calculated input matching as function of frequency

6.4 Improving using series inductance

The parasitic capacitance causing the mismatch for higher frequencies can be somewhat neutralized by taking an inductor in series with the input. Depending on the packaging, a bond-wire inductance could serve this purpose. Fig. 6.2 shows the effect of series inductance on the input reflection coefficient using the values from the previous section, note the different vertical scale. A typical value of 1 to 2 nH does indeed improve the matching.



(a) Variant I (b) Variant II

Fig. 6.2: Calculated reflection coefficient as function of frequency for different series inductances

7 Effects of nonlinearity

This chapter recaps some theory on the effects of differential and common-mode nonlinearity and provides definitions for the main figures that quantify it.

Any infinitely differentiable function $f(x)$ can be described as a Taylor series

$$f(x) = \sum_{n=0}^{\infty} \frac{f^{(n)}(a)}{n!} (x-a)^n \tag{7.1}$$

In which $f^{(n)}(a)$ denotes the nth derivative of f to x at $x = a$, divided by the factorial of n this is called the nth Taylor coefficient, here denoted as b_n.

$$b_n = \frac{f^{(n)}(a)}{n!} = \frac{1}{n!} \frac{\mathrm{d}^n f(a)}{\mathrm{d}\, x^n} \tag{7.2}$$

Table 7.1 list the frequency components in the output of a third-order system with Taylor coefficients b_1, b_2 and b_3 to which two tones are applied: at frequency f_1 with amplitude A_1 and at frequency f_2 with amplitude A_2.

The second-order intercept point is the power level at which the second-order intermodulation product in the output is as strong as the fundamental. If the fundamental is tone 1 and the interferer tone 2, this occurs when

$$b_2 A_1 A_2 = b_1 A_1$$

Solving for A_2 gives the amplitude

$$A_{IIP2} = \frac{b_1}{b_2} \tag{7.3}$$

Order	Frequency	Amplitude	Type
1	f_1	$b_1 A_1$	fundamental
1	f_2	$b_1 A_2$	
2	$f_1 + f_2$	$b_2 A_1 A_2$	2nd order intermodulation product
2	$f_1 - f_2$	$b_2 A_1 A_2$	
2	$2f_1$	$\frac{1}{2} b_2 A_1^2$	2nd harmonic
2	$2f_2$	$\frac{1}{2} b_2 A_2^2$	
2	0	$\frac{1}{2} b_2 A_1^2$	DC Shift
2	0	$\frac{1}{2} b_2 A_2^2$	
3	$2f_1 + f_2$	$\frac{3}{4} b_3 A_1^2 A_2$	3rd order intermodulation product
3	$2f_1 - f_2$	$\frac{3}{4} b_3 A_1^2 A_2$	
3	$f_1 + 2f_2$	$\frac{3}{4} b_3 A_1 A_2^2$	
3	$f_1 - 2f_2$	$\frac{3}{4} b_3 A_1 A_2^2$	
3	f_1	$\frac{3}{2} b_3 A_1 A_2^2$	3rd order cross modulation product
3	f_2	$\frac{3}{2} b_3 A_1^2 A_2$	
3	f_1	$\frac{3}{4} b_3 A_1^3$	3rd order compression
3	f_2	$\frac{3}{4} b_3 A_2^3$	
3	$3f_1$	$\frac{1}{4} b_3 A_1^3$	3rd harmonic
3	$3f_2$	$\frac{1}{4} b_3 A_2^3$	

Table 7.1: Tones generated by the second and third order nonlinearity

The third-order intercept point is the power level at which the third-order intermodulation product in the output is as strong as the fundamental. If the fundamental is tone 1 and the interferer tone 2, this occurs when

$$\frac{3}{4}b_3 A_1 A_2^2 = b_1 A_1$$

Solving for A_2 gives the amplitude

$$A_{IIP3} = \sqrt{\frac{4}{3}\frac{b_1}{b_3}} \tag{7.4}$$

The input-referred 1 dB compression point is the input level at which the output level of a single tone is 1 dB less than the value predicted by extrapolation. In the absence of higher-order nonlinearities, this occurs when

$$b_1 A + \frac{3}{4}b_3 A^3 = 10^{\frac{-1}{20}} \cdot b_1 A$$

Solving for A gives the amplitude

$$A_{CP-1dB} = \sqrt{(1 - 10^{\frac{-1}{20}})\frac{4}{3}\frac{b_1}{b_3}} \tag{7.5}$$

Rewriting in decibels the compression point can be related to the third-order intercept point as

$$ICP_{-1dB} = IIP3 - 9.6dB \tag{7.6}$$

The input referred 1 dB desensitation point is the input level at which an interferer causes the gain of the wanted signal to decrease by 1 dB. If the wanted signal is tone 1 and the interferer is tone 2, then in the absence of higher order nonlinearities, this occurs when

$$b_1 A + \frac{3}{2}b_3 A_1 A_2^2 = 10^{\frac{-1}{20}} \cdot b_1 A$$

Solving for A_2 gives the amplitude

$$A_{DP-1dB} = \sqrt{(1 - 10^{\frac{-1}{20}})\frac{2}{3}\frac{b_1}{b_3}} \tag{7.7}$$

Rewriting in decibels, the desensitation point can be related to the compression point as

$$IDP_{-1dB} = ICP_{-1dB} - 3dB \tag{7.8}$$

The 1 dB compression point itself has little meaning for wideband LNAs, the wanted signal normally is well below this level. The 1dB desensitation level is however of prime importance, a single interferer in the RF band above this level blocks any other signal. Because of their similarity usually only the compression point is specified.

The amplitudes can be converted to power when the impedance level is known. If the amplitude is a voltage V or current I and the impedance level is R then the power expressed in dBm is obtained with

$$P = 10\log\left(\frac{1}{1\text{mW}} \cdot \frac{V^2}{2R}\right)[dBm] \qquad P = 10\log\left(\frac{1}{1\text{mW}} \cdot I^2 \cdot 2R\right)[dBm] \tag{7.9}$$

For an LNA with differential outputs the definitions above are for the differential output, with the Taylor coefficients specifying the input to differential output relation. A similar description can be made for the input to common-mode output relation, which can be used for characterizing the disbalancing effect of an interferer. The imbalance is the ratio of the amplitudes at the individual outputs, rewritten in terms of common (CM) and differential (DM) outputs and expressed in decibels this is

$$\Delta A = 20\log\left(\frac{\frac{1}{2}A_{DM} - A_{CM}}{\frac{1}{2}A_{DM} + A_{CM}}\right)[dB] \tag{7.10}$$

For nominally balanced outputs the first-order common-mode Taylor coefficient is zero by design, in which case $\Delta A = 0dB$. The third-order common-mode Taylor coefficient may be non-zero, creating a disbalance in the fundamental under strong interference. If the wanted signal is tone 1 and the interferer tone 2, the common-mode component at f_1 is

$$A_{CM} = b_{1,CM} A_1 + \frac{3}{2} \cdot b_{3,CM} A_1 A_2^2 \tag{7.11}$$

Which shows that the common-mode output amplitude increases quadratically with interferer amplitude. The differential component at f_1 is

$$A_{DM} = b_{1,DM} A_1 + \frac{3}{2} \cdot b_{3,DM} A_1 A_2^2 \tag{7.12}$$

Substitution of (7.11) and (7.12) in (7.10) finally gives

$$\Delta A = 20 \log \left(\frac{\frac{1}{2}(b_{1,DM} + \frac{3}{2} \cdot b_{3,DM} A_2^2) - (b_{1,CM} + \frac{3}{2} \cdot b_{3,CM} A_2^2)}{\frac{1}{2}(b_{1,DM} + \frac{3}{2} \cdot b_{3,DM} A_2^2) + (b_{1,CM} + \frac{3}{2} \cdot b_{3,CM} A_2^2)} \right) [dB] \tag{7.13}$$

Again this equation only holds for small input amplitudes where the effect of higher-order odd nonlinearities may be neglected.

8 Limitations of previous designs

Even when the MOSFETs in a non-complementary noise-canceling common-gate and common-source LNA were perfect square-law, so the stages individually produce only second-order distortion, a third-order product does arise because:

- The common-gate MOSFET is in a feedback loop (its source is degenerated).
- A cascade of two second-order stages gives a third-order nonlinearity.

This chapter shows how the second-order non-linearity of the MOSFETS limits the performance.

The nonlinearity of the common-gate MOSFET is canceled in the same way as its noise, i.e. the nonlinear component in the current flowing through it is copied to the common-source stage and so ends up at the output in common-mode. This way two third-order components are generated:

1. A third-order component originating from the common-gate stage, though the noise-canceling mechanism present in both outputs common-mode.
2. A second-order component originating from the common-gate stage undergoing a second-order distortion in the common-source stage and hence present only in the common-source output. This nonlinearity is thus half common, half differential-mode.

The next two sections will show the performance limitations caused by these two effects, in two other versions of the common-gate common-source LNA, namely:

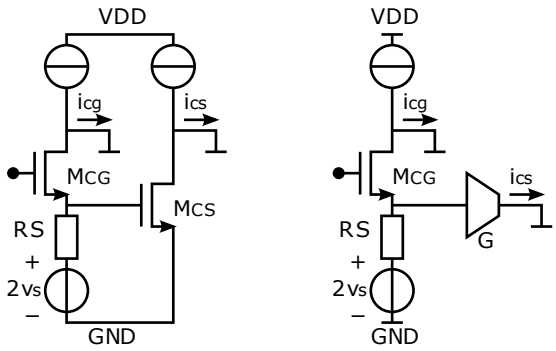
- The basic version [15] with only NMOS, shown in Fig. 8.1a.
- A version with an NMOS common-gate stage and a linear feed forward stage, shown in Fig. 8.1b. Because the distortion of the common-gate stage is canceled this circuit is linear, but not balanced for large input swings, as will be shown.

The third-order components, both common-mode and differential-mode, of these will be calculated.

8.1 Square-law CG, square-law CS

When the input voltage goes up the overdrive of the common-gate stage increases and that of the common-source stage decreases. This gives output currents of

$$I_{CG} = K_{CG} \cdot V_{OVCG}^2 - K_{CG} \cdot (V_{OVCG} - v_{in})^2 \tag{8.1}$$



(a) Square law CG and CS (b) Square law CG and linear feedforward stage

Fig. 8.1: Non-complementary noise canceling LNA's

$$I_{CS} = K_{CS} \cdot V_{OVCS}^2 - K_{CS} \cdot (V_{OVCS} + v_{in})^2 \tag{8.2}$$

In which the first terms are the DC current supplied by the current sources and the second terms the drain current.
Matching requires that

$$K_{CG} = \frac{1}{2R_S V_{OVCG}} \tag{8.3}$$

and balance requires

$$K_{CS} = \frac{1}{2R_S V_{OVCS}} \tag{8.4}$$

The input voltage is determined by the voltage source v_s and the drain current of the common-gate stage, the input voltage can be solved from

$$v_{in} = v_s - I_{CG} \cdot R_S \tag{8.5}$$

Substituting the result in (8.1) and (8.2) then gives output currents, which are rewritten in terms of common and differential-mode outputs

$$I_{DM} = I_{CG} - I_{CS} \qquad I_{CM} = \frac{1}{2}(I_{CG} + I_{CS}) \tag{8.6}$$

The normalized differential, common-mode, common-gate and common-source output current are plotted in Fig. 8.3a as function of the applied voltage v_s normalized to the overdrive.

Taking the derivative of the differential-mode current to the applied voltage gives the transconductance of the whole structure.

$$b_{1DM} = \frac{\mathrm{d}\, I_{DM}}{\mathrm{d}\, v_s} = \frac{2}{R_S} \tag{8.7}$$

Which corresponds to a current gain of two. Next the second derivative of the differential-mode drain current to the applied voltage is calculated,

$$b_{2,DM} = \frac{1}{2}\frac{\mathrm{d}^2\, I_{DM}}{\mathrm{d}\, v_s^2} = \frac{1}{2R_S V_{OVCS}} \tag{8.8}$$

This equation shows that the second-order distortion component is generated by the common-source stage only, that of the common-gate is canceled. The third-order Taylor coefficient is

$$b_{3,DM} = \frac{1}{6}\frac{\mathrm{d}^3\, I_{DM}}{\mathrm{d}\, v_s^3} = \frac{1}{4R_S V_{OVCS} V_{OVCG}} \tag{8.9}$$

This equation shows that the third-order distortion component is generated by the cascade of both stages. From (8.8) and (8.9) the input referred second- and third-order intercept point can be calculated. The amplitude at which the second-order intermodulation product intercepts the fundamental is

$$V_{IIP2} = \frac{b_{1,DM}}{b_{2,DM}} = 4V_{OVCS} \tag{8.10}$$

The amplitude at which the third-order intermodulation product intercepts the fundamental is

$$V_{IIP3} = \sqrt{\frac{4}{3}\frac{b_{1,DM}}{b_{3,DM}}} = \frac{4}{3}\sqrt{6}\sqrt{V_{OVCG} V_{OVCS}} \tag{8.11}$$

The results in (8.10) and (8.11) are plotted on a logarithmic scale in Fig. 8.2a for equal overdrives of the stages. This shows that unless some distortion compensating mechanism [16] is used the linearity of this basic version is fairly limited.

Taking the derivative of the common-mode drain current to the applied input voltage gives the disbalance

$$b_{1CM} = \frac{\mathrm{d}\, I_{CM}}{\mathrm{d}\, v_s} = 0 \tag{8.12}$$

The output is balanced for small signals by design.

Next the second- and third-order derivative of the common-mode drain current to the applied voltage are calculated

$$b_{2CM} = \frac{1}{2}\frac{\mathrm{d}^2 I_{CM}}{\mathrm{d}\, v_s^2} = \frac{3V_{OVCG} + V_{OVCS}}{8R_S V_{OVCG}^2} \tag{8.13}$$

$$b_{3CM} = \frac{1}{6}\frac{\mathrm{d}^3 I_{CM}}{\mathrm{d}\, v_s^3} = \frac{3V_{OVCG} + V_{OVCS}}{16R_S V_{OVCG}^3} \tag{8.14}$$

The third-order nonlinearity gives a unbalancing component that increases quadratically with the interferer level as explained in chapter 7. This imbalance for equal overdrive of the stages is plotted in Fig. 8.2b (solid line) as function of the amplitude normalized to the overdrive. This shows that the imbalance is 1 dB when the applied amplitude is 40% of the overdrive.

8.2 Square-law CG, linear feedforward

The expression for the output current of the common-stage is still (8.1) and since the input voltage is only determined by the voltage source and the common-gate stage (8.5) also still holds. The common-source stage now is linear with a transconductance that for reasons of balancing is the reciprocal of the source impedance.

$$I_{CS} = -\frac{v_{in}}{R_S} \tag{8.15}$$

Substituting the input voltage obtained from (8.5) in (8.1) and (8.15) and rewriting as in (8.6) again gives the differential and common-mode output currents. These are normalized to the source impedance and shown together with the normalized common-gate and common-source output currents as function of the applied voltage normalized to the DC overdrive in fig. 8.3b.

Taking the derivative of the differential-mode drain current to the applied voltage gives the transconductance of the whole structure.

$$b_{1DM} = \frac{\mathrm{d}\, I_{DM}}{\mathrm{d}\, v_s} = \frac{2}{R_S} \tag{8.16}$$

This again corresponds to a current gain of two. The second- and third-order derivative of the differential-mode drain current to the applied voltage are both zero

$$b_{2DM} = \frac{1}{2}\frac{\mathrm{d}^2 I_{DM}}{\mathrm{d}\, v_s^2} = 0 \qquad b_{3DM} = \frac{1}{6}\frac{\mathrm{d}^3 I_{DM}}{\mathrm{d}\, v_s^3} = 0 \tag{8.17}$$

This means that the IIP2 and IIP3 are now infinite. The common-gate stage does however still generate second- and third-order components. As a result of the distortion cancellation these do not end up in the output current differentially but are converted to common-mode, as shown in the next paragraph.

Taking the derivative of the common-mode drain current to the applied input voltage gives the small-signal disbalance

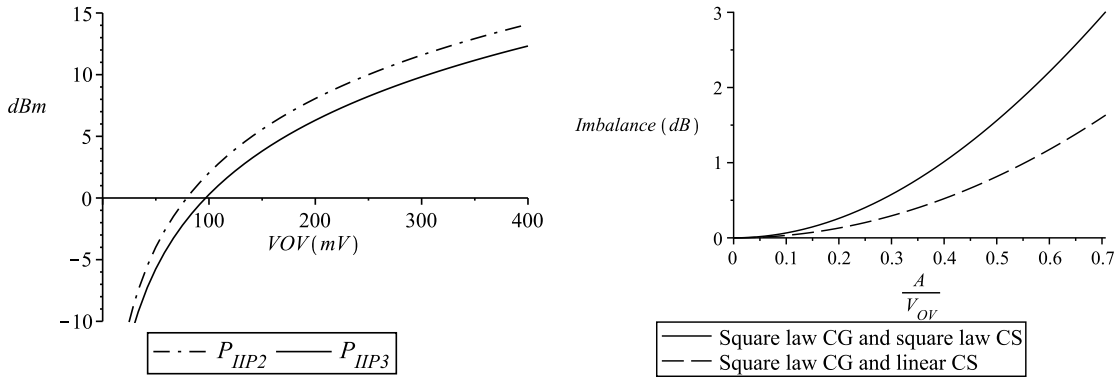
$$b_{1CM} = \frac{\mathrm{d}\, I_{CM}}{\mathrm{d}\, v_s} = 0 \tag{8.18}$$

This shows that the output is balanced for small signals. The second- and third-order derivative of the common-mode output current to the applied voltage are

$$b_{2CM} = \frac{1}{2}\frac{\mathrm{d}^2 I_{CM}}{\mathrm{d}\, v_s^2} = \frac{1}{4R_S V_{OVCG}} \tag{8.19}$$

$$b_{3CM} = \frac{1}{6}\frac{\mathrm{d}^3 I_{CM}}{\mathrm{d}\, v_s^3} = \frac{1}{8R_S V_{OVCG}^2} \tag{8.20}$$

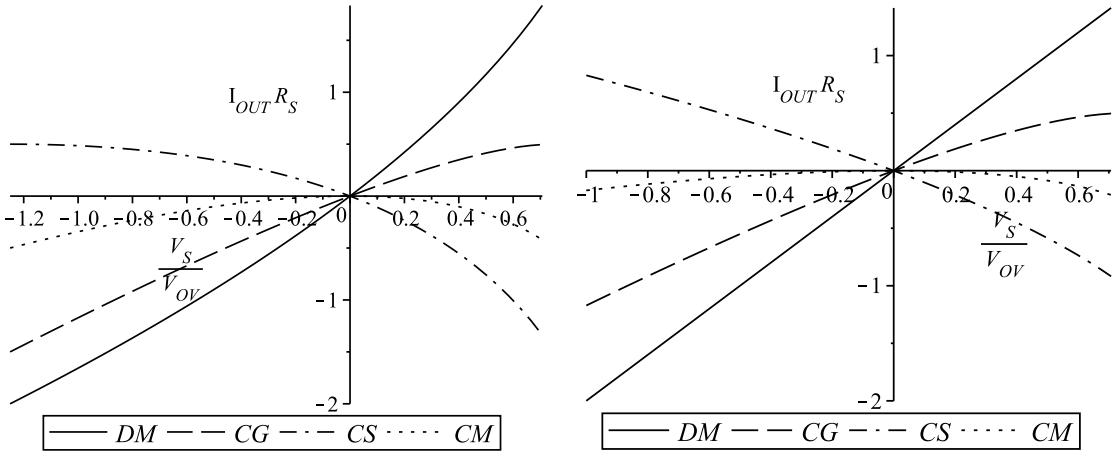
This is half the value of (8.14) for equal overdrives. This shows that linearizing the common-source stage has improved the common-mode behavior by only 3 dB. The imbalance this gives rise to according to (7.13) is plotted in Fig. 8.2b (dashed line) as function of the amplitude normalized to the overdrive. This shows that the imbalance is 1 dB when the applied amplitude is 56% of the overdrive. A highly interfer-robust balance thus requires zero second-order distortion in both stages.



(a) IIP3 and IIP2 for square-law MOSFETs as function of overdrive

(b) Imbalance in the fundamental component as function of normalized interferer amplitude

Fig. 8.2: Calculated effects of nonlinearity



(a) Square-law CG and square-law CS

(b) Square-law CG and-linear CS

Fig. 8.3: Calculated output currents normalized to antenna impedance as function of normalized applied voltage

9 Small-signal nonlinearity

Over a small region a function may be described by a finite Taylor series. In this report the Taylor series are limited to 3 terms, the minimum needed to describe the third-order intermodulation and interferer dependent imbalance. These effects of the nonlinearities were described in chapter 7.

9.1 Third-order intercept point

In this section the third-order intercept point for the idealized case that the biasing resistors may be treated as current sources, the coupling capacitances as shorts and the parasitic capacitances as opens is calculated. This gives insight and expressions sufficiently accurate for designing.

The nonlinearity of the drain current of as function of the gate source voltage is modeled by a third-order Taylor-series

$$I_{d,m} = b_{0,m} + b_{1,m} \cdot v_{gs,m} + b_{2,m} \cdot v_{gs,m}^2 + b_{3,m} \cdot v_{gs,m}^3 \tag{9.1}$$

In which the coefficients are computed with

$$b_{n,m}(V_{GS}) = \frac{1}{n!} \cdot \frac{\mathrm{d}^n I_{d,m}}{\mathrm{d} V_{GS,m}^n} \tag{9.2}$$

The output current of each stage is the difference of two drain currents, from an NMOS and a PMOS, whose gate source voltages vary in opposite direction. For the common-gate stage, which is composed of M1 and M2 this gives an output current of

$$i_{cg} = b_{1,M1} \cdot v_s - b_{1,M2} \cdot (\text{-}v_s) + b_{2,M1} \cdot v_s^2 - b_{2,M2} \cdot (\text{-}v_s)^2 + b_{3,M1} \cdot v_s^3 - b_{3,M2} \cdot (\text{-}v_s)^3 \tag{9.3}$$

$$= (b_{1,M1} + b_{1,M2}) \cdot v_s + (b_{2,M1} - b_{2,M2}) \cdot v_s^2 + (b_{3,M1} + b_{3,M2}) \cdot v_s^3 \tag{9.4}$$

Similarly for the common-source stage, which is composed of M3 and M4 the output current is

$$i_{cs} = b_{1,M3} \cdot (\text{-}v_s) - b_{1,M4} \cdot v_s + b_{2,M3} \cdot (\text{-}v_s)^2 - b_{2,M4} \cdot v_s^2 + b_{3,M3} \cdot (\text{-}v_s)^3 - b_{3,M4} \cdot v_s^3 \tag{9.5}$$

$$= -(b_{1,M3} + b_{1,M4}) \cdot v_s - (b_{2,M3} - b_{2,M4}) \cdot v_s^2 - (b_{3,M3} + b_{3,M4}) \cdot v_s^3 \tag{9.6}$$

The biasing point of each NMOS/PMOS pair may be chosen such that their second-order component is equal and therefor the quadratic terms in (9.4) and (9.6) fall out. For square-law devices this means that the overdrives are equal, for more realistic models this is not exactly the case but they should nevertheless be similar. The nonlinear terms of the common-gate stage end up at the output purely common-mode, the linear term purely differentially. The differential output current is thus

$$i_{dm} = i_{cg} - i_{cs} = (b_{1,M1} + b_{1,M2} + b_{1,M3} + b_{1,M4}) \cdot v_s + (b_{3,M3} + b_{3,M4}) \cdot v_s^3 \tag{9.7}$$

From which the IIP3 can be calculated as

$$V_{IIP3} = \sqrt{\frac{4}{3} \frac{b_{1,M1} + b_{1,M2} + b_{1,M3} + b_{1,M4}}{b_{3,M3} + b_{3,M4}}} \tag{9.8}$$

If the output is balanced the first-order Taylor coefficient of the common-gate stage ($b_{1,M1} + b_{1,M2}$) is equal to that of the common-source stage ($b_{1,M3} + b_{1,M4}$). Hence the IIP3 power ideally is the double (+3dB) of the common-source stage alone. The IIP3 of the common-source stage itself is the average of the intrinsic IIP3 of the N- and PMOS. The intrinsic IIP3 is a function of gate length and overdrive [17, p. 323]. For medium-low overdrives it is proportional to the square root of the overdrive and increases with gate length.

9.2 Incomplete cancellation and frequency dependence

In the previous section the third-order intercept point was calculated using some idealizing assumptions. This section deals with the non-idealities in a qualitative way. A more accurate analysis should take into account

- The effect of drain-source and source-bulk voltage.
- The incomplete distortion cancellation in the case of variant I.
- The residual second-order components and the frequency dependence of this component in the case of variant I.

Although these non-idealities are present simultaneously, they will, for clarity, be treated separately below.

In general the drain current of an MOSFET (a four terminal device) is a function of three voltage differences. For hand calculations the source is usually used as reference terminal, so the three voltages are: the gate-source voltage (v_{gs}), the drain-source voltage (v_{ds}) and the source-bulk voltage (v_{sb}). The dependence on the drain-source voltage can be made small by having a big intrinsic gain ($g_m \cdot r_o$) and keeping the voltage gain low. The source-bulk voltage only changes in the common-gate stage, and therefor does not end up in the differential output.

The common-gate stage is degenerated, hence its nonlinearity is reduced. In the case of variant I by a factor

$$\frac{1}{1+\frac{1}{(g_{m1}+g_{m2})R_S \| R_{1,2}}} = \frac{1}{2} \tag{9.9}$$

In the case of variant I a fraction of

$$1-(g_{m3}+g_{m4})\cdot R_S \parallel \frac{1}{2}R_{1,2} = \frac{4R_S}{R_{1,2}+2R_S} \tag{9.10}$$

of the nonlinearity of the common-gate stage ends up at the output differentially. Multiplying (9.9) and (9.10) shows that for $R_S = 50\Omega$ and $R_{1,2} = 500\Omega$ a fraction of 14.3% of the nonlinearity remains. This gives an IIP3 of

$$V_{IIP3} = \sqrt{\frac{4}{3}\frac{b_{1,M1}+b_{1,M2}+b_{1,M3}+b_{1,M4}}{\frac{2R_S}{R_{1,2}+2R_S}(b_{3,M1}+b_{3,M2})+b_{3,M3}+b_{3,M4}}} \tag{9.11}$$

If the third-order nonlinearity of both stages is equal, the IIP3 due to the incomplete cancellation is 1.2 dB lower then the value found in section 9.1 for $R_S = 50\Omega$ and $R_{1,2} = 500\Omega$.

As shown in chapter 8 even purely quadratic devices produce third-order distortion. Ideally these are compensated in the complementary structure, but mismatch between N- and PMOS and differences in signal path to N- and PMOS may leave some residue. Approximating the circuit as quasi DC[1], the third-order component due to the second-order nonlinearity in the common-source output is

$$\begin{aligned} i_{IM3,CS} &= (-v_{s1}^2 b_{2,M1} + v_{s2}^2 b_{2,M2})(-v_{g3}b_{2,M3} + v_{g4}b_{2,M4}) && (9.12)\\ &= \big((-v_{s1}^2+v_{s2}^2)(b_{2,M1}+b_{2,M2}) + (v_{s1}^2+v_{s2}^2)(b_{2,M1}-b_{2,M2})\big) \\ &\quad \times ((v_{g3}+v_{g4})(b_{2,M3}-b_{2,M4}) + (-v_{g3}+v_{g4})(b_{2,M3}+b_{2,M4})) && (9.13) \end{aligned}$$

In which (9.13) rewrites (9.12) in terms of unequal amplitudes and incomplete compensation of the second-order nonlinearity. In reality all the signals in the circuits depend on the input voltage via different paths giving frequency dependent amplitudes and phases and the quadratic term consist of intermdulation products and harmonics at different frequencies. This makes quantitive evaluation cumbersome. But the effect of the different paths to NMOS and PMOS can be analyzed qualitatively for variant I.

[1] That is: assuming all signals have no reactive part and are frequency independent.

If the fundamentals, the second-order components and the lower third-order intermodulation product fall in band they may be treated as frequency independ. This allows the use of (9.13) for describing the effect of the difference in amplitude due to capacitive voltage division. In variant I the AC-voltage at the NMOS side will be lower than the voltage at the PMOS side: $v_{s1} < v_{s2}$ and $v_{g3} < v_{s4}$. In strong inversion the second-order derivative of the drain current to the gate-source voltage is positive ($b_2 > 0$) and the third-order derivative negative ($b_3 < 0$). This means that the contribution by (9.13) is in antiphase with that of third-order nonlinearity, a small capacitive attanuation thus leads to a higher IIP3.

The frequency dependence for in band fundamentals is caused by the second-order components at the difference frequency $f_1 - f_2$ and the harmonic at $2f_1$ generated in the common-gate stage. In the common-source stage these mix with fundamentals f_1 and f_2 respectively, contributing to the IM3 product at $2f_1 - f_2$. Because for small two-tone spacings the difference frequency generated by M1 cannot flow through capacitor C_1 it will create a bigger second-order component at the gate of M3. So this contribution by the NMOS to the third-order intermodulation product, which is in phase with the contribution by the third-order nonlinearity, increases with decreasing tone spacing.

For large two-tone spacings the IIP3 of variant I will thus be higher than predicted by the third-order Taylor coefficients and it decreases with decreasing tone-spacing. In variant II these effects do not occur.

9.3 Balance under interference

Disbalance is caused by odd-order common-mode components, as explained in chapter 7. This section will only take into account the third-order component and therefor only applies for small disbalances. For a common-gate and common-source combination of which each second-order Taylor coefficient is zero this is composed of two parts.

- The third-order nonlinearity of the common-gate stage ($b_{3,CG}$) which is halved by the source degeneration and due to the noise canceling mechanism fully common-mode.
- The third-order nonlinearity of the common-source stage ($b_{3,CS}$) which is only present in one output and thus half common-, half differential-mode.

The positive direction of the drain current of the common-source stage is opposite to the direction of the output current of that stage, hence the nonlinearities get a minus sign. The common-mode gain (common-mode output component at the fundamental frequency divided by the input signal) due to an interferer with amplitude A_{int} is

$$G_{CM} = b_{1,CG} - b_{1,CS} + \frac{3}{2} \cdot (b_{3,CG} - b_{3,CS}) A_{int}^2 \tag{9.14}$$

This shows that when the third-order nonlinearities of the stages are equal the balance is not degraded by interference.

10 Large signal behavior

In the previous section a small signal model using only three Taylor coefficients has been used for the MOSFETs. For large signals the contribution of higher order terms becomes significant. For this reason a large signal model is used in this chapter.

Variation of the transconductances gives two unwanted large signal effects:

- a reduction of the differential output gain, i.e. compression
- an increase in the common-mode output gain, i.e. disbalance

which are described in the following two subsections.

10.1 Compression

The current gains for both variants were derived in chapter 4 as (4.6) and (4.16) for variant I and II respectively. To find the desensitizing effect of a change in transconductance of the common-gate stage on the gain the derivative of the gain is taken, for variant I this gives

$$\frac{\mathrm{d}\, A_i}{\mathrm{d}\, g_{m,CG}} = 2R_S \frac{1 - g_{m,CS} \cdot RS \parallel R_{1,2}}{(1 + g_{m,CG} \cdot R_S \parallel R_{1,2})^2} \tag{10.1}$$

Which shows that if $g_{m,CS} = \frac{1}{RS \| R_{1,2}}$ the overall gain does not change with a variation in transconductance of the common-gate stage, this is the same condition as that for full noise cancellation. For variant II this derivative gives

$$\frac{\mathrm{d}\, A_i}{\mathrm{d}\, g_{m,CG}} = 2R_S \frac{\frac{R_{1,2}}{R_{1,2}+2RL} - g_{m,CS} R_S}{(1 + g_{m,CG} R_S)^2} \tag{10.2}$$

which is zero for $g_{m,CS} = \frac{R_{1,2}}{R_S \cdot (R_{1,2}+2R_L)}$, again the same condition as for full noise canceling.

In the same way the effect of a change in transconductance of the common-source stage is found, which gives for variant I

$$\frac{\mathrm{d}\, A_i}{\mathrm{d}\, g_{m,CS}} = 2 \frac{R_S \parallel R_{1,2}}{1 + g_{m,CG} \cdot R_S \parallel R_{1,2}} \tag{10.3}$$

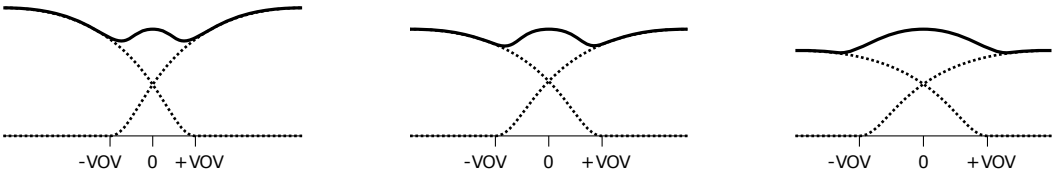
and for variant II

$$\frac{\mathrm{d}\, A_i}{\mathrm{d}\, g_{m,CS}} = 2 \frac{R_S}{1 + g_{m,CG} R_S} \tag{10.4}$$

Both show that the gain varies linearly with a change in transconductance of the common-source stage. Since the rate of change of the transconductance with input voltage should be similar for both stages to maintain large signal balance as explained in the next section, the common-source stage dominates the compression behavior. The transconductance of this stage is affected by two competing effects:

1. When the input voltage is bigger than the overdrive of the common-source transistors its transconductance, assuming square law behavior, increases with input voltage and hence the gain of the LNA increases with input power.
2. Non-ideal behavior like mobility reduction and velocity saturation makes the transconductance of MOSFETs to decrease with gate-source voltage and hence the gain of the LNA decreases with input power.

Increasing the DC overdrive reduces the first effect and increases the second, thus the compression point increases with decreasing DC overdrive. This is sketched in Fig. 10.1.



(a) Low overdrive (b) Medium overdrive (c) High overdrive

Fig. 10.1: Transconductance as function of input voltage for different DC overdrive voltages

The effect of mobility reduction and velocity saturation on the drain current can be modeled [18, subsection 16.2.3] as

$$I_D = K \cdot \frac{V_{OV}^2}{1 + \left(\theta + \frac{\mu_0}{2 v_{sat} L}\right) \cdot V_{OV}} \tag{10.5}$$

In which θ is empirical parameter modeling the mobility reduction due to the lateral field, v_{sat} the saturation velocity, μ_0 the low-field mobility and L the gate length. Taking the derivative to the overdrive voltage gives the transconductance

$$g_m\left(V_{OV}\right) = K \cdot \frac{V_{OV} \cdot \left(2 + \left(\theta + \frac{\mu_0}{2 v_{sat} L}\right) \cdot V_{OV}\right)}{\left(1 + \left(\theta + \frac{\mu_0}{2 v_{sat} L}\right) \cdot V_{OV}\right)^2} \tag{10.6}$$

An optimal compression behavior is achieved when the transconductance for big input amplitudes is the same as for zero input voltage, the situation sketched in Fig. 10.1b. This requires that the overdrive is chosen as half the asymptotic value, which is

$$\lim_{V_{OV} \to \infty} g_m\left(V_{OV}\right) = \frac{K}{\theta + \frac{\mu_0}{2 v_{sat} L}} \tag{10.7}$$

Solving

$$g_m\left(V_{OV}\right) = \frac{1}{2} \cdot \frac{K}{\theta + \frac{\mu_0}{2 v_{sat} L}} \tag{10.8}$$

for V_{OV} gives

$$V_{OV,opt.compr.} = \frac{\sqrt{2} - 1}{\theta + \frac{\mu_0}{2 v_{sat} L}} \tag{10.9}$$

Denoting the nominal transconductance, which is equal to the asymptotic value and twice the value at $V_{OV,opt.compr.}$, of the common-source stage as $g_{m,nom}$ the minimal instantaneous transconductance can be expressed as

$$g_{m,min} = \frac{4 \cdot (2 - \sqrt{2})}{(2\sqrt{2} - 1)^2} \cdot g_{m,nom} \tag{10.10}$$

Which shows that the dips in Fig. 10.1b are at 70% of the top value according to this model. In reality it will be slightly higher since the MOSFETs do not turn off as abruptly at $V_{OV} = 0$ as (10.6) describes but at low overdrive enter the weak inversion regime where this model does not hold.

The model used in this section can in principle also be used to calculate the IIP3. However whereas it describes the transconductance with reasonable accuracy the higher derivatives yield results that are to inaccurate to be used for designing. Therefor data extracted from a simulation model will be used in chapter 12 when designing. Nevertheless the result that for the overdrive in (10.9) the input referred third-order intercept voltage is inversely proportional to $\theta + \frac{\mu_0}{2 v_{sat} L}$ does show how the IIP3 depends on technology parameters and gate length.

10.2 Balance

When using only one polarity the transconductances of both stages change in opposite direction with input current, creating a common-mode output component as described in chapter 8. In the proposed complementary design the variation in the transconductance of n- and p-channel MOSFETs largely compensate each other. Imbalance means that there is a common-mode output component, which for variant I is

$$A_{CM} = \frac{i_{CG} + i_{CS}}{i_s} = 2\frac{(g_{mCG} - g_{mCS}) \cdot R_S \parallel R_{1,2}}{1 + g_{m,CG}R_S \parallel R_{1,2}} \tag{10.11}$$

and for variant II is

$$A_{CM} = \frac{i_{CG} + i_{CS}}{i_s} = 2\frac{(g_{mCG} \cdot \frac{R_{12}}{R_{12}+2R_L} - g_{mCS})R_S}{1 + g_{m,CG}R_S} \tag{10.12}$$

These equations show that if the transconductances satisfy

$$g_{mCG} = g_{mCS}$$

and

$$g_{mCG} \cdot \frac{R_{12}}{R_{12} + 2R_L} = g_{mCS}$$

for variant I and II respectively the output is balanced. To the first (the top value in fig 10.1) and second order (the top in Fig. 10.1 is at $V_{IN} = 0$) this is satisfied by design. For higher orders this is not necessarily the case. The third-order (the curvature in fig 10.1) may still be chosen equally by choosing the right quiescent current but here there is a trade-off: for good noise performance a low quiescent current is preferred for the common-gate stage while for good linearity a high quiescent current is preferred for the common-source stage. For higher orders equality cannot be guaranteed because

- The MOSFETS are at a different DC level, changing their characteristics.
- In the common-gate stage not only the gate-source voltage but also the source-bulk voltage vary. And the drain-source voltage in the common-gate stage changes more than in the common-source stage.

11 Design procedure

Using the foregoing analysis a two step design procedure is developed. First overdrives, the quiescent currents and the gate widths of the MOSFETs are found based on the noise and linearity requirements. Secondly the MOSFETs are scaled to compensate for the capacitive attanuation so the output is balanced at midband. The schematics for variant I and II are repeated below as Fig. 11.1 for convenience.

11.1 Biasing point

For the common-gate stage two requirements determine the overdrives and the quiescent current.

1. Noise and gain, favoring a low quiescent current
2. Large signal balance, favoring a medium overdrive

Choosing some minimum resistance and maximum voltage drop over this resistance gives the quiescent current, for this current a overdrive and width combination is then iteratively found that satisfies:

$$b_{1,M1} + b_{1,M2} = \frac{1}{R_S} - \frac{1}{R_1 + R_2} \qquad b_{2,M1} = b_{2,M2}$$

There are two requirements that give conditions for the overdrive of the common-source stage.

1. Linearity, favoring a high overdrive
2. Compression, favoring a medium overdrive

Designing for a specified linearity proceeds as follows

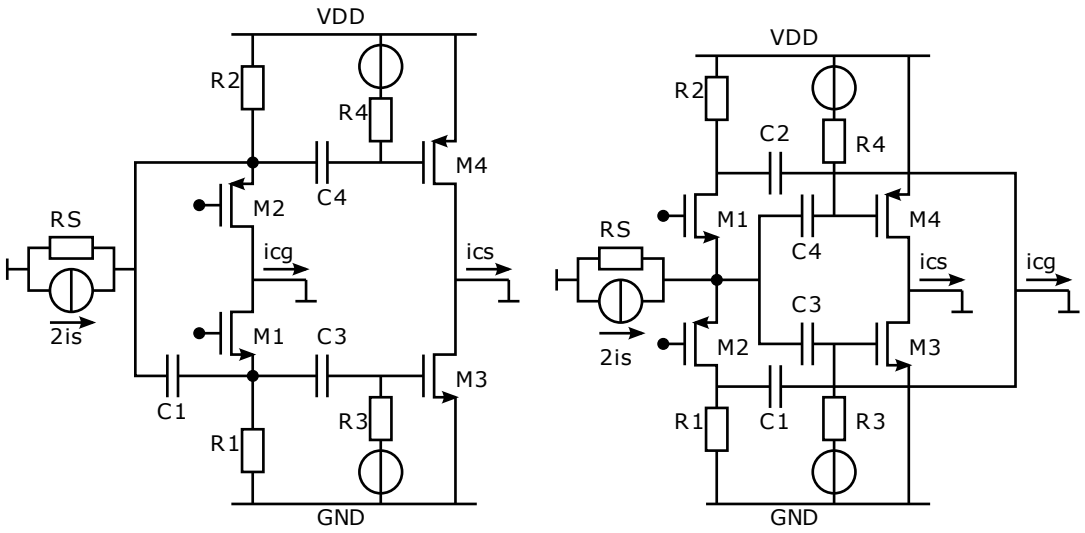
- The minimum overdrive is found from the IIP3 requirement minus 3 dB and the intrinsic IIP3.
- The overdrive of the device that has the biggest quadratic component is increased a bit so that the quadratic components are equal. Since the DC currents of both N- and PMOS have to be equal it is useful to first normalize the second-order component to the drain current.
- The drain current is found by dividing the required transconductance by the sum of the transconductances normalized to the drain current at the previously found overdrive of the N- and PMOS.

$$i_{d,CS} = \frac{g_{m,CS}}{\frac{g_{m,N}}{i_{d,N}} + \frac{g_{m,P}}{i_{d,P}}}$$

- Finally the widths are found by dividing the drain current by the current density at the previously found overdrives.

Alternatively the design can be for optimum compression as given by (10.9). As the excact technology parameters may be unknown the optimum overdrive level may be obtained from a transconductance vs. gate-source voltage plot. In this case the first two steps are:

- The maximum overdrive for N- and PMOS is found as the overdrive at which the transconductance is half the maximum value.
- The overdrive of the device that has the smallest quadratic component is shifted down until the the quadratic components are equal. Again normalization to the DC current is useful.



(a) Variant I (b) Variant II

Fig. 11.1: Schematics of the LNA designs with biasing circuits for M1 and M2 omitted

11.2 Capacitive attenuation compensation

Different from variant I, in variant II the output of the common-gate stage is also attenuated.This reduces the common-gate output current by fractions of approximately

$$\frac{C_1}{C_1 + C_{1a}} \quad \text{and} \quad \frac{C_2}{C_2 + C_{2a}}$$

These fractions are fixed by the technology and normally equal. The make the output currents equal again the output current of the common-source stage for variant II will be reduced by the same fraction.

Both variants have in common that the AC coupling between both stages causes attenuation. The gate voltage of M3 with respect to the source voltage of M1 is attenuated by

$$\frac{v_{g3}}{v_{s1}} = \frac{C_3}{C_3 + C_{3b} + C_{M3}}$$

Similarly the gate voltage of M4 with respect to the source voltage of M2 is attenuated by

$$\frac{v_{g4}}{v_{s2}} = \frac{C_4}{C_4 + C_{4b} + C_{M4}}$$

The coupling capacitance is chosen such that the smallest plate to ground capacitance is equal to the gate capacitance of the MOSFET it is driving. Choosing a smaller value increases the attenuation and therefore deteriorates the noise performance and increases power consumption, choosing a larger value hardly decreases the attenuation while reducing the bandwidth and matching.

To compensate for the losses the widths found for M3 and M4 using the steps in the previous section are scaled as

$$W_{3,I} = W_3 \frac{C_3 + C_{3b} + C_{M3}}{C_3} \qquad W_{4,I} = W_4 \frac{C_4 + C_{4b} + C_{M4}}{C_4}$$

and

$$W_{3,II} = W_3 \frac{C_3 + C_{3b} + C_{M3}}{C_3} \frac{C_1}{C_1 + C_{1a} + C_{1b}} \qquad W_{4,II} = W_4 \frac{C_4 + C_{4b} + C_{M4}}{C_4} \frac{C_1}{C_1 + C_{1a} + C_{1b}}$$

for variant I and II respectively.

12 Design example

In this section the proposed topology is implemented step by step in a 0.14 µm CMOS technology, following the steps in the previous chapter. For the capacitors asymmetrical plate-to-ground parasitic capacitors of 10% and 5% of their value will be used.

For reasonable noise performance the biasing resistors should be limited to 500 Ω. Choosing the source voltages of M1 and M2 at a quarter of the supply voltage gives a quiescent current of 900 µA. The transconductance of the common-gate stage should, not yet taking into account the capacitive voltage division, be 16 mS for variant I and 20 mS for variant II and the second-order Taylor coefficient should be zero. For variant I this gives gate widths of

$$W_1 = 24\mu\text{m} \qquad W_2 = 56\mu\text{m}$$

and gate-source voltages of

$$V_{GS1} = 713\text{mV} \qquad V_{GS2} = 812.5\text{mV}$$

For variant II this gives gate widths of

$$W_1 = 33\mu\text{m} \qquad W_2 = 91\mu\text{m}$$

and gate-source voltages of

$$V_{GS1} = 729\text{mV} \qquad V_{GS2} = 843\text{mV}$$

In Fig. 12.3b and Fig. 12.4b the resulting transconductance as function of the input voltage are shown as the dashdotted line. The transconductance decreases a bit with amplitude from the intended 16 and 20 mS for small input voltages but increases again for big (>200mV) swings. Fig. 12.3c and 12.4c confirm that the second-order component of the common-gate stage (dashdotted) is indeed zero at $V_{IN} = 0$.

To find the intrinsic Taylor coefficients of the MOSFETs the gate voltage is swept, while the drain voltage is kept constant and the drain current is measured. This current and the higher Taylor coefficients computed with (9.2), normalized to 1 µm gate-width, are plotted as Figs. 12.1a to 12.1d and Figs. 12.2a to 12.2d. From these the intrinsic IIP3 is computed which is plotted in Fig. 12.1g and Fig. 12.2g. These show that for 9dBm intrinsic IIP3 a gate-source voltage of 700mV is needed for the NMOS, while for the PMOS any value will do. Therefor the gate-source voltage of the NMOS is fixed to 700mV, at which the second-order Taylor coefficient normalized to the DC current, plotted in Fig. 12.1f, is 7.286 V^{-2}. The gate-source voltage of the PMOS is chosen such that its second-order Taylor coefficient is the same which reading off Fig. 12.2f is at 754 mV.

At these gate-source voltages the transconductance normalized to the DC current, plotted in Fig. 12.1e and 12.2e is 6.2519 V^{-1} and 5.7018 V^{-1} for N- and PMOS respectively. For variant I the transconductance of N- and PMOS combined should be $20 - \frac{1}{0.25} = 16\text{mS}$, which requires a quiescent drain current of

$$I_{DCS,I} = \frac{16}{6.2519 + 5.7018} = 1.34\text{mA}$$

For variant II the transconductance of N- and PMOS combined should be $20 \cdot \frac{250}{275} = 18.2\text{mS}$, which requires a quiescent drain current of

$$I_{DCS,II} = \frac{18.2}{6.2519 + 5.7018} = 1.52\text{mA}$$

At 700 mV and 754 mV the drain current per gate width, plotted in Fig. 12.1a and Fig.12.2a, is 61.88 A/m and 26.13 A/m for N- and PMOS respectively. Which for variant I gives widths of

$$W_3 = \frac{1.34}{0.06188} = 21.6\mu\text{m} \qquad W_4 = \frac{1.34}{0.02613} = 51.2\mu\text{m}$$

and for variant II of

$$W_3 = \frac{1.52}{0.06188} = 24.6\mu\text{m} \qquad W_4 = \frac{1.52}{0.02613} = 58.2\mu\text{m}$$

Figs. 12.3b and 12.4b shows the resulting transconductance (dashed) as function of the input voltage for variant I and II respectively. The transconductance drops with input voltage, but stabilizes for big (>250mV) swings. Fig. 12.3b and Fig. 12.4b also show the differential (solid line) and common-mode (dotted line) output Taylor coefficients when both stages are connected. The differential transconductance is 31.8 mS for variant I and for variant II it is 36mS. The common-mode transconductance is near zero for small (<175 mV) input swings, for bigger swing the balance degrades. Reading off fig 12.3d and 12.4d shows that the third-order components are 25.4 $^{\text{mA}}/_{\text{V}^3}$ and 23.4 $^{\text{mA}}/_{\text{V}^3}$, which predicts third-order intercept points at 12.2 and 13.1 dBm for variant I and variant II respectively.

Next the widths are corrected for the capacitive attenuation, with the smallest parasitic plate-to-ground capacitance at 5% this is 10% between the two stages and 5% at the common-gate output for variant II.
For variant I this gives gate widths of

$$W_3 = 23.8\mu\text{m} \qquad \text{and} \qquad W_4 = 56.3\mu\text{m}$$

which gives associated gate-to-channel (c_{gg}) and overlap (c_{gol}) capacitances of

$$c_{gg3} = 16.6\text{fF} \qquad c_{gol3} = 10.9\text{fF} \qquad c_{gg4} = 42.5\text{fF} \qquad c_{gol4} = 34.0\text{fF}$$

from which the value of the coupling capacitances can be calculated

$$C_3 = 550\text{fF} \qquad C_4 = 1530\text{fF}$$

For variant II this gives gate widths of

$$W_3 = 25.8\text{fF} \qquad W_4 = 61\text{fF}$$

which gives capacitances of

$$c_{gg3} = 18.0\text{fF} \qquad c_{gol3} = 11.8\text{fF} \qquad c_{gg4} = 46.1\text{fF} \qquad c_{gol} = 37.0\text{fF}$$

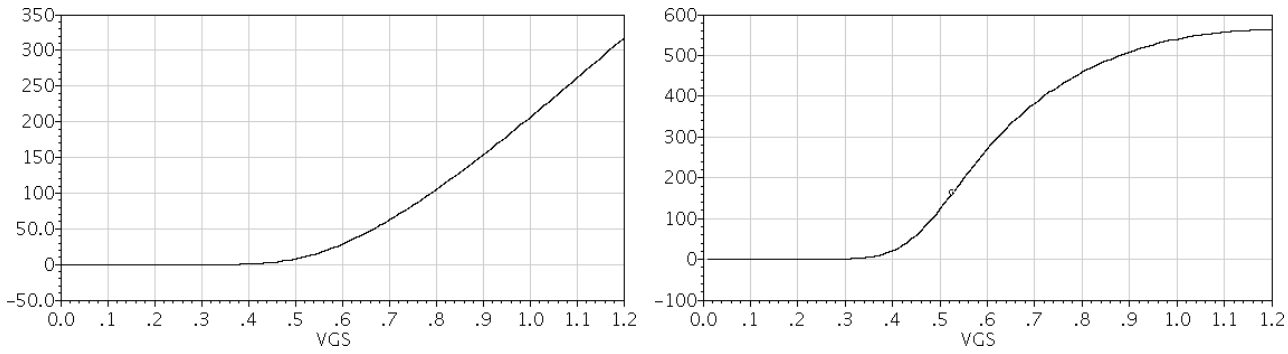
from which the value of the coupling capacitances can be calculated

$$C_3 = 596\text{fF} \qquad C_4 = 1662\text{fF}$$

Table 12.1 lists the main component values found in this chapter, together with the coupling capacitors found in chapter 5.

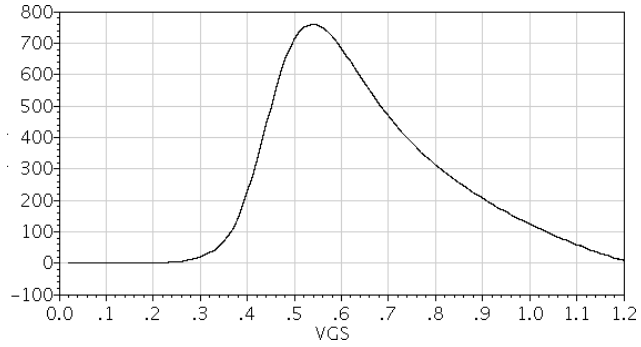
Component(s)	Variant I	Variant II
W1 [µm]	24	33
W2 [µm]	56	91
W3 [µm]	24.6	23.8
W4 [µm]	58.2	56.3
R1 [Ω]	500	500
R2 [Ω]	500	500
C1 [pF]	4	4
C2 [pF]		4
C3 [pF]	0.55	0.6
C4 [pF]	1.53	1.66

Table 12.1: Component values used for simulation

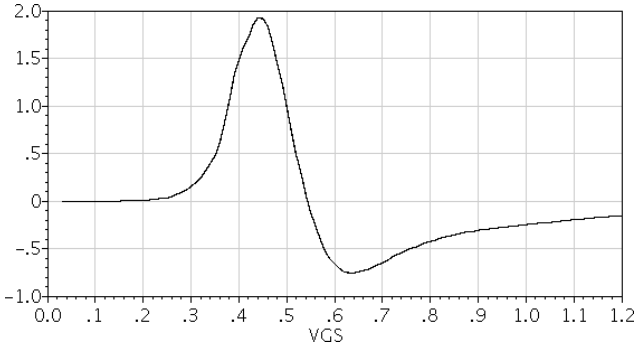


(a) b0 ($\mu A/\mu m$)

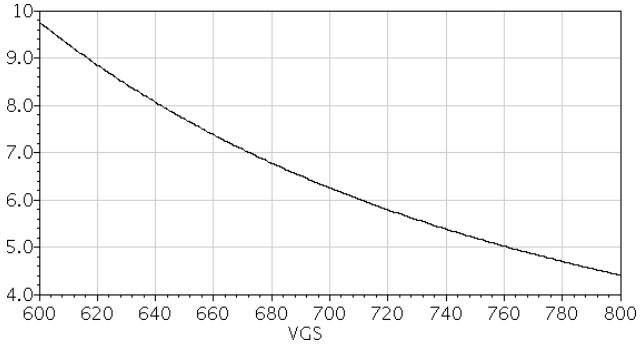
(b) b1 ($\mu S/\mu m$)



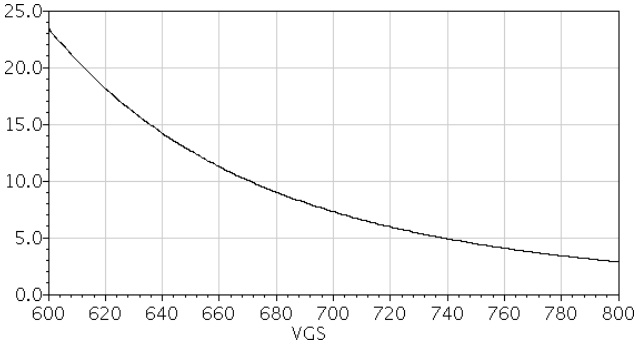
(c) b2 ($\mu A/\mu m \cdot V^2$)



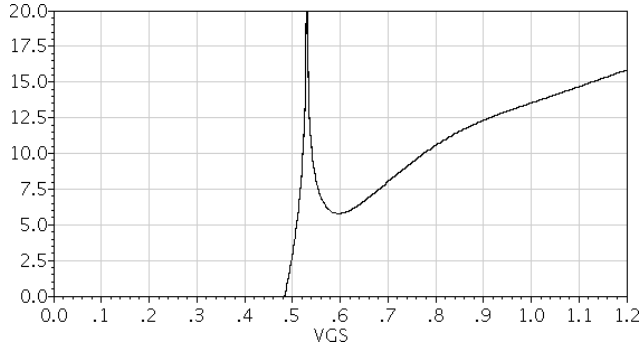
(d) b3 ($mA/\mu m \cdot V^3$)



(e) b1 normalized to b0 (V^{-1})

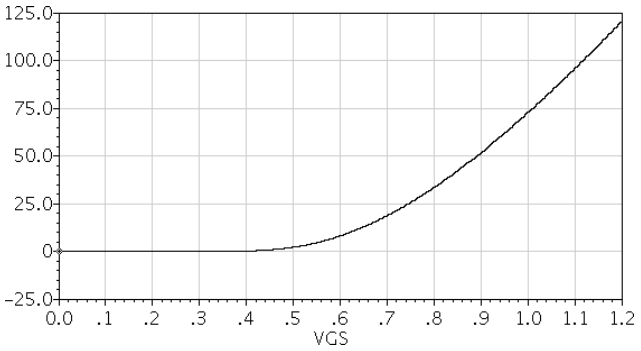


(f) b2 normalized to b0 (V^{-2})

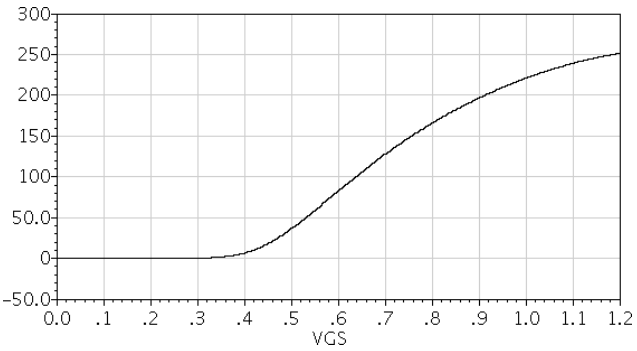


(g) IIP3 (dBm)

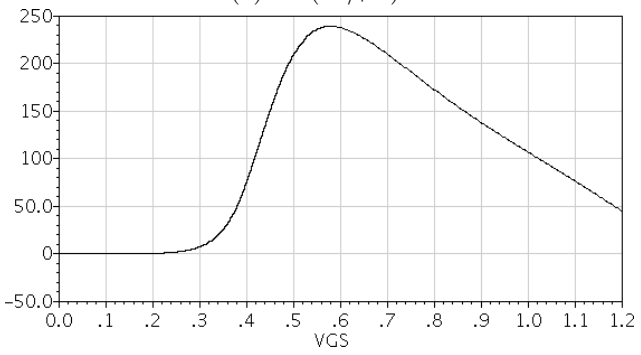
Fig. 12.1: Intrinsic Taylor coefficients and IIP3 of a 0.14 um NMOS



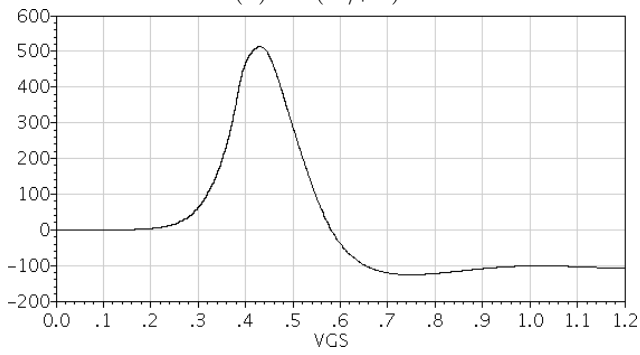
(a) b0 ($\mu A/\mu m$)



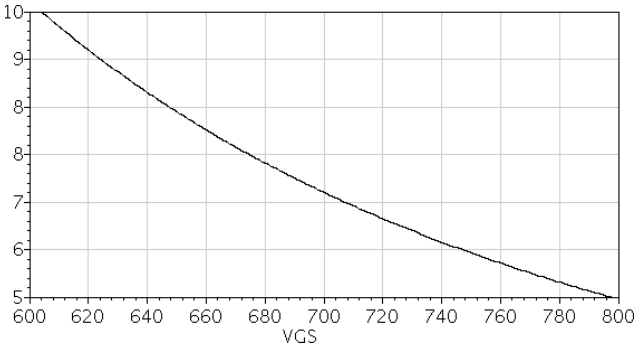
(b) b1 ($\mu S/\mu m$)



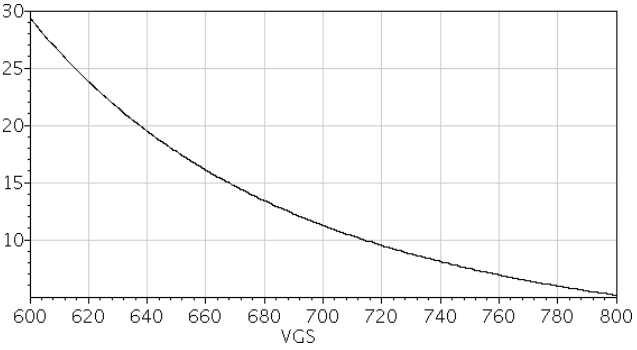
(c) b2 ($\mu A/\mu m \cdot V^2$)



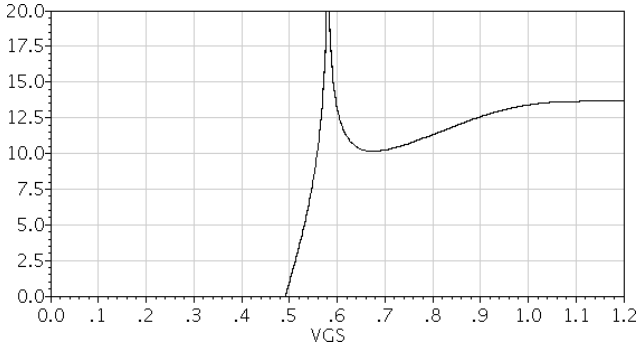
(d) b3 $\mu A/\mu m \cdot V^3$



(e) b1 normalized to b0 (V^{-1})

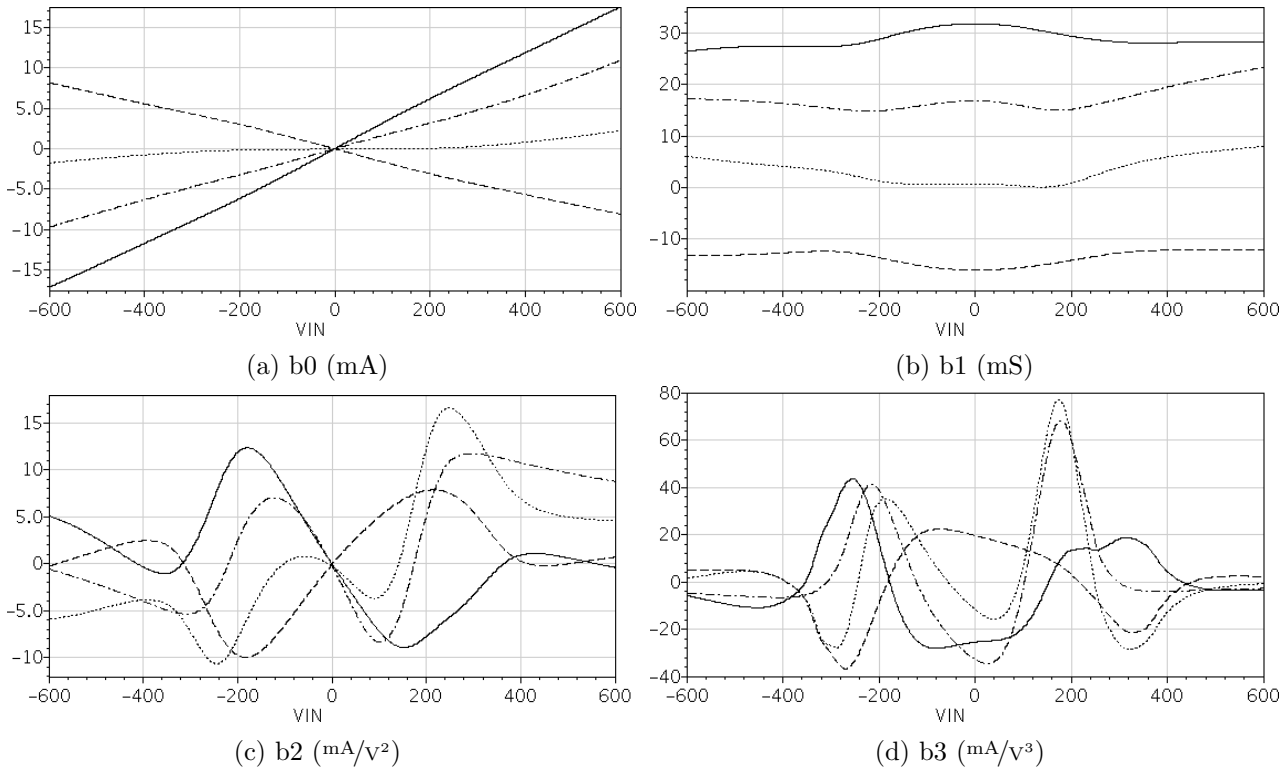


(f) b2 normalized to b0 (V^{-2})



(g) IIP3 (dBm)

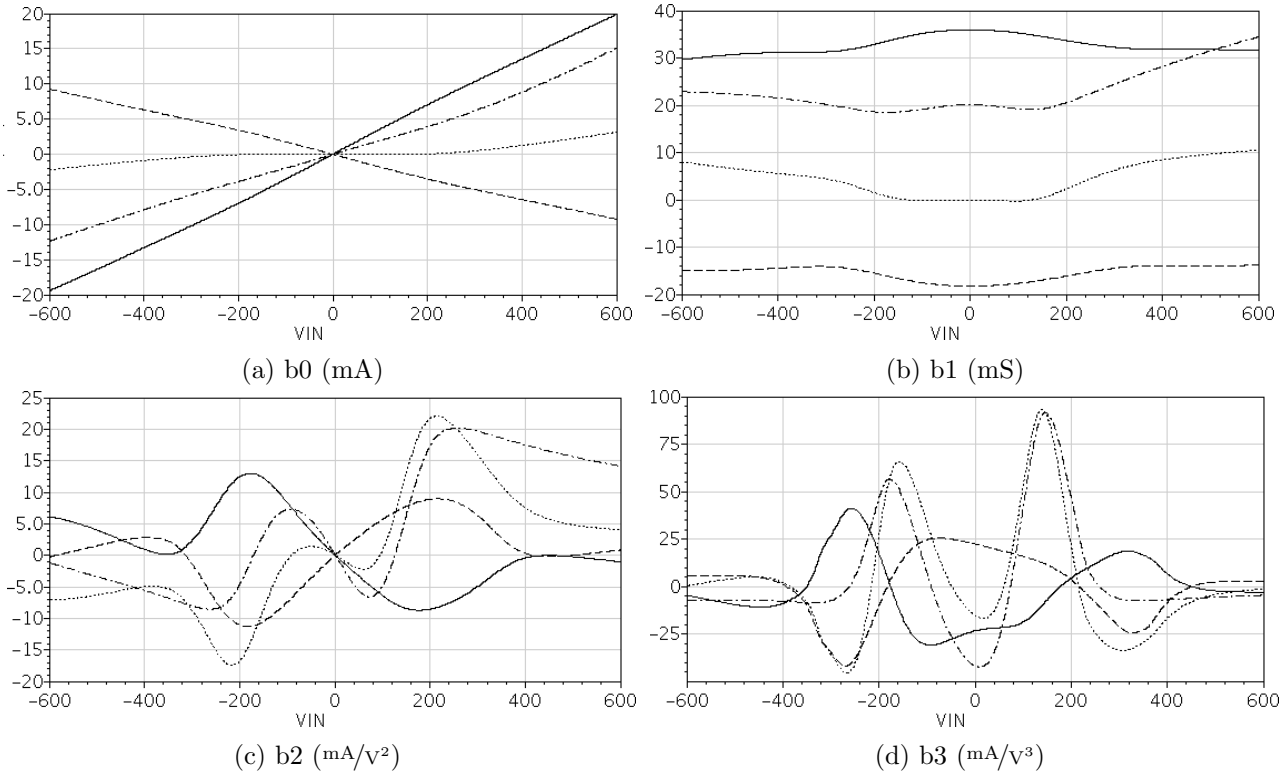
Fig. 12.2: Intrinsic Taylor coefficients and IIP3 of a 0.14 um PMOS



(a) b0 (mA) (b) b1 (mS)

(c) b2 (mA/V²) (d) b3 (mA/V³)

Fig. 12.3: Taylor coefficients of variant I. Solid: differential output, dashed: common-gate stage separate, dashdotted: common-source stage separate, dotted: common output



(a) b0 (mA) (b) b1 (mS)

(c) b2 (mA/V²) (d) b3 (mA/V³)

Fig. 12.4: Taylor coefficients of variant II. Solid: differential output, dashed: common-gate stage separate, dashdotted: common-source stage separate, dotted: common output

13 Simulation results

Both variants in Fig. 3.3 are simulated, using the values listed in table 12.1. The antenna is modeled as a 50 Ω resistor, the mixer in series with the IF-amplifier as a 25 Ω resistor and the supply voltage is 1.8V. The simulations were done with SpectreRF using a MOS Model 11 model for the 0.14 μm CMOS process by NXP.

The first property simulated is the small signal current gain for frequencies from 200 MHz to 5 GHz, reading off Fig. 13.1a gives a mid-band gain of 3.5 dB for variant I and 4.6 dB for variant II. The 1-dB band for variant I runs from 320 MHz to 3.4GHz and for variant II runs from 106 MHz (outside the plotted range) to 2.94 GHz, which shows that the bandwidth requirements are met. In Fig. 13.1b the gain to the individual outputs is shown, the outputs are not exactly balanced due to the approximations used when designing: for variant I the difference is 0.44 dB and for variant II this is 0.13 dB at 1 GHz. Furthermore Fig. 13.1b shows that the bandwidth for the common-source stage is bigger than for the common-gate stage in variant II due to the AC-coupling at only one output. Related to the bandwidth are the input impedance and input reflection coefficient, which are shown in Figs. 13.1c and 13.1d respectively. These conform well to the those found by calculation in chapter 6. Fig. 13.1f shows the normalized input impedance on a Smith chart.

Next the noise figure is simulated over the same frequency range, the result is shown in Fig. 13.1e, from which a noise figure of 5.2dB and 4.6dB at 1GHz for variant I and II respectively can be read off. The first value is considerably higher than predicted by (4.5) due to the capacitive attenuation as explained in section 4.4. Table 13.2 list the relative noise contributions of the individual components at 1GHz. The common-source stage contributes most noise followed by the antenna resistance. The rest of the components follows at a considerable gap, though the values for R1 and R2 underestimates their effects since they do not only contribute noise themselves but also cause attenuation. The noise contribution of the common-gate stage is bigger for variant I then for variant II since in the former the noise is not fully canceled.

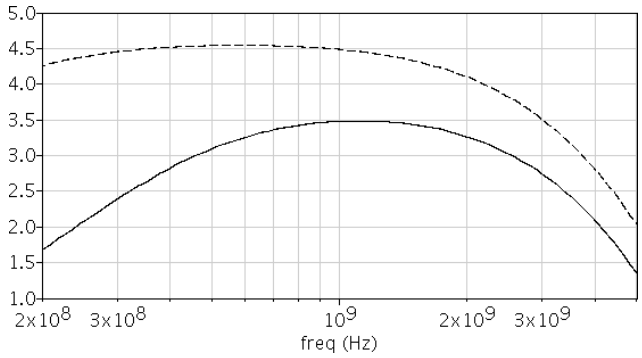
For characterizing the nonlinearity the IIP3 is simulated with a two tone test. The tones are chosen at 1GHz and 1.1GHz, giving a third-order intermodulation product at 900 MHz. Figs. 13.2a and 13.2b shows one of the fundamentals and the lower in-band third-order intermodulation product at the output, which (extrapolated from -20 dBm input level) intercept at an input power level of 14.8 dBm and 13.9 dBm for variant I and II respectively. For showing the frequency dependence of the nonlinearity the IIP2 and IIP3 are simulated as function of frequency. For simulating the IIP3 two tones, one at 1.0 GHz and one swept from 1.0 to 1.5 GHz are applied at the input with a power level of -20dBm. This gives a third-order intermodulation product that runs from 1.0 GHz downto 500 MHz. For simulating the IIP2 the second tone is swept from 1.5 to 2.0 GHz, which gives an second-order intermodulation product wich sweeps from 500 MHz to 1GHz. Figs. 13.2d and 13.2c show the resulting intercept points as function of the frequency of the swept fundamental. Clearly the third-order intercept point is strongly frequency dependent for variant I, which is a result of the frequency depended cascade of the second-order nonlinearities as explained in section 9.2. The same incomplete compensation of the second-order intermodulation product that makes the third-order intercept higher also makes the second-order intercept point lower in variant I.

To find the compression point a single tone at 1GHz is applied at the input and its power swept, compared to the extrapolated small signal gain the gain is reduced by one decibel at an input power level of 4.0 dBm for variant I and 5.0 dBm for variant II. Related to compression is the large signal balance. This is simulated using two tones, one at 1.2 Ghz and one at 800 MHz, where the first tone is kept constant and the second is swept in power. Fig. 13.2e shows the imbalance at the output in the fundamental whose power remained constant as function of the power of the other fundamental. Until the compression point the imbalance remains reasonable.

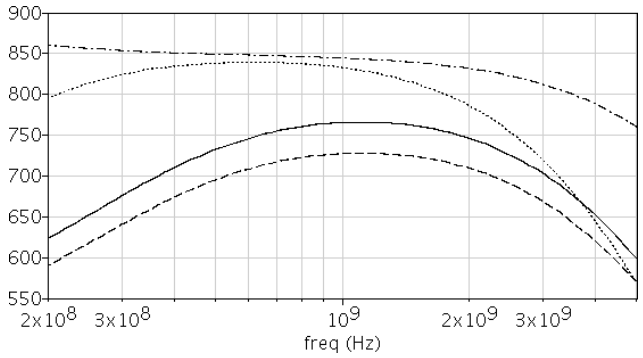
Table 13.1 lists the main simulation results of this chapter.

Property	Variant I	Variant II
P (mW)	4.3	4.4
Optimum current gain (dB)	3.5	4.6
Optimum noise figure (dB)	5.2	4.6
- 1dB bandwidth (GHz)	0.32 - 3.4	0.10 - 2.94
S_{11} @ 2.5 GHz (dB)	-7.2	-12.3
$IIP3$ @ $f_1 = 1$GHz & $f_2 = 1.1$GHz (dBm)	14.8	13.9
- 1 dB compression point (dBm)	4.0	5.0
Maximum imbalance due to interference (dB)	1.17	0.81

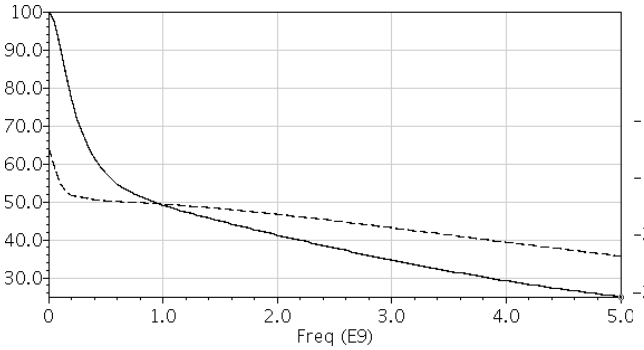
Table 13.1: Main numbers found by simulation



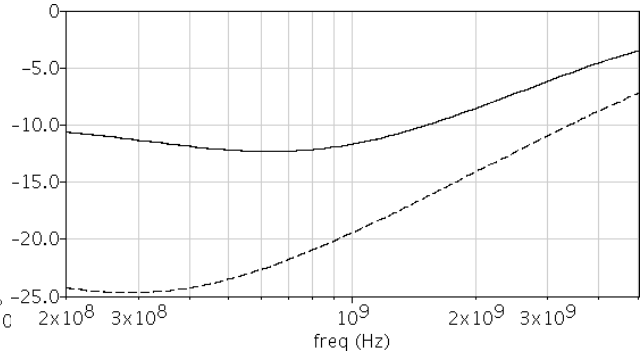
(a) AC current gain (dB)
solid: var. I, dashed: var. II



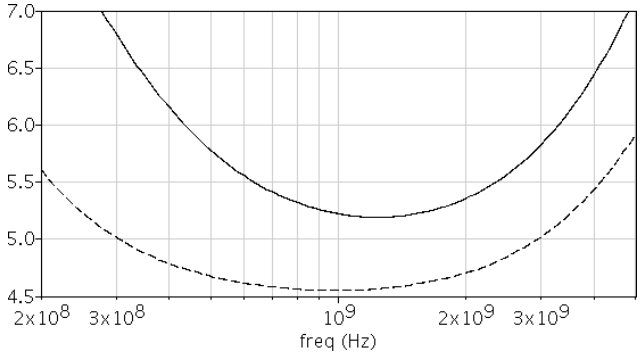
(b) AC gain to individual outputs (10^{-3})
solid: non-inverting output of var. I, dashed: inverting output of var. I, dotted: non-inverting output of var. II, dotdashed: inverting output of var. II



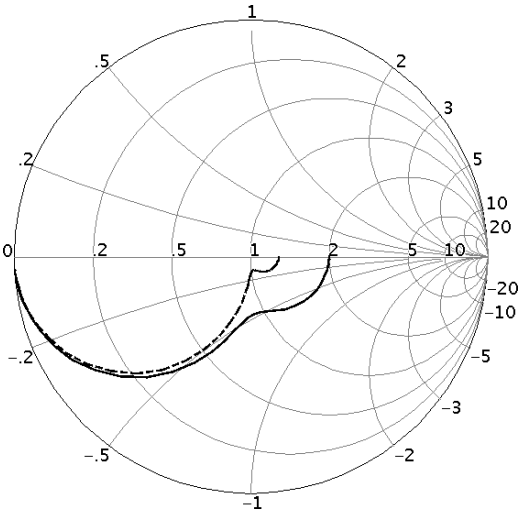
(c) Input impedance (ohm)
solid: var. I, dashed: var. II



(d) Input reflection coefficient (dB)
solid: var. I, dashed: var. II



(e) Noise Figure (dB), solid: var. I, dashed: var. II

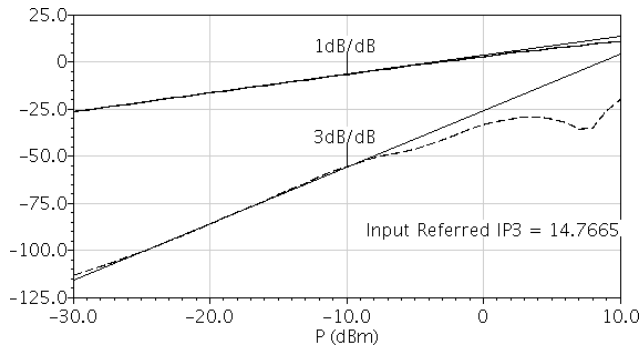


(f) Z-Smith chart showing the input impedance, solid: var. I, dashed: var. II

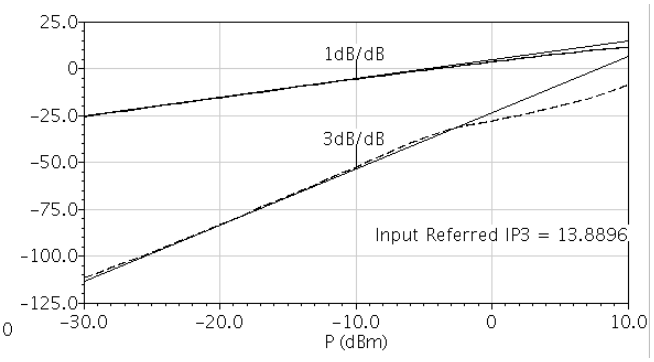
Fig. 13.1: Small signal simulation results

Component(s)	Variant I	Variant II
M3 + M4	32.36+23.88=56.24%	32.35+23.85=56.2%
RS	30.03%	35.05%
R1+R2	4.48+3.11=7.59%	3.64+3.75=7.39%
M1+M2	3.60+1.18=4.78%	0.06+0.04=0.1%
R3+R4	0.31+0.86=1.17%	0.69+0.34=1.03%

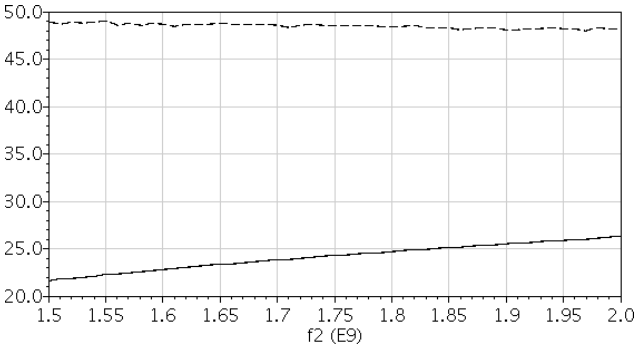
Table 13.2: Relative noise contributions



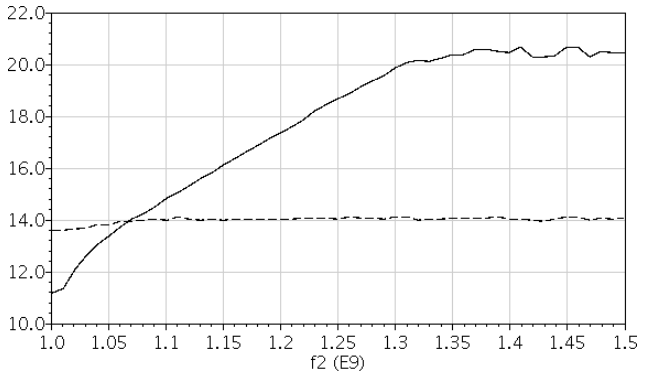
(a) Third-order intercept plot (dBm) variant I
solid: fundamental, dashed: IM3



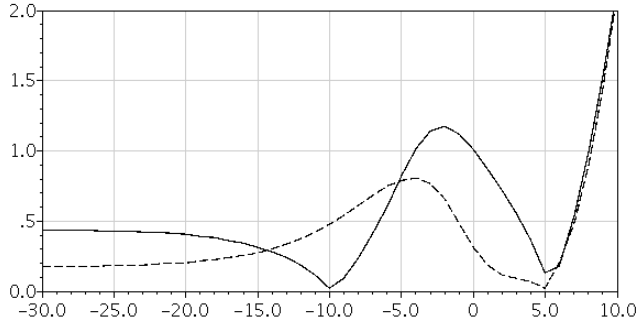
(b) Third-order intercept plot (dBm) variant II
solid: fundamental, dashed: IM3



(c) IIP2 (dBm) as function of frequency
solid: var. I, dashed: var. II



(d) IIP3 (dBm) as function of frequency
solid: var. I, dashed: var. II



(e) Imbalance (dB) as function of interferer level (dBm)

Fig. 13.2: Periodic steady state simulation results

14 Conclusions

This thesis has shown the need for an LNA with differential outputs which remain balanced under strong interference in an interference-robust, wideband receiver front-end. It has shown that an imbalance in the LNA output results in significant wideband second-order intermodulation in the mixer.

It was explained that interferer induced imbalance is caused by third-order common-mode nonlinearity. It was shown how the noise cancelling mechanism, wich uses feedback and cascading, causes this third-order distortion, even when only square-law devices are present and the input-output relation is linear.

An inductorless topology using a complementary common-gate and common-source stage that allows class AB operation has been proposed. The complementary structure allows NMOS and PMOS second-order non-linearity to compensate eachother. Due to this class AB operation it is power efficient, the quiescent current is less than a fifth of the peak output current. Of this topology two variants have been presented, one with AC-coupling at the input and one with AC-coupling at the output. Their properties have been analyzed and this analysis has been verified by simulation.

The noise figure and gain have been derived and it has been shown how these depend on biasing. To obtain reasonable noise figures the quiscent current of the common-gate stage is limited to about 1 mA in a 1.8 V supply voltage. The differences between the variants are

- AC-coupling at the output gives a lower noise figure because the AC-coupling at the input leads to attenuation of the input signal.
- AC-coupling at the output gives a slightly higher gain.

An AC-analysis has been performed which shows that for a 15% parasitic plate-to-ground capacitance a bandwith of more than a decade can be achieved. Here the differences between the variants are

- AC-coupling at the output gives a bigger relative bandwidth, but AC-coupling at the input gives a balanced output over the whole frequency band.
- AC-coupling at the output gives better input matching, but AC-coupling at the input gives a more balanced output impedance.

The balance may be improved by employing AC-coupling at both outputs at the expence of bandwidth.

The analysis of the non-linearities shows that due to the distortion cancellation the input referred third-order intercept point is approximately the intrinsic IIP3 of the MOSFETs in the common-source stage plus 3 dB. But AC-coupling at the input makes the IIP3 dependent on two-tone spacing. An biasing point optimal for compression has been derived. It has been shown that in order to maintain balance under interference the odd-order nonlinearities of the common-gate and common-source stage must be equal.

Using this analysis a step-by-step implementation procedure has been made, which is used for an implementation in a 0.14 microm CMOS proces. Table 13.1 list the main figures found by simulation.

AC-coupling at the output generally gives better results for two reasons:

- The NMOS and PMOS are directly coupled, giving a better compensation of their second-order nonlinearity.
- The impedance levels on both sides of the coupling capacitor do not have to be equal as is the case for AC-coupling at the input.

15 Future work

This chapter discusses some ideas for improving the performance of the LNA and some subjects for further reasearch when incorperating it into a receiver front-end

15.1 On the LNA

The basic topology of the LNA using a complementary common-gate and common-source stage works well at mid-band. Away from the center the performance degrades. Eliminating the need for AC-coupling can potentially improve performance considerably, not only avoiding the disadvantages of each coupling point mentioned in the previous chapter, but also extending the mid-band performance over a much wider bandwidth.

The AC-coupling between the two stages could be removed by going to a more recent technology using an lower supply voltage. Because the front-end does not have any voltage amplification before interferers that fall outside the IF-band are removed, this does not have a direct impact on interference handling capabilities. Of course the input voltage will stay the same and this mandates some voltage headroom, but the output voltage due to the series resistance of the mixer switches will reduce quadratically for the same gate capacitance. Currently connecting the gates of the common source stage would give a overdrive of $\frac{1}{2}V_{DD} - V_{TH}$, which is too high to give good compression behavior and power consuming. With every new technology node the supply voltage is reduced more than the threshold [19, section 25.2.2] and a DC connection becomes viable.

More problematic is the AC-coupling required by the common-gate stage. One way of removing the coupling capacitors is adding a folded cascode stage, as shown in Fig. 15.1a. This however limits the maximum output current to the quiescent current of the current sources and thus does not allow class AB operation. The cascode transistors add little noise themselves, but since the current sources now have to supply the quiescent current for two stages their contribution is increased.

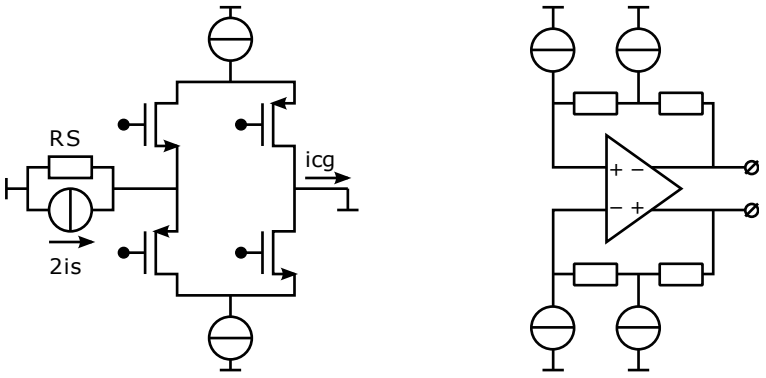
The improvement in linearity the proposed LNA gives over a non-complementary topology, as used in chapter 8, is due to the cancellation of the quadratic term in the MOSFET transfer function. This makes the proposed topology potentially sensitive to process spread and mismatch between components. The limitations this brings should be characterised.

15.2 On the front-end

Though not the primary point for research in this thesis, a lower noise figure and higher gain are always wanted. One way to improve noise performance is by impedance scaling the common-source stage which is the main noise contributor. This however requires a weighted addition of the output currents, which means the non-inverting and inverting output cannot connect to the same virtual ground node. One solution is shown in Fig. 15.1b, in which the weighted addition is performed by the resistors. If the currents are scaled $1 : n$ then the resistors are scaled $1 : (n-1)$ and the current sources on the right experiences a voltage swing of $\frac{n-1}{n}$ times the output voltage of the OTA. Since the current sources at the right represent the outputs of the mixer in series with the common-source output of the LNA, which has more voltage headroom than the common-gate stage, this may be acceptable.

Although it has been observed from simulations that the wideband second-order intermodulation product generated by the mixer is proportional to the imbalance of the LNA, its exact origin is not yet fully understood. A better understanding of it would allow for an optimization of the mixer for wideband applications.

An application where interference robustness of the LNA and mixer are paramount is beamforming at IF. Using a $N \times N$ Butler matrix [20], signals from N antennas can be combined to give N outputs, each corresponding to a spatial direction. This way a strong in-band interfer from a certain direction does not block reception from all other directions. Different from the passive Butler matrix (build with hybrid couplers and $\pi/8$ phase shifters), the active implementation at IF removes interferers only after down conversion.



(a) Common-gate stage with folded cascode (b) Two weighted-input TIA

Fig. 15.1: Circuit ideas for future work

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