

Mobility analysis in silicon for high-frequency surface acoustic wave applications

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18-03-2013

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Abstract

Preliminary work was done on the realization of acoustic charge transport devices in silicon. These devices utilize the inverse piezoelectric effect to induce surface acoustic waves (SAWs) using interlocking finger electrodes. SAWs are lattice deformations travelling across the surface of solids. In piezoelectric layers, these waves induce a piezoelectric field as well, modulating the band structure of the material. The moving band minima and maxima resulting from this can be used to transport charge carriers. For efficient charge transport, carrier velocity in the piezoelectric field should be higher than the SAW velocity. Thus, carrier mobility in the used substrate material should be sufficiently high to allow for this charge transport.

Mobility characterizations of high resistive Si wafers were performed investigating the viability of efficient acoustic charge transport. These characterizations were done using Hall bars and field effect transistors (FETs). Measurements on the Hall bars proved troublesome due to difficulties in applying a gate voltage using the used measurement setup. The results that were obtained were mobility values that were higher than values found in literatures by at least a factor of magnitude.

Measurements on FETs yielded more reliable results, measured FET-characteristics show expected behavior in general. Measurements were analyzed using an idealized FET model. Results lead us to believe that the high resistive Si wafers still have some background n-type doping. This is supported by multiple observations. First, n-type devices show relatively large leakage currents compared to p-type devices, especially for devices which have a high aspect ratio (long, narrow channels). Additionally, currents in n-type devices were found to be much higher in general, which can be attributed to the higher amount of charge carriers available.

Effective mobility values were found in the range of 400-600 cm²/Vs at 4 K and 250-300 cm²/Vs at 300 K for electrons. For holes effective mobility values of around 200-300 cm²/Vs at 4 K and around 100-150 cm²/Vs at 300 K were found.

Furthermore IDTs have been fabricated using nanoimprint lithography on Si using a novel fabrication method involving the application of an HSQ layer for etch selectivity and planarization. Utilizing this fabrication process, resonance frequencies up to 16 GHz were shown for devices made on a ZnO/SiO₂/Si substrate. Even more important, resonance frequencies of up to 23.5 GHz were shown for devices made in a CMOS compatible process on a SiO₂/ZnO/SiO₂/Si substrate. Both these measurement results are supported by theoretical calculations.

Further modeling has been done to determine electric field distribution in SAWs at the used frequencies and as a result, mobilities required for effective charge transport. The minimum required mobilities were found to be about the same order as the mobilities derived from FET measurements. As effective mobility values for acoustic charge transport devices are expected to be higher, they should allow for effective charge transport. .

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Chapter 1. Motivation

In signal processing, surface acoustic waves (SAWs) have been applied for several decades in devices such as filters¹ and oscillators². In these applications, SAWs are a way of transferring energy from a source to a receiver. In semiconductors, they can also be used to transport charges by changing the electronic structure of the material. This enables a wide range of interesting applications including spin transport³, acousto-optic modulation¹¹, photon detection/generation^{4,5}, single-charge pumping⁶ and applications within quantum information technology⁷.

So far, most of the charge transport experiments have been done on GaAs substrates, because of the piezoelectric nature of the GaAs, which is a major advantage in SAW generation. In addition, well-studied fabrication of quantum wells in this material, which limits electron motion to a single plane, allows better control over the particles. In industry, however, it would be more interesting to incorporate SAW-devices in widely used silicon technology. For example, recently, acoustic charge transport in Si has been achieved by Barros *et al.* in Ref. [8].

Applying SAW technology in devices on Si is far from straightforward. In the first place because it is more difficult to excite SAWs in Si, since it is not a piezoelectric material (this requires an additional piezoelectric layer). For applications that will be discussed here, there are additional important requirements on the substrate. In this thesis research is done to investigate whether carrier mobilities in Si are high enough to allow for acoustic charge transport. Additionally, Si has an indirect band gap in contrast to the direct band gap of GaAs. This means any experiments on the interaction between light and SAWs will yield significantly different results. In how far for instance optical generation of excitons is still possible will need to be investigated.

Finally, in most applications, it is beneficial to use higher-frequency devices to increase processing speeds. As $f=v/\lambda$, higher frequencies can be achieved in two different ways, either by reducing the wavelength (λ) of the generated SAWs, or by using a material in which the SAW-velocity (v) is higher. In the experiments done in this thesis so-called interdigital transducers (IDTs) are used to excite SAWs. These are sets of narrow interlocking fingers to which an RF signal is applied. By reducing the size of the fingers and the distances between them, the wavelength can be reduced. This will make the devices so small that optical lithography will not allow a sufficient resolution. Electron-beam lithography (EBL) could be used for the fabrication, but this method has the drawback of having a low throughput. Here, nanoimprint lithography (NIL) is used, allowing for relatively high throughput and excellent reproducibility, on top of this, the process for NIL is far less dependent on the substrate than an EBL-process.

Chapter 2. Theory

Surface Acoustic Waves

In bulk solids, mechanical energy can be carried by phonons, quasiparticles describing a propagating lattice deformation. These waves follow from solving Newton's equations of motion for atoms in a lattice⁹. They can either be transverse (atom motion perpendicular to wave propagation direction) or longitudinal (atom motion parallel to wave propagation direction). Additionally these can be optical phonons (in which neighboring atoms are displaced in opposite directions) or acoustic phonons (in which neighboring atoms are displaced in the same direction. For more information on bulk phonons see reference [9]. For a special case of acoustic phonons (acoustic waves) in which the wave travels along the surface, the wave equation has a different solution than in the bulk material because of the additional boundary conditions. Moreover, for piezoelectric crystals, piezoelectricity modifies the stress tensor and introduces new boundary conditions. In this case, the acoustic and piezoelectric fields decay along the normal direction of the surface and are restricted to a region very close to the surface (approx. one wavelength)¹⁴.

The wave equation for the acoustic field in a piezoelectric material is given by¹⁰:

$$\nabla \cdot \sigma = \rho \frac{\partial^2 \vec{u}}{\partial t^2} \quad (1)$$

Where σ is the stress tensor in the material, ρ is the density and u the displacement field in the material.

This equation can be solved numerically using the following relations¹⁰:

$$\sigma = c\varepsilon - e\vec{E} \quad (2)$$

$$\vec{D} = \epsilon\vec{E} + e\varepsilon \quad (3)$$

Where E and D are the piezoelectric field and the electrical displacement field respectively. Additionally, ε is the strain in the material, ϵ is the dielectric tensor, e is the piezoelectric tensor and c is the electrical stiffness tensor. The boundary conditions now require that the stress and the electrical displacement field have to be continuous over any interface present parallel to the surface in case of layered structures¹¹:

$$\sigma(z_{int}^+) = \sigma(z_{int}^-) \quad (4)$$

$$D(z_{int}^+) = D(z_{int}^-) \quad (5)$$

These solutions give rise to waves that can be present only at the surface of these materials, and hence are called surface acoustic waves (SAWs). The best known type of SAW is a wave in which all particles follow a circular motion around their equilibrium position. These waves, which behave like the ripples on the surface of water, are named Rayleigh waves, after Lord Rayleigh, who predicted them¹². An illustration¹³ of such a Rayleigh wave can be seen in Figure 1a. While in bulk waves energy is transported in all different directions, in Rayleigh waves all particle motion, and therefore all energy, is within a layer at the surface¹⁴. This layer has a thickness of approximately the wavelength of the SAW. Since SAWs only travel in a plane, their decay length is longer than in bulk waves, allowing them to transmit signals over greater distances. The displacement inside the material in both the z -direction and the x -direction is shown in Figure 1b.

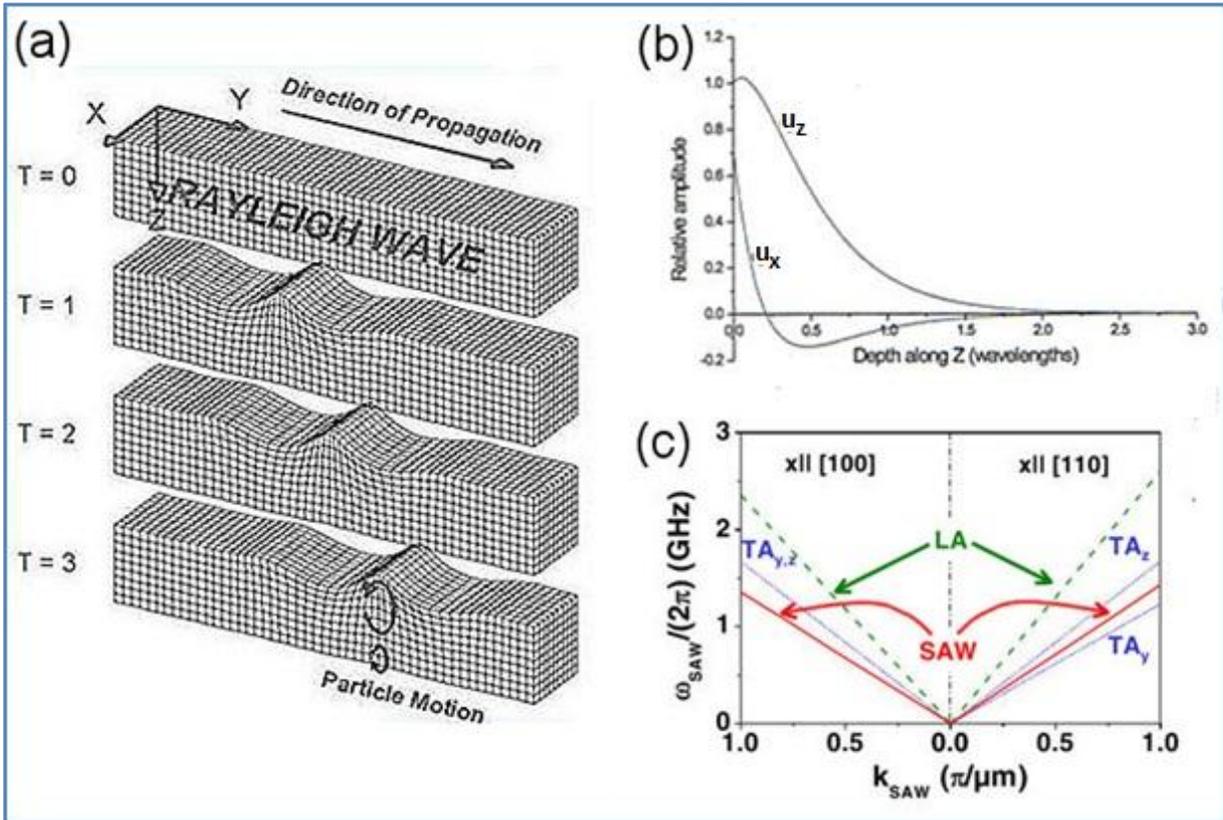


Figure 1.

(a) Illustration of a Rayleigh wave. A wave propagates in y -direction without any particles having a net velocity in that direction. As seen in the bottom picture individual particles make circular orbits around their equilibrium point, causing a wave to form at the surface. The amplitude of this circular particle motion is reduced rapidly down into the material. Additionally, deeper lying atoms make the circular motion in the opposite way. (Image taken from Ref. [13])

(b) Displacement amplitude as a function of the depth Z in the material. As can be seen, all atoms are displaced in a positive z -direction, meaning all atoms move up in the material. The fact that the line depicting the displacement in the x -direction has a zero crossing indicates the direction of motion reverses below a certain depth in the material. (Image taken from Ref. [14])

(c) Example of a dispersion relation in GaAs, the slope of the characteristics depends on substrate and wave direction in relation to the crystal planes. (Image taken from Ref. [11])

The velocity of a SAW is generally lower than the velocity of bulk acoustic waves, but still in the same order of magnitude, meaning the speed is in the order of several kilometers per second. An example of a dispersion relation for a SAW (in GaAs) can be seen in Figure 1c.

The linear relation between wavenumber k and angular frequency ω that can be seen is given by the relation:

$$\omega = v_p k \quad (6)$$

In equation (6), v_p is the phase velocity of the SAW, which is a parameter that depends on the materials used. This means that for a given sample the frequency of SAWs can be increased by increasing the wavenumber, so decreasing the wavelength.

Excitation of SAWs can be done by an electrical method which uses pairs of interlocking electrode structures, known as interdigital transducers (IDTs)¹⁵. Shown schematically in Figure 2a. When these IDTs are deposited on the surface of a piezoelectric material, a time varying electric potential difference between the two electrodes will lead to an electric field in this material. Since it is piezoelectric, it will respond by a mechanical deformation because of the inverse piezoelectric effect.

In Figure 2 additionally the aperture and the wavelength of the IDTs is depicted, these will correspond to the width and the wavelength of the excited SAW respectively.

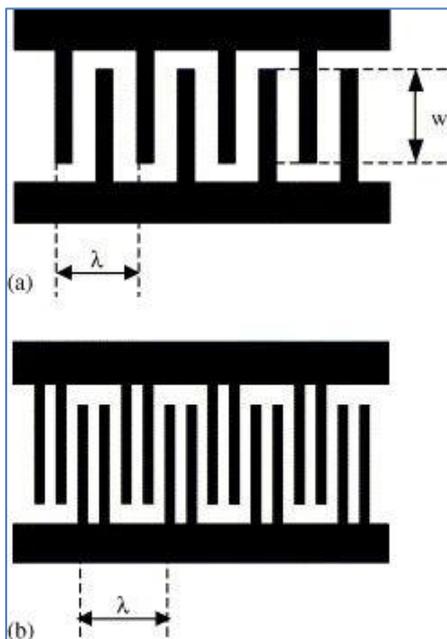


Figure 2. Schematic view of a single fingered IDT (a) and a double fingered IDT (b). The finger period λ will also be the wavelength of the SAW excited by these IDTs. Additionally the aperture w is shown, which will be approximately the width of the SAW generated. (Image taken from Ref. [15])

A SAW will now be generated when the frequency of the signal applied to an IDT with a period λ obeys the equality

$$f = \frac{v_p}{\lambda} \quad (7)$$

At this (resonance) frequency a SAW propagating in the direction perpendicular to the fingers will be generated. One can also use another IDT as a receiver to detect this acoustic wave.

Since the SAWs cause a mechanical deformation, in a piezoelectric material they will lead to an alternating electric field which causes a potential difference between the fingers of the detector IDT. This potential difference has the same frequency as the SAW excited by the input signal. To reduce internal reflections from IDTs, double-fingered IDTs can be made, having no surface metal at the point where the amplitude is greatest. An example can be seen in Figure 2b.

Additionally, SAWs can be generated at higher frequencies corresponding to higher harmonics of the resonance frequency¹⁶. For instance, for SAWs with a wavelength of a third of the finger period, displacement maxima will still coincide with one of the two electrodes, and all minima with the other but there will be maxima and minima in between. An illustration can be seen in Figure 3.

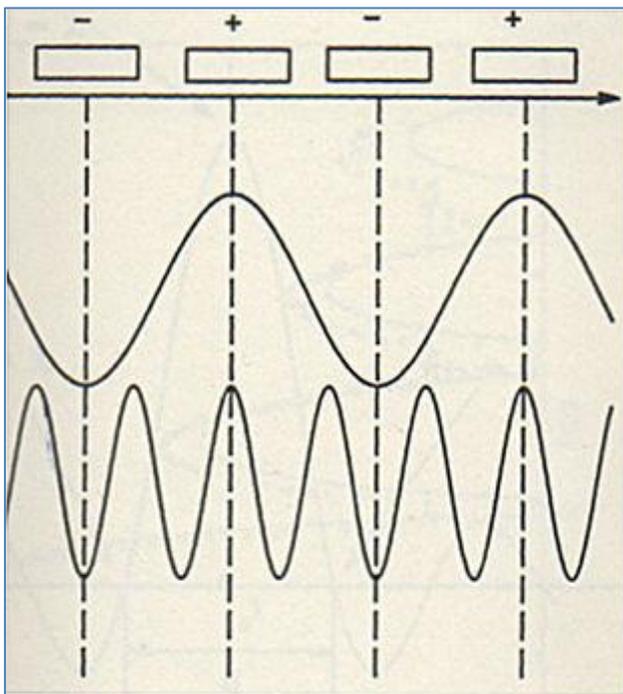


Figure 3. Illustration of the generation of higher order harmonics. In the top part a side-view of the IDT fingers can be seen with the base harmonic below it. At the bottom the third harmonic can be seen, which has maxima and minima corresponding to the same IDT fingers and will thus also be generated by this IDT, if driven at this mode's resonance frequency. (Image taken from Ref. [16])

When multiple layers are present near the surface of a material (within approximately one SAW wavelength), different SAW modes can be also induced because of the difference in acoustic velocity of different layer materials. These modes correspond to acoustic waves that show displacement profiles that have one or more nodes in the direction perpendicular to the surface. The contribution of these higher modes depends on the ratio between wavelength and layer thicknesses.

Although the use of SAWs described so far is already interesting enough to have its own set of applications, such as signal filtering¹, sensing¹⁷, etc., a lot more can be done using SAWs. Most exciting applications of SAWs use piezoelectric potential accompanying to the mechanical deformation.

In a semiconductor material, where conduction and valence bands are split by a band gap, piezoelectric potential wave will cause a periodic modulation of these bands and causes minima and maxima in conduction and valence bands, respectively. Electrons (holes) will reside in the minima (maxima) of conduction (valence) band. This is shown schematically Figure 4. As the periodic modulation is both spatial and temporal, electrons and holes will be transported through the material at the SAW velocity.

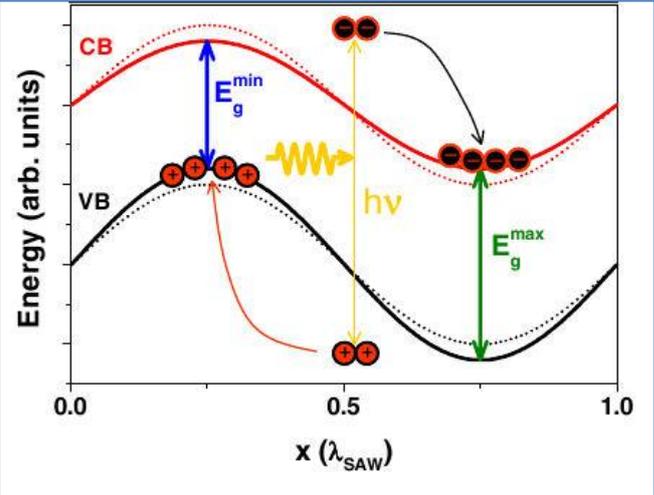


Figure 4. Schematic illustration of SAW induced periodic modulation of the band energy diagram in piezoelectric semiconductor. Electrons and holes (in this example excited optically) can be transported at the SAW velocity in the minima and maxima of the conduction band and valence band, respectively. (Image taken from Ref. [11])

A requirement for efficient transport (meaning the transport of charge carriers in a single wave minimum/maximum) is that the drift velocity of the electrons gained from the piezoelectric field should be at least equal to the SAW velocity⁸. Otherwise the electrons will be delayed, so much that they will not remain in a single SAW minimum and ‘lag behind’. Since the drift velocity is equal to the mobility times the electric field, this places the following constraint on the system:

$$\mu \vec{E}_{max} > v_{SAW} \quad (8)$$

Now taking $\vec{E} = -\nabla U$ with $U = U_0 \sin\left(\frac{2\pi x}{\lambda_{SAW}}\right)$ (where U is the potential, and U_0 the amplitude of the potential wave) gives

$$\mu \frac{2\pi}{\lambda_{SAW}} U_0 \left(\cos\left(\frac{2\pi x}{\lambda_{SAW}}\right) \right)_{max} > v_{SAW} \quad (9)$$

Since the maximum value of the expression on the left is for $\cos\left(\frac{2\pi x}{\lambda_{SAW}}\right) = 1$ this places requirements on the attained amplitude of the potential wave (which can be influenced to some degree by careful tuning of layer thicknesses based on simulation results, as will be discussed later). This requirement is:

$$U_0 > \frac{v_{SAW} \lambda_{SAW}}{2\pi \mu} \quad (10)$$

In designing the devices, this requirement should be taken into account.

Coupling between a moving potential wave and semiconductor bands may be achieved by using a piezoelectric semiconductor as substrate material (often GaAs, a III-V semiconductor, is used). In non-piezoelectric semiconductors it can also be generated by depositing a thin piezoelectric film on top of the semiconductor. In this way, periodic band modulation can also be achieved in silicon, which is not piezoelectric by itself. We will use different layer stacks to achieve this coupling in silicon, using ZnO as the piezoelectric material.

When electrons carried in a SAW minimum move across a potential barrier and a lateral confinement (for instance in the form of a quantum point contact) is present, the amount of electrons in the minimum can be adjusted by increasing this potential barrier (making the side-gate contacts more negative). One by one electrons are pushed out of the potential minimum by the applied potential barrier because of Coulomb repulsion. Potentially this can be done up until single electrons are transported with each SAW cycle.

A proof that electron-hole pairs can be transported in GaAs using SAWs has been given by Rocke *et al.* in Ref. [18]. Their results are shown in Figure 5. Here a photoluminescence spectrum is shown, made by illuminating a certain part of the GaAs sample with a pulsed laser and recording the spectrum returned by recombination of the excitons. When a SAW is driven at increasing acoustic power, one observes a drastic decrease in photoluminescence, indicating the excitons are not able to recombine due to the SAW. This can be explained by the spatial separation of electrons and holes in the potential minima and maxima of the conduction band and valence band. In Figure 5b, it is shown that these excitons can even be transported and allowed to recombine at another point, by making a metal contact which screens the SAW potential. Here recombination can occur and is in fact observed, proving the possibility of trapping, transporting and recombining excitons using a SAW.

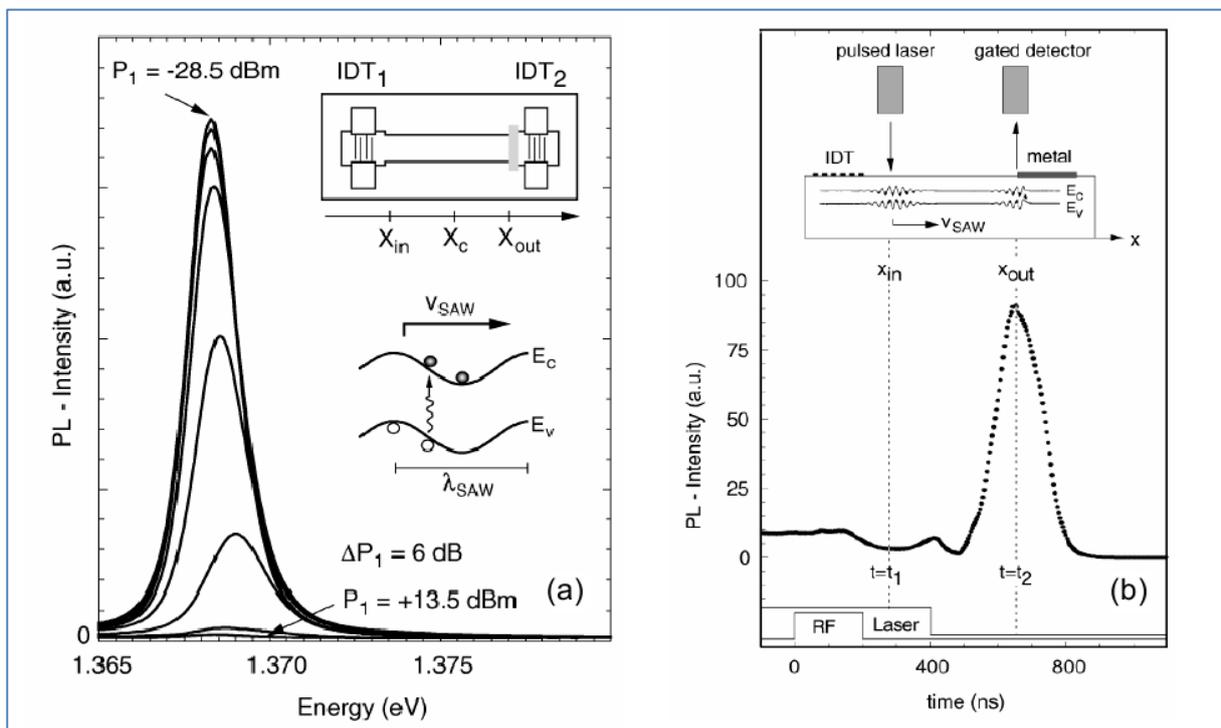


Figure 5. Results on the transport of electron-hole pairs using SAWs. In (a) a photoluminescence spectrum from GaAs sample is shown. At increasing SAW power, electron-hole pairs are split more strongly at the point the laser illuminates the sample. This means the amount of recombination is greatly reduced. In (b) the SAW is driven to a metal contact, which allows electron-hole pairs to recombine freely. After illuminating the sample at x_{in} , a time t later luminescence is shown; corresponding to the time the SAW needs to reach the metal contact. (Image taken from Ref. [18])

Another interesting experiment has been done by Shilton *et al.* in Ref. [19]. An illustration of the experiment is given in Figure 6 (a) and (b). A SAW is driven towards a quantum point contact (QPC) defined by two side-gate electrodes. Because a potential barrier exists in this channel, the moving SAW potential is modulated through the QPC. At the entrance region of QPC, some electrons are pushed out of the SAW potential because of Coulomb repulsion. Modifying the gate voltage will change the number of electrons that can be driven every SAW cycle. In this way, an integer multiple of electrons will be transported every cycle. The total current will then be $ne*f$, where f is the SAW frequency and n is an integer number. In this way a current standard can be defined by defining the Ampere as (a multiple of) the size of the current steps observed for charge transport using a SAW with a defined frequency.

Measurement results are shown in Figure 6 (c) and (d). Here the current is shown as a function of the voltage applied to the side-gates. This current shows distinct steps with a height of ef . This indicates gate voltages where an integer number of electrons are transported every cycle. In Figure 6d, the transconductance is plotted as a function of the gate voltage, here the quantization of the current is even clearer than in (c).

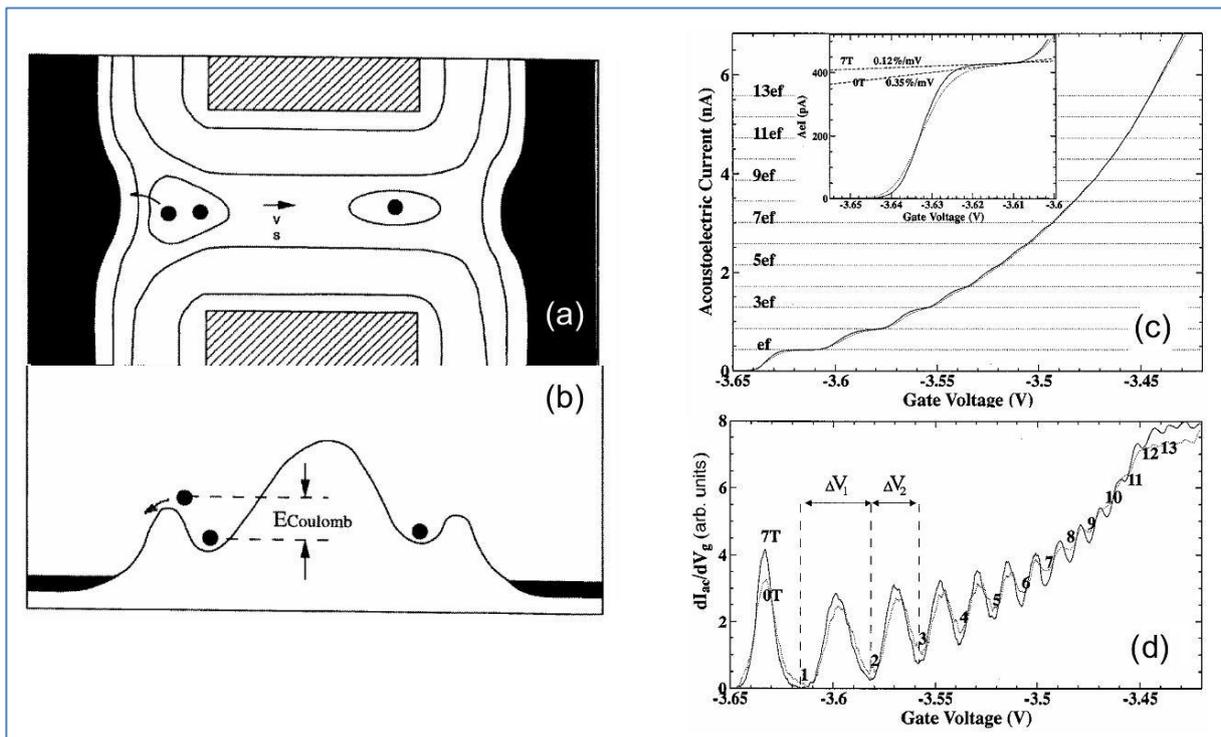


Figure 6. Results on single-electron transport through quantum point contacts. In (a) the active region is shown from above, showing side-gates at the top and bottom. In (b) a 'side-view' of the potential across the constriction can be seen, a SAW passes from left to right and carries electrons in its conduction band minima. If the gate voltage is negative enough, electrons are pushed out of the minima and only a limited number is carried per cycle. In (c) a current measurement can be seen depending on gate voltage, showing distinct steps. In (d) the transconductance dI/dV_g is plotted as a function of the gate voltage, showing distinct minima and maxima. (Image taken from Ref. [19])

Mobility measurements

Mobility values of the used silicon wafers are relevant for these experiments, since they determine the amplitude the electric wave should be able to attain (together with SAW frequency and wavelength). Therefore, mobility values for the used Si wafers should be measured. This can be done by means of for instance Hall bar measurements or MOSFET characteristics. The difficulty here is that it is difficult to obtain mobility values for intrinsic silicon, since its conductance is very low (due to the very low amount of charge carriers present). These carriers can be induced by applying a gate voltage, but in the final application in SAW-devices, electrons are only induced in gated regions, but then drawn to non-gated regions. However, gating will only decrease electron mobility because of electron-electron interactions, so these measurements will still give a lower bound for the mobility.

The method for deriving mobility from Hall bar measurements is based on the principle illustrated in Figure 7. A current is sent through a sample, and in a direction perpendicular to this current a voltage is measured, in the absence of a magnetic field this voltage is ideally zero. When applying an out-of-plane magnetic field however, charge carriers are deflected in the lateral direction because of the Lorentz force. When the system is given time to equilibrate (with this fixed current), a lateral electric field will be induced which counteracts the Lorentz force. As the Lorentz force depends on the velocity of the carriers, so does the lateral electric field. This velocity, in turn, depends on the mobility of carriers in the material. The full derivation on how to extract mobility from a Hall measurement is based on Ref. [20].

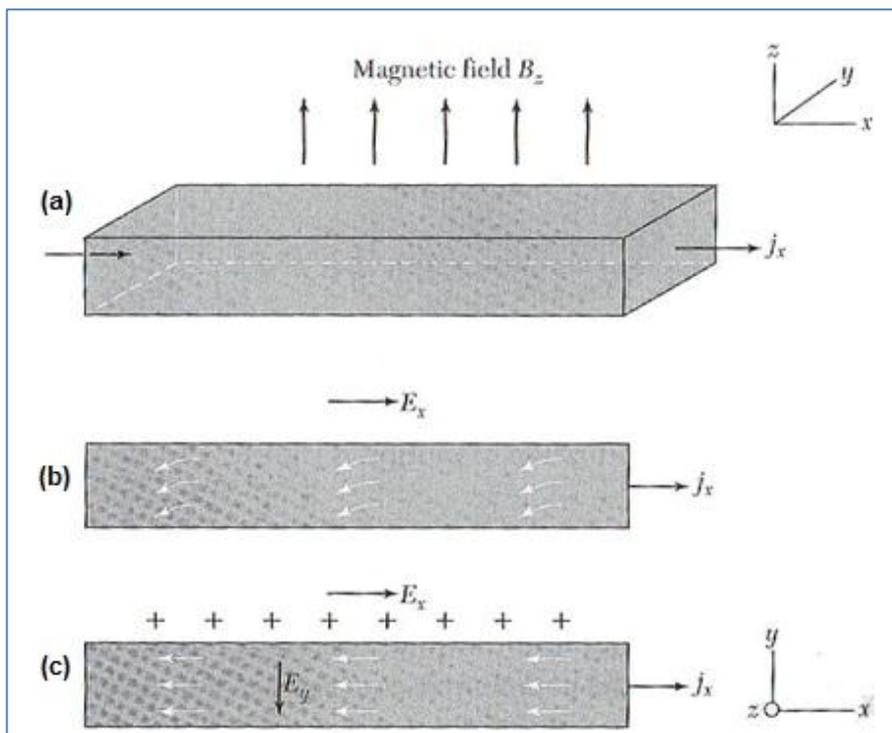


Figure 7. Schematic overview of the Hall bar measurements. (a) A bar is placed in a magnetic field, and a current passes through. (b) When just starting up, electrons with a velocity v (opposite to current due to their negative charge) experience a Lorentz-force $F_B = -e(v \times B)$ and, once in equilibrium (c), an opposite force $F_E = -eE$ due to surface charges on the bar. These surface charges generate an electric field, and can be measured as a potential perpendicular to the current direction and the magnetic field. (Image taken from Ref. [20])

When looking at Figure 7 (c), in an equilibrium condition, since the electric and magnetic (Lorentz) forces on the charges should cancel, no net current will flow in y-direction. (In every measurement only one type of charge carrier is present), this equilibrium condition means that:

$$F_y = e(E_y - v_x B_z) = 0 \quad (11)$$

Where E is the electric field, v the velocity and B the magnetic field, and the subscripts denote only components in the corresponding direction. Now the current density in x-direction j_x is given by $j_x = -n_e e v_x$ (for electrons). Inserting this in (11) and rewriting gives:

$$E_y + \frac{j_x}{ne} B_z = 0 \quad (12)$$

Now rearranging the terms gives:

$$\frac{E_y}{j_x B_z} = \frac{-1}{ne} \quad (13)$$

Now entering $E_y = U_y/W$ and $j_x = I_x/(W*d)$ gives

$$R_H = \frac{U_y}{I_x B_z} = \frac{-1}{d * ne} \quad (14)$$

Where R_H is defined as the Hall coefficient. Here d is the thickness of the conducting layer. Now the value of U_y/I_x is measured directly on the PPMS as a function of the magnetic field, so this term can be extracted.

Additionally we know the resistivity ρ is given by $\rho = -1/ne\mu$ for electrons and the sheet resistance R_s by $R_s = \rho/d$ with d again the thickness of the conducting layer. This means:

$$R_s = \frac{-1}{d * ne\mu} \quad (15)$$

And also:

$$R_s = \frac{\rho}{d} = \frac{R_l A}{Ld} = R_l \left(\frac{W}{L} \right) \quad (16)$$

Here R_l , W and L are the longitudinal resistance, width and length of the Hall bar, respectively. This means R_s can be easily determined by measuring the longitudinal resistance for a known geometry.

Now when comparing equations (14) and (15) the mobility can be extracted by means of:

$$\mu = \frac{R_H}{R_s} \quad (17)$$

This means the mobility can be derived when a measurement is done of the transverse resistance as a function of the magnetic field and the longitudinal resistance.

The method for deriving mobility from MOSFET characteristics²¹ is based on the fact that the current through the source-drain electrodes I_{SD} of a MOSFET is given by $I_{SD} = Nev$. Here N is the number of electrons, e is the electron charge and v is the electron velocity. Since the electron charge is known, the velocity (depending on the applied source-drain voltage) can be derived when the number of charge carriers is known.

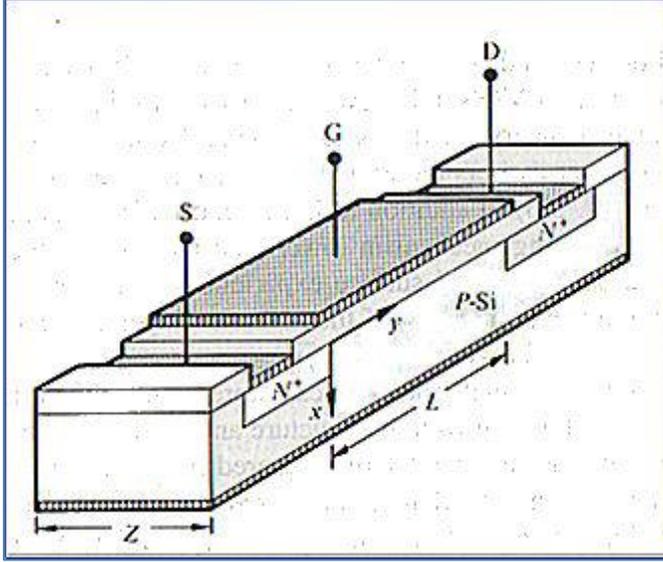


Figure 8. FET geometry used for deriving mobility values. S, D and G denote source, drain and gate electrodes, respectively. x is defined as the depth into the material and y as the distance along the induced channel. The source is connected to ground and different bias voltages are applied to the gate and drain for FET operation (positive voltages for n-type devices, negative voltages for p-type). (Image taken from Ref. [21])

Using the geometry shown in Figure 8, in which the source is grounded and bias voltages are applied to the drain and gate. Now the total source-drain current density (\vec{J}_{SD}) as a function of the applied electric field between source drain contacts (\vec{E}_{SD}) is:

$$\vec{J}_{SD} = \sigma \vec{E}_{SD} \quad (18)$$

Where the conductivity σ can be expressed as $n*q*\mu$, where n is the number of charge carriers per unit volume, q is the charge and μ is the mobility. Inserting this gives:

$$\vec{J}_{SD} = nq\mu\vec{E}_{SD} \quad (19)$$

Now the current is obtained by integrating over the area the current density flows through:

$$\vec{I}_{SD} = \iint \vec{J}_{SD} dx dz = \iint nq\mu\vec{E}_{SD} dx dz \quad (20)$$

Now, since all these terms are constant for every position z the integral over dz can be replaced by a multiplication with the width Z , additionally the charge per carrier q and the electric field E can be taken out of the integral over x , since they are independent of the position x :

$$\vec{I}_{SD} = Z\vec{E}_{SD} \left(q \int n\mu dx \right) \quad (21)$$

The term in the brackets now gives the effective MOSFET mobility $\bar{\mu}$ times the charge per unit area Q_A ²¹. Now integration over y gives (taking into account that l is independent of y):

$$\vec{I}_{SD}L = Z\bar{\mu} \int_0^L Q_A\vec{E}_{SD} dy \quad (22)$$

E is now given by $d\varphi/dy$ (with $\varphi(y)$ the local potential at any point y along the channel), Thus (further taking the source as grounded and drain potential as V_D).

$$\vec{I}_{SD} = \frac{Z\bar{\mu}}{L} \int_0^{V_D} Q_A d\varphi \quad (23)$$

The induced charge per unit area Q_A (as a function of $\varphi(y)$) can now be approximated using the model for a parallel plate capacitor, when the gate voltage exceeds a threshold voltage, needed for inversion to occur (the exact derivation can be found in [21]). The potential difference obtained is then $(V_G - V_T) - \varphi$, resulting in an accumulated charge per unit area of:

$$Q_A = C_A(V_G - V_T - \varphi) \quad (24)$$

With C_A the capacitance per unit area, given by $C_A = \epsilon_r \epsilon_0 / d$, with ϵ_r the relative dielectric constant of SiO_2 , ϵ_0 the permittivity of vacuum and d the SiO_2 dielectric layer thickness.

Combining equations (23) and (24) yields:

$$\vec{I}_{SD} = \frac{Z\bar{\mu}C_A}{L} \int_0^{V_D} (V_G - V_T - \varphi) d\varphi \quad (25)$$

Finally completing the integration yields:

$$\vec{I}_{SD} = \frac{Z\bar{\mu}C_A}{L} \left[(V_G - V_T)V_D - \frac{V_D^2}{2} \right] \quad (26)$$

With the restrictions that are $V_G - V_T > 0$ and $V_D < V_{SAT}$, indicating that the transistor is operation below its saturation voltage, which is the source-drain voltage for which the current reaches its maximum (for a given gate voltage). Additional approximations have been made in the geometry of the device. Effects occurring at the side of the device have not been taken into account; the device is basically seen as being infinitely wide. Therefore most accurate results will be obtained from wide (large Z) devices. On top of that, for higher drain voltages the depletion region will increase in width, meaning the effective length over which electrons see a potential drop (from the source to the point where pinch-off occurs) becomes smaller. This will lead to a decrease in the observed resistivity, increasing the current, meaning the saturation of the I - V characteristic will still show an increase in current for increasing drain voltage²¹.

Equation (26) will be used for deriving the mobility in two different ways. The first of these is by examining the transistor behavior when $V_D \ll V_G - V_T$. At this point the term including V_D^2 becomes so small it can be neglected, rewriting eq (26) now gives:

$$\bar{\mu} = \frac{\vec{I}_{SD}}{V_D} \left(\frac{L}{Z} \right) \frac{1}{C_A(V_G - V_T)} \quad (27)$$

In this way, by computing the slope of the I - V characteristic for different gate voltages V_G the mobility can be calculated.

A second way utilizes the point where pinch-off of the channel starts, the so-called saturation voltage $V_{D,SAT}$. When the drain voltage reaches this voltage the current will stop increasing.

As derived in [21], $V_{D,SAT}=V_G-V_T$. Inserting this in eq. (26) gives:

$$\begin{aligned}\vec{I}_{SD,SAT} &= \frac{Z\bar{\mu}C_A}{L} \left[(V_G - V_T)^2 - \frac{(V_G - V_T)^2}{2} \right] \\ &= \frac{Z\bar{\mu}C_A}{L} \left[\frac{(V_G - V_T)^2}{2} \right]\end{aligned}\quad (28)$$

Now, by measuring the current at its saturation value for varying gate voltages one can derive the effective mobility.

One point has to be made about this mobility. Since MOSFET structures operate in the extreme vicinity of the surface, the mobility derived from these calculations will not yield the exact values for bulk mobility in Si. The values found will be lower because of two reasons. The first of these reasons is that due to the applied gate voltage the electrons will be drawn to the surface and will scatter at the surface. Adding another scattering mechanism will decrease the effective mobility. The second mechanism is the increased amount of electrons present at the surface. This will lead to an increased amount of electron-electron interaction, also causing the effective mobility to be lower.

Still, the derived mobilities will give a useful indication of the (minimum) mobility in bulk silicon.

Chapter 3. Fabrication

Hall bars and FETs

For mobility measurements first Hall bars were fabricated on the high resistive ($>10\text{k}\Omega$) Si wafers that will be used for the charge transport experiments. Since these Hall bars did not give any useful results due to a design flaw (which will be discussed later), an optimized design was made. This new design was fabricated on the same type of wafers. Thirdly, also FET devices were made on these wafers as a second way to determine mobility values. The measurements from these (also discussed later) yielded some good results; however, for devices with p-type doping no reliable measurements could be done. Therefore, an additional run was done with adapted parameters for p-type doping.

In the remainder of this thesis, the three different runs are indicated as R1 through R3. The Hall bars made during the first process are indicated by R1-HB, the Hall bars and FETs in the second process as R2-HB and R2-FET respectively, and the improved p-type FETs made during the third process as R3-FET.

An overview of the process used for the R1-HB can be seen in Figure 9.

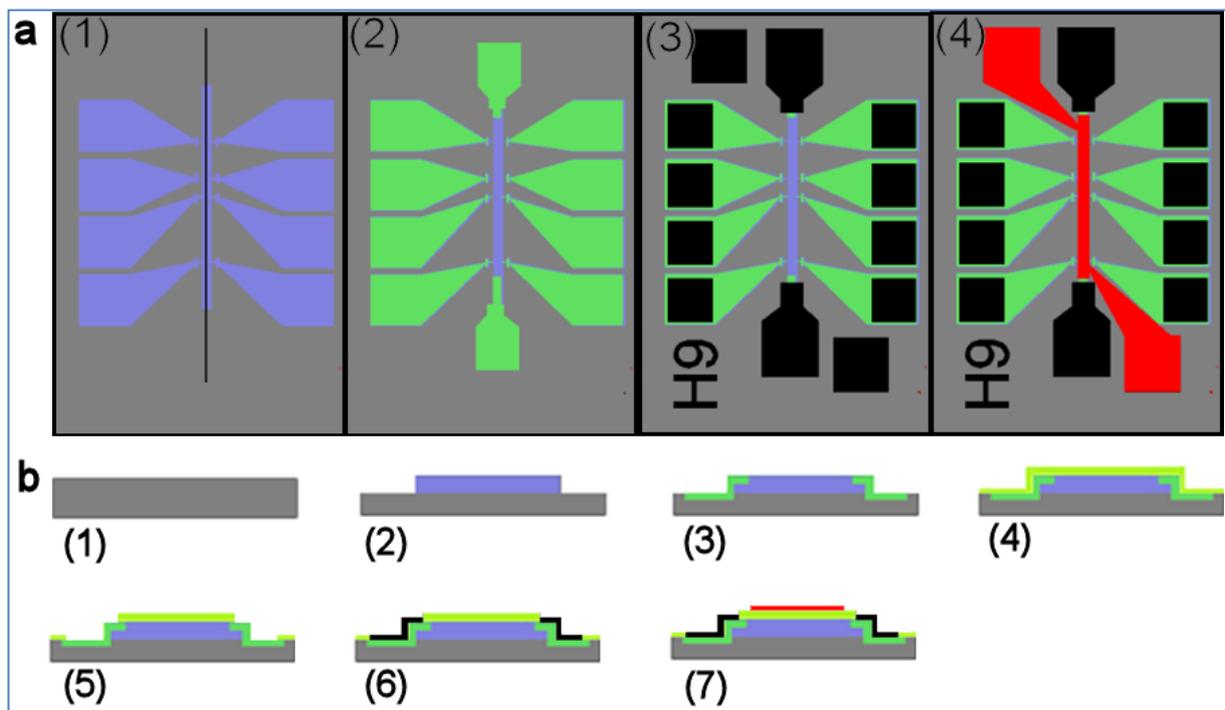


Figure 9. Fabrication scheme of the R1-HB devices, with (a) top view and (b) cross-section along the line indicated in a1. First, a mesa was etched into the Si (a1, b2). Then phosphorus-ions were implanted (a2, b3) and a gate oxide was grown (b4) (left out in (a) for clarity). Etching opens this oxide in the contact regions (b5) and subsequently performing a lift-off results in the contacts seen in a3 (and b6). Finally a metal gate is defined by a lift-off. (a4, b7)

In this process (R1) first a mesa was defined on the silicon, to do this a thermal oxide was grown on the Si which was about 50 nm thick, it was grown at 950°C for 30 minutes in an ultra-clean furnace (All oxides grown in this project were grown by dry oxidation). A pattern was defined on top of this using optical lithography (OL), resulting in photoresist covering the mesa. This process is done using Olin 907-17 photoresist. The photoresist was applied by spin-coating at 4000rpm for 30 seconds and then baked at 90°C. After exposing for 4 s in UV-light at 12 mW/cm² in an EVG620 mask-aligner a 60 second post-exposure bake at 120°C was done. Developing was then for 1 minute, followed by a 15 minute dehydration bake at 120°C. (All OL-processes described in this thesis have been done using this recipe, except when lift-off was performed or where mentioned otherwise)

After a BHF (Buffered Hydrogen Fluoride) etch was done for 30 seconds, removing the oxide layer. Following BHF etching and removing residual photoresist, Si etching (outside the SiO₂ region) was done in 25% TMAH (Tetramethyl Ammonium Hydroxide) at 75°C for 30 seconds. Then, the remaining SiO₂ was removed in BHF from the entire wafer. This resulted in a 260 nm thick mesa (verified using a profilometer) on the Si surface.

Subsequently, an n-type doping step was done using Phosphorus ions at a dose of $5 \times 10^{15} \text{ cm}^{-2}$ using an acceleration voltage of 50 kV. The pattern for this was defined again using optical lithography. Doping is needed in areas where current needs to be injected or drawn from the substrate. These areas are indicated in Figure 9 (b2) and correspond to the regions along the Hall bar where longitudinal and transverse voltages will be measured. Stripping the photoresist left after this implantation step proved tedious, as neither acetone nor nitric acid could strip this layer. Even an ozone-steam treatment could not remove this photoresist. It was found out that due to the implantation the photoresist was hardened and could only be removed by prolonged oxygen plasma treatment (periods of 2 hours or more). To activate the doping, a short RTA (rapid thermal annealing) step was done, in which a temperature of 900°C was reached for 1 min. This is done to restore the bonds between the Si and the doping ions that have been damaged during implantation.

Afterwards, a gate oxide was grown of around 30nm thick, using the same thermal furnace process as used previously, with the exception that the duration was reduced from 30 to 15 minutes. The resulting oxide layer was patterned using first an OL-process and subsequently a BHF etch, opening up the regions where contact to the Si substrate is needed, shown in Figure 9 (a3). In retrospect, there is an error here, as the contacts used for contacting the gate electrode were also etched into the oxide layer (top-left and bottom-right contact).

The optical lithography process used here was different, since after this a lift-off needs to be done, requiring undercut sidewalls, for reasons shown in Figure 10. To do this TI-35 photoresist is used, which a mask pattern is applied using an illumination for 23 seconds under a 12 mW/cm² UV lamp. After a stabilization period of 10 minutes an image reversal bake is done for 2 minutes at 120°C, rendering the exposed areas insoluble in the developer used. After this a flood exposure is done for 1 minute, illuminating the full wafer. Now the parts that have not been exposed in the first step are dissolved using photoresist developer. Now the remaining photoresist has the undercut profile required for lift-off. Afterwards a 50 nm Al layer was evaporated onto the wafer (using a 10nm thick Cr adhesion layer) in a Balzers BAK600 e-beam evaporation tool. Only the electrodes were left after the remaining photoresist was dissolved in acetone. Using an identical lift-off process (except for the oxide etch), finally the gate electrodes were grown.

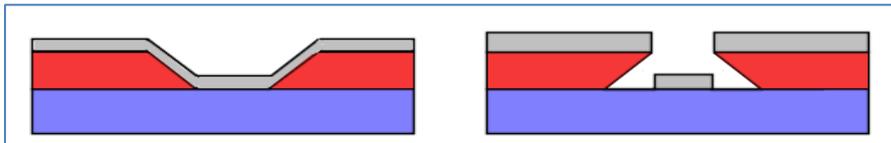


Figure 10. The importance of undercut sidewalls in lift-off. In the left picture, with overcut sidewalls, a closed metal layer (grey) is formed, and no solvent reaches the photoresist (red), meaning all metal will remain. In the right picture the photoresist can be dissolved, and only the metal on the substrate (blue) will remain.

The process used for R2 and R3 are identical to each other, with the exception of the p-type implantation parameters being different. The process used for R2/R3 differs from the one used for R1 in some places. The first difference between R1 and R2/R3 is the absence of a mesa structure. Since this mesa would not confine the electrons in a direction perpendicular to the surface, it does not provide any advantage. Additionally, in R2 and R3, high resistive Si wafers were first covered with a 164 nm thick layer of thermal SiO₂, grown in an ultra-clean furnace at 1100°C over a period of 135 minutes. The purpose of this layer is to protect the bare Si surface from unwanted contaminants and uncontrolled oxidation. Parts of this insulating layer will be removed in the process steps where contact needs to be made to the Si substrate. Thickness measurements using ellipsometry gave an oxide thickness of 164 nm.

Subsequently, ion-implantations have been done using Boron-doping for p-type regions and Phosphorus for n-type regions. Implantation has been carried out in regions defined again by OL, through the 164 nm oxide layer. Simulations showed that implanting through this oxide layer yields the same doping concentration in the Si near the surface as without the oxide layer. Implanting was done at 100keV with a dose of $5e^{14}$ cm⁻² (in R2) and $5e^{15}$ cm⁻² for p-type regions and $5e^{15}$ cm⁻² for n-type regions. A thermal annealing step was not used, since the next process step was an oxidation step in which already a temperature up to 900°C was reached. A thickness of 10.01 nm was verified using ellipsometry.

Then a high quality thin gate oxide was grown on the active gate regions. For this, first the protective oxide is removed at these places, after which an oxidation is done. Growth time for this oxide layer was 10 minutes at 900°C. Previously the furnace had been cleaned using a 4 hour cleaning process. Thickness of this oxide layer was measured by ellipsometry as well and found to be 10 nm varying only very little between the wafers..

Finally, in a fashion similar to the one used in R1, two lift-off steps were performed; one for the contact metal, and one for the gate metal. Again for the contact metal the oxide layer was opened up first, and for the gate metal this was not done. A difference between this process (R2/R3) and R1 was that here, for the contacts, the first 120 nm aluminum layer was grown using sputtering instead of evaporation, to improve the ohmic contact quality between the substrate and the contacts. Sputtering was sputtered in an Oxford PL400 Ar film sputtering tool. To improve ohmic contact quality, additionally the wafers were thermally under N₂ gas for 10 minutes at 450°C.

For the gate oxide sputtering was not done, as sputtering could cause damage to the high quality oxide layer. For this gate first 15 nm Ti was evaporated, followed by 65 nm of Pt using a Balzers BAK600 e-beam evaporation tool. An overview of these steps can be seen in Figure 12.

The FETs have been made in different sizes. The definition of these sizes is shown in the close-up in Figure 11. The width Z is given by the gate width and the length by the distance between the implanted regions, marked as L . Devices were made with lengths and widths varying from 5 to 50 μm .

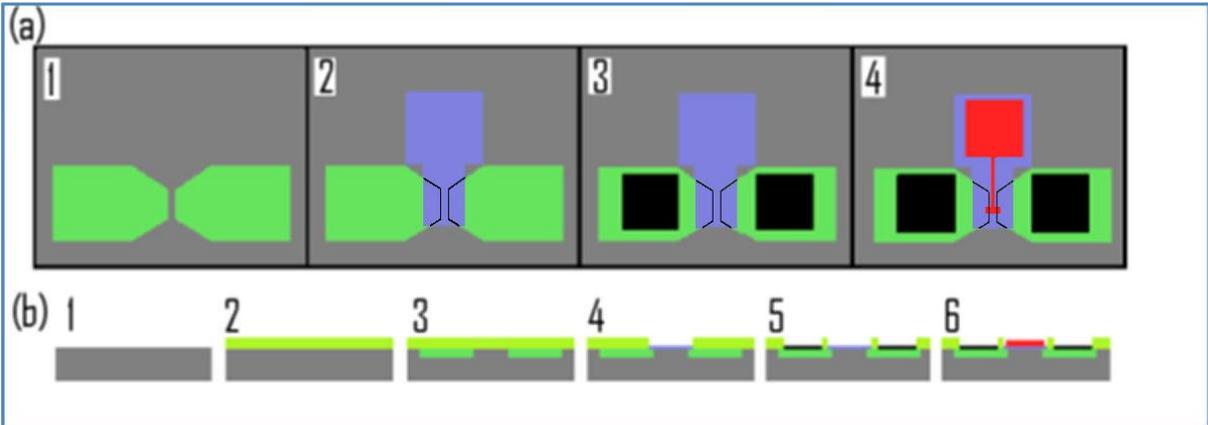


Figure 12. Overview of the FET devices made in R2 and R3. First a protective oxide layer is grown (b2), (this layer is not shown in (a) for clarity). Through this layer n-type and p-type ion implantation is done (a1, b3) (indicated by the black line in (a2 to a4) where the gate oxide is on top). Then a hole is etched in the protective oxide and a high quality gate oxide is grown (a2, b4) after which first the lead contacts (a3, b5) and then the gate (a4, b6) is grown.

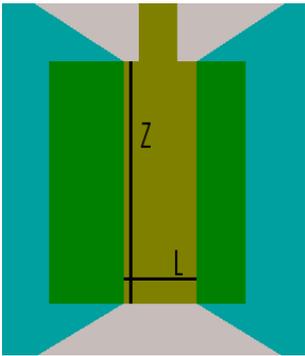


Figure 11. Close up of the FET active region showing the definition of the size of the FET. The length L is given by the distance between the implanted regions, and the width Z by the width of the gate.

SAW devices

For the SAW-devices, multiple processes have been done. In the first case²³, a 230 nm thick ZnO layer was deposited on top of a 100 nm SiO₂ layer grown on top of a DSP Si-001 wafer. The SiO₂-layer in between was used to increase the electromechanical coupling between the substrate and the ZnO layer. The ZnO was grown using a sputtering technique in which the sample was rotated for getting a uniform thickness across the 4" wafer. In Figure 13 an XRD-measurement can be seen, showing the ZnO layer is grown mainly in the 002-direction. Since ZnO has the highest piezoelectric activity in 002-direction, strong peak intensity is essential to generate SAWs. From the full width at half maximum (FWHM) value the minimal average grain size can be calculated using the Sherrer formula²², this gives grain sizes of approximately 15nm²³.

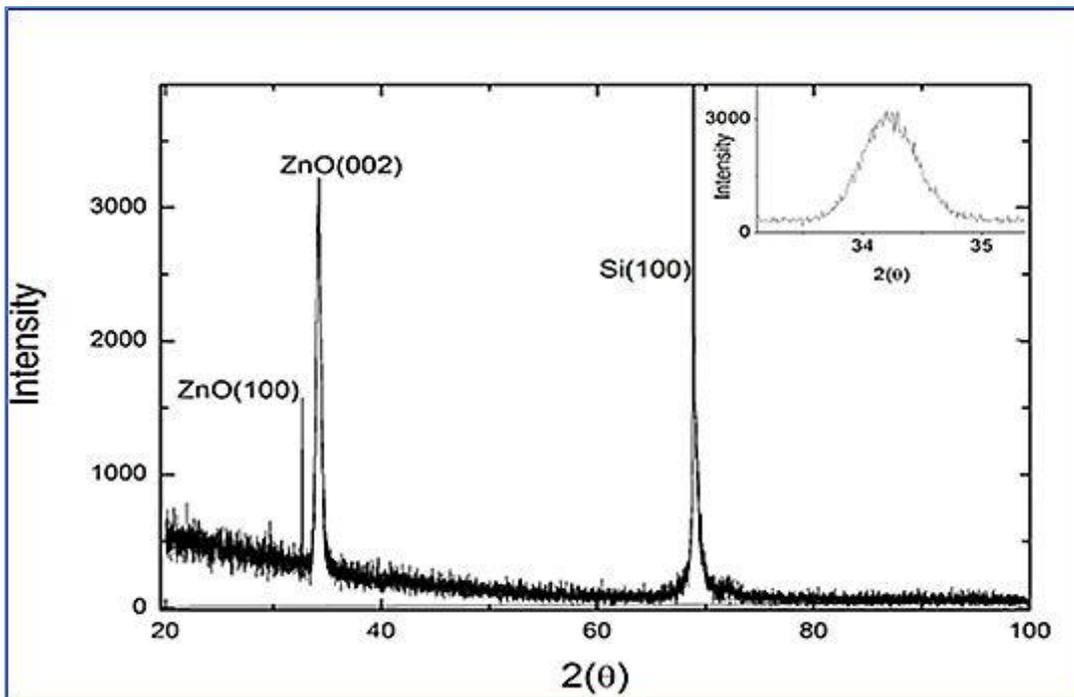


Figure 13. XRD measurements on the ZnO-coated samples show preferential growth in the piezoelectric 002-direction (perpendicular to the surface). From the FWHM of the peak (inset), the minimal average size of crystallites can be deduced. (Image taken from Ref. [23])

On top of this ZnO layer IDTs were fabricated using nanoimprint lithography (NIL). The templates (one for single-finger designs and one for double-finger designs), made by IMS Chips has structures to fabricate IDTs with finger widths (and inter-finger distances) of 65, 80, 100 and 125nm. The NIL-production process had already been optimized²⁴. An overview of this process is given in Figure 14. NIL is used as it provides several advantages over other methods. Conventional optical lithography would limit operation frequencies to a few GHz²⁵. E-beam lithography does offer the possibility of getting high frequencies²⁶, but does not have the same throughput as NIL, additionally it is far more substrate-sensitive.

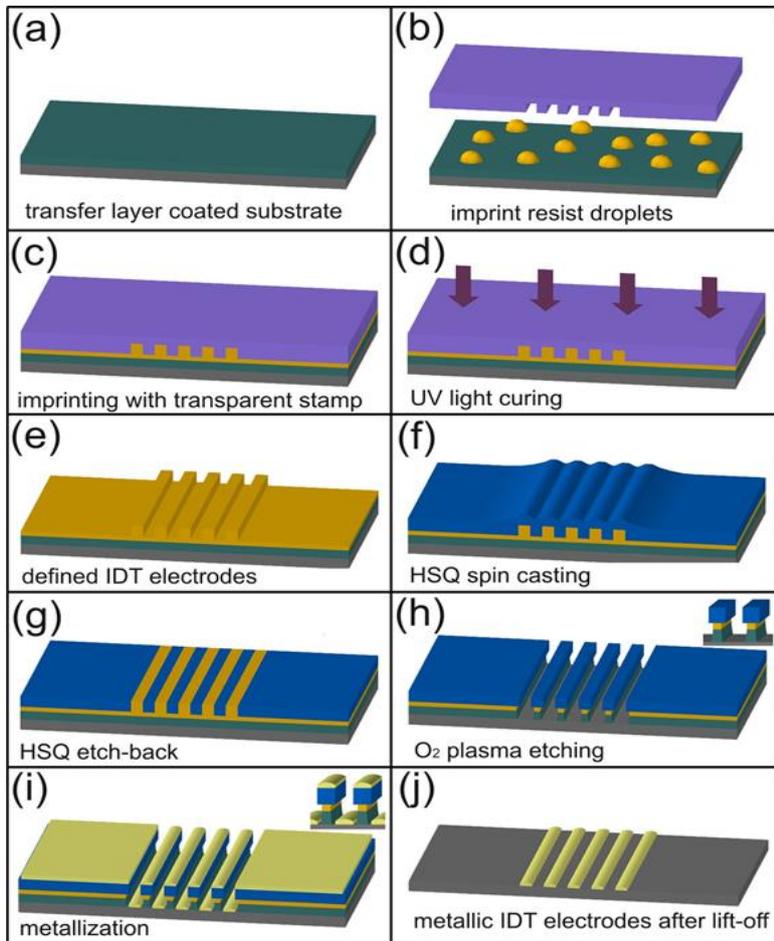


Figure 14. Process overview of the fabrication of IDTs using NIL. First imprint material is applied (b). Then it is imprinted using a stamp and cured with UV light (c+d). Subsequently HSQ is spin-cast (f). When an HSQ etch-back is now done in CHF_3 plasma and then an O_2 plasma etch is done (g+h) the sample has a nice undercut profile, allowing for lift-off of the gold IDTs (i+j). (Image taken from Ref. [23])

Before any patterning is done a PMMA transfer layer of about 80 nm thick is spin-coated (at 3000 rpm) and baked at 120°C for 2min. This layer is used to get an adequate undercut profile later in the process. Additionally, its solubility in acetone allows for an easy lift-off.

On top of this PMMA transfer layer a low-viscosity imprint liquid (Monomat (by Molecular Imprints)) was dispensed in a controlled way. The patterned template was then pressed into this imprint liquid with a force of 2-3 N using an Imprio™ 55 tool from Molecular Imprints, and then cured using UV-light with a wavelength between 230-360 nm at an exposure dose of $80 \text{ mJ}/\text{cm}^2$. This causes the liquid to harden, leaving a negative image of the template in the imprint liquid. This allows for the very exact replication of the structures in the template.

After this, an HSQ layer of about 160 nm thick was spin-coated on top of these imprinted structures, planarizing this surface. Subsequently, an etch-back was done in a CHF_3 -plasma, etching the HSQ planarization layer until the imprinted structures are exposed again. Due to a good etch selectivity between HSQ and imprint material/PMMA in oxygen plasma, an O_2 -plasma etch will etch into these features. Both CHF_3 and O_2 plasma etching were done using an Adixen AMS100DE plasma etching apparatus. This etching not only opens the surface, but even leaves a nice undercut profile, allowing for a good lift-off process to be performed. On top of this profile a 25 nm thick gold layer was deposited (using a 2-3 nm Cr adhesion layer) using a Balzers BAK600 e-beam evaporation tool. Because of the solubility of PMMA in acetone, lift-off was done by simply putting the sample in acetone and using an ultrasonic sound treatment.

In the imprint-template, the contact electrodes for the IDTs were defined by a grating, since a completely filled structure would cause a long-range thickness-variation in the HSQ planarization layer. This thickness variation would lead to equal thicknesses of HSQ above the contact regions and the open regions. This would cause some unintentional openings around the device during O₂ plasma etching leading unwanted metalized areas.

An alternative process has been used to fabricate ultrahigh-frequency SAW devices by using a different transfer layer. In this alternative way the ZnO layer was covered by an additional SiO₂ layer²⁷. Since ZnO is etched in photoresist developer it would be better if it is not present at the surface. Process started with thermal growth of a 105 nm thick SiO₂ layer on a DSP Si-001 wafer. On top of this a 40 nm or 80 nm (for single-finger and double-finger designs respectively) layer of ZnO was sputtered. ZnO layer was covered by a sputtered 20 nm thick SiO₂ layer which still allows a piezo-electric coupling between the IDTs and the ZnO layer.

The surface was then spin coated with a WiDE-C 80 (Brewer Science) layer of 80 nm thick, acting as a transfer layer for which PMMA was used in the previous process. IDT definition on this layer was done using the same process as described above. The only difference was the IDTs were defined in Al instead of gold. Lift-off was performed in 96 % HNO₃.

Chapter 4. Results

Hall bars

The result of the first Hall bar production process (R1) is shown in Figure 15. As said before, the fact that the gate electrodes (indicated by an arrow) are directly on top of the silicon substrate renders these devices unusable.

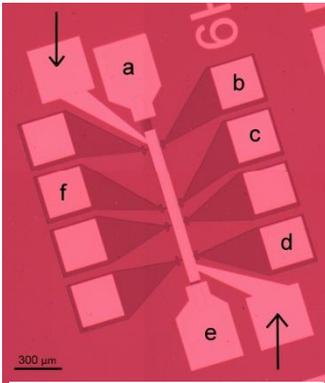


Figure 15. Image showing a Hallbar structure from the first run that was made. The contacts indicated by the arrows are directly on top of the Si substrate and thus cause erroneous measurements. Implanted regions are darker than the intrinsic Si and thus can be seen.

This was only found out after measurements had been done, of which the results can be seen in Figure 17, Figure 16 and Figure 18. These measurements were performed on a Physical Properties Measurement System (PPMS), capable of cooling the sample to 1.9 K and applying magnetic fields of up to 10 T. All these measurements were done on a single device. The dependence of the longitudinal and transverse resistance (R_L and R_T) on the magnetic field is shown. A current of 5 μA was applied by the PPMS between contacts labeled (a) and (e) in Figure 15. Longitudinal voltage was then measured between the contacts (b) and (d) and transverse voltage between the electrodes (c) and (f). By dividing this voltage by the applied current longitudinal and transverse resistance were calculated. This way of deriving the longitudinal resistance means the square resistance is equal to the $R_L/13$, as the distance between (b) and (d) is 650 μm and the width of the bar 50 μm .

In Figure 17, results are shown for measurements in which no gate voltage was applied to the gate electrode. It can be seen that the longitudinal voltage always shows quadratic behavior resembling Lorentz magnetoresistance. At 300 K, the transverse voltage shows linear behavior as expected. At 50 K and 100 K, however, this transverse resistance shows a dependence on the magnetic field remarkably like the longitudinal resistance. This might be explained by the fact that some small longitudinal component is measured as well. At 35 K, surprisingly, the transverse resistance becomes somewhat linear again, it is unclear why. At low temperatures (<80 K) however, the resistance increases very rapidly, as can be seen in Figure 16, in which the dependence of the longitudinal resistance on the temperature is shown. This rapid increase can be explained by the fact that electrons are “frozen” in the valence band.

Without applying a gate voltage however, there is no way of being sure the current flows through the Hall bar instead of through the surrounding silicon or the metal contacts. Therefore the measurement shown in Figure 18 was done. Here gate voltages were applied in addition to the measurement without a gate voltage. The PPMS had no suitable interface to apply a gate voltage; therefore a gate had to be connected externally. A Keithley 2400 Source/Measurement unit (SMU) was used for this. It can be seen that once a gate voltage is applied, noise levels increase significantly (in these results some data points were removed that were so far off that no other results would be visible). Yet only in the measurement at 100 K a real change in behavior is observed, where the transverse resistance becomes more linear when a gate voltage is applied. In the measurement at 10 K, the results are shown, but no useful data could be derived from this because of the resistance that was too high to measure accurately by the PPMS.

Additionally, in all measurements in which a gate voltage was applied, it was found that the gate current applied by the Keithley SMU was higher than the current applied by the PPMS. Because of this it was observed that the gate electrode was directly on the substrate and because of this no useful measurement could be done because current will run through the gate electrode instead of through the Hall bar itself.

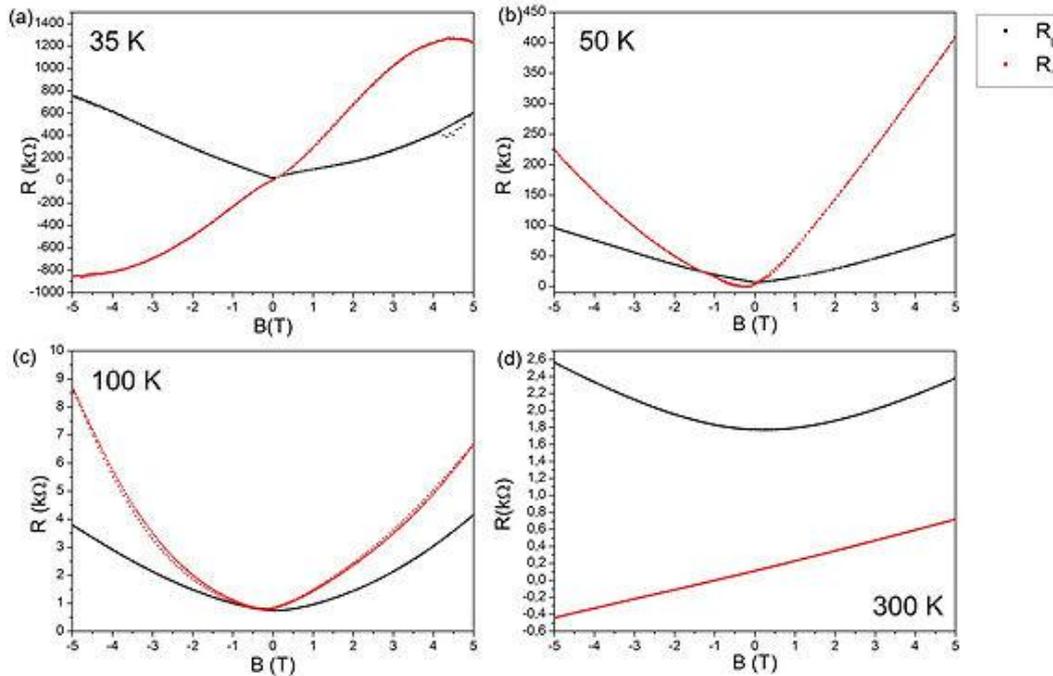


Figure 17. Graphs showing the longitudinal resistance and transverse resistance as a function of the applied magnetic field B at 35 K (a), 50 K (b), 100 K (c) and 300 K (d).

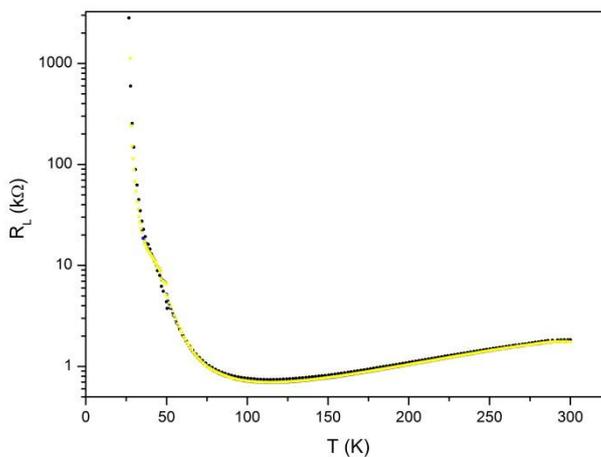


Figure 16. Figure showing dependence of the longitudinal resistance on temperature. This data was taken from 3 different measurements under the same circumstances. A large increase at low temperatures is seen due to the “freezing” of electrons in the valence band.

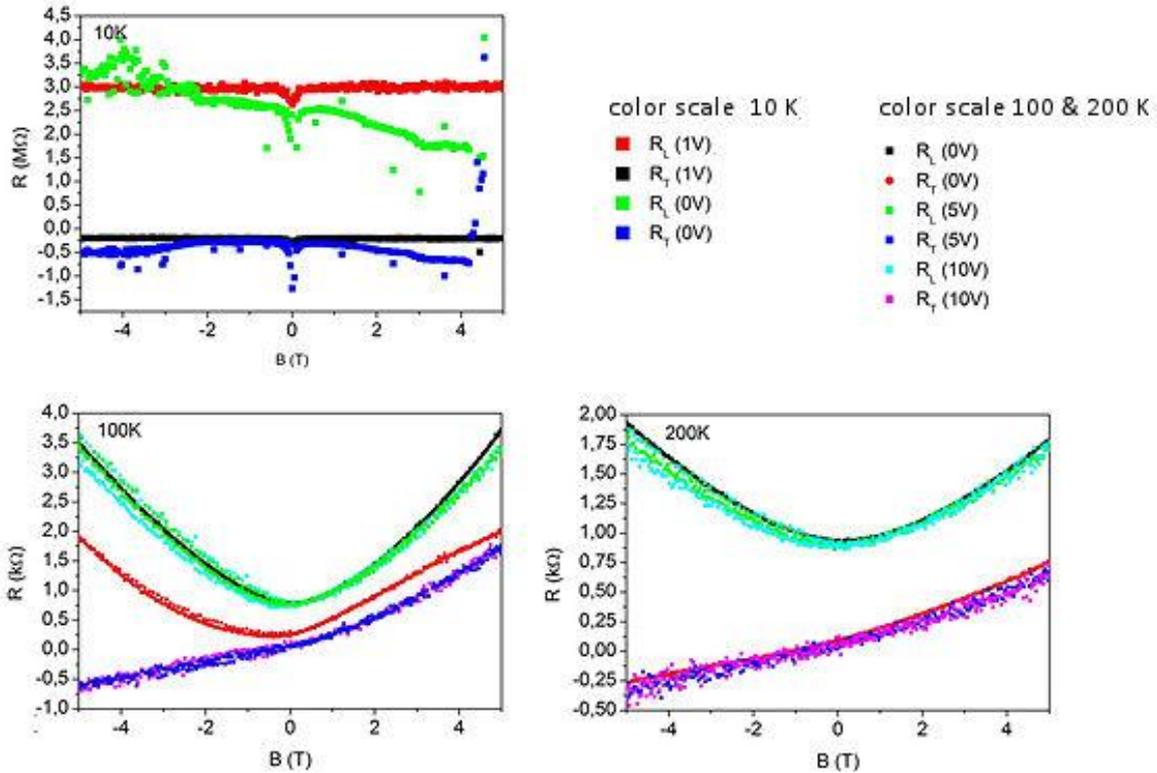


Figure 18. Figure showing longitudinal and transverse resistance at temperatures of 10 K (a), 100 K (b) and 200 K (c) for gate voltages of 0 V, 5 V and 10 V for 100 K and 200 K, and 0 V and 1 V at 10 K. At 10 K, no data was observed which showed anything recognizable, even when deviant data points due to noise were removed. At 100 K it can be seen that without a gate voltage, the transverse resistance shows behavior like the longitudinal resistance, which changes due to application of a gate voltage. At 200 K applying a gate voltage did not yield different behavior. In all cases, applying a gate voltage would increase noise levels significantly. In (b) and (c), measurement points that were far off have been removed, as these were so far off they could not be shown on the same scale.

From the measurements shown in Figure 17 and Figure 18 mobilities were calculated, shown in Table 2 for the non-gated Hall bars and Table 1 for gated Hall bars. These mobilities were calculated fitting the positive side of the transverse voltage in Figure 17 and Figure 18. The slope of this characteristic is the Hall resistance R_H . Dividing this by the square resistance at zero magnetic field yields these mobilities. Because of the fact that changing the gate voltage did not change behavior as shown in Figure 18, only for a gate voltage of 5 V, these values were calculated.

The fact that these mobilities are several orders of magnitude higher than known values of $1500 \text{ cm}^2/\text{Vs}$ at room temperature²⁸. further support the claim that these measurements are not reliable. The fact that these are that much higher is most likely due to the fact that current can run in more places than just the Hall bar and because of the current through the gate electrode, a much higher current is measured, yielding a higher mobility value.

T(K)	μ (cm^2/Vs)
35	2.05e6
50	1.65e6
100	1.55e5
200	8.40e3

Table 2. Table showing mobility values derived from non-gated Hall bars at different temperatures

T(K)	μ (cm^2/Vs)
100	64e3
200	14e3

Table 1. Table showing mobility values derived from Hall bars with an applied gate voltage of 5V at different temperatures.

In the run R2, the errors made in R1 have been dealt with in the new mask design. The resulting structures can be seen in Figure 19. Another difference is that in the process for the second wafer the gate thickness was reduced from 30 nm to 10 nm. Because for these devices the gate contact was not directly on top of the silicon, gate voltages could be applied.

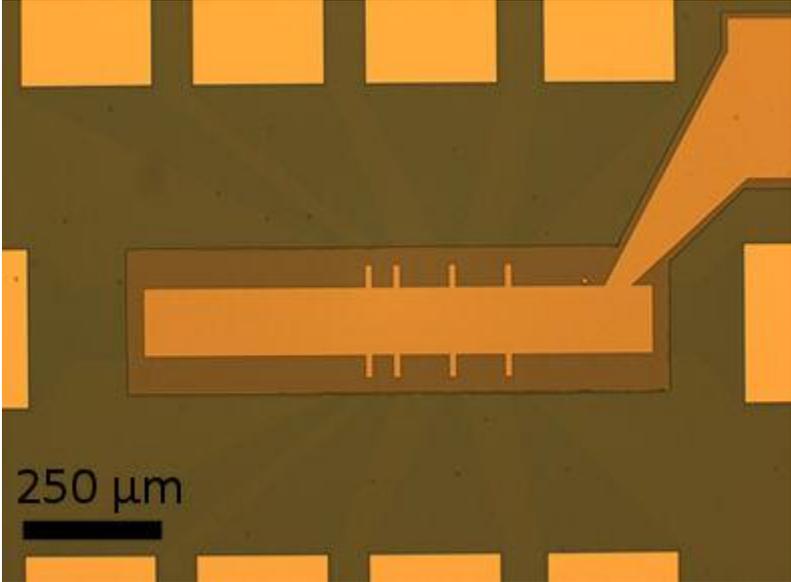


Figure 19. Results of the fabrication of the 2nd run of Hall bars, here no longer a mesa is used, causing the implanted region not to be as visible anymore, though they can still be seen. Also the oxide layer below the gate can be seen, which should insulate the gate from the substrate.

Resulting measurements can be seen in Figure 20 for an applied gate voltage of 1 V. As is clear, still a longitudinal magnetoresistance effect is observed as would be expected. In this case the Hall resistance shows a more linear behavior than in the previous run, though still being far from straight. Additionally, at higher temperatures longitudinal resistance is significantly higher than the transverse resistance, as would be expected (note the axis break in (d)). From these measurements, again mobilities were calculated, the results from these calculations shown in Table 3. Table showing mobility values

Table 3. Despite showing characteristics appearing more reliable, still these values show mobilities far higher than known values²⁸. Additionally still a gate (leakage) current was measured that was far higher than the current applied to the source-drain channel and significant noise levels were measured when applying a gate. (in Figure 20 the erroneous data points were removed).

T (K)	μ (cm ² /Vs)
4	4.8e5
100	7.3e4
200	1.4e4
300	5.1e3

Table 3. Table showing mobility values derived from the second run of Hall bars (R2) at different temperatures with an applied gate voltage of 1 V.

These unexpected measurement results were most likely caused by the difficulty in applying a gate voltage and the large current that would run in the gate. The PPMS is not suitable for applying a gate voltage in this way. It was decided to abandon trying to determine the mobility by Hall bars in favor of doing so by FET analysis.

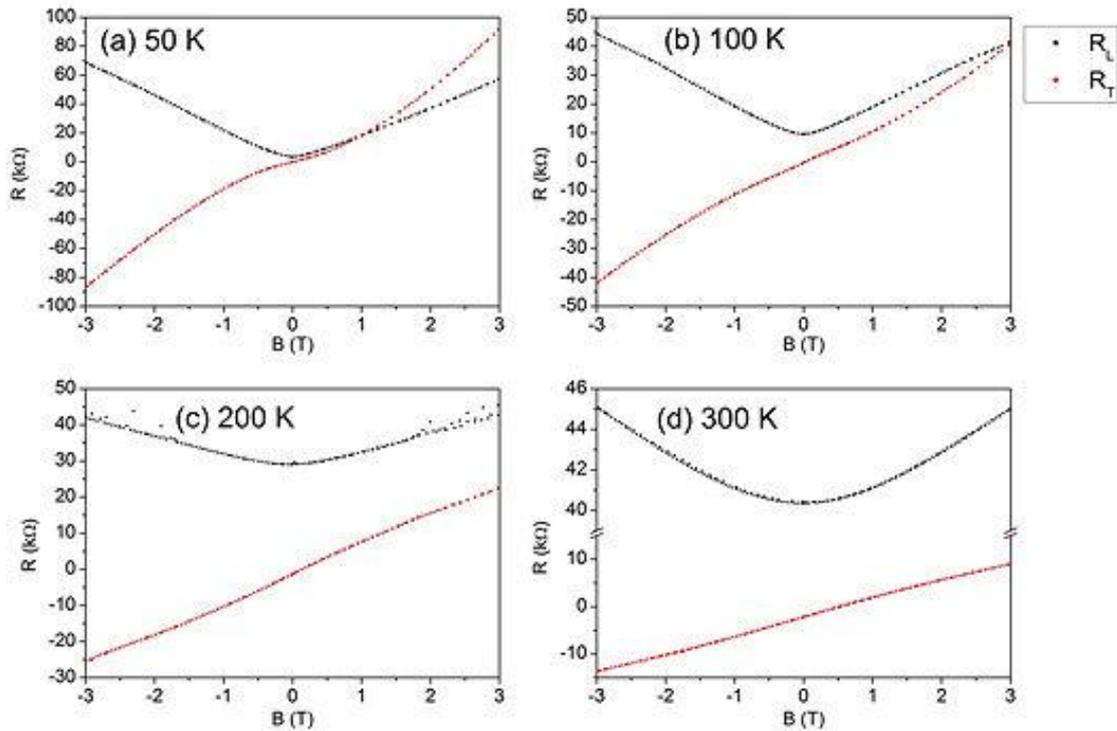


Figure 20. Figure showing longitudinal (black) and transverse (red) resistance at temperatures of 50 K (a), 100 K (b), 200 K (c) and 300 K (d). Measurements were done for a gate voltage of 1 V, noisy measurement points were removed. Even though the linear behavior of the transverse resistance and the quadratic behavior of the longitudinal resistance match expectations, the mobilities derived (shown in Table 3) still are far higher than expected.

FETs

Since the Hall bars did not give reliable results, new mobility tests were done using field-effect transistors (FETs). In these simple FETs, the source-drain current depends on the mobility of the electrons. The design for these devices was made by F. Müller. These FETs were made in R2 and R3 processes, as discussed previously.

Results from the FET fabrication can be seen in Figure 21. In this figure the source and drain contacts can be seen on the sides of a device with a gate contacts from the top in between. As can be seen in the close-up on the right, along the edges of the oxide layer some metal remained at some places. This metal will however, not be harmful to the measurements, since it neither connects the gate electrode nor the source and drain contacts. Additionally, it is not over the implanted region; therefore, it will not work as an “extra” gate either.

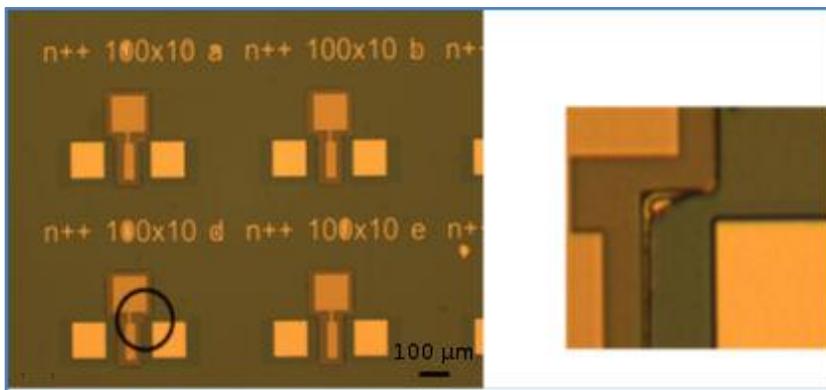


Figure 21. Optical microscopy images of the fabricated FETs showing n-type devices with a gate width of 100 μm and a length of 10 μm. Structure definition is good, but the lift-off process can be optimized further, as can be seen by the presence of remaining metal in the edges of the oxide layer.

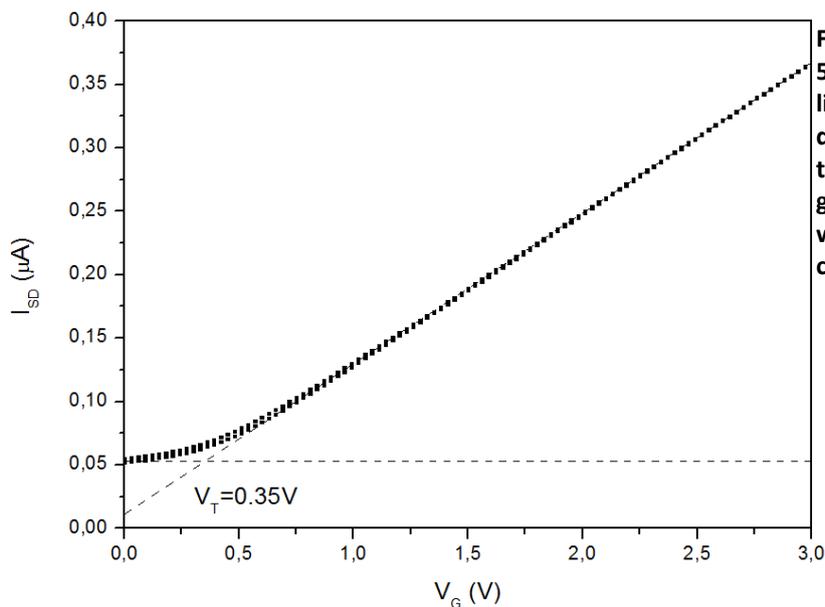


Figure 22. Gate sweep done for a 5x50 μm channel FET. By fitting a line to the linear part and determining the crossing point with the value of the current for 0 V gate voltage the threshold voltage was determined to be 0.35 V for a constant $V_{S-D}=10$ mV

To calculate the mobilities, first measurements were done using a double Keithley 2400 SMU. One of the SMUs was used for applying a source-drain voltage and subsequently measuring the source-drain current and the other one for applying a gate voltage. Measurements were done in a low-temperature probe-station, capable of cooling down to the boiling point of helium, 4.2 K. As can be seen in Figure 21, device dimensions are shown next to the devices as well. This means measurements could be done for different dimensions, for which different results were expected as well.

In the first run of transistors (from R2), measurements were done on n-type doped devices. First gate sweeps were done to determine the threshold voltage. An example is shown in Figure 22, here at 300 K a constant source-drain voltage of 10 mV was applied in a device with a channel width of 5 μm and length of 50 μm . The zero-gate-voltage level for this applied source-drain voltage is about 53 nA. When a line is drawn through the linear part of this graph, this 53 nA is crossed at a value of $V_G=0.35$ V. This is the threshold value used in the calculations of the mobility. For different temperatures, every time this gate sweep was also done, since at lower temperatures, higher gate voltages are needed to generate an inversion layer.

The results from the source-drain sweeps can be seen in Figure 23. Measurements were done only in the linear regime. Here it can be seen that at different gate voltages the source-drain I - V characteristic has a different slope.

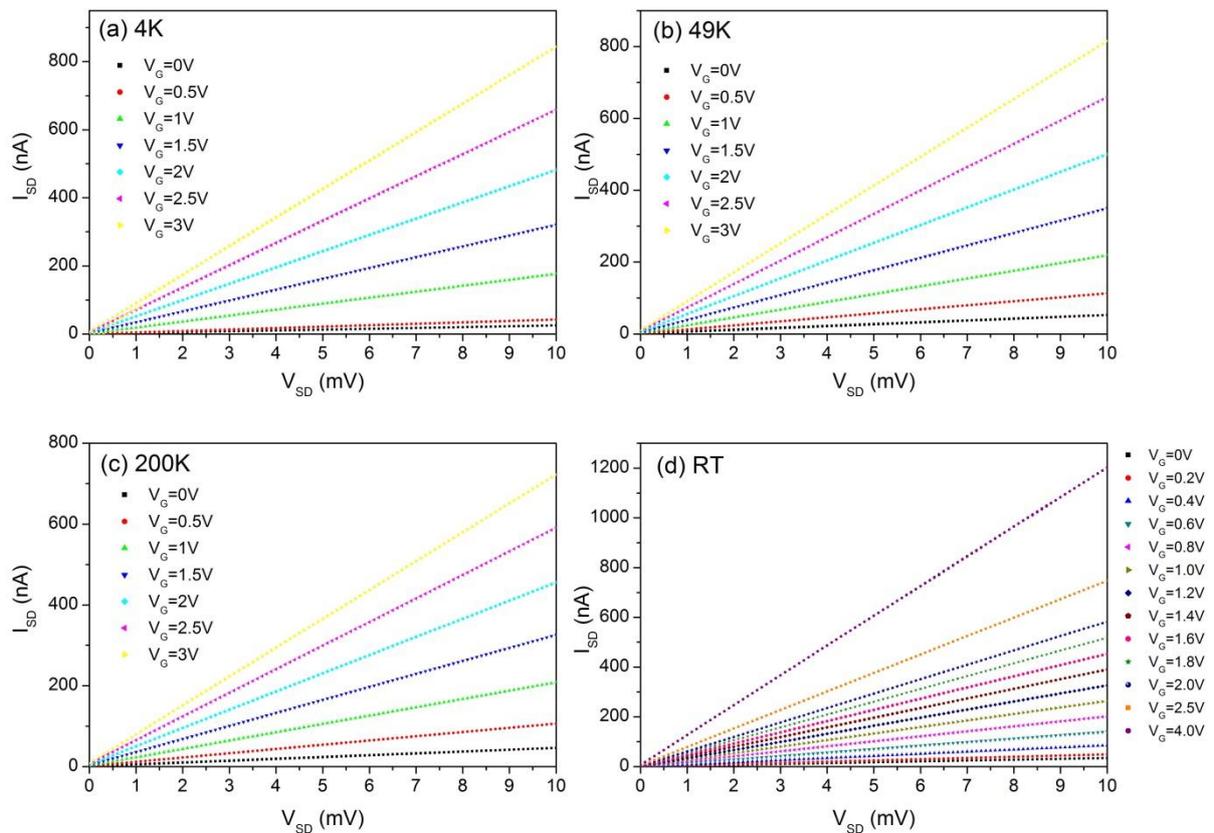


Figure 23. Source-drain sweeps done on 5x50 μm n-type devices at different temperatures, ranging from 4 K to room temperature (RT). Gate voltages range from 0-3 V, except for the RT-data, where it ranges from 0-4 V

The mobilities derived from these measurements (using threshold voltages derived from gate sweeps at corresponding temperatures) are shown in Table 4. These mobilities are far closer to previously reported values²⁸. Lower mobility values when compared to literature might be attributed to increased interactions (with the surface and other electrons) caused by gating. For more conclusive results, additional analysis outside the linear regime needs to be done as discussed below.

Table 4. Mobility values derived from the results shown in Figure 23.

T (K)	μ (cm ² /Vs)
4	1130±150
50	970±80
200	780±40
300	400±50

Besides these measurements on n-type devices, also measurements on hole mobility were done. Measurements done on the devices made in run R2 can be seen in Figure 24, source-drain sweeps at temperatures from 4 K to room temperature were made. It can be seen that only at gate values around 2 V, a sudden jump would occur. Raising the voltage any higher would not yield different results. Only at room temperature the step was more gradual.

As can be seen, in all measurements the current is very small compared to the current observed in electron mobility measurements. The mobility derived from these measurements (and the gate sweeps made on these devices) amounted to 5-50 cm²/Vs, which are values lower than expected²⁸. The cause of this was most likely the implantation dose (5e¹⁴/cm²) that was too low, due to most of the implantation ions being stuck in the oxide layer on top. Therefore in R3 devices were made with an increased p-type implantation dose.

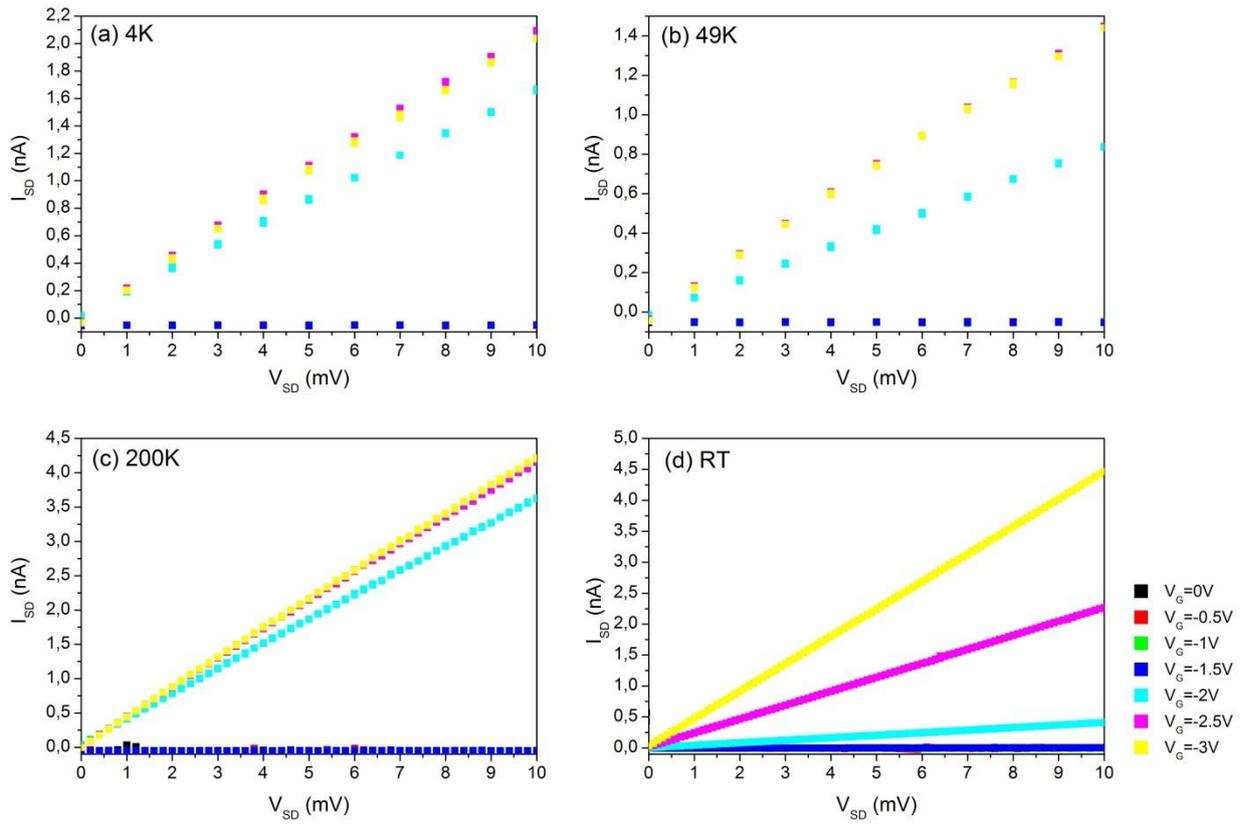


Figure 24. Source-drain sweeps done on $10 \times 20 \mu\text{m}$ p-type devices at different temperatures, ranging from 4 K (a) to room temperature (d). Gate voltages range from -0 to -3 V. It can be seen that only around a gate voltage of -2 V a sharp step occurs. Additionally, the currents measured are very low compared to the n-type devices.

After these measurements an extended analysis was done to characterize the FETs also outside of the linear regime, as well as to measure characteristics of the improved p-type devices. Both this second run of p-type devices R3, and a far more elaborate analysis of both p- and n-type devices were carried out in collaboration with J. van der Hoff, a B.Sc. student involved in the quantum dot project.²⁹

In these measurements, both source-drain and gate sweeps were done on devices of 5 different dimensions of $5 \times 50 \mu\text{m}$, $5 \times 20 \mu\text{m}$, $20 \times 20 \mu\text{m}$, $50 \times 15 \mu\text{m}$ and $50 \times 5 \mu\text{m}$, for both n-type and p-type devices. These measurements were done at a temperature of 4 K and at room temperature. An example of a full source-drain sweep as was made for all measurements is shown in Figure 25. In this figure again the source-drain voltage was swept for different gate voltages. When the drain-voltage is in the same order as the gate voltage pinch-off occurs and the device current approaches a saturation value. When the voltage “drain” contact becomes negative it starts acting as the source. The gate voltage, however, is still defined positive to the other contact (which has now become the drain). In this case, the gate voltage is always higher than both the source and the drain voltage, hence pinch-off will never occur and the channel will behave as an ohmic resistance. As the negative side of this characteristic is not used in any derivation, in the rest of the results shown (on the next pages), it will be omitted.

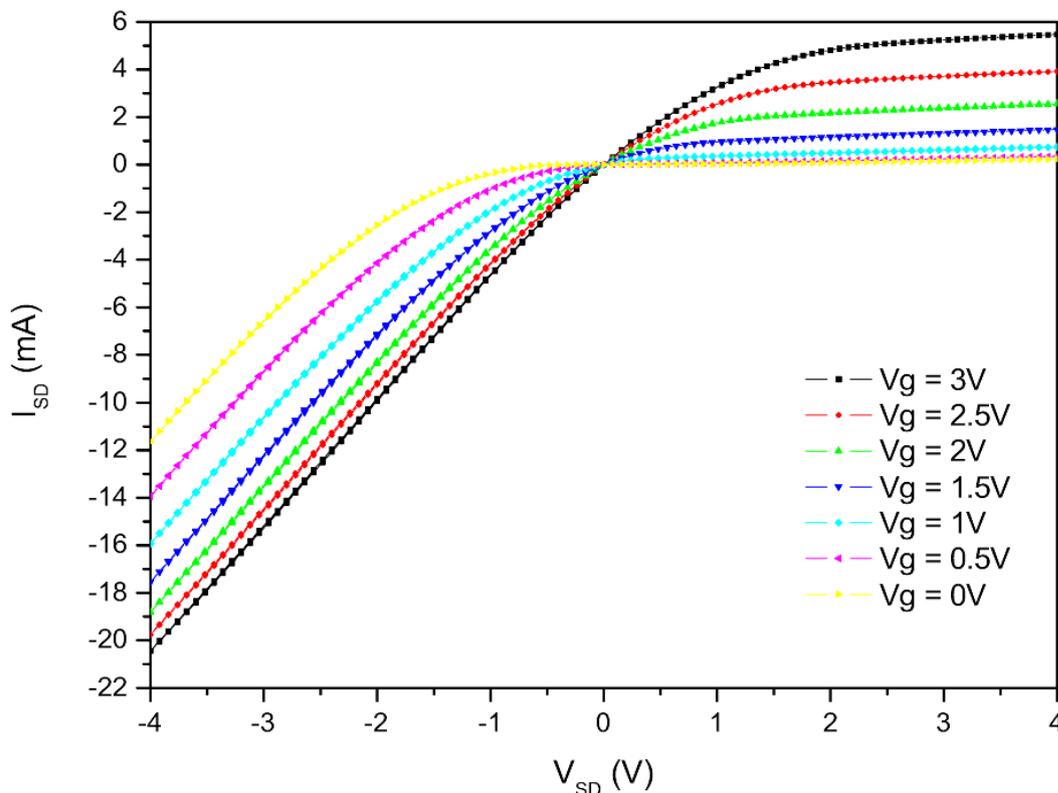


Figure 25. Source-drain sweeps made on an n-type device of $50 \times 5 \mu\text{m}$ at 4 K. Gate voltages ranging from 0-3 V were used. As long as $V_G - V_T > 0$ and $V_G - V_T > V_D$ the transistor will be in conductive mode. When the drain voltage becomes high compared to the gate the device will go into saturation as the difference between gate voltage and local potential in the channel is no longer significant to create an inversion layer.

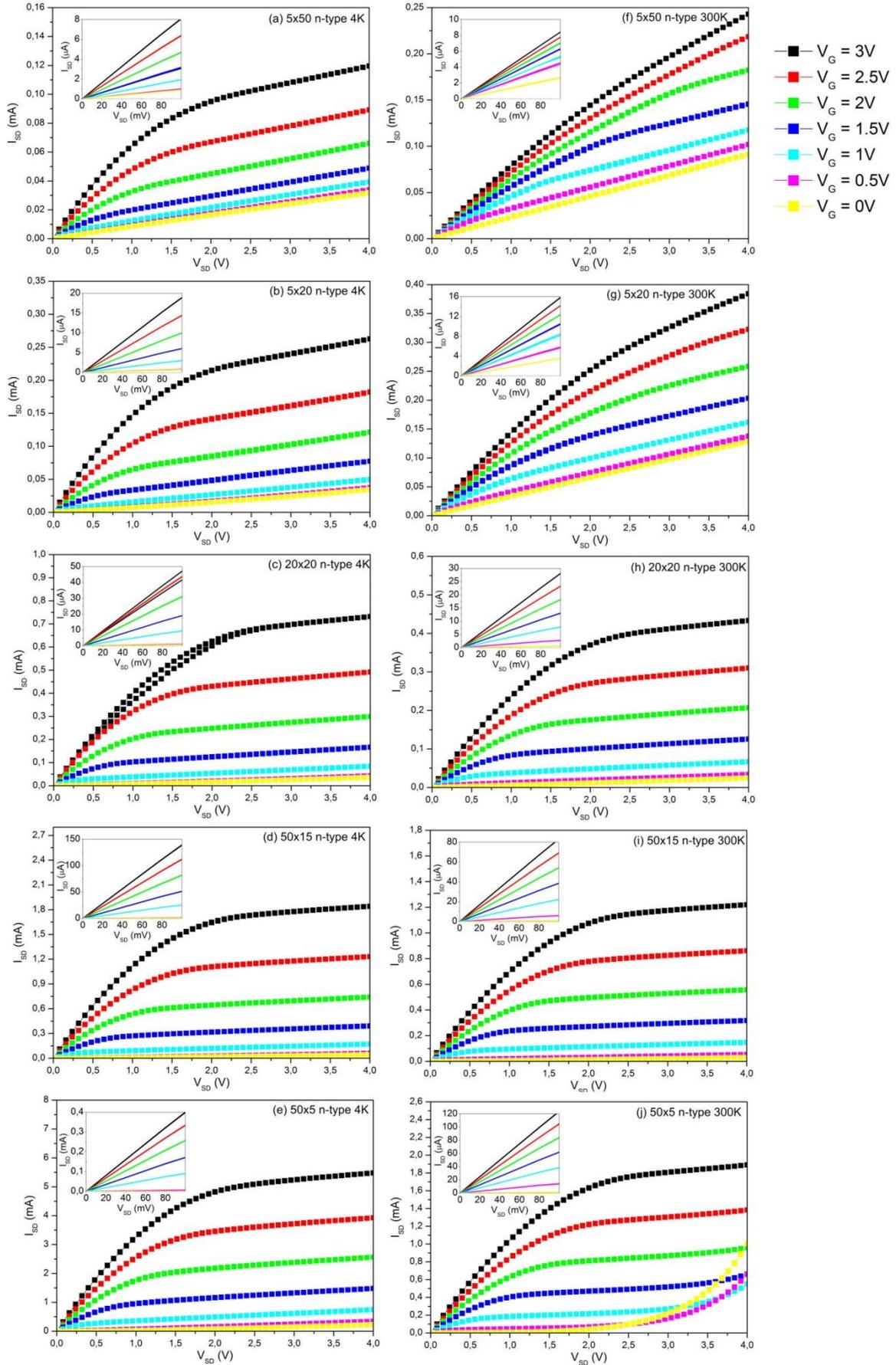


Figure 26. Source-drain sweeps made on different sizes of n-type devices at 4 K (left column) and room temperature (right column). The insets show the linear part of the characteristic from 0-10 mV.

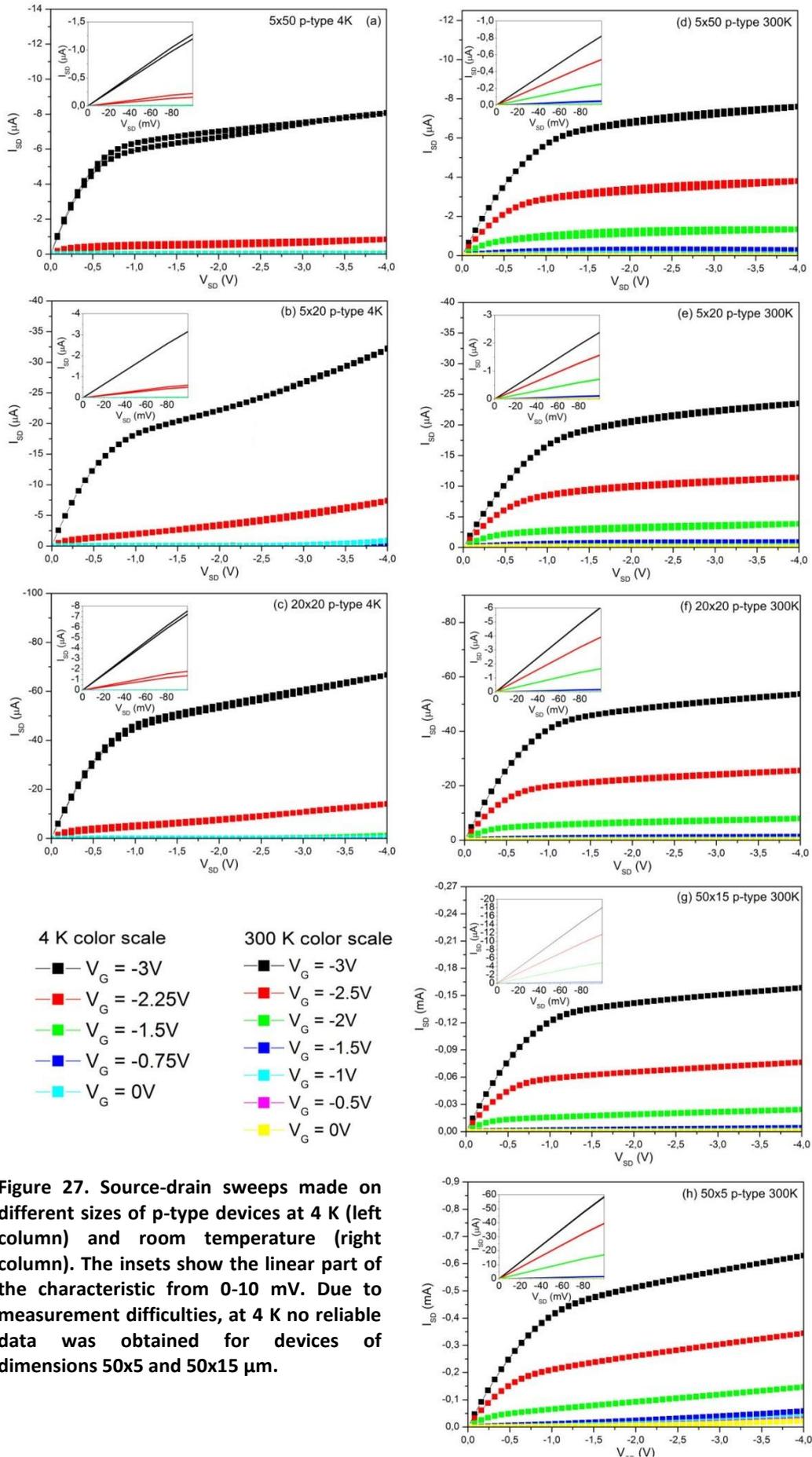


Figure 27. Source-drain sweeps made on different sizes of p-type devices at 4 K (left column) and room temperature (right column). The insets show the linear part of the characteristic from 0-10 mV. Due to measurement difficulties, at 4 K no reliable data was obtained for devices of dimensions 50x5 and 50x15 μm .

In Figure 26, the positive side of the measured data is shown for n-type devices at room temperature and at 4 K. The insets show a close-up of the linear part of this graph. In the devices with a high aspect ratio (a), (b), (f) and (g) it can be seen that there is a large relative leakage current; a current running even at zero gate voltage. This current may be attributed to this aspect ratio. In the model for a FET, an “infinitely wide” device is assumed, whereas in these cases the length far exceeds the width. It may be caused by some background doping in the high purity substrate, as for these devices this would cause more current to flow besides the gated regions compared to other devices.

In the I - V characteristic for the $50 \times 5 \mu\text{m}$ device at room temperature, Figure 26 (j), some peculiar behavior can be seen at low gate voltages, where the current starts increasing dramatically for higher source-drain bias voltage. This behavior resembles behavior of the avalanche effect, where high-energy electrons free more electrons when the bias is high enough. In this case however, this behavior would show even stronger at low temperatures (Figure 26 (e)) (since electrons could gain more energy before colliding with an atom), yet there it is absent. More likely, it is due to a breakdown of the long-channel-approximation, illustrated in Figure 28. This would mean that the length of the depletion zone could no longer be neglected compared to the length of the channel. Due to the fact that electrons now see a shorter distance for the same potential drop $V_S - V_{SAT}$ (from the source electrode to the ‘start’ of the depletion zone $L - \Delta L$), the current would increase. This does not explain the behavior fully however, as one would expect the current to increase linearly in this

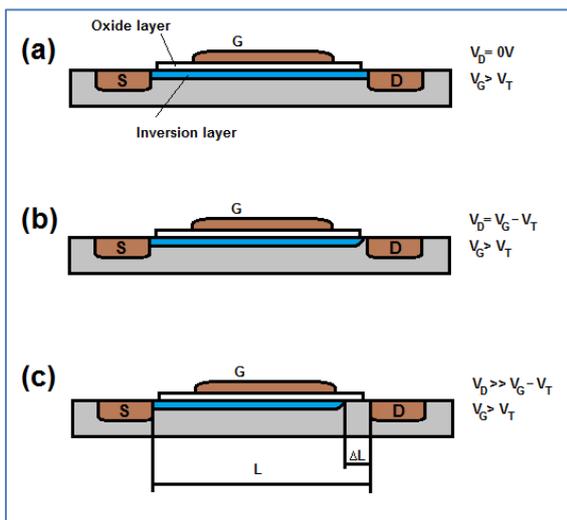


Figure 28. Inversion layer shape depending on gate voltage. (a) At low V_D the inversion layer extends from source to drain. (b) At $V_D = V_G - V_T$ saturation sets in, a small pinch-off region is seen. (c) At $V_D \gg V_G - V_T$ the pinch-off region extends a length ΔL . When ΔL can no longer be neglected compared to L the long-channel approximation breaks down and the current increases, as the channel length over which a voltage drop occurs increases.

case²¹. This effect is dominant at low gate voltages as for low gate voltages, the depletion zone gets wider as the potential difference between gate and local potential in the channel gets too small to create an inversion layer.

The double curve that can be seen in the measurement of the $20 \times 20 \mu\text{m}$ device at 4K most likely is due to temperature instability, as a change in the temperature changes the conductivity of the device and thus the shape of the I - V characteristic.

In Figure 27, the same data are shown for p-type devices. In these measurements it again proved difficult to acquire reliable data at 4 K. For high aspect ratio devices (50x5 and 50x15 μm) measurement data could not be acquired, because no adequate contact could be made between probes and electrodes. Additionally, the gate sweeps made (shown in the insets in Figure 31) at 4 K only showed useful data for the 5x20 μm device. For this device the threshold voltage was derived from the gate sweep. For the devices of 5x50 μm and 20x20 μm , the threshold voltage was approximated. This was done by estimating the turn-on gate voltage from the SD-characteristics shown in Figure 27; additionally it was compared to the threshold voltage of the 5x20 μm device. For 5x50 μm the threshold voltage was expected to be somewhat higher, and for 20x20 μm somewhat lower, based on a comparison with the n-type measurements.

For p-type devices, due to the significantly higher threshold voltage, the amount of useful data points in determining mobility is lower, due to the necessity for the gate voltage to be higher than the threshold voltage to get an inversion layer.

In Figure 29, data is plotted for the linear regime with on the y-axis $I_{SD}^*(L/Z)/(C_A^*(V_G-V_T))$ for different values of the gate voltage (the different data series), using a device with a channel length of 50 μm and length of 5 μm at 4 K. By plotting the data in this way, according to Equation (27) from the theory part, the slope of the graph gives the mobility value in m^2/Vs . For this graph, the threshold voltage was derived using the gate sweeps shown in the insets of Figure 30.

In Figure 29 a fit was made to the linear part of the data series. At higher V_{SD} it can be seen that the measurement points already start to deviate somewhat from this linear behavior as the saturation regime is approached. Next to the fit the mobility value corresponding to the slope of this fit is shown. In this way, mobility values were determined for all devices at both 4 K and 300 K. The results of these analyses can be seen in Table 5.

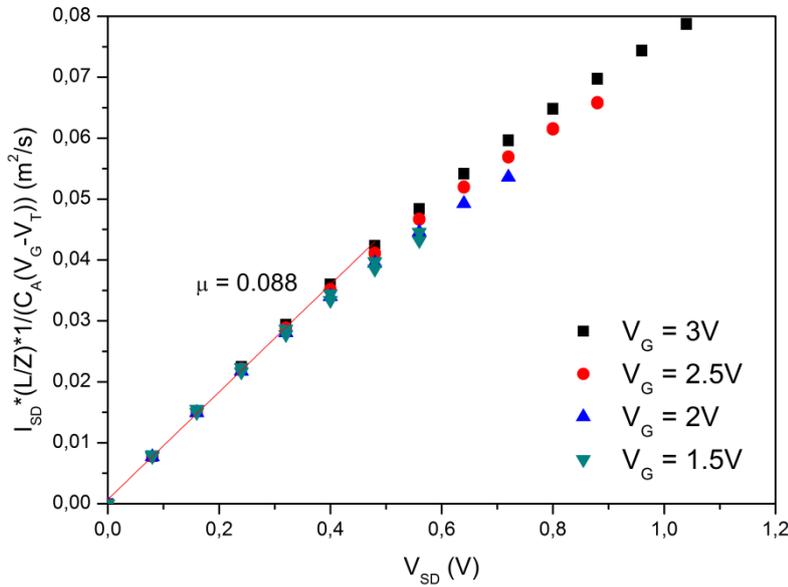


Figure 29. Plot of V_{SD} vs. $I_{SD}^*(L/Z)/(C_A^*(V_G-V_T))$ for a device of $5 \times 50 \mu\text{m}$ at 4 K. The different colors represent different gate voltages. By plotting in this way, the slope indicated gives the mobility in m^2/Vs . This plot focuses only on the linear regime, for lower gate voltages, already a nonlinear current is seen at higher source-drain voltages due to the fact that the saturation regime is approached quicker. For lower gate voltages the difference between gate voltage and threshold voltage was too low to get enough data points.

Additionally, mobility values were derived from the so-called “square-law”, by plotting the saturation current against the square of the gate voltage minus threshold voltage, as described in Equation (28) in the theory part. Here, again the saturation current was rescaled to $2 * I_{SAT}^*(L/Z) * (1/C_A)$, so the slope of the characteristic immediately gives the mobility for the device. The results are shown in Figure 30 (for n-type devices) and Figure 31 (for p-type devices) on the next pages. Additionally, the insets in these figures show the gate sweeps that were made at constant source-drain voltage, used to determine the threshold voltage. A fit was made to determine the mobility values, which are all shown in Figure 30 and Figure 31 as well as in Table 5.

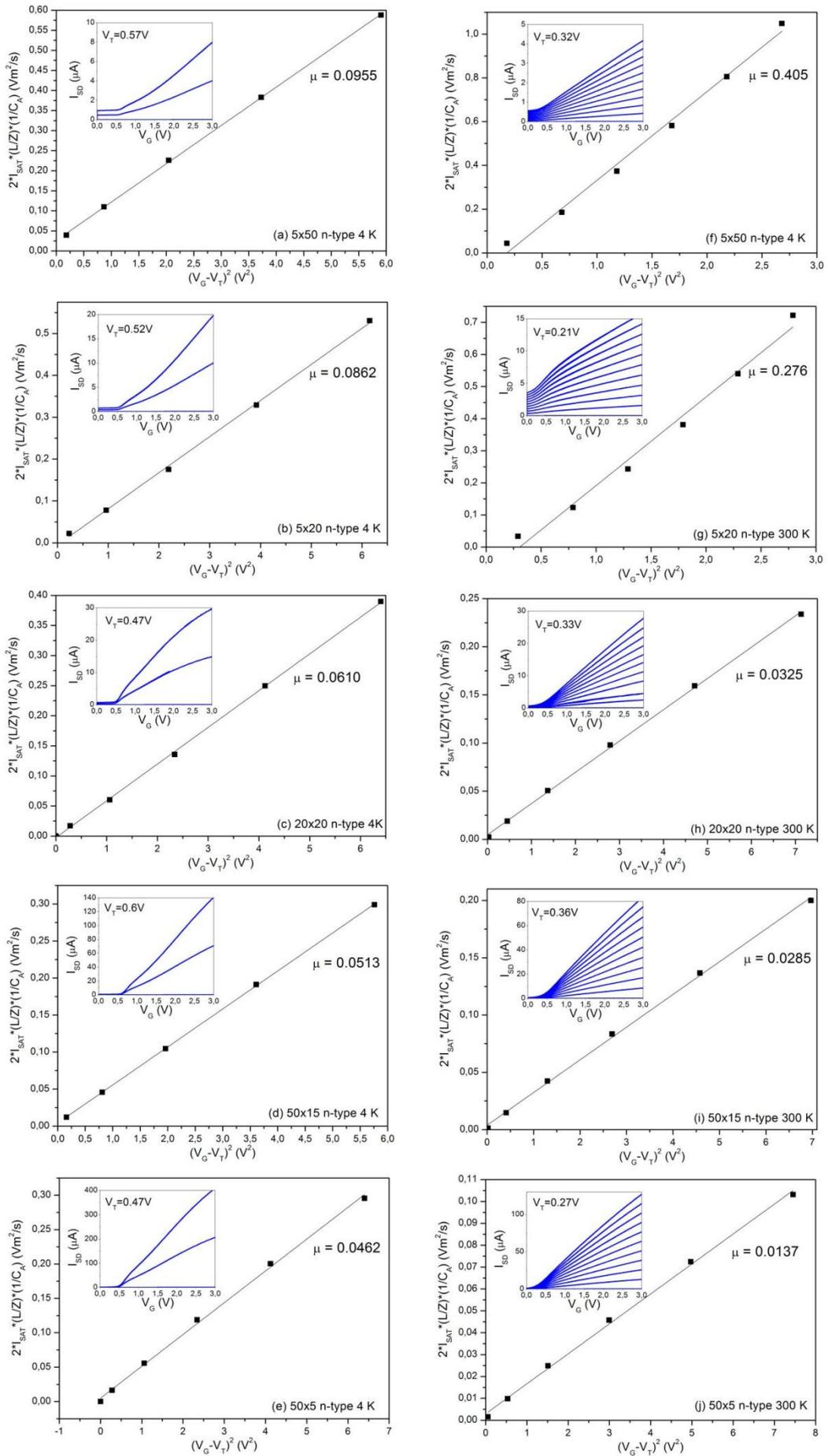


Figure 30. Graphs showing the dependence of the saturation current I_{SAT} on $(V_G - V_T)^2$. The y-axis has been rescaled to $2^{1/2} I_{SAT} (L/Z) (1/C_A)$ so the slope of the curve gives the mobility in m^2/Vs . The left column again shows data for 4 K measurements and the right column for room-temperature. The insets show gate sweeps from which the threshold voltage was derived.

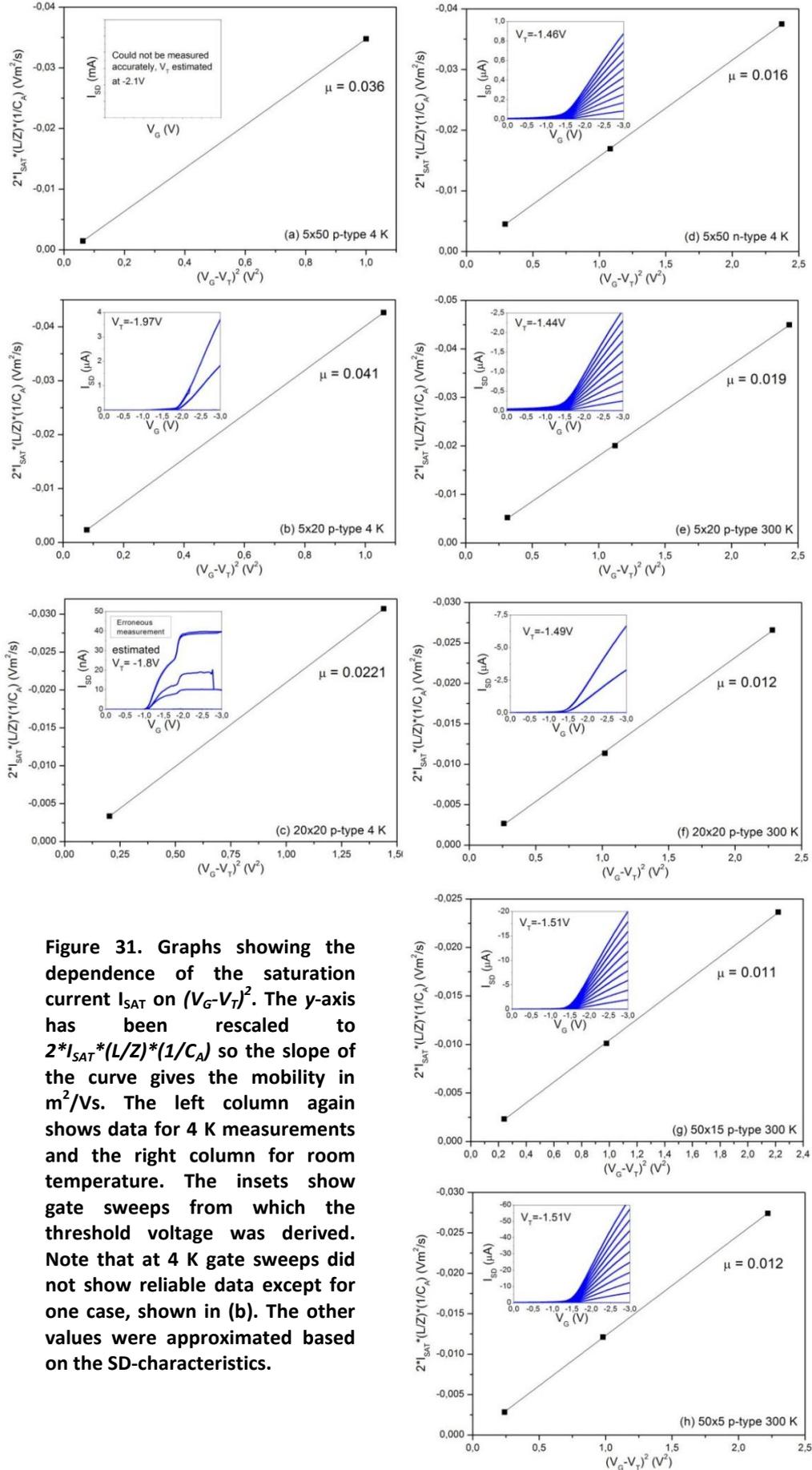


Figure 31. Graphs showing the dependence of the saturation current I_{SAT} on $(V_G - V_T)^2$. The y-axis has been rescaled to $2^*I_{SAT}*(L/Z)*(1/C_A)$ so the slope of the curve gives the mobility in m^2/Vs . The left column again shows data for 4 K measurements and the right column for room temperature. The insets show gate sweeps from which the threshold voltage was derived. Note that at 4 K gate sweeps did not show reliable data except for one case, shown in (b). The other values were approximated based on the SD-characteristics.

In Table 5 all calculated mobility values are shown. From all measurements multiple conclusions can be drawn about the properties of the wafers used:

First, most likely these high purity wafers still have some background charges which lead to n-type doping. This is reflected by the significant leakage current (the current at zero gate voltage) in measurements on the n-type devices in comparison to the p-type devices (most pronounced in Figure 26 (f) and (g)). It is further supported by the fact that for the n-type devices this effect is predominant in the devices with a narrow gate, where the n-type substrate would allow a current to run beside this gate. This is especially clear at room temperature; here thermal effects would increase the conductivity of the substrate by exciting electrons into the conduction band.

Table 5. Mobilities derived from FET characteristics for n- and p-type devices with different dimensions based on both an analysis of the linear part of the I - V characteristic and of the dependence of saturation current on the gate voltage. The relative differences between these two for different devices are quite similar in both measurements. The measurements indicated by a * were the ones done on devices showing very high leakage currents.

Device	RT mobility (cm^2/Vs)		4K mobility (cm^2/Vs)	
	Linear	Saturation	Linear	Saturation
<i>n</i> 20x20	270	325	500	610
<i>n</i> 50x5	120	137	420	462
<i>n</i> 50x15	240	285	460	513
<i>n</i> 5x20	580*	2760*	800	862
<i>n</i> 5x50	830*	4050*	880	955
<i>p</i> 20x20	100	120	150	221
<i>p</i> 50x5	100	120	no data	no data
<i>p</i> 50x15	90	110	no data	no data
<i>p</i> 5x20	160	190	270	410
<i>p</i> 5x50	140	160	310	360

Secondly, there is a great difference in the measured mobility values for different dimensions of devices. The mobilities derived from the longer and narrower (high aspect ratio) devices are higher than that derived from the shorter and broader (low aspect ratio) devices. This is most likely due to the leakage currents described above and due to the fact that the theoretical model which based on an “infinitely long” FET. The difference in mobility values given by the two models (a higher value in the saturation model) is most likely due to the limited applicability of equation (26) in cases where V_D approaches $V_G - V_T$ ²¹.

The values measured for the mobility, shown in Table 5, are mostly quite reliable. None of these are around the known value for bulk intrinsic silicon²⁸. Yet the relative difference between n-type and p-type devices is about the same factor of 3 different (with the exception of the n-type devices of 50x5, 5x50 and 5x20 μm at room temperature. The latter two of these can be attributed to the leakage current. The first one shows a low mobility, probably due to slight misalignment of the masks. (As in a short device this is far more critical than in a long device.

Finally, as mentioned before, the calculated mobility values are effective mobilities in FET-devices. Due to the gate voltage applied, surface effects and roughness play important roles in reducing the mobility value. In charge transport by SAWs, the effective mobility of carriers will most likely be higher due to the absence of this field and any strong force pushing electrons to this surface.

IDTs

As was discussed, multiple IDTs with different configurations of the top layers have been fabricated and characterized. Most of these characterizations have been done by S. Büyükköse.

In a first measurement series, IDTs were made on a 230 nm ZnO layer on top of the SiO₂ layer of 100 nm which is on the Si substrate. The result of an XRD-measurement of this layer configuration has already been shown in Figure 13.

The results of the fabrication process can be seen in Figure 32. These SEM pictures show a close-up of the fingers defined by NIL. The features are purely in the imprint material. The contact electrodes (one visible at the top of (a)) have a comb shape because the HSQ layer to applied needs to be planarized. If these contact pads would be continuous, the HSQ layer here would become too thick due to the lack of space to go for the material. This would cause the central region not to be opened up once a back-etch of the HSQ is done.

In Figure 33 the IDTs can be seen after HSQ deposition, back-etch, under-etch and lift-off have been done. It can be observed that for any finger width, the pattern in the imprint material is transferred to the metal in a satisfying way. Here the IDT metal is directly on top of the ZnO layer, allowing for SAW excitation.

Using an Agilent N5244A PNA-X network analyzer, the frequency spectrum of these devices was measured, with probes having a Signal-Ground and Ground-Signal configuration. In this measurement configuration a high-frequency signal is applied to one of the IDTs after which the amplitude and phase of the reflected and transmitted power is measured. To account for any reflections of a result of impedance mismatch, for instance off the receiver port, a calibration is done using a SOLT (Short, Open, Load, Through) calibration on a CS-8 calibration substrate (from GGB Industries). To eliminate the direct coupling between the sender and receiver IDTs, known as crosstalk, an inverse-Fourier transform was made of the frequency-spectrum to get time-domain data. Here, the cross-talk signals, travelling at the speed of electromagnetic waves (so at light speed) can be separated out by applying time-gating. After this a Fourier transform will show the frequency spectrum of the acoustic signal more clearly. Especially for samples with a low electrical resistance this transformation will greatly improve the quality of the measured signals as otherwise this crosstalk becomes dominant.

In Figure 34 the measured frequency response is shown. Both transmission and reflection data are shown for IDTs with different finger periodicities. One can see multiple resonances being present in these devices. All Rayleigh modes, some of which are higher order modes. These modes are caused by the SiO₂ and ZnO layers on top of the silicon and are dependent on the thicknesses of these layers. For SAWs with a small wavelength, the signal is carried mostly by these higher order modes, most likely due to a weak electromechanical coupling in the IDTs at these wavelengths. All modes are labeled R1 through R4 in Figure 34.

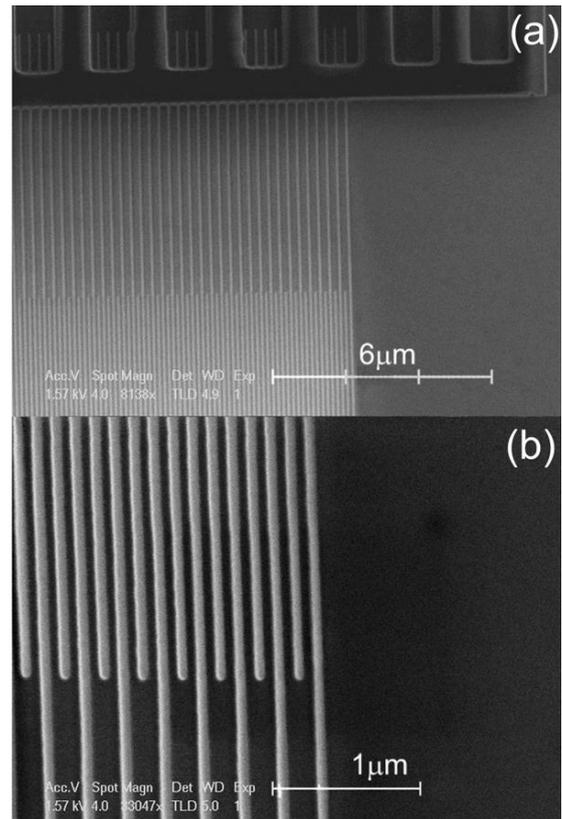


Figure 32. SEM pictures of imprinted substrates with a finger width of 65nm. In (a), the grating of the contact pads can be seen as well. In (b) it is shown that the fingers are straight and using this technique we have excellent critical dimension control. (Image taken from Ref. [23])

The reflection data is shown in two cases for different distances between the sender and receiver IDT, the red line showing transmission between IDTs a distance of 1081 μm apart and the blue lines for 405 μm apart. One can see that the further the IDTs are apart, the lower the transmission peak. This is because the SAW dissipates energy due scattering interactions with for instance defects or phonons. It can be seen that this scattering is more pronounced when the wavelength of the SAW gets smaller, due to the increased amount of interactions SAWs with smaller wavelengths have with the substrate.

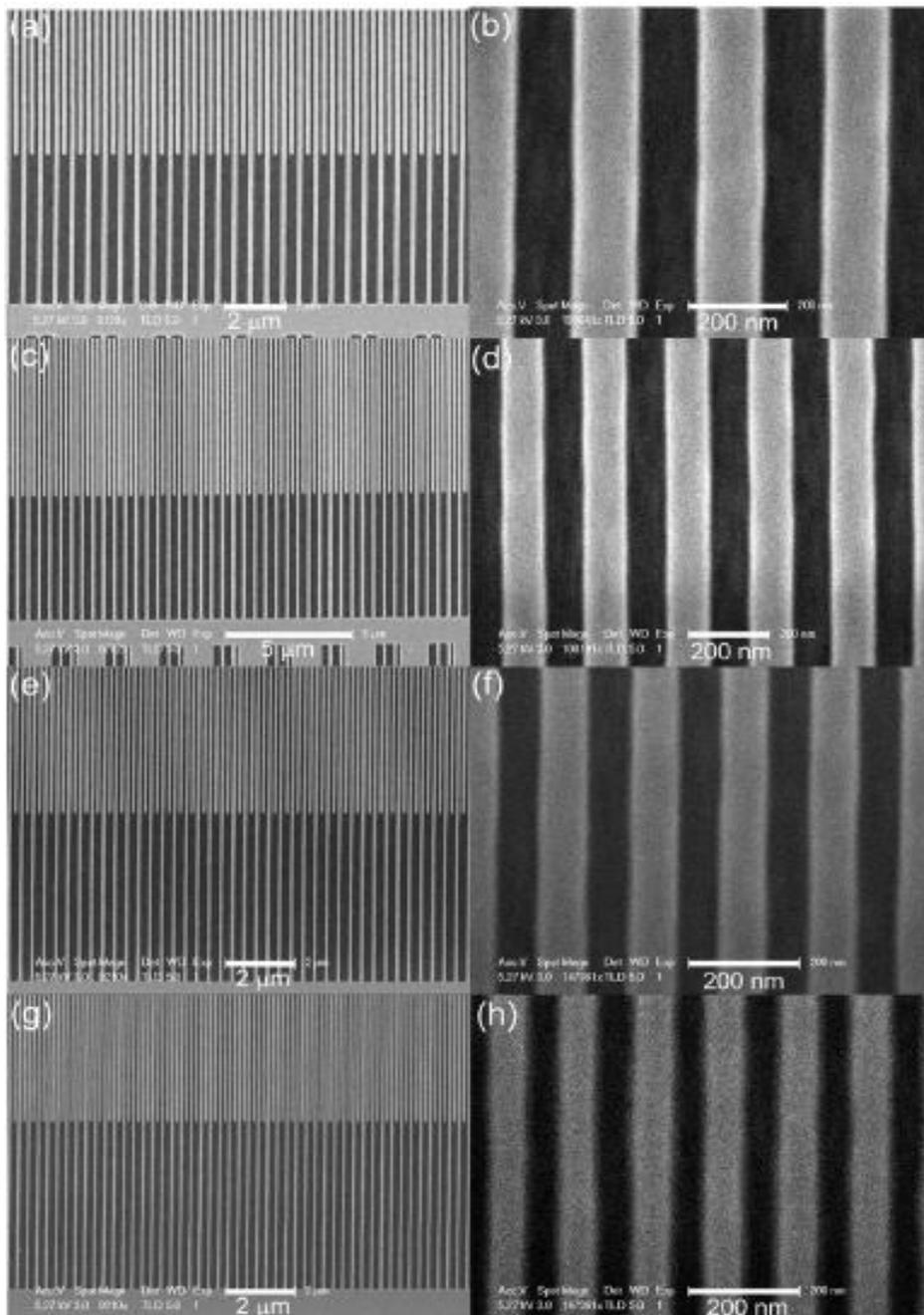


Figure 33. SEM images of metallized fingers, showing even after a complete process that the fingers are still insulated from each other and the critical dimension control is maintained. In (a) and (b) the finger width is 125 nm, in (c) and (d) 100 nm, in (e) and (f) 80 nm and in (g) and (h) 65 nm. Measurements have been done on these devices. (Image taken from Ref. [23])

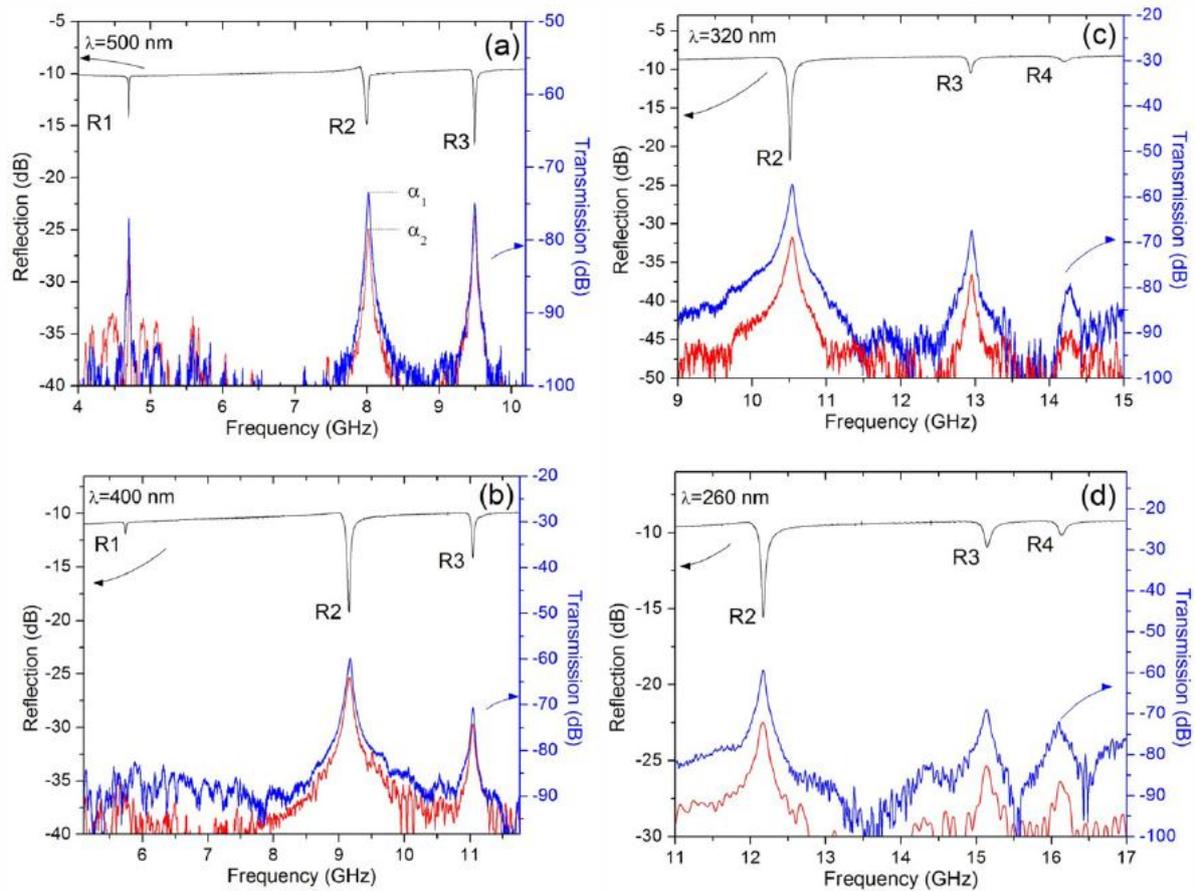


Figure 34. Measurement results on SAW transmission lines with the IDTs shown in Figure 33. Corresponding transmission and reflection peaks can be seen, meaning that indeed power is transferred from one IDT to the other by means of a SAW. In the transmission data red lines indicate distance between sender and receiver IDT of 1081 μm and the blue lines of 405 μm . (Image taken from Ref. [23])

As can be seen in Figure 34, transmission of signals of over 16 GHz is possible in these devices on Si. The fact that both transmission and reflection data is seen at the same frequencies shows that these are indeed signals carried by SAWs. These frequencies are higher than any frequencies shown in Si and show that NIL is indeed a good candidate for manufacturing IDTs. Additionally, simulations have been done on these devices using COMSOL Multiphysics. These simulations were done by S. Büyükköse and the results of these can be seen in Figure 35. The results of these measurements correspond well to the results of the simulations done on them, especially for the first and second order Rayleigh modes. For higher orders the slightly larger difference may be explained by imperfections in the ZnO layer, to which these modes are more sensitive. Details on the simulation setup and parameters can be found in [23].

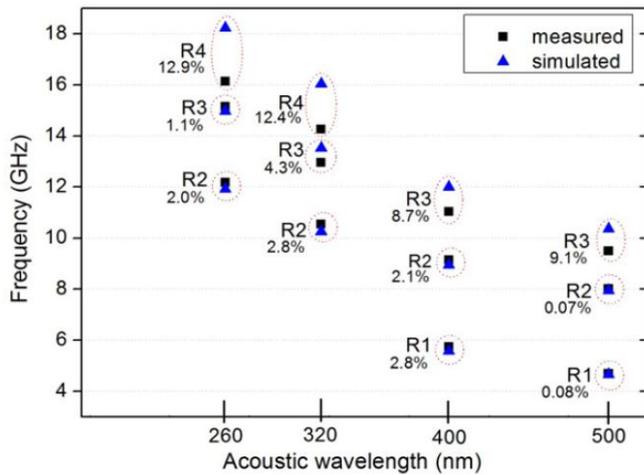


Figure 35. Comparison of the resonance frequencies obtained from simulation results and measurement results. These are done on IDTs manufactured on a ZnO/SiO₂/Si substrate. R1 through R4 indicate first to fourth order Rayleigh modes. (Image taken from Ref. [27])

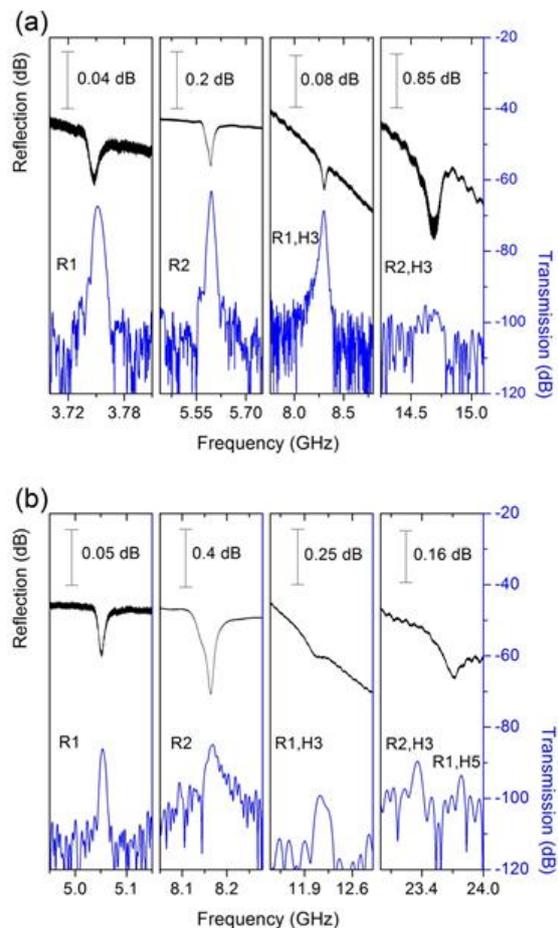
transmission peaks can be seen at frequencies ranging from 3.75 GHz to 14.6 GHz (depending on the Rayleigh mode and its higher harmonics) for devices with a 1 μm periodicity. Resonance frequencies range from 5.05 GHz to 23.4 GHz for devices with a 640 nm periodicity. The first and second Rayleigh modes are again indicated by R1 and R2, with higher harmonics indicated by an H followed by the order of the harmonic. These measurements show even higher frequencies than previously measured, allowing for even higher SAW speeds in the Si. Most importantly, the process in which these devices were made is CMOS compatible due to no ZnO layer being seen on the surface. The capping by SiO₂ allows for CMOS processes to be used on these samples.

The results of these measurements again are in agreement with simulations, as can be seen in Figure 37, further details on these simulations can be found in [27].

Figure 36. Measurement results of RF analysis of SAW transmission lines on a substrate with on top a ZnO layer sandwiched between two SiO₂ layers for SAW wavelengths of 1 μm (a) and 640 nm (b). Not only can SAWs be excited with this configuring, even higher frequencies can be reached as well. Higher harmonics are indicated by H3 and H5, and higher order SAW Rayleigh modes by R1 and R2. (Image taken from Ref. [27])

Using this same process, IDTs were also made on substrates having a 60nm ZnO layer on top sandwiched between two SiO₂ layers. The bottom of these two layers is 105 nm thick and the thickness of the top of these layers is 20 nm. Again ZnO piezoelectricity was verified using XRD-analysis. The results are shown in [27].

Results for double fingered IDTs with a periodicity (SAW wavelength) of 1 μm and 640 nm are shown in Figure 36, in these measurements the IDTs were placed 405 μm apart. In these figures corresponding reflection and transmission peaks can be seen at frequencies ranging from 3.75 GHz to 14.6 GHz (depending on the Rayleigh mode and its higher harmonics) for devices with a 1 μm periodicity. Resonance frequencies



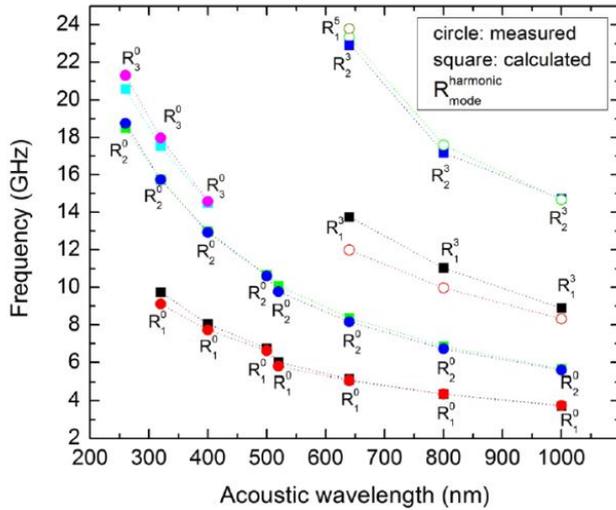


Figure 37. Comparison of the resonance frequencies obtained from simulation results and measurement results on IDTs manufactured on a $\text{SiO}_2/\text{ZnO}/\text{SiO}_2/\text{Si}$ substrate. R1 through R4 indicate first to fourth order Rayleigh modes. As indicated the subscripts of the R denote higher modes and the superscript higher harmonics. (Image taken from Ref. [27])

Finally, on these devices simulations were done on the electric field profile inside the material. These simulations have again been performed by S. Büyükköse. The simulations were done for a layer configuration of SiO_2 (20nm)/ ZnO (40nm -80 nm)/ SiO_2 (105 nm)/ Si . The results of these simulations for a ZnO thickness of 80 nm can be seen in Figure 38. Results are shown for the first and second order Rayleigh mode of a SAW with a wavelength of $1 \mu\text{m}$. Two different cases are distinguished. One in which the surface is covered with a thin metal later (indicated by 'short') and one without this metal layer. Since this metal layer shorts any piezoelectric potential difference at the surface it influences the depth profile as well. It can be seen that for the first Rayleigh mode, at the Si/SiO_2 interface (where charge transport should take place) it reduces the magnitude of the electric field, but at higher order modes in increases this magnitude, resulting in a higher electric field.²⁷

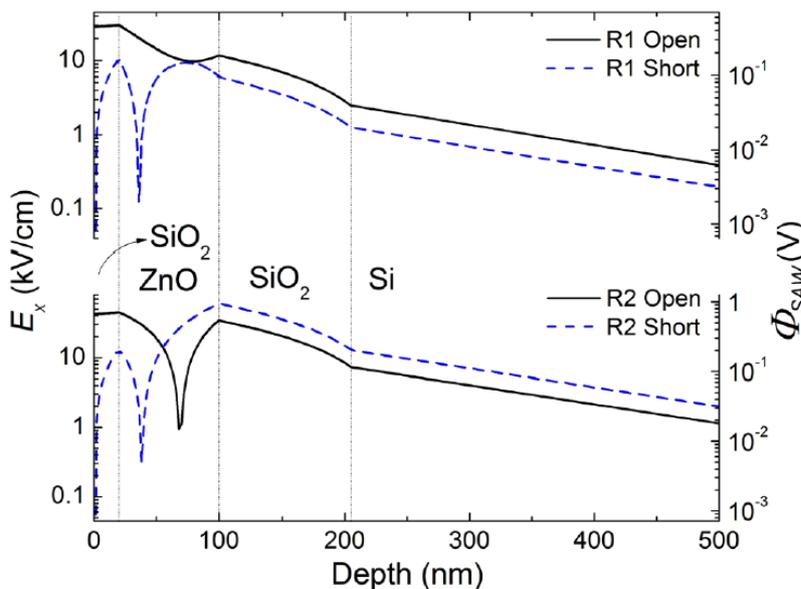


Figure 38. Simulation results on the piezoelectric field E and potential Φ inside the substrate as a consequence of a SAW with a wavelength λ of $1 \mu\text{m}$ at the surface. Results on both the first and second order Rayleigh mode are shown. Results are shown for a configuration with a cleared surface (open) and for a surface with a thin metal film on top (short). As can be seen this changes the electric field inside the material, for higher order modes the piezoelectric field is larger for a shorted surface. (Image taken from Ref. [27])

Based on the measured frequencies (in Figure 37) and the derived SAW velocity and the simulated potential distributions in the material (Figure 38), the minimum mobility values required for efficient charge transport were calculated. The results of these calculations for different modes and depending on a surface metal layer being present or not, are shown in Figure 39. These results show minimum required mobilities far lower than values reported in literature²⁸. Comparing these values to the values derived from the FET analysis, from Table 5, shows that mobility values at 4 K are sufficient for both electrons and holes to allow for efficient charge transport. At room temperature, if the effective mobility in charge transport measurements is equal to the effective mobility in FET measurement, hole mobility may limit efficient charge transport. Yet the effective mobility for charge transport is expected to be higher, meaning mobilities for both electrons and holes will most likely be high enough to allow for efficient charge transport.

As can be seen in Figure 39, only for the shorted R1 case and R3 at small wavelengths does the required mobility really get higher. When measuring at frequencies corresponding to the other modes, Mobility values should certainly be high enough.

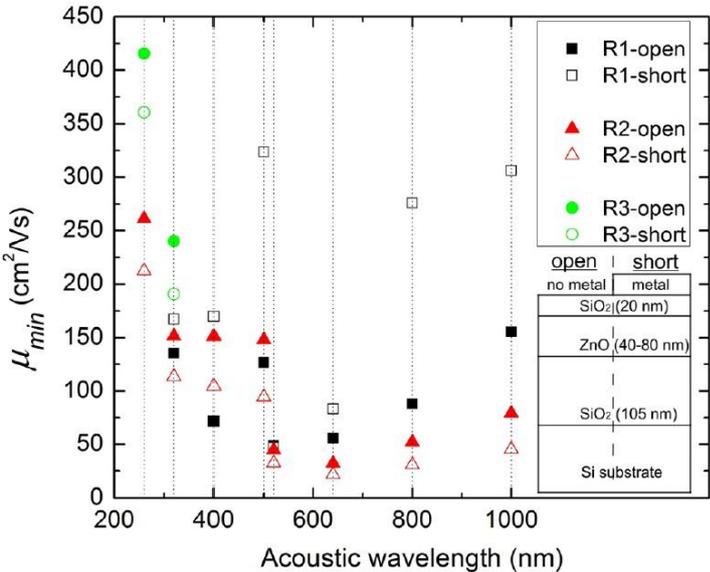


Figure 39. Calculated minimum required mobility values for efficient charge transport. These calculations were done based on the measurement results from Figure 37 and the simulation results from Figure 38. (Image taken from Ref. [27])

Chapter 5. Conclusions

Though no devices have yet been made which show charge transport, significant progress has been made towards realizing these devices. Calculations on the piezoelectric field distribution necessary for determining design parameters have been performed, mobility measurements have been done, and SAW generation at very high frequencies has been shown on Si substrates using a ZnO piezoelectric layer.

Mobility measurements have been done in different ways. First measurements were done on Hall bar devices; these yielded mobility values far higher than expected due to measurement errors. These measurement errors were caused by the inability of applying a gate voltage in the used measurement setup. Probably ground loops were formed yielding high amounts of noise and high gate currents. As a consequence of these unreliable measurements, mobility measurements on FETs were done.

Measurements on FET devices showed more reliable results. Measurements were done on devices of different dimensions and mobilities were derived by analyzing the linear part of the I - V characteristic and by analyzing the saturation current. Effective mobilities for electrons were around 400-600 cm^2/Vs at 4 K and around 250-300 cm^2/Vs at 300 K. Higher values were measured for devices with a high aspect ratio (long, narrow devices), but for these devices the model used was less accurate (as it assumed an “infinitely wide” FET. For holes it proved more difficult to get results due to low currents and problems in contacting the electrodes with the probe station. The mobility values for holes showed reasonably reliable results however, around 200-300 cm^2/Vs at 4 K and around 100-150 cm^2/Vs at 300 K.

As for the production of IDT devices using nanoimprint lithography, a novel fabrication approach utilizing the application of an HSQ layer for planarization and etch selectivity enabled excellent critical dimension control. Using these devices ultra-high resonance frequencies of up to 23.5 GHz were measured on devices utilizing a $\text{SiO}_2/\text{ZnO}/\text{SiO}_2/\text{Si}$ substrate layer structure. These devices were made using a CMOS-compatible process. The measured values were supported by numerical simulations. Even higher frequencies may be reached in materials with a higher SAW velocity.

Additional simulations were done on the electric field distribution inside the substrate, these show moderate required mobilities for efficient charge transport at the SiO_2/Si interface. Mobilities derived from FET measurements were around the same values, yet in SAWs, the effective mobility is expected to be higher due to the absence of a gate voltage drawing electrons to the surface. Therefore, efficient acoustic charge transport is expected to be feasible in devices made using this design process, though depending on the SAW mode, hole mobility may prove to be a limiting factor. The next step is to fabricate these and show acoustic charge transport in silicon.

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