University of Twente
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Designing a Low Noise Amplifier for Satellite Receivers in CMOS technology

Finding alternative low noise solutions

Master Thesis

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I dedicate this work to my grandparents,
from whom I inherited my technical ambition,
my drive and my faith.

Abstract

P.H. Woerlee et al. have demonstrated that due to downscaling the noise performance is improving. Calculations and simulations have been carried out to study the viability of a CMOS LNA, suitable for satellite receivers, in the current CMOS technology of 65 nm.

The used low noise amplifier (LNA) can be represented by a common source transistor (CS), based on the work of K. Shaeffer and T. Lee [4][5][6]. A common source transistor can be described by four main noise parameters (G_u, G_c, B_c, R_n) and two source parameters (G_s, B_s). The source parameters can be designed such that the minimum noise performance (F_{min}) can be reached.

An analytical model, based on the four noise parameters, is compared with simulation results. Despite some small differences the predictions of the CS model resemble the simulation model. The model gives design insight and it is used to find the best design for low noise performance.

The final and best design for low noise performance, having a noise figure of about 1 dB consists of a common source and cascode transistor together with a gate and drain inductance with a quality factor higher than 10. If a reasonable or good power match is desired an additional source inductance can be added, though the noise performance increases to just above 1 dB.

Although previously was found that a non-standard antenna resistance would give better noise performance [12], simulations have shown that a standard 50 Ω resistance gives similar noise performances as a non-standard antenna resistance.

A higher power dissipation results in a better noise performance, though a power dissipation of 20 mW can give near-optimal results.

An overview of the three designed circuits is given in the following table. Both NF and NF_{min} are given from 10.7 GHz to 12.75 GHz. The circuits were designed with a power constraint of 20 mW (I_d=16.667 mA) and a quality factor of 10 for the inductances.

Circuit type	$Width$	L_g	L_s	NF	NF_{min}	S_{11}	S_{21}
noise match	190 μm	400 pH	-	0.9 - 1.0 dB	0.7 - 0.8 dB	<-1.6 dB	>16.5 dB
n+p match	190 μm	600 pH	100 pH	1.0 - 1.1 dB	0.8 - 1.1 dB	<-11 dB	>13.0 dB
power match	190 μm	925 pH	180 pH	1.1 - 1.4 dB	1.0 - 1.3 dB	<-20 dB	>11.5 dB

The desired 1 dB noise figure can not be reached for all circuits. To improve the noise performance further it is advised to use higher quality inductances, especially a high quality gate inductance.

Acknowledgements

A study, done by myself but never on my own.

It is with great pleasure that I would like to thank everyone who made my study and this master thesis possible. The list of names would be immensely long if I name all of them personally. Fortunate I know that the ones supporting me, especially during the tough periods of my study, know that the following lines are meant for them.

I am grateful to my student colleagues, especially the ones sharing the same workspace, for providing a stimulating and fun environment in which to learn, to grow and to enjoy.

I would like to thank the chair holder of my master thesis department, for his mental support, his faith and his contangoes enthusiasm during my study.

The friends, that I have been neglecting during the final stages of my study, deserve some credits for not letting me down during the most stressful times. I thank them for the support and the patience they all had.

I cannot end without thanking my family and my boyfriend for providing a loving and understanding environment. They supported me, stimulated me, loved me and above all they had faith in me.

Enschede,
the Netherlands Augustus, 2007

Talitha Faber

Contents

Chapter 1

Introduction

Due to enhancing technology the use of Radio Frequency (RF) and microwave receivers has increased in the last decennia. These receivers are for example used in cordless telephones, cellular phones, Wireless Local Area Networks (WLAN) and in satellite downlinks. This last example, satellite receivers, is the one of interest in this report.

The entire satellite system, as depicted in figure 1.1 consist of a satellite dish, an antenna, alow noise block (LNB), a coaxial cable and an integrated receiver decoder (IRD). The LNB is a combination of a low noise amplifier (LNA) and a Block down converter. The combination of an LNB and a feed horn is referred to as an LNBF.

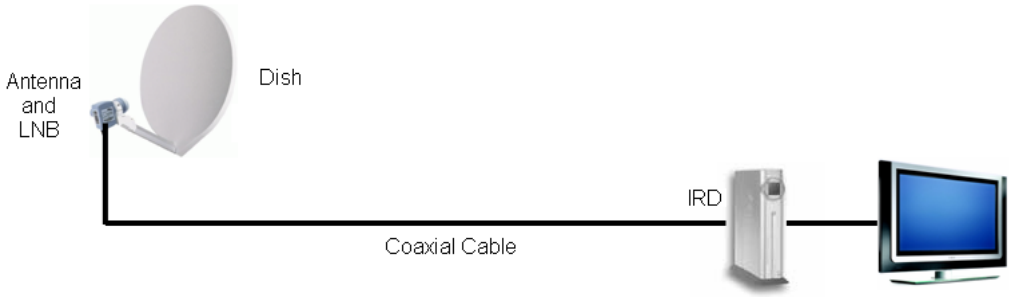

Figure 1.1: Satellite system

An LNA is placed at the front-end of a receiver system, following the antenna. The LNA increases the desired signal power, ensuring that as little noise and distortion as possible is added. The satellite frequency band is between 10.7 GHz and 12.75 GHz.

LNAs for satellite purposes are usually made with High Electron Mobility Transistors (HEMT's). The HEMT has a very good noise performance and makes it possible to design LNAs with sub-1 dB noise figure.

1.1 Thesis Motivation

Compared to mobile phone receivers, satellite receiver systems are still large and costly. Using CMOS technology for the LNA is a much cheaper solution compared with the accurate components that are used nowadays. Though it has not been possible yet to design an LNA working at this high frequency (10.7 GHz and 12.75 GHz) in CMOS technology with a similar low noise performance.

In recent years, CMOS technology has gotten smaller and smaller. P.H.Woerlee et al, have demonstrated that due to downscaling the noise performance of a single transistor is improving. Predictions have been done that with the CMOS technology of 50 nm a noise figure of

0.5 dB can be reached [1]. This prediction indicates the potential of CMOS LNAs. Apart from a decrease in cost the ease of adding digital functionality CMOS would also be an attractive result, as satellite systems heavily rely on digital coding/decoding.

The main resulting question is:

> Is it possible to design an LNA completely in CMOS technology which is suitable for satellite receivers?

Finding the answer to this question was the main goal of this master thesis. The steps that have been taken to find this answer are described in this report.

1.2 Thesis organization

After this short introduction the LNA will be thoroughly investigated and simulated. To give an idea of what will be discussed a small chapter organization is given beneath.

2nd chapter: Explanation of the noise fundamentals, based on the two-port noise theory and the main noise parameters. These parameters will be applied to a common source transistor, obtaining a noise model for a common source transistor.

3rd chapter: The influences of the source antenna on the noise performance will be explained.

4th chapter: An analytical model (the rho-model) will be compared with the simulation model (MOS-model 11) to determine the accuracy of the analytical model.

5th chapter: Power-constraint noise optimization and its influence will be discussed.

6th chapter: The complete LNA topology will be explained

7th chapter: Noise performance results with Spectre simulations will be shown.

8th chapter: Additional noise sources due to parasitics will be introduced and their effect on the noise performance will be shown with Spectre simulations.

9th chapter: Design improvements to obtain a lower noise performance will be mentioned and a more advanced analytical noise model will be discussed.

The thesis will end with conclusions and recommendations for future research on the same topic.

Chapter 2

Noise fundamentals

An LNA which achieves low noise performance is desired. Before trying to maximize the noise performance, it is useful to review the noise fundamentals. In this chapter a noise performance measure will be introduced and the noise fundamentals of a two-port network will be derived. The chapter concludes with analysis on a model, describing a simplified LNA.

2.1 Analytical noise model

To understand the noise contributions of an LNA an appropriate noise model can greatly simplify analysis and lead to useful design insight. For a (reasonable) simple analysis the noise theory of a classic two-port can be used [2]. A noisy two-port driven by a source with an admittance of Y_s and an equivalent shunt current noise i_s is depicted in figure 2.1.

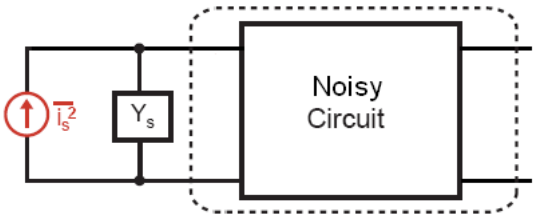

Figure 2.1: Noisy two-port driven by noisy source

2.1.1 Noise performance measure

For calculation purposes it is practical to have a measure in which the noise performance of a system can be expressed. A useful and well known measure for the noise performance is the noise factor (F) or the noise figure (NF) [3]. The noise factor is defined as:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{\overline{i_{total}^2}}{\overline{i_s^2}}. \tag{2.1}$$

The noise factor can be input or output referred, the derivations in this report describe the input referred noise factor. The noise factor can also be expressed in decibels and is referred to as the noise figure:

$$NF = 10log(F)\ [dB] \tag{2.2}$$

The noise factor is a measure of degradation of the signal to noise ratio by a device. The larger the degradation, the larger the noise factor. A noiseless system has F=1: the total output noise is entirely caused by the source. For instance, a two-port consisting of ideal inductors and capacitors (both lossless) has a noise factor F=1 (NF=0 dB).

2.2 Noise factor of a two-port

The noise performance of the two-port network can be analyzed with the introduced noise measure. To simplify the calculations the noisy two-port can be seen as a noiseless two-port with all the noise represented as input signals to the noiseless network, as depicted in figure 2.2.

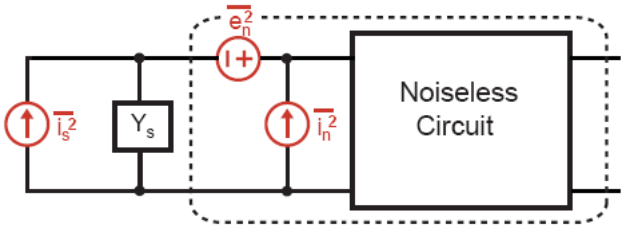

Figure 2.2: Noiseless two-port driven by noisy sources

The noise factor can be expressed as :

$$F = \frac{\overline{i_s^2} + \overline{|i_n + Y_s e_n|^2}}{\overline{i_s^2}} \tag{2.3}$$

In figure 2.2 the possible correlation between e_n and i_n has not been explicitly depicted. This can be done by splitting the i_n source in to two parts: i_u (part uncorrelated with e_n) and i_c (part correlated with e_n). The i_n source is now represented by the sum of these two:

$$i_n = i_c + i_u \tag{2.4}$$

resulting in a two-port network as depicted in figure 2.3.

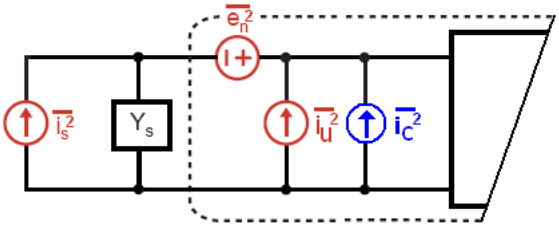

Figure 2.3: i_n split in a correlated and uncorrelated noise source

The correlated source i_c can be described as:

$$i_c = Y_c e_n = (G_c + jB_c) \cdot e_n \tag{2.5}$$

where Y_c expresses the correlation admittance [2], G_c the correlation conductance and B_c the correlation susceptance. Knowing this allows for representing the two-port as depicted in figure 2.4, in which Y_c is drawn as a fictive admittance element.

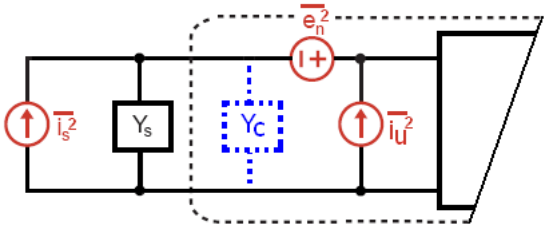

Figure 2.4: Representation of the correlation admittance

With the two-port representation of figure 2.4 the noise factor can be described by:

$$F = \frac{\overline{i_s^2} + \overline{|i_u + (Y_c + Y_s)e_n|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \cdot \overline{e_n^2}}{\overline{i_s^2}} \tag{2.6}$$

This expression contains three independent noise sources (e_n, i_u, i_s), which may be treated as thermal noise produced by an equivalent noise resistance (R) or conductance (G):

$$\overline{e_n^2} = R_n 4kT\Delta f, \tag{2.7}$$

$$\overline{i_u^2} = G_u 4kT\Delta f, \tag{2.8}$$

$$\overline{i_s^2} = G_s 4kT\Delta f, \tag{2.9}$$

Using these thermal noise expressions, the noise factor can be written as a function of its correlation and its source admittance (Y_c and Y_s), in which both are decomposed into a sum of a conductance (G) and a susceptance (B).

$$F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s} \tag{2.10}$$

This approach has resulted in a noise factor relation consisting of only four noise parameters (G_u, G_c, B_c, R_n) and two source parameters (G_s, B_s).

2.2.1 Obtaining F_{min}

For a two-port the optimal source admittance is the admittance that results in the lowest possible noise factor (F_{min}). Relation (2.10) can be used to find the absolute minimum noise factor F_{min}. By taking the first derivative of relation (2.10), with respect to the source admittance, and setting this derivative to zero results in a susceptance relation of:

$$B_s = -B_c = B_{opt}, \tag{2.11}$$

and a conductance relation of:

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \tag{2.12}$$

Both relation (2.11) and (2.12) should be fulfilled to minimize the noise factor. These relations can be substituted in relation (2.10) and after some rearrangements the minimized noise factor can be found to be:

$$F_{min} = 1 + 2R_n[G_{opt} + G_c] = 1 + G_c + 2R_n\sqrt{\frac{G_u}{R_n} + G_c^2} \tag{2.13}$$

This minimized noise factor represents the absolute minimum noise factor that can be obtained in the circuit. The noise factor can now be expressed in terms of F_{min} and the decomposed source admittance:

$$F = F_{min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (Bs - B_{opt})^2] \tag{2.14}$$

This relation shows that the lowest possible noise factor is achieved by eliminating the second term (G_s=G_{opt} and B_s=B_{opt}). The noise factor will be, for this condition, in the center of the noise circles as represented by figure 2.5.

The circles represent a equal noise factor and the center represents the minimum noise factor F_{min}.

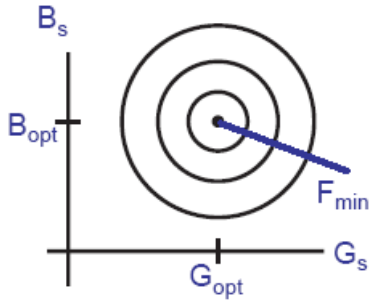

Figure 2.5: Circles of constant noise factor

2.3 Noise factor of a common source transistor

Based on the work of K. Shaeffer and T. Lee the main noise source of an LNA stage is the MOSFET common source transistor, as depicted in figure 2.6 [4][5][6].

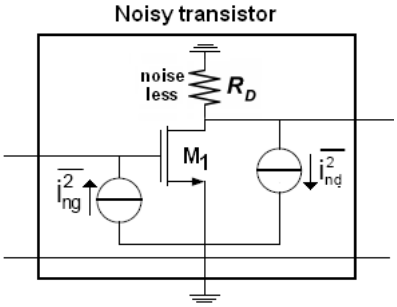

Figure 2.6: Noisy transistor model with drain noise and gate current noise source

The analyzed two-port network can be used to describe the noise of a common source transistor. It is necessary to describe the noise sources of the common source transistor as input sources of a noiseless transistor as depicted in figure 2.7; detailed derivations are added in appendix A.

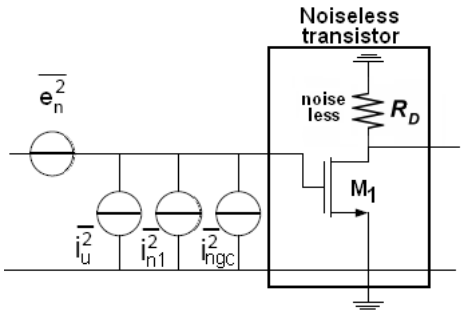

Figure 2.7: Complete input current model of a common source transistor

The noise model of the two-port network, as was found from section 2.2, has resulted in four noise parameters (G_u, G_c, B_c, R_n), the same noise parameters are valid for the common source transistor. Describing these noise parameters as a function of transistor parameters helps to find noise optimized solutions for a common source transistor.

Transistor parameter expressions of the noise parameters can be derived as described by T.Lee [2]. This set of derivations is added in appendix A, expanded with intermediate derivations and visualizations of the complex derivations. The resulting expressions, based on the assumption that the input impedance of a MOSFET is purely capacitive, are shown in table 2.1.

Parameter	Expression
G_c	0
B_c	$\omega C_{gs}(1 - \frac{g_m}{g_{d0}}\lvert c\rvert\sqrt{\frac{\delta}{5\gamma}})$
R_n	$\frac{\gamma g_{d0}}{g_m^2}$
G_u	$\frac{\delta\omega^2 C_{gs}^2(1-\lvert c\rvert^2)}{5g_{d0}}$

Table 2.1: MOSFETS main noise parameters

The most simple antenna admittance is a purely resistive admittance. In chapter 3 a more complex admittance will be introduced. In the case of a purely resistive antenna admittance (Y_s), the susceptance (B_s) is zero and the conductance (G_s) is than equal to $\frac{1}{R_s}$. The source admittance (Y_s) is expressed by:

$$Y_s = G_s + jB_s = \frac{1}{R_s} \tag{2.15}$$

Substituting the expressions for the noise parameters in relation (2.10) results in a noise factor for a common source transistor:

$$F = 1 + \underbrace{\frac{R_s\delta\omega^2 C_{gs}^2}{5g_{d0}}}_{i_g\ contribution} + \underbrace{\frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0} R_s\omega^2 C_{gs}^2}{g_m^2}}_{i_d\ contribution} - \underbrace{2|c|\sqrt{\frac{\delta\gamma}{5}}\frac{R_s\omega^2 C_{gs}^2}{g_m}}_{correlation\ contribution} \tag{2.16}$$

This relations shows that the noise factor depends entirely on transistor parameters, with exception of the antenna resistance (R_s) and the gate source capacitance (C_{gs}). C_{gs} can be described with the first-order transistor relation for the gate-source capacitance, for a MOST:

$$C_{gs} = \frac{2}{3}WLC_{ox} \tag{2.17}$$

It shows that C_{gs} is a function of C_{ox}, which is a process parameter, and a function of the transistor width and transistor length. The noise factor relation can be used to find optimal transistor dimensions together with an optimal antenna resistance R_s, resulting in the lowest possible noise factor for the given design.

Substituting the expressions for the noise parameters in relation (2.13) results in a minimum noise factor for a common source transistor described by:

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega C_{gs}}{g_m}\sqrt{\delta\gamma(1-|c|^2)} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\delta\gamma(1-|c|^2)} \tag{2.18}$$

Obtaining the minimal noise figure, also referred to as noise matching, is not the same as power matching, also referred to as impedance matching. For convenience the derivations for power matching are added in appendix B.

Obtaining minimal noise figure (noise match) and maximum power transfer (power match) at the same time is, in general, not possible. This will be explained in more detail in chapter 6.

2.4 Model visualization

To simplify the visualization of the common source transistor, that in this specific situation can be used to represent the simplified LNA, the common source transistor as depicted in figure 2.8.a will, from now on, be represented as depicted in figure 2.8.b.

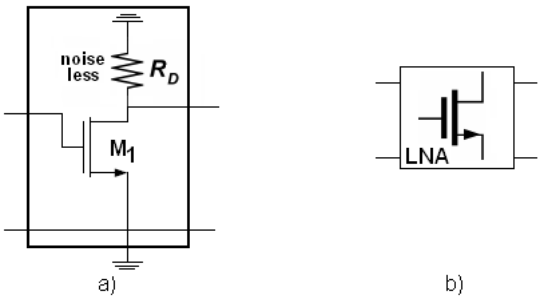

Figure 2.8: Common source transistor

2.5 Summary

It has been shown that an LNA can be modelled by a two-port network resulting in four noise parameters (G_u, G_c, B_c, R_n) and two source parameters (G_s,B_s).

A well chosen source admittance (Y_s) will result in noise match, obtaining the minimum noise factor (F_{min}) for a MOS device.

With the use of a two-port network, the noise factor of the main LNA noise source, the common source transistor, can be described as a function of transistor parameters, resulting in relation (2.16), repeated here for convenience:

$$F = 1 + \underbrace{\frac{R_s \delta \omega^2 C_{gs}^2}{5 g_{d0}}}_{i_g \ contribution} + \underbrace{\frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0} R_s \omega^2 C_{gs}^2}{g_m^2}}_{i_d \ contribution} - \underbrace{2|c|\sqrt{\frac{\delta\gamma}{5}} \frac{R_s \omega^2 C_{gs}^2}{g_m}}_{correlation \ contribution} \tag{2.19}$$

This noise factor relation together with methods of optimization will be discussed further in the next chapter. They will help in the search for the best design with the lowest possible noise factor.

Chapter 3

Noise influence of the antenna impedance

In chapter 2 the intrinsic noise sources of a MOSFET have been mentioned as contributing parts of the noise of the LNA. In this chapter the effect of the source admittance and the transistor width will be shown. Different types of source admittance will be introduced and discussed using the noise factor of a common source transistor. Some noise optimized possibilities will result from this, that will be used in the final design of the LNA.

3.1 Real antenna impedance

An antenna connected to a common source transistor, representing the LNA, has a source admittance Y_s (described by relation (2.15)), as depicted in figure 3.1. The LNA representation was explained in section 2.4.

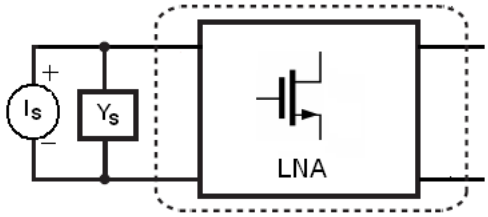

Figure 3.1: Model for the antenna

In case of a real source admittance the source susceptance B_s is zero, as was introduced in chapter 2. The source admittance can be described by:

$$Y_s = G_s = \frac{1}{R_s} \tag{3.1}$$

The antenna resistance plays an important part in the noise factor relation (2.16) and as such has a big influence on the noise factor.

3.1.1 Rho-model

An additional set of relations based on the transistor model is needed to study the noise influences of the transistor dimensions together with the antenna impedance (source admittance). The transistor model that is used is the rho-model, as used by T.Lee [2]. It has been chosen for its simplicity, in contrast to the MOS-Model 11 used in simulators. It can give design insight that can help to find the optimal design. According to earlier research the model is accurate enough to predict the noise performance. The basic derivations of the rho-model can be found in appendix C, the fundamentals will be given next.

The drain current I_d can be represented by:

$$I_d = WLC_{ox}v_{sat}E_{sat}\frac{\rho^2}{1+\rho} \tag{3.2}$$

and the conductance g_{d0} and the transconductance g_m by;

$$g_{d0} = \mu C_{ox}\frac{W}{L}V_{od} \tag{3.3}$$

$$g_m = \mu C_{ox}\frac{W}{L}V_{od}\frac{1+\frac{\rho}{2}}{(1+\rho)^2} \tag{3.4}$$

in which the last term is referred to as α:

$$\alpha = \frac{1+\frac{\rho}{2}}{(1+\rho)^2} \tag{3.5}$$

From these relations can be found that α can also be expressed as a function of the transconductance g_m and the conductance g_{d0}:

$$\alpha = \frac{g_m}{g_{d0}} \tag{3.6}$$

Finally, the first-order transistor relation, as introduced in section 2.3, for the gate-source capacitance for a MOST in saturation is needed:

$$C_{gs} = \frac{2}{3}WLC_{ox} \tag{3.7}$$

These rho-model relations can be substituted in relation (2.16). However this does not give much additional design insight, since this will result in a very complex relation. Although it can be used for analytical calculations, to find noise factor influences.

3.1.2 Reducing parameters

It is convenient to eliminate parameters from which values are known. The transistor parameters ($\gamma, \delta, \mu, c, C_{ox}, E_{sat}$ and v_{sat}), the operation frequency, the transistor length and the overdrive voltage need to be known to show the influence of the transistor width and the source impedance.

The operation frequency f is chosen such that it is in the center of the satellite frequency band: 11.7 GHz. Smaller device technology lowers the expected minimal noise figure. The smallest technology, of which transistor model libraries were available at the time of this project, was the $65nm$ technology. Resulting in a fixed minimal transistor length: $L = 60nm$.

Most of the remaining parameters are linked to the overdrive voltage (V_{od}). Giving a well chosen, though fixed, value to V_{od} allows for setting these parameters, for example 0.25 V.

With a fixed transistor length and a well chosen V_{od}, most of the parameters are fixed due to the relations of the rho-model. In appendix D, an example set of transistor parameters is given. These parameters are based on derivations by T.Lee [2] and model fitting procedures that will be explained in chapter 4. The noise factor relation (2.16) can now be rewritten as:

$$F = 1 \underbrace{+A * WR_s}_{i_g\ contribution} \underbrace{+\frac{B}{WR_s} + C * WR_s}_{i_d\ contribution} \underbrace{-D * WR_s}_{correlation\ contribution} \tag{3.8}$$

in which A, B, C and D constants based on the parameters given in appendix D.

As planned only the transistor width (W) and the antenna resistance (R_s) remain as variables, making it possible to do calculations to find the influence of the transistor width and the antenna resistance.

Given the parameter set in appendix D the terms B and C are much larger than the terms for A and D. This indicates that the effect of the gate current noise on the noise factor is much smaller than the effect of the drain current noise, and therefore there will be almost no correlation contribution. The drain current is, given this specific design, the dominant noise source and the main contribution to the noise factor is:

$$F_{reduced} = 1 + \frac{B}{WR_s} + CWR_s = 1 + \frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0} R_s \omega^2 C_{gs}^2}{g_m^2} \tag{3.9}$$

Neglecting the gate noise contribution, i.e. δ=zero, also influences the minimal noise figure NF_{min}. As shown in section 2.3 relation (2.18), F_{min} was represented by:

$$F_{min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega C_{gs}}{g_m} \sqrt{\delta\gamma(1 - |c|^2)} \tag{3.10}$$

Making δ=0 results in a minimum noise figure of 0 dB. It is of course an unrealistic prediction that $F_{min_{reduced}} = 1$, though neglecting the gate noise simplifies the analytical model leading to more design insight.

3.1.3 Analytical calculations

Both the transistor width (W) and antenna resistance (R_s) can be varied simultaneously, while keeping the transistor parameters, as given in appendix D, fixed. An optimal value for the transistor width and antenna resistance can be found, leading to the lowest possible noise factor [1]. The resulting image, using the complete noise factor relation, is depicted in figure 3.2 in which the noise factor is represented in decibels (noise figure). The influence of the 3^{rd} and 4^{th} are pointed out in the figure.

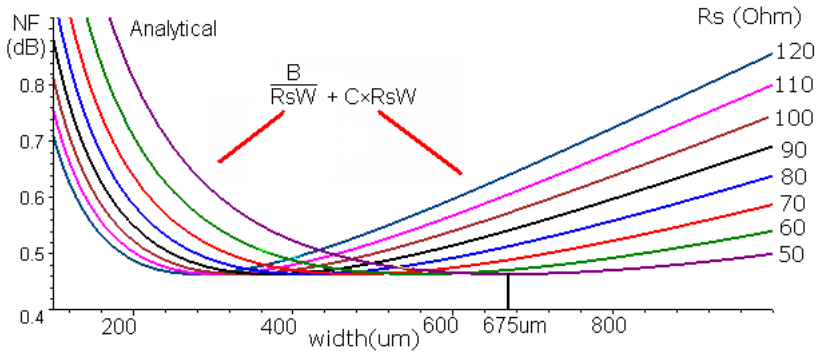

Figure 3.2: Noise figure versus transistor width while varying R_s

Figure 3.2 shows an absolute minimum, around 0.46 dB, for every antenna resistance. The following conclusions can be drawn from this:

- For every antenna resistance there exist an optimal transistor width;
- For every transistor width there exist an optimal antenna resistance.

[1] not to be confused with F_{min}, since B_s can in general not be equal to B_{opt} in case of a purely resistive antenna resistance

The minimum noise factor F_{min} is not shown in the figure. It is independent of the antenna resistance R_s and is according to relation (3.10) equal to:

$$F_{min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega C_{gs}}{g_m} \sqrt{\delta\gamma(1 - |c|^2)} = 1 + 0.03329 = 1.03329 \tag{3.11}$$

Equivalent to a minimum noise figure NF_{min} of 0.14 dB.

3.1.4 Optimal transistor width

The reduced noise figure $F_{reduced}$ described by relation (3.9) can be used to find an expression for the optimal transistor width, that results in the lowest noise figure given a resistive source impedance (not F_{min}). By differentiating relation (3.9) to the transistor width and setting it equal to zero, the optimal transistor width can be expressed as:

$$W_{opt} \approx \frac{3}{2} \frac{1}{wLC_{ox}R_s} \tag{3.12}$$

For the given transistor parameters and an antenna resistance of 50 Ω a transistor width W_{opt} of 618 μm is found, which is similar to the optimal transistor width of 675 μm found from figure 3.2 for $R_s = 50\,\Omega$. Resulting in a noise figure of 0.46 dB. This small difference between the optimal width using $F_{reduced}$ and the complete F shows again that the effect of the gate noise can be neglected.

3.2 Complex antenna impedance

The previous section has shown that, when using a purely resistive antenna impedance, there is an optimal antenna resistance and transistor width resulting in the lowest noise figure. In section 2.2.1 it was shown that, to obtain the absolute lowest possible noise figure, NF_{min}, it is necessary to match B_s to B_{opt}, where B_s represents the susceptance part of the source admittance. This part can be realized by a series capacitance or an inductance. The antenna together with the common source transistor can be represented by figure 3.3, in which Z_s represents the total source impedance.

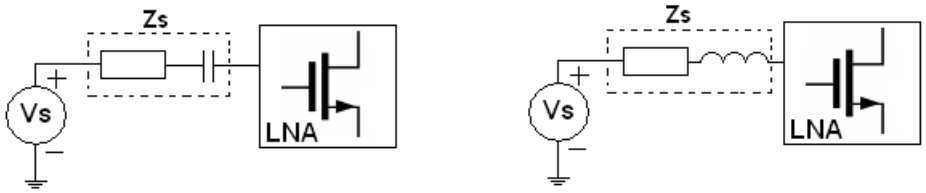

Figure 3.3: Model for the antenna with reactance

The noise factor including de term F_{min} is already given by relation (2.14). The noise factor was described in terms of conductance and susceptance. The impedance (Z_s) of the antenna can be written in terms of conductance and susceptance by:

$$Z_s = R_s + jX_s = \frac{1}{Y_s} = \frac{1}{G_s + jB_s} \tag{3.13}$$

In the following sections the influence of the two different types of reactance (capacitive or inductive) will be shown.

3.2.1 Capacitive reactance

When the antenna reactance consists of a capacitance, the model for the antenna and the LNA is as depicted in figure 3.4.

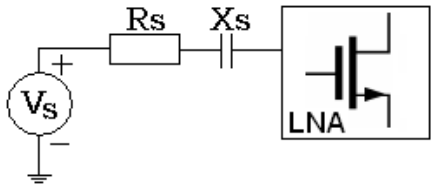

Figure 3.4: Model for the antenna with capacitive reactance

The source impedance can be described by:

$$Z_s = R_s + jX_s = R_s + \frac{1}{j\omega C} \qquad Y_s = \frac{1}{Z_s} = \frac{\omega^2 R_s C^2 + j\omega C}{1 + \omega^2 C^2 R_s^2} \tag{3.14}$$

where

$$I_m\{Y_s\} = B_s = \frac{\omega C}{1 + \omega^2 R_s^2 C^2} \qquad R_e\{Y_s\} = G_s = \frac{\omega^2 C^2 R_s}{1 + \omega^2 R_s^2 C^2} \tag{3.15}$$

It can be seen from relation (3.15) that not only the susceptance B_s but also the conductance G_s is influenced by adding a reactance to the model.

Both the conductance and the susceptance depend on the antenna resistance, antenna capacitance, transistor width and the operation frequency. Relation (3.15) and the main noise parameters from table 2.1 can be substituted in the noise factor relation (2.14). Specific values for the transistor width and antenna capacitance can now be found such that $B_s = B_{opt} = -B_c$ and $G_s = G_{opt}$, resulting in a noise factor equalling F_{min}.

Unfortunately it was found that either a negative antenna-capacitance or a negative transistor width is needed. Negative component values are not realistic. Adding a capacitor will therefore not result in obtaining F_{min}.

3.2.2 Inductive reactance

When the antenna reactance consists of an inductor, the model for the antenna and the LNA is as depicted in figure 3.5.

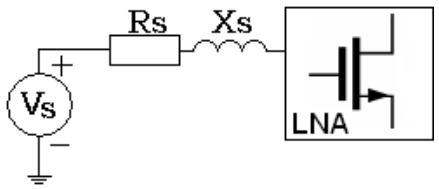

Figure 3.5: Model for the antenna with inductive reactance

The source admittance can be described by:

$$Z_s = R_s + jX_s = R_s + j\omega L \qquad Y_s = \frac{1}{Z_s} = \frac{R_s - j\omega L}{R_s^2 + \omega^2 L^2}, \tag{3.16}$$

where

$$I_m\{Y_s\} = B_s = -\frac{\omega L}{R_s^2 + \omega^2 L^2} \qquad R_e\{Y_s\} = G_s = \frac{R_s}{R_s^2 + \omega^2 L^2} \tag{3.17}$$

It can again be seen that not only the susceptance B_s but also the conductance G_s is influenced by adding a reactance to the model. In contrast to the situation with the capacitive source reactance, B_s is now negative as desired.

Both the conductance and susceptance depend again on the antenna resistance, antenna inductance, transistor width and the operation frequency. Relation (3.15) and the main noise parameters from table 2.1 can be substituted in the noise factor relation (2.13). Specific values for the transistor width and antenna inductance can now be found such that $B_s = B_{opt} = -B_c$ and $G_s = G_{opt}$, resulting in a noise factor equalling F_{min}.

Due to the minus sign in relation (3.17) all the component values become realistic values. A noise factor, equalling F_{min}, can be obtained by adding an antenna inductance. This leads to the conclusion that adding a series inductance leads to the lowest possible noise factor.

3.2.3 Analytical calculations

For an antenna resistance $R_s = 50\,\Omega$ it has been found analytically that, to obtain F_{min}, a transistor width of $197\,\mu$m and an inductance value of $2.2\,nH$ are needed. Both F_{min} and F, as represented by relation (2.13) and (2.14), can be plotted with these optimal values, resulting in figure 3.6. Both F_{min} and F are represented in decibels (noise figure).

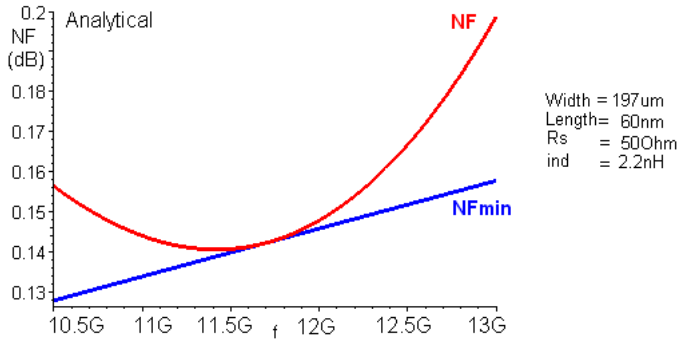

Figure 3.6: NF compared with NF_{min} (analytically), with optimal source inductance

Figure 3.6 shows that there is one frequency at which NF_{min} and NF are the same: at the center frequency that was used in the calculations.

From the calculation is found that the optimal transistor width given an antenna impedance with both a restive and inductive part was $197\,\mu$m. This is three times smaller compared to the optimal transistor width of $618\,\mu$m as found for a real antenna impedance of section 3.1 and as was expressed in relation (3.12). Concluding that the addition of a source inductance reduces the optimal transistor width.

When there is, for any reason, not the freedom to choose the width of the transistor, an inductance value can still be found to lower the noise factor. Though the obtained noise factor is most likely not as low as F_{min}. Only a specific set of inductance values has a positive influence on the noise factor given a specific transistor width. Figure 2.5 shows that for a B_s larger or smaller than B_{opt} the noise factor will increase, compared with F_{min}. When $B_s > 2B_{opt}$ the noise factor can become even worse than for the situation with $B_s = 0$.

The minimum noise factor F_{min} has not changed due to the change of B_s. As was shown in section 2.2.1 F_{min} is expressed by:

$$F_{min} = 1 + 2R_n[G_{opt} + G_c] = 1 + G_c + 2R_n\sqrt{\frac{G_u}{R_n} + G_c^2} \tag{3.18}$$

and thus independent of B_s and G_s.

The noise factor F has changed a lot due to the change of B_s and G_s, it has become very complex. The $F_{redcuced}$ noise figure relation as was given by relation (3.9) is now described by:

$$F_{reduced} = 1 + \frac{\left(\frac{R_s^2}{K^2} + \left(\omega C_{gs} - \frac{\omega L}{K}\right)^2\right)}{g_m^2 + R_s^2} \tag{3.19}$$

with L representing the antenna inductance and in which

$$K = \omega^2 L^2 + R_s^2 \tag{3.20}$$

Though the reduced relation indicates that δ is zero and therefore $F_{min_{reduced}}$=0 dB, as explained in section 3.1.2. Using $F_{min_{reduced}}$ means that the minimum noise figure is zero for all transistor widths, and no optimal transistor width exists.

3.3 Summary

In this chapter has been shown that there exist an optimal antenna resistance (conductance) together with a well chosen transistor width that achieves the lowest noise factor.

It has further been shown that adding an inductive susceptance to the source admittance lowers the noise factor even more. For a fixed antenna resistance there exist a transistor width and source inductance such that F_{min} can be obtained. This transistor width is much smaller than for the situation without the source inductance (section 3.1.3).

It can also be concluded that for a fixed transistor width there exist an antenna resistance and source inductance such that F_{min} can be obtained. When both the antenna resistance and the transistor width are fixed, a source inductance can still lower the noise factor, though most likely not as low as F_{min}.

Chapter 4

Rho-model vs MOS-model 11

In the former chapter calculations and design optimizations have been introduced with the use of the rho-model. The results from this model can only be used for the final design when the accuracy of the model predictions is known. It is therefore necessary to compare the rho-model (analytical) with the MOS-model 11 (simulation). The following three situations will be investigated to compare the two models.

1) The transconductance g_m as function of the gate source voltage V_{gs};

2) The influence of the source impedance together with the transistor width on the noise factor;

3) The gate noise contribution to the noise factor.

In appendix E the simulation conditions are explained and the standard circuit set-up is introduced.

4.1 g_m versus V_{gs}

Both g_m and V_{gs} are important design parameters. Therefore the influence of V_{gs} on g_m, of the two models, can be compared. A single transistor, with a transistor width of 200μm and an antenna resistance of $50\,\Omega$ is chosen for the first design. This transistor width is chosen to obtain a relatively low g_m, . An antenna resistance of $50\,\Omega$ is a standard antenna source value.

Often, transistor parameters based on earlier research are used, though the currently used CMOS-technology of $65nm$ is relatively new and transistor parameters for the rho-model where not used before in a similar setup at the time of this project.

The transistor parameters can be derived analytically with complicated calculations. Easier is to compare the rho-model (analytical), including known transistor parameters from former process technologies, with the simulation model. Changing the technology variables, like C_{ox}, E_{sat} and V_{th} can adjust the rho-model such that, in a specific range, it resembles the simulation model. The found values can be compared with MOS-model 11 to determine if the found values are reasonable values.

The circuit that represents the LNA as used in this section is depicted in figure 4.1. The bias circuit consists of a voltage source to set V_{gs}. The inductance is added as RF choke. The drain resistance is a noiseless resistance and will therefore not contribute to the noise figure.

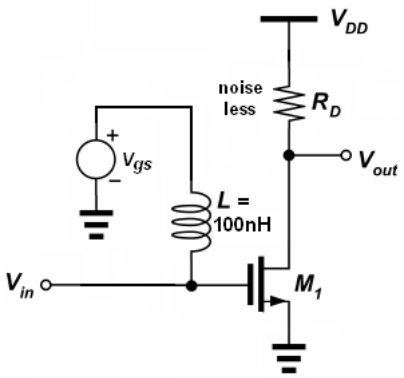

Figure 4.1: Circuit used as LNA

The results are shown in figure 4.2.a and 4.2.b. It can be seen from these figures that the rho-model resembles the simulation model when V_{gs} is between 500mV and 1V; there is a difference of about 1 %. The applied transistor parameters are given in appendix D; they will be used in the remaining of the LNA design.

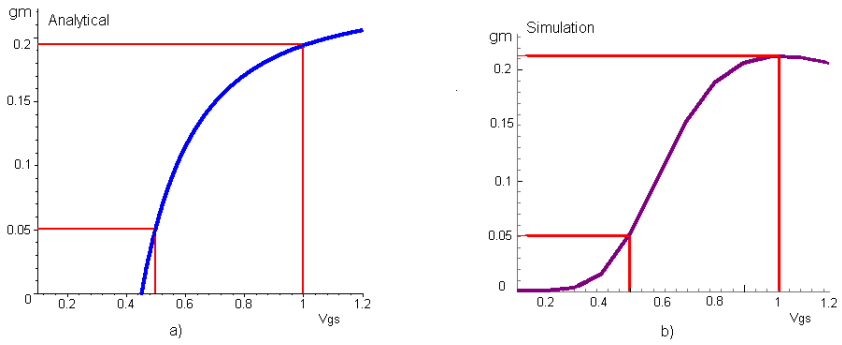

Figure 4.2: a) Analytical and b) Spectre simulation result for g_m vs V_{gs}

The value for V_{th} in the rho-model is 450mV while in the simulation V_{th} is between 300mV and 250mV. The difference in V_{th} between the two models can be explained by the reasoning that although both terms are named V_{th}, they represent something different due to the different models.

From the reasonable fit between the rho-model and the simulation model it can be concluded that the rho-model is accurate enough to continue with the other comparisons.

4.2 Antenna resistance and transistor width influences

In section 3.1 the theoretical influence of the antenna resistance R_s and the transistor width on the noise factor have been introduced. It was shown that according to the rho-model an optimal noise factor could be found when R_s and the transistor width are chosen correctly. A simulation has been done with the LNA circuit as was shown in figure 4.1.

The simulation result is given in figure 4.3.b. For comparison reasons the result given in section 3.1 is repeated in figure 4.3.a. The value of V_{gs} in the Spectre simulation was fixed at 700mV, which is in the middle of the V_{gs} range where the models can be compared. The value of V_{od} in the calculations is chosen as V_{gs}-V_{th}=0.75V-0.450V=0.25V.

The trend of both results is similar. For all antenna resistances there is an optimal transistor width that leads to the lowest noise factor, and vice versa. A little difference in the level of the noise figure is observable. This can be caused due to small differences in the transistor parameters.

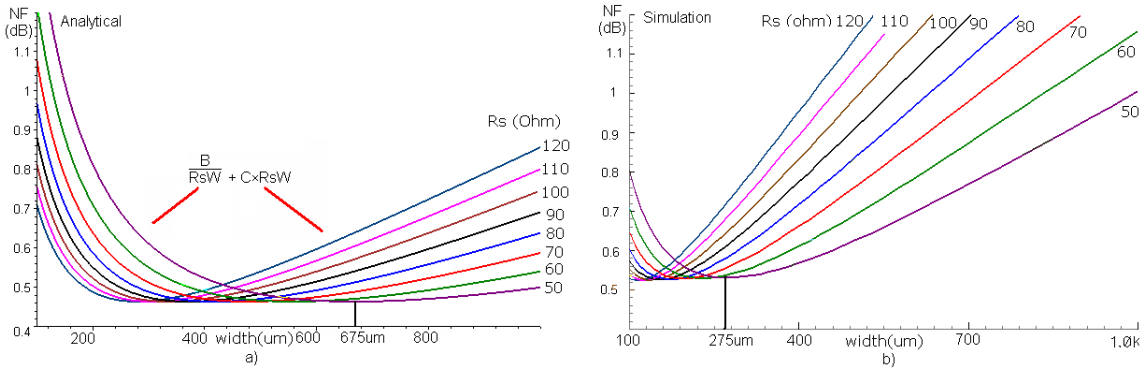

Figure 4.3: a) Analytical and b) Simulation sweep of both R_s and W

Despite the similarity in the noise figures of both the models, the transistor width to obtain the lowest noise figure is very different. While in the rho-model, for an antenna resistance of 50 Ω, a transistor width of 675 μm is resulting in the lowest noise figure, in the simulation model the lowest noise figure is found for a transistor width of 275 μm. The results from both the analytical calculations and the Spectre simulations, for R_s=50Ω, are summarized in table 4.1.

Analytical				Simulation		
$Width$	$Width_{reduced}$	NF	NF_{min}	$Width$	NF	NF_{min}
675 μm	618 μm	0.46 dB	0.14 dB	275 μm	0.53 dB	0.07 dB

Table 4.1: Calculation and simulation results for R_s=50Ω

For the rho-model the approximated optimal width was found to be:

$$W_{opt} \approx \frac{3}{2}\frac{1}{wLC_{ox}R_s} \tag{4.1}$$

The transistor length, the antenna resistance and the frequency are design parameters and equal in both the analytical calculations and the simulations. This indicates that the value for C_{ox} is perhaps incorrect, despite the match as found in section 4.1.

A possible reason for a different C_{ox} was found nearly at the end of the project and will be explained section 9.2.1. The analytical calculations that will be done in the intermediate chapters make use of the transistor parameters as given in appendix D and as used before.

4.3 Gate noise contribution

The analytical calculations as part of section 3.1.3 led us to the noise factor relation (3.8), in which A, B, C and D represented the values based on the parameter set in appendix D. It was found that B and C where much larger than A and D. The used noise analysis showed that the dominant noise source of the common source transistor is the drain current noise source, indicating that the gate noise may be neglected. This allows a simplification of the transistor noise model.

In simulation the LNA circuit of figure 4.1 can also be used to derive the noise summary. It was found that, for a transistor width of 275 μm (that gave the lowest noise according to the results from section 4.2) and an antenna resistance of 50 Ω, only a few terms contribute to the output noise. These terms are summarized in the table 4.2.

Parameter	Description	Noise contribution	% of total
r_n of input	input port noise	$1.49896 * 10^{-20}$	87.06
S_{th} of M_1	thermal noise	$1.67572 * 10^{-21}$	11.47
r_n of output	output port noise	$2.7401 * 10^{-22}$	1.59
S_{fl} of M_1	flicker noise	$2.88348 * 10^{-23}$	0.17
S_{ig} of M_1	induced gate noise	$1.66901 * 10^{-23}$	0.10

Table 4.2: Noise summary from simulation of single transistor (R_s=50Ω)

On the first row of this summary, the input port noise is represented. This is not a noise performance contributing term. It can be seen that the main noise contribution is S_{th}, thermal noise, representing 11.47% of the total noise. The term S_{fl} represents flicker noise and contributes only 0.17%. Even less is the contribution of the term S_{ig}, representing the induced gate noise which is only 0.10% of the total amount of noise.

The total output noise (TON) is the sum of all noise contributions. The noise factor can be calculated as follows:

$$F = \frac{TON - r_n \texttt{ of output}}{r_n \texttt{ of input}} = \frac{1.72184 * 10^{-20} - 2.7401 * 10^{-22}}{1.49869 * 10^{-20}} = 1.1306 \qquad (4.2)$$

Representing this noise factor as noise figure gives NF=0.53 dB. Figure 4.3 gave, of course, the same result.

The Spectre simulation confirm that for a common source transistor the gate noise contribution is very small and can be neglected. The reduced minimal noise figure $F_{min_{reduced}}$ becomes zero by neglecting the gate noise contributions as was explained in section 3.1.2. The minimal noise figure NF_{min} found by simulations was 0.07dB, which is near zero. Although it is unrealistic that $F_{min} = 0$, it is useful for the basic understanding of a LNA described by a single common source transistor.

4.4 Summary

Despite the small difference in g_m vs V_{gs} of 1 % and the optimal width difference the predictions of the rho-model resemble the simulation model. The rho-model can therefore be used to analyze the influences due to design changes.

When the noise figure increases or decreases in the rho-model, due to a certain design change, it may be expected that this will also happen in the simulation model. It is much easier and quicker to inspect first the influences on the rho-model before using the simulation model. This saves time and gives design insight (functional dependencies) which later on can help in making correct design choices.

Chapter 5

Power

In the previous chapters an analytical noise model, describing a common source transistor, has been derived. One important factor has not been taken into account: power consumption. Although a design with the lowest noise factor is desired, it is often not desired to have a high power consumption.

To study the influence of power, one could consider power as a constraint for the noise optimization. In the following sections, power will be introduced as a variable in the noise factor, enabling analytical calculations to show the influence of power on the noise performance.

5.1 Power-constrained noise optimization

To begin with, a resistive antenna impedance $Z_s = R_s$ will be considered. A common source transistor with its noise sources, as depicted in figure 5.1, will be analyzed. This topology was introduced in section 2.3 and appendix A.

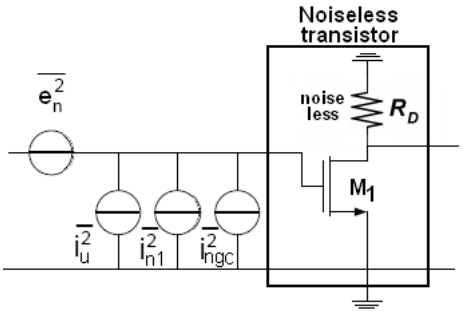

Figure 5.1: Common source transistor with its noise sources as input source

Often power is added to the noise figure representation in terms of circuit quality as described by T.Lee [2][7]. The used representation of the LNA is than already more advanced compared to a simple single transistor and the exact amount power is not specified. The power constrained noise optimization described next will have power as a parameter and is based on a single common source transistor. The noise factor needs to be expressed such that it takes power consumption into account to be able to say something about the influence of power on the noise performance. Some of the earlier presented relations, and the relations in appendix C, need to be linked to power dissipation.

Power is referred to as the supply voltage (V_{dd}) multiplied with the drain current I_d, see relation (3.2), resulting in:

$$P_d = V_{dd} \times I_d = V_{dd} W L C_{ox} v_{sat} E_{sat} \frac{\rho^2}{1+\rho} \tag{5.1}$$

This relation (5.1) can be rearranged such that ρ is written as a function of power consumption:

$$\rho = \frac{P_d \pm \sqrt{P_d^2 + 4P_d E_{sat} W L v_{sat} C_{ox} V_{dd}}}{2E_{sat} W L v_{sat} C_{ox} V_{dd}} \tag{5.2}$$

Both conductance g_{d0} and transconductance g_m, described by relation (3.3) and (3.4), are related to the relative gate overdrive voltage (ρ)[4][5][6]. With relation (5.2) both g_{d0} and g_m can be rewritten as a function of power:

$$g_{d0} = \frac{\mu P_x}{2L v_{sat} V_{dd}} \tag{5.3}$$

and by:

$$g_m = \frac{1 + (\frac{P_x}{2P_y}) P_x \mu C_{ox} E_{sat} W}{(1 + \frac{P_x}{2P_y})^2 P_y}, \tag{5.4}$$

in which P_x and P_y are represented by:

$$P_x = P_d + \sqrt{P_d^2 + 4P_d E_{sat} W L v_{sat} C_{ox} V_{dd}} \tag{5.5}$$

and

$$P_y = 2V_{dd} W L C_{ox} v_{sat} E_{sat} \tag{5.6}$$

The relations for g_{d0} and g_m, in terms of power, can be used in the noise factor relation for the common source transistor, relation (2.16), repeated here for convenience:

$$F = 1 + \underbrace{\frac{R_s \delta \omega^2 C_{gs}^2}{5 g_{d0}}}_{i_g \text{ contribution}} + \underbrace{\frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0} R_s \omega^2 C_{gs}^2}{g_m^2}}_{i_d \text{ contribution}} - \underbrace{2|c|\sqrt{\frac{\delta\gamma}{5}} \frac{R_s \omega^2 C_{gs}^2}{g_m}}_{\text{correlation contribution}} \tag{5.7}$$

Unfortunately, substituting g_{d0} and g_m in relation (5.7) will not lead to more insight. The substitution leads to a noise factor relation, described by F_{P_d}, that is only suitable to be used with a mathematical tool, like Maple, for complicated analytical calculations, which will be done in section 5.1.2. The minimal noise factor $F_{min_{Pd}}$ becomes also quite complicated. For more insight in the noise contributing factor the gate noise contribution can be neglected based on the results from section 3.1.2 and section 4.3.

5.1.1 Neglecting the gate noise contribution

As introduced in section 3.1, the contribution of the gate noise, to the noise figure, is very small compared to the contribution of the drain noise. The found relations for g_{d0} and g_m, given in relation (5.3) and (5.4) can also be substituted in the reduced noise factor relation as was given by relation (3.9) and repeated here for convenience:

$$F_{reduced} = 1 + \frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0} R_s \omega^2 C_{gs}^2}{g_m^2} \tag{5.8}$$

this results in a reduced power-constraint noise factor relation described by:

$$F_{P_d reduced} = 1 + \frac{\gamma P_y R_s}{P_x} \left(\frac{\frac{1}{R_s^2} + \omega^2 C_{gs}^2}{\mu C_{ox} E_{sat} W} \right) \frac{\left(1 + \frac{P_x}{P_y}\right)^4}{\left(1 + \frac{P_x}{2P_y}\right)^2} \tag{5.9}$$

in which P_x and P_y are represented by relation (5.5) and (5.6).

The reduced minimal noise figure $F_{min_{P_d}reduced}$, by neglecting the gate noise contribution ($\delta = 0$), is equal to 0 dB. It is of course an unrealistic prediction that $F_{min_{P_d}} = 1$, though neglecting the gate noise makes the analytical model much simpler leading to more design insight.

A closer look at the reduced noise factor relations reveals that relation (5.9) consist, next to the transistor parameters, out of four variables: the desired frequency f, power consumption P_d, the width of the transistor W and the antenna resistance R_s. The frequency is set to be 11.7 GHz, the center of the LNA frequency band. With only three remaining variables it is possible to study the influences of power on the noise factor.

Although the predictions will be done based on the reduced noise factor relation, the figures derived by analytical calculations, with the use of a mathematical tool, will be done with the entire power constraint noise factor F_{P_d}.

5.1.2 Analytical calculations

As shown in section 3.1.3, for a system with a resistive antenna source as depicted in figure 5.2, there exist a minimum noise figure (not NF_{min}) if the antenna resistance and the transistor width are chosen correctly. Indicating that also an optimal set can be found for the power constrained noise optimization method.

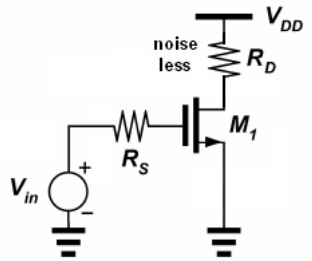

Figure 5.2: Single transistor with resistive antenna source

For now the antenna resistance R_s is fixed at 50 Ω. Using this value and the parameters given in appendix D, only two unknown variables remain: power and transistor width. In figure 5.3.a the influence of the transistor width on the noise performance for increasing power is shown.

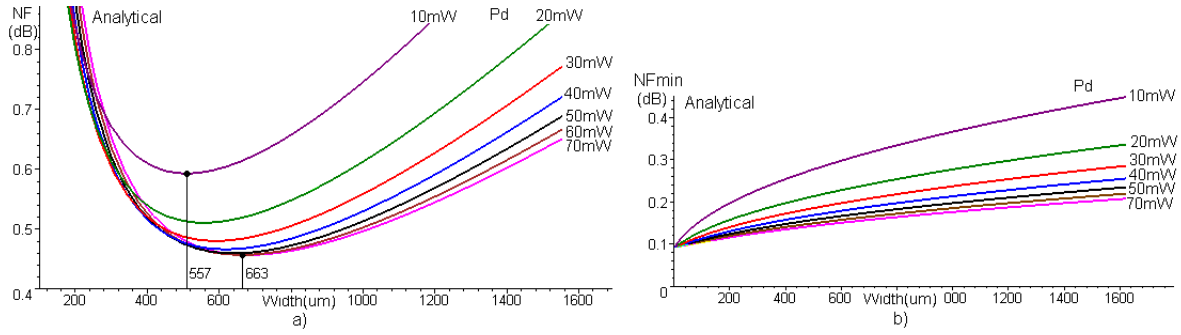

Figure 5.3: a) NF and b) NF_{min} vs transistor width while varying power ($R_s = 50\,\Omega$)

From figure 5.3.a can be seen that for a large transistor width a high power is causing less noise. For a small transistor width the opposite occurs. The very complex noise figure relation has a dominant part $1/W$ for very small transistor width, while for large transistor width the term W is dominant. An optimal width exist, for every power, leading to minimal noise figure.

The lowest noise figure, NF=0.47 dB is found for a transistor width of 663 μm and a relatively high power of 60 mW. The minimal noise figure NF_{min} is different given a different power, as can be seen from figure 5.3.b. A higher power results in a lower NF_{min}

This analytical result shows that for every power there is an optimum transistor width. Depending on the amount of power a systems may use, the optimum transistor width can be obtained. It can further be seen that the noise difference between 20 mW power and 60 mW is only 0.13 dB, which is a quite small difference for 40 mW more power.

5.1.3 Spectre simulations for constant antenna resistance

The analytical calculations need to be validated by Spectre simulations. To simulate a common source transistor with a power constraint the current I_d of the transistor must be kept constant while the transistor width is changed to find the optimal width. Qiaohui Zhang showed that a voltage-controlled-voltage-source (VCVS) with high gain can be used [12]. The used design is depicted in figure 5.4. With a noiseless drain resistance of 1 Ω the value of the drain current I_d will be equal to the value of V_{dc}. Varying V_{dc} results in the desired current, implementing different power consumption. For example V_{dc}=58.33mV gives an I_d= 58.33 mA which is equivalent to 70 mW power, due to a V_{dd} of 1.2 V.

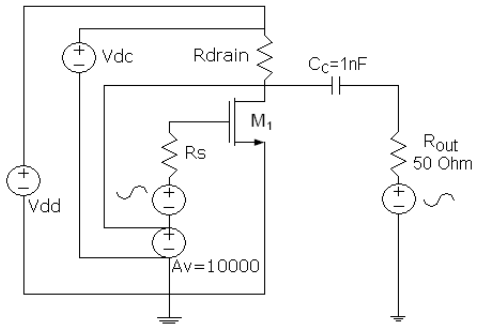

Figure 5.4: Schematic for power-constraint noise optimization

In figure 5.5.a the Spectre simulation results are shown for an antenna resistance (R_s) of 50 Ω. Similar to the analytical calculations, for a larger transistor width and higher power a lower noise factor is obtained. The trend of the Spectre simulations is similar to the trend of the analytical calculations, with the same transistor width difference as was found in section 4.2.

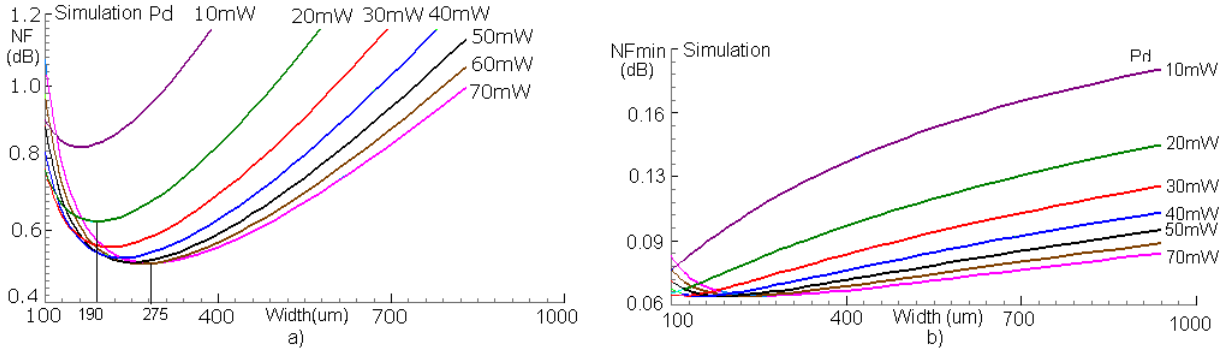

Figure 5.5: a) NF and b) NF_{min} (sim.) vs transistor width while varying power ($R_s = 50\,\Omega$)

The optimal transistor width is found for a power of 60 mW, the same power as found in the analytical calculations. The noise factor difference between a power of 20 mW and a power of 60 mW is very small. For a power of 60 mW the noise figure is 0.50 dB while for 20 mW power the noise figure is 0.63 dB. A difference of only 0.13 dB for 40 mW more power.

The trend of the minimal noise figure NF_{min} as depicted in figure 5.5.b is also similar to the analytical NF_{min} in figure 5.3.b, though the minimal noise figure is lower in simulation.

The similarities between the analytical calculations and the Spectre simulations indicate that the power constraint noise model is a representative model.

5.1.4 Spectre simulations for varying antenna resistance

It was seen, from figure 5.5 that an optimal transistor width can be found for every power-constraint, given an antenna resistance R_s of 50 Ω. Changing the value for the antenna resistance changes this optimal transistor width and changes the noise performance as well. All these variables make it very difficult to find an optimal situation.

Often, a design specification is given, eliminating at least one variable. In, for example, portable systems low power consumptions is desired. A similar circuit as depicted in figure 5.4 has been used for simulations but this time with I_d fixed at 16.667mA; obtaining a P_d of 20 mW.

Both the transistor width and the antenna resistance are varied resulting in figure 5.7. The figure shows that for the highest antenna resistance, $R_s = 120\,\Omega$, can obtain the lowest noise figure, NF=0.50 dB. While for an antenna resistance $R_s = 50\,\Omega$ the lowest noise figure is NF=0.63 dB. The difference between these minimum noise figures is only 0.13 dB.

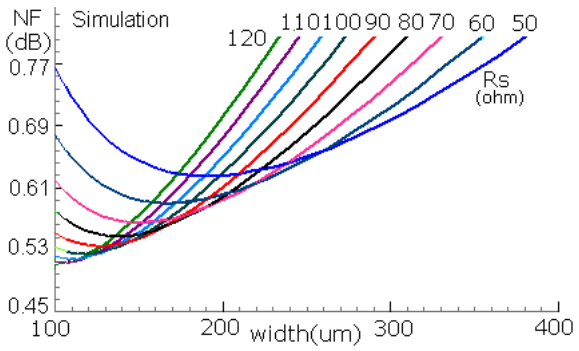

Figure 5.6: NF (sim.) vs transistor width while varying antenna resistance ($P_d = 20\,mW$)

A similar simulation with high power (I_d fixed at 58.334mA, $P_d = 70\,mW$) results in figure 5.7. This leads to a situation where the antenna resistance $R_s = 50\,\Omega$ obtains the lowest noise factor: 0.51 dB. The absolute minimum noise figures NF_{min} for $P_d = 20\,mW$ and for $P_d = 70\,mW$ are the same as depicted in figure 5.5, since the minimum noise figure is independent of the antenna resistance R_s.

Again is found that the noise difference for low and high powers is relatively small. The influence of the antenna resistance is different given a different power. For high power a small antenna resistance and for low power a high antenna resistance leads to the minimum noise figure.

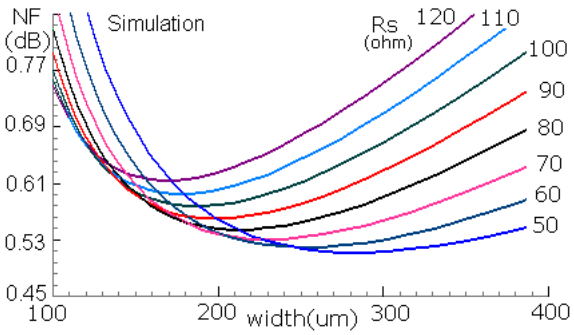

Figure 5.7: *NF* (sim.) vs transistor width while varying antenna resistance ($P_d = 70\,mW$)

5.2 Power-constrained noise optimization including B_s

In section 3.2.3 has been shown that F_{min} can be obtained with a proper choice of the transistor width and antenna inductance. Based on the same approach as described in section 5.1 a power constraint noise factor relation can be derived. While including both the antenna resistance and the source inductance, as depicted in figure 5.8, both the antenna conductance (G_s) and the antenna susceptance (B_s) will be used as described in section 3.2.2 and relation (3.17), repeated here for convenience.

$$I_m\{Y_s\} = B_s = -\frac{\omega L}{R_s^2 + \omega^2 L^2} \qquad R_e\{Y_s\} = G_s = \frac{R_s}{R_s^2 + \omega^2 L^2} \tag{5.10}$$

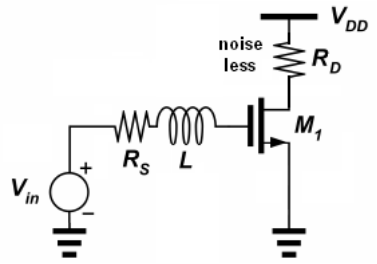

Figure 5.8: Single transistor with complex antenna source

The noise figure relation, including both power as a constraint and the relations from (5.10), becomes too difficult to give design insight. The reduced noise figure is now described by:

$$F_{P_d reduced} = 1 + \frac{\gamma P_y R_s K}{P_x}\left(\frac{\frac{R_s^2}{K^2} + \left(\omega^2 C_{gs}^2 - \frac{\omega L}{K}\right)}{\mu C_{ox} E_{sat} W}\right)\frac{\left(1 + \frac{P_x}{P_y}\right)^4}{\left(1 + \frac{P_x}{2P_y}\right)^2} \tag{5.11}$$

with L representing the antenna inductance and in which

$$K = \omega^2 L^2 + R_s^2 \tag{5.12}$$

5.2.1 Analytical calculations with R_s=50Ω

A different optimal set for every power and antenna resistance can be found. In table 5.1 the optimal sets for a standard antenna resistance of 50 Ω and a operating frequency of 11.7 GHz, are given for both the complete noise figure relation and the reduced noise figure relation.

	Complete noise figure F_{P_d}		Reduced noise figure $F_{P_d reduced}$	
Power	Width	Inductance	Width	Inductance
10 mW	289 μm	1.4 nH	200 μm	1.9 nH
20 mW	234 μm	1.8 nH	164 μm	2.4 nH
30 mW	189 μm	2.3 nH	134 μm	2.9 nH
40 mW	150 μm	2.9 nH	107 μm	3.7 nH
50 mW	115 μm	3.8 nH	84 μm	4.9 nH
60 mW	83 μm	5.3 nH	61 μm	6.8 nH
70 mW	53 μm	8.1 nH	40 μm	10.5 nH

Table 5.1: Power vs optimal design set

From these optimal sets can be seen that the difference between the two noise figures becomes smaller for higher power. The reduced noise figure, which is less complicated, can be used for rough predictions.

With the optimal design set for the complete noise figure, figure 5.9 can be derived analytically The minimum noise figure NF_{min} can also be derived to show that a noise figure equalling NF_{min} is obtained given the optimal design set. For a few of the power settings, from table 5.1, NF and NF_{min} are depicted simultaneously in figure 5.10.

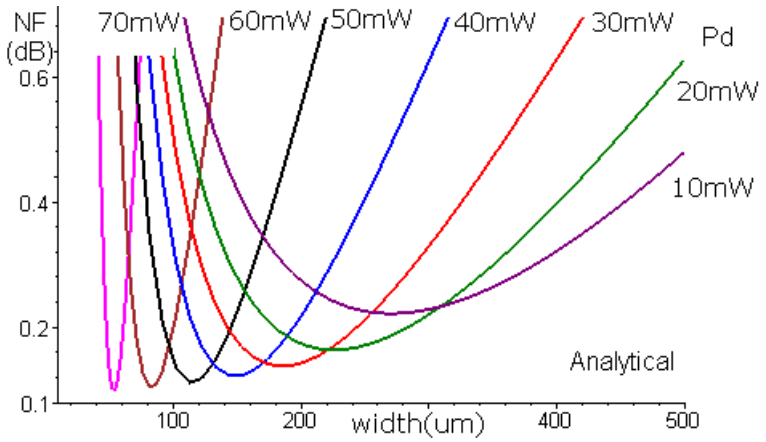

Figure 5.9: NF (analytical) versus transistor width, while varying power

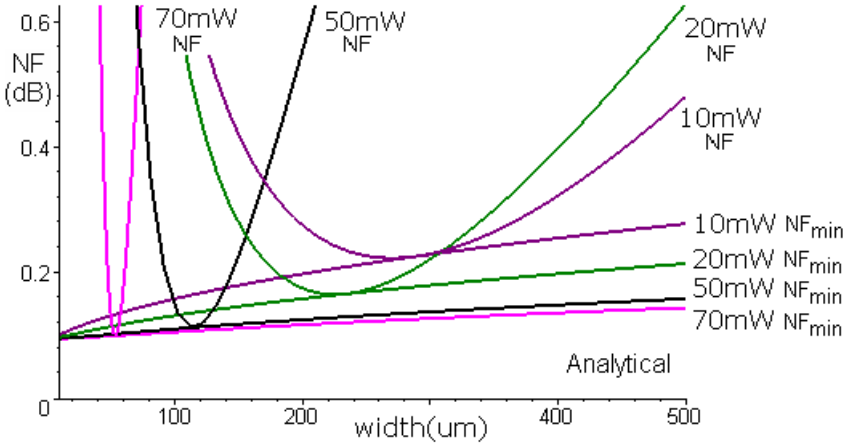

Figure 5.10: NF and NF_{min} (Analytical) versus transistor width, while varying power

From the simulations shown in figure 5.9 and 5.10 can be seen that for a high power a small transistor width and a relatively large inductance value are needed to obtain $NF{=}NF_{min}$ The noise figure is the smallest with the highest power. It can also be seen that a small change in transistor width has bigger influence on the noise figure for high powers than for low powers.

Although F_{min} was not changed due to the addition of the gate inductance it has changed by the addition of the power constraint. As can be see from figure 5.10 that the NF_{min} is the lowest for the highest power, though the absolute minimum is around 0.1 dB.

Compared with the outcomes of section 5.1.2, where the antenna impedance was purely resistive, it can be seen that a higher power now leads to a much smaller optimal transistor width and a lower noise performance.

5.2.2 Spectre simulations with R_s=50Ω

The analytical calculations with R_s=50Ω can be validated by comparison with Spectre simulations. The same circuit as from section 5.1.3 is used expanded with an antenna inductance, as depicted in figure 5.11.

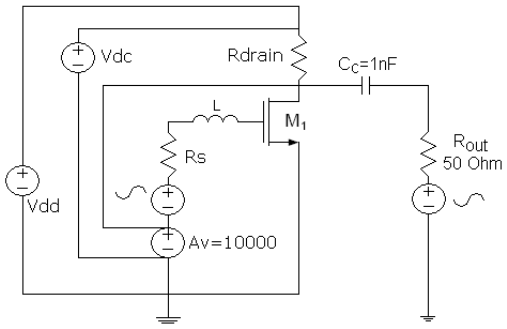

Figure 5.11: Schematic for power-constraint noise optimization including antenna inductance

First only the NF_{min} is simulated and shown in figure 5.12, from this figure can be seen that NF_{min} is increasing for very small transistor widths, especially for higher powers. When the gate inductance will be added such that $NF{=}NF_{min}$ this increase of noise figure means that for very small transistor widths the noise figure will increase as well compared to a little bigger transistor width.

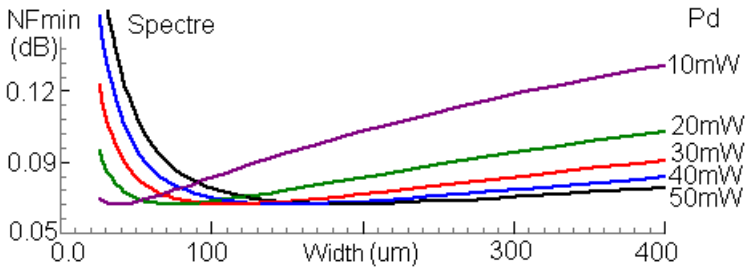

Figure 5.12: NF_{min} versus transistor width while varying power

The NF_{min} as predicted by the rho-model (analytical) did not show this change in NF_{min} for different transistor width, and is therefore not accurate enough for very small transistor widths.

In figure 5.13 the simulation results are shown for a power of 20 mW while varying the gate inductance. From this figure can be seen that adding a gate inductance will lead to a much lower noise figure. Though the change of gate inductance hardly changes the minimal noise figure (≈0.1 dB), while it does change the optimal transistor width.

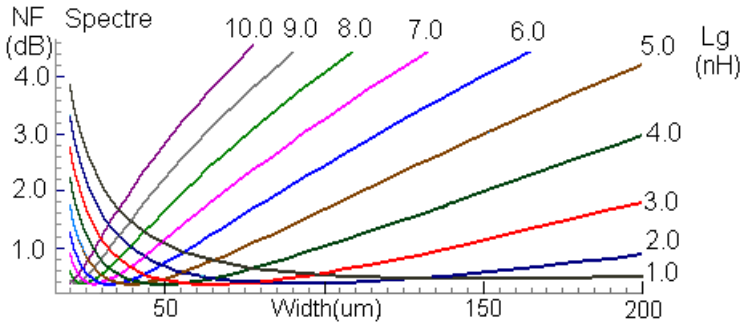

Figure 5.13: Noise figure versus transistor width while varying gate inductance

Based on the results found in this section a high power will only result in the lowest noise figure given a certain transistor width. Depending on the type of circuit optimal power can be found.

5.2.3 Analytical calculations with R_s=90Ω

In section 5.1.4 was introduced that, given a power of 20 mW, a higher antenna resistance gives a lower noise figure. Now an antenna inductance is added to the circuit the influence of a higher antenna resistance may have changed. Changing the antenna resistance to a higher value has resulted in some calculation problems. It has been found, analytically, that the highest antenna resistance that still allowed calculations was an antenna resistance of 90 Ω. Though the maximum power for this resistance was 40 mW. A higher power introduced a non existing design set (with negative component values). For the lower powers the model was able to derive a solution and the optimal transistor width and antenna inductance are summarized in table 5.2.

Power	Transistor width	Antenna inductance
10 mW	135 μm	3.1 nH
20 mW	91 μm	4.7 nH
30 mW	56 μm	7.7 nH
40 mW	26 μm	16.3 nH

Table 5.2: Power vs optimal design set

With these design sets for an antenna resistance of $R_s = 90\,\Omega$ a figure can be derived as depicted in figure 5.14. The minimal noise figure (NF_{90}) as depicted in figure 5.14 is shifted to the left compared with the minimal noise figure of the original antenna resistance of $R_s = 50\,\Omega$ (NF_{50}) as depicted in figure 5.10. The difference between NF_{50} and NF_{90} for a power of 20 mW is only 0.03 dB (0.16 dB-0.13 dB), which can be neglected.

The rho-model predicts that a standard antenna resistance will give almost the same noise figure, so it is not necessary to redesign the antenna resistance.

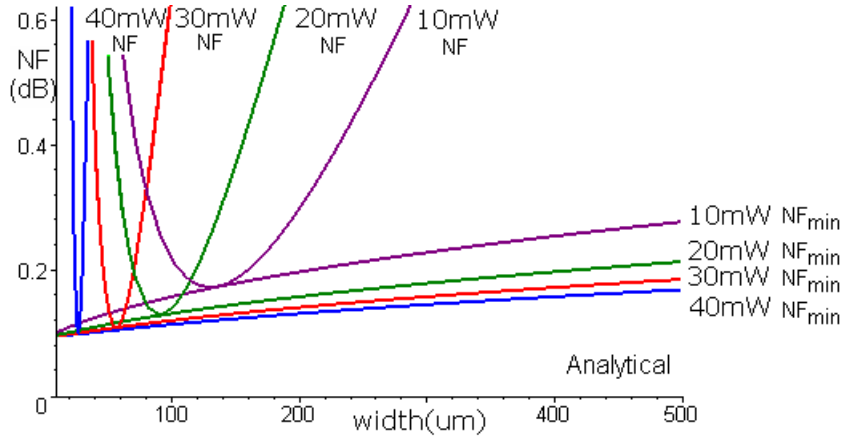

Figure 5.14: Noise figure NF and NF_{min} (analytical), while varying power ($R_s = 90\,\Omega$)

5.2.4 Spectre simulations with R_s=90Ω

The calculations from section 5.2.3 have shown that for a higher antenna resistance the optimal width given an optimal antenna inductance gets smaller.

Comparing the results from section 5.2.1 with section 5.2.2 showed that the optimal width in the simulation is much smaller than the optimal width found analytically. Simulations with an R_s=90Ω lead to optimal transistor widths so small that even for a relative small power, V_{gs} becomes higher than its supply voltage and deriving simulation results is no longer possible.

5.3 Summary

This chapter has shown that power has an influence on the noise figure of a single transistor. A higher power, together with a big transistor width, obtains a lower noise figure. Though this difference between the noise figures for different power levels is relatively small.

Adding an inductance to the antenna results in a different influence of the power and the antenna resistance. High power results in a design set with a small transistor width and a relative large inductance. Simulations have confirmed that higher power result in very small optimal transistor width when a gate inductance is introduced. For every gate inductance value a different optimal transistor width can be found.

A change of antenna resistance can also influence the noise figure. If the lowest possible noise factor is desired, changing the antenna resistance R_s to a different value can have a (relatively small) positive effect on the noise performance. The addition of a source inductance to the circuit, to obtain F_{min}, minimizes the influence of a different antenna resistance R_s even more.

Based on all the results from this chapter it has been found that increasing power can have either a positive or a negative influence on the noise figure, depending on the transistor width. Overall it is not desired to have large power consumption. A power constraint of 20mW can be used, this power is still high enough to give low noise figures and its lowest noise figure is obtained for a reasonable small transistor width (smaller than 250 μm).

Chapter 6

Low Noise Amplifier (LNA) Design

In the previous chapters the main noise sources of an LNA have been introduced and their influence has been explored. Both the analytical calculations and the Spectre simulations have shown that it is theoretically possible to obtain noise figures below 1 dB. In this chapter more low noise amplifier design issues will be considered. The first section defines the specifications of the LNA that needs to be designed. In the following sections the common design choices will be explained, in order to introduce the final design.

The in- and output parts of the LNA are omitted from all the figures, they can be found in appendix E together with more details on the simulations setup and the used analysis.

6.1 Requirements

In table 6.1 the design specifications and requirements for the CMOS low noise amplifier are summarized. An explanation of these requirements is given beneath.

Specification	Symbol	Target
Supply voltage	V_{dd}	$1.2\,V$
Available gain	G_a	$> 10\,\text{dB}$
Noise figure	NF	$<1\,\text{dB}$
Input reflection coefficient	S_{11}	$<0\,\text{dB}$
Power consumption	P_D	$\leq 20\,\text{mW}$
Frequency band	f	10.7-12.75 GHz
Reverse isolation	S_{12}	required
3rd order input interception point	IIP3	>-10 dBm

Table 6.1: LNA specifications

A gain of 10 dB is chosen as absolute minimum, based on the thesis from Araldo Kraats [13] this is the absolute minimum gain that the LNA must have to be implemented in the satellite system. The noise figure below 1 dB is needed to compete with currently available LNAs.

Power match is not absolutely required, assuming that the LNA will be implemented close enough to the antenna to overcome reflections. The input reflection coefficient S_{11} can be any value, as long as it is beneath 0 dB. When a reasonable power match can be obtained while fulfilling the requirement of a noise figure of 1 dB this is of course preferred.

The LNA will be used for satellite receiver applications, which has a frequency band, known as the Ku-band, from 10.7 GHz to 12.75 GHz. The LNA must fulfill the specifications for this frequency band.

A power constraint of 20 mW is chosen since in chapter 5 was found that, for a single common source transistor with large transistor width, a higher power resulted in only slightly better noise performance. High power consumption is often not desired and neither is a large transistor width. A choice has been made to have a power constraint of 20 mW for the final circuit. This power is still high enough to give low noise figures and its lowest noise figure is obtained for a reasonable small transistor width (smaller than 250 μm).

The reverse isolation of an LNA determines the amount of LO signal that leaks from the output (mixer) to the antenna. This leakage arises from capacitive paths, substrate coupling etc (Miller effect). Insufficient isolation can cause feedback and even instability. The reverse isolation is characterized by the reverse transducer gain power $|S_{12}|^2$.

Both gain variation and group delay variation are not considered as requirements, they can be digitally corrected since the LNA will be designed for a completely new (digital) environment.

6.2 Circuit Design

A common source (CS) transistor has been used to model the LNA. Unfortunately an LNA is in practise not as simple as a common source transistor, and it can not fulfill the design specifications. In the following sections the chosen LNA design, fitting the specifications, will be introduced and explained with the help of the theory from the previous chapters.

6.2.1 Antenna inductance as gate inductance

As has been introduced in section 3.2.2 adding a series inductance to the antenna source makes it possible to obtain F_{min} or at least to lower the noise factor. It is difficult to change the antenna impedance, easier is to add an inductance to the LNA as a gate inductance. In figure 6.1 this gate inductance L_g is shown together with a common source stage with resistive load, referred to as CS+LG+RD.

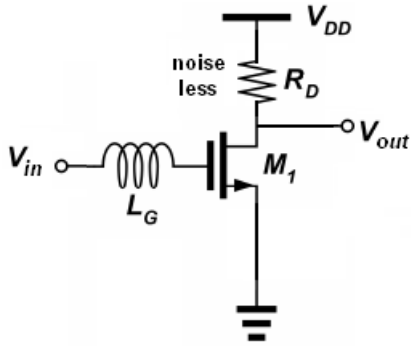

Figure 6.1: Common source transistor with gate inductance (CS+LG+RD)

This gate inductance can have a similar effect as an antenna inductance: it allows to obtain F_{min}, as long as the inductance is properly chosen.

The gate inductance L_g further sets the oscillation frequency. It must be said that a situation can be found where the oscillation peak is not at the center-frequency (11.7 GHz) of the frequency band, though the overall noise factor is lower, as represented in figure 6.2. The situation with overall lower noise (lowest line) is a better choice given the current design specification. So the addition of L_g will be used to lower the noise figure in the entire frequency band instead of only at the center of the frequency band.

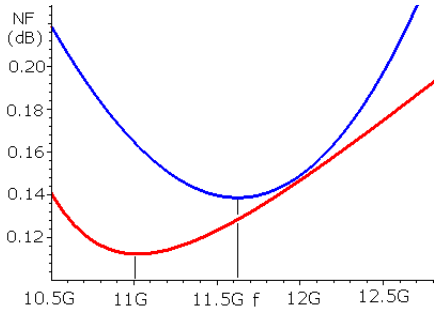

Figure 6.2: Noise figure example for different resonance frequencies

6.2.2 Source degeneration

With an inductance added to the source and to the gate of the transistor, as depicted in figure 6.3, power match can be obtained. This type of circuit, referred to as CS+LG+LS+RD, has been investigated by A. van der Ziel [10] and it is explained in more detail in appendix B.2.

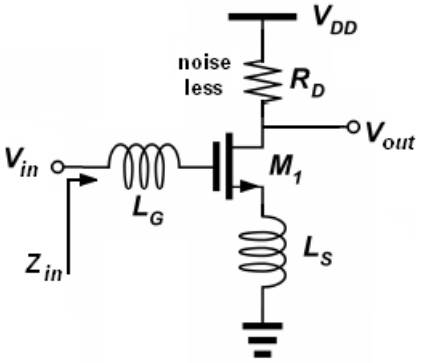

Figure 6.3: Narrowband LNA, biasing not shown (CS+LG+LS+RD)

The susceptance B_s, for a single MOS transistor, to obtain F_{min} (noise match) equals the susceptance B_{opt} as was given by:

$$B_{opt} = -B_c = \omega C_{gs}\Big(1 - \frac{g_m}{g_{d0}}|c|\sqrt{\frac{\delta}{5\gamma}}\Big) \tag{6.1}$$

while the susceptance B_s to obtain power match, with the source degeneration circuit as depicted in figure 6.3 must be:

$$B_s = \frac{1}{X_s} = \frac{1}{-j\omega(L_s + L_g)} = \omega C_{gs} \tag{6.2}$$

Unless the second term of B_{opt} is zero, power match and noise match will not occur simultaneously. Fortunately it was found that the gate noise contribution was relatively small indicating that the second term of B_{opt}, including the gate noise term δ, will be very small. The difference between B_{opt} and B_s is therefore also very small, resulting in almost similar noise figures for the single transistor and the source degenerated transistor [4][5][6].

In the design for the required CMOS LNA, is assumed that the LNA is mounted close enough to the antenna, eliminating the need for input impedance matching. It is therefore not obligatory to implement L_s. Simulations, as presented in the next chapter, will determine if the additional L_s can be used to obtain the lowest or nearly lowest noise factor while at the same time obtaining a reasonable power match ($S_{11} < 10\,\text{dB}$), referred to as n+p match.

6.2.3 Single-ended LNA

Completing the design requires a bias and an output circuitry. A typical single-ended LNA with bias circuit is depicted in figure 6.4.a. The cascode transistor M_2 reduces the Miller effect, improves the reverse isolation, and controls the drain voltage of M_1 and the output conductance.

The drain inductance L_d instead of a drain resistance ensures a high gain at the output. An additional capacitance at the output can be used to create resonance at the center frequency. The M_{bias} transistor forms a current mirror with M_1, the transistor width of M_{bias} is very small to minimize the power overhead in this bias circuit.

The current through M_{bias} can be set by R_c in conjunction with the V_{gs} of M_1. Resistance R_{bias} is chosen large enough to be able to ignore its current noise contribution but also to ensure a high impedance bias path for the AC-input signals.

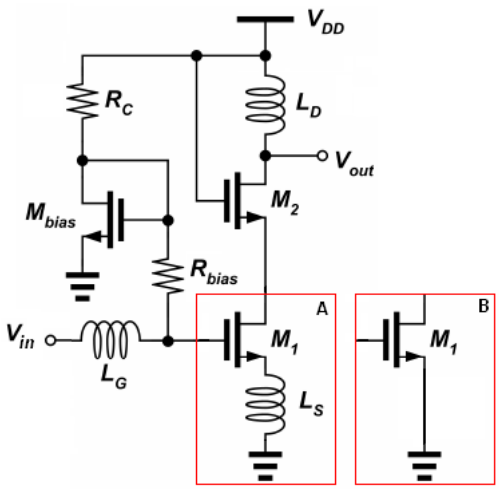

Figure 6.4: Single ended LNA with and without source degeneration

The circuit as depicted above can be described by CS+CASC+LG+LS+LD when the source inductance is included and as CS+CASC+LG+LD when the source inductance is not included. From now on, the term CASC for the cascode transistor and LD for the inductive load will no longer be specified.

6.3 Influences on the noise factor

Adding the extra components including the bias circuit will introduce a negative effect on the noise performance and most likely also on the transistor width obtaining the lowest NF. The addition of the components is needed to be able to fulfil all the design requirements though.

The noise contribution of the bias circuit can be calculated when the bias transistor is considered a simple small signal resistor $1/g_{m_{bias}}$ in parallel with R_c. Assuming that R_c is much bigger than $1/gm_{bias}$, resistance R_c may be neglected. The current noise due to the bias transistor can be calculated, in worst case conditions (power match), by:

$$i^2_{M_{bias}} = \frac{4KT\frac{1}{g_{m_{bias}}}}{(1/g_{m_{bias}} + R_{bias} + \frac{R_s}{2})^2} \tag{6.3}$$

R_{bias} and R_s are large and therefore the current noise of the bias transistor may be neglected. The current noise contributed to the LNA by R_{bias} is in worst case conditions (power match):

$$i^2_{R_{bias}} = \frac{4KTR_{bias}}{(1/gm_{bias} + R_{bias} + \frac{R_s}{2})^2} \approx \frac{4KT}{R_{bias}} \tag{6.4}$$

Showing that R_{bias} should be large enough to neglect its noise contribution.

The main extra noise contribution will come from the inductances L_g and L_s. An ideal inductor will be lossless and noiseless irrespective of the amount of current flowing through the winding. Unfortunate inductors have winding resistance and substrate losses. This resistance appears as a resistance in series with the inductor, the series resistance. Electrical current flowing through the coil will be converted into heat due to this resistance. Causing a loss of inductive quality.

6.3.1 Q factor

The quality factor (or Q) of an inductor is the ratio of its inductive reactance to its resistance at a given frequency and is a measure of its efficiency, as is given in relation (6.5) in which L now represents the inductance value. A high Q factor approaches the behavior of an ideal, lossless, inductor.

$$Q = \frac{\omega L}{R_L} \tag{6.5}$$

Using inductances with a high quality factor will minimize the additional noise contributing effects. In simulations it is possible to include the parasitic noise influences of the inductances, though another option would be to add resistances to the circuit representing the noise contribution from the inductances as is done in figure 6.5.

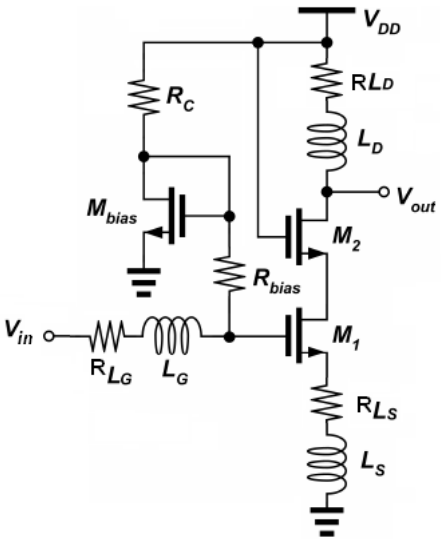

Figure 6.5: Single ended LNA including parasitics (CS+LG+LS)

The resistance values for R_{Ld}, R_{Lg} and R_{Ls} are determined with relation (6.5) for the center frequency of 11.7 GHz. This high frequency causes the resistances to be relatively large compared to LNAs designed for lower frequencies. This high frequency makes it difficult to design an LNA with low noise performance.

The analytical model has not included the quality factor of the inductances, which makes the model less accurate with respect to the simulations. In chapter 9, a more advanced noise model will be shown, including the quality factor.

6.4 Bias circuit for simulations

The bias circuitry, as introduced in section 6.2.3 sets the V_{gs} of M_1. When not all component values are known it is not advised to simulate the circuit with this type of bias circuitry. For the simulations an ideal voltage source will be used, fixing the drain current for the given power constraint, as represented in figure 6.6. This bias circuitry changes the V_{gs} automatically to obtain a fixed power during simulation, by setting V_{ref}=I_{ref}=$16,667mV$ a fixed power of 20 mW is obtained. This bias circuit does not contain any noise contributing components and is therefore noiseless.

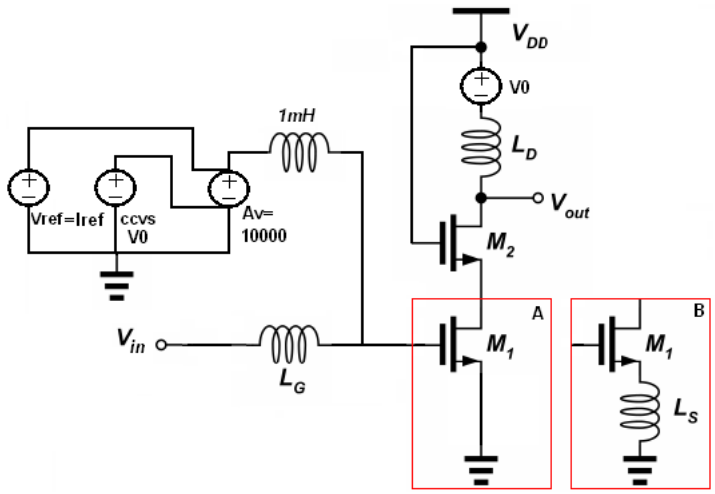

Figure 6.6: LNA with and without source degeneration, including ideal bias circuit

Although is has been shown in section 6.3 that the noise contribution of the bias circuit can be neglected, a small difference between the noise performance of both bias circuits can be expected. When the final design is known the current through M_1 will determine the component values for the bias circuit and the bias circuit can be implemented in the final design.

The circuits with the bias circuit used for simulations will be referred to as CS, CS+LG and CS+LG+LS, after implementing the practical bias circuit they are referred to as CS+B, CS+LG+B and CS+LG+LS+B.

6.5 Summary

This chapter has introduced a circuit with inductive source degeneration for power match. It has been explained that when the LNA will be placed close enough to the antenna, noise match is more important than power match and therefore it is not obligatory to implement a source inductance L_s. Though if a circuit design can be found that obtains the minimal or near minimal noise figure while at the same time obtaining a reasonable power match (S_{11} < 10 dB), implementing L_s is preferred.

The single-ended LNA design is introduced in which a cascode transistor is implemented to increase the gain and reduce the interaction of the tuned output with the tuned input.

The losses of the inductances are explained using the quality factor. The high frequency causes the parasitic losses to be of a reasonable size, which makes it more difficult to obtain a low noise performance. Lastly the bias circuit as used for simulations has been shown.

Chapter 7

Simulations with the LNA design

In chapter 3 its has been explained, and in chapter 4 it has been verified that there exists, for a common source transistor LNA with a fixed antenna resistance, an optimal transistor width to obtain the best noise performance. In this chapter the optimal transistor width, for the design as was introduced in chapter 6, will be determined with Spectre simulations. The circuit will be simulated with two different antenna resistances, both with and without the source and gate inductance, to show the influence of these inductances on the optimal width. If not specified differently the simulations are done for a frequency of 11.7 GHz.

7.1 Common source + cascode transistor

The LNA circuit that is used as first is depicted in figure 7.1 (CS) with Q=∞. The used bias circuit is the one as given in figure 6.6, which was designed such that a fixed power of 20 mW is obtained as explained in section 6.1. The input and output parts of the LNA circuit are still omitted from the figures; they can be found in appendix E. The antenna resistance was varied from 50 Ω to 150 Ω in the simulations.

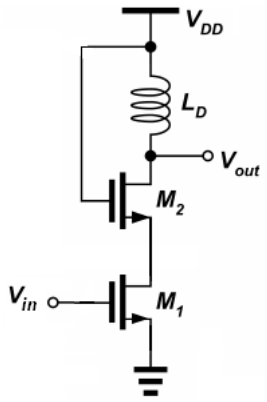

Figure 7.1: Common source + Cascode with inductive load, bias circuit not shown

From the simulation results, as depicted in figure 7.2 it can be found that for the standard antenna resistance of 50 Ω and Q=∞, the lowest noise figure of about 0.80 dB, for a transistor width of 190 μm. The lowest noise figure of about 0.70 dB is obtained for an antenna resistance of 100 Ω. Simulations with both antenna resistances, $R_s = 50\,\Omega$ and $R_s = 100\,\Omega$, will be done for the entire circuit, to compare their noise figures. Expected is, as was also found in section 5.2.3, that the change of antenna resistance will only have a small influence on the noise figure, if at all.

This simulation result is similar to the results shown in chapter 5 figure 5.6. There is a small difference in the optimal width given a certain antenna resistance, caused by the addition of the cascode transistor.

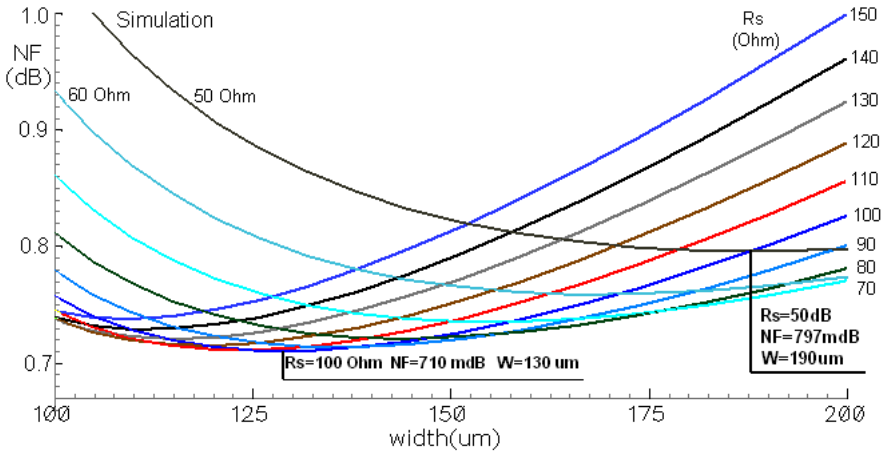

Figure 7.2: Noise figure versus transistor width while varying antenna resistance

A noise summary, as given in table 7.1 for a transistor width of 190 μm and an $R_s = 50\,\Omega$, shows the noise contributing parts. It can be seen that the thermal noise of M_1 is still the main noise contributing part. The thermal noise of M_2 has far more influence than the induced gate noise of M_1, which again shows that gate noise may be neglected.

Parameter	Description	Noise contribution	% of total
r_n of input	input port noise	$7.7672 * 10^{-18}$	78.63
S_{th} of M_1	thermal noise	$1.3998 * 10^{-18}$	14.17
r_n of output	output port noise	$5.46511 * 10^{-19}$	5.53
S_{th} of M_2	thermal noise	$1.7717 * 10^{-19}$	1.80
S_{fl} of M_1	flicker noise	$1.4634 * 10^{-20}$	0.15
S_{ig} of M_1	induced gate noise	$1.969 * 10^{-21}$	0.08
S_{fl} of M_2	flicker noise	$3.3653 * 10^{-21}$	0.02
S_{ig} of M_2	induced gate noise	$1.6857 * 10^{-22}$	0.00

Table 7.1: Noise summary from Spectre of cascode stage with $R_s = 50\,\Omega$

$$F = \frac{TON - r_n \texttt{ of output}}{r_n \texttt{ of input}} = \frac{9.8778 * 10^{-18} - 5.4651 * 10^{-19}}{7.7672 * 10^{-19}} = 1.202 \tag{7.1}$$

A noise factor of 1.202 equals a noise figure of 0.80 dB, as was also found from the simulation represented in figure 7.2.

Both the noise figures NF and NF_{min} for the CS circuit from section 5.1.3 and the CS+CASC circuit just presented are depicted in figure 7.3. Due to the addition of the second transistor (M_2) the noise figure has increased by about 0.16 dB compared with the noise figure results from section 5.1.3.

The minimum noise figure NF_{min} of the LNA has also changed due to the addition of the cascode transistor. The NF_{min} given a transistor width of 190 μm varies between 0.2 dB at 10.7 GHz and 0.26 dB at 12.75 GHz. A larger transistor width leads to a higher NF_{min}.

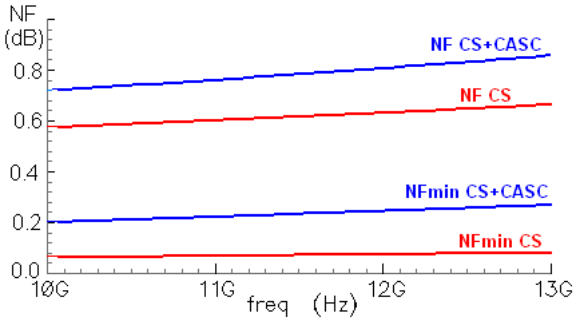

Figure 7.3: Noise figure versus frequency given an antenna resistance $R_s = 50\,\Omega$

7.2 LNA design with $R_s = 50\,\Omega$

The previous section introduced that for an antenna resistance of $R_s = 50\,\Omega$ the optimal width to obtain the lowest noise figure was $190\,\mu$m. This dimension was found for the CS circuit. The next step is to add both gate and source inductances to investigate their influence.

Earlier simulations where done having an infinite Q factor, as was explained in section 6.3 this is not realistic. With the currently available technology a Q factor of 10 is feasible. With this Q factor the inductance resistance can be described as a function of the center frequency and the inductance: $R_L = 0.1\omega L$, in which L represents the inductance.

First a simulation is done, only with inductance $L_d = 2\,nH$ and its parasitics (CS). It was found that the parasitics of L_d has hardly any influence on the noise figure. The lowest noise figure of 0.82 dB, was obtained for a transistor width of $190\,\mu$m. This is almost the same noise figure as was found in section 7.1: NF=0.80 dB.

While including the gate inductance L_g as shown in figure 7.4 block B (CS+LG), with a finite Q factor of 10, it is difficult to obtain a reasonable low noise figure. The noise contribution of the parasitics is quite large. The lowest noise figure of 0.75 dB at the center frequency of 11.7 GHz was found using a gate inductance of $L_g = 300\,pH$ and a transistor width of $190\,\mu$m. This is only 70m dB less than without the gate inductance (0.82 dB for CS)

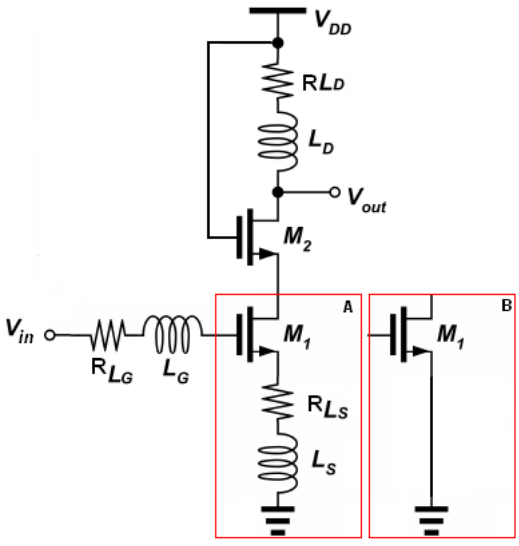

Figure 7.4: CS+LS+LG, bias circuit not shown

With the addition of the source inductance L_s as shown in figure 7.4 block A (CS+LG+LS), will increase the noise figure and obtains a reasonable power match S_{11} <10 dB, referred to as n+p match, . For a gate inductance $L_g = 600\,pH$ and a source inductance $L_s = 100\,pH$ a noise figure of 0.81 dB was obtained (at 11.7 GHz) with an input reflection coefficient S_{11} below -10 dB, for the entire frequency band. This was the optimal setting to obtain reasonable power match and simultaneously a low noise figure.

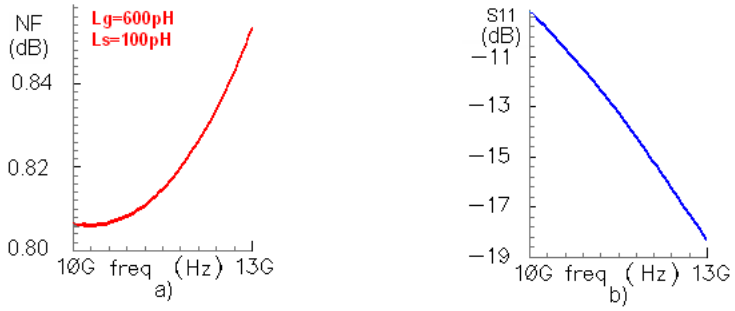

Figure 7.5: a) Noise figure and b) S_{11} versus frequency for n+p match

Both the noise figure and the input reflection coefficient S_{11}, of he CS+LG+LS circuit, are represented in figure 7.5.a and 7.5.b respectively. The noise figure of 0.81 dB at 11.7 GHz is similar to the noise figure of 0.82 dB at 11.7 GHz as was found for the circuit CS without the gate and source inductances, with as difference that now also a reasonable power match has been obtained.

Simulations have also been done with only the source inductance (CS+LS). This did not lead to a lower noise figure given the specified frequency band, nor did it lead to power matching. The combination of both the gate and the source inductance makes a low noise figure together with a reasonable power match possible.

7.2.1 Gain and S-parameters

For the circuit for n+p match circuit, CS+LG+LS Q=10, the available gain (G_a), the transfer gain (G_t), and two of the remaining S-parameters have been simulated. The results are as depicted in figure 7.6.

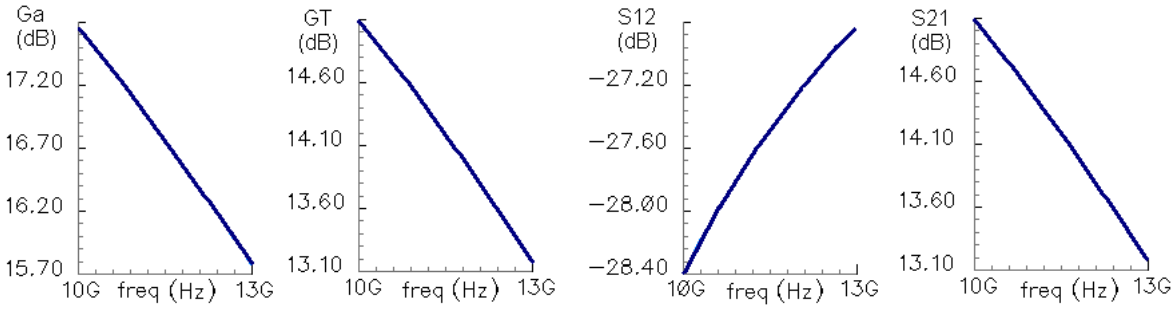

Figure 7.6: Simulation results, for noise match design ($R_s = 50\,\Omega$)

It can be seen that the available gain is according to the design specifications. Furthermore the transducer gain is the same as the forward transmission coefficient (S_{21}), as is expected (for LNAs). The reverse transmission coefficient (S_{12}) is also very good.

7.2.2 Summary for $R_s = 50\,\Omega$

In table 7.2 the simulation results, based on an antenna resistance of 50 Ω, are given. The noise figure is given for the center frequency of 11.7 GHz. For both S_{11} and S_{21} the worst case, for the entire frequency band, is given.

Circuit type	$Width$	L_g	L_s	NF	NF_{min}	S_{11}	S_{21}
CS Q=∞	190 μm	-	-	0.80 dB	0.24 dB	<-0.6 dB	>15.4 dB
CS Q=10	190 μm	-	-	0.82 dB	0.24 dB	<-0.7 dB	>14.9 dB
CS+LS Q=10	200 μm	-	100 pH	0.79 dB	0.33 dB	<-4.3 dB	>12.3 dB
CS+LG Q=10	190 μm	300 pH	-	0.75 dB	0.55 dB	<-1.5 dB	>16.4 dB
CS+LG+LS Q=10	190 μm	600 pH	100 pH	0.81 dB	0.75 dB	<-10. dB	>13.4 dB

Table 7.2: Results summary of LNA simulations with $R_s = 50\,\Omega$

In the analytical model the gate inductance was added as an ideal source inductance. The NF_{min} simulated is determined for the entire circuit including the inductance and its losses, therefore the minimal noise figure NF_{min} has increased.

The CS+LG design with Q=10 is the best choice if the lowest noise performance is desired. Though the CS+LG+LS design with Q=10 is better if a low noise figure and a reasonable power match (n+p match) are desired.

7.3 LNA with $R_s = 100\,\Omega$

Similar simulations as done in the previous sections have been done for this section. This time for an antenna resistance of 90 Ω. It was found in section 7.1 that this antenna resistance resulted in the lowest possible noise figure. If not specified differently the simulations are performed at 11.7 GHz and a power of 20 mW is used as constraint.

The simulations that need to be done for given the antenna resistance $R_s = 100\,\Omega$ are the same as for the antenna resistance $R_s = 50\,\Omega$. Except the gain and S-parameters for the n+p match design the simulation results will be summarized in section 7.3.2.

7.3.1 Gain and S-parameters

For the CS+LG+LS design with Q=10 a noise figure of 0.80 dB has been found for a transistor width of only 130 μm. For this design, the available gain (G_a), the transfer gain (G_t), and two S-parameters have been simulated as well. The results are depicted in figure 7.7.

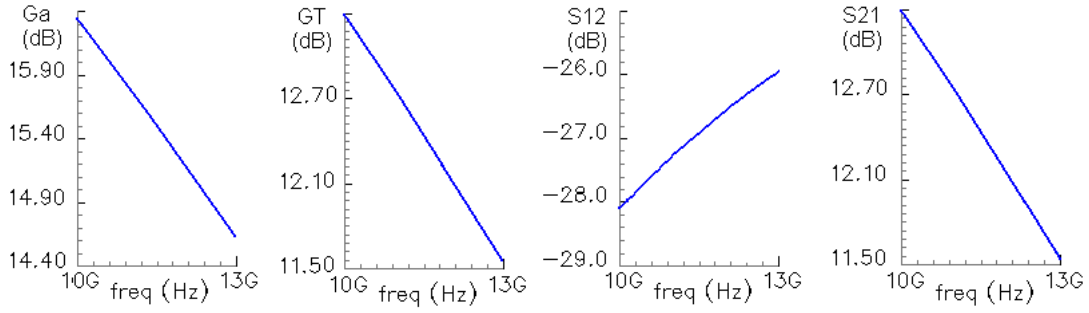

Figure 7.7: Simulation results, for noise match design ($R_s = 100\,\Omega$)

Again can be seen that the available gain is according to the design specifications. The transfer gain is the same as the forward transmission coefficient (S_{21}), as expected, and the reverse transmission coefficient (S_{12}) is very good.

The noise figure of the CS+LG+LS design with Q=10 is almost the same compared to the same design with a standard antenna resistance of 50 Ω.

7.3.2 Summary for $R_s = 100\,\Omega$

In table 7.3 the simulation results, with an antenna resistance of 100 Ω, are tabulated. The noise figure is given for the center frequency of 11.7 GHz. For both S_{11} and S_{21} the worst case, for the entire frequency band, is given. The CS+LG design with Q=10 is the best choice if the lowest noise performance is desired, this design also has the highest S_{21} value.

Circuit type	$Width$	L_g	L_s	NF	NF_{min}	S_{11}	S_{21}
CS Q=∞	130 μm	-	-	0.71 dB	0.22 dB	<-0.3 dB	>15.4 dB
CS Q=10	135 μm	-	-	0.74 dB	0.22 dB	<-0.4 dB	>15.0 dB
CS+LG Q=10	130 μm	450 pH	-	0.71 dB	0.53 dB	<-1.0 dB	>15.8 dB
CS+LG+LS Q=10	130 μm	1 nH	200 pH	0.79 dB	0.78 dB	<-10 dB	>11.7 dB

Table 7.3: Results summary of LNA simulations with $R_s = 100\,\Omega$

7.4 Noise match versus power match

One remaining question is if indeed a lower noise figure can be obtained when using the noise match method instead of a good power match method [4][5][6]. Based on the outcomes of section 7.2 simulations will be done with both the antenna resistance of 50 Ω and 100 Ω.

The power match description from appendix B.2 and the inductively-degenerated LNA including the Q factor (CS+LG+LS) is used. To start with a good power match method it is necessary to choose a transistor width. Any width may be chosen though for now the optimal width, as found in section 7.1, will be used. The rho-model gives an estimate of the C_{gs} that is needed to calculate both L_s and L_g. After some initial simulations, good power match values for the inductances have been found and the circuit has been simulated.

Both the results for the n+p match and for a good power match with an antenna resistance of 50 Ω are given in table 7.4.

Circuit	R_s	$Width$	L_g	L_s	NF	NF_{min}	S_{11}	S_{21}
n+p match	50 Ω	190 μm	600 pH	100 pH	0.81 dB	0.75 dB	<-10 dB	>13.4 dB
power match	50 Ω	190 μm	900 pH	140 pH	0.98 dB	0.88 dB	<-20 dB	>12.3 dB

Table 7.4: Design parameters and reflection coefficients for n+p match and power match

Both the noise figure and the input reflection coefficient, for a good power match and for a reasonable power match (n+p match) as was already described in section 7.2 are plotted in figure 7.8a and b, indicated with the term power match and n+p match.

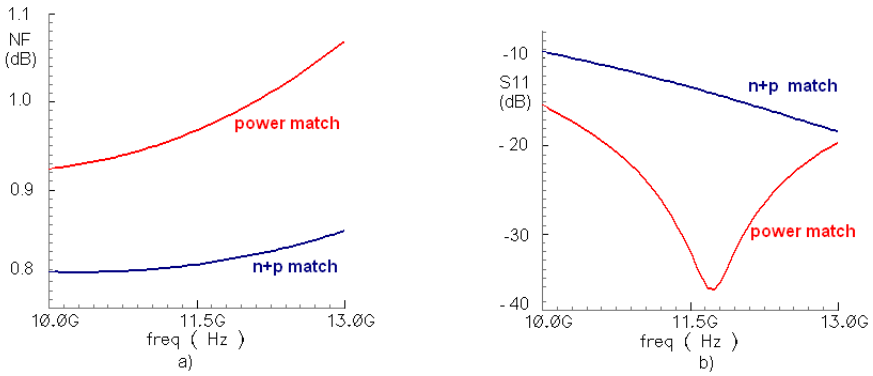

Figure 7.8: Noise figure and S_{11} for R_s=50 Ω, P_D=20 mW

From figure 7.8.a can be seen that the noise figure for the n+p match method is at least 0.10 dB lower than for a good power match method, due to the need of a much bigger gate inductance. In figure 7.8.b the input reflection coefficient is shown and indeed a good power match method gives a much lower S_{11}, especially at the center frequency.

For an antenna resistance of 100 Ω both the results of the n+p match and for a good power match are given in table 7.5.

Circuit	R_s	$Width$	L_g	L_s	NF	NF_{min}	S_{11}	S_{21}
n+p match	100 Ω	130 μm	1 nH	200 pH	0.79 dB	0.78 dB	<-10 dB	>11.7 dB
power match	100 Ω	130 μm	2 nH	375 pH	1.20 dB	1.05 dB	<-20 dB	> 8.0 dB

Table 7.5: Design parameters, noise figure and reflection coefficients for n+p match and power match

Both the noise figure and the input reflection coefficient, for good power match and for a reasonable power match (n+p match) as found in section 7.3 are plotted in figure 7.9a and b, indicated with the term power match and n+p match.

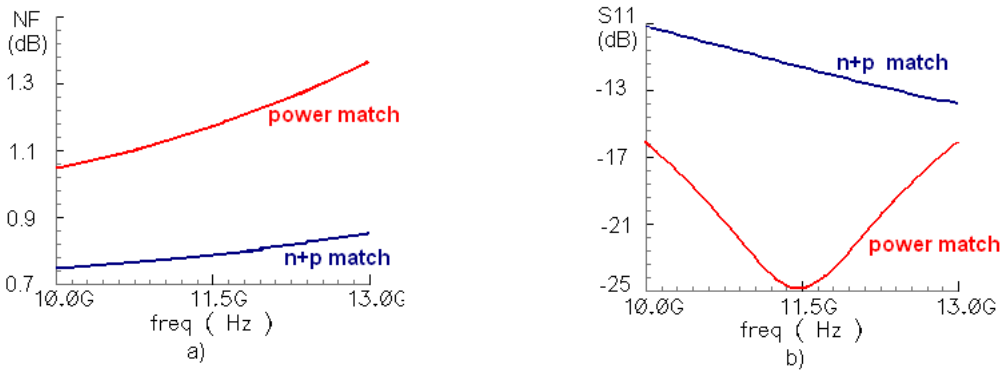

Figure 7.9: Noise figure and S_{11} for R_s=100 Ω, P_D=20 mW

From figure 7.9.a can be seen that the noise figure for the n+p match method is at least 0.25 dB lower than for a good power match method, due to the need of a much bigger gate inductance. In figure 7.9.b the input reflection coefficient is shown and indeed a good power match method gives a much lower S_{11}, especially at the center frequency.

Comparing the results in table 7.5 with those in table 7.4 shows that an antenna resistance of 50 Ω gives the best noise figure results given a good power match design.

The noise figure of an LNA for satellite receivers must be as low as possible. Therefore the noise match method with an antenna resistance of 50 Ω is better especially since the LNA can be mounted close to the antenna so the impedance match does not need to be very good. The chosen width for the power match method was the same as for the noise match approach, any other width would give another (worst) noise performance.

7.5 Final design including practical bias circuit

For both the n+p noise match method and a good power match method the ideal bias circuit as described in section 6.4 was used. The circuit as depicted in figure 7.10, with the practical bias circuit designed such that the power is set to 20 mW, is used for the next simulations.

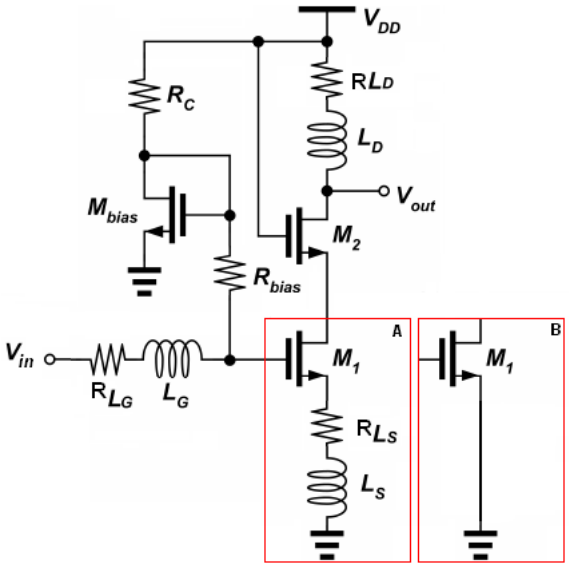

Figure 7.10: Block A) CS+LG+LS+B and Block B) CS+LG+B

The following four circuits, together with an antenna resistance of R_s=50Ω, will be simulated:
A) basic CS+B Q=∞;
B) noise match CS+LG+B Q=10;
C) n+p match CS+LG+LS+B Q=10;
D) good power match CS+LG+LS+B Q=10.

For these circuits the component values, as depicted in table 7.6, have been found to obtain the best performance. The final simulation results are depicted in table 7.7. The noise figure is given at three different frequencies and for S_{11} and S_{21} the worst case, for the entire frequency band, is given.

Circuit	R_s	$M_{1,2}$	M_{bias}	L_d	L_g	L_s	R_c	R_{bias}
A	50Ω	255 μm	20 μm	2 nH	-	-	290 Ω	20 kΩ
B	50Ω	190 μm	20 μm	2 nH	400 pH	-	190 Ω	20 kΩ
C	50Ω	190 μm	20 μm	2 nH	600 pH	100 pH	165 Ω	20 kΩ
D	50Ω	190 μm	20 μm	2 nH	900 pH	140 pH	155 Ω	20 kΩ

Table 7.6: Used component values per circuit ($R_s = 50\Omega$)

Circuit	10.7 GHz		11.7 GHz		12.7 GHz		S_{11}	S_{21}
	NF	NF_{min}	NF	NF_{min}	NF	NF_{min}		
A	0.80 dB	0.30 dB	0.87 dB	0.32 dB	0.91 dB	0.34 dB	<-0.9 dB	>14.1 dB
B	0.76 dB	0.59 dB	0.77 dB	0.65 dB	0.79 dB	0.69 dB	<-1.9 dB	>16.6 dB
C	0.83 dB	0.71 dB	0.84 dB	0.77 dB	0.86 dB	0.83 dB	<-11 dB	>13.3 dB
D	0.96 dB	0.84 dB	1.05 dB	0.91 dB	1.07 dB	0.97 dB	<-20 dB	>12.3 dB

Table 7.7: Simulation results per circuit ($R_s = 50\Omega$)

The noise figure of circuit C has increased from 0.81 dB to 0.84 dB at 11.7 GHz due to the noise of the bias circuit. The noise summary of circuit type C, depicted in table 7.8, shows that only the bias resistance R_{bias} of the entire bias circuit contributes to the output noise. The thermal noise of the non-ideal gate inductance is the main noise source.

Parameter	Description	Noise contribution	% of total
r_n of input	input port noise	$5.07696{*}10^{-18}$	76.0
r_n of output	output port noise	$5.18873{*}10^{-19}$	7.77
r_n of R_{lg}	resistance noise	$4.47642{*}10^{-19}$	6.71
S_{th} of M_1	thermal noise	$3.82936{*}10^{-19}$	5.74
S_{th} of M_2	thermal noise	$1.37743{*}10^{-19}$	2.06
r_n of R_{ls}	inductance loss	$7.03976{*}10^{-20}$	1.05
r_n of R_{bias}	resistance noise	$2.47949{*}10^{-20}$	0.37
r_n of R_{ld}	inductance loss	$1.746 *10^{-20}$	0.26
S_{ig} of M_1	induced gate noise	$1.08253{*}10^{-20}$	0.16
S_{fl} of M_1	flicker noise	$3.94132{*}10^{-21}$	0.06
S_{fl} of M_2	flicker noise	$1.47634{*}10^{-21}$	0.02
S_{ig} of M_2	induced gate noise	$3.50692{*}10^{-22}$	0.01

Table 7.8: Noise summary of Spectre for circuit B ($R_s = 50\,\Omega$)

The n+p match design (circuit C) has also been designed and simulated for a power of 10 mW and 30 mW to verify that a choice of 20 mW is sensible. It has been found that the noise factor of an optimized design is nearly independent of power dissipation. A power constraint of 20 mW is therefore indeed sensible

All four circuits obtain a noise figure near the critical 1 dB. Unfortunately more parasitics need to be included, which will be explained and simulated in the next chapter.

7.6 Summary

Only a small improvement in noise figure is reached by using a gate inductance due to its parasitic resistance. For a small amount of extra noise a reasonable power match can be obtained when both a gate inductance and a source inductance are added to the circuit.

Initially a higher antenna resistance, given a power constraint of 20 mW, resulted in a lower noise figure, though completing the design shows that a standard source antenna of 50 Ω gives the same noise performance.

It has been found that the noise match circuit CS+LG+B reaches the lowest noise figure, smaller than 0.8 dB for the entire frequency band. Though by accepting a slightly higher noise figure of 0.9 dB, a reasonable power match can be obtained. For a good power match the noise

figure is again slightly higher but still smaller than 1.1 dB for the entire frequency band. Based on the given specifications the noise match circuit is the best option.

The power constraint of 20 mW is a good choice. The noise factor of an optimized design is nearly independent of power dissipation.

All the found results are summarized in table 7.9. The noise figure is given at the center frequency of 11.7 GHz, and for S_{11} and S_{21} the worst case for the entire frequency band is given. If not specified otherwise a Q factor of 10 has been used. The last four circuits represent the circuits from section 7.5 that will be further investigated with additional noise sources:

A) basic CS+B Q=∞;
B) noise match CS+LG+B Q=10;
C) n+p match CS+LG+LS+B Q=10;
D) good power match CS+LG+LS+B Q=10;

Noise match design								
Circuit type	R_s	$Width$	L_g	L_s	NF	NF_{min}	S_{11}	S_{21}
CS Q=∞	50 Ω	190 μm	-	-	0.80 dB	0.24 dB	<-0.6 dB	>15.4 dB
CS	50 Ω	190 μm	-	-	0.82 dB	0.24 dB	<-0.7 dB	>14.9 dB
CS+LG	50 Ω	190 μm	300 pH	-	0.75 dB	0.55 dB	<-1.5 dB	>16.4 dB
CS Q=∞	100 Ω	130 μm	-	-	0.71 dB	0.22 dB	<-0.3 dB	>15.4 dB
CS	100 Ω	130 μm	-	-	0.74 dB	0.22 dB	<-0.4 dB	>15.0 dB
CS+LG	100 Ω	130 μm	450 pH	-	0.71 dB	0.53 dB	<-1.0 dB	>15.8 dB
N+P match design								
CS+LG+LS	50 Ω	190 μm	600 pH	100 pH	0.81 dB	0.75 dB	<-10 dB	>13.4 dB
CS+LG+LS	100 Ω	130 μm	1 nH	200 pH	0.79 dB	0.78 dB	<-10 dB	>11.7 dB
Exact power match design								
CS+LG+LS	50 Ω	190 μm	900 pH	140 pH	0.98 dB	0.88 dB	<-20 dB	>12.3 dB
CS+LG+LS	100 Ω	130 μm	2 nH	375 pH	1.20 dB	1.05 dB	<-20 dB	> 8.0 dB
Final four designs including practical bias circuit								
Circuit type	R_s	$Width$	L_g	L_s	NF	NF_{min}	S_{11}	S_{21}
A	50 Ω	255 μm	-	-	0.87 dB	0.325 dB	<-0.9 dB	>14.1 dB
B	50 Ω	190 μm	400 pH	-	0.77 dB	0.65 dB	<-1.9 dB	>16.6 dB
C	50 Ω	190 μm	600 pH	100 pH	0.84 dB	0.77 dB	<-11 dB	>13.3 dB
D	50 Ω	190 μm	900 pH	140 pH	1.05 dB	0.91 dB	<-20 dB	>12.3 dB

Table 7.9: Summary of simulations results

Chapter 8

Simulations with additional noise sources

The two most important noise sources, the gate and drain noise source, have been discussed. For most situations the use of only these noise sources is sufficient to predict the noise performance of the entire circuit. For the ultra low noise application in satellite receivers these two sources have been made as low as possible. As a result the contribution of other noise sources to the noise figure can become significant. Two additional noise sources are associated with the poly gate resistance and the noise due to the resistive substrate R_b. Both these sources will be explained and methods for minimization will be given.

8.1 Poly gate resistance

Thermal noise is also added by the poly sillicon gate section of a MOSFET. In figure 8.1 the gate, source and drain resistivity are illustrated. For a relatively wide transistor, the source and drain resistance can be neglected, whereas the gate distributed resistance becomes noticeable (see Behzad Razavi [3]) as noise of the LNA.

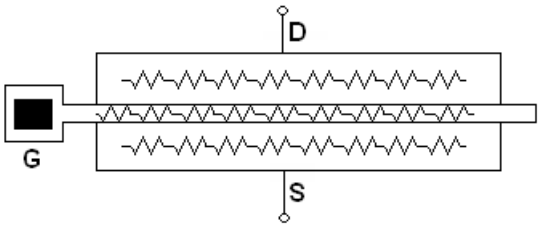

Figure 8.1: Single ended LNA

The gate electrode of currently used MOSFET technologies is made of polysilicon. Its resistivity is relatively high which may cause a noise contribution exceeding the channel noise. This noise source is modelled as a voltage source in series with the gate and has a noise power equal to:

$$\overline{v_g^2} = 4kTR_g\Delta f \tag{8.1}$$

The gate resistance R_g is given by:

$$R_g = \frac{KR_{\square}W}{n^2L} \tag{8.2}$$

Where $R_{\square}$ represents the sheet resistance of the gate material, W is the width of the device, L the gate length and n the number of gate fingers. The factor K is found to be 1/3 when each gate finger is contacted only at one end, and can be reduced to 1/12 when each gate finger is contacted at both ends [4][15].

Both the length and the width of the gate are determined by the process and the design approach. This leaves three methods to minimize the noise contribution of the gate:

1) Using a gate material that has a very low sheet resistance $R_{\square}$,
2) Contacting each gate finger at both ends to reduce the K factor
3) Using a multi-fingered structure to obtain a large n value.

Using the transistor dimensions of section 7.2 and contacting the gate fingers at both ends the expected gate resistance will be in the form of:

$$R_g = \frac{\frac{1}{12}R_{\square}W}{n^2L} \tag{8.3}$$

The number of gate fingers still needs to be set. A commonly used finger width is a width between $2\,\mu$m and $3\,\mu$m. Resulting in 71 fingers of $2.5\,\mu$m when the transistor width is around $190\,\mu$m. Resulting in a gate resistance of:

$$R_g = \frac{\frac{1}{12}\cdot 11\cdot 190 * 10^{-6}}{71^2\cdot 60nm} = 0.58\,\Omega \tag{8.4}$$

This is a small resistance and thus a small noise contribution. From this can be concluded that the gate resistance may be neglected when a reasonable folding factor is used.

8.2 Bulk resistance

The determination of the bulk resistance is more complicated than for the gate resistance. The image depicted in figure 8.2 shows two additional resistances: R_{bl} and R_{bv}.

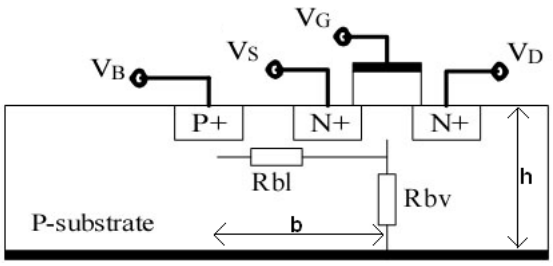

Figure 8.2: Bulk resistance in a NMOS transistor

The lumped resistance R_{bl} represents the equivalent distributed resistance between the bulk contact and the point underneath the channel. R_{bv} represents the equivalent resistance between this point under the channel and bottom substrate contact. They are given by:

$$R_{bl} = R_{\rho}\frac{b}{W\cdot h} \tag{8.5}$$

and

$$R_{bv} = R_{\rho}\frac{h}{W\cdot L} \tag{8.6}$$

where R_{ρ} is the substrate resistivity, b the distance between the gate and the bulk contact, h the thickness of the substrate and W and L the transistor width and length respectively. The small transistor length (60nm), needed in relation (8.6), causes R_{bv} to be much larger than R_{bl}. Due to the parallel relation between them the contributing effect of R_{bl} is very small and may therefore be neglected.

The parameters (R_ρ, b, L) in the expression of R_{bl} are all related to the used CMOS process. At first it seems that it is not possible to reduce the noise contribution of the bulk resistance. Though when double bulk contacts will be used in each transistor, as depicted in figure 8.3, the bulk resistance will be reduced by half. Another horizontal resistance appears due to the addition of the second bulk contact. The two bulk resistances are connected in parallel and its equivalent resistance is therefore half of its original value for a single bulk contact.

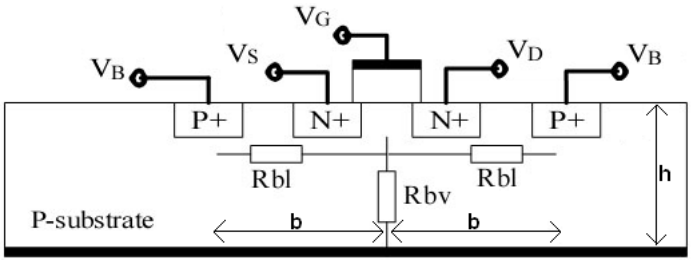

Figure 8.3: Bulk resistance in a double bulk NMOS transistor

8.3 Simulations with RF-library including ideal bias circuit

A more advanced transistor library for Spectre came recently available. In this RF library the discussed additional noise sources are readily included, which will make the simulation results even more accurate. The bulk resistance can easily be reduced by the use of a double bulk region, as was described in section 8.2. This is a simulation setting that is included in the RF-library of the transistor. The simulations in this section will be done with the bias circuit as was given in section 6.4. The poly gate resistance can be reduced with the folding factor. The noise performance influence of the folding factor will be shown next.

8.3.1 Folding to reduce the poly gate resistance

As described in section 8.1 the use of a multi-fingered structure lowers the influence of the poly gate resistance. The amount of gate fingers can be varied with the folding factor. A finger width of 2.5 μm is not uncommon.

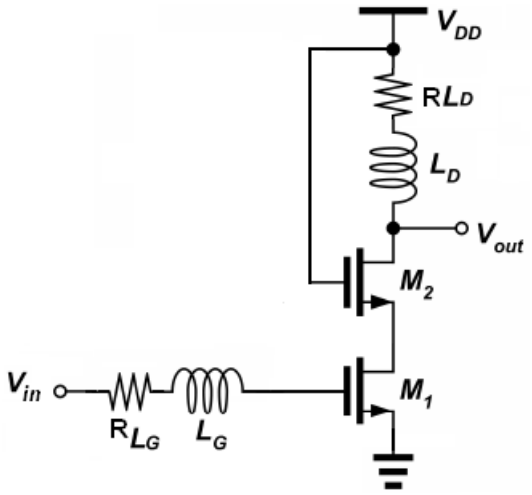

Figure 8.4: LNA with gate inductance (CS+LG)(bias circuit not shown)

Simulations are done with the circuit CS+LG, as depicted in figure 8.4, with Q=10 (using the ideal bias circuit given in section 6.4 and a gate inductance of 400pH as found in section 7.5.

In figure 8.5 simulations results are shown for different folding factors. It can be seen that a larger folding factor will reduce the noise figure. The difference between a folding factor of 50 and 100 is much bigger than between 100 and 150. The poly gate resistance is already that small for a fold of 100 that a higher fold will not make the poly gate resistance much smaller. It can be seen that folding factors larger than about 100 do not improve the noise performance much further.

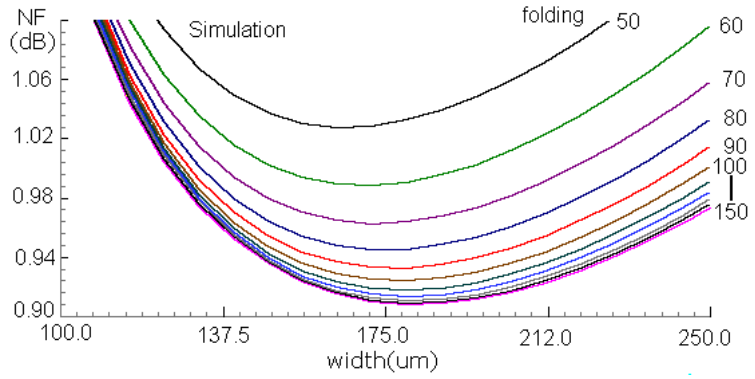

Figure 8.5: Noise figure versus frequency while varying the folding factor ($L_g = 400\,pH$)

8.4 Simulations with RF-library including practical bias circuit

In section 7.5 has been shown that the use of the practical bias circuit, instead of the ideal bias circuit, hardly had any influence on the noise figure. It is expected that this will still be the case with the RF-library.

8.4.1 CS+LG+B circuit

The CS+LG noise match circuit, with a gate inductance L_g of400 pH and a folding of 100, is simulated with the practical bias circuit (CS+LG+B). A noise figure NF between 0.92 dB and 0.97 dB and a NF_{min} between 0.75 dB and 0.88 dB, over the frequency band, is found for a transistor width of 190 μm.

Circuit	R_s	$W_{M_{1,2}}$	$W_{M_{bias}}$	Fold	L_d	L_g	L_s	R_c	R_{bias}
	50Ω	190 μm	20 μm	100	2 nH	400 pH	-	175 Ω	20 kΩ
CS+LG+B Q=10	NF		NF_{min}		S_{11}			S_{21}	
	0.92-0.97 dB		0.75-0.88 dB		<-1.6 dB			>16.5 dB	

Table 8.1: Design parameters and simulation results for noise match design

The noise figure is about 0.1 dB higher than was found in section 7.5. From the noise summary presented in table 8.2 can be seen that the bias circuit contributes 0.28 % of the entire noise. The noise summary also shows the contribution of r_g, r_{bulk} and r_{well}. These resistances, although very small, contribute to the difference between the noise found in this section and in section 7.5. One of the main noise contributors is the noise of the gate inductance.

Parameter	Description	Noise contribution	% of total
r_n of output	output port noise	$1.00758 * 10^{-17}$	77.4
S_{th} of M_1	thermal noise	$1.19054 * 10^{-18}$	9.15
r_n of R_{Lg}	inductance loss	$5.92263 * 10^{-19}$	4.55
r_n of input	input port noise	$4.93221 * 10^{-19}$	3.79
S_{th} of M_2	thermal noise	$2.12196 * 10^{-19}$	1.63
r_{well} of M_1	well noise	$1.81025 * 10^{-19}$	1.39
r_n of $r_g M_1$	gate loss	$1.74904 * 10^{-19}$	1.34
r_n of R_{bias}	resistance loss	$3.67751 * 10^{-20}$	0.28
r_g of M_2	gate loss	$1.86864 * 10^{-20}$	0.14
r_n of R_{Ld}	resistance loss	$1.65976 * 10^{-20}$	0.13
S_{ig} of M_1	induced gate noise	$1.56204 * 10^{-20}$	0.12
S_{fl} of M_1	flicker noise	$1.22392 * 10^{-20}$	0.09
r_{bulk} of M_1	well noise	$1.12999 * 10^{-20}$	0.09
r_n of M_2	resistance loss	$8.54097 * 10^{-21}$	0.07
S_{fl} of M_2	flicker noise	$2.2687 * 10^{-21}$	0.02
r_{bulk} of M_2	resistance loss	$9.81157 * 10^{-22}$	0.01
S_{ig} of M_2	induced gate noise	$3.20058 * 10^{-22}$	0.00
r_{jund} of M_1	resistance loss	$2.0992 * 10^{-22}$	0.00
r_{jund} of M_2	resistance loss	$9.6378 * 10^{-23}$	0.00
r_{junds} of M_1	resistance loss	$8.24891 * 10^{-23}$	0.00

Table 8.2: Noise summary from Spectre of CS+LG+B ($R_s = 50\,\Omega$)

The RF-library also shows the induced gate noise of M_2, r_{jund} and r_{juns}, though the noise contribution of these sources is that small that their noise contribution is almost zero.

8.4.2 CS+LG+LS+B circuit

The next step is to add the source inductance L_s and do some simulations with this circuit CS+LG+LS+B with a quality factor of 10 and continuing with a folding factor of 100. The S-parameter S_{11} must be below -10 dB for a reasonable power match design; this was only possible by adjusting both the source inductance and the gate inductance.

The circuit CS+LG+LS+B with Q=10 is simulated both for n+p match and a good power match with the practical bias circuit. The following table lists the optimal design parameters given a 20 mW power dissipation constraint.

Circuit type	R_s	$M_{1,2}$	M_{bias}	Fold	L_d	L_g	L_s	R_c	R_{bias}
n+p match	$50\,\Omega$	$190\,\mu$m	$20\,\mu$m	100	2 nH	600 pH	100 pH	$155\,\Omega$	$20\,k\Omega$
power match	$50\,\Omega$	$190\,\mu$m	$20\,\mu$m	100	2 nH	925 pH	180 pH	$140\,\Omega$	$20\,k\Omega$

Table 8.3: Design parameters for n+p match and a good power match

In figure 8.6.a and b the noise figure NF and NF_{min} for both circuits are shown and figure 8.6.b and c show both S_{11} and S_{21}. The noise difference between the two circuits is very small, varying from a difference of 0.1 dB at 10.7 GHz to a difference of 0.3dB at 12.75 GHz. A summary of these figures is given in table 8.4.

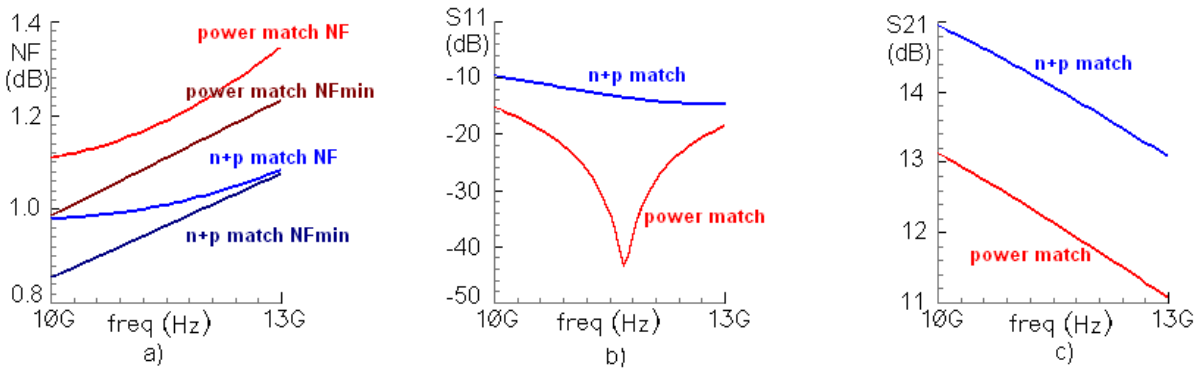

Figure 8.6: a) NF and NF_{min}, b) S_{11} c) S_{21} all versus frequency

Circuit	NF	NF_{min}	S_{11}	S_{21}
n+p match	0.95 dB	0.90 dB	<-10 dB	>13.5 dB
power match	1.20 dB	1.10 dB	<-20 dB	>11.5 dB

Table 8.4: Noise figure and reflection coefficients for n+p match and power match

Despite the effort of trying to find the lowest possible noise figure, the noise figure for the n+p match design is similar to the standard power match design [8]. Indicating that when the optimal transistor width is used, given the antenna resistance, a good power match can lead to a near optimal noise figure.

8.4.3 Power gain

The transducer power gain G_T, which was already shown as the forward transmission coefficient, is shown in figure 8.7 together with the operating power gain G_P and the available power gain G_A. It can be seen that for both circuits the G_T and G_P are very close, indicating that the input match is good. G_A is not very close to G_T since there is no output match.

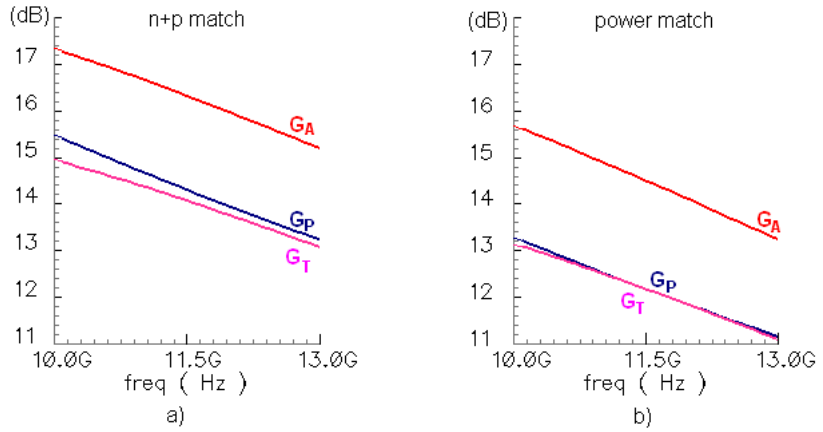

Figure 8.7: a) n+p match b) power match gain results versus frequency

The gain for the n+p match design is slightly higher compared to a good power match design.

8.4.4 Voltage gain

If both the input and the output are perfectly matched the voltage gain is 6 dB larger as the transducer power gain (S_{21}). Though in the current designs the output has not been matched to the 50Ω load and the voltage gain needs to be determined differently. For both the n+p match and a good power match the voltage gain has been simulated with an infinitely high load resistance. Resulting in a voltage gain as depicted in figure 8.8. It can be seen that the voltage gain of the n+p match design is higher than that of the power match design.

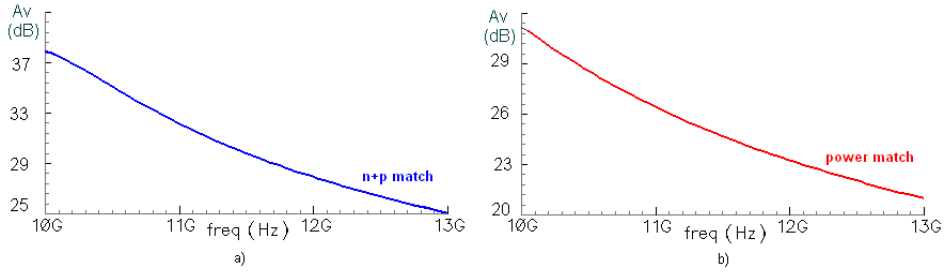

Figure 8.8: a) n+p match b) power match voltage gain results, versus frequency

8.4.5 IIP2 and IIP3

Linearity is also important in the design of a low noise amplifier. Intermodulation distortion (IMD) is a measure of the linearity of amplifiers. The 2^{nd} and 3^{th}-order intercept points (IP2 and IP3) are figures of merit for these specifications and allow distortion products to be computed for various signal amplitudes.

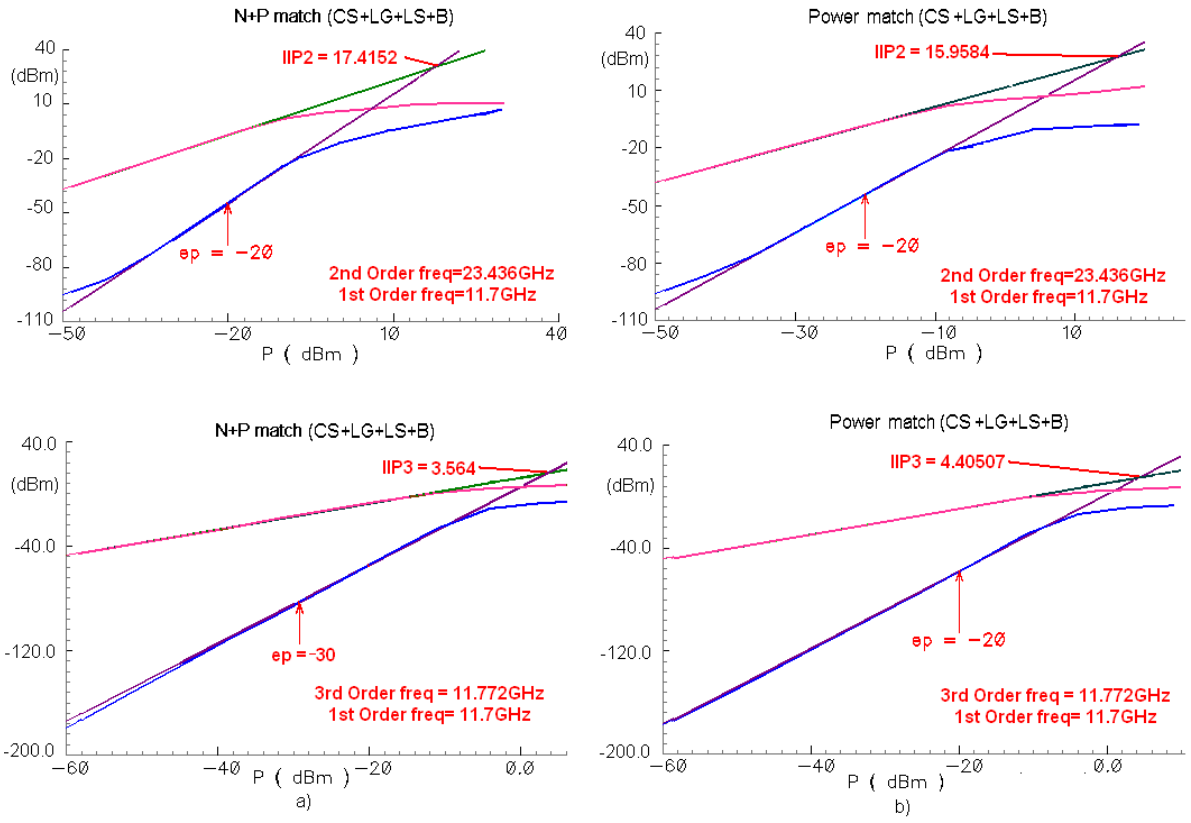

Figure 8.9: IIP2 and IIP3 a) for n+p match and b) for a good power match

A way of measuring the intermodulation intercept point, is by feeding two signals with a small frequency difference into the device-under-test (as described in appendix E.2.3). For both the n+p match and a good power match circuits from the previous section (table 8.3) the IIP2 and the IIP3 have been simulated and their results are depicted in figure 8.9.

8.5 Summary

Simulations with a more advanced RF-transistor library, which includes more noise sources showed that the poly gate resistance can be minimized by using a folding factor and by contacting each gate finger at both ends. The bulk resistance can be minimized by the use of a double bulk contact.

The practical bias circuit introduced only a small amount of additional noise compared with the noise introduced by all the other noise sources. Despite the effort to minimize the noise contribution of all the noise source a noise figure much lower than 1 dB is not obtained.

The noise match design is the only design which noise figure is below 1 dB, though both the n+p match and a good power match circuits obtain a noise figure near 1 dB while fulfilling the rest of the specifications, including the gain and linearity.

Chapter 9

Possible improvements

The LNA that has been designed, CS+LG+LS+B either for n+p match or power match, has a noise figure of near 1dB. It has been seen that it is impossible to obtain a much lower noise figure given the circumstances. The high frequency is one of the main difficulties in the design, as it causes the inductance losses to be relatively large. In the following section improvements on the design and on the model will be described. Both can be part of further research, perhaps with an even smaller transistor length (45nm).

9.1 Q-factor

Simulations that include a gate inductance have shown that a gate inductance which has a Q=10 can only lower the noise figure with a small amount compared with the circuit that has no gate inductance, CS. Due to the high frequency the parasitic resistance of the inductances is relatively high, especially of the gate inductance L_g. A higher Q factor can increase the noise performance, since it minimizes the parasitic resistances.

To show the influence of the Q factor, simulations for a varying Q factor will be done with the circuit as depicted in figure 9.1 (CS+LG+LS+B) and with the results found in section 8.4.2, with the RF-library.

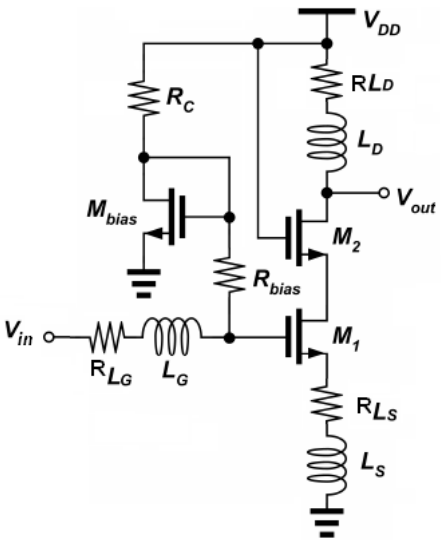

Figure 9.1: LNA with gate inductance (CS+LG+B)

The simulation results are depicted in figure 9.2, they show that a higher Q factor decreases the noise figure, as was expected. The difference between Q=10 and Q=24 is almost 0.3dB. The noise figure for the CS+B circuit (without the gate and source inductance and with infinite Q factor for the drain inductance), is depicted by the straight line.

From these simulations can be concluded that a Q factor higher than 10 is needed to obtain a noise figure below 1 dB. From figure 9.2 can also be seen that the addition of the gate and source inductance will only lower the noise figure, compared to a single CS+B circuit, when the quality factor is sufficiently large.

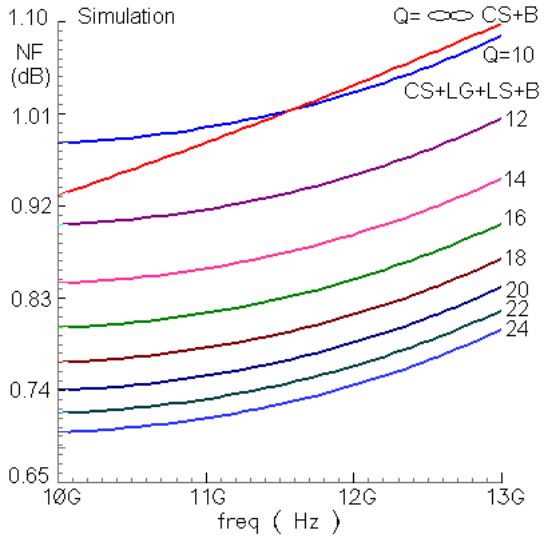

Figure 9.2: Noise figure versus frequency, while varying Q, (L_g=400 pH)

The used component values are summarized in table 9.1

Circuit type	$M_{1,2}$	M_{bias}	Fold	L_d	L_g	L_s	R_c	R_{bias}
CS+B Q=∞	225 μm	20 μm	100	2 nH	-	-	225 Ω	20 $k\Omega$
CS+LG+LS+B	190 μm	20 μm	100	2 nH	600 pH	100 pH	155 Ω	20 $k\Omega$

Table 9.1: Design parameters for n+p match circuit

NF_{min} has also been simulated for the single transistor CS+B Q=∞ circuit and found to be between 0.47 dB and 0.57 dB over the frequency band. This indicates that it is not possible, given the current topology, to obtain a noise figure lower than 0.5 dB. Due to the additional parasitics, also included in the RF-library such r_{well}, it is very difficult to reach F_{min} even with an infinite Q.

9.2 Model improvements

The used rho-model is relatively simple which makes it a nice model to work with. Though a difference in optimal transistor width has been found in section 4.2 comparing the rho-model calculations with the Spectre simulations. In chapter 7 has been found that the simulation results of the circuits that include the quality factor Q=10 for the gate inductance and include the additional noise sources are very different compared with the model. The model became less accurate for the more advanced circuit.

In the following sections a possible explanation for the transistor width difference and a short introduction to a more enhanced model will be given.

9.2.1 Layout parasitics

In chapter 4.2 a difference in optimal width was found, while comparing the analytical results with the simulations results. Based on the reduced noise factor $F_{reduced}$, as given in section 3.1.3, an optimal width was found:

$$W_{opt} \approx \frac{3}{2}\frac{1}{wLC_{ox}R_s} \tag{9.1}$$

As introduced in section 4.2 the transistor length, the antenna resistance and the operation frequency are design parameters and they are equal for both the analytical calculations and the Spectre simulations. This gives an indication that the value for C_{ox} is most likely to be incorrect, despite the found match in section 4.1.

For the rho-model C_{ox} can be determined by:

$$C_{ox} = \frac{3}{2}\frac{C_{gs}}{WL} \tag{9.2}$$

It was found in chapter 4 that C_{ox} is about $11\,\mathrm{mF/m^2}$, which was verified PROMOST. Assumed was that the Spectre simulations where done with MOS-Model-11, though it turned out that a more advanced model was used, including some additional layout parasitics. This model, the baseline model, includes three additional capacitance: C_1, C_2 and C_3. To incorporate these capacitances in the current model the value for C_{ox} becomes:

$$C_{ox} = \frac{C_{complete}}{WL} \tag{9.3}$$

With the use of the circuit as depicted in figure 9.3, it was possible to simulate the input impedance Z_{in} of a single common source transistor.

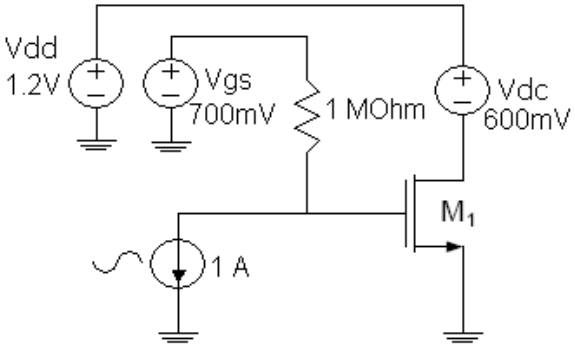

Figure 9.3: Simulation circuit to determine Z_{in} of a single transistor

With the input impedance Z_{in}, the complete transistor capacitance can be derived by:

$$C_{complete} = \frac{1}{\omega|Z_{in}|} \tag{9.4}$$

For a frequency of 1MHz it was found that $Z_{in} = 633\,k\Omega$, thus $C_{complete}$=250 fF. Resulting in a C_{ox} of about $22\,\mathrm{mF/m^2}$, which is exactly twice as large as the previously used C_{ox}. This calculation is only valid in the case of a common source transistor, with source, drain and bulk connected to ac ground.

In figure 9.4.a the analytical results, with the adjusted C_{ox} of 22 mF/m^2, are given and in 9.4.b the simulation results. It can be seen that the optimal width is now in the range of the optimal width found by simulations.

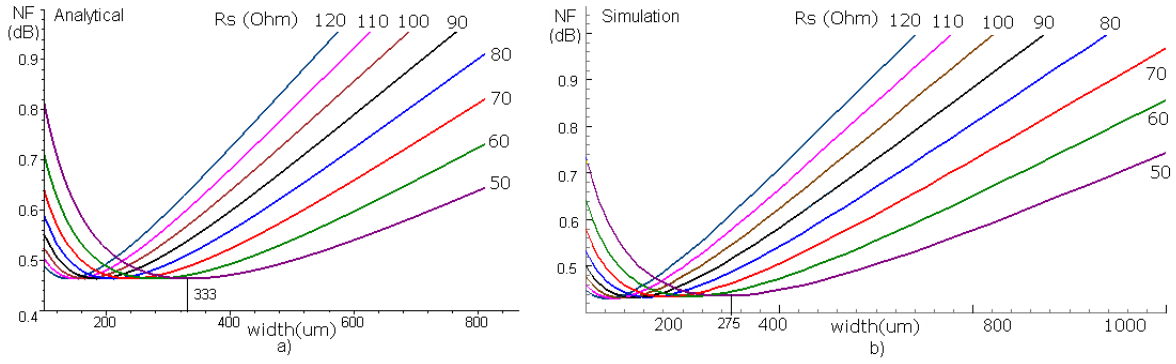

Figure 9.4: Noise figure versus transistor width, while varying R_s

In chapter 5 power constraint noise optimization has been introduced. With the adjusted value for C_{ox} a similar calculation as in section 3.1.3 is done and compared with the simulation results from section 5.1.3 as depicted in figure 9.7.a and 9.7.b respectively.

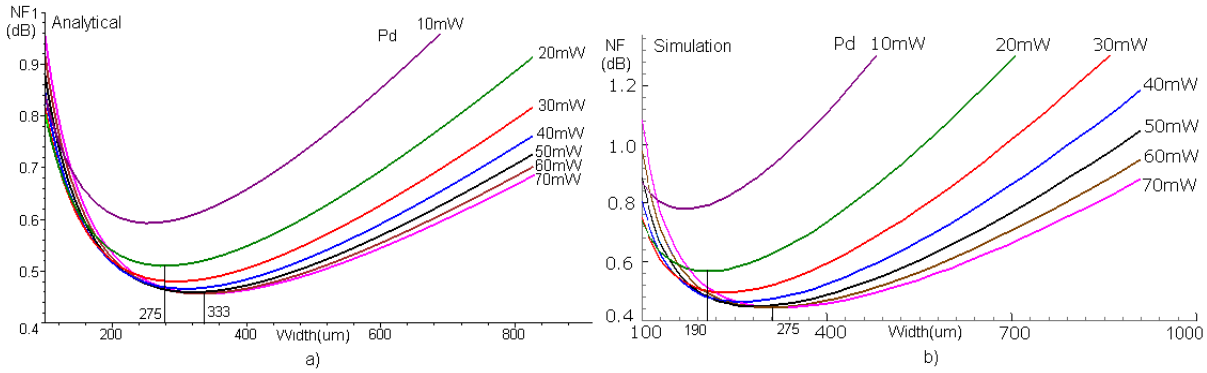

Figure 9.5: a) Analytical *NF* and b) Simulated *NF* vs transistor width, while varying P_d

Again can be seen that the results are very similar, and that the optimal width as predicted by the calculations is now very close to the optimal width found by simulations.

Though, unfortunately it is not this simple. The rho-model is not designed with these parasitics and multiplying C_{ox} by two in the model will cause a difference in g_m vs V_{gs} with MOS-model 11. The transconductance g_m is, in terms of the rho-model, expressed as:

$$g_m = \Big(\frac{1+\frac{\rho}{2}}{(1+\rho)^2}\Big)\mu C_{ox} W \rho E_{sat} = \alpha \mu C_{ox} W \rho E_{sat}, \tag{9.5}$$

As can be seen from this relation, the difference in g_m can be overcome by using half of the original value of the mobility factor μ, making g_m vs V_{gs} fit again. The change of μ will than again influence the noise figure performance as can be seen from figure 9.6.a. which is derived for calculations with the adjusted C_{ox} and $\mu/2$.

From figure 9.6 can be seen that the optimal width is still in the range of the optimal width found by simulations though the noise figure has increased (note: different y-axes) in the new situation and is now higher than the noise figure found by simulations.

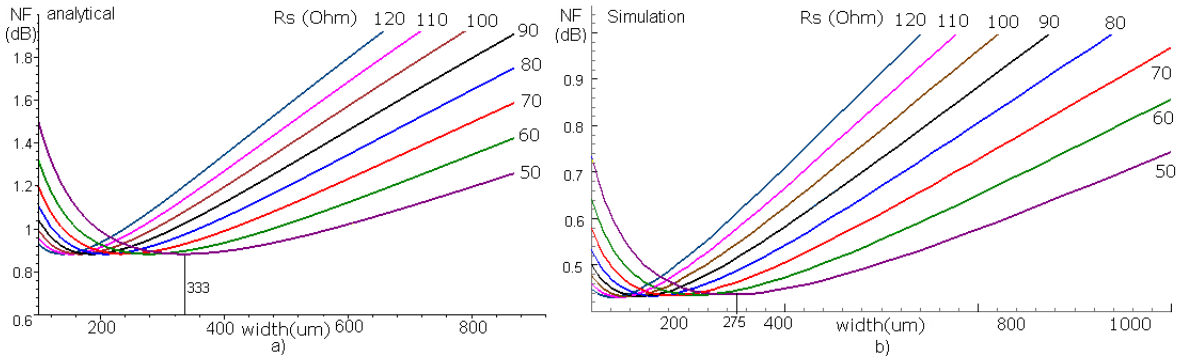

Figure 9.6: Noise figure versus transistor width, while varying R_s

For the power constraint optimization a difference in optimal power will also occur as can be seen from 9.7.a.

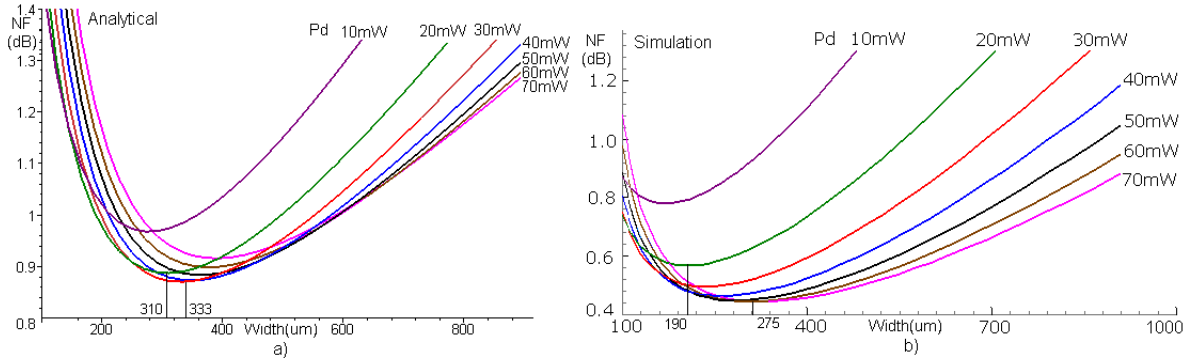

Figure 9.7: a) Analytical NF and b) Simulation NF vs transistor width, while varying P_d

With the original C_{ox} and μ it was found that for both the analytical and the simulation results a power dissipation of P_d=60 mW gives the lowest noise figure. With the adjusted C_{ox} and the adjusted μ a P_d=30 mW gives according to analysis the lowest noise figure. Furthermore can be seen that the calculated noise figure is higher than the simulated noise figure.

Either the noise figure versus transistor width or the g_m versus V_{gs} gives a fitting result. The method to adjust the model is just a fitting method. The layout parasitics C_1, C_2 and C_3 can not be added as simple as by multiplying C_{ox} and/or μ. Though as has been seen from figure 9.5 and figure 9.4, by only multiplying C_{ox} the noise figure calculation results are comparable with simulation results, allowing rough design predictions.

A reasonable model fit has been found for a single common source transistor which differs only 0.2 dB with the CS+CASC design.

9.2.2 Including gate parasitics in the model

By comparing the rho-model results with the simulation results it has been found that the model is only sufficiently accurate in case of ideal inductances. A more advanced model, including the quality factor of the inductances would be better.

L.Belostotski and J.W.Haslett have introduced, next to the noise model for good power match (CS+LG+LS+B), a more advanced noise model in which the gate parasitics of both the gate inductance and the poly gate resistance have been included [8]. This noise model is based on circuit of an inductively degenerated common source transistor with integrated gate inductor.

The model of L.Belostotski and J.W.Haslett has been investigated to determine if this model gives a better prediction of with the simulation results. From now on this advanced model will be referred to as the Belostotski-model.

The parasitics of the drain and source inductances have been neglected in the Belostotski-model. As was seen from previous simulations the parasitics of the drain inductance L_d hardly influences the noise figure and the parasitics of the source inductance L_s can be ignored as the size of the inductance is small so that it can be implemented with an inductance with a high quality factor. The parasitics of the gate inductance have a big influence on the noise performance and therefore they are included.

The noise factor of the Belostotski-model can be written as:

$$F_{Belostotski} = 1 + \frac{R}{R_s}\Big(1 + R\frac{\gamma\omega^2 C_{gs}^2}{\alpha^2 g_{d0}}\chi\Big) \tag{9.6}$$

where

$$\chi = \frac{\alpha^2\delta}{5\gamma}\Big(1 + \frac{1}{\omega^2 C_{gs}^2 R^2}\Big) + 1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} \tag{9.7}$$

and

$$R = R_s + R_G \tag{9.8}$$

The gate parasitics R_G, can be described by:

$$R_G = \frac{\frac{1}{\omega C_{gs}} - \frac{\omega C_{gs} R_s}{g_m} + R_g Q_{ind}}{Q_{ind} - \omega C_{gs} g_m} \tag{9.9}$$

Where Q_{ind} is the quality factor of the gate inductance L_g and the poly gate resistance R_g is expressed as:

$$R_g = \frac{R_\square W_f}{18 C_{gs}}, \tag{9.10}$$

where W_f represents the finger width after folding.

The source and gate inductances are described by:

$$L_s = \frac{Z_{in} C_{gs}}{g_m} = \frac{(R_s - R_g) C_{gs}}{g_m} \tag{9.11}$$

$$L_g = \frac{1}{\omega^2 C_{gs}} - L_s \tag{9.12}$$

as was also explained in more detail in appendix B.2.

Resulting in a Belostotski noise factor described by:

$$F_{belostotski} = 1 + \frac{R_g}{R_s} + \frac{\delta}{5g_{d0}R_s} + \frac{\delta Q_s^2}{5g_{d0}R_s} + \frac{\gamma g_{d0}}{R_s Q_s^2 g_m^2} - 2|c|\sqrt{\frac{\gamma\delta}{5}}\frac{1}{R_s Q_s^2 g_m} \tag{9.13}$$

in which Q_s is the quality factor of the input network:

$$Q_s = \frac{1}{\omega C_{gs}(R_s + R_g)} \tag{9.14}$$

Looking carefully at relation (9.13) shows that by replacing Q_s by relation (9.14) and making $R_g = 0$ the simple F_b relation as was given by relation (B.18) appears.

The noise factor for a common source transistor, based on the rho-model given in section 2.3 relation (2.16), was described by:

$$F = 1 + \frac{R_s\delta\omega^2 C_{gs}^2}{5g_{d0}} + \frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0} R_s \omega^2 C_{gs}^2}{g_m^2} - 2|c|\sqrt{\frac{\delta\gamma}{5}}\frac{R_s\omega^2 C_{gs}^2}{g_m} \tag{9.15}$$

Noise factor 9.13 and 9.15 can be compared analytically to find their differences. Both noise factors are used such that power constraint is taken in account. A power of 20 mW is used together with the adjustment of C_{ox} as was introduced in the previous section. A finger width of 1.7 μm is used for the Belostotski-model.

The noise figure versus the transistor width, for the Belostotski-model, is calculated given different Q factors. Its calculations results are given in figure 9.8. Both the Spectre simulations and these analytical calculations show that there is a minimum Q factor for the inductances before the addition of the inductances can actually improve the noise figure next to providing a power match design.

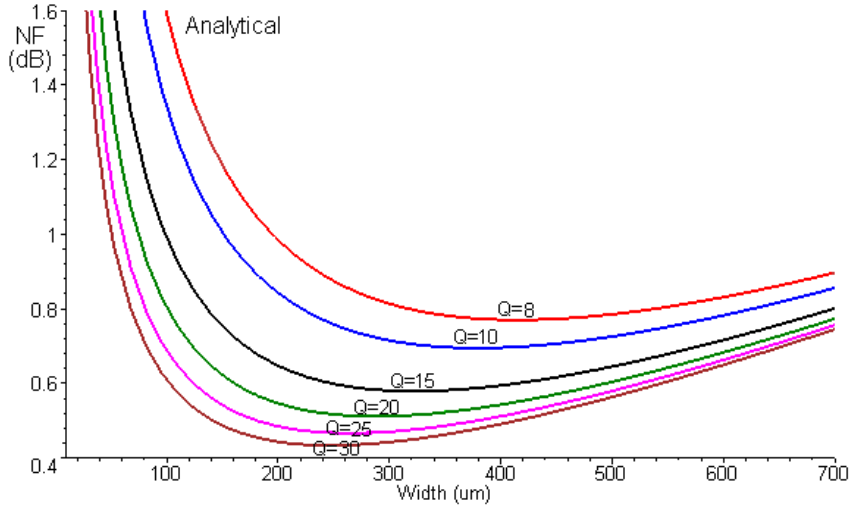

Figure 9.8: Noise figure versus transistor width, while varying Q

In the rho-model (analytical), the Q factor has not been implemented, though when we derive the noise figure versus transistor width, the noise figure of the rho-model has the same shape, remarkably, as the noise figure predicted by the Belostotski-model for a Q of 20.

The optimal transistor width for a Q=10 is, found in figure 9.8, 400 μm. For the simulations an optimal width of 190 μm was found. Indicating that the Belostotski model is also not as accurate as desired. The noise performance is a reasonable approximation. One can add between

0.1 dB and 0.2 dB of additional noise for the cascode device to make the noise performance approximation even better.

Determining the values of the gate and source inductance, L_g and L_s, using relation (9.12) and (9.11), resulted in L_g=658 pH and L_s=42 pH for a quality factor of 10. These values are different from the power match values found in section 8.4.2 though accurate enough to be used as a starting point in simulations.

9.3 Summary

Although in the previous chapter was found that a near 1 dB noise figure can be obtained, an even lower noise figure would be nice. A higher quality factor of the inductances will improve the noise figure.

In section 3.1.3 a difference in optimal width between the analytical noise model and the Spectre simulations was found. The capacitance value, used in calculations as C_{ox} turned out to be different in simulation compared with the originally used value for the calculations. With the adjustment of C_{ox} the model is representative for a single common source transistor and can be used for noise figure approximations.

The enhanced model of L.Belostotski and J.W.Haslett has been given and calculations have been done. Unfortunately this model did again show a difference for optimal width and for the values of the inductances. Only rough predictions can be made based on this enhanced noise model.

Chapter 10

Conclusions and recommendations

Conclusions

With the current CMOS technology of 65 nm it is possible, with the help of simulations, to design a low noise amplifier with a noise figure <1 dB. The best design for low noise performance smaller than 1 dB is a common source and cascode transistor together with a gate and drain inductance with a quality factor higher than 10. If a reasonable or good power match is desired, an additional source inductance can be added, though the noise performance increases to just above 1 dB.

Although initially was expected, based on previous research, that a non-standard antenna resistance results in a better noise performance. It has been found, by simulations, that a standard 50 Ω resistance with its optimal transistor width gives a similar noise performance as a non-standard antenna resistance.

A higher power results in a lower noise performance, though a power dissipation of 20 mW already gives very good results. This power is high enough to give near optimal noise performance and is still small enough to be acceptable.

Recommendations

An improved noise model for the entire low noise amplifier including the losses of the inductance will make it easier to design a low noise amplifier. A model as designed by Y. Koolivand et al. together with the the model of L.Belostotski and J.W.Haslett should be studied in more detail and if possible corrected to establish a better noise model[8][16].

It has been found that especially the losses of the gate inductance have a great influence on the noise performance. A bond wire inductance has a higher quality factor but also higher variation in inductance value. If this variation is not too big (<15%), perhaps these can be used for a n+p match design. It is recommended to study the options of inductances with a higher quality factor.

The performance trend has shown a lower noise figure given smaller transistor technology. Currently the newest technology of 45 nm is available for simulations and this technology could be used as a follow up of this report. It is expected that, with the use of the optimized transistor width, even lower noise figures will be found.

Appendix A

Noise parameters of a common source transistor

Thomas Lee [2] describes how one can obtain, based on a simple two-port network, a noise factor description of a common source transistor with exact expressions of the parameters. These derivations, together with some additional explanations and figures, are shown in this appendix.

A.1 Noise sources of a common source transistor

The MOSFET noise model by A. van der Ziel consists of two sources [9]. The (mean square) drain current noise is expressed as:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f, \tag{A.1}$$

where g_{d0} is the transconductance at zero drain bias and γ the drain noise coefficient. The gate current noise is expressed as:

$$\overline{i_{ng}^2} = 4kT\delta g_g\Delta f, \tag{A.2}$$

where

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}, \tag{A.3}$$

is the real part of the gate-to-source admittance and δ is the gate noise coefficient. The gate noise is further correlated with the drain noise, with a correlation coefficient defined formally as

$$c \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}}. \tag{A.4}$$

The long-channel value of c is theoretically $-j0.395$ when the reference direction of the gate noise is from source to gate, as depicted in figure A.1, and the reference direction of the drain noise is from drain to source.

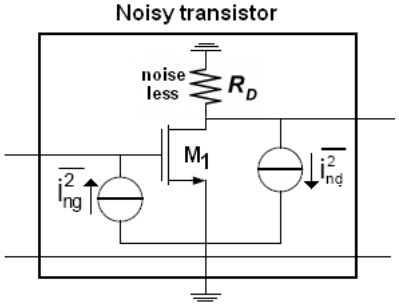

Figure A.1: Noisy transistor model with drain noise and gate current noise source

Four of the two-port noise parameters: the equivalent noise resistance modelling the drain voltage noise (R_n), the uncorrelated gate current noise (G_u), the correlated conductance (G_c) and the correlated susceptance (B_c), are described as follows:

$$R_n \equiv \frac{\overline{e_n^2}}{4kT\Delta f}, \tag{A.5}$$

$$G_u \equiv \frac{\overline{i_u^2}}{4kT\Delta f}, \tag{A.6}$$

$$Y_c \equiv \frac{i_c}{e_n} = G_c + jB_c, \tag{A.7}$$

These parameters can be derived for a common source transistor by referring the two fundamental MOSFET noise sources to the input port. The fundamental noise sources $\overline{i_{nd}^2}$ and $\overline{i_{ng}^2}$ as depicted in figure A.1 can be represented by $\overline{e_n^2}$ and $\overline{i_n^2}$ as depicted in figure A.2.

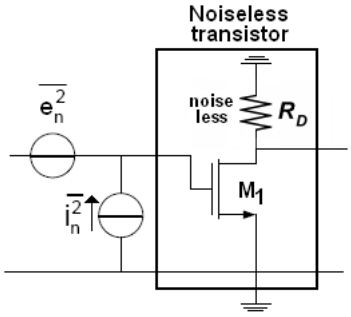

Figure A.2: Noiseless transistor model with noise sources as input sources

An expression for $\overline{e_n^2}$ is:

$$\overline{e_n^2} = \frac{\overline{i_{nd}^2}}{g_m^2} = \frac{4kT\gamma g_{d0}\Delta f}{g_m^2} \tag{A.8}$$

This expression for $\overline{e_n^2}$ allows to rewrite R_n.

$$R_n = \frac{\gamma g_{d0}}{g_m^2} \tag{A.9}$$

As introduced, in section 2.2, the source i_n can be split in two parts: i_u (part uncorrelated with e_n) and i_c (part correlated with e_n), as depicted in figure A.3.

$$i_n = i_c + i_u \tag{A.10}$$

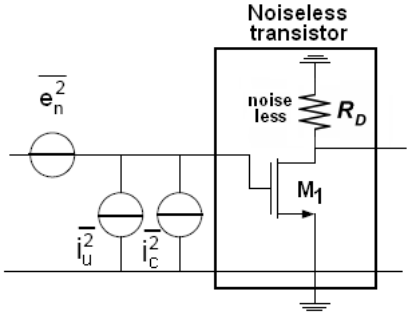

Figure A.3: Uncorrelated and correlated input current model representation

Due to the fact that the drain current noise still flows, even when the input is open-circuited and the induced gate current noise is ignored, the input referred noise voltage (e_n) is not completely modelling the drain current noise. To find the equivalent input current, divide the drain current by the current gain ($g_m/j\omega C_{gs}$).

It is necessary to divide the drain current by the transconductance and multiply it with the input admittance, to give the value of an equivalent input current noise that completes the modelling of i_{nd},

$$\overline{i_{n1}^2} = \frac{\overline{i_{nd}^2}|j\omega C_{gs}|^2}{g_m^2} = \frac{4kT\gamma g_{d0}\Delta f|j\omega C_{gs}|^2}{g_m^2} = \overline{e_n^2}|j\omega C_{gs}|^2 = \overline{e_n^2}\omega^2 C_{gs}^2 \tag{A.11}$$

It has been assumed that the input admittance of a MOSFET is purely capacitive. Relation A.11 shows that i_{n1} is proportional to e_n and therefore completely correlated with e_n.
The total equivalent input current noise i_c is the sum of the input-referred drain current noise contribution described by relation (A.11) and the part of the induced gate current noise (i_{ng}) which is correlated with $\overline{e_n^2}$.

$$i_c = i_{n1} + i_{ngc}, \tag{A.12}$$

resulting in a model as depicted in figure A.4.

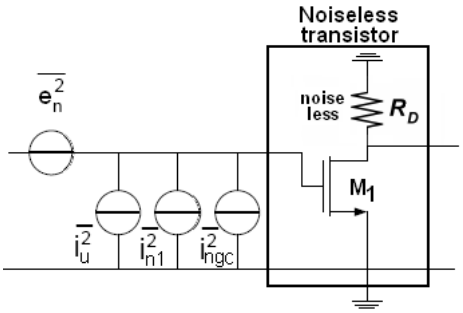

Figure A.4: Complete input current model

A.2 Derivations of the four of the noise parameters

The four noise parameters where found to be G_u, G_c, B_c, and R_n, with the above derived noise sources these parameters will now be derived: G_c, B_c, R_n and G_u.

The correlation admittance can be expressed, with the use of relation (A.11), as:

$$Y_c = \frac{i_c}{e_n} = \frac{i_{n1} + i_{ngc}}{e_n} = j\omega C_{gs} + \frac{i_{ngc}}{e_n} = j\omega C_{gs} + g_m \cdot \frac{i_{ngc}}{i_{nd}} \tag{A.13}$$

As Y_c is still not in a useful form, we need to incorporate the gate noise correlation factor. Multiplying both numerator and denominator of the last term of relation (A.13) by the conjugate of the drain current noise, allows to express relation (A.13) in terms of cross-correlation.

$$\frac{i_{ngc}}{i_{nd}} = \frac{\overline{i_{ngc} \cdot i_{nd}^*}}{\overline{i_{nd} \cdot i_{nd}^*}} = \frac{\overline{i_{ngc} \cdot i_{nd}^*}}{\overline{i_{nd}^2}} = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\overline{i_{nd}^2}} \tag{A.14}$$

The term i_{ngc} has been replaced by i_{ng}, because the uncorrelated part of the gate noise (i_{ngu}) has no contribution to the cross-correlation. The derivations can be continued in relation (A.15) to introduce the correlation coefficient that was represented by relation (A.4).

$$\frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{nd}^2}}\sqrt{\overline{i_{nd}^2}}}\sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{ng}^2}}} = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}}\sqrt{\overline{i_{nd}^2}}}\sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} = c \cdot \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}}. \tag{A.15}$$

The correlation admittance can now be described by:

$$Y_c = j\omega C_{gs} + g_m \cdot c\sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} \tag{A.16}$$

With relation (A.1), (A.2) and (A.3) this can be written as

$$Y_c = j\omega C_{gs} + g_m \cdot c\sqrt{\frac{\delta\omega^2 C_{gs}^2}{5\gamma g_{d0}^2}} = j\omega C_{gs} + \omega C_{gs}\frac{g_m}{g_{d0}} \cdot c\sqrt{\frac{\delta}{5\gamma}} \tag{A.17}$$

Assuming that c is purely imaginary and negative, even in the short-channel regime, and substituting $\frac{g_m}{g_{d0}}$ by α, finally a useful expression for the correlation admittance arises:

$$Y_c = j\omega C_{gs} - j\omega C_{gs}\frac{g_m}{g_{d0}} \cdot |c|\sqrt{\frac{\delta}{5\gamma}} = j\omega C_{gs}(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \tag{A.18}$$

The correlation admittance Y_c can be divided in terms of the correlation conductance G_c and the correlation susceptance B_c. Relation (A.18) shows that the correlation admittance is purely imaginary resulting in a G_c=0.

The total induced gate current noise can be rewritten as:

$$\overline{i_{ng}^2} = \overline{(i_{ngc} + i_{ngu})^2} = 4kT\Delta f\delta g_g|c|^2 + 4kT\Delta f\delta g_g(1 - |c|^2) \tag{A.19}$$

From this equality the last two-port parameter G_u, the equivalent noise conductance modelling the uncorrelated part of the gate current noise, can be derived and can, with the use of relation (A.6) and relation (A.19), be described as:

$$G_u = \frac{4kT\Delta f\delta g_g(1 - |c|^2)}{4kT\Delta f} = \frac{\delta\omega^2 C_{gs}^2(1 - |c|^2)}{5g_{d0}} \tag{A.20}$$

A.3 Summary of the noise parameters

A summary of the four noise parameters is given in table A.1.

Design variable	Expression
G_c	0
B_c	$\omega C_{gs}(1 - \frac{g_m}{g_{d0}}\|c\|\sqrt{\frac{\delta}{5\gamma}})$
R_n	$\frac{\gamma g_{d0}}{g_m^2}$
G_u	$\frac{\delta\omega^2 C_{gs}^2(1-\|c\|^2)}{5g_{d0}}$

Table A.1: Summary of the four noise parameters of a MOSFET

Appendix B

Power match

In RF is often referred to the source and load to be "power matched". This means that for a given source impedance, the load impedance is chosen such that the maximum available power is transferred from the source to the load.

B.1 Power match given a simple circuit

When a simple circuit as in figure B.1 is given, intuition tells that power match occurs when R_s=R_L. This can be verified by applying math:

$$I = \frac{V_s}{R_s + R_L} \tag{B.1}$$

$$P_L = R_L I^2 = R_L(\frac{V_s}{R_s + R_L})^2 = \frac{V_s^2}{R_s^2/R_L + 2R_s + R_L} \tag{B.2}$$

Finding a value for R_L for which the denominator is a minimum results in the maximum power transfer.

$$\frac{\partial}{\partial R_L} R_s^2/R_L + 2R_s + R_L = \frac{-R_s^2}{R_L^2} + 1 \tag{B.3}$$

resulting in: $R_L = \pm R_s$. To find out if R_L should be positive or negative, the denominator can be differentiated a second time, resulting in:

$$\frac{2R_s^2}{R_L^3} \tag{B.4}$$

This is a positive term for positive R_s and R_L, the denominator is a minimum when $R_L = R_s$.

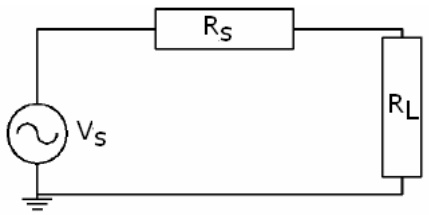

Figure B.1: Circuit with resistance

In general the source and load can consist of both a real and an imaginary part, as depicted in figure B.2. The circuit relation becomes:

$$I = \frac{V}{Z_s + Z_L} \tag{B.5}$$

$$P_L = R_L I^2 = R_L(\frac{V}{Z_s + Z_L})^2 = R_L \frac{V^2}{(R_s + R_L)^2 + (X_s + X_L)^2} \tag{B.6}$$

As before, minimizing the denominator results in maximum power transfer. Since reactance can be negative the denominator is easily minimized by making $X_L = -X_s$. The power equation is now reduced to:

$$P_L = \frac{V^2}{(R_s + R_L)^2} \tag{B.7}$$

Still the value of R_L needs to be found, though it can be seen that this maximization problem has the same form as in the purely resistive situations and the maximizing condition $R_L = R_s$ can be found again.

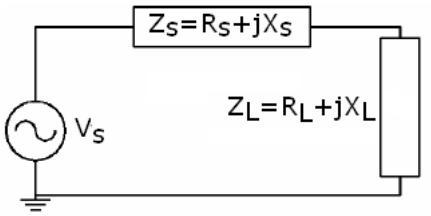

Figure B.2: Circuit with Admittance

Summarizing this means that the power to the load can be maximized when $X_s + X_L = 0$ and $R_s = R_L$; Z_s and Z_L are complex conjugates.

B.2 Power match for a common source transistor

The input impedance of a MOSFET is mostly capacitive, while the impedance of the antenna is resistive. Power match is often one of the design specifications to reduce wave reflections. Providing a match to the source, without introducing more noise, is difficult. Several LNA topologies have been introduced by T.Lee [2], resulting in a design for power match and low noise figure: an inductively degenerated common-source amplifier as depicted in figure B.3.

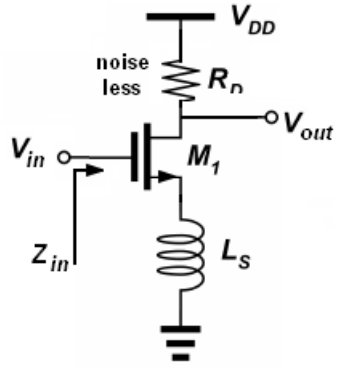

Figure B.3: Inductively degenerated common-source amplifier

With an inductance added to the source of the common-source transistor, the input impedance of the circuit changes. The input impedance, represented by relation (B.8) becomes that of an RLC network, with a resistive term directly proportional to the inductance value.

$$Z_{in} = j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s \tag{B.8}$$

The real part of this input impedance $\frac{g_m}{C_{gs}}L_s$ should equal $50\,\Omega$, which requires a source inductance of:

$$L_s = \frac{Z_{in}C_{gs}}{g_m} = \frac{R_sC_{gs}}{g_m} \tag{B.9}$$

As described by Thomas Lee and as can be found from relation (B.8), the input impedance is purely resistive at one specified frequency, the resonance frequency [2]. The imaginary part is zero for the resonance frequency, resulting in a power match.

$$I_m\{Z_{in}\} = X_s = j\omega L_s + \frac{1}{j\omega C_{gs}} = 0, \tag{B.10}$$

this means that the resonance frequency is determined by:

$$\omega^2 = \frac{1}{L_sC_{gs}} \Longleftrightarrow f = \frac{1}{2\pi\sqrt{L_sC_{gs}}} \tag{B.11}$$

Since both C_{gs} and L_s are set, the resonance frequency is set as well. To have more design freedom, the resonance frequency can be set by another inductance placed at the gate of the common-source transistor, shown in figure B.4.

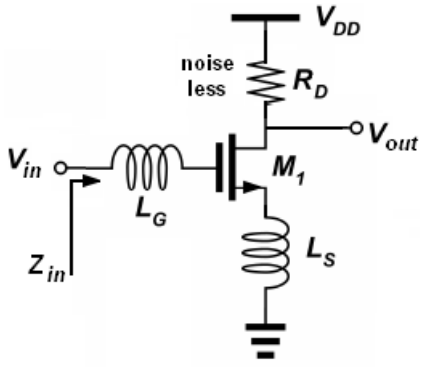

Figure B.4: Narrowband LNA (biasing not shown)

The input impedance of figure B.4 becomes:

$$Z_{in} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}}L_s, \tag{B.12}$$

The real part of this input impedance is still the same, resulting in the same expression for the source inductance as in relation (B.9). The imaginary part should be zero at the resonance frequency to obtain power match.

$$I_m\{Z_{in}\} = X_s = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} = 0, \tag{B.13}$$

This means that the resonance frequency is determined by:

$$\omega^2 = \frac{1}{(L_s + L_g)C_{gs}} \Longleftrightarrow f = \frac{1}{2\pi\sqrt{(L_s + L_g)C_{gs}}} \tag{B.14}$$

Given the resonance frequency the gate inductance can now be found and is determined by:

$$L_g = \frac{1}{\omega^2 C_{gs}} - L_s \tag{B.15}$$

B.2.1 Noise figure at power match

Both K. Shaeffer and L. Belostotski have derived the noise figure relation of an inductively degenerated LNA [4][5][6][8]. The simplified form of this noise figure, without the gate inductor parasitic resistance and gate finger parasitic resistance, can be written as:

$$F_b = 1 + \frac{R_s g_{d0} \gamma w^2 C_{gs}^2}{g_m^2} \chi \tag{B.16}$$

where

$$\chi = 1 + \frac{\delta g_m^2 (1 + \frac{1}{w^2 C_{gs}^2 R_s^2})}{5\gamma g_{d0}^2} - \frac{2|c| g_m \sqrt{\frac{\delta}{5\gamma}}}{g_{d0}} \tag{B.17}$$

resulting in a noise figure of:

$$F_b = 1 + \underbrace{\frac{R_s \delta \omega^2 C_{gs}^2}{5 g_{d0}} + \frac{\delta}{5 R_s g_{d0}}}_{i_g \ contribution} + \underbrace{\frac{\gamma g_{d0} R_s^2 \omega^2 C_{gs}^2}{R_s g_m^2}}_{i_d \ contribution} - \underbrace{2|c| \sqrt{\frac{\delta\gamma}{5}} \frac{R_s \omega^2 C_{gs}^2}{g_m}}_{correlation \ contribution} \tag{B.18}$$

The inductances L_s and L_g are determined by relations B.9 and B.15 respectively.

It can be found that, compared with relation (2.16), repeated in relation (B.19) a drain noise contribution is eliminated and a small gate noise term is introduced for power matching.

$$F = 1 + \underbrace{\frac{R_s \delta \omega^2 C_{gs}^2}{5 g_{d0}}}_{i_g \ contribution} + \underbrace{\frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0}}{R_s g_m^2} R_s^2 \omega^2 C_{gs}^2}_{i_d \ contribution} - \underbrace{2|c| \sqrt{\frac{\delta\gamma}{5}} \frac{R_s \omega^2 C_{gs}^2}{g_m}}_{correlation \ contribution} \tag{B.19}$$

In section 4.3 has been found that the gate noise contribution can be neglected, indicating that the use of a power match model results in a reduced noise figure expression of:

$$F_{b_{reduced}} = 1 + CWR_s = 1 + \underbrace{\frac{\gamma g_{d0} R_s^2 \omega^2 C_{gs}^2}{R_s g_m^2}}_{i_d \ contribution} \tag{B.20}$$

The reduced noise factor expression for a single transistor is described by:

$$F_{reduced} = 1 + \frac{B}{WR_s} + CWR_s = 1 + \frac{\gamma g_{d0}}{R_s g_m^2} + \frac{\gamma g_{d0} R_s^2 \omega^2 C_{gs}^2}{R_s g_m^2} \tag{B.21}$$

Comparing these two relations reveals that the term $\frac{B}{WR_s}$ has been eliminated. This makes the noise figure F_b a straight line instead of a parabolic figure. The parabolic figure allows to find an optimum transistor width. To maintain the parabolic figure the reduced noise figure for power match should therefore be described as:

$$F_{reduced} = 1 + \frac{\delta}{5 R_s g_{d0}} + \frac{\gamma g_{d0} R_s^2 \omega^2 C_{gs}^2}{R_s g_m^2} \tag{B.22}$$

Maintaining a parabolic figure, resulting in an optimum width given an antenna resistance.

B.3 Noise circles

In the noise model of the common source transistor the inverse of impedance was introduced: admittance. The desired admittance to obtain power match can be written in terms of conductance and susceptance as $Y_c = G_{max} + jB_{max}$.

In section 2.2.1 was introduced that to achieve noise matching and thus a minimum noise figure, G_s should equal G_{opt} and B_s equals B_{opt}. It would be ideal to have both noise matching and power matching at the same time. Unfortunately this is, generally, not possible. This can be shown with the help of an noise circle image, as depicted in figure B.5.

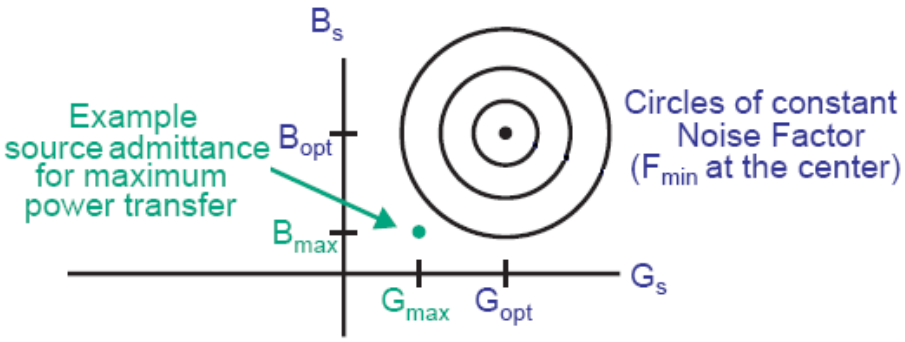

Figure B.5: Noise circles versus maximum power transfer

In the noise circle figure the noise factor location for maximum power transfer is pointed out with a dot (B_{max},G_{max}). It can be seen that, for this example, this point lies not in the center of the constant noise circles. One can generally not achieve minimum noise figure if maximum power transfer is desired and vice versa. This will be explained in more detail in chapter 6.

Appendix C

Rho-model

The downscaling of transistor size has introduced the high-field effect of velocity saturation. To be able to accommodate velocity saturation, the drain current, can be described by [2]:

$$I_d = \frac{\mu C_{ox} W}{2L}(V_{gs} - V_{th})V_{dsat}. \tag{C.1}$$

The conductance g_{d0} can be found by differentiating I_d to V_{dsat}.

$$g_{d0} = \frac{\partial I_d}{\partial V_{dsat}} = \mu C_{ox}\frac{W}{2L}(V_{gs} - V_{th}) = \mu C_{ox}\frac{W}{2L}V_{od}, \tag{C.2}$$

in which C_{ox} is the gate oxide capacitance per unit area and V_{od} is the overdrive voltage $V_{gs}-V_{th}$.

The drain current saturates when the velocity does, and the velocity saturates at smaller voltages as the device gets shorter. V_{dsat} may be expressed more generally, as described by P.K. Ko ([11]), by the following approximation:

$$V_{dsat} \approx (V_{gs} - V_{th})||(LE_{sat}) = \frac{(V_{gs} - V_{th})(LE_{sat})}{(V_{gs} - V_{th}) + (LE_{sat})} \tag{C.3}$$

in which E_{sat} is the velocity saturation field strength. The drain current can now be rewritten as:

$$I_d = \frac{\mu C_{ox} W}{2L}(V_{gs} - V_{th})[(V_{gs} - V_{th})||(LE_{sat})], \tag{C.4}$$

resulting in

$$I_d = \frac{\mu C_{ox} W}{2}\frac{(V_{gs} - V_{th})^2 E_{sat}}{V_{gs} - V_{th} + LE_{sat}} \tag{C.5}$$

Using the relative gate overdrive voltage ρ, defined by:

$$\rho = \frac{V_{gs} - V_{th}}{LE_{sat}} = \frac{V_{od}}{LE_{sat}} \tag{C.6}$$

and relation:

$$v_{sat} = \frac{1}{2}\mu E_{sat} \tag{C.7}$$

the drain current can be rewritten as

$$I_d = WLC_{ox}v_{sat}E_{sat}\frac{\rho^2}{1+\rho} \tag{C.8}$$

The transconductance g_m can be found by differentiating I_d from relation (C.5) to V_{gs}. After substitution of relation (C.6) the transconductance can be described as:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{\mu C_{ox} W V_{od}}{L}\Big(\frac{1}{1+\rho} - \frac{\rho}{2(1+\rho)^2}\Big) \tag{C.9}$$

Rewriting the transconductance g_m results in;

$$g_m = \Big(\frac{1+\frac{\rho}{2}}{(1+\rho)^2}\Big)\mu C_{ox} W \rho E_{sat} = \alpha \mu C_{ox} W \rho E_{sat}, \tag{C.10}$$

in which α represents:

$$\alpha = \frac{1+\frac{\rho}{2}}{(1+\rho)^2} \tag{C.11}$$

From these relations can be found that α can also be expressed as a function of the transconductance g_m and the conductance g_{d0}:

$$\alpha = \frac{g_m}{g_{d0}} \tag{C.12}$$

Appendix D

Process parameters

An example of transistor parameters, as have been used in the analytical calculations in section 3.1.3 and in chapter 4, is given in the following table:

Process parameter	Value
γ	$2/3$
δ	$4/3$
c	0.395
V_{dd}	$1.2\,V$
L	$0.06\,\mu m$
C_{ox}	$11\,mF/m^2$
μ	0.035
E_{sat}	$6\,MV/m$
v_{sat}	$\frac{\mu}{2}Esat$
V_{od} section 4.1	$V_{gs} - V_{th}$
V_{od}	$0.25\,V$

Table D.1: Summary of the transistor parameters

These parameters will not give a good match with the simulation model, though they show a trend that follows the simulation model. When the noise figure increases in the model due to a design change, it can be expected that it will also increase in the simulation model. Only the exact amount of increase will be different.

Appendix E

Simulation setup

In this appendix basic information regarding the simulation, such as the simulation setup and the type of analysis, is provided. In all cases, only NMOS transistors with a minimum transistor length of $0.06\mu m$ are used.

E.1 Setup

The simulations are done at a simulation temperature of 16.85 °C (equal to 290°K). The supply voltage is an ideal voltage source (V_{dd}) of 1.2 V. The output impedance has been set at 50 Ω and is further neglected as a design parameter. The focus is on low noise performance, on the input impedance and on the available gain. The impedance of the mixer stage (to be added in cascade with the LNA) can be set to match to the output of the LNA. For the AC-coupling part, ideal capacitances (C_c) of 1 nH are used to couple the ac-signals to the input and output port. The resulting simulation setup is shown in figure E.1

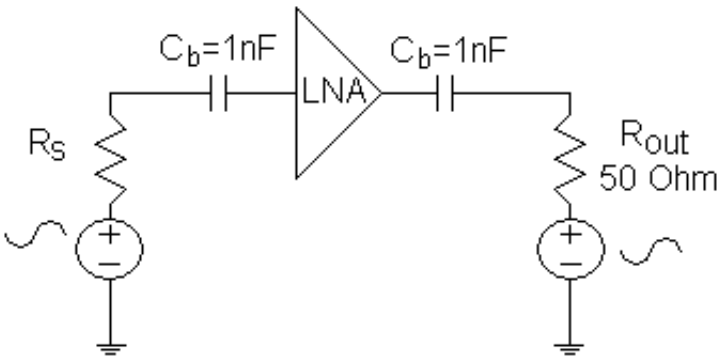

Figure E.1: Simulation setup

This setup is used for all the Spectre simulations unless specified otherwise (as for power optimization). The LNA is in figure E.1 represented by a triangle-block.

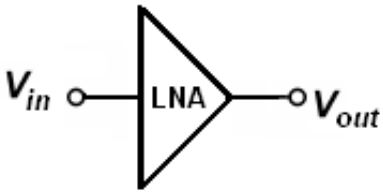

Figure E.2: Reduced simulation setup

This block is the circuit part that changes with the progress of the report. In the chapters that discuss Spectre simulations only the LNA block (the internals of the LNA) will be shown.

E.2 Analysis

Several type of analysis can be done with Spectre. A short introduction of the analysis in this report will be given [14].

E.2.1 Small signal Noise (SP and Noise)

Small signal noise simulations can be performed with both SP and noise analysis.

- The noise analysis provides the noise figure, NF;
- The SP analysis provides both the NF_{min} and NF;

E.2.2 Small signal Gain (SP)

Scattering parameters, also referred to as S-parameters, are based on the incident and reflected waves in a system, they represent the reflection and transmission coefficients when the match network is terminated:

- S_{11} is the input reflection coefficient;
- S_{12} is the reverse transmission coefficient;
- S_{21} is the forward transmission coefficient;
- S_{22} is the output reflection coefficient.

With the S-parameters gain measurements can be done. With respect to an LNA the three power gain definitions, commonly used in LNA design can be described as:

Transducer power gain G_T, is defined as the ratio between the power delivered to the load and the power available from the source [14].

$$G_T = |S_{21}|^2$$

Operating power gain G_P is defined as the ratio between the power delivered to the load and the power input to the network.

$$G_P = \frac{1}{1 - |S_{11}|^2}|S_{21}|^2$$

Available power gain G_A is defined as the ratio between the power available from the network and the power available from the source.

$$G_A = \frac{1}{1 - |S_{22}|^2}|S_{21}|^2$$

The power available from the source is generally larger than the power input to the LNA, so $G_P > G_T$. The closer the two gains are, the better the input matching is. Similarly when G_A is close to G_T there is a good output match.

E.2.3 IP2 and IP3 simulation (PSS)

A two tone test needs to be done to measure the IP2 and the IP3 curve. Two tones, ω_1 and ω_2 with the same amplitude, coming from adjacent channels, drive the LNA simultaneously.

The IP2 is defined as the extrapolation point of the power of the 1st order tones ω_1 and ω_2 , and the power of the 3rd order tones ω_2 - ω_1 and ω_2 + ω_1 at the load.

The IP3 is defined as the extrapolation point of the power of the 1st order tones ω_1 and ω_2 , and the power of the 3rd order tones $2\omega_1$ - ω_2 and $2\omega_2$ - ω_1 at the load.

List of Figures

List of Tables

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