Bachelor Thesis

The applicability of $SrTiO_3$ in memristive devices - a preliminary investigation

by

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Abstract

A Memristor has the ability to remember its resistance when no bias is applied, making it suitable for numerous applications in, e.g., data storage and neuromorphic circuitry.

HP already demonstrated a working memristor using TiO_2. In this report $SrTiO_3$ (STO) was considered in the fabrication of an oxygen vacancy based memristor on a Nb-doped STO substrate. A model to fabricate such a device is presented as well as the measurements characterizing the different layers in this memristor.

Measuring STO proved to be challenging, piercing through thin layers and the forming of Schottky barriers with different materials need to be taken into account. Ultimately switching behaviour in a single layer was observed, leading to the conclusion that STO still is a good candidate for memristive applications.

Contents

Introduction

A Memristor, a portmanteau for memory and resistor, has the ability to remember its resistance when no bias is applied making it suitable for numerous applications in for example data storage and neuromorphic circuitry. Since the prediction of this fourth passive electrical component in 1971 by Leon O. Chua [1], numerous attempts have been made to find this missing element. In 2008 HP claimed to have fabricated a device using TiO_2 that mimics the properties of the theoretical memristor based on charge displacement [2], as will all be explained in Chapter 1.

Inspired by the research of HP, this report explores the possibilities of fabricating the memristor using $SrTiO_3$. This idea arose because the research group ICE has a lot of experience with this material. $SrTiO_3$ is chemically and thermally very stable and its resistance is highly dependent on oxygen deficiencies. These are important features for a material used in memristors, as will also be explained in Chapter 1. The main goal is to prove that $SrTiO_3$ is a suitable material for making memristors. A design for a $SrTiO_3$ based memristor is proposed in Chapter 2. Based on the design, the performed measurements are presented in Chapter 3, followed by the discussion and conclusions.

Chapter 1

Theoretical Background

The theoretical aspects of this thesis will be discussed in this chapter. Resistive switching and Schottky barriers will be explained in Section 1.1 and Section 1.2 respectively. Section 1.3 explains the memristor function and why it took researchers a long time to find the memristor. Also a few applications of memristors are presented. Finally the used materials will be discussed in Section 1.4.

1.1 Resistive Switching

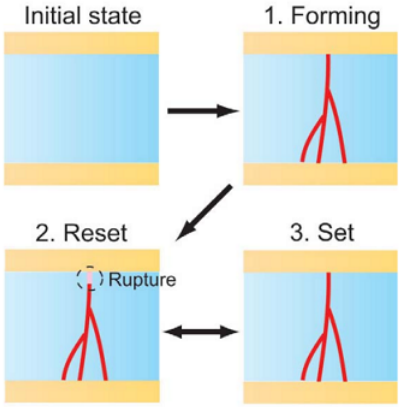
Resistive switching is the phenomenon where the resistance of a dielectric material changes under the influence of an acting electric field or current. This process is reversible and non-volatile, meaning it remains in its previous resistive state even with zero bias applied. Several mechanisms are proposed to explain resistive switching, however no comprehensive theory has been presented yet.

1.1.1 Types of Resistive Switching

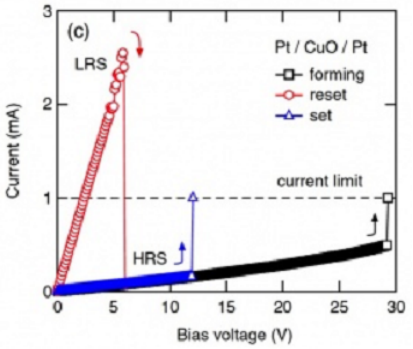
There are two types of resistive switching: unipolar and bipolar. Usually, dielectrics with binary oxides produce unipolar switching behaviour whereas devices with ternary and even more complex [3] oxides produce bipolar switching. Unipolar switching is independent of polarity, bipolar switching is dependent. A strange case is that of the TiO_2 which has been reported to switch both unipolar and bipolar [4].

Unipolar

Unipolar switching is enabled by electroforming of the material. In this process the material is exposed to a high electric field causing it to near breakdown (prevented by a compliance current), this is referred to as a soft breakdown. Caused by the electric field, filaments are formed in the material, resulting in a small channel allowing the current to flow. The system is in a low resistance state (LRS). Now, without using a compliance current, a high enough voltage will cause a high current which in turn will rupture the filament at the interface, this is the reset process. The system is back in a high resistance state (HRS). In the HRS, a large enough voltage (yet lower than the forming voltage, the blue curve in Fig. 1.1b) will restore the filament and thus switch the device to an LRS. This process is repeatable and a recent study has shown that a filament indeed is the conductive mechanism [5]. A visualization of this process can be seen in Fig. 1.1a and Fig. 1.1b.



(a)



(b)

Figure 1.1: The forming and setting processes in a unipolar switching device [6] (a) and a visualization of the V,I characteristic for these processes [5] (b).

Bipolar

Bipolar switching is a more complex process which also includes a dependency on polarity. Raising the positive voltage yields a switch to an LRS, a large negative voltage switches the device back to an HRS. The main difference between unipolar and bipolar is the fact that, in bipolar, switching takes place over the entire interface and not just a single (local) filament.
There are a few possible explanations for the switching behaviour including: phase transition of perovskite-type structures, Schottky barriers formed at the semiconductor-metal interface and trapping and de-trapping of carriers [7].

1.1.2 Materials

Typically, transition metal oxides are used for resistive switching devices. The high relative permittivity ϵ_r of these materials contributes to dense carrier concentrations when the material is polarized under the influence of an acting electronic field. Binary oxides such as TiO_2 have been reported to be good candidates in resistive switching devices. In this report the usage of $SrTiO_3$ is considered. Not only the metal oxide plays a role in resistive switching, also the contact material is of interest.

1.2 Schottky Barriers

When a metal is in contact with another metal electrical transport behaves Ohmic. In other cases where a metal is joined with a semiconductor the behaviour is either Ohmic or a Schottky barrier is formed. This section will explain both outcomes and is based on several sources [8][9][10][11].

1.2.1 General Theory

. Fig. 1.2a shows a junction between a metal and an n-type semiconductor just before they are in contact, Fig. 1.2b shows the band diagram when the Fermi levels are equilibrated. In this figure it is assumed that the work function for the metal is higher than the work function for the semiconductor (i.e., $\Phi_m > \Phi_s$), this is also a condition for rectifying behaviour.

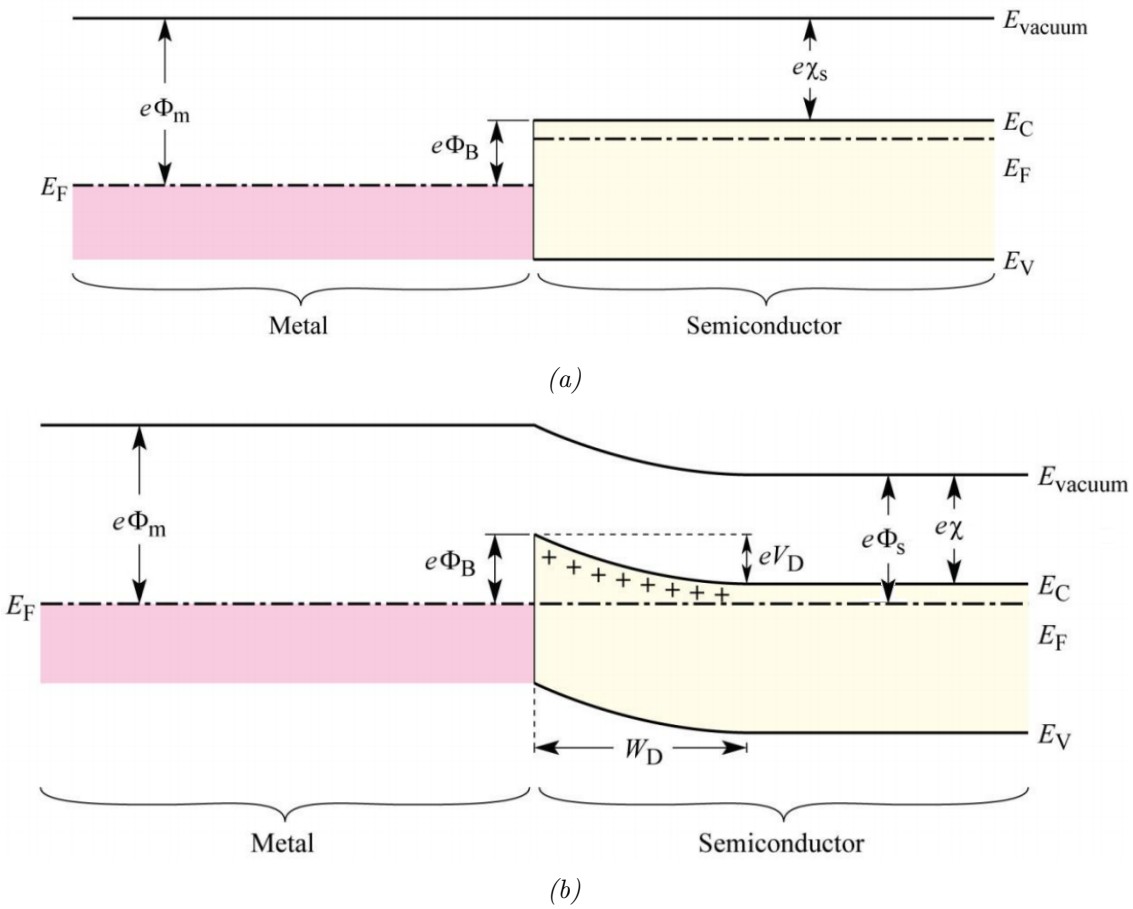


Figure 1.2: The band diagram for semiconductor/metal interface before (a) and after (b) contact (adapted from [10]).

When the two layers are joined, electrons move from the conduction band of the semiconductor to the metal (diffusion) until the Fermi levels are lined up. Now the metal becomes slightly negative creating a 'barrier' for more electrons to transfer from the semi-

conductor to the metal. This barrier is called a Schottky barrier and is given by Eq. 1.1.

$$\Phi_B = \Phi_m - \chi_s \tag{1.1}$$

With χ_s the electron affinity of the semiconductor.
Creating this barrier also results in a potential difference in the semiconductor (i.e., the potential difference between the height of the barrier and the conduction band), this diffusion potential is given by:

$$eV_D = e\Phi_B - (E_C - E_F) = e\Phi_m - e\Phi_s \tag{1.2}$$

For electrons to move from metal to semiconductor the barrier is the Schottky barrier as given in Eq. 1.1, to move from semiconductor to metal the barrier is given by the diffusion potential in Eq. 1.2.
In equilibrium, there is an area in the conduction band of the semiconductor area where there are less electrons, this region is called the depletion layer W_D and is given by Eq. 1.3

$$W_D = \sqrt{\frac{2\epsilon}{qN_d}V_D} \tag{1.3}$$

Here N_d is the donor concentration and ϵ the permittivity of the semiconducting material ($\epsilon = \epsilon_0\epsilon_r$). It can be seen the depletion width is proportional to the square root of the diffusion potential and inversely proportional to the square root of the carrier concentration. When the semiconductor is heavily doped, the depletion width will decrease and electrons will be able to tunnel through the potential barrier, this results in Ohmic behaviour ($N_d > 10^{18} cm^{-3}$).

1.2.2 Applying a bias

When a bias is applied there is an external electrical field acting on the junction, two cases can be distinguished: forward bias and reverse bias. Forward (reverse) bias means the metal is connected to the positive (positive) terminal of a battery. In Fig. 1.3 the junction is displayed with an applied positive (1.3a) and negative bias(1.3b).

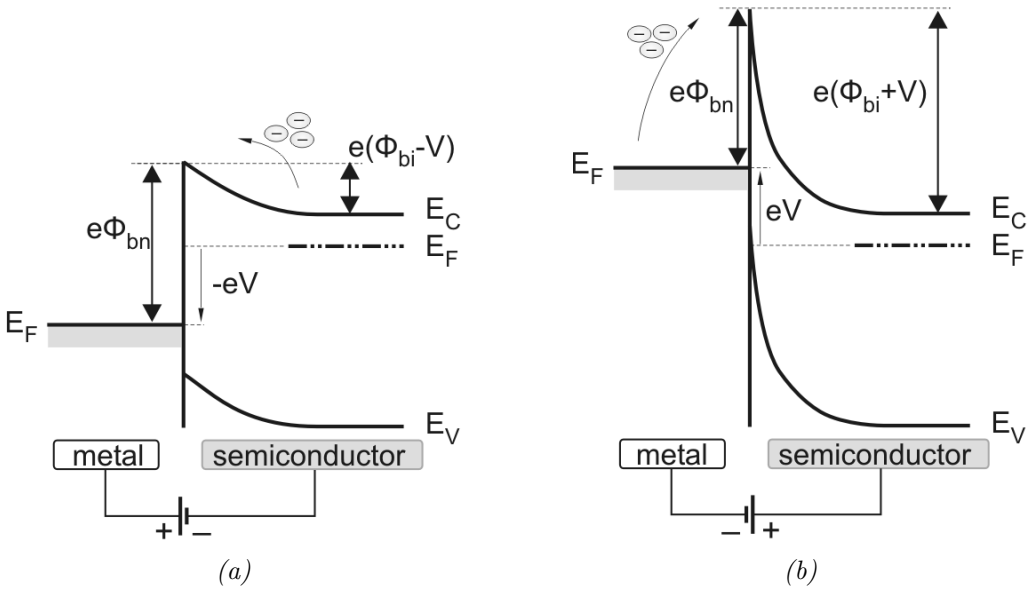


Figure 1.3: Band diagrams for Schottky barriers with positive (a) and negative bias (b) [9]

In the case of a voltage V, electrons are attracted by the positive terminal, lowering the built in potential V_D with V yet Φ_B remains the same. Electrons from the semiconductor can overcome the barrier more easily, resulting in a positive breakthrough.
When a negative voltage V is applied, the bands are further deformed and the potential V_D is increased by V.
With an applied bias Eq. 1.3 can be rewritten to Eq. 1.4:

$$W_D = \sqrt{\frac{2\epsilon}{qN_d}(V_D - V)} \tag{1.4}$$

It is clear that a negative bias will increase the depletion width, making it more difficult for electrons to tunnel through the barrier. A large negative bias, however, will decrease the barrier width (not the depletion width) making it easier for electrons to tunnel through, this results in a negative breakdown.

1.2.3 Ohmic barrier

It was already stated that heavily doped semiconductor/metal junctions could result in Ohmic behaviour. There is another way to create an Ohmic contact between the semiconductor and a metal, when $\Phi_m < \Phi_s$ electrons can easily go from the metal to the semiconductor and back, there is no potential to overcome.

1.3 Memristor

1.3.1 How the memristor was found

Four fundamental electrical variables are known: current, voltage, charge and flux. For a long time, only three fundamental passive circuit elements were known connecting these variables: the resistor, the inductor and the capacitor. Every component links two variables as can be seen in Fig. 1.4.

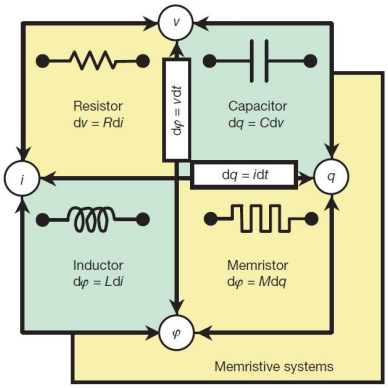


Figure 1.4: The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor [2].

A long time the connection between flux and charge was unknown, no fundamental circuit element could link them. In 1971 the Chinese American theorist Leon Chua came up with the the theory that for symmetry reasons a relation between these two variables should exist [1]. He credited the relation to a fourth passive electrical component, that was unknown until then. It was named 'fundamental' because its properties could not be imitated by a combination of the other fundamental components. The name 'memristor' was connected to this device, because of the property of behaving like a non-linear resistor with memory. In practice, this means that the resistance varies depending on the amount of charge floating through. When the charge flows in one specific direction, the resistance increases, when the charge flows in the opposite direction, the resistance decreases. A measure for this variation is given by the 'memristance', a specific property of a memristor. The memristance is defined as follows:

$$M(q) \equiv \frac{d\varphi}{dq} \tag{1.5}$$

In the case of linear elements, M is a constant and the memristance is identical to the resistance. If M is itself a function of q, yielding a nonlinear circuit element, the situation is more interesting [2].

One of the resulting properties of memristive systems is the existence of a hysteresis effect. When a positive voltage is applied to a memristor, a positive current will flow which will decrease the resistance (V/I) of the material, and the current will become higher. When the voltage is decreased again, the current will decrease too, but slower because the resistance still decreases. When the voltage is negative, the resistance will increase again due to the opposite direction of the flow of charge, and the current decreases. When finally the voltage goes back to zero, the resistance will increase slower until it is back at

its original value. Depending on the frequency, the loops will be flatter or more convex. When the frequency increases, per loop less charge will flow through the system, so the resistance will change less. At very high frequencies, memristive theory predicts therefore the hysteresis effect will degenerate, resulting in a straight line representative of a linear resistor. This hysteresis effect is shown in Fig. 1.5.

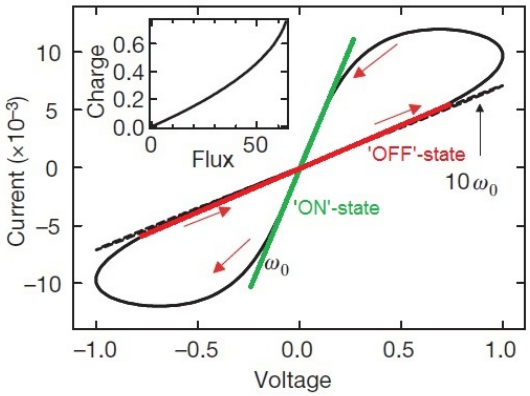


Figure 1.5: The hysteresis effect in a memristive device. I is shown as a function of V. As can be seen, the resistance depends on its past (adapted from [2]).

Besides the fact that the resistance of a memristor can change, the component has the important property that it 'remembers' its resistance. When for a certain time no current passes through the memristor, the memristor will keep its value. To this property the memristor owes its name, a combination of 'memory' and 'resistance'.

In 2008, researchers in the HP laboratories deposited titanium on a layer of platinum oxide. What they found doing measurements was a lot of hysteresis so they decided to determine the structure of their layer. Unintentionally, the titanium had oxidized with oxygen from the platinum oxide electrodes and formed TiO_2 at the interface of the two layers. Looking into this layer, they found two regions: one region with pure titanium dioxide (TiO_2) and one region with oxygen deficient titanium dioxide (TiO_{2-x}). The oxygen deficient layer contains about 5% less oxygen, so X is in the order of 0.05. For a long time, the researchers did not know what kind of behaviour they measured, until one of them coincidental found the article of Leon Chua [12]. The researchers of HP had unintentionally made a memristor.

In 2010 researchers in London tried to remake the memristor of HP [3], but instead of placing a layer of (TiO_{2-x}), they placed a layer with excess oxygen atoms, (TiO_{2+x}). Both layers were made with radio-frequent sputtering at room temperature. The bilayer was placed between two Ti/Pt electrodes and measured with a Semiconductor Characterisation System. In this case, hysteresis was also found and the material was determined to be a memristor.

Taking resistive switching into account, the operation of these memristors can easily be explained. In the case of the memristor of HP, the region with oxygen vacancies contains a lower resistivity than the region without, see also Fig. 1.6. An external field causes the vacancies to move. The total resistivity of the material is the sum of the resistance of both

regions over the full length of D. Depending on the direction of the field the region with dopants will become larger or smaller, causing the total resistance to decrease or increase, respectively.

Determining the memristance for the found device, showed for the simplest case of ohmic electronic conductivity, linear ionic drift in a uniform field with average ion mobility μ_v and $R_{on} \ll R_{off}$, the following relation [2]:

$$M(q) = R_{off} \cdot \left(1 - \frac{\mu_v R_{on}}{D^2}\right) \tag{1.6}$$

Here D is the thickness of the film. The square dependence on this thickness D is one of the main reasons why it took very long to find a real memristor (based on oxygen vacancies). Memristance is a million times better observable at the nanometer scale than at the micrometer scale and nearly unnoticeable at the millimetre scale or bigger [12].

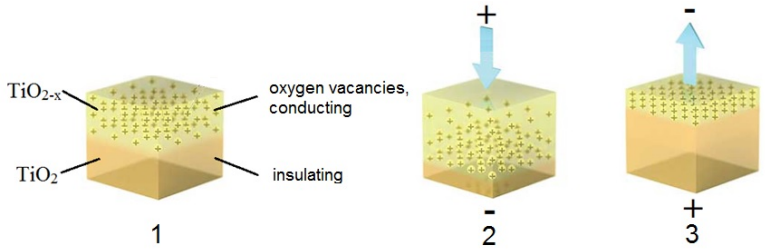


Figure 1.6: The operation of a memristor. 1: The memristor consists of two layers, the layer with oxygen vacancies has a much lower resistivity. 2: A positive bias will cause the holes to move through the material, increasing the region of lower conductivity, causing the total resistance of the material to decrease. 3: A negative bias will cause the holes to move to one side of the material, decreasing the region of lower conductivity, causing the total resistance to increase (adapted from [12]).

1.3.2 Criticism

Apart from the excitement about the found memristor [12], Meuffels and Soni doubt the HP-memristor to be a real memristor [13]. The memristor shown in Fig. 1.6 has a "built-in" chemical potential. As long as the oxygen vacancy concentration gradient exists inside the material, the material is concerned with a flux of the involved species (the electrons and the charged oxygen vacancies) which will recombine if they meet. As pointed out, a memristor must exhibit the "no energy discharge property", or in other words, when V(t) = 0 V, I(t) = 0 A and vice versa. This rule is clearly violated as long as a chemical concentration gradient exists somewhere in the device material. The HP-memristor would therefore behave like a chemical capacitor until it has reached equilibrium state.

Meuffels and Soni further came up with a thought experiment [13]. The memristance of a device is given as $R(w(t))$ ($w(t)$ is the internal state variable at time t). After an infinitesimal time interval of length dt, the memristance has changed from $R(w(t))$ to a value of $R(w(t + dt))$. Both states must be real states in a thermodynamic sense and both states must be correlated to a physical modification in the system (in case of the HP-memristor to the different size of the dopant region). Otherwise, no change in resistance would be observed, thus both states must be some type of equilibrium states for

the system. When a certain amount of charge flows through the memristor, the state changes and the new state sort of stores the "information" of the charge that has passed through. Analysing this system in terms of thermodynamics and assuming the temperature T and the pressure p to be constant, the Gibbs free energy G would be the relevant thermodynamic state function. The equilibrium states of our memristor ($R(w(t))$ and $R(w(t+dt))$) have a constant amount of Gibbs free energy, otherwise the device would arbitrarily fluctuate ending up in a very noisy resistor. This means that the memristor or "information" states must be separated from each other by Gibbs free energy barriers. Any change of state requires the input of "thermodynamic work". Landauer's principle requires at least an amount of $RTln2$ of work is done, (where R is the molar gas constant) to erase some "information" from a memory device. In other words, to go from $R(w(t))$ to $R(w(t+dt))$, at least $RTln2$ is needed. So far so good, but Meuffels and Soni point out in their calculations that for the memristor there is no restriction in minimum amounts of energy to change the states and the memristor therefore violates Landauer's principle [13]. Finally, the violation of the "no energy discharge property" causes the memristor to be unable to store its "information", as the gradient currents will change the state.

The memristor device based on oxygen vacancies is not entirely perfect: it loses some information when powered off and may be a little bit different from what Leon Chua described [1]. Nevertheless it still exhibits most of the properties predicted and a lot of applications can be thought of, as will appear in the next section.

1.3.3 Applications

As discussed above, apart from the capacitance, resistance and inductance and the fact that no different memristors behave in a different way, a lot of applications can be thought of. Two of these applications will be highlighted to emphasize the importance and relevance of new research into these kinds of materials.

Memory devices

One of the first applications the researchers of HP introduced for their memristor was the use in a memory device [12]. The memristors are placed in a matrix in which every memristor is bound by two crossing nanowires. In this way, every memristor is controlled by applying a voltage over the two attached crossing wires, as can be seen in the image below (Fig. 1.7). To close the switch, a positive voltage is applied across the two wires to be connected. To open the switch, the voltage is reversed.

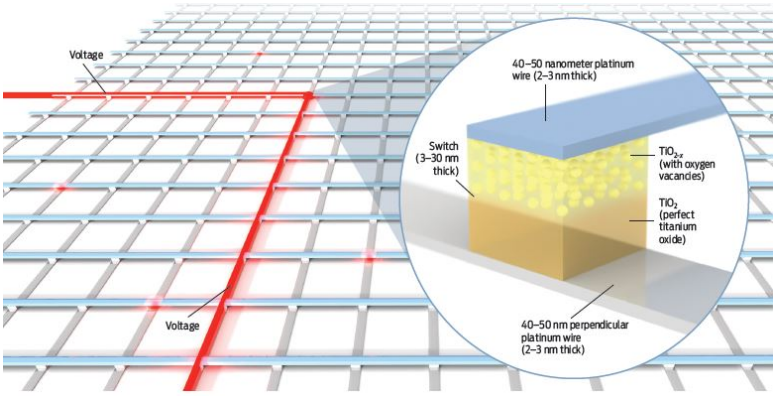


Figure 1.7: Design for a memory device based on memristors. By applying a voltage over the two connected wires, the resistance of the memristor can be changed (writing) or the resistance can be measured (reading) [12].

A big advantage of memory based on these materials is that it only costs energy to read and write information. In the meantime (neglecting diffusive currents) the resistance remains the same so no power is needed. This also means that in case of a power cut, no information from the memristor memory device will be lost and when the power is back again, no recovery procedures are needed. According to the scientists at HP, the wires and switches can be made very small, eventually down to a width of around 4 nm. Then multiple crossbars could be stacked on top of each other to create a very high density of stored bits. They finally showed that a circuit could be shrunk by a factor of about ten in area, just by replacing several specific transistors with a crossbar of memristors. The specifications of the system even improved in terms of its speed relative to power-consumption performance [12].

Neuromorphic circuitry

A very interesting feature of memristors is that they more or less behave the same like synapses in the human brain. Neurons (brain cells) are connected to each other with synapses. The Hebbian theory states that signals between two neurons which are often active at the same time are amplified [14]. So, in essence, a synapse is a two-terminal device whose resistance can be tuned by the charge flown through it, or as one can imagine, a biological version of a memristor. This analog makes it attractive to emulate synaptic functions with solid-state memristor devices. One of the key bottlenecks to emulate the biological systems in hardware is the large connectivity among neurons. For example, a neuron can be connected to 10^4 other neurons via synapses [15][16]. Neuromorphic circuitry with memristors promises a lot of possibilities, among others self learning computers.

1.4 Materials

In this report $SrTiO_3$ is considered as a material for a memristor, this section provides basic information regarding the used materials.

1.4.1 $SrTiO_3$

Strontiumtitanate, $SrTiO_3$ or STO is a material with a perovskite structure. This means an ABO_3 structure as in Fig. 1.8. Because of this structure STO is often used as a substrate for the epitaxial growth of high temperature superconductors. Besides, STO has applications in the fields of ferroelectricity, optoelectronics and macroelectronics. STO has a very larger dielectric constant, ~ 300 at room temperature and much larger at lower temperatures ($\sim 10^4$)[17]. The lattice parameter of STO is 3.928 Å[18]. STO undergoes a metal insulator transition upon light doping. STO is a typical nonpolar band insulator with an indirect band gap of 3.27 eV, but STO can show a metallic phase with a exible tunability in electrical conductivity depending on the concentration of O_3 [19]. This transition property combined with the fact that STO is thermal and chemical very stable [19], makes it in theory a very suitable material for application in a memristor.

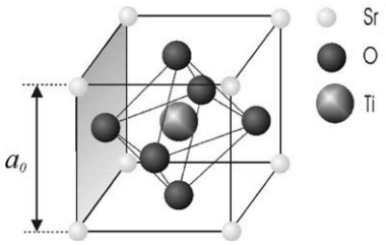


Figure 1.8: Perovskite structure for STO [20].

1.4.2 Nb:$SrTiO_3$

Niobium doped STO or NSTO is STO where some of the Ti atoms are replaced by Nb atoms. Since the Niobium ion has a different charge than Titanium (Nb^{5+} vs Ti^{4+}), electrons are free to move around, making the NSTO electrical conductive. The electrical conductivity and the good conditions for epitaxial (lattice parameter of 3.949 Å- 3.968 Å) growth make NSTO a good material for electronics substrates [18].

1.4.3 $(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}$

$(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}$ or LSAT is material commonly used as a substrate for thin films in superconductivity and ferroelectric applications. Since it can be grown at a relative low cost and has a good lattice match with many oxide materials lattice parameter of 3.868 Å, it is believed to replace $LaAlO_3$ and $SrTiO_3$ substrates. LSAT has only a small lattice mismatch with STO and these substrates are known to be well insulating [21]. LSAT is therefore ideal as an insulating substrate for STO.

Chapter 2

Design for the STO memristor

Based on the memristor design of HP [12] the design of Fig. 2.1 is proposed for STO. Because of the conductive properties and because it has the same lattice parameters, the STO is grown on a NSTO substrate.

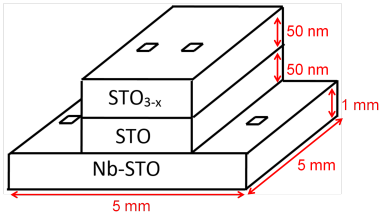


Figure 2.1: The design for a memristor based on STO. A common 5x5x1.0 mm NSTO substrate is used on which two layers of STO are deposited, one with and one without oxygen vacancies. The order of these two layers is arbitrary, just as the thickness of 50 nm. This thickness is chosen as a starting point because it is easy to grow with the help of PLD. Compared to the memristor of the researchers in London (30 nm [2]) these layers are slightly thicker. This is to prevent the measurement equipment to pierce through the layer. Measurements need to verify if these are proper dimensions. The small squares are contact points.

Regarding the design of Fig. 2.1, the following conditions should apply:

- **The contact points on the STO layer** should make Ohmic contact with the material, so it does not disturb the electric behaviour of the memristor.
- **The STO layer with oxygen vacancies** should be conductive.
- **The STO layer without oxygen vacancies** should not be conductive, or at least have a very high resistance.
- **The combination of STO with and without oxygen vacancies** should show memristive behaviour, or in other words:
  - A pinched hysteresis loop for I-V measurements.
  - The area inside the hysteresis loops will decrease for higher frequencies.
  - The hysteresis loop will become a straight line for very high frequencies.

- **The interface of STO with NSTO** should make Ohmic contact.
- **The NSTO substrate** should be conducting.
- **The contact points on the substrate** should make Ohmic contact with the material.

Chapter 3

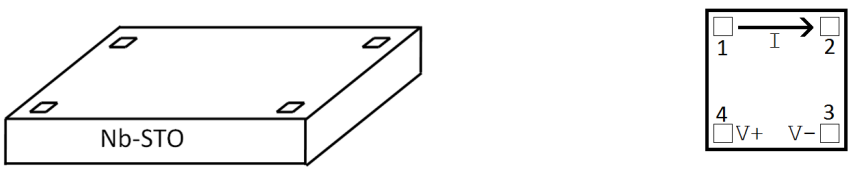
Measurements and Results

To be able to fabricate the memristor discussed in the previous chapter, the separate layers need to be characterized. This chapter focusses on these layers with the exception of the STO layer with oxygen vacancies. The fabrication of these layers and the conducted experiments on them will be described and discussed in this chapter.

All measurements are performed by a Keithley 2401 Low Voltage SourceMeter Instrument, connected to a probe station with soft gold coated needles. Soft needles are used to minimize damage to the sample. Different LabView programs are used to perform voltage and current sweeps. All measurements are performed in air at room temperature.

3.1 NSTO substrate

A 5x5x1.0 mm, (001) oriented, 0.5 wt% niobium doped STO substrate of manufacturer CrysTec was used. The substrate was treated with acetone and ethanol to clean the surface. A thin film of 17 µm photoresist was applied using a spinner at 6000 rpm. Using a shadow mask, four contact points of (300x300 µm) were made. After that 4 nm of the top layer was etched away by argon etching to remove all dirt and water molecules that were left. Subsequently a layer of 2 nm titanium was deposited by RF sputtering. On top of this, 120 nm of gold was sputtered. Titanium was used, because it has a better bond with the substrate than gold. After chemical lift-off with acetone and ethanol, the sample looked like the sketch displayed in Fig. 3.1a.



(a) *(b)*

Figure 3.1: Schematic views of the NSTO substrate, with in 3.1b a view from the top.

3.1.1 Van der Pauw measurement

After preparing the sample, a Van der Pauw measurement was performed on the substrate. This method eliminates contact resistance and is used to determine sheet resistivity (for a more detailed explanation of the Van der Pauw method, see Appendix B). The setup displayed in Fig. 3.1b shows the current flowing from contact point 1 to 2 with the voltage drop measured over contact point 4(+) and 3(-), this is referred to as I,$V_{12,43}$.
Eight measurements were performed by sweeping the current from 0 A to 0.1 A, four in the horizontal direction, i.e. I,$V_{12,43}$,I,$V_{21,34}$,I,$V_{34,21}$ and I,$V_{43,12}$, and four in the vertical direction, i.e. I,$V_{14,23}$,I,$V_{41,32}$,I,$V_{23,14}$ and I,$V_{32,41}$. For each orientation the mean of the four measurements was taken, as is common in a Van der Pauw measurement. The results are shown in Fig. 3.2.

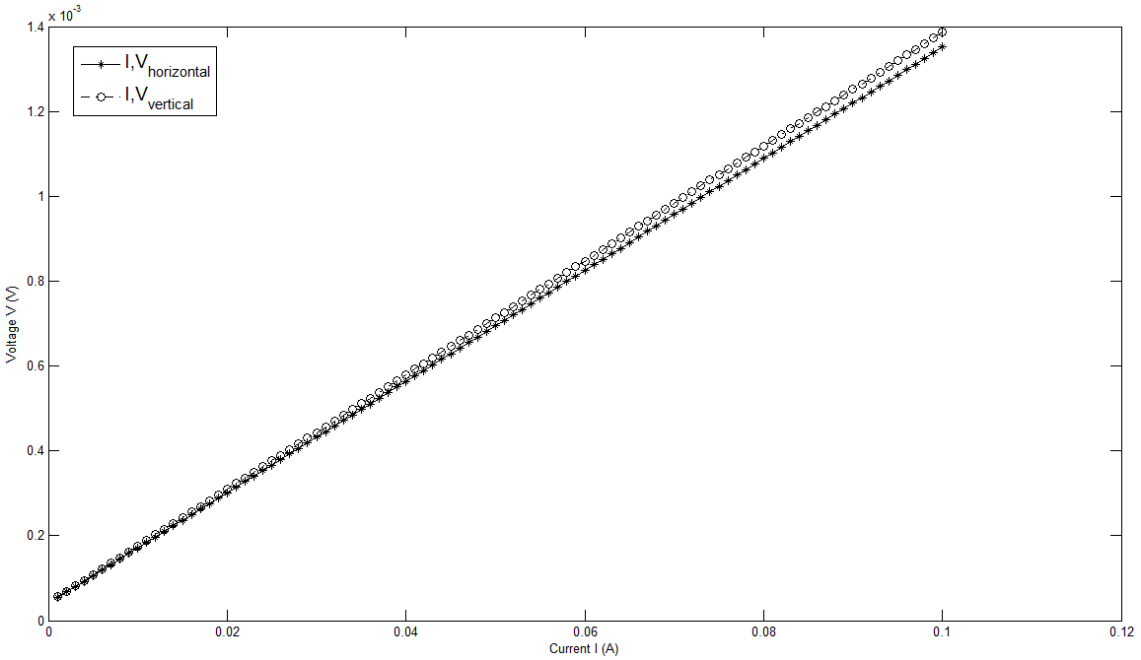


Figure 3.2: I,V curves for the Van der Pauw measurements performed on the NSTO substrate, where $I,V_{horizontal}$ and $I,V_{vertical}$ are the means of the measurements in horizontal and vertical direction respectively. $0 \leq A \leq 0.1$ *with source delay* t_s*=0.01 s.*

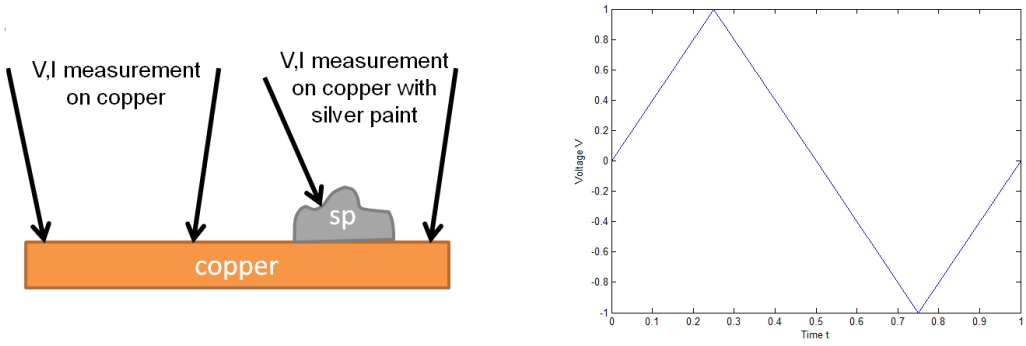
The resistance was determined from the slopes of the graphs:

$$R_{horizontal} = 0.0131\ \Omega$$
$$R_{vertical} = 0.0135\ \Omega$$

The results are within a 5% range of each other indicating an accurate Van der Pauw measurement was performed. Clearly the substrate shows Ohmic behaviour and has a low resistance making it a good substrate for further experiments.
In a previous study by Reinier Nielen, a resistance of R=0.0148 Ω was found for STO/NSTO. Comparing this result to the measured resistance for NSTO confirms Reiniers presumption that he measured the NSTO instead of the STO/NSTO layer (by piercing through the STO layer with the probes) [22].
Note that the curve does not pass through the origin, this is most likely caused by either the Keithley or the LabView program.

3.1.2 Influence of contact materials

The upcoming experiments are simple two-terminal measurements from top to bottom (perpendicular to the surface). To prepare the substrate for these measurements it was glued on a copper plate (10x10x1.0mm) with silver paint. To rule out any behaviour caused by these additions, measurements were performed on the copper and silver.
The first measurement was performed on copper. The resistance was measured with four different distances between the probes (2, 4, 6 and 8 mm) to investigate homogeneousness. The second measurement was on copper with silver paint. Fig. 3.3a shows both setups. Since there is a need to check for hysteresis, both measurements were performed by sweeping the voltage Fig. 3.3b shows the applied voltage.



(a) *(b)*

Figure 3.3: Schematic view of the setup (a) and the applied voltage characteristic (b)

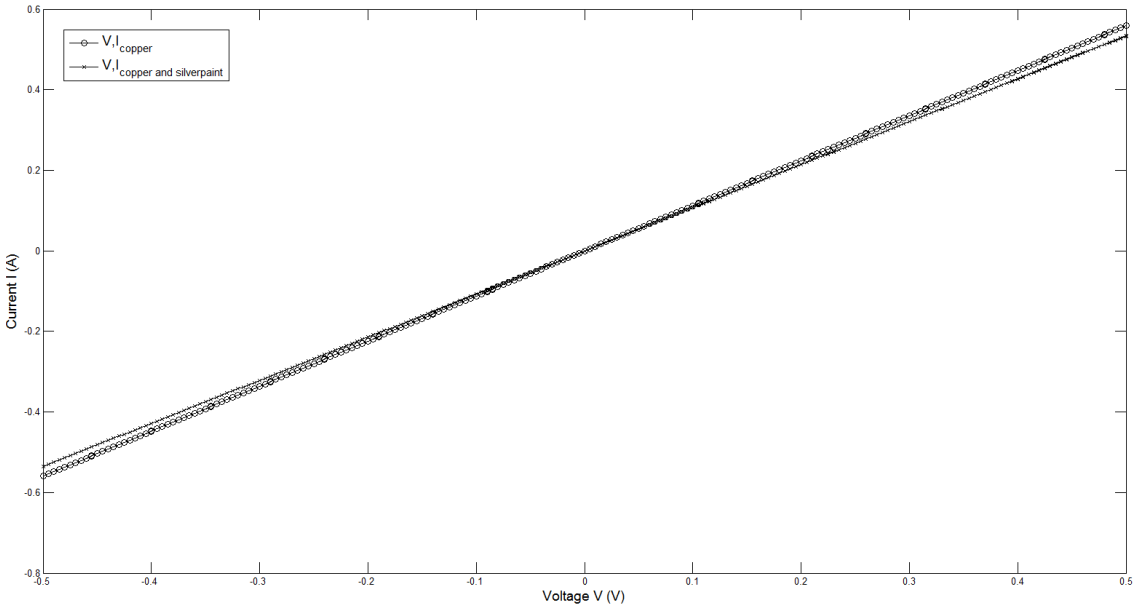


Figure 3.4: V,I curves for measurements on copper with probe distance d = 8 mm and for silver paint on copper.

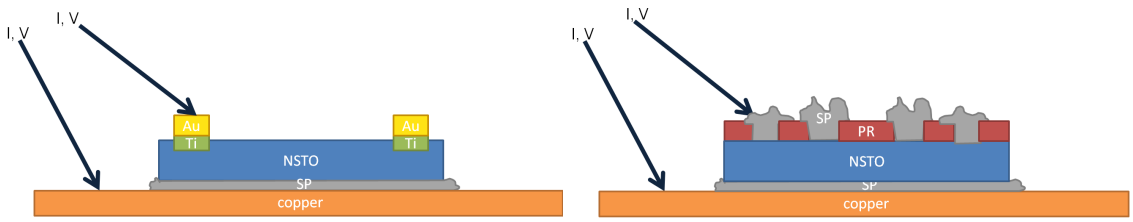
Since the four measurements on copper were very similar, only the 8 mm measurement is displayed in Fig. 3.4. From this figure can also be deduced that the resistance for silver on copper is slightly larger than the resistance of copper, as expected. Both graphs are linear so the Ag/Cu interface behaves Ohmic. The measured resistances are:

$$R_{Cu} = 0.8935\ \Omega$$
$$R_{Ag/Cu} = 0.9350\ \Omega$$

The resistance for copper is relatively high compared to literature values [23]. This originates from the contact resistance with the probes and the resistance in the wires from the probes to the Keithley sourcemeter. Also Oxidation visibly occurred while heating the copper plate so this may be of influence as well.

3.1.3 Au/Ti/NSTO and Ag/NSTO

To investigate the electrode/substrate interface, measurements were performed on the earlier described Au/Ti contacts (see Fig. 3.5a). After these measurements the contacts were replaced by silver contacts which will be described later on, the reason to use silver contacts will become clear in Section 3.2.



(a) *(b)*

Figure 3.5: Schematic side view the Au/Ti/NSTO (a) and Ag/NSTO contact setup (b).

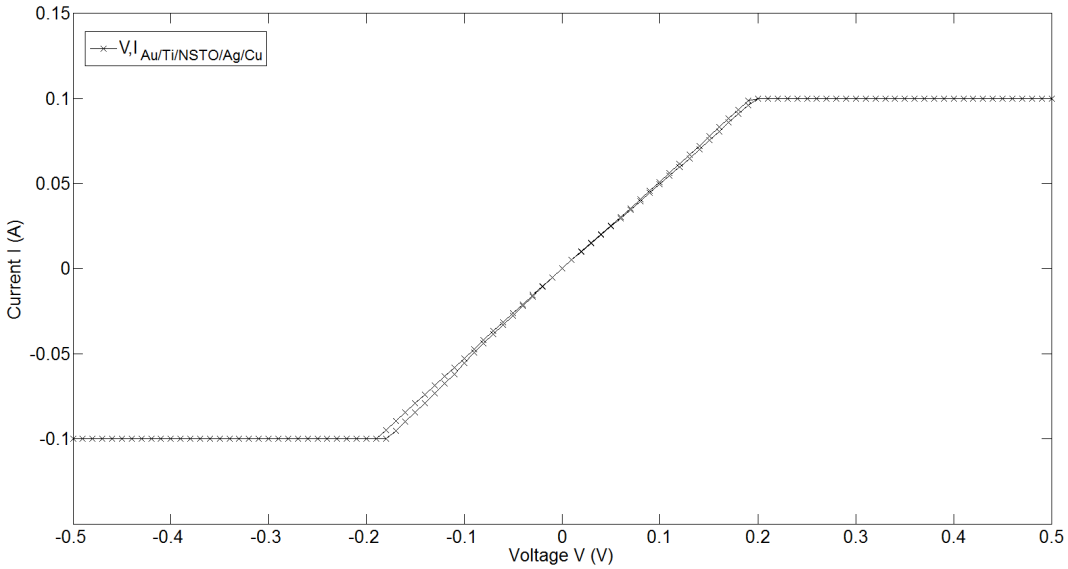
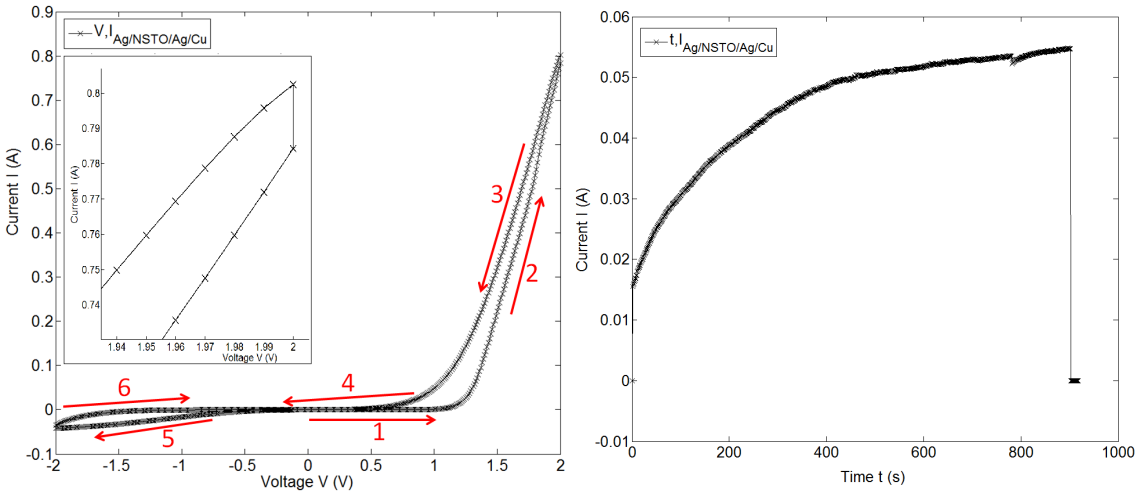


Figure 3.6: V,I curve for NSTO with $-0.5 \leq V \leq 0.5$, step voltage V_s=0.01 V, source delay t_s=0.01 s and compliance current I_c=0.1 A. When compliance is reached, the voltage stops increasing.

For both the Au/Ti and Ag contacts, voltage sweeps were performed on several contacts. Fig. 3.6 shows the result of one of the measurements where the Ohmic behaviour for the Au/Ti can be seen. Other contact points show the same fashion with one exception. In that measurement the probe visibly pierced through the contact resulting in non-Ohmic behaviour. The fact that Au/NSTO is the resulting contact interface (gold coated probes) leads to the suggestion that the thin layer of Ti also influences the measurements. Measurements on the least damaged contact show a resistance of

$$R_{Au/Ti/NSTO/Ag/Cu} = 1.9046\ \Omega$$

After completing the measurements on the Au/Ti contacts the sample was thoroughly cleaned in acetone and ethanol. A thin film of 17 µm photoresist was applied using a spinner at 6000 rpm. With photolithography, four small squares (300x300 µm) of photorisist were removed. After this, the substrate was heated for 20 minutes at 200 °C to solidify the layer of photoresist. This is a necessary step to prevent the photoresist from solving into the silver paint's solvent. With a small brush, contact points of silver paint were applied to the small squares. Despite the different sizes of the blobs of silver paint, all four points have the same contact surface. For a schematic view refer to Fig. 3.5b. The same type of V,I sweep was performed on this sample, Fig. 3.7a shows the results.



(a) *(b)*

Figure 3.7: V,I curve for NSTO with $-2 \leq V \leq 2$, step voltage V_s=0.01 V, source delay t_s=0.01 s and compliance current I_c=1 A, the inset displays an enlarged view for V>1.94 V (a). (b) shows the t,I curve for NSTO with an applied constant voltage V=1.5 V and a time delay of t_s=1 s for measuring the current.

Clearly this graph shows completely different behaviour from the previous results. Until V≈1.25 V, no current flows. For higher voltages, the current increases very fast. When the voltage is swept back, the current decreases but not as fast as it increased, indicating a lower resistance. At V≈0.75 V the current the resistance is very high. When the voltage reaches V≈-0.75 V, a low negative current is measured, which stops when the voltage is increased again. It can be concluded that the graph shows diode-like characteristic with a positive breakdown at V≈1.25 V. The same value was obtained in repeated measurements. In these measurements it also appeared that the negative breakdown is at V≈5 V. The obtained behaviour can be explained by the forming of a Schottky barrier at the Ag/NSTO interface (refer to Section 1.2). The graph also shows hysteretic behaviour

which was further investigated by applying a constant voltage of V=1.5 V. This voltage was maintained for 900 seconds and the current was recorded. On the first hand the graph obtained may look like an electrical response to the applied electrical field, however experiments in which a voltage stair (voltage builds up to V=1.5 V in 10 seconds) was applied instead of a step show no different curves.
The hysteretic behaviour can be explained with the help of Fig. 3.7b. A short time at a given voltage immediately lowers the resistance thereby resulting in the observed hysteresis. It can also be observed that no charge builds up since removal of the electrical field instantly results in zero current.
The inset in Fig. 3.7a shows a jump at the turning point of the voltage sweep (in this case V=2 V), this can also be explained by Fig. 3.7b; at the turning point the voltage remains constant because the measuring program measured two points. In addition the Keithley caused a short delay due to internal switching.

3.2 STO layer without oxygen vacancies

In this section the measurements on STO are described. Different types of contact materials are considered: gold/titanium (Section 3.2.1, 3.2.2 and 3.2.3), silver paint (Section 3.2.4) and titanium (Section 3.2.5.

All thin films of STO were deposited by pulsed laser deposition with equal parameters. An STO single crystal was used as target. The laser pulse frequency was 4 Hz, and the pulse energy density was about 1.5 J/cm^2. During the deposition process, a substrate temperature 740 °C and an oxygen pressure of 1 millibar were set. The deposition rate of STO in the CombiSystem was determined to be 0.46 nm/s. To obtain a layer thickness of about 50 nm, deposition lasted for 108 s. After the deposition of a layer, the substrate temperature was decreased to 600 °C, where the annealing process started. The oxygen pressure was raised to 1 bar and for 15 minutes the temperature stayed at 600 °C. After this step the temperature was further decreased with 10°C per minute to 450 °C. After a 30 minute anneal, the sample was brought back to room temperature.

3.2.1 Van der Pauw measurement

A layer of 50 nm STO is epitaxially grown on top of a 5x5x1.0 mm, (001) oriented, 0.5 wt% Nb:$SrTiO_3$ substrate. Using the same procedure as described in Section 3.1 four Au/Ti contact points were sputtered.
Since a homogeneous layer of STO is assumed, a Van der Pauw measurement was prepared again. The expectation, however, was that the resistance would be very high and might even be out of range. A lot of different curves and types of behaviour were obtained so a Van der Pauw measurement was not possible. One important result is displayed in Fig. 3.8.

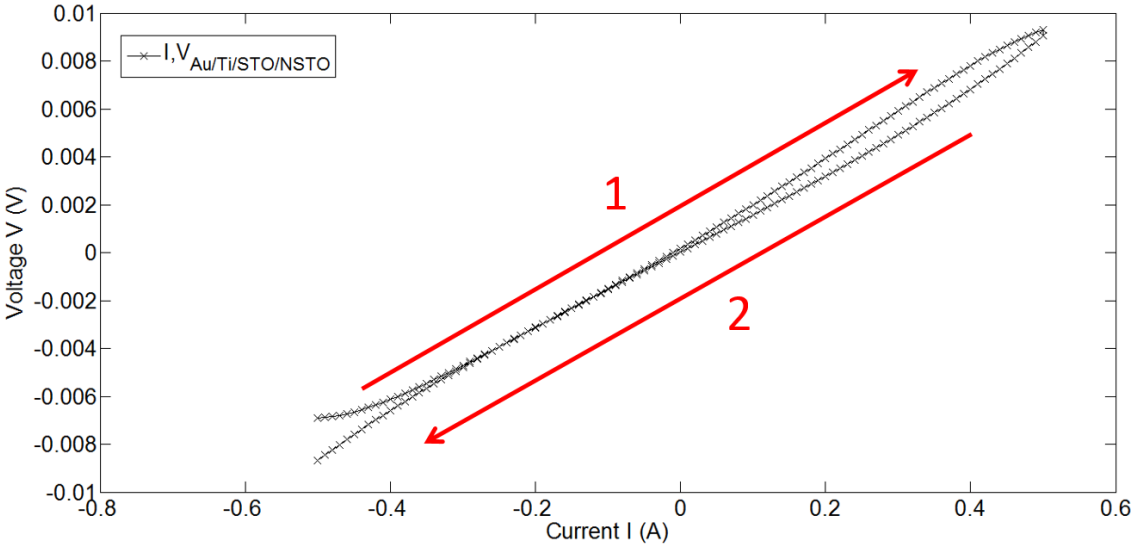


Figure 3.8: I,V curve for a Au/Ti/STO/NSTO four point measurement with $-0.5 \leq I \leq 0.5$*, step current* I_s*=0.005 A and source delay* t_s*=0.01 s.*

The measurement started at I=-0.5 A and made a sweep to I=0.5 A and back. Starting at I≠0 results in slight non-linear behaviour, this is a response to the sudden presence of a current. When the resistance is measured a value of

$$R_{Au/Ti/STO/NSTO} = 0.017 \pm 0.001\ \Omega$$

is obtained. This result is very similar to the results obtained in Section 3.1.1. This indicates that the probes pierced through the STO layer and measured the substrate.
There were also measurements performed in a smaller current range, these were very different and are discussed in Appendix C.

3.2.2 Au/Ti/STO/NSTO/Ag/Cu

The first approach on measuring the STO layer was a Van der Pauw setup, this proved to be a good way to characterize the NSTO substrate but seemed less fruitful for the STO layer. The Van der Pauw measurement required four probes not piercing through the contacts and/or the STO layer. There was also a need to measure through the STO layer and not just on the surface. This is why it was decided to mount the sample on a copper plate like the substrate was in Section 3.1.3.
Now two terminal measurements could be performed. STO is considered an insulator and contact resistance appeared to be in the order of 1 Ω (refer to Section 3.1), so $R_{contact} << R_{STO}$ and contact resistance could be neglected. These measurements reduced the probability of piercing through the layer (four probes on contact points versus one probe on a contact point). Also electrical contact could be verified more accurately by placing two probes on the same contact point and monitoring the conduction. A schematic view of the sample on the copper plate is given Fig. 3.9.

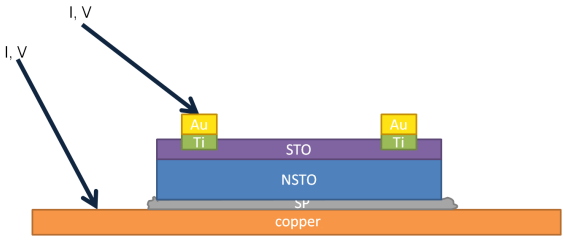


Figure 3.9: Schematic side view the Au/Ti/STO/NSTO contact setup.

In previous measurements it was unclear if the current provided by the Keithley actually went through the STO layer so the method of measuring was changed. Instead of sweeping the current, the voltage was swept, producing an electric field. The resulting current was recorded. The voltage was swept from negative value to either zero or a positive value. A lot of measurements were performed before the displayed curves. After moving the probes multiple times, some Ohmic behaviour was observed. The results are displayed in Fig. 3.10.

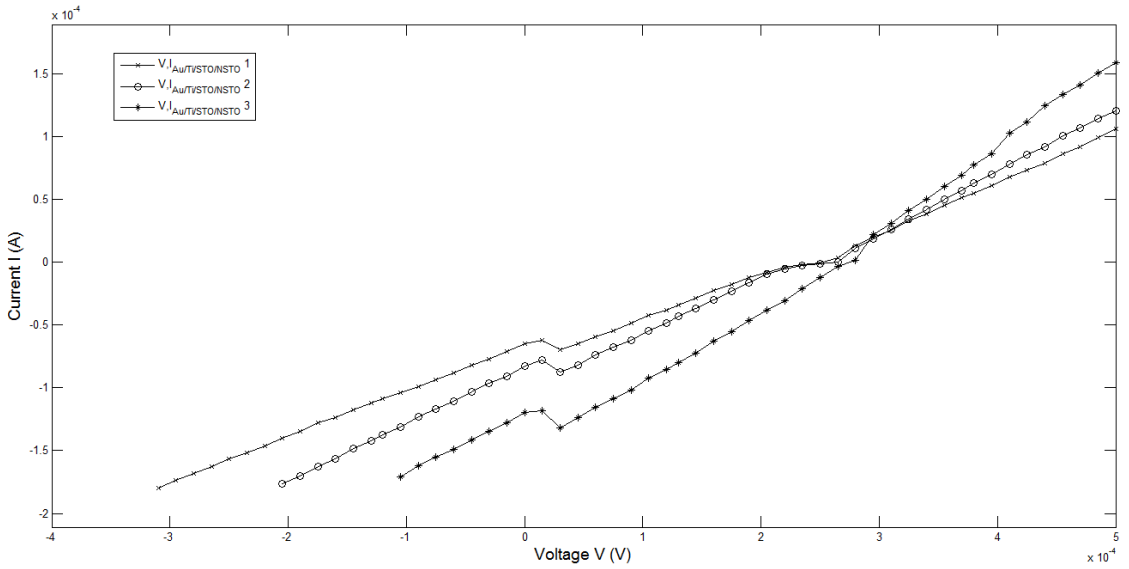


Figure 3.10: V,I curve for a Au/Ti/STO/NSTO four point measurement with $-3 \cdot 10^{-4} \leq V \leq 5 \cdot 10^{-4}$*, step voltage* V_s*=1.25·10-4 V and source delay* t_s*=0.1 s.*

The three curves are consecutive measurements, the resistance decreased after each measurement. All measurements showed a 'jump' at V=0 V, also for V=0 V, I≠0 A. The resistances measured were:

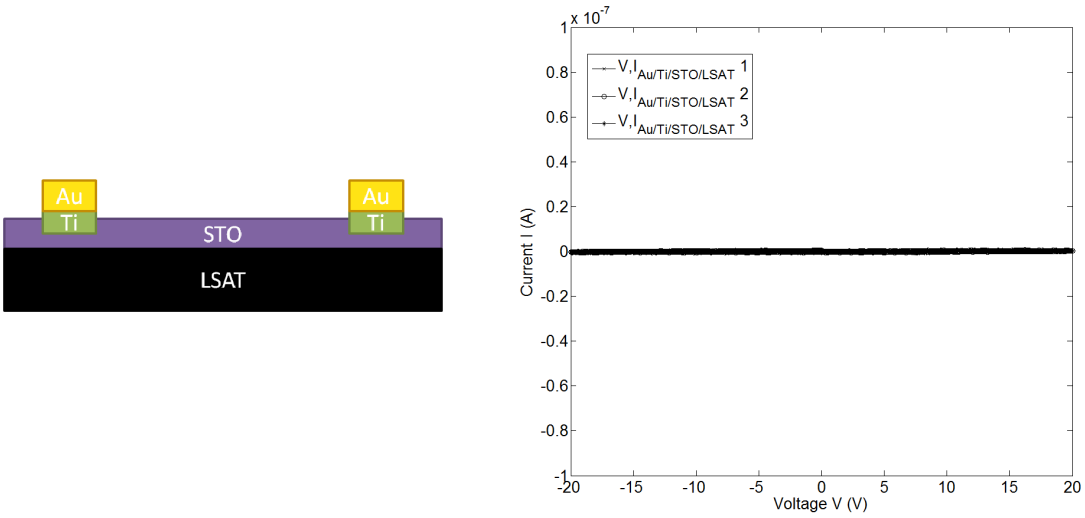
$$R_1 = 2.994\ \Omega$$
$$R_2 = 2.475\ \Omega$$
$$R_3 = 1.815\ \Omega$$

These results are in the same order of magnitude as the result obtained as in Section 3.1.3 and thus indicate that the substrate was measured again.

The conclusion was drawn the method of measuring was faulty, i.e., a proper sweep should start at V=0 V, move up to a positive voltage, go back to a negative voltage and end at V=0 V as displayed in Fig. 3.3b. Since there was no program available that was able to perform these kind of sweeps, a new program had to be written in LabView. All further measurements were performed using this program (and small adaptations of it, e.g., for a constant voltage measurement).
Note that the measurements discussed in section 3.1.2 and 3.1.3 were also performed with this 'new' program. Chronologically these measurements were performed after the measurements discussed in Section 3.2.4, but for the sake of clarity the measurements on the substrate were presented earlier in this report.
Finally, to prove that the substrate was measured instead of the STO layer the measurements discussed in Section 3.2.3 were conducted. Together with the results from Section 3.1.1, this should be sufficient to confirm the hypothesis of measuring the substrate.

3.2.3 STO on LSAT, gold contact points

A new layer of 50 nm of STO is epitaxially grown on LSAT by using Pulsed Laser Deposition. The substrate used was a 5x5x1.0 mm LSAT substrate, manufactered by CrysTec. On top of the substrate, again four Au/Ti contact points were sputtered using the same procedure as described in Section 3.1. A V,I sweep as described in Fig. 3.3b was applied. As LSAT is not conducting, any conduction in this substrate originates from the STO layer, even if the contact points pierce through (into the non-conducting LSAT). The setup and the measurements are shown in Fig. 3.11.



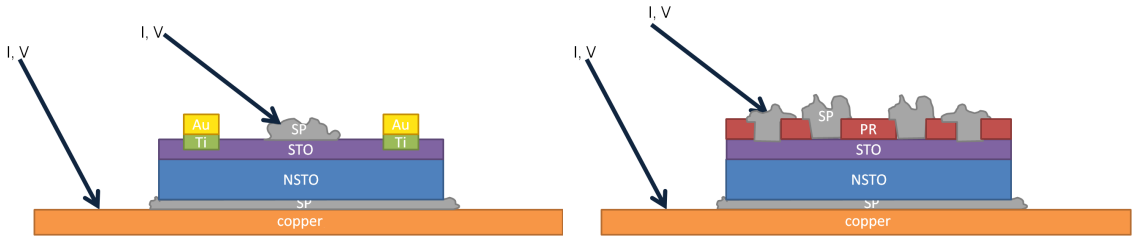
(a) *(b)*

Figure 3.11: Schematic view of the Au/Ti/STO/LSAT setup (a) and the V,I curve forAu/Ti/STO/LSAT with $-20 \leq V \leq 20$, step voltage V_s=0.1 V and source delay t_s=0.01 (b).

Fig. 3.11b shows that no conduction is measured, even when + or - 20 V is applied. Contact between the probes and the contact points has always been verified visibly and electrically. More comments on these measurements can be found in Appendix C. From these measurements can be concluded that the Ohmic measurements obtained before were due to piercing through the contact points.

3.2.4 STO on NSTO, silver contact points

The previous section concluded that Ohmic measurements were a result of piercing through the layer. Thicker contacts were needed so piercing through would be less likely. As a small experiment a droplet of silver paint was deposited on the surface of the sample with four gold contact points, obviously the layer was cleaned first with acetone and ethanol. Fig. 3.12a shows a schematic view of the setup. Again the voltage was swept as in Fig. 3.3b. The results were quite remarkable compared to all previous measurements, diode-like behaviour with hysteresis was observed. The results were very reproducible and more contact points were needed. A new STO layers was deposited on NSTO using the same procedure as previous depositions. To acquire the silver contact points, the same procedure as described in Section 3.1.3 was used. Ultimately 16 contact points were made, again the contact surface was the same for every contact point, a schematic view of this configuration is displayed in Fig. 3.12b.



(a) (b)

Figure 3.12: Schematic view of the Au/Ti/STO/NSTO (a) and the Ag/STO/NSTO (b) setups.

The first measurements on the second sample are shown in Fig. 3.13. This figure displays a magnification of the V,I sweep, there was only a positive breakthrough so emphasis has been put on the positive region. Consecutive sweeps resulted in lower resistance, each curve became more steep, this behaviour was observed in experiments on all contact points. The same rectifying and diode-like behaviour is observed in measurements on the substrate (Section 3.1.3) with silver contact points. This rules out that the behaviour is caused by the STO/NSTO interface. The observed kind of behaviour can be explained by the forming of a Schottky barrier at the Ag/STO interface. When comparing the results from the substrate and the STO layer a few differences become clear from further measurements:

1. The positive breakthrough voltage is higher for Ag/STO/NSTO ($V \approx 1.5V$) than for Ag/NSTO ($V \approx 2V$).
2. The negative breakthrough voltage is lower for Ag/STO/NSTO ($V \approx -15\ V$) than for Ag/NSTO ($V \approx -5\ V$).
3. The resistance for Ag/STO/NSTO ($R \sim 10^7\ \Omega$) is significantly higher than for Ag/NSTO ($R \sim 1\ \Omega$).

The first two points can be explained by Eq. 1.4, since NSTO is a doped substrate, $N_{d,NSTO} > N_{d,STO}$. This decreases the depletion width and ensures easier transport. At large negative voltages, tunnelling will take place and since the depletion width for NSTO is smaller, so is the barrier width, enabling easier tunnelling. Since STO is an insulating layer, the resistance is expected to be larger than that of a conducting substrate.

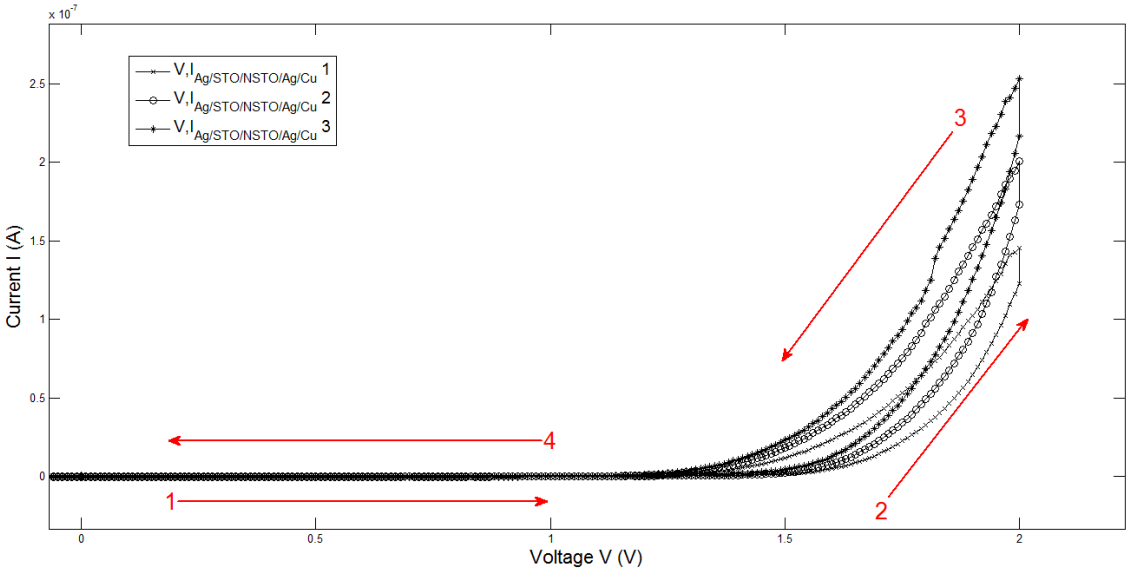


Figure 3.13: Magnification of three V,I sweeps for Ag/STO/NSTO/Ag/Cu, all with the same parameters: $-2 \leq V \leq 2$, step voltage V_s=0.01 V,compliance current I_c=1·10^{-6} A and source delay t_s=0.01 s.

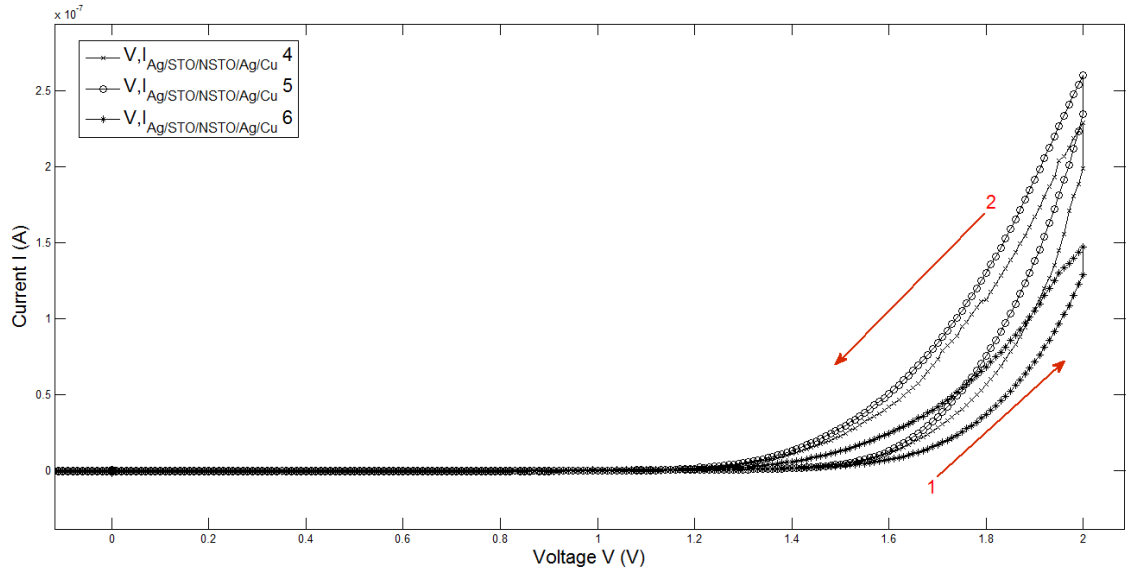


Figure 3.14: Magnification of three V,I sweeps for Ag/STO/NSTO/Ag/Cu, all with the same parameters: $-2 \leq V \leq 2$, step voltage V_s=0.01 V,compliance current I_c=1·10^{-6} A and source delay t_s=0.01 s. Measurement 4 was the first on the particular contact point, measurement 5 was after several sweeps and measurement 6 was performed a day later.

Obviously the resistance depended on previous measurements, several experiments were performed to investigate what influences this behaviour. One of these experiments was to perform several sweeps and find some stable configuration, i.e., with every sweep the material breaks down slightly, until it reaches a point where a consecutive measurement is very similar to the previous one. To check whether time was of influence, a 'stable'

position was obtained, the sample was stored in Nitrogen for a day. After a day the sample was measured again with the same parameters and compared to the final measurement of the day before, refer to Fig. 3.14 for the result. It is observed that the curve is steeper than the one from the day before, therefore time did not influence the measurements.

After investigating a time dependence, the response to a constant voltage was considered. First a stable configuration was acquired on a new contact point (V,$I_{Ag/STO/NSTO/Ag/Cu}7$ in Fig.3.15), after this measurement a constant voltage V=1.5 V was applied for 30 minutes. A sweep was performed after the constant electric field and V,$I_{Ag/STO/NSTO/Ag/Cu}8$ in Fig.3.15 was measured. Clearly the resistance had increased with the positive constant voltage, a possible explanation for this behaviour is that it is caused by heating, however the power dissipation is very low, i.e. P$\sim 10^{-6}$ J/s.
After 30 minutes without an electric field, another sweep was performed resulting in V,$I_{Ag/STO/NSTO/Ag/Cu}9$, the curve is, as expected steeper than the previous curve. It can be concluded that long time exposure to an electric field results in increasing resistance.

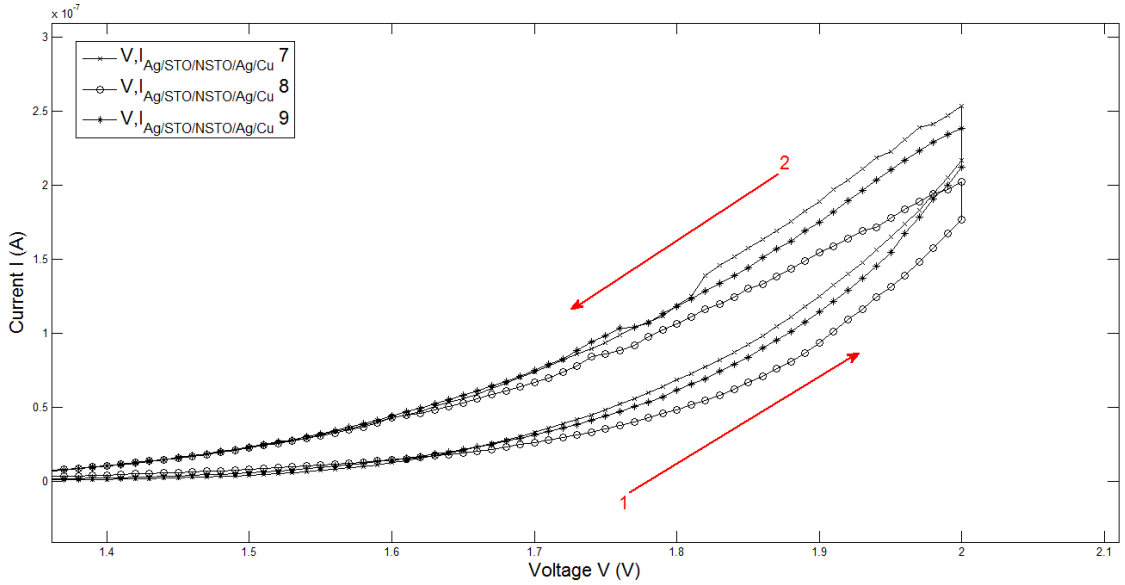
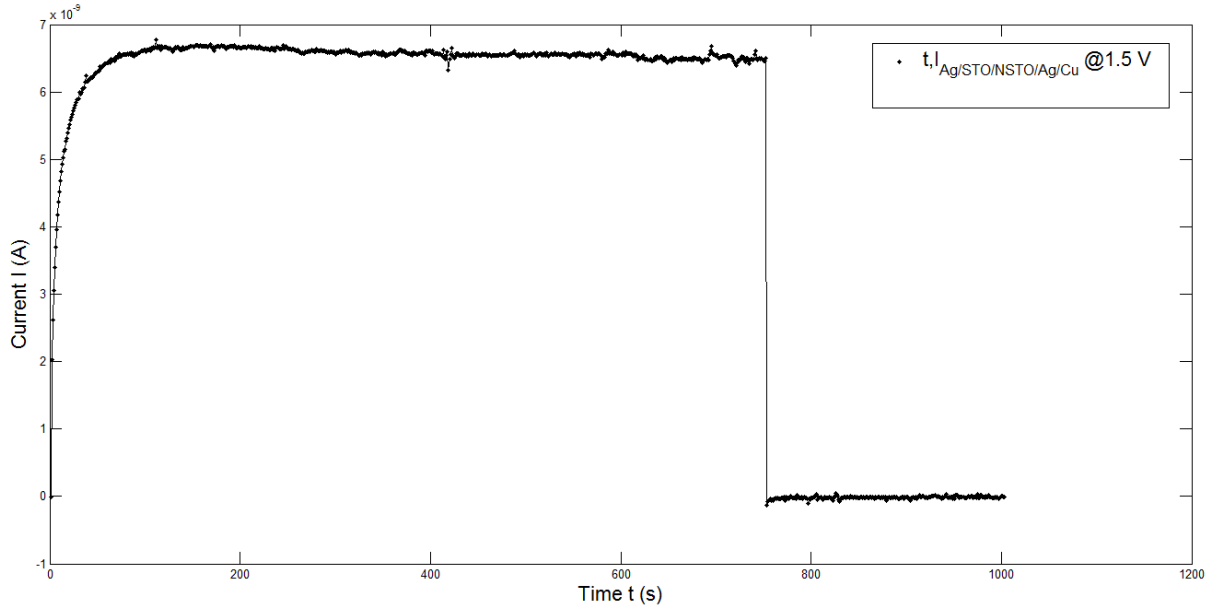
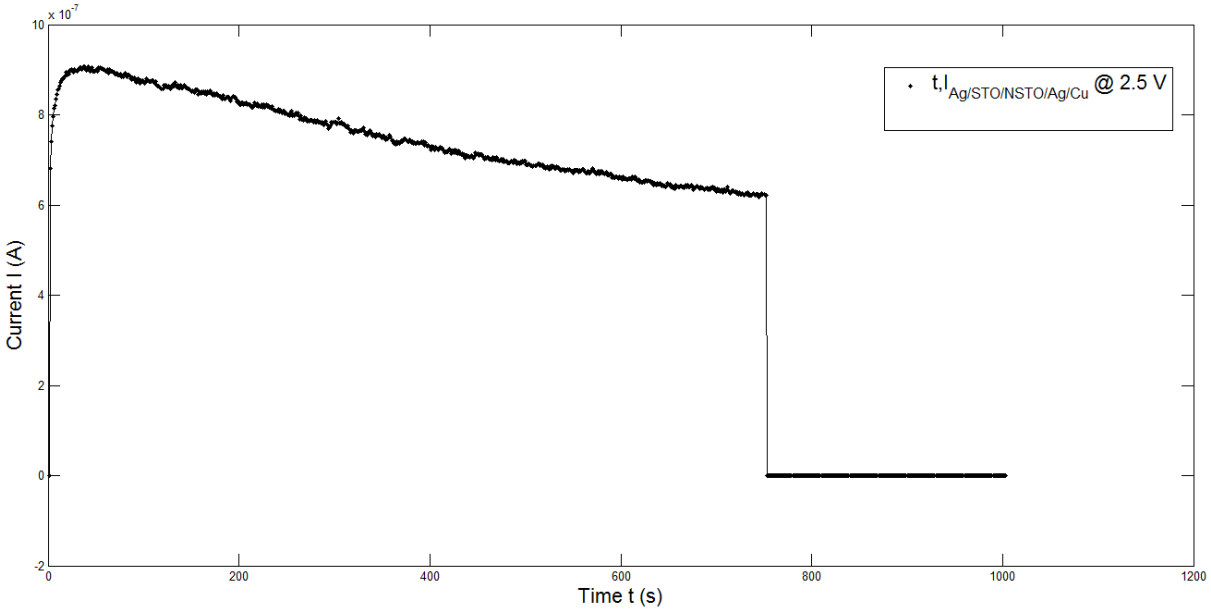


Figure 3.15: Magnification of three V,I sweeps for Ag/STO/NSTO/Ag/Cu, all with the same parameters: $-2 \leq V \leq 2$, step voltage V_s=0.01 V,compliance current I_c=1·10^{-6} A and source delay t_s=0.01 s. Measurement 7 was performed first. Measurement 8 was performed after 30 minutes at a constant voltage V=1.5 V, measurement 9 was after 30 minutes in rest after measurement 8.



(a)



(b)

Figure 3.16: t,I curves for Ag/STO/NSTO/Ag/Cu, measurements performed during 12.5 minutes under the influence of a constant voltage V=1.5 V (a) and V= 2.5 V (b).

The increasing resistance over time under the influence of an electric field has been further investigated by recording the current over time. These measurements were performed with a constant voltage V=1.5 V and V=2.5 V and are displayed in Fig. 3.16a and Fig. 3.16b respectively. Indeed the resistance increased over time and for the V=2.5 V case, the increase was more noticeable than for the V=1.5 V case. It is plausible that this effect is caused by heating since the power dissipation is considerably larger for higher currents ($P=I^2R$).

At this point the conclusion can be drawn that measuring STO is challenging. Contact was realized by Au/Ti contacts, Au contacts (the gold coated probes, by piercing through a layer) and silver paint. The first results with hysteretic behaviour occurred when measuring the silver paint contacts. Since the measurements on the substrate with Au/Ti contacts (Fig. 3.6) displayed Ohmic behaviour, the hypothesis was made that the titanium was responsible for Ohmic contact at the Au/Ti/NSTO interface. Contact with silver paint resulted in a Schottky barrier, this can be explained by the difference in work functions, refer to Table 3.1.

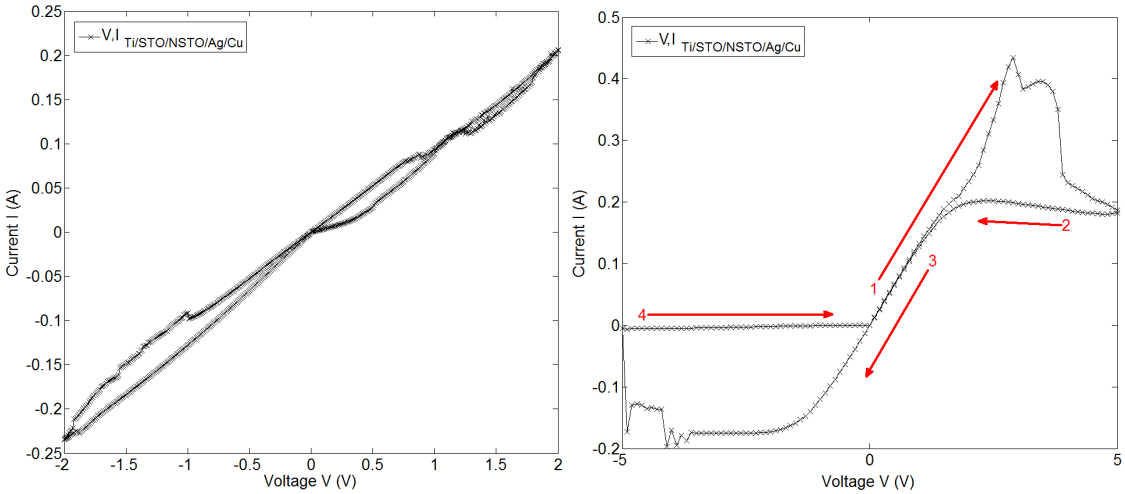
Gold	5.1 - 5.47 eV, depending on the lattice structure
Silver	4.26 - 4.47 eV, depending on the lattice structure
Titanium	4.33 eV
Indium	4.09 eV

Table 3.1: Work functions for different materials

The work function of gold is considerably higher than the work functions for silver or titanium. In one of the measurements on the Au/Ti/NSTO/Ag/Cu sample diode-like behaviour was observed (the exception discussed in Section 3.1.3). The probe went through the contact point resulting in contact between the gold probe and the NSTO substrate creating a Schottky barrier, further measurements with Au/(N)STO interfaces have to be performed to confirm this.

3.2.5 STO on NSTO, Titanium contact points

Again a layer of 50 nm STO is epitaxially grown on top of a 5x5x1.0 mm, (001) oriented, 0.5 wt% Nb:$SrTiO_3$ substrate. Using the same procedure as described in Section 3.1 eight Ti contact points were sputtered. Due to time restrictions only a few measurements were performed on this sample. The first two measurements on a new contact point are displayed in Fig. 3.17a and Fig. 3.17b respectively.



(a) *(b)*

Figure 3.17: V,I curve for Ti/STO/NSTO/Ag/Cu with step voltage V_s=0.01 V, source delay d_s=0.01 s, $-2 \leq V \leq 2$ (a) and $-5 \leq V \leq 5$(b).

Fig. 3.17b shows bipolar resistive switching, in this single measurement the system switches to a HRS (LRS) at V≈ 4 V (V≈ -4 V). Clearly the system was already in a LRS (R∼ 10 Ω) during the first measurement, also the threshold voltage was not reached, this was a READ operation. When the voltage increased in the second measurement a switch occurred at V≈ 4 V. This switch was to a 'medium' resistance state ('MRS') since it switched back to the LRS on the way back (arrow 2). In the LRS it continued until V≈ -4 V, the system switched to a HRS (R∼ 10^3 Ω). Unfortunately, due to lack of time, no further measurements were performed to check for reproducibility. An explanation for the switch to the 'MRS' could be a sudden drop in resistance due to heating. Also the system was not trained (performing several sweeps to stabilize the material) and therefore not stable.

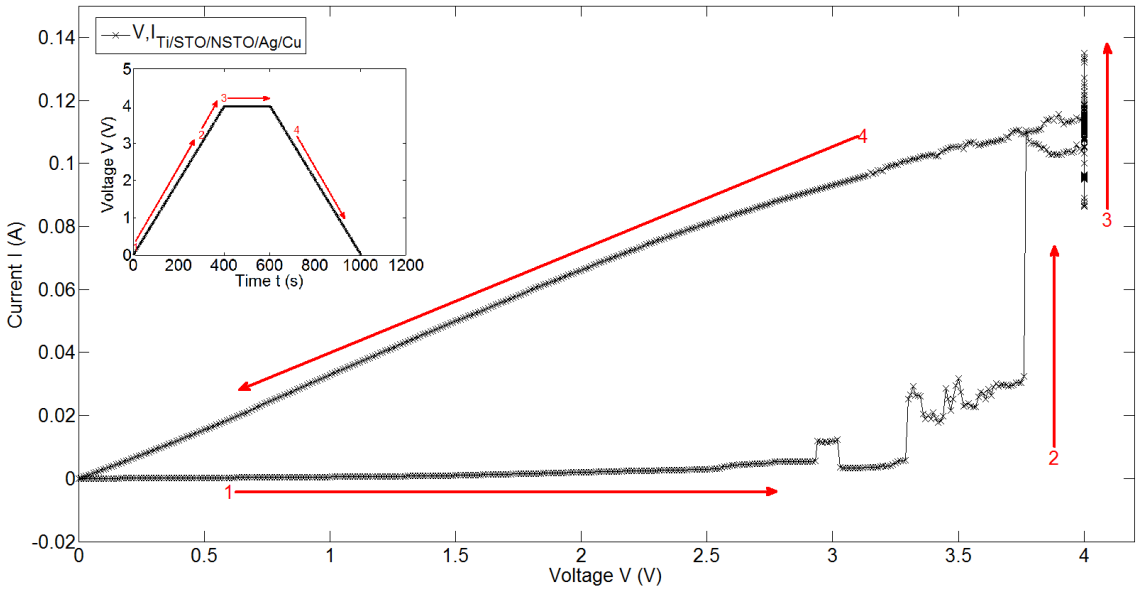


Figure 3.18: V,I curve for a constant voltage measurement with a sweep up and down. $-2 \leq V \leq 2$, step voltage V_s=0.01 V and source delay t_s=0.01 s.

Finally a constant voltage measurement was performed, note that the system was still in an OFF state. Fig. 3.18 displays the result, the inset shows the voltage over time with corresponding arrows. Again a switch to a LRS takes place at V$\approx$ 4 V. There is not enough evidence to state that this behaviour is reproducible.

Chapter 4

Discussion and Conclusion

A lot of the results have been discussed already in the previous chapter, this chapter will provide an overall discussion and conclusion.

4.1 Discussion

During the experiments, two ways of making contact points were used, i.e., RF sputtering and 'painting'. With sputtering, atoms were deposited at very high energies. This could mean that the Ti and Au atoms caused oxygen vacancies when hitting the STO layer and thereby changed the electrical properties. In what proportion these vacancies were created is unknown and worth some further research. It is good to note that the Ti sputtering performed on the sample discussed in Section 3.2.5 happened at a high sputterbias, i.e., Vtextsubscriptsputter=300 V. The sputtering on all the other samples was performed at $V_{sputter}$=150 V. The observed switching behaviour could therefore be a result of more oxygen vacancies compared to the other samples. To obtain more clarity on this it is recommended to perform Hall measurements on layers before and after sputtering to determine the carrier concentrations.

Measurements were performed without the need of sputtering using silver paint as contacts. Schottky barriers were formed when using this material, indicating a work function that was too high to obtain Ohmic contact. Indium can be a suitable material for a non-sputtered contact point, since it can be pressed on the layer manually. As it appears from Table 3.1, Indium has a very low work function, even lower than the work function for Titanium. According to the assumptions made in Section 3.2.4, In contacts should therefore behave Ohmic on top of STO. So if Ti behaves Ohmic because of its low work function, In should behave Ohmic as well.

In Section 3.2.5 real switching behaviour was observed, although the stability of the on and off state was not checked by repeated measurements. Repeated measurements are recommended, because this material shows the most fruitful behaviour for suitability in memristive applications. The observed ON/OFF ratio in a single experiment was about 10^2, this is considered large for a first measurement.
The physics that caused the bipolar switching behaviour inside the material are not clear. It is possible that during the deposition of the Ti contacts a lot of oxygen vacancies occurred at the Ti/STO interface resulting in a comparable memristor structure as in Fig. 1.6, the oxygen vacancies could also originate from oxidation of the Ti electrodes. Also it

could be one of the other models proposed for resistive switching mentioned in Section 1.1. In the model proposed and the measurements conducted, the layer thickness of STO was about 50 nm. Thickness could very well influence the electrical behaviour of the material, this may be worth studying.

4.2 Conclusion

The goal of this research was to find out if STO is a suitable material for use in memristive devices. After measuring the NSTO substrate and the STO layer it became clear that contact material plays a significant role in characterizing a complex oxide like STO. Also the method of measuring is important, probes are very likely to pierce through thin layers and contacts. It can also be concluded that silver paint should not be used as a contact material. If one wants to use sputtered contacts he should bear in mind that sputtering may influence the STO layer, more research needs to be conducted to confirm this presumption.
Finally, switching behaviour and hysteresis has been observed when using the relatively low work function material Titanium as a contact. These observations certainly do not exclude STO as a candidate material for memristive applications.

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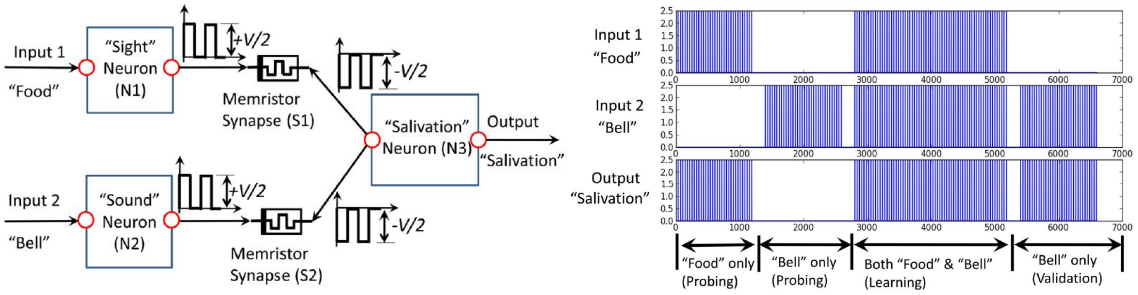
Appendix A

Simulating the Pavlov effect

A very simple, but great example of a neuromorphic circuit that can be made with memristors is the Pavlov effect. This theory is based on research done by Wang et al. [24]. The Pavlov effect can simply be described by the following example: when a dog is given a signal, for example with a bell, every time he gets food. After a while he will still produce saliva, even when no food is given to the dog. The Hebbian theory explains this behaviour: "Cells that fire together, wire together". The memristor system of the Pavlov effect can be seen in Fig. A.1a, and the simulation in Fig. A.1b.

When a neuron receives a receptor potential, it starts emitting both forward (along the output) and backward (along the input) a series of action spikes. The amplitude of these spikes is constant at a "half voltage" V/2, but the frequency depends on the strength of the stimulus. The synapses that connect the neurons determine if the signal is passed or not, by having a high or low resistance. At the start, Memristor Synapse 1 has a very low resistance, so the "Sight" signal of the food will be proceeded and result in the "Salivation" output. Memristor Synapse 2 has a very high resistance, so the "Sound" signal resulting from the bell will not cause the "Salivation" output. In the "Learning" process, both the "Sight" and "Sound" neurons will produce a signal. As stated before, the "Salivation" neuron will not only send a forward (along the output) signal, but also a backward signal (along the input) due to the activation of the "Sight" signal. When the backward negative signal -V/2 of the "Salivation" neuron overlaps with the positive V/2 signal of the "Sound" neuron, a "full" voltage drop of V is set over the Memristor Synapse 2. This will cause the memristor to switch and the resistance to drop. Now, the "Sound" neuron will trigger the "Salivation" neuron as well, because it is no longer blocked by Memristor Synapse 2. The dog has learned something.



(a) *(b)*

Figure A.1: The Pavlov system with the neural network made of memristors (a) and a simulation of this network (b) [24].

Appendix B

Van der Pauw Measurements

This appendix is based on the theory of Van der Pauw [25].

Electrical resistance can in principle easily be determined. Two contacts are connected to the material and a known voltage V is applied. By measuring the current I the resistance can be determined by Ohms law:

$$R = U/I \tag{B.1}$$

In a simple ohmmeter this principle is used. However, in these measurements, the measured resistance is the sum of the contact resistance and the resistance of the material, while only the resistance of the material is requested:

$$R_{total} = R_{contact} + R_{material} \tag{B.2}$$

To avoid this problem, Van der Pauw came up with a method using four contact points, preferably in the corners of the material. Two of the contacts are used to apply a controlled current through the material. The other two contacts are used to measure the voltage drop (see Fig. B.1. Because no current flows through these contacts, contact resistances do not play a role.

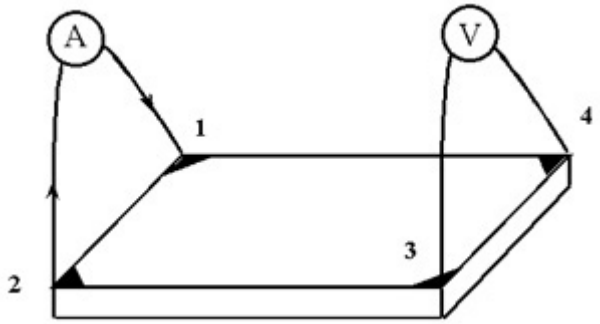


Figure B.1: Van der Pauw measurement with four contacts, two to apply a current, two to measure the voltage [26].

In a Van der Pauw measurement, eight measurements are performed, four in the horizontal and four in the vertical direction. $R_{horizontal}$ ($R_{vertical}$) is determined by taking the average of the horizontal (vertical) measurements. The accuracy of the Van der Pauw measurement is determined by comparing these resistances. When they are in a 5% range,

the measurement is accurate.

Combined with a Hall measurement, properties like resistivity, carrier type, sheet carrier density and carrier mobility can be measured. Finally, with the help of the formulas Van der Pauw derived, sheet resistance can be calculated from the measurements. For this report, these kind of measurements are not needed, so this will not be explained.

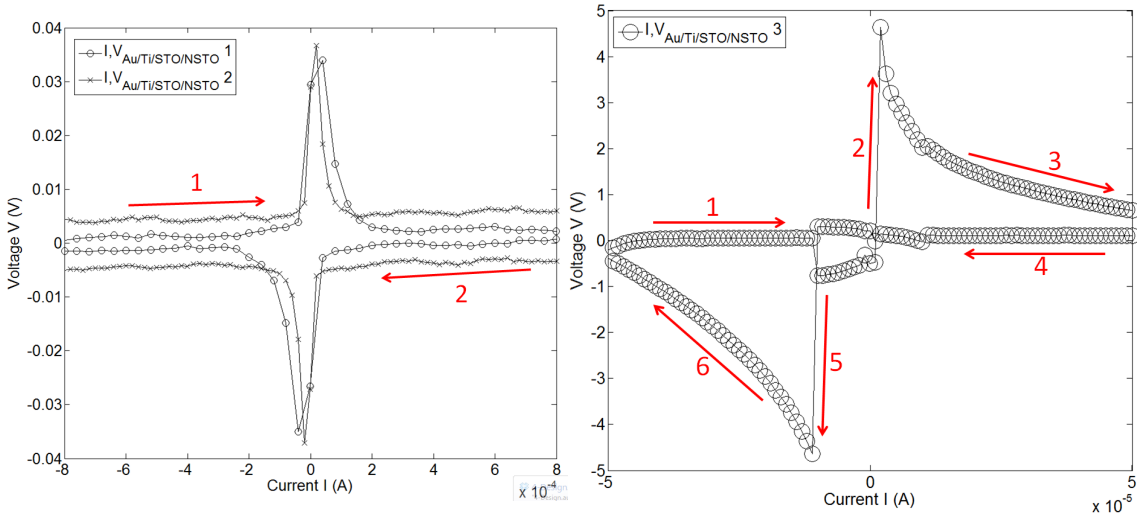
Appendix C

Other measurements

Not all measurements performed during this bachelor thesis are described in the report. This because the measurements went wrong or did not contribute enough to answer the research questions. Still some measurements give interesting results and are worth discussing. For completeness, these measurements are presented in this appendix.

C.1 Au/Ti/STO/NSTO

In the report, a four point measurement on the substrate is given in Fig. 3.8. In this measurement, the current was swept from I=-0.5 A to I=0.5 A and back to I=-0.5 A. This showed a straight line and a resistance of R=0.0017 Ω. There were also measurements performed in a smaller range of I, i.e., from I=-1·10^{-3} I to I=1·10^{-3} and from I=1·10^{-4} A to I=1·10^{-4} A, the results are displayed in Fig. C.1.



(a) *(b)*

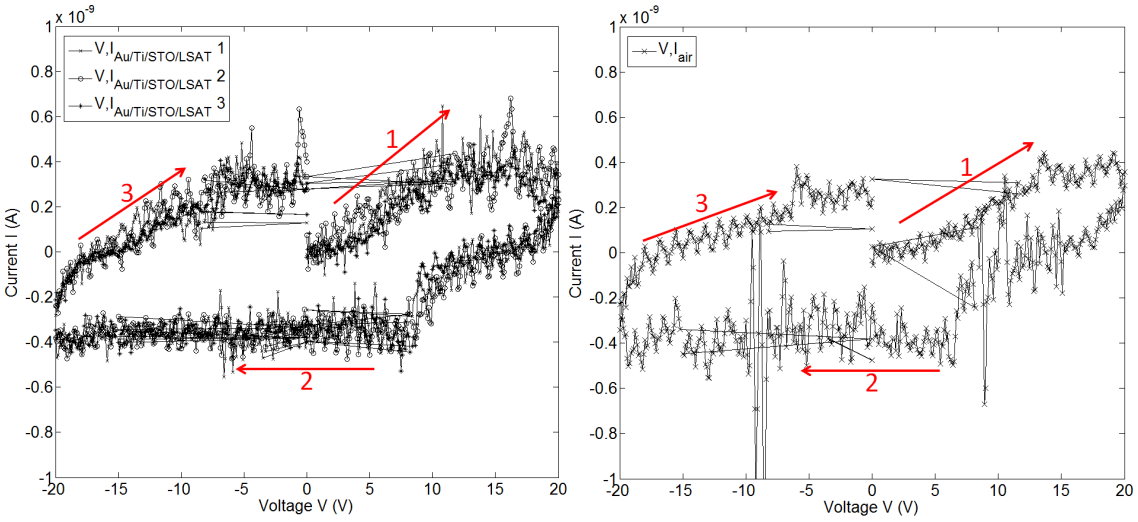
Figure C.1: Magnification of the I,V curves for NSTO with -1·10^{-3}<I<1·10^{-3}, source delay d_s=0.01 s and step I_1 I_{s1}=4·10^{-5} A and step I_2 I_{s2}=2·10^{-5} (a). (b) shows a magnification of the I,V curve for NSTO with -1·10^{-4}<I<1·10^{-4}, step I_3 I_{s3}=1·10^{-6} I for $I,V_{Au/Ti/STO/NSTO}3$ and source delay d_s=0.01 s.

The graphs in Fig. C.1 show a magnification of the obtained peaks. The resistance found for these peaks is in the order of R=200 Ω. A possible explanation for the peaks is

that in that small region of I, the resistance of the grown layer of STO is measured. The resistance found for the for the remaining region of I was in the order of R= 1 Ω. The explanation for this behaviour is that somehow, a great part of the current flows through the substrate. Another explanation is that because as stated in Section 3.2.1 only the high conducting substrate is measured. In these small regions of I, only the internal resistance of the Keithley plays a role, resulting in the obtained behaviour. Also the real current through the sample was not monitored, ultimately the method of measuring was changed to voltage sweeps and no further research was done to characterize this kind of behaviour.

C.2 Au/Ti/STO/LSAT

As can be seen in Fig. 3.11b in Section 3.2.3, no current was measured through the STO layer grown on top of the LSAT. But, when zoomed in on the straight line, some current shows up. This can be seen in Fig. C.2a.



(a) *(b)*

Figure C.2: Magnification of the V,I curve for STO grown on LSAT with -20< V<20, step V V_s=0.1 V and source delay d_s=0.01 s (a) and the same measurement performed in air (b).

Clearly some current was measured, although its value was very low. The measurement was verified by disconnecting the probes from the sample and performing another V,I sweep, 'measuring' the air. This measurement showed exactly the same behaviour as the measurement for the STO on LSAT as can be seen in Fig. C.2b. Together with the fact that the connection of the probes with the contact points was checked (as explained in Section 3.2.3), it can be concluded the STO layer was not conducting.