ELECTROSTATIC TUNING OF $LaAlO_3$-$SrTiO_3$ INTERFACE DEVICES

Master of Science Thesis

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ABSTRACT

We report transport measurements on structured $LaAlO_3$-$SrTiO_3$ interface devices with a $SrCuO_2$-$SrTiO_3$ capping layer and Au top gate electrode. The properties of the 2DEG at the interface were tuned by an applied top gate voltage. These properties included the carrier density, the average global carrier mobility, and the longitudinal resistance in a magnetic field.

The quality and reproducibility of the devices was strongly improved in this work. The structuring hard mask layer was insulating in all samples, the average global mobility was increased by an order of magnitude, and the gate leakage current was comparable to the lowest value in literature, at most.

An electrostatic model was devised to describe the effects of gating on the 2DEG. Qualitative features, such as an increase in the carrier density due to the presence of a top gate electrode, were predicted and confirmed by measurements. The capacitance equation of the top-gated 2DEG was found to have additional terms with respect to the equation in the parallel plate capacitor model. These terms were related to the density of states of proposed band diagrams in literature and the shape of the confinement potential at the interface. Strong indications of the validity of this capacitance model were found by experiment.

The measurements also laid bare some anomalous effects that could not directly be explained. The measured emergence of a resistance upturn, accompanied by a large positive magnetoresistance at low temperature, could not be explained by the Kondo model, or by the magnetoresistance related to spin-momentum locking alone. The magnetoresistance of the samples with an applied top gate was also anomalous and could not be described by weak antilocalization theory, size effects or classical magnetoresistance alone.

In a broader perspective, the development of top-gate tunable, structured high-mobility $LaAlO_3$-$SrTiO_3$ devices is a major step towards the creation of a quantum point contact in an oxide heterostructure. The fabrication of such a device could lead to the first observation of (quantum) ballistic transport in a strongly correlated electron system like $LaAlO_3$-$SrTiO_3$, enabling the study of new phenomena arising in such devices.

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1. INTRODUCTION

In the present time, technology to improve the quality of life, healthcare and environment is an ever-growing part of society. The ability to speak to one another by video on a device that is smaller than the average person's hand, whilst the people having the conversation are located the Earth's diameter apart, is something no one could have imagined thirty years ago. The enabling developments in electrical engineering, information technology and related industries would not have been, if it wasn't for discoveries in physics and the development of materials that make such devices work.

Therefore, the scientific community is constantly looking for ways to exploit new materials. This thesis is about increasing the understanding one of them, based on lanthanum aluminate and strontium titanate (LAO-STO). It focuses on methods to create reliable, electrically tuned devices in it, and on measurements of the electrostatic control over the material. The techniques that have been developed in the process are valuable for future work, as they are major steps in reaching a long-term goal of achieving controlled quantum and ballistic transport in this system.

LAO-STO shows great potential for applications, as most of the exotic physics that occur in oxides, the materials class based on oxygen ions in the crystal, also occur at the LAO-STO interface. Oxides, in general, are interesting materials for applications in future electronics, due to their very local electronic states and the large variety of physical phenomena that are observed in them. Due to certain properties, it can also become a building block for solid state quantum computers or be used as a chemical sensor. But before we explore the LAO-STO system, we will start with a brief introduction into the physics of materials.

1.1 MATERIALS PHYSICS

Material science in general considers the fundamental study of materials with interesting properties, and the translation of these properties to useful applications. For instance, chemical material scientists develop organic fibers that get stronger in each generation, in order to make high-quality, very strong ropes for nautical purposes, or for use in carbon bodies for sports cars.

In materials physics, mainly solid state materials are studied. The properties of interest are based on either the atoms or ions that make up the solid state crystal lattice, or the electrons that are present in the system. These ions and electrons together determine all properties of the material, but physicists are mainly concerned with the electric, magnetic, thermal and optical properties of the material. In this thesis, we studied the electric and magnetic behavior of electronic states at the *interface* between two materials.

Interfaces are interesting systems to study. An interface is the border between two regions, and very special physics may apply. For example: at the interface between two countries, road rules may be different. At a border between countries that drive on either the left or the right side of the road, the lanes have to cross safely in order to prevent major traffic jams or accidents.

More subtle phenomena may also arise. For instance, when driving on the road crossing the border between Germany to the Netherlands, the legal speed limit in both countries is different. To avoid dangerous situations after crossing the border, the speed on the German side of the border has to be adjusted to the Dutch laws. Therefore, the rules in the Netherlands partly determine the rules in Germany, close to their interface, the border.

In material, the laws are not set by a government, but they are the laws of physics. Electronic classification is done by the band structure of the material. A band structure is the electronic map of the material in terms of energy and momentum. In this map, for a certain energy, there can either be states or no states present in a material. Like on a road map, there can be either a road or no road at a given position. If there is a state, it can be filled with an electron. By the Pauli exclusion principle, no two electrons of equal energy, momentum and spin can be in the same state. So, any new electrons will have to be in an unoccupied state. Since every electron tends to minimize its energy, every added electron will require a higher energy to occupy an unfilled state in the system. This is like filling a bucket with marbles: ideally, every added marble will be higher off the ground than all the others. This will give every next marble a higher height energy, as we learned in middle school. The filling of electrons continues until all electrons that should be in the material, are in it. The energy of adding one more electron is called the Fermi energy. The position of this energy in the band structure determines whether a material can conduct electricity. In figure 1.1, three simplified band structures are shown for a metal, semiconductor and insulator. The dashed line is the Fermi energy, the purple area is the valence band and the blue area is the conduction band.

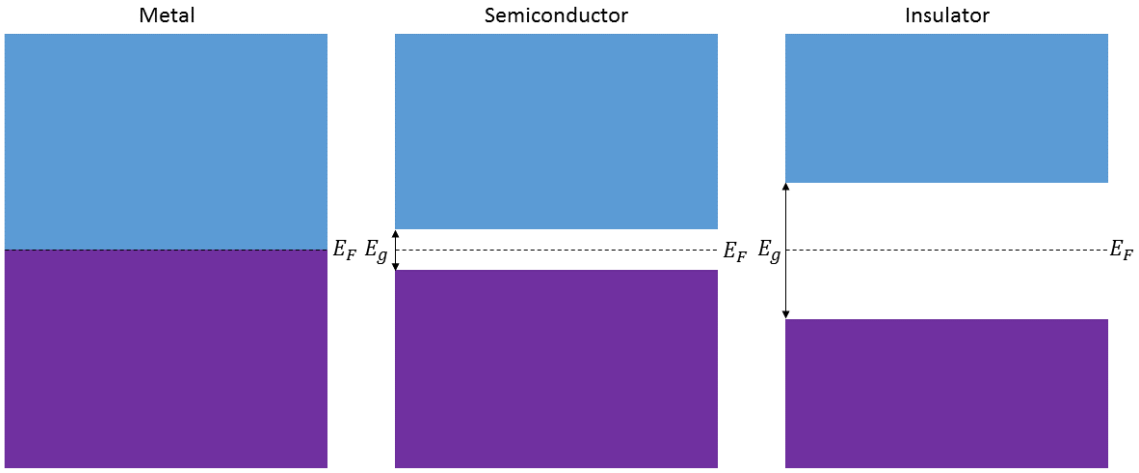

Figure 1.1 Simplified band structure of a metal, semiconductor and insulator.

The white areas denote the energy levels at which there are no states, which is given by an energy gap that is unique to the material. From the actual, not simplified, band structures, many more properties of the material can be derived. For instance, it can describe a material's ability to conduct heat, or determine the color of LED lights, which is coupled to the energy gap.

This thesis is about the question what happens if one puts two materials with different band structures together and how we can use the emergent phenomena in the light of applications.

1.2 OXIDE MATERIALS

The discovery [1] of a conducting interface between the band insulators $SrTiO_3$ and $LaAlO_3$ has triggered extensive research on its origin and properties over the years [2-5]. It is a quasi-two-dimensional (q-2D) member of the family of complex oxides, a class of materials has shown remarkable physics over the years. For instance, high-temperature superconductivity was discovered in 1986 [6] in a complex oxide, but also effects like ferroelectricity [7], Mott insulation [8] and spin ice ordering [9] have been reported or predicted in complex oxide systems.

1.2.1 INTERFACES IN COMPLEX OXIDES

Many of the interesting phenomena that occur in various oxides are observed at the LAO-STO interface, which makes its physics very rich. This versatility makes it a very promising candidate for applications [10]. Superconductivity has been reported [11] as well as magnetic effects [12] and even their coexistence [13]. The properties of the interface are tunable by many parameters [14], most profoundly the LAO thickness [15,16] and the growth conditions [2,3,12,17]. The physics are very local, as is demonstrated by writing very small conducting lines onto the interface with a conductive Atomic Force Microscope (AFM) [18,19].

Electrostatic tuning of the 2DEG has first been shown by back-gating through the STO substrate [15,20,21], after which tuning with top gates on the LAO surface was shown [22-25]. Electrostatic tuning is well known from the semiconductor industry and as such, makes a reliable method to change the properties of a 2DEG. Moreover, it is reversible – up to certain values – and fundamental aspects can be measured with high certainty.

Electrostatic tuning can control many properties of the LAO-STO system. Superconductivity in LAO-STO is gate-tunable [20,25], as is the reported Rashba spin-orbit coupling [26,96]. Channels can be completely depleted [24,27], which should allow for the structuring of nanoscale devices as in GaAs-AlGaAs 2DEGs [28]. The tunable spin-orbit coupling opens possibilities for application in spintronics [29], which is an emerging field with great promise in next-generation, ultrafast electronics.

1.3 THIS THESIS

At the start of this work, in February 2014, top-gated structures had been grown by a few groups [22-25,30]. There were some problems in the fabrication of the samples, such as insulating layers that turned conducting [31], contact pinch-off (tested during this work), relatively high gate leakage [25], and lower mobility of structured devices as compared to unstructured ones [30].

A recent development is the use of a capping layer, as introduced by Huijben *et al.* [32], which should pave the way towards high-mobility structured devices. The reported electron mobility is of such order that mean free path lengths can become larger than typical structural features. If this happens, ballistic transport [28] may be observed for the first time in an oxide heterostructures. What happens to the electrons in such a strongly correlated system when ballistic transport sets in, is an open question at the moment. The high mobility is also beneficial for possible applications in electronics, as it increases the switching speed between 'on' and 'off' states of a transistor.

In order to achieve these milestones, it is of crucial importance to develop reliable devices with reproducible results. This thesis is about top-gating a structured, capped LAO-STO device and measuring it by transport experiments. We strive to understand the underlying physics, both from a fundamental point of view and for an outlook to applications.

The thesis outline is as follows. In the next chapter, the LAO-STO system is introduced, including its governing physics in more depth and the methods to tune it. In chapter 3, the confinement of the electrons near the interface is discussed and the effect of gating is introduced in terms of the variation of a chemical potential. The fourth chapter is about key techniques of fabrication, with a focus on improvements to the fabrication that were developed during this work. In chapter 5, the results of transport measurements on the 2DEG, and their interpretation in terms of material properties and transport effects. The thesis will then be wrapped up by a conclusion.

2. THE $LaAlO_3$-$SrTiO_3$ INTERFACE

The discovery of a conducting interface between lanthanum aluminate ($LaAlO_3$, LAO) and strontium titanate ($SrTiO_3$, STO) [1] has triggered extensive research on the origin of the conduction mechanism and ways to use it in applications. In this chapter, we discuss the state-of-the-art knowledge on the constituent materials $LaAlO_3$ and $SrTiO_3$, several explanations for the origin of the conductivity, methods to tune the interface properties and proposed (sub)band structures to explain the observed phenomena in these interfaces.

2.1 STRONTIUM TITANATE AND LANTHANUM ALUMINATE

Strontium titanate and lanthanum aluminate are both transition metal oxides with a perovskite lattice structure. A perovskite has a structure formula that can be written as ABO_3, where A and B are cations and the oxygen is the anion. The structure (figure 2.1) consists of alternating layers of AO and BO_2. A is the heavier cation, so in the case of $SrTiO_3$, A = Sr and B = Ti and for $LaAlO_3$, A=La and B=Al.

The valence of these ions creates electrically neutral layers of $(Sr^{2+}O^{2-})^0$ and $(Ti^{4+}(O_2)^{4-})^0$ in STO. $LaAlO_3$ has alternating LaO and AlO_2 layers where both La and Al have 3+ valence. This implies alternately charged layers of $(La^{3+}O^{2-})^+$ and $(Al^{3+}(O_2)^{4-})^-$, which results in an intrinsic polarization between these sheets. To distinguish between both cases, STO is a non-polar oxide and LAO is referred to as polar.

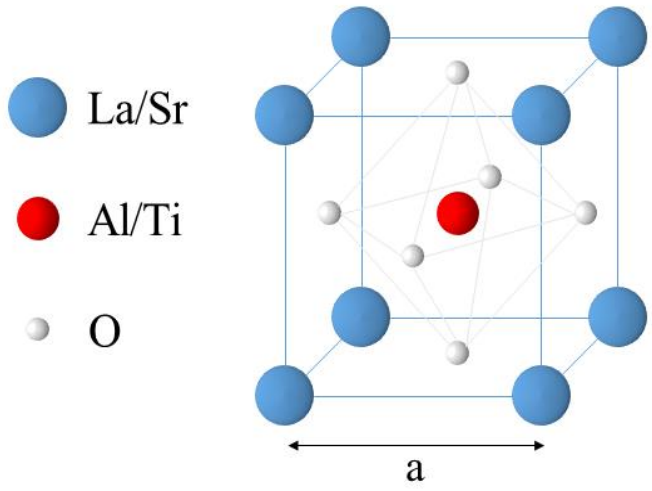

Figure 2.1 perovskite lattice structure of $SrTiO_3$ and $LaAlO_3$.

Of the two materials, $LaAlO_3$ is the material that has the most straightforward properties. It is a wide-gap insulator (5.6 eV [33]) and has a high dielectric constant, which is 24 in the bulk [43] and 16 as an amorphous thin film on Si [35]. The latter makes it applicable as a gate dielectric in silicon electronics [34]. Because of its lattice parameter, $LaAlO_3$ can also be used as a substrate for oxide superconductors [35,36].

$SrTiO_3$ displays some interesting phenomena and the physics that govern these are less understood than the physics that govern the observed phenomena in $LaAlO_3$.It is also wide-gap insulator with a gap of 3.3 eV [33]. Superconductivity in the class of oxide materials was first discovered in $SrTiO_3$ [37]. It also has a very high dielectric constant at low temperatures [38] that is dependent on the local electric field strength [39]. Like $LaAlO_3$, its lattice constant matches that of many interesting materials [40] and the termination of the crystal at the surface (TiO_2 or SrO plane) can be controlled [1,41]. This makes it a very suitable substrate for epitaxial growth.

Some basic properties of both $LaAlO_3$ and $SrTiO_3$ are listed in table 2.1.

Property	$LaAlO_3$	$SrTiO_3$
Lattice parameter	3.789 Å [42]	3.9051 Å [41]
Dielectric constant	24 (bulk)[43] 18 (thin film) [34]	300 (bulk, 300 K) [38] 24000 (bulk, 4.2 K) [38] < 24000 (4.2K, in E-field) [39]
Band gap	5.6 eV [33]	3.3 eV [33]
Color	Transparent	Transparent to dark blue, depending on oxygen vacancies
Magnetism	Diamagnetic [44]	Diamagnetic [45]

Table 2.1 materials properties of $LaAlO_3$ and $SrTiO_3$

At the interface, the lattice mismatch of ~3% is expected to produce strain, which is a change in the lattice parameters of the crystal. This may influence the dielectric properties [46] of the $SrTiO_3$ and the band structure at the interface [47].

2.2 ORIGIN OF CONDUCTIVITY AT THE LAO-STO INTERFACE

The origin of the conductivity at the interface is a subject of strong debate; a single answer would greatly improve the understanding of the material system and its potential for applications. However, we do know some boundary conditions for a conducting interface:

- The surface of the STO has to be TiO_2-terminated in the (100) direction [1]
- The growth of the LAO has to be epitaxial [1];
- The LAO has to be at least four unit cells (uc) thick [15];

The 2DEG conductivity seems to be a delicate interplay between different effects, of which the major propositions on its origin are discussed below.

2.2.1 ELECTRONIC RECONSTRUCTION

The discovery of the interface [1] was paired with an explanation based on the polar discontinuity. This is caused by depositing a polar material on a non-polar one. In figure 2.2a), a schematic of the LAO-STO interface is depicted, showing the polar and non-polar materials that are grown epitaxially to a sharp interface. In figure 2.2b), a distribution of the charges in the z-direction is given for the situation in figure 2.2a). One can attribute an electric field to these charges by integrating them along the z-axis, which results in figure 2.2c). Then, if one considers this electric field as the gradient of a potential, the electric field can be integrated along the z-axis to find the electric potential along this axis as is depicted in figure 2.2d). In this image, the electrostatic potential diverges as the layer grows thicker: this way, an infinite energy could be built up. Since every physical system tends to minimize its energy, this potential build-up, known as the polar catastrophe scenario, has to be avoided.

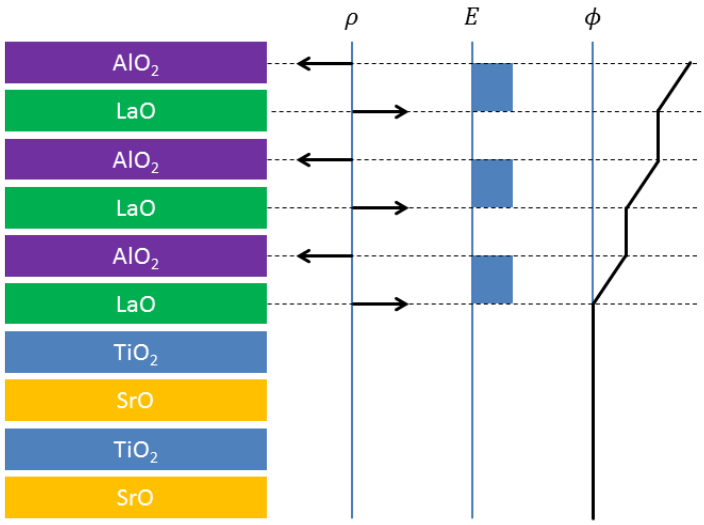

Figure 2.2 Origin of the polar catastrophe; a) Representation of the LAO-STO interface, b) charge distribution per layer along the z-direction, c) corresponding electric field along the z-direction, d) corresponding electric potential along the z-direction.

The explanation that was given [1,2] for the avoidance of the polar catastrophe is subtle. For every two unit cells, an electron is transferred from the top LAO surface towards the interface. This changes the valence of the first TiO_2 layer from 0 to $-1/2$, by changing the valence of half the Ti^{4+} ions to Ti^{+3}. This is called the electronic reconstruction scenario, which depicted in figure 2.3. The mixed-valence state of the Ti-ions in the STO has been shown by Nakagawa *et al.* [2].

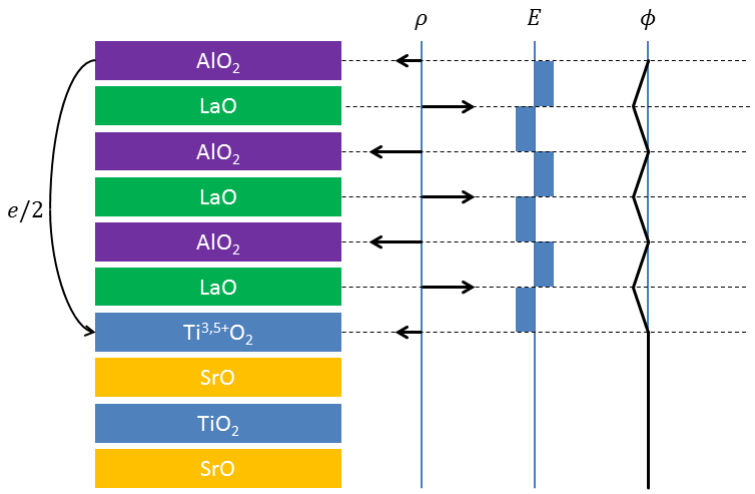

Figure 2.3 Solution to the polar catastrophe: electronic reconstruction. a) Representation of the electron transfer to the LAO-STO interface, b) new charge distribution per layer along the z-direction, c) corresponding electric field along the z-direction, d) corresponding electric potential along the z-direction.

This scenario implies that there is a transfer to the interface of one electron per two unit cells. The resulting sheet carrier density, calculated from the lattice parameters of LAO, is of the order of $3 \cdot 10^{14}$ cm^{-2}. This is three orders of magnitude higher than that of typical GaAs-AlGaAs samples [28].

In the electronic reconstruction scenario, the bands of LAO and STO align in a special way. The STO bands bend down near the interface and the LAO bands go up in energy away from the interface [2,4]. The energy of the LAO continues to increase until the LAO valence band at the surface reaches the level of the conduction band of the STO at the interface, as depicted in figure 2.4. The electrons at the LAO surface now have enough energy to dope the interface and prevent the polar catastrophe. There is no need to increase the LAO valence band energy any more for higher thickness, since the polar catastrophe has already been avoided. By Density Functional Theory calculations, this energy is reached for 4 unit cells of LAO [4]. As compared to the measured critical thickness [15] that is also 4 unit cells, the model is very appealing.

However, from the LAO lattice parameter, one can calculate the carrier density at the interface that results from the doping of one electron per 2 unit cells to be $\sim 3 \cdot 10^{14}$ cm^{-2}. The intrinsic carrier density is found to be much lower [1,17,20,24]. Also, the binding energy offset between 2 and 6 layers of LAO is only ~ 300 meV [48]. This is an order of magnitude lower than one would expect from the band alignment in figure 2.4, which suggests an energy shift of $E_{g,STO} = 3.3$ eV. These measurements suggest that the pure electronic reconstruction scenario is not the full explanation to the emergence of conduction at the LAO-STO interface.

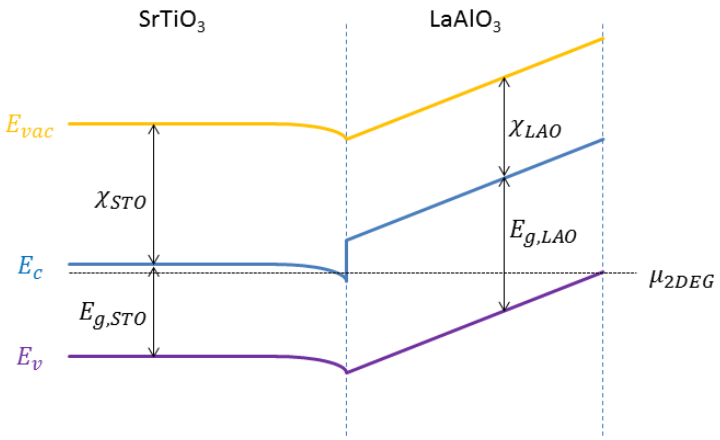

Figure 2.4 schematic band alignment across the LAO-STO interface following the electronic reconstruction scenario. The chemical potential μ of the 2DEG is in the conduction band of the STO just at the interface. χ is the electron affinity of the insulators and E_g is the energy gap.

2.2.2 INTERMIXING

The polar catastrophe also is to be avoided in junctions between type-III-V and type-IV semiconductors, where a charge imbalance occurs at the interface [1]. Here, an intermixing takes place between the two connecting elements to create the half charge needed to prevent the potential to diverge. This mechanism is depicted for the LAO-STO interface in figure 2.5.

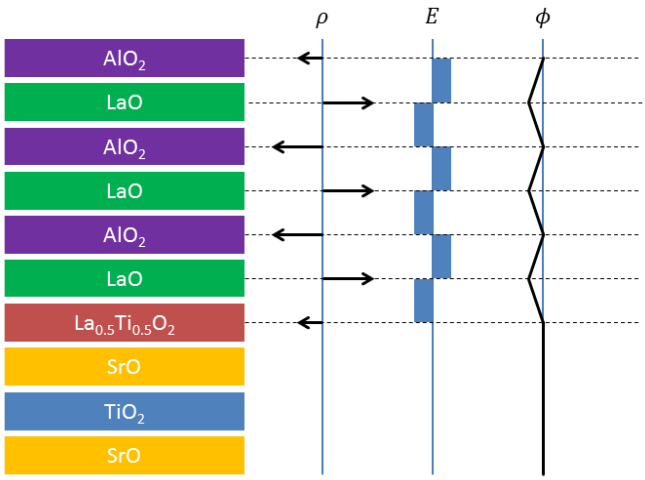

Figure 2.5 the solution to the polar catastrophe via intermixing at the LAO-STO interface.

Such an intermixing scenario can induce conduction at the interface, as STO can be doped by La [e.g. 49] to become conducting, because of the La-valence of 3+ and the Ti valence of 4+. It has been investigated [50,51] that this can be the case for the LAO-STO interface, but other studies [52,53] found out that intermixing is not necessary for interface conduction. Therefore, intermixing is considered a possible origin of conduction, but only as one that adds to a more fundamental mechanism.

2.2.3 OXYGEN VACANCIES

Strontium titanate can be doped by removing oxygen from the lattice [54] and this was shown to occur at the LAO-STO interface by Siemons *et al.* [3]. The oxygen deficient compound, $SrTiO_{3-x}$, is conducting because the removal of oxygen anions (O^{2-}) from the lattice leaves a positively charged, bound vacancy in the lattice. For charge neutrality, this needs to be compensated. This is done by doping two electrons into the system, which have an energy E_{imp}, the energy of the impurity doping band, as depicted in figure 2.6.

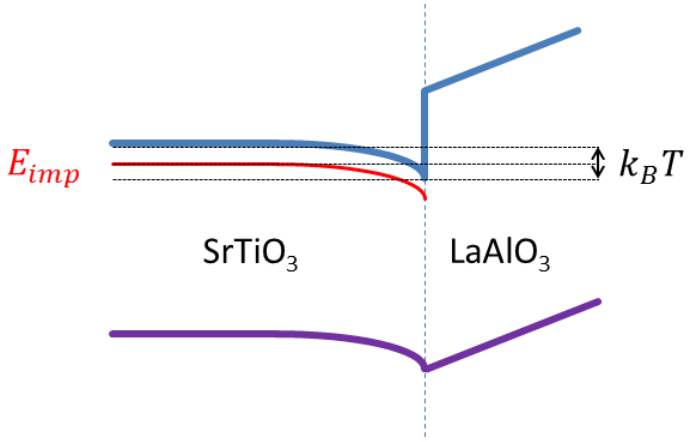

Figure 2.6 Impurity doping and thermal distribution of Fermi level k_BT.

If this energy is close to the Fermi level, these carriers contribute to the conduction by thermal smearing of the Fermi level, over a scale $\sim k_BT$. This leads to a temperature-dependent carrier density n_s, as is observed by Ref. [54] in oxygen-deficient $SrTiO_{3-x}$. The temperature-dependent increase as compared to the zero-temperature value is known as thermal activation.

The interface can be deliberately doped by oxygen vacancies by reducing the deposition pressure [3]. Huijben *et al.* [32] claim to have removed the oxygen vacancies as they measure a temperature-independent carrier density. This carrier density has to have another origin than oxygen vacancies. Thus, like intermixing, oxygen vacancies may provide additional carriers to the interface, on top of a more fundamental conduction mechanism.

2.2.4 CHARGE TRAPPING AT THE LAO SURFACE

A slightly modified, refined version of the electronic reconstruction scenario is the idea of charge trapping at the interface by surface charges [5]. The mechanism is based on the idea that defect states at the LAO surface emerge as a result of the polar discontinuity, at random positions. These defect states dope the 2DEG at random places and the mechanism can be described by a trapping potential, as depicted on the left side of figure 2.7. A low LAO thickness creates a deep trapping potential well with small spatial variance, which is the deepest well in the picture. As the LAO layer becomes thicker, the trapping potential becomes shallower and the spatial variance larger. At a certain thickness, this causes the doped areas at the interface to overlap – right part of figure 2.7 – and a metal-insulator transition takes place.

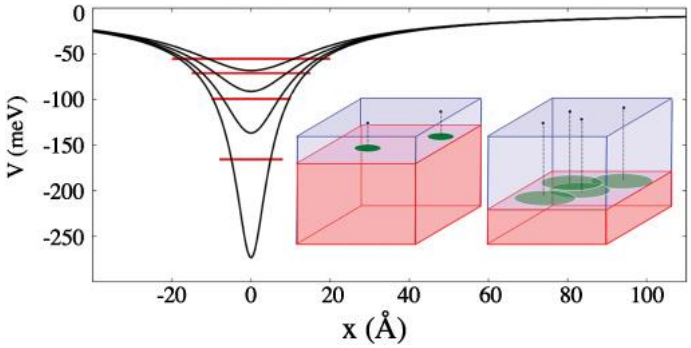

Figure 2.7 Charge trapping potential by defects at the LAO surface. The curves go from lowest LAO thickness d_{LAO} (deepest well) to highest. The inset shows the origin for the Anderson metal-insulator transition: as the doped areas by the surface defects overlap, global conduction will take place. Image taken from [5].

This scenario is appealing since it explains the recently measured large disorder at the interface [55]. However, the defects are positioned randomly on the surface and in this picture, the critical thickness can vary locally. On a scale much larger than the average dopant distance L_{ee} (~3 nm), this variation will average out. These considerations have not yet been disproven by measurements and further measurements of local charge carrier fluctuations can provide more insights on the validity of this scenario.

2.2.5 SUMMARY

There exists no generally accepted consensus on the origin of the conduction at the LAO-STO interface. Several intrinsic (e.g. electronic reconstruction) and extrinsic (e.g. oxygen vacancies) mechanisms of doping have been identified. Some of these are discussed above. It is possible that a combination of these mechanisms is needed to model the conduction in a given sample.

2.3 TUNING THE PROPERTIES OF THE 2DEG BY GROWTH

The many mechanisms that can influence the origin of the conductivity can also be used to tune the properties of the 2DEG. In this section, we discuss various methods to tune the properties of the 2DEG in the fabrication process.

2.3.1 STO SUBSTRATE

The STO substrate is the base for every LAO-STO 2DEG device. In the electronic reconstruction scenario, the substrate needs to be TiO_2-terminated in order to achieve conductivity at all [1]. One would expect a SrO-terminated substrate to yield a p-type interface, but it appears that the polar catastrophe is solved by an ionic reconstruction rather than an electronic one in this case [2].

The cleanliness of the STO surface is an important parameter for the performance of a device made on it in terms of electron mobility and spatial homogeneity. Adatoms or clusters of adatoms on the surface act as additional scattering centers, which affect transport through the 2DEG. This is bad for studying the physics of the interface as the transport properties of the interface change. It is also bad for developing electronic devices based on LAO-STO, as there is more scattering introduced, which reduces the mobility of the system. The same holds for impurities at the surface, defects in either STO or grown LAO, and irregular step edges, which can all act as additional scattering centers. Adding scattering centers to the interface is to be avoided as much as possible when transport in the LAO-STO system is studied.

At this point, a commercial STO substrate is of a higher crystal quality than thin films of STO grown on another substrate [41]. The latter would introduce a new control parameter to the system: strain. Strain affects the band structures of a material as the lattice parameters of the crystal are altered. This change in the band structure can in turn affect dielectric [7], thermoelectric, and conductive properties of the material [56]. Despite the low quality of STO thin films as a substrate, a study on the effects of strain on the LAO-STO interface has been done by Bark et al [57]. This study shows that the 2DEG quality is very dependent on the strain in the system. STO thin films were grown on different substrates, on which they grew the LAO film. The results are shown in figure 2.8. Besides the effects described there, strain is known to affect the properties of oxide-based ferroelectric thin films dramatically. They found that strain strongly affects the dielectric constant of a material and as such, can be used to engineer the dielectric properties of STO.

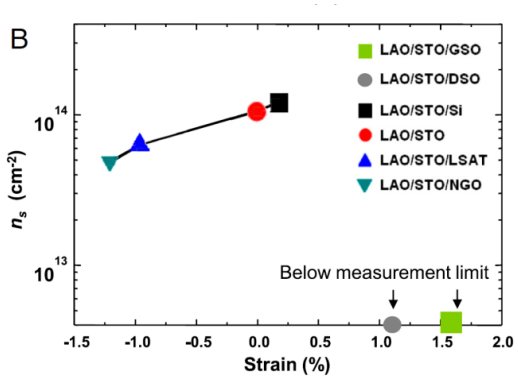

Figure 2.8 Strain dependence of the charge carrier density of as-grown films of LAO on STO on different substrates. The growth of LAO on an STO substrate is the 0% reference value. Image taken from [57].

2.3.2 LAO GROWTH PARAMETERS

Next, we discuss some effects of different growth parameters on the properties of the interface, as described in literature. This subsection considers growth by Pulsed Laser Deposition (PLD), which is a technique that has many growth parameters. In the references from literature given below, some of these parameters are consequently given, but some parameters are almost always left out. For instance the substrate-target distance, growth frequency and the laser spot size are rarely given in literature.

Temperature. Caviglia *et al.* [17] demonstrated a strong dependence of the carrier density and the mobility on the growth temperature. A lower growth temperature yielded a lower carrier density and a higher mobility. This was attributed to the increased crystallinity of the LAO film at lower growth temperatures, which was monitored by X-ray diffraction and RHEED oscillations [17(SI)].

Stoichiometry. Sato *et al.* [58] studied the role of various PLD parameters on the La/Al ratio in the LAO films. They found the laser fluence (energy density) and spot size to have a large role on this ratio. The carrier density was plotted against the stoichiometric ratio and a variation of two orders of magnitude was reported as a result of changing the ratio. In the same study, a model was used to explain this observation: an off-stoichiometric La/Al ratio enhances ionic reconstruction at the interface, instead of electronic reconstruction. This leads to the suppression of carrier density at the interface. Later, in a Molecular Beam Epitaxy (MBE) growth study, it was found that only Al-rich $LaAlO_3$ results in a conducting interface [52].

Oxygen background pressure. Siemons *et al.* [3] found that a *l*ow oxygen background pressure during growth induces oxygen vacancies in the STO that heavily dope the 2DEG. Several studies [15,54] claim that the formation of oxygen vacancies can be reduced if the deposition is followed by a post-anneal at high oxygen pressure ($\sim 10^2$ mbar). At higher oxygen background pressures during growth, magnetic effects may emerge at the interface [12].

Film thickness. The thickness of the LAO layer determines whether the interface is conducting at all [15]. Above this critical thickness, the thickness is of importance to the mobility and magnetoresistance [16]. Structural properties (e.g. strain, density of defects) of the LAO film [59] are dependent on the thickness, which might have a large influence on the thickness-dependent tunneling characteristics [60]. Magnetic effects [12] in samples grown at higher oxygen pressures appeared at a higher thickness (26 uc), whereas lower thickness samples (15 uc) did not show this behavior [1].

2.3.3 CAPPING LAYERS

In this work, we use a capping layer of $SrCuO_2$ (SCO) and STO to reduce the amount of oxygen vacancies at the interface [32]. It was argued that the SCO layer enhances oxygen diffusion into the system by decreasing the energy barrier for the oxygen at the surface. This diffusion reduces the amount of oxygen vacancies. This mechanism is schematically depicted in figure 2.9.

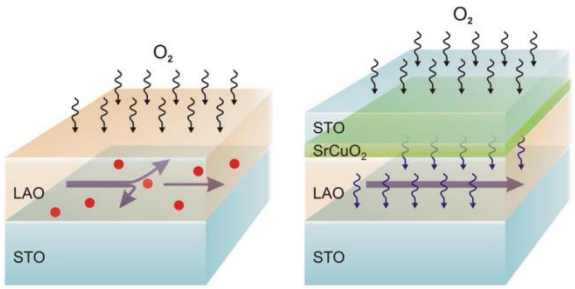

Figure 2.9 Suppression of oxygen vacancies by enhanced surface diffusion; a) low oxygen diffusion on a normal LAO-STO interface, with the red dots representing the oxygen vacancies; b) SCO-STO-capped LAO-STO interface, where the oxygen vacancies are suppressed by the enhanced O_2 diffusion. Image taken from Ref. [32].

A signature of the absence of oxygen vacancies is the absence of thermally activated carriers, as is shown in figure 2.10a). The carrier density has a constant, low value of $\sim 6 \cdot 10^{12}$ cm^{-2} for all temperatures. This makes devices based on this material stack very interesting to study, as the oxygen vacancy doping is reduced to a minimum and other possible origins of the conduction can be studied in more detail. In the paper, they found that intermixing is also absent by studying the interface by Scanning Transmission Electron Microscopy (STEM), a technique that allows to image the individual atoms in a cross-section. The carrier mobility was reproducibly found up to 6,000 cm^{2}V^{-1}s^{-1} and was attributed to the reduction of the amount of oxygen vacancies, which act as scattering centers.

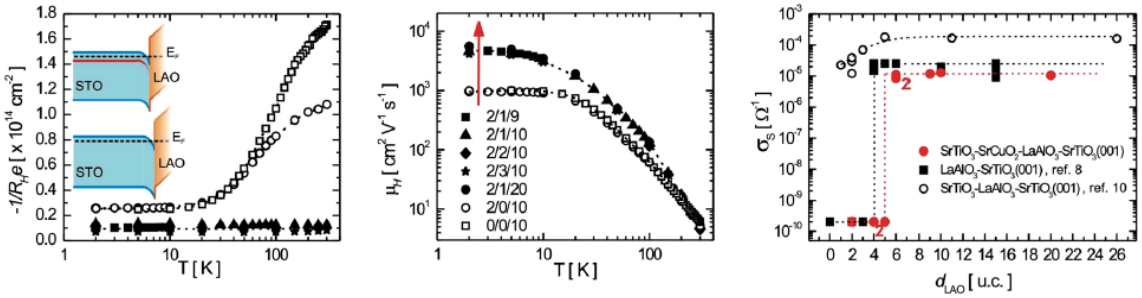

Figure 2.10 Characteristics of SCO-STO capped LAO-STO. Open symbols represent the normal LAO-STO interface, closed symbols represent the capped sample. a) carrier density as function of temperature. The inset shows the band diagrams for both interfaces, where the oxygen doping band is represented by the red line; b) mobility versus temperature; c) sheet conductivity versus LAO thickness. The critical thickness for these samples is 6 uc. Image taken from Ref. [32], Ref. 8 and Ref. 10 in the image are Ref. [15] and Ref. [61] in this work.

In figure 2.10c), one sees that the critical thickness has increased to 6 uc, which is an effect that has been seen for other capping layers [61-63], a parallel electron-hole bilayer was observed, where the holes and electrons were spaced only 1 nm apart. The application of the ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) as capping layer has led to a switchable ferroelectric state in the 2DEG [64].

2.3.4 ADSORBENTS ON LAO SURFACE

Adsorbed chemicals in fluid or gas phases can also be of large influence on the conductivity [65]. This is shown in an electronic reconstruction representation in figure 2.11. Because of this sensitivity, the LAO-STO interface may be used as a sensor for chemicals in a solution or in the atmosphere. This is limited by all other tuning opportunities, which act as uncertainties in this application and sensors require as little uncertainties as possible to be functional.

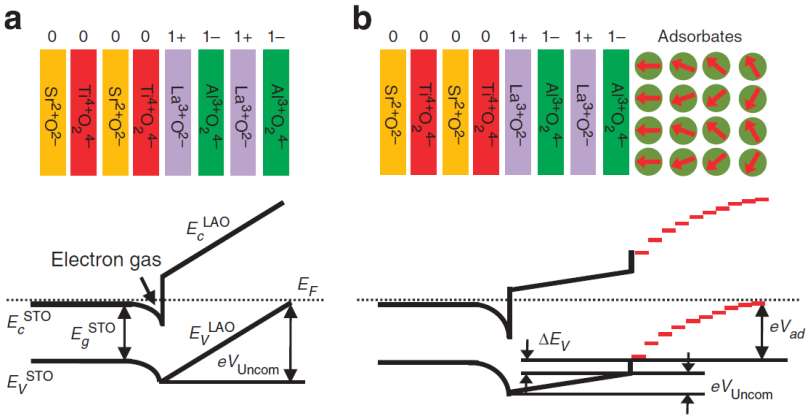

Figure 2.11 Influence of adsorbents on band alignment. Image taken from Ref. [65].

2.4 ELECTROSTATIC TUNING OF THE 2DEG

The properties of the interface can thus be tuned during growth, but these properties cannot be changed anymore after a device has been fabricated. To tune the electronic transport properties of the device, electrostatic tuning can be done. A model for the effects of electrostatic tuning will be derived in chapter 3. Here, we discuss reports of electrostatic tuning in literature, which is done by back-gating through the STO substrate, and by top-gating through the LAO film.

2.4.1 BACK-GATING

Back-gating was the first demonstrated method to tune the 2DEG electrostatically [15]. It is easily realized experimentally, as it is generally done by applying silver paint to the back side of the sample and gluing it on a metallic plate [15,21].

The result and setup of one of the first reported back-gating experiments on LAO-STO [20] are shown in figure 2.12. Because of the high dielectric constant of STO at low temperature, the 2DEG can easily be manipulated from afar by such a gate. Both the carrier density and the mobility can be tuned by back-gating [21]. By tuning the carrier density, different electronic phases in the 2DEG – e.g. superconductivity, spin-orbit coupling – have been shown to be experimentally accessible [20,26,96].

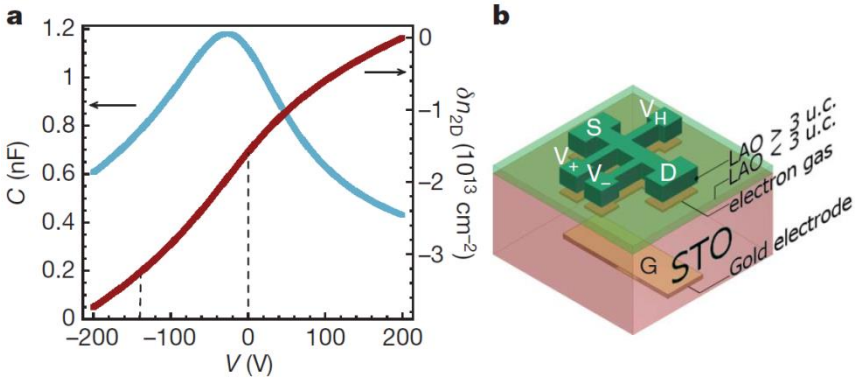

Figure 2.12 Electrostatic tuning of the 2DEG by back-gating. Image taken from Ref. [20]. a) Measured capacitance as function of gate voltage and derived carrier density by the parallel plate capacitor model; b) schematic of the sample geometry.

As observed by Bell *et al.* [21], the carrier density and the mobility both increase by applying a positive gate voltage, as depicted in figure 2.13a). This increase in carrier density can easily be understood by regarding the back-gated system metal as a parallel plate capacitor: as the gate is positively charged, it attracts negatively charged electrons onto the other side. The change in mobility is not so straightforward: it implies that the average scattering time or the effective mass in changed as the carrier density is manipulated. This was attributed to a change in the electron distribution in the confinement direction: for a negative gate voltage, the 2DEG is pushed closer to the interface and vice versa. Calculations of the electron distribution were done, which are shown in figure 2.13b). The different scattering mechanisms at play were suggested to be stronger near the interface, which would explain the change in mobility.

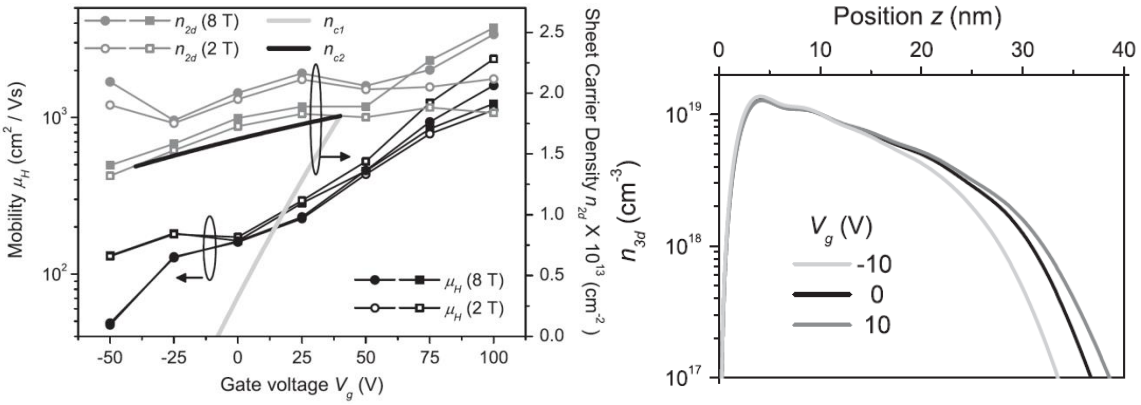

Figure 2.13 measured effect of back-gating to 2DEG properties. Image taken from Ref. [21]. a) tuning of mobility and carrier density by back-gating. b) Calculated distribution of electrons in the out-of-plane direction as a function of gate voltage.

2.4.2 TOP-GATING

For the development of nanoscale devices, it is of importance to tune the 2DEG on a scale of the order of the mean free path of the electrons. This cannot be done by back-gating, which has a very large area of effect as it is done through the substrate. Top-gating through the LAO layer is

Due to the high intrinsic carrier densities in LAO-STO 2DEGs and the, therefore, required high electric field strengths to tune it, top-gating was considered impractical [14] as compared to back-gating, where high field strengths can be attained due to the extremely high dielectric constant at low temperatures.

Before gating of LAO-STO heterostructures was considered, LAO has been investigated as a gate dielectric for semiconductor systems by Edge *et al.* [34]. In this study, the amorphous LAO showed promising results to create high electric fields with low gate voltages, due to its reportedly high thin film dielectric constant $\epsilon_r \sim 18$.

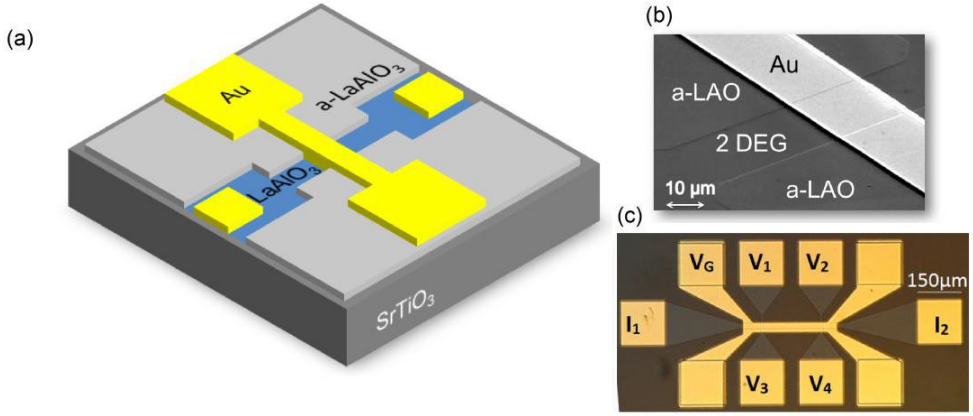

Figure 2.14 Top-gated devices in structured LAO-STO systems. Image adapted from Ref. [25]; a) schematic of an Au-LAO-STO tunnel junction, which can be used as a field-effect transistor device; b) SEM image of a fabricated devices as in 2.a; c) Top-gated Hall bar structure, which was the starting point for the Hall bars measured in this thesis.

The first successful top-gated devices were done by reduction of the carrier density to better tunable values. This has been done by capping with YBCO ($YBa_2Cu_3O_7$) [22,23], where the YBCO has also been utilized as a top gate electrode. With such samples, the compressibility of the 2DEG was investigated [23] and the first LAO-STO field-effect devices were produced [22]. Top-gating by a metal electrode (Au) has been demonstrated later on [24,25]. With such devices, the first modulation of superconductivity in LAO-STO by a top gate was achieved [25] and field-effect devices with full depletion of the 2DEG were reported [24]. With a top electrode, tunneling through the LAO was investigated by [60], which will be discussed in more detail in chapter 5.

2.5 BAND STRUCTURE

The band structure of the 2DEG is subject to much debate, as is an intricate interplay between many factors, like the origin of the conductivity. The main factors that describe it are the confining electric field, the band structure of the STO and the strain at the interface [47,66,67].

The confining electric field is related to the carrier density (chapter 3), which may originate from several subbands in the resulting subband structure of the 2DEG [66,68]. For a single-band 2DEG like the one in the GaAs-AlGaAs system, the wave function and the confinement potential can be solved self-consistently [69]. As more bands are introduced, this becomes a more complex calculation. An attempt to apply a self-consistent tight-binding approach to the system has recently been done for a doped STO surface [67], but such a calculation for the LAO-STO interface has not yet been reported.

2.5.1 PROPOSALS BASED ON MEASUREMENTS

Density Functional Theory (DFT) calculations [47,70,71] show that the conduction band of STO is closer to the Fermi level than the valence band is. In the conduction band, the Ti-3d orbitals are the ones closest to the Fermi level. This corresponds to the electronic reconstruction scenario, where the Ti-ions are the ions that are changed in valence.

The orbital energies of the STO Ti-3d orbitals were mapped out by X-ray photoemission for different LAO layer thicknesses by Saluzzo *et al.* [72], who showed a constant energy shift of these orbitals above $d_{LAO} = 4$ uc, the critical thickness of the LAO layer.

Measurements of surface states can be done by Angle Resolved Photo-Emission Spectroscopy (ARPES), a surface-sensitive technique [e.g. 73]. ARPES is unsuitable for studying LAO-STO as the interesting part is buried beneath the surface. Despite this drawback, the method has been successfully applied to investigate the surface states of STO, as is discussed below.

The surface of STO was made conducting by oxygen vacancy doping by Santander-Syro *et al.* [68]. Measurements uncovered that the surface states possess several subbands that cross the Fermi energy. These subbands originate from the Ti 3d orbitals in the system, for d-wave symmetry was assumed. In the bulk, the bottoms of the bands are at the same energy, but at the surface, they split into multiple subbands due to the strong electric field and the resulting confinement of electrons. This is depicted in figure 2.15 below.

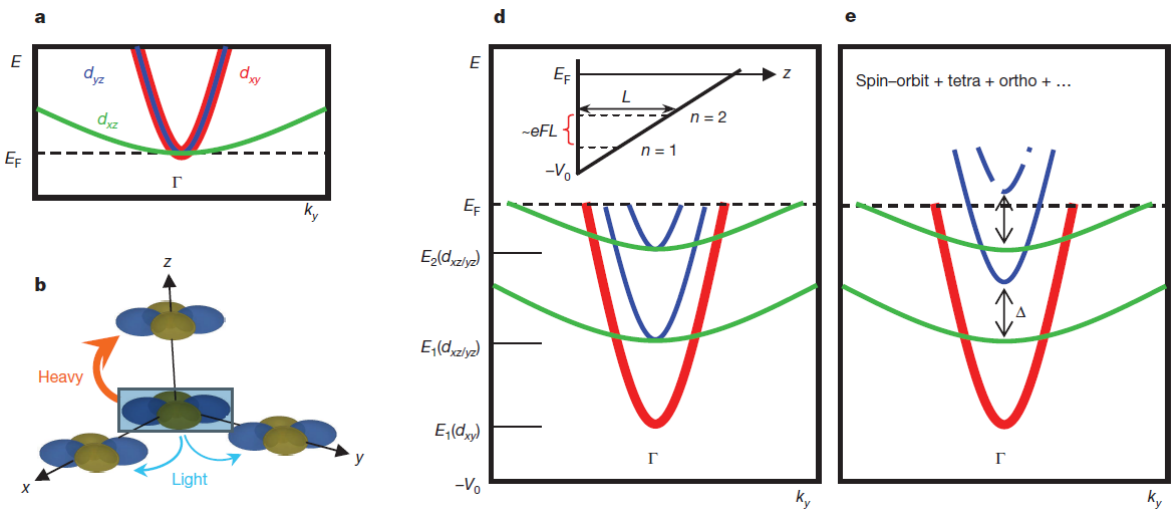

Figure 2.15 Proposed subband structure by Santander-Syro *et al.* [68]. Image taken from this reference. a) Bulk band structure of STO with Ti $3d_{xy}$, $3d_{xz}$ and $3d_{yz}$ bands; b) proposed band conduction mechanism, where the in-plane conductivity has the lower effective mass due to better band alignment of the in-plane bands; d) subband splitting as a result of the confinement potential from the inset; e) additional subband splitting due to spin-orbit interactions and structural distortions in the material. This structure fits best to the ARPES measurements done for the same work.

Such results treat a bare STO surface, but the authors argue that, regarding the strikingly similar results for several studies of the STO ground state in heterostructures and STO based devices [11,15,71,74], the band structure of the 2DEG between LAO and STO and the conducting STO surface states will not be very different. We emphasize that such results should be taken with a grain of salt as the origin of the conductivity can have a large influence on the (sub)band structure, as discussed in the section introduction.

In their study of the response of the system to a magnetic field, Joshua *et al.* [66] found a critical carrier density at which non-linear Hall signals emerge. They explain this phenomenon with a Lifshitz transition: a phase transition between 2D- and 3D-dominated conductivity. In the Ti 3d band picture, this can be understood as a strong increase in the contribution to transport of the out-of-plane bands, $3d_{xz}$ and $3d_{yz}$. This Lifshitz transition was ascribed to band hybridization by an atomic spin-orbit coupling energy ΔASO [75, 76]. In this study, figure 2.15d) was modified to this assumption, the result of which is given in figure 2.16i).

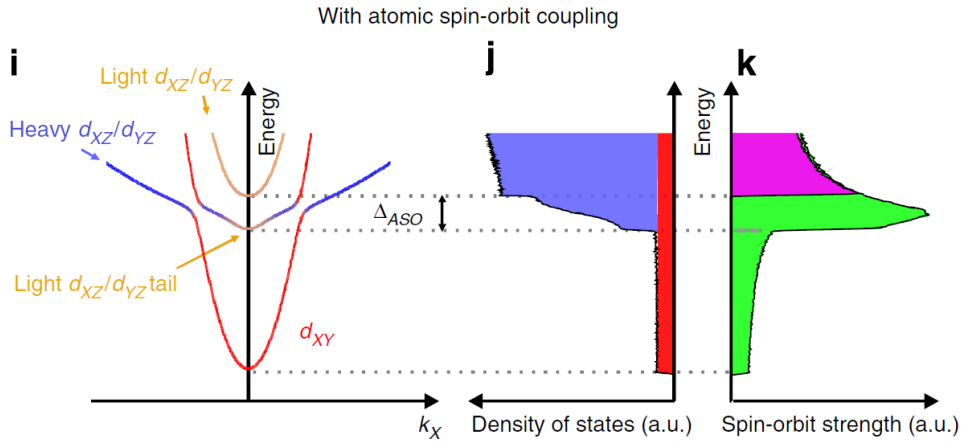

Figure 2.16 Influence of the atomic spin-orbit interaction on the band structure. Image taken from [66]. i) hybridized bands with atomic spin-orbit interaction; j) density of states as function of energy in this picture; k) spin-orbit coupling strength α as a function of energy.

In this picture, the density of states is given by 2.16j). In the case of parabolic bands, as pictured in figure 2.15d), one would assume a constant 2D density of states for each band [28]. This is lifted by the strong atomic spin-orbit coupling at the interface, which is a result of the strong confinement potential. The strength of this spin-orbit coupling α is dependent on the energy, which was also argued in [26,30].

2.5.2 SUBBAND STRUCTURE CALCULATIONS

Density Functional Theory (DFT) calculations for an STO-LAO superlattice have been carried out by Popović *et al.* [71]. They find that the electrons are expected to occupy multiple subbands that form at the interface. The resulting subband structure is given in figure 2.17.

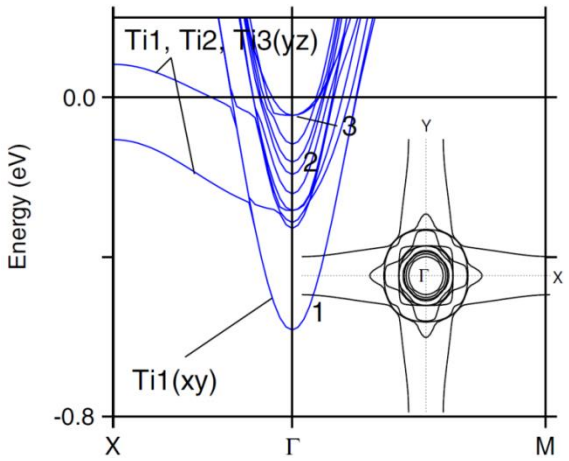

Figure 2.17 Calculated subband structure for the STO surface in an $STO_{7.5}$-$LAO_{7.5}$-superlattice. The inset shows the resulting Fermi surface in the xy-plane. Image taken from Ref. [71]

This calculation shows that heavy, localized subbands are to be expected. These localized subbands can be filled by electrons in the electronic reconstruction scenario, though they will not contribute to conductivity and thus be invisible in a Hall measurement. The electronic reconstruction scenario may thus be true, as electrons may 'hide' in these localized subbands.

The results presented above are all based on the STO surface and its resultant band structure. In an attempt to describe the LAO-STO interface subbands themselves, Van Heeringen *et al.* [47] used a **k** · **p**-model. This model is based on DFT calculations, from which a simplified Hamiltonian is written down, that is valid for low energies. This Hamiltonian is then solved to obtain the energy eigenvalues of the subbands involved at the LAO-STO interface.

The resulting band structure is somewhat different than the band structures described above: the heaviest band is the lowest in this model and is strongly non-parabolic. This gives it a non-constant density of states, as is depicted in figure 2.17a). Figure 2.17b) shows the prediction of the location of peaks in a Shubnikov-de Haas experiment, which match experimental results on SCO-STO capped samples [77]. This measurement shows that this model can be applied in certain samples, but its validity on an uncapped LAO-STO interface is yet to be confirmed.

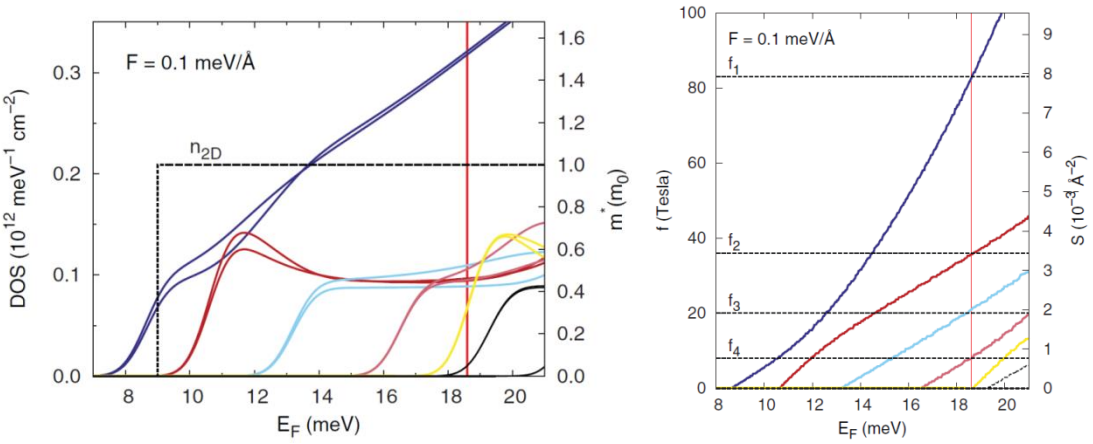

Figure 2.18 Results of **k** · **p**-model calculations, image taken from Ref. [47]; a) subband density of states from the **k** · **p**-model; b) predicted location of Shubnikov-de Haas peaks.

3. ELECTROSTATICS OF THE $LaAlO_3$-$SrTiO_3$ INTERFACE

The physical properties of the 2DEG at the heterointerface between LAO and STO depend strongly on the shape of the confining potential [21,47,59,68]. This is why the clear difference between top- and back-gating is not surprising. Not only carrier density and mobility are differently affected, there is also evidence that the mechanism of superconductivity depends on the confinement potential [20], as well as the mechanism of spin-orbit coupling [26] and possibly many more interesting properties.

In this chapter, the effects of electrostatic tuning of the 2DEG are discussed. First, the concept of potential confinement of the carriers is introduced. Next, we discuss a simple model for the band alignment at the LAO-STO interface, which we refine to include metallic top-electrodes. Based on this simple model, we derive an expression for the capacitance as a function of carrier density, which depends on the top-gate voltage. We also give an expression for back-gating, which exemplifies the differences between the two gating methods.

3.1 CONFINEMENT POTENTIAL

The charge carriers are (electrostatically) confined in a region of ~ 10 nm close to the heterointerface [3,21,67]. The resulting quantum mechanical energy level spacing results in a complex subband structure [47], depending on the potential in which these energy levels reside. The simplest model for the confinement potential is a triangular potential well that extends into the STO, with an infinite barrier on the LAO side (figure 3.1a)).

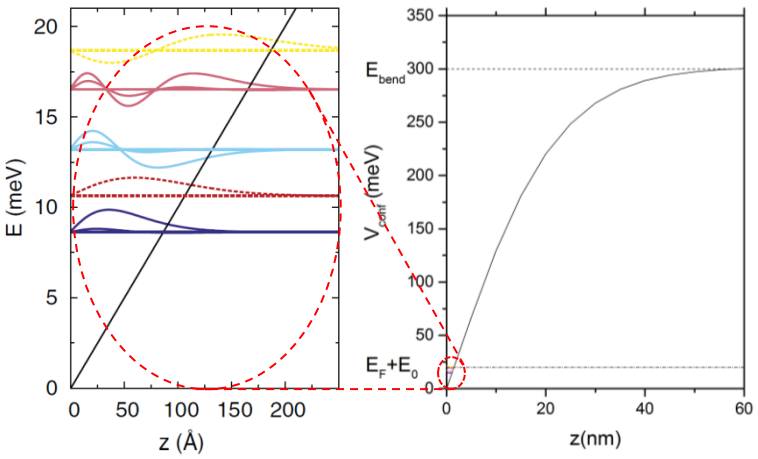

Figure 3.1 Confinement potentials a) triangular potential well with Airy wave functions. Image taken from Ref. [47]; b) Calculated potential well for a single-band model. The relation of figure (a) to figure (b) is given by the red dashed ellipses.

The slope of the confinement potential is the local electric field, which is taken as a parameter for calculations. For the GaAs-based 2DEG, calculations have been done to model this potential well accurately [69]. This is done by solving the wave function in the z-direction self-consistently, i.e. by writing down a trial wave function, relate the potential to the wave function by the Poisson equation and minimize the energy with respect to the variational parameter.

Unfortunately, such a model is not directly applicable to the LAO-STO interface due to three complications:

1. The underlying bulk band structure includes several bands with different geometry [47,67], where the model by Ihn considers a single band;
2. In the model based on GaAs-AlGaAs, the dielectric constant is the same and constant everywhere. The STO dielectric constant ϵ_{STO} is very different from the one in LAO, ϵ_r, and is also electric field- and temperature-dependent [34,38,39];
3. The electric field strength in LAO is lower than the electric field strength of a surface charge $e\Delta n_s$: according to the electronic reconstruction model, this field would be completely cancelled to avoid the polar catastrophe [1]. However, a small, remnant field has been measured [48].

This makes the confinement in the LAO-STO system harder to model than in the GaAs-AlGaAs system. This has been done for an oxygen-vacancy-induced STO surface 2DEG by King *et al.* [67], where a potential well depth of ~ 270 meV was used [78]. We note that this is value is very close to the LAO core-level shifts of ~ 300 meV found by Slooten *et al.* [48].

We now address the generic shape of the potential well. It is a solution to the Poisson equation as it screens the interface electric field into the STO. Therefore, it is continuous and contains no local minima, except at the interface. This can be solved for a known charge distributions and known boundary conditions. The actual charge distribution is unknown, but we can describe the boundary conditions. Deep in the STO, the electric field must be zero by energy minimization, so the first boundary condition is

$$\frac{\partial V}{\partial z}(z = \infty) = 0.$$

For the second boundary condition, we assume that all the charge sits exactly at the interface and it generates an electric field

$$\frac{\partial V}{\partial z}(z = 0) = \frac{en_s}{\epsilon_{STO}\epsilon_0}.$$

This is a strong assumption that disregards the suggested spreading of the wave functions into the STO [3,21,47]. The resulting potential well in a single-band model with these boundary conditions is given in figure 3.1b). This shape is very similar to the shape found by [67] for the self-consistent tight-binding approach.

We model the filling of this potential well following the reasoning by Ihn [67]. The chemical potential of the 2DEG with respect to the bottom of the well is given by the sum of the energy of the lowest subband, E_0, and the Fermi energy with respect to this energy, E_F, so

$$\mu_{2DEG} = E_0 + E_F.$$

From the calculations by Van Heeringen *et al.* [47], we obtain that $\mu_{2DEG} \sim 25$ meV for samples with carrier density $n_s \sim 10^{13}$ cm^{-2}, which includes the offset from the bottom of the potential well, as visible in figure 3.1(a). Then, the wave functions are in the part of the potential well that is approximated by a triangular potential well, as can also be seen from figure 3.1(b).

3.2 BAND ALIGNMENT

LAO and STO are band insulators, which undergo a band alignment when they are brought into contact [79]. This band alignment is governed by the energy levels in the materials. The relevant energy levels in LAO and STO are given below [33].

Parameter	Formula	STO	LAO
Band gap	E_g (eV)	3.3	5.6
Electron affinity	χ (eV)	3.9	1.3
Charge neutrality level above valence band	$\Phi_{CNL} - E_v$ (eV)	2.6	3.8
Charge neutrality level below vacuum	Φ_{CNL} (eV)	4.6	3.1

Table 3.1 Energy levels in LAO and STO

In figure 3.2a) through c), we plot the band alignment of the LAO-STO interface , as calculated from the values in table 3.1. We note that the values in table 3.1 are bulk values and the thin film energy levels can be different due to e.g. strain, which alters the band structure by changing the lattice parameters. In figure 3.2a), the LAO and STO energy levels are shown, with respect to the vacuum level E_{vac}. The conduction band bottom E_c, the valence band top E_v and the charge neutrality level above the valence band are depicted. The charge neutrality level below vacuum is denoted as the Fermi energy E_F, since these play the same role in these diagrams.

By requiring thermal equilibrium at the interface, the charge neutrality levels of the STO and the LAO are pinned and the vacuum level is misaligned (figure 3.2b). This vacuum level represents the electrostatic potential, which has to be continuous by Gauss' law of electrostatics. The discontinuity is solved by screening the potential shift in the material with the smallest band gap, in this case STO. We relate to the layer in which (bound) charge is induced this way as the screening region. It has a spatial extent parameter, the screening length λ_s, and a bending energy E_{bend}, which is defined as the energy difference between the bottom and top energies of the layer. This creates a potential well close to the interface and a band offset of both the conduction and valence bands, as depicted in figure 3.2c). Calculated from these bulk values, we find $E_{bend} = 1.5$ eV, which is an order of six higher than experimental values [67]. This supports the statement that thin film energy levels may differ from bulk values.

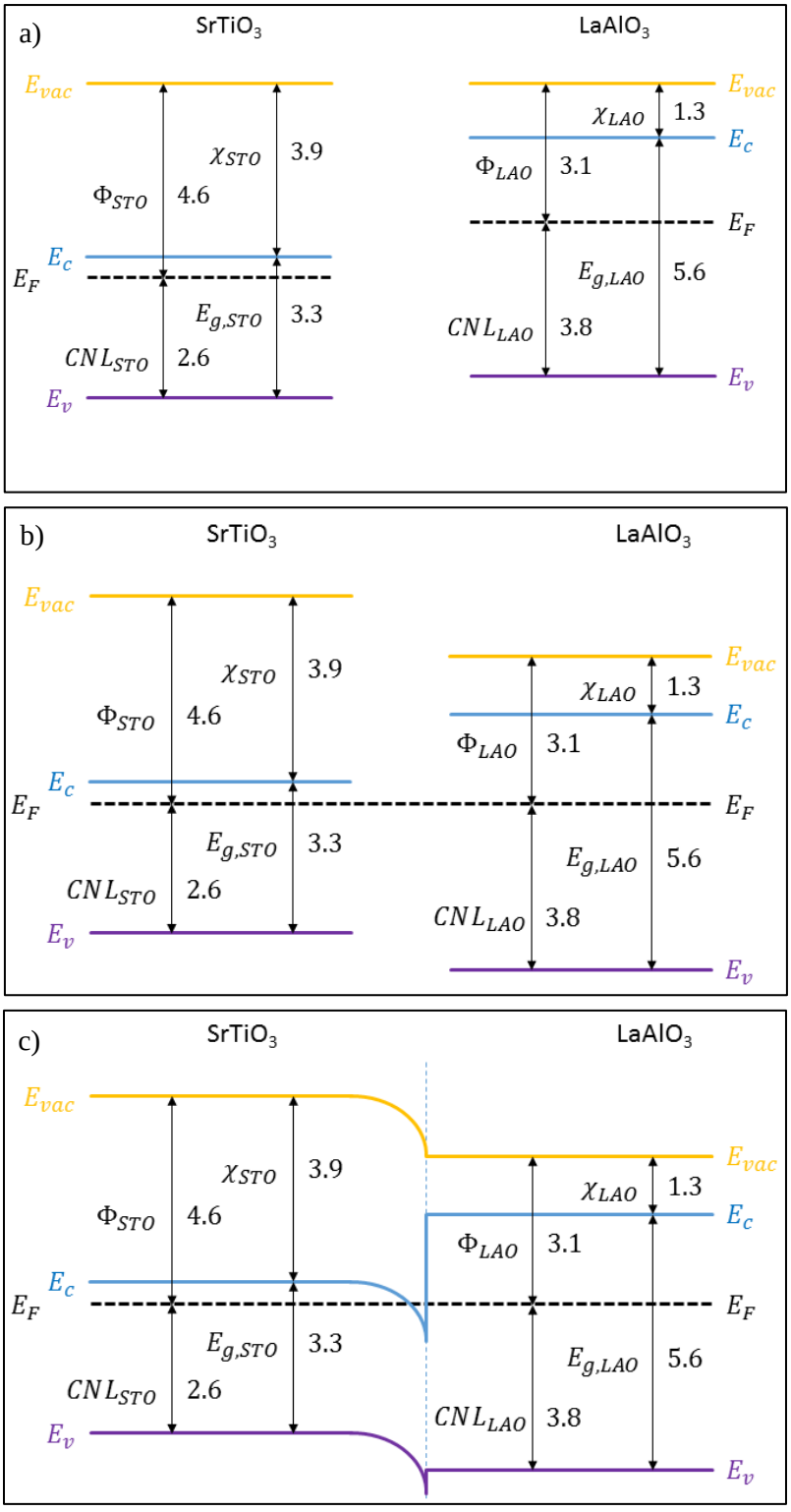

Figure 3.2 Band alignment of the LAO-STO interface; a) band energies of both materials with respect to the vacuum level; b) energy levels from a) after pinning the Fermi levels; c) band bending in STO. This makes E_{vac} continuous along the interface, defining a potential well in the STO and an energy barrier between the well and the LAO.

In this picture, the electrostatic potential buildup due to the electric field in the polar material (LAO) is completely compensated by the electronic reconstruction. This is an approximation that corresponds to experiments conducted by Slooten *et al.* [48]. In that study, a shift of the LAO core-level energy of 300 meV was found between a sample below and above the critical thickness. Above 6 uc, the total shift appears to be constant in thickness.

We take this thickness-independent internal potential build-up $E_i \sim 300$ meV across the LAO layer into our model. In figure 3.2, this internal potential build-up is included in the band offset ΔE_c. Then, we may write

$$\Delta E_c = E_{g,LAO} - E_{g,STO} + E_i - \Delta E_v.$$

3.2.1 APPLICATION OF A METAL GATE ELECTRODE

When a metal top gate is added, another Fermi level pinning takes place: between the LAO and the Au. The Au top electrode creates a screening in the LAO. The screening length associated with this additional (3D) charge carrier density n is given by [79]:

$$\lambda_s = \sqrt{\frac{2\epsilon_r \epsilon_0 |\Phi_b|}{ne}},$$

where Φ_b is the Schottky barrier between the metal and the dielectric. We assume the $\epsilon_r = 18$ [34], $n = n_s^{3/2}$and $n_s \sim 10^{13}$ cm^{-2}. The Schottky barrier height is given by [33]:

$$\Phi_b = S(\Phi_m - \Phi_{CNL}) - (\chi_{Ox} - \Phi_{CNL}),$$

where Φ_m is the work function of the metal, Φ_{CNL} is the charge neutrality layer and χ_{Ox} is the electron affinity of the oxide. The factor S determines the effect of screening on the energy levels on a long scale. For simplicity, we take $S = 1$ since typical LAO film thicknesses are smaller than the charge screening length scale; thus the equation simplifies to:

$$\Phi_b = \Phi_m - \chi_{Ox}.$$

Using typical values for the work functions of metals [80] and the electron affinities of the oxides in table 3.1. We find the Schottky barrier heights listed in table 3.2.

Metal	Φ_m(eV)	$\Phi_b(STO)$(eV)	$\Phi_b(LAO)$(eV)
Au	5.1	1.2	3.8
Ag	4.26	0.36	2.96
Pt	5.65	1.75	4.35

Table 3.2 Schottky barriers between LAO, STO and different gate metals.

In turn, we may now calculate the screening length for, e.g., Au with a Schottky barrier height of 3.8 eV and find $\lambda_s \sim 15$ nm, which is much longer than the LAO film thickness in a typical heterostructure. Thus, for a simple estimate, we assume that the potential difference drops linearly across the LAO layer, and arrive at the band alignments shown in figure 3.3(a) and (b).

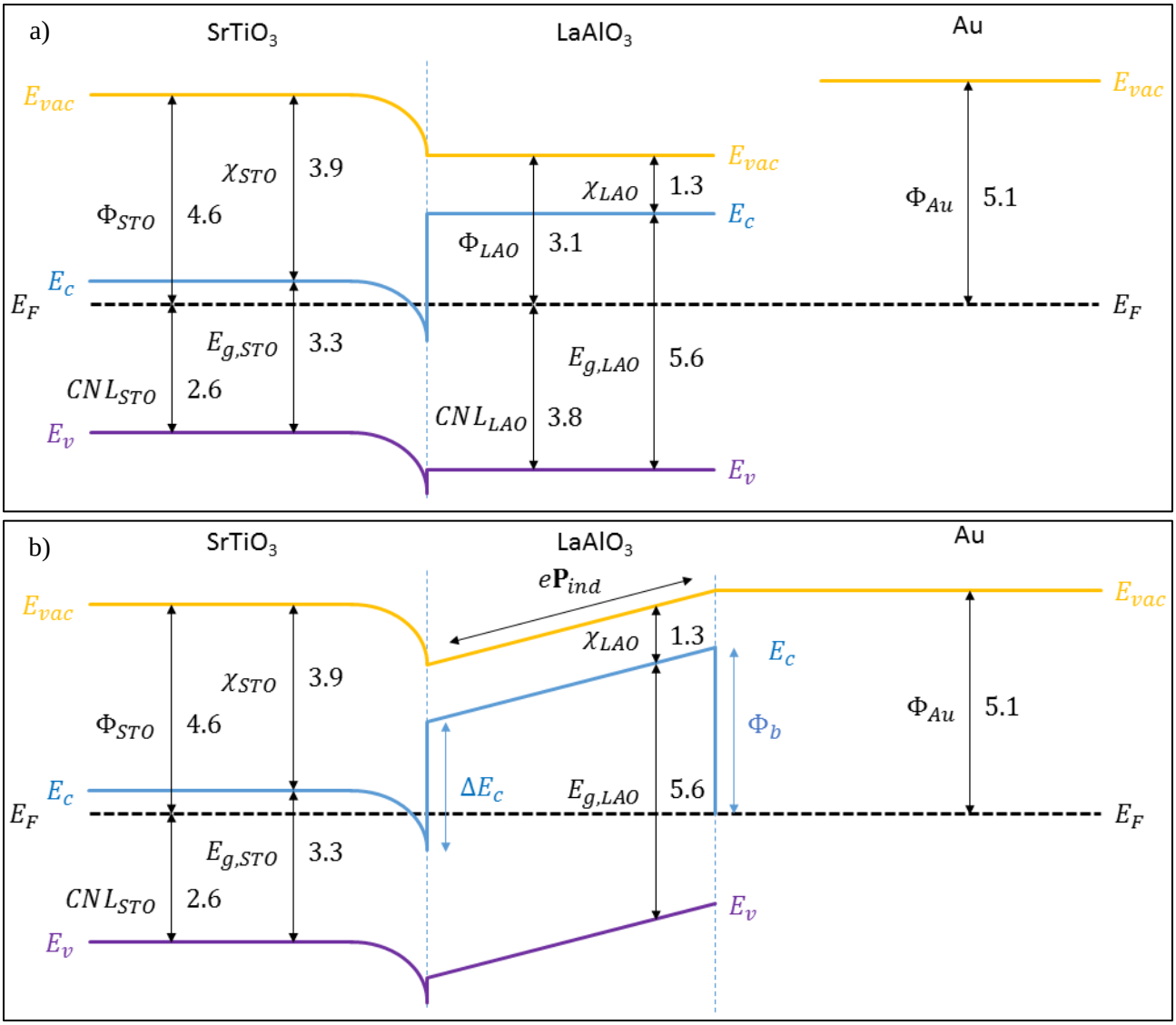

Figure 3.3 Band alignment with gate electrode; a) Fermi level pinning of Au and LAO-STO interface, as calculated in figure 3.2c). b) creation of a charge inversion layer that is larger than the LAO film thickness and assumes a linear potential gradient across the LAO. The $e\mathbf{P}_{ind}$ is the induced polarization by applying the top gate material.

In figure 3.3a), the chemical potential (Fermi energy) of the Au and the 2DEG are chosen equal in thermal equilibrium, which corresponds to the experimental situation when the top-electrode is connected to the same electrical potential as the 2DEG through the external wiring (i.e., "top-gate electrode and 2DEG are grounded."). As discussed above, we assume a linear potential drop in the LAO, which is equivalent to a constant induced polarization $e\mathbf{P}_{ind}$ and a shift in carrier density of:

$$e\mathbf{P}_{ind} = e^2 \Delta n_s.$$

compared to the system without a top gate electrode.

From figure 3.3b), we find this induced polarization to be:

$$e\mathbf{P}_{ind} = \frac{\epsilon_0 \epsilon_r}{d_{LAO}} [\Phi_b - \Delta E_c + E_0 + E_F],$$

where $E_0 + E_F$ is the energy in the potential well, see next section. Following calculations by, e.g., Van Heeringen *et al.* [47], this energy amounts to ~ 20 meV, where ΔE_c and Φ_b are of the order of eV. Since

$$E_0 + E_F \ll \Phi_b, \Delta E_c,$$

we have

$$\Delta n_s \approx \frac{\epsilon_0 \epsilon_r}{e^2 d_{LAO}} [\Phi_b - \Delta E_c].$$

The valence band offset is small compared to the conduction band offset, so we neglect it. Then we may write

$$\Delta E_c \approx E_{g,LAO} - E_{g,STO} + E_i = 2.6 \text{ eV}.$$

Using $\Phi_b = 3.8$ eV from table 3.2, we find for $\epsilon_r = 10$ and $d_{LAO} = 3.75$ nm (10 uc):

$$\Delta n_s \sim 2 \cdot 10^{13} \text{ cm}^{-2},$$

which is of the order of the carrier density of the bare heterostructure (without top-gate electrode).

With additional capping layers, following Huijben *et al.* [32], one would expect a major change in this reasoning as a first thought. There will be additional energy barriers between the stacked layers as their electron affinities are different and the top material (e.g. STO) will have a different Schottky barrier height. However, all these additional energy barriers and the change in the Schottky barrier height will cancel out, as one takes the relative electron affinities into account. As long as the screening length is longer than the film thickness, we expect our order-of-magnitude estimate to apply.

3.3 THE EFFECT OF A TOP GATE VOLTAGE

One can apply a gate voltage between the top gate and the 2DEG by attaching a voltage source between the gate and the 2DEG. In the following, we define the 2DEG as the negative side of the voltage source, and the gate as the positive side. See figure 5.1 for details of this wiring.

3.3.1 PARALLEL PLATE CAPACITOR MODEL

A top gate on LAO-STO is often modeled as a simple parallel plate capacitor [24,30]. This is a model that depends only on the device geometry and the dielectric constant ϵ_r of the dielectric material. The capacitance of a system relates an accumulated charge on a capacitor to the voltage drop across that capacitor. For a parallel plate capacitor, it is given by:

$$C = \frac{\epsilon_r \epsilon_0 A}{d},$$

where ϵ_r is the effective dielectric constant of the dielectric material, A is the area of the capacitor and d is the distance between the two plates. The carrier density can be written as a a number of charged carriers Q/e per unit area A, so via $\Delta Q = C\Delta V$, one can extract the dependence of the carrier density on the gate voltage:

$$n_s(V_G) = \frac{\epsilon_r \epsilon_0}{ed} V_G + n_s(0) \rightarrow \Delta n_s = \frac{\epsilon_r \epsilon_0}{ed} V_G.$$

The derivative of the carrier density with respect to the gate voltage is defined as the capacitance per square $C_{sq} = C/A$:

$$C_{sq} \equiv e\frac{dn_s}{dV_G} = \frac{\epsilon_r \epsilon_0}{d}.$$

This simple model supports the intuition that a positively charged gate attracts more (negative) electrons into the 2DEG and vice versa. However, this simple model holds only when both electrodes are simple metals such as Au. Unfortunately, this is not the case when gating a 2DEG, as is described extensively in chapter 9 of Ref. [69] for the GaAs-AlGaAs system.

3.3.2 CAPACITANCE BY A CHEMICAL POTENTIAL DIFFERENCE

In a top-gated LAO-STO system, one of the electrodes is a 2DEG and not a simple metal. The applied gate voltage enters as an offset between the chemical potential of the top gate and that of the 2DEG:

$$-eV_G = \mu_G - \mu_{2DEG},$$

where μ_G is the chemical potential of the top gate and μ_{2DEG} is the chemical potential of the 2DEG. The minus sign of the voltage term is due to the electric field E that the voltage induces and the corresponding electrostatic potential ϕ is defined via $eE = -\nabla\phi$. In figure 3.4a), we have defined the bottom of the potential well in the STO as $\mu \equiv 0$, so we can give an expression the chemical potential of the top gate:

$$\mu_G = -E(\mathbf{P}_{gate}) + \Delta E_c - \Phi_b.$$

Here, $E(\mathbf{P}_{gate})$ is the energy that corresponds to a gate-induced polarization $\mathbf{P}_{gate}$ in the LAO. This energy is an electrostatic energy and can be written as the energy of a parallel plate capacitor with an induced carrier density Δn_s.

$$E(\mathbf{P}_{gate}) = \frac{e^2 \Delta n_s}{\epsilon_r \epsilon_0} d_{LAO}.$$

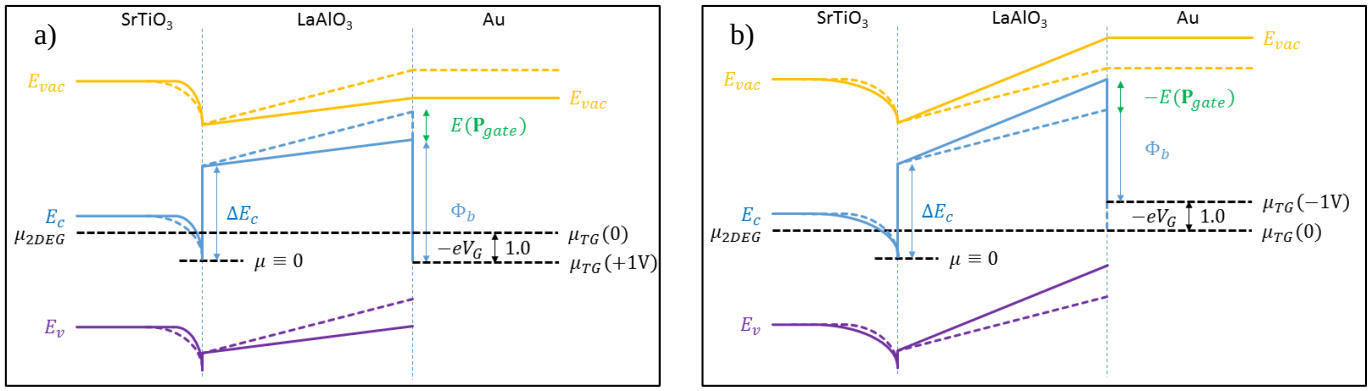

Figure 3.4 Effect of a gate voltage on the band alignment of the system, where a gate-induced polarization energy $E(\mathbf{P}_{gate})$ adds to the barrier. The dashed lines correspond to the band alignment in figure 3.3b, which is the case for zero gate voltage. a) positive gate voltage, with a relatively narrow potential well. b) negative gate voltage, with a relatively broad potential well.

In section 3.1, we found the chemical potential of the 2DEG to be

$$\mu_{2DEG} = E_F(n_s) + E_0(n_s).$$

Now, we can properly define the effect of a top gate voltage V_{TG} on the 2DEG:

$$-eV_{TG} = \mu_{TG} - \mu_{2DEG} = -\frac{e^2 \Delta n_s}{\epsilon_r \epsilon_0} d_{LAO} + \Delta E_c - \Phi_b - E_F(n_s) - E_0(n_s).$$

Via the derivative of the carrier density n_s to the gate voltage V_G, we can find the capacitance per square. If we take the derivative of the equation above with respect to the carrier density n_s, we find:

$$\frac{dV_G}{dn_s} = \frac{e d_{LAO}}{\epsilon_r \epsilon_0} + \frac{1}{e}\frac{dE_F}{dn_s} + \frac{1}{e}\frac{dE_0}{dn_s}.$$

We can invert this equation to find the capacitance per square:

$$C_{sq} = e\left(\frac{dV_G}{dn_s}\right)^{-1} = \left(\frac{1}{\epsilon_r \epsilon_0}\left[d_{LAO} + \frac{\epsilon_r \epsilon_0}{e^2}\frac{dE_F}{dn_s} + \frac{\epsilon_r \epsilon_0}{e^2}\frac{dE_0}{dn_s}\right]\right)^{-1}.$$

Here, the first term represents the geometrical factor that corresponds to the parallel plate capacitor model. The second term can be recognized as the inverse of the density of states at the Fermi level:

$$g_{2D}(E_F) \equiv \frac{dn_s}{dE}(E_F).$$

The second term of the capacitance above is also called the quantum capacitance $C_q = e^2 g_{2D} A$. It depends on the density of states, which can be taken as the sum over the density of states of all contributing subbands. The structure of the subbands is subject of much debate [47,66-68,71], so a capacitance measurement as a function of the carrier density could reveal valuable data on the density of states of the subband structure. In such a measurement, one can translate the carrier density to the Fermi level by:

$$E_F(n_s) = \int_0^{n_s} \frac{1}{g_{2D}(n_s')} dn_s'.$$

The third term is the dependence of the $n = 0$ solution of the Schrödinger equation in the confinement potential well. This potential well has been discussed in section 3.1 and close to the interface, it can be considered triangular with the interface electric field as the slope. This electric field originates from an assumed surface charge at the interface and thus, is proportional to the carrier density. In a quantum mechanical potential well, the energy of the solutions of the Schrödinger equation becomes larger as the well becomes narrower. In this potential well, the potential becomes narrower as the carrier density is increased. We can thus relate the carrier density n_s to the energy level E_0 via the potential well width W_0, the width at E_0:

$$\frac{dW_0}{dn_s} < 0 \; \forall \; n_s; \; \frac{dE_0}{dW_0} < 0 \; \forall \; E_0 \rightarrow \frac{dE_0}{dn_s} > 0 \; \forall \; n_s.$$

To determine whether the signal of these effects can be resolved in experiments, we can perform a simple order-of-magnitude calculation, where we assume $E_0 \sim 10$ meV [47], $n_s \sim 10^{13}$ cm^{-2}, $g_{2D} \sim m_e/\pi\hbar^2$, and $\epsilon_r = 18$ [64]:

$$d_{LAO} \sim 2 - 10 \text{ nm};$$

$$\frac{\epsilon_r \epsilon_0}{e^2} \frac{1}{g_{2D}} \sim 0.2 \text{ nm};$$

$$\frac{\epsilon_r \epsilon_0}{e^2} \frac{dE_0}{dn_s} \sim 0.1 \text{ nm}.$$

3.4 THE EFFECT OF A BACK GATE VOLTAGE

A back-gate experiment differs from a top-gate experiment, as the band alignments do not play a role and the thickness of the dielectric layer is several orders of magnitude larger, but so is the dielectric constant in the STO ($\epsilon_{STO} \sim 24{,}000$ at zero electric field [39]). The latter makes back-gating possible. Here, we briefly discuss the effect of a back-gate voltage on the 2DEG, following the steps in the previous section for the top-gate.

For a back-gate the potential well is on the same side of the interface. This implies that the boundary conditions from section 3.1 are changed in case of an applied electric field. Because of this field, the potential gradient deep in the STO is not zero anymore, but has a value

$$\frac{\partial V}{\partial z}(\infty) = eE = \frac{eV_{BG}}{d_{STO}},$$

where V_{BG} is the applied back-gate voltage and d_{STO} is the thickness of the STO substrate.

To describe the response of the 2DEG to an applied back-gate voltage, we want to write down the capacitance per square relation. For this, we draw the band alignment picture of an applied back gate of Ag, since the samples are usually mounted with silver paint [21]. The band alignment picture is given in figure 3.5.

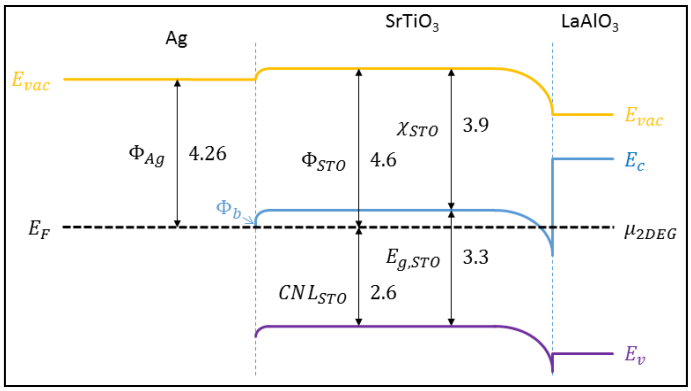

Figure 3.5 Band alignment of an applied back-gate to the STO substrate of the LAO-STO interface.

Here, a small downward bend is created, because the work function of the Ag is between the conduction band edge and the Fermi level of the STO.

The chemical potential of the 2DEG is the same as for the top-gated situation, but the chemical potential of the gate is different. An expression can be deduced from the band alignment in figure 3.5, with the same reasoning as for the top gate:

$$\mu_{BG} = -\frac{e^2 \Delta n_s}{\epsilon_{STO}\epsilon_0} d_{STO} + E_{bend} - \Phi_b.$$

Now, we can write the gate voltage equation:

$$-eV_{BG} = \mu_{BG} - \mu_{2DEG} = -\frac{e^2 \Delta n_s}{\epsilon_{STO}\epsilon_0} d_{STO} + E_{bend} - \Phi_b - E_F - E_0.$$

so the capacitance per square becomes

$$C_{sq} = e\left(\frac{dV_G}{dn_s}\right)^{-1} = \left(\frac{1}{\epsilon_{STO}\epsilon_0}\left[d_{STO} + \frac{\epsilon_{STO}\epsilon_0}{e^2}\frac{dE_F}{dn_s} + \frac{\epsilon_{STO}\epsilon_0}{e^2}\frac{dE_0}{dn_s}\right]\right)^{-1},$$

which is very similar to the result for the top-gated capacitance per square. Like for the top-gated capacitance, we can make an order-of-magnitude estimate of the terms in this equation, where we assume $E_0 \sim 10$ meV [47], $n_s \sim 10^{13}$ cm^{-2}, $g_{2D} \sim m_e/\pi\hbar^2$, and $\epsilon_{STO} = 24{,}000$ [39].

$$d_{STO} \sim 5 \cdot 10^{-4} \text{ m};$$

$$\frac{\epsilon_{STO}\epsilon_0}{e^2}\frac{1}{g_{2D}} \sim 3 \cdot 10^{-7} \text{ m};$$

$$\frac{\epsilon_{STO}\epsilon_0}{e^2}\frac{dE_0}{dn_s} \sim 1.5 \cdot 10^{-7} \text{ m}.$$

Here, the capacitance is dominated by the geometrical factor, which justifies the usage of a parallel plate capacitor model to a certain extent. Effects of the density of states are expected to be visible, but as very small features.

By the same reasoning as for the top gate, the change in carrier density due to a connected top gate can be calculated. Again, we consider $E_F, E_0 \ll E_{bend}, \Phi_b$, so the change in carrier density due an induced dipole across the STO is

$$\Delta n_s = \frac{\epsilon_0 \epsilon_{STO}}{e^2 d_{STO}}[\Phi_b - E_{bend}] \sim 3 \cdot 10^{10} \text{ cm}^{-2}.$$

We used the same assumptions as for the order of magnitude calculation, and Φ_b between Ag and STO from table 3.2. This change is two to three orders of magnitude lower than the typical carrier density at the LAO-STO interface, so the carrier density correction due to an induced dipole across the STO can be safely neglected.

Comparing the capacitance relations, the term dE_0/dn_s in the back-gated situation will be different due to the change in one of the boundary conditions for the Poisson equation. The effect for a single state in such confinement potential can be addressed using a model based on chapter 9 of [69]. In this approximation, the boundary condition of the confinement potential can be expressed in terms of the spatial expectation value of the resulting wave function, $\langle z \rangle$. The term in dE_0/dn_s can also be expressed in $\langle z \rangle$ via the solutions of the wave function in a self-consistent potential well.

Then, solving the gate voltage equation, one finds that $\langle z \rangle$ increases for a positive back-gate voltage, whereas it decreases for the positive top-gate voltage. This result is also interpretable in a Coulomb approach, where a positively charged gate attracts the negatively charged 2DEG. This was already discussed in section 2.4 for the back-gate measurements and calculations by Bell *et al.* [21].

In other words, the induced local electric field has a different sign for top- and back-gate voltages. The reasoning above must also hold for the LAO-STO system, despite the fact that the potential cannot be solved self-consistently with one wave function, because there are multiple subbands present in the potential well. If a self-consistent solution to the confinement potential can be made with multiple subbands involved, this can prove the suggested fundamental difference between top- and back-gating.

4. DEVICE DESIGN AND FABRICATION

The physical properties of oxide heterostructures depend sensitively on growth parameters of the materials, such as substrate temperature, oxygen pressure and target stoichiometry. In chapter 2, the most important parameters for LAO-STO, and ways to tune them have been discussed.

Before this work, several problems occurred in top-gated LAO-STO devices [25,30]. First, the hard mask layer used for top gating was often not insulating [31], so the structuring method had to be improved with a different hard mask material. Second, mobility was not as high as for unstructured samples [30], which were ascribed to organic residue from the photoresist used in patterning. Third, the sample design was tested during this work (not reported in this thesis) and contacts were pinched off easily by applying a gate voltage, so design had to be improved. Lastly, the gate leakage was found significantly lower in another study [24] than in the ones conducted in Twente [25,30], so new gate processing methods were to be considered.

In this chapter we discuss device design, substrate quality, film growth, structuring techniques, and gate patterning to improve the fabrication process. In chapter 6, we consider drawbacks of the current fabrication method and make suggestions for further improvement.

4.1 DEVICE DESIGN

In this work we studied devices in the Van der Pauw and in Hall bar geometry. Below, we discuss design criteria for these devices and present a sample design for top-gated Hall bars.

4.1.1 VAN DER PAUW GEOMETRY

A Van der Pauw measurement [79], as pictured in figure 4.1, can provide a good estimate of the Hall constant R_H and the sheet carrier density R_s by the Van der Pauw formula:

$$e^{-\pi\frac{R_A}{R_s}} + e^{-\pi\frac{R_B}{R_s}} = 1,$$

where $R_A = V_{12}/I_{34}$ and $R_B = V_{13}/I_{24}$, in which the choice of the corners 1, 2, 3, and 4 is arbitrary. This formula has no closed-form solution for R_s. However, if R_A and R_B are close in value, one may use the arithmetic mean and write

$$R_s' = \frac{\pi}{\ln(2)}\frac{R_A + R_B}{2}.$$

R_s' is a good approximation of the actual sheet resistance in most cases. In case of a large anisotropy ($R_A \gg R_B$ or vice versa), the Van der Pauw equation must be solved numerically.

The Van der Pauw measurement of a film can be wired in different ways, which are depicted in figure 4.1:

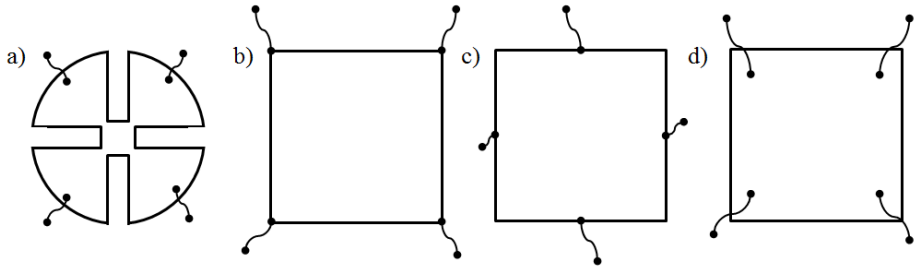

Figure 4.1 Wiring of Van der Pauw measurement, in order of preference; a) Ideal cloverleaf wiring, probing the region in the middle; b) Wiring to the exact corners of the sample; c) Wiring to the exact middle of the edge of the sample; d) wiring inside the sample perimeter.

The most favorable measurement is the cloverleaf (a), since this minimizes the influence of the contact geometry and only measures the central square. The contacts on the film perimeter are somewhat less favorable but should still show a good result as long as their contact area is much smaller than the film surface area (b, c). Under all circumstances, the contacts should not be placed within the film perimeter (d), as this adds conducting paths on the other side of the straight line between the current contacts; these are not properly probed by the voltage probes.

4.1.2 HALL BAR

A Hall Bar is a device in which the Hall resistance and a four-point longitudinal resistance can be simultaneously measured in a straightforward geometry. A typical Hall Bar is shown in figure 4.2.

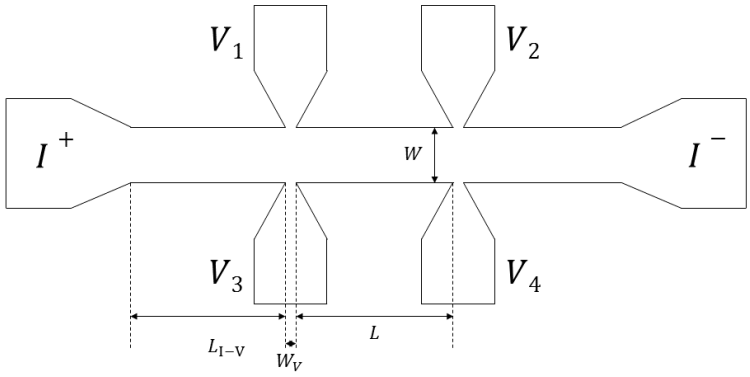

Figure 4.2 Hall bar geometry with two current pads I^+ and I^- and voltage pads V_{1-4}.

A measurement of sheet resistance is carried out by running a current between the current contacts I^+ and I^- and measuring a voltage between different voltage pads. The longitudinal voltage, V_L, is measured between contacts 1/3 and 2/4. The Hall voltage, V_H, is measured between contacts 1/2 and 3/4, in an out-of-plane magnetic field. The origin of this Hall voltage is described below.

An applied magnetic field exerts a Lorentz force on the charge carriers, which pick up a drift momentum perpendicular to the externally applied current. As a result, a Hall voltage V_H develops which can be picked up between voltage probes on opposite sides of the Hall bar. This Hall voltage is different for conduction with one type of carriers and for more types of carriers. For one carrier type, it is given by

$$V_H = \pm\frac{IB}{n_s e},$$

where the sign is positive for hole-dominated conduction, and negative for electron-dominated conduction [79]. In chapter 2, the subband structure of LAO-STO interface was discussed to have more than one subband, so a Hall signal based on more than one band would not be a very surprising result. For two types of carriers, the relation is already much more complex [86]:

$$\frac{dV_H}{dB} = \pm\frac{I}{e}\frac{n_1\mu_1^2 + n_2\mu_2^2 + (\mu_1\mu_2 B)^2(n_1 + n_2)}{(n_1\mu_1 + n_2\mu_2)^2 + (\mu_1\mu_2 B)^2(n_1 + n_2)^2}.$$

This is a nonlinear relation that assumes the form of the one-carrier-type equation if $\mu_1 = \mu_2$. In the measured field ranges presented in this section, we always observed a linear dependence between the Hall voltage and the magnetic field. This means that, although several (sub)bands may contribute to the transport, we cannot distinguish between them based on our data. Therefore, in the case of multi-band conductivity, we measure an average mobility over the contributing bands. This measured mobility is determined by the Hall effect and the sheet resistance, via $\sigma = n_s e\mu$. The relation between carrier mobility and scattering time is given in Appendix B.

For an accurate measurement of the Hall voltage, we chose voltage taps with short lateral dimensions, to minimize an eventual distortion of the electrochemical potential in the Hall structure due to scattering in the contact region. However, the contact width has a lower bound, which is given by the largest characteristic length scale. We assume to be the mean free path of about 2 μm to be the largest possible characteristic length scale. The contact width should be larger than this at any circumstance, so the lithographic resolution and an eventual constriction by an applied electric field are taken into account. The lithographic resolution for the used structuring method was tested to be of the order of ~1 μm on either side of the contact. Electric field constriction of the contact can occur due to the depletion of carriers in that region, since the field can become focused and stronger locally. Therefore, we chose to use a contact width of 15 μm in the design, as contacts of 10 μm used previously [30] were pinched off easily [31].

In order to avoid probing the Hall voltage at a too low value and, as such, overestimate the carrier density, the voltage contacts should be placed far enough from the current contacts. As a rule of thumb, $L_{I-V} > 4W$ is used. Furthermore, in a top-gated structure, it is favorable to make the gate area as small as possible. The leakage current is proportional to the leakage probability P times the gate area A,

$$J = I/A \propto P \rightarrow I \propto AP,$$

where P is the sum of the probability of all leakage sources, such as defects and tunneling.

The resulting Hall bar sample layout is shown in figure 4.3:

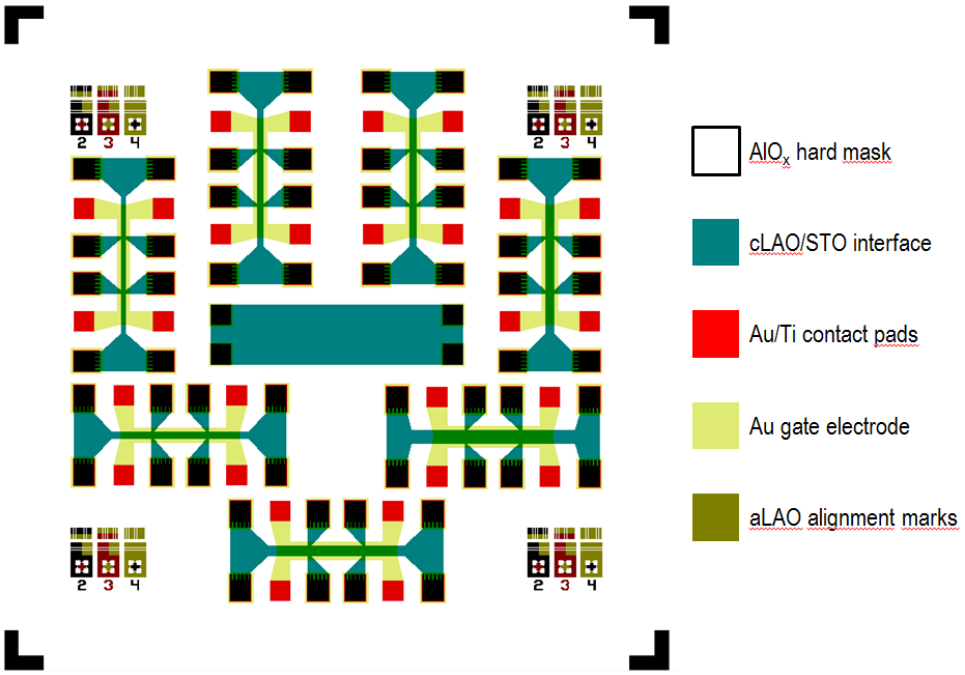

Figure 4.3 The sample design with seven Hall bars of $W = 30 - 100$ µm, $L = 400$ µm. Note the rectangular RHEED window in the middle. The Hall bar has been designed such that the gate area is smallest, current contact resistance is low, voltage contacts are 15 µm wide, the contact line from the metal to the 2DEG is maximized and as many devices as possible fit on one chip.

4.2 TECHNIQUES FOR DEVICE FABRICATION

In this section, techniques for high quality device fabrication are discussed. High quality is defined as solving all the problems listed in the introduction of this chapter, i.e. a reliably insulating hard mask, a high mobility, no contact pinch-off, and low leakage currents. The choice of these techniques is argued and results on quality checks are given, along with some remarks on the techniques and their downsides. The whole fabrication procedure is given in Appendix A.

4.2.1 SUBSTRATES

Substrate quality is a key parameter to create good heterostructures as it forms the ground on which the structure is built. The $SrTiO_3$ substrates used in this work (Crystec 5×5 mm^2, miscut $< 0.1°$ or $< 0.2°$) is single-terminated at the TiO_2 plane of the STO crystal, by removing all SrO from the surface [41]. This process is done as follows. The STO crystal has a mixed termination of SrO and TiO_2 planes. The SrO plane can react with demineralized (DI) water and OH^- adsorbs to SrO. The substrates are sonicated in DI water for 30 min, such that all the SrO on the surface is hydroxylated. Then, the substrate is treated with 87,5% buffered hydrofluoric acid (BHF), these SrO-OH groups will dissolve in the acid and the TiO_2 planes remain.

After etching, the surface is annealed in a tube furnace at 950°C for 1.5 or 2 h to form smooth, TiO_2-terminated terraces. This surface is then inspected using Atomic Force Microscopy (AFM). This should show a well-defined pattern of steps of 0.39 nm height with no contamination. Other techniques, such as X-Ray Diffraction (XRD) or X-Ray Photoelectron Spectroscopy (XPS) can be used for characterization, but these are not applied in this work. The resulting AFM images for different substrate qualities are shown in figure 4.4.

In figure 4.4a), one can see that terraces with a regular step height and terrace width can be prepared. Wider terraces ($d > d_{th} \sim 400$ nm) show holes with one unit cell depth near the step edges, like figure 4.4b). These holes could be removed by further annealing. We did not choose to do so, as further annealing creates jagged step edges as depicted in figure 4.4c). These form because the step edges have a preferred alignment with the crystal axis, which could pose a problem with epitaxial growth. The grown film always has a slight lattice mismatch – 3% for LAO on STO, chapter 2 – and on a scale of tens of nanometers, this can cause irregular growth of the thin film. This is not the case for smooth edges, as the length scale of the crystal axis alignment along these edges is smaller than the length scale at which anomalous growth occurs.

Irregular step edges such as 4.4d) may present a similar problem, since these two or more unit cell steps may have implications for the epitaxial growth of the LAO. By this problem and their height alone, they may become very large scattering centers. On 4.4e) a light superstructure can be observed on the terraces and their height of ~ 0.2 nm indicates non-single-terminated STO. Finally, 4.4f) is the surface of an unannealed substrate after the BHF etch, which shows the importance of this step when one requires a substrate to look like 4.4a) or 4.4b).

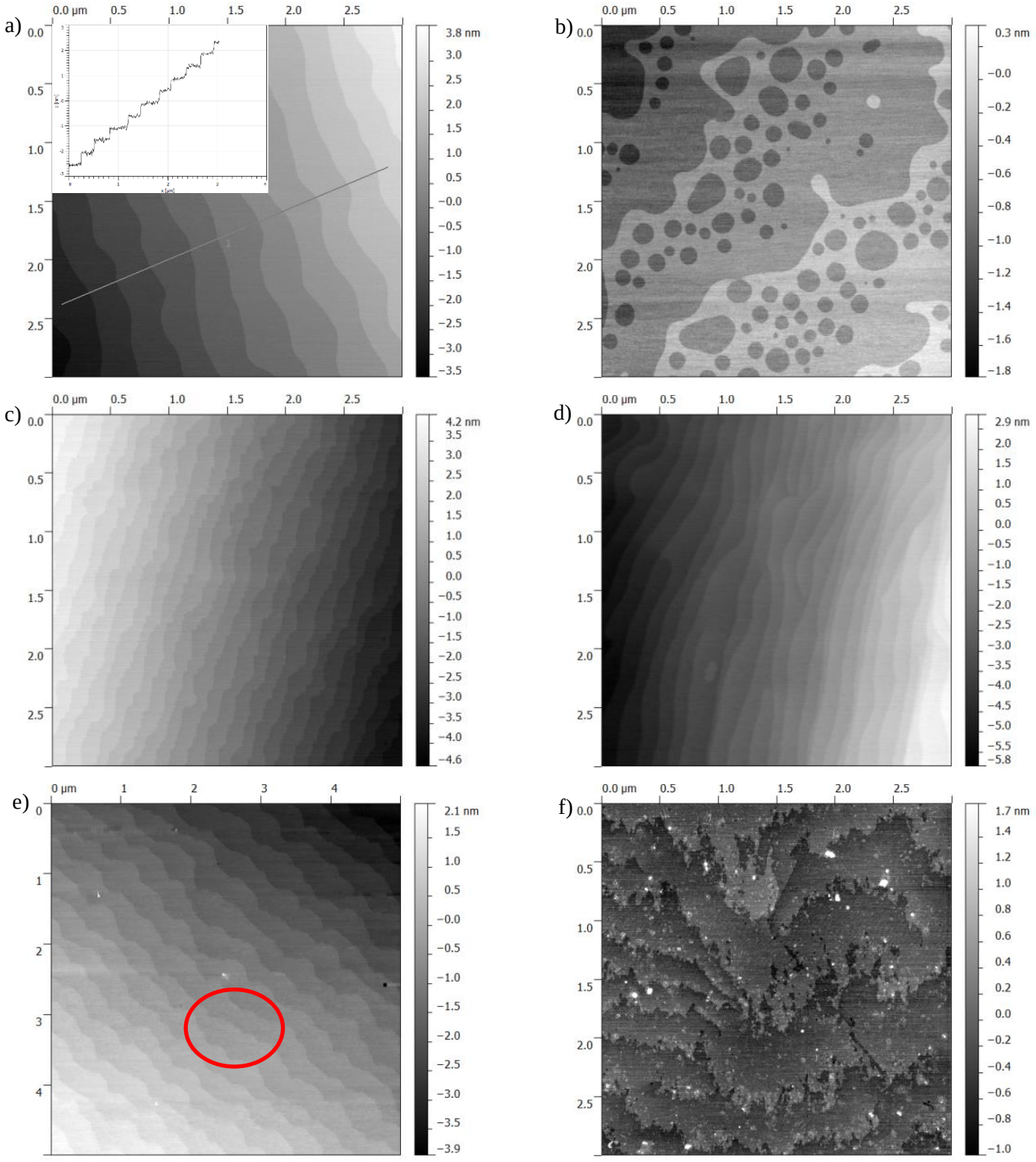

Figure 4.4 AFM images of STO substrates. a) Good substrate with medium-sized terraces. The inset shows the height profile along the line; b) Good substrate with large terraces; c) bad substrate due to irregular steps; d) bad substrate due to mixed termination, in the red circle (hard to see); e) bad substrate due to overannealing, which results in jagged edges; f) (dirty) substrate before annealing.

4.2.2 FILM GROWTH

The LAO film serves two purposes: the creation of the 2DEG and being the gate dielectric for the top gate. As a gate dielectric, the film should be as insulating as possible. Several studies [59,60] have shown an unusual increase in the (tunneling) current across the LAO for a thickness $d > \sim 20$ uc. This effect was originally attributed to Zenger tunneling [59]. More recently, it was suggested that a structural transition causes this increase [60]. In the same studies lower limit was found at ~ 5 uc, which is consistent with the leakage current measurements by Eerkes [30]. There, the leakage current was lowest at ~ 11 uc. We chose the LAO thickness at 10 uc with eventual capping layers of 1 uc SCO and 2 uc STO, to easily compare results to Ref. [32].

The LAO(-SCO-STO) films are grown by Pulsed Laser Deposition (PLD). This is a technique that grossly preserves the stoichiometry of the target material, as compared to sputtering or evaporation techniques. The deposition is fast as compared to e.g. Molecular Beam Epitaxy (MBE) [81]. The principles of PLD are as follows.

The (STO) substrate is placed on a heater stage in a vacuum chamber with a controlled background pressure of deposition gas. This gas is typically oxygen for oxide depositions and typical pressures are 10^{-6} to 10^{-2} mbar [81]. The temperature is controlled by a resistive heater in the sample stage and a thermocouple to measure the temperature. Opposite to the substrate, a target is mounted. To deposit, a Kraft excimer laser ($\lambda = 248\,nm$) on the target in pulses. By each incoming pulse, a plasma plume is formed perpendicular to the target surface, which deposits material onto the substrate at a frequency of ~ 1 Hz, typically.

Layer-by-layer growth of the sample is controlled by Reflection High Energy Electron Diffraction (RHEED). This technique uses the scattering of high energy electrons off the surface of a sample placed in the electron beam to image the growth of a thin film on the sample. The scattering occurs via refraction and reflection, the first of which provides information on the material that is in the top layer of the sample. The reflection intensity is an indication of the smoothness of the surface, which is a measure for the coverage of the upper monolayer of deposited material, as is described below.

On a clean, atomically flat surface, islands of the deposited material form when the deposition starts. This diffuses the reflected electron beam, lowering the intensity of the elastically reflected beam. This process continues until the coverage of the new layer is exactly 0.5 Past this point, the surface roughness decreases and the RHEED intensity increases again, until the layer is finished. This gives rise to oscillations in the intensity, in which each maximum is a completed monolayer of atoms. When RHEED oscillations are monitored during deposition, one can control the thickness of the film to the accuracy of unit cells of the deposited material. Since the LAO-STO system is very dependent on the LAO film thickness, this is a crucial control parameter. In figure 4.5, RHEED oscillations are depicted of the growth of LAO, SCO and STO of a sample used for the research in this thesis. More RHEED results growth are discussed in Appendix A.

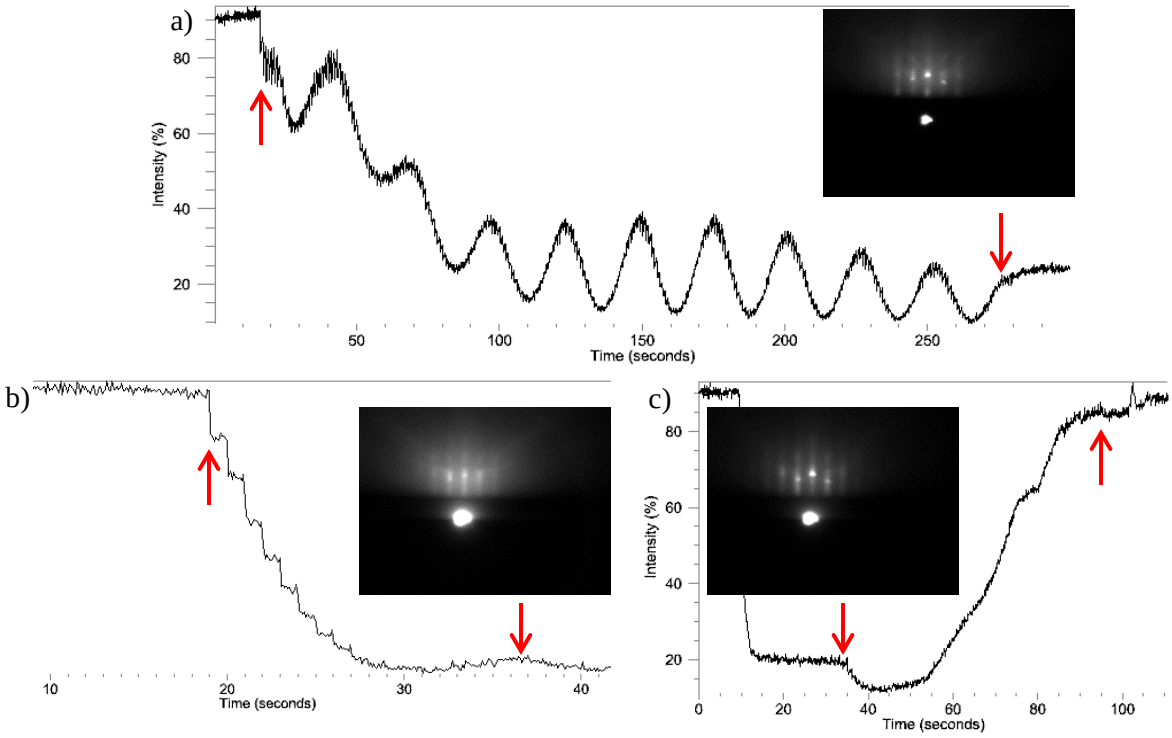

Figure 4.5 RHEED oscillations during the deposition of 20140819-3; a) LAO, b) SCO, c) STO. The insets show the RHEED images after the deposition. The red arrows mark the begin and end of the deposition. In (c), the increase of intensity around $t = 80$ s is due to an external source.

The growth parameters for the LAO(-SCO-STO) films [30,32] are summarized in table 4.1.

	Normal	Capped sample		
Parameter	LAO	LAO	SCO	STO
p_{O2} (mbar)	$1.7\ 10^{-3}$	$4.0\ 10^{-5}$	$6.0\ 10^{-2}$	$6.0\ 10^{-2}$
T (°C)	850	850	600	600
Fluence (J cm^{-2})	1.3	1.3	1.3	1.3
Frequency (Hz)	1	1	1	1
Spot size (mm^2)	1.5	1.76	1.76	1.76
Mask type (mm^2)	55.9	2×15	2×15	2×15
Pulses per unit cell	17	18	14	17

Table 4.1 Deposition conditions for the epitaxial LAO and LAO-SCO-STO layers.

4.2.3 Structuring the LAO-STO 2DEG

The most common techniques to fabricate a micrometer- or nanometer-sized structure on a thin film are ion etching and lift-off. These are done after performing a lithographic masking or writing technique on a light or electron-beam sensitive layer, called photoresist or e-beam resist, respectively. Ion etching is unsuitable for STO(100) substrates, since the ion etching technique locally dopes the substrate, which becomes highly conducting as a result [82]. Lift-off lithography avoids using ion etching, but resists are organic and burn at deposition temperatures.

Nevertheless, numerous methods have been reported to structure the LAO-STO 2DEG [83,84]. The basic working principle is the use of an oxide masking layer, also called a hard mask, that is deposited at room temperature and does not burn when heated to LAO deposition temperatures. Since it is deposited at room temperature, organic resist can be used to pattern the hard mask using a lift-off patterning technique.

For LAO-STO interfaces, it was found that mobility is suppressed when using a lift-off technique on the STO surface [30] in comparison to unpatterned thin films. A reason for this might be that some burnt-up photoresist residue remains on the surface, destroying conductivity locally and reducing global mobility. Also, the amorphous LAO used as a masking layer turned conducting for most samples grown according to the recipe presented by Eerkes [30,31].

Both these problems are avoided by using an AlO_x masking layer, where the subscript x denotes the possible off-stoichiometry of the crystalline Al_2O_3 target. This layer can be chemically etched away during patterning, as presented by Banerjee *et al.* [83]. Using this method, the photoresist does not touch the STO surface and therefore, cannot leave residue to locally suppress mobility. However, if the etching is done too short, there will be AlO_x residue that has the same effect on conductivity as photoresist residue.

Furthermore, the AlOx layer proved to be highly insulating for all samples that were used. In the work by Banerjee *et al.* [83], the hard mask is eventually etched away by applying sodium hydroxide (NaOH). This would expose the 2DEG to the top electrode, shorting it and making it unsuitable for gating. In this work, this step is skipped in order to keep the 2DEG spatially isolated from the top electrode.

In order to determine the quality of the Hall bars and the lithographic resolution of the etch step, AFM was done on a sample that had been processed up to the etching step. This is depicted in figure 4.6. Figure 4.6a) shows the surface of a Hall bar that has been patterned with photoresist, after which it was lifted off in acetone and cleaned in acetone and ethanol. The STO steps are barely visible, aligned from the top left to the bottom right corner. The zoom of figure 4.6b) shows that the residue on the surface is organic, from the web-like surface structure. This leads to the hypothesis that this is photoresist residue on the STO.

This residue was not seen when AlO_x etching was done. However, surface adsorbents (or AlO_x residue) were visible, as depicted in figure 4.6c). We investigated the origin of the claim by Banerjee *et al.* [83] that the Hall bars patterned this way have similar mobility to unstructured films. For this, the sample was put in the PLD system and exposed to deposition conditions. After this, the adsorbents were gone and the sample showed rough terraces of 0.39 nm thickness, as is depicted in figure 4.6d). However, small pits can be observed on this sample, which might become additional scattering centers at the interface. After depositing the epitaxial LAO-SCO/STO film, the surface steps can be resolved clearly, the surface is nearly clean and the edge between the Hall bar and the AlO_x film is sharp, as depicted in figure 4.6e). A zoom on the Hall bar surface (fig. 4.6f)) shows the excellent steps that are still visible, with a step height of $\sim 0.4 \pm 0.04$ nm, which corresponds to the unit cell reported by Huijben *et al.* [32]. The image is blurry after growth due to strain relaxation of the film, as was also observed by Ref. [84].

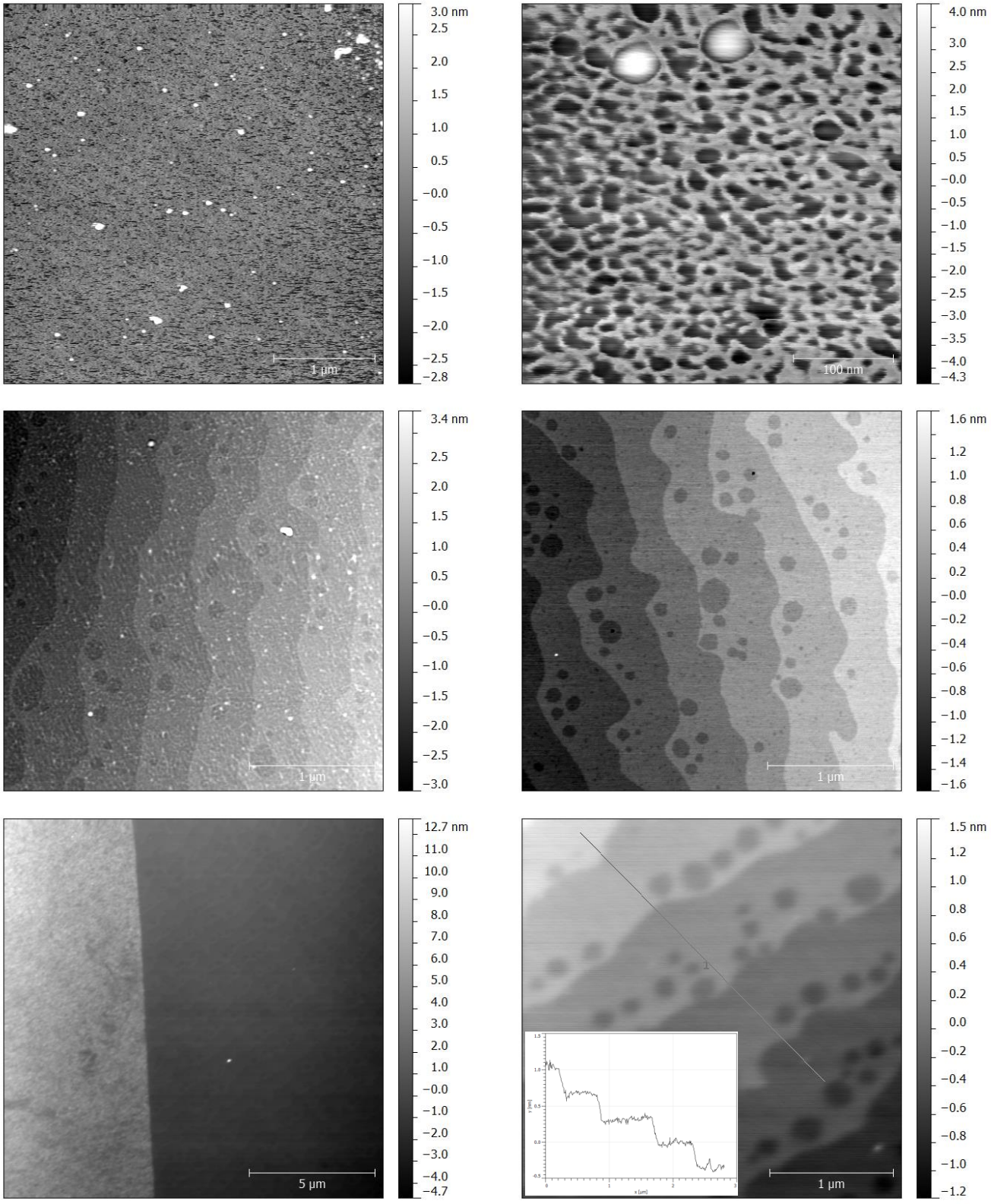

Figure 4.6 AFM images of Hall bar areas after patterning. a) 'Bare' STO after lift-off of AlO_x deposition: steps barely visible (angle ~60°); b) Zoom of image (a), showing an organic network; c) Sample 20140523-1 after AlO_x etch; d) Sample 20140523-1 after deposition conditions; e) Hall bar edge of sample 20141003-2 after LAO-SCO-STO deposition; f) zoom of e) on the Hall bar area. The height profile along the line is shown in the inset.

4.2.4 GROWTH OF AU GATE ELECTRODE AND KI ETCHING

In this work, RF sputtering of Au was used for depositing the top gate, similar to Ref. [24,85]. The RF sputtering was done in a Perkin Elmer model 6300 and was done very gently, to decrease the energy of the incoming Au atoms, thus preserving the quality of the dielectric layer. Atoms with higher energy have a higher probability to pierce through and reduce gate performance. The parameters for the gentle sputtering are presented below. This resulted in a reproducible Au film that is greenish transparent in color after $t = 34$ min, and has a thickness of ~ 60 nm.

Parameter	Value
Table spacing (inch)	2.2
p_{Ar} (mbar)	$8.2\ 10^{-2}$
$P_{rf}(W)$	N/A
$U_{target}(V)$	-200
Deposition rate	~ 1 nm min^{-1}

Table 4.2 Sputtering parameters for Au gate electrode

After sputtering, the gate electrodes were patterned via standard UV-lithography (Appendix A). After patterning, the gold that does not belong to the gate or the contacts was etched away by a buffered potassium iodide (KI) solution, a solution that dissolves gold. The solution was prepared with mass ratio 2g KI, 1g I_2 and 40 mL H_2O. This solution was further diluted 1:10 with H_2O and heated to about 50°C on a hot plate before etching. The sample was etched for 20 s in this solution and washed twice in DI water for 30 s. The sample was blow-dried with nitrogen and checked for quality. Then, the photoresist was removed by soaking in acetone and ethanol.

In the first mask design, the contacts were not protected during the etching step, which made them etch away as well. Since the exact solution and etching temperature are not optimally controlled, it is very advisable to protect any gold that is on the sample during etching by a protective photoresist layer.

4.3 FABRICATION SUMMARY

Below, we summarize the improvements to sample fabrication made during this work.

- AlO_x is a better insulator than the amorphous LAO used in previous research [30], because it showed a negligible leakage current, if any, for all samples in this work;
- The use of the very gentle gate deposition has led to very low leakage currents, as will be shown in chapter 6;
- The use of a KI etching technique rather than lift-off protects the top surface during processing. Previously, it was less protected against adsorbents and aggressive chemicals. This adjustment should make the process more reproducibly;
- With the new mask design, the contact pinch-off was not observed for any sample;
- The mobility of top-gated devices was increased by an order of magnitude: $\mu \sim 2000$ cm^{2}V^{-1}s^{-1} (chapter 6) as compared to $\mu \sim 300$ cm^{2}V^{-1}s^{-1} [30].

So, on all points mentioned in the introduction of the chapter, significant improvement was established. However, the highest reported mobility values [32] are still an order of magnitude higher than the value stated above. The origin is elusive. It might be in the processing method, still, for instance the small pits in figure 4.6d). Also, the epitaxially grown sample in the Van der Pauw configuration had a mobility of only $\sim 4{,}000\ \mathrm{cm^2V^{-1}s^{-1}}$, which is still somewhat lower than the systematically reached values of $6{,}000\ \mathrm{cm^2V^{-1}s^{-1}}$ by Huijben *et al.* [32].

The above considerations on fabrication aspects has led to a fabrication procedure that is described extensively in Appendix A. It is summarized below:

1. TiO_2-terminated $SrTiO_3$ substrate preparation by buffered HF etch and surface annealing;
2. Atomic force microscopy to check substrate quality;
3. Amorphous AlO_x deposition;
4. Patterning of alignment mark geometry
5. Amorphous LAO deposition;
6. Lift-off of photoresist in acetone and ethanol;
7. Patterning of Hall bar geometries;
8. Wet etching on AlO_x layer;
9. Deposition of crystalline $LaAlO_3$ (and $SrCuO_2$/$SrTiO_3$ capping layer);
10. Deposition of gate Au;
11. Patterning of Au/Ti contact geometries;
12. Ar ion milling Au/Ti contact geometries;
13. Deposition of Ti and Au as contact metal to the 2DEG;
14. Lift-off of photoresist in acetone and ethanol;
15. Patterning of gate electrodes;
16. Etching of excess gate Au by a KI solution;

This order of steps is chosen such that sensitive surfaces are covered by materials that are easily removed throughout the entire process. In step 3, the STO is covered until LAO deposition in step 9, after which the Au electrode is directly deposited to protect the LAO surface.

4.3.1 FUTURE WORK

In terms of masking layer insulation and gate characteristics, the fabrication procedure was optimized and we foresee no direct improvements that could be made, let alone that they would be needed to use the techniques for studying LAO-STO heterostructures.

The large variations in mobility – that is also systematically lower than expected – leave room for improvement. The somewhat rougher surface of the STO after removal of AlO_x suggest a systematic study on depositing the AlO_x layer with different deposition parameters, aiming for a deposition that is as gentle as possible. In addition, a systematic study of the growth of the LAO-SCO-STO stack in this PLD system has to be conducted to optimize mobility in light of the long-term goal of attaining ballistic transport. This study should include an in-depth analysis of substrate quality. It is also interesting to study different cuprate interlayers to determine whether these also enhance the oxygen diffusion into the sample and improve the material even more.

5. TRANSPORT EXPERIMENTS ON STRUCTURED LAO-STO DEVICES

In this chapter, we present and discuss the results of transport experiments on several LAO-STO samples. Unless stated otherwise, all measurements were performed on SCO-STO samples with layer thicknesses of 10/1/2 unit cells of LAO-SCO-STO, as introduced in Ref. [32].

5.1 EXPERIMENTAL DETAILS

The measurements were conducted in two measurement setups. The top-gate measurements were done in a Quantum Design model 6000 Transport Physical Property Measurement System (PPMS) with the built-in resistance bridge. This system is not designed for voltages in excess of 20 V, thus, so for the required high back gate voltages of up to 200 V [20], back-gated measurements were done in a bath cryostat setup with high-voltage wiring.

Sheet resistance and sheet carrier density were measured either in Van-der-Pauw configuration (unpatterned films; for a discussion of the Van-der-Pauw method see chapter 4) or in Hall bar geometry (structured devices). Here, an AC excitation current (500 nA – 1 μA) was injected along the longitudinal direction of the Hall bar device (see figure 5.1). The longitudinal resistance was measured between two voltage probes along the direction of the current flow. The carrier density was determined by a measurement of the Hall effect in a magnetic field, as described in chapter 4.

Gating was done by Keithley Source Measure Units (SMUs) in both, the PPMS and the bath cryostat setup. Top-gating was done by a Keithley model 2401 SMU which can source up to 21 V and measure leakage currents down to 0.1 nA and back-gating was done by a Keithley model 2400 SMU which can source up to 210V. Low-pass filters were used to remove high-frequency noise, and to avoid abrupt changes in the applied voltage.

Connections to the sample were made by Al wires using a wedge wire bonder. The Van der Pauw measurements were wired according to figure 4.1b) and the top-gated Hall bars were wired according to the wiring diagram presented in figure 5.1.

The transport measurements in the PPMS Transport were done by using the built-in resistance bridge electronics. It can measure four current-voltage channels simultaneously, with twelve connections down into the cryostat. Each Hall bar requires six connections by figure 5.1 to measure, and one to gate. The PPMS can accurately control the temperature from room temperature down to 2K and the magnetic field up to 9T. In most measurements, the magnetic field was swept to 4T.

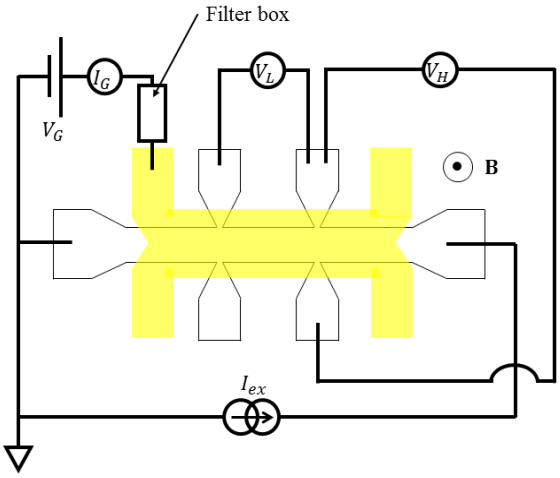

Figure 5.1 Hall bar wiring diagram. The characteristics of the filter box are: $R = 100$ kΩ; $C = 2.2$ μF; $V_{max} = 250$V. Crossing lines are not connected to each other. In the bath cryostat setup, I_{ex} was generated by an AC voltage dropping over a large resistance before entering the sample.

The transport measurements in the bath cryostat were done by sourcing an AC voltage by a SR830 lock-in amplifier, which drops over a large resistance (1 MΩ) to transform into a current. This current is assumed constant in measurement, as the resistance in the sample is of the order of 1 kΩ, A lock-in amplifier sends out an AC voltage at a user-set frequency and can pick up a voltage of the same frequency. This measurement rejects noise at other frequencies other than the measurement frequency, as well as any DC drift picked up in the measurement setup, and is thus superior to e.g. a DC voltage measurement.

The bath cryostat was not equipped with a built-in (superconducting) magnet. To do the Hall measurement, a manually-wound coil was mounted next to the sample and a large (10A) current was applied to drive a magnetic field of 300 mT, which was user-calibrated. The Hall voltage was then measured at $B = 0$ T and $B = 300$mT, to determine the slope $dV_H/dB(0)$ of the Hall voltage with respect to the magnetic field, thus cancelling any offset in the Hall signal due to inhomogeneities in the sample.

5.2 Fermi level pinning by the Au top electrode

As discussed in section 3.3, applying a top electrode and connecting it to the 2DEG pins the Fermi levels of the 2DEG and the electrode for zero gate voltage. This can influence the carrier density, which can be measured with a Hall measurement.

Our first observation is that the sheet carrier density (as measured by the Hall effect before and after patterning the top-gate) increases when the LAO comes into contact with the metallic electrode. This is shown in figure 5.2.

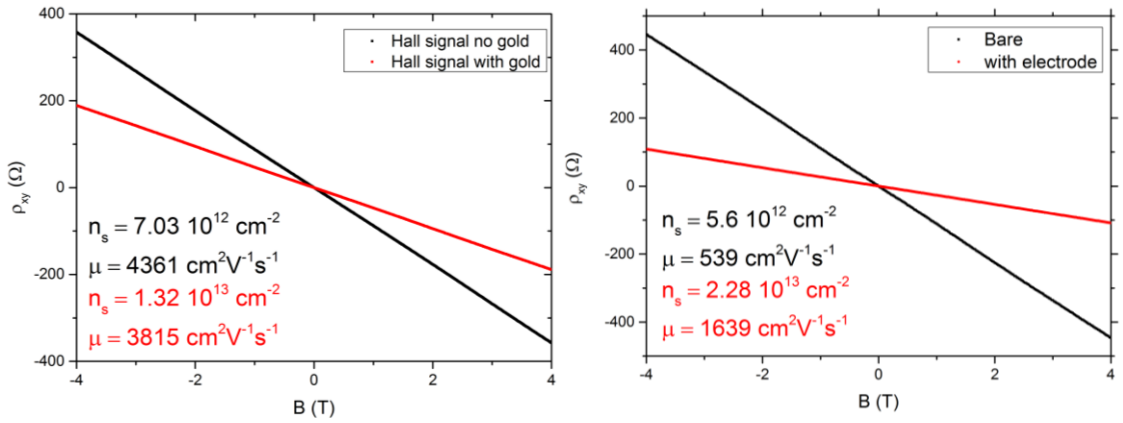

Figure 5.2 Hall signals of samples before and after gate electrode deposition at $T = 2$K; a) Van der Pauw measurement on sample 20140819-4; b) Hall bar measurement on sample 20140819-3.

The Van-der-Pauw measurement in figure 5.2a) was first measured directly after the LAO-SCO-STO deposition, after which the gate electrode deposition was done by sputter deposition. The corners of the sample were protected by photoresist drops during the deposition, after which a lift-off step exposed the corners again for contacting the 2DEG. The Au top layer was connected by wire bonding on a dried drop of silver paint on the middle of the gate electrode.

In a similar fashion, The Hall bar in figure 5.2b) was measured before and after patterning the top-gate electrode. Here, we patterned the gate electrode using the lift-off technique instead of defining the pattern subtractively by KI etching.

The gate leakage was measured to be negligible for the Hall bar sample. A systematic leakage test was not conducted for the Van der Pauw measurement, but we can rule out a large shunt through the Au layer as the measured gate resistance was ~ 1 MΩ and the sheet resistance of the LAO-STO was ~ 100 Ω.

The Hall signals before and after the deposition are significantly different. For the Van der Pauw measurement, the calculated carrier density was almost twice as high as before. For the structured sample, the carrier density increased fourfold. The mobility of the Van der Pauw sample was slightly lower after the deposition. The mobility of the Hall bar sample was higher after depositing the gold layer, because a resistance upturn – see section 5.3 – was not observed after depositing it.

The magnitude of the increase in carrier density can be estimated using the simple model of Fermi level pinning of the 2DEG and the top gate, discussed in section 3.2. For an Au top gate, we predict a carrier density increase of $\Delta n_s \sim 10^{13}$ cm^{-2}. This is the case in both measurements, as $\Delta n_{s,1} = +0.6 \cdot 10^{13}$cm^{-2} and $\Delta n_{s,2} = +1.6 \cdot 10^{13}$cm^{-2}.

The difference in Δn_s calls for a more detailed analysis. Such an analysis must include the effects of strain (relaxation), changes in the dielectric properties, surface adsorbents, exposure to process chemicals, mechanical stress during deposition etc. We did not perform such an analysis.

5.3 TEMPERATURE DEPENDENCE OF TRANSPORT PROPERTIES

The sheet resistance, carrier density and mobility of Hall bar devices as function of temperature have been measured. These quantities as a function of temperature are related to scattering mechanisms in the material and can be used to compare these samples with previously characterized samples.

5.3.1 CARRIER DENSITY AND MOBILITY

The absence of thermally activated carriers, as expected for SCO-STO capped samples [32], is validated from measurements of the Hall signal at different temperatures. With these carrier densities and the sheet resistance, one can determine the carrier mobility according to the formulas in Appendix B. This measurement is done for all samples during cooldown to 2K. The results of the first measured SCO-STO capped sample with gate electrode are presented below.

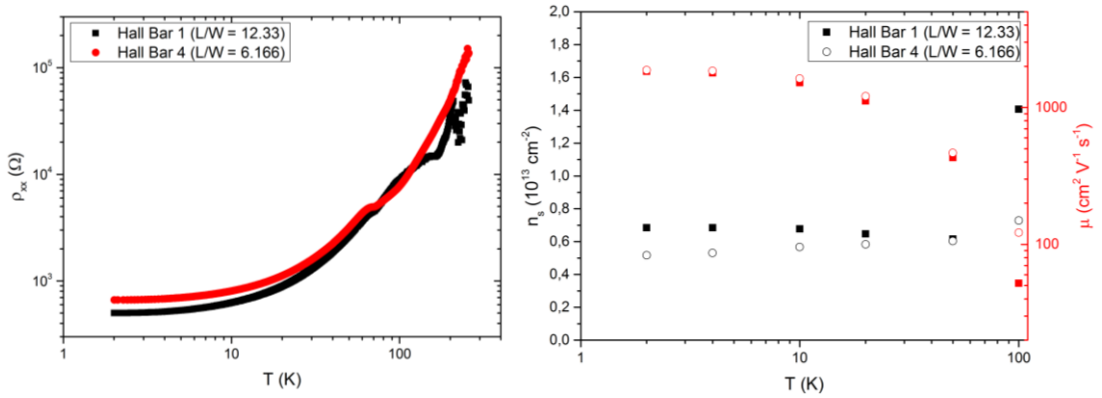

Figure 5.3 a) sheet resistance, b) carrier density and mobility versus temperature for sample 20140611-2.

This measurement shows that the carrier density as a function of temperature is approximately constant, a strong indication that the enhanced oxygen diffusion mechanism holds in this sample. The mobility of $\sim 2{,}000\ \mathrm{cm^2V^{-1}s^{-1}}$ at $T = 2\mathrm{K}$ was lower the value for the unstructured film of figure 5.2a).

The contacts of this sample were severely damaged during the gate KI etching step, which made it impossible to gate this sample in a follow-up measurement. The kink in the sheet resistance around $T = 70\mathrm{K}$ is consistent with a reported structural transition in STO [87].

5.3.2 ANOMALOUS (MAGNETO)RESISTANCE AT LOW TEMPERATURES

Most samples displayed metallic sheet resistance dependence on the temperature, as is depicted in figure 5.3a). However, when the Hall bar sample of figure 5.2b) was tested to investigate the carrier density before and after applying the Au gate electrode, it displayed a resistance upturn below 20K. This behavior disappeared after the gate electrode was added. The measurements of the sheet resistance, carrier density and mobility are given in figure 5.4.

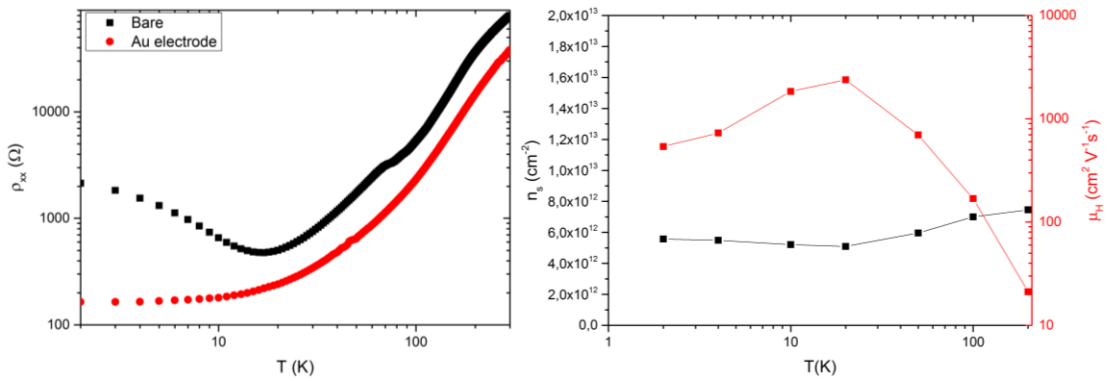

Figure 5.4 Anomalous behavior as a function of temperature; a) Sheet resistance for Hall bar 1 on 20140819-3, b) derived carrier density and mobility for the bare Hall bar.

The sheet resistance of the black line at $T = 2$ K is 3 times higher than the resistance at 20 K, which is reflected in the mobility in figure 5.4b). The carrier density as calculated from the Hall signals was approximately constant in temperature. The Hall signals were linear in field up to 4T. The mobility of the bar Hall bar changes from $\sim 2600\ \mathrm{cm^2 V^{-1} s^{-1}}$ at 20K to $\sim 500\ \mathrm{cm^2 V^{-1} s^{-1}}$ at 2K. The value at 20K goes up by a factor of ~ 1.5 at 2K for other samples, so the measured mobility at $T = 2$K is an order of magnitude lower than expected ($\sim 4000\ \mathrm{cm^2 V^{-1} s^{-1}}$).

Another phenomenon was observed during this measurement: a large, positive, temperature-dependent magnetoresistance that occurred only in the bare Hall bar of figure 5.4a). The temperature-dependent magnetoresistance before and after the gate electrode deposition is shown in figure 5.5.

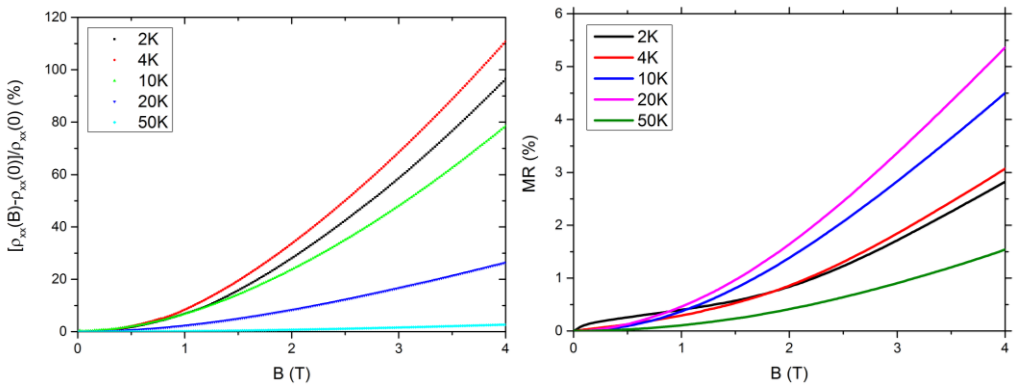

Figure 5.5 Magnetoresistance as function of temperature in sample 20140819-3 after symmetrization; a) Large magnetoresistance of up to 100% at 4T in a bare Hall bar; b) Strongly reduced magnetoresistance after applying an Au top layer.

All magnetoresistance curves in figure 5.5 are positive and, except for the 2K curve of the sample with gate electrode, almost parabolic. The curve at $T = 2$K of figure 5.6b) shows a slight resistance dip around $B = 0$ and is almost parabolic for higher fields. As function of temperature, the curves vary in both figures. For the bare Hall bar, the magnetoresistance increases strongly for decreasing temperature, except for the curve at $T = 2$K, which is slightly below the 4K-curve.

The interpretation of this data is unclear. The resistance upturn has close resemblance to an upturn due to the Kondo effect [88], with the Kondo temperature T_K below 2K. However, the Kondo effect would imply a negative magnetoresistance as has been observed in magnetic samples [12]. This is clearly not the case in this sample, so the Kondo may be ruled out as the origin of the resistance upturn.

The large magnetoresistance values as in figure 5.5a) cannot be explained by localization effects, where the magnetoresistance values are typically a few percent at maximum [89]. A scenario that would fit the large magnetoresistance curve is the magnetoresistance of a 2D system with spin-momentum locking, e.g. a topological insulator [73]. In a topological insulator, backscattering of surface states is forbidden as the spin of a forward moving state is orthogonal to the spin of a backwards moving state. Therefore, their inner product is zero, which makes the scattering probability from one to the other zero. This changes in an out-of-plane magnetic field, in which the spins are tilted out-of-plane. This out-of-plane tilt lifts the orthogonality of the backward and forward states and there is a possibility to scatter into one another, that depends on the out-of-plane angle. For higher fields, the angle increases, which enhances the backscattering probability. The typical resistance increase in this scenario is of the order of the sheet resistance.

So, if one of the bands of the 2DEG possesses strong spin-momentum locking, this could explain this magnetoresistance. This spin-orbit locking should then originate from Rashba spin-orbit coupling [90], which has been measured in LAO-STO [20,30] and is thought to originate from the strong confinement potential and the lack of surface inversion symmetry at the interface [66,67].

The resistance upturn, however, is not explained by this suppression of backscattering scenario. On the contrary: this scenario implies a lower resistance at $B = 0$. Thus, a complete explanation for these curves cannot (yet) be given based on the concept described above.

In summary, the shape of the upturn and the large magnetoresistance point suggest an anomalous spin-scattering effect. Unfortunately, these effects were removed from the sample as the Au top layer was applied and these effects could not be studied in more detail. An interesting challenge for future research is to reproduce these results, either by growth or by gating the interface into this regime by changing the carrier density. The latter would show this anomaly to be a reversibly tunable effect, which would be interesting in the light of possible applications.

5.4 TOP-GATING

Several top-gated, structured samples of SCO-STO capped LAO-STO devices have been fabricated, following the design presented in section 4.1 and the procedure discussed in Chapter 4 and Appendix A. In the following, the characterization of these samples is discussed.

5.4.1 GATE LEAKAGE

The gate leakage is an important parameter for device performance. A leakage current indicates an alternative conducting path, which may complicate the interpretation of a given physical effect and may be undesirable in device applications. We present data on the gate leakage of two samples: a sample of which the gate was defined by lift-off and a sample of which the gate was processed with KI etching.

The lift-off sample had a leakage profile comparable to earlier results [25]:

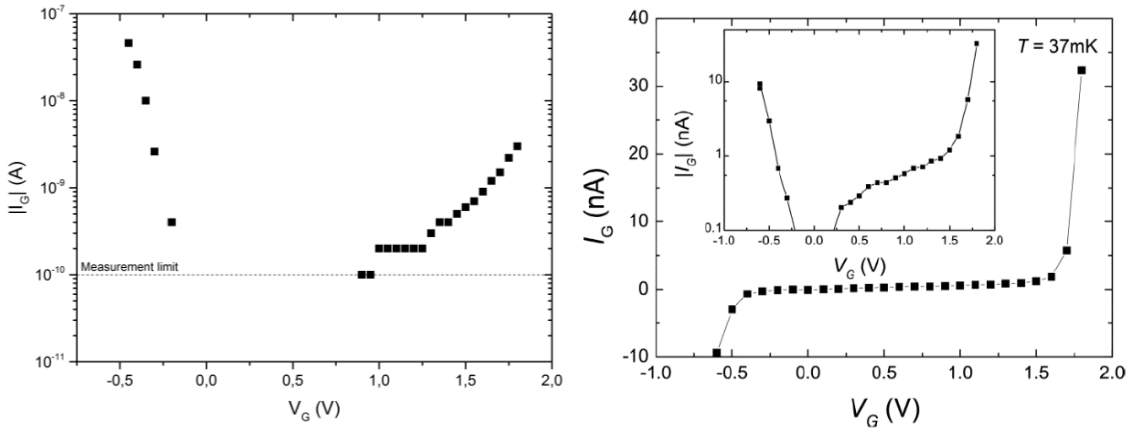

Figure 5.6 gate leakage of top-gated LAO-STO samples. a) absolute value of gate current for lift-off sample 20140819-3 at $T = 2$K; b) Leakage current taken from Ref. [25], at $T = 37$ mK.

The leakage currents in figure 5.6a) are reversible and show nonlinear dependence of the gate current on the gate voltage, very similar to the inset of figure 5.6b). The leakage of the sample that was made with the KI etching was below the measurement limit of 0.1 nA for all gate voltages between -0.6V and $+1.7$ V.

A positive gate voltage of 1.7V means there is an electric field of ~ 340 MV/m across the LAO-SCO-STO layer, as it is ~ 5 nm thick [32]. This electric field strength is of the order of the breakdown field, which can be deduced from figure 5.6b), where the leakage current increases rapidly above 1.7V. Dielectric breakdown destroys the dielectric material, so the measurement was stopped at 1.7 V to preserve the sample for future measurements. Further tests can show the breakdown field in this material stack to explore the experimental boundaries that can be reached in these samples.

The gate leakage can be calculated as a current density to compare performance to literature. The gate area in the measurement of figure 5.6a) was $55{,}000$ μm^2, so $I = 0.1$ nA corresponds to $J \sim 0.2$ μA cm^{-2}. In table 5.1, we compare this data to literature reports on leakage currents [24,25,60(SI),91]. We first state that samples with epitaxially grown oxide electrodes show orders of magnitude higher leakage than those with metal electrodes [22,23]. Förg *et al.* even reported leakage currents up to 150 nA, and they measured down to only -400 mV. Therefore, we have only included samples with metal top electrodes in the table below. The gate current and gate current density are given for gate voltages of -0.2 V and $+0.5$ V, respectively.

Reference	d_{LAO} (uc)	T (K)	Gate area (μm^2)	Gate current (nA)	Current density ($\mu A\ cm^{-2}$)
KI etching (this work)	$10/1/2$	2	$\sim 45{,}000$	$< 0.1, < 0.1$	< 0.2
Lift-off (this work)	$10/1/2$	2	$\sim 55{,}000$	$\sim 0.4, < 0.1$	$\sim 0.8, < 0.2$
Singh-Bhalla *et al.*	14	100	$\sim 32{,}000$	$\sim 3.2, \sim 200$	$\sim 1, \sim 65$
Eerkes *et al.*	12	0.037	$\sim 5{,}000$	$< 0.1, \sim 0.3$	$< 2, \sim 6$
Hosoda *et al.*	9	300 2	$\sim 5{,}000$	$\sim 0.01, \sim 0.01$ $< 0.01, < 0.01$	~ 0.2 < 0.2
Jany *et al.*	5/8 (BTO)	300	$\sim 3{,}000$	$\sim 10, \sim 0.5$	$\sim 30, \sim 1.6$

Table 5.1 Gate performance of the devices in this work and devices from literature. Literature values taken from Refs. [24,25,60(SI),90].

This table shows that the leakage current of the lift-off device comparable to references such as Ref. [25], but with an order of magnitude larger gate area. Our KI etched sample has the lowest leakage currents reported to date for such large gate areas and its current density is comparable to the best values in literature, reported by Hosoda *et al.* [24].

The leakage data from figure 5.6 can be interpreted as a reversed Schottky diode [92], as the positive voltage is on the metal side of the metal-semiconductor junction. From extensive research on gate leakage currents, the Schottky barrier (section 3.3) between the LAO and the top gate electrode may be determined.

5.4.2 TUNING OF CONDUCTING PROPERTIES

The main purpose of a gated device is to (reversibly) tune the conducting properties of the conductor underneath. The sheet resistance of two different SCO-STO capped samples were tuned by an applied top gate voltage to the Au top layer, as is presented below.

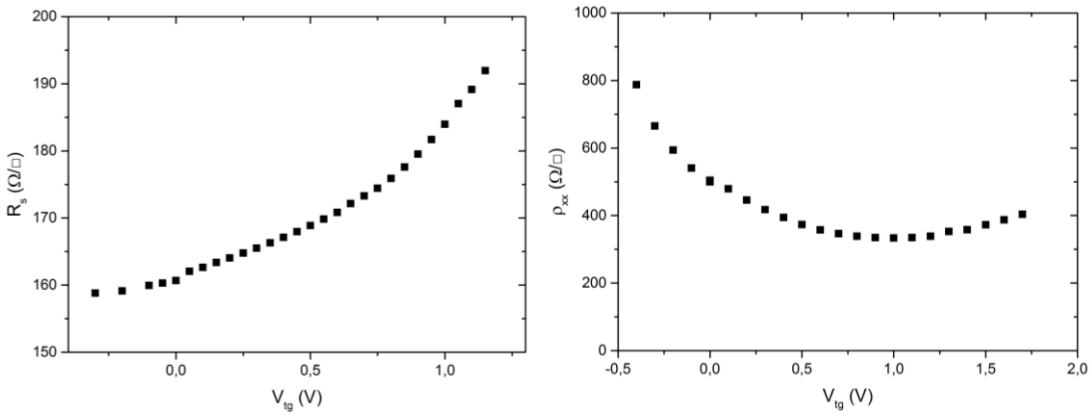

Figure 5.7 Sheet resistances versus gate voltage. a) sample 20140819-3; b) sample 20141010-3.

The sheet resistance is shown to be gate tunable in the same order of magnitude for both samples. The difference in shape will be explained below. From this sheet resistance data and the corresponding Hall signals – that were perfectly linear up to $B = 4\text{T}$ for all gate voltages in both samples – one can extract a carrier density and Hall mobility as function of gate voltage, as is done in figure 5.8.

From these graphs, one immediately sees that a positive gate voltage induces more carriers in the system, as expected from a reasoning based on capacitance. The mobility is reduced as the gate voltage increases, which is in line with earlier measurements of top-gated LAO-STO devices [24,30]. As presented in figure 5.8c) and d), the mobility has a negative, linear dependence on the carrier density.

In the right two figures, there is a discontinuity at $V_G = 0\text{V}$. This can be ascribed to the fact that the gate was swept to (very high) gate voltages, before the values for the negative gate voltages were probed. This shows that the electrostatic tuning is not completely reversible, at least not for very high gate voltages. The red marked data points in figure 5.8d) are the values taken at negative gate voltages.

At a first glance, the carrier density and mobility dependence on the gate voltage look different for both samples. But, as was discussed in chapter 3, the gate voltage actually induces a difference in carrier density from the equilibrium value. This equilibrium carrier density is different for both samples and if one looks at the curve between $n_s = 21 \cdot 10^{12}\text{cm}^{-2}$ and $n_s = 28 \cdot 10^{12}\text{cm}^{-2}$, the shape is similar. The same holds for the mobility in this region, as is seen from the very similar graphs in figure 5.8c) and d). This offset in equilibrium value also explains the difference in shape of the sheet resistance graphs, figure 5.7a) and b).

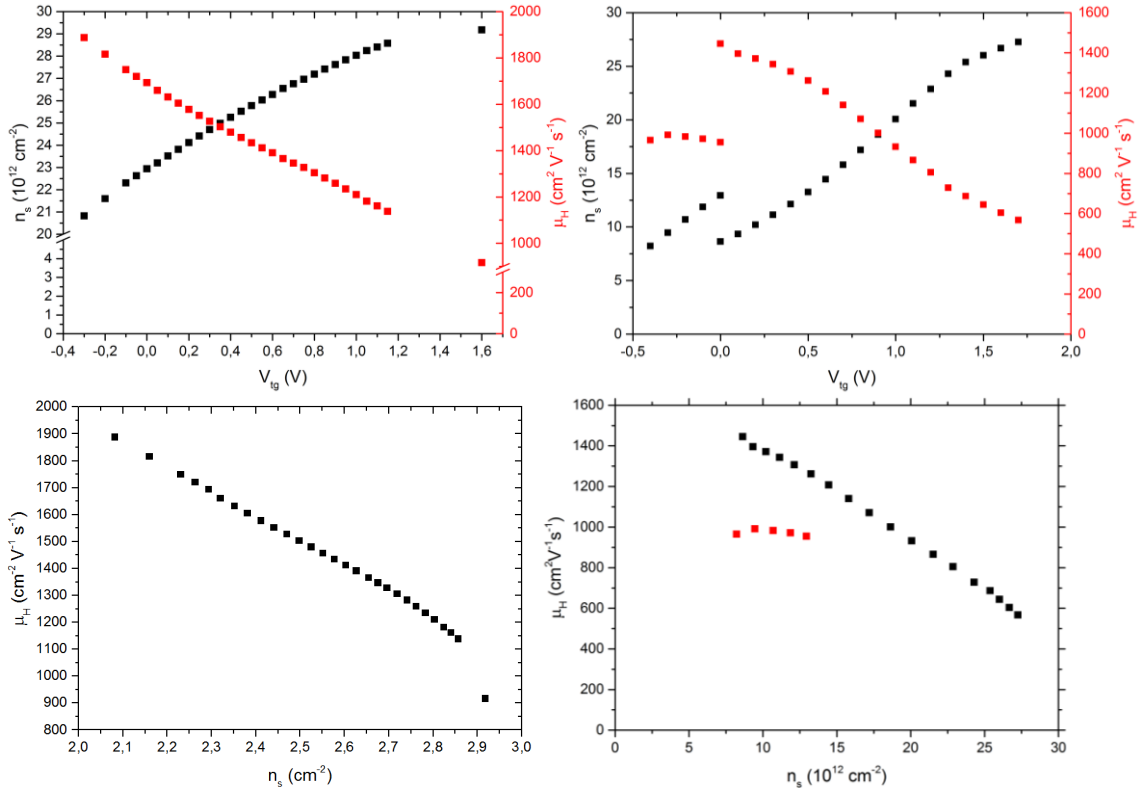

Figure 5.8 Carrier density and mobility tuning by top-gating; a) tuning of sample 20140819-3, gated to negative values first and then to positive values; b) tuning of sample 20141010-3, which was gated positively before going to negative values; c) extracted mobility versus carrier density of sample 20140819-3; d) extracted mobility versus carrier density of sample 20141010-3.

The tunability of the carrier density and especially that of the mobility presented above is large for a top-gated sample. This can be seen in table 5.2, an overview of mobility and carrier density tuning in literature [20,21,24,30,61,93].

Reference	Gate type	d_{LAO} (u. c.)	T_{dep} (°C)	μ ($\mathrm{cm^2V^{-1}s^{-1}}$)	n_s ($10^{12}\mathrm{cm^{-2}}$)
This work	Top	$10/1/2$	$850/600$	$500-1900$	$8-30$
Eerkes *et al.*	Top	12	850	$215-230$	$16-22$
Hosoda *et al.*	Top	9	800	$800-1800$	$0-26$
Caviglia *et al.*	Back	>4	800	$30-260$	$\sim 28-60$
Bell *et al.*	Back	10	800	$50-1500$	$14-25$
Joshua *et al.*	Back	>4	$650-800$	various	$13-25$
Fête *et al.*	Back	no data	650	$4000-7000$	$2.5-4.5$

Table 5.2 Electrostatic tunability of mobility and carrier density in LAO-STO samples for this work and various references. A few growth conditions are given for comparison.

This table shows that the attained mobility of sample 20140819-3 is the highest mobility to date to have been achieved in a structured, top-gated sample. However, this is not the upper limit that is expected for these samples. Figure 5.4a) showed that that the gold on top of the LAO is not influencing the mobility strongly, so a perfectly structured device with a perfect epitaxial film growth should be able to attain a mobility above $6{,}000\ \mathrm{cm^2V^{-1}s^{-1}}$ [32].

The discontinuity at $V_G = 0\mathrm{V}$ only occurs if the gate voltage was swept to $|V_G| > 800\ \mathrm{mV}$ before going back. This might be related to the transient resistance described in Appendix C. If this transient resistance is shown to be related to a long-term structural effect, this might explain the 'permanent' change in the carrier density and the mobility. This discontinuity was not observed in the sheet resistance, which suggests that the discontinuity might also be due to an anomaly in the Hall signal after gating to high gate voltages. Another possible explanation is that the Hall signal is suppressed by introduced *p*-type carriers in the STO, after sweeping down from large gate voltages.

5.4.3 CAPACITANCE

In chapter 3, the capacitance per square for a top-gated LAO-STO interface was discussed and linked to important quantities for the description of the system, such as the density of states and the quantization energy of the lowest subband. This capacitance is easily derived from the data in figure 5.8 by taking the derivative of the carrier density to the gate voltage, as was discussed in section 3.3.

In figure 5.9, the capacitance per square for both samples is presented, dependent on the carrier density.

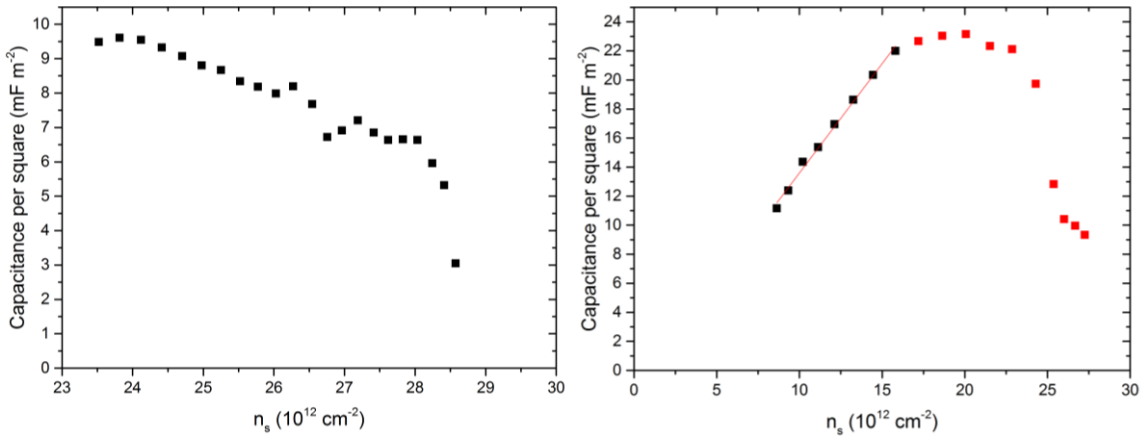

Figure 5.9 Capacitance per square as function of carrier density, as derived from figure 5.8; a) capacitance per square of sample 20140819-3; b) capacitance per square of sample 20141010-3, with a linear fit through the data points up to the point where this linear dependence stops. The negative gate voltage values from figure 5.8b) were neglected in this calculation.

Figure 5.9a) shows an almost linear dependence of the capacitance with a small negative slope up to a sheet carrier density of about $28 \cdot 10^{12}\ cm^{-2}$. There, the capacitance plummets as more carriers are attempted to add to the 2DEG. In figure 5.9b), the capacitance increases linearly to a certain point, which is at $n_s \sim 16 \cdot 10^{12}$ cm^{-2}. Beyond this point, it appears linear until is drops slowly and then abruptly at a carrier density of $\sim 24 \cdot 10^{12}$ cm^{-2}. The linear fit of figure 5.9b) goes close past the origin, but the origin is outside of the error margin.

Like the sheet resistance and carrier density/mobility measurement, figure 5.9a) and b) are different. However, a similar trend can be observed in both samples, if the same carrier density range is concerned: around $n_s = 20 \cdot 10^{12} - 25 \cdot 10^{12}$ cm^{-2}, the capacitance per square has a slightly negative slope, before a sharp transition takes place at $n_s \sim 28 \cdot 10^{12}$ cm^{-2} (figure 5.9a) or $n_s \sim 24 \cdot 10^{12}$ cm^{-2} (figure 5.9b)

Referring to literature, we may speculate on the origin of the features in these graphs,. Firstly, the maximum value of the capacitance per square in figure 5.9b) is exactly the value that Singh-Bhalla *et al.* [60(SI)] found for a 10 u.c. LAO sample at $T = 100$K. There, a linear slope below a certain gate voltage was reported, which persists down to a level two orders of magnitude lower, where it became constant in gate voltage again. These 'low' and 'high' plateaus may be applicable here, where we have probed the transition between the linear regime and the 'high' constant plateau. They suggest this capacitance characterization to originate from the formation of dipoles in the STO substrate [SI].

A more interesting interpretation of this data relates to the critical carrier density n_c reported by Joshua *et al.* [66]. The transition from the linear regime to the constant regime of the capacitance per square appears to be at the value found for the supposed Lifshitz transition, $n_c \sim 16.8 \cdot 10^{12}$ cm^ $- 2$ (section 2.4). However, nonlinearity in the Hall signals were not observed in this measurement. These are used as the hallmark of the Lifshitz transition by Joshua *et al.*

However, we suggest that nonlinearities may appear when the sample is measured in higher magnetic field strengths. In the paper, it was measured up to $B = 14\text{T}$ to detect the nonlinearities, where we measured up to only $B = 4\text{T}$ (mainly to save time) and. Also, the mobility that was obtained in the paper was mostly higher than the mobility we found above.

Joshua *et al.* suggest a 2D band structure with constant DOS except in the region in which the Lifshitz transition takes place. Here, the density of states increases linearly in energy, as a result of the band hybridization. Using the quantum capacitance relation derived in subsection 3.2.1, we suggest that the linear increase of the capacitance can be the result of this linear increase of the density of states in energy. In the region above the band hybridization range, the density of states is approximately constant, as is the capacitance above $n_s \sim 17 \cdot 10^{13}$ cm^{-2}. This suggestion is strengthened by the data of Singh-Bhalla *et al.* [60(SI)], as their 'low' plateau may be connected to the lower region of the band structure of figure 2.16, where the density of states is again constant and the conduction is supposed to be only in the $3d_{xy}$ band.

At this point, it is unclear how to interpret the data in light of the calculations by Van Heeringen *et al.* [47], who suggest a different subband structure than Joshua *et al.* [66].

The interpretation above does not explain the sharp drop in the capacitance at the highest carrier densities. We suggest this sharp drop might be due to a density of states effect that is outside the range of the picture by Joshua *et al.*, or an effect that is related to a response of the system to a very high gate voltage, either at the top interface with the gate electrode, or the interface region and the bulk STO.

Another explanation may be given by looking at expression (refer to the theory section here) where the third term in the capacitance relation, dE_0/dn_s, may relate to this figure. This term relates to the potential well shape and can provide information on its behavior with an applied top gate voltage.

For this, we use the reasoning of section 3.3, and we assume a constant density of states in the region directly above $n_c \sim 17 \cdot 10^{12}$ cm^{-2}, so only the potential well term dE_0/dn_s depends on the carrier density. In the capacitance relation in section 3.3, the capacitance depends on dE_0/dn_s with a power of -1. The linear dependence on the carrier density as shown in figure 5.10a) then suggests:

$$\frac{dE_0}{dn_s} \propto n_s^{-1} \rightarrow E_0(n_s) \propto \ln n_s.$$

This fits the description given in section 3.3, where the derivative of the lowest subband energy E_0 to the carrier density n_s is suggested to be definite positive for all n_s.

The measured slope does not support a model where the effective distance d of the parallel plate capacitor changes. Such a model is based on an assumption that the capacitor is not between the metal and the interface itself, but between the metal and the center-of-mass of the wave function, $\langle z \rangle$, in the potential well.

This dependence would influence the measured capacitance per area the following way:

$$\frac{C}{A} \propto \frac{1}{d} \propto \frac{1}{d_{LAO} + \langle z \rangle}.$$

Following the reasoning in chapter 3, the slope of the confinement potential is increased by putting in more carriers. Then, the electrons are confined closer to the interface, which is a reduction of $\langle z \rangle$. By the equation above, the capacitance should then increase as a function of carrier density, instead of the experimentally observed decrease.

For future research, we suggest to measure the capacitance as function of the carrier density for lower carrier densities. This could reveal the existence of the 'lower' plateau as seen by Singh-Bhalla *et al.* [60(SI)] and provide more information about the band hybridization region.

5.4.4 MAGNETORESISTANCE

The magnetoresistance of a material can provide information on relaxation times and length scales in it [20,26,28,30,87,88,94]. For instance, the (gate-tunable) spin-orbit coupling that has been reported [26,30] was measured by magnetoresistance curves and fitting the Maekawa-Fukuyama function to them. The magnetoresistance of our samples has also been measured and already at $V_G = 0$V, the curve is in strong disagreement with the curves presented earlier, as depicted in figure 5.10.

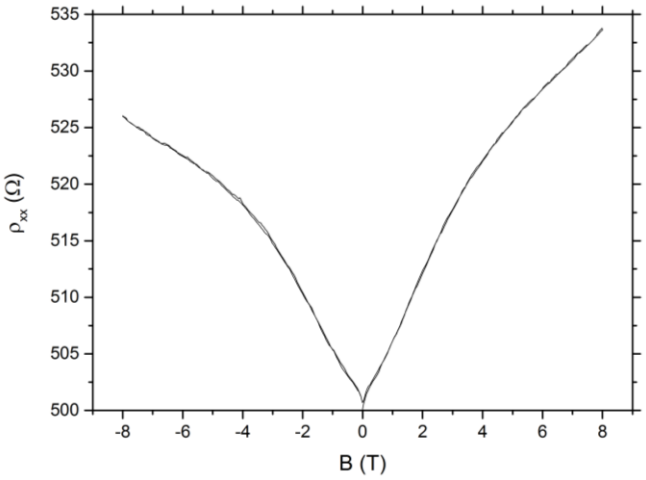

Figure 5.10 Magnetoresistance of sample 20141010-3 at $V_{TG} = 0$V.

There is a small kink at small field (~200 mT) and a larger kink at a larger field (~5T), between which the resistance is close to linear in field. This linear behavior was also observed by Wang *et al.* [95] for a bare LAO film grown at $p_{O_2} = 10^{-4}$ mbar. The magnetoresistance measured there is much larger. The origin of the linear behavior is suggested to be scattering off the steps of the substrate, which in that case was 200 nm. The substrate from figure 5.10 had a step width ~800 nm, as measured by AFM.

The magnetoresistance for several gate voltages has been measured for both samples discussed in the previous subsection. The results after interpolation and symmetrization are presented in figure 5.11. For all curves with $V_G \geq 800$ mV, an exponential correction for the transient resistance (Appendix C) has been applied. This could influence the exact shape of the curves, so these curves should not be used for quantitative analysis, as we do not know the origin and behavior of this transient resistance.

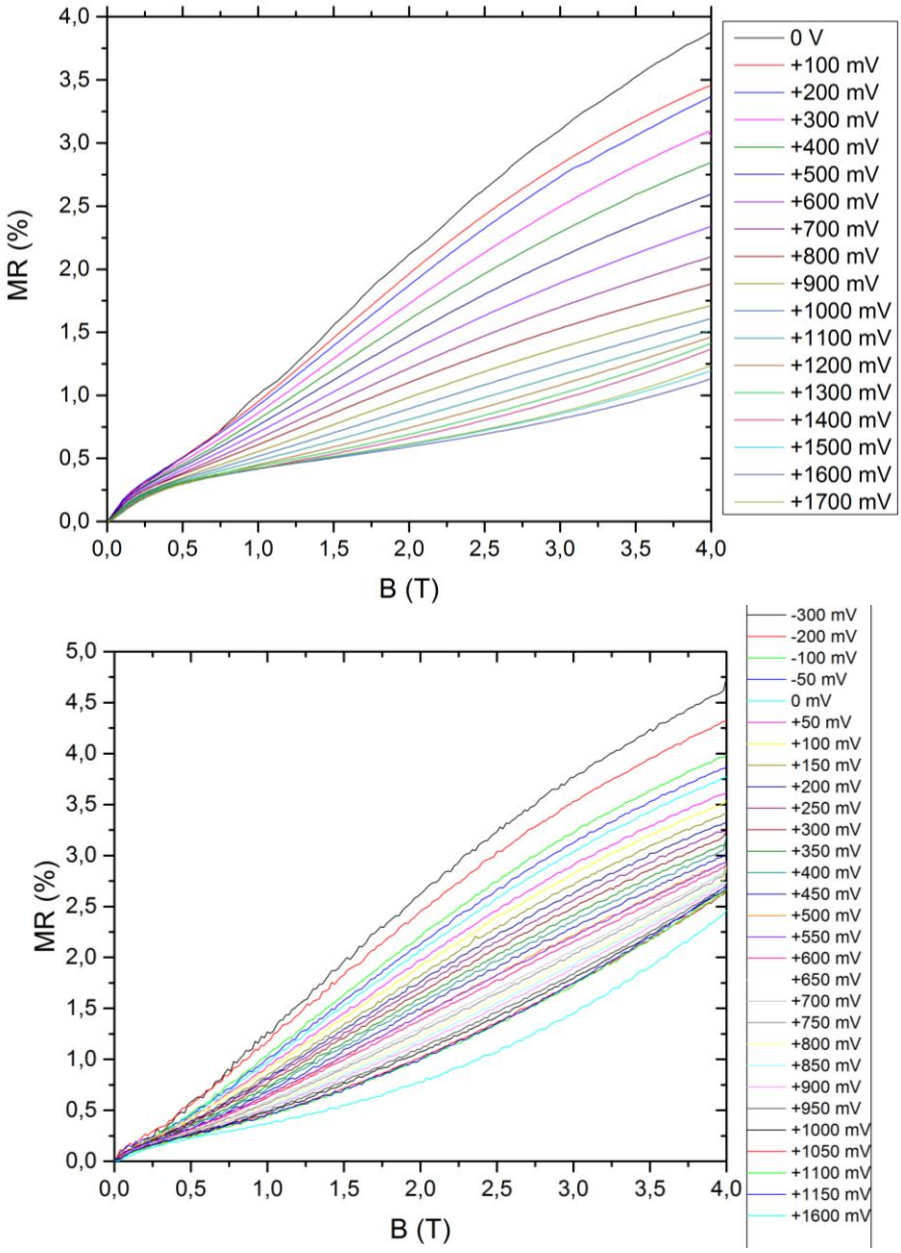

Figure 5.11 Magnetoresistance as a function of applied top gate voltage. a) magnetoresistance curves of sample 20140819-3. b) magnetoresistance curves of sample 20141010-3.

Several features can be observed in these figures:

- The magnetoresistance is positive for all gate voltages and magnetic fields below 4T;
- There is a resistance dip (or conductance peak) around $B = 0$T for all gate voltages;
- The magnetoresistance at $B = 4$T goes down as a the gate voltage is increased;
- The curvature of the lines changes as the gate voltage is increased;
- The large magnetoresistance effect from section 5.2 is absent in these measurements.

We were unable to fit these curves with the Maekawa-Fukuyama formula, as is done by Caviglia *et al.* [20]. This formula can be generalized to the HLN formula of weak antilocalization [94], for which the fit also did not converge. However, we could scale this to a magnetic size effect. When magnetic size effects are considered, the curves are found to scale to the inverse of the cyclotron radius for low fields:

$$l_{cyc}^{-1} = \left[\frac{\hbar}{eB}\sqrt{2\pi n_s}\right]^{-1}.$$

This as depicted in figure 5.13 for sample 20141010-3. Here, the values for $2\,l_{cyc} = W_V$, the width of the voltage contacts and $2\,l_{cyc} = W_{steps}$, the width of the STO steps, are given. No change is seen at lengths comparable to the terrace width . However, the effective length scale is compatible with the width of the voltage contacts $W_V = 15$ µm and may therefore be interpreted as a classical magnetic size effect [28]. This is peculiar, as the mean free path is much smaller than this typical size.

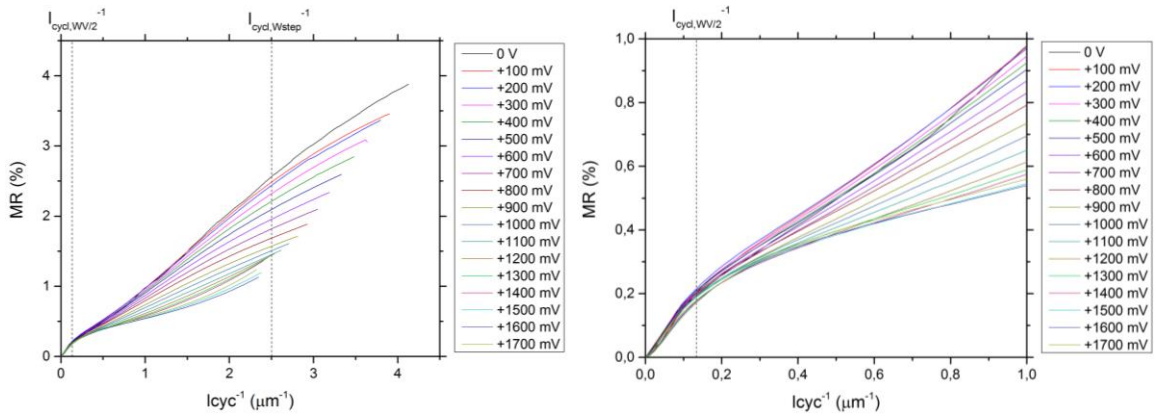

Figure 5.12 Magnetoresistance as function of the inverse of the cyclotron radius; a) 4T range; b) zoom on lower l_{cyc}^{-1}.

Ben Shalom *et al.* [96] investigated the out-of-plane magnetoresistance of LAO-STO interfaces at lower temperatures, at which the samples have onsets to superconductivity, for different back gate voltages. They measured op to 14T with magnetoresistance up to 200% at this magnetic field scale. In comparison to these values, the magnetoresistance values are much lower. However, the same trend in resistance as function of magnetic field is visible in their figure 1, with the exception of the dip in the middle.

On the MR-axis, a scaling factor is yet to be found. The fact that these curves bend down by increasing the gate voltage is unlike other work [26,96], even for top-gating [30]. The latter suggests that the mobility is not the dominant factor in the magnetoresistance tunability, which could have been an explanation if this gate tunability would consistently have been dependent on the gate voltage with a different sign for top and back-gating.

We suggest that the dependence presented here is an interplay between different effects, such as spin-orbit coupling, size effects and classical magnetoresistance. This interplay is very interesting for future work, as it may reveal even more interesting phenomena emerging at the LAO-STO interface.

5.5 BACK-GATING

In this work, back-gating has not been done as extensively as top-gating. To test the hypotheses formulated in chapter 3, the mobility and carrier density have been tuned, although for a different sample than the two samples discussed in the section above. The sheet resistance, carrier density, mobility and capacitance per square of this sample are given in figure 5.13. During these measurements, the top gate voltage was set at 0 V.

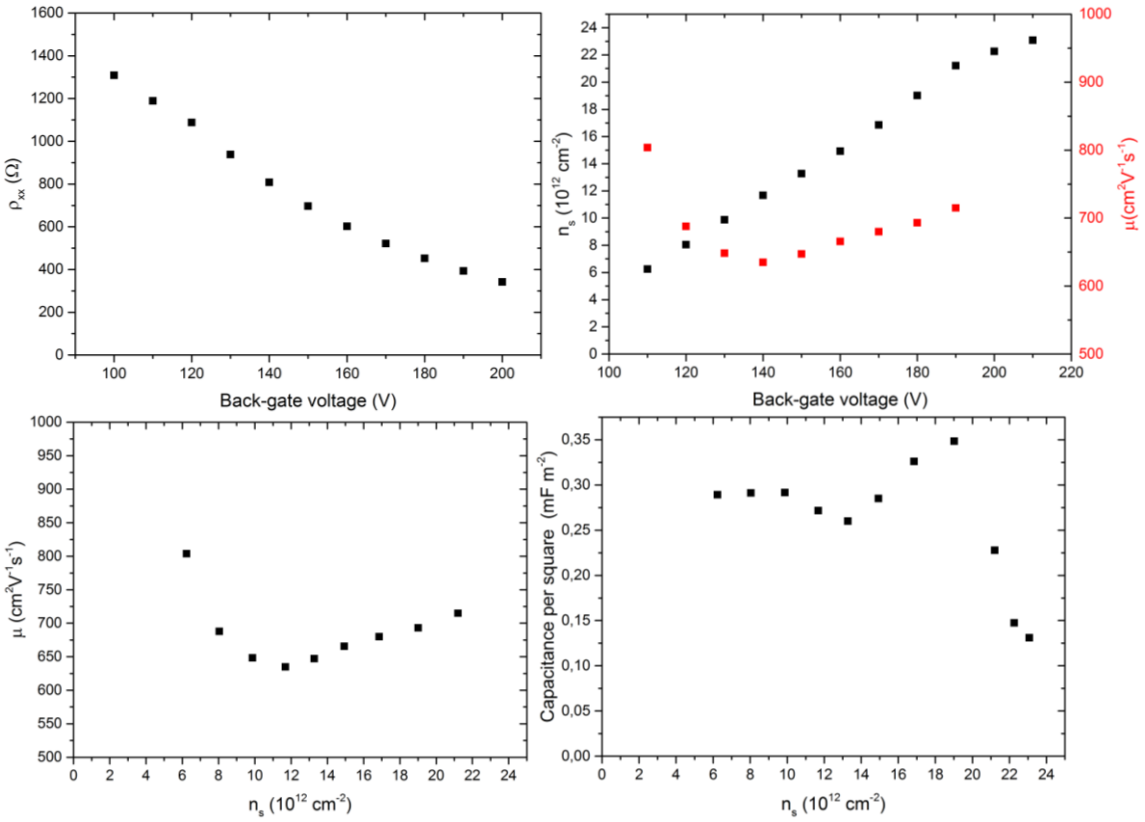

Figure 5.13 Back-gate characteristics of sample 20140523-3 at $T = 4.2$K; a) Sheet resistance at $B = 0$ versus gate voltage; b) carrier density and calculated Hall mobility versus gate voltage; c) carrier density versus Hall mobility; d) capacitance per square versus carrier density.

The back-gate voltage was so high because an attempt was made to scan the whole range of the back-gate voltage source of $\pm$ 200 V. However, such high back gate voltages can cause irreversible behavior due to charge trapping in the STO [20]. We suggest this is the reason why the 2DEG was near depletion around + 110 V already.

The measured sample had a bad RHEED signal for the SCO layer, so it is uncertain if the capping layer was grown correctly and the oxygen diffusion enhancement was effective. This is probably why the mobility is a few times lower than the mobility of the samples measured in section 5.4. The temperature dependence of the carrier density was not measured for this sample.

The mobility and carrier density are found to be back-gate tunable in this sample, and the results compare well to previous research [21]: both mobility and carrier density increase with increasing gate voltage in a certain range in carrier density. However, below a certain carrier density, which is outside of the measurement range of Ref. [21], we observed a mobility enhancement as the 2DEG is depleted further.

Similar to the top gate measurement, the capacitance per square is non-constant and different regimes can be identified. Here, we also observe a linear increase of the capacitance in a certain carrier density range. There is no plateau visible above the linear regime, but there appears to be a flattening out below $n_s \sim 12 \cdot 10^{12}\mathrm{cm}^{-2}$, similar to the values found by Singh-Bhalla *et al.* [60(SI)]. The sharp decrease of the capacitance at high carrier density is also observed in the back-gate measurement. This supports the suggestion that this is a feature of the density of states that is outside the modeled region by Joshua *et al.* [66].

5.6 SUMMARY

We have measured transport properties of SCO-STO capped LAO-STO interfaces with a top gate electrode. We showed a strong influence of adding the top gate electrode on top on the carrier density, where the mobility appeared unchanged. The leakage current that was measured in a sample with an gate, etched by KI was comparable to the best values in literature.

We could tune the carrier density and the mobility of the 2DEG in a large range, but have not yet done measurements in the near-depletion zone. The tuning features correspond to literature and are consistent in different samples. From a capacitance analysis, we suggest that a top-gated device can be used for direct measurements of the density of states of the 2DEG and the potential well at the interface. A back-gating experiment supports the data of the top-gate capacitance, where the mobility was found to increase strongly when gating below a certain carrier density.

The magnetoresistance of these samples were also tuned by a gate voltage. The shape of the magnetoresistance curves is unlike shapes found in earlier work, and suggests that an interplay of multiple effects at hand in these samples. The curves did scale to the inverse of the cyclotron radius, which suggests that one of the effects responsible for this behavior is a magnetic sizing effect. An anomalously high magnetoresistance was found for one sample, which was accompanied by a resistance upturn below $T \sim 20\mathrm{K}$.

5.6.1 FUTURE WORK

The demonstrated potential to tune the carrier density and the mobility by a top gate voltage opens possibilities to explore the physics of these interfaces even further. A step that can directly be taken is to further explore the capacitance-carrier density diagram and go to lower carrier densities. This might lay bare the lower region in the band structure, where one expects to be only in the $3d_{xy}$-band. The strongly increasing mobility in the back-gating measurement suggest we have already entered this regime once and the mobility of this regime can be much higher than the mobility in the higher carrier density region. If we can show this strongly increasing mobility for the lowest carrier density values, that would be a big step towards the long-term goal of observing nanoscale (ballistic, quantum) transport.

The change in carrier density we found after adding the gate electrode supports the simple electrostatic model derived in chapter 3. This shows that this approach to describing the electrostatics of the system has physical evidence. This model has also shown that the capacitance is not a simple parallel plate capacitor but a quantity that probes fundamental properties of the system. Further electrostatic modeling with the inclusion of methods such as DFT will provide more insights on the exact effects of gating, as well as increased understanding of the role of the potential well and the spread of the wave function on the band structure. An experiment that could be done to further explore the electrostatics model is an investigation of the effect of the gate metal work function on the carrier density of the 2DEG, by varying the top-gate electrode material, e.g. Pt, Ag.

During the work on this thesis, we did proof-of-concept measurements for simultaneous top- and back-gating and conductance pinch-off by a split-gate. The simultaneous top- and back-gating experiment resulted in too few data to make an analysis, but a result was that the top- and back-gates worked independently in voltage ranges of $-20 < V_{BG} < 0$ V and $0 < V_{TG} < 0.4$ V and the average carrier mobility was no longer intrinsically coupled to the carrier density. The split-gate showed complete conductance pinch-off for a setup with two gate electrodes spaced < 1 μm apart. Conductance quantization was not yet observed in this device, but the proposed improvements on the fabrication (chapter 4) are expected to result in sufficient mobility values to observe an effect related to the emergence a quantum point contact.

6. CONCLUSION

We have fabricated and measured $SrCuO_2$-$SrTiO_3$-capped $LaAlO_3$-$SrTiO_3$ devices with a top gate electrode. The transport behavior of these samples was presented and discussed with references to literature. An overview of the physics at the $LaAlO_3$-$SrTiO_3$ interface was presented, including ways to tune its properties and proposals for its band structure.

The fabrication procedure was strongly improved in comparison to the procedure for making structured, top-gated LAO-STO devices that was used before the start of this work. We introduced a $SrCuO_2$-$SrTiO_3$ capping layer, which increased the mobility of the samples by an order of magnitude. Another order of magnitude increase is expected from a thorough, systematic study of growth parameters and structuring techniques using this capping layer. Furthermore, the fabrication reliability of the samples was greatly increased by using an always insulating AlO_x hard mask layer instead of sometimes conducting amorphous $LaAlO_3$. The gate leakage was reduced to the lowest values found in literature, or even lower, by using a gentle sputtering procedure with KI etching to define the gates.

A simple model was devised to describe the effect of gating on the properties of the 2DEG at the LAO-STO interface. It was found that the carrier density of the 2DEG is strongly influenced by the presence of a top-gate electrode and this shift should be dependent on the work function of the metal. The capacitance that was is not a simple parallel plate capacitance, but a capacitance that depends on fundamental properties of the 2DEG. The difference between top- and back-gating the 2DEG was ascribed to the different effect these gating techniques have on the confinement potential.

Electrostatic tuning, or field-effect modulation, of the 2DEG was measured by transport experiments. A change of the carrier density after adding a gate electrode was measured experimentally and found of the order of the original carrier density, as predicted by the electrostatic model. A future study is to confirm the dependence of this carrier density offset on the work function of the gate metal, as predicted from the model. The carrier density and mobility could be tuned by a top-gate voltage in a relatively large range in comparison to literature. The magnetoresistance was also found gate-tunable, but the shape was such that no widely used fitting model applied. A theoretical study on magnetoresistance is needed to explain the measured curves and the way these curves were tuned by the top-gate voltage. The same holds for the anomalous behavior of a sample without top-gate electrode, which showed a large magnetoresistance increase and a resistance upturn.

The measured capacitance was in strong disagreement with a parallel plate capacitor model and showed good agreement with the derived electrostatic model. The data were compared to predictions based on proposed band structures for LAO-STO in literature, which imply that the measured capacitance is a direct measurement of the density of states as function of the carrier density. The results also suggested a direct measurement of the quantization energy in the potential well. Similar features of the capacitance were observed in a back-gate measurement, supporting the derived electrostatic model.

In general, this work has contributed to the understanding of electrostatic gating of the 2DEG at the LAO-STO interface. We have suggested that gating can probe fundamental properties of the 2DEG, and that gating can manipulate them. We have identified the role of the chemical potential in the gating process and used this to explain experiments. The improvement of the fabrication process of top-gated structured LAO-STO devices has made major steps towards the long-term goal of creating nano-electronic devices in this material system.

APPENDIX A: STEP-BY-STEP FABRICATION PROCEDURE

The fabrication procedure of the samples grown in this work involves many steps, as listed in chapter 4. In this appendix, these steps are presented in a chronological order to present the reader an idea of the entire sample fabrication process and all the actions involved to make a single sample before measurement.

A.1 AlO_X BASE LAYER

First, the substrates are treated according to the method described in subsection 4.2.1. After checking the quality and terrace width with AFM, the preparations for the deposition of AlO_x are made. AlO_x demonstrated good insulating properties as a masking layer [84], but might leave residue on the STO surface.

A single-crystalline Al_2O_3 (sapphire) target is ground for smoothness and put into the PLD chamber. The substrate is cleaned by sonication in acetone and ethanol (5 min each) and mounted on a heater with double-sided carbon tape. The target holder and the heater are put into the PLD chamber, where the pressure is reduced to $2 \cdot 10^{-7} - 5 \cdot 10^{-7}$ mbar by degassing the heater and target holder. During degassing, the laser optics are aligned. A mask (15×2 mm^2) is used to select the most homogeneous part of the laser beam and an alignment laser is used to make sure the high-energy laser beam hits in the right spot. Based on the desired laser fluence and spot size, the positions of the mask and the focusing lens, as well as the desired laser energy are calculated. An optical attenuator is used to tune the laser energy to the calculated value.

When the laser settings are done, the focusing lens is adjusted such that it hits the target in the center. Here, it is focused and, therefore, has the calculated energy density. If the laser beam hits too much off-center, the ablated spot on the target becomes out-of-focus. As a result, the laser fluence and plasma kinetics change, leading to bad films or films with irreproducible results. We chose a laser fluence of 1.5 J/cm^2 and a spot size of 2.3 mm. The laser voltage is set between 22.0 and 24.0 kV, depending on the maximally attainable laser energy. The corresponding film thickness for these settings is 0.08 nm/pulse, as has been determined by AFM.

Then, a shutter is placed between the target and the substrate to prevent material to deposit while preablating the target. An oxygen flow is set up (20 ml/min), with the main pumping valve closed such that the deposition pressure $p_{O2} = 2.2 \cdot 10^{-1}$ mbar. A few pulses are fired upon the target in order to make an imprint to check the sharpness of the ablation area as well as a final check where it hits.

If necessary, adjustments are made and the process of making an imprint is repeated. If the imprint is in the correct spot, the target is preablated (4 scans at 5 Hz, scan width 4 mm. This is done to remove any material other than the target material from the ablation area, and to create a reproducible stoichiometry at the target surface.

During preablation, one can adjust the position of the heater in order to make the plume hit the substrate head on. If the center of the plume does not hit the substrate in the middle, film thickness and quality may vary, which leads to irreproducibility.

After preablation is done and the preablation area has been checked, the actual deposition can be done. The shutter is moved out of the way and 400 pulses are fired at the target, at a frequency of 1 Hz. This leads to a film of about 32 nm thick, which is thick enough to prevent the LAO from punching through, which could induce interdevice conductivity. It is thinner than the planned gate layer ($d \sim 40$ - 60 nm), so this thickness of the AlO_x layer should not compromise the connections to the gate. Furthermore, a thickness of 32 nm has been found to provide some contrast between the AlO_x and LAO parts of the sample later on, which makes lithography and quality checks easier.

A.2 Amorphous LAO alignment markers

Alignment markers are used to align all the subsequent patterning steps in the fabrication process (Hall bars, contacts and gates). The markers used in this thesis are described by Eerkes [30], and are deposited by PLD after defining them by UV lithography. The lithographic step is done in the cleanroom, by spinning a layer of OLIN 907-12 photoresist (PR) on the sample (6000 rpm, 45 s) after cleaning it by sequential sonication in acetone and ethanol (5 min each). This is baked at 100°C for 1 min, after which excess resist is removed from the backside of the sample by rubbing it onto a piece of cleanroom paper that was sprayed with acetone. Then, a mask is aligned to the edges of the sample and the parts uncovered by the mask (light field) of the sample is exposed to 10 mW UV light for 7 s. After exposure, the photoresist is put in a developer solution (OPD 4262) for 40 s, after which development is stopped by two rinsing steps of 30 s in DI water. The result of the lithographic step is checked under a high contrast microscope, which provides contrast for thickness variations of the order of 10 nm.

After lithography, the PLD deposition is done in a similar way as the AlOx layer, but with a single-crystalline $LaAlO_3$ target. For this deposition, the fluence of the laser is set to 1.3 J/cm^2, the deposition pressure is $1.7 \cdot 10^{-3}$ mbar O2 and the spot size is 2.3 mm^2 for the 55.9 mm^2 mask. At room temperature, 4000 pulses are fired at 5 Hz, which results in amorphous markers of about 100 nm thick. These markers are on the corners of figure 4.3 and are marked as 2, 3, 4.

A.3 AlO_x wet etching

After the markers have been deposited, it is possible to perform the etch step on the AlOx hard mask, defining the structure of the 2DEG, via the method as described by Banerjee *et al.* [83]. This step is done on the same day as the next step to minimize the exposure of the bare STO to contaminants before depositing the epitaxial film.

For this step, lithography is performed on the sample, similar to the process for the alignment markers, except for the part from the alignment step onwards. The etch mask defining the structure is now aligned with the markers to a precision of about 2 µm. After the UV exposure, the development is done in separate glassware and the sample is kept in the OPD 4262 developer solution for 2 minutes. This increased time ensures that the AlO_x is chemically etched away from

the surface, which lays the STO surface bare. After the etching, excess solution is sprayed off with DI water. The remaining photoresist is removed by soaking in acetone for 1 min and spraying the sample with ethanol before blowing the sample dry. After this step, the sample is put into the PLD chamber as soon as possible to minimize the amount of contaminants in this step.

A.4 EPITAXIAL FILM GROWTH

In this work, two types of epitaxial oxide films have been grown: LAO, in the non-magnetic regime [12,30], and LAO-SCO-STO, following Huijben *et al.*[32]. The recipe for the growth of the LAO-SCO-STO layer is discussed below.

The deposition in the PLD-RHEED system is somewhat similar to the AlO_x base layer deposition. Now, the targets used are single-crystalline $LaAlO_3$, sintered-powder $SrCuO_2$, and single-crystalline $SrTiO_3$. Also, the sample is mounted on the heater through silver glue (Leitsilber) instead of carbon tape to enable deposition at elevated temperatures. The sample is mounted such that a large area in the middle of the sample, the so-called RHEED window, is aligned with the heater x-axis. This makes the alignment of the RHEED beam easier and improves the resolution of the oscillations.

After the heater with the sample is placed in the chamber, preablation for all targets is done at room temperature and an oxygen pressure of $5 \cdot 10^{-5}$ mbar. Then, the alignment of the RHEED is done. First, the valve connecting the RHEED to the chamber is opened and the voltage is set at 35 kV. At this voltage, the current is ramped up to about 1.0 A, for which the direct beam should be visible on the phosphorus screen. This direct beam is tuned by changing the x- and y-deflection, the focus of the beam and the aperture grid. When this beam looks round, the x- and y-deflections are linear and the beam is coming from the center of the aperture, the sample is positioned in place. This is done such that there is a refractive reflection from the surface of the substrate, by changing the y position and the in-plane and azimuthal angles of the heater stage.

Now, the sample is heated to the deposition temperature of the LAO, 850°C, as fast as possible, in the background pressure of $5 \cdot 10^{-5}$ mbar. Meanwhile, the position and rotation of the heater stage is being adjusted since the RHEED image changes due to thermal expansion of the heater and the sample. At the deposition temperature, the RHEED signal is recorded by measuring the peak intensity of the main reflected spot. For the LAO, the RHEED signal is expected to drop [32] during the deposition, so the initial intensity is tuned to about 95%. The deposition is done while monitoring the RHEED signal. After the tenth peak, the deposition is stopped, which ensures the thickness of the layer to be 10 unit cells. The RHEED signal for the LAO deposition, as well as the RHEED image after the LAO deposition at 850°C, are depicted in figure 4.6a).

Then, the sample is cooled quickly to 600°C, at which the SCO and STO are deposited. The RHEED signal is adjusted during this cooldown, and the oxygen pressure is increased to $6 \cdot 10^{-2}$ mbar after the cooldown. The single unit cell of SCO is deposited, for which it is expected that the RHEED signal drops during the deposition of a single unit cell [32].The deposition is monitored by the RHEED signal and image given in figure 4.6b.
Directly after the SCO is deposited, the STO deposition is prepared by tuning the RHEED signal

to about 25% intensity, as the intensity is expected to rise as the STO is deposited [32]. The RHEED signature of the STO deposition is depicted in figure 4.6c. After the STO is deposited, the sample is cooled down to room temperature at 10°C/min in the deposition pressure. The deposition parameters for the entire deposition are given in table 4.1.

When a normal LAO film is concerned, the above steps are taken with the exception that only the LAO is deposited and a change of parameters, following Eerkes' recipe [30]. These parameters are also given in table 4.1.

A.5 Au gate deposition

After the epitaxial film growth, a base Au layer is deposited by RF sputtering across the entire sample, from which shape of the gates is defined later. The deposition of this film is done directly after the deposition of the epitaxial oxide layer, in order to minimize contamination of top surface by further processing with photoresist, developer, acetone and ethanol, which can alter the properties of the 2DEG significantly, as discussed in chapter 2.

Eerkes *et al.* [25,30] used a different method of creating a top gate. E-beam evaporation of Au was used to grow the top gate gently with minimized leakage currents. The sputtering technique discussed below also guarantees a slow deposition, which is gentle enough to avoid large leakage into the sample for top gate voltages over 1V, as is shown in chapter 5.

For the Au sputtering, a Perkin Elmer model 6300 is used. Loading the sample is done automatically after mounting it onto the sample holder with thermal paste. After loading the sample, the argon deposition pressure in the chamber is set to $8.2 \cdot 10^{-2}$ mbar– instead of the usual $2 \cdot 10^{-2}$ mbar – from a background pressure $< 1 \cdot 10^{-6}$ mbar. The correct target, sample position and operation mode are chosen and the table spacing is increased manually from 1.6 to 2.2 inches to decrease the impact energy of the Au particles on the surface. Then, a plasma is ignited by turning on a radiofrequency (RF) source, while keeping the measured forward power unmeasurably low and the target bias around -200 V, which is also very low as compared to usual values around -1000 V. The deposition is carried out in 34 min during which the deposition parameters are monitored carefully. This results in a film thickness of 30 – 50 nm, as checked by AFM. This film is slightly transparent and looks greenish rather than gold.

A.6 Contacts

Contact to the 2DEG is made by Au/Ti contacts, where the Ti ensures better adhesion of the contact to the STO substrate. After depositing the base Au layer, UV lithography as described in section A.2 is done to define a pattern for the contacts, aligned with the alignment marks.

Then, argon ion beam etching (dry-etching) is used to penetrate the deposited layers into the STO substrate. This should also render the STO locally conducting [82], improving the contact of the metal to the 2DEG. For the etching, the sample is mounted on a sample holder with vacuum grease and put in the etching chamber, where the etch pressure of $4 \cdot 10^{-4}$ mbar in argon is set with a background pressure of $\sim 3 \cdot 10^{-7}$ mbar. The sample stage is cooled by a flow-separated water cooling system and the used etch parameters are given in table A.1.

Parameter (unit)	Value	Parameter (unit)	Value
p_{Ar} (mbar)	$4 \cdot 10^{-4}$	V_{beam} (V)	350
p_b (mbar)	$3 \cdot 10^{-7}$	I_{beam} (mA)	25
Angle	90°	V_{acc} (V)	60
Etching time (min)	8	I_{acc} (mA)	1
Rotation speed (rpm)	4	I_{dis} (A)	0.21
$I_{neutralizer}$ (mA)	31	V_{keeper} (V)	22.6

Table A.1 Parameters for argon ion etching

After etching, the sample is transferred to the Perkin Elmer sputtering machine, where the sputtering is done with the settings given in table A.2, at an argon pressure of $2 \cdot 10^{-2}$ mbar and a table spacing of 1.6 inch.

Step	P_{rf} (W)	t (s)	U_{target}(V)
Ti cleaning	250	120	-1100
Etch	150	15	-550
Ti deposition	150	60	-950
Au deposition	150	180	-1100

Table A.2 Sputtering parameters for depositing contacts.

After the sputtering step, the contacts are lifted off by sonication for 5 min in acetone, after which the sample is cleaned by sequential sonication in acetone and ethanol (5 min each).

A.7 DEFINING THE GATES BY KI ETCH

The shape of the gates is defined by using UV lithography to create a protective photoresist mask over the gate and contact areas, after which the exposed Au areas are etched with KI, a solution that dissolves Au. The contact areas need to be protected to prevent them from being etched away. This is impossible to repair, since the contacts cannot be made into exactly the same spot as before. Repeating the contacts deposition step implies a bad contact to the 2DEG as there would be a gap due to the ion milling in the previous step.

During the standard UV lithography (section A.2), the exposure time and development time are increased to 8 s and 45 s, respectively. This is done because there may be strictly no residue of any photoresist after development on the sample, which could block the KI to dissolve the gold. This residue would lead to a connection between the gate material and the contacts to the 2DEG, shorting the gate electrode and rendering it useless.

After lithography in the cleanroom, a solution containing KI is prepared with a mass ratio of 2:1:10 of KI:I_2:H_2O. This solution can be made for future use, if the solution is sonicated for at least 30 min prior to usage. The KI solution is further diluted 1:10 with DI water in a glass beaker, which is then placed on a heater. This heats it to about 50°C, for which a 50 nm Au test layer was found to be dissolved in 15 s.

Then, the sample is dipped in this solution for 20 s, which should at least dissolve a film of 67 nm if the above etch rate is scaled linearly. The etching is stopped by two rinsing steps of 30 s in DI water. The sample is blown dry and under an optical microscope, we check if there is Au residue on the uncovered areas. If there is too much residue, the above process is repeated with 5 s etching time until the residue is gone. After this check, the photoresist is removed by sequential sonication in acetone and ethanol for 5 min. The sample is stored in a nitrogen-rich desiccator until wiring it for measurement.

APPENDIX B: RESISTANCE TRANSIENT AT HIGH GATE VOLTAGES

During the transport experiments described in chapter 5, the longitudinal resistance did not retrace in magnetic field for gate voltages above 800 mV. This is displayed for the longitudinal resistance trace for $V_G = +900$mV, figure B.1. This appendix is about the characteristics of this phenomenon that we introduce as a transient resistance. It has the same basic behavior for all curves, which makes transient resistance an effect that should be taken into account when measuring top-gated LAO-STO devices, but might also be used for applications in future work.

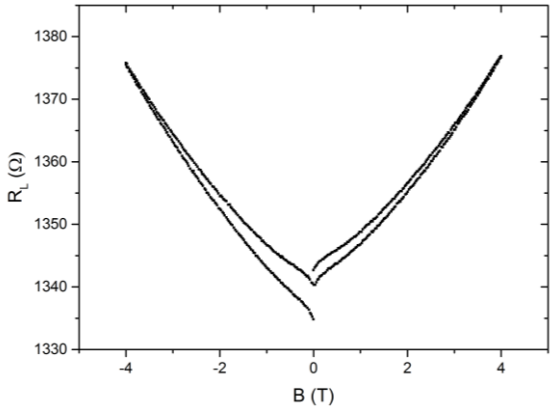

Figure B.1 Badly retracing longitudinal resistance signal for $V_G = +900$ mV in sample 20140819-3.

In all measurements, the magnetic field was swept to negative values before it went to positive values, so from figure B.1, we find that the longitudinal resistance drifts upwards in time. This measurement was done at a sweep rate of $dB/dt = 10$ mT s^{-1}, so such a full sweep takes $1600\ s \sim 23$ min to complete. The transient resistance seems to slowly decay in time, because the spacing between the traces for negative field is larger than the spacing between the traces for positive field.

B.1 HALL SIGNAL

Such a transient was only observed in the longitudinal signal. The Hall signal of the same sample, together with a linear fit through the data, is shown in figure B.2a). The regular residual of this fit is given in figure B.2b), which shows that there is no trace of a time-dependent term in this signal, except for the small hysteresis of $< 1\%$ of the Hall resistance at 4T. We attribute this hysteresis to the high magnetic field sweep rate in the measurement.

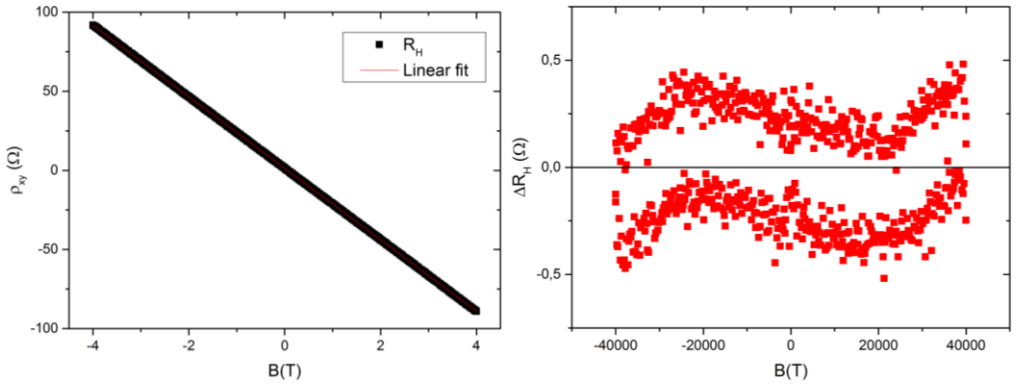

Figure B.2 absence of transient resistance in the Hall signal at $V_G = 900$ mV in sample 20140819-3. a) Hall signal, with linear fit. b) residual of the data with respect to the fit in a).

B.2 RESISTANCE CORRECTION

Attempts to compensate for the drift in figure B.1 were done during the work on this thesis. The decay in time was approached as an exponential fit, for which this fitting formula was used:

$$R_L(V_G, B, t) = R_L(V_G, B) - A(V_G)e^{-\frac{t-t_0}{\tau_{TR}}}.$$

Here, $R_L(V_G, B, t)$ is the measured data and $R_L(V_G, B)$ is the response of the longitudinal resistance to the magnetic field. The second term on the right is the drift correction term and consists of a gate-voltage dependent amplitude $A(V_G)$ and an exponential decay in time with a typical time scale τ_{TR}. Using this formula, we can find the longitudinal resistance as a function of gate voltage and magnetic field if we extrapolate the drifting trace from figure B.1 to infinity:

$$R_L(V_G, B) = R_L(V_G, B, t = \infty).$$

For the corrections of the magnetoresistance traces, the fit formula was fitted through the three points at which $B = 0$, so $t = 0, 800, 1600$ s. This has resulted in the red curve in figure B.3.

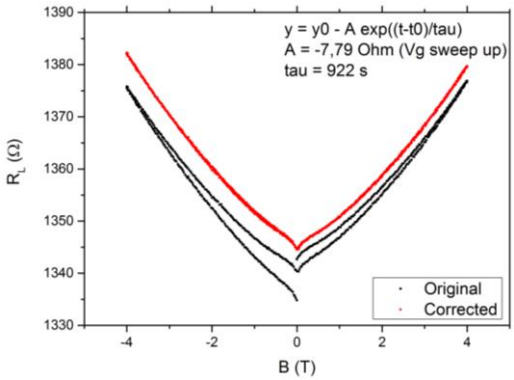

Figure B.3 correction of the transient resistance by subtracting an exponential term in time, with the main parameters, the corrected curve (red) and the as-measured data (black).

The resulting corrected curve is a retracing, symmetric curve around $B = 0$. This method was applied to all curves for $V_G \geq +800$ mV.

One measurement on this sample, the measurement at $+1600$mV, was taken after the gate voltage was swept down from a higher value of $+1900$ mV. This resulted in a downward drift, as depicted in figure B.4. This shows that the transient resistance is dependent on the history of the sample.

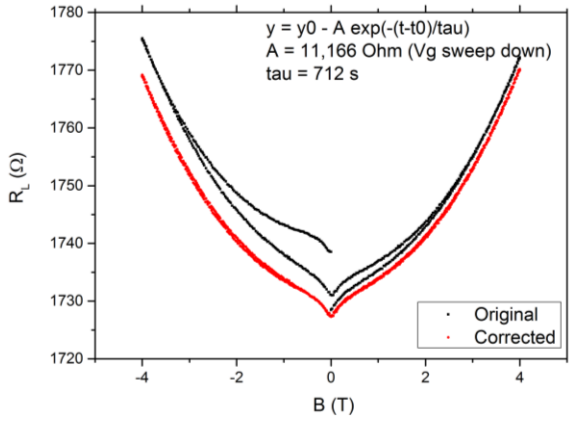

Figure B.4 Downward transient resistance in the longitudinal resistance at $V_G = +1600$ mV.

The dependence of the fit parameters A and τ_{TR} on V_G can be used for a future model of the transient resistance. During the measurements, the gate voltage was increased within 5 minutes after each measurement. The parameters A and τ_{TR} have been plotted against V_G in figure B.5.

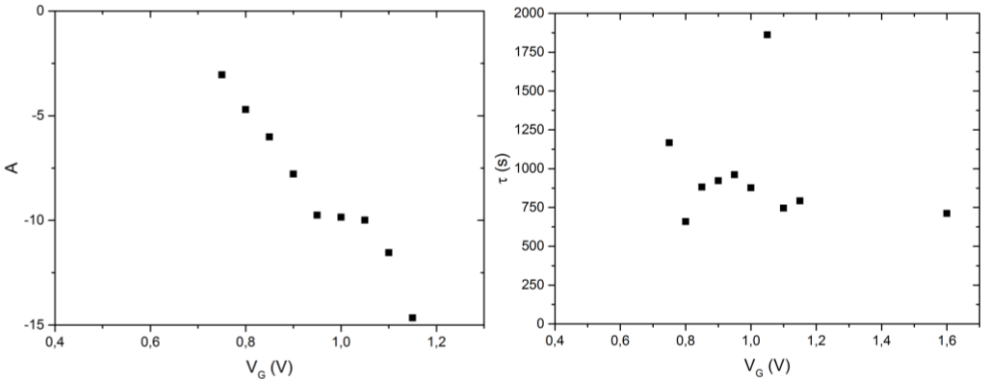

Figure B.5 Fit parameters as function of gate voltage for the transient resistance in sample 20140819-3. a) the amplitude A in Ω; b) time constant τ in s.

The drift amplitude A appears to be linear with gate voltage, where the linear fit would cross the x-axis at about 650 mV. However, it depends on the sample history, since $A = +11\ \Omega$ for the $+1600$ mV measurement in figure B.4. So, we cannot interpret this A to be linearly dependent on the gate voltage, but as a quantity that depends on the gate voltage and the gate voltage history.

The transient resistance time constant τ_{TR} appears constant, except for the value at $+1050$ mV, where there had been a break in the measurements of about 1 h. Even the value at $+1600$ mV, with the different history, is within the error margin if the value for the other measurements. So, in this measurement, the relaxation time of the transient resistance presents itself as a constant in the measurement, as long as the measurement is carried out directly after changing the gate voltage.

B.3 DISCUSSION

This transient resistance was observed for more samples, but this one is presented here as it was the one with the best traces after the exponential correction. It always set in at about $V_G \geq 800$ mV and always moved the resistance upwards for an upward changed gate voltage in time. This suggests that the transient resistance is not a measurement artefact, but something that originates from the system.

The origin of this transient resistance is elusive. It is a long-term effect and thus cannot be caused by free electrons, that have many orders of magnitude lower relaxation times. We suggest that a possible explanation could be in the structure of the STO (e.g. structural transitions [97], or at the interface between the top surface and the gate electrode, which could result in a slowly changing polarization in the LAO.

The dependence of the transient resistance on the history of the sample is interesting from an application point of view. The effect might be applicable in a memory device or even as a memristor. The latter might be possible as it changes its resistance over two timescales: a short, immediate response to the electric field by the free electrons in the 2DEG, and a longer response that refers to the transient resistance.

APPENDIX C: 2D ELECTRONIC TRANSPORT

In this thesis, the LAO-STO 2DEG is probed by transport measurements. This Appendix is a short summary of the theory of 2D electronic transport.

First, a short discussion is presented on the diffusive transport regimes and related length scales in the LAO-STO interface for different references. Then, a categorized list of formulas is given for different quantities that are measured in this thesis.

C.1 DIFFUSIVE TRANSPORT

Electronic transport can be classified into three regimes of conduction mechanisms: diffusive, ballistic and quasi-ballistic [28]. The distinguishing factor between these regimes is the mean free path, which is the velocity v_F of the electrons at the Fermi energy times the average time between scattering events τ:

$$l = v_F \tau.$$

From previous measurements [1,24,30,32], the mean free path can be estimated from the mobility and carrier density, that are related to the Fermi velocity and scattering time. This is done in table B.1.

Reference	Mobility and carrier density	Mean free path
Ohtomo and Hwang	$\mu \sim 5000\ cm^2\ V^{-1}s^{-1}, n_s \sim 1.0\ 10^{17}\ cm^{-2}$	$l \sim 26\ \mu m$
Huijben	$\mu \sim 50000\ cm^2\ V^{-1}s^{-1}, n_s \sim 6.0\ 10^{12}\ cm^{-2}$	$l \sim 2\ \mu m$
Eerkes	$\mu \sim 300\ cm^2\ V^{-1}s^{-1}, n_s \sim 1.9\ 10^{13}\ cm^{-2}$	$l \sim 20\ nm$
Hosoda	$\mu \sim 1200\ cm^2\ V^{-1}s^{-1}, n_s \sim 1.8\ 10^{13}\ cm^{-2}$	$l \sim 20\ nm$

Table C.1 Determination of the mean free path of samples found in literature

The devices that are studied are following the design by Eerkes, but with a move to attain high mobility with the technique of Huijben *et al.* As such, the mean free path is expected to be lower than or equal to 2μm. As such, we may assume the mean free path to be of the order of a micrometer and assume the transport through a ≥ 30 μm wide, 400 μm long device to be in the diffusive regime.

C.2 FORMULAS IN DIFFUSIVE 2D TRANSPORT

This section is a categorized list of formulas in 2D transport, that serves the purpose of a quick reference while reading this thesis. The formulas were extracted from several text books and papers, Refs. [28,30,79,87,93].

BASIC FORMULAS IN 2D TRANSPORT

2D Drude conductivity of metals

$$\sigma = \rho_{xx}^{-1} = \frac{n_s e^2 \tau}{m^*},$$

Mobility of charge carriers

$$\mu = \frac{e\tau}{m^*}.$$

Hall signal for a single-band conductor

$$\frac{d\rho_{xy}}{dB} = -\frac{1}{n_s e}.$$

Carrier density and mobility in terms of experimentally measured values

$$n_s = \frac{I}{e}\left(\frac{dV_H}{dB}\right)^{-1}$$

$$\mu = \frac{L}{W}\frac{1}{V_L}\frac{dV_H}{dB}$$

Einstein relation

$$\sigma = eDg_{2D}(E_F),$$

Diffusion constant

$$D = \int_0^\infty \langle v(0)v_F(t)\rangle dt = \frac{1}{2}v_F l$$

Classical magnetoresistance

$$\frac{\rho_{xx}(B) - \rho_{xx}(0)}{\rho_{xx}(0)} = (\mu B)^2$$

Boltzmann equation in the relaxation time approximation

$$\frac{\partial g}{\partial t} + \mathbf{v}\cdot\frac{\partial}{\partial \mathbf{r}}g + \mathbf{F}\cdot\frac{1}{\hbar}\frac{\partial}{\partial \mathbf{k}}g = \frac{g_0 dt}{\tau}$$

DISPERSION RELATIONS AND ENERGY

Density of states

$$g_{2D}(E) = \frac{dn_s}{dE}$$

Density of states of a parabolic 2D band with effective mass m^*

$$g_{2D} = \frac{m^*}{\pi\hbar}.$$

Fermi energy of a parabolic band

$$E_F = \frac{\hbar k_F^2}{m^*}$$

Fermi velocity of a parabolic band

$$v_F = \hbar k_F / m^*$$

Fermi wave vector

$$k_F = \sqrt{2\pi n_s}$$

Effective mass

$$m^{*-1} = \frac{\partial^2 E}{\partial k^2},$$

MULTI-BAND CONDUCTIVITY

Drude conductivity for two contributing bands

$$\sigma_{xx} = e(n_1\mu_1 + n_2\mu_2) = e\sum_i n_i\mu_i.$$

The resistivity for two contributing bands

$$\rho_{xx}^{-1} = \frac{1}{en_1\mu_1} + \frac{1}{en_2\mu_2} = \frac{1}{e}\sum_i \frac{1}{n_i\mu_i}.$$

Hall coefficient for two contributing bands

$$\frac{d\rho_{xy}}{dB} = \pm\frac{1}{e}\frac{n_1\mu_1^2 + n_2\mu_2^2 + (\mu_1\mu_2 B)^2(n_1 + n_2)}{(n_1\mu_1 + n_2\mu_2)^2 + (\mu_1\mu_2 B)^2(n_1 + n_2)^2}.$$

CHARACTERISTIC LENGTH SCALES

Mean free path

$$l = v_F \tau$$

Fermi wavelength

$$\lambda_F = \frac{2\pi}{k_F}\sqrt{\frac{2\pi}{n_s}}$$

Cyclotron radius

$$l_c = \frac{v_F}{\omega_c} = \frac{\hbar}{eB}\sqrt{2\pi n_s}$$

QUANTUM CORRECTIONS TO CONDUCTIVITY

Weak (anti) localization (localization for $\alpha_{WL} = -1/2$, antilocalization for $\alpha_{WL} = 1$)

$$\Delta\sigma = \alpha_{WL}\,\frac{e^2}{\hbar}\ln\frac{\tau_i}{\tau},$$

HLN formula for weak antilocalization in a magnetic field, where ψ is the digamma function

$$\Delta\sigma = -\frac{e^2}{2\pi^2\hbar}\left[\psi\left(\frac{1}{2}+\frac{1}{\tau a}\right) - \psi\left(\frac{1}{2}+\frac{1}{\tau_1 a}\right) + \frac{1}{2}\psi\left(\frac{1}{2}+\frac{1}{\tau_2 a}\right) - \frac{1}{2}\psi\left(\frac{1}{2}+\frac{1}{\tau_3 a}\right)\right]$$

Maekawa-Fukuyama formula, where $\Psi(x) = \ln(x) + \psi(1/2 + 1/x)$

$$\frac{\Delta\sigma(H)}{\sigma(0)} = \Psi\left(\frac{H_i}{H_i + H_{so}}\right) + \frac{1}{2\sqrt{1-\gamma^2}}\Psi\left(\frac{H_i}{H_i + H_{so}(1+\sqrt{1-\gamma^2})}\right) - \frac{1}{2\sqrt{1-\gamma^2}}\Psi\left(\frac{H_i}{H_i + H_{so}(1-\sqrt{1-\gamma^2})}\right)$$

Rashba spin-orbit Hamiltonian

$$H_R = \frac{\alpha}{\hbar}\boldsymbol{\sigma}\cdot\mathbf{p}\times\hat{\mathbf{z}}$$

Rashba spin-orbit coupling strength

$$\alpha = \frac{e\hbar^2}{4m^{*2}c^2}\frac{dV}{dz}$$

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NOMENCLATURE

2DEG	Two-dimensional electron gas
A	Area
AFM	Atomic Force Microscopy
ARPES	Angle-Resolved Photoemission Spectroscopy
Å	Ångström, unit of length (10^{-10} m)
B	Magnetic field
BHF	Buffered hydrofluoric acid solution
C	Capacitance
C_{sq} (C/A)	Capacitance per square, capacitance per unit area
d	Layer thickness
D	Diffusion constant
DFT	Density Functional Theory
DI	De-ionized
e	Elementary charge ($1.602 \cdot 10^{-19}$ J)
eV	Electronvolt, unit of energy ($1.602 \cdot 10^{-19}$ J)
E	Electric field strength
E_0	Energy of the bottom of the lowest subband in the potential well
E_{bend}	Energy associated with the band bending of STO near the LAO-STO interface
E_c	Energy at the bottom of the conduction band
E_F	Fermi energy
E_g	Energy of the band gap
E_i	Energy as a result of a potential buildup in LAO on STO
E_v	Energy of the top of the valence band
E_{vac}	Energy level of the vacuum in band alignments
ϵ_0	Electric permittivity in vacuum ($8.854 \cdot 10^{-12}$ F m^{-1})
ϵ_r	Relative dielectric constant of a material
g_{2D}	Density of states in two dimensions
$\hbar$	Reduced Planck constant ($1.054 \cdot 10^{-34}$ Js)
I	Applied current
J	Current density (current per lateral surface area (3D) or channel width (2D))
k_F	Fermi wave vector
L	Length: parallel dimension in two-dimensional sytems
l	Mean free path of an electron in diffusive transport
LAO	$LaAlO_3$, lanthanum aluminate
LAO-STO	The interface between LAO and STO
L_{ee}	Average free electron-electron distance in a conductor
l_{cyc}	Cyclotron radius of an electron in a magnetic field
λ_F	Fermi wavelength

λ_s	Screening length
m^*	Effective mass of an electron in a solid
m_e	Electron mass
MBE	Molecular Beam Epitaxy
μ	Mobility or chemical potential
n_s	Sheet carrier density
P	Polarization density
PLD	Pulsed Laser Deposition
Pt	Platinum
RHEED	Reflection High Energy Electron Diffraction
ρ	Resistivity
SCO	$SrCuO_2$, strontium cuprate
SO	Spin-orbit coupling
STEM	Scanning Tunneling Electron Microscopy
STO	$SrTiO_3$, strontium titanate
σ	Conductivity
T	Temperature
τ	Relaxation time from the Boltzmann equation in relaxation time approximation
τ_e	Elastic relaxation time
τ_i	Inelastic relaxation time
τ_φ	Phase-breaking relaxation time
uc	Unit cell of a solid state lattice
v_F	Fermi velocity
V	Voltage
V_{BG}	Back-gate voltage
V_L	Longitudinal voltage
V_G	Gate voltage
V_H	Hall voltage
V_{TG}	Top-gate voltage
W	Width: lateral dimension in two-dimensional transport systems
W_0	Width of the confinement potential well at energy E_0
ϕ	Electrostatic potential
Φ_b	Schottky barrier
Φ_m	Work function of a metal m
Φ_{CNL}	Energy level of the charge neutrality layer
YBCO	$YBa_2Cu_3O_7$, yttrium barium copper oxide
χ	Electron affinity
$\langle z \rangle$	Expectation value of the spatial extent of the wave function in z-direction, center-of-mass of the wave function
Ω	Ohm, unit of resistance
ω_c	Cyclotron frequency

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