Superconductivity in **Ge/Si** core-shell nanowire quantum dots.

Applied Physics Bachelor Thesis
June 24, 2015
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Abstract

Superconductivity through semiconducting nanowires can open up many new possibilities in research of physics. In this project we investigate the effect of different metal contacts on tunnelling supercurrents through a semiconducting Ge/Si core-shell nanowire. The requirements for a tunnelling supercurrent through a semiconducting nanowire are transparent contacts and ballistic transport throughout the nanowire. We made multiple devices and tested aluminium, niobium, palladium and titanium as contacts in different configurations. For samples with contacts of pure niobium, pure aluminium or a stack of palladium, niobium and aluminium; we find high contact resistances and energy barriers at the contact interfaces. In a sample with contacts consisting out of 0.4 nanometers titanium, 15 nanometers palladium and 50 nanometers aluminium; we find low contact resistances and no energy barriers. These properties indicate that a layer of Ti and Pd on top of the nanowire is essential for transparent contacts in our system. With these contacts, this sample seems to meet the requirements and is a promising candidate for a tunnelling supercurrent through Ge/Si core-shell nanowires. Aside from these progressions towards our main goal we have also seen results indicating the possibility of measuring enhanced weak localization in these superconductor to nanowire to superconductor systems. The validity of these measurements needs to be verified.

Acknowledgement

In my first year, when I started studying Applied Physics at the University of Twente, I was immediately brought in contact with the NanoElectronics (NE) group due to a first year students orientation project. I remember having a lot of fun while studying the Aharonov-Bohm effect and meeting people from the research group itself. It was for this reason that the NanoElectronics group was at the top of my list when I went searching for a bachelor assignment at the end of my fourth year of studying. After various introductions into multiple research topics within NE, I stumbled upon the research presented in this thesis. The combination of superconductivity, semiconducting nanowires and quantum dots seemed like an interesting and unique recipe that was completely in line with my interests.
In the first few days of working on my project I came in contact with numerous fun, helpful and intelligent people. The first person I met was of course my daily supervisor Joost Ridderbos. Even though it was a very busy period for him, he always made sure I could ask him questions that helped me gain insight in both theory and experiments. Besides being a good tutor, it was also really fun to work together with Joost on this project. With this project I also became part of the silicon quantum dot team of NanoElectronics. The atmosphere in this team was really good and I had many enjoyable meetings with Floris Zwanenburg, Sergey Amitonov, Matthias Brauns and Chris Spruijtenburg who also helped me out greatly with the experiments if Joost was occupied.

I'd like to thank all of the aforementioned people together with Wilfred van der Wiel and the entire NanoElectronics group for their help and support during my time within NE, making my project both fun and challenging!

Contents

1 Introduction

> *Curiosity is the wick in the candle of learning.*
>
> — **William Arthur Ward**
> (American writer)

Most of science is driven by curiosity. Scientists have a drive to explore and learn about the world around them. The research that will be presented here is a good example of this need for exploration and experimentation. The combination of various concepts of physics into one single device opens up many new possibilities and leads to even better understanding of its underlying parts.
In this research project we will combine semiconductors, superconductors and quantum dots in order to try to create a new type of hybrid device that gives control over single holes as well as Cooper pairs. Even though the research is driven by curiosity, its applications are well worth the effort. It has been shown that superconducting carbon nanotubes can be used to create highly sensitive magnetic sensors called SQUIDs [1]. Using the same principles, this should also be feasible with nanowires as we can build the same type of Josephson junctions with these nanowires. Another interesting application of superconducting nanowires is the possible detection of Majorana fermions, which are particles that are their own antiparticle and are non-Abelian anyons as well [2, 3]. Superconducting nanowires can also be used as a source for entangled particles, as a Cooper pair can be split up into two entangled electrons which can be transported to each a different location [4]. The Majorana fermions and entangled particle sources may seem like applications within science only, they might however be important in the future of computing and communication. Majorana fermions have a theoretical application as a qubit with little environmental influence, leading to a long coherence time [3]. This is due to their non-Abelian anyon properties, where interchanging particles will not only induce a phase change, but will also make the system go into a different state whereas Abelian particles would remain in the same state. Entangled particles can be used as a new type of secure communication [5]. These applications are far ahead of us in the future however, and for this project we will focus on superconductivity through a non-superconducting nanowire.

In order to give a good overview of each relevant aspect we have divided the theory in each of its parts. We will start with discussing the structure and functioning of the Ge/Si core-shell nanowires that will be used. After introducing these nanowires we will go through the key elements in superconductivity and superconductivity through non-superconducting materials. The third part of the theory will let us get familiar with the principles of quantum dots. These quantum dots were not incorporated into our measured devices, but are an important ingredient for future work. After each part of the theory has been discussed, we will look at what happens when we combine these three areas of physics.
As soon as we have described the theory of our system, we will dive into the fabrication

process and measurement procedures. In the experimental aspects and results we will describe and discuss the various samples we created and their relevant properties that were measured. These properties all relate to the ability of supporting a tunnelling supercurrent through the nanowires such as low contact resistance, no energy barriers and high ballistic transport. From these data we will conclude which materials show promising results for achieving superconductivity in our Ge/Si core-shell nanowires and we will give recommendations for adjustments and experiments in future work.

Theoretical aspects

2

2.1 Ge/Si core-shell nanowires

Nanowires are extremely small wires with diameters in the order of 10 to 50 nanometers (10^{-9} m). Due to this very small size, the electronic properties of a nanowire can be approximated by that of a 1-dimensional object. Semiconducting nanowires are promising candidates for the replacement of metal-oxide-semiconductor field-effect-transistors (MOSFETs) [6].

The type of nanowires we are using in our research is a nanowire with a core of germanium and a coaxial shell of silicon. The resulting band structure from this geometry is visible in figure 2.1 and is known as type-II or staggered band alignment. Due to the band alignment between silicon and germanium, the Fermi energy level will be situated in the band gap of the shell and in the valence band of the germanium core. This Fermi level position means that there are unoccupied electron states (holes) available in the valence band of the core, and thus we have a certain concentration of free charge carriers.
The mean free path length of the Ge/Si nanowires is also an interesting and useful property and has been reported to be as high as 540 nm [7]. This means that over distances of about 0.5 μm there will be ballistic transport, which entails that the transport of electrons will have little electrical resistivity due to scattering. In comparison: earlier research in supercurrents through semiconducting nanowires by Kouwenhoven et al. used n-type InAs core-shell nanowires, which have a mean free path of 10 to 100 nanometers [8]. This large mean free path of the Ge/Si nanowires will prove to be a very useful property in the next section where we start to involve superconductivity in these nanowires.

2.1.1 Schottky barriers

When we connect metal contacts to the nanowire, we are in principle creating a Schottky barrier due to the metal-semiconductor interface [9]. This Schottky barrier will introduce band-bending which will change our band alignment in a way that is similar to the band-bending of a p-type semiconductor in contact with a metal which is pictured in figure 2.2. In this picture we have the Schottky barrier height $e\phi_b$, and $e\phi_s - e\phi_m$ is the difference between the work functions of the semiconductor and the metal. We can see that close to the interface there is an energy barrier due to the band banding when the Fermi energy levels are lining up in both materials. If we apply a negative gate voltage over the Schottky barrier we lift the valence and conduction bands in the bulk semiconductor upwards in the energy diagram while keeping the valence and conductance bands energy levels at the interface fixed. As the Fermi level will remain constant, this gate voltage will result in more available states in the valence band and a smaller energy barrier as the slope of the valence band over the distance W will increase.

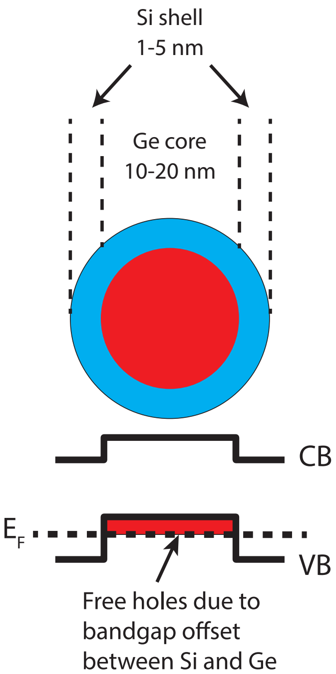


Fig. 2.1: Illustration of the band structure of a Ge/Si core-shell nanowire. The ~500 mV offset between the valence bands of Germanium and Silicon gives an intrinsic free holes concentration in the Germanium valence band [10].

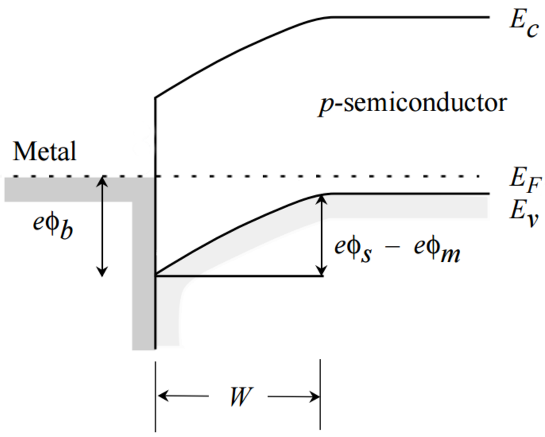


Fig. 2.2: Band bending for an metal to p-type semiconductor interface at no applied bias. Edited from source Singh [11].

As in practice the actual band alignment may differ from nanowire to nanowire due to impurities and even more from different types of contact materials with different work functions, we can actually have the Fermi level in the band gap of the nanowire at zero applied gate voltage. This means that at temperatures close to 0 Kelvin there will be no conductance through the nanowire. At higher temperatures however (such as room temperature) the Fermi-Dirac distribution changes from being a sharp step function, with the step positioned at the Fermi energy, into a wider distribution. This broadening of the Fermi-Dirac distribution creates unoccupied available states within the valence band resulting in finite conductance.

2.2 Superconductivity

Superconductivity is the name of the phenomenon where a material can conduct a current with zero resistance. In 1957 a theory of superconductivity was published by J. Bardeen, L.N. Cooper and J.R. Schrieffer which attributed the existence of superconductivity to attractive interaction between electrons due to virtual exchange of phonons when the energy difference between electron states is smaller than the phonon energy $\hbar\omega$ [12]. When this attractive force dominates it will be favourable for the electrons to form pairs of opposite spin. These pairs of electrons are the so called Cooper pairs. Cooper pairs are capable of moving through a material without scattering by the lattice which translates to the material

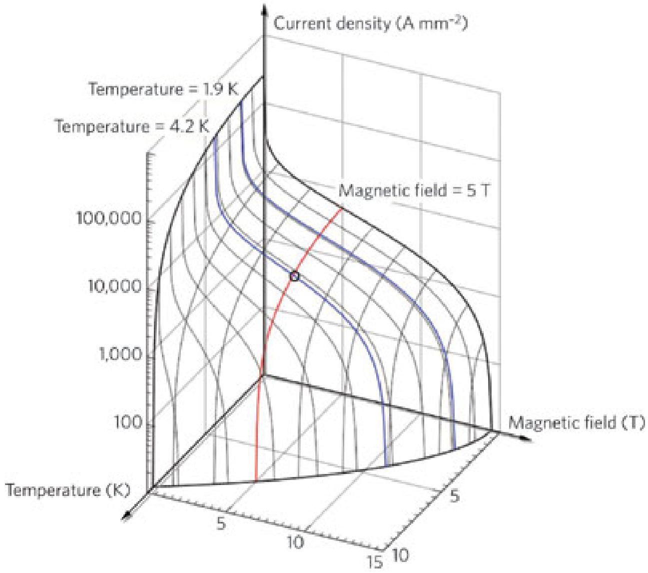


Fig. 2.3: The relation between the current density, the applied magnetic field and the temperature of a superconductor (NbTi) and it's superconducting state. Below the surface the material will be superconducting, above the surface it will return to normal conductance. Image taken from Brüning and Collier [13].

having zero electrical resistance in it's superconducting state. In a more practical approach this means that when a current is sourced through a superconducting wire, there will be a zero voltage drop over the wire as given by Ohm's law ($U = I \cdot R$, where $R = 0$). The current that is sourced should not be too high however. Each superconductor has a certain critical current, as well as a critical temperature and critical applied magnetic field above which it will stop superconducting. These three properties form a surface as can be seen in figure 2.3 under which the material is superconducting and above which the material returns to normal conduction. The physical origin of these critical values are beyond the scope of this project.

Together with the forming of Cooper pair comes the creation of an energy gap as can be seen in figure 2.4. This energy gap is centred around the Fermi energy within the superconductor and goes from $E_F - \Delta$ to $E_F + \Delta$. Inside the energy gap only Cooper pairs are allowed, and single electrons and holes reside in the bands above and below the energy gap.

2.2.1 Josephson junctions

When a non-superconducting material is placed between two superconducting leads, such as in figure 2.4, a Josephson junction is created. When the distance between the two superconducting leads is small enough, a supercurrent will be able to tunnel from one superconducting lead through the non-superconducting material to the other superconducting lead. The size of this supercurrent will be determined by the phase difference between the two superconducting leads and is determined by

$$I_s = I_c \sin(\phi) \quad (2.1)$$

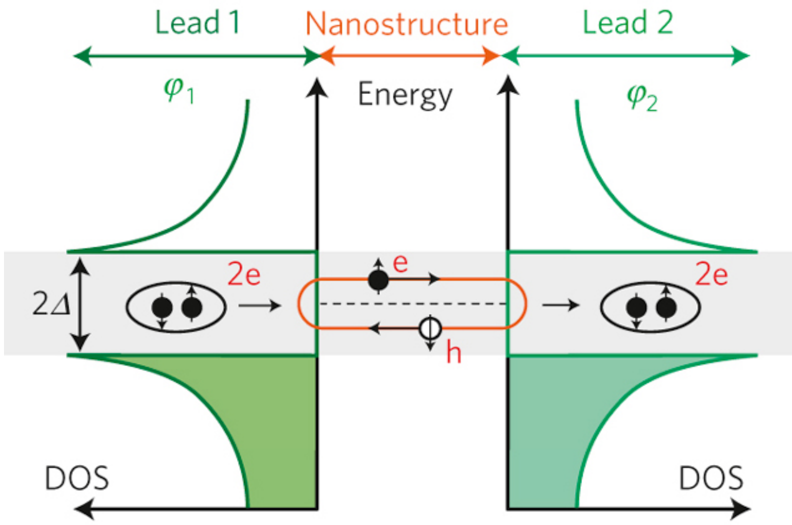


Fig. 2.4: Schematic illustration of a junction of two superconducting leads with a nanostructure in between. The superconductors have respective phases $\phi_{1,2}$ and an energy gap of 2Δ. Image taken from Pillet et al. [15].

Here I_s is the supercurrent through the superconductor-normal conductor-superconductor (S-N-S) system, I_c is the critical current of the superconductor and ϕ is the phase difference between the two superconductors [14]. The critical current is determined by

$$I_c R_n = \frac{2\Delta}{e} \tag{2.2}$$

Where R_n is the normal state conductance, Δ is the superconducting gap and e is the elementary charge. The sine term from equation 2.1 can become negative if $\pi < \phi < 2\pi$. This means that through adjusting the phase difference between the superconducting leads we can actually reverse the direction of the supercurrent. More about this supercurrent reversal will be discussed in section 2.4.

2.2.2 Andreev reflection

When Cooper pairs tunnel through an S-N (superconductor to normal conductor) interface they use a process called Andreev reflection [14]. This process is illustrated in figure 2.4. During this process an incoming Cooper pair is split into two single electrons. One electron travels through the normal conductor and the other electron combines with a hole in the normal conductor. This process makes sure there is conservation of charge, energy and momentum [14]. When the electron in the normal conductor has an energy $E_F + \epsilon$ there will be a difference in momentum between the hole and the electron of $\Delta k = \frac{2\epsilon}{\hbar \nu_F}$. This difference in momentum will lead to a difference in phase between the hole and the electron. When this difference in phase exceeds π the the electron and hole will switch from being in-phase to out-of-phase. From this we can derive a length over which the electron and hole remain phase coherent:

$$L = \frac{\pi}{\Delta k} = \frac{h\nu_{F,N}}{4\epsilon} \tag{2.3}$$

Where $\nu_{F,N}$ is the Fermi velocity of the electron in the normal conductor. When we consider the size of the superconducting gap Δ as the maximum excess energy ϵ at which Andreev reflection takes place, we can define a phase coherence length in the ballistic regime:

$$\xi_{N,C} = \frac{h\nu_{F,N}}{4\Delta} \tag{2.4}$$

Or in the case of a diffusive interface:

$$\xi_{N,D} = \sqrt{\frac{h}{4\Delta}\nu_{F,N}l_e} = \sqrt{\xi_{N,C}l_e} \tag{2.5}$$

Where l_e is the mean free path of the electrons in the normal conductor. If the phase coherence length is exceeded, superconductivity will be lost [14].

Weak localization

At a diffusive N-S interface region in the situation where the phase coherence length ξ_N is much greater than the mean free path l_e, we can have quantum interference effects which lead to increased probability for backscattering via closed time-reversed trajectories[14]. This backscattering (by which the electron waves do partially not reach the N-S interface) will result in a decrease in normal state conductance. This effect is called weak localization. Weak localization can however easily be evaded by applying a small magnetic field, which breaks the time-reversibility of the electron trajectory and thus decreases the amount of backscattering.
An even more interesting case of this situation is when the interface between normal- and superconductor is nearly completely transparent. Instead of only having the effect of backscattering electrons, we also have backscattering over closed time-reversible trajectories of Andreev reflected holes that are created at the interface. This backscattering of electrons and holes approximately doubles the weak localization decrease in conductance and is called enhanced weak localization. The effects of weak localization and enhanced weak localization are made visible in figures 2.5 and 2.6. Enhanced weak localization can be suppressed by a small applied magnetic field just like common weak localization. It can however also be suppressed by applying a bias voltage. This bias voltage will result in a difference in momentum between the hole and electron as stated in section 2.2.2. The difference in momentum makes sure that the hole scatters differently from the electron. This means that two holes will have a slim to no chance of phase coherent interference, eliminating the enhanced weak localization.

2.2.3 Quasiparticle tunnelling

Having a superconducting gap as seen in figure 2.4 raises an interesting question: what happens when we apply a bias large enough such that the band below the energy gap in superconducting lead 1 lines up with the band above the energy gap in superconducting lead 2? This situation is illustrated in figure 2.7. In this figure we can see from three different energy configurations the resulting current in figure 2.7D. Under zero applied bias voltage and a sourced current that is below the superconductor's critical current, we will have Cooper

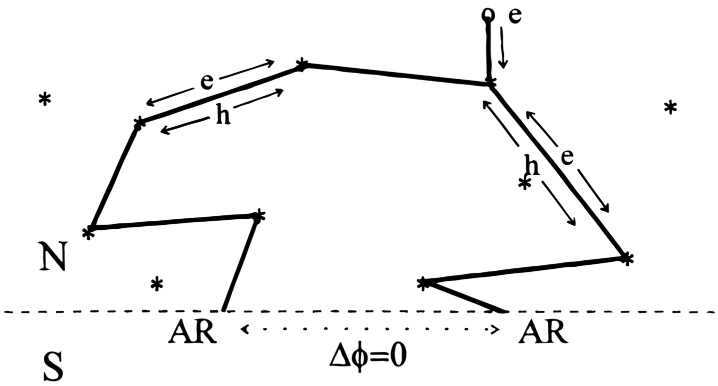


Fig. 2.5: The effects of weak localization and enhanced weak localization made illustratively visible. The asterisks represent scattering sites. Weak localization takes place in the case where only electrons suffer from backscattering, whereas enhanced weak localization takes place when both electrons and holes get backscattered. Image taken from Harmans [14].

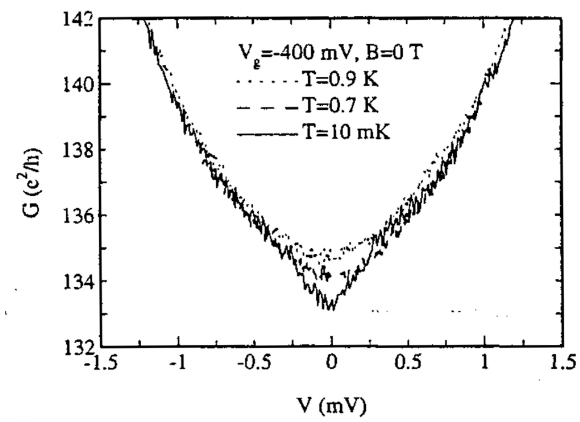


Fig. 2.6: The resulting dip in conductance from enhanced weak localization. Measured in a Sn ($T_c = 3.722K$ [16]) contact to a GaAs-AlGaAs heterostructure. The dip is visible around zero voltage bias and disappears for higher voltages and temperatures. Image taken from Harmans [14].

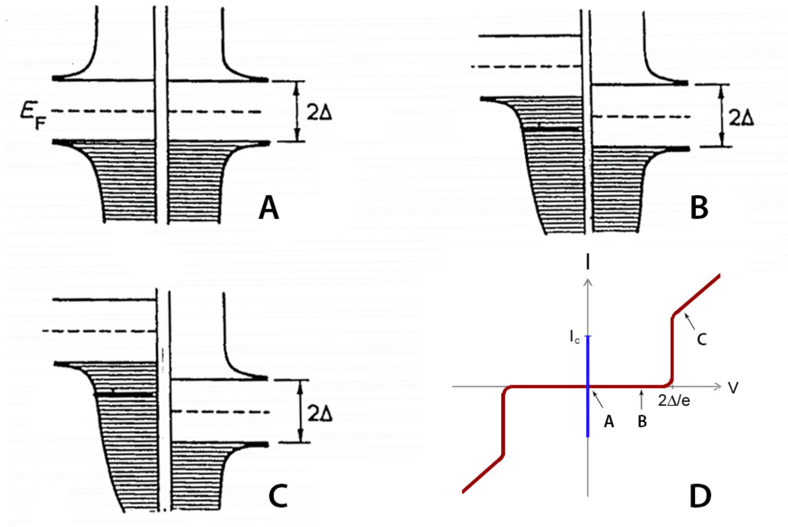


Fig. 2.7: Different stages of applied bias voltage over two superconducting leads with an insulator in between. **A.** Zero applied bias voltage. **B.** Applied bias voltage of greater than zero but smaller than $2\Delta/e$. **C.** Applied bias voltage greater than $2\Delta/e$. **D.** Illustrative resulting I-V curve with the situations sketched in A. to C. indicated. The blue curve corresponds to Cooper pair tunnelling, the red curve corresponds to quasiparticle tunnelling. Edited from source Harmans [14].

pair tunnelling and the resulting I-V curve will be the blue curve found in figure 2.7D. If we however apply a voltage bias instead of sourcing a current we get situations B or C depending on the applied voltage. We then have quasiparticle tunnelling and the resulting I-V curve is the red curve visible in figure 2.7D. Here it is well visible that the quasiparticle tunnelling current starts as soon as the applied voltage is greater than $2\Delta/e$.
The quasiparticles we speak of are simply electrons or holes tunnelling from the bands above and below the superconducting gap. The reason for referring to these particles as quasiparticles is due to their interaction with their surroundings. Due to effects like coulomb interaction between electrons in the superconductor, the effective mass of the electrons is altered for example. This makes their behaviour slightly different from ordinary (free) electrons [16].

This quasiparticle tunnelling process illustrates the difference between voltage and current sourcing nicely. When sourcing a current, Cooper pair tunnelling is possible as long as one remains below the critical current. Once the critical current is exceeded the system will switch to quasiparticle tunnelling. When a voltage bias is applied instead of sourcing a current we can only get quasiparticle tunnelling and there will be no supercurrent.

2.3 Quantum dots

The still ongoing miniaturization of solid state devices has allowed us to scale the size of transistor features from 10 μm to ~30 nm over the course of 30 years [17]. With current electron beam lithography equipment, features below 10 nm have been achieved [18]. These extremely small devices do not only allow us to create faster electronics, but also grant us

the power to explore physics in the realm of quantum mechanics.
One type of these small devices is a quantum dot. Quantum dots are typically artificial structures defined in a semiconductor material with sizes ranging from nanometers to a few microns [19]. Due to the charge binding to the nuclei in semiconductors, the actual free electrons in these regions may go from one single electron to several thousands.

A typical quantum dot device is shown in figure 2.8. In this device the electrons are already confined in two dimensions due to the one-dimensional silicon structure, such as a nanowire. The electrons are confined in the third dimension by the introduction of energy barriers created by top or bottom gates. When we apply source and drain contacts to the edges of the silicon structure we are able to control the current flow through the quantum dot by varying the source-drain, top-gate and/or back-gate voltages.
As can be seen on the right side of figure 2.8, the inside of the quantum dot exists out of multiple energy levels. These energy levels correspond to the discrete energy spectrum found in a 1-dimensional particle in a box system.
In order to let one electron on or off the dot, we need to properly align the source, drain and dot-state energy levels as is shown in figure 2.9. This figure represents the current flow control of a quantum dot at low temperatures. At higher temperatures the thermal fluctuations will allow the electrons to jump from lower occupied states to higher unoccupied states and tunnel out of the dot when this state has a higher electrochemical potential than the source or drain reservoir.
If we measure a current and plot this against the applied gate voltage we can see periodicity in the current peaks caused by the tunnelling process. To explain the periodicity we use the Constant Interaction Model. This model assumes that the Coulomb interaction between the electrons is independent of N and is described by the capitance of the dot, C [20]. If we want to add one electron to the dot, we have an addition energy of $E_{add} = e^2/C + \Delta E$, where C is the dot capacitance, e is the elementary charge and ΔE is the energy between two succeeding quantum states. The periodicity in current peaks is then explained by the constant value for the charging energy $E_c = e^2/C$ that has to be added to the system in order to make the next energy level available for the electrons, with after every few electrons a minor offset of ΔE required for the next quantum state.

When measuring a quantum dot it is common practise to sweep the source-drain voltage at different values of gate voltages, while measuring the current. A typical result of these measurements can be seen in figure 2.10. The diamond shaped white regions of zero conductance in this figure are known as Coulomb diamonds. In these regions there are no states within the dot aligned properly with the source and drain in order to make a current flow. It can be seen that the size of the blockade region changes as the gate voltage is adjusted. This is caused by shifting of the energy levels inside the quantum dot, which brings the levels closer or further away to the source or drain electrochemical potential, depending on the change in gate voltage. At the point where the diamond closes, a quantum dot energy level is either aligned with both source and drain electrochemical potentials if $V_{SD} = 0$, or is situated exactly in the middle between these potentials if $V_{SD} > 0$. It is also clearly visible that the diamonds which correspond to electron numbers $N = 2, 6$ and 12 are larger than the others. This is due to the additional amount of energy required for the next electron to occupy the next quantum state as the current energy level is completely filled. These specific numbers are only valid for a two-dimensional disk-shaped quantum dot. The

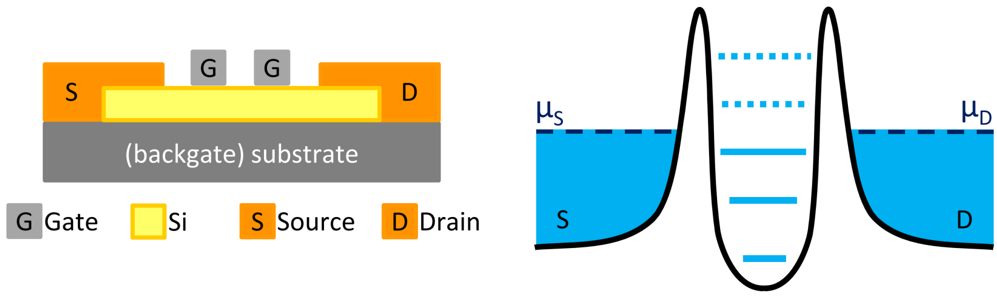


Fig. 2.8: Left: sketch of a quantum dot structure using a 1-dimensional Silicon structure as the material in which the quantum dot is defined. **Right:** The energy landscape corresponding to this structure when a negative voltage is applied to the two top gates and a positive voltage is applied to the back-gate. μ_S and μ_D represent the electrochemical potential of the source and drain respectively. The lines inside the well represent filled electrons states, and the dashed lines represent unoccupied states. Image taken from Zwanenburg et al. [21].

magic numbers for a 1-dimensional quantum dot are unknown to us.
The lines parallel to the diamond edges correspond to the excited states of the electrons. This means that an electron in for example the ground state jumps to the first excited state (or higher). The energy for this jump is in most cases much lower than the addition energy of an electron, and thus it is possible for the electrons already in the dot to occupy these states.

2.4 Super-Semi devices

Now we get to the most interesting part: the combination of Ge/Si core-shell nanowires, superconductors and quantum dots. While quantum dots were not actually integrated into the measured devices, we will discuss the possibilities they open up in this section. We will also review some useful device parameters and how to obtain them from measurement data.

2.4.1 Superconducting semiconductors

In section 2.2.1 we discussed Josephson junctions, in which a non-superconducting material is placed between two superconductors. In our research we used the Ge/Si core-shell nanowires discussed in section 2.1 as the non-superconducting material. Due to the non-superconducting material being a semiconductor, we can include a quantum dot in the system by introducing gates.
In figure 2.11 we can see three regimes that exist in a system consisting out of two superconductors with a quantum dot in between. The first is called strong coupling in which Cooper pairs can tunnel from the source to the drain through a single orbital level on the dot when this level is aligned with E_F of the source and drain. This occurs when the width of the quantum dot energy level Γ is much larger than the superconducting gap Δ and the charging energy E_c. The width of the quantum dot energy level corresponds to the finite lifetime of it's respective energy level, as electrons tunnel into and out of the quantum dot

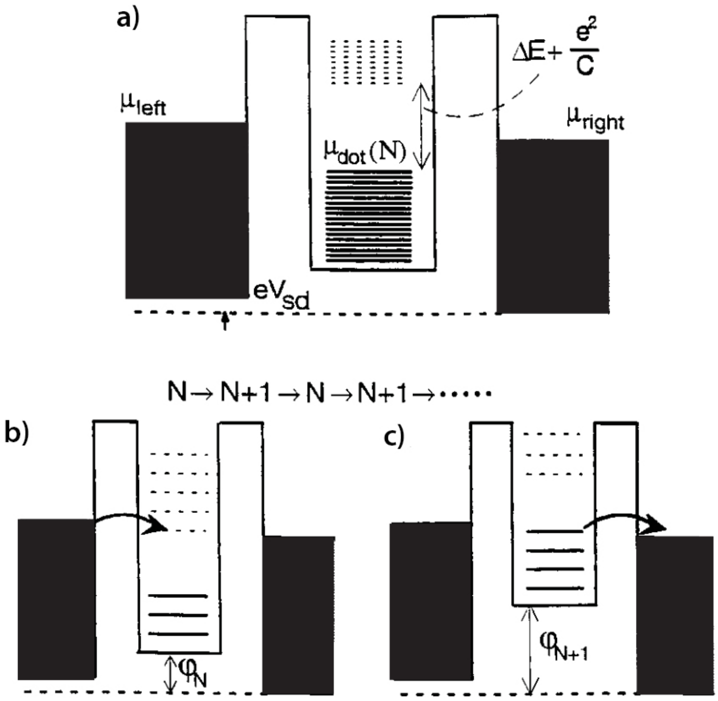


Fig. 2.9: **a)** Quantum dot is filled with N electrons and is at energy level $\mu_{dot}(N)$. There are no available states for the electrons from the source and drain to tunnel to within the quantum dot, and there will be no resulting current. **b)** Due to a positive applied gate voltage, the next energy level is made available to the left reservoir and an electron will tunnel onto the dot. **c)** The electron in the now occupied $\mu_{dot}(N+1)$ state is also able to tunnel to the right reservoir leaving the state unoccupied again. By repeating steps b and c, a current will flow from the left to the right reservoir. Image taken from Kouwenhoven et al. [19].

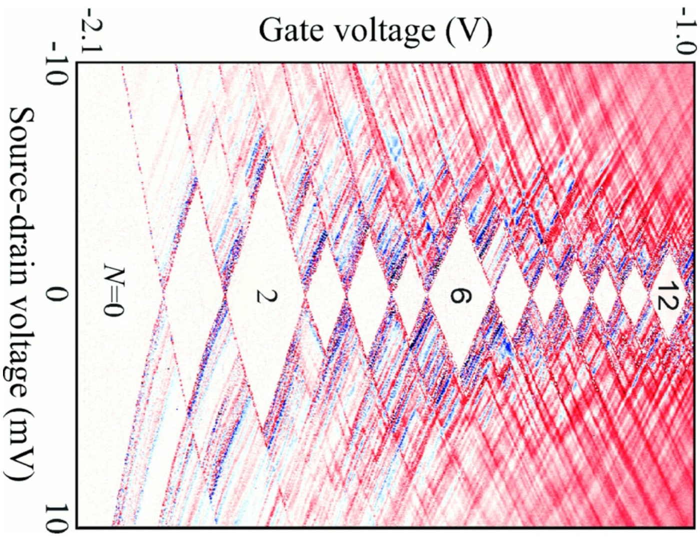


Fig. 2.10: Differential conductance $\partial I/\partial V_{sd}$ plotted in colour scale versus V_g and V_{sd} of a GaAs-based vertical quantum dot at zero magnetic field. The white regions correspond to a differential conductance close to zero. Each diamond shaped white area corresponds to a fixed number (indicated) of electrons within the quantum dots. The lines running parallel to the diamond edges indicate excited states. Image taken from Kouwenhoven et al. [22].

level [4]. The second regime is the weak coupling regime, where only quasiparticles from above the superconducting gap in the source can tunnel to the empty quasiparticle states below the superconducting gap in the drain. As mentioned in section 2.2.3 this requires a minimum voltage difference of $2\Delta/e$. This regime is reached when the width of the quantum dot energy levels is much smaller than Δ and E_c. The third and most complicated regime is the intermediate coupling regime, occurring when the width of the energy levels is comparable to Δ and E_c. Here Cooper pairs can tunnel only under specific conditions from the source to the drain through co-tunnelling. In figure 2.12 we can see two cases of this co-tunnelling process. In the first one where the quantum dot energy level is already occupied by two electrons (or zero) of opposite spin the Cooper pair from the source will go through a co-tunnelling process which results in a Cooper pair in the drain with zero phase difference. If however the state in the quantum dot is filled with an odd number of electrons (such as one), the Cooper pair that has tunnelled from source to drain will experience a phase shift of π. If we now recall equation 2.1 and we insert the phase shift of π as ϕ we obtain a supercurrent of $I_s = -I_c$. This means that the direction of the supercurrent has actually reversed!
Instead of reversing the supercurrent, it is also possible to increase or decrease the critical current as demonstrated in figure 2.13. As we apply a negative voltage to the Ge/Si nanowire we actually increase the carrier density inside the nanowire. This increase of carrier density leads to a decrease in normal state resistance and recalling equation 2.2 this leads to a higher critical current [8, 10].

2.4.2 Determining device properties

One useful characteristic of any solid-state device is the electron or hole mobility. This mobility indicates how strong the electron or hole drift velocity will respond to an applied electric field [16]. We want the mobility in our nanowires to be high, such that we have high ballistic transport. This means that the holes can travel relative long distances before scattering. In order to derive a formula for the mobility we start with

$$\sigma = nq\mu_h \tag{2.6}$$

where σ is the conductivity, n is charge carrier (holes) density, q is the elementary charge and μ_h is the hole mobility. We can also define the conductivity as

$$\sigma = G\frac{L}{\pi r^2} \tag{2.7}$$

which is the conductivity expressed as the conductance multiplied by the device length and divided by the device area. If we combine equations 2.6 and 2.7 and take $n = \frac{Q}{q\pi r^2 L}$ for the carrier density we get

$$\mu_h = \frac{GL^2}{Q} \tag{2.8}$$

with $Q = C_G(V_p - V_g)$ where C_G is the gate capacitance, V_p is the pinch-off voltage and V_g is the gate voltage we get

$$\mu_h = \frac{GL^2}{C_G(V_p - V_g)} \tag{2.9}$$

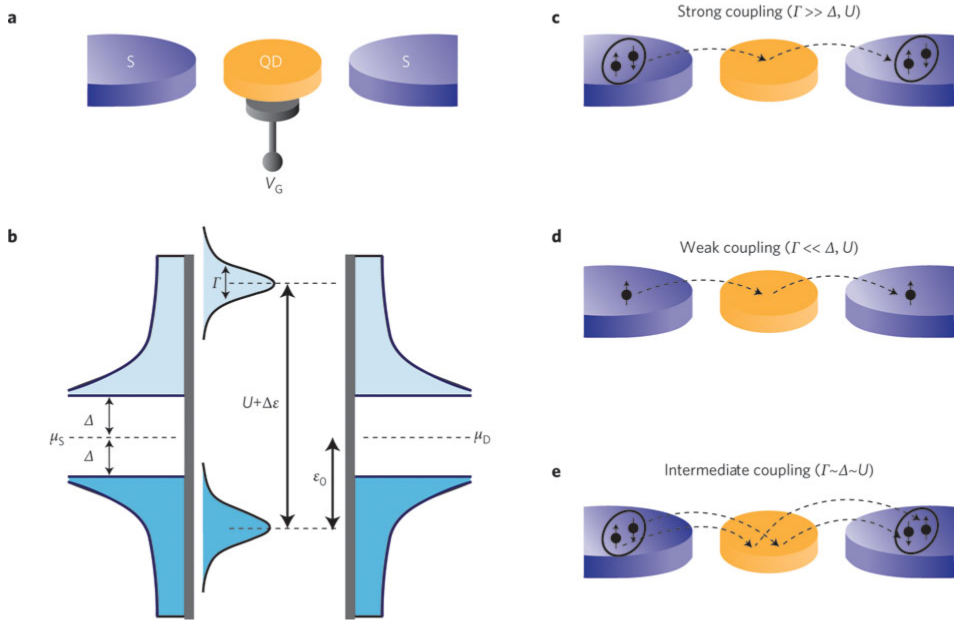


Fig. 2.11: **a)** Illustration of a superconductor to quantum dot to superconductor system. The quantum dot is capacitively coupled to the gate electrode. **b)** Energy diagram of the device in a. μ_S and μ_D are the electrochemical potentials of the source and drain respectively. Δ is the superconducting gap, Γ is the width of the quantum dot level, U is the charging energy E_c, $\Delta\epsilon$ is the spacing between two successive energy levels and ϵ_0 is the energy difference from the highest occupied energy level to the Fermi level of the source and drain at zero voltage bias. **c)** Strong coupling regime. In this regime Cooper pairs tunnel through a single quantum dot energy level from the source to the drain when their Fermi level lines up with the highest occupied energy level. **d)** Weak coupling regime. Only quasiparticle tunnelling (see section 2.2.3) is allowed. **e)** Intermediate coupling regime. Cooper pairs can tunnel from source to drain depending on the configuration of the energy levels. Image taken from De Franceschi et al. [4].

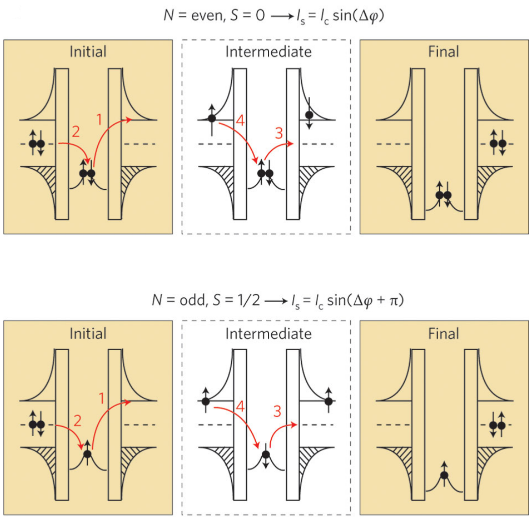


Fig. 2.12: Co-tunnelling process in the intermediate coupling regime for both N = even and N = odd number of electrons. For an even number of electrons we can see that after the process, the Cooper pair is no different from before the process. For an odd number of electrons we can see that the Cooper pair picks up a phase shift of π during the co-tunnelling process. Image taken from De Franceschi et al. [4].

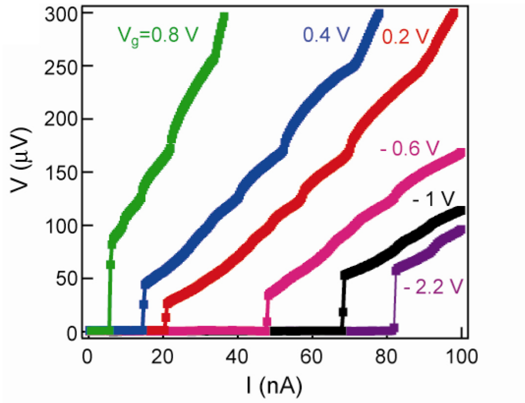


Fig. 2.13: Tunable supercurrent in a Ge/Si core-shell nanowire. Through adjusting the gate voltage the critical current can be controlled. Image taken from Xiang et al. [10].

We can replace $\frac{G}{V_p - V_g}$ by $\frac{\partial G}{\partial V_g}$ if we take $V_g = 0$ resulting in

$$\mu_h = \frac{\partial G}{\partial V_g} \frac{L^2}{C_G} \tag{2.10}$$

We can also replace $\frac{\partial G}{\partial V_g}$ by $\frac{\partial I}{\partial V_g} \frac{1}{V_{sd}}$ which leads to our final equation for the mobility:

$$\mu_h = \frac{\partial I}{\partial V_g} \frac{L^2}{C_G V_{sd}} \tag{2.11}$$

Which is the transconductance multiplied by the device length squared, divided by the gate capacitance times the source drain voltage. The gate capacitance is then calculated using the model of a metal cylinder on an infinite metal plate, and is found to be

$$C_G = \frac{2\pi\epsilon_0\epsilon_r L}{ln(2t/r)} \tag{2.12}$$

where ϵ_0 is the permittivity of vacuum, ϵ_r is the dielectric constant of the material between the nanowire and the back-gate, L is the length of the wire, t is the thickness of the dielectric and r is the radius of the nanowire [23].

Another useful property is the contact resistance of the superconductor to the nanowire. If we want to have a supercurrent tunnelling through the nanowire we need to make sure that the Cooper pairs are able to traverse the S-N-S interfaces without too much trouble. The exact execution of the determination of these contact resistances will be discussed in the next chapter.

Experimental aspects

3

In order to create the devices mentioned in the previous chapter, we have to go through various steps. The nanowires are grown by the Photonics and Semiconductor Nanophysics group from Eindhoven University of Technology. These nanowires have to be deposited and contacted on the sample and then we have to connect our sample to a measuring device. This chapter describes these fabrication steps as well as the measurement procedure.

3.1 Device fabrication process

Ge/Si core-shell nanowires are generally grown using the vapor-liquid-solid mechanism [24]. A gold nanoparticle is used as a catalyst such that the precursor gas (for example silane SiH_4 or germane GeH_4 in their vapour phase) can decompose into pure silicon or germanium respectively. The gold nanoparticle forms a Au-Si alloy droplet as it is placed on a silicon surface. The silicon or the germanium in the precursor gas will be adsorbed into this Au-Si alloy droplet when it is released into the reaction chamber. When the droplet gets saturated with the designated atoms, the material will precipitate and the nanowire is formed. By first executing this process using germanium and afterwards repeating with silicon, a nanowire with a germanium core and a silicon shell is formed.

After the nanowires have been grown, we use photolithography to create the structure seen on the left in figure 3.1. We will be able to connect the large contact pads to our printed circuit board (PCB) and connect their smaller ends to the actual devices. The area between the contacts written with photolithography has a size of ~7 μm by 7 μm. After the photolithography step we use electron-beam lithography (EBL) to write so called bitmarkers on our samples. These bitmarkers can be seen on the right in figure 3.1 and allow us to locate the nanowire positions by a simple bit-like counting system.
After preparing the sample for use, we can deposit the Ge/Si nanowires by using a paper tip. By scraping over the nanowire growth sample with a paper tip the van der Waals force will keep most of the nanowires touched by the paper, stuck to its surface. We can then scrape this paper over the prepared sample to randomly deposit the nanowires on its surface. Using a microscope we can image usable nanowires and locate them using the bitmarkers as seen in figure 3.2.
With the pictures of the nanowires on the sample we can use electron-beam lithography to write structures on top of the nanowires which will form our measurement devices. We have two types of devices: 2-probes, which exist out of 2 contact pads with a distance of 150, 200 or 250 nm in between and 4-probes, which exist out of 2 contact pads and 2 finger-like structures in between them as can be seen in figure 3.3. The different contact distances of the 2-probes allow us to create different channel lengths for our devices. This channel length is important due to the phase coherence length of our system. The main

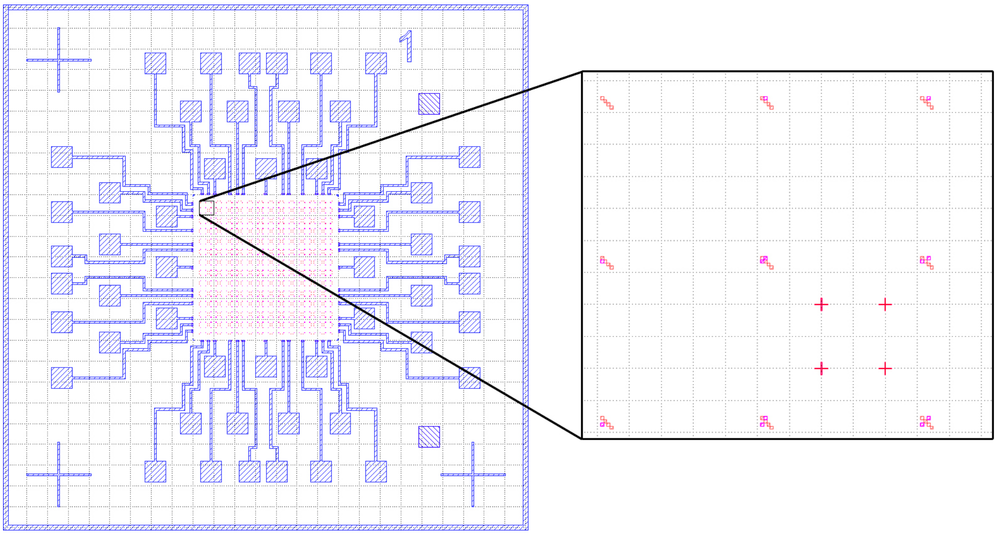


Fig. 3.1: Left: photolithography pattern (blue) with 54 contact pads. The smaller structures (not visible) are the bitmarkers and EBL alignment crosses. **Right:** Blow-up of the first quadrant of the sample existing out of 9 bitmarkers. These bitmarkers are placed 50 μm apart from each other.

difference between 2-probes and 4-probes is that with a 4-probe we can source a current over the outer two contact pads and measure the voltage drop over the inner two contacts. Using this technique we will only measure the actual resistance of the wire, while with a two probe we would measure both the wire resistance and the contact resistance. It is also possible to extract the contact resistance from a 4-probe measurement by calculating the resistance over each of the paths that are available for a current with the four contacts (six in total). When comparing these six resistances we will find a dependence on distance as well as an offset attributable to the contact resistance. As was mentioned in section 2.4.2, we need a small contact resistance (transparent contacts) in order to achieve superconductivity through our nanowires.
When the EBL structures have been written in the resist (polymethyl methacrylate or PMMA) on the sample we can use Electron-beam Physical Vapour Deposition (EBPVD) to evaporate the material onto the sample. With this evaporation technique both the sample and the material sources are placed in a vacuum chamber which is evacuated to a pressure of $10^{-6}\,mbar$. In the vacuum chamber an electron beam will heat up the source material with a power of ~$10\,kW/cm^2$ [25]. The source material will then transition to its gaseous phase and this gas of atoms will expand in the vacuum chamber to cover all surfaces, including the sample. Due to our control over the electron beam's power we can evaporate a controlled layer in the order of angstroms per second on our sample. In the final step we use lift-off in order to obtain our designed structures.

In the last step of making our sample ready for measurement we need to make it compatible with the measurement devices available. In order to do this we mount the sample on a printed circuit board (PCB) and use a wire bonder to connect the sample to the PCB contacts using aluminium wires. The resulting and final device is shown in figure 3.4.

Fig. 3.2: Example of a microscope image after depositing nanowires. Both the nanowire and bitmarkers used for localization are indicated.

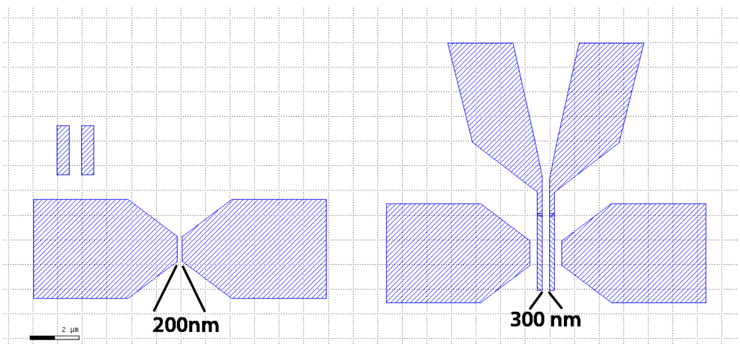


Fig. 3.3: **Left:** 2-probe EBL model (200nm version). **Right:** 4-probe EBL model.

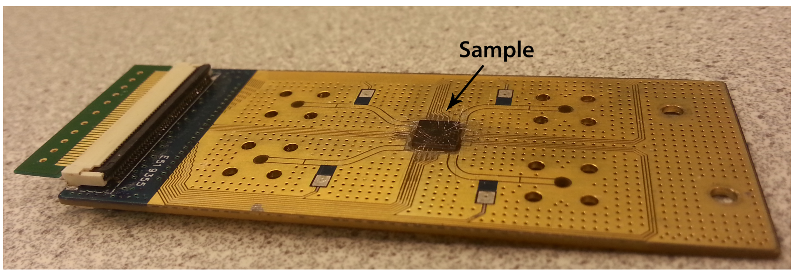


Fig. 3.4: Sample 1L07 mounted and wired to a PCB.

Device name	1A08	1E03	1E04	1F03	1L07
Nanowire batch	H02783	H02220	H02220	H02220	H03138
Material #1	Nb (80 nm)	Nb (80 nm)	Pd (5 nm)	Al (60 nm)	Ti (0.4 nm)
Material #2	N/A	N/A	Nb (60 nm)	N/A	Pd (15 nm)
Material #3	N/A	N/A	Al (5 nm)	N/A	Al (50 nm)

Tab. 3.1: Overview of all measured devices and their relevant properties. If multiple materials are listed for the same sample then these materials are stacked vertically with #1 on the bottom and #3 on top.

3.1.1 Device specifications

The devices we measured all went through the same design procedure where only the evaporated materials differed from each other. In table 3.1 a quick overview of the samples measured before and during this project and their relevant properties is found. The superconducting materials were chosen on basis of their critical temperature, followed by some trial-and-error experiments to see their effects on the contact transparency. Niobium has a critical temperature of 9.5 Kelvin and a superconducting gap of 3.05 meV, and aluminium has a critical temperature of 1.14 Kelvin and a superconducting gap of 0.34 meV [16].
As one can see, samples 1A08 and 1E03 both consisted out of pure niobium. The difference between the two was that the 1A08 sample was treated with a plasma etch in order to remove any unwanted material on the nanowires, so that the contact interfaces would be cleaner. The measurements of this device indicated that this treatment had no effect on the transparency of the contact interfaces when compared to the 1E03 sample. The 1A08 sample is also the only sample with the H02783 nanowire batch. The nanowires have improved in the H02220 batch and even further improved in the latest H03138 batch. These improvements are found in properties such as wire resistivity, the uniformity of the resistivity and mobility.
In table 3.1 it can be seen that instead of only using superconductors as contacts we also use titanium in combination with palladium. Palladium has the advantage that its work function matches very well with that of the Ge/Si nanowire resulting in a low Schottky barrier height [26, 27]. This low Schottky barrier gives transparent contacts which is required for a tunnelling supercurrent. The titanium seems to even further strengthen this effect for reasons that are still unknown to us.

3.2 Measurement procedure

Our measurements consist of three parts: source-drain sweeps, gate-sweeps and a combined source-drain and gate sweep which is called bias spectroscopy. Source-drain sweeps can be done by either sourcing a current or a voltage and measuring the voltage over the wire or current through the wire respectively. The resulting I-V curve gives us information about whether there is superconductivity through the nanowire (only when sourcing a current), whether there is an energy barrier (Schottky, superconducting gap) present in the system and about the size the resistance of the wire (or the system in case of a 2-probe). An example of a source-drain sweep (for sample 1L07) can be found in figure 3.6. From the measured resistance we can calculate the resistivity with

$$\rho = R\frac{A}{l} \tag{3.1}$$

where R is the device's resistance, A is the nanowire cross-sectional area and l is the channel length of the device. We can find the latter two parameters by using a Scanning Electron Microscope image as seen in figure 3.5.

A gate sweep is used to find the pinch-off region of the nanowire and calculate the nanowire's mobility. By applying a fixed source-drain voltage while sweeping the back-gate and measuring the source-drain current we can measure at what back-gate voltage we push the Fermi level out of the germanium valence band, which results in zero current. Using the slope $\partial I_{sd}/\partial V_g$ before the current hits zero (in the pinch-off region) we can determine the mobility of the charge carriers within the nanowire as shown in section 2.4.2. The position of the pinch-off region is used in the combined measurement of voltage source-drain and gate sweeps to conserve time by only measuring regions of interest. An example of a gate sweep (for sample 1L07) can be found in figure 3.7.

A bias spectroscopy is a very useful and powerful tool to see a lot of device features, such as the pinch-off region and energy barriers, in one single graph. For a bias spectroscopy we execute a source-drain sweep at a starting value for the back-gate voltage, which we then repeat for a set number of steps until we reach the end value for the back-gate voltage. By measuring the current in each of these sweeps we can combine these three variables into a plot as seen in the previous chapter's figure 2.10 for a quantum dot. As the result from a bias spectroscopy consists out of many gate sweeps for different source-drain voltages, we can make a good estimate of our nanowire mobility from this measurement.

For the bias spectroscopy as well as for the ordinary source-drain sweep we can instead of plotting the current also plot the conductance by calculating the $\partial I_{sd}/\partial V_{sd}$ for each data point. This proves to be a useful tool in visualizing barriers around zero voltage bias as the conductance, in contrast to the current, is supposed to be constant at zero bias on the left side of the pinch-off region.

We did measurements in a liquid helium dewar (base temperature 4.2 K) using a dipstick and in a dilution refrigerator (base temperature at 15 mK). In all set-ups we use a matrix module and a Delft Electronics IVVI-DAC rack. We used a DAC module to control our set-up through a computer and export measurement data.

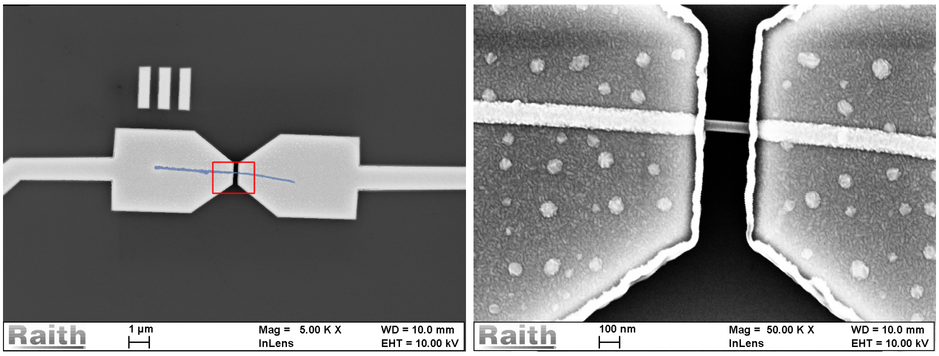


Fig. 3.5: Left: False coloured Scanning Electron Microscope (SEM) image of one of the 2-probe devices of sample 1E03. The three bars in the top indicate that the contacts were designed with 300 nm spacing in between. **Right:** Zoomed SEM image of the region indicated in red in the left image. From this image we can determine the channel length and the device diameter.

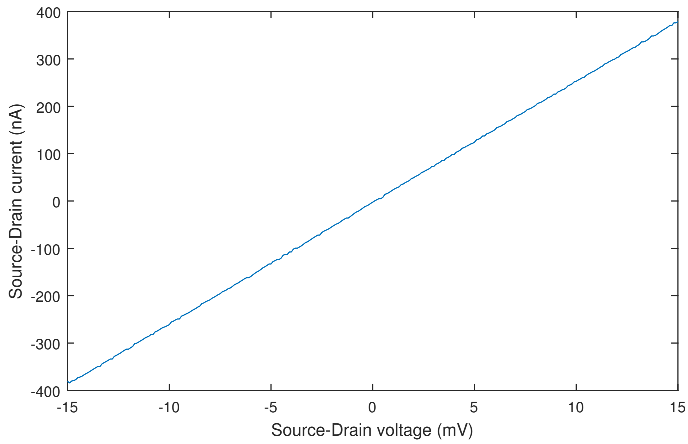


Fig. 3.6: Voltage sourced source-drain sweep at zero back-gate voltage. A linear I-V relation is clearly visible. Sample 1L07, measured at 4.2 K.

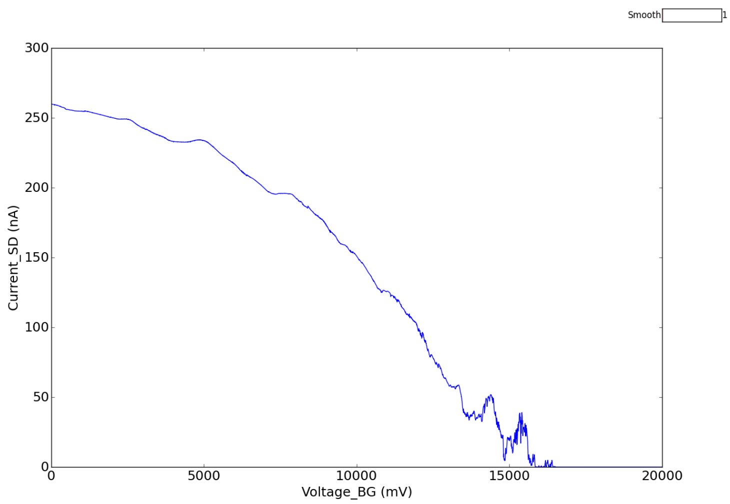


Fig. 3.7: Gate sweep with source-drain voltage of 10 mV. The nanowire is pinched at a back-gate voltage of around 16 Volts. We use the region before this pinch-off voltage to determine the hole mobility in the nanowire. Sample 1L07, measured at 4.2 K.

Results and discussion

4

Here we present the results of our measurements in order to characterize the fabricated samples and discover whether they allow for Cooper pairs to tunnel through the nanowires. We measured sample 1F03 (H02220 nanowires, 60 nm Al) in a liquid helium dewar with a dipstick and in a dilution refrigerator together with sample 1E04 (H02220 nanowires, Pd-Nb-Al (5-60-5 nm)). We measured sample 1L07 (H03138 nanowires, Ti-Pd-Al (0.4-15-50 nm)) in a liquid helium dewar with a dipstick only. We also include some results of earlier measurement performed with sample 1E03 (H02220, 80nm Nb) and 1E04 in a liquid helium dewar in order to compare their relevant data. In the measurements we used a current sourced source-drain sweep to see whether we have a tunnelling supercurrent, and a voltage sourced source-drain sweep to discover relevant I-V characteristics such as barriers and resistances. Gate sweeps were used to discover the pinch-off region for each wire and bias spectroscopies were used to calculate mobilities from the pinch-off region for multiple source-drain voltage values.

4.1 Source-drain sweeps and nanowire resistances

During this project we performed source-drain sweep measurements of samples 1F03 (Al) and 1L07 (Ti-Pd-Al) at 4.2 Kelvin and of samples 1E04 (Pd-Al-Nb) and 1F03 at 15 mK base temperature. In earlier measurements we measured 1E04 and 1E03 (Nb) at 4.2 Kelvin as well. In figure 4.1 A to C we find the results of voltage sourced source-drain sweeps performed at 4.2 Kelvin for samples 1E04, 1L07 and 1F03. The first thing we notice is that samples 1E04 and 1F03 show signs of a barrier around zero bias voltage, whereas sample 1L07 has a completely linear I-V relation. Other devices of samples 1E04 and 1F03 also had this energy barrier in their source-drain measurements, and only one device of 1L07 showed signs of an energy barrier. When we performed current-sourced measurements below the critical temperature of samples 1E04, 1E03 and 1F03 we also saw this barrier, and no supercurrent.
From the results of the source-drain measurements we can calculate the resistance of the devices and, if we have the channel length and diameter of the devices through SEM imaging, we can also calculate the resistivity. The exact wire resistance and contact resistances can only be determined by measurements using 4-probes, which require nanowires longer than 900 nm. For devices that had an energy barrier around zero voltage bias we calculated the resistance from the linear part on the positive voltage side, this value differed often only slightly from the negative side. The results for the resistance calculations can be found in table 4.1 and for the samples of which we have determined the nanowire diameters and channel lengths, the resistivity can be found in table 4.2.
In table 4.1 we can see that the 1L07 device (which uses the H03138 nanowire batch) has much smaller resistances than the other three devices (which use the older H02220 nanowire

Resistance ($k\Omega$)	NW1	NW2	NW3	NW4	NW5	NW6	NW7
1L07	110,7	39,1	20,2	23,7	20,0	47,8	38,5
1F03	2,33·10^6	158,6 (BG -15V)	1,90·10^3 (BG -15V)	897,4 (BG -10V)	1,36·10^3 (BG -10V)	-	-
1E04	351,4	270,9	-	-	-	-	-
1E03	477,8	462,5	529,1	6,74·10^3	-	-	-

Tab. 4.1: Resistances for various nanowires (arbitrary numbering) of samples 1L07, 1F03, 1E04 and 1E03 measured at 4.2 K base temperature. Of the 1F03 sample, most nanowires were measured with an applied back-gate voltage as these wires were pinched at zero back-gate voltage.

Resistivity ($k\Omega \cdot nm$)	NW1	NW2	NW3	NW4	NW5	NW6
1F03	-	-	8,55· 10^3	9,70· 10^3	3,91· 10^4	5,40· 10^3
1E03	7,09· 10^3	2,80· 10^3	-	-	-	-
1E04	8,66· 10^3	4,43· 10^3	5,45· 10^3	-	-	-

Tab. 4.2: Resistivity for various nanowires (matching numbering of tables 4.1 and 4.3) of samples 1F03, 1E03 and 1E04 measured at 4.2 K base temperature. All these samples use the same nanowire batch H02220. Sample 1L07 not included due to unknown channel lengths and nanowire diameters.

batch). These resistances do not say very much about the nanowires, as their channel lengths and diameters may differ greatly. The order of magnitude difference between the 1L07 sample and the others however, is a good indication of more transparent contacts and improved nanowires. When we look at the resistivity of the 1F03, 1E03 and 1E04 samples we can see that they are all in the same order of magnitude. This indicates that the different type of contact materials with which they were fabricated had little influence on the total resistance of the system.

Nanowires 2,3,4 and 5 of the 1F03 sample were measured with an applied negative back-gate voltage. This was due to the nanowires otherwise being in pinch-off region, as will be shown in the next section, which gave resistances that were not representative of the actual nanowire resistances.

Of all the measured samples, we only had one working 4-probe on the 1L07 sample. The data from this device lets us calculate a contact resistance of ~8 $k\Omega$ and a nanowire resistance of ~8.5 $k\Omega$ over an interval of 300 nanometer. We included the fact that this contact resistance and nanowire resistance are almost equal into our calculations, as this meant that the contact in between the two contacts through which is measured has a resistance in parallel with that of the nanowire. This inclusion gave us the mentioned values of the contact and nanowire resistances.

Mobility ($cm^2/V \cdot s$)	NW1	NW2	NW3	NW4	NW6	NW7	NW8
1L07	-	136,4 $\pm$ 6,79	-	-	79,6 $\pm$ 3,90	-	-
1F03	7,53 $\pm$ 1,47	-	1,05 $\pm$ 0,05	1,12 $\pm$ 0,07	-	0,06 $\pm$ 0,18	0,05 $\pm$ 0,35

Tab. 4.3: Mobilities for various nanowires (matching numbering to table 4.1) of samples 1L07 and 1F03 measured at 4.2 K base temperature. Of the 1L07, most wires did not pinch-off within the safe range for the back-gate voltage and so no mobilities could be calculated of these wires. The errors were taken from the standard deviation of the mobility values for the various gate-sweeps.

4.2 Bias spectroscopies and nanowire mobilities

It has been mentioned in the previous section that some of the nanowires of the 1F03 sample were measured with a negative back-gate voltage applied, as they would have been in pinch-off region otherwise. In figure 4.2 A to C we can see a series of bias spectroscopies for the same nanowires of samples 1E04, 1L07 and 1F03 as the source-drain plots. Here we plotted the back-gate voltage on the x-axis, the applied source-drain voltage on the y-axis and plotted the conductance as a colour scale. In the graph for the 1F03 sample we can clearly see the region of zero conductance for all source-drain voltages (black colour) come into existence from $V_{BG} = -6V$ up to more positive voltages of the back-gate. This means that as stated before, at zero applied back-gate voltage the nanowire is completely pinched off. All other measured samples did not show this behaviour.
In the bias spectroscopy graphs we can also see the barriers around zero source-drain voltage for sample 1E04 and 1F03, which seem to be independent of the applied back-gate voltage (up to -10 and -20 Volts respectively). In the bias spectroscopy graph of the 1L07 sample we see the non-zero constant positive conductance for each source-drain sweep outside of the pinch-off region which becomes larger for more negative back-gate voltage due to accumulation of holes in the nanowire.
From these bias spectroscopy data we can extract mobilities for nanowires of each sample. These values of the mobility can be found in table 4.3. We have not been able to calculate any mobilities for the 1E03 and 1E04 samples, as there were no bias spectroscopies performed for the 1E03 sample and the 1E04 sample did not pinch-off within safe ranges of the back-gate voltage. Of the 1L07 sample only 2 nanowires have shown pinch-off.
From the limited set of data it seems that the 1L07 samples have a much higher mobility than that of the 1F03 sample. It should be noted however that the channel length and diameter of the 1L07 sample were not known. Their mobility has been calculated with an approximated diameter of 30 nm and a channel length equal to the 2- and 4-probe design contact distances.

4.3 Conductance measurements

Inside the dilution refrigerator, which brought our samples 1E04 and 1F03 to a base temperature of 15 mK, we performed a lock-in measurement with sample 1E04. In this lock-in measurement we combined a DC source-drain voltage with a smaller AC voltage. By measuring the change in current in response to the AC voltage we can directly extract the conductance $\partial I/\partial V$ of our nanowire from these data, instead of having to numerically approach the conductance. The result of this lock-in measurement, performed with a back-gate voltage of -2 V, is visible in figure 4.3 B. In figure 4.3 A we see the expected features of this conductance vs. source-drain voltage plot as seen in InAs-Al nanowires at multiple temperatures by Chang et al. [28]. In figure 4.3 C we see the conductance determined numerically from a source-drain sweep at 4.2 Kelvin and a back-gate voltage of -2 V. We see that the gap in conductance becomes wider with this higher temperature, and we also see the minor extra dip around zero source-drain voltage has disappeared. This extra dip in conductance was also not seen in the measurement in figure 4.3 A. The large peaks just before the gap in this figure, caused by turn-on of quasiparticle tunnelling, do seem to be missing in our measurements, while our base temperature was at 15 mK which is below the critical temperature and below the lowest displayed temperature in figure 4.3 A.

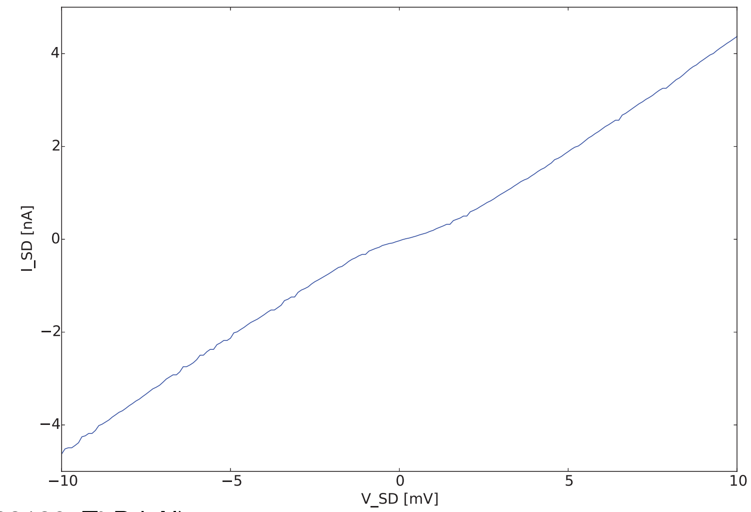
4.4 Discussion

4.4.1 Barriers

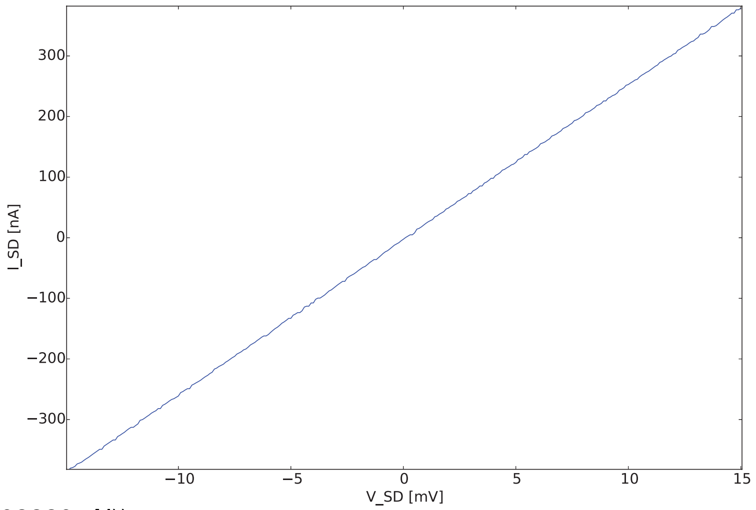
The first apparent result of the previous experiments is that no superconductivity has been achieved. We measured all samples except 1L07 (Ti-Pd-Al) below their respective superconductor's critical temperatures with no visible supercurrent. In all of these devices we noticed an energy barrier around zero applied source-drain voltage bias. This barrier can be caused by a Schottky barrier, by the superconducting gap or by being too close to pinch-off with the back-gate voltage. The exact height and width of a Schottky barrier is dependent on the band structure of both the metal, the semiconductor and the interface between the two. As these band structures can vary due to defects and fabrication imperfections, the exact size of the barrier is not very constant and predictable. The Schottky barrier can however be engineered into being very small by matching work functions of the metals and semiconductors used. This will make the band bending at the interface decrease in size and thus offer more transparent contacts. When we compare the results of 1F03, 1E04 and 1L07 we seem to have been successful in creating these transparent contacts in the 1L07 sample, where the combination of aluminium, palladium and a small layer of titanium showed no visible signs of an energy barrier. It seems that the combination of titanium and palladium is the cause of the transparent contacts, as combinations of palladium and aluminium did not have this contact transparency (sample 1E04).

The superconducting gap can also be a cause of a visible barrier. As mentioned in section 2.2.3, the superconducting gap (Δ) adjusts the density of states in such a way that around the Fermi energy ($E_F \pm \Delta$) there are no states available for holes and electrons. In order to

A) 1E04 (H02220, Pd-Nb-Al)



B) 1L07 (H03138, Ti-Pd-Al)



C) 1F03 (H02220, Al))

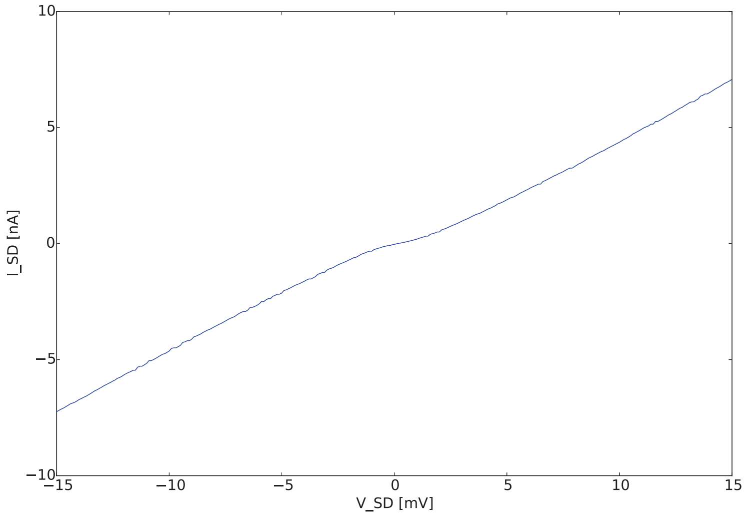


Fig. 4.1: Voltage sourced source-drain sweeps for samples 1E04 (A), 1L07 (B) and 1F03 (C). For the 1F03 sample we set the back-gate to a voltage of -15 V, in order to measure outside of the pinch-off region. In samples 1F03 and 1E04 we clearly see an energy barrier around zero bias, whereas the I-V relation of sample 1L07 is completely linear. Taken at base temperature of 4.2 Kelvin

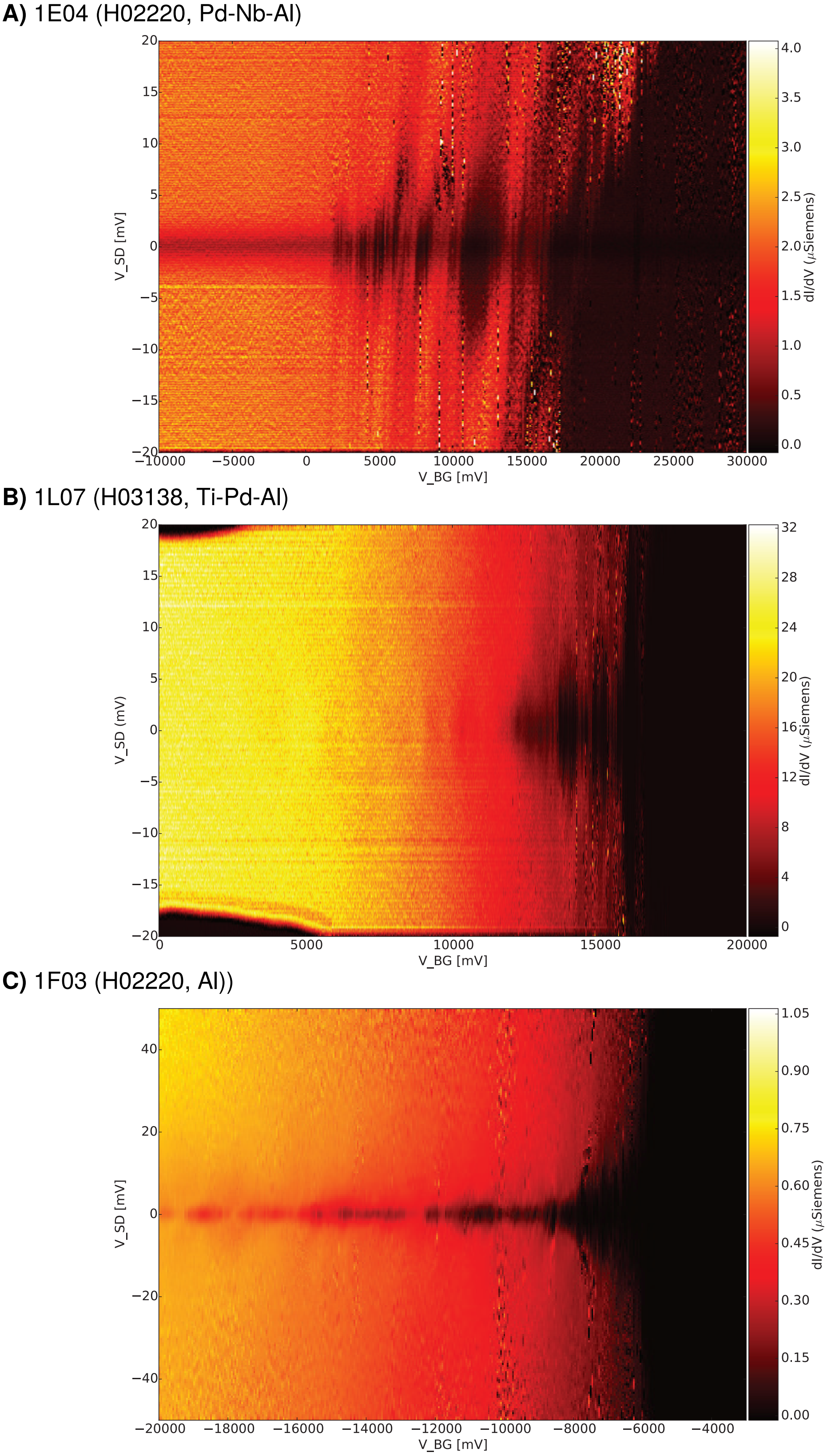
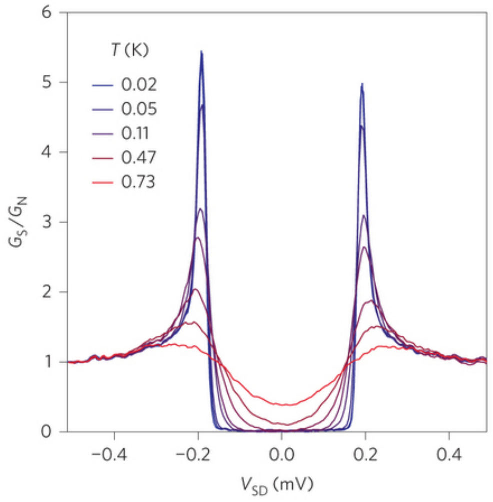
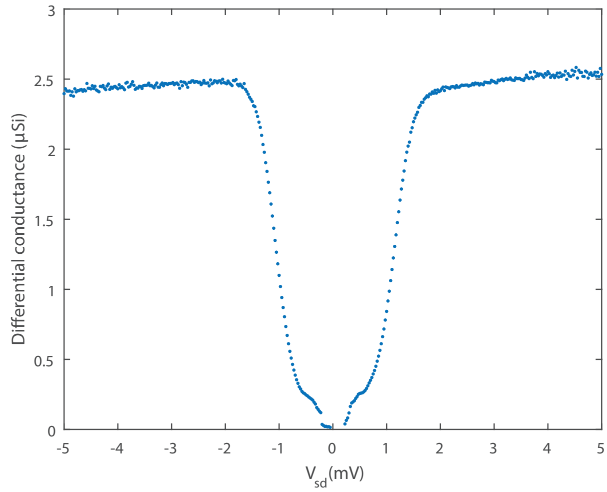


Fig. 4.2: Bias spectroscopy of samples 1E04 (A), 1L07 (B) and 1F03 (C) with dI/dV as colour scale, for the same nanowires as in figure 4.1. The graphs show a clear energy barrier outside of the pinch-off regions for samples 1E04 and 1F03, which is not present in the 1L07 sample. Sample 1F03 also seems to be pinched at zero back-gate voltage. The extra black parts of B in the top left and bottom left are due to clipping effects of the current measurement. Taken at base temperature of 4.2 Kelvin

A)



B)



C)

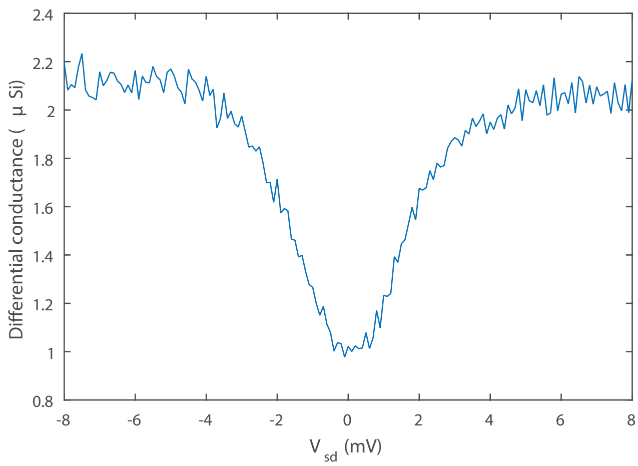


Fig. 4.3: Differential conductance versus source-drain voltage in different measurements. **A)** Differential conductance of an InAs-Al nanowire at various temperatures. We can see the gap around zero voltage and the peaks on its edges become sharper and more defined with lower temperatures. Taken from Chang et al. [28]. **B)** Lock-in measurement of the same nanowire as in figures 4.1 and 4.2 of sample 1E04 at 15 mK base temperature and a back-gate voltage of -2 V. On top of the expected dip in conductance we also see a smaller dip closer to zero bias voltage. **C)** Calculated dI/dV from a source-drain sweep of the same nanowire and at the same back-gate voltage as in B, but at a base temperature of 4.2 K. The small extra dip in conductance has disappeared and the larger gap in conductance has broadened.

get normal state conductance we need to apply a source-drain voltage larger than $2\Delta/e$. From the superconducting gaps of niobium (3.05 meV) and aluminium (0.34 meV) we expect energy barriers of 6.1 meV and 0.68 meV for the niobium and aluminium samples respectively. We see in figure 4.1 C (sample 1F03, aluminium at 4K) and figure 4.1 A (sample 1E04, niobium at 4K) a barrier of ~2 meV. It is apparent that the visible barriers do not match the mentioned 2Δ values. For the 1F03 sample this is not surprising as the aluminium is measured at 4.2 Kelvin and is thus above its critical temperature, which means that there is no superconducting gap. In the 1E04 sample measured at 4.2 Kelvin the superconducting gap should be visible as it is below niobium's critical temperature and the superconducting gap size is larger than the visible energy barrier in figure 4.1 A. The fact that it is not visible could mean that the superconducting gap is suppressed by an unknown factor (we have $B = 0$, $T < T_c$ and $I = 0$), or that we have a diffusive contact interface which causes smudging of the features.
The gap in figure 4.3 B and C is also caused by some energy barrier. Usually when $T < T_c$ the energy barrier seen is the superconducting gap in a Josephson junction. The width of the measured energy barrier does not agree with this, just like we had seen in the source-drain sweeps. We also expect the features in figure 4.3 B, such as the slope of the conductance dip and the height and sharpness of the conductance peak just before the dip to be more like the features seen in 4.3 A, as our base temperature is even lower (15 mK) than the lowest shown temperature. The fact that these features are smudged supports the mentioned case of a diffusive interface.
The one sample that showed no signs of any sort of barrier was 1L07, which existed out of Ti-Pd-Al (0.4nm-15nm-50nm). This sample has only been measured at 4.2 Kelvin which is above the critical temperature of aluminium, explaining the absence of the superconducting gap. This sample currently shows the most promise for achieving our goal as it has shown promising results for low contact resistances and high ballistic transport which are the primary requirements for superconductivity through our nanowires.

4.4.2 Resistance and mobility measurements

It should be noted that the data presented for the resistances and mobilities are only estimates, and that their actual values may differ from the given results. The reason for this is that the wire resistances can only be successfully determined by 4-probe measurements, most of which could not be performed due to fabrication problems. Most of the measurements were thus done using 2-probes, meaning we indistinguishably measure the resistance of both the wires and the contacts. Only for sample 1L07 we have calculated the actual wire resistance and contact resistances using a 4-probe. We suspect that the other samples have very high contact resistances, which could explain their very low mobility values.
The mobility calculations themselves are also not very accurate. We have already stated that the actual wire diameters and channel lengths of the 1L07 nanowires are unknown, and we must add to this that the model we used is only valid if the channel length is much larger than the thickness of the dielectric layer which in turn should be much larger than the diameter of the nanowire, which is not the case. If these requirements are not met, the screening from the metal contacts will lower the effective electric field from the back-gate and thus decrease the capacitive coupling of the back-gate to the sample. As the effective capacitance is actually smaller than the one obtained from calculations, we will underestimate our hole

mobility in the nanowire.
We have also seen that the pinch-off region of the 1F03 sample was in the negative back-gate voltage range, whereas the other earlier fabricated H02220 batch nanowire samples (1E04 and 1E03) had their pinch-off regions in the positive back-gate voltage range. We suspect that this nanowire batch has degraded over time, which will be tested by a future sample from this H02220 nanowire batch with Ti-Pd contacts.

4.4.3 Conductance dip

An interesting feature in figure 4.3 B is the minor extra dip in conductance that can be seen around zero applied bias voltage. This extra dip in conductance looks very similar to the dip in conductance visible in figure 2.6, which was attributed to enhanced weak localization. Whether we are actually seeing enhanced weak localization or not is difficult to confirm with our current measurements. If we repeat the measurement while applying a small magnetic field, the extra dip would have to disappear if it is caused by enhanced weak localization. Another suggestion for the origin of the extra dip has been that we are actually seeing the superconducting gap of aluminium on top of that of niobium. This superconducting gap of aluminium is approximately 0.68 mV, but we see the extra dip coming into existence around ~0.5 mV. This gap size is close to the superconducting gap of aluminium, but this is not a decisive result. If we repeat the measurement with a magnetic field that is smaller than the critical magnetic field of aluminium in order to maintain the superconducting gap, the dip in conductance should remain visible whereas it would disappear if it was caused by enhanced weak localization.

Conclusion

5

We have currently not yet succeeded in measuring superconductivity through our nanowires. Most of our samples showed energy barriers, high resistances and low mobilities. Through experimentation with different types of metal contacts and nanowires we have however met the most important requirements of low contact resistance and high ballistic transport. With our latest sample 1L07, which uses the new H03138 nanowire batch, we have seen no signs of any type of barrier. These properties make this sample (with Ti-Pd-Al contacts) a promising candidate for allowing a supercurrent to tunnel through the nanowires.
Aside from these progressions towards achieving our goal of superconductivity through Ge/Si core-shell nanowires, we have also seen some interesting results that may indicate the possibility of measuring enhanced weak localization at the interface between our nanowires and superconductors.

5.1 Future Work/Outlook

The most evident follow-up experiment would be to cool the 1L07 sample down to below the critical temperature of aluminium. If we perform a current sourced source-drain sweep at such a temperature we could see whether we have achieved conductivity through our nanowires or whether we are still missing an important requirement. One of these requirements could be that the phase coherence length mentioned in section 2.2.2 is smaller than the nanowire channel length. In order to determine the phase coherence length we need to obtain the Fermi velocity of the holes in our nanowires. Usually Angle-resolved photoemission spectroscopy (ARPES) can be used to obtain this velocity, but this technique requires aiming a photon source at our nanowires which cannot be done due to their small diameters of around 30 nanometers. We have not yet discovered any techniques for determining the Fermi velocity that are applicable to our nanowires.
Another issue may be the layer of palladium in our contacts. Although palladium seems to give transparent contacts to our nanowires, its stable Pd-105 isotope which has a natural abundance of 22.33%, also has a nuclear spin of +5/2 [29]. This nuclear spin will give rise to an intrinsic magnetic field that may destroy our superconductivity. The other stable and naturally occurring isotopes Pd-102, Pd-104, Pd-106, Pd-108 and Pd-110 all have a nuclear spin of 0 and do not contribute to this effect. One solution to this problem may be using PdH instead of normal Pd. PdH is a superconductor by itself with a critical temperature of 9 Kelvin if the ratio Pd to H is 1:1 [30]. If PdH still has the transparent contact characteristics, then together with its superconducting properties it may be the ideal choice for our contact material. In order to create this material we need to expose palladium to a hydrogen gas. The palladium will then exothermically absorb the hydrogen and form PdH. In the fabrication process, the use of PdH in the Electron Beam Physical Vapor Deposition step may be a problem, as the hydrogen seems to be removed from the palladium at temperatures of

300 $^{\circ}$C or higher [31]. This means that we need to expose the palladium to hydrogen after the evaporation process. The effects of the hydrogen gas on the nanowires is currently unknown, so we may need to apply a mask on our sample in this process if any effects of the hydrogen on the nanowire performance are seen.

Once we have achieved superconductivity through our nanowires we can try and see the effects of an applied magnetic field, which should change the critical current of a Josephson junction. With this magnetic field we can also investigate the validity of the extra conductance dip in figure 4.3 being caused by our enhanced weak localization measurement. We also need to verify whether the H02220 batch of nanowires degraded over time, using the control device mentioned in section 4.4.2. This device can verify both the nanowire degradation, and the property of the stack of titanium and palladium resulting in transparent contacts to our nanowires.

Once we have characterized the superconducting properties of our sample, we can add top-gates to our sample design. These top-gates will allow us to create the quantum dot systems mentioned in section 2.3. With these new devices we can start experimenting with the energy level width of the quantum dot in order to access multiple regimes of coupling between the quantum dot and the superconductors. If we are able to tune this coupling we can use this to selectively control Cooper-pair and quasiparticle tunnelling and enter the the intermediate coupling regime described in section 2.4. From inside this intermediate coupling regime we can choose to start a new challenge to create entangled particles, measure Majorana fermions or discover even more new and interesting physics.

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Colophon

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