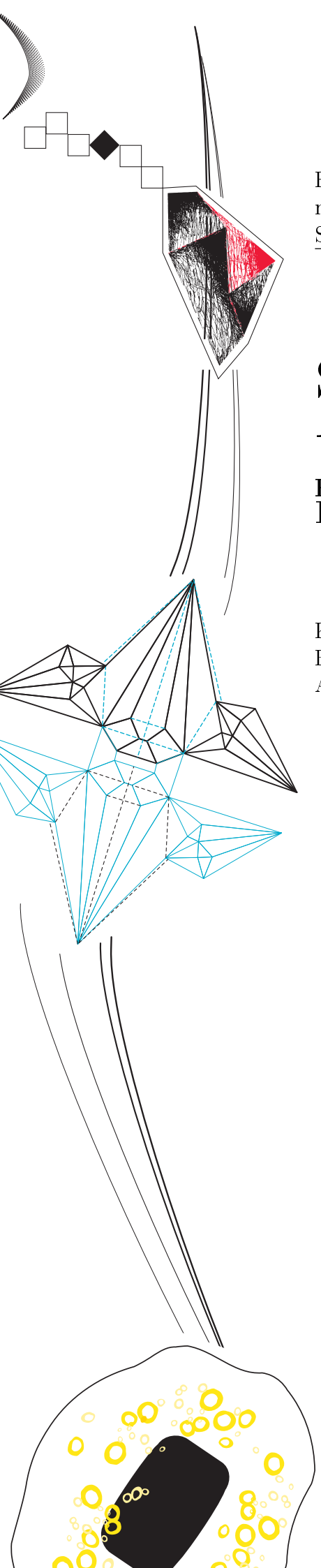

Faculty of Electrical Engineering,
mathematics and Computer Science
Supervisor: dr. ir. A.J. Annema

Switching Behavior of AMLEDs

for Implementation in Opto-coupling Devices on CMOS chips

K.P. De Meyere
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Abstract

The use of Complementary Metal-Oxide Semiconductor (CMOS) chips is becoming more predominant in every day life, it being included in general appliances such as cell phones, televisions and tablets, to name a few. They are often used as control systems that operate at a much lower voltage than the system it controls and must work in electrical isolation from it. One method of doing so is to use an opto-coupling device that connects the two circuits using EM waves.

An opto-coupling device often has a substantial power consumption but a solution was proposed by A.J. Annema et al. to reduce this by using a Single Photon Avalanche Detector (SPAD) on the receiving end and an Avalanche Mode Light Emitting Diode (AMLED). The AMLED would have to emit a minimal amount of photons for it to be detected and can be turned off much faster and efficiently than a forward LED. Using these components would lead to reduced power consumption and less interference on the rest of the system due to changing magnetic or electric field.

The problem with the AMLED is that its switching behavior is not well defined and is most likely influenced by dead time, a period of time in which there are no mobile carriers in the depletion layer.

The assignment was to investigate the existence and effect of dead time in a semiconductor through simulations and experiments. Through the use of Sentaurus, a simulation program, and experimental set-ups it was attempted to find the effects of the dead time.

In the end there were no conclusive results as the simulation software ignored the probabilities of avalanching, making it avalanche every time possible and the experiments could not find evidence of the dead time due to the large amount of charge injected by the saturation current of the transistor used.

A possible solution to make the experiments described in this report work is to employ a transistor with a low saturation current, in the order of pA.

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1 Introduction

The use of Integrated Circuits (IC) on Complementary Metal-Oxide-Semiconductors (CMOS) is found in many of today's everyday appliances such as cell-phones, tablets and laptops. They are also found in many forms of control systems that can maintain high voltage functions while maintaining a low power output. In order to do so, these low voltage control systems have to interact with the devices through methods that keep both devices isolated.

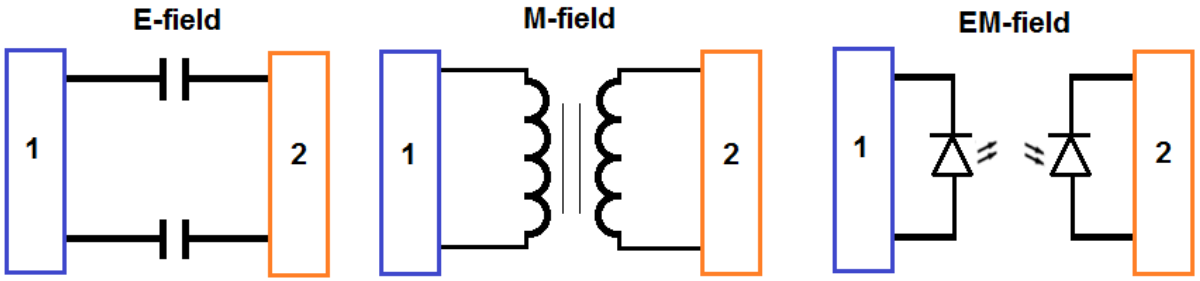

Figure 1.0.1: Different methods to communicate between circuits.

Figure 1.0.1 contains symbolic representations for the different methods to communicate between two circuits. Circuits 1 and 2 are the signal modulating circuit and readout circuit respectively. The one on the left consists of two decoupling capacitors that keep the DC components from traveling between the two circuits with the use of electric fields. The second method is to use a transformer to communicate between circuits 1 and 2 using a changing magnetic field. The third option is to use electromagnetic (EM) waves emitted by an LED and detected using a photo-detector. Both magnetic and electric fields can influence the circuits by inducing unwanted currents or voltage differences. EM fields, on the other hand, do not influence circuits and would produce the least amount of interference.

1.1 Theory

There are two components to the opto-coupler: the LED and photo-detector. The light emitted by the LED has to have an energy high enough to excite an electron in the photo detector up to the conduction band. This would result in a significant power consumption as the LED would consistently consume energy. A solution to this is to use a digital signal transfer with two distinct states, on and off, that can be detected by the photo-detector. If only two states have to be detected it is possible to use a SPAD. The working principle of a SPAD is that a single photon incident on the device is enough to cause avalanching in the device, thus forming a current through the diode. The diode would continue to avalanche until the system is quenched [1]. The benefit of using such a device is it can detect low amounts of photons and will always generate the same signal when it detects them. Considering the LED is only turning on and off, this is ideal for this situation if the light's energy is sufficient to cause avalanching.

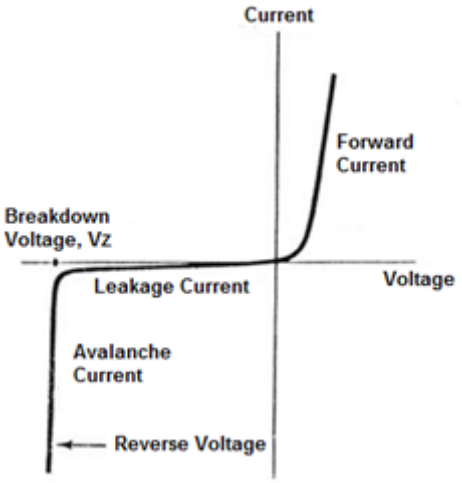

Figure 1.1.1: IV Curve of a standard diode

As stated before, the light emitted by the LED has to be sufficient enough to be detectable by the photo-detector. This requires a substantial amount of forward voltage and will require a driving signal that can be modulated from 0 to this voltage, a power intensive signal to create. It is possible to make the LED switch intensities of which only one can be detected, but this would lead to a high amount of power loss as not all photons generated are used.

A possible solution is to use an Avalanche Mode LED (AMLED) that generates light when subjected to a sufficiently high reverse voltage. As can be seen in Figure 1.1.1, the benefit of using an AMLED is that the power emitted increases substantially more than to the standard LED once the diode is in avalanching. If the signal is biased near the breakdown voltage, it should be possible to create photons with substantial energy to be detected, thus reducing power loss.

The switching behavior of an AMLED is limited by a few factors. The most prominent limiting factor is the dead time that arises after avalanching. The dead time defines the period in which the depletion layer is devoid of mobile charge carriers thus prohibiting the start of avalanching. [1] This limits the rate at which the AMLED can turn on and off and thus limiting the rate of data transfer. S. Cova et al. calculated a dead time of 1 μs for a standard SPAD [2] resulting in a maximum switching rate of 1MHz.

After each time the junction breaks down it has to be quenched. This can be done both passively or actively, depending on the circuit. A passive quenching circuit utilizes linear components such as resistors or capacitors to reset the electric fields within the semiconductor. An active quenching circuit uses the signal to quench the system as by changing the voltage drop over the diode. Active quenching is generally faster but it also more power intensive.

The final aspect that has to be kept in mind is the transmission of the photons from the LED to the SPAD. This is done by implementing silicon oxide trench isolation between the two components to act as a wave guide, albeit a poor one. The refractive index of silicon is lower than glass, resulting to photon loss to the surrounding material.

This won't be investigated in the report though, as this report will focus entirely on the avalanching behavior of silicon.

This work aims to investigate the implementation of opto-coupling on CMOS chips through the use of SPADs and AMLEDs. SPAD technology is advanced enough to not warrant further investigation, but AMLEDS require more attention. The switching behavior of avalanching diodes were simulated using Sentaurus and then tested through experimentation to determine the effect of dead time and the possible restrictions in signal transfer.

2 Sentaurus Simulations

In order to avoid wasting time and money, it is essential to model any design made beforehand. This can best be done using the Sentaurus Workbench Tool, a program that allows for the design and simulation of custom semiconductor designs. Any theory can first be tested using this program and will give insight on the behavior of the design. This, off course, is no substitute for an actual semiconductor to test on, but making real ones takes time and money thus it is most effective to first design a semiconductor that appears to work as intended and to then test it physically.

A detailed description of the design process is given in Appendix A(5.1). The design for a standard BJT was provided by S. Dutta, a design that was subsequently altered to try and investigate the effects of changing various parameters. BJTs were investigated as it would provide a way to inject carriers into the depletion layer, decreasing the amount of dead time.

2.1 Avalanching in BJT Models

The first step was to make a conceptual design based off of the limitations of the production facilities. The company that provides the custom CMOS service provided rules and limitations which the design would have to follow.

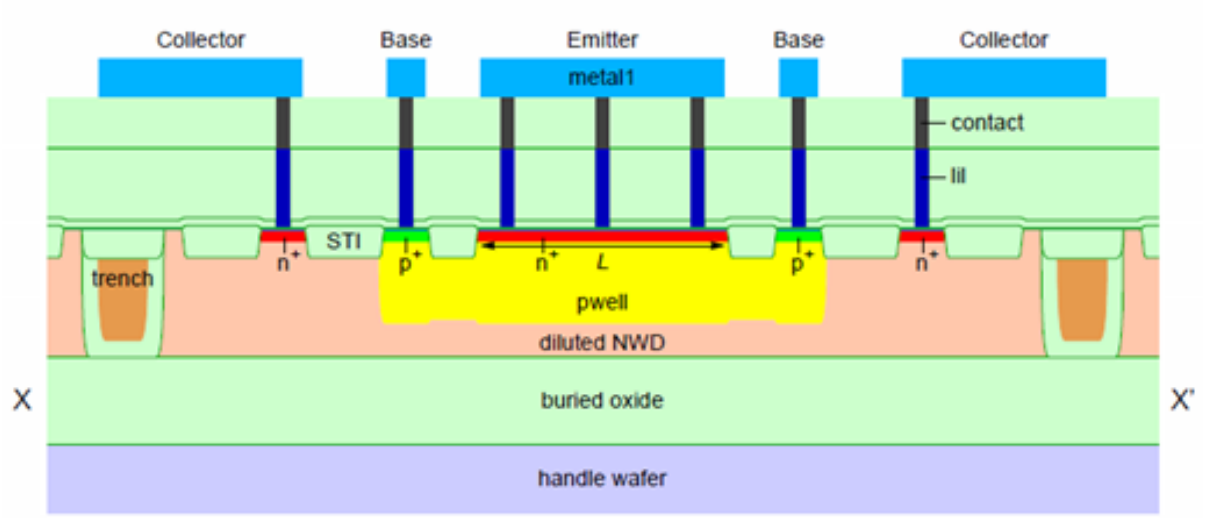

Figure 2.1.1: A standard npn transistor design used as basis for simulation designs.

This design is overly complex and simulating it would require a lot of time and processing power. It is, however, possible to simplify this structure. The design in Figure 2.1.1 is symmetrical, thus it is possible to reduce the structure to the mirrored design. By cutting the structure in half, there would be only 1 of each contact.

Taking this into account, two designs were made, both of which follow the general principle of the provided example, but with slight variations, as seen in Figure 2.1.2.

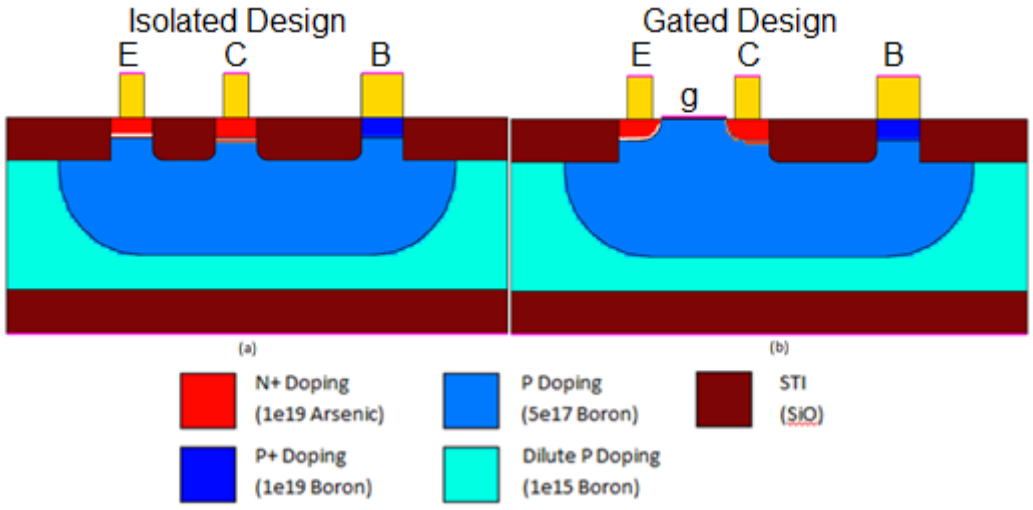

Figure 2.1.2: Two designs made in Sentaurus: (a) is half the structure of Figure 2.1.1 (b) replaces an STI with a gate. Units: cm^{-3}

In the picture shown above, the red regions are n+ doped areas whereas the blue areas are p doped, where the doping levels are indicated in the legend. These two structures are very similar to the design in Figure 2.1.1, with the main difference being the use of a dilute p-well substrate instead of an n-well. The other difference is the position of the contacts, the order is mixed around. This is mainly done in order to force avalanching to

occur near one of the STIs.

The difference between the two designs is the Shallow Trench Isolation (STI) between the emitter and the collector. The reason for this was to investigate its effect on the behavior of the system as well as to reduce the possibility of shorting the emitter and collector. This does, however, increase the distance the electrons would have to travel, thus decreasing the current gain and response time of the system.

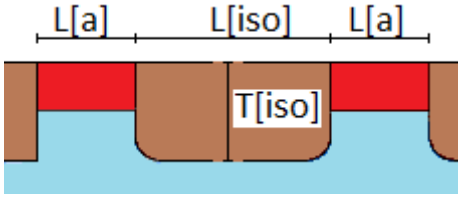

Figure 2.1.3: Close-up on varying distance.

Based on that same principal, the distance between the collector and emitter (L[iso] in Figure 5) was made to be 0.3, 0.4 and 0.5 μm for the two designs, resulting in a total of 6 structures. The idea behind this was to investigate the effect if increasing the distance between the emitter and the collector. The isolated design also used the increased distance to provide something to compare the results of the gated designs with. These distances were chosen based upon the physical capabilities of the production of CMOS chips.

2.1.1 Characterization of BJTs

To make the BJT emit light it has to avalanche. This only happens when one of the junctions (base, collector, base-emitter, collector-emitter) is subjected to a high enough potential difference, higher than their breakdown voltage. In this design, the emitter-base will be the subject of investigation as this is the junction that has the lowest breakdown voltage in physical transistors.

The switching behavior would be tested by modulating a signal around the breakdown voltage. An on-off signal with a DC offset slightly lower than the breakdown voltage will run through the BJT and cause the emitter-base junction to avalanche at regular intervals. When the signal is off the current through the emitter is near zero while it will be substantially larger when the signal is turned on.

In order to do so, it is important to clearly define the breakdown voltage of the emitter-base junction. It can be defined in two ways. The simplest way is to sweep the junction using an increasing biasing voltage. Each design would be made made subject to a range of voltages and then plotted onto an IV plot with a semi-logarithmic scale from which it should be possible to determine the breakdown voltage. The saturation current should stay low until the breakdown point, after which it should increase substantially, and this sudden change in current is used to define the breakdown voltage.

The second option is to use the built in "BreakAtIonIntegral" command which forces the simulation to stop when breakdown occurs [3]. It is a neat tool provided by Sentaurus which could shorten simulations significantly. This is the method that was used as it provided the nicer graphs, ones that did not show erratic behavior past breakdown.

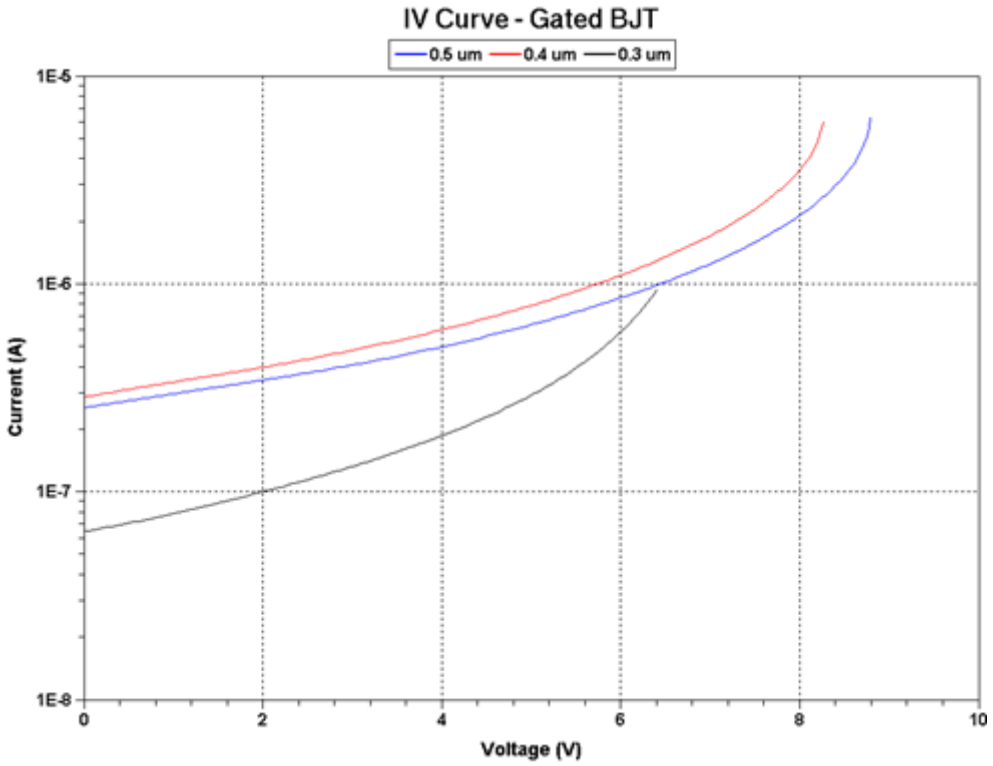

Figure 2.1.4: IV Curves for the three different BJT designs with gate.

The results were subsequently graphed onto a semi-logarithmic scale. Figure 6 shows the IV curves for the three different gated BJTs obtained using the "BreakAtIonIntegral" command. Each line features a sharp increase near the end indicating that it is approaching breakdown. Similar behavior was visible on the IV curve for the isolated design but it had one curve that looked as though it did not complete the simulation (there was no significant current increase near breakdown). The reason for this was not found and every simulation consistently stopped at that point. See Appendix B (5.2) for the other IV plot of the isolated BJT.

Breakdown Voltage V_{BR} per design:

Gated 0.3 μm	6.40 V
Gated 0.4 μm	8.26 V
Gated 0.5 μm	8.78 V
Isolated 0.3 μm	4.95 V
Isolated 0.4 μm	7.61 V
Isolated 0.5 μm	8.98 V

The table above shows the voltages at which each simulation ended. These values were used to determine the DC biasing to be used in the pulsing simulations. Each design

was biased just below these values and then simulated to go past the breakdown. If the frequency is low enough, every time the junctions are pushed into avalanche they should observe a significant current change. If the frequency is too high there might be some pulses missing.

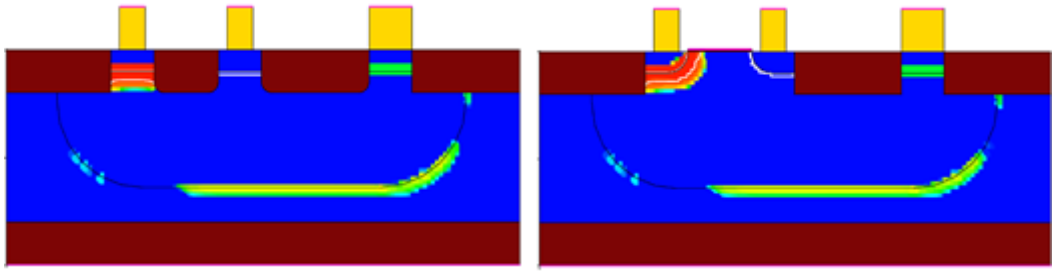

Figure 2.1.5: Impact Ionization within the structures.

Subsequently, the location of the breakdown is identified using Sentaurus Visual.

As seen in Figure 2.1.5, the impact ionization occurred primarily at the emitter junction with some ionization happening between at the other junctions and the substrate/base interface due to the differences in doping levels. The emitter junction was avalanching and would release photons into the device and the surrounding isolation would act as waveguides.

To test the switching behavior, a 100MHz signal was simulated to run through the design. This value is much higher than 1MHz and is therefore expected to be influenced by the dead time. If the dead time were present, the junction should not avalanche at every instance and at some points no current should run through the emitter even though the voltage was past breakdown. These can be identified by missing pulses, irregularities in the current-time plot.

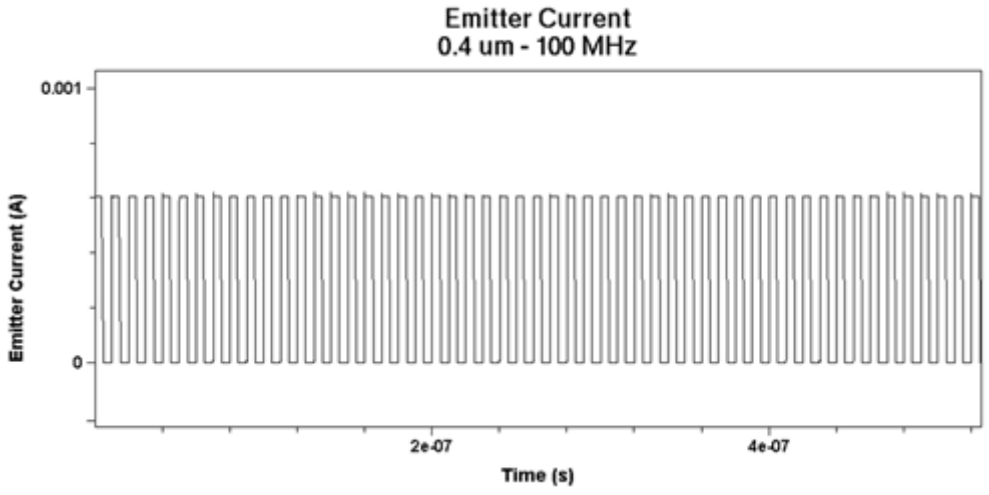

Figure 2.1.6: Current through emitter node in the simulation when subjected to a 100MHz signal.

The current through the emitter contact was in phase with the signal indicating that the emitter-base junction was avalanching. There were no irregularities, no missing pulses, though and this indicated that the dead time did not act on the system.

Every frequency used to drive the device resulted in a similar graph as Figure 2.1.6, a square wave with the same frequency as the signal and no missing pulses. This was the case for every design, both gated and isolated. There was a single instance where pulses went missing but the missing pulses were erratic and non-periodic. This graph was considered to be an outlier as it could not be replicated. See Appendix C(5.3) to see this graph.

The results of the simulation did not support the existence of significant dead time in the junctions. There is solid evidence that the dead time should influence the avalanching behavior [1][2] but it is possible that Sentaurus cannot simulate this effect entirely.

2.2 Avalanching in PN Junction

In order to check the validity of the results, a simple PN-junction was simulated. This junction would be tested in similar ways as the BJT before but it will be more predictable in behavior. A total of three junctions were designed and investigated by comparing the depletion width of the simulated device with the expected value. If these matched up, the junctions were made subject to the same test as the BJT designs where they would be repeatedly pushed into breakdown to find the missing pulses.

Figure 2.2.1: Standard BJT design with doping profile.

A set of regular PN junctions had been modeled in Sentaurus. They were each identical in shape but featured different doping profiles. The design itself is visible in Figure 2.2.1 and the electrodes had been attached to the different sides of the junction. The reason this design is so elongated is to ensure that the depletion width of the design is within the structure itself and that it does not come in contact with the electrodes. The doping levels themselves are uniform and consist of three different levels (one per design): 10^{16}, 10^{17} and 10^{19} dopants per cubic centimeter.

2.2.1 Depletion Width

In literature, it is found that the depletion width of a PN-junction is given by the following equations [4]:

$W = (x_d n + x_d p) = (\frac{-2}{q}(\frac{N_A+N_D}{N_A N_D}V_{bi})(eq.1)$
$V_{bi} = -U_T ln(\frac{N_A N_D}{n_i^2})$(eq.2)

In this equation, q is the charge of an electron, N_A and N_D are carrier concentrations (Acceptor and Donor), V_{bi} is the built in voltage, U_T is the thermal voltage equivalent and ni is the intrinsic carrier concentration. The values calculated using equation eq.1 are 0.418 μm, 0.143 μm and 0.016 μm for the doping concentrations 1, 2 and 3 respectively. This equation assumed a uniform doping level throughout each region which is exactly the case in this design.

There are two ways to determine the depletion width from the simulation. The first one is to rely on the built in program that will show where it is but because the algorithm for finding this is unknown, it is best to find the depletion layers manually. This is done by either plotting the electric potential or the number of carriers as a function of distance. Both graphs would show a sudden drop or gain at the edge of the depletion layer which indicated where the depletion layer is.

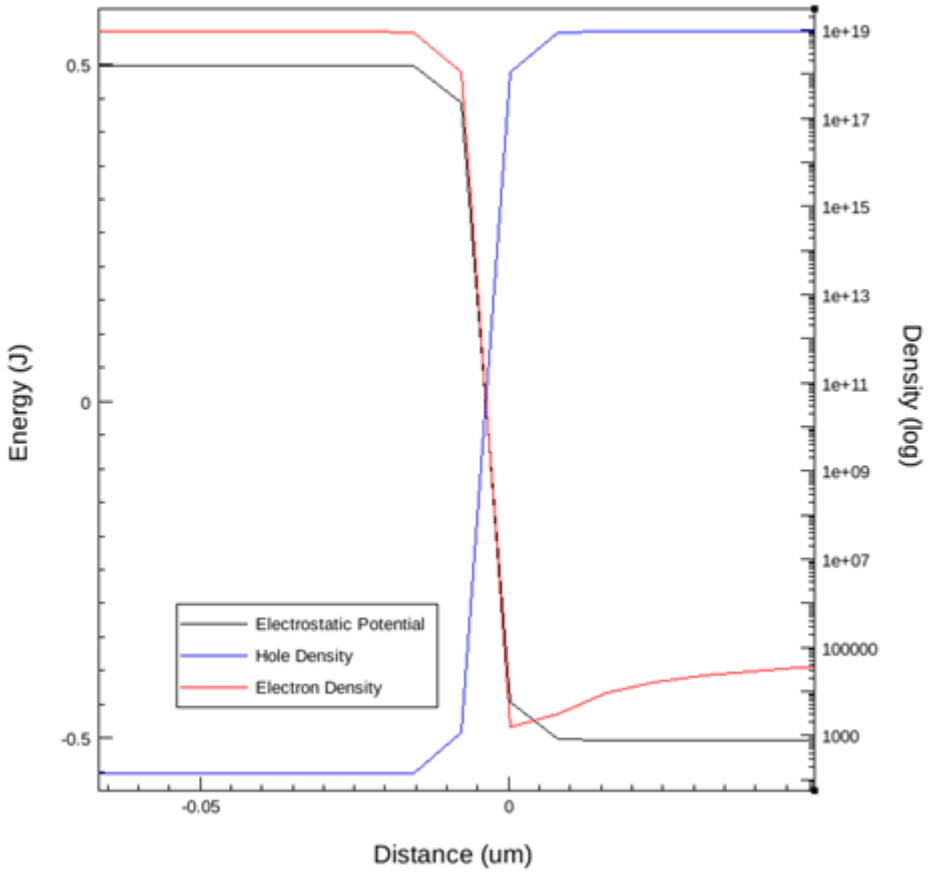

Figure 2.2.2: Carrier concentrations and electric potential for doping concentration 3.

From this graph it was possible to approximate the depletion layer. The layer is indicated by the sudden increase or decrease in carrier concentration, as well as by the drop in electric potential. According to the graphs obtained, the depletion widths are 0.4 μm, 0.15 μm and 0.015 μm for doping concentrations 1, 2 and 3 respectively. These values are close matches to the results obtained using equations 1 and 2, so it proves that the junction is sufficiently simulated in the program.

Earlier iterations did not show the expected results but that was resolved by increasing the meshing size, which in turn increased the duration of the simulations. In the end, these values were very close to each other and support the claim that the simulations can provide valuable insight into the behavior of a semiconductor. It also provided some insight into the workings of the program as the meshing of the structure was detrimental to getting the correct result, which should be kept in mind for future simulations.

2.2.2 Characterization of PN Junction

The next step was to determine the breakdown voltage of the different junctions. This was done exactly the same way as with the BJTs, by sweeping the voltages from 0 to some high value. This time, however, the " BreakAtIonIntegral" command was omitted to observe the behavior of the simulation past the breakdown point. It resulted in the following graph:

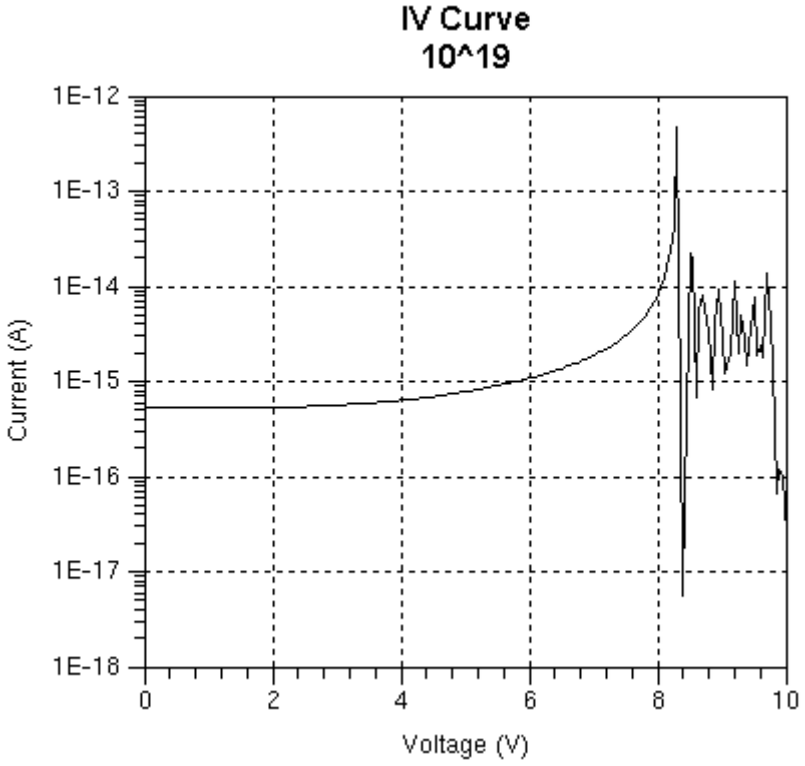

Figure 2.2.3: IV Curve for doping concentration $10^{19} cm^{-3}$.

Figure 2.2.3 shows the IV curve obtained for doping concentration 3 and there was a sharp increase in current past the 8V mark. The graph itself was not very clear as to what happens past this point but it gives a rough estimate for the breakdown voltage. The breakdown voltages were ∼55V, ∼19.5V and ∼8V for doping concentrations 1016, 10^{17} and 10^{19} respectively. The breakdown voltage increases as the doping level decreases, as dictated by B. Van Zeghbroeck[5].

Using these values, the junctions were biased at a point below the breakdown voltage and repeatedly made to avalanche using a on-off pulsing. Just like before, the current through the devices should result in a square wave that is in phase with the input signal up until a repetition rate of ∼1MHz. After that point some pulses are expected to be missing, which is the point of this experiment.

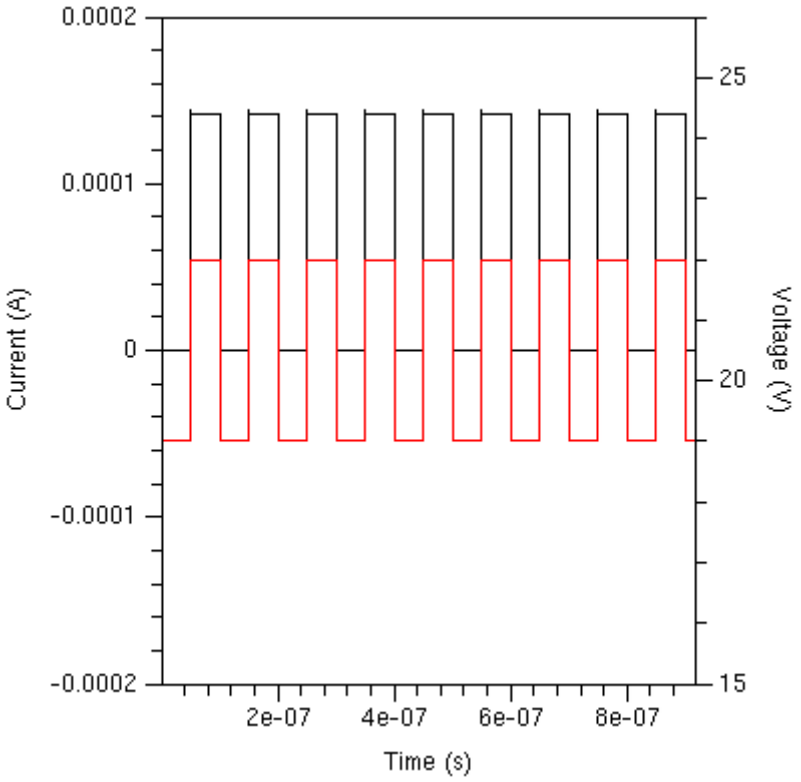

Figure 2.2.4: Transient sweep using a 10MHz on-off signal on the $10^{17}\ cm^{-3}$ junction.

Figure 2.2.4 shows the current through the emitter junction. Just like the BJT simulations, there was no evidence of a finite repetition rate. The simplicity of the design should have made the dead time interfere at some point, but a 1GHz signal did not evoke any result either. This begs the question as to whether Sentaurus is fully able to simulate the desired avalanching behavior.

2.3 Evaluation of Simulations

Based on the results obtained for both the BJT and the PN-junction, the dead time should have no influence on the signal transfer if avalanching silicon is used in an opto-coupling device. This, however, contradicts other sources [1][2] and brings into question to what extend Sentaurus is able to simulate an avalanching diode.

Further investigation lead to finding a fundamental problem with the way Sentaurus simulates semiconductors. Sentaurus uses a deterministic approach to solving the problem while avalanching is a stochastic event. This means that Sentaurus does not take into account probabilities and assumes that a system will avalanche whenever it is possible.

This is problematic as the finite repetition rate is heavily reliant on the probability of it not avalanching. This means that Sentaurus is not equipped to simulate the desired switching behavior and so experiments might yield other results.

3 Experiments

Due to the limits of Sentaurus's capabilities to simulate avalanching models, some experiments were performed in order to find the dead time because, according to sources [1] [6], it should exist. Based on these sources, V. Agarwal made a few circuit designs meant to test the avalanching behavior of physical diodes and BJTs. There were a variety of circuit designs with a few different quenching circuits. The following design is the one that was used throughout this report:

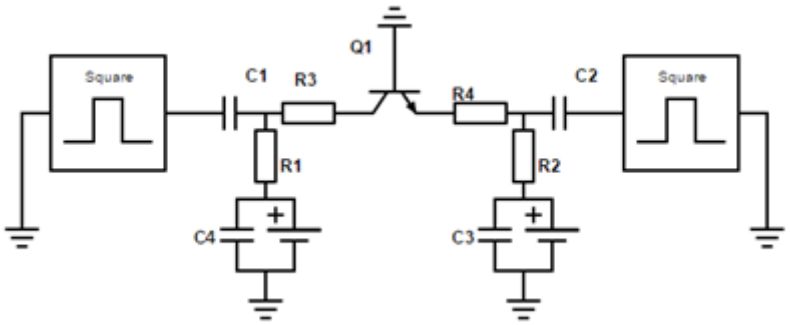

Figure 3.0.1: Circuit design featuring the possibility to actively quench the transistor.

This design features three different circuits for each terminal of the transistor. The most simple one is the base, which is grounded. The junction with the lowest breakdown voltage is the emitter-base junction and the base should not influence this.

The circuit on the emitter side featured a coupling capacitor (C2), a decoupling capacitor (C3), a pulse generator, a DC voltage supply and two resistors (R2 and R4). The DC voltage supply was used to set the biasing point just below the breakdown voltage. The pulse generator would modulate the voltage above the breakdown voltage, making a current flow. The current that flowed through R4 should be very low unless the junction is in breakdown. By measuring the voltage over the resistor R4 it should have been possible to identify when the avalanching event.

The collector's circuit was exactly the same as the emitter's circuit but it served a different purposed. This circuit was made in the case free carriers had to be injected into the BJT. By applying a voltage on the collector junction some carriers would get injected into the PCB which should reduce the dead time of the system, thus increasing the maximum frequency obtainable. The two signal generators would be synchronized in order to inject the carriers at the right time.

In the end the circuit looked more like this:

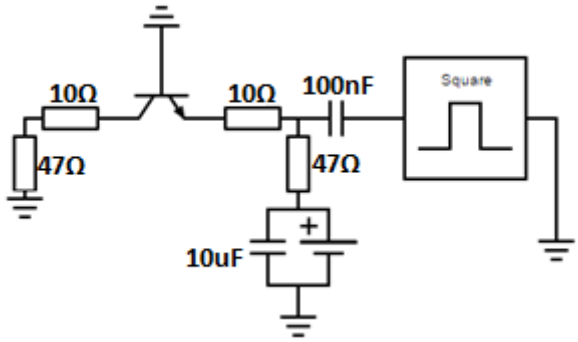

Figure 3.0.2: Simplified version of Figure 3.0.1.

This circuit was then implemented on a PCB design, by V. Agarwal, PCB designed using Agilent Technologies'Advanced Design System (ADS). It is a tool to design PCB which can then be fabricated. The reason a PCB was used is because it would reduce parasitic influences. SMD components generally produce more stable measurements than their through hole components counterparts. When working with high frequencies, small pieces of wires can act as inductors and create strange impedances. Proper design can create distance between components and thereby reduce the parasitic inductance. V. Agarwal had already performed the experiment using through hole components but he could not find any missing pulses. He concluded that the parasitic influences of the through hole components were too high and that SMD components might yield better results.

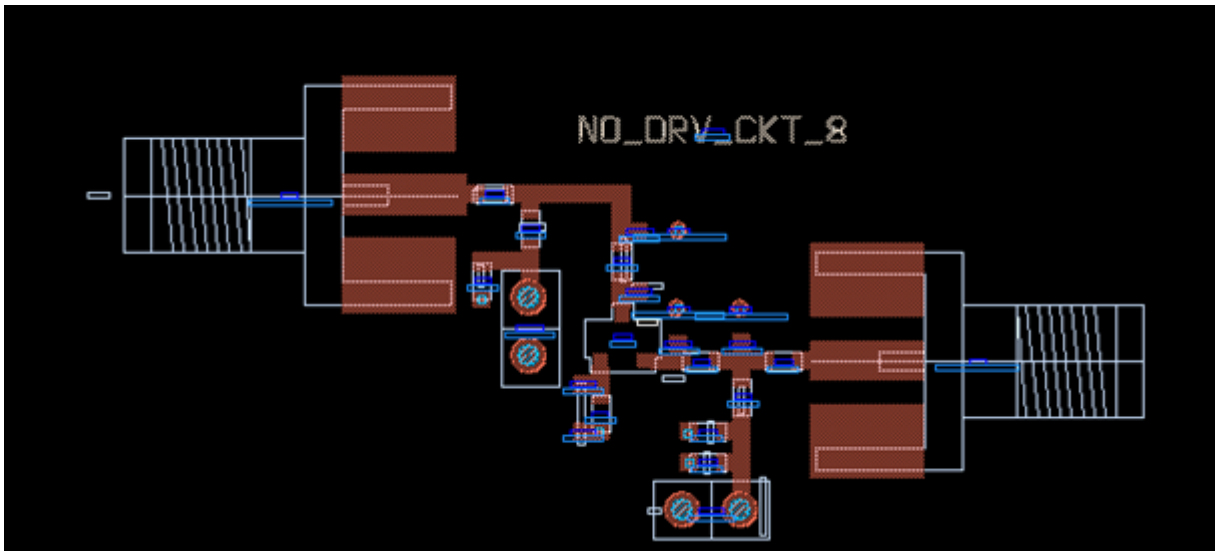

Figure 3.0.3: ADS design of Figure 3.0.1

The design in Figure 3.0.3 is based around the structure of an SOT23 package transistor. The terminals are defined as seen in Figure 3.0.4. The brown areas are conductive

contacts whereas the white lines indicate the presence of potential PCB components. There are few differences between this design and the one in Figure 3.0.1, the main differences being the ability to add a load between the base and a second decoupling capacitor, in case they were needed. The rest is exactly the same.

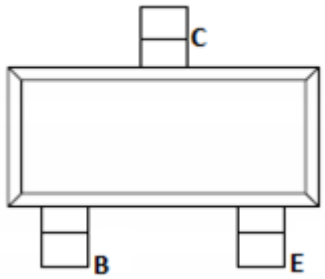

Figure 3.0.4: Contact definition of SOT23.

With this design, the components were soldered to the PCB and resulted in the circuit shown in Figure 3.0.2.

The first transistor used with this design is the PMBT2369, an NPN switching transistor which allows a maximum voltage of 5V across the emitter-base junction. [7] This indicates that the breakdown voltage is close to 6 volts. The breakdown voltage was then found using the Hewlett Packard Semiconductor Parameter Analyzer (HP4156B) by performing DC sweep from 0 to 9V and plotting the results on a semi-logarithmic scale:

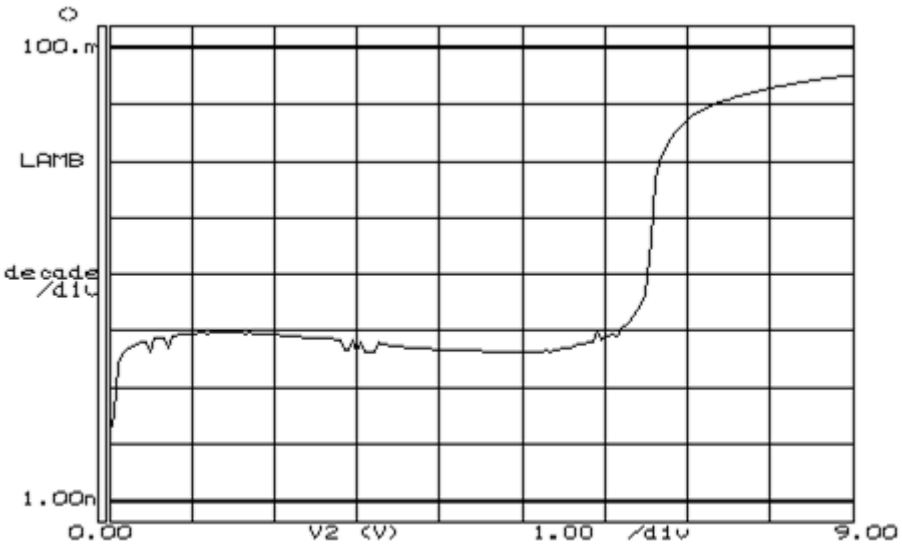

Figure 3.0.5: Preliminary IV Curve for the DC sweep of PMBT2369.

As stated in the simulations section, the breakdown was defined at the point where $\frac{dI}{dV}$ was the largest. In Figure 3.0.5, this point was at 6.5V. The device also displayed a saturation current of about $\sim$1 μA, which is could impact the avalanching behavior. The

saturation current also goes down before the breakdown voltage is reached, a phenomenon that is out of place and places doubt on the data collected with the HP4156B. The most important part of this graph was the breakdown voltage which was clearly indicated and was close to the expected value.

3.1 Repeated Avalanching Experiment

This transistor was then soldered onto the PCB board and connected to a variable DC source (Agilent E3631A) and the pattern generator (Anritsu Pulse Pattern Generator MP1763C). A differential probe (N2803A) with a specialized tip (N2838A) was placed across resistor R4 and attached to an oscilloscope (Agilent Infiniium Digital Signal Analyzer). The first experiment was to keep the biasing voltage at zero to see how the current would change when the transistor is met with an on-off pulse but is not avalanching. The function generator was set to create a 1.2V peak-to-peak square wave which would drive the system. The voltage difference was measured over a prolonged period of time to collect more pulses within a single set of data, increasing the likelihood that a pulse is missing somewhere indicating the unwanted repetition rate.

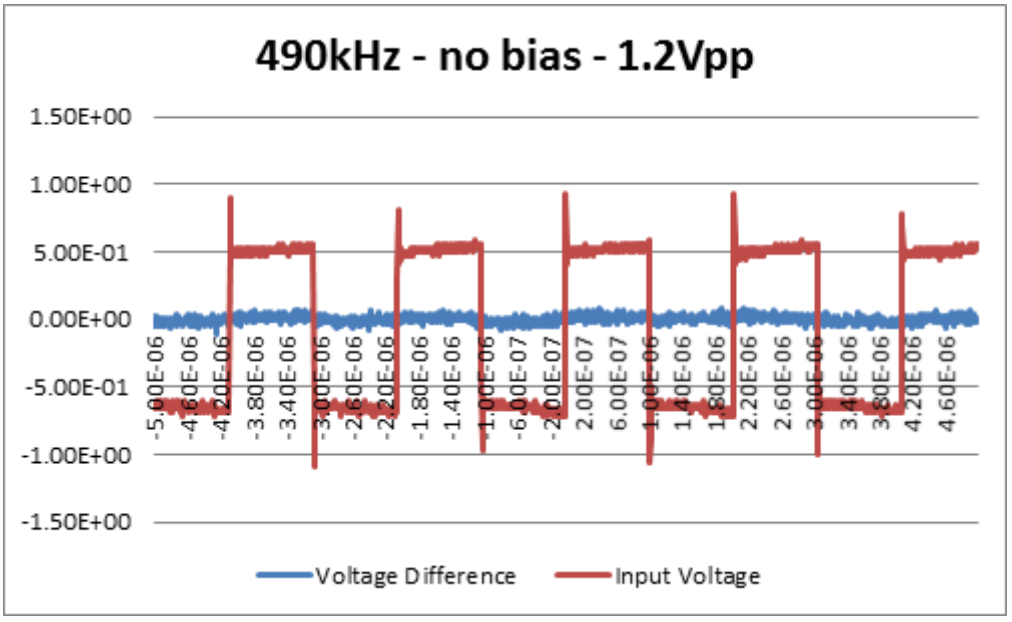

Figure 3.1.1: Voltage input vs voltage difference across resistor R4, no bias.

The first frequency tested was a 490kHz block wave without biasing voltage. Without a bias the emitter-base junction should not break down and no current should run through resistor R4. Figure 3.1.1 shows the result of this experiment and it confirms that the current is unaffected when the junction is not avalanching.

Subsequently, the bias voltage was raised to 6.5 volts and modulated using the same block wave as before. Upon avalanching, a current should run through resistor R4 at every peak of the signal and no current should appear at the troughs.

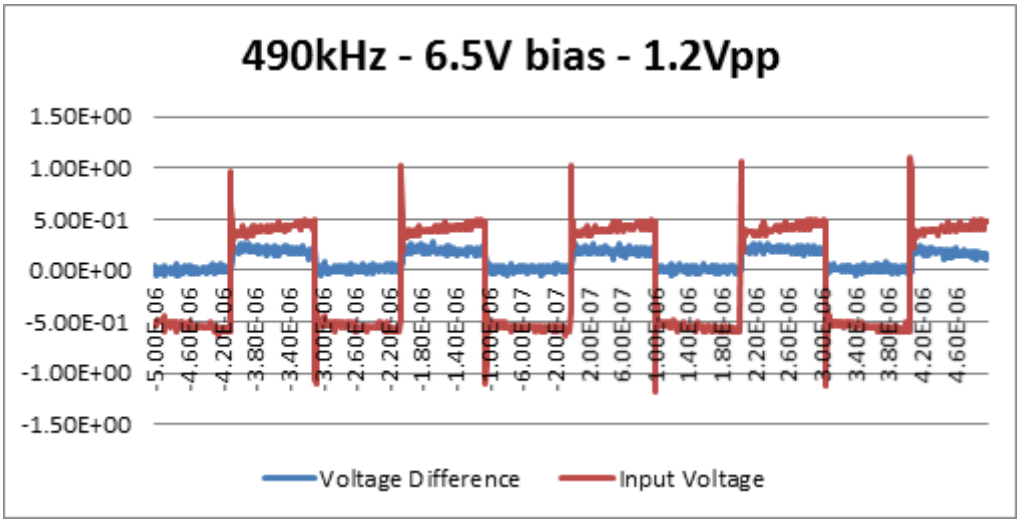

Figure 3.1.2: Voltage input vs voltage difference across resistor R4, 6.5V bias.

Figure 3.1.2 showed that the device avalanched once the voltage was pushed past 6.5 volts and that the method works as intended. Comparing this graph with the one in Figure 3.1.1 showed that there was a clear difference between the two. While the voltage remained 0 when there was no biasing voltage, there were peaks in Figure 3.1.2 every time the voltage went above the breakdown point. This was ideal as it showed that both the setup worked as intended and that the emitter-base junction did indeed breakdown around 6.5V. The frequency was raised to 50MHz. The same signals were applied as with the 490kHz signal: the device was first tested without biasing voltage and then with to act as comparison between the two. The only difference is that the peak-to-peak voltage was increase to 1.8V to increase the difference in saturation and breakdown current.

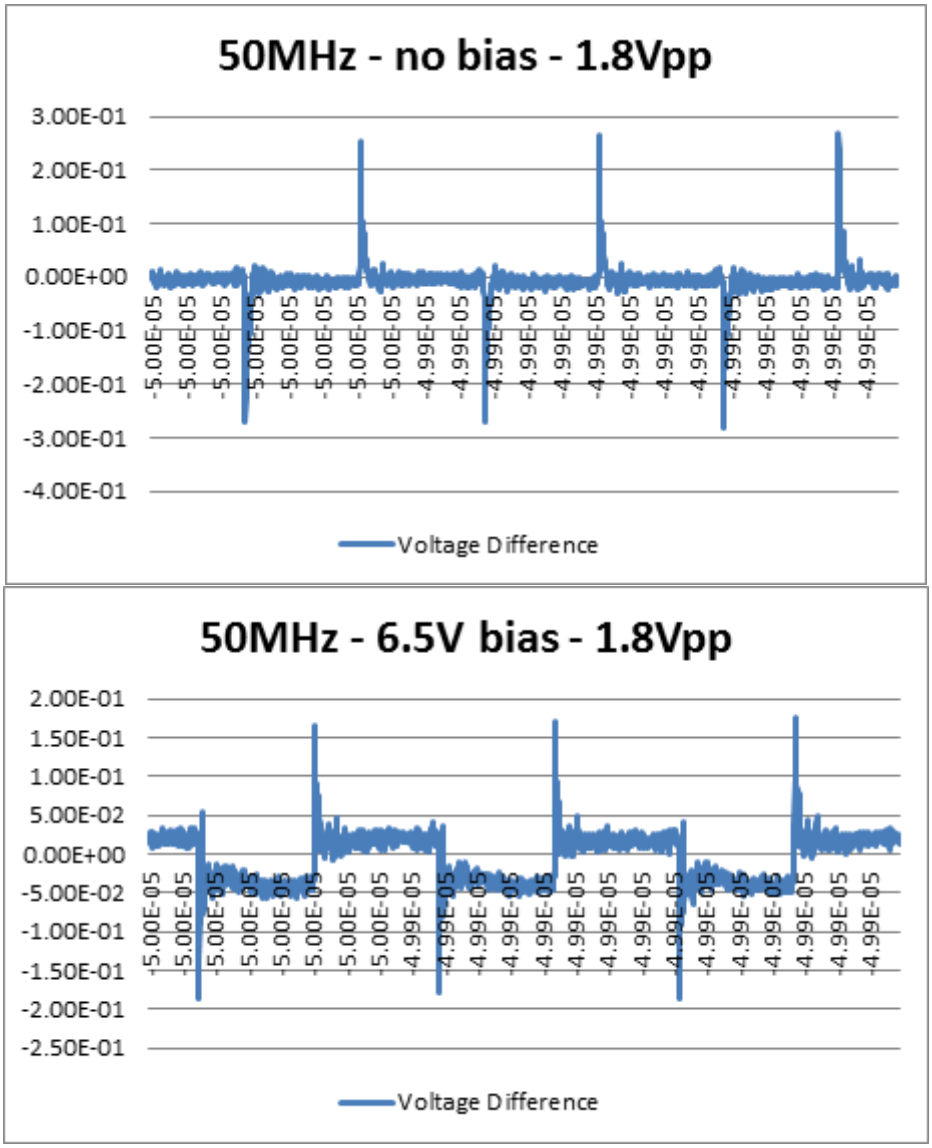

Figure 3.1.3: : Voltage differences over resistor R4 with a) no bias and b) 6.5 bias.

The device showed similar behavior as with the 490kHz signal, the graphs in Figure 3.1.3 show that no current runs through the transistor (with the exception of a few peaks) and it started to avalanche at regular intervals as it was being pushed past breakdown. The peaks themselves or most likely the effect of the coupling capacitor releasing its charge every time a square pulsed through. This was later verified by simulations using LTSpice (See Appendix E(5.5)). The results did not show any unwanted repetition rate. The frequency was then raised to 200MHz, and even 500MHz, but there were still no missing pulses and noise was already starting to show up significantly. Each experiment displayed similar behavior and therefore different explanations for this were explored.

The first theory was that the junction was in Zener breakdown, allowing electrons to tunnel through the depletion layer without needing time to replenish the layer with mobile carriers, hence no dead time. A breakdown voltage of 6.5V indicates that the junction could be either an avalanching or Zener diode. A diode is expected to be dominated by the Zener effect when the breakdown voltage is below 5V and the avalanching mechanism

when the breakdown voltage is above 10V [8], but 6.5V is somewhere in the between and thus this had to be investigated.

When a junction is highly doped it will create a narrow depletion width and usually have low breakdown voltages. The depletion layer is so thin that electrons are able to tunnel through it, causing a current to flow. It has a negative temperature coefficient [9] meaning that an increase in temperature should decrease the breakdown voltage.

Avalanche breakdown only occurs in lowly doped junctions as it requires a larger depletion width than a Zener Diode. The mechanism is based on impact ionization, one electron could ionize atoms within the depletion layer, releasing additional electrons. Those released electrons would do the same and this results in the so called Avalanching effect [9].

If the transistor was indeed in Zener breakdown then the temperature coefficient should be negative, which can be verified by performing a DC sweep of the emitter-base junction at varying temperatures.

3.2 Characterization of Transistors

Based on that, the transistor was tested using a more accurate measurement setup. The PMBT2369 was tested at three different temperatures (-10°C, 25°C and 75°C) by doing a DC sweep using the Keithley Semiconductor Characterization System (4200-SCS), a more accurate machine than the HP4156B. Keithley has a current compliance of 0.1A as to minimize the damage to the machinery used. The component was taped onto a clean wafer and placed in a probe station (Cascade Summit 1100) that could regulate the ambient temperature. It was left in the station for 10 minutes before each measurement was taken for the PCB to reach the desired temperatures.

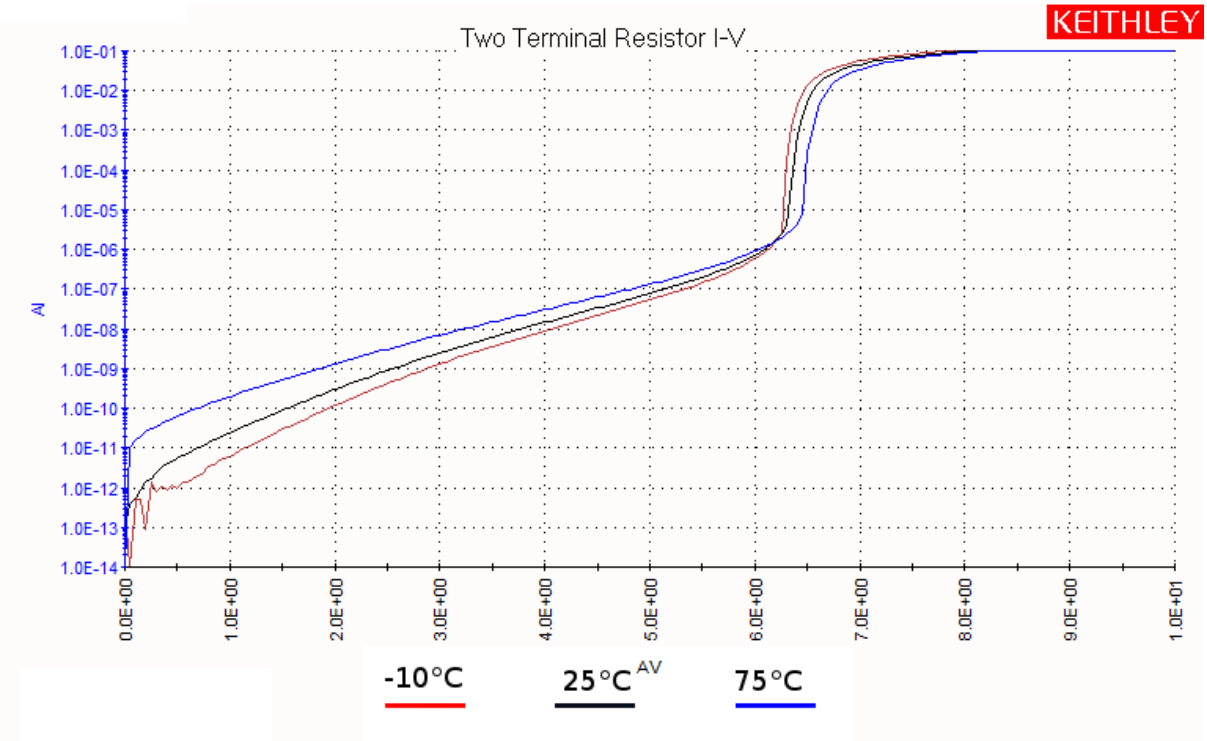

Figure 3.2.1: IV curve for the PMBT2369 transistor at varying temperatures.

The first component to be tested was the PMBT2369 transistor as it is the one used in the previous experiments. Figure 3.2.1 displays the IV characteristics of the transistor at different temperatures and it can be seen that the slope shift to the right as temperature increases. This indicates that the breakdown voltage increases with the temperature and thus the device had a positive temperature coefficient, proving avalanching was the dominant breakdown mechanism.

Based on Figure 3.2.1, the saturation current was actually quite high before going into breakdown (1μA. Two other transistors were tested to see if they had a better saturation currents. Two transistors (BSV52 and BFM520) were tested the same way as the PMBT2369 and their results were plotted in a similar manner. Both components feature a maximum collector-emitter voltage of 5 and 8 respectively, so both should have a breakdown voltage of around those values.

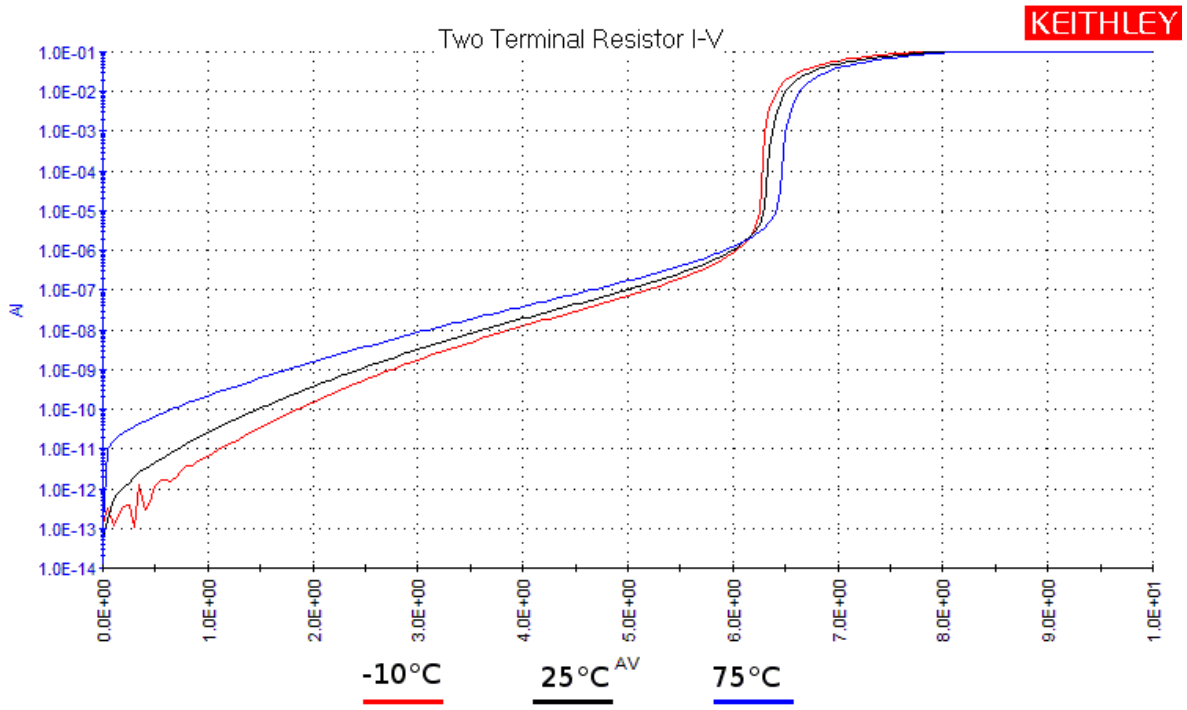

Figure 3.2.2: IV curve for the BSV52 transistor at varying temperatures.

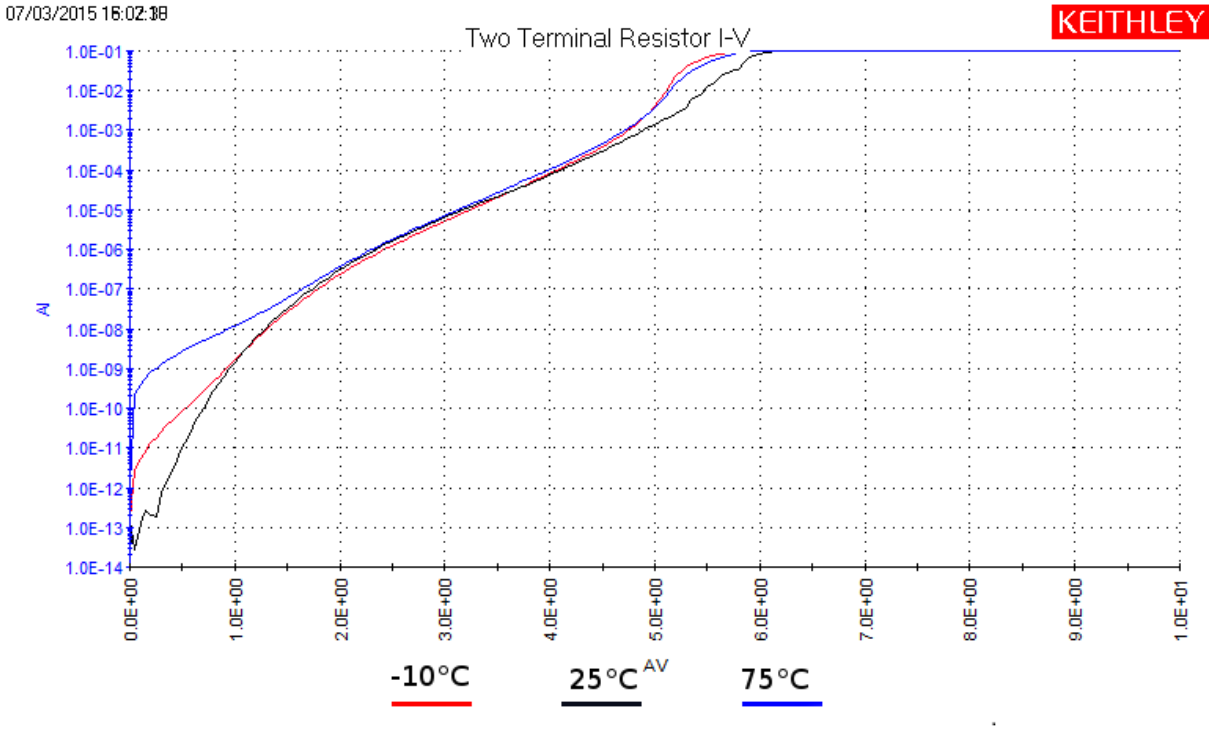

Figure 3.2.3: IV curve for the BFM520 transistor at varying temperatures.

Both graphs shown in Figure 3.2.2 and Figure 3.2.3 feature the results obtained. The BSV52 showed a remarkably similar behavior to the PMBT2369, the saturation current is even the same. The BFM520, however, had a much higher saturation current than

the other two and there was no clear indicator of breakdown. The current through the transistor quickly rose to a value above 0.1A which is above the limit set by the machine.

This showed that the BFM520 was unsuitable for testing purposes and the BSV52 was too comparable to the PMBT 2369 so it should not yield different results when subjected to a block wave so switching experiment was not repeated.

3.3 Evaluation of Experiments

The experiments did not reveal any data to support the presence of a dead time. After investigating the effect of temperature on the breakdown voltage it was shown that the breakdown mechanism was dominated by avalanching and not Zener breakdown so the effect of tunneling electrons should be minor, if not negligible.

A possible solution was proposed by V. Agarwal, that the leakage current could have been the source of high repetition rates. Most papers talk about situations where the leakage current was in the order of pico-ampere but the transistor had 1 μA saturation current which is a magnitude of 10^3 larger.

Unlike a SPAD, the dark count rate is an essential variable that makes the AMLED work. A high dark count rate increases the chances of avalanching when the junction is supposed to be in breakdown. Increasing the dark count rate is done by injecting the depletion region with free carriers whenever the junction is not avalanching. According to Y. Kang et al. the current is actually the source of carrier injection, defined by the following equation [10]:

$N_{DM1} = I_{DM}/q$ (eq.3)

This equation defines the carriers injects N_{DM1} as a function of the dark current I_{DM}, duty cycle τ and the primary charge of an electron q. When assuming a repetition rate of 50MHz there are about 62,500 carriers being injected into the depletion layer during the time the device is not above the breakdown voltage. Each electron has the ability to start avalanching and the paper gives an equation to calculate that probability:

$P_d = 1 - exp(-N_{DM1}P_a)$ (eq.4)

The probability that the dark carriers (P_d) triggers an avalanche is defined as a function of N_{DM1} and P_a, the probability of starting avalanching by every carrier. P_a in this case is equal to $\sim$0.5 according to McIntyre [11] for this system, assuming k is equal to 1. This results in a Pd of $\sim$1, so the carriers injected would avalanche every time the signal pushed the voltage past breakdown and the junction would break down every time. This means that the dark count rate is high enough to keep up with the signal and the finite repetition would be significantly higher than the maximum frequency that can be modulated.

4 Conclusion

In the end, the finite repetition rate of AMLED was not demonstrated in either simulations or in the experiments. The simulations are entirely reliant on the ability of Sentaurus to simulate avalanching while the transistor used in the experiments featured a fairly high saturation current, something that could cause significant carrier injection thus reducing the dead time. Nothing can conclusively be said about the results obtained but there are substantial theories to support the failures of each simulation and experiment.

A possible interpretation of the results is that a high leakage current could actually be beneficial to the switching behavior of an AMLED. The carrier injection would substantially increase the maximum rate of data transfer than can be attained, but it would also increase the power consumption of the device. The reason for using an AMLED was to reduce the energy consumed in the LED in the "off" state. It might not be ideal, but it is worth further exploration to compare the energy efficiency of these types of transistors with forward LEDs.

For future experiments it is suggested to use a simulation program that takes into account the stochastic nature of avalanching in order to observe the finite repetition rate. The dead time is heavily reliant on the probabilities of avalanching and it cannot be properly simulated. There are currently no known programs that do so.

The second suggestion is to find and test a low leakage transistor. The dark count rate is directly proportional to the saturation current and when using a transistor with a low level of leakage the finite repetition might start to become apparent. Most papers talk about situation with a saturation current below 1nA.

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5 Appendices

5.1 Appendix A

The Sentaurus Workbench consists of various tools, of which one a handful will be used in this report. The first tool is the Sentaurus Structure Editor (SDE). Using the custom programming language provided for this program, it is possible to make accurate designs on a microscopic scale.

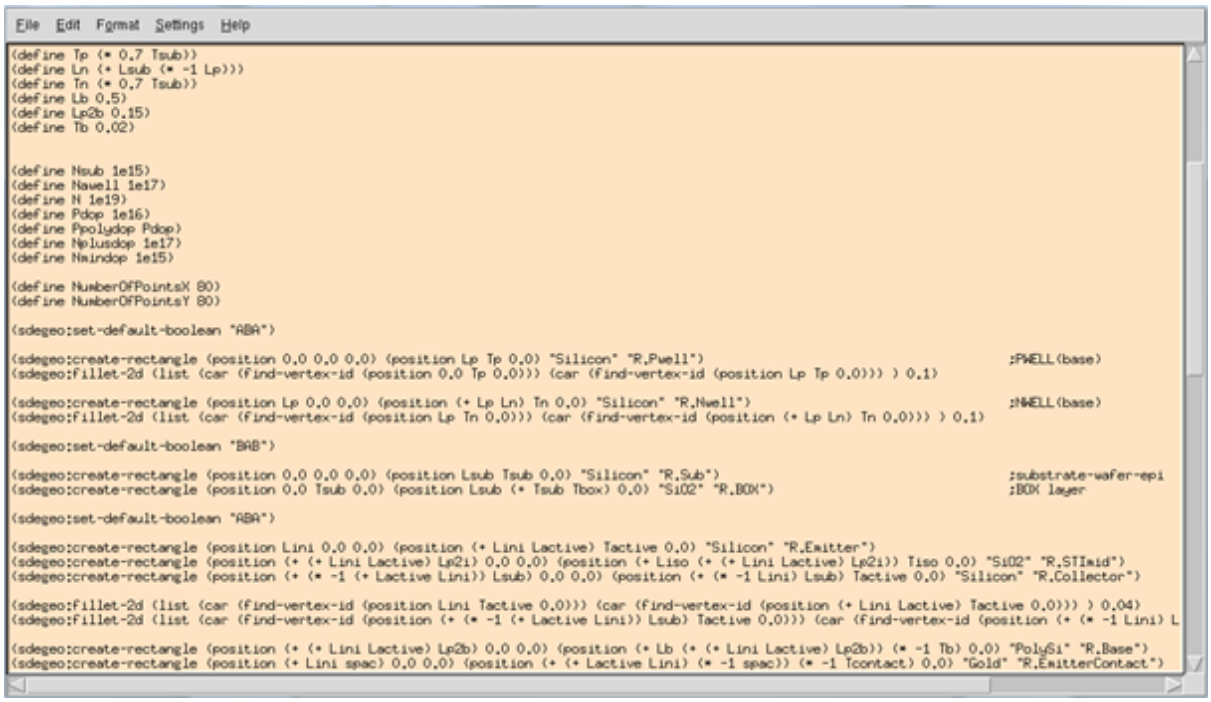

Figure 5.1.1: Sample coding for a BJT junction.

Figure 24 shows a sample code used to create a BJT junction in 2D. The code shown defines various variables that are used to define geometric shapes. These geometric shapes are given material properties, a function provided by the program. It allows for the clear distinction between material types such as Silicon and Glass. Subsequently, it is also possible to specify the doping concentration in each material, allowing for the choice in dopants as well as the amount of dopants added.

The structure must then be meshed into smaller sections so that the properties of the structure can be determined. A smaller mesh means a higher resolution and will most likely result in the most accurate result, but will also increase the time required to simulate the structure in any given conditions.

Once the above is written out, the code is imported in the Sentaurus Structure Editor, a 3D editing program that works much like SolidWorks.

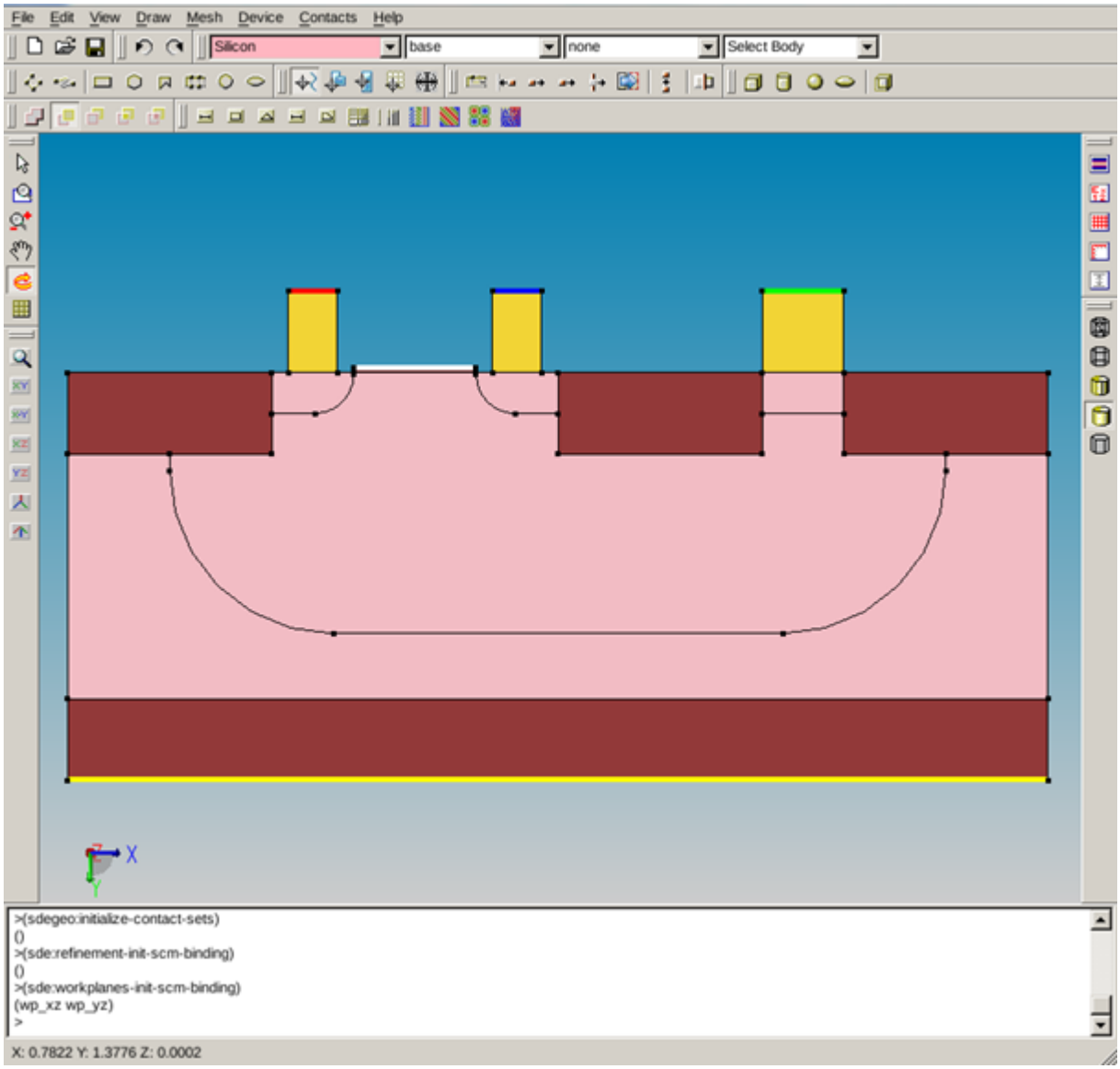

Figure 5.1.2: A design imported to Sentaurus Structure Editor.

The program provides various tools, but it is more time consuming to use the tools provided by the program in order to make an accurate design, thus the structure is usually made in SDE. Figure 25 a design that was made using the coding method, clearly showing the distinction between gold (yellow), Silicon (pink) and glass (brown) areas. It also clearly indicates the different contacts, namely the gate (white), emitter (red), base (green) and collector (blue).

By using the code provided by the Sentaurus manuals it is possible to define the physical limitations and implications of the system. It is possible to include thermal effects, tunneling, gravity, etc. The following image shows which settings were used for most of the simulations in this paper:

```
File {

        Grid="n@node@_parameterized_diode_msh.tdr"

        Plot="n@node@_parameterized_diode_des.tdr"
        Current="n@node@_parameterized_diode_des.plt"
        Output="n@node@_parameterized_diode_des.log"

}

Electrode {
        {Name="emitter" Voltage=0.0}
        {Name="base" Voltage=0.0}
        {Name="bottom" Voltage=0.0}
        {Name="collector" Voltage=0.0}
        *{Name="gate" Voltage=0.0}

}

Physics{
        Mobility(PhuMob eHighFieldSat(GradQuasiFermi) hHighFieldSat(GradQuasiFermi))
        EffectiveIntrinsicDensity(BandGapNarrowing(Slotboom))
        Recombination(SRH(DopingDependence) eAvalanche(Eparallel) hAvalanche(Eparallel)
        Radiative Auger(WithGeneration) ConstantCarrierGeneration (value=1e15))

}



Plot {
        AvalancheGeneration eIonIntegral hIonIntegral eDensity hDensity
        eAlphaAvalanche hAlphaAvalanche eCurrent eDriftVelocity hDriftVelocity hCurrent
        Potential SpaceCharge ElectricField hIonizationIntegral
        Doping DonorConcentration AcceptorConcentration
        AugerRecombination BandGap
        SRHRecombination
        RadiativeRecombination
        TotalRecombination
}

Math {
        Extrapolate
        RelErrControl
        NotDamped=50 Iterations=40
        Number_of_Threads=4
        Digits=5
        ExtendedPrecision(80)
        *BreakAtIonIntegral

        ComputeIonizationIntegrals(WriteAll)
        *CurrentPlot(IntegrationUnit=cm)

}
```

Figure 5.1.3: Settings used in the simulations.

Once the parameters are defined, it is possible to create a signal that will be used for the simulations. The following code was used to make a DC sweep of one of the semiconductors:

```
Solve {
        Coupled{Poisson}
        Coupled{Poisson Electron}
        Save(FilePrefix="Ground_")

        *Ramping V-collector up
        Load(FilePrefix="Ground_")
        Quasistationary
                (InitialStep=0.05 Maxstep=0.05 MinStep=0.001
                Goal {Name="collector" Voltage=-0.7}
                )
        {Coupled{Poisson Electron Hole} }

        Quasistationary
                (InitialStep=0.005 Maxstep=0.005 MinStep=0.0005
                Goal {Name="emitter" Voltage=10}
                *Plot{Range=(0 0.551333) Intervals=50}
                )
        {Coupled
                {Poisson Electron Hole}
                Plot (Time= (0.15; 0.155) NoOverwrite)}
        CurrentPlot(Time=(range=(0 0.1) intervals=100))


}
```

Figure 5.1.4: Signal defining code.

With this it was possible to do a DC sweep of the various semiconductor devices designed before.

5.2 Appendix B

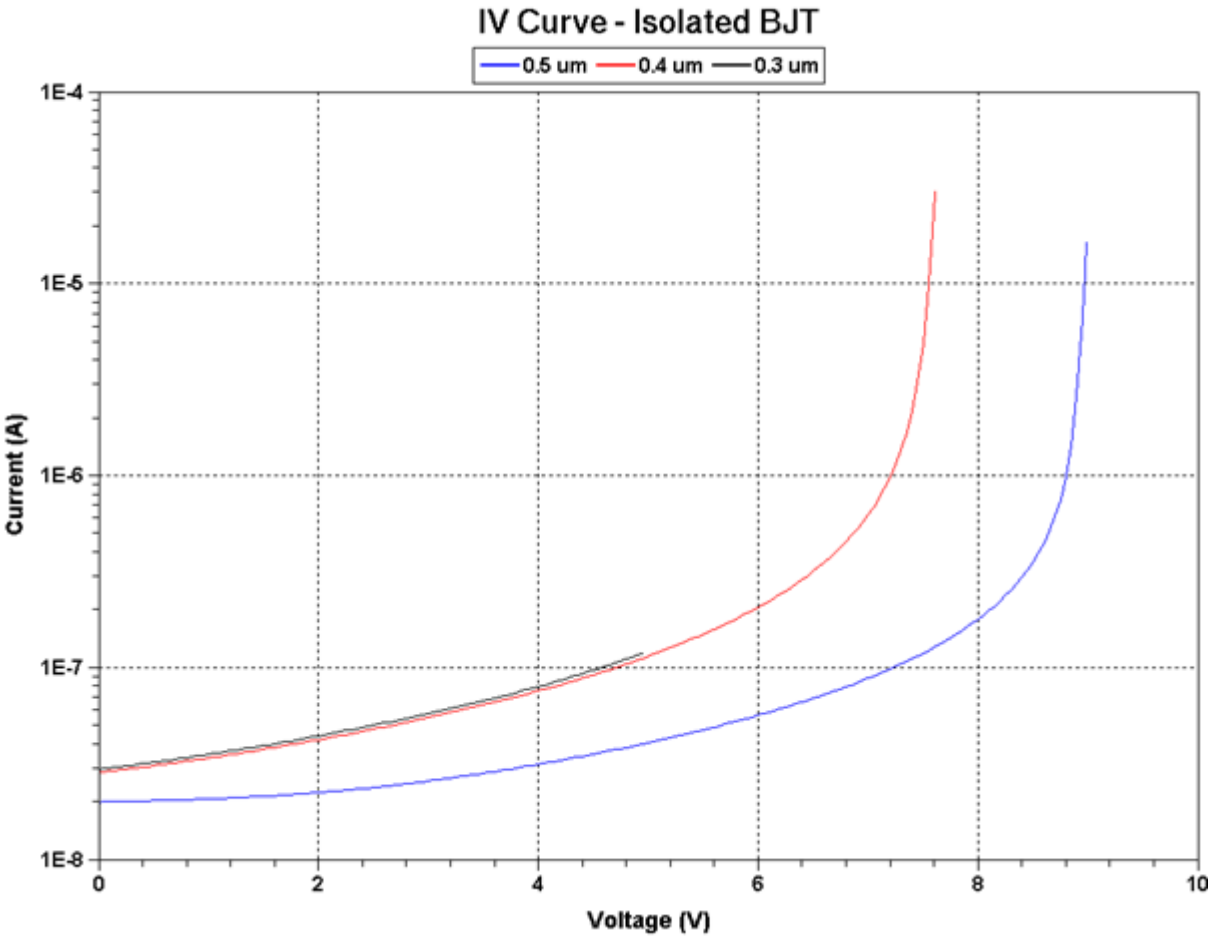

Figure 5.2.1: IV Curves for the three different BJT designs with gate.

5.3 Appendix C

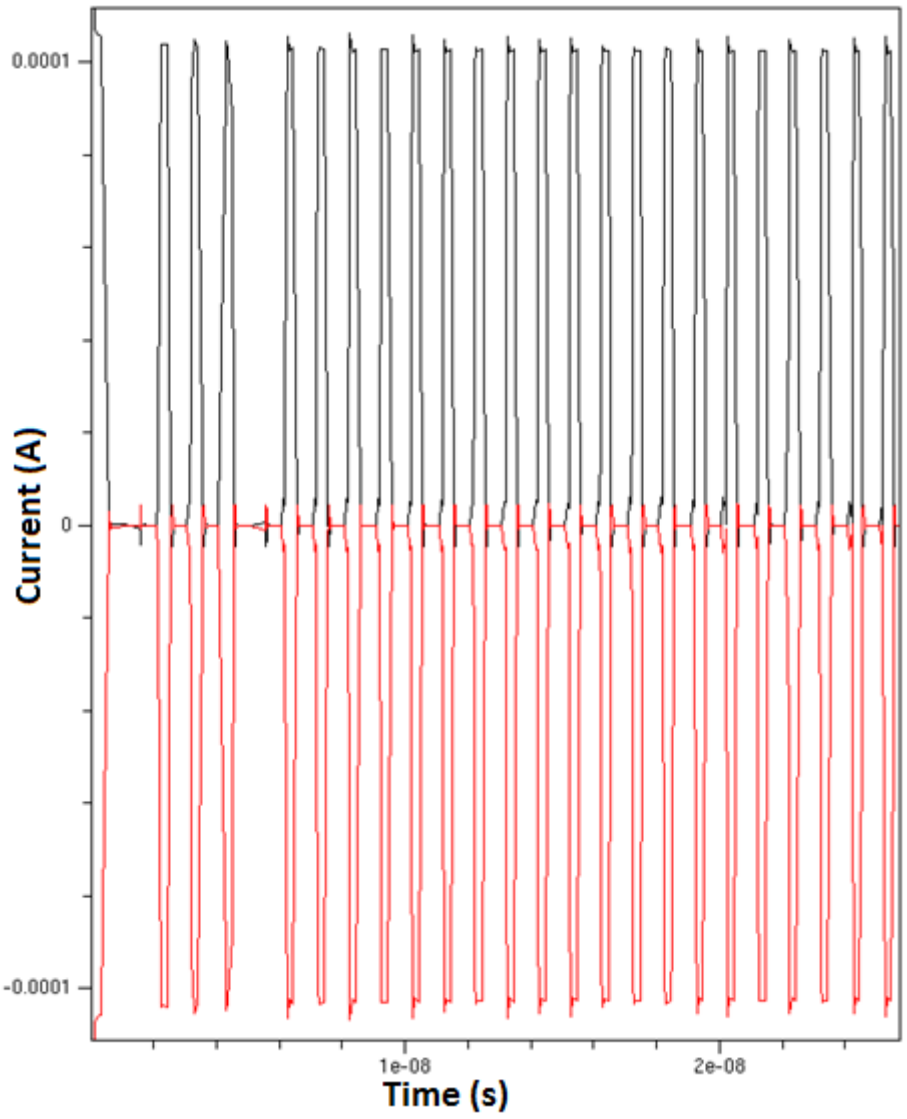

Figure 5.3.1: Missing pulses graph. Could not be replicated.

5.4 Appendix D

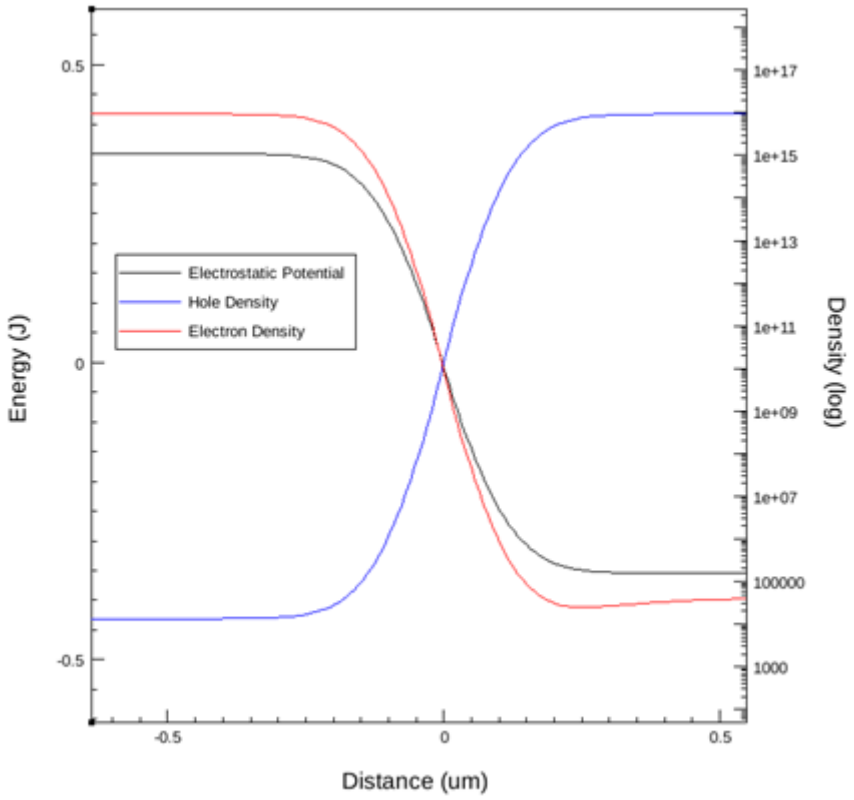

Figure 5.4.1: Carrier concentrations and electrostatic potential for Doping 1.

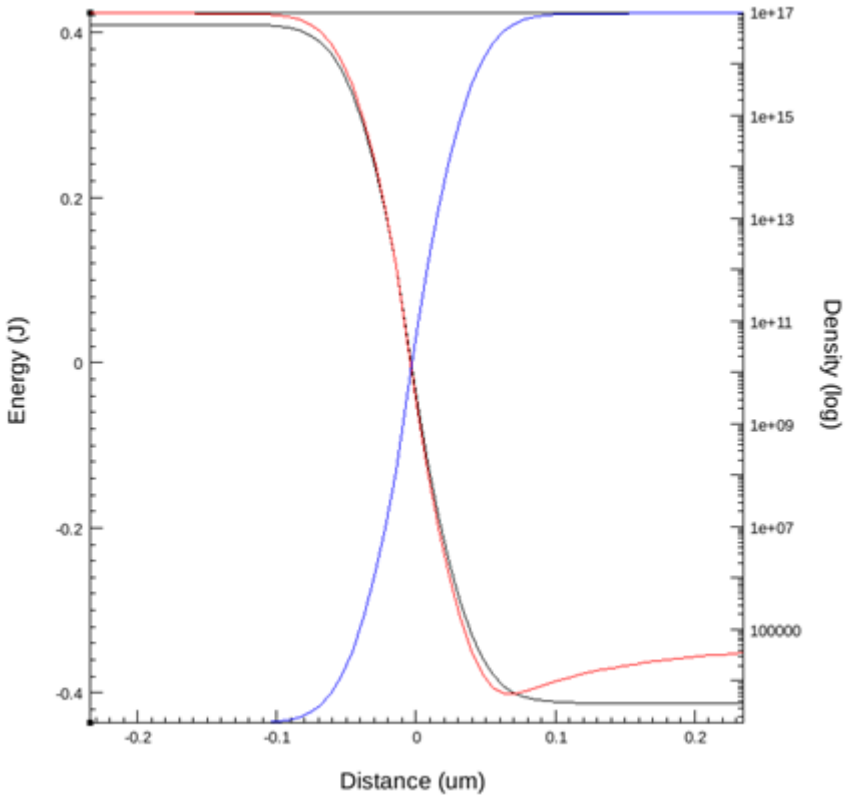

Figure 5.4.2: Carrier concentrations and electrostatic potential for Doping 2.

5.5 Appendix E

This simulation was performed to identify the nature of the large peaks in the experimental data collection. The circuit in Figure 3.0.2 was replicated and made subject to an on off pulse with a frequency of 50MHz.

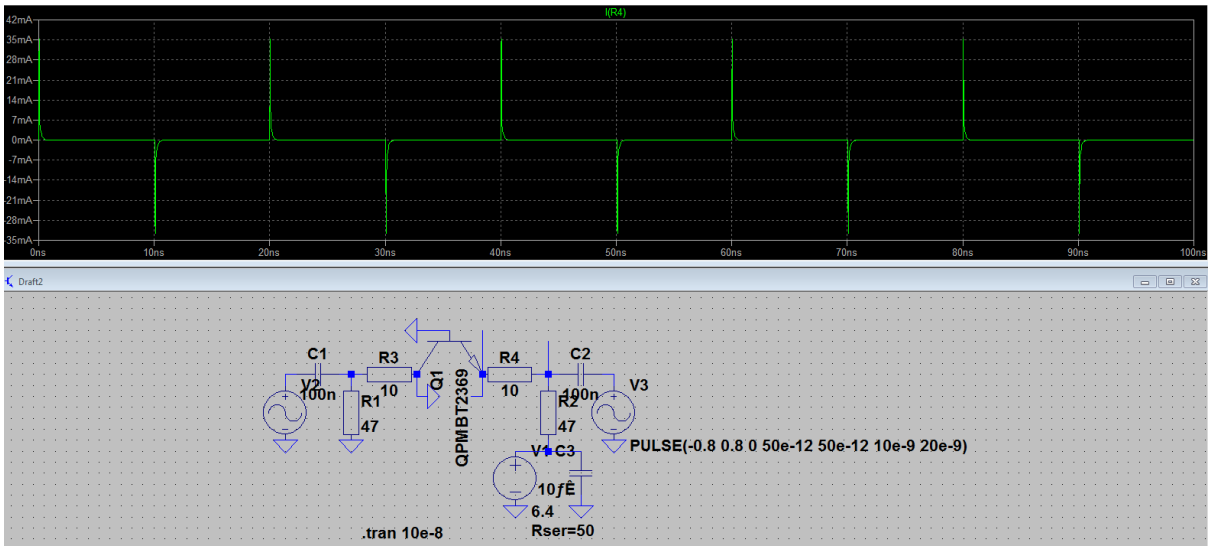

Figure 5.5.1: Simulation Results using LT Spice.

This figure showed that the peaks were within expected results and that the coupling capacitor is charging and discharging in that small amount of time. As the signal became faster, the charging effects became too large and results could not be measured any more.

5.6 Appendix F

The gated design was also used to investigate the effect of the gate voltage on the breakdown voltage, but as this was not used to simulate switching behavior, it was left out of the paper.

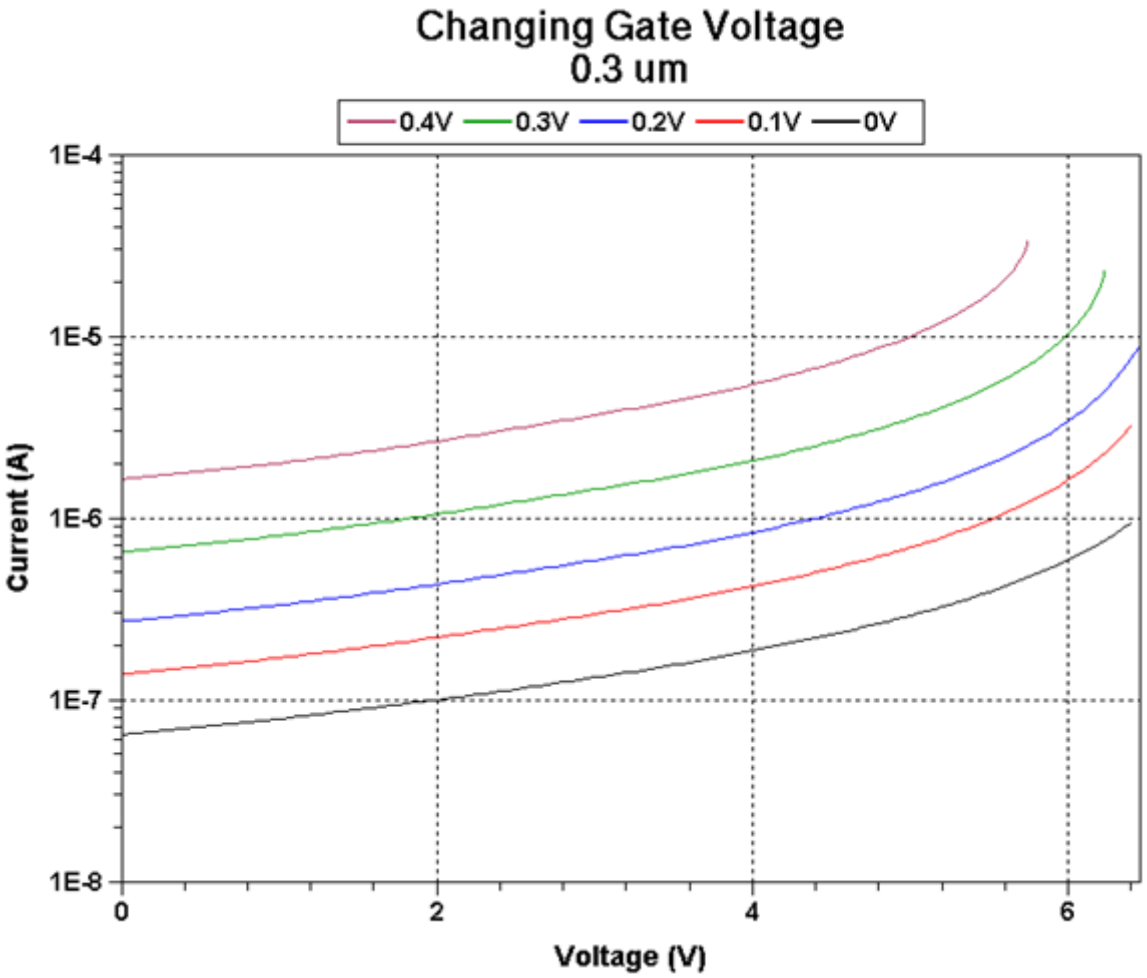

Figure 5.6.1: The IV curves with different Gate Voltages.

This figure clearly showed that the breakdown voltage decreased with an applied electric field (due to the gate voltage) but also gained a substantial amount of leakage current.