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Improving the Linearity of a Single Stage Boost Converter Audio Amplifier

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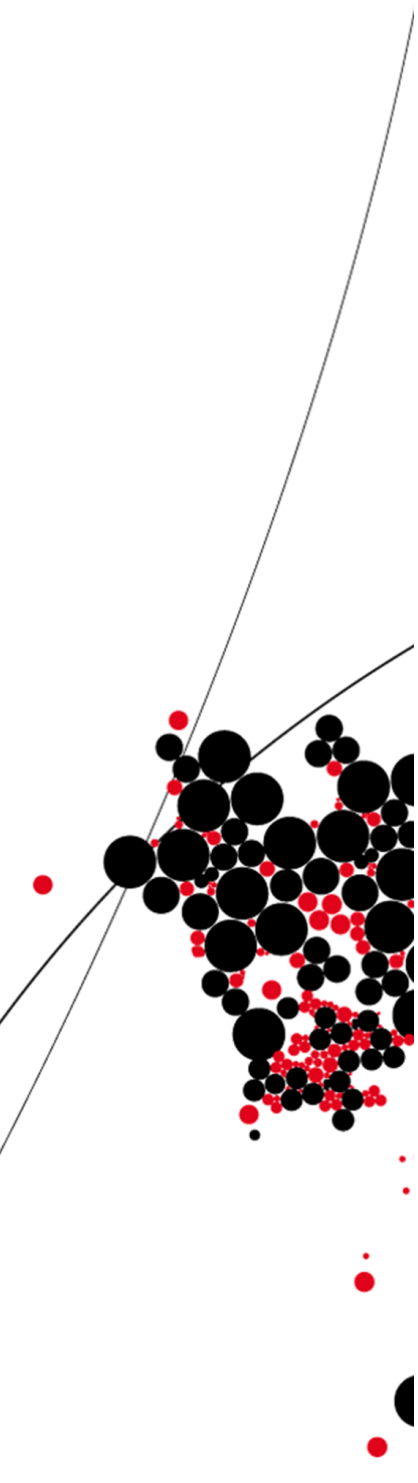

Abstract

Traditionally a two stage implementation (Boost converter + Class D) is used for low voltage supply to high output power audio amplifications. This work proposes an audio amplifier using a boost converter topology only. The goal is to improve overall system efficiency, reduce cost and increase boost converter linearity. In this work general linearization methods are adapted for use in a dynamic boost converter. A double loop feedback structure is used: an inner average current mode control loop sets the inductor current and the outer voltage loop controls the inner loop based on the required output voltage. The large signal behaviour of the current mode controlled converter shows square root behaviour, this square root is pre-distorted in the outer control loop to improve the linearity. A design is made for an amplifier which has a power gain of 5 x compared to a standard single ended class D amplifier. Simulations including parasitic elements show that the closed loop system with pre-distorter has a THD improvement of about 6 for low frequencies. The improvement decreases for higher frequencies, as the output capacitance of the converter reduces the load impedance. The decreasing load impedance influences the effectiveness of the pre-distorter. A prototype is created to compare simulation results to circuit implementation. The measured THD is 0.6 % with versus 1.3 % without pre-distorter at 10 W output power. The results show that for a full bandwidth audio application it is not the best choice to use a boost converter as amplifier, as THD levels are quite high for higher frequencies. Performance is severely limited by the changing bias dependent dynamics, which limit the possible voltage loop gain. As subwoofer amplifier however, a boost converter amplifier is much more feasible.

Nomenclature

ACMC **Average current mode control** is a current programmed control scheme. This scheme sets the duty cycle of switches based on the average current in the inductor

EMC **Electromagnetic Compatibility** is the branch of electrical engineering concerned with the unintentional generation, propagation and reception of electromagnetic energy which may cause unwanted effects such as electromagnetic interference (EMI) or even physical damage in operational equipment.

FFT A **Fast Fourier Transform** algorithm computes the discrete Fourier transform (DFT) of a signal, or its inverse. Fourier analysis converts a signal from its original domain (often time) to a representation in the frequency domain and vice versa.

GBW **Gain-bandwidth product** for an amplifier is the product of the amplifier's bandwidth and the gain at which the bandwidth is measured. For OP-AMPs the gainbandwidth product will also be equal to the unity-gain bandwidth of the amplifier.

PCB A **Printed Circuit Board** mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate.

PCMC **Peak current mode control** is a current programmed control scheme which is widely used in DC-DC converters. This scheme sets the duty cycle of switches based on the peak current in the inductor

PWM **Pulse Width Modulation** is a modulation technique used to encode information into a pulsing signal. This pulsing signal is often made by switching the load on and off at a fast rate. The average of this pulsing signal contains the information.

RMS In physics the **Root Mean Square** is a characteristic of a continuously varying quantity, such as a cyclically alternating electric current, obtained by taking the mean of the squares of the instantaneous values during a cycle. It is equal to the value of the direct current that would produce the same power dissipation in a resistive load.

THD The **Total Harmonic Distortion** of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

List of Symbols

Symbol	Description	Definition
β	Feedback gain	
Δ_{I_L}	Inductor current ripple	
$\Delta_{V_{out}}$	Output voltage ripple	
η	Efficiency	
γ	Pre-distorter in to converter output voltage gain	
$\langle I_C \rangle$	Average steady-state output capacitor current	
$\langle I_L \rangle$	Average steady-state inductor current	
$\langle V_L \rangle$	Average steady-state inductor voltage	
ω_0	Primary pole frequency	
ω_{rhpz}	Right half plane zero frequency	
ϕ_{boost}	Required phase boost at the crossover frequency in the voltage loop compensator	
A	Forward gain	
C_o	Output capacitance	
C_p	Pole capacitor in a type 2 compensator	
C_z	Zero capacitor in a type 2 compensator	
D_c	Duty Cycle	$D_c = \frac{P_s}{T_s}$
D_c'	1-D_c	
D_m	Duty cycle limit which is allowed for stability	
$D_{c,H\to L}$	Duty cycle high to low transition	
$D_{c,L\to H}$	Duty cycle low to high transition	
f_c	Loop gain crossover frequency	
f_s	Switching frequency	$f_s = \frac{1}{T_s}$
G_{DC}	DC-gain of the transfer function	
I_c	Control current of the current mode loop	$I_c = \frac{V_c}{R_s}$
I_L	Inductor current	
I_C	Output capacitor current	
$I_{L,max}$	Maximum inductor current	
I_{R_L}	Output resistor current	
k	Necessary separation between the pole and zero frequency positions in the voltage loop compensation network	
K_f	Proportional gain of a type 2 compensator	
L	Inductor	

M	Current/voltage boost converter transfer ratio
M_1	Slope of the inductor current during on period
M_2	Slope of the inductor current during off period
M_c	Slope of the external ramp
P_s	Period the bottom switch is active
Q	Quality factor
Q_{gate}	Total MOSFET gate charge
R_L	Output load resistance
R_s	Current sense gain
R_z	Zero resistor in a type 2 compensator
$R_{\Theta JA}$	Silicon junction to ambient thermal resistance
$R_{ds,on}$	MOSFET drain-source resistance in the on state
R_{esr}	Equivalent inductor series resistance
R_{lower}	Bottom voltage loop feedback divider resistor
R_{upper}	Top voltage loop feedback divider resistor
S_n	Switch
T_s	Time of one switching period
T_{loop}	Feedback loop gain, also $A\beta$
V_{bias}	Output voltage bias level
$V_{c,pd}$	Pre-distorted control voltage of the current loop
V_{comp}	Type 2 compensator output voltage
V_c	Control voltage of the current loop
V_{DD}	Power supply
V_{dist}	Distortion voltage
V_e	Feedback loop error voltage after summation point
V_{gs}	MOSFET gate source voltage
V_L	Inductor voltage
V_{OUT}	Amplifier output voltage
V_{ramp}	Amplitude of the PWM ramp
V_{ref}	Input signal of the amplifier

Contents

Chapter 1

Introduction

Audio amplifiers have been around for more than 100 years, however their topology has not changed much over the years. Linear output stage amplifiers (Class A, Class AB) were the norm until switch mode amplifiers were introduced. The switching amplifier or so called Class D amplifier was first proposed in 1958[1] and has become increasingly popular for power efficient applications.

Linear output stage amplifiers have a very poor efficiency, with a theoretical maximum efficiency of 25% for Class A and 78.5% for Class AB amplifiers. Class D increases the maximum theoretical efficiency to 100 %.

In all cases the maximum voltage swing at the output of the amplifier is limited to the supply voltage. In some cases the supply voltage is fixed, for example in a car where the nominal battery voltage is 12 V. It immediately follows that the maximum power is therefore also fixed because in audio applications the load impedance is fixed (often 4 Ω or 8 Ω). When more signal swing is required the only possible option is to increase the supply voltage.

Traditionally a boost-converter is used to generate a higher supply voltage and a second power stage (often Class D) is used to generate the audio signal as shown in figure 1.1. This principle is then applied in cases where supply voltage is limited, and more output power is required, for example in mobile phones, portable audio systems and as mentioned before car radio.

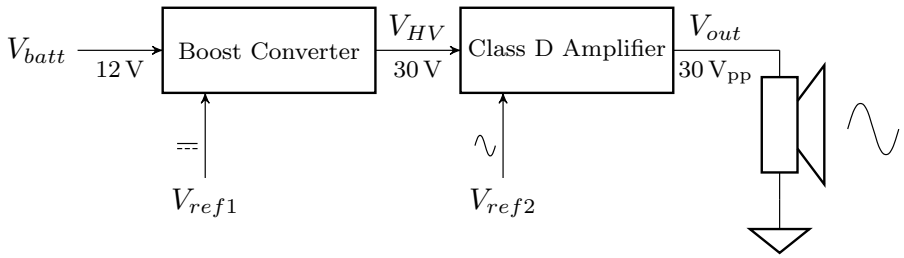

Figure 1.1: Traditional setup of an audio amplifier chain when more output power is required. The limited supply voltage is boosted and then fed to the audio amplifier itself.

In the two stage design any audio power stage can be used but normally in the type of applications mentioned a Class D power stage is used for efficiency and compactness. This power stage is based on the PWM principle: switching very fast between the supply and ground and then filter the signal to generate an average audio signal. This requires two transistors for switching and usually an inductor plus capacitor for filtering.

A boost converter also works by switching, in this case an inductor is charged and discharged in a buffer capacitor to generate a higher output voltage. The output voltage is compared to a reference which controls the switching. Without the controller this circuit also requires two transistors and an inductor plus buffer capacitor. Which makes up for the bulk of the space requirements and cost of the circuit.

Despite the high efficiency of Class D amplifiers and boost converters, a cascade of a boost converter and Class D amplifier will reduce the overall efficiency of the system. If signal generation can be performed with a boost stage, the overall efficiency would be higher and component count and system cost can be reduced. This principle is shown in figure 1.2. The challenge becomes the linearity requirement of the amplifier as boost converters are inherently very non-linear.

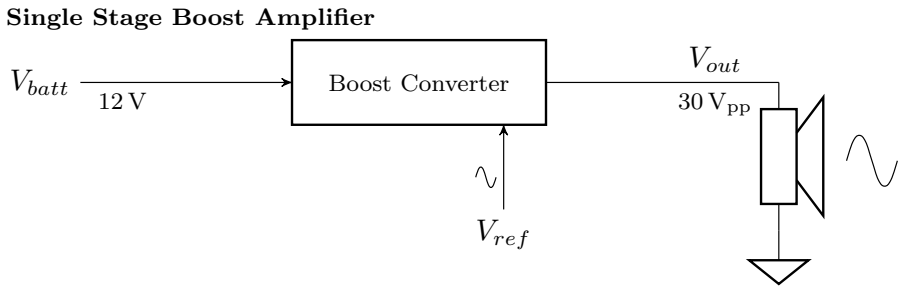

Figure 1.2: Proposed structure for generating an audio signal with a single stage boost converter amplifier. The audio signal is directly generated by the boost converter.

Throughout this thesis a full analog design is made, keeping car audio in mind. This means that the supply will be a 12 V (battery) source.

1.1 Motivation

The controller of the boost converter will try to make the output voltage equal to the reference voltage. If the reference voltage is made variable, the boost converter could be directly used to generate an audio signal with the same swing as in the two stage system. The (Class D) power stage could then be omitted completely. This cuts the component count and therefore reduces the space requirements and costs of the amplifier. This is especially important in applications where space is an issue, in mobile phones and hearing aids for example. As mentioned before, the efficiency is also increased when one stage is omitted, this is especially important in mobile applications.

A single stage is also beneficial in cases where piezo-electric speakers need to be driven, as they require a high operating voltage[2] due to their high impedance. Under water sensor nodes for example need to work a long time from a single battery charge and use piezo-electric elements for communication, the efficiency gain by using a single stage would be very welcome.

One of the major challenges in using a boost converter as an amplifier is the highly non linear control to output voltage transfer. This results in harmonic distortion at the output of the converter, unwanted in linear audio applications.

The aim of this thesis is to study the non-linear behaviour of a boost converter and investigate techniques to make the boost converter more linear for use in audio applications. The goal is to create a fully analog amplifier with an equal THD (Total Harmonic Distortion) figure as a Class D amplifier used for the same application (car audio).

1.2 Thesis Outline

The core of this research is focused on the linearization of a boost converter implemented as audio amplifier. In chapter 2 common linearization techniques are given and the common forms of control for boost converters are described. In the same chapter work from literature is examined to see what has been done before.

In chapter 3 the large signal non-linear behaviour of different current mode control schemes is examined. This is new and has not been done before in literature.

In chapter 4 a design is proposed based on the findings of the prior chapters. This design is simulated and the improvement of different linearization techniques is shown. Next the design is mapped on components and a prototype is made in chapter 5. Measurements are then compared to simulation.

Finally in a concluding chapter (chapter 6) the whole process is summarized and evaluated, based on this evaluation recommendations are given for future work.

Chapter 2

Existing linearization techniques

How can the problem of linearizing a boost converter be addressed? It is of interest to know what has been done in literature and investigate the theory behind the linearization of boost converters. Both will be discussed in this chapter.

The default solution for linearization is feedback. Feedback makes the system behave correctly in the presence of parasitics, improves non-linearities and reduces the sensitivity for component variations. For boost converters different forms of control can be used. Most of the control schemes include feedback in order to minimize the effect of circuit parameters on output voltage. In section 2.3 three control schemes which work by the use of feedback are presented.

A second option for linearization is pre-distortion. Pre-distortion can be an effective way to reduce the error and is used in a feed-forward kind of way. This makes pre-distortion however sensitive for component variations. A detailed explanation about pre-distortion is given in section 2.5.

These two forms can also be combined to reduce distortion even further by integrating a pre-distorter into the feedback loop which brings the best of both worlds.

The boost converter power stage is introduced first, whereupon control methods for this power stage using feedback are discussed next. Existing implementations of pre-distortion for a boost converter are shown and then the combination of feedback and pre-distortion is discussed.

2.1 Boost Converter Power Stage

Switched mode converters work by regulating either output voltage or current by switching storage elements, like inductors and capacitors. These elements can be configured into different electrical configurations which results in a different transfer from input to output. Not only the configuration of the elements is important, the transfer also depends on the component values itself.

There are three main basic topologies, a boost switched mode converter is used to step-up the supply voltage to a higher voltage. A buck switched mode converter will step-down the supply voltage to an output voltage lower then the supply voltage and finally a buck/boost switched mode converter can step-up and step-down the supply voltage. For audio amplification the selection is limited to converters which can create a higher output voltage(boost, buck/boost) with respect to the supply voltage. A (synchronous) buck converter is actually already used as an audio topology, namely Class D. In this thesis the focus is on boost converters because of the generally more simple structure in comparison with buck/boost converters. Buck/boost converters also invert the supply voltage which is problematic for an IC-realization.

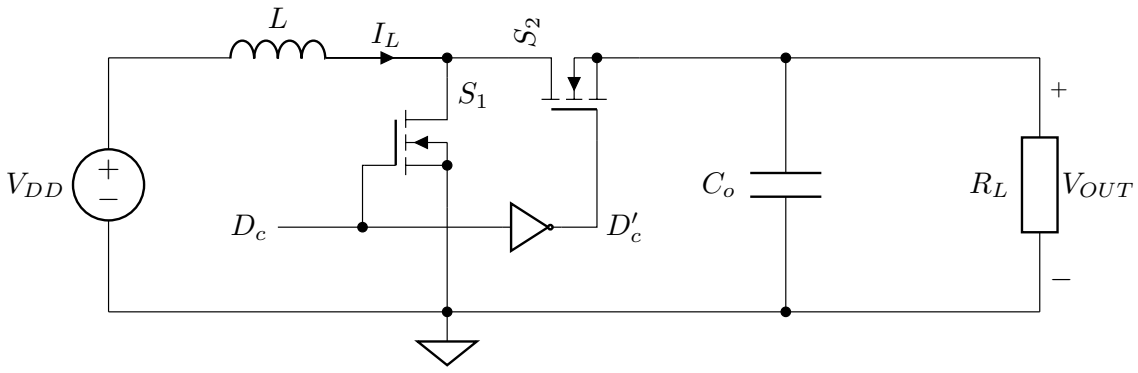

Figure 2.1: Simplified synchronous boost converter. This circuit is agnostic for the way it is controlled, the control vector is the duty-cycle input. This structure with the switches, inductor and output capacitor is also called the power stage.

By switching storage elements (see figure 2.1) the current and voltage from input to output can be controlled. This will be the control vector for amplifying the audio signal. There are problems as mentioned in the section above, such as a non-linear control to output functions and duty cycle dependent small signal dynamics. These problems will be discussed in further chapters.

The basic structure of a boost converter is shown in figure 2.1. In this case a synchronous boost converter is shown, where synchronous means that the top and bottom switch are switched in anti-phase. In the non-synchronous case switch S_2 is replaced by a Schottky-diode. The problem with non-synchronous rectification is that the current flow is unidirectional, for audio amplification it is required to have a bi-directional current flow to be able to source and sink current to and from the speaker. Another advantage of synchronous rectification is the improved efficiency[3], this is the result of lower $R_{ds,on}$ resistance.

The definition of duty cycle (D_c) is the amount of time the bottom switch (S_1) is closed. $D'_c(1-Dc)$ will be the amount of time the top switch is conducting. This will be the case throughout this work and symbols D_c and D'_c will be used respectively.

As mentioned before a boost converter works by switching storage elements. In steady-state two rules always hold: volt-second balance and current-second balance or charge balance. This means that in equilibrium the average voltage over the inductor is zero and the average charge into the capacitor is also zero[4, p. 25]. The balance equations can be used to calculate the input to output voltage transfer functions. The balance equations are:

$$\langle V_L \rangle = \frac{1}{T_s} \cdot \int_0^{T_s} V_L(t)dt = 0$$
$$\langle I_C \rangle = \frac{1}{T_s} \cdot \int_0^{T_s} I_C(t)dt = 0$$

The waveforms representing the balance equations are shown in figure 2.2. It can be seen that the cycle integral over both waveforms is always zero. In the next part of this section the amplitude of these waveforms is derived.

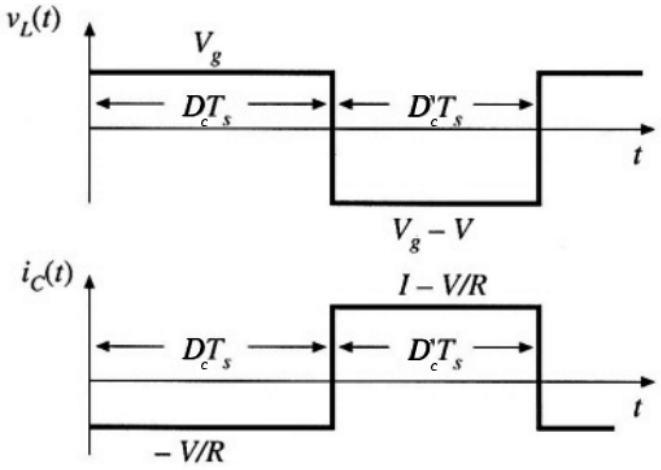

Figure 2.2: The boost converter balance waveforms. It can be seen that the voltage and current integral over 1 cycle is always zero[5].

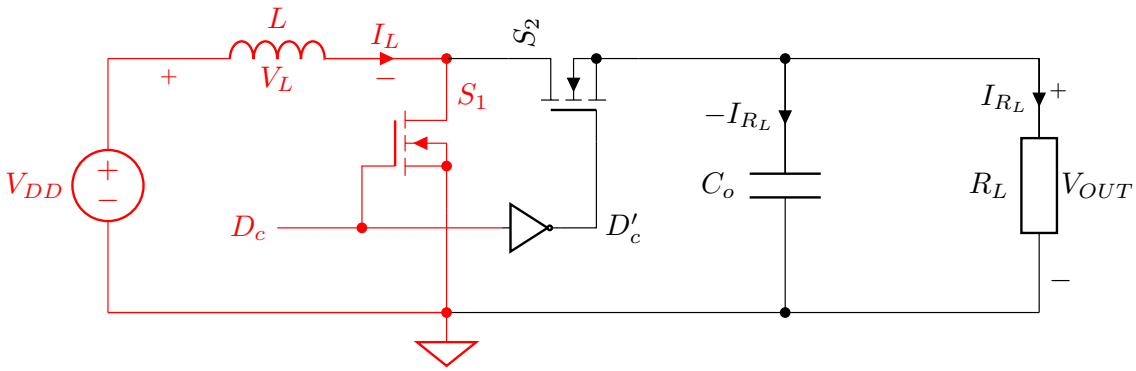

Figure 2.3: State 1 of the synchronous boost converter, in this state the inductor is charged and the current for the load is supplied by the capacitor.

In state 1 (figure 2.3) the inductor is charged and the load current is supplied by the capacitor. The voltage over the inductor in state 1 is the supply voltage. The capacitor supplies the load.

$$V_L = V_{DD}$$
$$I_C = -I_{R_L} = -\frac{V_{OUT}}{R_L}$$

In state 2 (figure 2.4) the inductor is discharged into the output capacitor and the load current is also supplied by the inductor. The voltage over the inductor in state 2 is the difference between the supply voltage and the output voltage. The capacitor is charged in this cycle.

$$V_L = V_{DD} - V_{OUT}$$
$$I_C = I_L - I_{R_L} = I_L - \frac{V_{OUT}}{R_L}$$

These two states can then be applied to the volt-second and charge balance:

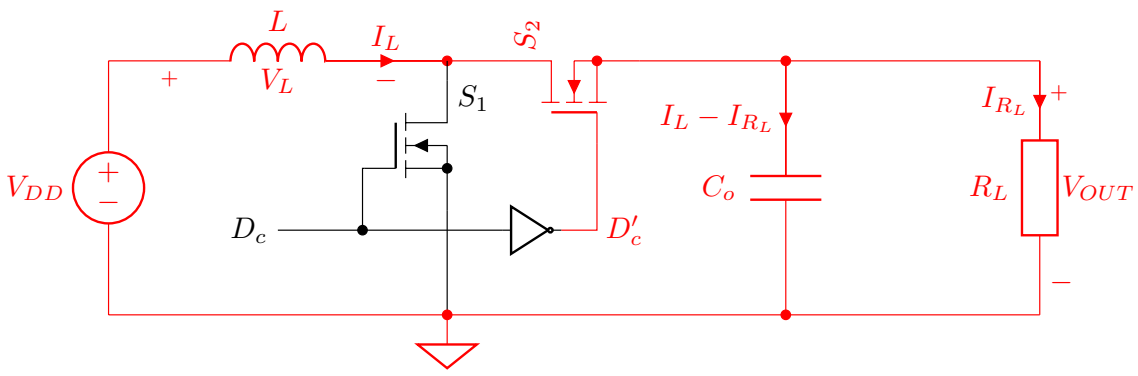

Figure 2.4: State 2 of the synchronous boost converter, in this state the inductor is discharged in the output capacitor recharging the capacitor in the process.

$$\langle V_L \rangle = \frac{1}{T_s} \cdot \int_0^{T_s} V_{DD} \cdot D_c t + (V_{DD} - V_{OUT}) \cdot D'_c t \; dt = 0$$
$$\langle V_L \rangle = V_{DD} \cdot D_c + (V_{DD} - V_{OUT}) \cdot D'_c = 0$$
$$\langle I_C \rangle = \frac{1}{T_s} \int_0^{T_s} -I_{R_L} \cdot D_c t + (I_L - I_{R_L}) \cdot D'_c t \; dt = 0$$
$$\langle I_C \rangle = -I_{R_L} \cdot D_c + (I_L - I_{R_L}) \cdot D'_c = 0$$

From these equations the inductor current vs load current relation is found:

$$I_{R_L} \cdot (D_c + D'_c) = I_L \cdot D'_c$$
$$\frac{I_{R_L}}{1 - Dc} = I_L \tag{2.1}$$

The volt-second balance can then be rewritten to get the supply-to-output voltage transfer function M:

$$0 = V_{DD} \cdot D_c + (V_{DD} - V_{out}) \cdot D'_c$$
$$0 = V_{DD} - V_{out} \cdot D'_c \text{ (where } D_c + D'_c = 1)$$
$$M = \frac{V_{out}}{V_{DD}} = \frac{1}{D'_c} = \frac{1}{1 - D_c} \tag{2.2}$$

Transfer function M is plotted in figure 2.5. Here it is already evident that controlling the converter based on duty-cycle gives much distortion because the transfer function is highly non-linear. From this graph it is also clear that the output voltage can never be lower than the input voltage, M is always larger than one.

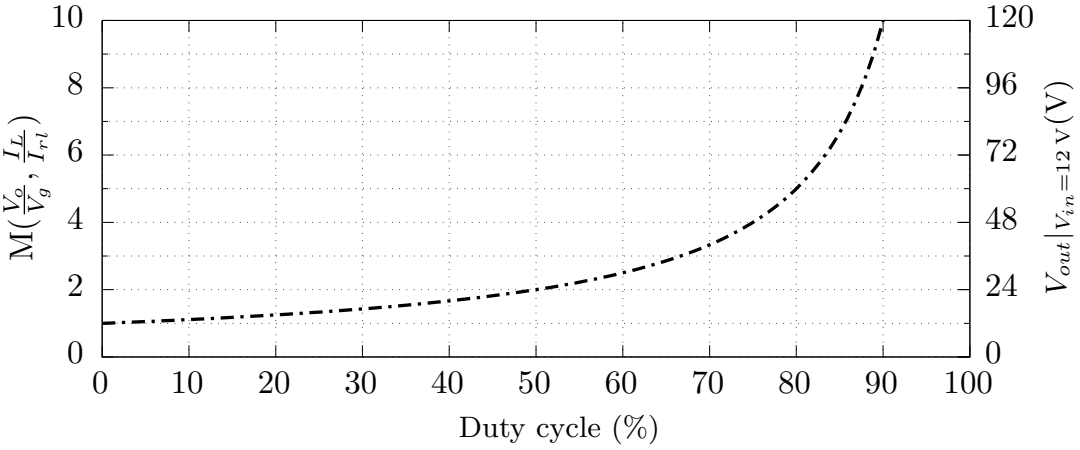

Figure 2.5: Voltage transfer of a ideal boost converters, with asymptotic behaviour when D goes to 1. This transfer is highly non-linear as can be seen.

The maximum M which can be achieved in practical situations is about 5-6[5, p 45], this is determined by losses in the system. These losses pose a limits to the maximum output voltage of the amplifier and therefore the maximum swing of the audio signal.

The calculations done in this section are the basis of the large signal transfer characteristics of the boost converter and will be used throughout this thesis.

Large and small signal dynamics

For the boost converter it is important to look at large signal behaviour and small signal behaviour. The large signal behaviour is important if a pre-distorter needs to be designed as a large signal model is needed to derive the inverse gain and phase functions of the amplifier.

The small-signal dynamics are of importance for designing feedback and stable operation of the control loop. A boost converter has very complex dynamics. As can be seen in the next sections these dynamics depend on component values and parasitics but are also largely depended on operating conditions (duty cycle, load resistance). It is important to know limiting factors because those will later help in designing the feedback around the converter and to make sure the control loop is stable in all cases.

The power stage of a boost converter always has a dominant pole which limits the total bandwidth of the converter. This primary pole depends on the type of control scheme used and is mostly a function of R_L and C_o.

Right Half Plane Zero

One small signal effect which is very limiting is the right half plane zero, inherent to boost and buck/boost converters. This refers to a zero in the right half of the Laplace plane. It is a small signal effect and makes feedback design difficult, this RHPZ will thus be encountered in this work when the feedback loop is to be closed and therefore some information is given.

The right half plane zero differs from a tradition zero, which lies in the left half of the s plane. A normal zero will boost the phase and gain but a right half plane zero will boost the gain and lags the phase further down quickly destroying phase margin[4, p 127].

From a large-signal perspective the right half plane zero can be seen in the following way: if there is a transient step up in duty-cycle the output voltage will first decrease. This is the result of the indirect energy transfer principle of a boost converter. When the duty cycle increases, the inductor is charged longer. In that period the load will pull more charge from the capacitor dropping the output voltage.

This effect more or less depends on the size of the inductor (how fast can it be charged to diminish the effect) and the load resistance (how much current does the load need). Later the exact equations for the right half plane zero are given.

2.2 A measure for distortion

A good audio amplifier should in the ideal case be completely linear. This means that the output signal $V_{out} = A \cdot V_{in}$, where A is the amplification factor or gain. Non linearities in the amplifier introduce distortion. If for example an ideal sine is applied to the control input of the open loop boost converter from section 2.1 the distortion of the sine wave is clearly visible, the result is shown in figure 2.6.

A measure for distortion can be given by looking at the harmonics of the output signal of a system. In a completely linear system there will be no harmonics, in a system with a non-linear transfer curve harmonics will be present. The total harmonic distortion (THD) is then defined by the following equation:

$$\%\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 ... + V_n^2}}{V_1} \cdot 100\% \tag{2.3}$$

Equation 2.3 gives the ratio of harmonic content with regard to the fundamental frequency. $V_1 ... V_n$ are the corresponding RMS voltages, where V_n is the RMS voltage of nth harmonic and n = 1 is the fundamental frequency. It will be used throughout this thesis as a performance metric of the amplifier. It is important to note that this equation does not include the noise terms, this is another measurement called total harmonic distortion plus noise (THD + N) shown in equation 2.4.

$$\%\text{THD + N} = \frac{\sqrt{V_2^2 + V_3^2 ... + V_n^2 + V_{noise}^2}}{V_1} \cdot 100\% \tag{2.4}$$

The noise must be integrated over the measurement bandwidth, for audio this is often 100 kHz[6, p. 85]. However THD + N will not be used as performance metric here because it will make comparison to simulations impossible due to the piecewise linear nature of the SIMPLIS[7] simulator. SIMPLIS does not include noise simulations so only THD can be measured in simulation. The measurements of the prototype are also pure THD, not THD+N, for a fair comparison.

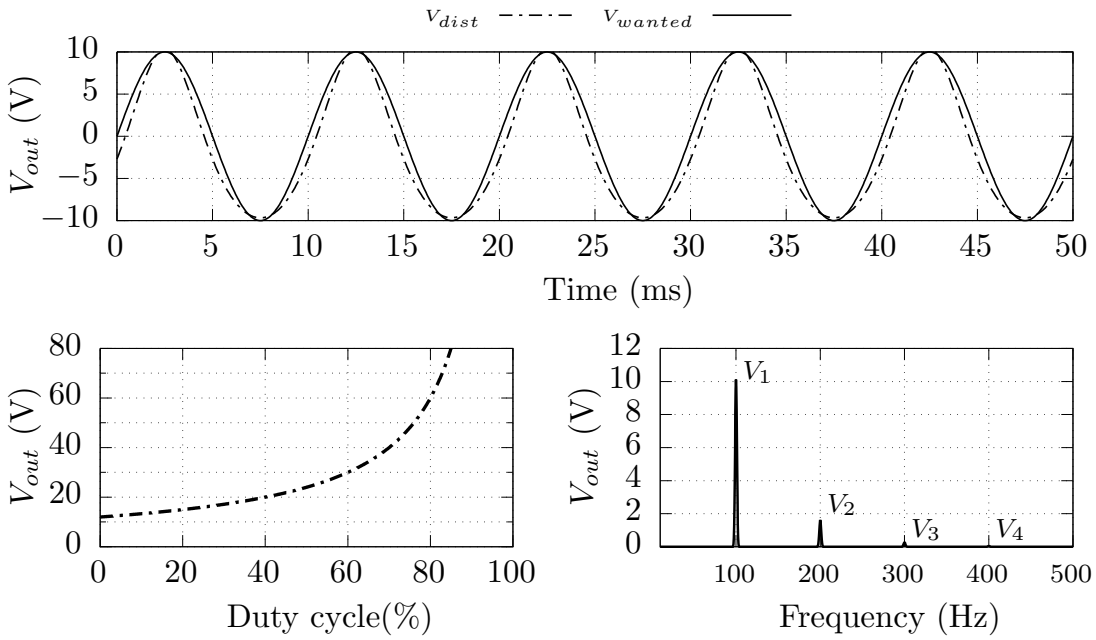

Figure 2.6: The result when an ideal sinusoidal duty cycle is applied to the control input. The output is biassed at 30 V and the mean is subtracted before plotting. The bottom of the sine is compressed and the top is expanded, the wanted output in is shown in solid black. The amplitude spectrum of the distorted signal is shown in the last graph, showing the distortion component amplitudes.

Using a Fast Fourier Transform(FFT) the distortion components V_2, V_3, V_4 etc. can be determined, this is shown in the last graph in figure 2.6. The open loop boost converter has predominantly second order distortion. The total TDH of the V_{dist} signal is calculated as approximately 17 %.

For practicality reasons in all simulations and measurements the fundamental frequency is compared to the first two even and the first two odd distortion components. This means that 4 harmonics are used to calculate the THD. However all the distortion components are looked at and it is verified that the first four distortion components are indeed dominating the THD figure.

2.3 Feedback

As mentioned before, negative feedback is an effective way of reducing distortion and making the system resistant to circuit variations. The general structure of negative feedback is shown in figure 2.7. The scaled output voltage is compared to the reference voltage and they are made equal. Disturbances inside the loop such as noise and distortion which appear at the output are reduced by the loop gain.

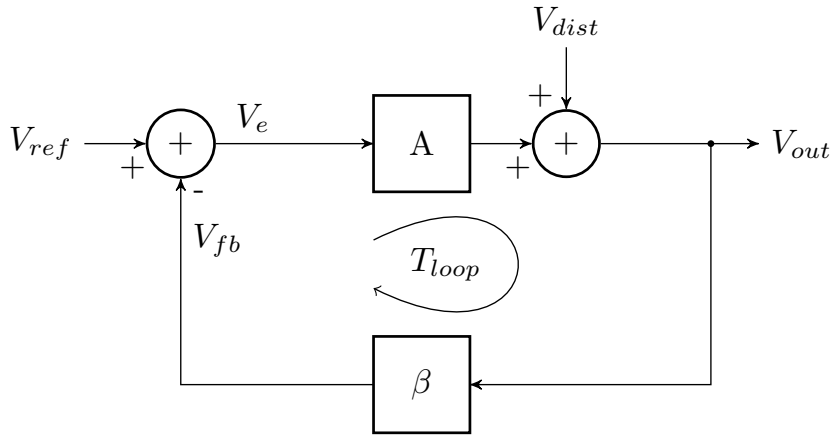

Figure 2.7: Block view of negative feedback. Harmonic distortion components (V_{dist}) are modelled as an addition inside the feedback loop.

Negative feedback can be mathematically described as:

$$\begin{aligned} V_{out} &= A(V_{ref} - \beta V_{out}) + V_{dist} \\ V_{out}(1 + A\beta) &= AV_{ref} + V_{dist} \\ V_{out} &= \frac{A}{1 + A\beta}V_{ref} + \frac{1}{1 + A\beta}V_{dist} \end{aligned} \tag{2.5}$$

Equation 2.5 shows that the harmonic distortion components are suppressed with the factor $1+A\beta$, reducing the total harmonic distortion.

The loop gain is defined as T_{loop} in figure 2.7, in this case the gains A and β are multiplied for a total loop gain of $A\beta$.

For large A and therefore large loop gain expression 2.5 reduces to:

$$\lim_{A\to\infty} V_{out} \approx \frac{1}{\beta}V_{ref} + 0 \cdot V_{dist} \tag{2.6}$$

It can be seen that the distortion voltage is completely removed from the output signal. To suppress the distortion and thereby linearize the amplifier it is therefore imperative to have a large loop gain. The distortion components are reduced by the factor $1 + A\beta$.

Stability

In negative feedback systems, stability is a challenge when loop gain is increased as much as possible. In real systems, A is dependent on frequency and introduces a phase shift.

As can already be seen from equation 2.5, there is a problem when $A\beta$ becomes -1. This can happen when the phase of the output signal lags 180° with respect to the input signal and the value of $A\beta$ equals 1. This is a possibility when the designed loop gain is too big and the combined phase shift of A and β is large enough.

For a stable audio amplifier there should be enough margin between the phase of the loop and $-180°$ at the point where the loop gain is unity. This margin is called phase margin. It's conjugate is called gain margin, this margin takes the difference in gain between unity and the gain found at the $-180°$ point.

This should be kept in mind when designing feedback for systems including a boost converter. The forward gain A might needs extra compensation components in the feedback gain β for satisfying the stability criteria mentioned above. This compensation can for instance add a positive phase in such a way that stability is ensured.

There is an additional problem when designing feedback for a dynamic boost converter. The small signal transfers of the power stage are strongly dependent on the large-signal operating point, therefore the maximum amount of loop gain is limited as a design needs to be made for the worst case dynamics. For a fixed output voltage boost converter this is less problematic.

2.4 Control methods

To make a control system of the boost converter, feedback is introduced around the power stage to be able to track the reference signal.

Two types of control schemes are commonly used in switch mode converter applications. The first control scheme is called voltage mode control. In this scheme the duty cycle of the converter is directly set based on the output voltage of the power stage. Current programmed control is the second control scheme which is widely used. In this control strategy the duty cycle is set based on the inductor current, a secondary voltage loop then sets the inductor current to regulate the output voltage.

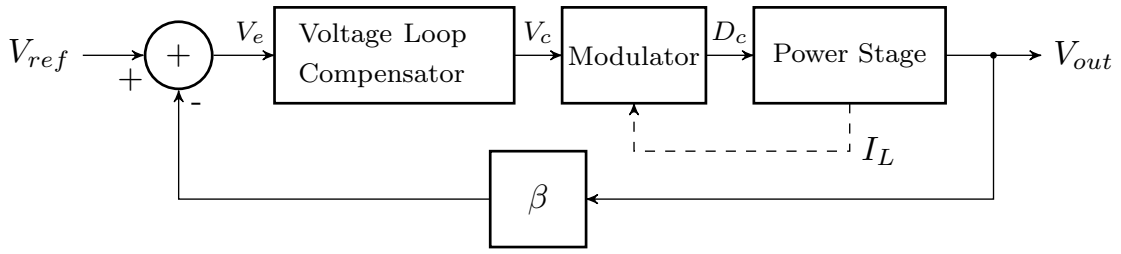

Figure 2.8: General sturcture of controlling a boost converter. In all cases the output voltage is sensed and compared to the reference signal. In case of current mode control the inductor current is also used in the modulator.

To get a clear overview of the control loop used in boost converters figure 2.8 should provide some insight. In all control schemes the output voltage is sensed, in current control the inductor current is used in the modulator as extra feedback parameter.

Using a control loop to control the output voltage, a dynamic boost converter can be designed, because a time varying V_{ref} results in a time varying output voltage. One example is a DC-AC inverter. In [8] a "Boost DC - AC Inverter" is shown where a double control loop is used (voltage feedback and current feedback). However this system is too slow for audio applications as it only has to generate a 50 Hz output sine wave at mains voltage levels.

In the next sections the working principle, advantages, dynamics and problems of both control schemes are discussed. Based on this discussion a control scheme is selected which will be most suited for linearization and therefore for the use as audio amplifier.

Voltage mode control

The simplest form of control in terms of components is voltage mode control. The output voltage of the converter is sensed and compared to the reference voltage. The resulting error signal will set the duty cycle of the converter. The structure for voltage mode control is shown in figure 2.9.

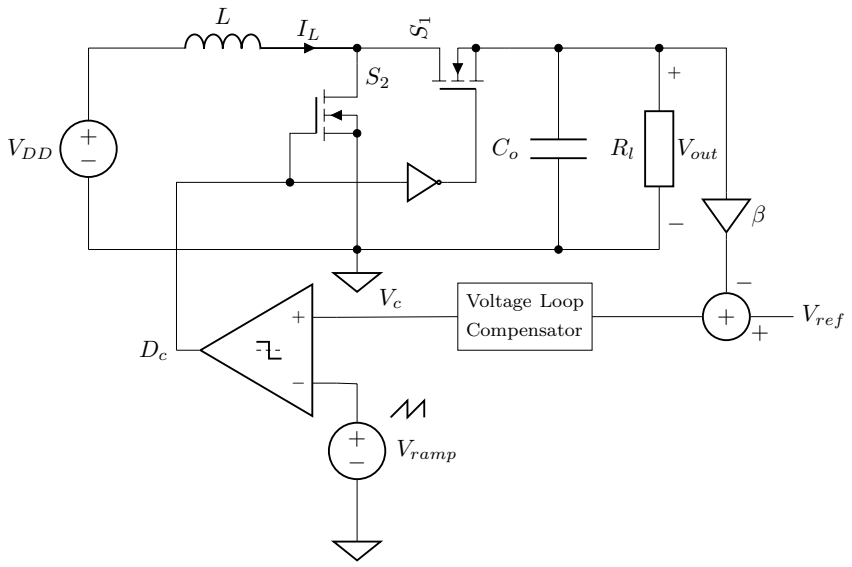

Figure 2.9: Boost converter with voltage mode control.

Large signal

The large signal transfer of the power stage is unchanged, feedback is used to linearize the control to output transfer. The quality of linearization is dependent on the loop gain $A\beta$ as shown in the section above. The large signal transfer function from V_c to V_{out} now also contains the PWM-modulator gain, where V_{ramp} is defined as the peak to peak voltage of the ramp signal:

$$D_c = \frac{V_c}{V_{ramp}}$$
$$\frac{V_{out}}{V_{DD}} = \frac{1}{1 - D_c}$$
$$V_{out} = \frac{V_{DD}}{1 - \frac{V_c}{V_{ramp}}} = \frac{V_{DD} V_{ramp}}{V_{ramp} - V_c}$$

Small signal

The total amount of loop gain that is possible in voltage mode control is limited due to the presence of a double pole in the small signal control to output voltage transfer function[4]. This causes a phase shift in the power stage down to -180° which requires a electronically complex compensator to close the loop with enough phase margin for a stable system. In addition to the double pole, the effect of RHPZ makes the system stability worse. Hence typical system with VMC have limited bandwidth to make the system stable. These effects are shown in figure 2.10.

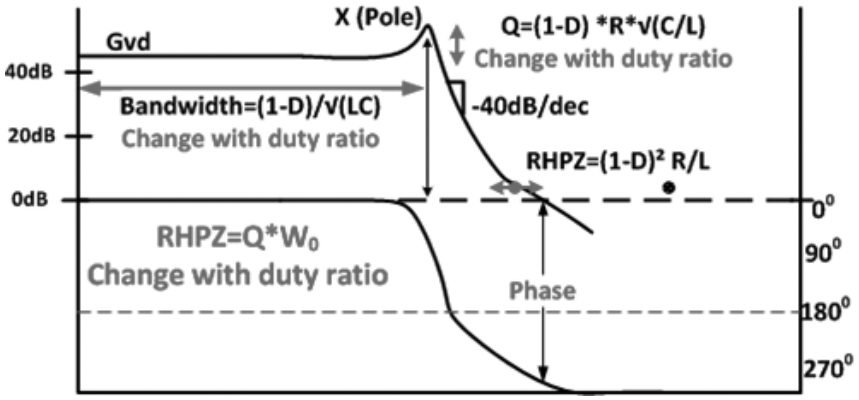

Figure 2.10: Small signal transfer of a voltage mode controlled boost converter. The second order primary pole and right half plane zero are indicated. The DC-gain, primary pole and right half plane zero all move with duty cycle.

The DC-gain, primary pole and right half plane zero (section 2.1) of a voltage mode controlled boost converter are given by[9]:

$$G_{DC} = \frac{V_{DD}}{(1-D_c)^2}$$
$$\omega_0 = \frac{1}{\sqrt{LC}} \cdot \sqrt{\frac{(1-D_c)^2 R_L}{R_L}} = \frac{1}{\sqrt{LC}} \cdot \frac{V_{DD}}{V_{out}}$$
$$\omega_{rhpz} = \frac{(1-D_c)^2 R_L}{L}$$

As can be seen in the equations the DC gain, primary pole and right half plane zero position are dependent on operating point, as everything is dependent on duty cycle. This is shown in figure 2.10. Especially the moving second order pole makes feedback design difficult in a dynamic boost converter. The small signal dynamics of voltage mode control are a reason to look into different control schemes such as peak and average current mode control. These will be discussed in the following sections.

Peak current mode control

Peak current mode control (PCMC) is a current programmed control scheme which is widely used in DC-DC converters. This scheme sets the duty cycle of switches based on the peak current in the inductor.

The goal of current mode control is to make a voltage controllable current source, effectively removing the inductor from the voltage control loop at DC and low frequencies. In an ideal current-mode converter the output current is only dependent on the average inductor current.

The main advantage of current programmed control is its simpler dynamics and first order small signal control to output voltage transfer. Therefore v_{out}/v_c contains one less pole than is the case with voltage mode control[5, p. 439]. This makes it possible to design a wide-band voltage controller (Figure 2.13) without the use of complex phase compensation techniques.

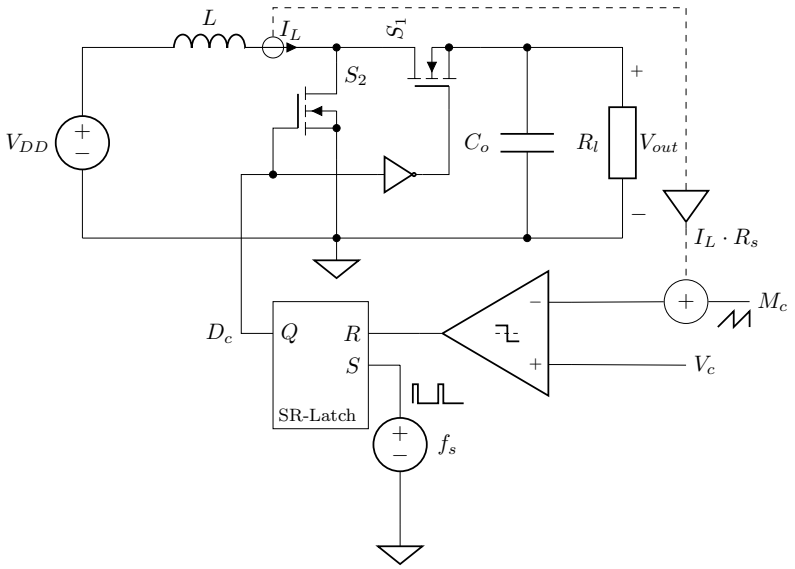

Figure 2.11: Boost converter with peak current mode control.

The complete circuit of a PCMC boost converter is shown in Figure 2.11. If the added ramp M_c in figure 2.11 is ignored for now, the waveform from Figure 2.12 is obtained. This figure describes the principle behind peak current mode control. Each cycle the latch is set by the clock which turns on the bottom transistor, in this period (T_1) the inductor current rises until it reaches the control signal V_c at the comparator. At this instant the latch is reset and the second part of the cycle begins. The inductor will discharge in the output capacitor and load until the next clock sets the latch and a new cycle begins.

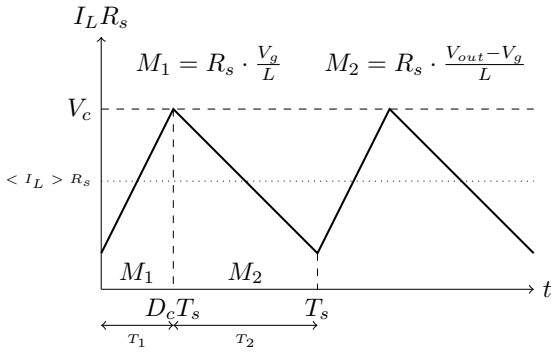

Figure 2.12: Boost converter comparator waveform with peak current mode control.

An extra loop is required in order to accurately set the output voltage. This voltage loop will set the peak current in such a way that the output voltage is correct. The total system is shown in figure 2.13. A compensator structure in the voltage loop is required for stability and has the added benefit of high DC loop gain.

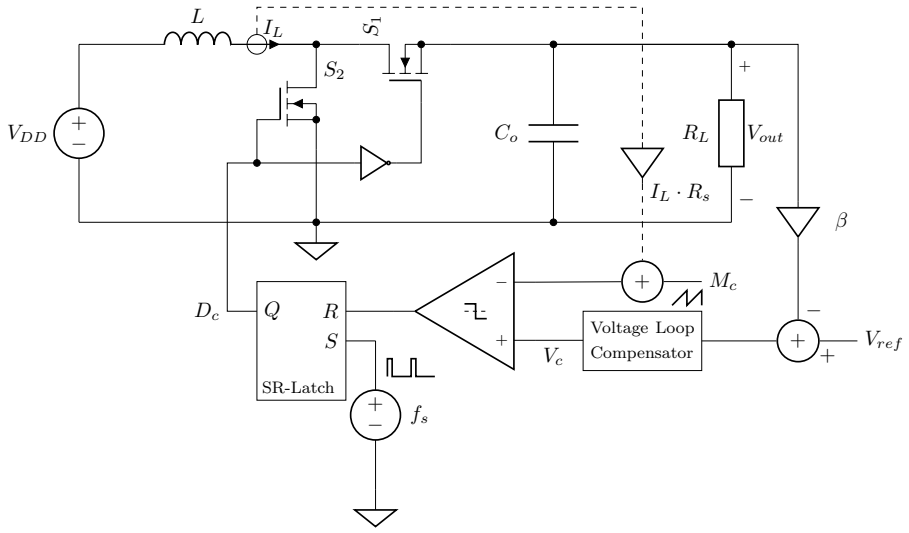

Figure 2.13: Boost converter with peak current mode control including secondary voltage loop.

Stability

The feedback of I_L as used in peak current mode control can cause instability under the specific condition that the steady-state duty cycle is greater than 50 %[5]. It is not unstable in the sense that the inductor current will be subjected to an exponential increasing value but in the sense that the duty cycle will never reach a constant value. This effect is called sub-harmonic oscillation and it can happen when there is a perturbation in the inductor current. An illustration of this effect is shown in Figure 2.14. When sub-harmonic oscillations occur the peak inductor current stays controlled, it does however increase current ripple in the inductor.

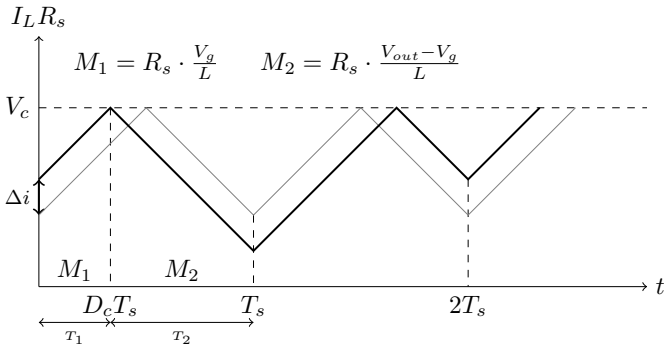

Figure 2.14: A perturbation in inductor current causing sub-harmonic oscillations(D=0.5).

To prevent oscillations for $D > 0.5$ an external ramp (M_c) can be added to the inductor current sense signal, as shown in figure 2.11. The stability is then determined by the combination of the external ramp and the up and down slopes of the inductor current. The absolute value of the damping factor α needs to be smaller than 1:

$$\alpha = \frac{M_2 - M_c}{M_1 + M_c} \tag{2.7}$$

There are some common choices for M_c[5, p. 448], to give damping to the sub-harmonic oscillations. It can be proven analytically that equation 2.8 is the minimum M_c that leads to stability for all duty cycles.

$$M_c = \frac{1}{2} M_2 \tag{2.8}$$

Another option is given below where $\alpha = 0$, this choice will remove oscillations after one switching period, and is know as dead-beat control.

$$M_c = M_2$$

The resulting inductor current waveform is shown in figure 2.15, M_c is added as shown in figure 2.11. It is clear that for higher duty-cycles the ramp will have a greater influence.

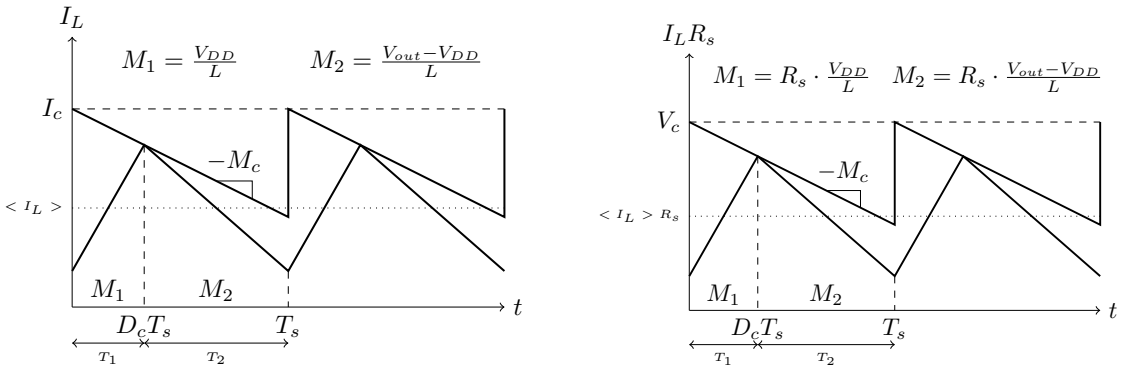

Figure 2.15: Boost converter with peak current mode control in the presence of an artificial ramp. This ramp will dampen sub-harmonic oscillations. The left graph shows the slopes in the current domain, the right graph converts these slopes to voltages via the current sense gain (R_s).

Large signal

In a large signal steady state way the converter sets the peak output current of the inductor. In equation 2.1 the average steady state inductor current is given, this current can then be added to half of the inductor current ripple ($0.5M_1T_1$) and the value of the slope compensation (M_cT_1) to get to the large signal control to inductor current relation. For a graphical representation see figure 2.15.

$$\begin{aligned} I_c &= \langle I_L \rangle + \frac{1}{2}\frac{V_{DD}T_sD_c}{L} + \frac{M_cT_sD_c}{R_s} \\ &= \frac{I_{R_L}}{1-D_c} + \frac{1}{2}\frac{V_{DD}T_sD_c}{L} + \frac{M_cT_sD_c}{R_s} \end{aligned} \tag{2.9}$$

Including current sense resistor the equations become:

$$\begin{aligned} V_c &= \langle I_L \rangle R_s + \frac{1}{2}\frac{V_{DD}R_sT_sD_c}{L} + M_cT_sD_c \\ &= \frac{I_{R_L}R_s}{1-D_c} + \frac{1}{2}\frac{V_{DD}R_sT_sD_c}{L} + M_cT_sD_c \end{aligned}$$

In chapter 3 this relation is used to derive the large signal control to output voltage behaviour.

Average current mode control

Another form of current mode control is average current mode control. The goal of average current mode control is to control the average inductor current, instead of the peak inductor current. It uses a proportional-integral-compensator (PI-compensator) in the current control loop to control the average sensed inductor current. Average current mode control is widely used in active power factor correction circuits[10, 11] as the average current drawn from the supply can be easily tracked and controlled.

The key difference in average current mode control is the insertion of a current loop compensator into the current feedback path. This current compensator has an integrator pole in s = 0 which

results in high loop gain at lower frequencies. This integration will eliminate the average current control error, present in preak current mode control, at low frequencies.

The complete schematic of average current mode control is shown in figure 2.16, here it can be seen that the inductor current is fed into the current loop PI-compensator. The output voltage of this compensator is used to generate the duty-cycle for the converter.

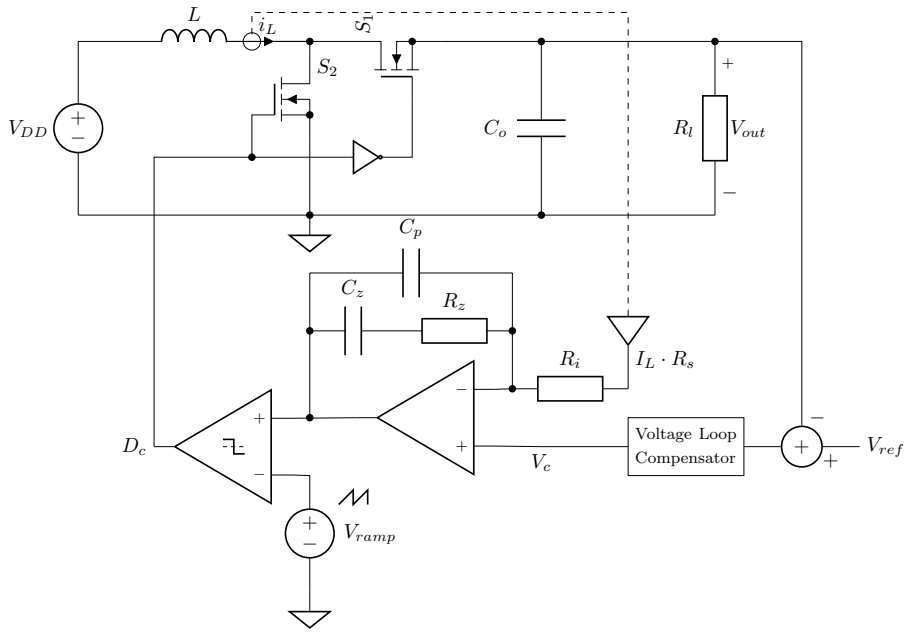

Figure 2.16: Boost converter with average current mode control. The current loop comparator has now been replaced by a PI network which has high loop gain for low frequency signals. This allows the converter to accurately set the DC current in the inductor.

Average current mode control has a couple of advantages over peak current mode control, especially when it is used in a dynamic boost converter[11]:

First the switching noise immunity is considerably better as the inductor current is not directly used to generate the duty-cycle but first passed though the compensator. In peak current mode control a noise spike in the sensed inductor current, caused by switching on the bottom switch, can result in the turn off of the switch if the spike reaches the control voltage.

There is no slope compensation requirement, in peak current mode control slope compensation is required for stability if duty cycles exceed 50 %. In a dynamic boost converter, the downslope of inductor current varies considerably as the output voltage changes. A fixed ramp providing adequate compensation will then overcompensate much of the time, which results in performance degradation and increased distortion.

Peak current mode control suffers from a large peak/average current error if the control current becomes small. In a boost converter used for audio applications the control currents become small in the sine wave zero crossings. In these zero crossings the average current is distorted, resulting in distortion at the output. To achieve low distortion, the peak/average error must be small. There should be a small inductor current ripple to achieve a small peak/average error. A small current ripple however cannot be achieved as the inductor size should be small for wideband control. The small inductor size places the RHPZ at high frequencies but also gives high current ripple.

Average current mode control thus approximates the intended behaviour of the ideal current control loop much better than peak current mode control, thus creating a voltage controllable current source which is only dependent on the DC or average inductor current.

Stability

Average current mode control also suffers from sub-harmonic oscillations, which are expressed in the same way as in peak current mode control. They originate from the same cause as in peak current mode control and have to do with the slope of the inductor current and the slope of the V_{ramp} signal (figure 2.16). The inductor current slope after passing through the current loop compensator should not be larger than the V_{ramp} slope.

To prevent these oscillations no specific compensation slope is required as is the case in PCMC. There is a limit to the current loop compensator gain + modulator gain at the switching frequency to achieve stability[11]. This gain is set by the proportional part of the PI-compensator(K_f) and the V_{ramp} amplitude.

In literature different ratios for inductor down-slope versus the compensator + modulator gain are given. The design procedure given by older literature postulates that the slope of the sensed inductor current in the off-time(M_2), should then not be larger than the slope of the V_{ramp} signal[11, 12]. The slope is influenced by the current sense gain R_s, the inductor size and the proportional gain of the compensator, giving the following stability criterium:

$$M_2 R_s K_f \leq V_{ramp} f_s$$

The limit for sub-harmonic oscillations can then be expressed as[12]:

$$\begin{aligned} D_m &= \frac{1}{2} + \frac{M_c}{K_f(M_1+M_2)} = \frac{1}{2} + \frac{V_{ramp} f_s}{K_f(M_1+M_2)} \\ M_1 &= R_s \frac{V_{DD}}{L}, M_2 = R_s \frac{V_{DD}-V_{out}}{L}, K_f = \frac{R_z}{R_i} \\ \rightarrow D_m &= \frac{1}{2} + \frac{V_{ramp} f_s}{K_f R_s (\frac{V_{DD}}{L} + \frac{V_{DD}-V_{out}}{L})} \end{aligned}$$

Where D_m is the maximum duty cycle which is allowed for stability given a V_{ramp} and proportional gain K_f. Later in the design of the average current mode loop K_f is chosen depending on the maximum duty cycle needed. K_f is determined by the compensator and is given in section 4.3.

In [11] the maximum value of K_f is given. At this mid-frequency gain the inductor down-slope is equal to the slope of the PWM-ramp:

$$\begin{aligned} K_f &= \frac{M_c}{M_2} = \frac{V_{ramp} f_s}{M_2 R_s} \\ &= \frac{V_{ramp} L f_s}{(V_{DD}-V_{out}) R_s} \end{aligned} \tag{2.10}$$

The calculated K_f (equation 2.10) gives stability for all duty-cycles, as D_c is bigger then 0.5 when sub-harmonic oscillations occur:

$$\begin{aligned} D_m &= \frac{1}{2} + \frac{M_c}{\frac{M_c}{M_2}(M_1+M_2)} = \frac{1}{2} + \frac{M_2}{(M_1+M_2)} \\ &= \frac{1}{2} + \frac{M_2}{M_1} + 1 = \frac{1}{2} + \frac{D_c}{1-D_c} + 1 = \frac{1}{2} + D_c \end{aligned}$$

In [13] it is pointed out that limiting the V_{ramp} slope to be equal to the inverted inductor down-slope is actually an over-design which results in too much damping. In [13] Q factor expressions are given to properly damp the sub-harmonic poles. The Q-factor definition is the same as in peak current mode control defined by Ridley[14]. Some extra performance can be gained by using this

method of compensation as the mid frequency gain can be higher.

$$\begin{aligned} Q &= \frac{1}{\pi[(M_1 + M_c)/(M_1 + M_2) - 0.5]} \\ M_1 &= R'_s \frac{V_{DD}}{L}, M_2 = R'_s \frac{V_{out} - V_{DD}}{L} \\ M_c &= V_{ramp} f_s, R'_s = R_s \frac{R_z}{R_i} \\ &= \frac{1}{\pi[(R'_s \frac{V_{DD}}{L} + V_{ramp} f_s)/(R'_s \frac{V_{out}}{L}) - 0.5]} \end{aligned} \tag{2.11}$$

The V_{ramp} slope M_c can be chosen in such a way to satisfy the Q value that is wanted for the system. Where the target should be 0.7 to 1 for optimal damping. The mid frequency gain K_f is related to M_c by equation 2.10.

Large signal

In average current mode control, the control action sets the average current in the inductor. For low frequency signals loop gain is high because the loop contains an integrator, high loop gain means that the average current is set in an accurate way.

The resulting steady state transfer is then obtained by using the insight from section 2.1. The average inductor current is related to the load current by the factor D'_c:

$$I_c = \langle I_L \rangle = \frac{I_{R_L}}{1 - D_c}$$

The time behaviour of the system is shown in figure 2.17. The filtered inductor current $V_{comp,out}$ is compared with a triangle to obtain the duty cycle. If the inductor current is plotted it can be seen that the control signal coincides with the average inductor current. This is beneficial because later it can be seen that this simplifies the design of a pre-distorter a great amount.

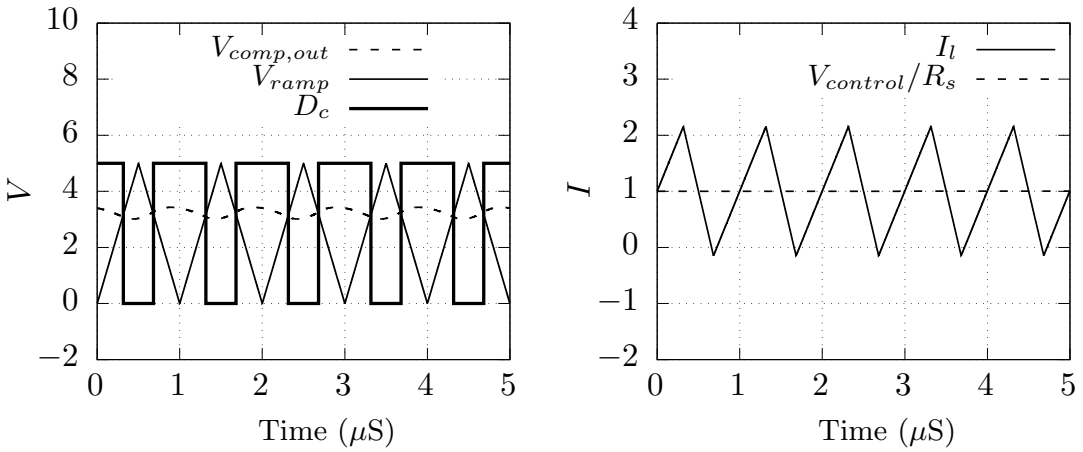

Figure 2.17: Simulated large signal behaviour of the average current mode control loop. The $V_{control}/R_s$ signal is applied at the V_c node and the inductor current, compensator output and duty cycle generation is shown.

Small signal

The small signal characteristics for average current mode control can be found in literature[15]. The right half plane zero is the same as in voltage mode control. For the first pole position the assumption is made that the largest contribution to the output pole is made by the load impedance. The RHPZ can be derived from the equations given in [15, eq. 6].

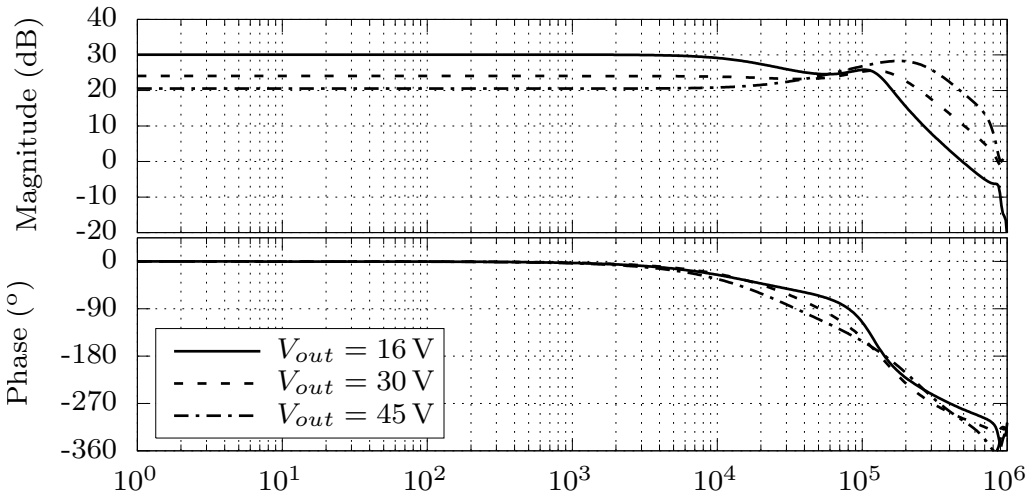

Figure 2.18: Simulated small signal transfer of an average current mode controlled boost converter at different output voltages. The effect of the RHPZ can clearly be seen at $V_{out} = 45\,\mathrm{V}$ - $30\,\mathrm{kHz}$. The DC-gain coincides with the equation given below.

$$G_{DC} = \frac{R_L(1-D_c)}{2R_s} = \frac{R_L V_{DD}}{2R_s V_{out}}$$
$$\omega_0 \approx \frac{2}{R_L C}$$
$$\omega_{rhpz} = \frac{(1-D_c)^2 R_L}{L}$$

For resistive load the primary pole is dominated by the R_L and C_o, it can also be seen that the second order primary pole has been reduced to a first order pole.

One important thing to note is that these equations are valid for the case the current is positive, for usage as audio amplifier the current direction can also be negative. The change in small signal dynamics needs to be investigated before design is possible.

Other linearization methods can be used in conjunction with feedback to make further improvements to the linearity, for example introducing pre-distortion inside the control loop. In chapter 3, the large signal behaviour of both current mode control techniques presented in this section is used to investigate the linearity. The goal is to create a pre-distorter for the current mode control loop for an extra improvement in linearity. First the general principle of pre-distortion is explained and how it can be applied, before doing a detailed investigation in chapter 3.

2.5 Pre-distortion

Next to feedback there is another technique to improve linearity, when the non-linear behaviour of a system is known a feed-forward technique can be used to compensate for the non-linearity of the amplifier. The concept of pre-distortion works by inversely modelling the amplifier's gain and phase characteristics. Combining the two systems will then create a system that is more linear. It works by 'inversly distorting' the amplifier input and therefore compensating for the non-linearity in the amplifier itself. This principle is shown in figure 2.19.

Possible challenges lie in the fact that the non-linear behaviour of the amplifier can change depending on temperature and component variations. When the amplifier drifts the effectiveness of the pre-distorter will be reduced. Pre-distortion often also requires calibration as absolute component values are unknown.

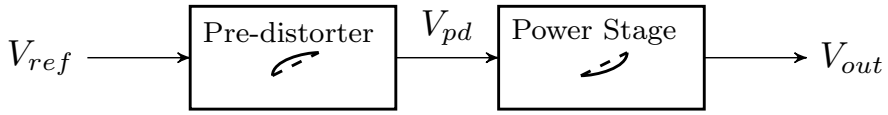

Figure 2.19: Pre-distortion principle. Where PD is the pre-distorter implementing the inverse transfer function of the power stage (PS) of the converter.

The multiplication factor of the pre-distorter is chosen in such a way that the output will become a linear function of the input value.

$$\begin{aligned} V_{pd} &= H_{pd}(V_{ref}) \\ V_{out}(V_{pd}) &= H_{ps}(V_{pd}) \\ V_{out}(V_{ref}) &= H_{ps}(H_{pd}(V_{ref})) \sim a \cdot V_{ref} \end{aligned} \tag{2.12}$$

To design a pre-distorter, a large signal model of the amplifier needs to be derived so that the pre-distorting function can be determined. For the pre-distortion of a boost converter the large signal transfer characteristics of the control input to output voltage need to be investigated, this can be different for specific control methods and will be worked out in chapter 3.

Bridge mode - Bride Tied Load topology

Another way to improve the linearity of an amplifier is to create a duplicate of the circuit and connect the load between the amplifier outputs (see figure 2.20). Connecting the load in bridge mode will quadruple the power delivered to the load and this connection scheme will cancel even-order harmonic distortion products.

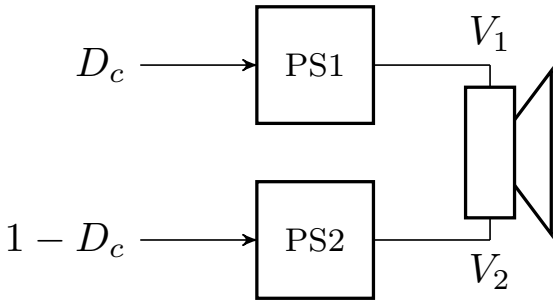

Figure 2.20: Schematical representation of bridge mode in audio amplifiers. The inputs are inverted and the load is connected between the amplifier outputs.

Putting two boost converters in bridge mode will result in the following large signal transfer function:

$$\begin{aligned} V_1 &= V_{in} \cdot \frac{1}{1-D} \\ V_2 &= V_{in} \cdot \frac{1}{1-(1-D)} \\ V_{out} &= V_1 - V_2 \\ &= V_{in} \cdot \left(\frac{1}{1-D} - \frac{1}{1-(1-D)} \right) \\ &= V_{in} \cdot \left(\frac{2D-1}{D(1-D)} \right) \end{aligned}$$

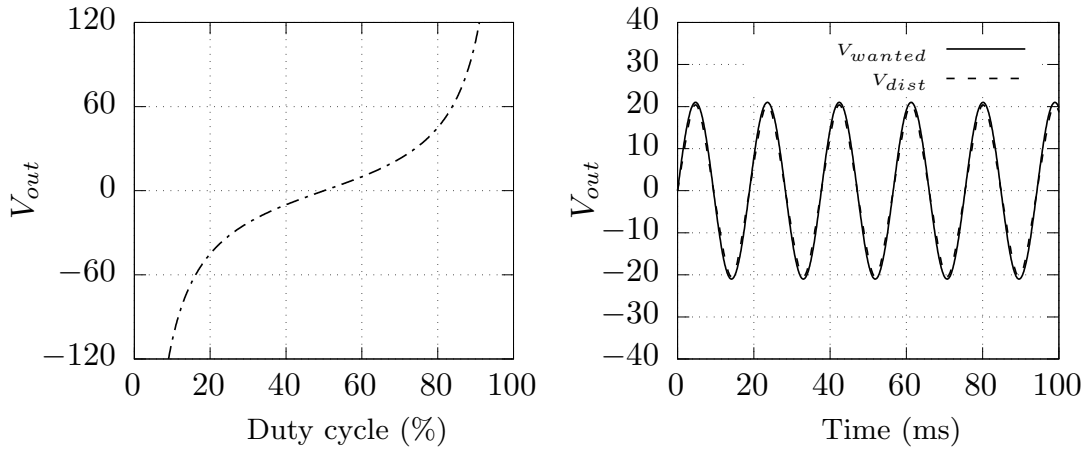

Figure 2.21: In bridge mode the tranfer function is more linear and therefore the distortion is reduced. This effect is also visible from the sinusoidal signals, the compression / expansion behaviour is now reduced in comparison with figure 2.6

When this function is plotted (figure 2.21) it can be seen that the transfer function become more linear from 30% to 70% duty cycle.

Another clear advantage is that the output signal is biased at 0 V preventing the need for a large and costly DC-blocking capacitor as compared to a single ended approach. This is required for audio applications as DC current in the speaker needs to be prevented.

It should be noted that odd-order harmonic distortion is not cancelled so in the end feedback is still needed to reduce the harmonic distortion of the bridged-boost stage.

A bridge mode converter is inherently stable when used in an open loop way. Two boost converters each with individual feedback can also be used however the modelling complexity increases as the order of the system increases. When using two converters open loop there is an additional point of interest, both need to be perfectly matched in terms of DC output offset, otherwise a DC current will flow through the loudspeaker.

In [2], a bridge mode boost converter for audio applications is designed where a hysteretic duty cycle generator is combined with a PID feedback controller. In this paper 3 W is delivered in an 8 Ω load with a THD of 0.52% from a battery voltage of 3.6 V. This corresponds with a voltage boost factor of 12 dB.

In [16], a boost converter is used in a bridge to drive a 4 Ω load with 0.5% THD @ 1 kHz, 4 W. 3 times more power is obtained in comparison with a class D amplifier

Pre-distortion in combination with a bridged topology has also been done, for example in a buck/boost amplifier[17]. In this work an analogue pre-distortion approach is taken where the reference signal for the PWM generator is pre-distorted using a specially biased MOSFET circuit. A prototype power stage was built and results show that a supply to output voltage gain of up to 9 dB and reduction in THD from 6% down to 3% at 1 kHz was obtainable using analogue pre-distortion. A factor two improvement, the improvement increases as frequency drops. At 600 Hz the improvement is a factor 4.

2.6 Combining feedback and pre-distortion

There have been several implementations of pre-distortion for voltage mode controlled switch mode boost converters[18–20]. In these applications feedback is combined with pre-distortion to improve the linearity of the converters.

All these techniques focus on the PWM generator circuit. In the traditional case, the transfer from control-voltage to duty-cycle in a PWM-generator is constant with gain $1/V_{ramp}$(Figure 2.9). In combination with the $1/(1-D)$ transfer characteristics of the open-loop power stage the output voltage is still non-linearly dependent on the control voltage and can be expressed as:

$$V_{out} = V_{in} \cdot \frac{1}{1 - \frac{V_c}{V_{ramp}}}$$

In a modulated-ramp PWM-generator[18] the voltage ramp is modulated by varying the capacitive charge current (see figure 2.22). This results in a duty cycle which is dependent on the control current:

$$D = 1 - \frac{V_b C}{I_{CON} T}$$

This can then be added to the boost-converter conversion ratio function to arrive at a linear control to output transfer:

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{1}{1-D} = \frac{1}{1 - (1 - \frac{V_b C}{I_{CON} T})} \\ &= \frac{I_{CON} T}{V_b C} \end{aligned}$$

The large signal transfer given above is a linear function of I_{CON}. A PID voltage compensator was used to close the feedback loop, as mentioned in the small signal section of voltage mode control (2.4). The PID voltage loop compensator structure is required to get enough phase and gain margin for stable operation.

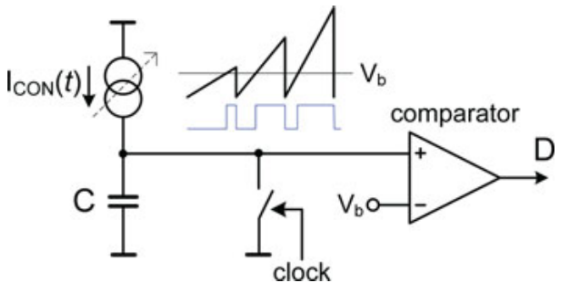

Figure 2.22: The PWM-generator used in the modulated ramp PWM boost converter. The control is done via a variable current which charges a capacitor[18].

[21] proposes a differential boost converter for high quality sine wave generation. Frequencies of up to 2 kHz can be generated by using a non-linear control method. A THD figure of 2 % is obtained at an output voltage level of 90 V_{pp}, while using a 25 V supply.

In [20] a dynamic linearizing modulator for the boost converter is proposed, which transforms the open-loop boost converter into a linear amplifier. The converter is feedback controlled on a cycle by cycle basis control scheme, no traditional control scheme has been used. Its operating frequency is as high as one-fifth the switching frequency. No THD or voltage boost factors are given.

In literature the combination pre-distortion and feedback has been done numerous times for voltage mode control. However as discussed in this chapter voltage mode control has some disadvantages. The second order power stage transfer limits the amount of loop gain and therefore reduces the quality of linearization.

In contrast current mode control does not have a second order power stage transfer which allows for more loop gain. Next to this, pre-distortion has not been attempted for current mode control. In the next chapter pre-distortion for current mode controlled converters is investigated. This can then be combined with voltage feedback to improve the linearity even more.

Chapter 3

Pre-distortion of a current mode controlled boost converter

With the insights gained in the previous chapter a look can be taken at the non-linear behaviour of the current mode controlled boost converter. The results can then be used to design a pre-distorter and insert it into the feedback loop before the current input.

In the previous chapter, the difference in large signal control to output current transfer between peak current mode control and average current mode control can be found. In this chapter it is shown that a peak current mode control inner loop is not a good candidate for pre-distortion and that average current mode control fixes the pre-distortion difficulties found in peak current mode control. The large signal transfer of average current mode control is easily pre-distortable in an analog way.

After investigation of non-linearities the inverse function pre-distorter can be designed to linearize the current loop control to output voltage transfer.

3.1 Identification of non linear behaviour

In the previous chapter, the steady-state large signal behaviour of the large signal control to inductor current transfer has been discussed of both peak-current-mode control and average-current-mode control. These large signal transfer characteristics can be used to find the non linear behaviour of the power stage. In this section the analytical expressions are given or numerically approximated if a pure analytical expression is not possible.

Peak current mode control

In chapter 2 the analytical expression (equation 2.9) for the control current is derived. For clarity the figure and equation is once again given here.

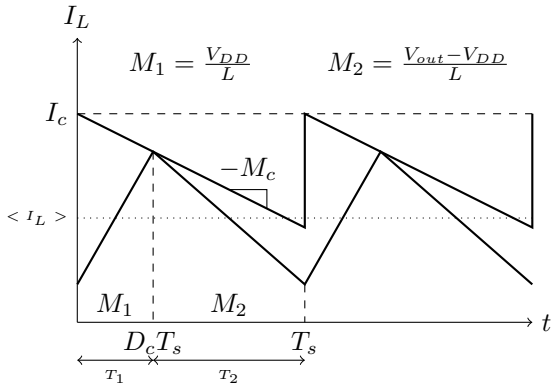

Figure 3.1: Boost converter with peak current mode control in the presence of an artificial ramp. This ramp will dampen sub-harmonic oscillations.

The following control equation shows the large signal behaviour of peak current mode control:

$$I_c = \frac{I_{R_L}}{1-D_c} + \frac{1}{2}\frac{V_{DD}T_sD_c}{L} + M_cT_sD_c \tag{3.1}$$

If the small ripple approximation is applied in the same way as in section 2.1 the second and last term of expression 3.1 can be neglected. In that case the following equation holds:

$$I_c \approx \langle I_L \rangle = \frac{I_{R_L}}{1-D_c}$$

Using this equation the large signal control to output voltage transfer is given as:

$$I_c = \frac{I_{R_L}}{1-D_c} \quad I_{R_L} = \frac{V_{out}}{R_L} \quad D_c = 1 - \frac{V_{DD}}{V_{out}}$$
$$\rightarrow I_c = \frac{V_{out}}{R_L\frac{V_{DD}}{V_{out}}} = \frac{V_{out}^2}{R_LV_{DD}}$$
$$V_{out} \approx \sqrt{I_cV_{DD}R_L} \tag{3.2}$$

From these equations it can be concluded that changing the control scheme from duty cycle control to current mode has a large influence on the linearity. From the highly non linear behaviour of the open loop converter the large signal control to output voltage transfer function has now changed to a square root of the control signal. This is under the assumption that the small ripple approximation holds.

For the application as audio amplifier it is not valid to assume the ripple is small because of the large bandwidth requirements (the inductor size determines the RHPZ position and therefore poses an upper limit to bandwidth). A small valued inductor is required to place the RHPZ at a sufficiently high frequency. The exact requirements however will be derived in chapter 4. For now a large current ripple is assumed, so another approach is required.

The large signal non-linear behaviour of peak current can also be exactly derived by using equation 3.1. The goal is to find the I_c to V_{out} transfer characteristics. This can be done by rewriting equation 3.1 to find the duty cycle dependence on I_c. I_{R_L} can then be filled in and using the voltage relation (equation 2.2) the total transfer function can be derived:

$$D_c = \frac{4I_cL + 2M_cL + V_{DD}T_s}{2M_cL + V_{DD}T_s} - \frac{\sqrt{4I_c^2L^2 - 8I_cL^2M_c - 4I_cLT_sV_{DD} + 16I_{R_L}L^2M_c + 8I_{R_L}LT_sV_{DD} + 4L^2{M_c}^2 + 4LM_cT_sV_{DD} + T_s^2V_{DD}^2}}{4M_cL + V_{DD}T_s}$$

$$I_{R_L} = \frac{V_{out}}{R_L} \quad V_{out} = \frac{V_{DD}}{1-D_c}$$

It can be seen that it is not easy to derive an analytical expression for the dependence of V_{out} to I_c as I_{R_L} and thus V_{out} is also present in the square root term of the duty cycle. This is already an indication that a pre-distorter cannot be easily implemented for peak current mode control.

Using Maple[22] (an algebraic solver) the exact I_c to V_{out} expression is calculated. The full expression however is mathematically very complex and is therefore not shown here. A graph can be created for the large signal transfer function, this can be compared to the small ripple approximation that was made in equation 3.2. The graph gives a better view compared to the analytical expression given by the algebraic solver.

Table 3.1: Parameters used for simulating Peak and Average Current Mode Control.

Parameter	**Value**
V_{DD}	$12\,\mathrm{V}$
f_s	$1\,\mathrm{MHz}$
L	$3.3\,\mu\mathrm{H}$
R_L	$8\,\Omega$
M_c	$\frac{1}{2}M_2 = 5\,\mathrm{MV\,s^{-1}} = 5\,\mathrm{V\,\mu s^{-1}}$

Using the component parameters calculated in chapter 4 (table 3.1) the following transfer is acquired:

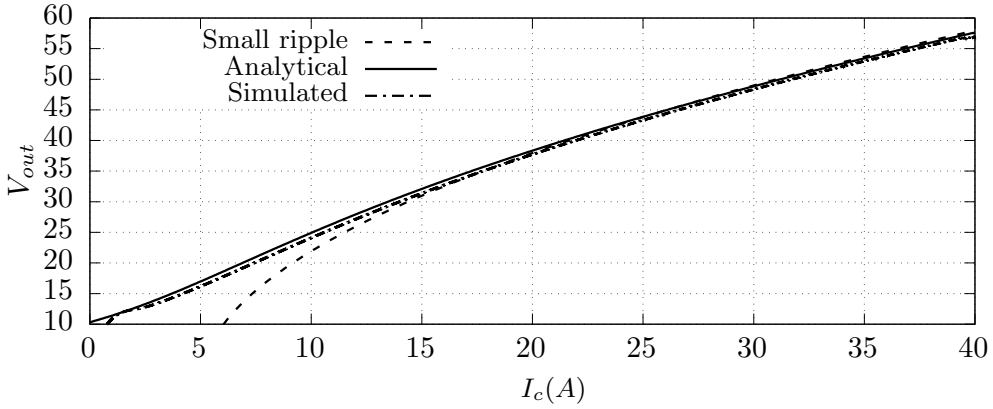

Figure 3.2: The small ripple approximation (equation 3.2) versus the analytical expression (I_c to V_{out} using Maple) for peak current mode control is plotted here. Only for large currents the expression will follow the small ripple square root function. A large signal SIMPLIS simulation is also included to show that the analytical expression matches the behaviour of the peak current mode control power stage.

As can be seen in the graph, the simulated and analytical traces start with a $1/(1-D_c)$ behaviour and transitions to square root behaviour at $30\,\mathrm{V}$. Looking at figure 2.15 and equation 2.9 this behaviour can be explained. The ripple is for small control signals much larger than the average current. The systems behaves in that case as a PWM-generator where the control signal is compared to the inductor current ramp. The duty cycle is thus directly determined by the control signal giving the traditional $1/(1-D_c)$ behaviour shown in equation 2.2.

At higher control levels the average current is large compared to the ripple and the small ripple approximation is more valid, the region in between is the transition region. This behaviour can be mitigated by selecting a large inductor, however a larger inductor will mean that the system will not meet it's bandwidth requirements (low RHPZ position with a fixed load).

Concluding, two regions can be defined: The first region where the control signal is smaller than the inductor current ripple and a region where the control signal is much larger than the ripple. The section in between is a transition region.

Looking at the equations for peak current mode control the transfer is dependent on inductor size, slope compensation (which is also dependent on inductor size, section 2.4), switching time, supply voltage and load resistance. In a real world implementation all these components have an uncertainty next to the fact that the square root only holds for large currents.

This shows that for peak current mode control it is very hard to create a pre-distorter which works in all regions. A simulation with a squarer as pre-distorter also shows this is the case. In this simulation the bias is chosen in such a way that the valley of a 100 Hz sine wave with an amplitude of 8.5 V is at the level given in table 3.2. Looking at figure 3.2 it is can be expected that a sine with a minimum value at 30 V gives better THD results compared to a sine with a minimum at 15 V as 30 V is the start of the square root region.

Table 3.2: Simulation results for the PCMC power stage with a squarer pre-distorter. Showing improved THD when working in the square root region of PCMC.

Sine Valley	**THD (%)**
15 V	2.84
30 V	0.56

Another control scheme can be used to overcome this issue. In the next section this is discussed in detail.

Average current mode control

As mentioned in the previous chapter average current mode control filters the sensed inductor current in such a way that the average inductor current is set. Which is very beneficial in this case because then the square root action is valid over the entire operating region. Pre-distortion can then be implemented with a simple squarer circuit.

The derivation of the large signal voltage transfer function of average current mode control is given and is dependent on the supply voltage and load resistance:

$$\begin{aligned} I_c = \langle I_L \rangle = \frac{I_{R_L}}{1 - D_c} \quad I_{R_L} = \frac{V_{out}}{R_L} \quad D_c = 1 - \frac{V_{DD}}{V_{out}} \\ \rightarrow I_c = \frac{V_{out}}{R_L \frac{V_{DD}}{V_{out}}} = \frac{V_{out}^2}{R_L V_{DD}} \\ V_{out} = \sqrt{I_c V_{DD} R_L} \end{aligned} \tag{3.3}$$

In this case the ripple and inductor sizes are of much less importance for the large signal transfer. As with peak current mode control a simulation is also done with the components selected in chapter 4.

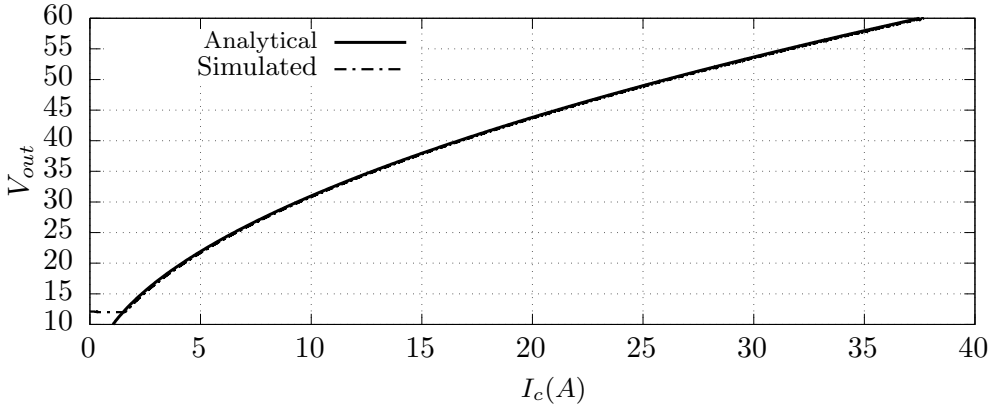

Figure 3.3: The large signal transfer of ACMC is plotted here, the analytical expression (equation 3.3) matches the SIMPLIS simulation very well.

In figure 3.3 the analytical expression versus simulation is plotted. The simulation shows square root behaviour over the full control range (except when limited by the supply), which means that average current mode control is a good candidate for the current control loop because pre-distortion can be easily applied.

Figure 3.4 shows the distortion behaviour of the average current mode control loop. The square root behaviour expands the input sinusoidal in the valleys and compresses the top op the sine wave. This gives primarily second order distortion as can be seen in the third graph. The total TDH of the V_{dist} signal is calculated as approximately 8.7 %. This is a reduction in THD of approximately a factor two, compared to the open loop boost converter THD shown in figure 2.6.

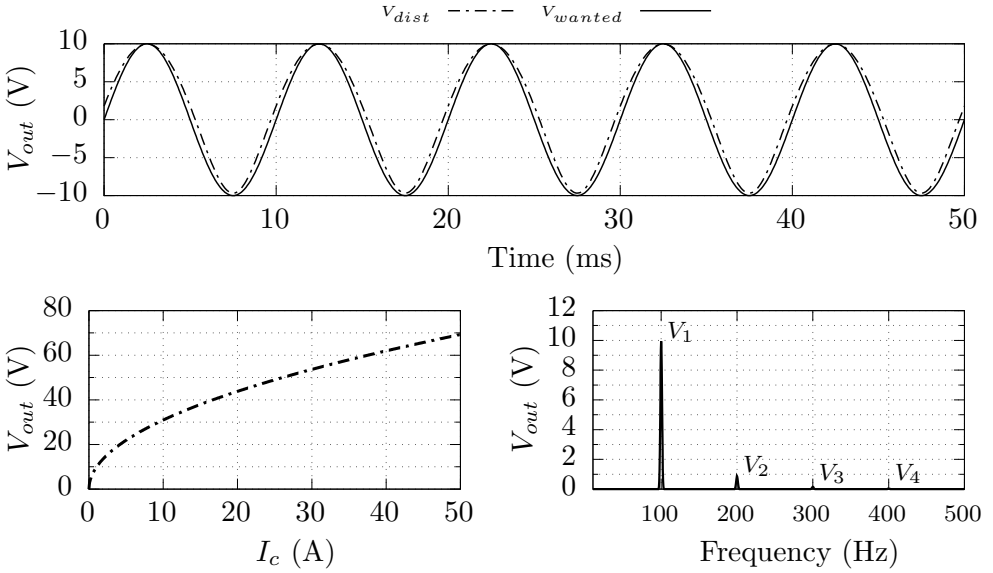

Figure 3.4: Distortion behaviour when an ideal sine is applied to the ACMC control input. The output is biassed at 30 V and the mean is subtracted before plotting. The bottom of the sine wave is expanded and the distortion behaviour is predominantly second order.

In the next section a derivative is made when the output is biased and what that means for the large signal transfer curve.

3.2 Utilization as audio amplifier

For now the forward current steady state transfer characteristics of peak current mode control (figure 3.2) and average current mode control (equation 3.3) have been derived. It has been shown that the large signal transfer of peak current mode control is not unified for different operating conditions and is largely dependent on component sizing and slope compensation. The large signal transfer of average current mode control however is very well defined in steady state and independent of components and slopes. The only variables left are supply voltage and load resistance.

Both types of control schemes can be linearized using feedback, which will be applied in this work. As seen in the sections above, the non-linear behaviour of both control schemes is in the same order of magnitude so feedback will reduce non-linearities by the same amount in both types of converter controllers.

To obtain even more improvement of the converter's linearity, it has been explained that a pre-distorter can be used. It is desirable that the pre-distorter is easy to implement. If this is the case it can be done in an analog way. For peak current mode control it is difficult to implement a simple pre-distorter because the different operating regions require different pre-distorter actions. For average current mode control it has been shown in equation 3.3 that the output voltage is the square root of the control voltage. Hence pre-distortion can simply be implemented in the analog domain, where the pre-distortion function is implemented with a squarer circuit.

Another important factor when using the converter for audio applications is that there should be no DC current through the loudspeaker. The output is biased at a certain DC level and a DC blocking capacitor forms a high pass filter in combination with the load. This will have some effects on the transfer curve, now the current and voltage relations are decoupled. The current will be zero at the bias voltage, negative for voltages below the bias and positive for voltages above the bias level. For simulations the DC blocking capacitor is modelled as an ideal voltage source with voltage V_{bias}, this is shown in figure 3.6.

Pre-distorter

In this section the knowledge of the above sections is used to derive the pre-distorter transfer curve. As shown in section 2.5 the combined transfer of the power stage and pre-distorter should result in a linear function of the output signal versus the input signal. It will be introduced in the control loop as shown in figure 3.5. The pre-distorter block is introduced between the voltage loop and current loop making the control to output voltage transfer of the inner loop more linear. Residual non-linearity will be suppressed with the same loop gain, making the total system more linear.

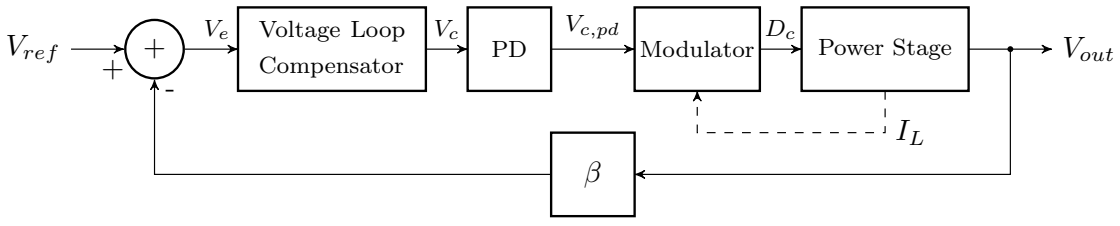

Figure 3.5: Introduction of the pre-distorter in the feedback loop. The block is introduced between the voltage loop and current loop making the inner loop more linear. Residual non-linearity will be suppressed with the same loop gain making the total system more linear.

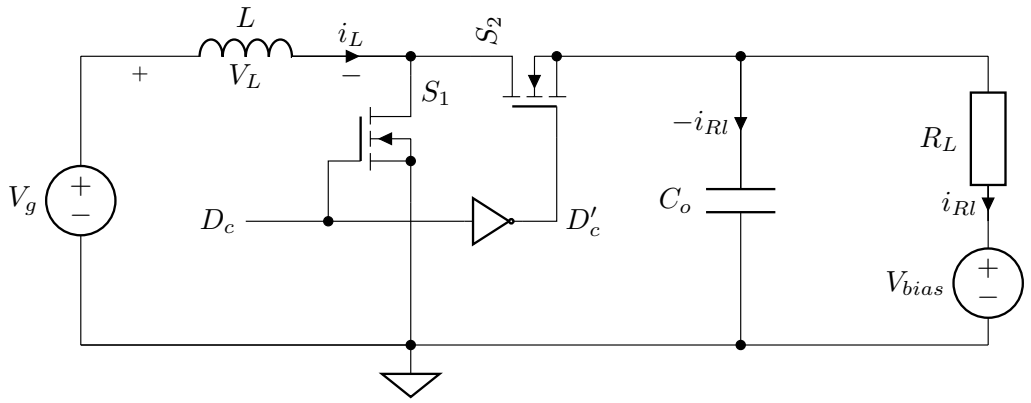

Figure 3.6: Decoupling the boost converter will change the load current, decoupling is modelled here with a voltage bias at the output of the converter. In a real world application decoupling will be done with a large electrolytic capacitor.

Adding a decoupling capacitor changes the power stage in the following way (figure 3.6), the load current is now dependent on the bias level. Decoupling is modelled as a bias voltage source at the output of the converter. Using figure 3.6 the new equation for the load current can be used in combination with the equations for the boost converter power stage:

$$\begin{aligned} I_c = \frac{I_{R_L}}{1-D_c} \quad I_{R_L} = \frac{V_{out}-V_{bias}}{R_L} \quad D_c = 1 - \frac{V_{DD}}{V_{out}} \\ \rightarrow I_c = \frac{I_{R_L}}{1-(1-\frac{V_{DD}}{V_{out}})} = \frac{V_{out}-V_{bias}}{R_L\frac{V_{DD}}{V_{out}}} = \frac{V_{out}^2 - V_{out}V_{bias}}{R_L V_{DD}} \\ V_{out} = \frac{V_{bias}}{2} + \frac{\sqrt{4I_c V_{DD} R_L + V_{bias}^2}}{2} \end{aligned} \tag{3.4}$$

The pre-distorter curve is now not a pure square of the control voltage but also includes a linear term depending on the bias voltage. The equations (3.4) show a a lower limit where the pre-distorter works, from half the bias voltage level without an upper limit (see the middle graph of figure 3.7). The lower limit is given by the point where the square root term is zero:

$$\begin{aligned} \frac{\sqrt{4I_c V_{DD} R_L + V_{bias}^2}}{2} &= 0 \\ \rightarrow 4I_c V_{DD} R_L + V_{bias}^2 &= 0 \\ \rightarrow I_c &= -\frac{V_{bias}^2}{4V_{DD}R_L} \end{aligned}$$

Below this level the pre-distorter gain reverses, causing instability in the feedback loop. In reality the output voltage will be symmetrical around V_{bias} giving a maximum output voltage of 45 V.

These equations do not include the current sense gain (R_s), which is chosen in the current controller

and wanted voltage gain. If both are included the pre-distorter equation becomes:

$$V_c = V_{out} \cdot \gamma$$

$$V_{c,pd} = I_c \cdot R_s = \frac{(\frac{V_c}{\gamma})^2 - \frac{V_c}{\gamma} V_{bias}}{R_L V_{DD}} \cdot R_s \tag{3.5}$$

$$V_{out} = \frac{V_{bias}}{2} + \frac{\sqrt{4\frac{V_{c,pd}}{R_s} V_{DD} R_L + V_{bias}^2}}{2} \tag{3.6}$$

$$= \frac{V_{bias}}{2} + \frac{\sqrt{4(\frac{V_c}{\gamma})^2 - 4(\frac{V_c}{\gamma})V_{bias} + V_{bias}^2}}{2}$$

$$= \frac{V_{bias}}{2} + \frac{\sqrt{(-2(\frac{V_c}{\gamma}) + V_{bias})^2}}{2}$$

$$= \frac{V_{bias}}{2} + \left| \frac{V_{bias}}{2} - \frac{V_c}{\gamma} \right| \tag{3.7}$$

The V_c to output voltage gain (γ) can be chosen freely, and will influence the bias levels at which the voltage loop will work. For example figure 3.7 uses a gain of 5, this means that the output bias level of 30 V will be at 6 V. Later it is shown that this is a good bias level due to the 12 V supply voltage of the voltage compensator.

Equation 3.7 is in the form of equation 2.12 and is linear dependent on the control voltage. This is the required pre-distorter behaviour as the power-stage output voltage is now linearly dependent on the control voltage. The relevant curves are shown in figure 3.7. The derivative of V_{out} to V_c is only based on the voltage feedback factor γ.

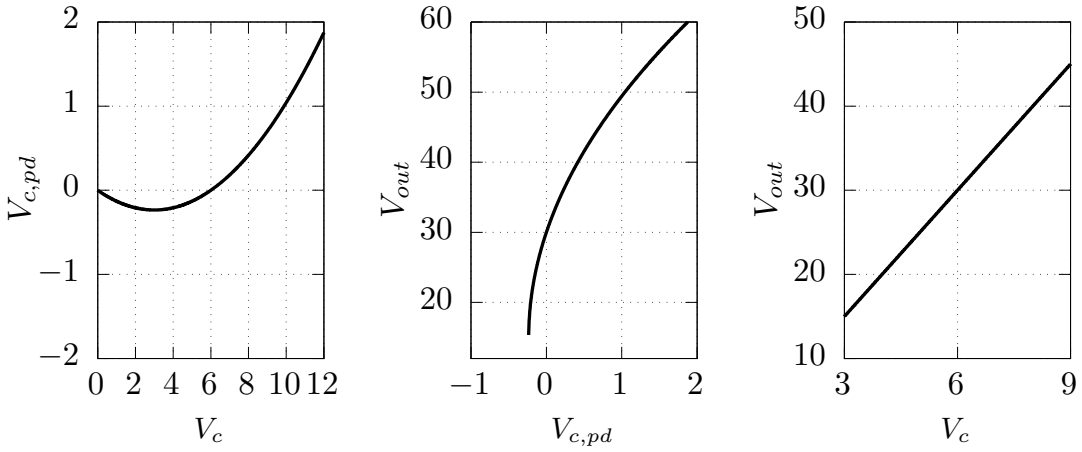

Figure 3.7: Different large signal transfer curves in the signal chain. First the voltage-loop output to control-voltage is shown. Then the control-voltage to output voltage. If these two are combined the voltage-loop output to output-voltage transfer is a linear function, the gain determined by the chosen gamma (γ).

3.3 Other distortion sources

The intrinsic non-linear transfer of the power stage is not the only contribution to the distortion at the output. There are additional effects in a real-world implementation that cause additional non-linearities. In this section they are listed in order of significance.

Dead-time

A real-world implementation brings a challenge when the switches are implemented using MOS-FETS. It is impossible to turn on these 'switches' infinitely fast. If the synchronous switches are

switched at the same time there is a point where one is turning off and the other is turning on, somewhere in the middle they both conduct. This phenomenon is called cross conduction, from an efficiency and system perspective it is undesirable to have cross-conduction, at worst the MOSFETs could even be damaged. Therefore dead-time needs to be introduced, the switch controller (gate driver) waits some time to turn on a switch after the other switch has been turned off[1]. In figure 3.8 it is shown how dead-time is implemented where there is always a certain non-overlap time between switching moments.

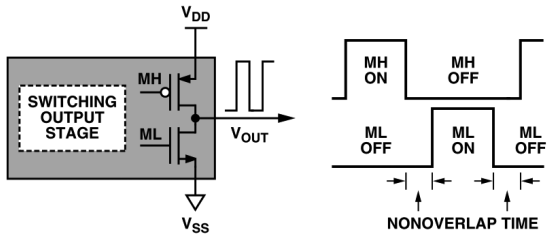

Figure 3.8: Dead-time implemented in a Class D output stage[1], where both switches are never on at the same time.

Depending on the directionality of current flow in the converter this time will either be subtracted or added to the duty cycle, giving an offset in duty cycle. The effect of dead-time on the open loop duty cycle to output transfer is shown in figure 3.9. The transition region where the current reverses ($D_c = 60\,\%$ where $V_{out} = 30\,\mathrm{V}$, the output bias point) can also be clearly seen, in this region the switches are soft-switching.

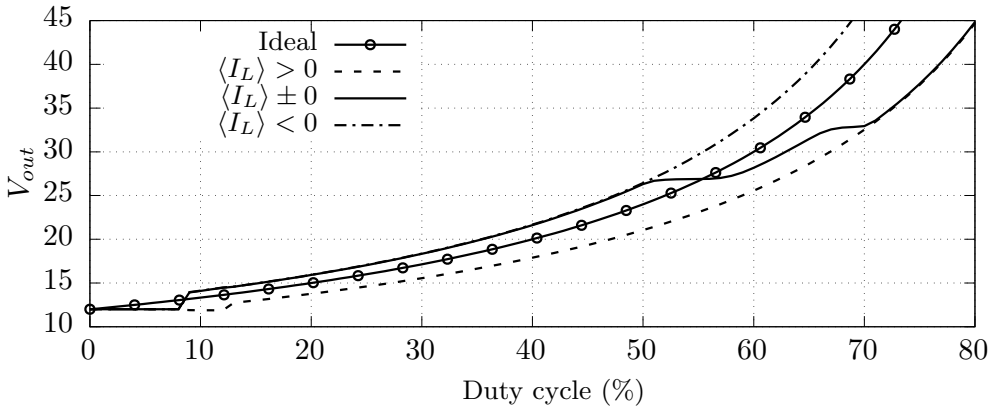

Figure 3.9: The influence of dead-time on the open-loop power stage is depicted here. The signal-to-on dead-time is 12% and the signal-to-off dead-time is 8% of one switching cycle (can also be seen by the steps at low duty cycles). The three cases are plotted where the average inductor current is always bigger than zero, crosses zero at the bias level of 30 V and is always smaller than zero.

This effect is mitigated in a closed current loop as can be explained intuitively. When the inductor current set-point increases and the system is operating in the flat output voltage regions of figure 3.9, the output voltage will not increase with increased duty-cycle. That means that the inductor current will also not increase, the current loop will compensate for this phenomenon and increase the duty cycle even further until the required current can be delivered to the load.

Non-ideal components

Another source of distortion comes from a difference in the $R_{ds,on}$ resistance of the MOSFETs. This is the result of a difference in voltage drop over the MOSFETs in the different switching cycles giving distortion. Therefore the top level switch should be bootstrapped. In this way the gate source voltage is equal for both MOSFETs resulting in the same on state channel resistance[23].

When selecting an inductor it is important that one is selected with low inductance change versus current, as a non-linear inductance also causes distortion[24].

Power supply ripple

Power supply ripple is the result of insufficient power supply decoupling in combination with inductances resulting in AC variation on the DC power supplies. Care should be taken when designing bias networks referenced to supplies with ripple because bias points can shift resulting in distortion.

Components should be selected with enough power supply rejection ratio and it is best to make stabilized supplies with voltage regulators for sensitive components and bias networks.

Chapter 4

Design of a linearized boost converter

After the selection of a proper control topology the complete system with linearization is implemented. In this chapter the average current mode loop is designed, the pre-distorter is introduced between the current control input and voltage loop output. The voltage loop compensator is dimensioned in such a way that the system is stable and has enough phase margin. The system is then simulated and small signal and large signal results are obtained.

Before the start of the design it is important to determine design boundaries and specifications of the system. These parameters determine design decisions, relevant bandwidths of the system and component choices.

Using the specifications design can start by dimensioning the power stage, subsequently the current mode control loop, pre-distorter and voltage loop can be designed. The final design is verified by simulation, the results of these simulations are given in the last part of this chapter.

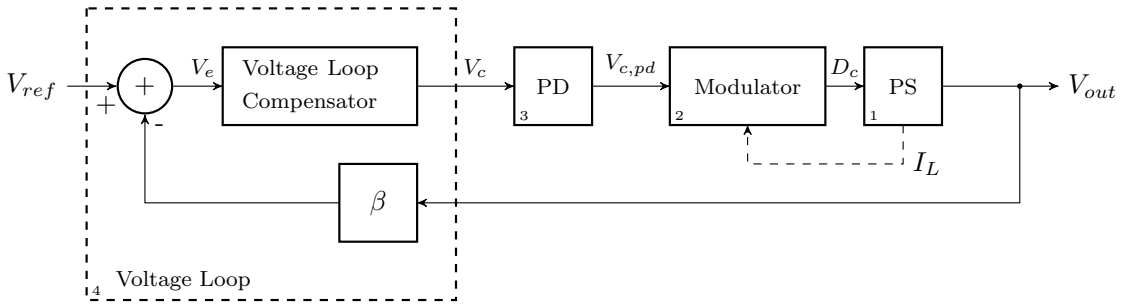

Figure 4.1: Structure of the converter to be designed.

An overview of the structure to be designed is given in figure 4.1. A design is made from right to left, starting with the power stage (1) and ending with the voltage loop (4) design.

4.1 Design boundaries and specifications

The main goal of this work is to design a single stage boost converter for generating dynamic audio signals. In this section relevant design parameters are given and a comparison is made with the two stage design in terms of output power, THD, load specification and component selection.

Supply Voltage

The target application is car audio, the amplifier in this case is powered from a 12 V car battery. In the rest of the design this voltage is used as supply voltage for the amplifier. For measurements later on a net connected power supply is used instead of a battery.

Amplifier load

The impedance of speakers used for car audio is in the range of 2 Ω to 8 Ω. Previously it is determined that the right half plane zero position is very load dependent. A lower load resistance will diminish the phase of control to output transfer of the inner loop at lower frequencies. For the proof of concept design a load of 8 Ω is assumed, to relax the design constraints.

It is also possible to reduce the inductance value of the inductor and make a design for a 4 Ω load but this will give twice the ripple current, making design harder and less efficient.

Furthermore for all the simulations and measurements an 8 Ω resistor is used for simplicity while in reality a loudspeaker is a complex impedance where the impedance varies with frequency. Also taking these effects into account is outside the scope of this project, the implications of this are discussed in the last chapters (chapter 5 and 6).

Output power

Because this is a proof-of-concept design, a single-ended topology is chosen. The 12 V supply of a car battery gives a maximum output signal swing of 12 V_{pp}. The maximum achievable output power in an 8 Ω is then given as:

$$P_{out} = \frac{V_{rms}}{R_L} = \frac{(\frac{V_{pp}}{2\sqrt{2}})^2}{R_L} = \frac{(\frac{V_{DD}}{2\sqrt{2}})^2}{R_L} = \frac{(\frac{12}{2\sqrt{2}})^2}{8} = 2.25\,\text{W}$$

For the design of the boost converter the aim is a factor 5 power increase. This gives comparable output power levels to a Class D bridge tied load (BTL) topology amplifier. A factor 5 in power means that the output amplitude should increase with at least the square root of 5. For a 12 V supply this means that the 6 V amplitude needs to increase to 13.5 V. To create some headroom, a 15 V amplitude is targeted.

The output voltage range which the boost converter needs to supply can then be easily calculated. First the bias voltage needs to be determined, taking into account that the pre-distorter works from $V_{bias}/2$ (see section 3.2), the bias voltage is set to 30 V. This allows 15 V swing.

The minimum output voltage is 15 V and the maximum output voltage is 45 V, corresponding with $D_c = 0.2$ to $D_c = 0.73$. These values are used in the design procedure as minimum and maximum duty cycles.

Total Harmonic Distortion

Total harmonic distortion should be as low as possible, however realistic values should be given. The THD of audio amplifiers is measured at 1 kHz. In this research a frequency versus THD sweep is made for different power levels. These can be compared to measurements from literature.

In figure 4.2 the THD from a standard single ended Class D chip(TPA3122[25]) is plotted. Here it can be seen that THD values between 0.01% and 0.1% are realistic at a 1 kHz output frequency, furthermore the THD increases as the output frequency increases.

The THD peak at 10 kHz is explained by the topology, as this chip uses a single ended topology the second harmonic of 10 kHz is just in the audio bandwidth. The loop gain at 10 kHz is the lowest resulting in the most distortion at this frequency.

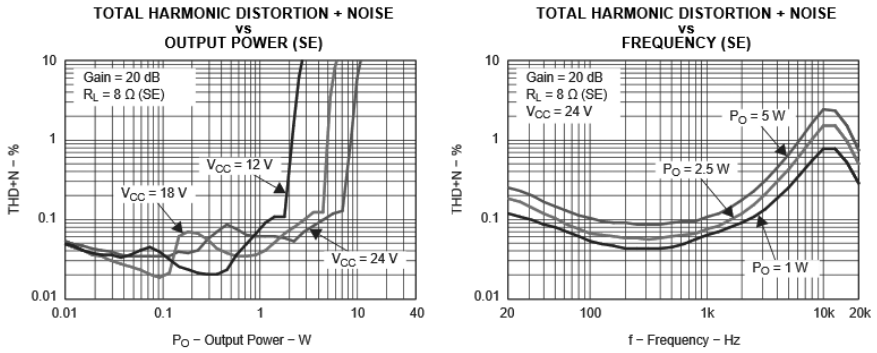

Figure 4.2: THD figures from a standard 15 W Class D amplifier(TPA3122) used for single ended audio amplification[25].

Summary

A summary of all specifications is given in table 4.1. These specifications are the basis for the design in the following sections and for the creation of a prototype in chapter 5. The required gain in the amplifier, maximum voltages components need to handle and bandwidth requirements follow from these specifications.

Table 4.1: Summary of all the specifications for the boost audio amplifier.

Requirement	**Value**
Supply voltage	12 V
Output bias voltage	30 V
Input voltage swing	Line level (± 0.5 V to 1.5 V)
Output voltage swing	± 15 V (30 V)
−3 dB BW	20 Hz to 20 kHz
Minimum load resistance	8 Ω
Output power in 8 Ohm	12.5 W
Total harmonic dist. (1 kHz)	0.1 % @ 10 W

4.2 Design of the Power Stage

Before the current loop compensator can be designed, the power stage components need to be dimensioned. The values of these components are required for further design and need to be determined first.

The components of the power stage determine the final bandwidth of the converter. Primarily the position of the right half plane zero, which in combination with the load resistance, determines the inductor size and switching frequency. The output capacitor influences the bandwidth of the converter as the output capacitor sets the primary pole of the current mode control loop.

The procedure is then as follows:

1. Set the minimum load resistance → in this work 8 Ω.
2. Place right half plane zero at 4 times the voltage loop gain crossover.
3. Calculate the required inductor size for that right half plane zero position.
4. Based on the recommended inductor current ripple of 20 % to 40 %[26] the switching frequency can be determined.
5. Set the output capacitor as a trade-off between voltage ripple and output pole location.
6. Continue design with current loop and voltage loop.

All the steps are elaborated in the next section, based on this design procedure the component sizes for the power stage can be determined.

Inductor size

The size of the inductor will determine the inductor current ripple and the right half plane zero position and consequently the maximum voltage loop crossover frequency. To negate the effect of the right half plane zero, the maximum bandwidth of the voltage loop should be around 20 % to 30 % of the right half plane zero position as explained in [27]. Therefore a trade-off exists between ripple current, switching frequency and maximum voltage loop bandwidth.

The voltage loop gain crossover should be as high as possible, a realistic value however is 20 kHz. This gives the opportunity to arrive at decent values for the rest of the design process. The 20 kHz crossover then places the right half plane zero position at 80 kHz based on the 4 times requirement shown above.

The worst case right half plane zero position is at maximum duty-cycle, in this case 0.73 or 45 V. The inductor size required for this worst case right half plane zero position is (as derived in appendix A):

$$f_{rhpz} = \frac{(1-D_c)^2 R_L}{2\pi L}\left(\frac{V_{out}}{V_{out}-V_{bias}}\right) \tag{4.1}$$

$$\begin{aligned} L &= \frac{(1-D_c)^2 R_L}{2\pi f_{rhpz}}\left(\frac{V_{out}}{V_{out}-V_{bias}}\right) \\ &= \frac{(1-0.73)^2 \cdot 8}{2\pi \cdot 80\text{e}3}\left(\frac{45}{45-30}\right) = 3.5\,\mu\text{H} \end{aligned}$$

The recommended ripple in boost converters is 20 % to 40 %[26] of the maximum inductor current. Using the specifications mentioned above, the maximum ripple can be calculated. From the maximum ripple, the inductor size and switching frequency can be determined to satisfy the right half plane zero position.

$$\begin{aligned} \Delta_{I_L} &= 0.4 \cdot I_{out,max} \cdot \frac{V_{out}}{V_{DD}} \\ &= 0.4 \cdot \frac{V_{out,max}-V_{bias}}{R_L} \cdot \frac{V_{out}}{V_{DD}} \\ &= 0.4 \cdot \frac{45-30}{8} \cdot \frac{45}{12} = 2.81\,\text{A} \end{aligned}$$

Where Δ_{I_L} is the inductor ripple current and $I_{out,max}$ the maximum output current of the converter.

Now the switching frequency can be determined to satisfy the ripple requirement, in section 4.3 it is shown that the switching frequency also determines the current loop crossover frequency:

$$\begin{aligned} f_s &= \frac{M_2(1-D_c)}{\Delta_{I_L}} \\ &= \frac{(V_{out}-V_{in})(1-D_c)}{L\Delta_{I_L}} \\ &= \frac{(45-12)\cdot(1-0.73)}{3.5\text{e}{-6}\cdot 2.81} = 905\,\text{kHz} \end{aligned}$$

The practical inductor value is calculated to be 3.3 µH for an even higher right half plane zero frequency. The switching frequency can then be rounded up to 1 MHz for approximately the same ripple. The switching frequency of 1 MHz also happens to be the approximate upper limit for a discrete implementation as switching with a frequency higher than 1 MHz will become increasingly difficult due to component delay and dead-times. Next to those issues driving the switching

MOSFETS will require f_s more power, which can be problematic as heat in the gate drivers become an issue:

$$P_{gate-driver} = \frac{1}{2} C_{gate} V^2 f_s$$
$$P_{switch,total} = 2P_{gate-driver} = C_{gate} V^2 f_s$$

Output Capacitor

The capacitor will determine the primary pole of the control to output voltage (section 2.4), how well the pre-distorter works and the voltage ripple at the output of the converter.

For a full audio range it is desirable to have the output pole placed as high as possible, in that way there is minimal phase shift in the V_c to V_{out} transfer of the current mode controlled stage at the voltage loop crossover, allowing for a higher voltage loop gain (the voltage loop design procedure will be explained later in section 4.5).

For a pre-distorter which works for all audio frequencies it is also important to choose the output pole location as high as possible.

Both requirements are a trade-off between pole location and voltage ripple because the voltage ripple at the output would become higher with a higher pole frequency.

The output voltage ripple is defined as[26]:

$$\begin{aligned} \Delta_{V_{out}} &= \left| \frac{I_{out,max} D_c}{f_s C} \right| \\ &= \left| \frac{\frac{V_{out} - V_{bias}}{R_L} D_c}{f_s C} \right| \\ &= \left| \frac{(V_{out} - V_{bias}) \cdot (1 - \frac{V_{DD}}{V_{out}})}{f_s C R_L} \right| \end{aligned} \tag{4.2}$$

From equation 4.2 it can be seen that the ripple will be highest when the voltage excursion is the biggest. In this case at maximum output voltage of 45 V. This is verified by figure 4.3 where the output voltage versus ripple voltage is shown. At the bias level the ripple is lowest as can be expected because there is no inductor DC current.

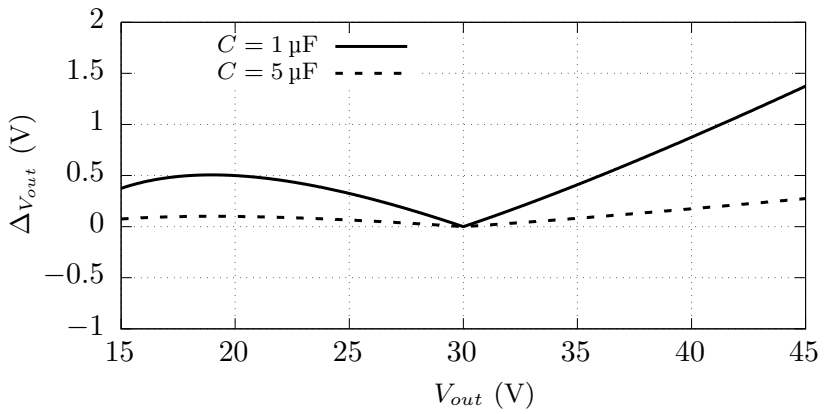

Figure 4.3: The influence of output capacitance on the ripple at a certain output voltage (equation 4.2). It shows that for large excursions from the bias level the ripple increases as shown in equation 4.2. As expected the ripple reduces by a factor five when the capacitor is increased equally.

For an output load resistance of $8\,\Omega$ a $1\,\mu F$ capacitor gives about $1.4\,V$ ripple at $45\,V$ output voltage. This is about the maximum allowed voltage ripple as EMC can become an issue in real world applications.

The output pole of the current mode loop is defined as (see appendix A):

$$\omega_0 = -\frac{2}{RC} + \frac{D_c' V_{bias}}{V_g RC} \tag{4.3}$$

Using a $1\,\mu F$ capacitor as output capacitor gives an output primary pole at $V_{out} = 30\,V$ of:

$$\begin{aligned}\omega_0 = -\frac{2}{RC} + \frac{D_c' V_{bias}}{V_g RC} \rightarrow f_0 &= \frac{2}{2\pi RC} - \frac{D_c' V_{bias}}{2\pi V_g RC} \\ &= \frac{2}{2\pi \cdot 8 \cdot 1e{-}6} - \frac{(1-0.6)\cdot 30}{2\pi \cdot 12 \cdot 8 \cdot 1e{-}6} \approx 20\,kHz\end{aligned}$$

The output capacitor also determines how well the the pre-distorter works over frequency, as mentioned before. The impedance of the $1\,\mu F$ capacitor is in parallel with the load impedance and together they will decrease the total load impedance of the converter:

$$\begin{aligned}Z_L &= R_L // Z_{C_{out}} \\ &= \frac{R_L}{j\omega R_L C_{out} + 1}\end{aligned}$$

This effect is shown in figure 4.4, the load impedance change begins at $300\,Hz$ from that point the effectiveness of the pre-distorter will begin to decrease. A solution would be to decrease the output capacitor to for example $0.1\,\mu F$.

As $1\,\mu F$ already gives a high voltage ripple, a factor 10 increase would mean the voltage ripple would become unacceptably high. This decrease in performance is thus inevitable for a static pre-distorter configuration.

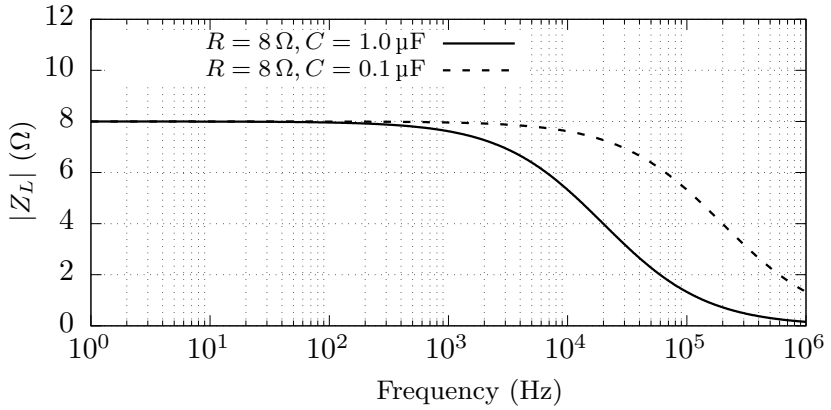

Figure 4.4: Influence of the output capacitor on load impedance. The load impedance decreases with frequency as the impedance of the output capacitor becomes influential.

The values found in this section are practical for design and physical implementation. The rest of the converter is designed with a power stage inductor value of 3.3 µH, an output capacitance of 1 µF and a switching frequency of 1 MHz.

4.3 Designing the current current mode control loop

Before the pre-distorter and the voltage loop can be designed, the inner current loop needs to be designed. The structure of the average current mode control loop is shown in figure 4.5.

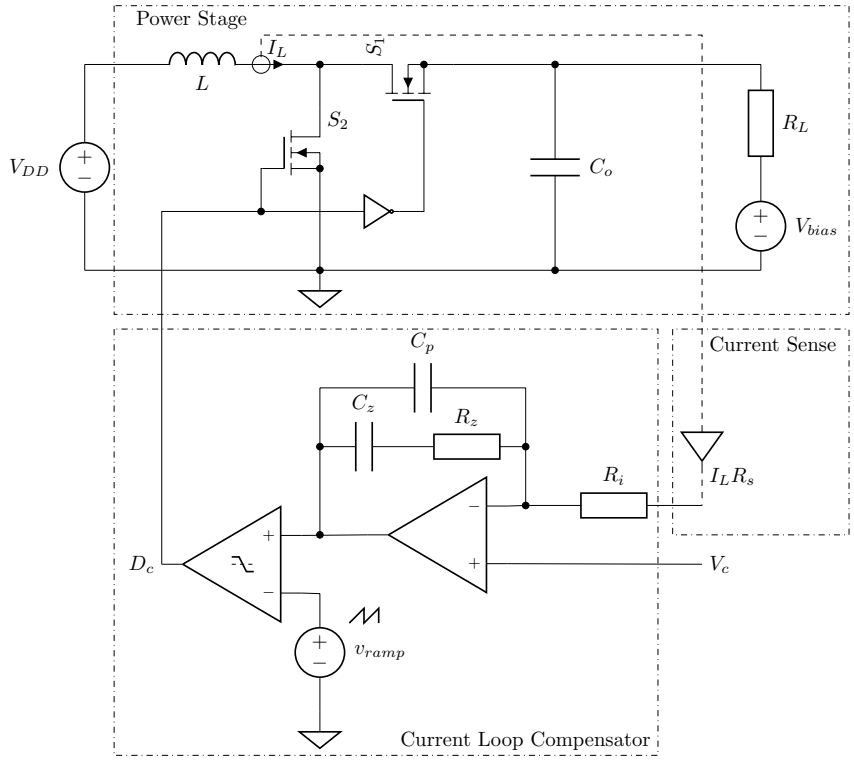

Figure 4.5: Average current mode control inner loop.

The design starts with the description of the current loop compensator. After the equations describing the behaviour of the current compensator, the current sense gain is determined. By combining both parts, the quality factor of the loop can be determined and the pole and zero positions of the current loop compensator can be calculated.

The corresponds to:

1. Determine the current sense gain.
2. Place the zero in the compensator based in the required current loop gain crossover.
3. Set mid frequency gain (K_f) based on the required Q-factor (equation 2.11).
4. Place the pole of the compensator at $f_s/2$ to attenuate the switching ripple.
5. Calculate component values based on mid frequency gain and the required pole and zero locations.

Each item is explained in detail in the following sections.

Using the specifications and power stage design from the preceding sections and the knowledge from chapters before, the current mode loop design is started.

All small signal results are obtained at three different bias levels which represent the boundary of where the converter can work. The lowest output voltage is chosen at 16 V as 15 V causes convergence issues in the simulator. An output voltage of 30 V will be the center of the working region and is the same as the bias voltage level. The upper boundary of the output voltage is defined as 45 V, this is the point where the phase dynamics are the worst due to the right half plane zero.

There is not a lot of literature available on how to properly design the current mode loop[11, 13, 28]. Additionally these methods do not include the fact that the load is biased at the output of the converter essentially decoupling the current and voltage relations. This has amongst others influence on the right half plane zero position (section 2.1). A derivation for the DC-gain, primary pole and right half plane zero has been done in appendix A.

It is possible to follow the design guidelines described by literature but they should be validated using simulation. This is now especially important as existing models might not accurately predict the behaviour of the converter.

Current loop compensator design

The components for the power stage are now known, the values can be used to design the average current mode control compensator. Ideally the current compensator should eliminate the current control error at low frequencies which exists in peak current mode control. This eliminates the bad peak to average ratio in the control to output current caused by the slope compensation and high inductor ripple, as shown in the previous chapter.

The design procedure from Yan[13] is followed to obtain a working average current mode control loop. The current loop compensator structure is shown in figure 4.6.

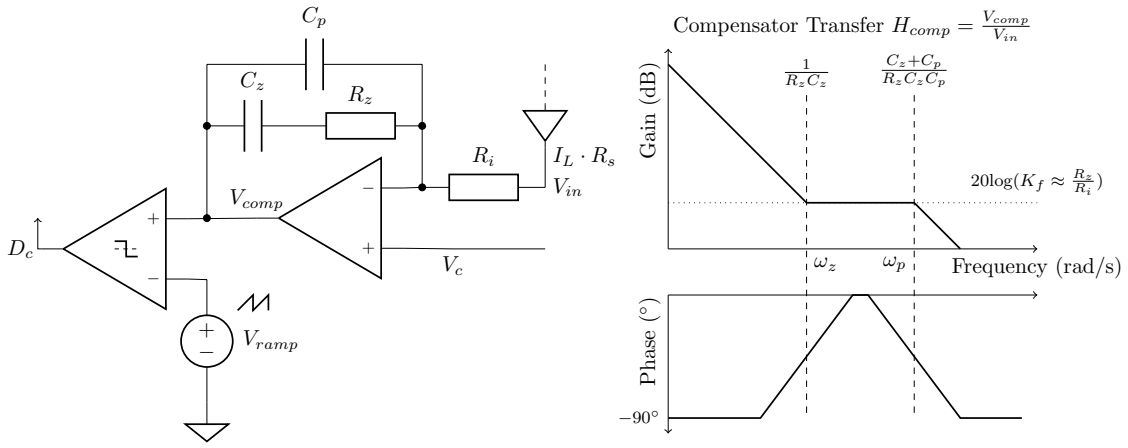

Figure 4.6: Current loop compensator structure with two poles and one zero. A pole at DC will facilitate the integration function. The higher frequency zero increases the phase for enough phase margin and a pole at half the switching frequency will attenuate the switching ripple.

The transfer from V_{in} to V_{comp} is given by:

$$H_{comp} = \frac{V_{comp}}{V_{in}} = \frac{1 + C_z R_z s}{sR_i(C_z + C_p)(1 + sR_z\frac{C_z C_p}{C_z + C_p})}$$

$$\omega_z = \frac{1}{R_z C_z}$$

$$\omega_{p1} = 0, \omega_{p2} = \frac{C_z + C_p}{R_z C_z C_p}$$

$$K_f = \frac{R_z C_z}{R_i(C_z + C_p)} \approx \left.\frac{R_z}{R_i}\right|_{C_z >> C_p}$$

These equations can be used to calculate the component values for the current compensator based on the required pole and zero locations. R_z, R_i, C_z and C_p are given in figure 4.6.

Current sensor gain

Before the design procedure can be followed, the current sense gain needs to be chosen. This converts the inductor current to the voltage domain, which can be handled by the current compensator op-amp.

In equation 2.11 it can be seen that the current sense gain influences the maximum K_f in the current loop compensator. Another point that should be considered is the power supply for the current sensing amplifier, this gives the voltage range for the sensed current. A 5 V supply will be used for the current loop based on available components, this will be explained later in the physical implementation chapter. The zero output current level will be at 2.5 V. This gives a voltage range of ± 2.5 V.

The maximum current in the inductor is given as:

$$\begin{aligned} I_{L,max} &= I_{R_L,max} \cdot \frac{V_{out}}{V_{DD}} + \frac{1}{2}\Delta_{I_L} \\ &= \frac{V_{out,max} - V_{bias}}{R_L} \cdot \frac{V_{out}}{V_{DD}} + \frac{1}{2}\Delta_{I_L} \\ &= \frac{45 - 30}{8} \cdot \frac{45}{12} + \frac{1}{2} \cdot 2.81 = 8.43\,\text{A} \end{aligned}$$

It will be shown later that a current sense gain of 0.1 is beneficial as it gives a decent K_f in the compensator and fits in the voltage range with a maximum output voltage of 0.85 V.

Design procedure & stability

Now that all components of the power stage, the switching frequency and the current sense gains are known, the compensator for the current loop can be designed. The job of the current compensator is to create a high loop gain at low frequencies such that the average current is correct. The design should be made for worst case conditions (where the inductor current slopes are largest, see section 2.4 for the stability criteria) so that it is stable for the whole range (15 V to 45 V) of operating conditions. For this system the worst case will be at an output voltage of 45 V.

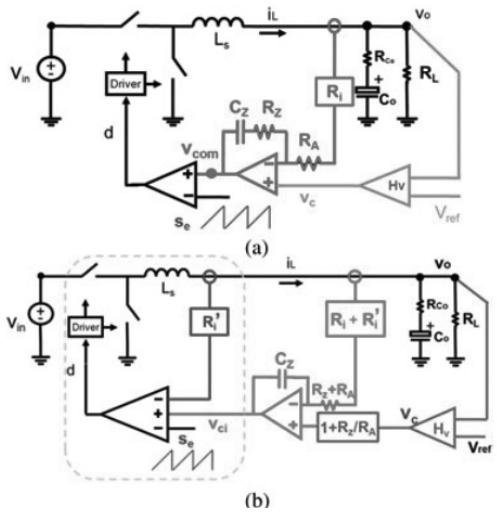

Figure 4.7: Separation of feedback in an average current mode controlled buck converter, the separation principle can be applied on a boost converter in the same way[13].

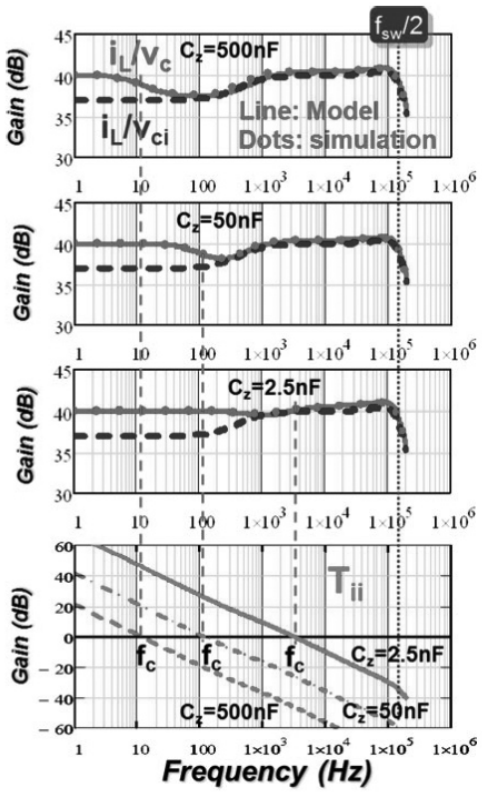

Figure 4.8: The transitioning between peak current mode control and average current mode control is shown in this figure[13].

As said before, in [13] the design procedure for the current loop compensator is given. The authors first derive an equivalent circuit with the proportional and integral terms of the feedback separated, the result is shown in figure 4.7. The inner loop corresponds to the proportional feedback term ($R_i' = R_i K_f$), where R_i is the current sense gain and K_f the mid-frequency gain. The outer current loop represents the integral action of the current loop compensator. It is easy to see that the inner loop is the same as the peak current mode control. V_{ci} to I_L therefore shows the power stage under peak current mode control, where V_c to I_L shows the power stage under average current mode control.

This separation of feedback is used to show the transitioning behaviour if the crossover of the integration loop is varied (see figure 4.8). Based on this transitioning behaviour the design of the current loop compensator can be started.

1) Zero placement based on the required integration loop gain
The goal of the mid frequency zero in the compensator, is to revert the phase shift caused by the integration pole at $s = 0$. This integration will eliminate the current control error of peak current mode control at low frequencies. The place of the zero corresponds with the integration loop crossover frequency[13] (see figure 4.7 and 4.8).

The pole-zero pair of the power stage causes V_c to I_L gain deviation under current mode control if the crossover is not chosen high enough. This happens at mid frequency[13] as shown in figure 4.8. To eliminate this gain deviation the loop gain crossover frequency needs to be higher then the pole location f_0 of the plant in worst case conditions:

$$f_{0,V_{out}=45\,\mathrm{V}} = \frac{2}{2\pi RC} - \frac{D_c' V_{bias}}{2\pi V_{DD} R} = \frac{2}{2\pi \cdot 8 \cdot 1\mathrm{e}{-6}} - \frac{(1-0.73)\cdot 30}{2\pi \cdot 12 \cdot 8} \approx 26\,\mathrm{kHz}$$

The current loop compensator zero location and thus the integration loop crossover frequency, should be above this pole[13]. For sufficient phase margin it is suggested[13] that this zero should be at one tenth of the switching frequency, in this case at 100 kHz, using simulation this can be verified. After simulation the zero position can be tweaked to get the desired phase margin at the cross-over frequency.

2) Select RC components and set external ramp compensation
The gain ratio, V_{ramp} and the inductor current slope have influence on the Q-factor of the sub-harmonic pole. A design is made for a Q factor of 1 to damp the sub-harmonic poles sufficiently. The mid frequency gain ratio should be selected by setting R_i and R_z. The V_{ramp} amplitude is chosen as 5 V.

The inductor current slopes and V_{ramp} can be entered in the the Q-factor equation (2.11), the equation still holds for the decoupled case as the inductor slopes do not change, only the average inductor current is different. Using this equation the mid-frequency gain ratio is set:

$$\begin{aligned}
Q &= \frac{1}{\pi[(R_s' \frac{V_{DD}}{L} + V_{ramp} f_s)/(R_s' \frac{V_{out}}{L}) - 0.5]}, R_s' = R_s \frac{R_z}{R_i} \\
\frac{1}{Q\pi} + 0.5 &= \frac{R_s' \frac{V_{DD}}{L} + V_{ramp} f_s}{R_s' \frac{V_{out}}{L}} = \frac{V_{DD}}{V_{out}} + \frac{V_{ramp} f_s L}{R_s' V_{out}} \\
Rs' &= \frac{V_{ramp} f_s L}{V_{out}(\frac{1}{Q\pi} + 0.5 - \frac{V_{DD}}{V_{out}})} \\
\frac{R_z}{R_i} &= \frac{1}{R_s} \cdot \frac{V_{ramp} f_s L}{V_{out}(\frac{1}{Q\pi} + 0.5 - \frac{V_{DD}}{V_{out}})} = \frac{1}{0.1} \cdot \frac{5 \cdot 1\mathrm{e}6 \cdot 3.3\mathrm{e}{-6}}{45(\frac{1}{\pi} + 0.5 - \frac{12}{45})} \approx 6.6
\end{aligned}$$

This sets every parameter in the current loop compensator, R_z is taken as 20 kΩ and R_i as 3 kΩ. Initially the zero was to be placed at $f_s/10$ but simulations showed that the phase margin was insufficient, the zero is now placed at $f_s/15$ for >45° phase margin. The pole should be at $f_s/2$ to attenuate the switching ripple (especially the higher harmonics):

$$\begin{aligned}
C_z &= \frac{1}{2\pi f_z R_z} = \frac{1}{2\pi \cdot 66\mathrm{e}3 \cdot 20\mathrm{e}3} \approx 120\,\mathrm{pF} \\
C_p &= \frac{C_z}{2\pi f_0 R_z C_z - 1} = \frac{80\mathrm{e}{-12}}{2\pi \cdot 500\mathrm{e}3 \cdot 20\mathrm{e}3 \cdot 120\mathrm{e}{-12} - 1} \approx 18\,\mathrm{pF}
\end{aligned}$$

Every component in the current loop is now designed and simulations can be done to verify the loop gain and transfer functions.

3) Voltage compensation design
Now that the current loop is well defined, a voltage loop compensator can be designed with the same compensator structure as the current loop compensator. The average current mode loop V_c to V_{out} transfer function will be the basis for the voltage loop compensation design. This will be done in the next part of this chapter.

Resulting system

The complete current loop can now be build in SIMPLIS for simulation. The schematic from figure 4.9 is implemented in the simulation tool. With this simulation tool, AC analysis can be performed to get the small signal behaviour of the system. Using an FFT on the data from time domain simulation, the THD can be determined. The results of these simulations will be shown later at the end of this chapter.

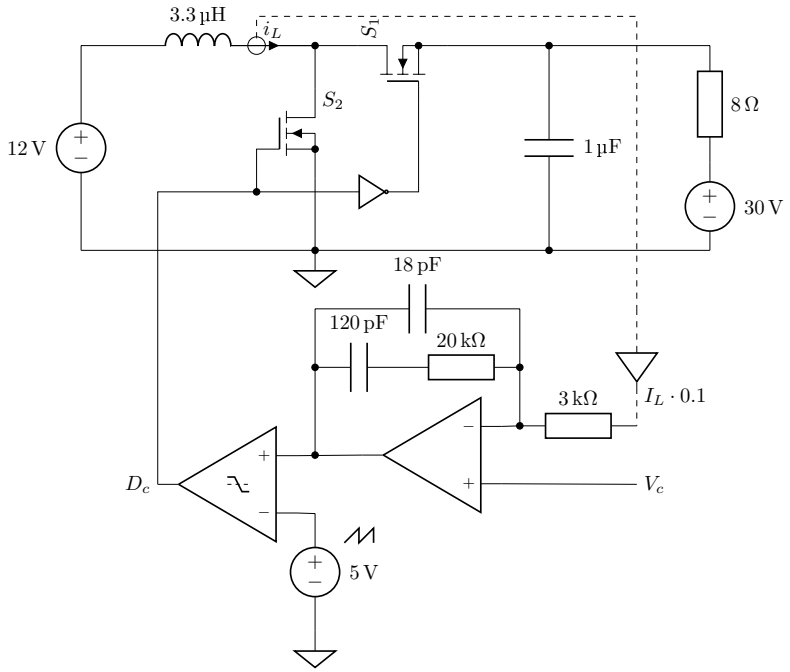

Figure 4.9: The resulting system after the current loop design. All component values are shown. This schematic will be used in simulation to investigate the current loop performance.

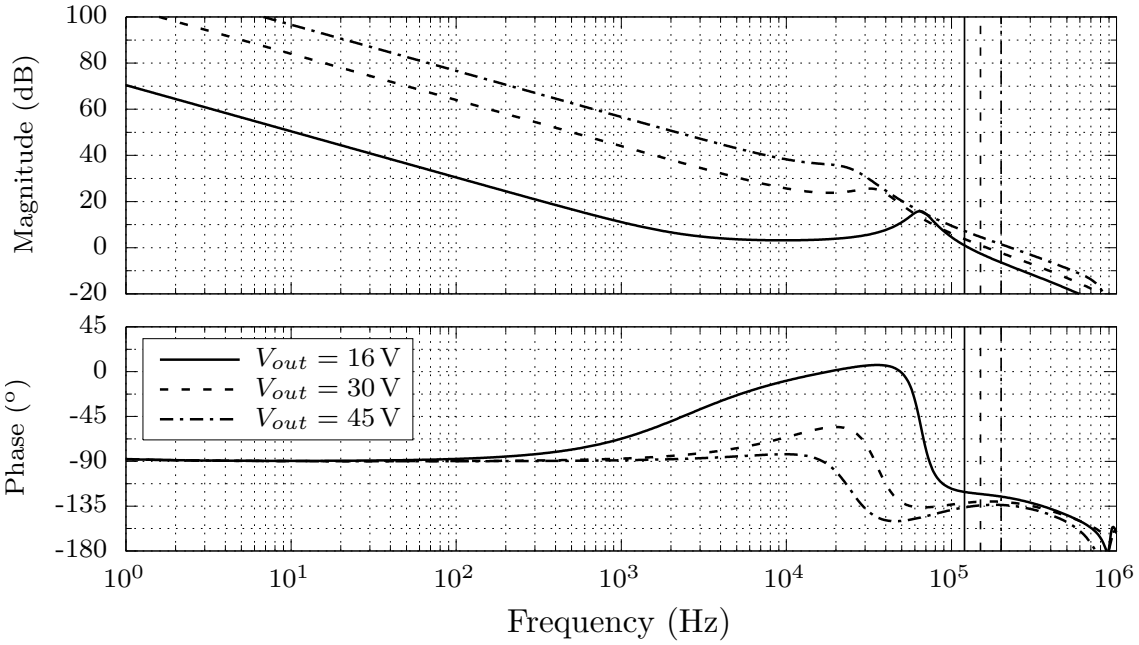

Figure 4.10: **Loopgain** The simulated current loop gain is plotted for different output voltages, as the output voltage drops the loop gain also drops. The phase margin can be deduced from the graph and is in all cases more than 45°.

For stability it is important that for each operating condition the phase margin is sufficient. In the

previous section a design was made for a phase margin $> 45°$. Figure 4.10 shows the loop gain of the average current mode controlled inner loop. It can be seen that at crossover the phase margin is at least 45° in each case. This means that the current loop is unconditionally stable, when used within the designed limits (output voltage between 15 V to 45 V).

The current loop gain drops (figure 4.10) as the output bias is decreased, this can be explained by looking at equation 2.1. The duty-cycle to inductor current gain is low for low duty-cycles, this shows up as a gain drop in the loop gain. Looking at figure 4.11 the control to inductor current transfer can be seen. The resulting graphs are flat except for the graph at the lowest bias level. This is the result of the drop in loop gain at the lowest bias level.

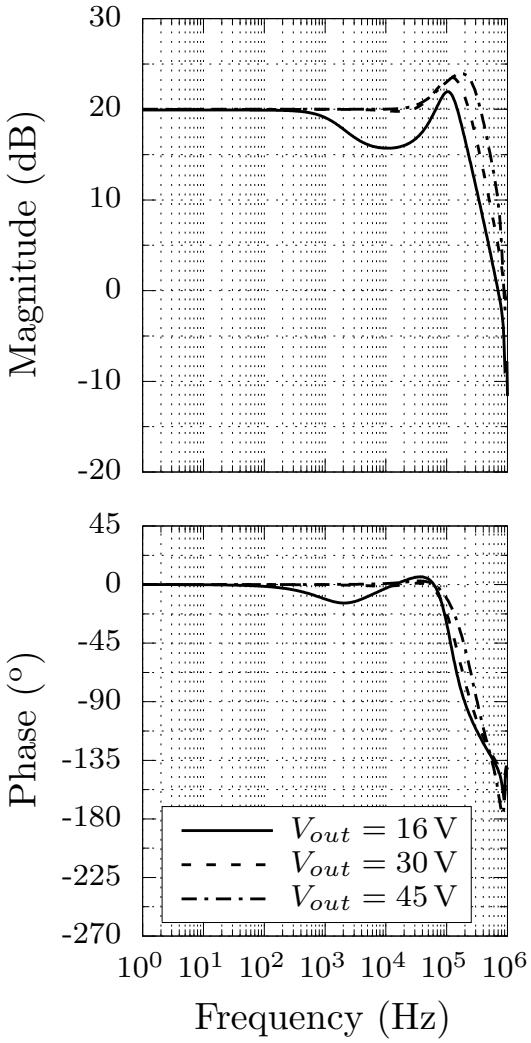

Figure 4.11: **Il/Vc transfer** The simulated control to inductor current transfer is plotted here, it shows that a flat control to inductor current is achieved. A small deviation is seen where the output voltage is the lowest. This is caused by the low loop gain at 16 V shown in figure 4.10.

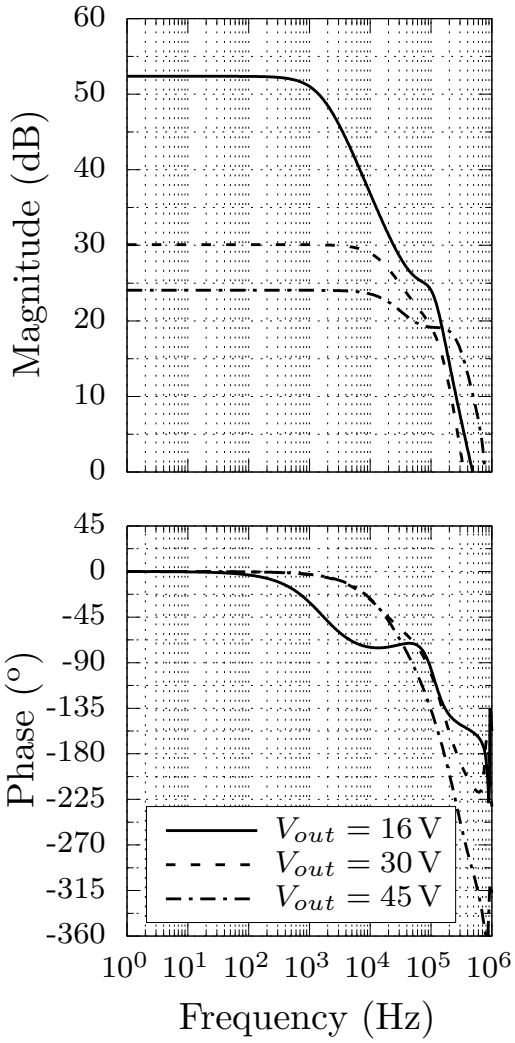

Figure 4.12: **Vo/Vc transfer** The simulated control to output voltage is plotted for different output voltages, this transfer can be used for designing the voltage loop. There is also no peaking at Fs/2 indicating a good damping of the sub-harmonic poles.

The control to output voltage transfer is shown in figure 4.12, this shows the large non-linear DC-gain of the converter at different bias levels. The primary pole location at the different bias levels correspond with the pole location given in equation 4.3.

Furthermore it is also interesting to see the right half plane zero becomes a normal zero if the

current is negative ($V_{out} = 16\,\mathrm{V}$), this behaviour and the locations of the right half plane zero frequency correspond with equation 4.1.

Figure 4.12 is used later for the voltage loop design.

4.4 Designing the Pre-distorter

Next the pre-distorter can be introduced before the control terminal of the current loop. As can be seen in section 3.2 the pre-distorter for the average current mode controller is a second order polynomial function.

The function that needs to be implemented is (equation 3.5):

$$\begin{aligned} V_{out} &= \frac{V_{pd,in}}{\gamma} \\ V_{pd,out} &= \frac{(\frac{V_{pd,in}}{\gamma})^2 - \frac{V_{pd,in}}{\gamma} V_{bias}}{R_L V_{DD}} \cdot R_s \\ V_{pd,out} &= \frac{R_s}{\gamma^2 R_L V_{DD}} (V_{pd,in})^2 - \frac{R_s V_{bias}}{\gamma R_L V_{DD}} V_{pd,in} \end{aligned} \tag{4.4}$$

It is still possible to choose the control voltage to output voltage gain gamma (γ). As mentioned in section 3.2 a gain of 0.2 is beneficial because that will set the output bias level at the voltage compensator to half the supply voltage of the voltage loop (12 V).

If this polynomial is going to be implemented in a circuit implementation, a non-linear block is needed which has a square input (the first term) and a linear input.

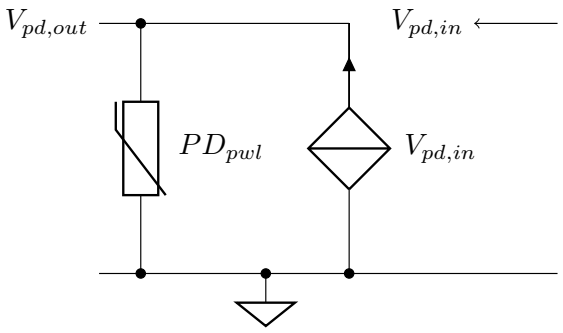

Figure 4.13: The predistorter implementation in the simulation tool, the input voltage is converted to a current and fed in a non-linear resistor. $V_{pd,out}$ is fed into the high impedance opamp input terminal of the current feedback loop.

In the SIMPLIS simulator it is impossible to insert non-linear blocks or functions. Therefore a piecewise-linear (PWL) model is made in Matlab. The pre-distorter will then be a piecewise resistor + voltage controlled current source representing the non linear transfer given in the equations above. This implementation is shown in figure 4.13.

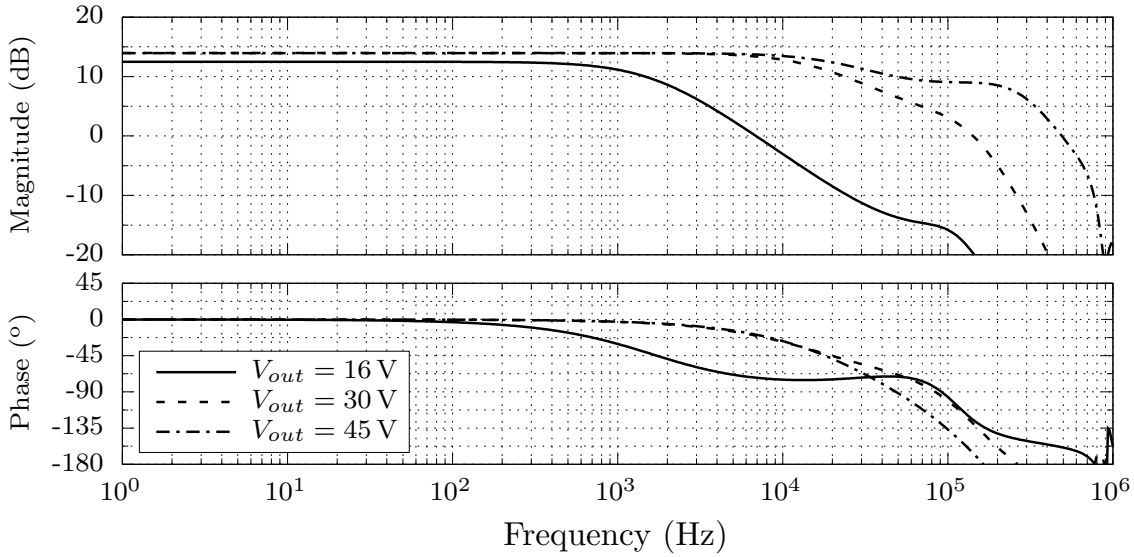

Figure 4.14: **Vo/Vpd,in transfer** The simulated pre-distorter input to current loop output voltage transfer is shown in this plot, here the pre-distorter action can be seen clearly as the DC-gain is now constant at different bias levels.

The resulting small signal transfer of the current loop including pre-distorter can be seen in figure 4.14. For this simulation the pre-distorter shown in figure 4.13 has been introduced before the control input of figure 4.9.

The DC-gain at different output voltages is now constant in comparison with figure 4.12, exactly what is expected when a pre-distorter is introduced.

4.5 Designing the voltage feedback

The last stage of the design before a fully functional amplifier is acquired, is the voltage feedback loop. This loop makes the output voltage track the reference voltage, where the reference signal will be the audio signal. The gains and phases of the current loop and pre-distorter are now known and can be used to design a compensator for the voltage feedback loop.

The design needs to be done two times, first without pre-distorter and secondly where the pre-distorter is included in the loop. This is done because the improvement with pre-distorter can then be investigated. The first thing that needs to be determined is the voltage loop crossover frequency. This is set to 20 kHz to stay away from the RHPZ-position as described in section 4.3.

The following design procedure is followed:

1. Determine the feedback resistors for the required closed loop DC-gain (figure 4.15).
2. Determine the worst case gain and phase values of the average current mode control to output voltage transfer, at the wanted voltage loop crossover frequency.
3. If a pre-distorter is included, multiply the found gain value with the pre-distorter gain.
4. Use the k-factor design[4, p 263] to determine the required pole and zero separation in the compensator for a certain voltage loop phase margin (figure 4.18).
5. Calculate the compensator (figure 4.16) components based on the k value.

All steps are explained in detail in the following sections.

Voltage sensor gain

From the specifications it is known that the input amplitude is a maximum of 1.5 V and the output amplitude 15 V. This means that the feedback should have an attenuation of 10 x. The question

is then how to set the feedback factor.

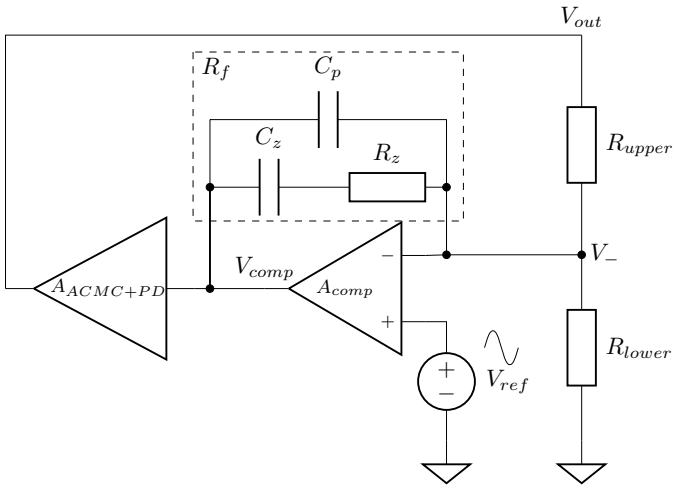

Figure 4.15: Simplified schematic for calculating the closed loop voltage transfer of the whole system. This is not a trivial non-inverting op-amp configuration, as R_f will inject current at higher frequencies.

The simplified feedback system is shown in figure 4.15. In the traditional $A/(1 + A\beta)$ system the closed loop gain is set by the β of the system as shown in section 2.3. However in this system it is not possible to separate feedback factor β and forward gain factor A.

R_{lower} does not play a role from a small signal point of view due to the virtual ground point at the negative input terminal. It is consequently only possible to calculate the loop-gain $A\beta$ and not the separate A and β factors. The closed loop gain has to be derived in a different way to find the components which set the required closed loop gain.

At first glance the ratio between R_{upper} and R_{lower} set the system gain and makes the system behave like a typical non-inverting op-amp, this can be seen intuitively as R_f is open for DC.

The closed loop transfer and DC gain can be calculated in an alternate way with the help of the superposition principle at the V_- node. V_{out} and V_{comp} are dependent sources, however superposition is still valid provided the controlling variable is not set to zero when the sources are deactivated[29]. The full derivation is done in appendix B.

With the results from appendix B and A_{comp} set to infinity, the closed loop transfer is obtained:

$$\lim_{A_{comp}\to\infty} \frac{V_{out}}{V_{ref}} = \frac{A_{ACMC+PD}(R_{lower}R_f + R_f R_{upper} + R_{lower}R_{upper})}{R_{lower}(A_{ACMC+PD}R_f + R_{upper})} \tag{4.5}$$

Where R_f is infinite at DC:

$$\lim_{R_f\to\infty} \frac{V_{out}}{V_{ref}} = 1 + \frac{R_{upper}}{R_{lower}}$$

The DC gain is determined by the R_{upper} and R_{lower} resistors in the same way as a non-inverting amplifier. When the frequency becomes higher R_f will also play a role, influencing the closed loop gain for higher frequencies. Equation 4.5 is used later to compare closed loop simulations and measurements to the analytical closed loop derivation.

Using $R_{upper} = 18\,\text{k}\Omega$ and $R_{lower} = 2\,\text{k}\Omega$ a 10 x DC-gain is obtained.

Compensator design

The compensator structure for the voltage loop is a type 2 compensator with an integrator pole and a pole plus zero. The zero is used to compensate for the extra phase shift caused by the integrator pole. The high frequency pole attenuates output voltage ripple. The compensator structure is shown in figure 4.16.

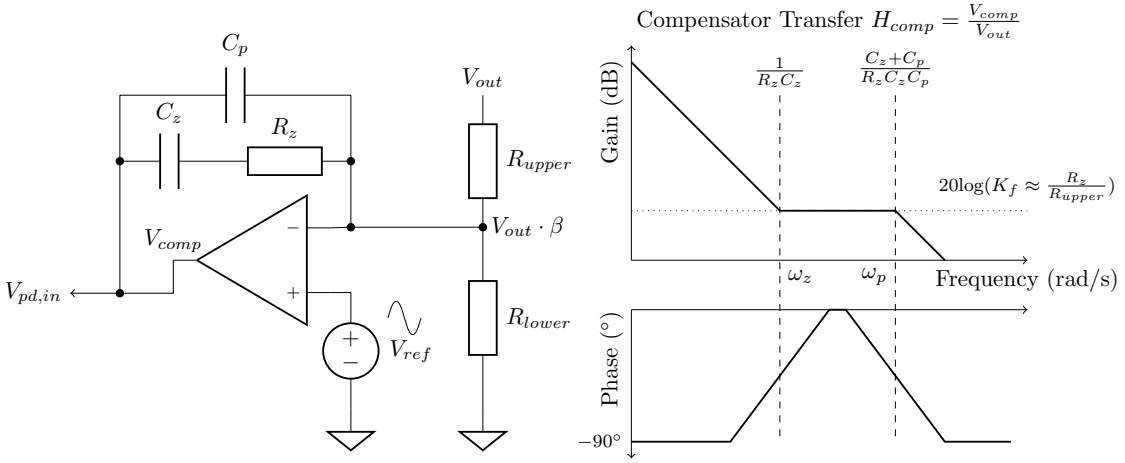

Figure 4.16: The compensator structure that will be used for the voltage loop compensator is shown here.

The transfer from V_{out} to V_{comp} is given by:

$$H_{comp} = \frac{V_{comp}}{V_{out}} = \frac{1 + C_z R_z s}{sR_{upper}(C_z + C_p)(1 + sR_z \frac{C_z C_p}{C_z + C_p})}$$

$$\omega_z = \frac{1}{R_z C_z}$$

$$\omega_{p1} = 0, \omega_{p2} = \frac{C_z + C_p}{R_z C_z C_p}$$

$$K_f = \frac{R_z C_z}{R_{upper}(C_z + C_p)} \approx \frac{R_z}{R_{upper}}\bigg|_{C_z >> C_p}$$

The component values are calculated based on the k-factor design described in the next section.

K-factor stabilization tool

For setting the loop gain it is possible to do manual pole and zero placement in the compensator to select a loop gain cross-over frequency with the required phase margin, this is however tedious and quite involved.

In the 1980s Dean Venable introduced the concept of K-factor compensation of converters[4, p 263]. The K-factor indicates the necessary separation between the pole and zero frequency positions in the compensation network to get the required phase boost at the crossover frequency (figure 4.18).

The current loop control to output voltage transfer can be used to acquire the phase and gain at the desired loop crossover frequency. Together with the wanted phase margin at crossover the k value can be calculated.

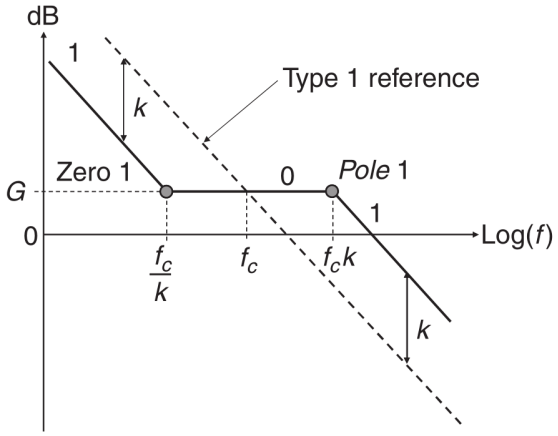

Figure 4.17: Principle of k-factor compensation design[4, p 263], the pole and zero are split around f_c, a certain gain and phase boost is achieved at the desired crossover frequency.

In this case the voltage loop compensation is designed for the worst case of the current stage (figure 4.14) so that the system is stable for the whole designed output voltage range. The derivation for the pole placement can be done in the following way[4, p 264]:

$$
\begin{aligned}
f_z = \frac{f}{k}, f_0 = kf \\
\phi_{boost} &= \tan^{-1}\left(\frac{f}{f_z}\right) - \tan^{-1}\left(\frac{f}{f_0}\right) \\
&= \tan^{-1}(k) - \tan^{-1}\left(\frac{1}{k}\right) \\
&= \tan^{-1}(k) - 90 + \tan^{-1}(k) \\
\tan^{-1}(k) &= \frac{\phi_{boost}}{2} + 45 \\
k &= \tan\left(\frac{\phi_{boost}}{2} + 45\right)
\end{aligned}
$$

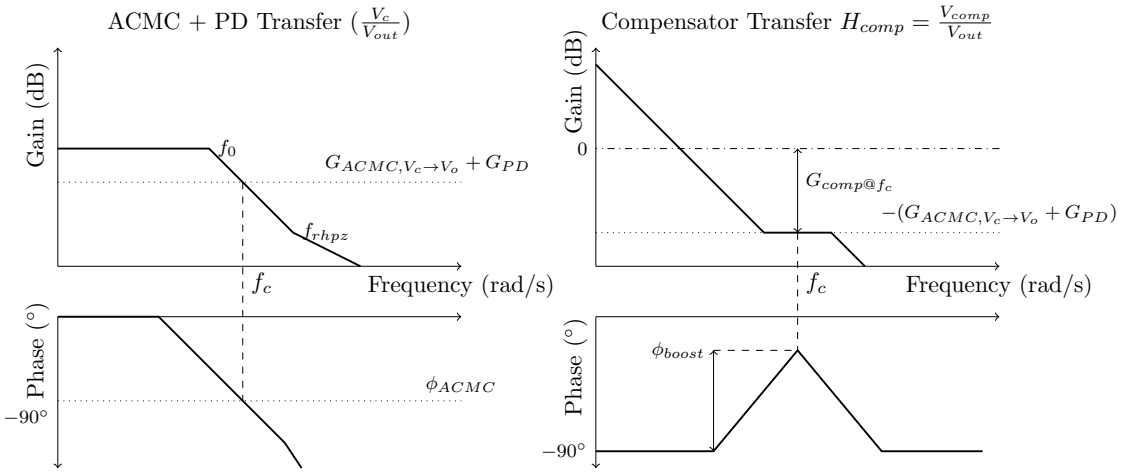

Figure 4.18: Application of k-factor compensation design[4, p 263] on the average current mode controlled power stage. The gain and phase of the current mode loop are used to calculate the required mid frequency gain and phase boost in the compensator.

The amount of phase boost (see figure 4.18) that is needed can be calculated, the final phase should

be -180 plus the phase margin.

$$\begin{aligned}\phi_{boost} &= -180 + PM + (-\phi_{ACMC}) + 90 \\ &= PM - \phi_{ACMC} - 90\end{aligned}$$

The $-90°$ follows from the integrator pole ($s = 0$) in the voltage loop compensator. The power stage also contributes with a negative phase shift. Adding these together the final required phase boost is found to meet the phase margin. From this phase boost the k can be calculated as shown above.

$$G_{comp@f_c} = -(G_{ACMC,V_c \to V_o} + G_{PD}) \tag{4.6}$$

The required gain boost or reduction at the voltage loop cross-over frequency is also given (equation 4.6), the sum of the mid frequency voltage loop compensator gain and the average current mode gain should be zero per definition of the crossover frequency. This gain should include the gain of the average current mode control to output voltage at the desired crossover frequency and the pre-distorter gain. This principle is shown in figure 4.18.

The component values for the compensator (figure 4.16, see also figure 4.19) can then be calculated using the found k:

$$\begin{aligned}C_z &= \frac{1}{2\pi f_c G_{f_c} k R_{upper}} \\ C_p &= C_z(k^2 - 1) \\ R_z &= \frac{k}{2\pi f_c C_p}\end{aligned}$$

A 45° - 60° phase margin is chosen to prevent large overshoot, which would cause instability as the output voltage would increase beyond the designed 45 V.

Together with the current controlled power stage transfer and pre-distorter gain, the voltage loop compensator can be designed. The same procedure can be followed without including the pre-distorter gain. This allows for two versions where the improvement with pre-distorter can be compared to the system without pre-distorter.

Resulting system

Using the values from the previous section the compensation components can be calculated. A summary is given in the following table:

Table 4.2: Design parameters for the voltage loop

Parameter	**Value**
Voltage sensor gain	0.1
Voltage loop crossover f_c	20 kHz
Phase margin	45° - 60°
DC-gain	10 x

As said before, the design needs to be done two times, first without pre-distorter and secondly where the pre-distorter is included in the loop. For the first case figure 4.12 can be used in the k-factor design. Using figure 4.14 the phase and gain parameters for the second case can be determined. This principle has been explained in figure 4.18.

Table 4.3: Parameters for K-factor design and the resulting component values. The parenthesized values are standard component values, these values are used for simulation and prototype implementation.

	Without pre-distorter	**With pre-distorter**
Current Loop Gain ($G_{ACMC} + G_{PD}$)	22.5 dB	12.4 dB
Current Loop Phase (ϕ_{ACMC})	$-55°$	$-70°$
Voltage Loop Crossover f_c	20 kHz	20 kHz
Phase Margin	60°	60°
Compensator Crossover Gain ($G_{comp@f_c}$)	-22.5 dB	-12.4 dB
Compensator Phase Boost (ϕ_{boost})	25°	40°
R_{upper}	18 kΩ	18 kΩ
R_{lower}	2 kΩ	2 kΩ
C_p	3.72 nF (3.9 nF)	859 pF (820 pF)
C_z	5.49 nF (5.6 nF)	3.09 nF (3 nF)
R_z	2.27 kΩ (2.2 kΩ)	5.51 kΩ (5.6 kΩ)

It can be noticed that the phase shift which is used in the k-factor design, in the case with pre-distorter, is less than the value resulting from figure 4.23. This value is deliberately taken more negative to have more phase boost and therefore enough phase margin when output voltages are low. This problem is the result of having to design for a fixed case which determines the component values. A dynamic voltage compensator structure for example implemented in the digital domain would circumvent these issues.

The complete system is shown in figure 4.19 where the components from table 4.3 can be filled in.

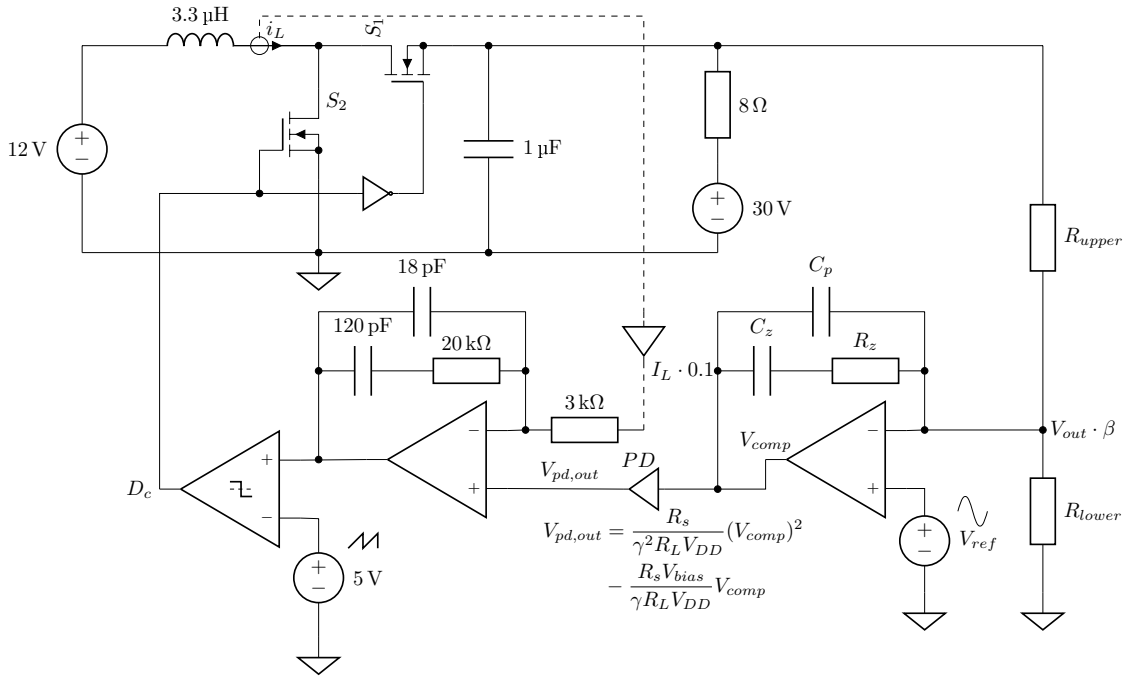

Figure 4.19: The resulting system after the voltage loop design. All component values are shown. This schematic will be used in simulation to investigate the voltage loop performance. The values for the voltage compensator are given in table 4.3.

For stability of the voltage loop it is of interest to look at the loop gain at different bias points, these are plotted without pre-distorter in figure 4.20 and with pre-distorter in figure 4.21. The integration action of the voltage compensator can clearly be seen in both figures, giving high DC-gain for low frequencies. It also shows that the loop gain changes depending on output voltage

level, this is due to the highly changing plant dynamics shown in figures 4.12 and 4.14, and is unavoidable.

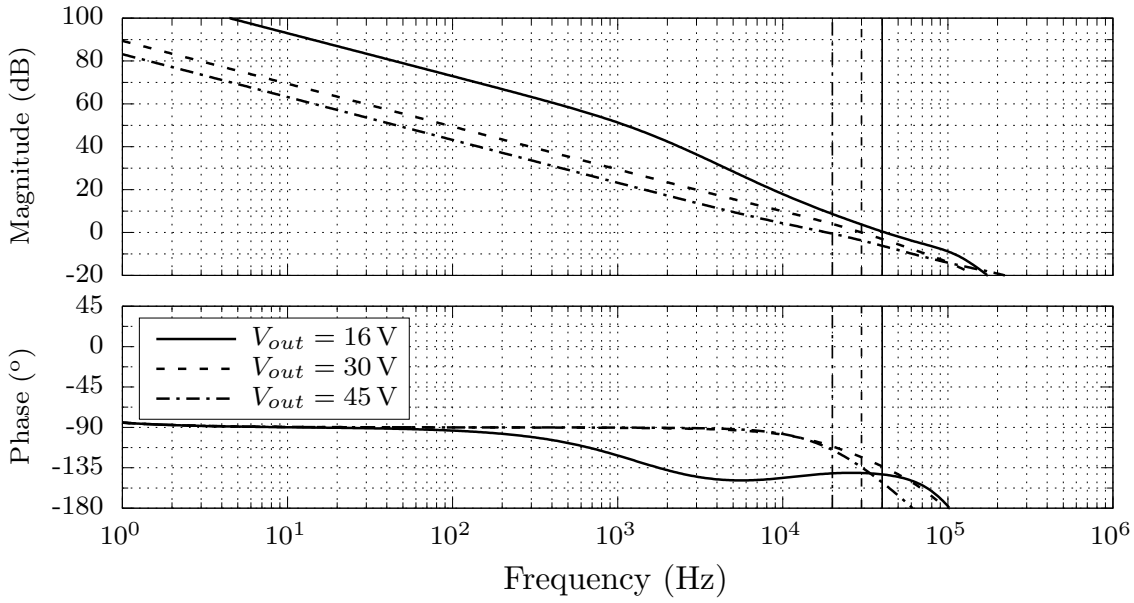

Figure 4.20: **Loopgain** The simulated voltage loop gain without pre-distorter is plotted for different output voltages, as the output voltage drops, the loop gain crossover also drops. The phase margin can be deduced from the graph and is worst case about 40°.

The loop gain with pre-distorter is mostly constant as the DC-gain of the current mode loop is constant if a pre-distorter is included. For low output voltage however the loop gain crossover frequency is reduced, this is due to the low in frequency output pole at 16 V shown in figure 4.14.

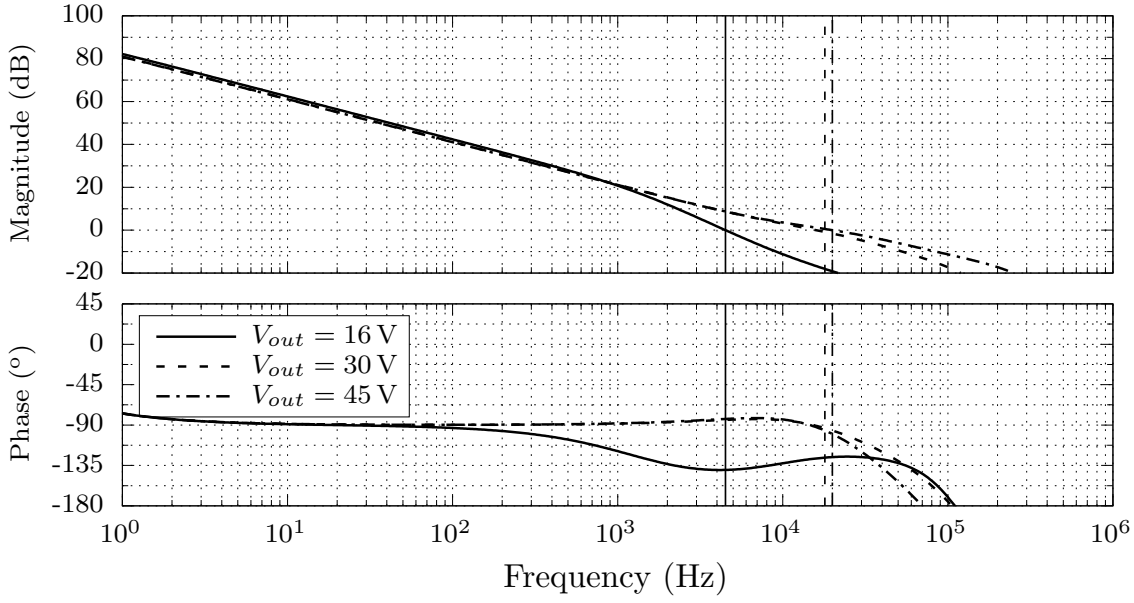

Figure 4.21: **Loopgain** The simulated voltage loop gain with pre-distorter is plotted for different output voltages, as the output voltage drops the loop gain crossover also drops. The phase margin can be deduced from the graph and is worst case about 40°. For larger voltages the phase margin is much larger (85°)

Closed loop transfer

For the final system it is of interest to know the closed loop bandwidth, the $-3\,\mathrm{dB}$ point should be at least at $20\,\mathrm{kHz}$. The closed loop transfer functions are plotted for different bias levels in figure 4.22 and 4.23.

These are then compared with the analytically derived transfer function shown in equation 4.5. The analytical transfer function is subsequently estimated as an analytical expression of $A_{ACMC+PD}$ is not available. The s-domain estimation of $A_{ACMC+PD}$ is made in MATLAB from the simulated current loop V_c to V_{out} transfer function at the different bias levels.

The bandwidth is much larger than $20\,\mathrm{kHz}$ in almost all cases, except in the lowest voltage case with pre-distorter. This can be explained by looking at the loop-gain with pre-distorter in graph 4.21. The loop-gain crossover at $4\,\mathrm{kHz}$ causes the premature gain drop at the lowest bias level with pre-distorter.

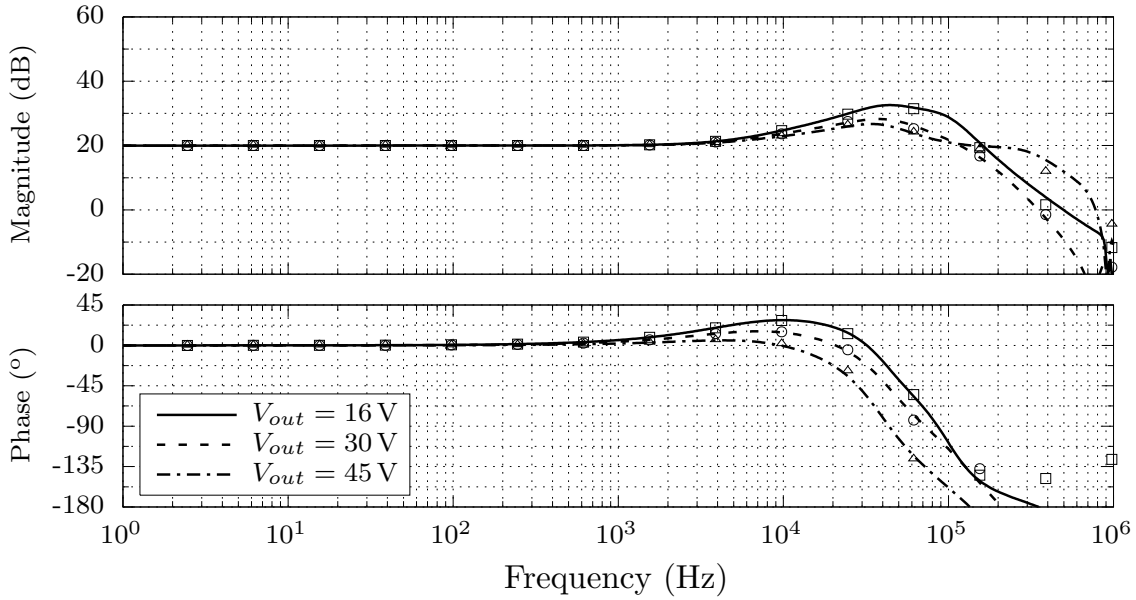

Figure 4.22: **Vout/Vref** The closed loop transfer without pre-distorter, there is gain peaking in all cases due to the influence of the R_f feedback in the voltage compensator structure. The points show the estimated analytical transfer (equation 4.5) where the lines represent simulation results.

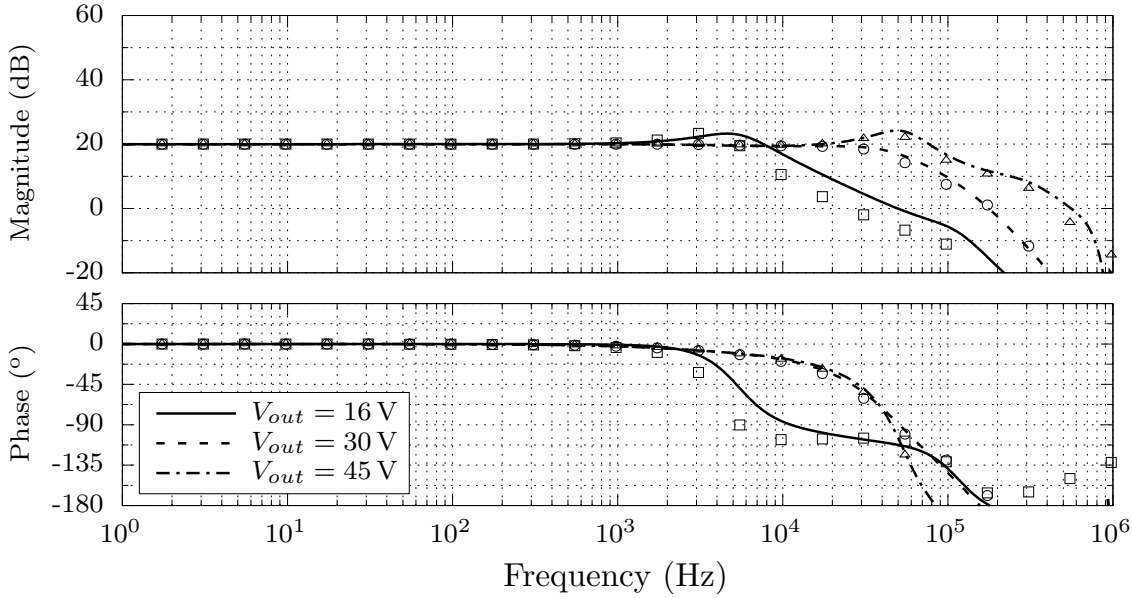

Figure 4.23: **Vout/Vref** The closed loop transfer with pre-distorter. The points show the estimated analytical transfers (equation 4.5) where the lines represent simulation results.

In both bode plots the predicted closed loop transfer calculated in the appendix matches the simulation results. The only outlier is the 16 V transfer with pre-distorter. It is suspected that this is the result from the s-domain transfer function estimation of $A_{ACMC,V_c \to V_{out}}$ which does not match completely.

4.6 Simulation results

After designing all the individual components, the system can be verified using simulation. Small signal behaviour has already been looked at in the previous section. Now it is of interest to look at large signal behaviour to verify the power stage mathematics from chapter 3 and pre-distorter equations.

After large signal simulations the THD can be found. For all the THD simulations an output amplitude of 10 V is used to have enough output voltage swing. In this way the distortion will be easily measurable. Two cases are simulated for both open voltage-loop and closed-loop systems: without and with parasitic effects in the power stage.

A list of these parasitic effects:

- Current sense resistor (5 mΩ)
- Equivalent series resistance in the inductor (6 mΩ)
- R_{on} of the MOSFETs (17 mΩ)
- Body diode in the MOSFETs
- Dead-time in the gate-driver (As measured in chapter 5)
- 1 quadrant supply with decoupling
- Decoupling capacitor

These parasitic effects limit the minimum amount of distortion that is achievable. These parasitic effects are unavoidable if the system is built in a circuit implementation so therefore they should also be simulated for comparison to the prototype circuit implementation later.

The results of all large signal simulations are decimated and low-pass filtered as otherwise graphs would become cluttered and the comparison to the analytical expressions unclear.

Current loop

The small signal characteristics for the current loop are already investigated in the current loop and pre-distorter design sections. Now it is of interest to verify the calculations done in chapter 3 and see if the pre-distorter works as expected.

Figure 4.24 shows the output voltage when the control input is not pre-distorted. Both the output voltage and inductor current are low-pass filtered before they are plotted. From chapter 3 it is expected that the current is linearly dependent on the control and the output voltage follows equation 3.6.

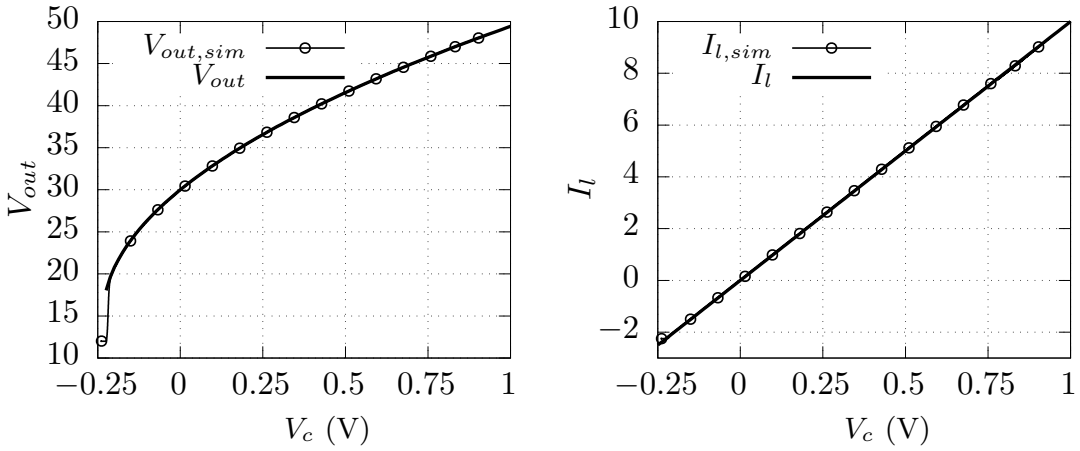

Figure 4.24: The control voltage is swept without the use of pre-distortion using simulation. The resulting $V_{out,sim}$ and $I_{l,sim}$ are shown, the in chapter 3 predicted (equation 3.6) V_{out} and I_L are plotted in the same graph.

With pre-distorter the output voltage is linearly dependent on the control voltage and the current is quadratic, predicted by equation 3.7 and 3.5. Figure 4.25 shows the simulated output voltage and inductor current next to the predicted output voltage and inductor current.

The simulation results match with the predicted equations and show that the output voltage is now linearly dependent on the control voltage.

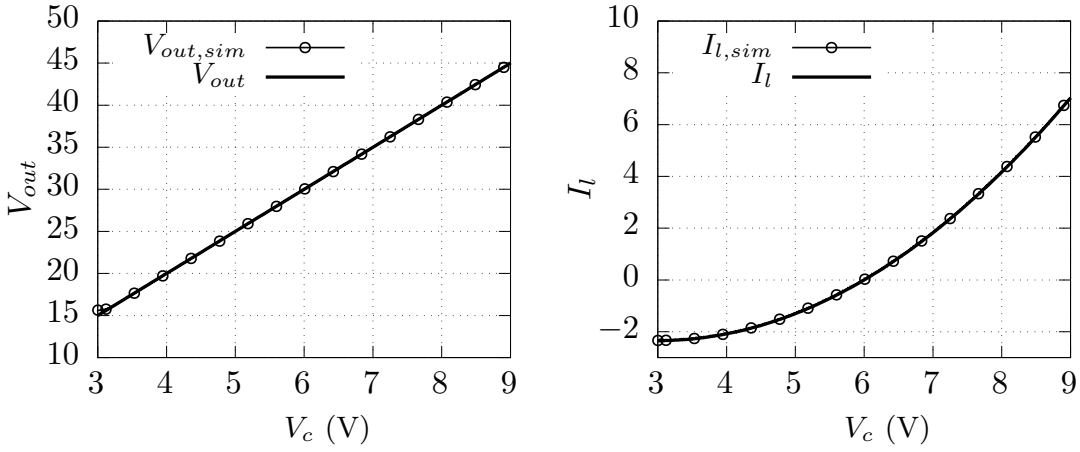

Figure 4.25: The control voltage is swept including pre-distorter using simulation. The resulting $V_{out,sim}$ and $I_{l,sim}$ are shown, the in chapter 3 predicted (equation 3.7) V_{out} and I_L are plotted in the same graph.

Now that the output voltage is linearly dependent on control voltage, the improvement in THD can be investigated in an open voltage loop way. Four simulations are done to investigate the THD

improvement of the pre-distorter. The THD without and with pre-distorter is simulated for the ideal power stage and for a power-stage with non-ideal components. All simulations are done at an output amplitude of 10 V. The results of both simulations can be seen in figure 4.26.

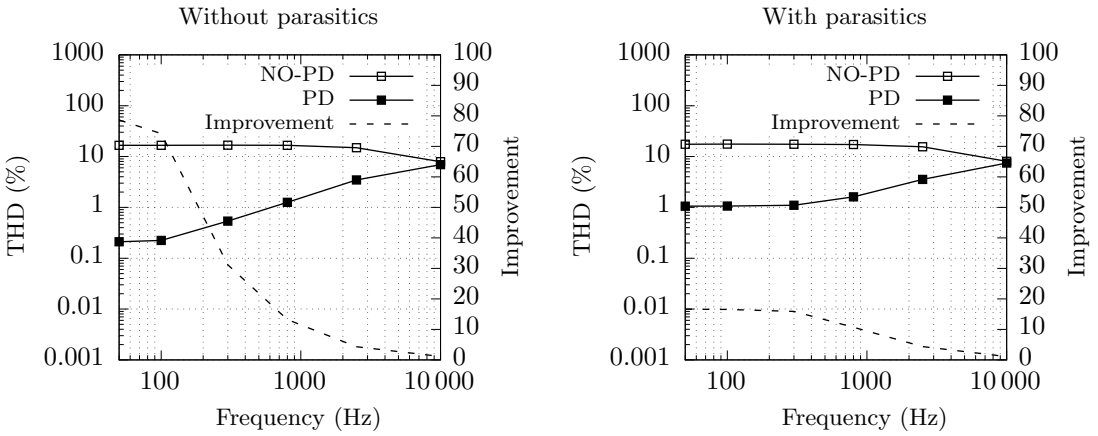

Figure 4.26: In this graph the open voltage loop distortion is plotted, all simulations are done at an output voltage amplitude of 10 V.

Without parasitics the improvement in THD is very large for low frequencies, a frequency dependent improvement is also visible in both graphs. As predicted in the power stage design section (4.2), this can be explained by the impedance of the output buffer capacitor. This impedance drops to 16 Ω at 10 kHz. The output load impedance is then reduced from 8 Ω to 5.5 Ω. As the pre-distorter curve is also dependent on the load resistance one can imagine that for higher frequencies the effectiveness of the pre-distorter is reduced.

With parasitics the effectiveness is reduced but an improvement of 15 x is still obtained.

Voltage loop

The voltage loop can now be closed, this results in the completed audio amplifier. Large signal simulations can be performed to show that the voltage loop works as intended.

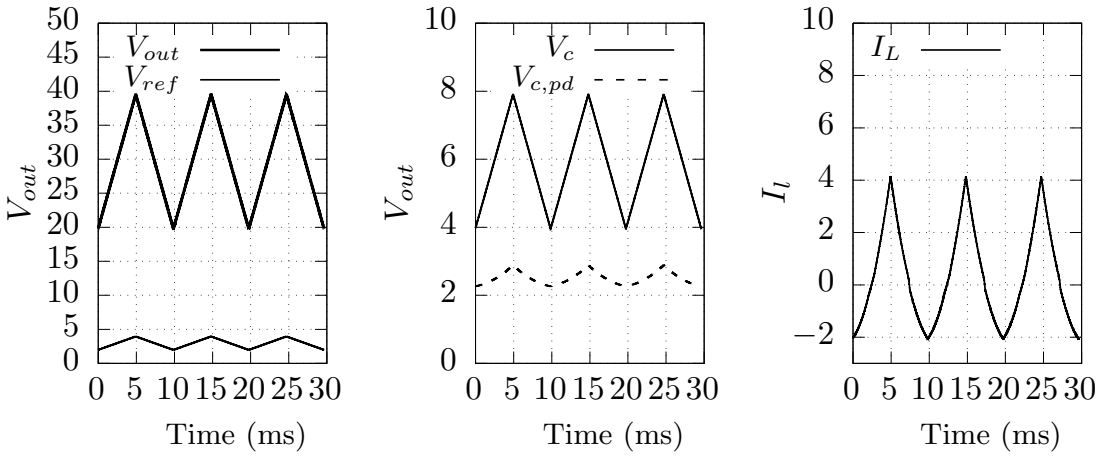

Figure 4.27: A 100 Hz triangle wave is applied to the reference input of the voltage loop. In this figure the pre-distorter action can clearly be seen in the second graph, the control voltage is pre-distorted and the voltage loop output V_c closely follows V_{ref} indicating the pre-distorter works as intended. The current follows the quadratic behaviour shown in figure 4.25.

A good way to show the pre-distorter action is to apply a triangle signal. A 100 Hz triangle wave is applied to the reference input of the voltage loop, the result is shown in figure 4.27. In this figure

the pre-distorter action can clearly be seen, in the second graph the control voltage is pre-distorted and the voltage loop output V_c closely follows V_{ref}, indicating the pre-distorter works as intended.

Pre-distortion of the current loop showed a big improvement in THD, this can now be combined with feedback for more distortion reduction. The simulation results are shown in figure 4.28.

Results shows that an extra improvement of 10x with pre-distortion is obtained for lower frequencies. It can also be seen that THD saturates to 0.01%. Using the results from the previous section a larger improvement should be expected. A possible explanation is the aliasing of the output voltage ripple, resulting in closed loop distortion depending on the size of the ripple. This process has been described for Class D amplifiers in[30, 31]. Next to this effect the voltage loop without pre-distorter also has 10 dB more loop-gain at an output bias of 30 V. This extra 10 dB gives another factor 3 improvement.

Another effect is the THD rise as the frequency increases. This behaviour can be explained by looking at the voltage loop gain in figure 4.20. As the loop gain decreases the error suppression also decreases, which results in higher THD for an increase in frequency.

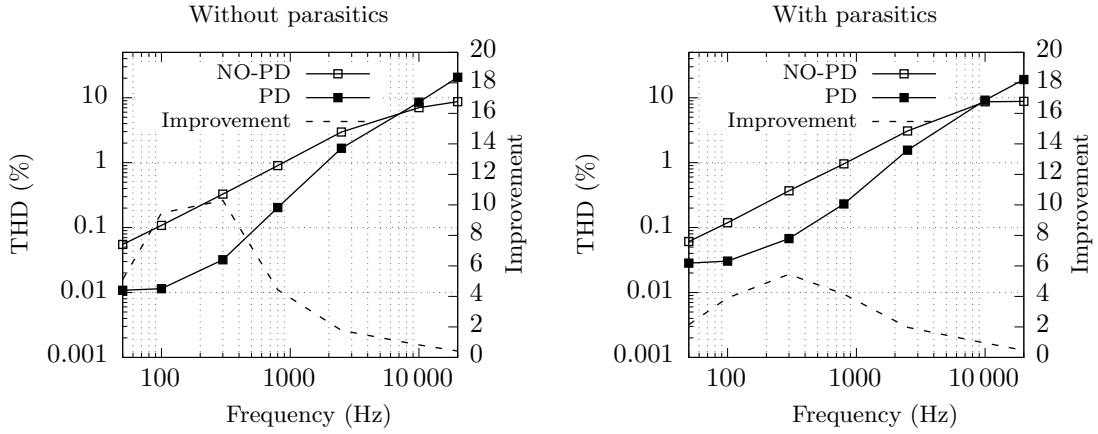

Figure 4.28: In this graph the closed voltage loop distortion is plotted for an output voltage of 10 V. The improvement in distortion is less impressive compared to pre-distortion of the current loop only, however total THD is still reduced by a factor 10. With parasitic elements however the THD improvement is reduced to a factor 5x.

The THD improvement of the pre-distorter also decreases as frequency rises. In chapter 3 the pre-distorter function has been derived, equation 3.5 shows a dependence on the load resistance. In section 4.3 the effect of the output capacitance is calculated. Figure 4.4 shows that the load impedance begins to change at 300 Hz. This is the point where the effectiveness of the pre-distorter begins to decrease as shown in figure 4.28.

With parasitic elements included in the simulation the minimum THD rises which further reduces the effectiveness of the pre-distorter.

Conclusion

In this chapter the power stage components have been selected using the required specifications. Limitations where found in the minimum load resistance as this determined the right half plane zero position. Another limitation came from the trade-off between maximum output voltage ripple, pre-distorter effectiveness and output pole location.

The trade-off between these components have been weighed and components where selected. Using the selected power stage components the current loop was designed. The V_c to V_{out} transfer of the current loop was used to design the voltage loop. The total system was then simulated.

Simulations show that it is possible to create a full bandwidth audio amplifier, with a THD level

comparable (factor 2) to the Class D amplifier mentioned in the specifications at the beginning of the chapter. The amplifier designed can now be converted to a real world design.

Chapter 5

Physical implementation and measurements

The design phase is now finished and the final design can be converted to a prototype circuit implementation. A circuit implementation brings forth a whole new set of parameters that should be taken into account. Some non-ideal effects have already been discussed, such as dead-time introduced in the power stage. Additionally components have a propagation delay, a limited gain-bandwidth and there is a maximum current and voltage components are able to handle. This is a non exhaustive list, however and important parameters will be discussed in detail in their corresponding section.

In the first part of this chapter the circuit implementation and component choices will be discussed, continuing with the design of a PCB.

A microcontroller will be used to protect the board against faults, for this controller software has to be created. The microcontroller can switch the power stage on and off based on a button press and fault conditions.

The top-level structure is shown in figure 5.1. The implementation is started at the power stage and preceding components are discussed in order.

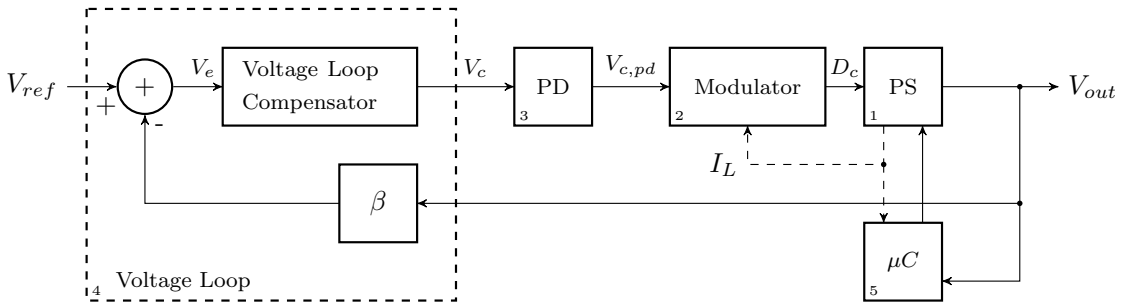

Figure 5.1: The top level view of the physical implementation, all the major components from the design are shown. A microcontroller is added to monitor current and voltages and to be able to turn the power stage on and off.

Finally measurement results will be presented and discussed in detail. Based on the discussion recommendations can be made for future work.

5.1 Implementation

In this section the different component are discussed in numerical order as shown in figure 5.1. For each component the considerations are explained and physical components are selected based on those requirements and considerations.

Power Stage

The most important part of the circuit is the power stage. The power stage also has some of the most intense design requirements as it will handle a lot of current and high voltages. Components are selected with a maximum output voltage of 60 V in mind. This is done to have enough voltage margin for start-up transients and possible fault conditions do not instantly destroy the components.

Inductor

The first part of the power stage is the inductor. For the inductor it is important to look at a few parameters: the series resistance, current handling capability, inductance de-rating and saturation current.

Saturation should be avoided at all times as the self-inductance drops rapidly, increasing the inductor current even more. This prevents the amplifier from working correctly and can even result in catastrophic failure of one of the power switches, depending on positive or negative current through the inductor.

A flat inductance to inductor current is required as a changing inductance over current introduces distortion (see section 3.3).

In section 4.3 the maximum inductor current ripple has been calculated, combining this value with the DC current the maximum inductor current is obtained:

$$\begin{aligned} I_{l,max} &= I_{R_L,max} \cdot \frac{V_{out}}{V_g} + \frac{1}{2}\Delta_{I_l} = \frac{V_{out,max} - V_{bias}}{R_{load}} \cdot \frac{V_{out}}{V_g} + \frac{1}{2}\Delta_{I_l} \\ &= \frac{45-30}{8} \cdot \frac{45}{12} + \frac{1}{2} \cdot 2.81 = 8.43\,\text{A} \end{aligned}$$

Using this maximum current an inductor can be selected, the goal is to have a flat self-induction up to 9 A and a DC resistance which is as low as possible. The inductor selected is a WE-HCC SMD High Current Cube 3.3 µH inductor[32] with 6 mΩ series resistance, a flat self-inductance up to 9 A and a saturation current of 15.5 A.

Gate driver

As the converter is a synchronous converter both switches are implemented with a MOSFET. Both switches are NMOS devices as gate charge and $R_{DS,on}$ are lower compared to a PMOS device as top switch. A gate driver is required to drive the switches as the top level switch requires a bootstrapped gate voltage to turn on.

The gate driver should have build-in dead time to prevent cross-conduction but this should be as low as possible to prevent harmonic distortion. Another requirement is the bootstrap voltage rating, the result of the addition of maximum output voltage plus gate source voltage.

Based on these requirements the LM5106[33] is selected. This device has programmable dead-time and a bootstrap voltage rating of 118 V.

There is a limit to the capacitance this device can drive based on thermal properties. When selecting MOSFETs there is a trade-off between gate charge and $R_{DS,on}$. The maximum gate

charge can be calculated if a maximum temperature rise of 50 °C is allowed:

$$\begin{aligned} R_{\Theta JA} &= 165.3\,^{\circ}\mathrm{C\,W^{-1}} \\ P_{max} &= \frac{50}{165.3} \approx 300\,\mathrm{mW} \\ 2C_{gate} &= \frac{2P_{max}}{f_s V^2} \\ 2Q_{gate} &= C_{gate}V = \frac{2P_{max}}{f_s V} \\ Q_{gate} &= \frac{0.3}{1\mathrm{e}6 \cdot 12} \approx 25\,\mathrm{nC} \end{aligned}$$

The bootstrap diode should at least have a maximum repetitive peak reverse voltage of:

$$\begin{aligned} V_{bootstrap} &= V_{out} + V_{gs} \\ &= 60 + 12 = 72\,\mathrm{V} \end{aligned}$$

A Schottky diode with a V_{rpr} of 100 V has been selected as bootstrap diode. The bootstrap capacitor needs to be a certain size to prevent bootstrap voltage ripple and is dependent on the gate charge. Based on calculations in the data sheet[33] the minimum capacitance needed is 5.7 nF. A common 100 nF capacitor is used instead as there are already many present on the board.

MOSFETs

The MOSFET selection can be done based on the maximum allowed gate charge and maximum drain-source voltage. The MOSFETs need to be able to withstand the maximum output voltage of 60 V, giving a minimum required V_{ds}.

MOSFET selection is also a trade-off between conduction + ripple loss and capacitive switching loss, the maximum capacitive gate loss has been calculated in the section describing the gate driver selection. The conduction and ripple loss is given as[34]:

$$\begin{aligned} P_{con} &= I_L^2(R_{ds,on} + R_{esr}) \\ P_{I_{rip}} &= \frac{1}{3} I_{rip}^2(R_{ds,on} + R_{esr}) \end{aligned}$$

When the converter is running at the designed output power of 12.5 W, the dissipated power is:

$$\begin{aligned} I_{out} &= \sqrt{\frac{P_{out}}{R_L}} = \sqrt{\frac{12.5}{8}} = 1.25\,\mathrm{A} \\ I_L &= \frac{I_{out}}{1 - D_c} = \frac{790\mathrm{e}{-3}}{1 - 0.73} = 4.62\,\mathrm{A} \\ I_{rip} &= \frac{1}{2}\frac{V_g}{L} T_s D_c = \frac{1}{2} \cdot \frac{12}{3.3} \cdot 0.73 = 1.32\,\mathrm{A} \\ P_{con} &= I_L^2(R_{ds,on} + R_{esr}) = 4.62^2 \cdot (R_{ds,on} + 0.006) \\ P_{I_{rip}} &= \frac{1}{3} I_{rip}^2(R_{ds,on} + R_{esr}) = \frac{1}{3} \cdot 1.32^2(R_{ds,on} + 0.006) \end{aligned}$$

The PSMN018-80YS[35] is selected based on the minimum required drain source voltage of 60 V, maximum current rating of 45 A, gate charge and a low $R_{ds,on}$. The device has a maximum drain source voltage of 80 V, a maximum gate charge of 25 nC at a gate overdrive voltage of 10 V and a low $R_{ds,on}$ of 17 mΩ.

This gives a total loss of:

$$\begin{aligned} P_{gatedriver} &= 300\,\text{mW} \\ P_{con} &= 4.62^2 \cdot (0.017 + 0.006) = 490\,\text{mW} \\ P_{I_{rip}} &= \frac{1}{3} \cdot 1.32^2 (0.017 + 0.006) = 12\,\text{mW} \\ P_{loss,total} &= P_{switch} + P_{con} + P_{I_{rip}} = 0.3 + 0.49 + 0.012 = 802\,\text{mW} \end{aligned} \tag{5.1}$$

Giving a theoretical efficiency (without including current and voltage loop power usage) of:

$$\eta = (1 - \frac{P_{loss,total}}{P_{out}}) \cdot 100$$
$$\eta = (1 - \frac{0.802}{12.5}) \cdot 100 \approx 93\,\%$$

This number will eventually end up lower as there are also reverse recovery charge losses, cross conduction losses and drain charge losses not taken into account.

Output Capacitors

The output capacitance needs to be 1 µF. It is a bad idea to just have one capacitor as output capacitor due to the following reasons: capacitance de-rating due to voltage bias, current handling capabilities and equivalent series resistance.

Ceramic capacitors suffer from reduced capacitance when the bias voltage across the device is increased. To mitigate this effect smaller valued capacitors can be chosen, as the effect is reduced for smaller capacitance values. The package size can be increased or a different dielectric can be selected.

For this design 5 1206 sized 100 V rated capacitors are chosen with a capacitance of 220 nF each, to have a total capacitance of about 1 µF if the voltage de-rating is also taken into account.

Final schematic of the power stage

The components discussed above are added to the design next to some additional features. The design and additional features can be found in figure 5.2.

There is a provision for a snubber circuit to reduce transients. Gate source voltage rise time limiting for the MOSFETs is possible, and a switch has been added to allow driving the power stage with a fixed duty-cycle generated by the microcontroller which is useful for testing or starting up the converter.

A current shunt is added into the power path for current sensing, this will be discussed in the next section.

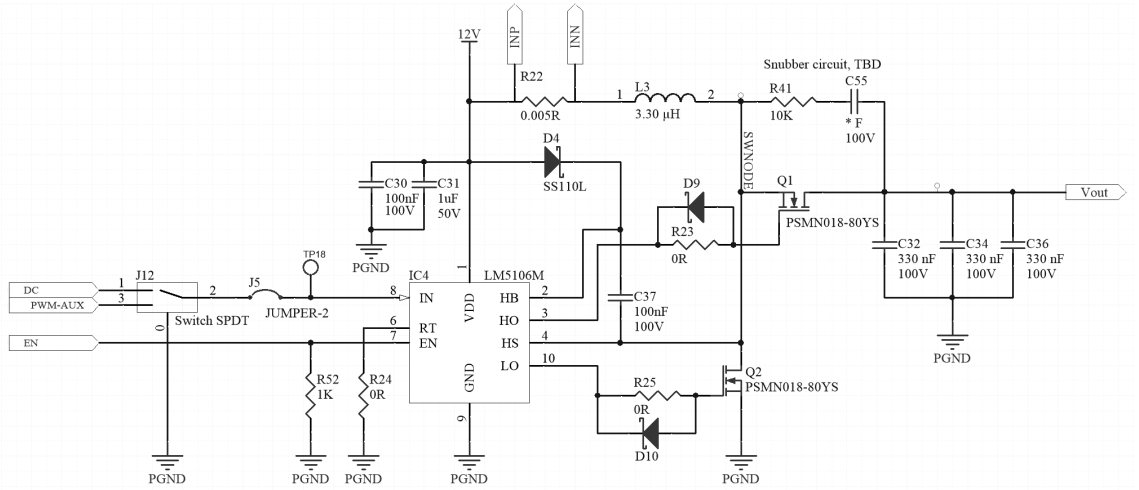

Figure 5.2: Final design for the power stage.

Current loop

The current loop will be made with discrete components. There are a few devices that need to be chosen: a current sense chip, compensator op-amp, duty cycle generation comparator and active elements for the ramp generation. The supply voltage for each component in the current loop is 5 V.

Current sense

Bi-directional current sensing is needed for current sensing in the supply line of output stage. The current shunt which will convert current to voltage is shown in figure 5.2.

For the current sense the following list of requirements is made:

- Bi-directional current sense
- Common mode voltage rating of at least 12 V
- Internal gain to convert differential shunt voltage to single ended output voltage
- Small signal bandwidth of 5 MHz to not distort current ramp
- Low noise and high accuracy

Using these requirements the AD8210[36] is selected as current sense IC. The current sense voltage output can be biased at half the supply for bi-directional operation, 2.5 V will then be the zero current level. The IC has a common mode input range from -2 V to 65 V at a supply voltage of 5 V. The differential shunt voltage to single ended output voltage gain is 20 x.

The small signal bandwidth is 450 kHz, this is a lot less then the required 5 MHz. This can however be used in an advantageous way as $f_s/2$ pole, the $f_s/2$ pole in the current compensator can then be left out.

The 5 mΩ current shunt combined with the gain of 20 gives the required current sense gain of 0.1.

Compensator

The compensator is integral to the average current mode control scheme. The device should have high DC-gain as this determines the precision of the average current mode action.

For the current compensator the following list of requirements is made:

- High DC-gain
- Gain-bandwidth of at least 10 MHz as the current ramp is 1 MHz
- Common mode input range of 2 V to 4 V

- Output range of 2 V to 4 V
- Single supply voltage of 5 V

For the current compensator a rail-to-rail output, high GBW op-amp is selected: LMH6639[37]. Which has a 100 dB DC-gain, a 0 V to 4 V common mode input range, a gain-bandwidth of 190 MHz and a rail-to-rail output stage. The op-amp works at a single ended supply of 5 V.

Duty-cycle generation

The signals from the compensator structure and the PWM triangle generator are combined to generate the duty cycle. This is done with a comparator. For this sub-circuit propagation delay is of importance because all delay inserted into the loop will reduce the phase margin of the current loop. Another requirement is fast rise time, which will be guaranteed if a low propagation delay comparator is selected.

For the comparator the Texas Instruments LMV7219[38] is selected. This device has a propagation delay of 7 ns, resulting in an extra phase shift of:

$$P_{prop} = \frac{7}{1000} \cdot 360^\circ = 2.3^\circ$$

Not very significant so perfect for this application.

PWM triangle Generator

A triangle oscillator is integrated on the board for generating the PWM-ramp. Using the calculations from [39, p A-44] a 1 MHz oscillator can be created using a high-speed op-amp and high-speed comparator. The op-amp should have a high gain-bandwidth and have a slew rate bigger than $10\,\mathrm{V\,\mu s^{-1}}$.

The same op-amp and comparator as from the current loop are used as they satisfy the requirements as the op-amp has a full-power bandwidth of 28 MHz and a rail-to-rail output stage.

The theoretical schematic of the triangle wave generator is shown in figure 5.3.

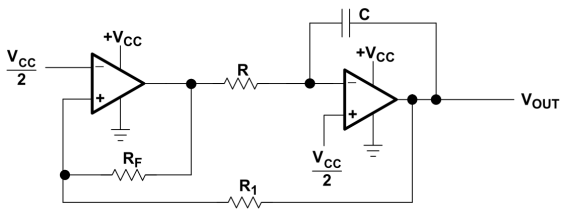

Figure 5.3: Triangle wave oscillator, the frequency and amplitude can be set by the feedback components[39].

The oscillator can be configured using the following equations, also taking into account the minimum and maximum op-amp output voltages:

$$V_{ramp} = \frac{V_{CC}}{2} \pm \frac{V_{CC}R_1}{2R_F} = \frac{5}{2} \pm \frac{5R_1}{2R_F}$$

$$f_{osc} = \frac{1}{4CR}\left(\frac{R_F}{R_1}\right)$$

The target frequency is 1 MHz and the ramp voltage should close to the 5 V supply rails. Using resistors from the standard E24 range 15 kΩ and 16 kΩ come very close to the required ramp voltage:

$$V_{ramp} = \frac{5}{2} \pm \frac{5R_1}{2R_F} = \frac{5}{2} \pm \frac{5 \cdot 15\text{e}3}{2 \cdot 16\text{e}3} = 2.5 \pm 2.35 = 0.15\,\mathrm{V} - 4.85\,\mathrm{V}$$

Using the same 16 kΩ for resistor R the capacitor value can be calculated:

$$C = \frac{R_F}{4 f_{osc} R R_1} = \frac{16e3}{4 \cdot 1e6 \cdot 16e3 \cdot 15e3} = 16.6\,\text{pF}$$

LT-Spice simulation and measurements showed that feedback resistor R_F was a bit to large and would saturate the output stage of the integrator. Changing the resistor to 13 kΩ gives a triangle with an amplitude which fits in the output voltage range of the integrator op-amp.

To keep oscillating at the correct frequency the capacitor size needs to be increased to 20 pF.

$V_{ref}/2$ is made on board with a resistive divider and filter capacitor to increase the power supply rejection.

Final schematic of the current loop

The components discussed above are added to the design next to some additional features. These additional features can be found in figure 5.4.

There is a provision with R58 and R56 to add extra hysteresis to the comparators if the need arises. Test points are added so every important signal in the current loop can be easily measured with the oscilloscope.

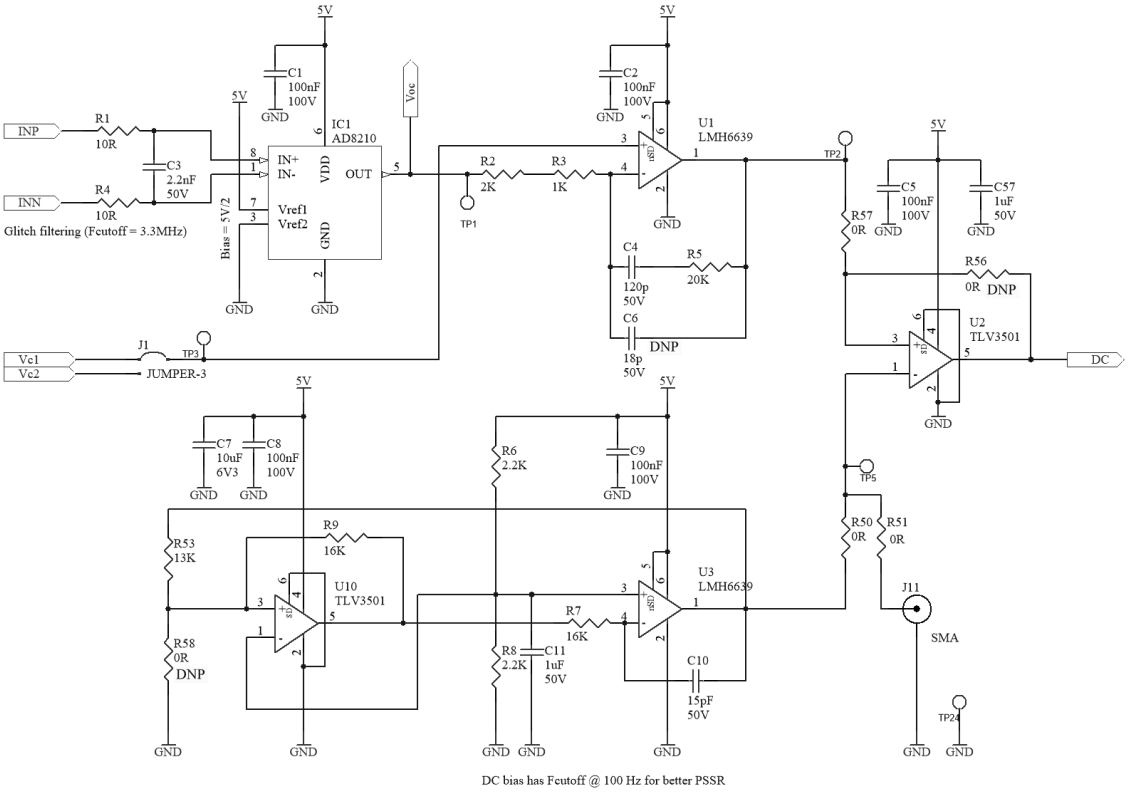

Figure 5.4: Final design for the current loop.

Pre-distorter

As derived in chapter 4 the pre-distorter needs to implement a second order polynomial with a linear term and a quadratic term. This requires a chip capable of multiplication. In the analog domain this can be realised using a trans-linear circuit.

The polynomial that needs to be implemented is shown in equation 4.4 and repeated here, the half supply bias of the current loop should also be added:

$$V_{pd,out} = \frac{R_s}{\gamma^2 R_L V_g}(V_{pd,in})^2 - \frac{R_s V_{bias}}{\gamma R_L V_g} V_{pd,in} + \frac{V_{supply,current-sense}}{2}$$

This results in the following V_c to $V_{cp,pd}$ and V_c to V_{out} transfer curve:

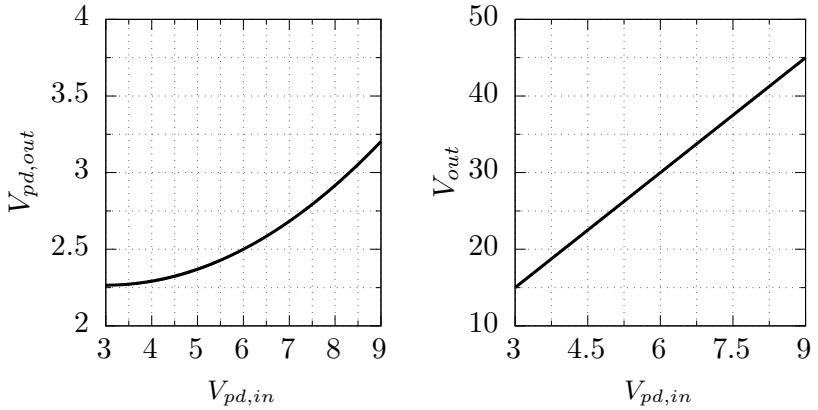

Figure 5.5: The voltage-loop output to control-voltage is shown, including the current loop's 2.5 V zero current bias level. The voltage loop out to converter output voltage is shown in the right figure.

As can be seen in figure 5.5 the voltage loop output is biased at 6 V or half the 12 V supply of the voltage loop. The pre-distorter converts the 6 V bias level to the zero current bias level of 2.5 V.

Again a list of requirements for the multiplier can then be made which are partly based on the voltages ranges shown in figure 5.5:

- Multiplication inputs
- Linear term input
- Small signal bandwidth which is larger than the voltage loop bandwidth (20 kHz)
- Minimum multiplier input voltage range of 3 V to 9 V
- Output voltage range of 2 V to 4 V
- High accuracy and low multiplication error

Unfortunately there is a limited amount of analog multipliers available, the AD633[40] is selected to perform the pre-distortion action. It fits the requirements with one exception, the input voltage range is limited to 8.5 V with a 12 V supply after which performance decreases. A maximum output voltage amplitude of 12.5 V will be in the full performance range of the pre-distorter.

Another downside is the requirement for dual supply operation. This means that a -12 V supply is also needed. As this is a prototype dual supply operation is not a problem. However when it is used in a final product an alternative solution needs to be found. Dual supply operation is very unpractical when working from battery power.

The functional schematic of the AD633 is shown in figure 5.6. The multiplier has a large signal transfer function defined as:

$$V_{out} = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z$$

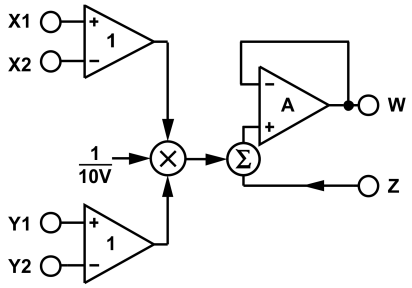

Figure 5.6: The functional block diagram of the AD633 multiplier chip[40].

Equation 4.4 needs to be mapped on the transfer function shown above:

$$\begin{aligned} V_{out} &= \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z, X_1 = Y_1, X_2 = Y_2 = 0 \\ &= \frac{(X_1)^2}{10} + Z \end{aligned}$$

The coefficients need to be transformed to make equation 4.4 fit, the half supply current sense bias should also be added to the Z-input:

$$\begin{aligned} Z &= -\frac{R_s V_{bias}}{\gamma R_L V_g} V_{pd,in} + V_{cs,bias} \\ &= -\frac{R_s V_{bias}}{\gamma R_L V_g} V_{pd,in} + \frac{V_{supply,cs}}{2} \\ X_1 &= \sqrt{10 \frac{R_s}{\gamma^2 R_L V_g}} (V_{pd,in}) \end{aligned}$$

This results in:

$$V_{out} = \frac{(\sqrt{10 \frac{R_s}{\gamma^2 R_L V_g}} (V_{pd,in}))^2}{10} + \frac{R_s V_{bias}}{\gamma R_L V_g} V_{pd,in} + \frac{V_{supply,cs}}{2} \tag{5.2}$$

Final schematic of the pre-distorter

Using the equations above the polynomial can be implemented in hardware (see figure 5.7). For the Z-input an inverting summation amplifier is used to make the first part of Z negative. A negative 2.5 V is added to set the correct current bias level.

The quadratic input is made directly form the input voltage as this is a positive value. Filling in the circuit parameters and the input voltage ratios can be calculated:

$$\begin{aligned} Z &= -\frac{0.1 \cdot 30}{0.2 \cdot 8 \cdot 12} V_{pd,in} + 2.5 \\ X_1 &= \sqrt{10 \frac{0.1}{0.2^2 \cdot 8 \cdot 12}} (V_{pd,in}) \end{aligned}$$

These ratios can be set using the trimmer potentiometers shown in figure 5.7 and need to be calibrated before the first use of the board. Again different test points are added which help in calibrating the pre-distorter and give easy access to the relevant signals.

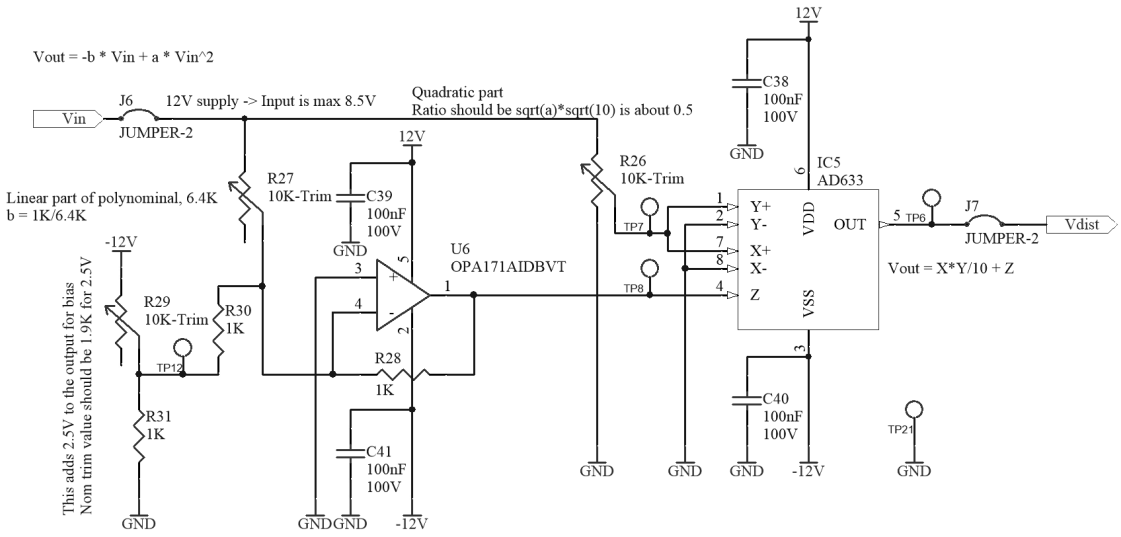

Figure 5.7: Final analog implementation of the pre-distorter. The bias and polynomial coefficients can be set by the potentiometers.

Voltage loop

The final analog part of the design implementation is the voltage loop compensator. This part has less strict design requirements as the speed of the voltage loop is slow compared to the current loop.

The reference voltage is biassed at 3 V to make a 30 V output bias. As mentioned in the specifications the line-input signal has a swing of $\pm$ 1.5 V_{pp} setting the common mode input range. Optionally the line-input signal can be amplified by a pre-amplifier.

The same PI-compensator structure as in the current loop is used and therefore the same kind of op-amp requirements are needed:

- High DC-gain as this determines the low frequency performance
- Gain-bandwidth of at least 200 kHz, 10 times the loop cross-over
- Common mode input range of 1.5 V to 4.5 V
- Output range of 3 V to 9 V as the pre-distorter input voltage bias is set at 6 V

A supply voltage of 12 V is used for the voltage loop components. A general purpose OPAMP is selected: the rail-to-rail output TI OPAx171[41]. It comes in dual OPAMP package so the same device can be used for the pre-amplifier. It has a DC gain of 130 dB and a common mode input rage of 0 V to 10 V at a 12 V single supply.

Final schematic of the voltage loop

The final implementation is shown in figure 5.8. The feedback is implemented as a resistive divider with 10 times division ratio. The input signal is coupled in with a DC-blocking capacitor, the high-pass input filter has a cut-off of 10 Hz.

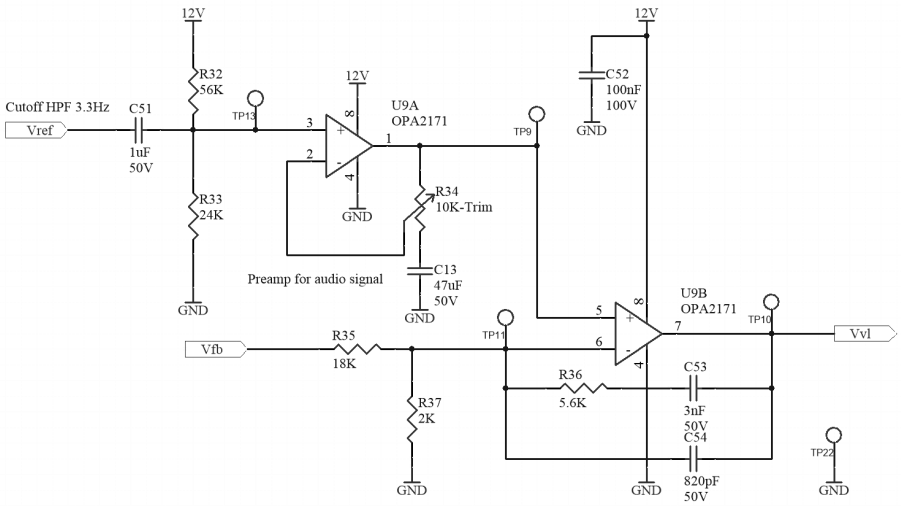

Figure 5.8: Final design for the voltage loop.

Microcontroller

A powerful ARM cortex-M3 microcontroller(ATSAM3S1BB[42]) is added to the design. In its basis it needs to do be able to turn on the power stage at the push of a button and monitor the inductor current and output voltage. If the inductor current or output voltage become too high the microcontroller will turn of the power stage to protect the components. Optionally the microcontroller can also be used to implement the voltage controller + pre-distorter in the digital domain using its 12-bit DA and AD-converters.

Over-current protection is done by feeding the current sense signal to an analog comparator. The comparator compares a reference voltage made by the DAC to the actual current sense value. The output voltage is monitored by applying it to an ADC so the software can take action if the voltage becomes to high. This method is fine for a prototype. In a production device however protection should be done in hardware. This prevents a software bug from physically destroying the power stage.

The microcontroller has a 3.3 V power supply voltage. The input range of the ADC and output voltage range of the DAC are also 3.3 V. To be able to measure the output voltage of the converter it needs to be scaled down to a maximum of 3.3 V. A divider ratio of 19 x is chosen to be able to measure up to about 63 V. This is a bit higher than the specified maximum design voltage of 60 V. A buffer is added after the feedback resistors as the AD-converter has low impedance at a conversion speed of $1\,\mathrm{MS\,s^{-1}}$.

A button is added to switch the power stage on and off and status indicator leds are put on the board. A fixed duty cycle PWM signal is also generated by the controller, the PWM signal can be applied to the power stage for diagnostic purposes and to start up the board by charging the output decoupling capacitor to the 30 V bias voltage.

As an optional feature a second DAC channel is routed to the current loop input, this gives the possibility to implement the pre-distorter and voltage loop in the digital domain. This is not in the scope of this research but it can be used in future work (see section 6.1).

USB is added which gives the possibility to stream digital audio to the board or create a serial port used for debugging.

Software

Software is written for the functions specified above. All the protections are interrupt based, where the interrupt trigger events. The different events that are possible are show in figure 5.9.

The following voltage and current limits are chosen:

$$I_{max} = 20\,\mathrm{A}$$
$$V_{max} = 60\,\mathrm{V}$$

Over-current protection is done by generating a voltage with the integrated 12-bit DAC and comparing it to the instantaneous current sense value. The sensed current voltage is divided by two using a voltage divider in hardware. The DAC voltage is then calculated by and is converted to a binary value:

$$\begin{aligned} V_{DAC} &= \frac{V_{cb} + I_{max} R_s}{2} \\ &= \frac{2.5 + I_{max} \cdot 0.1}{2} \\ B_{DAC} &= \frac{V_{DAC} \cdot 2^{12}}{3.3} = \frac{(2.5 + I_{max} \cdot 0.1) \cdot 2^{12}}{2 \cdot 3.3} \end{aligned}$$

The comparator generates an interrupt when an over-current conditions is detected, resulting in a near instantaneous turn off of the gate driver.

Over-voltage protection is done by continuously running the ADC and checking if the ADC voltage is over the specified value (see below), this is all done in the ADC hardware. An ADC interrupt is generated when over-voltage is detected. The ADC trigger level is determined by:

$$V_{trig} = \frac{V_{max}}{ADC_\beta} = \frac{V_{max}}{19}$$
$$B_{trig} = \frac{V_{trig} \cdot 2^{12}}{3.3}$$

The pipelined ADC runs at $1\,\mathrm{MS\,s^{-1}}$ with a 12 cycle conversion delay. This means that the system can be shut off in approximately $12\,\mu\mathrm{s}$.

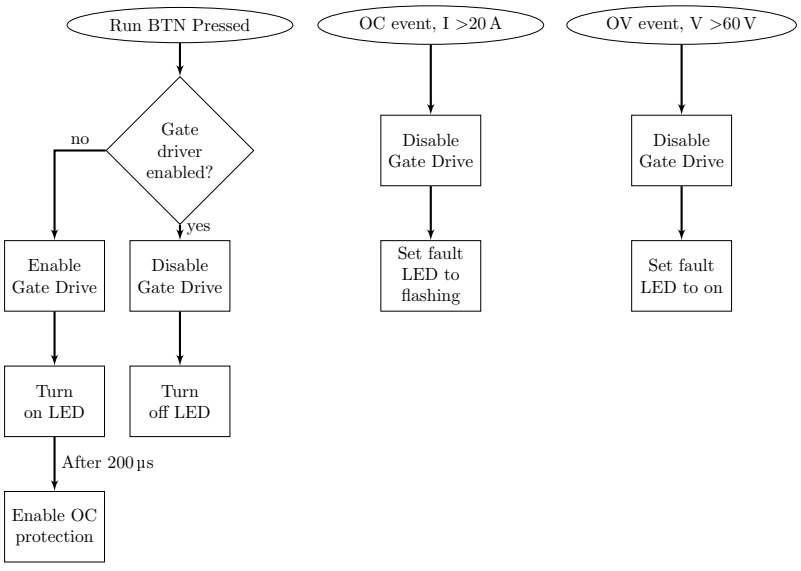

Figure 5.9: The different events are shown in this graph. All functionality is interrupt based and the actions that are taken are depicted here.

Final schematic of the controller

The final implementation is shown in figure 5.10. Here the different buffers can be seen, the status leds, the button and feedback structures. A JTAG-header is added to the design to be able to program the controller.

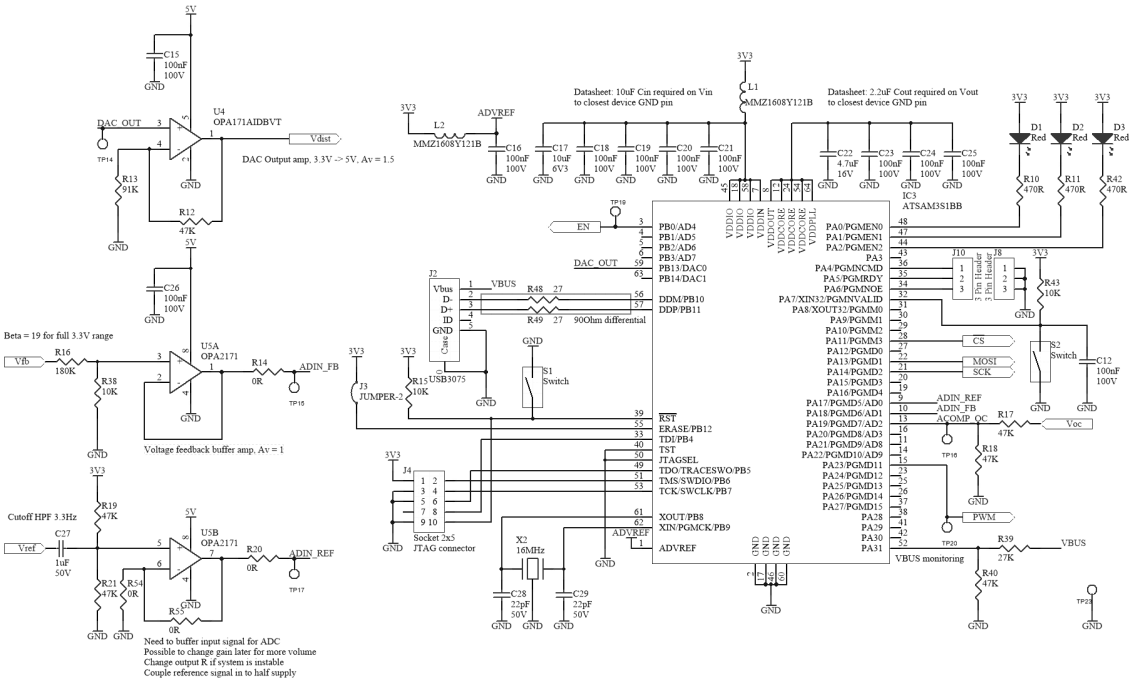

Figure 5.10: Final design for the microcontroller subsystem. The different buffers and auxiliary components can be seen here.

Supplies

Different subsystems require different supply voltages. The whole current loop works at a supply voltage of 5 V as this is the maximum allowed by the selected components. The voltage loop has a single supply of 12 V, the pre-distorter works at ± 12 V. Finally the microcontroller runs at a supply voltage of 3.3 V.

An external power supply will supply the 12 V system voltage and the −12 V for the pre-distorter. Two 1% linear voltage regulator are used to create a 3.3 V and 5 V supply from the 12 V system voltage. These also help in creating stable supplies and rejecting 12 V supply ripple.

All voltages are connected to LED indicators to show the supplies are active. Low impedance ceramic capacitors are added to the system voltages. The final components for the supply section of the prototype is shown in figure 5.11.

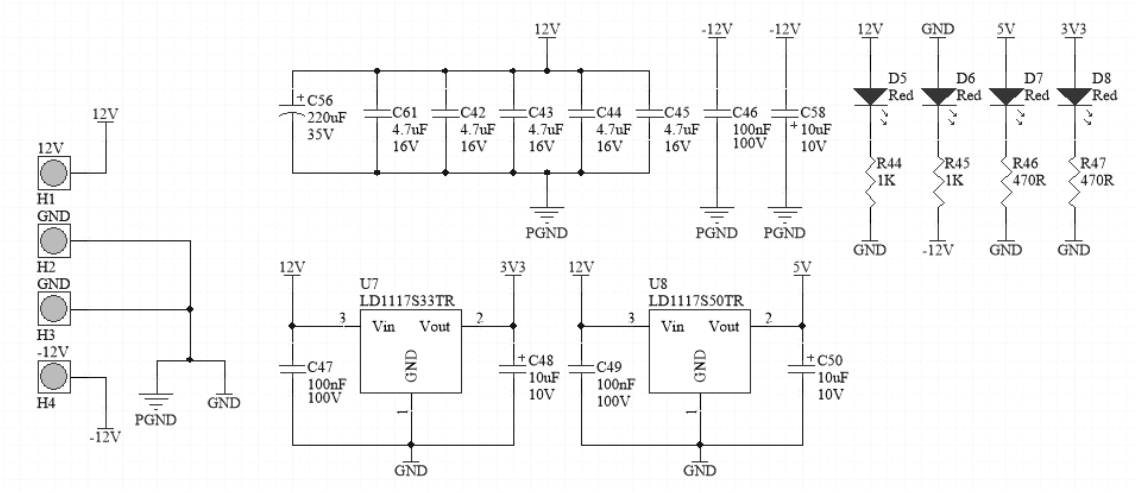

Figure 5.11: Power supply for the prototype. All supply voltages are decoupled and LED indicator lights are added to show the supplies are active.

5.2 PCB Design

After schematic entry all components are placed on the PCB. Care should be taken as there are high currents and voltages involved in the design.

A 4-layer PCB is used, signal traces are on the top layer, the second layer is full ground. A third layer is used as power layer with power-planes at different voltages. The bottom layer is used for crossing signal traces on layer one, but is mostly connected to ground. The usage of power and ground planes prevents potential IR drop when big currents are flowing. A nearby ground plane also prevents crosstalk between signal traces, this is necessary as the 1 MHz duty cycle signal has fast rise times and is close to sensitive parts of the system.

A 3D-render of the prototype is shown in figure 5.12. The high current high voltage part of the circuit is kept as separate as possible from the rest of the circuit, this can be seen in the left part of the PCB. The high current path can easily be seen by the thick traces and is kept short. The current direction stays the same between switching stages, which reduces EMI.

Furthermore the recommended PCB-layout, as given in the datasheet of the different components, is used as much as possible.

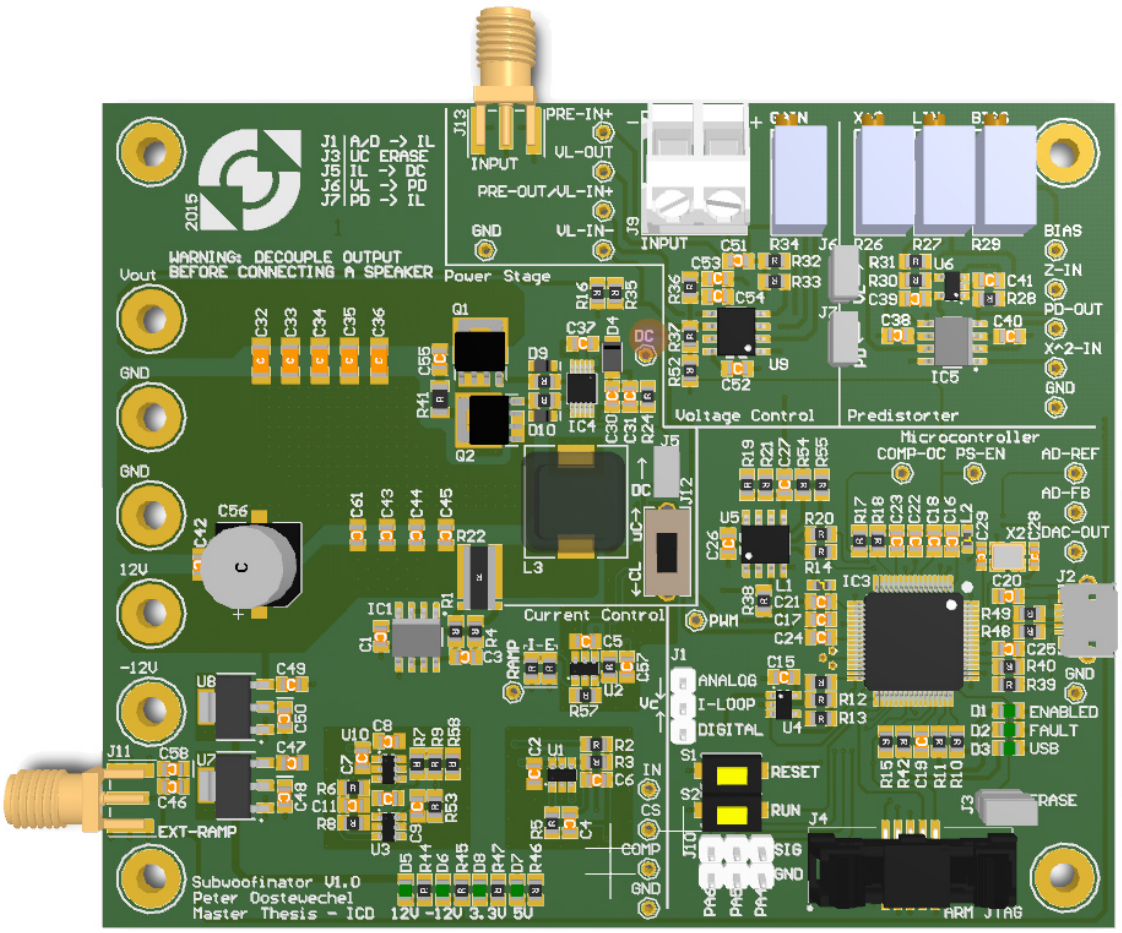

Figure 5.12: 3D-rendering of the PCB-prototype. The power stage and supply connections are at the left side of the PCB. The control hardware is laid around that section.

The PCB is designed with flexibility in mind as this is a prototype implementation, a lot of options are possible if a problem is encountered.

For instance the circuit is split into different sections corresponding with the general structure shown at the beginning of this chapter (figure 5.1). The inputs and outputs of each section can be connected by jumpers so each section can be tested individually. This also gives the possibility to skip the pre-distorter to do comparative measurements.

An option is added to connect an external PWM-ramp generator. The input signal can be connected either via SMA or the terminal block shown at the top.

5.3 Measurements & Discussion

Hardware and software are now designed and fabricated. A prototype is created and measured, the results can then be compared to simulation and discussed.

First the measurement devices and measurement set-up is shown, so it is clear how results are obtained. Patches to the circuit are listed to fix errors that are overlooked in the design phase. Next critical signals of each sub-system are shown and large signal measurements, small signal measurements and THD figures are given.

Finally the results are discussed and possible explanations for derivations from simulation are given, improvements and points for attention are suggested.

Improvements and changes after prototype creation

After soldering and preliminary testing of the board some changes are needed to finalize the board. After these changes the prototype is ready for the final measurements.

The first issue encountered is the needed inversion of the duty cycle signal. A logic high at the gate driver turns on the top switch, while duty cycle is defined as the time the bottom switch is on. An inverter is placed between the duty cycle output of the current control loop and the duty cycle input of the gate driver, solving the problem.

A second problem lies in the power supply, if the output voltage of the converter needs to decrease the supply needs to sink current from the bias capacitor. As all power supplies available are single quadrant supplies, these can only source current. This results in a big supply ripple and the supply going out of regulation. To solve this issue a bank of decoupling capacitors is inserted in the 12 V supply rail. These capacitors can absorb the excess charge stabilizing the 12 V supply rail.

Summarizing:

- Insert inverter between current loop and gate driver
- Add supply decoupling to prevent power supply ripple and supplies going out of regulation

Measurement Setup

Different kind of instruments are used for measurements and calibration. For large signal measurements the oscilloscope is used, for calibrating the pre-distorter and other general measurements the 6-digit multimeter is employed. THD measurements are done with the Rohde & Schwarz UPL Audio Analyzer, intended for these kind of measurements.

Table 5.1: Different devices are used in the set-up and are listed below. The most important one is the audio analyzer used for measuring THD.

Device	**Type**
Oscilloscope	Agilent DSO-X 3024A
Audio Analyzer	Rohde & Schwarz UPL Audio Analyzer
Power Supply	Rohde & Schwarz HMP4040
Arbitrary Waveform Generator	BK Precision 4065 2-channel AWG
Multimeter	Agilent 34401A

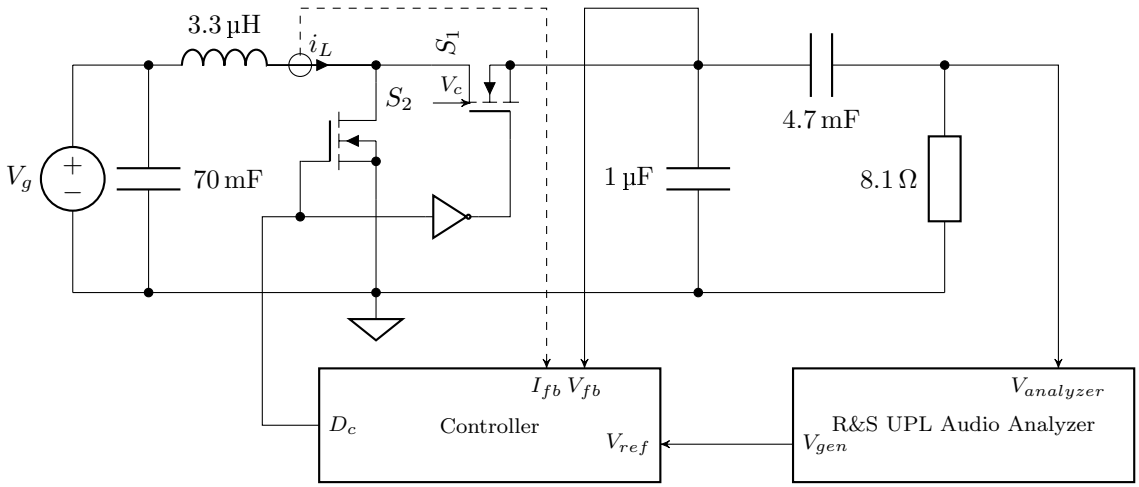

Figure 5.13: Measurement setup for THD and transfer function measurements. The supply is decoupled as explained in the previous section. The load is decoupled from the converter with a large capacitor ($f_0 = 4.2\,\text{Hz}$).

The measurement setup for THD and transfer function measurements is shown in figure 5.13. The supply is decoupled as explained in the previous section and the load is decoupled from the

converter with a large DC blocking capacitor. This high pass filter has a cut-off frequency of $f_0 = 4.2\,\text{Hz}$.

Power Stage

The power stage is first measured and verified as the behaviour of this sub-circuit needs to be correct before the control loop can be turned on. This is done by applying the fixed PWM-signal made by the microcontroller to the power stage.

Gate Driver

The gate-driver plus MOSFET combination is measured to investigate the dead-times, switching waveforms, ground bounce and ringing. Figure 5.14 shows the power stage input duty cycle and V_{gs} voltages of both the switches.

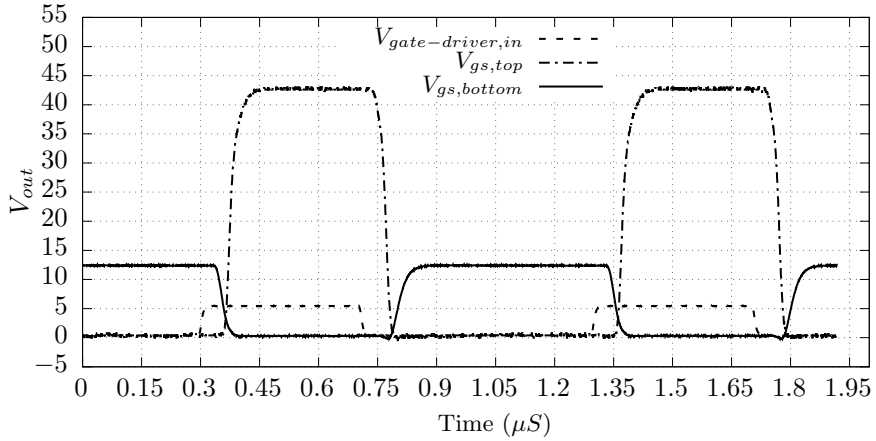

Figure 5.14: This graph shows the switching waveforms and dead-time generated by the gate driver at an output voltage of 30 volt (Dc = 60%). It can be seen that the switching waveforms are very clean, there is no ringing present and barely any ground bounce.

The bootstrap action of the top switch is clearly visible as the output voltage of the converter is 30 V. Both gates are driven with an overdrive voltage of about 12 V. No ringing is present so the optional snubber circuit is not needed.

Using figure 5.14 the dead-times in the gate driver can be deducted. These are shown in table 5.1. These dead-time values can be used in simulations including parasitics.

Table 5.2: Measured dead-time in the gate-driver.

Transition	**Top Switch**	**Bottom Switch**
$D_{c,L\to H}$	126 ns	56 ns
$D_{c,H\to L}$	84 ns	122 ns

Current Loop

An important part of the current loop is the duty cycle generation. This means that the comparator and PWM-generator need to be working as intended. First the PWM-generator is measured and measuring continues with the comparator.

PWM Generator

The PWM-generator is measured for linearity and frequency. The generated triangle is shown in figure 5.15. A linear ramp is required is from 1 V to 3.7 V, corresponding with a converter output voltage of 15 V to 45 V. This is the case as can be seen in the figure.

The frequency of the signal is measured as 1.06 MHz which is close to the wanted 1 MHz, the deviation can be explained by component spread and parasitic elements.

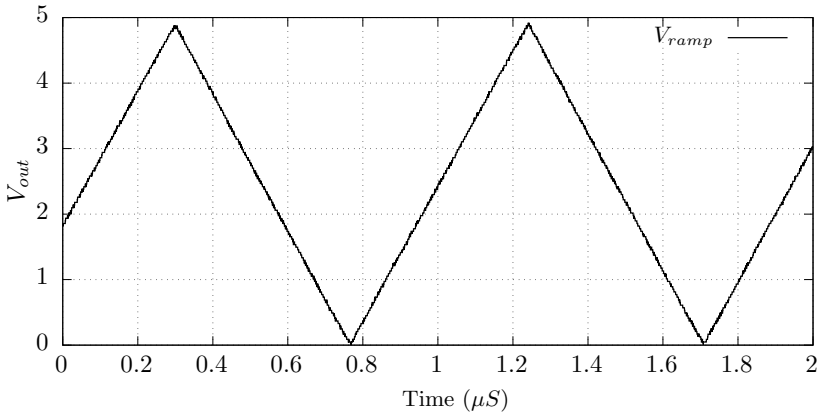

Figure 5.15: This graph shows the on-board generated ramp. The linearity is good over the whole working range of 1 V to 3.7 V.

The THD of the whole converter is also compared with an external ramp provided by the BK-Precision 4065, it has a linearity of less than 0.1% deviation full scale[43]. No measurable difference in distortion is found so the internal ramp generation is at least as good as the arbitrary waveform generator.

Comparator

The comparator works as intended with a measured propagation delay of 8 ns. This is a bit more than the specified typical 7 ns delay in the datasheet, however this discrepancy has a negligible effect on the performance of the circuit.

Pre-Distorter

The pre-distorter needs to be calibrated as mentioned in the implementation section of this chapter. Using the trim-potentiometers and equation 5.2 the correct coefficients for $V_{pd,in}$ and $V_{pd,in}^2$ can be set:

Measured values for $V_{current,bias} = 2.5011\,\text{V}$, $R_L = 8.11\,\Omega$ and $V_{bias} = 30.467\,\text{V}$ are used:

$$Z = -\frac{0.1 \cdot 30.467}{0.2 \cdot 8.11 \cdot 12} V_{pd,in} + 2.5011 = -0.157 \cdot V_{pd,in} + 2.5011$$

$$X_1 = \sqrt{10 \frac{0.1}{0.2^2 \cdot 8.11 \cdot 12}} (V_{pd,in}) = 0.507 \cdot V_{pd,in}$$

The pre-distorter can be disconnected from the rest of the circuit to set the correct X and Z values. An arbitrary $V_{pd,in}$ between 3 V to 9 V can be applied at the input terminal, the X and Z input terminals can then be measured. Using the trim-potentiometers the correct values can be set.

In hindsight the current implementation of the pre-distorter with static settings is not the best way to implement it, as the settings are very component and circuit dependent. A small offset or drift in the bias level or current sense gain for example will quickly reduce the pre-distorter performance, which can also be seen in the next section.

A better way to implement the pre-distorter coefficients would be to use feed-forward techniques to set the correct scaling values however this can only be partially done if the system is running, so ways to do that should be investigated.

In a real application battery voltage can vary between 12 V to 14.5 V. Supply voltage should be fed forward to the pre-distorter.

Another issue observed is the reversal of the loop gain if the output signal swings close to or below −15 V, corresponding with a converter output of 15 V. At this voltage the amplifier latches up for half an input sine period. This can be explained by looking at figure 3.7 where the pre-distorter gain reverses if the pre-distorter input voltage drops below the 3 V.

Voltage loop

Large signal measurements are done to verify the large signal behaviour of the system, the small signal transfer functions are measured afterwards to verify the bandwidth of the amplifier.

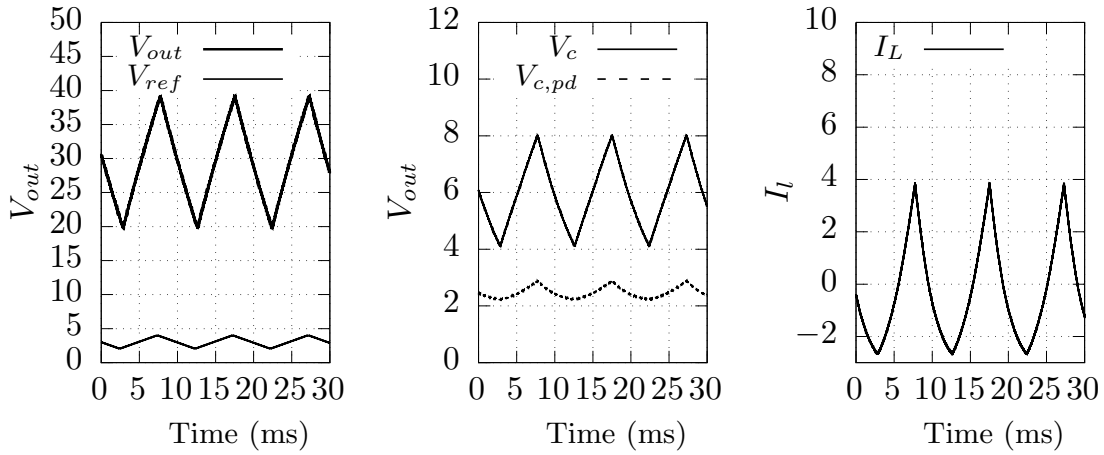

Figure 5.16: A 100 Hz triangle wave is applied to the reference input of the voltage loop and the different signals are measured on the amplifier board. In this figure the pre-distorter action can clearly be seen in the second graph, the control voltage is pre-distorted and the voltage loop output V_c shows little corrective action indicating the pre-distorter works as intended.

A 100 Hz triangle is applied to the amplifier and relevant signals are measured to verify large signal behaviour. The results of these measurements are low pass filtered before shown in figure 5.16. This figure shows that the pre-distortion works as intended as the output of the voltage loop shows little corrective action for the current loop, indicating a linear control to output voltage transfer of the current loop. It is however not perfect as there is a small non-linearity in the downward slope of the V_c signal.

It was found that even a small offset in the bias level added to the Z-input of the pre-distorter has a large influence on the linearity of the V_c slopes and thus the linearity of the converter. This again shows that the current implementation of the pre-distorter is sub-optimal.

Small Signal

The closed loop transfer of the voltage loop is measured to investigate the closed loop reference to output voltage transfer function of the prototype converter. The UPL analyzer can only measure the gain of the transfer function when using the 110 kHz analyzer so the phase is excluded from the bode plots.

The transfer function is measured with a 1 V amplitude sine wave. Figure 5.17 and 5.18 show the resulting transfer functions.

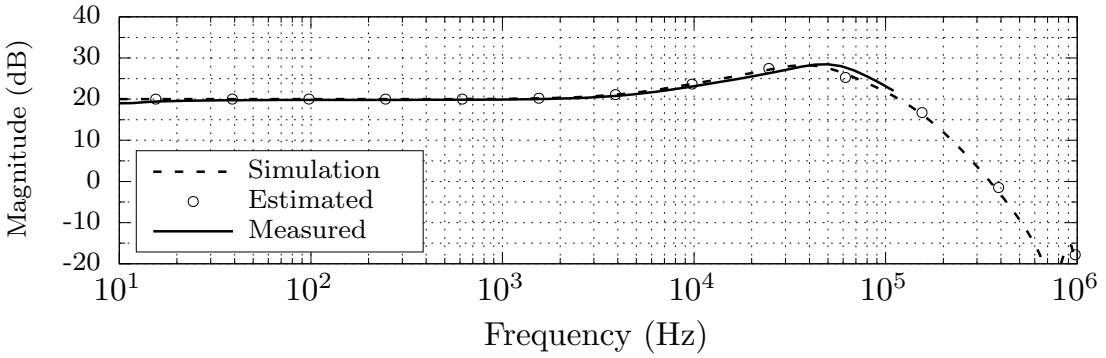

Figure 5.17: **Vout/Vref** The closed loop transfer without pre-distorter measured at an output voltage of 30 V. As can be seen the measured, simulated and estimated analytical transfers (equation 4.5) match.

As predicted by the analytical closed loop expression and simulations the non-pre-distorted converter has a gain peak at about 50 kHz. This is the result of the interaction between feedback network of the voltage loop and the feedback impedance around the voltage compensator.

It should be investigated if this can be resolved by changing/scaling the feedback network components while keeping the same compensator behaviour. Another solution is to apply equalization before the input terminal to attenuate the gain boost, this can be done with a simple RC low-pass filter network for example.

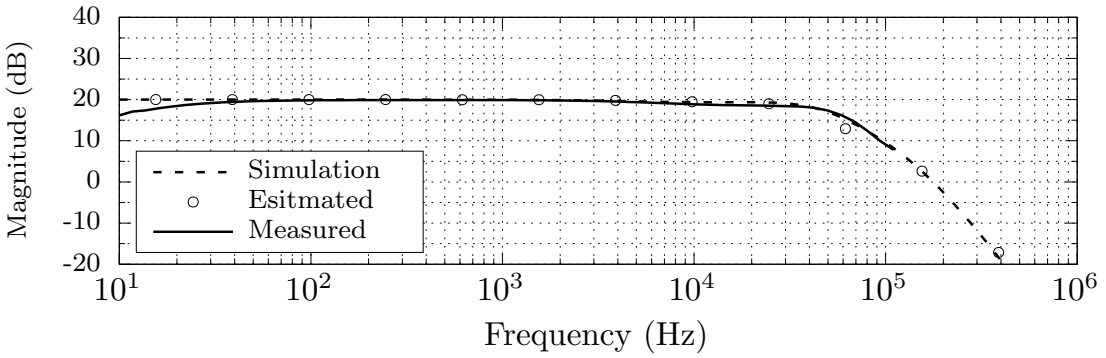

Figure 5.18: **Vout/Vref** The closed loop transfer with pre-distorter measured at an output voltage of 30 V. As can be seen the measured, simulated and estimated analytical transfers (equation 4.5) match.

With pre-distorter the transfer curve is almost flat with a -3 dB bandwidth of 50 kHz, which is more than the required 20 kHz. Both converters have a low frequency -3 dB cut-off of at least 20 Hz.

Efficiency measurements

Optimal efficiency is not the focus of this thesis, however some efficiency measurements have been done to get an indication of the efficiency of the converter.

The baseline power consumption of the prototype without a running power stage is 2.4 W, this includes the microcontroller, ramp generator, idle currents in the voltage loop, pre-distorter and current loop and 7 status leds.

When the power stage is switched on the power consumption increases by 0.6 W with no DC output current. This is partly dissipated in the gate-driver as gate loss and as ripple loss in the inductor.

This is a factor two higher than calculated in equation 5.1. It is suspected that there is additional switching loss due to reverse recovery charge and capacitance at the switching node.

As calculated before gate loss is a large part of the power consumption in the power stage, this is the result of the selected low $R_{ds,on}$ MOSFETs which have large gate capacitance. In further designs a better trade-off should be made between switching loss and conduction loss in the MOSFETS.

THD measurements

Finally the THD measurements can be done, these measurement can then be compared to the simulated THD results in chapter 4. Different types of measurements are done, the THD versus power is plotted at a frequency of 1 kHz and the THD versus frequency is plotted at an output voltage of 10 V.

These measurements are compared to simulation and discrepancies are discussed.

Measurement Automation

The measurements are automated using Matlab with the GPIB control port available on the UPL Audio Analyzer. This will simplify measurements, speed up the process and reduce errors.

The UPL audio analyzer is configured as shown in table 5.3.

Table 5.3: Configuration for the UPL Audio Analyzer when performing THD measurements

Generator		*Analyzer*		*Measurement*	
Output type	Balanced	Input type	Balanced	Type	THD
Output impedance	10 Ω	Input impedance	200 kΩ	Mode	Precision
Output function	Sine	Bandwidth	110 kHz	Harmonics	D1-D4
Low distortion	On	Coupling	AC coupled	Unit	Percent
Voltage limit	1.2 V	Voltage range	Auto		

Using the measurements results from figure 5.17 and figure 5.18 the generator output voltage is equalized. This is done to have the same output voltage for each frequency and therefore a fair THD measurement. Otherwise the gain peaking at higher frequencies occurring in the non-pre-distorted converter would skew measurement results.

Two types of measurements are done by the script, THD versus frequency and THD versus power. The automated frequency sweep uses an output voltage of 10 V and 20 frequency points. THD vs Power measures the THD at an output frequency of 1 kHz, which is the norm in the audio field. 50 measurements are done ranging from 0.01 W to 20 W. All measurements are averaged over 8 measurement points.

Results

The measurement results are shown in this section. The THD versus frequency is shown in figure 5.19. The simulated THD without pre-distorter closely matches the measurement results.

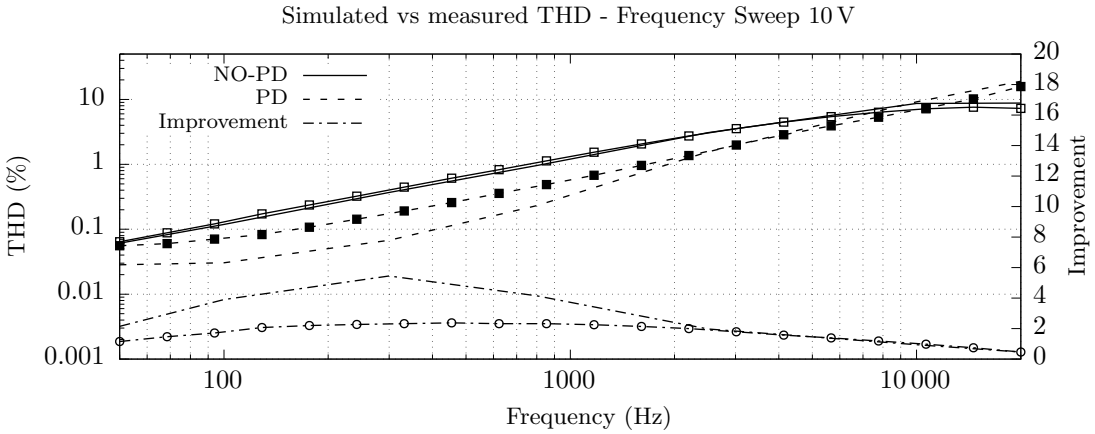

Figure 5.19: In this graph the closed voltage loop distortion measurements (marked lines) over frequency are compared to the simulation results for an output voltage of 10 V. The simulation include the parasitic elements, which are also present in the prototype implementation.

The THD measured with pre-distorter is off in the low frequency region. The improvement with pre-distorter has reduced from a maximum of 6 to about 2.5. A possible explanation for this reduction in effectiveness has already been mentioned in the pre-distorter section above. The pre-distorter is set in a static way where a small offset in either bias, $V_{pd,in}$ or $V_{pd,in}^2$ set-point has a large influence on the performance. Furthermore the voltage loop gain crossover could be increased as there is enough phase margin. This possibility was overlooked during the design phase.

Finally the results show that the THD for frequencies above 10 kHz is worse with pre-distorter. It is possible this is the result of the significantly changed load impedance, actually making performance worse at those frequencies.

The THD versus power is shown in figure 5.20. Again the THD without pre-distorter comes close to simulated values for larger powers.

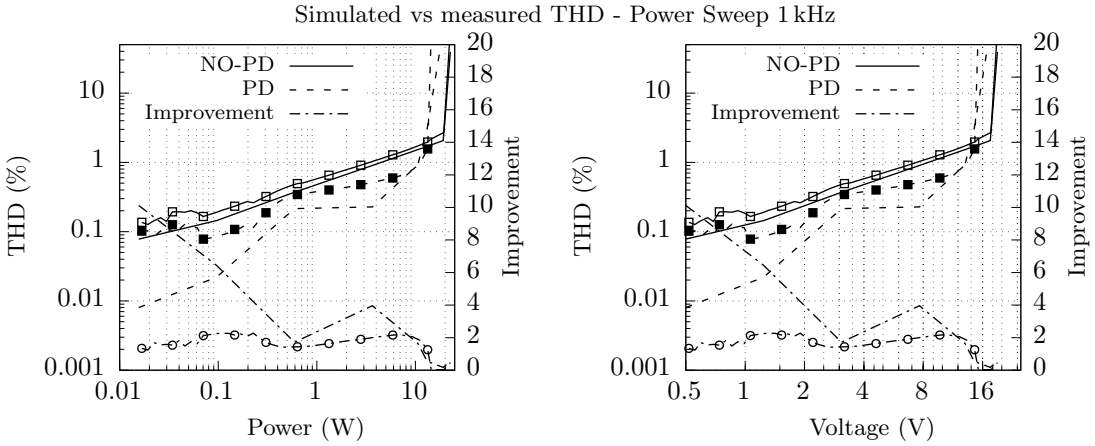

Figure 5.20: In this graph the closed voltage loop distortion measurement is compared to the simulation results for an output voltage of 10 V. Marked lines correspond with the measurement results, non marked lines with simulation. The simulation include the parasitic elements, which are also present in the prototype implementation.

A discrepancy can be seen for small amplitudes where there is in both cases a large difference between simulated values and measured values, it is suspected this is due to the output voltage ripple. At these low voltages the analyzer automatically switches to another input range and it is possible it can not handle the signal plus ripple at these small amplitudes. Another indicator that

this is the case, is the noisy THD measurement at small output voltages. This is after averaging eight times. For future measurements a big low pass filter can be introduced before the audio analyzer to prevent voltage ripple from skewing measurements.

At around 3 V the analyzer switches input range and the results become smooth. Another interesting thing happens at this point, the converter with pre-distorter shows a THD-plateau until 9 V. This does not happen in the non-pre-distorted amplifier. The explanation for this phenomenon is as follows: when the output amplitude increases the current loop control to output voltage transfer without pre-distorter becomes increasingly more non-linear, increasing THD. If the pre-distorter works as intended THD levels should stay the same for increasing output voltages, until other circuit non-linearities will start to play a role.

The amplifier with pre-distorter clips / latches-up at 14.5 V, the point where the loop gain reverses. The non-pre-distorted amplifier only clips when the output amplitude is greater than 18 V, all the way down to the 12 V supply rail.

Specification summary

At the beginning of chapter 4 the specifications for the amplifier where given, in table 5.4 an overview of the measured specifications is given and an evaluation is given if the prototype is as specified.

Table 5.4: Summary of all the realized specifications in the prototype.

Requirement	**Value**	**Realized**	**On Spec**
Supply voltage	12 V	12 V	✓
Output bias voltage	30 V	30.1 V	✓
Input voltage swing	Line level (± 0.5 V to 1.5 V)	0.5 V to 1.5 V	✓
Output voltage swing	± 15 V (30 V)	± 14.5 V	✗
−3 dB BW	20 Hz to 20 kHz	20 Hz to 20 kHz	✓
Minimum load resistance	8 Ω	8 Ω	✓
Output power in 8 Ohm	12.5 W	13 W	✓
Total harmonic dist. (1 kHz)	0.1 % @ 10 W	0.6 % @ 10 W	✗

5.4 General Considerations & Discussion

Some general considerations and suggestions can be made after the whole process of design, simulation and taking measurements has been completed.

A multitude of problems have been observed with regard to the pre-distorter implementation. It has proven difficult to calibrate and sensitive to circuit variations and drift. The pre-distorter improves the THD but not by the amount predicted by simulations. Furthermore it only works well for a fixed load resistance which is not the case for a speaker. Another improvement could be made if the current sense gain is increased, this makes the pre-distorter less vulnerable to offsets. Increasing the current sense gain also improves noise immunity.

A number of improvements can be made to the system if the voltage loop plus pre-distorter were to be implemented in the digital domain. This has a number of advantages:

- The voltage loop compensation can be done dynamically and not only for the worst case dynamics.
- The output current can be measured next to the output voltage for load impedance calculations, these values can then be used for digital pre-distortion based on the calculated load impedance.
- The supply voltage can be measured and used in the pre-distorter to increase PD power supply rejection.
- In the digital domain the squarer can be implemented in an easy way.

The provisions to implement this are already available on the prototype but due to the limited time and scope of this project this is not implemented. This is something which can be looked at in further research.

Next to the problems with the pre-distorter, a number of comments can be made on the THD of the amplifier. Especially for higher frequencies the THD is rather high, which can be explained by the loop gain decrease when the frequency becomes higher. This raises the question if the amplifier is suitable for the full audio range. It could however be used as a subwoofer amplifier (20 Hz to 200 Hz with THD figures below 0.1 % at 10 W). In audio the most power is in the bass frequencies so it makes sense to do that from an efficiency point of view.

Furthermore an average current mode controlled converter gives primarily second order distortion as can be seen in figure 3.4. The implementation complexity was an argument to skip a bridge tied load implementation but in hindsight this would be an effective option to reduce most of the distortion. However as one side of the bridge sees half the load impedance the design should be done for 4 Ω impedance, giving extra issues with regard to the RHPZ position and ripple current in the inductor.

Problems have been observed with regard to the power supply being one quadrant. In a car this problem is mitigated because current flowing back to the battery will charge the battery, the typical 4 mΩ internal resistance does also give minimal supply ripple.

In future research a better trade-off between switching loss and ripple loss needs to be made. Using the equations shown in 5.1 figure 5.21 is constructed. A higher $R_{ds,on}$ gives better low power efficiency while only influencing high power efficiency outside the range of the amplifier proposed in this work.

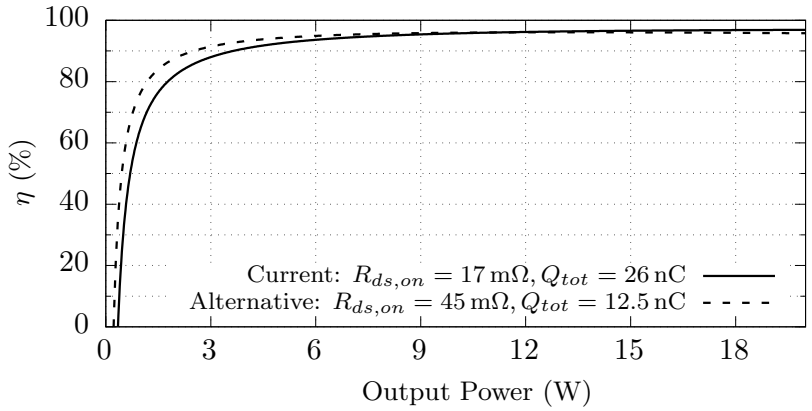

Figure 5.21: Theoretical efficiency versus output power. A higher $R_{ds,on}$ MOSFET will give more efficiency at low output powers.

Chapter 6

Conclusion & Recommendations

Traditionally a two stage implementation (Boost converter + Class D) is used for low voltage supply to high output power audio amplifications. This work has proposed an audio amplifier using a boost converter only. The goal is to improve efficiency and reduce component count which reduces cost. However boost converters are inherently very non-linear, resulting in a poor audio amplifier.

Literature shows limited attempts in using a dynamic boost converter as audio amplifier due to the inherent non-linearity and changing dynamics of the power stage. In this work general linearization methods have been adapted for use in a dynamic boost converter. A double loop feedback structure is used: an inner current control loop sets the inductor current and the outer voltage loop controls the inner loop based on the required output voltage. The non-linearity of the current mode controlled converter has been investigated with the goal of inserting a pre-distorter in the outer control loop which further improves linearity.

The results show that the widely used PCMC converter is a bad candidate for usage as audio amplifier due to the way the controller is implemented on the system level. Slope compensation required for stability in such converters, will overcompensate much of the time resulting in reduced system performance. The peak/average inductor current ratio for small currents is bad, resulting in distortion at the output. Furthermore the large signal behaviour is analytically complex making it difficult to pre-distort.

Average current mode control does not suffer from the last two issues and is a better approximation of the intended ideal current source behaviour. Furthermore it has a square root large signal transfer making it easily pre-distortable. Both reasons to use an average current mode stage for implementing the current loop.

Decoupling is needed for a single ended audio amplifier, changing the large signal transfer characteristics of the converter. The converter retains the square root behaviour but there is a minimum output voltage of $V_{bias}/2$. For this square root behaviour a pre-distorter is created which linearizes the current loop between 15 V to 45 V output voltage.

The pre-distorter curve is dependent on supply voltage, load impedance, current sense gain in the current loop and output bias voltage. Especially the load impedance is troublesome in a statically configured pre-distorter. If a speaker is connected as the impedance changes over frequency, reducing the effectiveness of the pre-distorter.

A design is made for an amplifier which has a power gain of 5 x compared to a standard single ended class D amplifier. The amplifier works supply voltage of 12 V and a load impedance of 8 Ω. The minimum load impedance is limited by the trade-off between right half plane zero position, switching frequency and inductor current ripple. No good models are available for a decoupled average current mode controlled converter which complicates design. Next to a own derivation done for the DC-gain, primary pole and RHPZ in appendix A simulations were used to verify each design step. Feedback design is further complicated by bias dependent dynamics resulting in a

sub-optimal controller over the whole output voltage range.

Two separate designs are made, with and without pre-distorter so that they can be compared with regard to performance. Both amplifiers have full audio bandwidth.

Simulations including parasitic elements show that the closed loop system with pre-distorter has a THD improvement of about 6 for low frequencies. The improvement decreases for higher frequencies as the output capacitance of the converter reduces the load impedance. As the load impedance is included in the pre-distorter settings, this is to be expected.

A prototype has been created to compare simulation results to circuit implementation. The THD improvement is further reduced to about 3 for low frequencies. This is due to the chosen implementation for the pre-distorter, small off-sets or drift in circuit parameters quickly reduce pre-distorter performance. In hindsight the current static implementation of the pre-distorter is not the best way to implement it, as the settings are very component and circuit dependent.

The measured THD is 0.6 % versus 1.3 % without pre-distorter. These results are obtained at 10 W output power and 1 kHz output frequency. These THD values are comparable with literature[2, 16], however as both authors used a bridge tied load configuration, the obtained 0.6 % THD is a pretty good result.

Concluding it is possible to create a single stage boost converter audio amplifier for the full audio range. Adding the pre-distorter does improve the THD by a small amount and this makes the THD performance dependent on load impedance. As the speaker impedance is not constant the amplifier without pre-distortion works better for a speaker connected load. This might be solved by implementing a digital pre-distorter and digital voltage loop compensator.

For full range audio applications it is not the best choice to use a boost converter as amplifier, as the THD levels are quite high for higher frequencies. Performance is severely limited by the right half plane zero which limits the possible voltage loop bandwidth and therefore loop gain. As subwoofer amplifier however, a boost converter amplifier is much more feasible.

6.1 Recommendations & Further Research

During design, the lack of good average current mode control models for the decoupled boost converter was quite limiting. Research can be done how the decoupling changes the small signal models of the average current mode control stage.

Alternatively more control schemes need to be investigated, such as non-linear control methods like sliding mode control[2]. In this work both the voltage loop and current loop compensator have fixed components, where the compensators have been designed for worst case scenarios. This results in underperformance for non worst case conditions. Non-linear control solves these issues.

Moreover the pre-distorter settings are dependent on the load impedance making it sub-optimal for speaker loads, it might be interesting for further research to do current measurements to calculate the load impedance. A digital voltage controller and pre-distorter can then be used to handle this information. This has the additional benefit of also solving the problem of a fixed component voltage loop compensator, as the compensator can be adapted in the digital domain for different bias points.

When designing careful inspection of loop gain plots should be done to prevent sub-optimal design. In this case the voltage loop gain crossover with pre-distorter could be increased as there is still enough phase margin. This possibility was overlooked during the design phase, and would have increased the improvement in THD with pre-distorter.

The crossover of the voltage loop gain is rather high, it might be possible to create a higher order compensator to have more loop gain at lower frequencies. Allowing for a better subwoofer amplifier.

Furthermore one of the motivations to use a boost converter as amplifier was the improved efficiency. As this work was about linearization, efficiency has not been investigated. This can be done in further research.

The audio susceptibility of the converter also needs to be investigated as in a real world car application supply voltage can vary between 12 V to 14.5 V depending on the speed and state of the car.

Appendix A

Derivation: Small signal dynamics in ACMC when decoupled

Using the large signal equations and the average switch model derived in fundamentals of power electronics[5], the DC gain, the primary pole location and right half plane zero location can be derived.

A.1 DC Gain

The small signal DC-gain of the decoupled converter can be found by differentiating the large signal transfer function found in chapter 3:

$$V_c = \frac{(V_{out}^2 - V_{out}V_{bias})R_s}{R_L V_{DD}}$$

$$V_{out} = \frac{V_b}{2} + \frac{\sqrt{4V_c V_{DD} R_L R_s + V_b^2 R_s^2}}{2R_s}$$

$$\frac{dV_{out}}{dV_c} = \frac{R_L V_{DD}}{\sqrt{4V_c R_L R_s V_{DD} + R_s^2 V_b^2}} = \frac{R_L V_{DD}}{R_s\sqrt{4\frac{V_c}{R_s} R_L V_{DD} + V_b^2}}$$

A.2 Right half plane zero and primary pole location

Using chapter 7 and 12 of the fundamentals of power electronics[5] the position of the right half plane zero and primary pole can be determined. Using figure A.1 the small signal averaged equations can be determined. In this model the assumption is made that $I_L = I_c$ which is the case in average current mode control.

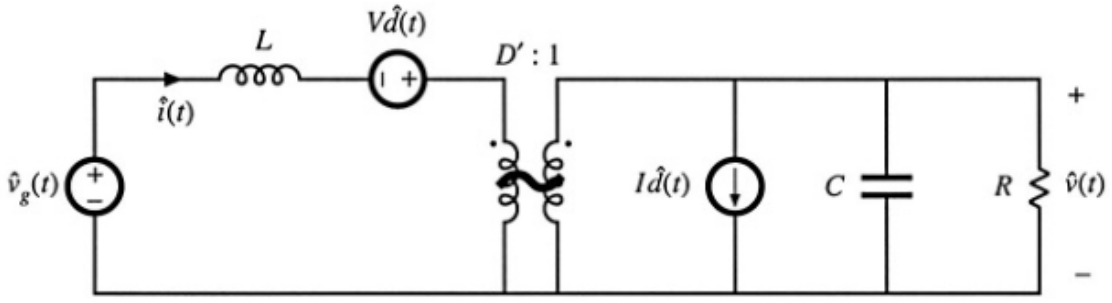

Figure A.1: Small signal model used for deriving the right half plane zero and primary pole locations when the converter is decoupled[5].

$$L\frac{d\hat{i}_L(t)}{dt} = \hat{v}_g(t) - D'\hat{v}(t) + V\hat{d}(t)$$
$$C\frac{d\hat{v}(t)}{dt} = D'\hat{i}_L(t) - \frac{\hat{v}}{R} - I_L\hat{d}(t)$$
$$\hat{i}_g(t) = \hat{i}_L(t) + \frac{I_L}{D'}\hat{d}(t)$$

These equations can be written in the s-domain with the Laplace transform:

$$sL\hat{i}_L(s) = \hat{v}_g(s) - D'\hat{v}(s) + V\hat{d}(s)$$
$$sC\hat{v}(s) = D'\hat{i}_L(s) - \frac{\hat{v}(s)}{R} - I_L\hat{d}(s)$$
$$\hat{i}_g(s) = \hat{i}_L(s) + \frac{I_L}{D'}\hat{d}(s)$$

Now the first Laplace equation can be used to find $\hat{d}(s)$ where the assumption of $\hat{i}_L = \hat{i}_c$ is made:

$$sL\hat{i}_c(s) = \hat{v}_g(s) - D'\hat{v}(s) + V\hat{d}(s)$$
$$\hat{d}(s) = \frac{sL\hat{i}_c - \hat{v}_g(s) + D'\hat{v}(s)}{V}$$

The $\hat{d}(s)$ can then be filled in to the second equation:

$$sC\hat{v}(s) = D'\hat{i}_L(s) - \frac{\hat{v}(s)}{R} - I_L\left(\frac{sL\hat{i}_c - \hat{v}_g(s) + D'\hat{v}(s)}{V}\right)$$

Using the large signal bias points I_L and V another step can be made in deriving the $\hat{i}_c to \hat{v}$ can be made:

$$I_L = \frac{I_{rl}}{D'} = \frac{V - V_{bias}}{D'R} = \frac{V_g}{D'^2R} - \frac{V_{bias}}{D'R}$$
$$V = \frac{V_g}{D'}$$

These can be filled in:

$$sC\hat{v}(s) = D'\hat{i}_c(s) - \frac{\hat{v}(s)}{R} - \left(\frac{V_g}{D'^2R} - \frac{V_{bias}}{D'R}\right)\left(D'\frac{sL\hat{i}_c - \hat{v}_g(s) + D'\hat{v}(s)}{V_g}\right)$$
$$sC\hat{v}(s) = D'\hat{i}_c(s) - \frac{\hat{v(s)}}{R} - \frac{sL\hat{i}_c - \hat{v}_g(s) + D'\hat{v}(s)}{D'R} + \frac{V_{bias}(sL\hat{i}_c - \hat{v}_g(s) + D'\hat{v}(s))}{V_gR}$$

Split to individual components:

$$sC\hat{v}(s) = \left(D' - \frac{sL}{D'R} + \frac{sLV_{bias}}{V_gR}\right)\hat{i}_c(s) - \left(\frac{2}{R} - \frac{D'V_{bias}}{V_gR}\right)\hat{v}(s) + \left(\frac{1}{D'R} - \frac{V_{bias}}{V_gR}\right)\hat{v_g}(s)$$

Set $\hat{v}_g(s) = 0$ for small signal $\hat{i}_c$ to $\hat{v}$ transfer:

$$sC\hat{v}(s) = \left(D' - \frac{sL}{D'R} + \frac{sLV_{bias}}{V_gR}\right)\hat{i}_c(s) - \left(\frac{2}{R} - \frac{D'V_{bias}}{V_gR}\right)\hat{v}(s)$$
$$\frac{\hat{v}(s)}{\hat{i}_c(s)} = \frac{D' - \frac{sL}{D'R} + \frac{sLV_{bias}}{V_gR}}{sC + \frac{2}{R} - \frac{D'V_{bias}}{V_gR}} = D'\frac{1 - s\left(\frac{L}{D'^2R} - \frac{LV_{bias}}{D'V_gR}\right)}{sC + \frac{2}{R} - \frac{D'V_{bias}}{V_gR}}$$

Which gives the following equations for the right half plane zero and primary pole positions:

$$\omega_{rhpz} = \frac{1}{\frac{L}{D'^2R} - \frac{LV_{bias}}{D'V_gR}} = \frac{D'^2R_L}{L}\left(\frac{V_g}{V_g - V_{bias}D'}\right) = \frac{D'^2R_L}{L}\left(\frac{V_{out}}{V_{out} - V_{bias}}\right)$$

$$\omega_0 = -\frac{2}{RC} + \frac{D'V_{bias}}{V_gRC} \rightarrow f_0 = \frac{2}{2\pi RC} - \frac{D'V_{bias}}{2\pi V_gRC}$$

Using figure 4.12 the results obtained above can be validated:

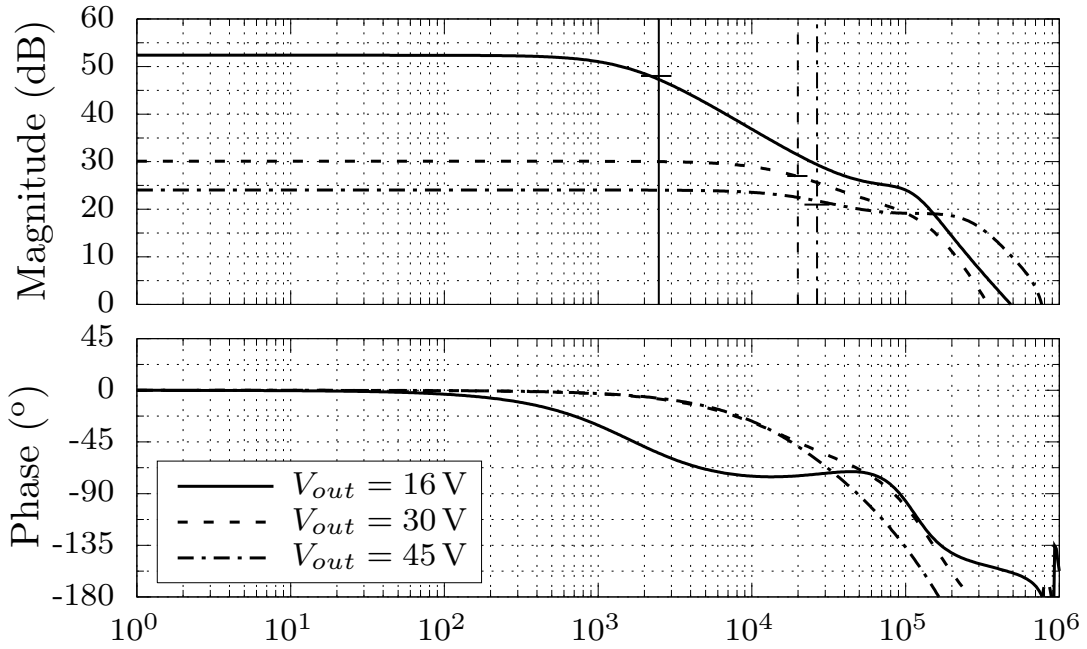

Figure A.2: **Vo/Vc transfer** The control to output voltage of the ACMC stage is plotted for different output voltages. These can be used to verify the primary pole and right half plane zero locations. The lines indicate the corresponding calculated pole frequencies and the horizontal lines the $-3\,\mathrm{dB}$ point of the bode plot.

The calculated primary pole locations are:

$$f_0 = \frac{2}{2\pi RC} - \frac{D'V_{bias}}{2\pi V_gRC}$$

$$f_{0,V_{out}=16} = \frac{2}{2\pi \cdot 8 \cdot 1\mathrm{e}{-6}} - \frac{(1-0.25)\cdot 30}{2\pi \cdot 12 \cdot 8 \cdot 1\mathrm{e}{-6}} = 2.5\,\mathrm{kHz}$$

$$f_{0,V_{out}=30} = \frac{2}{2\pi \cdot 8 \cdot 1\mathrm{e}{-6}} - \frac{(1-0.60)\cdot 30}{2\pi \cdot 12 \cdot 8 \cdot 1\mathrm{e}{-6}} = 19.9\,\mathrm{kHz}$$

$$f_{0,V_{out}=45} = \frac{2}{2\pi \cdot 8 \cdot 1\mathrm{e}{-6}} - \frac{(1-0.73)\cdot 30}{2\pi \cdot 12 \cdot 8 \cdot 1\mathrm{e}{-6}} = 26.5\,\mathrm{kHz}$$

These locations closely match the pole locations given by simulation as shown in figure A.2. The

same can be done for the right half plane zero positions:

$$f_{rhpz} = \frac{D'^2 R_L}{2\pi L}\left(\frac{V_{out}}{V_{out} - V_{bias}}\right)$$

$$f_{rhpz,V_{out}=16} = \frac{(1-0.25)^2 \cdot 8}{2\pi \cdot 3.3\text{e}{-6}}\left(\frac{16}{16-30}\right) = -248.0\,\text{kHz}$$

$$f_{rhpz,V_{out}=30} = \frac{(1-0.60)^2 \cdot 8}{2\pi \cdot 3.3\text{e}{-6}}\left(\frac{30}{30-30}\right) = \infty\ \text{kHz}$$

$$f_{rhpz,V_{out}=45} = \frac{(1-0.73)^2 \cdot 8}{2\pi \cdot 3.3\text{e}{-6}}\left(\frac{45}{45-30}\right) = 84.4\,\text{kHz}$$

Interestingly but not surprisingly the right half plane zero becomes a normal zero when currents are negative. Furthermore as expected, there is no right half plane zero at zero output current. The right half plane zero starts to influence the system only at positive output currents.

Appendix B

Derivation: Vref to Vout closed loop gain

A system gain of 10 is required, to calculate the closed loop transfer the simplified system from figure B.1 is used. First intuition says that the ratio between R_{upper} and R_{lower} set the system gain and makes the system behave like a typical non-inverting op-amp. However in this system it is not possible to separate feedback factor β and forward gain factor A. It is only possible to calculate the loop gain $A\beta$. The closed loop gain has to be calculated in a different way than the standard $A/(1 + A\beta)$ as A is not known.

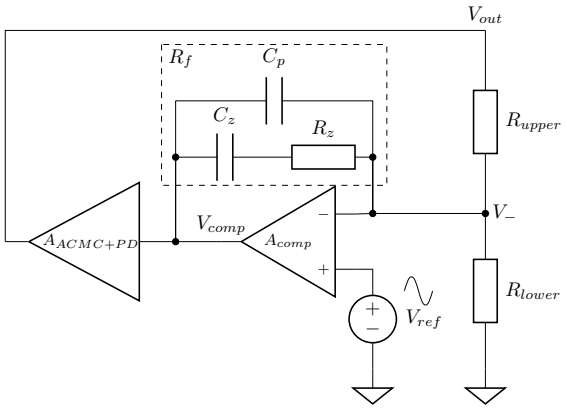

Figure B.1: Simplified schematic for calculating the closed loop voltage transfer of the whole system. This is not a trivial non-inverting opamp system as R_f will inject current at higher frequencies.

The loopgain ($A\beta$) of this system is given by:

$$T_{loop} = H_{ACMC,V_c \rightarrow V_{out}} H_{PD} H_{comp}$$

Where H_{comp} is given by[27, p. 336]:

$$H_{comp} = -\frac{R_f}{R_{upper}}$$

The closed loop transfer and DC gain can be calculated in an alternate way with the help of the superposition principle at the V_- node. V_{out} and V_{comp} are dependent sources, however superposition is still valid provided the controlling variable is not set to zero when the sources is deactivated[29]. The controlling variables are not set to zero when applying superposition in this derivation, so superposition can be used.

Superposition is done at the V_- node, with $V_{comp} = 0$ in one case and $V_{out} = 0$ in the other case.

$$\begin{aligned} V_{out} &= V_{comp} A_{ACMC+PD} \\ V_{comp} &= A_{comp}(V_+ - V_-) \\ V_- &= V_{comp} \frac{R_{upper}//R_{lower}}{R_{upper}//R_{lower} + R_f} | V_{out} = 0 \\ &= V_{out} \frac{R_f//R_{lower}}{R_f//R_{lower} + R_{upper}} | V_{comp} = 0 \end{aligned}$$

These equations can then be combined to get the transfer from V_{ref} to V_{out}

$$\begin{aligned} V_{comp} &= A_{comp} \left(V_{ref} - \left(V_{comp} \frac{R_{upper}//R_{lower}}{R_{upper}//R_{lower} + R_f} + V_{out} \frac{R_f//R_{lower}}{R_f//R_{lower} + R_{upper}} \right) \right) \\ &= A_{comp} V_{ref} - A_{comp} \left(V_{comp} \frac{R_{upper}//R_{lower}}{R_{upper}//R_{lower} + R_f} + V_{out} \frac{R_f//R_{lower}}{R_f//R_{lower} + R_{upper}} \right) \end{aligned}$$

$$\frac{V_{out}}{A_{ACMC+PD}} = A_{comp} V_{ref} - \frac{A_{comp} V_{out}}{A_{ACMC+PD}} \frac{R_{upper}//R_{lower}}{R_{upper}//R_{lower} + R_f} - A_{comp} V_{out} \frac{R_f//R_{lower}}{R_f//R_{lower} + R_{upper}}$$

$$\frac{V_{out}}{A_{comp} A_{ACMC+PD}} = V_{ref} - \frac{V_{out}}{A_{ACMC+PD}} \frac{R_{upper}//R_{lower}}{R_{upper}//R_{lower} + R_f} - V_{out} \frac{R_f//R_{lower}}{R_f//R_{lower} + R_{upper}}$$

$$V_{ref} = V_{out} \left(\frac{1}{A_{comp} A_{ACMC+PD}} + \frac{1}{A_{ACMC+PD}} \frac{R_{upper}//R_{lower}}{R_{upper}//R_{lower} + R_f} + \frac{R_f//R_{lower}}{R_f//R_{lower} + R_{upper}} \right)$$

Simplify and set A_{comp} to infinity to get the closed loop transfer:

$$\frac{V_{out}}{V_{ref}} = \frac{(R_f R_{lower} + R_f R_{upper} + R_{lower} R_{upper}) A_{ACMC+PD} A_{comp}}{A_{ACMC+PD} A_{comp} R_f R_{lower} + A_{comp} R_{lower} R_{upper} + R_f R_{lower} + R_f R_{upper} + R_{lower} R_{upper}}$$

$$\lim_{A_{comp} \to \infty} \frac{V_{out}}{V_{ref}} = \frac{A_{ACMC+PD}(R_{lower} R_f + R_f R_{upper} + R_{lower} R_{upper})}{R_{lower}(A_{ACMC+PD} R_f + R_{upper})} \tag{B.1}$$

Where R_f is infinite at DC:

$$\lim_{R_f \to \infty} \frac{V_{out}}{V_{ref}} = 1 + \frac{R_{upper}}{R_{lower}}$$

Bibliography

[1] B. E. Gaalaas, "Class D Audio Amplifiers: What, Why, and How," Analog Devices, Tech. Rep., 2006.

[2] G. Maizonave and M. Andersen, "Double-Boost DC-AC Converter with Sliding-Mode Control for Portable Audio," *Aes.Org*, pp. 1–7, 2009. [Online]. Available: http://www.aes.org/e-lib/browse.cfm?elib=15212

[3] Texas Instruments, "Synchronous rectification boosts efficiency by reducing power loss," Tech. Rep., 2013. [Online]. Available: http://www.ti.com/lit/an/slyt515/slyt515.pdf

[4] C. Basso, *Switch-Mode Power Supplies Spice Simulations and Practical Designs*, 2008. [Online]. Available: http://books.google.co.kr/books?id=Sf2kDaZI1MEC

[5] R. W. Erickson, *Fundamentals of Power Electronics*, 2002.

[6] W. G. Jung, *Op Amp Applications Handbook*. Newnes, 2005. [Online]. Available: https://books.google.com/books?id=dunqt1rt4sAC{&}pgis=1

[7] SIMetrix Technologies, "SIMetrix/SIMPLIS, Power Circuit analog simulation, design and simulate switching power electronics systems," 2015. [Online]. Available: http://www.simetrix.co.uk/site/simetrix-simplis.html

[8] P. Sanchis, A. Ursæa, E. Gubía, and L. Marroyo, "Boost DC AC Inverter : A New Control Strategy," *IEEE Transactions on Industrial Electronics*, vol. 20, no. 2, pp. 343–353, 2005.

[9] Texas Instruments and R. Zaitsu, "Voltage-Mode Boost Converter Small Signal Control Loop Analysis Using the TPS61030," Tech. Rep. May 2007, 2009.

[10] K. Habib, A. Alam, and S. Khan, "Average Current Control Mode Boost Converter for the Tuning of Total Harmonic Distortion & Power Factor Correction using PSIM," vol. 14, no. 5, 2014.

[11] L. Dixon, "Average Current Mode Control of Switching Power Supplies," Tech. Rep., 1999.

[12] T. Suntio, M. Rahkala, I. Gadoura, and K. Zenger, "Dynamic effects of inductor current ripple in peak-current and average-current mode control," *IECON'01. 27th Annual Conference of the IEEE Industrial Electronics Society (Cat. No.37243)*, vol. 2, no. C, pp. 1072–1077, 2001.

[13] Yingyi Yan, F. Lee, and P. Mattavelli, "Analysis and Design of Average Current Mode Control Using a Describing-Function-Based Equivalent Circuit Model," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4732–4741, 2013. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6387313

[14] R. B. Ridley, "Continuous-Time Model For Current-Mode Control," vol. 6, no. 2, 1991.

[15] T. O'Brien, J. Lee, and J. Beecroft, "A unified small signal analysis of DC-DC converters with Average Current Mode Control," *2009 IEEE Energy Conversion Congress and Exposition*, pp. 647–654, 2009. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5316523

[16] M. Prokin, "Boost bridge amplifier," p. 609, 2001. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp={&}arnumber=5741074

[17] T. H. Birch, D. Nielsen, A. Knott, and M. A. E. Andersen, "Predistortion of a bidirectional Cuk Audio amplifier," pp. 1–10, 2014.

[18] V. Michal, "Modulated-ramp PWM generator for linear control of the boost converters power stage," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2958–2965, 2012.

[19] K. Jha and S. Mishra, "Large-signal linearization of a boost converter," in *2010 IEEE Energy Conversion Congress and Exposition, ECCE 2010 - Proceedings*, no. Dlm, 2010, pp. 4140–4144. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp={&}arnumber=5617739

[20] S. K. Mishra, K. Jha, and K. D. T. Ngo, "Dynamic linearizing modulator for large-signal linearization of a boost converter," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 3046–3054, 2011.

[21] K. Jha, S. Mishra, and A. Joshi, "High-Quality Sine Wave Generation Using a Differential Boost Inverter at Higher Operating Frequency," *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 373–384, 2015. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6828776

[22] Maplesoft, "Maple for Academics." [Online]. Available: http://www.maplesoft.com/products/Maple/academic/

[23] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2001. [Online]. Available: https://books.google.nl/books/about/Design{_}of{_}Analog{_}CMOS{_}Integrated{_}Circuit.html?id=hdavQgAACAAJ{&}pgis=1

[24] Texas Instruments, "Selecting the right inductor for ultra-low distortion Class-D audio amplifiers," 2015. [Online]. Available: https://e2e.ti.com/blogs{_}/b/analogwire/archive/2016/01/29/inductor-linearity-for-ultra-low-distortion-class-d-audio-amplifiers?DCMP=TPA3251D2{&}HQS=hpa-aap-aud-TPA3251D2-twit-blog-20160129-wwe{&}hootPostID=8564dddb0609937e9220dfab15b7f921

[25] ——, "TPA3122: 15-W STEREO CLASS-D AUDIO POWER AMPLIFIER," Tech. Rep., 2007.

[26] ——, "Basic Calculation of a Boost Converter's Power Stage," Tech. Rep., 2011.

[27] C. Basso, "The Right Half Plane Zero, a Two-Way Control Path," Tech. Rep., 2008.

[28] J. Sun and R. Bass, "Modeling and practical design issues for average current control," *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, vol. 2, pp. 980–986, 1999.

[29] W. Leach, "On the application of superposition to dependent sources in circuit analysis," 1994. [Online]. Available: http://users.ece.gatech.edu/mleach/papers/superpos.pdf

[30] L. Risbo and C. Neesgaard, "PWM Amplifier Control Loops with Minimum Aliasing Distortion," in *120th AES Convention*, Paris, 2006.

[31] S. Wei and J. S. Chang, "THD of Closed-Loop Analog PWM Class-D Amplifiers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, no. 6, pp. 1769–1777, 2008. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=4447006$\delimiter"026E30F$nhttp://ieeexplore.ieee.org/ielx5/8919/4563499/04447006.pdf?tp={&}arnumber=4447006{&}isnumber=4563499

[32] Würth Elektronik, "WE-HCC SMD High Current Cube Inductor - 7443330330," Tech. Rep., 2015. [Online]. Available: http://katalog.we-online.de/pbs/datasheet/7443330330.pdf

[33] Texas Instruments, "LM5106 100V Half Bridge Gate Driver with Programmable Dead-Time," Tech. Rep. October, 2009. [Online]. Available: www.ti.com/lit/ds/symlink/lm5106.pdf

[34] H. Ma, "High-Voltage Class-D Power Amplifiers - Design and Optimization," PHD, University of Twente, 2015.

[35] NXP Semiconductor, "PSMN018-80YS," Tech. Rep. October, 2010.

[36] Analog Devices, "AD8210: High Voltage Current Shunt Monitor," Tech. Rep., 2009. [Online]. Available: http://www.analog.com/static/imported-files/data{_}sheets/AD8212.pdf

[37] Texas Instruments, "LMH6639 190MHz Rail-to-Rail Output Amplifier with Disable 190MHz Rail-to-Rail Output Amplifier with Disable," Tech. Rep., 2013. [Online]. Available: www.ti.com/lit/ds/symlink/lmh6639.pdf

[38] ——, "LMV7219 7-ns 2 . 7-V to 5-V Comparator with Rail-to-Rail Output," Tech. Rep., 2015. [Online]. Available: www.ti.com/lit/ds/symlink/lmv7219.pdf

[39] R. Mancini and B. Carter, "Op Amps for everyone," Tech. Rep. SLOD006B, 2002. [Online]. Available: http://www.sciencedirect.com/science/book/9781856175050

[40] Analog Devices, "AD633: Analog Multiplier," Tech. Rep., 2011.

[41] Texas Instruments, "OPAx171 36-V, Single-Supply, General-Purpose Operational Amplifiers," Tech. Rep., 2015.

[42] Atmel, "ATSAM3S1BB Datasheet," Tech. Rep.

[43] BK Precision, "Dual Channel Function / Arbitrary Waveform Generators 4060 Series," Tech. Rep., 2015.