# UNIVERSITY OF TWENTE.

**Faculty of Electrical Engineering,**
**Mathematics & Computer Science**

# Approximation of an ideal bandpass filter using an N-path filter with overlapping clocks and harmonic rejection

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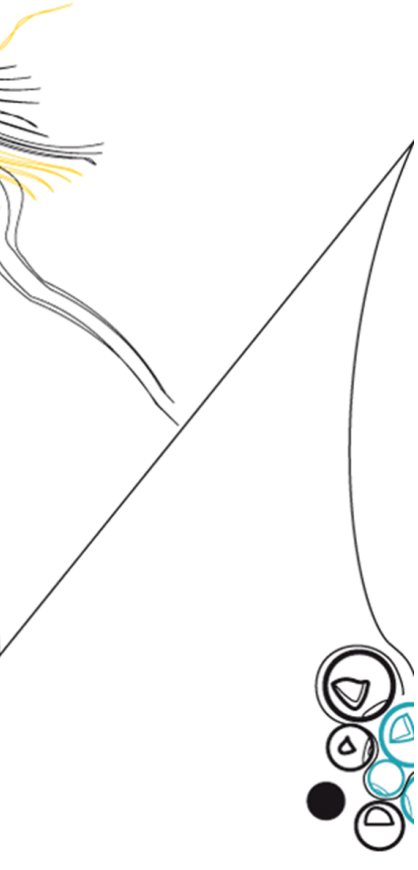
**MSc. Thesis**
**August 2012**



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# 1 Preface

Before you lies the accumulation of five years Electrical Engineering at the University of Twente. I started with the design of an oscillator using self-clocked N-path filters. Unfortunately strong indications were found that this would not be possible and the subject was changed to the improvement of N-path band-pass filters. Special thanks go to my daily supervisor Milad for the many fruitful discussions as well as his extensive knowledge on the N-path filters. My thanks also go to my fellow students at the ICD chair for their input.

# 2 Summary

N-path filters are switched filters that allow baseband transfer functions to be transformed to an arbitrary frequency. These filters have gained renewed interest after many years of absence due to the availability of high speed transistors enabling N-path filters to be used at gigahertz frequencies. Much research on N-path filters has been done already starting in the 1960s [1]. Most authors use a first-order RC low-pass filter as a baseband network to create a band-pass filter resembling a high-Q LC tank. Analytical solutions are available for such networks. Other functions such as notch filters and constant delays are possible. The focus of this thesis is the band-pass filter. The use of the N-path topology for a band-pass filter allows for narrowband filters which are easily tuned as the centre frequency is determined by a clock signal. The filter shape is dictated by the baseband transfer function.

The tuneability of this filter makes it suitable for upcoming applications such as software defined radio (SDR). Practical N-path filters suffer from two problems that limit their applicability. The first is that it does not only pass the desired frequency content but also the contents that are present around the harmonics of the clock much like comb filters (harmonic transfer). This puts strong demands on any mixer in a subsequent stage which has to supress these harmonics. The second problem is that the filter will fold the harmonics $k \cdot N - 1$ and $k \cdot N + 1$ $(k \in \mathbb{N})$ into the desired signal at the fundamental harmonic (harmonic folding). Strong interferers at these frequencies can corrupt the desired signal. This work aims to provide solutions to these problems.

The proposed solution against harmonic transfer is the use of harmonic rejection mixers instead of the simple switches that are commonly used. This idea conserves the folding properties of typical N-path filters while effectively suppressing the band-pass filters at higher harmonics of the clock. These mixers can easily be implemented by impedance scaling at the cost of area in each path. The suppression of higher harmonics greatly relaxes the design of a subsequent mixer stage. Each harmonic rejection mixer requires roughly $N$ switches and impedances. This means that the area required for switches and impedances scales with $N^2$ which may be problematic for large $N$.

The harmonic folding can be resolved by increasing the number of clock phases. Creating non-overlapping clocks with a high number of phases is difficult at RF as it generally requires very high frequencies. The option of using overlapping clocks was explored to allow for other clock generation techniques to be used such as ring oscillators. The idea is proven to be possible provided that a good adder is available.

A filter combining harmonic rejection mixers and overlapping clocks has been simulated to show their potential. This filter uses 24 clock phases with a duty cycle of $0.125$. The harmonic rejection mixers use 12 phases with a switched capacitor low pass filter. The resulting filter has a bandwidth of $8MHz$, a noise figure of $4.8dB$ and a gain of $7.2dB$. The transfer function shows no harmonic transfer up to the $11th$ harmonic and the first folder is the $23rd$ harmonic. Although each application requires different specifications, the filter shows the potential of the two techniques.

# Contents

# 3 Introduction

Typical receiver architecture consists of a band-pass filter, low noise amplifier (LNA), mixer, channel-select filter and an analog-to-digital converter (ADC). The band-pass filter aims to remove all large out-of-band blockers. This filter is usually off-chip and non-tuneable. The LNA amplifies the signal to prevent the noise of subsequent stages from corrupting the desired signal. The mixer then converts the amplified signal to baseband. The channel-select filter selects the desired channel which is then sampled by the ADC for further digital processing. Of course many other topologies exist. This thesis focusses on the design of an integrated and tuneable band-pass filter.

The band-pass filter determines the bandwidth of the signal that is fed into the LNA. Many radio techniques utilise only a small portion of the radio spectrum. Besides the signal of interest, the spectrum contains many other signals with varying power levels which may be well above the signal power level. It is desirable to remove these unwanted signals as soon as possible in the receiver chain as it relaxes the linearity requirements of the components. A band-pass filter with the bandwidth of the signal is thus desired. Many filter topologies are available which all have their own positive and negative aspects. Active filters are generally noisy and much power is used to limit their noise contribution. In addition, the dynamic range is often very limited. Some passive filters such as surface- and bulk-acoustic wave (SAW and BAW) filters require special materials and fabrication techniques that make them relatively expensive. Moreover, they are not tuneable and arrays of them are required to cover the specified frequency band of interest. A relatively new option at RF frequencies is the N-path filter. N-path filters can be used to approximate inductor-capacitor (LC) tanks. In contrast to LC filters, N-path filters can potentially achieve higher quality factors. Because they are made of only switches and capacitors, they can easily be integrated in CMOS. The centre frequency can easily be tuned by adjusting the clock frequency.

N-path filters suffer from two issues that limit the application of N-path filters in place of LC tanks: harmonic transfer and harmonic mixing. This thesis aims to find solutions to remove these two effects. First, the much researched resistor-capacitor (RC) N-path filter using non-overlapping clocks is investigated. This knowledge is then used to predict the behaviour of two variations: overlapping clocks and harmonic rejection mixers. Simulations are both done using RC and switched-capacitor (SC) filters. The solutions found are combined into one filter to show the potential of the proposed techniques.

# 4 N-path filter

In its most general sense, an N-path filter is a filter that consists of N parallel paths. Each path contains two mixers and a baseband transfer function. The mixers effectively shift this baseband transfer function to a band-pass transfer function. The baseband characteristics can take any form making it possible to use a wide range of baseband filter topologies to create any desired filter shape. This thesis only focuses on low-pass baseband filters in order to create band-pass filters at RF comparable to an LC tank. First the characteristics of an 'ideal' N-path filter are described. Realistic filters suffer from several non-idealities which are discussed subsequently. Due to the many possibilities for implementing the mixers and baseband transfer function, a commonly-researched variant is chosen to be examined: an N-path filter using a RC low-pass network and square-wave mixing functions. The properties of this filter are then used to predict the behaviour of other variants.

## 4.1 Ideal N-path filter

Each path of the filter consists of two mixers with a baseband transfer function between them. This general topology of an N-path filter is shown in Figure 1. $h(t)$ is the baseband impulse response. $p(t)$ and $q\ (t)$ are the mixing functions and usually equal in shape although a phase difference is possible. The functions $p_1(t)$ through $p_n(t)$ and $q_1(t)$ through $q_n(t)$ are equal in shape but have phase difference between them. The phase difference between phases $p_1(t)$ - $p_n(t)$ and $q_1(t)$ - $q_n(t)$ ($1 \leq n \leq N$) is given by equation **4.1**.

$$\phi_{diff} = \frac{2\pi}{N} \cdot n, \qquad 1 \leq n \leq N-1, \qquad N \in \mathbb{N} \tag{4.1}$$

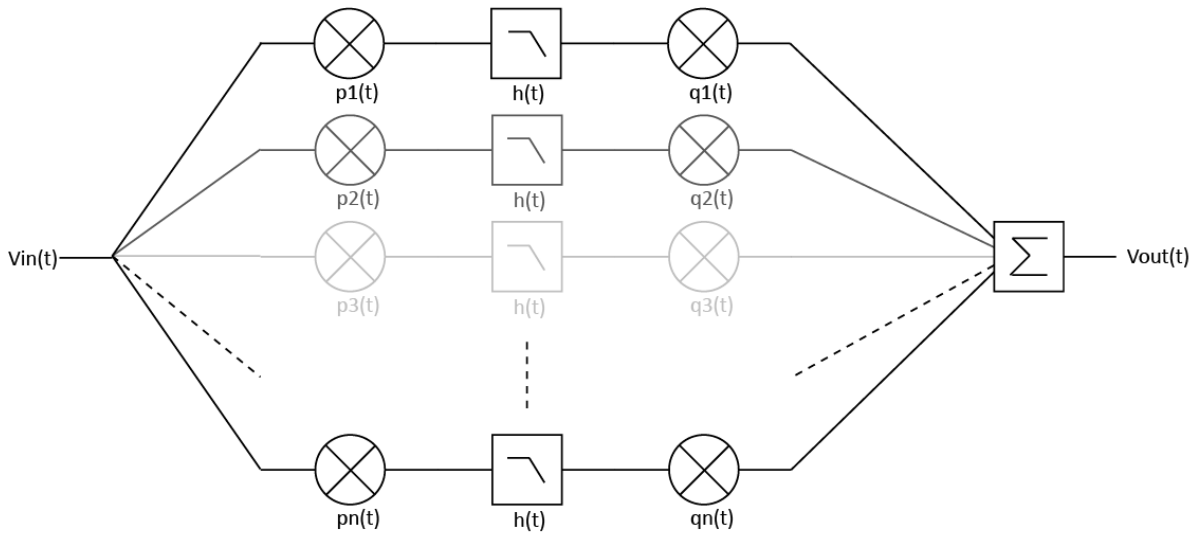


**Figure 1 – N-path band-pass filter. The input signal is first mixed down to baseband, then low-pass filtered and mixed up again. The outputs of all stages are then summed together. Adapted from Borelli [2].**

In the ideal case the mixing functions p(t) and q(t) are sinusoidal waves. In order to be insensitive to the phase of the input signal, a minimum of two paths with sine and cosine mixing functions is required. Figure 2 shows the workings of such a filter. Only the desired frequency content is preserved, all other signals are removed.

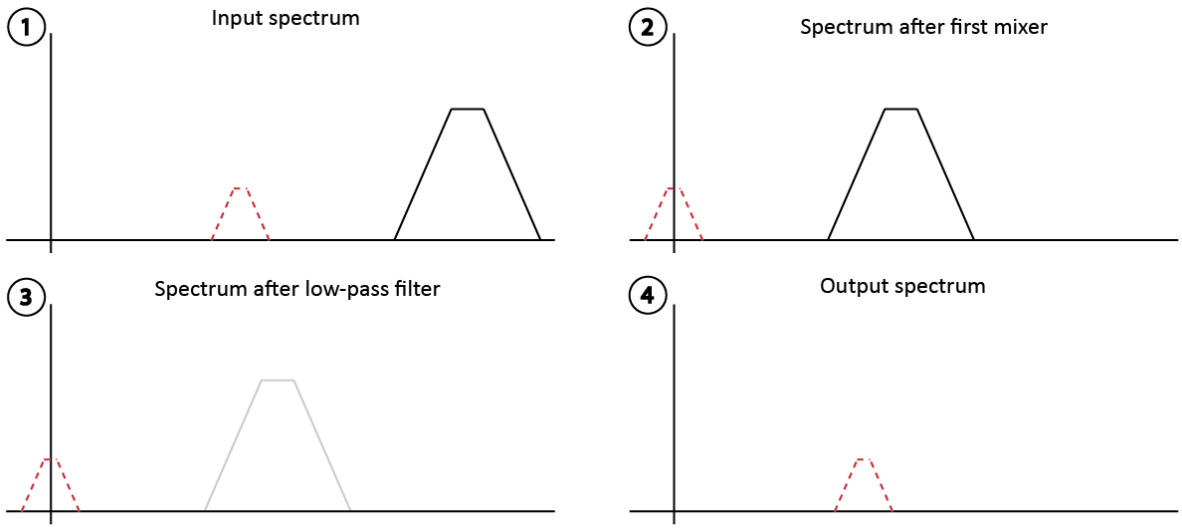


**Figure 2 – Operation of the N-path filter in the frequency domain. The dotted signal is the desired signal. The original spectrum (1) is shifted to baseband (2) where it is filtered (3). The signal is shifted back to RF and only the desired signal remains (4). The sum frequencies are of higher frequency than the original signals; they are assumed to be filtered out along with the rest of the signals and are not depicted in this image for reasons of clarity.**

### Baseband transfer function and bandwidth

The bandwidth of the band-pass filter is equal to twice the bandwidth of the baseband transfer function. For a first-order RC network the bandwidth is mainly dependent on the RC combination and the duty cycle of the clock. R represents the total resistance including any resistance, such as source and switch resistance, between the source and the capacitor C. For a low-pass network the bandwidth (-3dB) is defined by equation **4.2**. The bandwidth of the filter is a function of the duty cycle of the clock. The short exposure to the input signal divides the time constant by the duty cycle; D.

$$BW_{low-pass} = \frac{D}{2\pi RC}\ [Hz] \tag{4.2}$$

The band-pass filter has twice the bandwidth of the baseband filter resulting in equation **4.3**.

$$BW_{band-pass} = \frac{2D}{2\pi RC} = \frac{D}{\pi RC}\ [Hz] \tag{4.3}$$

An observation is that as the number of phases increases (and thus the duty cycle decreases), the bandwidth decreases. For a fixed bandwidth this means that the total capacitance can stay the same for a given bandwidth, for any number of stages as long as the R is kept constant. This makes the scaling towards a higher number of phases area-efficient as the capacitors generally consume much more area than the resistors.

## 4.2 Deviation from ideal behaviour

The ideal filter path can be realised using just two paths with quadrature sinusoidal mixing functions. Practical filter paths use square-wave mixing functions instead of sinusoidal ones. This introduces flaws which can be compensated for by using more than two paths resulting in an N-path filter.

### Non-ideal mixing functions

Multiplying with a sine-wave is problematic in practice as it requires linear analog multipliers. A practical mixing function is the square-wave which can be made using switches. One positive aspect of using switches is that the amplitude of the output waveform is independent of the amplitude of the mixing waveform. The frequency content of a square-wave also contains higher harmonics which will cause the mixing of higher frequency components to baseband and back up. Two general assumptions that are commonly made and will also be used in this chapter are that the clock phases are non-overlapping and have zero rise and fall times.

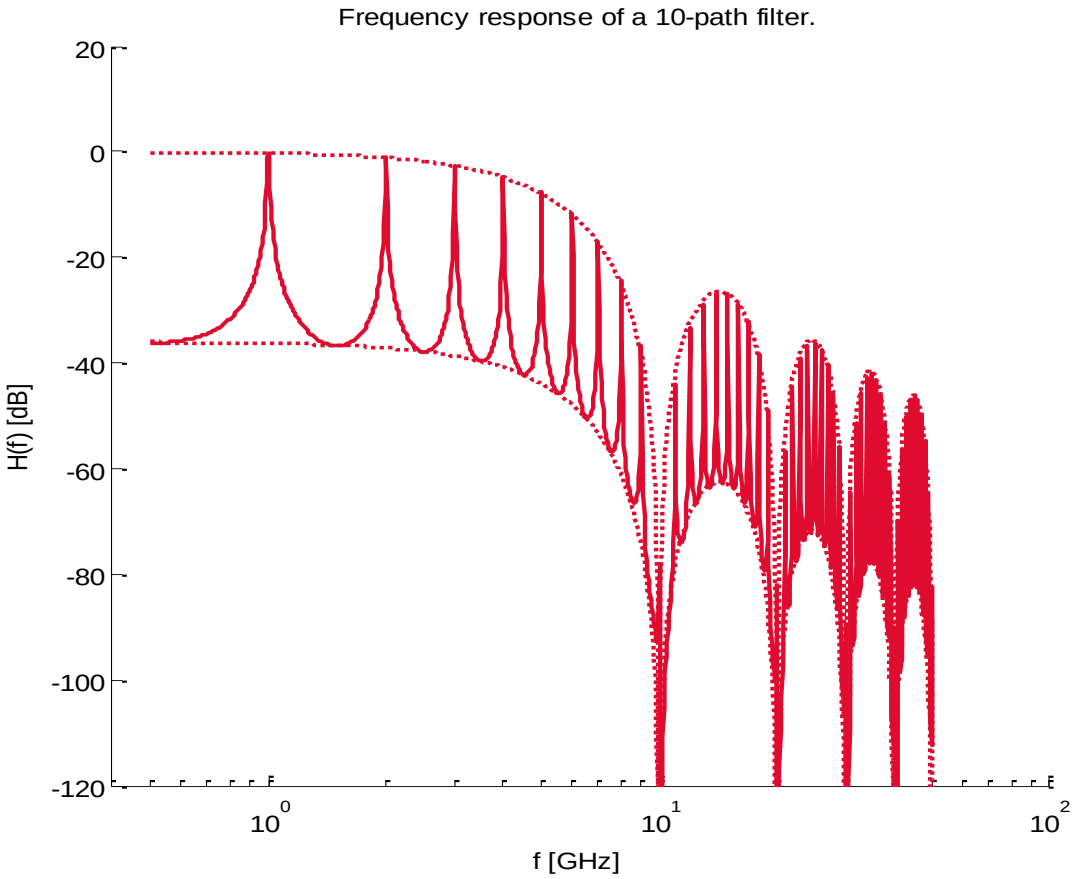


**Figure 3 – Frequency response of a 10-path filter. The dotted lines represent the envelope of the transfer function and are governed by equation 4.4. The distance between the dotted lines is given by equation 4.5.**

### Transfer function

As square-wave mixing functions contain higher harmonics, so does the resulting transfer function; the filter does not only pass the fundamental harmonic but also the higher harmonics. This results in a comb-like frequency response. Frischl has provided an analytical solution for this transfer function given the circuit in Figure 4 [3].

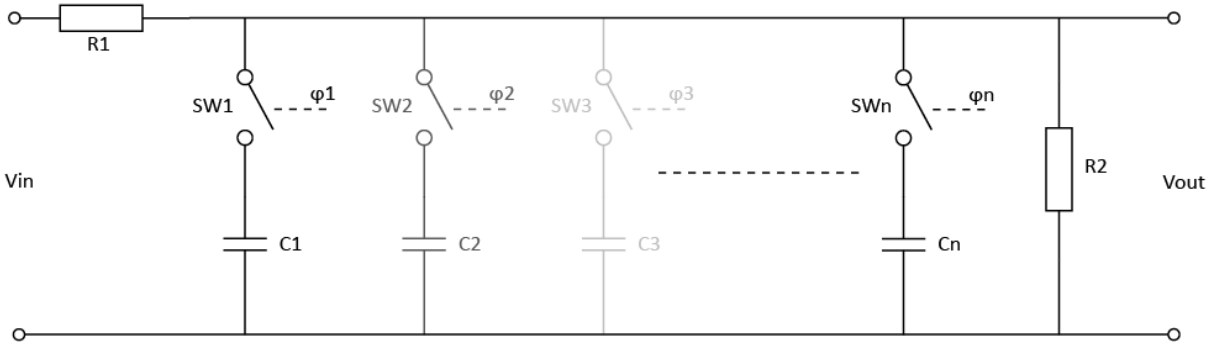


**Figure 4 - N-path filter used by Frischl [3]. This circuit is an efficient implementation of a RC N-path filter. R1 and the capacitors form the RC low-pass network. The switches act as both the input and output mixers.**

The filter shown in Figure 4 was used by Frischl to deduce several properties. This circuit is used by many authors when analysing N-path filters. Although some authors do not include R2, others generalise even further and allow any impedance at the in- and output [4]. The envelope of this filter shape is dependent on the number of clock phases. This is a result of the square mixing waveform. The frequency response is depicted in Figure 3. The comb-like transfer function is bounded between the dotted lines. The envelope of the comb-filter is given by equation **4.4**. This envelope is the result of the square-wave mixing function. The transfer of higher harmonics drops as the input frequency gets closer to $f_{clk}/D$. The envelope has a notch at multiples of $f_{clk}/D$.

$$Envelope(f) = \mathrm{sinc}^2\left(\pi D \cdot \frac{f}{f_{clk}}\right) \qquad 4.4$$

Using the paper of Frischl an analytical solution for the peak-to-valley ratio has been found when R2 has an infinite value (equation **4.5**). The solution is a function of the quality factor of the filter, Q, here defined by the ratio of the bandwidth and the centre frequency.

$$R_{p-v} = 10 \cdot \log_{10}\left(\frac{\cosh\left(\frac{\pi}{Q}\right) - 1}{\cosh\left(\frac{\pi}{Q}\right) + 1}\right)\ [dB] \qquad 4.5$$

The peak-to-valley ratio is directly related to the quality factor. This means that for a given Q, it is not possible to change to peak-to-valley ratio without changing the topology. The peak-to-valley ratio is dependent on the matching between the paths. Mismatch between the paths and clock phases will result in a smaller peak-to-valley ratio [5].

### Harmonic folding

Higher harmonics fold back as result of aliasing. They fold back into the mirrored spectrum; the Nth harmonic folds back to DC, the N-1th harmonic onto the fundamental, etcetera. This behaviour is problematic if it is not possible to filter the N-1th harmonic from the input. This is the case for a small N or a very wide input band. Strong signals at N-1th harmonic will corrupt the desired signal. The folding is dependent only on the number of phases, not the duty cycle nor the specific topology of the stages. When a suppression of 40dB is required for folders, a filter of 2$^{nd}$ order (20dB/decade) requires at least a decade (11 phases), to filter out the unwanted signals.

## 4.3 Aim of this thesis

The transfer and folding of higher harmonics is undesired. The aim of this thesis is to provide realisable options that remove these effects. In order to provide a clear focus several constraints are used. These constraints result in a loss of generality meaning that there may be other solutions or optimisations possible. For all simulations of solutions a 10-phase filter with a bandwidth of $10MHz$ and a centre frequency of $1GHz$ is used. This number of phases is chosen to be low enough to be realisable but high enough to remove undesired effects such as phase sensitivity at the input. The UMC65LL (65nm low leakage) process is used to provide a reference about which component values are realistic. Simulations were only done at circuit level. Layout and fabrication was not possible within the time constraints.

It is desirable for the filter to be passive: only passive components and switches can be used. Active components introduce additional noise and power consumption, although it is not ruled out that better overall performance may be achieved using active components. Filtering is preferably done as soon as possible in the receiver chain as to limit the large signals from strong blockers. The filter will be designed to be placed directly behind a 50Ω antenna. Large components are often desirable. Large capacitors are typically required for low noise. Large switches are beneficial as their lower resistance has less effect on the functionality of the circuit. As a layout will not be made a limit to the total area cannot be used. A set of guidelines is used to provide limits. For a band-pass filter with a bandwidth of 10MHz, the total capacitance must be below 1nF.

The power consumption should be below 50mW for a centre frequency of 1GHz. This figure does not include power consumed by clock generators and other peripheral circuitry. This power consumption can be roughly coupled to the amount of transistors allowed. The power consumed by a single MOSFET can be estimated using equation **4.6**.

$$P_{sw} = C_{gs} \cdot {V_{gs}}^2 \cdot f_{clk} \qquad 4.6$$

Large MOSFETS need additional transistors to provide the current required to switch them. It is assumed that these driving transistors consume power equal to that of the main switches. The swing at the gate is assumed to be 1.2V. The total allowed capacitance is found using equation **4.7**.

$$C_{gs} = \frac{P_{sw}}{{V_{gs}}^2 \cdot f_{clk}} \cdot \frac{1}{2} = \frac{50 \cdot 10^{-3}}{1.2^2 \cdot 10^9} \cdot \frac{1}{2} = 17pF \qquad 4.7$$

From simulation it is determined that a minimum-length OSFET has a capacitance of $1.32fF/\mu m$ of width when the source and bulk are tied together. The total gate width is thus allows to be nearly $13 \cdot 10^3 \mu m$. A 10 stage filter can thus use $1.3 \cdot 10^3 \mu m$ of switches per path.

# 5 Filter paths

An endless amount of variations are possible when designing the filter path. There is a wide choice of low-pass filters available of which two options are explored in this thesis. The first is a simple resistor-capacitor (RC) filter and the second is based on the switched capacitor (SC) technique.

## 5.1 RC filter

The RC N-path filter was described in chapter 4. This filter allows for a constant bandwidth set by the RC time constant. This circuit is limited in its performance. Large capacitors require a lot of area while large resistors in the signal path add a lot of noise. The bandwidth is dependent on the absolute value of the components. This is problematic as the spreads in component values in modern technologies can be very large. The bandwidth must thus either be tuneable after production or wide enough to cover any process corners. The baseband filter is shown in Figure 5.

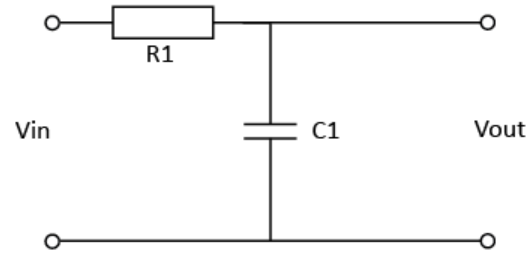


**Figure 5 - RC low-pass filter.**

### Filter path

In order to create a filter path, two mixers have to be added. Figure 6 shows the simplest case in which the mixers are two switches. The switches are driven by a square-wave with $1/N$ duty cycle.

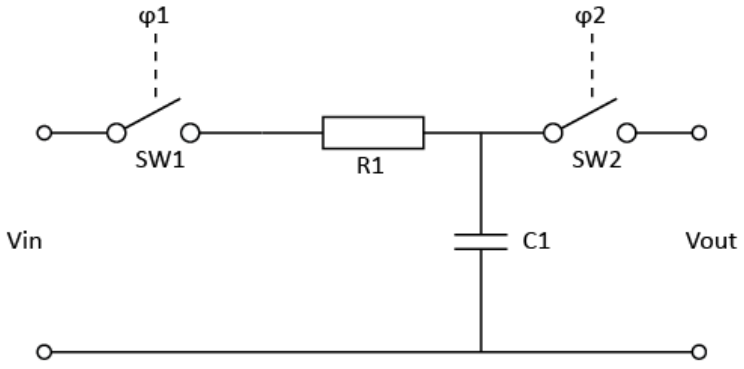


**Figure 6 – RC path. The phases $\phi_1$ and $\phi_2$ are $180^\circ$ apart.**

The time domain functioning of this filter is as follows. The RC filter has a much higher time-constant than the switch on-time. This means that the voltage on the capacitor cannot keep up with the input but will instead contain the average voltage of the input during the time the switch is on. The output for an ten filter is shown in Figure 7. The averaging results in loss as some signal energy is lost in the process. The loss of signal is given by equation **4.4**. As can be deduced from the equation, the loss decreases for a smaller duty cycle.

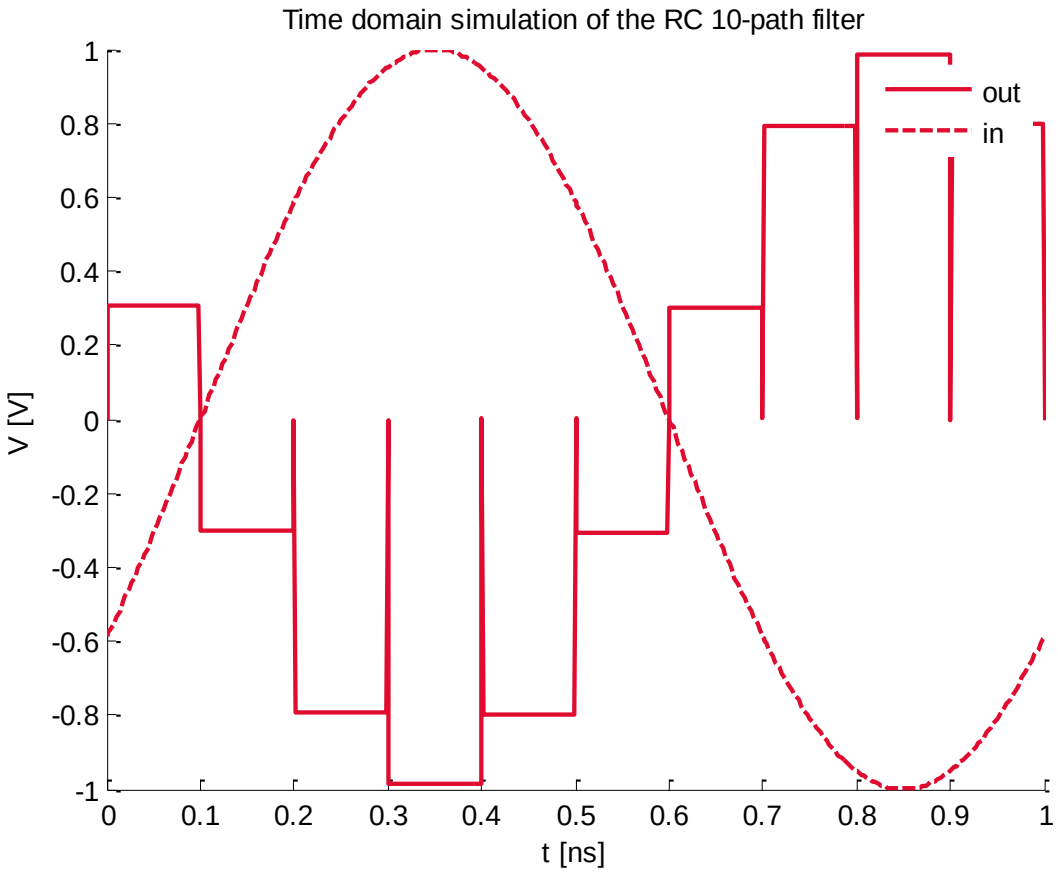


**Figure 7 - Time domain simulation of the in- and output of the RC filter. The output is inverted as the input and output clock phases are $180°$ apart.**

### Effect of switch resistance

The switch resistance of the first switch just adds to the total resistance of the filter. The only critical point is that the resistances should match between stages or the ultimate rejection will be less. The switch resistance may actually replace the resistor. This allows for a smaller switch with all the advantages that it brings such as more relaxed drive requirements and higher speed. The second switch is in series with the signal path and will add noise. Its value should be low compared to the source resistance to limit its noise contribution.

### Noise performance

The performance figure used for filters is the noise figure. The noise figure is defined by equation **5.1**

$$NF = 10 \cdot \log_{10} \frac{SNR_{out}}{SNR_{in}} \; [dB] \qquad 5.1$$

The noise figure represents the amount of noise the circuit adds compared to the input. In the case of a linear circuit, when the circuit adds no noise, the minimum noise figure of 0 is obtained. This is not true for non-linear circuits as noise from other frequencies might be folded onto the desired signal. When the switch resistance is very low, the noise is generated by the resistor from the RC low-pass filter. This resistor both includes R1 (as in Figure 6) and the source resistance. The minimum noise figure can be reached by choosing the value of R1 equal to zero. This makes the source

resistance the only noise source. For low-noise operation, the resistances in the filter should be chosen as low as possible.

### Limits on component values

The resistor of the RC filter cannot be smaller than $50\Omega$ as this is the source impedance. This limits the maximum value of the capacitor. For a 10 phase filter with non-overlapping clocks, the duty cycle is 0.1. Calculation of the maximum capacitor size using equation **4.3** results in a value of $63.5pF$. This is below the maximum of 100pF set in section 4.3.

## 5.2 SC filter

The resistor in the RC filter can be replaced by a switched capacitor circuit. This circuit is shown in Figure 8. A capacitor with two switches will show behaviour of a resistor at baseband when the switching frequency is well above the signal frequency. This is the case for a high-Q N-path filter and thus this technique can be used. The effective resistance seen is given in equation **5.2**.

$$R_{eq} = \frac{1}{f_{clk} \cdot C1} \qquad 5.2$$

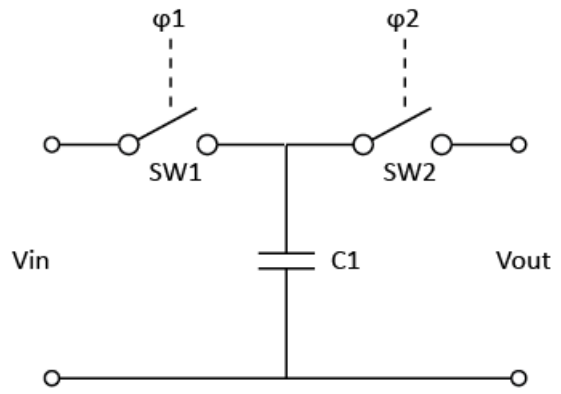


**Figure 8 - A switched-capacitor resistor.**

### Bandwidth

Combining this 'resistor' with a capacitor results in the low-pass filter shown in Figure 9. This filter has a bandwidth given by equation **5.3**.

$$BW_{low-pass} = \frac{f_{clk}}{2\pi} \cdot \frac{C1}{C2} \qquad 5.3$$

The bandwidth is the result of a ratio of two capacitors which can be made more accurate in CMOS than the absolute value of a resistor and capacitor. Since the bandwidth is a linearly dependent on the clock frequency, the resulting filter has a constant-Q, this in contrast to the constant bandwidth of the RC filter.

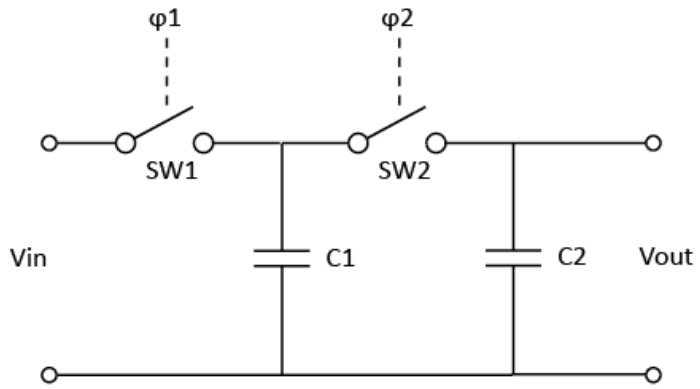


**Figure 9 - A switched-capacitor low-pass filter.**

### Filter path

The low-pass SC filter can be combined with two additional switches to form a path for an N-path filter just like the RC filter. As the input of the SC filter already contains a switch, the addition of another switch is not required. The actual path has only one additional switch at the output. This is shown in Figure 10.

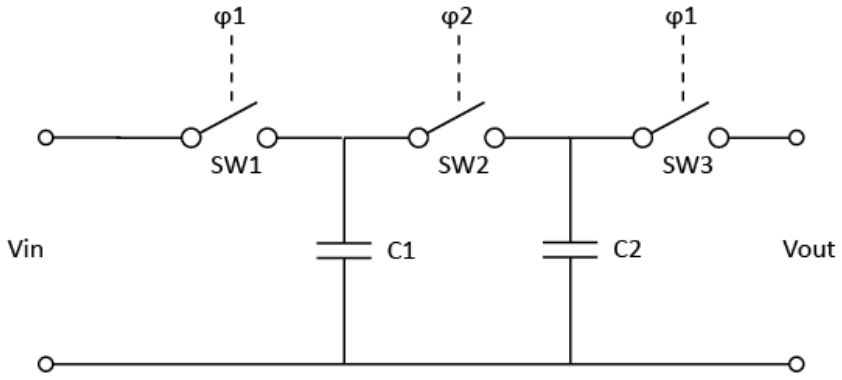


**Figure 10 – Single SC path. The phases $\phi_1$ and $\phi_2$ are $180°$ apart.**

The time domain behaviour of the SC filter is different from the RC filter. As the time constant of the input capacitor is much lower than the duration of the switch on-time, the input signal is sampled. The output is shown in Figure 11. The bandwidth is twice the baseband bandwidth and given by equation **5.5**.

$$BW_{band-pass} = \frac{f_{clk}}{\pi} \cdot \frac{C1}{C2} \qquad 5.4$$

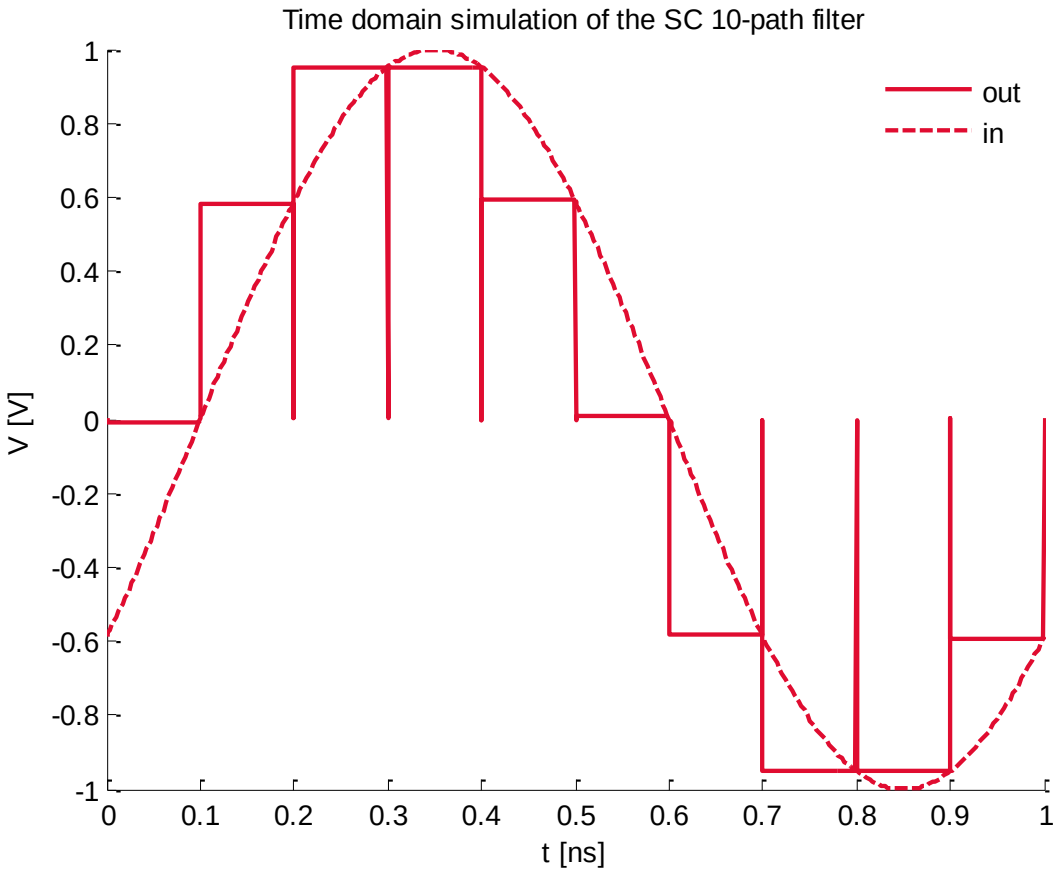


**Figure 11 - Time domain simulation of the in- and output of the SC filter.**

### Effect of switch resistance

Ideally, the switches should have zero resistance. Finite resistances will limit the bandwidth of the filter. The time constant of the switch/ source resistance and C1 should be much smaller than $T/N$ in order to not be bandwidth-limiting (equation **5.5**). As the source resistance is fixed, even for zero switch resistance, the value of C1 has an upper limit.

$$2\pi R_{source} C1 \ll T \qquad 5.5$$

Solving equation **5.5** for a source resistance of $50\Omega$ and a period of $1ns$ results in equation **5.6**.

$$C1 \ll \pi\ [pF] \qquad 5.6$$

This upper limit directly places an upper limit to the value of C2 as the target bandwidth is 10MHz. Rewriting equation **5.3** results in equation **5.7**.

$$C2 = \frac{f_{clk}}{\pi} \cdot \frac{C1}{BW} \qquad 5.7$$

Combining equation **5.6** with equation **5.7** results in equation **5.8** which gives the upper limit for C2.

$$C2 \ll \frac{f_{clk}}{BW}\ [pF] \qquad 5.8$$

For the desired bandwidth of $10MHz$ at $1GHz$, the value of C2 should be much lower than $100pF$.

### Noise performance

Any noise in the SC filter is added through the switch resistances. A zero switch resistance results in a NF of 0 if no noise is folded into the fundamental from other frequencies. The switch resistances should therefore be chosen to be as low as possible.

# 6 Harmonic folding

Mixing with square waves results in the folding of higher harmonics into the fundamental. The N-path topology rejects this folding to a large extent. An N-path filter will fold harmonics k·N-1 and k·N+1 ($k \in \mathbb{N}$) into the desired signal at the fundamental harmonic. In order to push out the first harmonic that folds back N must be increased, i.e. more clock phases must be used. Non-overlapping clock phases (Figure 12), as commonly used, are difficult to create at high frequency. They are typically generated using an N-times higher clock signal which is then brought to the desired frequency using logic ensuring that the phases are non-overlapping. A large N thus requires very high clock frequencies which are often not practical.

## 6.1 Overlapping clocks

Which harmonic folds back is a property of the number of clock phases, not the duty cycle of the clock. This raises the question whether overlapping clocks can be used. Overlapping clocks (Figure 13) are easily generated using ring oscillators. High speed ring oscillators with a high number of phases are already demonstrated at high frequencies [6]. Many ring oscillators do however produce a lot of jitter. The effect of jitter is not a consideration in this thesis. Most ring oscillators produce 50% duty cycle clocks but by using logic the duty cycle can be reduced. Mathematical models focus on describing filters with non-overlapping clocks and thus no mathematical basis exists for the use of overlapping clocks [4] [5].

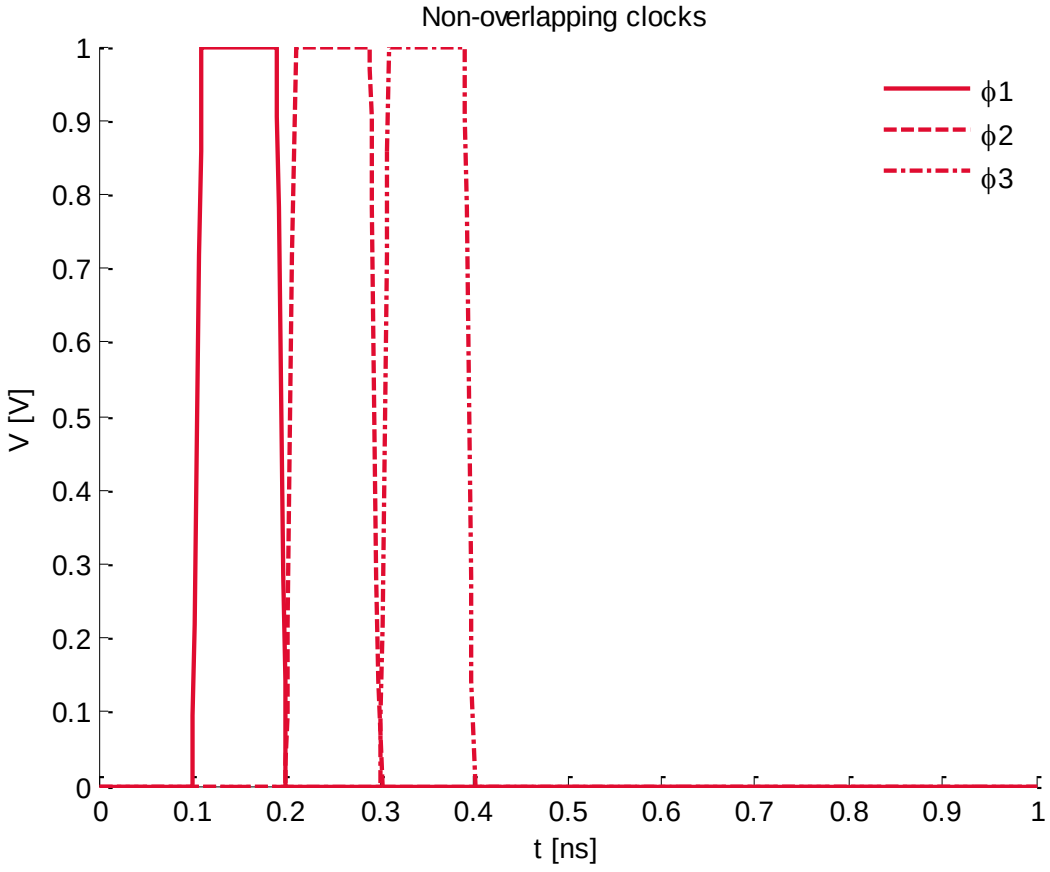


**Figure 12 - Non-overlapping clocks, the two clock phases are never high at the same time. Only three of the 10 clock phases are shown for reasons of clarity.**

Increasing the duty cycle beyond $1/N$ results in several problems. As multiple paths are connected to the in- and output node, they might interact. This is clearly a problem when the summing function is done by connecting all outputs to a single node as done by Frischl [3]. The overlapping clocks will short the output which results in strong attenuation.

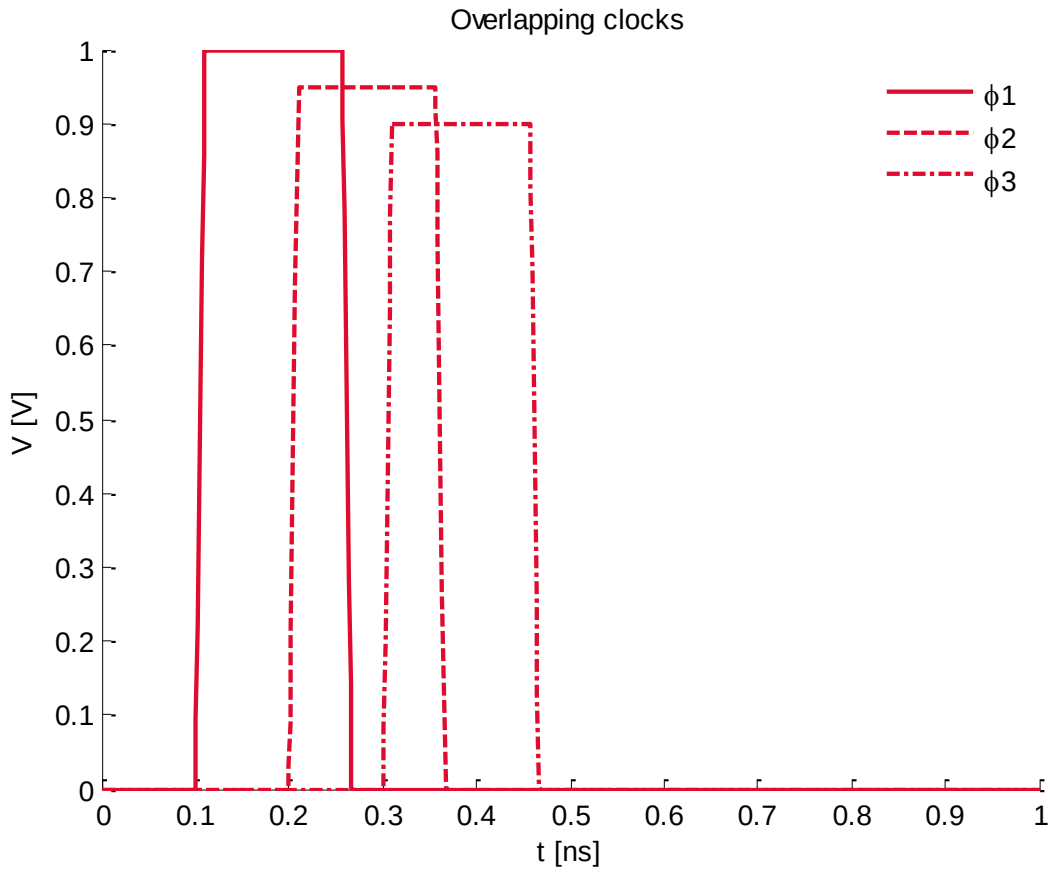


**Figure 13 - Overlapping clocks. The amplitudes of the second and third phase have been scaled for reasons of clarity.**

Another problem is the loss of time-constant multiplication. The time constant scales with the inverse of the duty cycle as given by equation **4.3**. When using non-overlapping clocks, increasing the number of paths does not require additional capacitance making scaling area-efficient. Fixing the duty cycle while increasing the number of clock phases would linearly increase the amount of area required.

### Ideal adder

The use of an ideal adder compared to shorting all output together results a problem in simulation as the signal at the input of the adder will not return to zero once the output switch opens. In order to ensure that this happens, a $1M\Omega$ noiseless resistor to ground was added at each output. The adder is implemented in VerilogA using the code given in chapter 14. The resulting topology is shown in Figure 14 for the case of a RC low-pass filter. The SC filter is identical expect that the circuit of Figure 10 is inserted between the dotted lines.

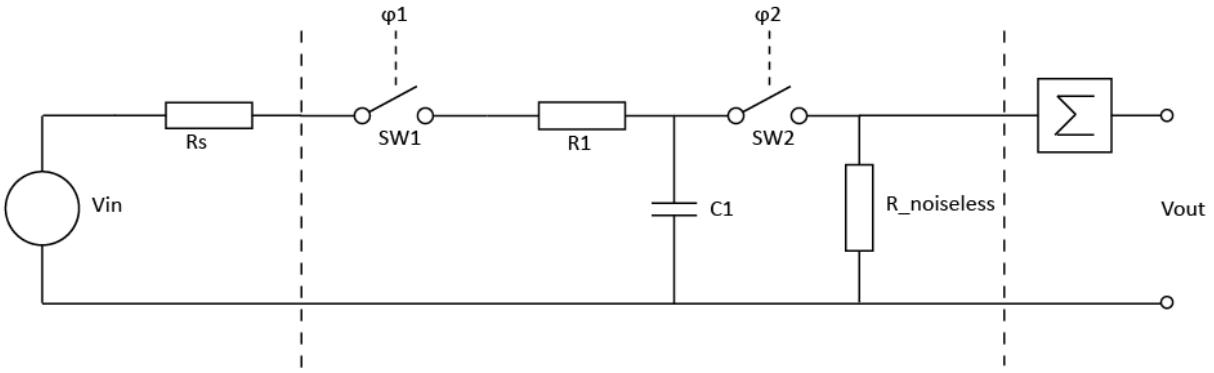


**Figure 14 - RC N-path using ideal adder. Only one path is shown between the dotted lines.**

## 6.2 Simulation of overlapping clocks

Two 10-path filters (RC and SC) were simulated to examine the effect of the overlapping clocks on the filter performance. When the source impedance is zero and the outputs of each path are added using an ideal adder, the overlapping clocks should not have any effect on the shape of the transfer function. The input signal is fixed by the source so no effect can be present there. The outputs are not connected to each other so no interaction can take place there. The only difference will be that the amplitude of the output changes as the addition of multiple signals results in gain. The transfer at $f_{clk}$ will be determined as a function of the duty cycle $50\Omega$ source impedance. For non-zero source impedance it is expected that the value of the resistor (or SC resistor) is of influence on the transfer. Strong attenuation is expected as R1 decreases (or C1 increases) with respect to the impedance of the source.

### Transfer versus duty cycle

The duty cycle was swept from 0.1 to 0.5. The baseband capacitance was chosen to be $10pF$ in order to make the value of R1 larger than Rs. No significant changes in folding behaviour and bandwidth were observed and are therefore not shown here. The transfer function shows that the notch in the envelope of the transfer function is a function of D, not N.

$$f_{notch} = \frac{f_{clk}}{D} \qquad 6.1$$

Figure 15 shows the transfer of a 10-path filter at 1GHz versus the duty cycle. In this plot, the source impedance is $50\Omega$ and the switch impedance is $0\Omega$. The zero switch impedance was chosen to eliminate the effect from the switch from the results. The graph shows that from a transfer point-of-view, it is beneficial to use overlapping clocks as the signal strength increases.

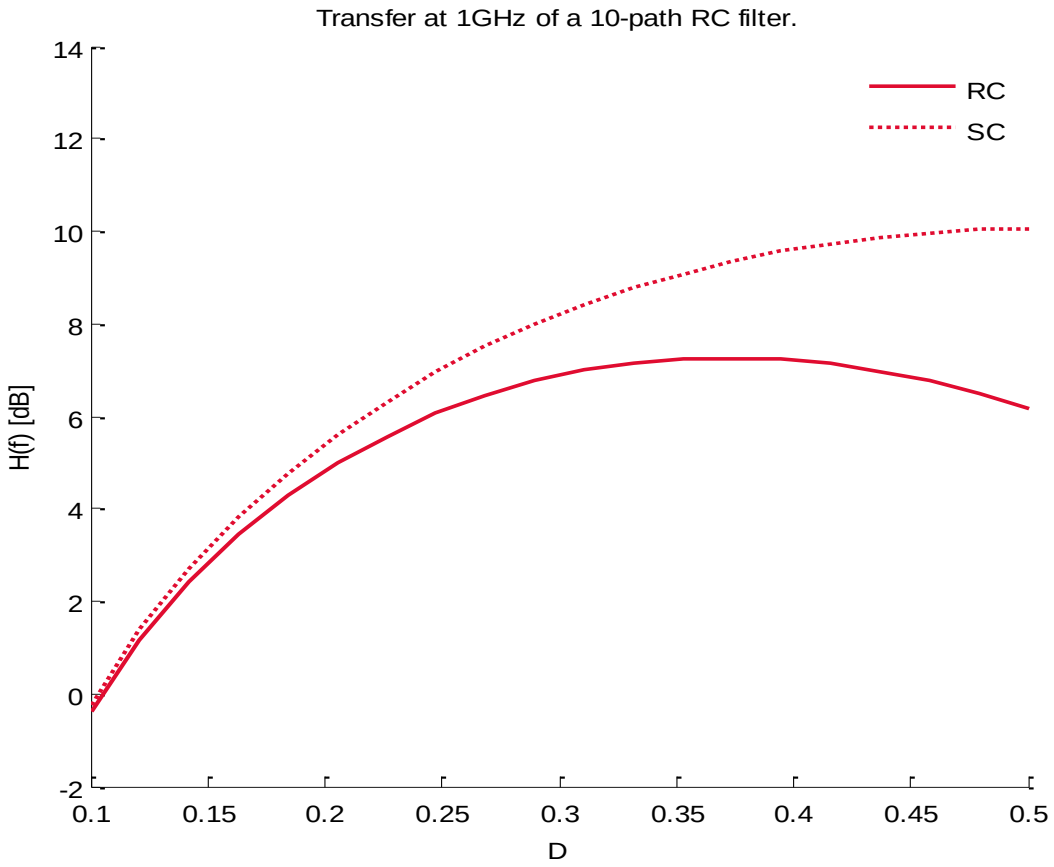


**Figure 15 - Transfer at 1GHz of a 10-path filter versus duty cycle. The bandwidth is kept constant at around 10MHz by scaling the (SC) resistance.**

# 7 Harmonic transfer

Mixing using simple switchers causes the transfer function to also pass higher harmonics. This is a result of the spectral content of the mixing function. This is illustrated in Figure 11 and has been explained in chapter 4.

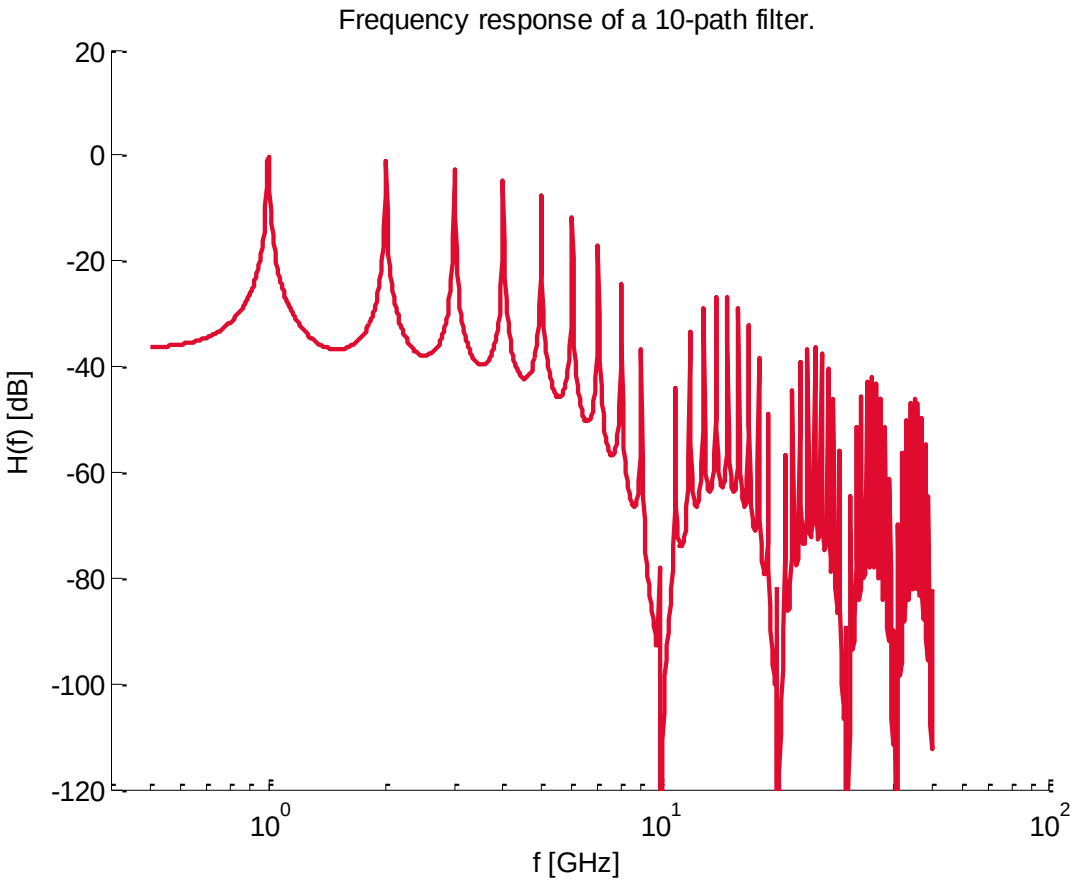


**Figure 16 – Harmonic transfer. The transfer function not only passes the desired fundamental but also higher harmonics.**

Harmonic transfer is undesired and in this chapter several methods of reducing the harmonic transfer are introduced. First the rejection of even harmonics is discussed followed by the rejection of specific harmonics and finally the rejection of all harmonics except$(k \cdot N) \pm 1$.

## 7.1 Rejection of even harmonics

The rejection of even order harmonics allows half of the harmonics to be removed in one go. The easiest option is to use a balanced circuit, as it will not allow any even harmonics to pass. Another option in the case of the switched capacitor circuit is to put the capacitor in series with the input signal. This option is used by Faruque [7] and effectively creates a balanced signal from a single-ended input. The requirement of a floating capacitor may be downside. Using a capacitor to generate the required negative voltage may be a benefit if a differential input signal is not available. The rejection of just even harmonics has been done before and is therefore not been considered here [8].

## 7.2 Rejection of specific uneven harmonics

The rejection of uneven harmonics is more problematic than even harmonics as they do not share a common divider larger than the fundamental harmonic. Uneven harmonics can have common dividers between them such as 3 and 9, allowing them to be removed together. Prime numbers do

not have this property and must thus be removed one-by-one. The first three uneven harmonics are all prime numbers. Rejection of harmonics can be done at baseband, by having interaction between the baseband voltages or at RF by combining the outputs in a smart way. Since all information is available both in baseband and at RF, both allow the rejection of harmonics.

The baseband capacitors effectively store the time-domain waveform. By introducing interaction between the capacitors, certain waveforms will not be able to exist. Even harmonics may for instance be supressed by placing a resistor between the first and the $\left(\frac{N}{2}+1\right)th$ capacitor. Uneven harmonics will have equal voltages at these nodes but even harmonics have opposite voltages which will cancel each other. The same works for uneven harmonics. When the 1st and the 3rd capacitor of a 6-path filter are connected using a resistor, the third harmonic is suppressed. The downside of this method is that multiple harmonics cannot effectively be removed together as each interaction interferes with the others. A choice must thus be made for a single uneven harmonic to reject.

RF rejection is possible by connecting baseband capacitors to multiple clock phases. The effect is similar to the situation described in the paragraph above for baseband rejection; differences in the waveforms of different frequencies are exploited to reject them. The same problem applies here as well as rejection of multiple harmonics is problematic. As rejection of all harmonics is desired this option has not been investigated further.

## 7.3 Harmonic rejection mixer

The ideal sine-wave mixer can be emulated by making a staircase-approximation using weighted square-wave multipliers. More phases can be used to make the approximation the better. Due to mismatch limitations there will be a point where the effect of mismatch dominates the behaviour instead of the weighing function. Where this limit is located as not been researched. The baseband capacitors effectively store a discrete-time representation of the input signal. The ideal coefficients can be found by applying the inverse Fourier-transform to a discrete spectrum of length N. This spectrum should only contain the fundamental harmonic. For ten phases this works as follows:

$$F(s) = [0\ 1\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0] \qquad 7.1$$

A complex filter would be required to implement the resulting filter coefficients. In order to limit complexity the choice was made to only use the real components as shown in equation **7.2**. The coefficients are multiplied by N to normalise the values such that the peak is equal to one.

$$F[n] = N \cdot \mathcal{R}\{\mathcal{F}^{-1}[F(s)]\} \qquad 7.2$$

The resulting spectrum contains the 9th harmonic and is given by equation **7.3**.As the spectrum is periodical, the harmonic rejection mixer will pass the 9th, the 11th, the 19th and so on, harmonics.

$$F(s) = [0\ 1\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1] \qquad 7.3$$

The coefficients from equation **7.2** are the weighing functions of the different paths. Figure 17 shows the coefficients of F[n] for a 10-phase filter. As active components are excluded from this research the weighing must be done using passive components. The easiest option is to attenuate signals for the coefficients smaller than one. Resistive dividers are very noisy. They also introduce a frequency-dependency to the filter making the filter have differently for different centre frequencies. It is

possible to scale the resistors of the RC filter to match the coefficients. This is shown in Figure 18. When using a single harmonic rejection mixer, the total resistance should be taken into account when scaling the resistors. The scaled resistors should be equal to $(R1 + R_s)/F[n]$. However, this is not true when multiple paths are connected to the input. When harmonic rejection mixers are used for each path, N paths will be connected to the input at all times. The paths will interact and load the input, resulting in attenuation of the input signal. As the connected phases are both opposite in phase and signal (for even N), the shape of the input signal is not changed and the source impedance does not have to be taken into account. This is beneficial as the absolute value of the source impedance if often not well-defined. The amount of attenuation is dependent on the ratio of $R_s$ and $R_1$. When $R_1$ is much larger than $R_s$ there will be no attenuation. When $R_s$ is much larger than $R_1$, there will be no signal. The exact attenuation is dependent on the coefficients chosen in the filter paths, the duty cycle and the value of $R_1$.

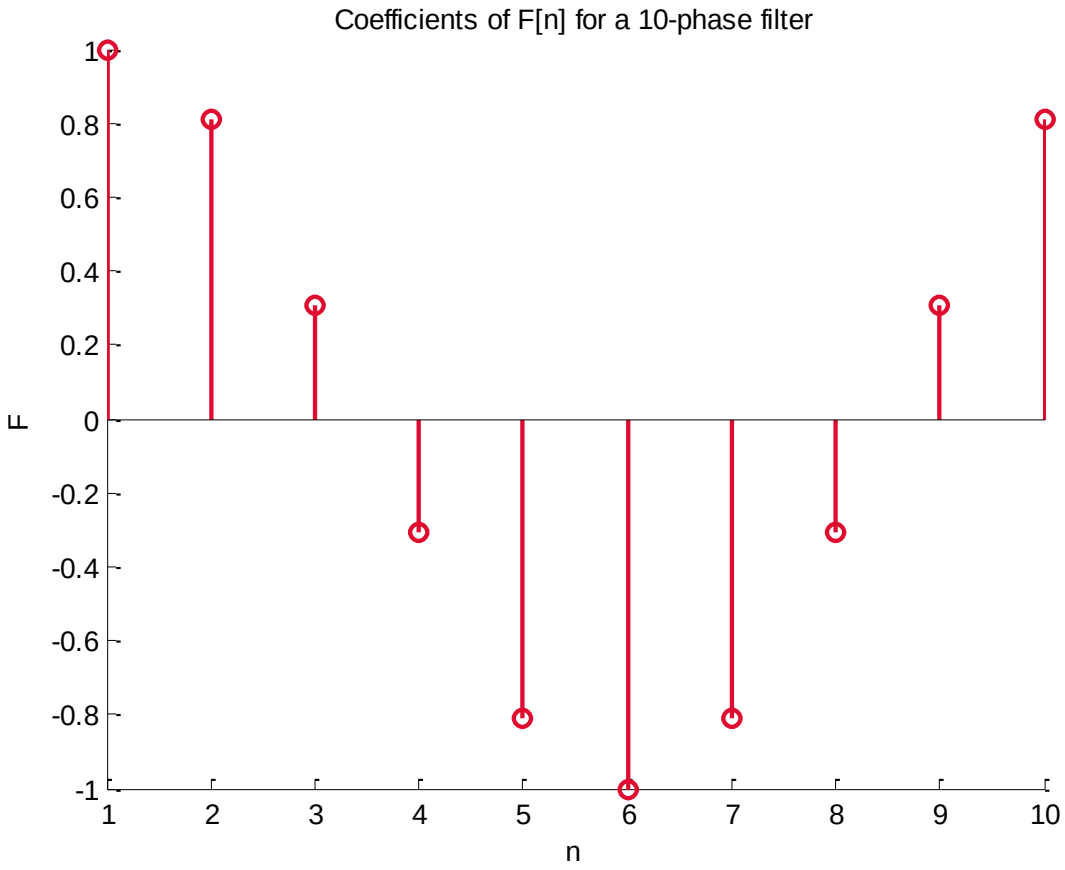


**Figure 17 – Coefficients of $F[n]$ for a 10-phase filter, calculated using equation 7.2.**

The scaling of the resistor values works for any impedance and the same technique can also be applied to the SC filter. This is shown in Figure 19. Due to the fact that the impedance of capacitors scales with the inverse of the component value, the capacitors must be multiplied by the coefficients instead of divided.

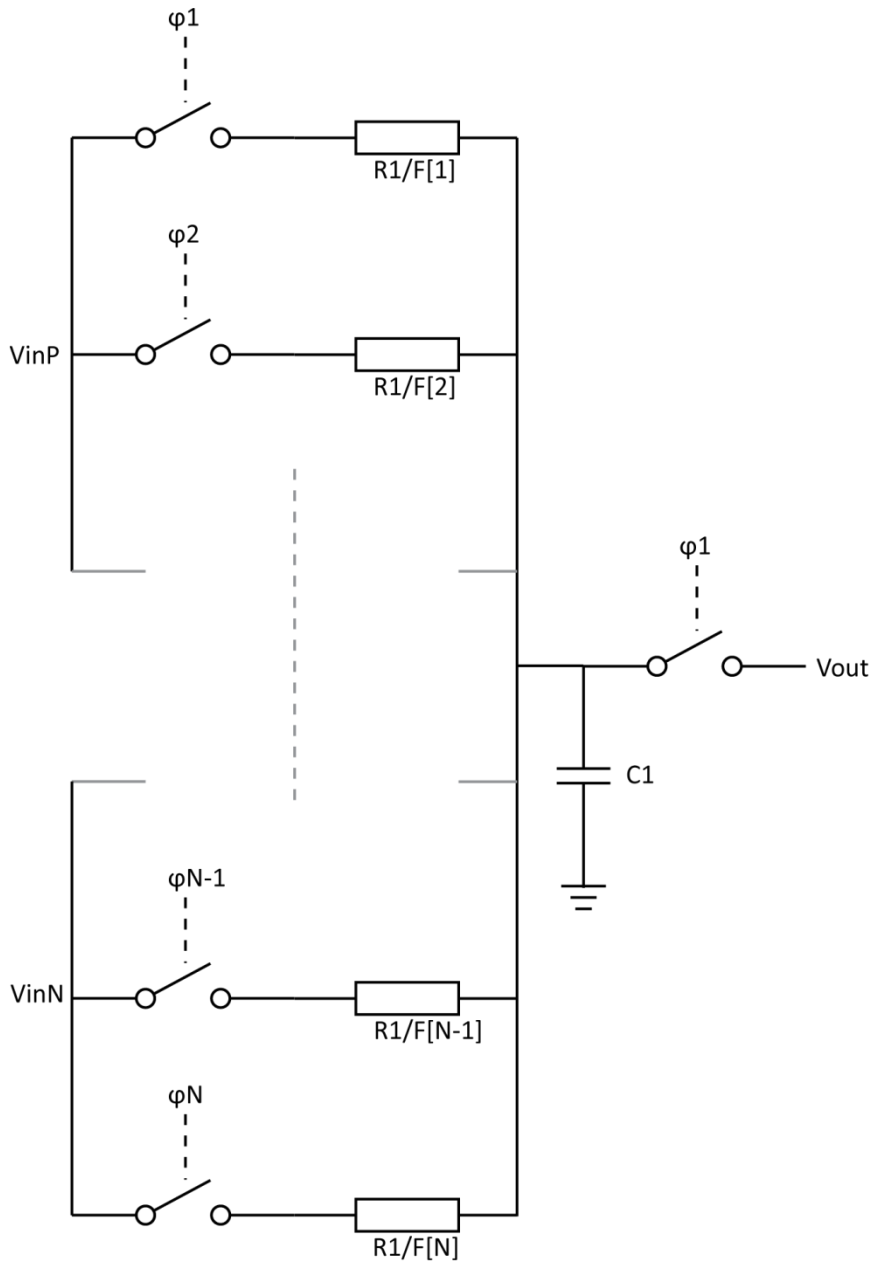


**Figure 18 - RC harmonic rejection mixer using scaled resistors to achieve the desired mixing function. The coefficients $F[n]$ result from equation 7.2. The inputs VinP and VinN represent the differential input voltage.**

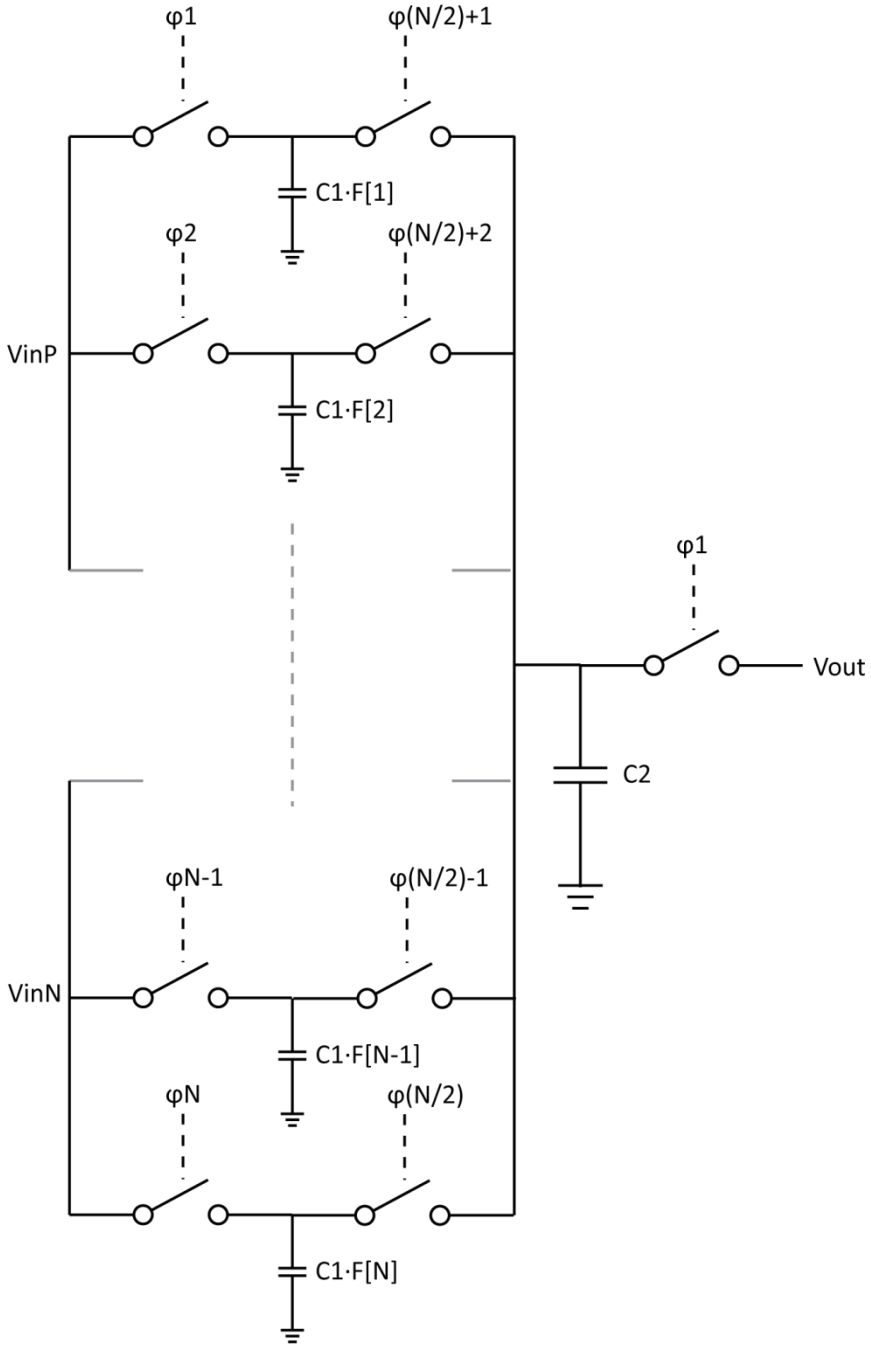


**Figure 19 - SC harmonic rejection mixer using scaled capacitors to achieve the desired mixing function. The coefficients $F[n]$ result from equation 7.2. The inputs VinP and VinN represent the differential input voltage.**

Half of the coefficients (for even N) are negative. As resistors with a negative value do not exist, it is required to use the inverted signal. This most straight-forward way is to use a differential input signal. This signal can be obtained using a differential antenna or a BalUn. A BalUn converts a balanced (differential) to an unbalanced (single ended) signal, or the other way around as is desired here. The BalUn is shown in Figure 20. It consists of two transformers with a $\sqrt{2}:1$ ratio. This ratio is chosen such that the impedances at both sides of the transformer match with respect to ground.

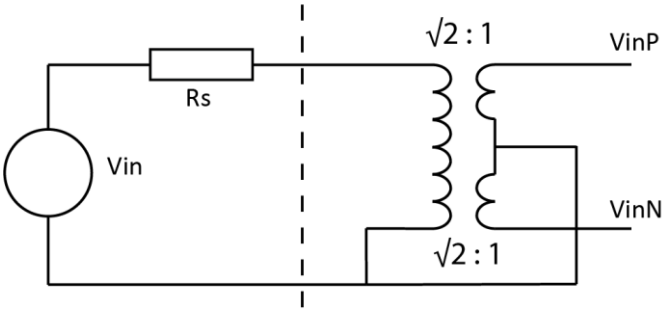


**Figure 20 – BalUn with 1:1 impedance transformation.**

The bandwidth when using harmonic rejection mixers is higher than the bandwidth of a filter with square-wave mixers. The effective duty cycle is increased from 1/N to 1. However, the bandwidth is not equal in each path. Addition of the bandwidth of the different paths results in the total bandwidth.

The 'bandwidth multiplication factor' or $F_{bandwidth}$ is used to denote the increase in bandwidth when using harmonic rejection mixers compared to simple square-wave mixers. This factor is the same if the RC filter is replaced by a SC filter and given by equation **7.4**.

$$F_{bandwidth} = N \cdot \sum_{n=1}^{N} |F[n]| \qquad 7.4$$

This function is dependent on the phase of $F[n]$. For an input phase of 0 the factor is shown in Figure 21 as a function of the number of clock phases. Some input phases show a lower factor than others, especially at low, even, N. This is due to the fact that even coefficients may contain two zeros (one for uneven). A zero results in an infinite resistance with zero bandwidth. This decreases the duty cycle from 1 to $\frac{N-2}{N}$. The resistance of the other paths is changed at the same time and the decrease in duty cycle is less than the decrease in duty cycle. It does however always save area as less components are required.

The increase in bandwidth is problematic for the noise performance. The increase in bandwidth must be compensated for by additional resistance (assuming that the maximum area is already used for the capacitors) resulting in a higher noise figure.

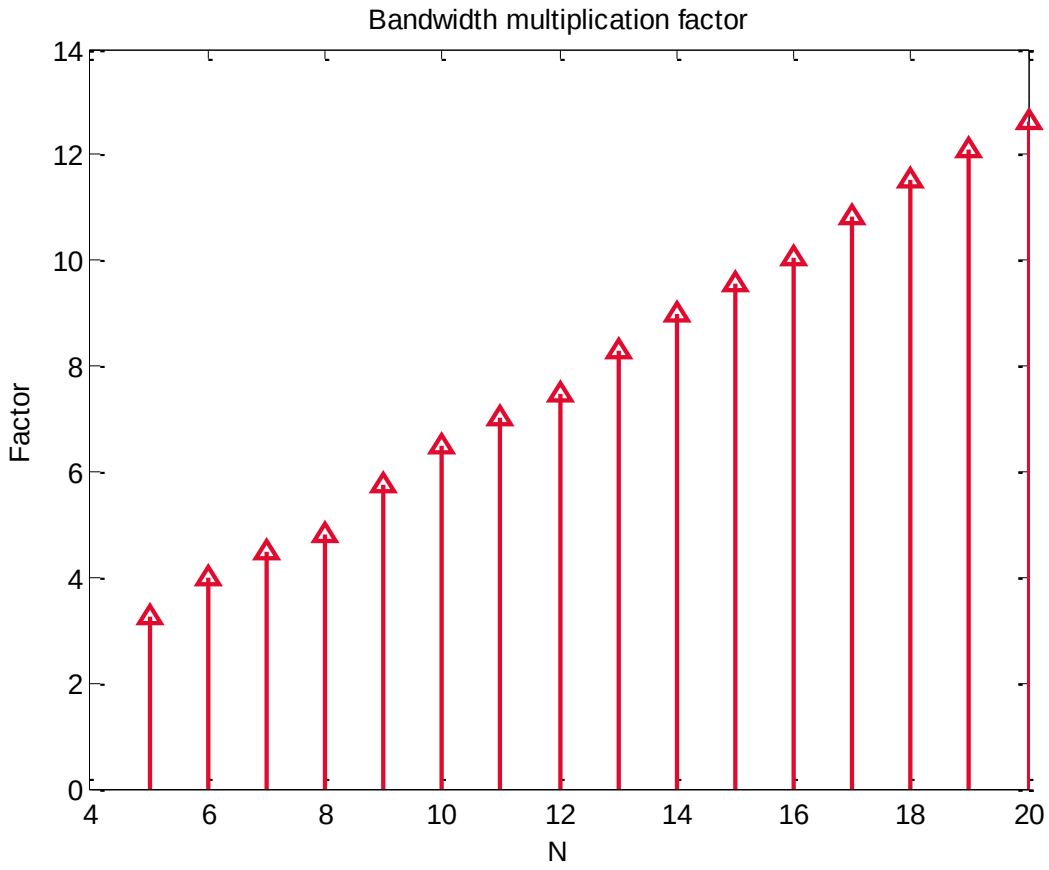


**Figure 21 - Bandwidth multiplication factor versus N.**

## 7.4 Simulation of harmonic rejection mixers

The RC and SC filters have been simulated using harmonic rejection mixers. The frequency response was determined as well as the folding behaviour and the noise figure. For the RC filter the effect of the baseband capacitor was simulated. For the SC filter both the effect of the switch resistance and the effect of the baseband capacitor was simulated. In all cases the bandwidth was kept constant to around $10MHz$ by scaling the (SC) resistors.

### RC Harmonic rejection mixer

The RC network was simulated using a baseband capacitance of $60pF$ as found in section 5.1 . The switch resistance was chosen at the smallest value allowed by the constraints set in paragraph 4.3. With a total of 110 switches in the filter, each switch has a minimum value of 4.2Ω. The transfer function can be found in Figure 22. It shows that the transfer function has the expected shape; all harmonics up to the 9th have been supressed.

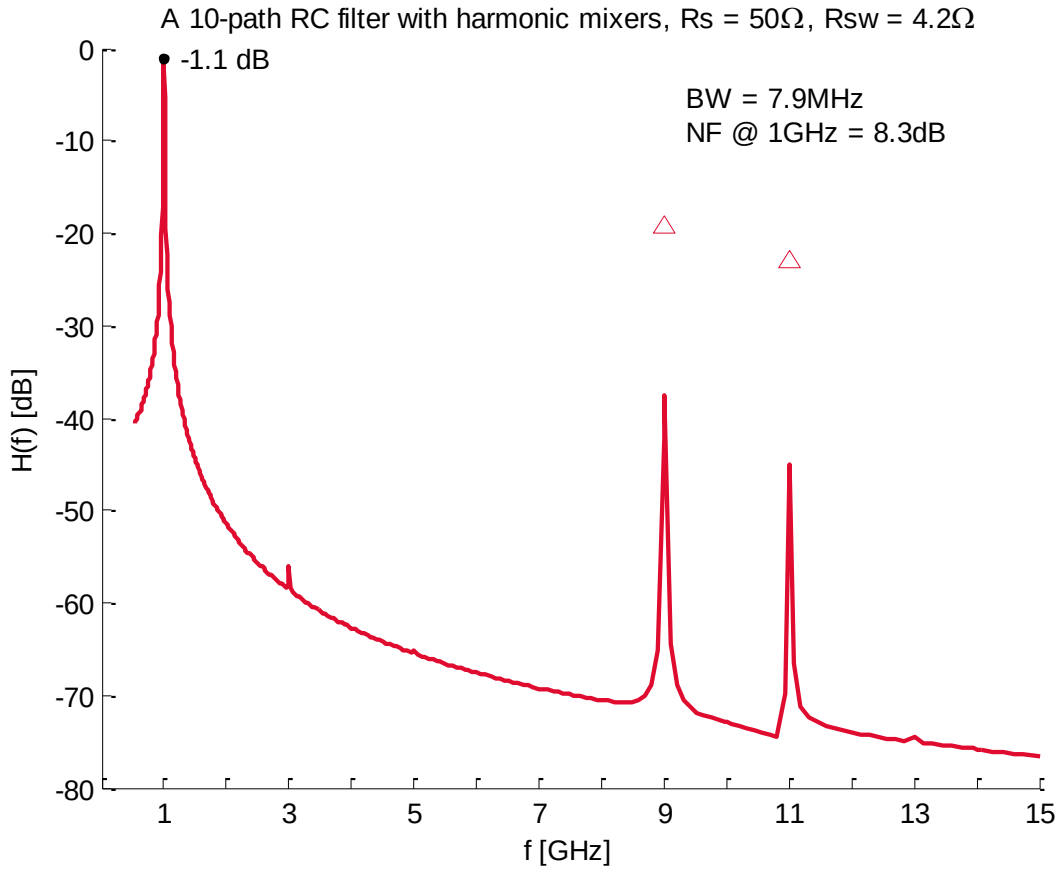


**Figure 22 - Properties of a 10-path RC filter. The line represents the transfer function. The triangles are the strengths of folders. Folders below -100dB are not shown.**

The triangles show the strength of the folder back into the fundamental. Folders below $100dB$ are not depicted. The filter's folding behaviour has not changed as only the 9th and 10th harmonic fold back with significant strength. This is expected as the folding behaviour is a function of the number of paths, not the properties of the individual paths. The filter does show significant losses and a high noise figure. This limits the applicability when used directly behind an antenna as the overall noise figure will be high.

The value of the baseband capacitor has been swept from 10 to $100pF$. The bandwidth is kept constant at $10MHz$ so the value of the resistors changes as well. The results can be seen in Figure 23. The transfer is not a strong function the baseband capacitance but the noise figure is, higher values for the capacitance result in lower noise figures.

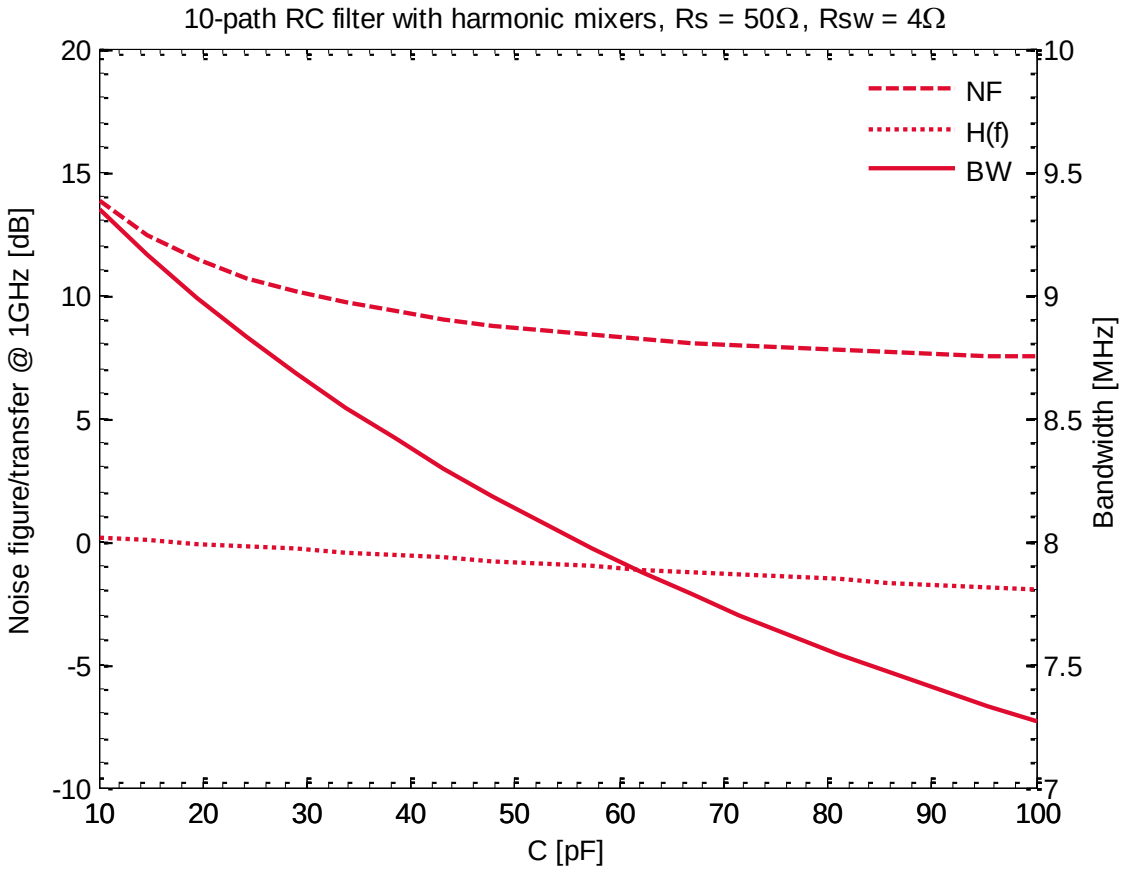


**Figure 23 – Transfer function and noise figure of a RC 10-path filter using harmonic rejection mixers as a function of the baseband capacitance.**

### SC Harmonic rejection mixer

Changing the value of C1 allows the harmonic rejection mixer to be implemented in a similar style as with the RC filter. The simulations that were performed on the RC filter were repeated for the SC filter. The switch resistance was chosen at the smallest value allowed by the constraints set in paragraph 4.3. With a total of 210 switches in the filter, each switch has a minimum value of 9.7Ω. Figure 24 shows the transfer function. The shape is roughly the same however, the harmonics are rejected a bit less. This is the result of the source resistance limiting the bandwidth a bit due to the RC time constant of $R_s$ and $C_1$. The loss has decreased while the noise figure has dropped significantly. A value of $60pF$ was used for $C_2$ which results in a large value for $C_1$. Lowering the value results in a smaller time constant and better matching. For the SC filter folders at 9 and $11GHz$ fold back stronger than in the case of the RC filter (-20dB vs -10dB). This is due the sampling nature of the SC filter. The strength with which harmonics fold back is stronger as ideal sampling is approached by decreasing the source and switch impedance.

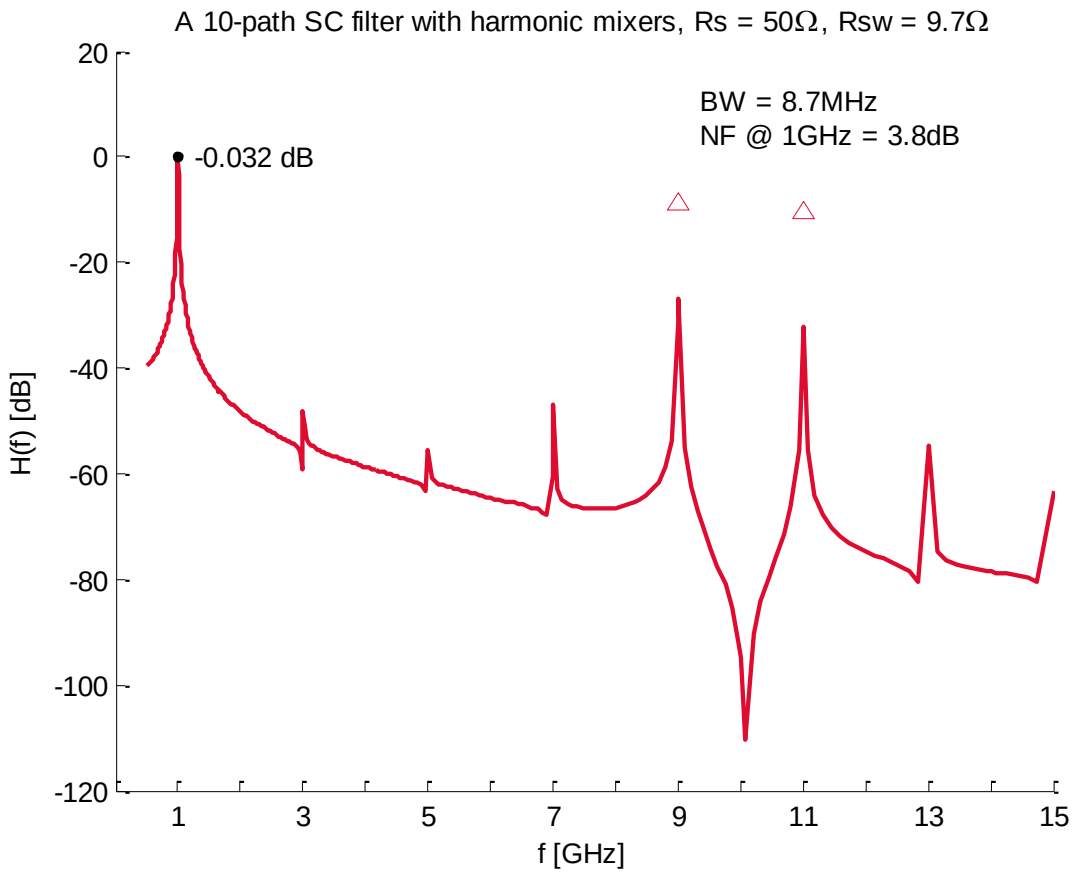


**Figure 24 – Properties of a 10-path SC filter. The line represents the transfer function. The triangles are the strengths of folders. Folders below -100dB are not shown.**

In order to explore the possibility of using smaller switches, the switch resistance was swept from 1 to$100\Omega$. The results are shown in Figure 25. It is clear that smaller switches degrade the performance of the filter as the noise figure goes up and the transfer goes down. This shows that the SC filter must have large switches for low-noise operation. Large switches will result in higher power consumption compared to the RC filter's smaller switches. If low-noise is not required for a certain application the RC filter might be a better option as the RC filter consumes less power for a given transfer function.

The effect of changing the size of the capacitors was also examined. Figure 26 shows the results. The bandwidth is kept constant at $10MHz$. The noise figure slightly drops at larger capacitances together with the transfer function. This shows that for a SC filter, the value of the baseband capacitor is less critical than for the RC filter.

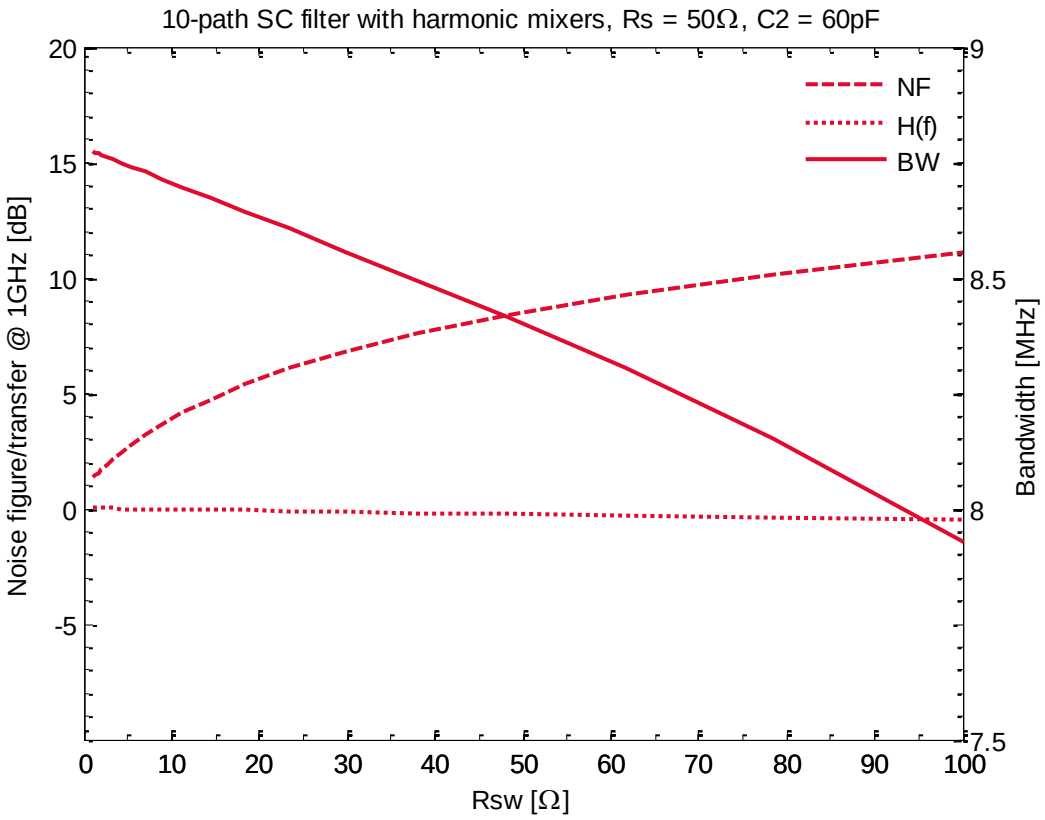


**Figure 25 - Transfer function and noise figure at 1GHz of a SC 10-path filter using harmonic rejection mixers as a function of the switch resistance.**

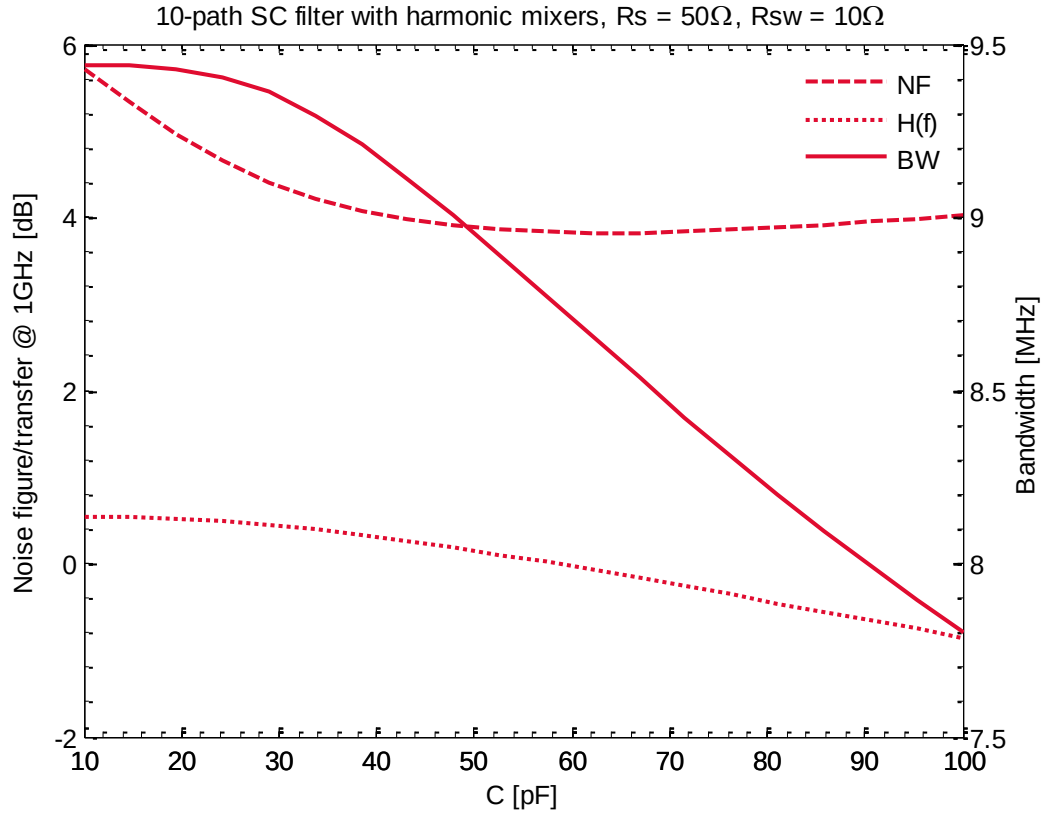


**Figure 26 - Transfer function, noise figure and bandwidth as a function of the capacitance value, for a aimed constant bandwidth of 10M.**

# 8 Addition of outputs

The output signals of each path must be added. The easiest way is shorting the output together but this only works for non-overlapping clocks. There are several ways to add analog signals. Among these are voltage addition and current addition. Voltages are difficult to add as voltages must be added in series. Voltage addition is therefore considered not to be an option. Currents are easier to add as the output nodes can be shorted together. As the output is in fact the voltage on the capacitor, a V-I conversion step is required. Whether an I-V conversion is required after summation is dependent on the circuit that follows after the filter.

## 8.1 V-I conversion

Passive V-I conversion can easily be achieved by the use of an impedance. Assuming that the current is sensed an ideal current sensor (zero input impedance), the impedance will pull the output to ground. The value of the impedance should thus be as high as possible to prevent loading of the filter which would result in loss.

## 8.2 I-V conversion

Converting a current into a voltage by passive means requires again an impedance. A current sensing element should have a very low input impedance. The transconductance of an impedance is dependent on the impedance value. This is problematic as the low input impedance conflicts with a high transconductance. A low transconductance results in signal attenuation which will increase the overall system noise.

## 8.3 Averaging

Another option is to connect all outputs together through a high impedance. The output will be the average of each path. For small overlaps, averaging might even be beneficial as it prevents strong peaks at the output during overlap. Averaging can be done by tying the outputs together using resistors. The resistors will then perform both the V-I and the I-V conversion. Resistors are very noisy when large values are used. Small values will create strong interaction between the baseband nodes causing attenuation.

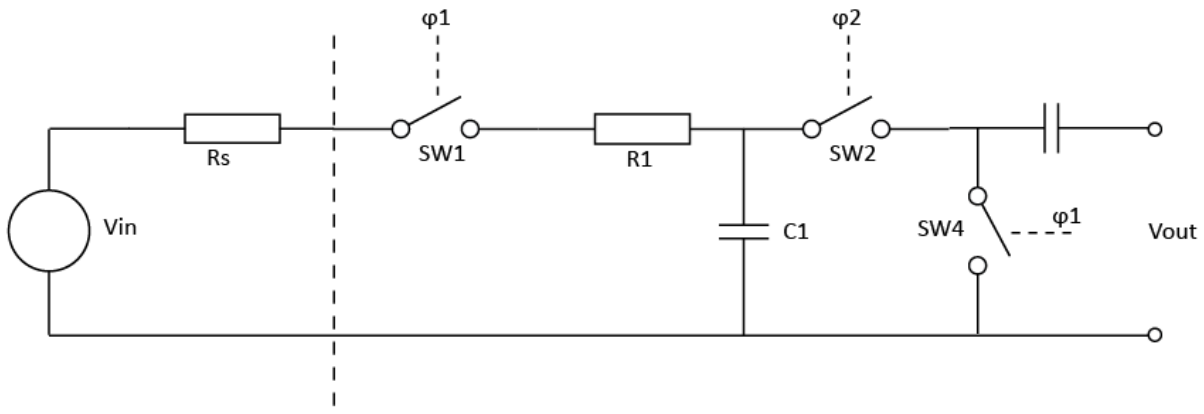


**Figure 27 - Capacitive adder for RC circuit**

As the output is AC, it is possible to use capacitors to perform the function of the resistors. The downside is that the effective impedance of the average is frequency-dependent. This can be solved by switching capacitors on and off depending on the centre frequency. Figure 27 shows the circuit

when this technique is used. The output each path is tied together. SW4 is required to return the output to zero when SW2 is off. SW2 and SW4 are each other's inverse.

### Value of the capacitor

The output capacitor should not load the baseband capacitor to prevent loss. A small value is therefore preferred. Too small a value will result in practical problems. The switches will be implemented using transistors which also have a capacitance. The output capacitor should be much larger than the capacitance of the switch. Another problem is that very high impedances will result in very high output impedance which can cause problems for subsequent circuits. To simulate the functionality of the capacitive averager, an impedance of ten times $R_1$ was chosen. Equation **8.1** gives the impedance of the output capacitor, $C_{out}$;

$$Z_{Cout} = 10 \cdot R_1 = \frac{1}{2\pi f_{clk} C_{out}} \qquad 8.1$$

This formula can be rewritten to equation **8.2** giving the value of $C_{out}$.as a function of $R_1$.

$$C_{out} = \frac{1}{20\pi f_{clk} R_1} \qquad 8.2$$

### Simulation

The circuit of Figure 27 was simulated using a value of $6pF$ for C1. The values for $R_1$ and thus $C_{out}$ are dependent on the duty cycle in order to keep the bandwidth at $10MHz$. Simulation of this circuit using the SC resistor resulted in the same functionality and is not shown here. The noise figure of the SC is lower but the transfer is equally low. The folding behaviour is not significantly changed when using capacitive averaging and the results of pxf simulations are not shown here.

Figure 28 shows the results of the simulations. The high noise figure is expected due to the choice of a small capacitor. Increasing the duty cycle does increase the noise figure but not too much. This is most likely due to the fact that the value of $R_1$ goes down as the duty cycle goes up. The bandwidth does change but only slightly and remains within 10% of the desired value of $10MHz$. The large downside of using capacitive averaging is the high loss. The simulation was also run with a source impedance of $0\Omega$, no significant changes in the loss and bandwidth were found, indicating that the losses are a result of the capacitive averager.

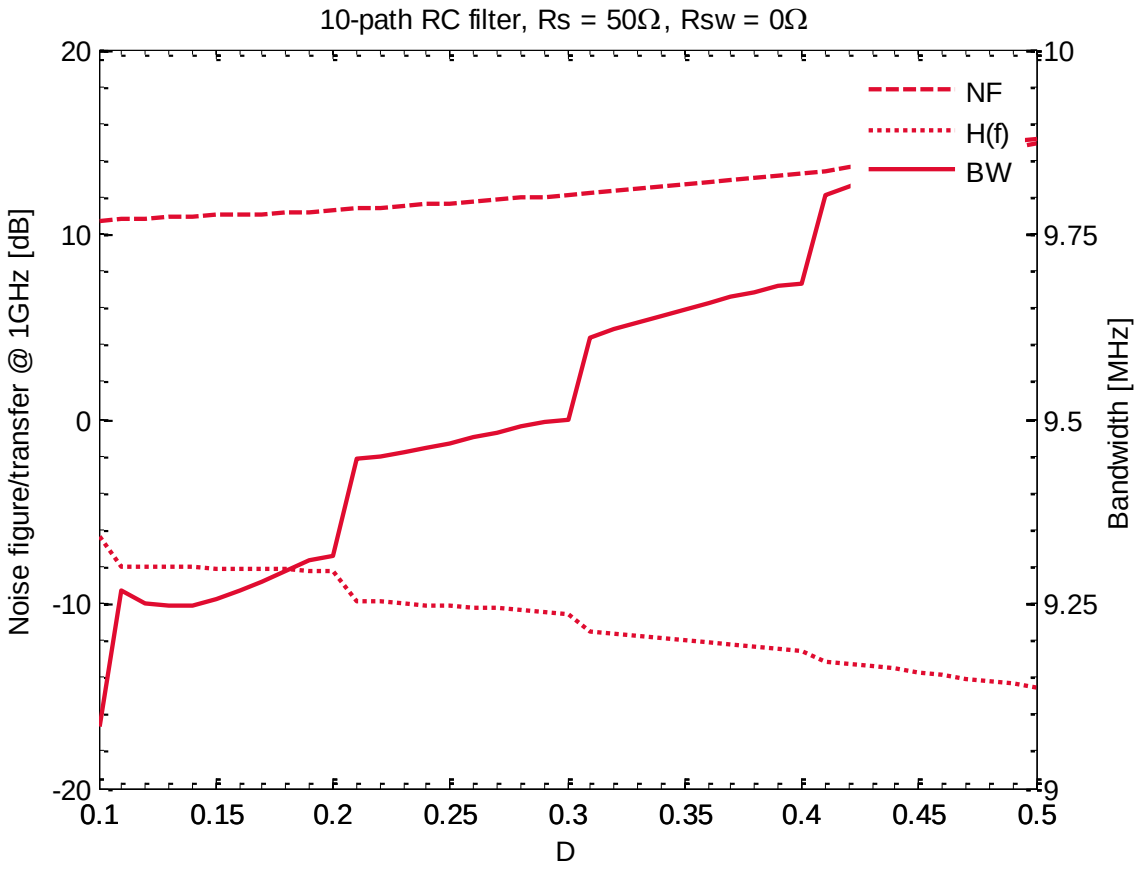


**Figure 28 - Simulation of a 10-path filter with capacitive averaging at the output.**

## 8.4 Active adder

The averaging of the output as described in the previous section introduces interaction between the paths introducing additional losses. This interaction can be removed by forcing the output to a constant voltage. This can be done by adding an opamp to create an adder. The schematic for this adder is shown in Figure 29. The voltages Vin[1] trough Vin[N] represent the voltages on the baseband capacitors. The number of inputs can easily be extended to any desired number. The opamp forces the common node at the inverting input to zero.

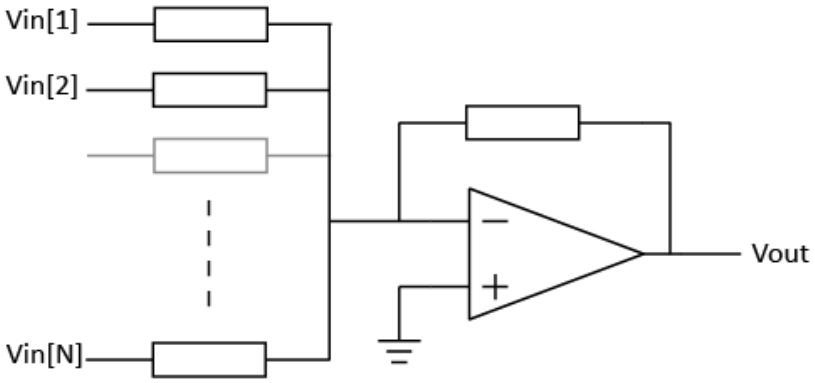


**Figure 29 - Opamp adder, the output is the negative sum of Vin[1] through Vin[N].**

If all impedances are equal the output voltage is given by equation **8.3**.

$$V_o = -(Va + Vb + Vc + Vd) \qquad 8.3$$

This addition results in the desired gain as shown in chapter 6. The circuit of Figure 29 was used in simulation with the capacitors from section 8.3 as the impedances. The opamp was implemented using a voltage controlled voltage source with a gain of $1^6$ and no bandwidth limitations. The shape of the transfer function is not influenced and thus not shown here. Figure 28 shows the bandwidth and both the noise figure and transfer at 1GHz as a function of the duty cycle. The results are similar to those found in chapter 6. As an LNA is usually required to amplify the received signal, it is assumed that the LNA can take the role of the opamp.

Addition can be done in many different ways of which the opamp adder is only one. As active circuits are not the focus of this thesis and the adder may be integrated with the LNA, the specific implementation of the adder is not further investigated.

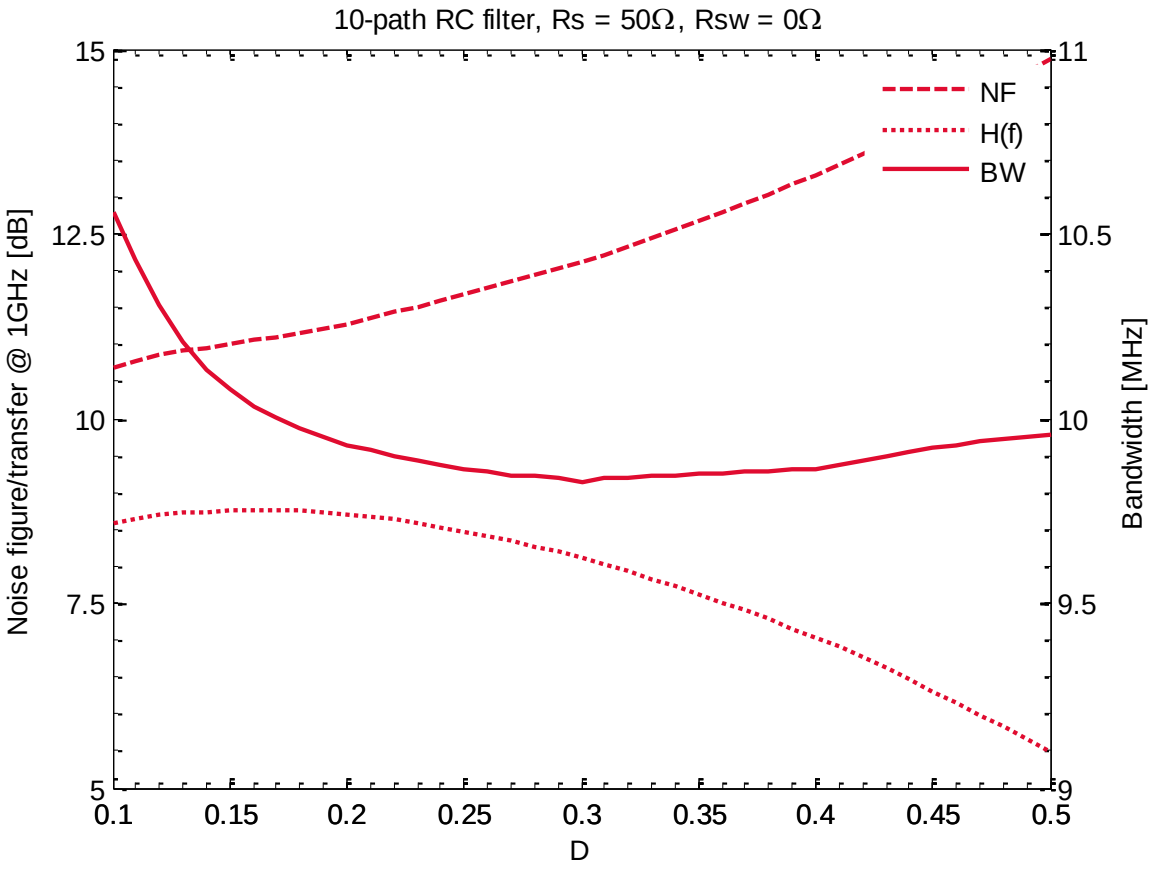


**Figure 30 - NF, H(f) and BW as a function of the duty cycle with opamp adder at output.**

# 9 Mismatch sensitivity

Simulations must be done in order to test whether the filter is sensitive to mismatch and if it is possible to create a working filter within CMOS processing variations. Mismatch simulations were performed as follows. A random variable with a Gaussian distribution, a mean of 1 and a certain standard deviation was created. The values of the component tested for mismatch is multiplied by this variable. A Monte Carlo simulation using ADEXL using 100 runs is used to determine the effect of this mismatch. A standard capacitor value of $10pF$ was chosen and any other parameters were scaled to ensure a roughly constant $10MHz$ bandwidth. The graphs shown in this chapter use the *boxplot* function of MATLAB. On each box, the central mark is the median, the edges of the box are the 25th and 75th percentiles, the whiskers extend to the most extreme data points not considered outliers, and outliers are plotted individually.

A standard RC filter is sensitive to phase mismatch. Simulations were done with non-overlapping clocks with random duty-cycle with a μ of 1/N and a σ of 0.01. Monte Carlo simulation shows that most properties of the filter do not change. This bandwidth, noise figure and transfer function remain almost constant. The main difference is in the folding. The 3$^{rd}$, 5$^{th}$, and 7$^{th}$, harmonics suddenly fold back to around -60dB, compared to less than -100dB without mismatch. This is shown in Figure 31.

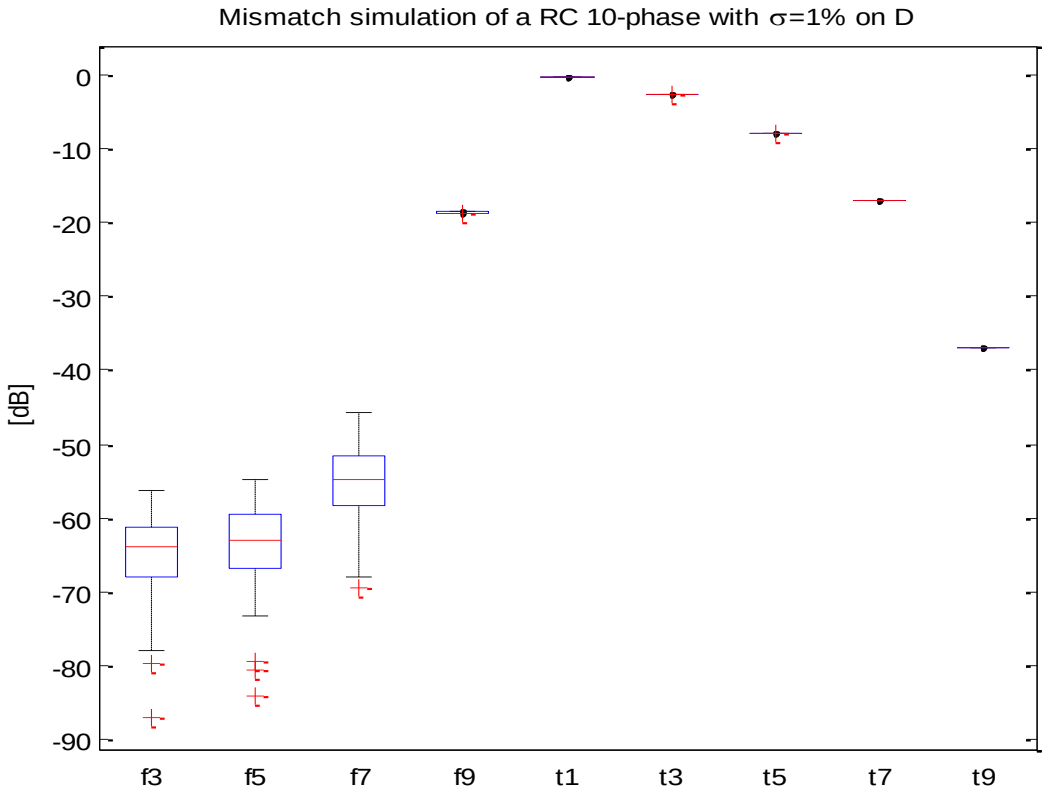


**Figure 31 - Results from Monte Carlo (duty cycle) for a square-wave mixer. The letters on the horizontal axis stand for f(olding) and t(ransfer), the number for the harmonic.**

The harmonic rejection mixer was also simulated and similar results are found, these are depicted in Figure 32. The NF and bandwidth are insensitive to variations in duty cycle and not plotted. The

folders are sensitive resulting in folders of around -60dB. The transfer function shows no sensitivity to phase mismatch. This is most likely due to the fact that any phase error at the input will also be present at the output, cancelling the effect on the transfer function.

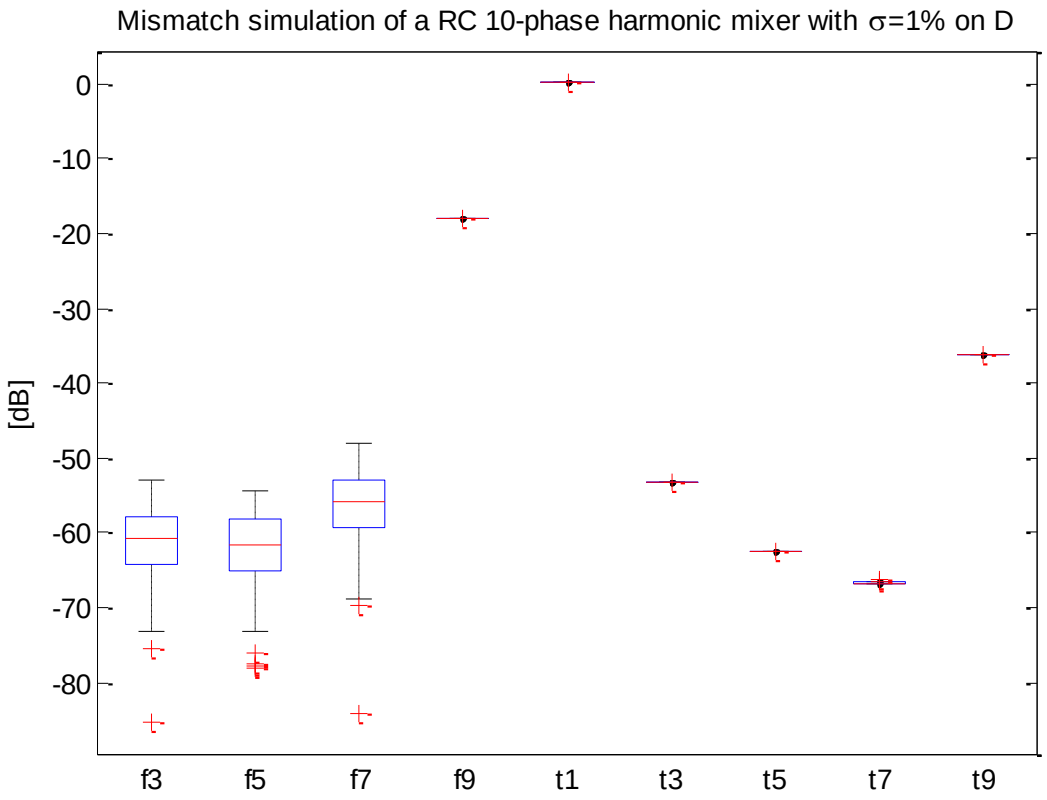


**Figure 32 - Results from Monte Carlo (duty cycle) for a harmonic rejection mixer. The letters on the horizontal axis stand for f(olding) and t(ransfer), the number for the harmonic.**

In a standard N-path filter, mismatch between the (SC) resistors will change the effective bandwidth of each path, just as the mismatch between clock phases does. The main difference is that mismatch in the impedance of the output switches does not influence the filter, this in contrast to the clock mismatch. Mismatch in impedances might be more problematic for harmonic rejection mixers as it will influence the weighing function and thus the workings of the harmonic rejection mixer. The RC 10-phase filter using harmonic rejection mixers has been simulated with 1% mismatch for each resistor in the mixer. The results can be found in Figure 33. The effect on folding is less than for the clock mismatch but the effect on the transfer function is stronger. The rejection of harmonics is decreased by a maximum of about 10dB.

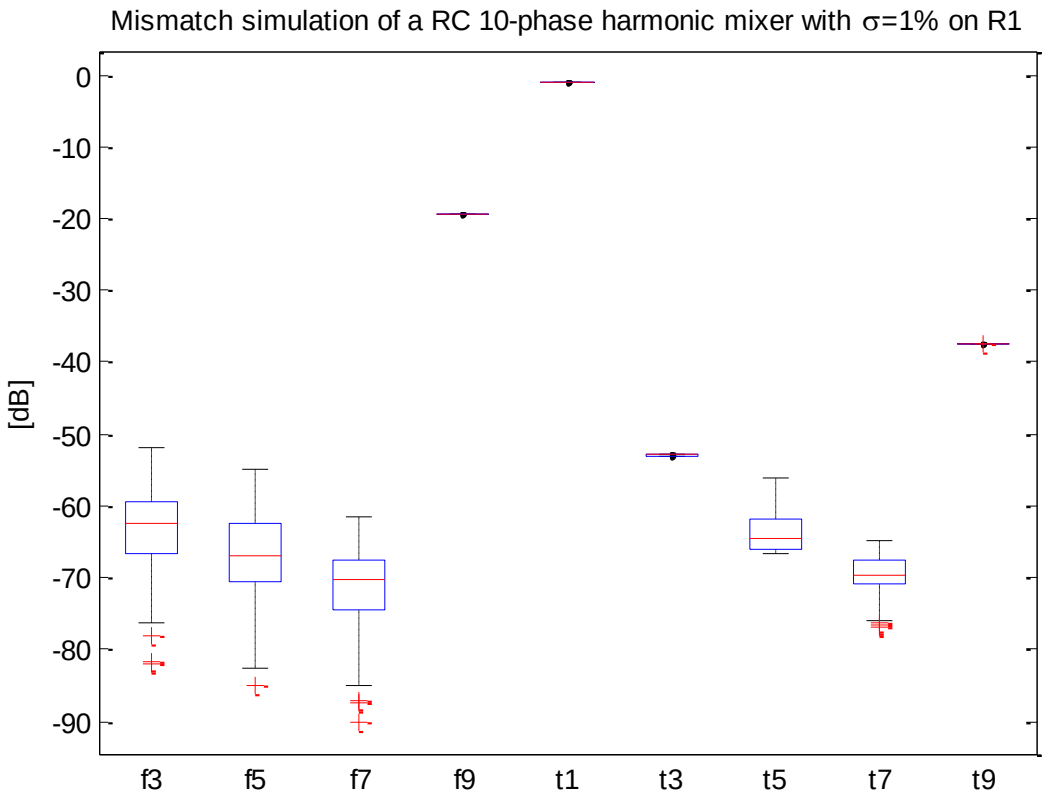


**Figure 33 - Mismatch simulation for mismatch in R1. The letters on the horizontal axis stand for f(olding) and t(ransfer), the number for the harmonic.**

# 10 Filter optimisation

Due to the large number of possible applications, no 'best' solution exists. As the aim of this research is beneficial for applications that required a clean transfer function and no folding, a solution is presented that combines the solutions presented in chapters 6 and 7.

One question that arises is whether overlapping the clocks will change the working of the harmonic rejection mixer. In the case of switched capacitors this is not a problem. When the switch is closed, the small capacitor is put in parallel with the large capacitor. When a capacitor from another stage is now connected in parallel, it sees the baseband capacitor parallel to the small capacitor. For high-Q filters, the total capacitance seen is close to the baseband capacitor and the overlapping only results in a small error. In the case of the RC filter, overlapping clocks will result in a parallel connection of resistors lowering the total resistance to (almost, as the values differ between paths) half. This alters the bandwidth and noise performance.

The optimal filter is very application-dependent. A standard N-path filter can have a low noise figure but the bandwidth is poorly defined due to the uncertainty of the source impedance. Harmonic rejection results in the desired transfer function at the cost of increased losses. In the case of the RC filter the noise figure is also very high. Increasing the number of clock phases results pushes out the folders. The overlapping clocks prove to be no problem if a good adder can be used. The folding behaviour does not suffer from the overlapping clocks. The use of passive capacitive adder results in high losses and is not favourable. Adding active devices to increase the gain is desired. The optimal filter would therefore consist of a SC baseband filter using harmonic rejection mixers and an active adder, with overlapping clocks. Such a filter would show a near-LTI band-pass response with folding only at very high frequencies.

As the folding harmonics are to be filtered out before entering the filter (for instance embedded in antenna design), some room in the frequency spectrum must be given to filter. When all harmonics up to the 10$^{th}$ are not allowed to fold, a 12-path filter (for an even number of paths) is required. However, when the 10$^{th}$ harmonic is still to be used, the 11$^{th}$ harmonic cannot be filtered out to prevent folding as the spectral spacing is not enough. To increase this spacing a hybrid solution was used. A 24-path filter is combined with 12 phase harmonic rejection mixers. These mixers clean the transfer function up to the 10$^{th}$ harmonic while pushing folders out to the 23$^{rd}$ harmonic. The coefficients for the harmonic rejection mixer contain two zeros. These result in only 10 paths for each harmonic rejection mixer (12-2) There are 24 paths with two switches per mixer, plus one switch at the output. This results in equation **10.1**.

$$\#switches = (20 + 1) \cdot 24 = 504 \qquad 10.1$$

In chapter 4 the maximum total switch width was calculated. The allowed width of one switch is thus given by **10.2**.

$$W_{switch} = \frac{W_{tot}}{\#switches} = \frac{13 \cdot 10^3}{504} = 25.6\ [\mu m] \qquad 10.2$$

A NMOST switch with $1.2V_{gs}$ has an estimated $R_{on}$ of $500\Omega/\mu m$. A rough calculation results in a switch resistance as given by **10.3**.

$$R_{on} = \frac{500}{25.6} = 20\Omega \qquad 10.3$$

Such a large switch resistance results in a high noise figure of 4.8dB. Lowering the switch resistance to 10Ω reduces the noise figure to 3dB, while a 5Ω switch will result in a noise figure of 1.8dB. Such large switches will greatly increase the power consumption to 100 and 200mW respectively. As an ideal adder is used, in practice additional power will be consumed in the adder.

The baseband capacitors have a value of 40pF. The SC-resistors have a base value of about $0.17pF$. The total capacitance in the filter is given by equation **10.4**. This value about the maximum of 1nF specified in chapter 4.

$$C_{tot} = 24 \cdot (40 + 7.5 \cdot 0.17) = 990\ [pF] \qquad 10.4$$

The performance of this filter is shown in Figure 34. The overlapping clocks result in gain (7.2dB) while all folders are pushed out to the expected 23rd harmonic and higher.

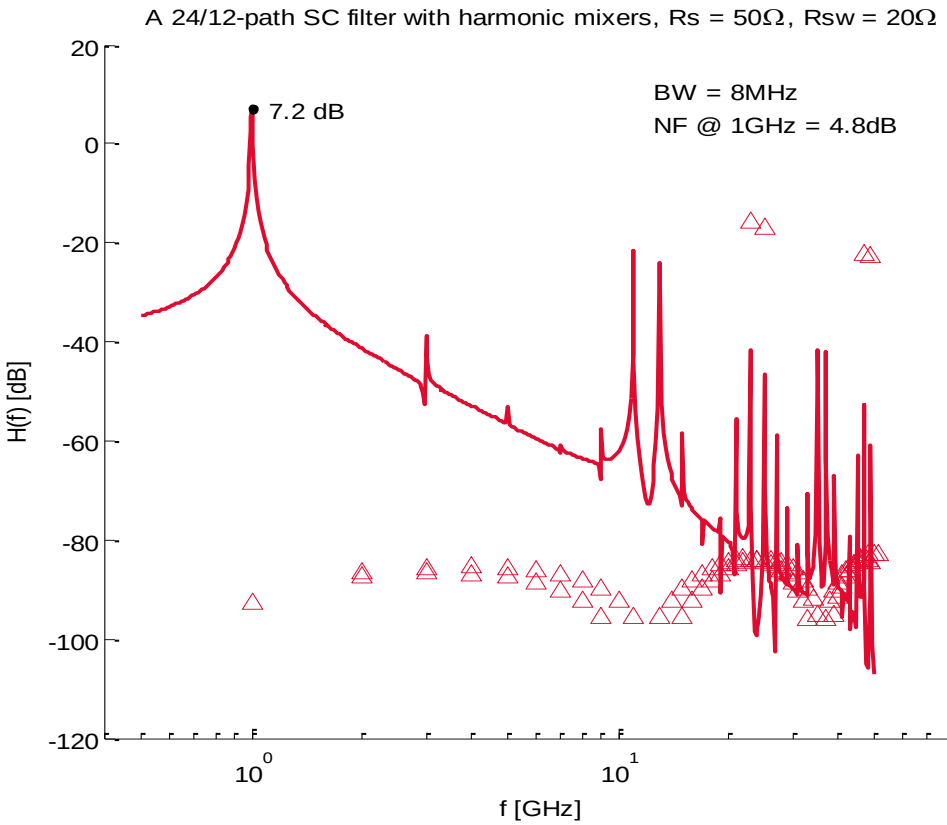


**Figure 34 - Frequency response of a 24-path filter using 12 phase harmonic rejection mixers and switched capacitor resistors. The triangles denote the strength of folders, folders from negative frequencies are given on the positive axis.**

To show that the filter is capable of performing equally well at different centre frequencies, the same filter was simulated for different centre frequencies from 1 to 5GHz. The resulting transfer function is shown in Figure 35. As can be seen in the image, the gain does not change significantly and also the filter shape is preserved. It should be noted that the simulation does not take parasitics into account and that some attenuation at higher frequencies is to be expected.

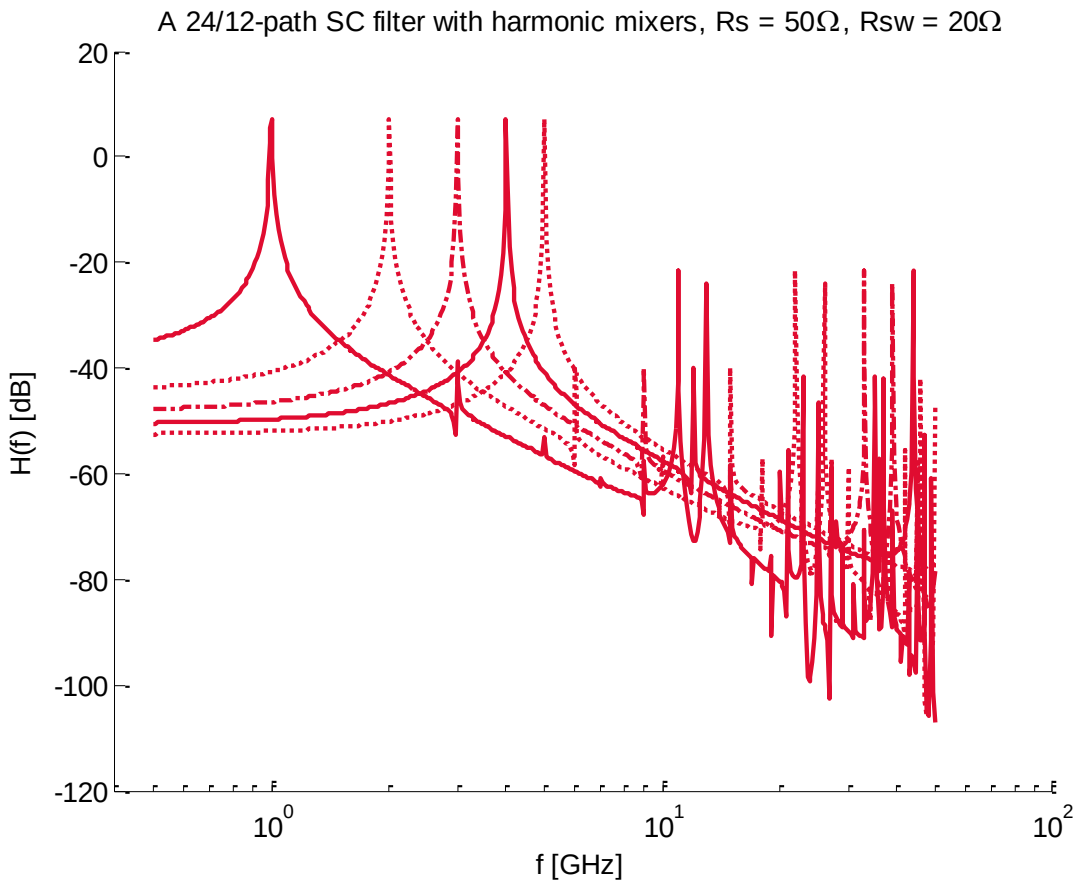


**Figure 35 - Transfer function for different centre frequencies from 1 to 5GHz.**

# 11 Conclusion

The aim of this thesis is to find a solution for two issues found in typical N-path band-pass filters. The first issue is the comb-like transfer function of the filter; the filter shape is repeated around harmonics of the clock. The second issue is the folding of signals present at harmonics onto the desired signal at the fundamental. A solution was found for both issues. The performance of the solutions was simulated using both an RC and SC low-pass filter. The noise figure was typically higher for the RC filter compared to the SC filter. The SC filter does require very low-ohmic switches increasing area and power consumption.

The comb in the transfer function can be suppressed by using harmonic rejection mixers instead of square-wave mixers. Harmonic rejection mixers can be implemented in a passive manner by impedance scaling. The harmonic rejection mixers suppress the transfer of harmonics up to the $k^{th}$ harmonic, with $k$ being the number of phases used for the harmonic mixer. This number can be equal to the number of paths but a less is also possible. When $N$ phases are used for the harmonic rejection mixers, the area required for the switches and resistors scales with $N^2$ which may be problematic when $N$ is large.

The filter will fold the harmonics $k \cdot N - 1$ and $k \cdot N + 1$ $(k \in N)$ onto the desired signal at the fundamental harmonic. No solution has been found that removes the dependency on $N$. It is shown that the folding behaviour is not dependent on the duty cycle of the clock. The common assumption that the clock is non-overlapping is thus not required. This allows the use of different methods for the generation of the clock signals such as ring oscillators. Once requirement that results from the use of overlapping clocks is that a good adder is required to sum the outputs. When a good adder is present, for instance an opamp adder, overlapping clocks result in signal gain. The adder might be combined with the LNA to save power and area.

It has been shown that the use of harmonic rejection mixers can be combined with overlapping clocks resulting in good performance. An example circuit has been simulated. This filter consists of 24 paths with a SC low-pass filter using harmonic rejection mixers. The harmonic rejection mixers only use 12 phases to save power and area. Each phase has a duty cycle of 0.125. The filter has a transfer function that does not pass any harmonic for a full decade. The first harmonic to fold back is the 23$^{rd}$. The noise figure is 4.8dB and has a gain of 7.2dB at 1GHz. The total power consumption is approximately 50mW and around 1nF of capacitance was required for the filter to operate.

As each application has its own set of requirements, no optimised solution can be given. Harmonic rejection mixers and overlapping clocks do enable specifications that previously were not attainable with N-path filters.

# 12 Recommendations

During the course of this thesis several ideas were discarded due to the fact that they fall outside the scope of this thesis or due to time constraints. This chapter aims to provide some direction to future research into N-path filters with overlapping clocks and/or harmonic rejection mixers.

### Adaptive mixing function

Harmonic mixers as presented in this thesis show a strong increase in area when increasing N (area goes up with $N^2$). Depending on the application, it might not be required to reject all harmonics or some harmonics might require stronger rejection than others. Making the impedances controllable can provide adaptive harmonic rejection. The total number of phases to make the harmonic rejection mixer might then be much smaller than N.

### Implementation of active adders

In this thesis, the need for a good adder has been shown. In simulations ideal adders were used but not implemented. Before the overlapping clocks can be used an implementation of the adder must be made.

### Increasing the peak-to-valley ratio

The filter order can be increased by increasing the order of the low-pass filter. This can be achieved by using a higher-order low-pass filter or by cascading entire filters. Cascading doubles the required area. Making the low-pass filter of higher order will result in a higher peak-to-valley ratio.

# 13 Bibliography


[1] L. Franks and I. Sandberg, “An Alternative Approach to the Realization of Network Transfer Functions the N-path Filter,” *Bell System Technical Journal,* vol. 1350, p. 1321, 1960.

[2] M. T. Borelli, “Analysis of Commutated Networks Employing Feedback Circuits,” *Aerospace and Electronic Systems, IEEE Transactions on,* Vols. AES-5, no. 1, pp. 39-45, 1969.

[3] R. Frischl, “Analysis of a Commutated Network,” *Aerospace and Navigational Electronics, IEEE Transactions on,* Vols. ANE-10, no. 2, pp. 114 - 123, 1963.

[4] Y. Sun and I. T. Frisch, “A General Theory of Commutated Networks,” *Circuit Theory, IEEE Transactions on,* Vols. CT-16, no. 4, pp. 502-508, 1969.

[5] A. Ghaffari, E. A. Klumperink, M. C. Soer and B. Nauta, “Tunable High-Q N-Path Band-Pass Filters Modeling and Verification,” *Solid-State Circuits, IEEE Journal of,* vol. 46, no. 5, pp. 998-1010, 2011.

[6] O. Elissati, E. Yahya, S. Rieubon and L. Fesquet, “A novel High-Speed Multi-phase Oscillator Using Self-Timed Rings,” in *International Conference on Microelectronics*, 2010.

[7] S. M. Faruque, “Switched-capacitor FIR cell for n-Path filters,” *Electronics Letters,* pp. 431-432, 1982.

[8] M. Darvishi, R. Van der Zee, E. Klumperink and B. Nauta, “A 0.3-to-1.2GHz Tunable 4th-Order Switched gm-C Bandpass Filter with >55dB Ultimate Rejection and Out-of-Band IIP3 of +29dBm,” in *IEEE International Solid-State Circuits Conference*, San Francisco, 2012.

[9] H. C. Patangia, B. Zenone and C. Wang, “A Novel Switched-Capacitor Oscillator Based On The N-Path Filter Approach,” in *Circuits and Systems, 1991., IEEE International Sympoisum on*, Arkansas, 1991.

[10] H. Wupper, “A Modified N-Path Filter Suited for Practical Realization,” *Circuits and Systems, IEEE Transactions on,* Vols. CAS-21, no. 3, pp. 449-456, 1974.

[11] C. L. Phillips, “A Study of Quadrature Bending Mode Signal Cancellation by the Use of Commutated Networks,” NASA, Huntsville, 1966.

[12] T. R. Nilsen, “Commutated Network Filter,” United States Navel Postgraduate School, Monterey, 1969.

[13] A. Monpapassorn, “High Frequency/Low Voltage CMOS Adder,” *Thammasat Int. J. Sc. Tech.,* vol. 5, no. 2, pp. 48-52, 2000.

[14] M. Ahmed, I. Khan and N. Minhaj, “Novel Electronically Tunable C-Multipliers,” *Electronics*

*Letters,* vol. 31, no. 1, pp. 9-11, 1995.

[15] K. Möhrmann von and W. Heinlein, “N-Pfad-Filter hoher Selektivität mit spulenlosen Schwingkreisen,” *Frequenz,* vol. 21, no. 12, pp. 369-375, 1967.

# 14 Appendix A – VerilogA code

The code of the ideal adders is given below in the case of three inputs. The code can easily be extended to a higher number of inputs.

```
module NpathfilterAdd3(in1,in2,in3,out);

input in1;
input in2;
input in3;

output out;
voltage in1,in2,in3,out;

analog
        begin
                V(out) <+ V(in1) + V(in2) + V(in3);
        end

endmodule
```

# 15 Appendix B - Simulation details

This chapter covers the simulator settings used to obtain the results.

## 15.1 Component parameters

The simulation is parameterised and contains the following values/formulas.

### Source parameters

Parameters of signal source.

**Table 1 - General parameters.**

| Parameters | Value |
|---|---|
| Source resistance ($R_s$) | $50\ [\Omega]$ |
| PAC magnitude (square wave mixer) | $0.5\ [V]$ |
| PAC magnitude (harmonic rejection mixer) | $1\ [V]$ |
| XF magnitude (square wave mixer) | $0.5\ [V]$ |
| XF magnitude (harmonic rejection mixer) | $1\ [V]$ |

### Clock generation

The clocks are generated using ideal voltage sources with a pulse as output. The pulse shows linear behaviour at the edges. The settings for these sources are listed in the table below. The value k ranges from 0 to N-1 for phases 1 through N. All values are default, some are different between simulations, this is indicated with the simulation results.

**Table 2 - Settings for the clock sources.**

| Parameter | Default value |
|---|---|
| Delay time | $k \cdot \frac{T}{N}[s]$ |
| Zero value | $0\ [V]$ |
| One value | $1\ [V]$ |
| Period of waveform | $T\ [s]$ |
| Rise time | $tr \cdot T\ [s]$ |
| Fall time | $tf \cdot T\ [s]$ |
| Pulse width | $tp \cdot T\ [s]$ |
| tr | $0.001$ |
| tf | $0.001$ |
| tp | $A - tr - tf$ |
| T | $1\ [ns]$ |
| A | $1/N$ |
| N | $10$ |

### Switches

The ideal switches have the following parameters. These parameters are fixed throughout simulations.

**Table 3 - Parameters of the ideal switches.**

| Parameters | Value |
|---|---|
| Open voltage | $1\ [mV]$ |
| Closed voltage | $2\ [mV]$ |
| Open switch resistance | $1\ [T\Omega]$ |
| Close switch resistance | $1\ [m\Omega]$ |

## 15.2 Simulation parameters

Four simulations were set: pss, pac, pnoise and pxf. All simulations are periodic as the filter is swiched.

### Periodic steady stage

Settings:

**Table 4 - PSS settings.**

| Parameter | Value |
|---|---|
| Beat frequency | $1\ [GHz]$ |
| Accuracy | $Moderate$ |

### Periodic AC

Settings:

**Table 5 - PAC settings.**

| Parameter | Value |
|---|---|
| Points per decade | $200$ |
| Maximum sideband | $15$ |

### Periodic noise

Settings:

**Table 6 - Pnoise settings.**

| Parameter | Value |
|---|---|
| Maximum sideband | 15 |
| Reference sideband | 0 |

### Periodic XF

Settings:

**Table 7 - PXF settings.**

| Parameter | Value |
|---|---|
| Maximum sideband | 15 |