UNIVERSITY OF TWENTE.

Faculty of Electrical Engineering,
Mathematics & Computer Science

Behavioral Models of Nonlinear Power Consuming Loads

Pieter van Vugt
M.Sc. Thesis

May 29, 2013

Supervisors:
Prof. dr. ir. F.B.J..Leferink
Ir. R.B.Timens
Ir. F. J. K. Buesink
Dr.ir. M.J. Bentum
Dr. ir. L.J. Spreeuwers

Telecommunication Engineering Group
Faculty of Electrical Engineering,
Mathematics and Computer Science
University of Twente
P.O. Box 217
7500 AE Enschede
The Netherlands

Summary

In recent years, the increasing number of nonlinear loads on the power mains in office buildings has been known to cause problems with poor power quality and the transformers of the building getting too hot. Fixing this afterwards can be very costly. To predict and prevent these problems, it is desirable to simulate the power network with these nonlinear loads. In this report, low frequency models are developed for two kinds of nonlinear loads commonly found in office buildings. The devices under modeling (DUMs) are a Compact Fluorescent Light bulb (CFL bulb), which is a load with a rectifier bridge without power factor correction (PFC) and a switched mode power supply (SMPS) with active PFC, as commonly found in an office PC. The electrical behavior of these two devices is representative of the majority of loads in an office building. The models are low-frequency and computationally light so that many DUMs and their interaction can be simulated at once. A gray-box modeling strategy is adopted, where the structure of the input circuit looking into the DUM from the power mains is assumed to be known and is modeled in SPICE. This can be done because these input circuits are often very similar between devices. Methods of parameterizing these circuits from measurement are developed, so that in order to use the model for a different but similar DUM, no intimate knowledge is needed of its internals. The accuracy of the models is verified by comparing the output of the models with actual measurements, using clean voltage and current waveforms as well as waveforms measured at locations with poor power quality.

Dr. ir. Igor Stievano from Politecnico di Torino (the Polytechnic University of Turin) has expertise in a nonlinear black-box modeling approach. We have been working together and he has tried to make a black-box model of the rectifier without PFC. His result, which is also presented in this report, was very similar to the gray-box model, and it contributed to the quality of both gray-box models because of that.

Table of Contents

1 Foreword

The last part of the Electrical Engineering Master program is, as with any other Master program, the Master research assignment. Within the Electrical Engineering Master, I follow the Telecommunication and Networks track. Electro-Magnetic Compatibility (EMC) is one of the elective courses within that track, and of all the electives that I followed, EMC was the one that intrigued me the most. Perhaps this was due to the fact that earlier I encountered EMC related issues during my Bachelor assignment, where I analyzed the performance of a device that had digital and analog RF circuitry on the same circuit board. This device turned out to be poorly laid out, from an EMC point of view. Because of this, I decided I wanted to do my Master's assignment in EMC. My Master assignment concerns power quality, which is a part of EMC.

The work presented in this report is the master thesis project of Pieter van Vugt, performed at the University of Twente and Thales Hengelo, from September 2012 until June 2013.

~ ~ ~

This work is dedicated to my loving fiancé

Ellysa Susanto

And her sweet little daughter

Clarita Evania

2 Introduction

Product standards such as EN61000-3-2, have been designed to make sure the disturbance on the power network is kept within acceptable bounds, to avoid disturbing other appliances on the network. When these standards were formulated, most loads on the power network were linear, such as heaters, incandescent light bulbs and AC motors. At the time, it was assumed that the load diversity would stabilize the network voltages, so that small nonlinear consumers would not influence the power quality in an unacceptable way. Therefore, it was only deemed necessary to create standards for electrical appliances that use more than 75 Watt (or 25 Watt depending on the type of device [1]), as the occasional nonlinear load of less than that was not expected to cause problems.

However with the increase in use of CFL light bulbs, LED lighting and a lot of other modern, energy efficient electronics, the number of nonlinear loads below 75 Watt on a typical power network has increased dramatically in the last decade. This has recently been found to cause problems for instance in office buildings [2][3]. In other words, the assumptions that were made when the standards were developed appear to be no longer valid.

Nonlinear loads that consume more than 75 Watt are required by EN61000-3-2 to have a power factor corrector (PFC), which is a circuit that mitigates the nonlinear behavior of the load and makes it behave more like a resistor. However, the PFC does not entirely succeed in this, and the behavior of the load is usually still quite nonlinear. And just like with the loads below 75W, the number of loads with PFC has increased as well over the last few decades, as computers, monitors, laptop chargers and fluorescent tubes are all generally of this type.

The problem with all these nonlinear loads is that they cause transient currents, not only when they are switched on, but also in steady operation. The transient current consumed when equipment is switched on is only a single disturbance, which does not cause problems very quickly. But with these nonlinear loads however, a similar, but smaller transient current appears every 10ms, i.e. twice every 50Hz period. These transients add up for every similar load that is in operation at any given time on the power network.

To quantify the problem and to predict the interference towards other equipment, it is desirable to be able to model the behavior and interaction of these nonlinear loads. This is also relevant on ships and in rural areas where the impedance of the power network is relatively high or the available power on the network is limited, while many of these nonlinear loads are present.

The goal of this project is to create black-box models, macro-models or behavioral models of common nonlinear loads. The macro-model can be constructed easily from the circuit diagram of the equipment and using basic spice models for the devices. However, when connecting many of these macro-models in a large network the simulation time will become extensively long. By converting the macro-model to a behavioral model, the simulation time can be drastically decreased. Furthermore, these models will need to have designable parameters that can be adapted so that the engineer who uses the models can optimize the power network design and choice of loads to reduce electromagnetic interference. These behavioral models can be accurate yet efficient enough so they can be used in simulations where many of these loads are connected to a non-ideal power network.

The model should be constructed so that its parameters can be derived from on measurements. This way, the model can be adapted to represent an individual device, without having detailed knowledge of the inner workings of the device under modeling (DUM).

At Politecnico di Torino (the Polytechnic University of Turin), there is a research group lead by Prof. F.G. Canavero who are very active in the area of black-box modeling of high-frequency I/O ports on IC's [4][5][6][7][8]. We are working together with Dr.ir. Igor Stievano from that group, and he will see if their expertise in modeling of I/O ports on ICs allows them to apply their methods to nonlinear loads on the power net as well.

2.1 Report Outline

The rest of the report is structured as follows. In Chapter 3 the results of the preliminary literature study on the subject of this thesis is presented. Chapter 4 discusses the various nonlinear loads that can be found in an office building, categorizes them and presents the devices that will be modeled in this work. In Chapters 5 and 6 the models and their parameterization methods are discussed, respectively. Measurements on the DUMs are presented in Chapter 7, and model validation is done in Chapter 0. The user manual for the models is found in Chapter 9. In Chapter 10 the conclusions of this work are presented, and a look is taken into future work.

3 Literature Survey

In this chapter the findings from the literature survey that was performed at the beginning of the project are presented. First the kinds of papers that have been searched for are motivated, and then the findings of the survey are summarized.

3.1 Direction of Search

The literature survey was focused on finding papers on modeling loads on the power grid, but also on modeling nonlinear electrical input ports in ICs. The reason for this is that as frequencies on printed circuit boards become higher and higher, more signal integrity analysis is needed to make products that function reliably. Because of this, in recent years a lot of work has been done on modeling the behavior of I/O ports on chips, which are nonlinear devices. It might be possible that a behavioral modeling technique usually applied to input ports of high speed electronics can be adapted to model a nonlinear load on the power network.

3.2 Summary of gathered literature

In this section, the relevant literature and information found during the literature survey is summarized.

Most models of loads on the mains found in literature that are purely concerned with their voltage-current behavior are linear models, for instance [9], where a linear model is treated of a DC motor armature. Also, very often the models are concerned about high-frequency conducted emissions, for example in [10], where the proposed model predicts conducted emissions of a SMPS from 20 kHz to 100 MHz. Other works include [11], where a method of predicting high frequency conducted EMI is developed, and design considerations for the active PFC are presented. These high-frequency emissions can cause a power cable to act as an antenna and cause radiated emissions, or they can propagate along cables and interfere with other nearby equipment connected to the same power network (conducted EMI). This can be a serious issue too, as is reflected by the fact that electronic products to be sold commercially have to comply with standards such as CISPR 22 or EN 55022 [12], which even describe standardized methods and equipment for compliance testing.

However for the purpose of this work, the high frequency conducted emissions are not relevant. Especially with the CISPR 22 or EN 55022 standards in place that limit their intensity, these high frequency emissions are not expected to propagate very far onto the power network, so they should not cause the kind of building-wide problems that this work addresses. Rather, it is the low frequency emissions and distortions that cause building wide power quality problems [2][3].

The main interest in this work is the low frequency behavior of electronics, but that does not mean that modeling techniques designed for high-frequency electronics are necessarily irrelevant to this work. It is worth investigating if for instance modeling techniques applied to high speed Input/output (I/O) buffers of integrated circuits (ICs) can be adapted and applied to loads on the mains driven by 50 Hz.

A well-known format for making black-box behavioral models of I/O ports on ICs is the IBIS (Input/Output Buffer Information Specification) standard. IBIS was developed in the early 1990's when the PCI bus was being developed. The higher speed of the PCI bus made signal integrity (SI) simulations necessary, so Intel, together with other companies, developed IBIS as an open standard for I/O buffer simulation. A basic IBIS model consists of V-I and V-t curve data as well as values for parasitics (R, L, and C) of the packaging of the IC, and it is possible to derive this model from measurements, if the vendor of the IC does not provide the model. [13][14]

In recent years as the communication speeds on printed circuit boards increased further, the standard IBIS models were found to be no longer sufficiently accurate. For this reason, alternate methods of behavioral modeling I/O buffers have been developed. Dr. I. Stievano and Prof. F. Canavero et al. have developed a method of constructing parametric black-box models that can be derived from measurements. These models are based on the MπLog method and are nonlinear and purely mathematic [4][5][6][7][8]. This method works by means of a set of basis functions. These basis functions, for instance Gaussian radial basis function (GBF) are scaled and dilated as a function of a set of parameters and present and past input voltage values. Then these are summed to form the current. The parameters are derived from measurements, and they define the behavior of the model. For a more detailed explanation of this methodology, please refer to [7] and other references to papers by the same author. As mentioned in the introduction, Dr. I. Stievano and Prof. F. Canavero have been asked to work with us to see if they could apply their techniques to the DUMs considered in this work. Aside of GBF, Spline Functions can also be used [15]. An extensive overview of the possible basis functions and the general mathematics related to this kind of nonlinear behavioral modeling strategy, independent of domain, is given in [16]. While the aforementioned works all concern the time domain, it should be mentioned there is also a somewhat similar approach possible for behavioral modeling in the frequency domain [17].

All the literature mentioned above is purely concerned with the voltage and current behavior of the loads. However in order to effectively develop a model, it is necessary to gain an understanding of the internal operation of the loads as well. In [18] an overview is given of possible ways to model a SMPS with active PFC, with the intention of aiding engineers who need to design such a device. While the goals and requirements for the modeling strategies in that paper are very different than they are for this work, it still provides valuable insight in how an active PFC operates. A brief overview of the different types of PFC is found in [1], as well as detailed information on the EN 61000-3-2 standard, governing the requirements for the performance of a PFC.

4 Devices under Modeling

In this Section we look into the devices that will be modeled in this work. Central to this discussion is the power factor correction (PFC) that some devices have, and others do not. So first in Section 4.1 the function of a PFC is briefly discussed and a common misunderstanding about the power factor is cleared up. There are several kinds of nonlinear loads on the mains that could be modeled. However due to time limitations, a choice was be made for the two most relevant loads: The *rectifier without PFC* and the *Active PFC*. The first is modeled by studying a compact fluorescent light bulb (CFL bulb), and the second by studying a Switched Mode Power Supply (SMPS) with active PFC as is commonly found in personal computers. The reason for these choices will be outlined in Section 4.3, but in Section 0 first the variety in common nonlinear loads is presented and categorized.

4.1 Power Factor Correction

Nonlinear loads that consume more than 75 W (or 25 W in some cases [1]) are required to have power factor correction. A power factor corrector (PFC) is a circuit that attempts to make the device draw a current that is proportional to the instantaneous voltage, i.e. make it behave more like a resistor, and increasing the power factor to above some value, usually 0.9. Whether a PFC is required for a device or not depends on the power that it consumes, and what kind of device it is. The rules for lighting are for instance different than for other equipment. These requirements come from the NE 61000-3-2 standard.

It should be noted however that the term "power factor" in this context does not refer to the displacement power factor, which is the cosine of the phase difference between a sinusoidal voltage and current. The power factor used here is calculated from the active power and apparent power. The active power is defined as the average of the instantaneous power:

$$P = \frac{1}{T}\int_0^T p(t)\,dt$$

Where $p(t) = i(t)v(t)$. Apparent power is the product of the RMS value of the voltage and current:

$$S = I_{RMS}V_{RMS}$$

The power factor is then defined as:

$$\lambda = \frac{P}{S}$$

This definition is always valid, regardless of waveform or application. When the voltage and current are both a perfect sine, then the cosine of the phase difference between the two, the displacement power factor, has indeed the same value as the equation above. However, once nonlinearities are considered, and the current and/or voltage are no longer perfect sines, then the definition of displacement power factor can no longer be used, unless you define it for every harmonic. This also means that the power factor can be much less than unity because of non-sine shaped current waveforms, even though there is no displacement in the fundamental harmonic.

4.2 Range of Common Nonlinear Loads

There is a wide range of appliances that are commonly found in an office building, that present nonlinear loads on the mains. LED lighting, modern phone chargers, CFL light bulbs or fluorescent tubes, laptop chargers, personal computers and monitors, to name a few. These nonlinear loads represent virtually all the load on the mains in a modern office building. But even though the range of appliances is large, they can still be fitted into categories, when looking at the behavior of the currents that they draw. The current is determined by the topology of the input circuitry. The categories that can be distinguished are as follows.

- **Single sided rectifier**
  These are low-power devices, that generally consume only a few Watt. They draw a highly distorted current only on one side of the 50Hz sine (either on the positive or the negative side) because of the single rectifying diode and lack of PFC. Common example: LED lights.
- **Double sided rectifier without power factor correction**
  These are devices that draw current on both sides of the 50 Hz sine, but have no PFC, so their currents are also highly distorted. Behind the rectifier there is sometimes a switched mode power supply (SMPS). Common examples: CFL bulb, mobile phone chargers.
- **Passive power factor correction**
  These loads also contain a double-sided rectifier, but because they consume more than a certain amount of power, they are required to have a PFC. A passive PFC is made up of large capacitors and coupled inductors that act as differential mode chokes, creating a large low-pass filter, that lets the current waveform more closely resemble a sine. This PFC can be part of a switched mode power supply. Common example: (Old-fashioned) PC power supplies.
- **Active power factor correction**
  These loads contain also a double-sided rectifier, but behind it there is an active PFC, which is an active switching circuit that attempts to always draw a current through the rectifier bridge from the mains that is proportional to the instantaneous input voltage, i.e. it tries to follow the sine. This circuit is normally an integral part of a SMPS. The active PFC requires smaller passive components and is generally more effective than a passive PFC. Common example: PC power supplies, laptop chargers.

4.3 Devices under Modeling

In this work two of the above classes will be modeled: the double sided rectifier without PFC, and the active PFC. In this section these choices are motivated.

The double sided rectifier without PFC is a very common load and is found for instance in CFL light bulbs. In modern buildings, but also in buildings that recently have been renovated, by far most lighting is of this kind. The wide implementation of these CFL bulbs makes it a very relevant category, and one that is likely to be of significant influence on the power quality in buildings. The primary device under modeling (DUM) representing this category is a Karwei home brand 11W CFL bulb (Item number: 292935).

Figure 1: Karwei own brand 11W CFL bulb internals

The SMPS with active PFC is commonly found in computers and other appliances that consume more than 75 Watt, or 25 Watt in the case of lighting. Because the components are smaller than with a passive PFC, the active PFC is also found in laptop chargers or mini-PC power supplies, which are also increasingly common in office buildings. Computer power supplies can still be found on the market with passive PFC, (as of November 2012), but they have become fairly hard to find. This makes the active PFC more interesting to model, as the contribution to the total load in a building from passive PFCs is becoming less and less over time. The primary DUM representing this category is a Be Quiet® Pure Power L7 (300 Watt) PC power supply.

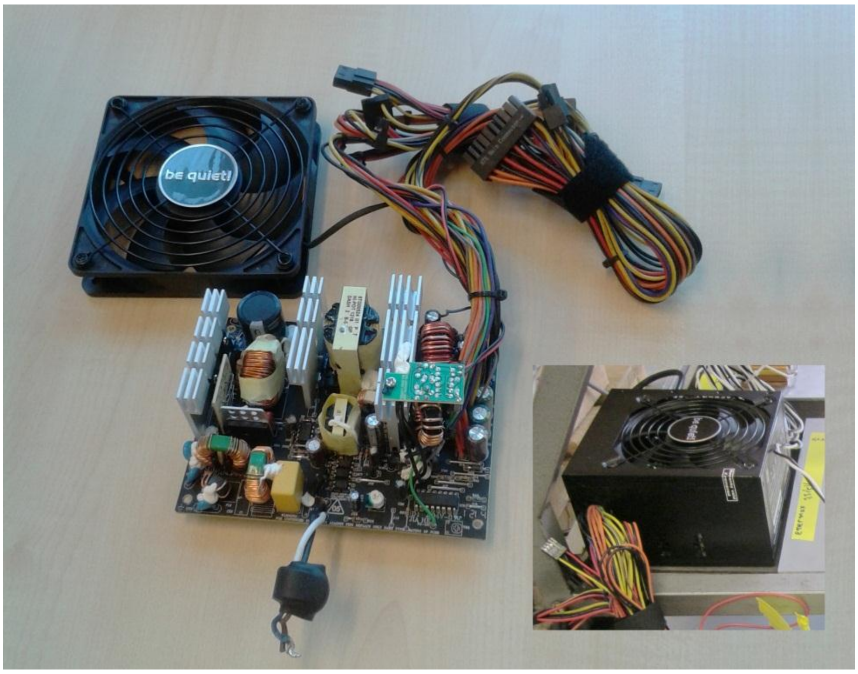

Figure 2: Be Quiet® Pure Power L7, 300W PC power supply internals

Aside of the two primary DUMs introduced above, several other secondary DUMs have been modeled as well, to validate the developed models. This is treated in Section 0.

5 Models

In this chapter the models for the two primary DUMs that were introduced in Chapter 4 are developed. These are the *Rectifier without PFC* model and the *Active PFC* model. But before we dive into the models themselves, first the requirements of the models are listed and formalized in Section 5.1. In Section 5.2 approaches to making models are categorized in White-, Gray- and Black-box modeling. The way each type of model is constructed is looked into, the principle behind the models and their advantages and disadvantages are explained. After that the models developed in this work are presented and explained. Some of the models (for instance the Gray-box models) can be used for many different DUMs, as they have parameters that can be fitted to an individual DUM. Parameterizing these models however is the subject of Chapter 0.

5.1 Requirements and Considerations for the Models

In the introduction (Chapter 0) the background and purpose of the project was explained and most model requirements that come forth from that have been mentioned already. However, before proceeding with model development, all the requirements and primary and secondary goals are formalized and listed in this section.

The purpose of the models developed in this work is to simulate the behavior and interaction of many DUMs connected to the same power network. To make this possible the models have to be computationally light, as many DUMs will be simulated at the same time.

Most modern electronics, including the SMPS and CFL bulb, contain fast switching circuits, which produce high frequency current emissions, usually between 10 kHz and 100 kHz. However these high-frequency emissions do not propagate far onto the power network, so on the scale of a complete building, they are not expected to contribute to power quality problems. Hence it is not required to model this switching behavior. Note that this makes it significantly easier to make computationally light models as well.

Nonlinear loads on the power network generally have two types of transient currents that can cause interference on the power network. The first type is the inrush current that occurs when the load is switched on or connected. These current transients can be large, but they only happen occasionally and are therefore considered to be only a single disturbance. The second type is the current transients that occur in steady operation, usually twice every 50 Hz period. These current transients are generally much smaller than the inrush currents, but they are produced continuously and synchronously by every nonlinear load that is operational at a given time. This causes these current transients to add up and even influence each other. Therefore these steady state transients are expected to cause a lot more power quality issues than the inrush currents. For this reason, the models developed in this work should accurately simulate steady state operation, while accurately simulating inrush currents is much less important.

Current transients from nonlinear loads on the power network will cause the voltage waveform on the network to be distorted, which in turn will affect the currents drawn by these loads, both in their timing and in their waveform. This interaction needs to be simulated accurately, in order to make realistic predictions on the behavior of the power network. In other words, the model should react realistically to distortions in the voltage waveform.

An office building rarely only has one type of computer and light bulb in it, so to run a realistic simulation of a power network it should contain a multitude of loads. Fortunately most loads can be classified according to their electrical behavior, as is explained in Section 0. The models should be constructed in such a way that, as much as possible, they can be parameterized to represent any DUM in their class. Furthermore, it is not desirable to have to take apart every DUM to parameterize its model, so the parameterization needs to be performed based purely on (non-destructive) measurements.

In summary:

- The models need to be computationally light
- The models do not need to simulate high frequency (> 10 kHz) switching behavior
- The models should accurately simulate steady state behavior, inrush transients are less important
- The model should react realistically to distortions in the voltage waveform
- The model needs to be able to be parameterized to represent a wide variety of DUMs
- The model parameterization should be based on measurement

5.2 White-, Black- and Gray-Box Models

There are many different ways in which models can be constructed. It is quite impossible to provide an exhaustive list, but all models fit in the three categories discussed in this section: white-box, gray-box and black-box.

5.2.1 White-Box Models

These models contain the full design of the DUM. All components, such as transistors, capacitors and so on are present in the model. Even parasitic effects, such as leakage capacities can be taken into account. A common example of such a model is a SPICE model containing a complete design of a DUM.

The advantage of the white-box model is that it provides full insight into why the behavior of the DUM is the way it is. It is also very accurate since all nonlinearities and dynamic behavior can be simulated, and this kind of model is also most likely to respond realistically to unusual circumstances.

The white-box model has disadvantages as well, however. Making it requires intimate knowledge of how the DUM is designed and built. This can be a problem when the manufacturers of a DUM want to protect their intellectual property (IP). Another disadvantage is that these kinds of models are generally large and complex, and take a very long time to simulate. This makes it impossible to simulate large systems that contain many white-box models of sub-systems, or to simulate the interaction between a large number of DUMs.

5.2.2 Black-Box Models

Black-box models are strictly behavioral models. They contain no information on the internal structure of the DUM, and they only describe the behavior on its electrical terminals. These descriptions can be mathematical equations relating voltage, current and time or frequency, or they can contain voltage-current or voltage-time graphs. There can be multiple graphs or equations for different states of the DUM (e.g. a V-t diagram for the transition from a logic low to a logic high state and a separate one for the transition from a logic high to a logic low state). A common example of black-box behavioral models is the IBIS model. IBIS models are commonly used to simulate the behavior of the I/O ports of ICs on a printed circuit board.

There are several advantages to the black-box models. One advantage is that it protects the IP of the manufacturer, since it contains no information about its design. It is also computationally much more simple and efficient than the white-box model. This enables the simulation of large systems with many black-box models, or the simulation of the interaction of many DUMs. In addition, these models can often be constructed from measurement, so that these models can be obtained even if the manufacturer of the DUM doesn't provide them.

The disadvantage is that it is difficult if not impossible to include all the nonlinear or dynamic behavior of the DUM. Usually the behavior of the model is accurate in common situations, but if a situation needs to be simulated that the maker of the model did not foresee, then there is no guarantee the simulation will give an accurate result. For instance, an IBIS model will contain V-I data for up to twice the supply voltage, but it contains no data for when a higher voltage is applied.

At Politecnico di Torino (the Polytechnic University of Turin), there is a research group called the 'EMC group' lead by Prof. F.G. Canavero who has been very active in developing black-box models for I/O ports of ICs, that are more accurate then IBIS models [4][5][6][7][8]. We have asked them to work with us to see if their expertise in modeling of high-frequency I/O ports on ICs allows them to apply their methods to nonlinear loads on the power net. Dr. Igor Stievano from the EMC group has been found willing to work on this.

5.2.3 Gray-Box Models

The gray-box model is a compromise between a white- and a black-box model. It contains some information of the design of the DUM, but only insofar it is relevant to the behavior of the terminals. For instance, the structure of the input or output buffers of a chip might be known, but the inner workings, its signal processing and logical operations are not. In some cases, the knowledge of the design of the DUM contained in the gray-box can be based on what is commonly found in devices similar to the DUM. For instance, in Section 5.4 we will look at a compact fluorescent light bulb (CFL), where we can assume that looking into the DUM from the mains we will first find a series resistor, a diode bridge rectifier, a capacitor and then a load that is fed by DC. The trick is then off course to parameterize the elements correctly, through measurement.

The advantage of the gray-box model is that it can simulate the dynamic and nonlinear behavior very accurately while still mostly hiding the intellectual property of the manufacturer. The models might be more complex than the black-box models, but still much more simple and efficient than the full white-box models. Furthermore, the person making the gray-box model will need to dimension the components in the 'white' part of the model, but he will not need to take into account explicitly all the possible circumstances that the DUM might be subjected to. If the white part is accurate enough, it will respond accurately to any input. This makes it easier to make the model from measurement, since not all unusual circumstances need to be measured, as is the case with a pure black-box model. In addition, this also makes the models more flexible.

The disadvantage is that some knowledge of the DUM is required to select the correct model (e.g. a model for a CFL bulb will not be applicable to a PC power supply with active power factor correction.) It can also sometimes be difficult or even impossible parameterize the model though measurement, depending on the type of DUM.

5.3 Rectifier without PFC, IBIS (Black-Box)

IBIS is an industry standard for modeling nonlinear in- and output behavior of digital IC's. A load on the mains could be viewed as an input port for very low frequencies with a nonlinear behavior. IBIS models use V-I curves to describe nonlinear voltage-current characteristics of inputs. The problem is, the V-I characteristic of the CFL is not only nonlinear, it is also not static. The rising part of the 50Hz sine gives rise to a different VI-curve compared to the falling part of the sine. This is illustrated in Figure 3. IBIS has no specification for this type of behavior. IBIS does support separate V-t curves for output buffers from low-to-high and high-to-low transitions, but not for V-I curves and these V-t curves only apply to signal outputs.

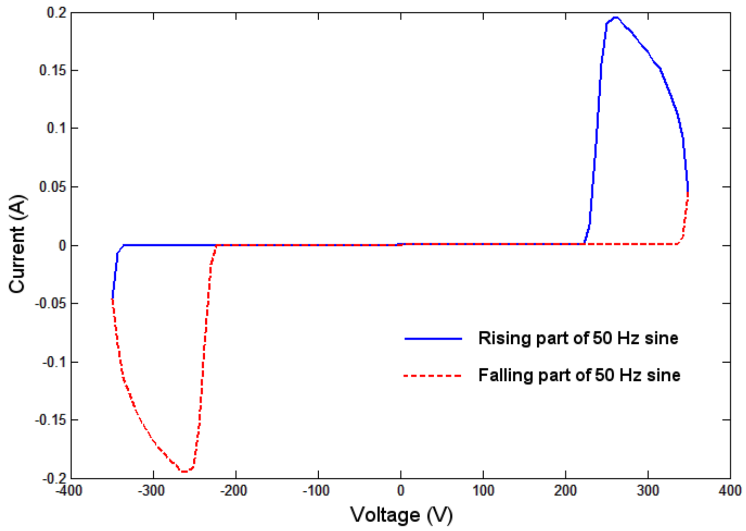

Figure 3: The V-I curve of a CFL lamp is not only nonlinear, but also not static. (plot from simulation, as described in Section 5.4)

Furthermore, it is not likely that a model based on static V-I data will respond accurately to, for instance, an under- or overvoltage. It therefore appears that for this kind of load, IBIS does not provide capable models.

Aside of the V-I curve data, the IBIS model can also contain packaging model information, in the form of an RLC circuit. This means the IBIS model can be used if it is placed behind a rectifier bridge in SPICE, and its packaging section contains the buffer capacitor. The V-I curve would then represent de load behind the rectifier/capacitor. However, this would effectively convert the model into the gray-box model discussed in the next section, because the first few components looking into the DUM are now explicitly modeled.

5.4 Rectifier without PFC, Gray-Box

For appliances in the *Rectifier without PFC* category (see Section 0), the first few components found looking into the appliance from the mains are often well known: a resistor or NTC, a diode bridge, a capacitor and a load. (An NTC is a resistor with a negative temperature coefficient.) In this paragraph it is explained how this knowledge can be used to make a gray-box model of these appliances. In Section 6.1, it is explained how this model can be parameterized through measurement, so that these models can be used without intimate knowledge of the internals of the DUM.

5.4.1 The SPICE Model

In this Section, first the functional schematic is shown, and its operation is explained. After that the actual implementation is SPICE is discussed, since some special care needs to be taken to avoid numerical difficulties that either lead to very long simulation times or even errors.

5.4.1.1 Functional Model Design

The basis of this model is very straight forward. The basic model is a simple circuit, presented in Figure 4.

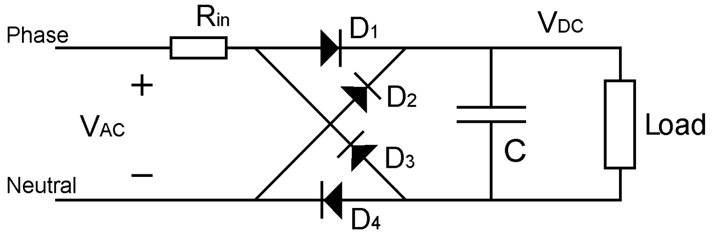

Figure 4: Simplified schematic for the gray-box CFL lamp model

These are the actual components found when you for instance open a CFL lamp and look what is inside, which immediately validates their presence in this model. Except for R_{load}, since it represents the rest of the DUM, and its structure and behavior is unknown. However, since this load is fed by a DC voltage, a series inductance is not relevant, and any shunt capacitance can be taken into account by the C in the schematic. Nonlinear behavior should in most cases not cause too many problems assuming the DUM is in normal operation and the DC voltage is constant enough. To make the model accurate across a larger range of input voltages, it can be examined whether the load is most accurately modeled as a resistor (as seen in Figure 4), as a DC current source, as a load that dissipates a constant power, or with a V-I characteristic.

The value of the load might however change if the DUM consumes more or less power while in different states of operation. This may not be the case for the CFL bulb, but for instance a light dimmer will have a variable load as the light intensity is turned up or down by the user. However, this would affect all behavioral models, and in this model the load can be adjusted easily.

Assessing if the model is valid for the DUM can be done by measuring the current during normal operation, as it will show the current peaks around when the voltage is at its maximum or minimum, as can be seen from Figure 5.

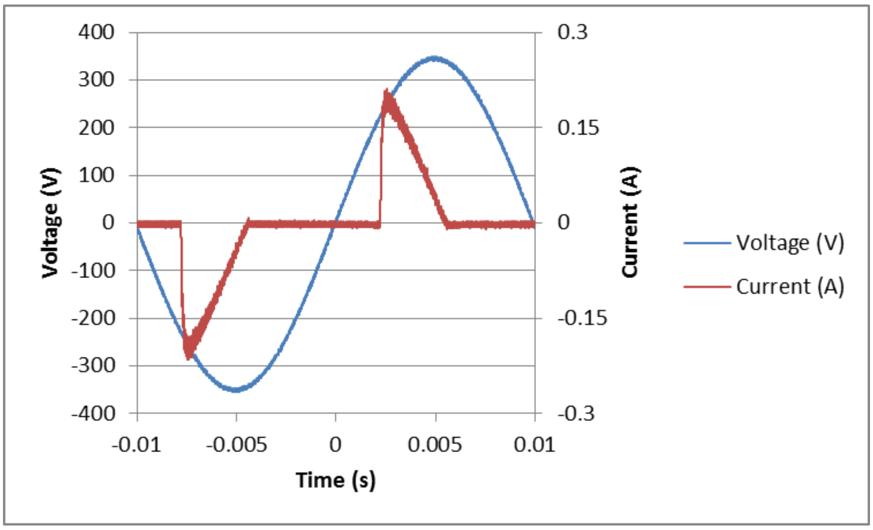

Figure 5: Measurement CFL lamp (By R.B. Timens)

5.4.1.2 Model Implementation in SPICE: Rectifier

When you look closely at Figure 4, you notice that most of the circuit is behind the rectifier, and that neither DC line is directly connected to the reference (ground). While this is the case in reality as well, it is very difficult, if not impossible for LTspice to simulate it in this way. One solution could be to attach the ground reference in the SPICE model to the negative DC line behind the rectifier, instead of to the neutral. This enables the simulation of a single DUM to run, as there are now only a very few components without reference. However this would create a problem if the model is to be used in a larger simulation with a model of the power network with an earthed neutral. In that case, diode D4 would be shorted. So a way needs to be found that allows both sides of the rectifier to be referenced to ground without creating a short circuit and without creating new numerical problems. The circuit that is shown in Figure 6 allows this. It is a modified version of the rectifier used in the Black-Box model developed by I. Stievano, which is discussed in Section 5.6.

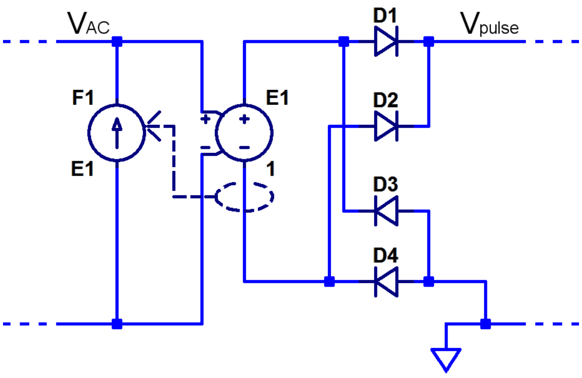

Figure 6: SPICE Implementation of the rectifier. The dashed arrow is only an illustration of the dependency

The circuit contains of a voltage controlled voltage source that feeds the voltage information to the diode bridge. There is also a current controlled current source, which feeds back the current emission from the diode bridge to the AC part of the circuit. The dashed arrow with loop is only an illustration that graphically shows the dependency of the current source. This circuit de-couples the

AC and DC parts of the model, allowing them both to be referenced to ground, while minimizing the poorly referenced part of the circuit, and without changing the behavior of the model.

5.4.1.3 Model Implementation in SPICE: Load

Loads in the *Rectifier without PFC* category do usually not act as a linear resistor. In the case of an SMPS without PFC, the load acts as a constant power dissipating load, while the CFL bulb draws a constant current almost irrespective of input voltage. It should be noted, that when the input voltage amplitude during simulation is the same as the voltage that was used during the parameterization process (see Section 6.1) then it does not really matter what kind of load is used. However, when over- and under-voltages are simulated, then the correct type of source should be used in the simulation.

In the SPICE implementation, all three variants are modeled in parallel, as is illustrated in Figure 7. The loads that are not in use are simply given a default value (see below the loads in the Figure) that causes them to draw only a negligible amount of current or no current at all.

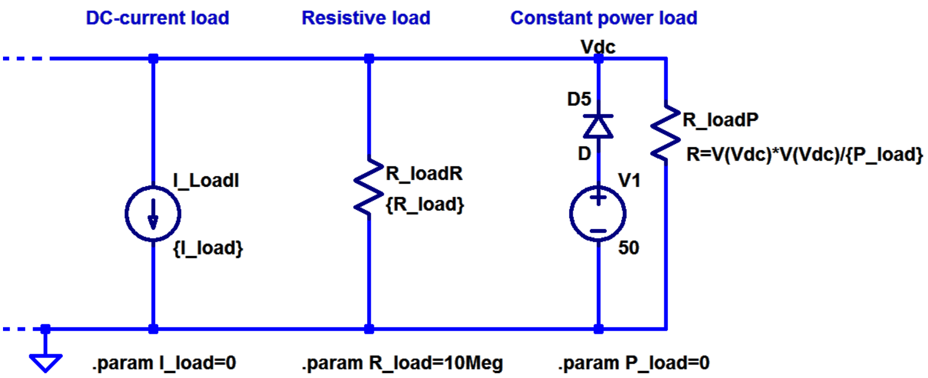

Figure 7: SPICE Implementation of the loads

Special care is taken of the constant power load. This load is modeled using a behavioral resistor, with the following resistor value:

$$R_{loadP} = \frac{V_{DC}^2}{P_{load}}$$

Where P_{load} is a parameter chosen by the user. Modeling the load in this way however creates a numerical problem when the simulation starts. When V_{DC} is still 0 V, this resistor would draw an infinite current. To prevent this problem, a DC voltage source (labeled 'V3') and a diode is placed in parallel (see Figure 7), which makes sure V_{DC} is always at least 50 V. This is less than any normal operating voltage, even if V_{AC} is only 115 V_{RMS}, but it is enough to prevent numerical problems.

5.5 Active PFC, Gray-box

In this section a gray-box model of the switched mode power supply with active power factor correction is developed. First the DUM is taken apart and the schematic of the input circuit is presented, its operation is explained and the challenges with developing a low-frequency gray-box model are briefly considered. After that, two approaches are taken to develop a low-frequency gray-box model of the SMPS with active PFC. In the first approach, only basic spice components are used, just like has been done for the *rectifier without PFC* model in the previous section. This approach however, proves to be unfeasible due to the complexity of the DUM. In the second approach a clean measured current waveform is taken to represent the basic static operation of the DUM, which is then combined with gray-box elements in SPICE to add the dynamic behavior.

5.5.1 Active PFC: Schematic and Operation

When trying to make a gray-box model of the SMPS with active PFC, we first need to find out how its input circuit looks, i.e. the first section of the circuitry looking into it from the mains. To this end, the BeQuiet PC power supply has been opened and its circuitry has been examined. The most interesting part of this circuitry is shown in Figure 8. Note that the inductors in the line filter are not considered interesting, because they are designed to filter only high frequencies, in which we are not interested for this model. The capacitance in the line filter however draws a reactive current, so the capacitance is included.

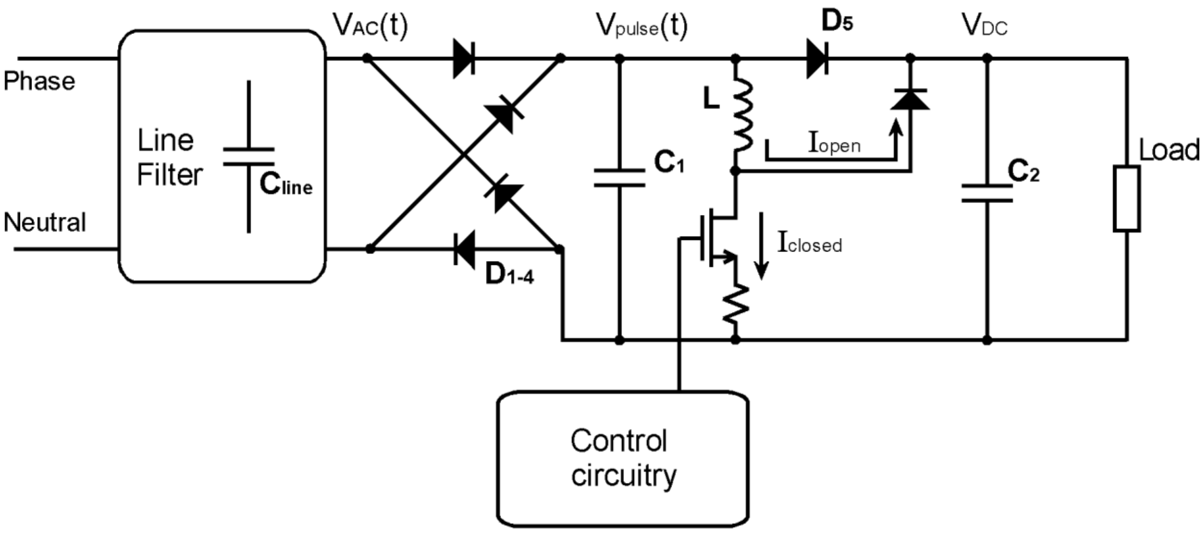

Figure 8: Input circuit found in the Be Quiet! SMPS

The basic operating principle of the circuit can be deducted from this schematic. The function of an active PFC is to draw a current proportional to the input voltage. This means that a current needs to be drawn across the rectifier bridge, even if the absolute value of the voltage to the left of it, $|V_{AC}(t)|$, is lower than the DC voltage on the right, V_{DC}.

This is how it works: The transistor acts as a switch. When it is closed, a current will flow through the switch and though the inductor (I_{closed}), as long as $V_{pulse}(t)$ is greater than 0 V. (note that $V_{pulse}(t) \approx |V_{AC}(t)|$.) A moment later, the switch will open. However, an inductor, having stored magnetic energy, will try to keep the current flowing. But since the switch is now open, the only way for the current to flow is through the diode on the right (I_{open}), and into the buffer capacitor C_2. This way, a current can be "pumped" from the AC side of the circuit to the DC side of the circuit, even if $|V_{AC}(t)| < V_{DC}$.

This circuit is called a boost converter [19].

Challenges in Developing a Low-Frequency Gray-Box Model

Now from the perspective of modeling this device, there are two main challenges. The first challenge is that the circuit contains a control loop. This control loop needs to be modeled, because it directly controls the current waveform that our model needs to generate. However, the implementation of the control circuit in the DUM is impossible to find out from the DUM because it contains a chip that is not labeled, and is therefore an unknown model. We can deduce however that there are at least three factors that affect this control circuit and the resulting current [18]:

- The purpose of the PFC is that the current is made proportional to the instantaneous input voltage. This means that $V_{AC}(t)$ or $V_{pulse}(t)$ needs to be an input for the control circuit.
- The DC voltage, V_{DC}, needs to have the correct value. Note that V_{DC} could become infinitely large, if the current pumped into buffer capacitor C_2 is greater than the current that the load draws. To prevent this, V_{DC} needs to be an input factor for the control circuit as well.
- Finally the instantaneous voltage difference between V_{DC} and $V_{pulse}(t)$ will influence the maximum current the circuit can pump, due to physical limitations.

All these factors need to be correctly modeled in order to obtain an accurate model.

The second challenge to modeling this device, is that the model as depicted in Figure 8 is a high-frequency model. The switching frequency of this circuit appears to be about 55 kHz, based on measurement. This makes the model very computationally intensive to use, while one of the major requirements of the model is to make it computationally light, so that for instance the interaction of many DUMs can be simulated. This means that a low-frequency equivalent model needs to be developed that takes all the aforementioned aspects into account, without actually simulating the high-frequency switching behavior.

5.5.2 Modeling Using Basic SPICE Components

Figure 9 shows the basic functional schematic of the low-frequency model. The top half is the PFC circuit, and the bottom half is the control circuit. The reason there are two voltage controlled current sources is because apart from of the current pumped into the buffer capacitor C_2, during the time the switching transistor in Figure 8 is closed, a current will also flow directly down to the negative DC line.

The control circuit as depicted in Figure 9 is based on [18]. V_{REF} is the reference voltage that the DC voltage should follow. The voltage error amplifier then makes a voltage V_{ERR} as a function of the DC voltage and V_{REF}. To let the current follow the voltage waveform, which is what a PFC is supposed to do, V_{ERR} is multiplied with V_{pulse}. This way, a current will be drawn with the shape of the input voltage, but scaled so that the DC voltage is kept at the correct value.

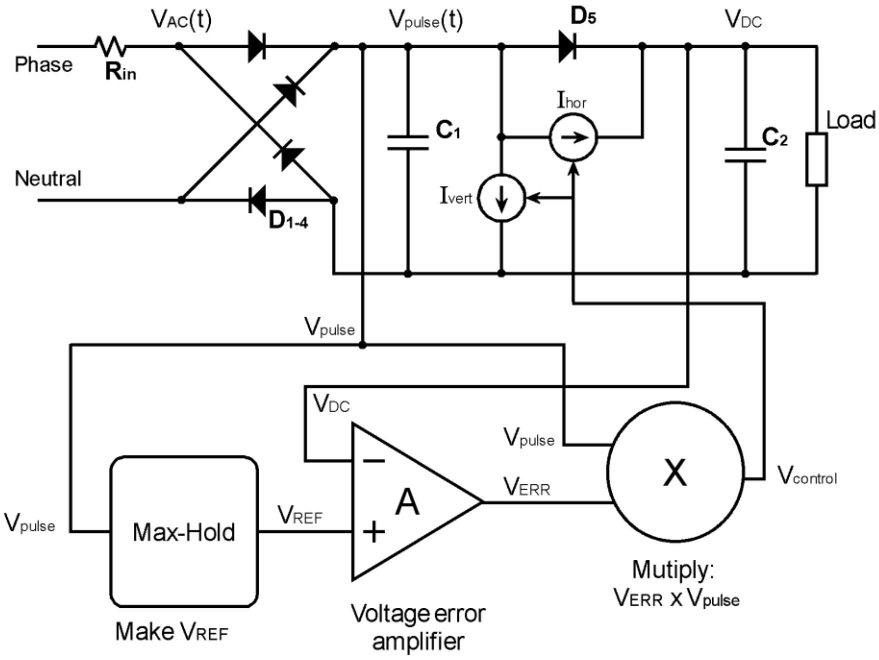

Figure 9: Current functional implementation of the active PFC model. [18] Served as reference.

Figure 10 shows the implementation of the control circuit in SPICE. The multiplier on the right works using a SPICE trick: it is an operational amplifier implemented as a voltage controlled voltage source, with the approximate transfer function:

$$V_{OUT} \approx \frac{R_2 + R_1}{R_1} V_{IN}$$

Substitute R_1 = 1 and R_2 = V_{ERR} (That's the SPICE trick, making it a behavioral resistor), the transfer function becomes:

$$V_{OUT} \approx \frac{V_{ERR} + 1}{1} V_{IN} \approx V_{ERR} V_{IN}$$

For V_{ERR} >> 1.

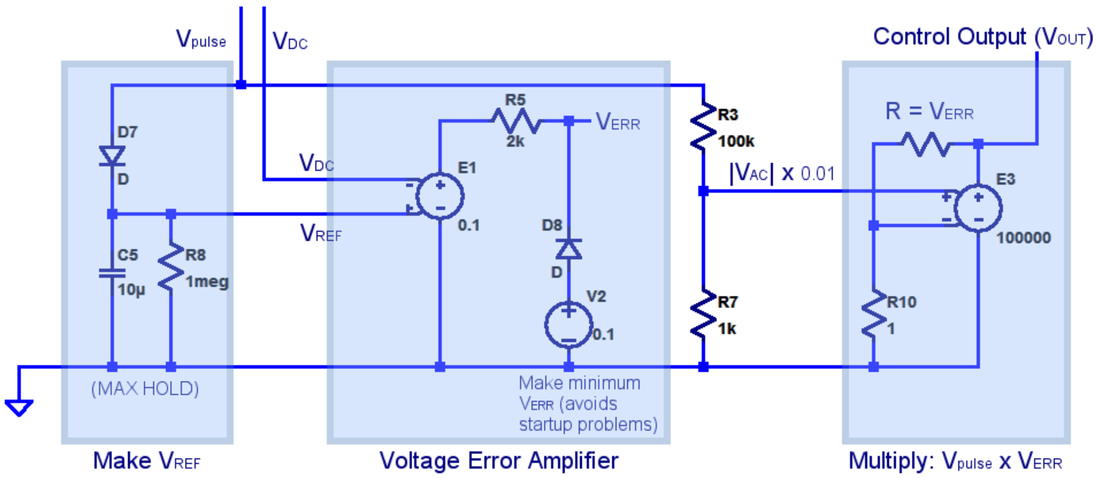

Figure 10: Current detailed implementation of contol circuit model

Preliminary Simulation

In Figure 11 the active PFC is simulated and compared to a measurement obtained with a clean sinusoidal voltage without distortion. It can be seen here that the current waveform does not resemble the measured one. It appears that modeling the active PFC with its physical properties translated to a low frequency, and with its unknown control loop configuration may not be feasible. In addition, changing component values sometimes inexplicably results in numerical errors in SPICE. The biggest problem may however be that with the considerable complexity of the SMPS there are many different topologies which produce very different current waveforms. This has been illustrated in Figure 12, where measurements of two different DUMs with active PFC are put next to each other. So making a model that fits many different DUMs this way is impossible. For this reason another approach is looked into, which is presented in the next section.

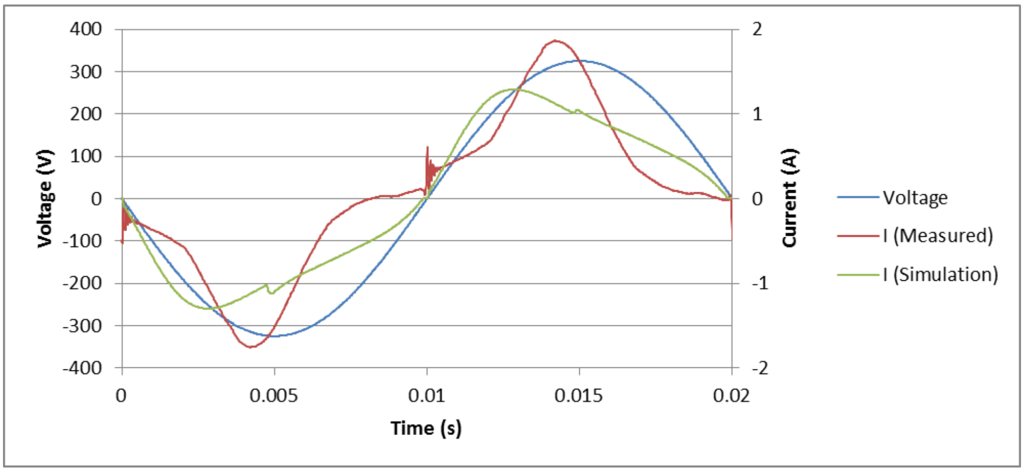

Figure 11: Simulation versus measurement, SMPS model

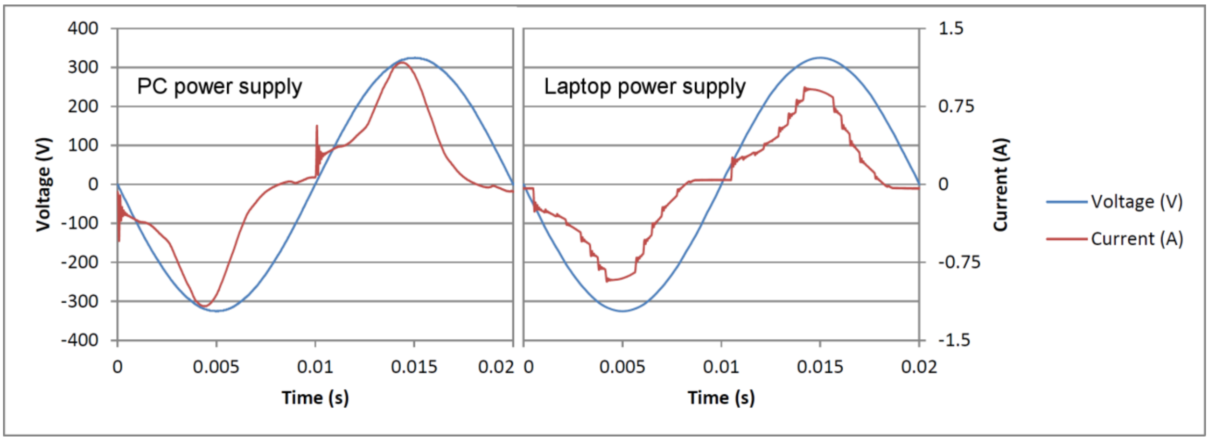

Figure 12: Current waveforms of two different DUMs with active PFC. Laptop power supply is treated in Section 8.4.2.

5.5.3 Modeling Using a ‘Prototype’ Current Waveform

In this section, another approach is explored to model the active PFC. The basis for this model is a measured current waveform in combination with a gray-box style SPICE input circuit. The idea is that the measured current waveform defines the basic static behavior of the active PFC, while the rest of the circuit adapts the current waveform to make it react dynamically to the voltage waveform and load.

First its functional design is explained, starting with a simple model, after which then several elements will be added to make the model more accurate, including a simple control loop which is still required for this model. After that the exact implementation in SPICE is presented. The final model and its parameters are then presented, where the impact and importance of the various parameters of the model are explored. Lastly, some aspects and properties of the model are looked into, such as performance and startup effects of the model.

5.5.3.1 Functional Model Design: Basic Model

Figure 13 shows a simplified functional schematic of the *Active PFC* model. The current sources that were controlled in Figure 9 by a control circuit now simply repeat a measured current waveform infinitely. This measured current waveform is shown in Figure 14 and is called the prototype current waveform. It is the current that was measured with a clean 230 V_{RMS}, 50 Hz sine, with the load dissipating 150 W. Note that since the prototype current sources are behind the rectifier, they only have to repeat one positive current peak.

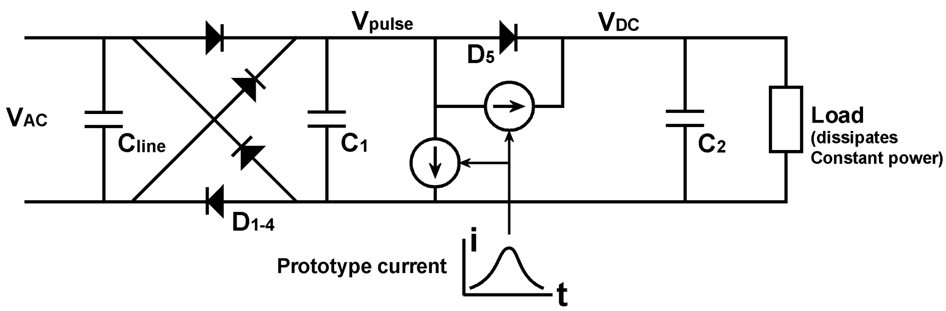

Figure 13: Simplified functional schematic of the SMPS model

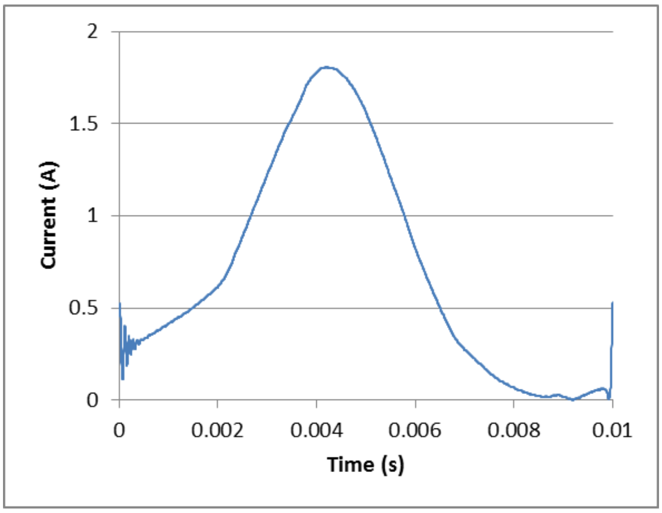

Figure 14: Prototype current: absolute value of the measurement using a clean 230 V_{RMS}, 50 Hz sine voltage

5.5.3.2 Functional Model Design: Prototype Current and Control Loop

While the model as it is presented in Figure 13 will respond accurately to distortions in the voltage, the model cannot respond realistically to a change in RMS voltage and it can only model one value for the load, since the current magnitude of the prototype current is fixed. To make the model more adaptive, a control loop has to be incorporated. But before this can be done in a meaningful way, first the load and DC voltage on the right (V_{DC}) needs to be looked into.

As the SMPS is supposed to provide a constant power to the PC regardless of the input voltage, it is convenient to model the load in such a way that it will dissipate a constant power. This value for power is not necessarily part of the model itself, like the value of a capacitor. It will be a parameter that is set by the user of the model in many cases. This is because the load can be considered to be a property of the environment of the SMPS, and not part of the SMPS itself.

The value of V_{DC} in the actual DUM is at least somewhat larger than $\hat{V}_{pulse}$, where $\hat{V}_{pulse}$ denotes the amplitude of V_{pulse}. (Note that $V_{pulse} \approx |V_{AC}|$). This can be seen from the presence of diode D_5 in Figure 15, which is an actual component present in the DUM. If V_{DC} was smaller, then an additional narrow peak should have been visible in the current measurement at the instance the diode would conduct. The absence of this peak means that, in steady operation, the diode is always reverse biased and V_{DC} is larger than the amplitude of V_{pulse}. However, the exact value of V_{DC} is unknown. For the model the choice has been made to create a reference voltage that is 10% higher than the amplitude of V_{pulse}, which the control loop will attempt to let V_{DC} follow. The choice for the DC voltage should not affect the behavior of the models at the terminals, provided diode D_5 will not conduct. This is explained in Section 5.5.3.7.

The reference voltage V_{REF} is created by a max-hold circuit and an ideal amplifier with amplification A = 1.1, as can be seen in Figure 15.

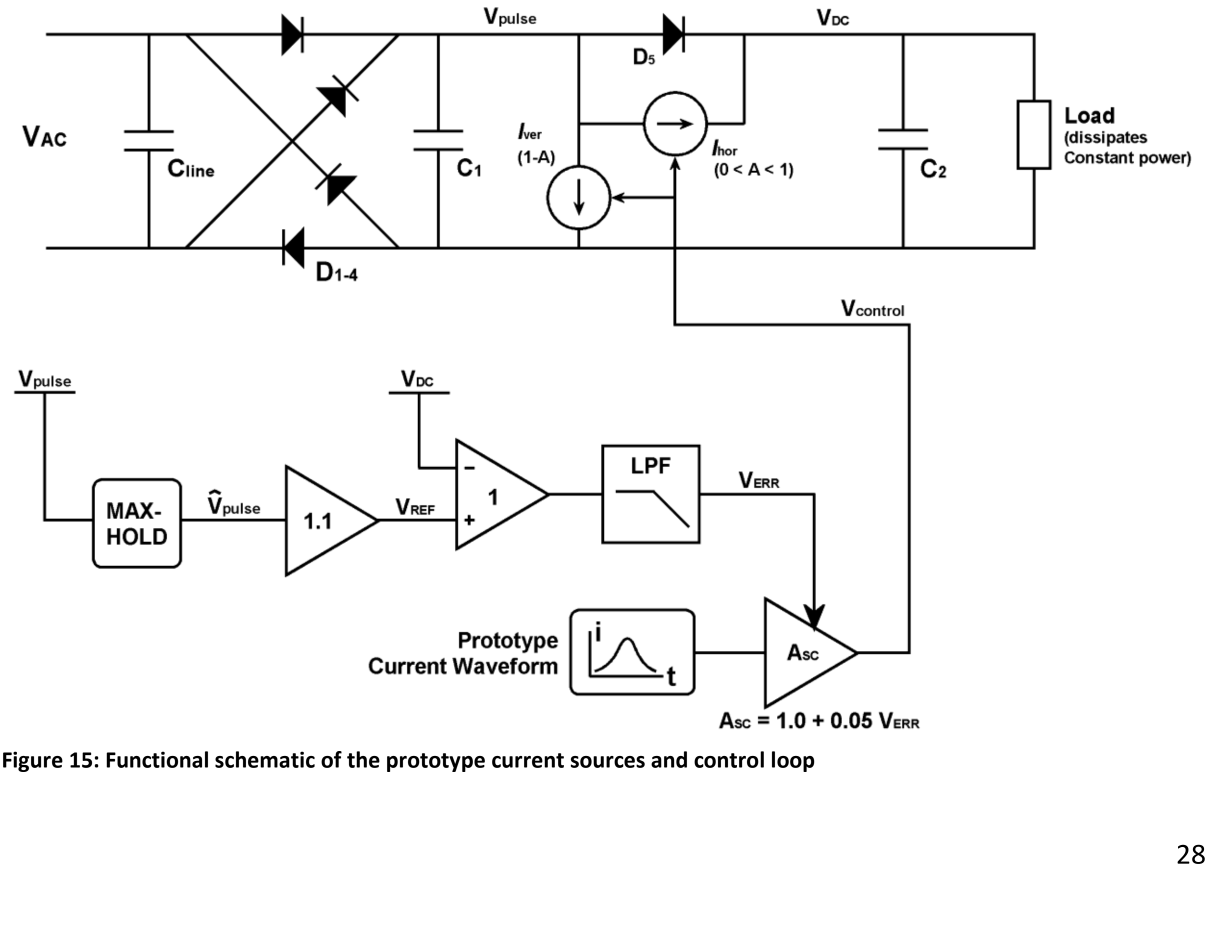

Figure 15: Functional schematic of the prototype current sources and control loop

The control loop will attempt to make the DC voltage V_{DC} follow the reference voltage V_{REF}. Since the power dissipated in the load is an external parameter, the only way to control the voltage is to scale the prototype current waveform. To this end, a voltage error amplifier is implemented. Its output is $V_{REF} - V_{DC}$ and this is then low-pass filtered to create V_{ERR}. The low-pass filtering is to ensure that the ripple on V_{DC} does not directly influence the current waveform, so it will adjust the current amplitude over several 50 Hz periods. This is common practice in the control loop of an SMPS according to [18]. The prototype current waveform is amplified by A_{SC}, and the signal that results goes to the controlled current sources. Note that A_{SC} is not a constant, but it is a function of V_{ERR}. It controls the feedback amplification, i.e. how aggressively the current sources react to V_{ERR}, and at what value of the load power, the V_{ERR} should be 0. It has the form

$$A_{SC} = a + b\, V_{ERR}$$

It is desirable to let V_{ERR} be zero under typical load and input voltage conditions. This means that in case of a well-chosen prototype current measurement, a should be 1. The value of b determines how much the current magnitude is influenced by V_{ERR}. On one hand, a high value will let V_{DC} approach V_{REF} more closely. But on the other hand, the low-pass filter in the voltage error amplifier causes V_{ERR} to respond slowly, so a high value of b can result in too much overshoot or even slow oscillations in V_{DC}. Default values: $a = 1$ and $b = 0.05$.

The result, $V_{Control}$, is sent to the two prototype current sources, I_{hor} and I_{ver}. The reason for the second, vertical current source (I_{ver}) was already explained in Section 5.5.2; while the switching transistor is closed, a current flows directly to the negative DC line. But another useful way to look at it is that the horizontal source pushes current from a low voltage to a high voltage, which means it delivers power into the circuit. This cannot be right, because all the power should come from the mains. So the vertical current source is there to sink the same amount of power that the horizontal source delivers into the circuit. The current magnitude of both sources should in general not be equal however, as the voltage across them is not equal either.

It turns out to be cumbersome to analytically determine what the ratio the two magnitudes should be. This is because both the voltages across the sources and their currents are all pulsed, and all have different waveforms. Furthermore, the current waveform will be unique to every DUM, so a general number that fits all DUMs cannot be given. And finally, even if this ratio is correctly calculated, it needs to be changed again because the efficiency of an SMPS is less than 100%. The efficiency itself would be a measured quantity, since it is for a large part determined by the black-box part of the model. The most straightforward way to obtain a value is therefore to manually match simulation with measurement. How this is done is explained in Section 6.2, and in the manual in Section 9.2 (Step 2).

It is desirable that the sum of the amplification of both voltage controlled current sources is unity, so that here is no hidden amplification in this part of the circuit. So if the horizontal source has amplification A, then the vertical source should have $1 - A$, where $0 < A < 1$.

Note that the ratio is independent of the input voltage or V_{pulse}, because we choose V_{DC} to be 1.1 times $\hat{V}_{pulse}$, rather than for instance $\hat{V}_{pulse}$ + 10 V. This gives $\hat{V}_{pulse}$ and V_{DC} a fixed ratio, which makes the ratio of the amplification factors of the current sources also fixed. This enables the model to adapt the current it draws automatically to the input voltage. This mechanism does however assume a constant efficiency, which in general actually changes with different input voltage or load.

5.5.3.3 Functional Model Design: Capacitor Compensation

As can be seen in Figure 13, the prototype current sources are placed behind a capacitor, rectifier and another capacitor. The reason the rectifier and capacitors are present in the model is to capture the dynamic behavior of the active PFC. It turns out that the capacitively loaded rectifier determines for a large part how the active PFC responds to distortions in the voltage waveform, just like with the CFL bulb. However, these capacitors also introduce a problem; the prototype current waveform has been measured at the mains, to the left of the rectifier and capacitors, while it is used in this model on the right, behind the rectifier and capacitors. The capacitors have an influence on the current waveform, which needs to be compensated for, otherwise their effect would be present twice; once because the components are there in the SPICE model, and once because their effect is already included in the prototype current waveform.

Without compensation, there is a period of zero current near the voltage zero-crossing and sudden step in the current a little later, which is not observed in measurement (see Figure 16, left). This happens because the capacitor C_1 in the simulation is not empty when the input voltage approaches zero, making V_{pulse} higher than $|V_{AC}|$, causing the current through the diode bridge to stop, until $|V_{AC}|$ is higher again. In addition, the capacitors cause a phase shift in the current waveform.

There are two possible solutions to this problem. The first solution is to add another current source (See Figure 17, left) that draws the opposite current of the sum of the current that went in and out of both capacitors during the prototype measurement. This current waveform is shown in Figure 17, on the right. This current compensates the phase shift, and causes the capacitor C_1 to be empty near the zero crossing, so that the unwanted zero current time and consequently the sudden step in the current are nearly gone (see Figure 16, right). The effect that the capacitor has on the dynamic behavior of the model is however retained, as can be seen from the distortions in Figure 16, especially after the zero-crossing. This is because the capacitor currents will respond to distortions in the input voltage, while the current source that compensates for the capacitor has a fixed current waveform which will not respond. The response of the capacitor currents to voltage distortions should not be affected by the compensating current source due to the superposition principle that applies to linear components such as capacitors.

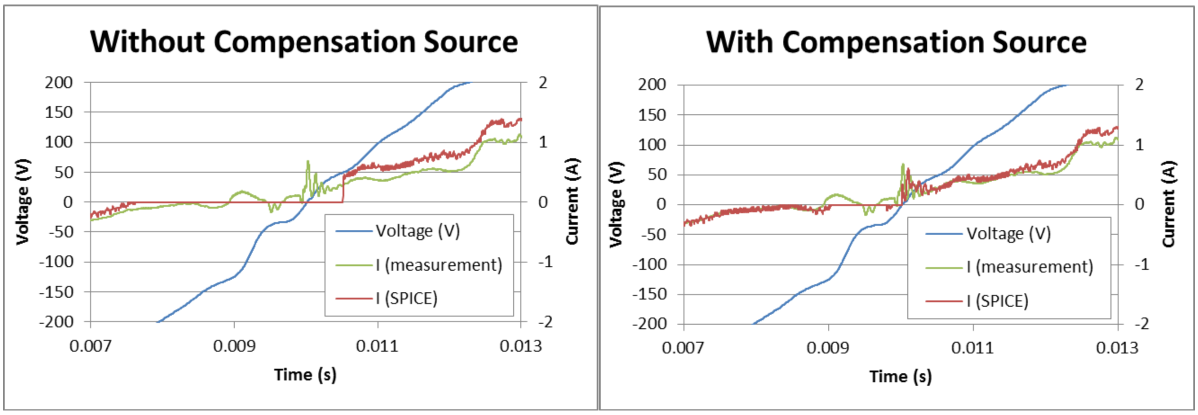

Figure 16: Effect of capacitor compensation on SMPS simulation, and comparison with measurement with Carré building voltage (Detail). C_{line} **is zero to better illustrate the effect.**

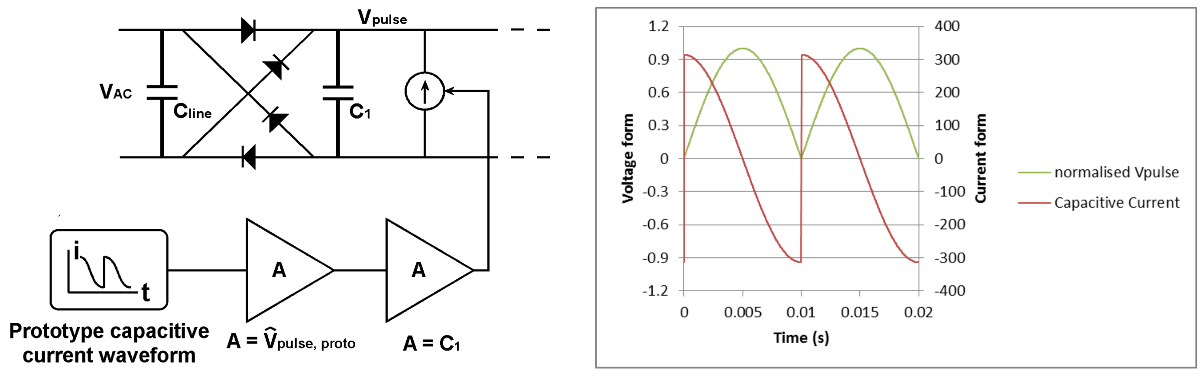

Figure 17: Functional schematic of capacitor compensation. Left: Functional schematic, Right: prototype capacitive current waveform (V_{pulse} plotted in the same figure for visual reference only)

Figure 17 shows the functional schematic of this solution. The basic current waveform, which is loaded from file, is constructed assuming unity voltage amplitude, a capacitor value of 1 Farad, and a 50 Hz net frequency. This waveform is then multiplied by $\hat{V}_{pulse,proto}$ (which is the $\hat{V}_{pulse}$ during the prototype measurement), and by the value of $C_1 + C_{line}$. This way the current wave form magnitude matches the ideal capacitor current for the correct input voltage amplitude and actual capacitor size. This setup makes this solution flexible with respect to the input voltage amplitude that was used during the prototype measurement, as well as capacitor size.

The disadvantage of the above solution is that it makes the model more computationally heavy. The second solution is therefore preferred, where the capacitor current as it occurred during the prototype current measurement, is simply subtracted from the prototype current in the prototype current file. This way, the current is compensated for without adding extra complexity to the model. However, the values of C_1 and C_{line} need to be known for this. How to obtain these values is explained in Section 6.2, and also in the manual in Section 9.2, where it is also explained how the prototype current file can be adapted.

5.5.3.4 Model Implementation in SPICE: Prototype Current and Control Loop

In the previous sections we looked at the functional and mathematic design of the model. In this section and the next few sections it will be shown how the model is implemented in SPICE. First we will look at the control loop and the main prototype current sources.

The control loop is shown in Figure 18, and the signal flow is from left to right. First on the left is the max-hold circuit, which gives an output voltage about equal to the amplitude of V_{pulse}. The reference voltage needs to be 10% higher than this, so an ideal amplifier is used to make V_{REF}. The max-hold circuit discharges slowly across R_2 (10 MΩ), so that V_{REF} is adjusted when the input voltage changes during simulation.

The error voltage amplifier is again implemented by an ideal amplifier, with amplification 1. There is a 1st order low-pass filter at its output that suppresses the ripple on the signal V_{ERR}. The resistor, R_{LPF}, is a behavioral resistor, which has a low value (10 Ω) for a few milliseconds at startup, and is 10 kΩ the rest of the time. This is so that the low-pass filter is disabled at startup so that V_{ERR} will have the correct value almost instantly, instead of having to wait till the capacitor C_{LPF} is charged up and causing the model to draw a much too large current for the first couple of 50 Hz periods. The value of R_{LPF} is being controlled as follows. It has value that is a function of the voltage $V_{startup}$ (highlighted in green). It is 10 kΩ when $V_{startup}$ is 0 V and 10 Ω when $V_{startup}$ is 1 V. V_{starup} is simply created by a voltage source that only gives a short 1V pulse at startup, as can be seen in Figure 18.

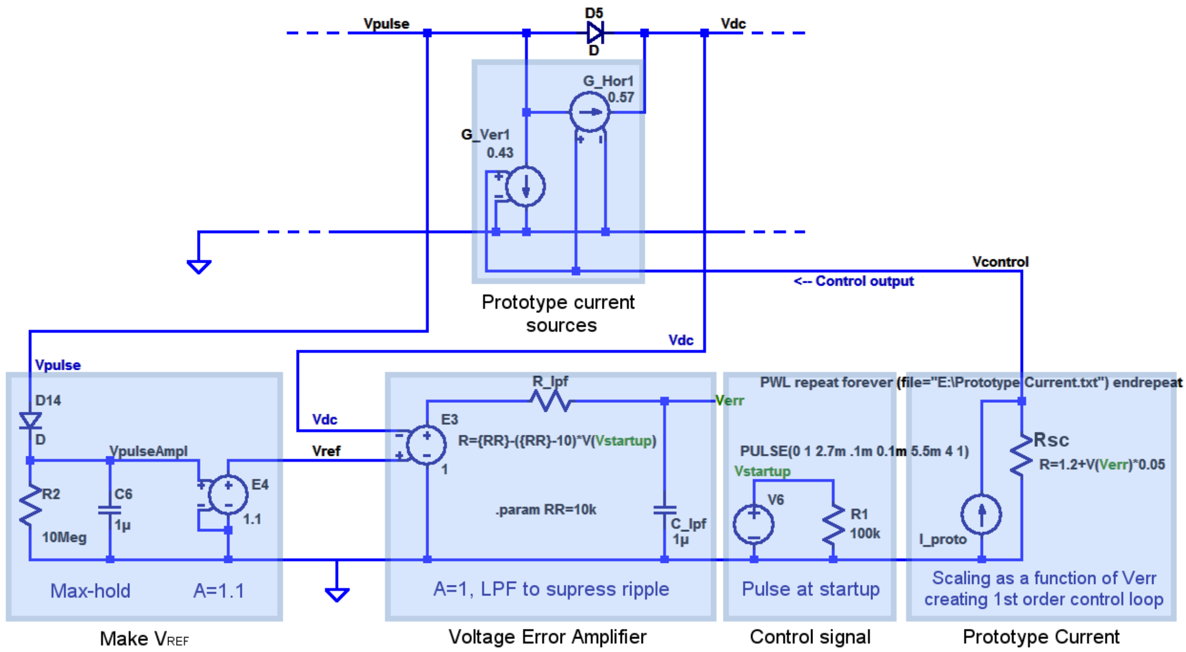

Figure 18: SPICE implementation of the SMPS control loop model. The labels highlighted in green show the relationships between the behavioral resistors and the voltages they depend on.

All the way on the right in Figure 18, there is a current source that reads the prototype current waveform from file and repeats it forever. The current is scaled and converted to a voltage by the resistor R_{SC} to the right. This resistor is also a behavioral resistor, and its value is a function of V_{ERR}, specifically,

$$R_{SC} = A_{SC} = 1 + 0.05 \cdot V_{ERR}$$

This equation controls some of the important feedback properties of the control loop and is explained in Section 5.5.3.7.

One remark on the prototype current file needs to be made. In case of a 50 Hz power network, the prototype current waveform file should be (a multiple of) 0.01 seconds long. When LTspice repeats a PWL file however, it seems to fuse the first and last points of the file together. This means that the last point in the file should have time stamp 0.01 and not 0.01 minus one time step. (e.g. the last point should be 0.01 and not 0.00998 in case of 10 µs time steps.) If this is not done correctly, the timing will be off significantly after several periods.

5.5.3.5 Model Implementation in SPICE: Load

An SMPS needs to deliver a constant power to the appliance it provides power for, regardless of input voltage or power quality. Because of this the load is modeled in such a way that it sinks a constant power, which is a parameter that can be defined by the user of the model. This is done using a behavioral resistor, with the following resistor value:

$$R_{loadP} = \frac{V_{DC}^2}{P_{load}}$$

Where P_{load} is a parameter chosen by the user. Modeling the load in this way however creates a numerical problem when the simulation starts. When V_{DC} is still 0 V, or close to it, this resistor pulls an enormous current that the control loop cannot handle. To prevent this problem, a DC voltage source (labeled 'V3') and a diode is placed in parallel (see Figure 19), which makes sure V_{DC} is always at least 100 V. This is less than any normal operating voltage, even if V_{AC} is only 115 V_{RMS}, but it is easily enough to prevent numerical problems.

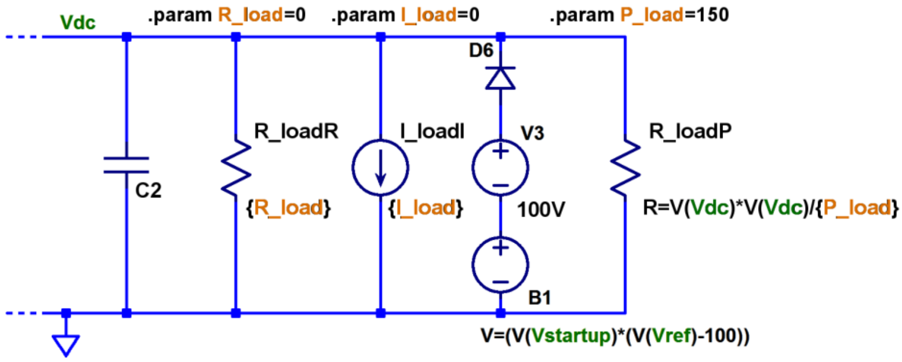

Figure 19: SPICE implementation of the load dissipating a constant power. (Green: dependent voltages, orange: user parameters)

The main difference in the load implementation with the *Rectifier without* PFC model is the presence second voltage source (labeled 'B1' in Figure 19). It is there to shorten the startup effects of the model. $V_{startup}$ is a control voltage that is 1 V for a few milliseconds during the first 50 Hz period of the simulation. This causes B1 to push V_{DC} to up to V_{REF} during that time, which charges C_2 up as fast as V_{REF} reaches its target voltage. This in turn allows the control loop to find its equilibrium much faster.

The other two loads, R_{loadR} and I_{loadI} are there to model resistive and DC current type behavior, respectively.

5.5.3.6 Model Implementation in SPICE: Rectifier

It can be seen from Figure 13 that just like with the *Rectifier without PFC* model, most of the circuit is behind the rectifier, and neither DC line is directly referenced to ground. While this is the case in reality as well, it is impossible for LTspice to simulate it in this way. The simulation stops with a "Time step too small" error. One solution could be to move the ground reference in the SPICE model to behind the rectifier. This enables the simulation of a single DUM to run, as there are now fewer components without reference. But even then the simulation often slows down to an unacceptable degree and the same error still occurs on occasion. Moreover, this would create a problem if the model is to be used in a larger simulation with a model of a power network with an earthed neutral. In the latter case, diode D_4 would be shorted. So a way needs to be found that allows both sides of the rectifier to be referenced to ground without creating a short circuit and without creating new numerical problems. For this reason, the same circuit as described in Section 5.4.1.2 for the *Rectifier without PFC* model is used, which is repeated in Figure 20. This is a modified version of the rectifier used in the Black-Box model developed by I. Stievano, which is discussed in Section 5.6.

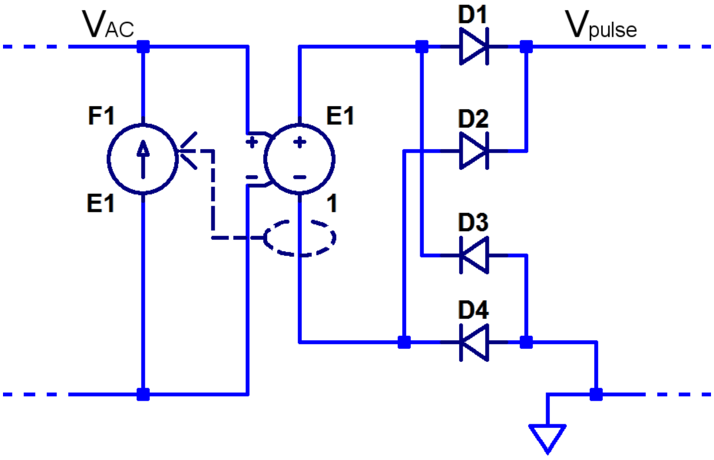

Figure 20: Implementation of the rectifier in SPICE. The dashed line is only an illustration of the dependency (Same as Figure 6)

The circuit contains a voltage controlled voltage source that feeds the voltage information to the diode bridge. There is also a current controlled current source, which feeds back the current emission information from the diode bridge to the AC part of the circuit. The dashed arrow with loop is only an illustration that graphically shows the dependency of the current source. This circuit de-couples the AC and DC parts of the model, allowing them both to be referenced to ground, while minimizing the unreferenced part of the circuit and without changing the behavior of the model.

5.5.3.7 Overview and Parameters of the Model

At first glance the model seems very complex, with many component values and parameters to choose. For this reason this section will look into the various parameters and will explain how they affect the model or the simulation. Many parameters turn out to be not very critical and can generally be left to their default value for any DUM. To give a complete picture of the model in Figure 21 the complete spice implementation is shown.

The parameters and component values that need to be chosen carefully are listed below. Note that this section doesn't explain how to find the correct values for the model. This is done in Sections 6.2 and 9.2.

- Prototype waveform: This waveform should be obtained by a clean measurement (i.e. using a 230 V_{RMS}, 50 Hz sine voltage without distortion), and modified as explained in Sections 6.2 and 9.2. The best results are expected when the measurement is performed with a typical or average load and RMS voltage. This is because the more the load and RMS voltage in the simulation differ from the conditions used during measurement, the less accurate the model is expected to be.
- C_1 and C_{line}: These component values affect how sensitive the current waveform is to distortions in the voltage waveform. C_1 only contributes when the diode bridge is conducting, which it usually stops doing as the input voltage approaches zero, while the effect of C_{line} is always visible. C_{line} also determines the current value near the zero crossing when the voltage is clean.
- *Amplification factors of the prototype current sources*: indirectly determine the efficiency of the model; that is, the ratio between the power drawn from the mains and the power dissipated in the load. An efficiency of > 100% is possible if they are chosen incorrectly.

- Load: In many cases this is a parameter of the environment of the DUM, but in some cases, such as with fluorescent tubes which are rated more than 25 W, the SMPS is integrated with its load, and the load can be seen as a parameter of the DUM itself.

The following parameters have little or no direct effect on the steady state behavior of the model when they are chosen within certain bounds that will be highlighted.

- R_{in}: This component should have a value of less than 20 Ω. It is explained in Section 6.2 that in the input impedance of the DUM/model for frequencies of up to several kHz, the capacitors are dominant, meaning that the exact value of R_{in} is not too critical. (This in contrast to the *rectifier without PFC* model where R_{in} definitely *is* critical!) Increasing R_{in} can suppress high frequency current noise a little that is a result of noise in the voltage waveform. However a too high value will influence the control loop to draw more current, and makes the startup effects last longer. Hence the recommendation to keep R_{in} below 20 Ω. Default value: 10 Ω.
- The resistors around the C_{line} capacitor are just to prevent numerical problems in SPICE, and hence should have a low value, i.e. 1 or 0.1 Ω.
- C_2 (buffer capacitor): This component affects the ripple on V_{DC}, and the inrush current upon startup. The ripple on the V_{DC} has no direct influence in the current waveform as it is filtered out by the low-pass filter in the control loop. It does however affect the response time of the control loop. Default value: 120 µF.
- RC time of the low-pass filter in the Voltage error amplifier: A short RC time will regulate the DC voltage to its desired value quickly, but the current waveform will be influenced by the increased ripple on the V_{ERR} signal. A long RC time will cause the control loop to react slowly and might cause overshoot in the DC voltage, and it will take a long time for V_{DC} to settle on the desired value. Note that the value of C_2 also influences how quickly the control loop responds. Default values: 10 kΩ · 1 µF = 10 ms, i.e. the RC time is half the period of the 50 Hz sine.
- V_{REF}: Changing V_{REF} (i.e. the voltage that V_{DC} will attempt to follow) does not change the behavior of the input current of the model at all, provided that
    - V_{DC} is always greater than the amplitude of V_{pulse} at all times, otherwise diode D_5 will conduct
    - The amplification factors of the horizontal and vertical current sources are modified accordingly
    - The power dissipated in the load will remain the same

  Note that the inrush current will be affected, as more charge will flow into the buffer capacitor C_2 when the voltage is higher, though this can also be compensated for by changing the value of C_2, again provided the power dissipated in the load will remain the same. By default, $V_{REF} = A_{REF} \cdot \hat{V}_{pulse}$, with $A_{REF} = 1.1$.
- RC-time in the max-hold circuit: the max-hold circuit should provide a stable voltage, as ripple-free as possible. However, when the RMS voltage is expected to change during the simulation, the RC time should be shorter so that V_{REF} will adjust itself dynamically to the to the changing RMS voltage. Default values: 10 MΩ · 1 µF = 10 s.
- R_{SC} (behavioral resistor that scales the prototype current as a function of V_{ERR}): The equation for this resistor value controls the feedback amplification, i.e. how aggressively the current

sources react to a V_{ERR}, and at what value of the load power, the V_{ERR} should be 0. It currently has the form

$$A_{SC} = a + b\ V_{ERR}$$

It is desirable to let V_{ERR} be zero under typical load and input voltage conditions. This means that in case of a well-chosen prototype current measurement, a should be 1. If the load being much higher than during the prototype current measurement causes diode D_5 to conduct, then increasing a to 3 or 5 might help. However be aware that the constant power load can cause unexpected behavior when a is increased too much. The value of b determines how much the current magnitude is influenced by V_{ERR}. On one hand, a high value will let V_{DC} approach V_{REF} more closely. But on the other hand, the low-pass filter in the voltage error amplifier causes V_{ERR} to respond slowly, so a high value of b can result in too much overshoot or even slow oscillations in V_{DC}. Default values: a = 1 and b = 0.05.

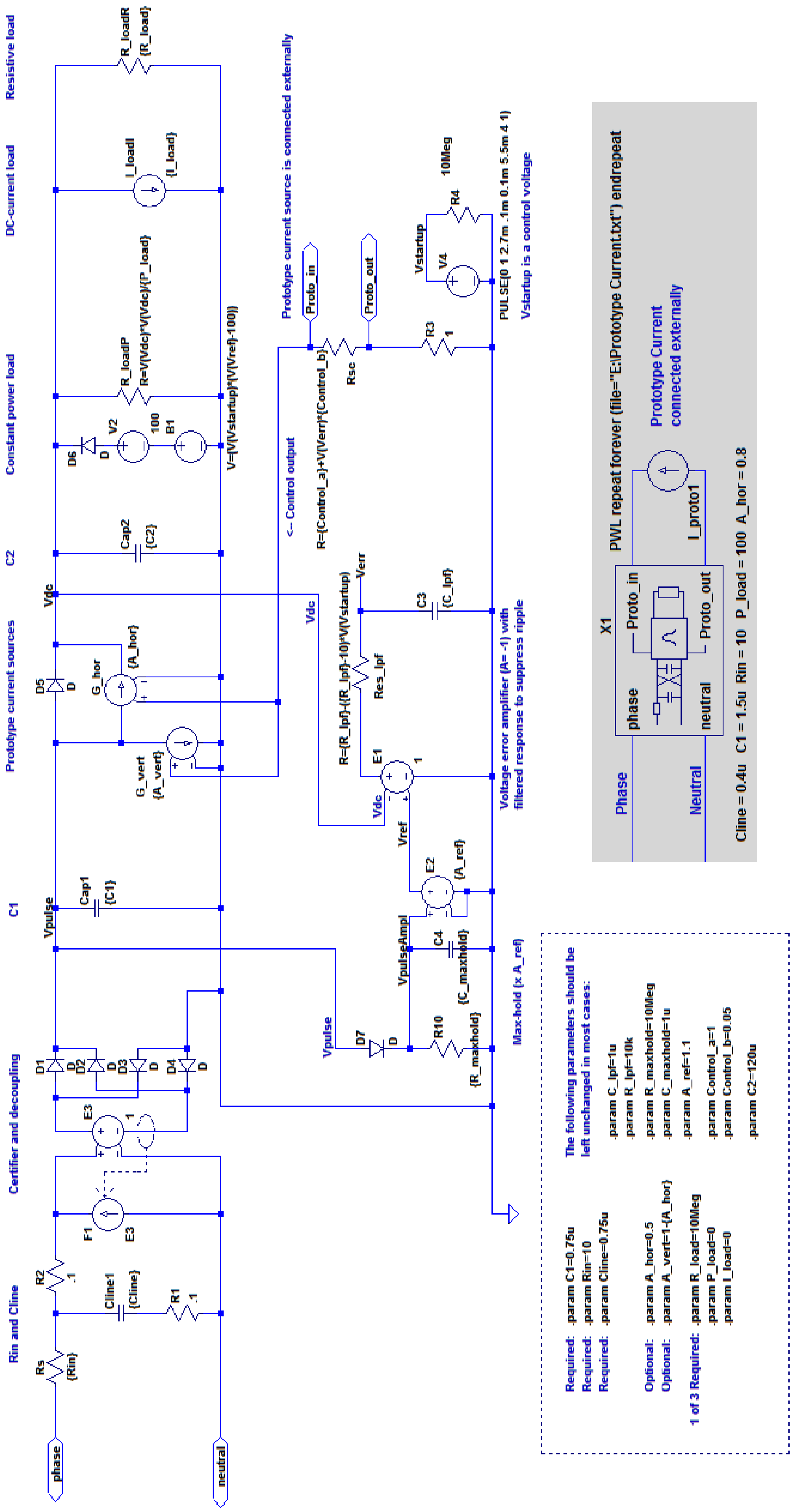

Figure 21: Overview of the SPICE implementation of the SMPS model

5.5.3.8 Expected Performance

We have now created a relatively simple model that responds adequately to distortions to the voltage waveform, and that will adapt to changes in RMS voltage and can be simulated with a user-specified load on the secondary side of the SMPS.

However, the model only works if the frequency of the input voltage is exactly the same as the frequency of the prototype current waveform. This is not expected to be a problem for the type of simulation this model is being developed for, since a deviation of one or two Hz is not expected to have a significant effect on power quality. So it should be no problem to fix the frequency to an exact value for the simulation.

The model is also based on the assumption that the current waveform, apart from its magnitude, does not change shape when the power dissipated in the load changes or when the RMS value of the input voltage changes. This is an approximation that is likely to produce a larger error as the difference in conditions in the simulation increases from the conditions under which the prototype current waveform was measured.

5.5.3.9 Inrush Currents

The model is not meant to simulate startup effects of the active PFC. However that does not mean that the model has no startup effects, as the control loop needs to find its equilibrium, and the capacitors need to be charged. This however does not reflect the cold start behavior of the real DUM. Currently the control loop takes the most time to start up. After about 1 full period the current amplitude has settled to within a few percent of the final value. If a large accuracy is needed, another period can be used to let the loop fully settle.

5.6 Rectifier without PFC: Black-Box

As mentioned in the Introduction, Dr. I. Stievano has been working with us to see if he could create black-box models of the Rectifier without PFC load. The result was a SPICE netlist that was very similar to the schematic of the gray-box model. It turns out that this SPICE model is a very concise description of the behavior of such a load. Every component describes an equation that is crucial part of the behavior of the DUM. The only place in the model where Stievano's black-box model really differs is in the rectifying bridge. That part of the netlist has been visualized in Figure 22.

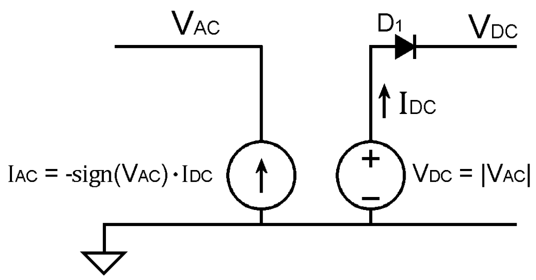

Figure 22: Visualization of the Black-Box Rectifier designed by I. Stievano

The voltage source provides a rectified version of V_{AC}, while the current source emits a 'de-rectified' version of the DC current. The diode D1 makes sure that the current cannot reverse in the DC part, just like with the real diode bridge. In this model there are several equations that can represent the diode:

Piece wise linear:

$$I_D = \begin{cases} 0 & \text{For } V_D \leq 0 \\ 10\ V_D & \text{For } V_D > 0 \end{cases}$$

Quadratic:

$$I_D = \frac{1}{4}\left(V_D + |V_D|\right)^2 = \begin{cases} 0 & \text{For } V_D \leq 0 \\ V_D^2 & \text{For } V_D > 0 \end{cases}$$

Exponential:

$$I_D = 1 \cdot 10^{-12} e^{\left(\frac{V_D}{0.026} - 1\right)}$$

The characteristics of these variations are plotted in Figure 23. Especially the exponential curve is very steep.

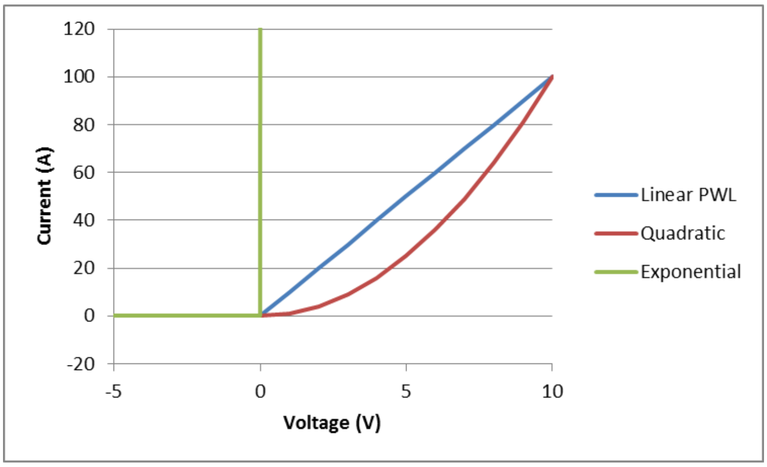

Figure 23: Characteristic of various implementation of the Diode

An important advantage of this method is that circuits on both sides of the rectifier can be directly referenced to ground without changing the behavior of the model, which is not possible when the rectifier is represented by 4 diodes. The problem with having the DC side of the circuit in SPICE not directly referenced to ground is that LTspice will slow down or even stop and generate an error ("time step too small"). Because of this important advantage, an adaptation of this circuit has been used for both Gray-box models developed in this work, as is described in Section 5.4.1.2 (*Rectifier without PFC* model) and Section 5.5.3.6 (*Active PFC* model).

Active PFC: Black-box

At the time of writing, Dr. Stievano has not yet attempted to model the Active PFC.

6 Parameterizing Gray-Box Models

Having a gray-box model structure as described in Sections 5.4 and 0 is useless if you have no values for the various components it contains. In this chapter it is explained how the parameters can be estimated from measurement. The focus in this chapter will be on understanding the principals of the parameterization process, and understanding how it works, rather than on explaining exactly how to do it. A step by step manual is provided in Chapter 9.

6.1 Rectifier without PFC, Gray-Box

In this section, several ways are presented to parameterize the gray-box model for the Rectifier without PFC using measurements. The first method is to manually fit the simulated current waveform with the current measurement. In the second and third methods the measurements are analyzed by computer. For easy reference the model schematic is repeated in Figure 24.

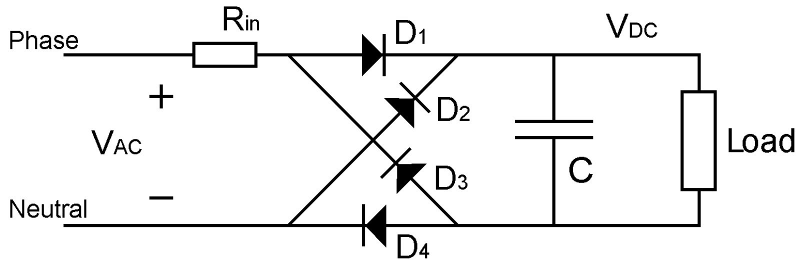

Figure 24: Rectifier without PFC model (repeat of Figure 4)

6.1.1 Parameterizing from Measurement Manually

The model can be parameterized manually, by fitting the model current to the measured current by varying the values for *C*, R_{load} and R_{in}. The plots in Figure 25 through Figure 30 provide an aid for that, as they show how changing various values affects the current waveform.

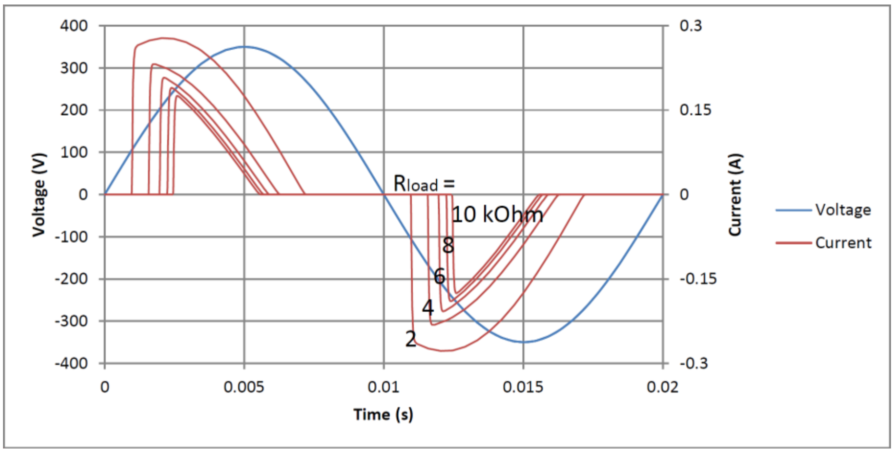

Figure 25: varying R_{load}

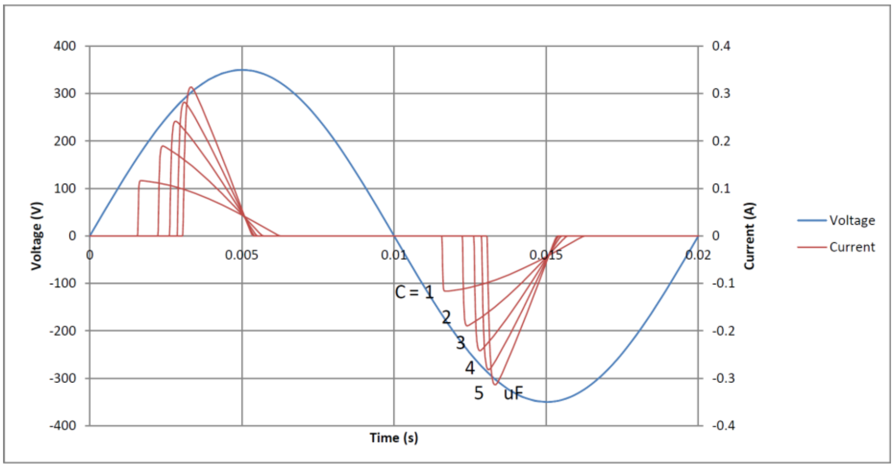

Figure 26: Varying *C*

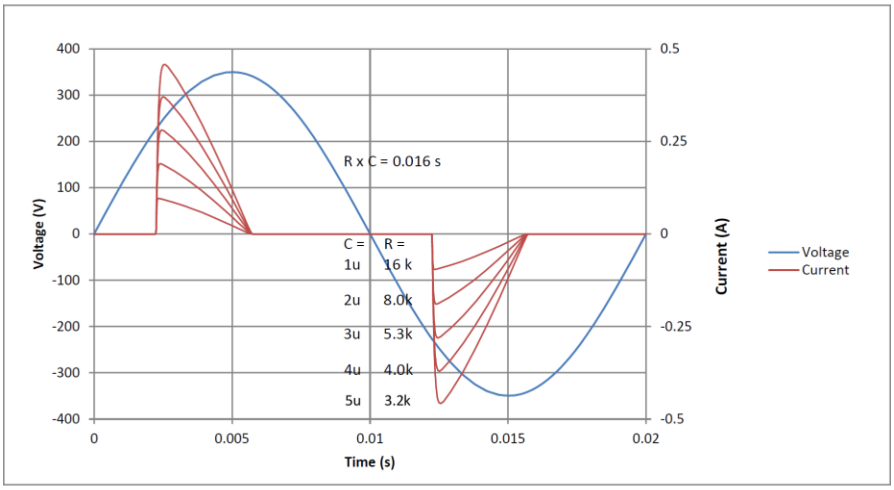

Figure 27: Varying both R_{load} and *C*, but keeping (R_{load} x *C*) constant

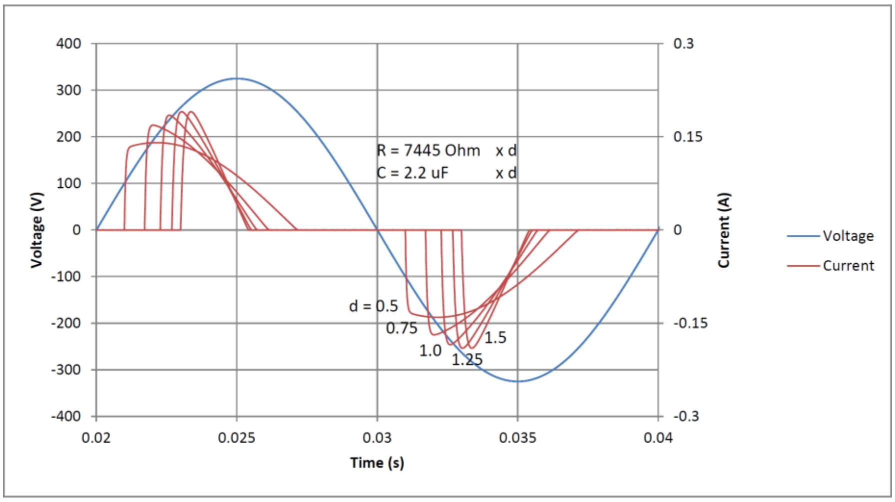

Figure 28: Varying both R_{load} and *C*, but keeping (R_{load} / *C*) constant

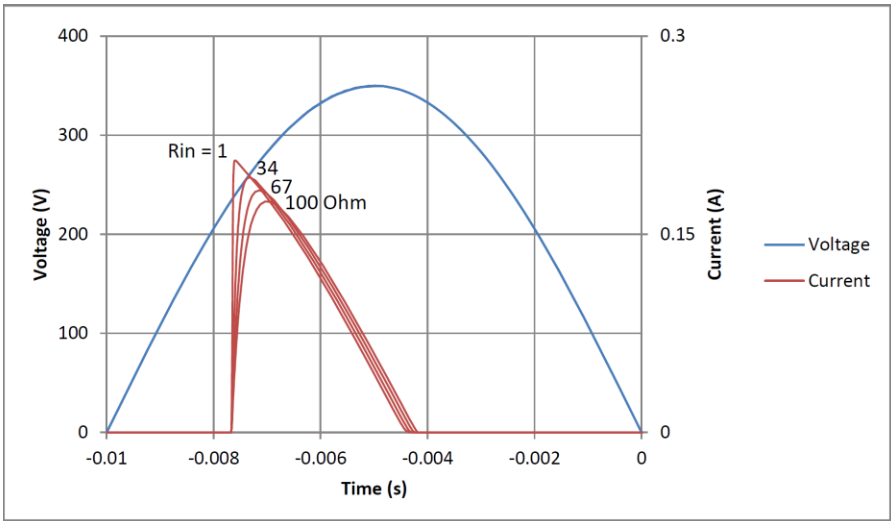

Figure 29: Varying R_{in}, plot showing only the positive peak for better readability

When looking at Figure 29, it seems at first glance that the value of R_{in} is not very important to the behavior of the CFL bulb. However when the voltage waveform is distorted, as in the simulation in Figure 30, the importance of R_{in} becomes much more obvious. After the values for C and R_{load} have been determined, a dirty voltage and measurement and simulation can be used to more easily determine R_{in}.

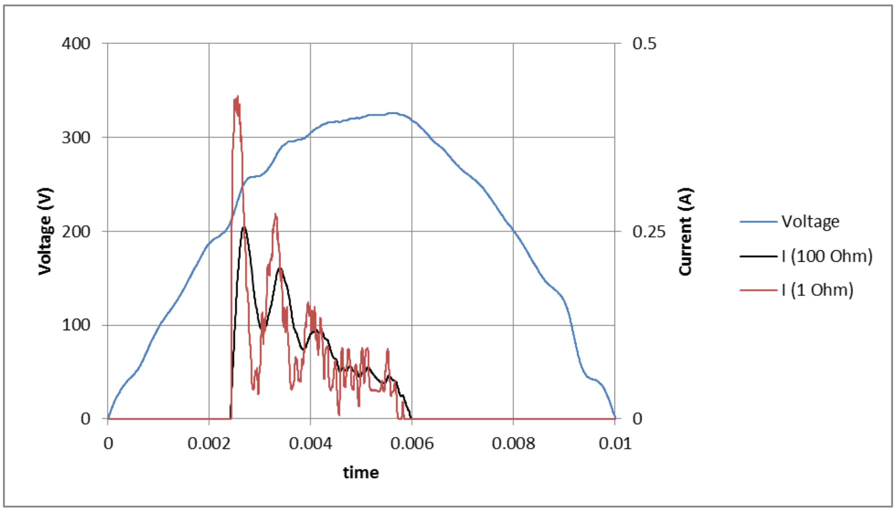

Figure 30: Importance of R_{in} on current waveform in case of distorted voltage (simulation). For clarity, only 1 and 100 Ω is shown.

The advantage of this method is that a very precise match can be obtained between the measured current wave form and the simulated wave form of the model. The disadvantage is that it is a labor intensive method of parameterizing.

6.1.2 Parameterizing from Measurement by Computer: Step Response

It would be convenient if the model can be parameterized from a measurement automatically. The computationally most straightforward method is to apply a DC-step function from a voltage source with a resistor of high value in series (e.g. 5 kΩ), and to measure the voltage and current on the terminals of the DUM. The DC voltage eliminates the effect of the diode bridge, and the high-ohmic impedance of the voltage source negates the effect of R_{in} and makes sure the measured voltage is approximately equal to the voltage across the capacitor, V_C. This reduces the circuit of Figure 4 to the circuit in Figure 32, and gives rise to the measured V_C and I_s (simulation) shown in Figure 31.

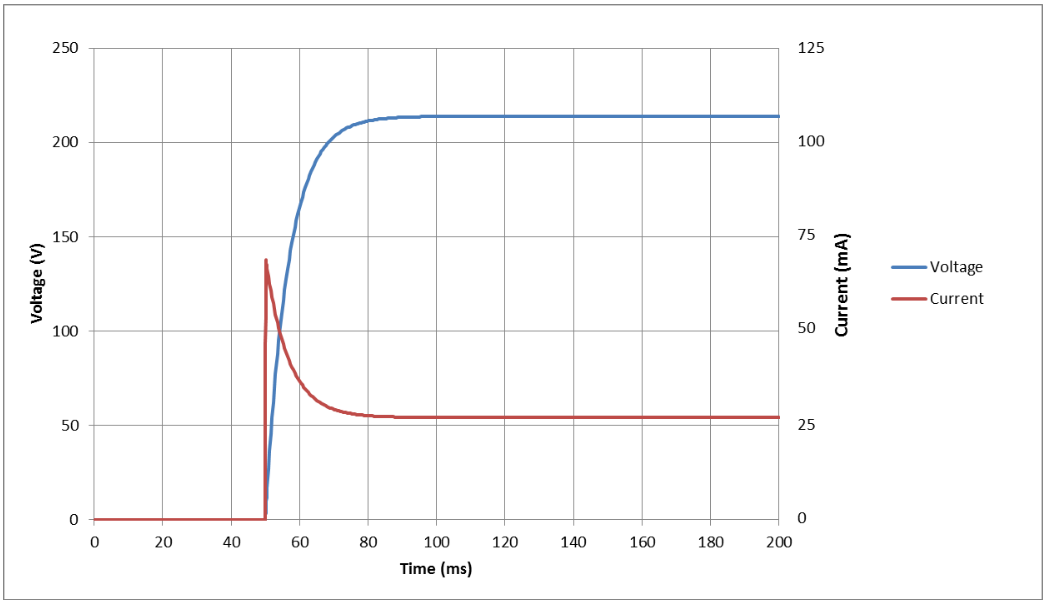

Figure 31: Simulated response to the high-ohmic voltage step function

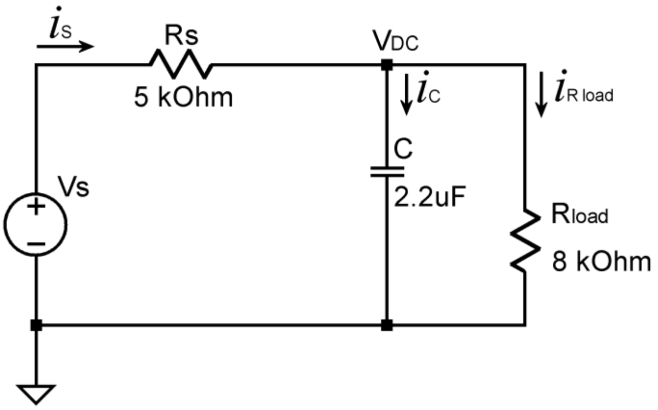

Figure 32: A high-omic step function from the source effectively reduces the model to these relevant components

From the voltage and current in Figure 31, model parameters are extracted as follows. The current into the capacitor $i_t(t)$ can be seen to be

$$i_C(t) = i_s(t) - i_{Rload}(t) = i_s(t) - \frac{R_{load}}{V_{dc}(t)}$$

Where i_s is the measured current from the power source, and i_{Rload} the current into the load. The general constitutive relation of a capacitor is

$$v_C(t_1) = \frac{1}{C}\int_{t_0}^{t_1} i_C(t)dt$$

Where t_0 is a time where the capacitor is empty (or equivalently, $v_C(t)$ = 0 V).

Rearranging, you have

$$C = \frac{1}{v_C(t_1)} \int_{t_0}^{t_1} i_C(t)dt$$

To apply it to this model, we substitute $i_C(t)$ and note that $v_C(t)$ is V_{DC} in our schematic and define the boundaries of the integral. We find the equation for the capacitance:

$$C = \frac{1}{v_{DC}(t_{steady})} \int_{t_{step}}^{t_{steady}} i_s(t) - \frac{v_{DC}(t)}{R_{load}} dt$$

Where t_{step} is the time at which the step function starts, and t_{steady} is the time where the measured current (i_s) and voltage (v_C) do no longer change. The exact value of t_{steady} is not critical. R_{load} can simply be found through

$$R_{load} = \frac{v_{DC}(t_{steady})}{i_C(t_{steady})}$$

This approach was implemented in a spreadsheet in Excel, and it works well when current and voltage waveforms from a simulation are analyzed, to within an accuracy of about 3% for both C and R_{load}. However, in this simulation, R_{load} is linear, which might well not be the case for realistic devices. In many cases the DUM will become operational when V_{DC} becomes large enough, which is likely to lower R_{load} in the middle of the measurement. Also if R_{in} is an NTC (resistor with a negative temperature coefficient), the NTC will disrupt the current peak, and no accurate estimation of the capacitance can be performed anymore. Obtaining the measurement described is also difficult as it requires specialized measurement equipment to generate the high-ohmic step-voltage source.

6.1.3 Parameterizing from Measurement by Computer: Normal Operation

It would be more convenient then to estimate the values of C, R_{load} and R_{in} from a measurement in steady state operation. Then the DUM would be working on a regular 50 Hz, 230 V_{RMS} power source, and any start up effects will have passed. An NTC will already be low-ohmic, and the device modeled by the load will be operational during the whole of the measurement, and its value will be more likely to be constant. Such a measurement is possible on site, even if the voltage waveform is distorted (see Section 8.1).

A MATLAB script has been written for this purpose that automatically estimates the parameters. First it makes initial guesses of the values for C and R_{load}, and after that it runs the simulation inside MATLAB repeatedly with an optimization routine to find more accurate values for C and R_{load}, and to find a value for R_{in}.

The initial guesses for C and R_{load} are extracted from the measurement as follows.

The plot of the measurement of a 11W CFL bulb in steady state operation shown in Figure 5 is repeated in Figure 33. First the load is estimated. For this we need to know the average current and the DC voltage behind the rectifier. The average current is obtained simply by averaging the absolute value of the current at the terminals for an integer multiple of periods. Determining V_{DC} however requires a closer inspection of the measurement, as it is not directly available.

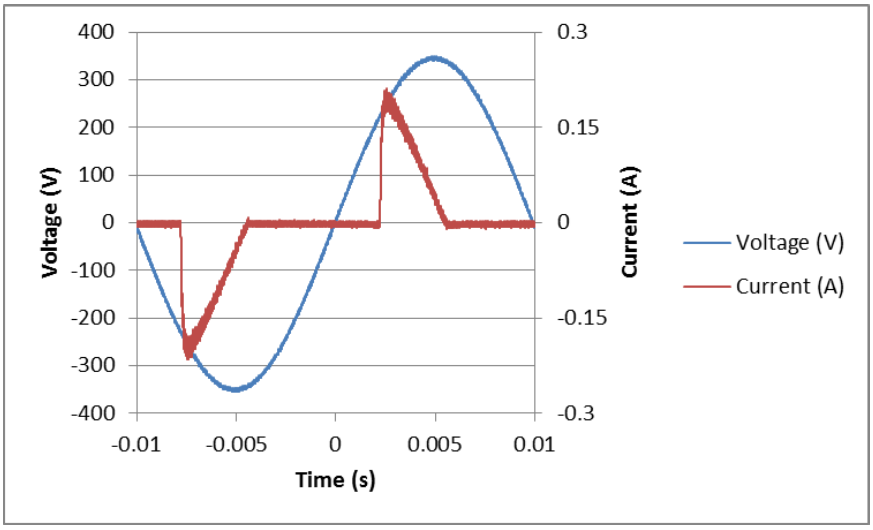

Figure 33: Measurement CFL lamp (By R.B.Timens, same graph as Figure 5)

There is always a ripple on the DC voltage. Note that while the current is flowing, the capacitor is charged and the DC voltage rises, and when no current flows, the DC voltage drops because the capacitor is discharged through the load. This is illustrated in Figure 34, obtained through SPICE simulation.

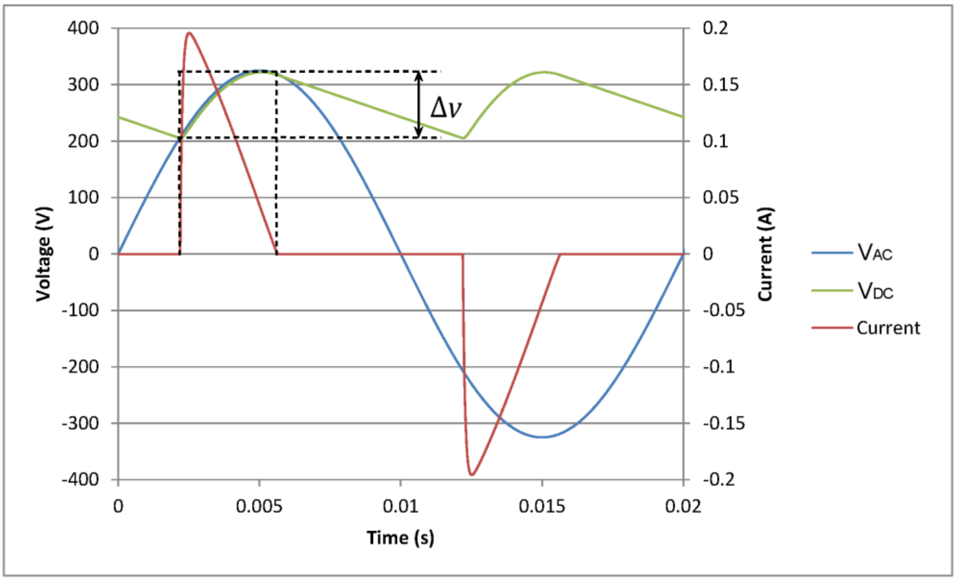

Figure 34: Ripple behind the rectifier on the DC voltage (SPICE simulation of model)

It can be seen that the input voltage is approximately equal to the minimum of the DC-ripple just at the moment the current starts to flow. Similarly, the input voltage is approximately the maximum of the ripple just as the current stops. Note that when R_{in} has a large value, the current does not necessarily stop at the maximum of the sine, but might stop later, meaning the maximum of the ripple might have a lower value. The actual voltages behind the rectifier should be a little lower because of the voltage drop across the diode, which is typically 0.6 to 1.2 volts. This observation allows a fairly accurate estimation of the average V_{DC}, and together with the average current, an estimate of the load is obtained. It should be noted that there are several different ways a load could behave: as a resistor, as a constant DC current load, or as a constant power load, or perhaps even a combination of those.

Determining the value for the capacitor is also possible. For this we look at a different equation for capacity than before:

$$C = \frac{\Delta q}{\Delta v}$$

So we need to determine how much charge flows into the capacitor during the time when the capacitor is charged (*Δq*), and the rise in voltage that this charge causes (*Δv*). We already determined *Δv* when we determined the ripple in V_{DC}, above. And *Δq* can be determined by integrating the current flowing into the capacitor, which is the measured current minus the current going into the load:

$$\Delta q = \int_{t_{peak\ start}}^{t_{peak\ stop}} i_s(t) - i_{load}(t)\ dt$$

Where from $t_{peak\ start}$ to $t_{peak\ stop}$ is the time interval during which the current is flowing, and $i_{load}(t)$ is the current through the load:

$i_{load}(t) = v_{DC}(t)/R_{load}$	for a resistive load
$i_{load}(t) = I_{DC,load}$	for a constant DC current load
$i_{load}(t) = v_{DC}(t)^2/P_{load}$	for a constant power load

P_{load} can be an external parameter, but it also be estimated using the average measured current and the estimated average V_{DC}.

$$P_{load} = I_{Average} \cdot V_{DC,Average}$$

Note that choosing the correct type of load while calculating the integral has a significant effect on the accuracy of the estimation of *C*.

The MATLAB script that has been written to carry out the above analysis is included in Appendix A. It contains several mechanisms to cope with noisy data as best as possible, and it uses all the periods in the measurement to get the most accurate result. The script makes no assumptions about the time intervals between data points, so that exported waveforms from LTspice can be analyzed as well. (The time intervals between data points in exported files from LTspice are not constant.) When the measurement data from Figure 5 is analyzed by the script, it can be compared to the manual fit, which is done in the next section.

The above principle is used by the MATLAB script to get an estimate on *C* and R_{load}. After that an optimization routine to improve the accuracy of the values is run. To this end, the model has been implemented in MATLAB (courtesy of Dr. I. Stievano), and this MATLAB implementation is used to automatically compare measurements with simulation. The values for R_{in}, *C* and R_{load} are varied by the optimization routine to find the best possible fit. To avoid local optima, *C* and R_{load} are always varied together, while either keeping their product constant (R_{load} x *C*) or their ratio constant (R_{load} / *C*). As can be seen from Figure 27, keeping (R_{load} x *C*) constant changes only the height of the current peaks, while keeping their timing exactly the same. By contrast, Figure 28 shows that keeping

(R_{load} / C) constant has a large effect on the timing. More details on this procedure and its implementation can be found in Appendix A.

In theory, the MATLAB script is not dependent on the frequency and RMS voltage, as long as the DUM is in normal operation. Even with a distorted sine the script still produces a result. Moreover, the result should be more accurate for the value of R_{in} if the current is distorted. This relaxes the requirements for the measurement setup. We will see in Chapter 0 that, based on the measurements presented in Section 7.1.4, the results from dirty measurements indeed appear to be accurate.

6.1.4 Comparison Parameterization Methods

In the Table 1, the initial results of the parameterization is shown. Based on these results, the method of parameterization was chosen that was used and further developed.

Table 1: Preliminary comparison parameterization methods

Method	Error in R_{in}	Error in C	Error in R_{load}	Comment
Manual fit	-10 %	0.20 %	N/A	Error compared to component values found inside DUM
DC-pulse measurement, analysis by computer	N/A	1.5 - 3.2 %	0.7 - 1.1 %	Analyzed simulated waveforms only
Steady-State measurement, analysis by computer (Initial guess only)	N/A	-6.0 %	-2.8 % *	* Error compared to result of manual fit
Component value found in CFL	33 Ohm	2.2 uF	7669 Ohm *	* value from manual fit

Note that component tolerances are typically 5%.

The manual parameterization is the most accurate method but also the most labor intensive.

The DC-pulse measurement analysis is accurate, but will only work if the load is a linear resistor, which usually will not be the case, and a value for R_{in} is not estimated. Also, generating the necessary source with the high output impedance is difficult. And if the R_{in} is an NTC (resistor with a negative temperature coefficient) the measurement will fail to give a useful result.

The steady-state measurement using the MATLAB script is the least accurate, but the accuracy is improved significantly by the optimization routine that was not included in Table 1. This method is also far more flexible than the DC-pulse. The necessary measurement is done while the DUM is in steady state operation, so an NTC is not an issue, and even a non-resistive load does not lead to large errors. It can even analyze measurements affected by a distorted voltage with good accuracy (see Section 8.1).

Because of the flexibility of the MATLAB script and its practicality, this method will be developed and will be the focus of the *Rectifier without PFC* model.

6.2 Parameterizing the *Active PFC* model

In this section we will look into the parameterization process for the *Active PFC* model. The focus in the section will be on understanding the principals of the parameterization process, and understanding how it works, rather than on explaining exactly how to do it. A step-by-step manual is provided in Section 9.2.

The SMPS with active PFC is a very complex device to parameterize directly from measurement. The problem is that a large part of how the current waveform looks is determined by the control loop, and not only by the physical properties of a few components, as is the case with a rectifier without PFC. For this reason a measurement is used as a the basis for this model, that captures the static behavior of the DUM. There are also a few passive components that define crucial elements of the dynamic behavior of the model, and luckily these are parameterizable though measurement.

Not all the elements in the *Active PFC* model need careful parameterization; many of them can keep their default value for any DUM. This section will only treat the parameters directly affect the behavior of the model, as has been discussed in Section 5.5.3.7. For easy reference, the schematic for the model with only the relevant parameters is presented in Figure 35.

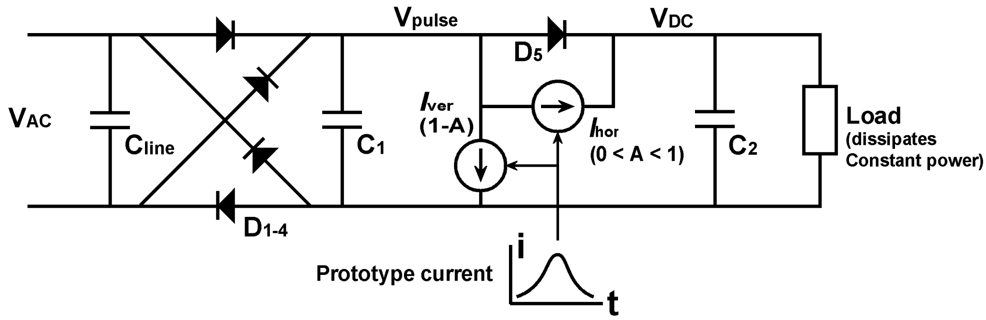

Figure 35: Basic schematic of the *Active PFC* model

Prototype Current

Central to the model is the prototype current waveform. The assumption is made that current waveform of the DUM has a basic shape that is simply scaled according to the amount of current the DUM needs. So the current waveform is measured under typical conditions and with a clean voltage, and then this current waveform is simply repeated during simulation, its amplitude scaled to accommodate the load.

This, off course, is an approximation. When the load of an SMPS varies, or when the RMS voltage changes and the current changes to compensate, the current waveform shape does change. The more the current amplitude drawn in simulation differs from the current drawn during the prototype measurement, the more inaccurate this approximation will be. For this reason, the prototype current measurement should be performed under typical or average circumstances that are expected in the simulation. If the range of circumstances are expected to differ a lot, for instance because the user of the model wants to vary the load across a wide range, then it might be a good idea to make several prototype currents, each measured with a different load.

Note that up to this point only the RMS voltage value and the load value are considered, and not yet distortions in the voltage waveform. Distortions will be discussed later, as they are modeled by different elements in the model. Because distortions aren't modeled by the prototype current, it is very important that the prototype current waveform is measured using a clean voltage.

The prototype current sources are placed behind a capacitor (C_{line}), rectifier and another capacitor (C_1). Even with a clean voltage, these elements all have an effect on the current that is drawn from the mains. However, with the prototype current principle, these effects now count twice, because the prototype current was measured at the mains (where the effect is included), and not behind the rectifier and capacitors, where the sources are now. So the sources are drawing a current which includes the effects of the capacitors and rectifier, in addition to the effects of these elements which are present in the model as well. The effect of these capacitors therefore needs to be removed from the prototype current. Since the prototype current is measured using a clean sine, it is relatively easy to do this, using the basic equations for capacitors. If the voltage is:

$$v(t) = \hat{V} \sin(\, 2\pi f\ t\,)$$

Where $\hat{V}$ is the voltage amplitude and f is frequency (usually 50 Hz or 60 Hz), then the capacitive current is

$$\begin{aligned} i_C(t) &= C \frac{\mathrm{d}}{\mathrm{d}t} v(t) \\ &= C \frac{\mathrm{d}}{\mathrm{d}t} \left\{ \hat{V} \sin(2\pi f\ t) \right\} \\ &= C \cdot 2\pi f \cdot \hat{V} \cos(2\pi f\ t) \\ &= \hat{I}_C \cos(2\pi f\ t) \end{aligned}$$

Where C is the capacitance and $\hat{I}_C$ is the capacitive current amplitude. These currents need to be subtracted from the prototype current. Now note that for C_1, the voltage is V_{pulse}, which is not a sine, but a rectified sine. So after a half period, the above equation for $i_C(t)$ is no longer valid for C_1. But the prototype current only needs to be a half period because it is situated behind the rectifier, so for parameterization this equation is still useful. Off course, in order to actually remove the effects of C_{line} and C_1 from the prototype current, the values of their capacitance or current amplitude ($\hat{I}_C$) need to be found. How this is done will be discussed a separate subsection below, on *Capacitors*.

Load

An SMPS generally produces a DC voltage that is regulated to maintain the same value, regardless of input voltage or load. This means that, when the load remains constant, it is reasonable to expect an SMPS to always behave as a load that dissipates a constant power, regardless of input voltage. This can be verified using the slow triangle measurement, or by measuring with several RMS voltages and calculate the average voltage × current to get power, and see if the resulting value is constant.

Amplification Factors of the Prototype Current Sources

As explained in Section 0, part of the current needs to be pumped into the C_2 capacitor (through the horizontal source) and part needs to go directly down to the negative DC line (through vertical source). So we need to find the ratio between the current that goes into C_2 (horizontal) and the current that goes down to the negative DC line (vertical).

Two effects are captured in this ratio. One effect is that in the actual boost circuit part of the current indeed goes to the negative DC line (see Figure 8 in Section 5.5.1), and the other is the efficiency of the DUM. While it would be possible to analytically calculate the first effect, the latter effect will just be a measured quantity, because is it in part determined in the black-box portion of the model. Because of this, calculating the first effect serves no purpose.

The way to parameterize the ratio of the amplification factors is then to run the simulation, recreating the circumstances of load and voltage of the prototype current measurement. So the load is set to dissipate the same power as during the measurement, and the voltage is clean and has the same amplitude. The ratio is then varied until the current amplitude from simulation matches with the measurement.

The prototype current sources are implemented as voltage controlled current sources. The ratio is applied using their amplification factors. To avoid unintended amplification in this part of the model, the sum of both amplification factors should be 1. In other words, if the horizontal source has amplification A, (with $0 < A < 1$) then the vertical source should have $1 - A$.

Capacitors

In this section we will discuss how C_{line} and C_1 capacitances are estimated. First C_{line} is looked into. For this we need to consider that during a 50 Hz period, the rectifier has two different states. It either conducts current, or it does not. The latter occurs near the voltage zero crossings. This means that at the zero crossings, the current that the DUM draws must be due to components in front of the rectifier. When looking at a clean voltage measurement, in many cases this current looks like a DC that changes sign twice every period. In actuality however, this is a cosine, namely the current due to the line filter capacitance C_{line}, as is illustrated by the green line in Figure 36.

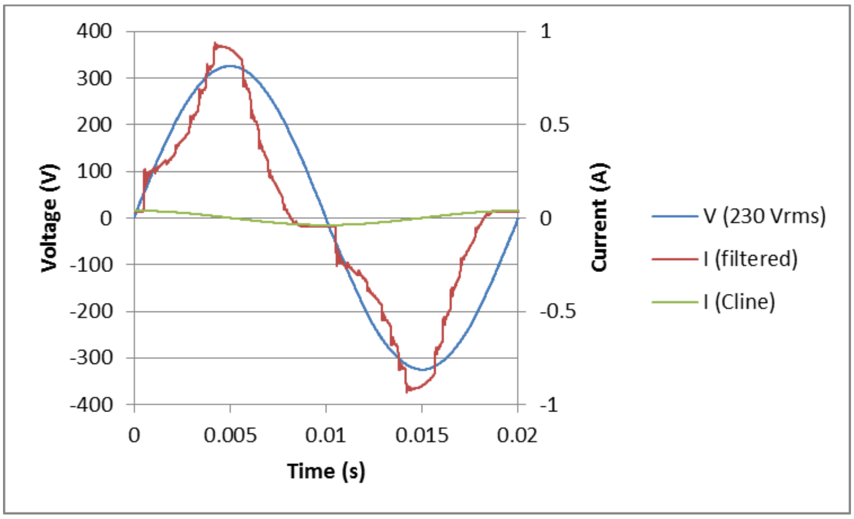

Figure 36: Plot of the line filter current equation (green line)

Calculating capacitance from measured current amplitude or vice versa is done by a simple equation:

$$\hat{I} = C \cdot 2\pi f \cdot \hat{V}$$

$$C = \frac{\hat{I}}{2\pi f \cdot \hat{V}}$$

If the capacitive current amplitude is not as readily available there is a different way to find C_{line}, which will be discussed a little later on.

Finding a value for C_1 is a little more difficult, as it is not directly distinguishable from the prototype current, since they are both found behind the rectifier. However, there is a way to find the total capacitance $C_1 + C_{line}$. For this, the distorted voltage measurement is needed. The prototype current sources do not respond to voltage distortions, but the capacitors do. So the current distortions are due to the capacitors. So the idea is to vary the capacitance values until the amplitude of the current distortion in simulation matches with measurement. When the rectifier is conducting, both capacitors are essentially in parallel, meaning the current distortion depends on the sum of C_{line} and C_1. If C_{line} is already known however, then only C_1 needs to be varied to obtain a match. If C_{line} is not yet known then you can focus on the current distortions near the zero crossings, where the rectifier isn't conducting, and find a match there by tuning C_{line}, and after that tune C_1 to get a match in the areas where the rectifier is conducting.

Resistor R_{in}

So far in this discussion the value of R_{in} has not yet been discussed. This is because its effect on the behavior of the DUM is limited. In an SMPS the resistor at the input is usually an NTC (resistor with a negative temperature coefficient). These have a non-zero value when they are cold, and when the SMPS is turned on, their own current heats them up and they become low-ohmic. So in steady state operation, which this model is designed to simulate, R_{in} will have a very low value. There will also be some parasitic resistance in the inductors that are present in the line filter that would add to the value of R_{in} in the model, but still R_{in} is expected to be only few ohms at most.

With this in mind, note that the input impedance of the model when the rectifier is conducting is

$$Z_{in}(\omega) = R_{in} + \frac{1}{j\omega(C_{line} + C_1)}$$

If $C_{line} + C_1$ is in the order of 2 µF, which appears to be a realistic value, then for frequencies up to a few kHz, the reactive part will be dominant. This is why R_{in} is not a very critical parameter. Note that this is different for the *Rectifier without PFC* model, where both R_{in} and the capacitance are often both much bigger, causing R_{in} to be dominant rather than the capacitance.

If the voltage waveforms, in spite of filtering, still have too much sampling or quantization noise, the effect on the current noise can be suppressed somewhat by making R_{in} a bit bigger, making Z_{in} a little bigger for high frequencies. But do note that the extra voltage drop across R_{in} will cause the control loop to draw more current, which affects the parameterization of the prototype current sources as well as the start-up time of the model. It is therefore advisable to keep R_{in} below 20 Ω.

7 Measurements

Since the goal is to parameterize the models by analyzing measurements, measurements will need to be performed that will provide the information needed for parameterization. Aside from that, measurements need to be done by which we can assess the accuracy of the model. In this chapter the measurements that were performed for this work are presented. The DUMs that the measurements in this chapter were performed on are the CFL bulb and the PC power supply introduced in Section 4.3.

Generally, measurements for parameterization will be done under circumstances that are as ideal as possible, by using a very clean and low-impedance voltage source, giving a clean sine or other waveform that will provide the information needed. However, some information can most easily be obtained using a distorted voltage. For checking the validity of the model, variations in the power source can be introduced, such as over/under voltage, different frequencies and waveforms. But perhaps the most interesting test for the validity of the model is to measure the performance of the DUM when it is powered by a voltage waveform from an outlet in the wall, which provides a distorted sine. Then it is checked if the model reacts in the same way when the measured dirty voltage is applied to the model.

7.1 Measurement Setup

Since we are interested in measuring the behavior of the DUM for the purpose of making an accurate model, rather than checking its compliance to industry standards such as EN61000-3-2, it is not necessary to do the measurements according to methods specified in those standards. This means that it is for instance not required to use a Line Impedance Stabilization Network (LISN) for these measurements. However, the measurement setup does need to be protected from distortions on the power network. This is what a LISN is intended to do. However, while a LISN isolates the measurement setup from high frequency conducted emissions from the mains (and vice versa), it is completely ineffective for the low-frequency distortions that are relevant to this work, such as the distortions on the sine in Figure 37. So instead of a LISN, the measurement setup is protected by a programmable power supply.

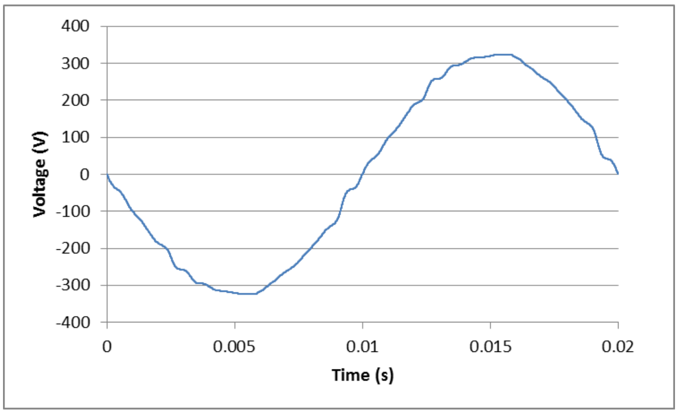

Figure 37: Distorted voltage measured at the wall outlet in the Carré building at the University of Twente

The functional diagram of the setup used in the measurements is shown in Figure 38, and Figure 39 shows a photo of this setup.

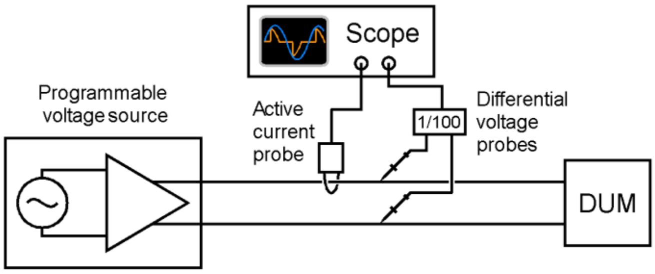

Figure 38: Functional schematic of the measurement setup

The components are

- Programmable power source (Spizenberger + Spes Viechtach, SyCore/PAS 5000)
- Active current probe (Tektronix TCP202)
- Differential voltage probe (Testec TT-SI 9010)
- Scope (Tektronix TDS 3032B)

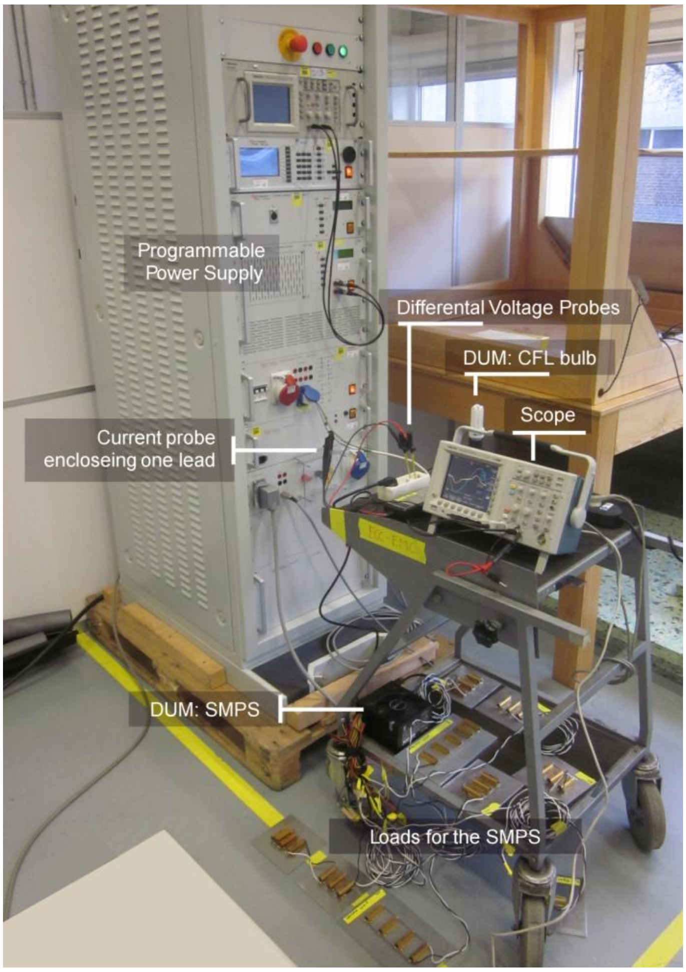

Figure 39: Photo of the measurement setup at the Thales EMC lab.

Aside of providing good protection from distortions on the power network, there are other advantages to using a programmable power supply as well. As mentioned above, measurements will be conducted using the voltage waveform from a wall outlet. However, while the voltage waveform from a wall outlet is obviously realistic, it also changes a lot in time, because people are turning appliances on and off all the time in buildings. This means it is impossible to make a repeatable measurement of the behavior of the DUM, just by plugging it in into the power outlet. Fortunately the programmable power supply can generate any voltage wave form from a .csv file. So the voltage waveforms from power outlets were measured at two locations (Thales EMC lab and the Carré building at the University of Twente) and saved to a .csv file. Then the power supply generates the wave forms from the .csv file, and the behavior of the DUM connected to the power supply is measured. This way, the exact same waveform can be recreated at will, making it possible to repeat and compare measurements. The validity of this method will be looked into in the next section.

7.1.1 Validation of Measurement Setup

The question we want to answer is: how accurately is the voltage wave form reconstructed by the power supply, and how closely does the setup represent the wall-outlet. To answer this, the voltage waveforms at the Thales EMC lab were measured along with the current waveform of the CFL bulb which was plugged into the outlet too, during the measurement. This allows a comparison to be made between how the CFL bulb behaved during the measurement and how it behaves when the power supply is used to reconstruct the measured voltage waveform. This comparison is visualized in Figure 40.

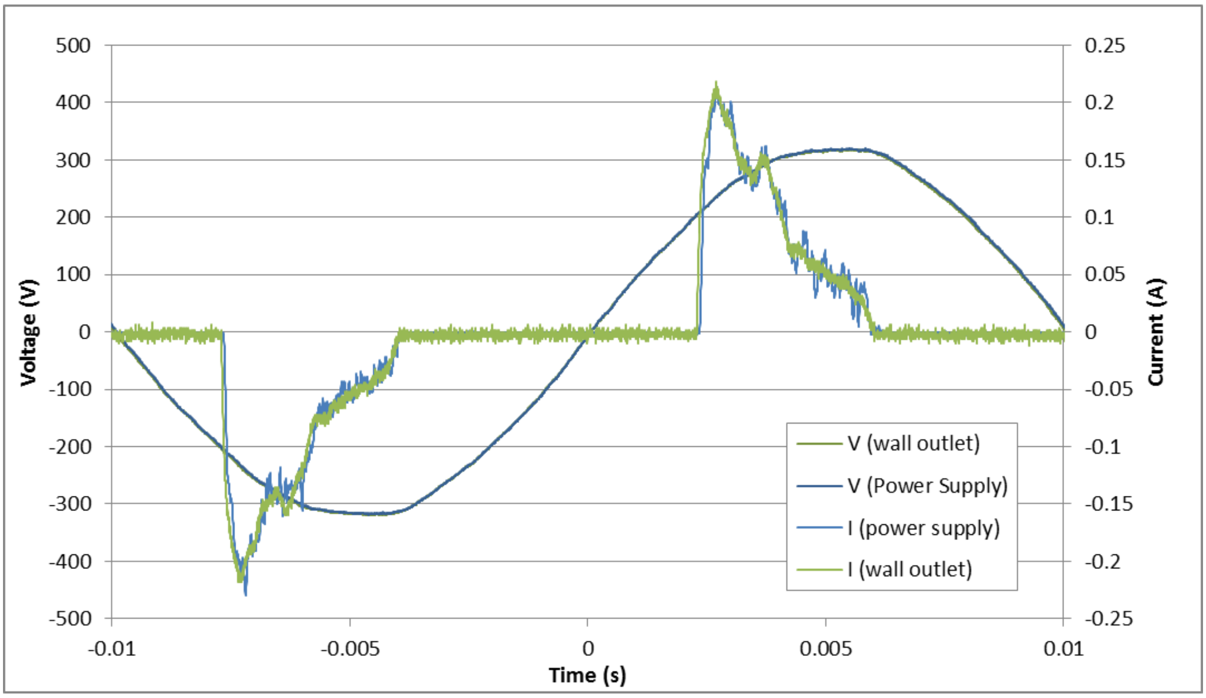

Figure 40: Comparison of CFL behavior: plugged directly into the wall outlet, vs. when the power supply reconstructs the outlet voltage waveform.

It can be observed that the current waveform of the CFL bulb follows approximately the same shape in both measurements, but that the current waveform where the power supply is used (blue line) has an additional ripple of approximately 40 mA (peak-peak). This could be due to the power supply reconstructing the voltage waveform with a finite amplitude resolution and quantization frequency (introducing sampling/quantization noise on the voltage), or because the power supply has a lower impedance at higher frequencies than the wall outlet.

Since the output impedance of the power supply is designed to be very low up to high frequencies (many tenths of kHz), the latter explanation seems likely. We will also see in Section 8.1 that the gray-box model displays a similar behavior when simulating with the same voltage waveform. In this simulation, the voltage source is ideal, so it has a low impedance for high frequencies as well, but the sampling/quantization noise has been filtered out (see Section 7.1.2). This suggests that the extra ripple is indeed due to the low output impedance of power supply.

This means that, in spite of the difference in Figure 40, the measurements with the power supply are useful for model validation. The models developed in this work do not model the power mains network in a building, but only the loads, and the ideal voltage source in SPICE seems to do a good job at simulating the programmable power supply.

7.1.2 Averaging on the Scope, Distortion

The current and voltage waveforms have all been averaged over a 100 times (except for the triangle measurement) until the waveforms no longer changed on the scope screen, before they were saved to file. This way there should be very little noise in the data. However, the scope has a limited amplitude resolution, so when you zoom in, the quantization is visible. Depending on the principle of the model, it may be necessary to apply a filter to smooth these quantization steps out, in order to get a realistic prediction for the current out of the model. More on this can be found in Section 8.1.1, and the filter is described in the next section.

7.1.3 Filtering

In many plots the data has been filtered. Whenever this is the case, it will be mentioned in the title of the figure or in the text. Unless otherwise stated, the filter is a moving average filter with n=19 taps which, with the equipment used here, equates to 38 µs averaging for a single 50 Hz period. This filter is applied afterwards in excel, rather than in real-time during the measurement. Sample n is the average from sample $n - 9$ to $n + 9$. This way, the filter causes no delay.

The filter with 19 taps is found to be sufficient to filter out the worst of the sampling/quantization noise effects from the scope, without dampening the relevant dynamic behavior. In some cases the filter will suppress high frequency emissions from the switching circuit in the DUM. But this is not considered a problem since we are developing low frequency models, so we are not interested in these switching effects.

How to apply such a filter to data in Excel is explained in Section 9.3.

7.1.4 Slow Triangle Voltage

One of the waveforms produced by the programmable power supply is a slow triangle voltage, with a period time of 4 or 6.7 seconds. This slow voltage triangle is basically a DC sweep and it will give us the data for the V-I curve of the load on the DC-bus inside the DUM. It is expected that when the absolute value of the voltage |V|, goes up or down, different currents will be observed, due to different switch-on and switch-off effects inherent to most DUMs. For a steady state model, the down-ramp is the most interesting one.

Due to the limitations of the scope, it was not possible to capture .csv data of the voltage and current simultaneously. Because of this, there is a time offset between the voltage and current plots. The only way to correct for this was to realign the plots visually using a screen capture from the scope. Due to the duration of the triangle pulse and the limitations of the scope, these measurements have not been averaged.

7.2 Rectifier without PFC: CFL Lamp

In this section the measurements performed on CFL lamps are presented. Measurements have been conducted using the following voltage conditions (using the programmable power supply unless otherwise noted):

- 'Ideal' 50 Hz, 230V_{RMS} sine
- Over voltage (+10%, 253 V_{RMS})
- Under voltage (-10%, 211 V_{RMS})
- Under voltage (-50%, 115V_{RMS})
- 100 Hz sine
- 36 Hz sine (no visible flicker)
- 15 Hz sine (severe flickering)
- Square wave (50Hz, 260 V amplitude)
- DC 260 V
- Slow triangle voltage (378 V amplitude, T = 4 seconds)
- Wall outlet waveform[1], location: Thales EMC lab
- Wall outlet waveform[1], location: Carré building, University of Twente

The amplitude of the DC and square voltages is chosen to be 260 volt, because based on the 'ideal' 50 Hz measurement, the DC voltage behind the rectifier is estimated to be of around that value. In Figure 41 a close up photo is shown of the measurement setup with the CFL bulb DUM.

[1] During the measurement, the programmable power supply reconstructed the waveform that was measured earlier at the mentioned locations. This is to ensure repeatability of the experiment. The power quality in the Carré building is significantly worse than in the Thales building.

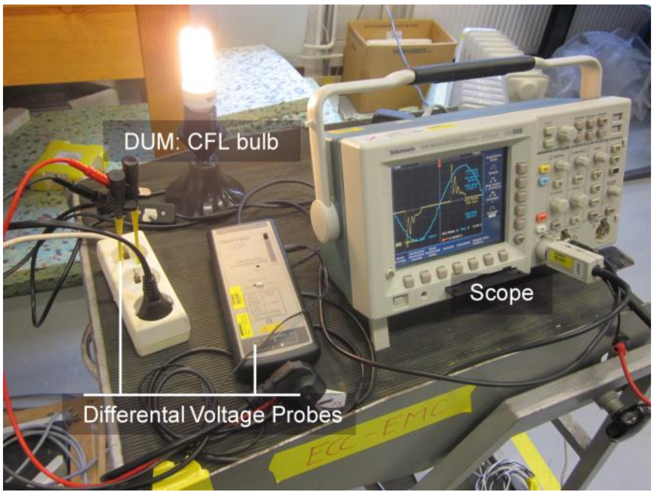

Figure 41: Photo of the measurement setup: CFL bulb. (Current probe is out of sight)

7.2.1 Relevant Measurements

In this section the most interesting and relevant measurements are plotted that have been performed on the CFL bulb.

In Figure 42, the basic measurement is shown for the "ideal" 50 Hz 230 V_{RMS} sine voltage form. It can be seen that the measurement closely matches the one performed by R.B Timens in Figure 5.

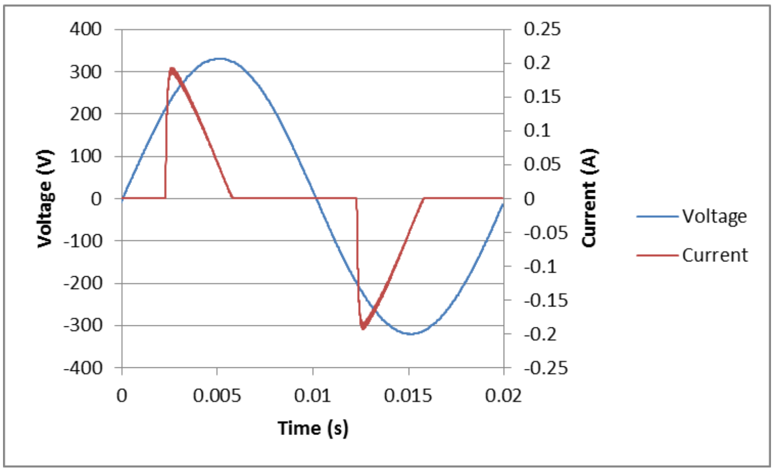

Figure 42: Behavior of CFL bulb, voltage waveform: 230 V_{RMS}, 50 Hz sine

As explained in Section 6.1.3, this data already gives sufficient information for the MATLAB script to estimate the value of the capacitor and load.

Superimposing the plots for different RMS voltages gives us the plot of Figure 43. While the timing and the height of the current peaks differ between the voltages, visual inspection reveals that the total current drawn during one period is roughly the same.

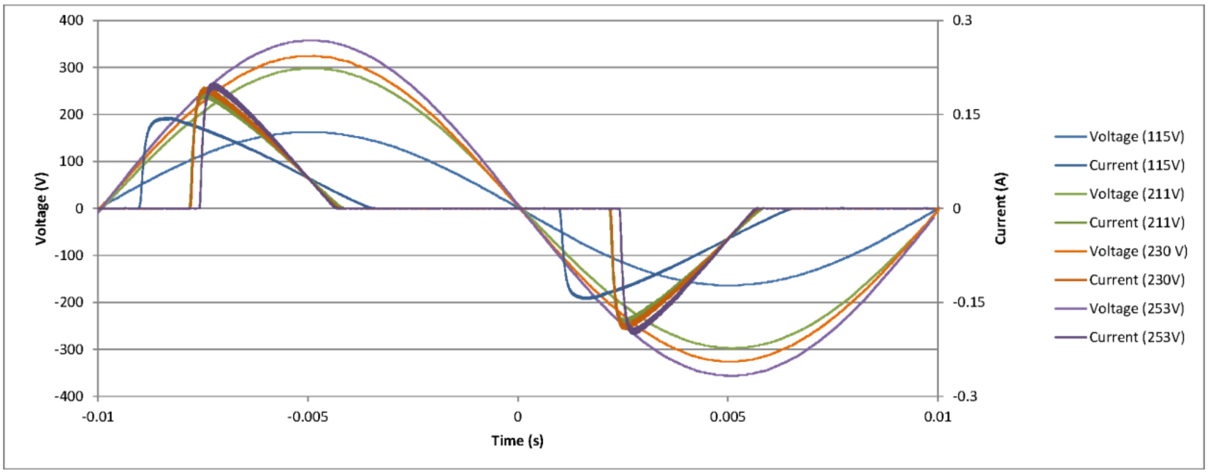

Figure 43: Behavior of CFL bulb for various RMS-voltages (50Hz sine)

This impression is verified by the slow triangle voltage measurement, which reveals the DC current is almost invariant with voltage. The raw measurement is shown in Figure 44. When the absolute value of the voltage is rising, start-up effects are seen. For making or verifying steady state models, this is not interesting. However when absolute value of the voltage is declining, the CFL bulb is already in steady state operation. When only taking the declining parts of the measurement into account, as is highlighted in the figure, a steady-state V-I curve of the load can be obtained. This V-I curve is plotted in Figure 45.

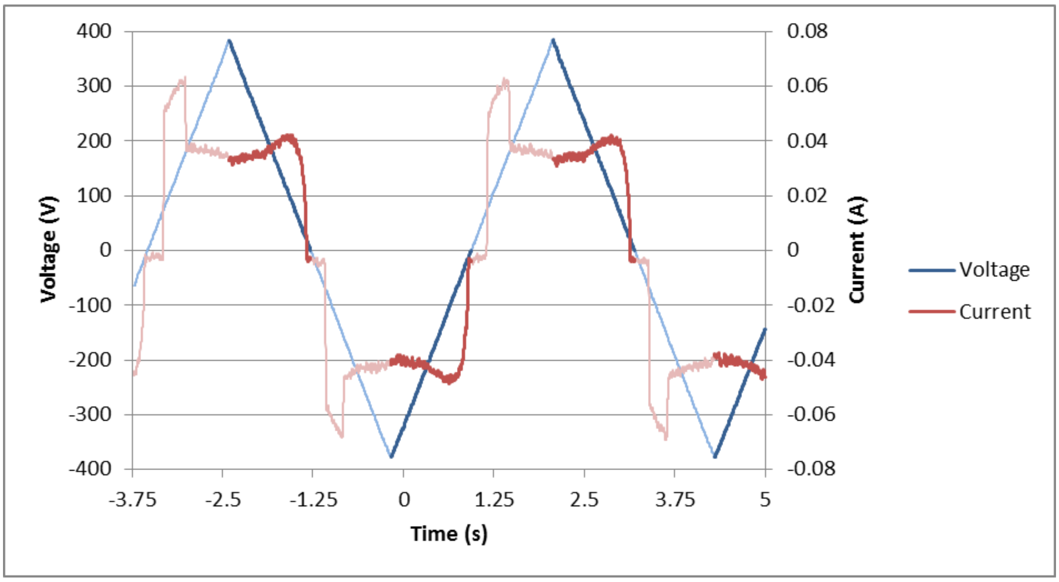

Figure 44: Behavior of CFL bulb excited by a slow triangle voltage (T = 4 sec, $V_{amplitude}$ = 379 V, filtered)

It can be seen in Figure 45 that for a wide range of DC voltage, roughly 200-380 V, the current drawn by the CFL bulb differs by less than 5 mA, and about 10 mA when measuring from 50 V. Note that this is approximately the V-I curve that belongs to the load behind the rectifier and capacitor, and *not* the V-I curve as seen directly on the terminals of the CFL bulb under normal operation when a 50 Hz sine is applied.

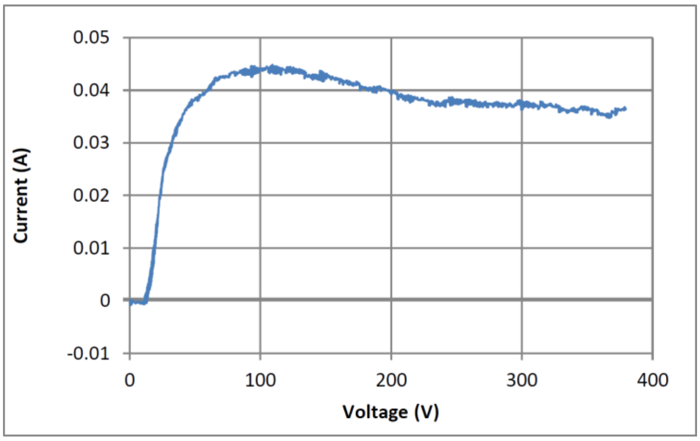

Figure 45: V-I curve of the load behind the rectifier and capacitor, obtained though slow triangle voltage measurement

The V-I curve seen when the CFL bulb is driven by a 50 Hz sine is shown in Figure 46, for various RMS voltages. The arrows in the plot show the direction on time.

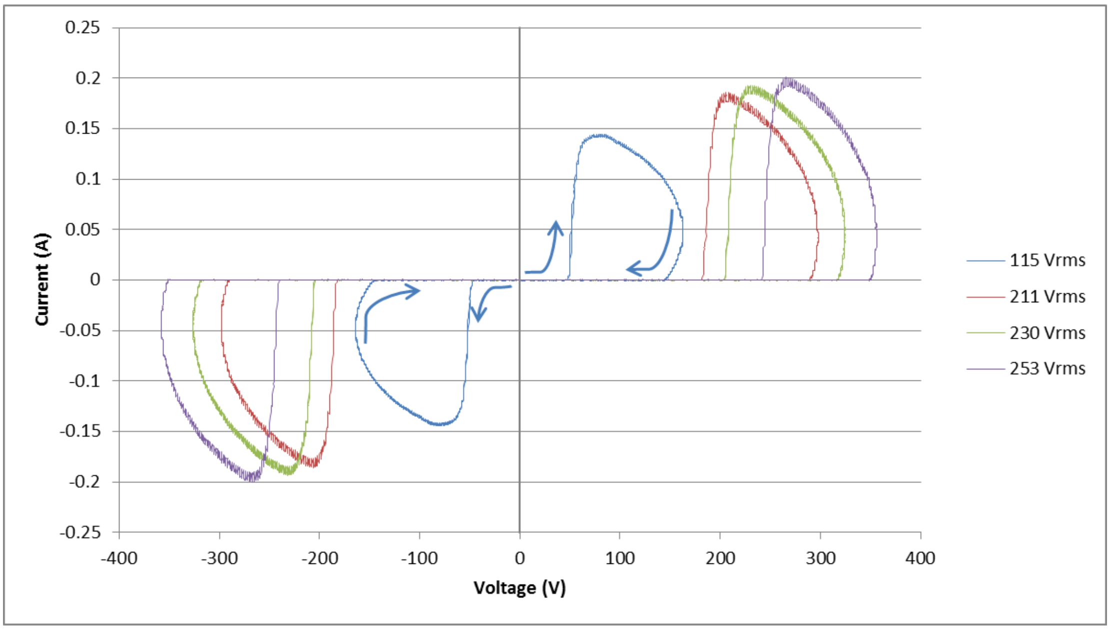

Figure 46: V-I curve CFL light bulb when driven by 50 Hz sine of various RMS voltages

Figure 47 and Figure 48 show how the CFL bulb responds when it is powered by the power supply recreating the voltage form measured at the Thales EMC lab and the Carré building, respectively. It can easily be seen that the shape of the current peaks is very sensitive to the shape of the voltage. Even with the relatively decent power quality at the Thales EMC lab, the current peak is distorted quite significantly.

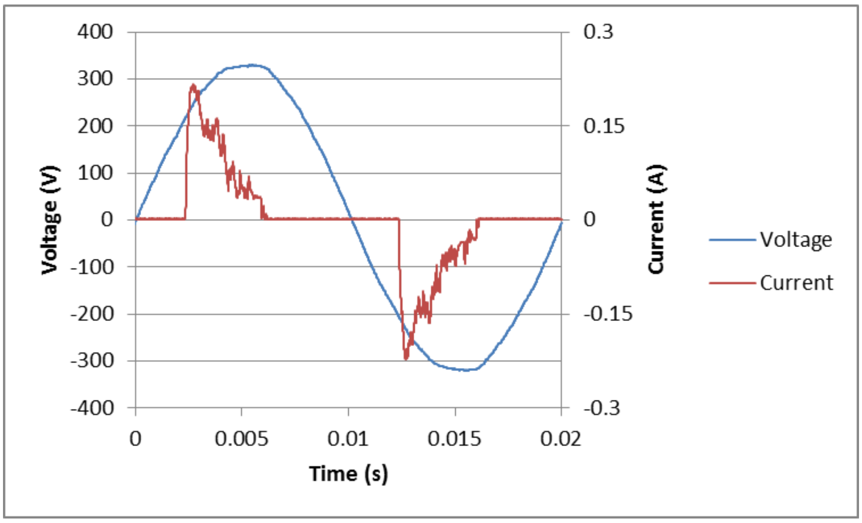

Figure 47: Behavior of CFL bulb when excited by the (reconstructed) waveform from the Thales EMC lab wall outlet

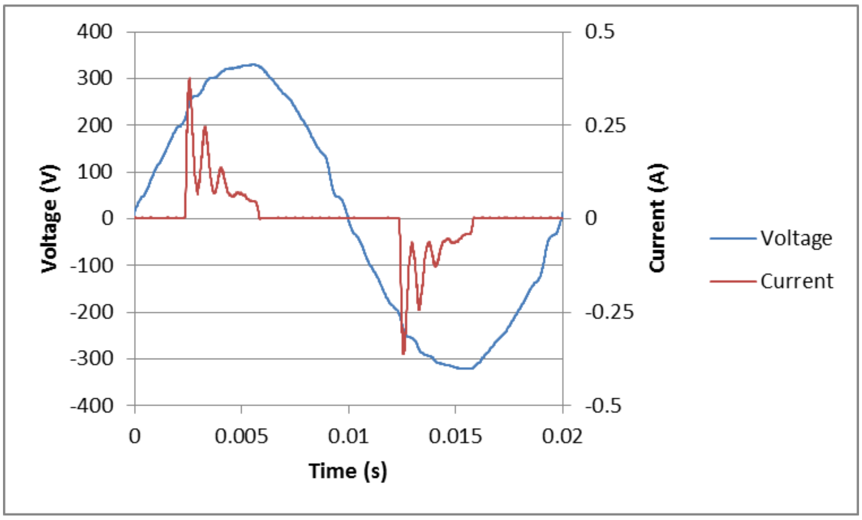

Figure 48: Behavior of CFL bulb when excited by the (reconstructed) waveform from the Carré building wall outlet

7.3 Active PFC: PC Power Supply

In this section, some relevant measurements are presented that have been carried out on the PC power supply with Active PFC. All measurements have been performed with the DUM under several different load conditions:

- 90 Watt (load realistic for an idle computer)
- 150 Watt
- 210 Watt
- 270 Watt (almost maximum load)

The loads consisted of several power resistors, connected to the various output voltages, according to their rated current as mentioned in the manual. Figure 49 shows a photo of the DUM and its loads. During the measurements with the 270 Watt load, the SMPS started to smell a little, so after every few measurements the SMPS was turned off for a while to allow it to cool down. It was not considered necessary or wise to try the full 300 Watt load.

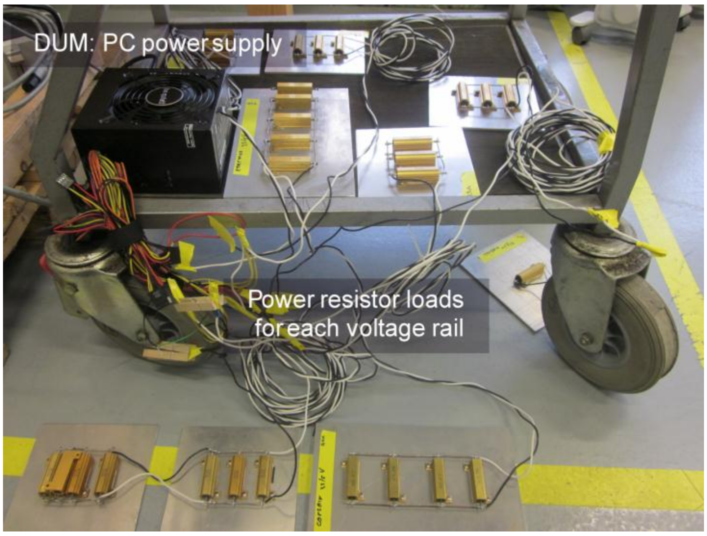

Figure 49: DUM: PC power supply with resistive loads

The measurements that have been performed are:

- 'Ideal' 50 Hz, 230V_{RMS} sine
- Over voltage (+10%, 253 V_{RMS})
- Under voltage (-10%, 208 V_{RMS})
- Under voltage (-50%, 115V_{RMS}, which is within specifications for the SMPS)
- Slow triangle voltage (320 V amplitude, T = 6.67 seconds)
- Wall outlet waveform, location: Thales EMC lab (230 V_{RMS}, 210+270 W only)
- Wall outlet waveform, location: Carré building, University of Twente, Scaled to:
    - 115 V_{RMS}
    - 208 V_{RMS}
    - 230 V_{RMS}
    - 253 V_{RMS}

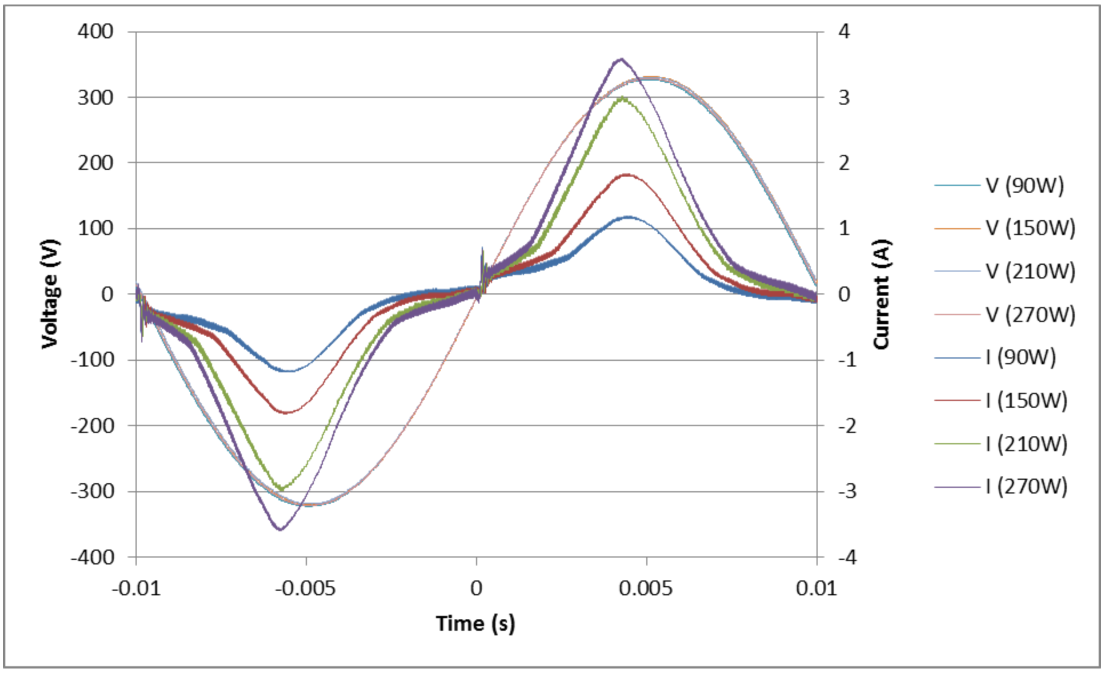

Figure 50: Behavior SMPS: 230 V_{RMS}, 50 Hz sine, various loads, averaged but unfiltered

Figure 50 shows the response of the SMPS to a clean 230 V 50 Hz sine voltage, under different load conditions. Note that the different current waveforms are approximately scaled versions of each other.

Figure 51 shows the I-V curves from the same set of measurements as shown in Figure 50. Note that the active PFC attempts to turn this into a straight line, but does not succeed completely. Also note that the curve is still open, just like with the CFL bulb.

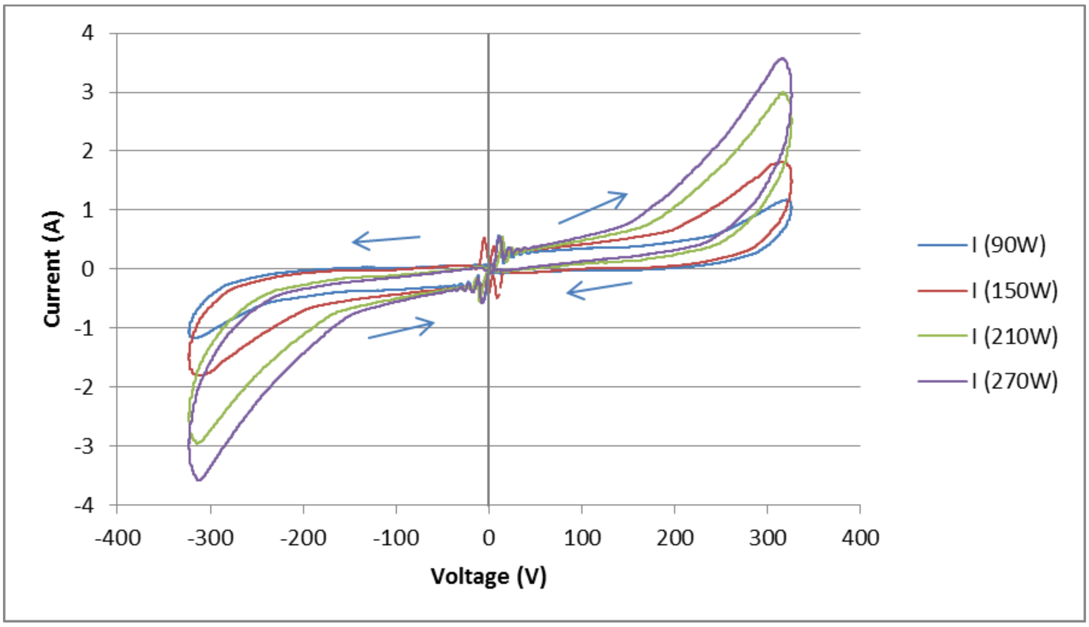

Figure 51: V-I curve resulting from Figure 50, filtered (230 V_{RMS}, 50 Hz sine)

The slow triangle voltage measurement shown in Figure 52 clearly shows a different behavior then with the CFL bulb. Instead of drawing an almost constant current when in steady operation, the SMPS draws a lower current when the voltage is higher. This is not unexpected, as the SMPS on its secondary side needs to provide a constant voltage and current (and hence power) regardless of input voltage. To maintain the power needed to provide the secondary side, more current needs to be drawn as the voltage drops.

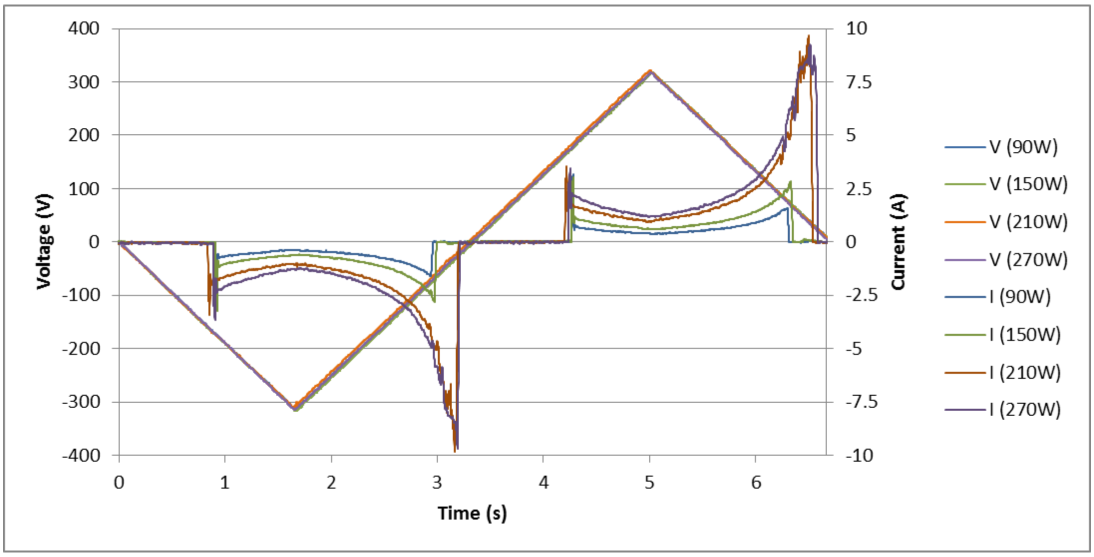

Figure 52: Slow triangle voltage measurement (filtered) for various loads

The V-I curve that results from the triangle measurement is shown in Figure 53. Again start-up effects are removed from the measurement to produce this plot. Multiplying the voltage and current in this V-I curve creates the voltage-power curve in Figure 54, which indeed reveals that the SMPS draws a constant power as long as it can maintain it.

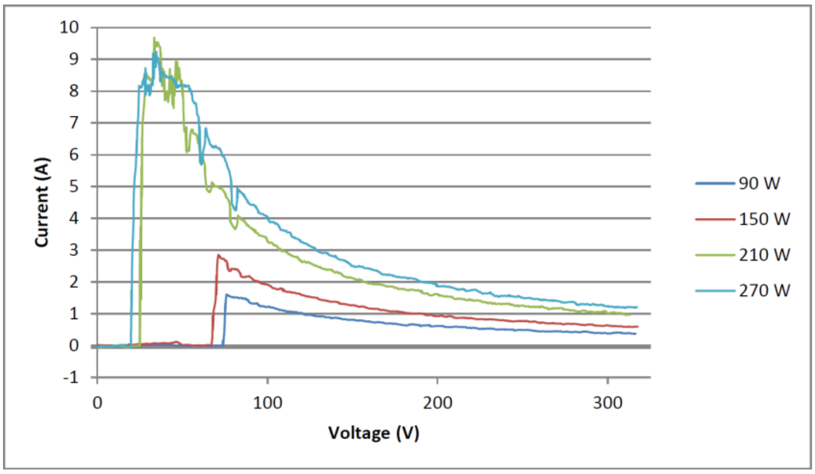

Figure 53: V-I curve resulting from the slow triangle voltage measurement (filtered) for various loads

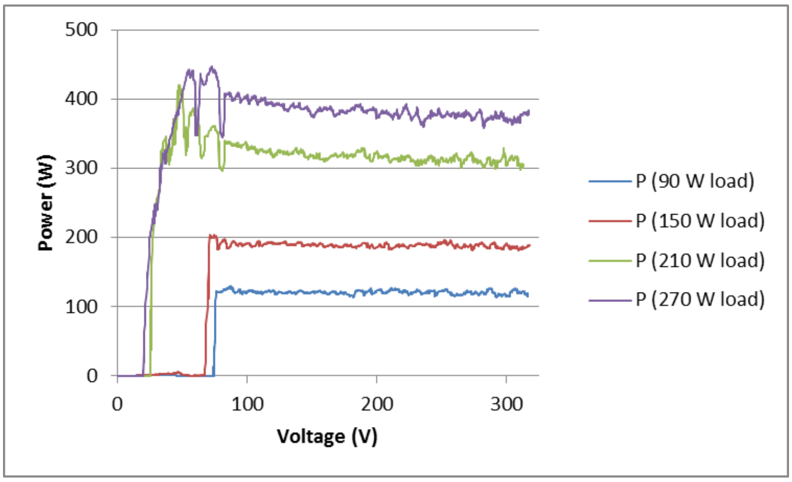

Figure 54: V-P curve (power as function of input voltage) resulting from the slow triangle measurement

The responses to over- and under voltages in Figure 55 show that the current magnitude goes up as the voltage goes down, as is expected from the slow triangle voltage analysis. It should be noted however that the current waveform not only changes in amplitude, but also somewhat changes in shape as well, more so than when the load was varied in Figure 50.

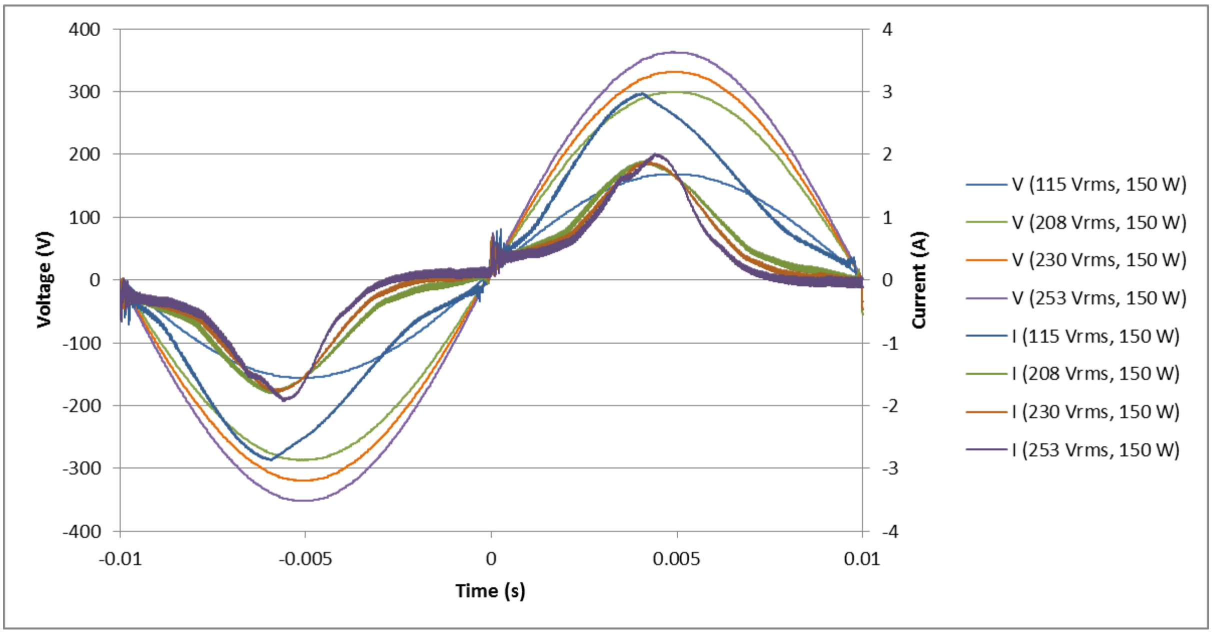

Figure 55: Behavior SMPS for different RMS voltages (load: 150W)

In Figure 56 we see the response to the 230 V_{RMS} Carré building voltage, for the various loads. Just as with the clean voltages in Figure 50, the currents seem to be scaled versions of each other, however the amplitude of the distortions seem to be fairly constant.

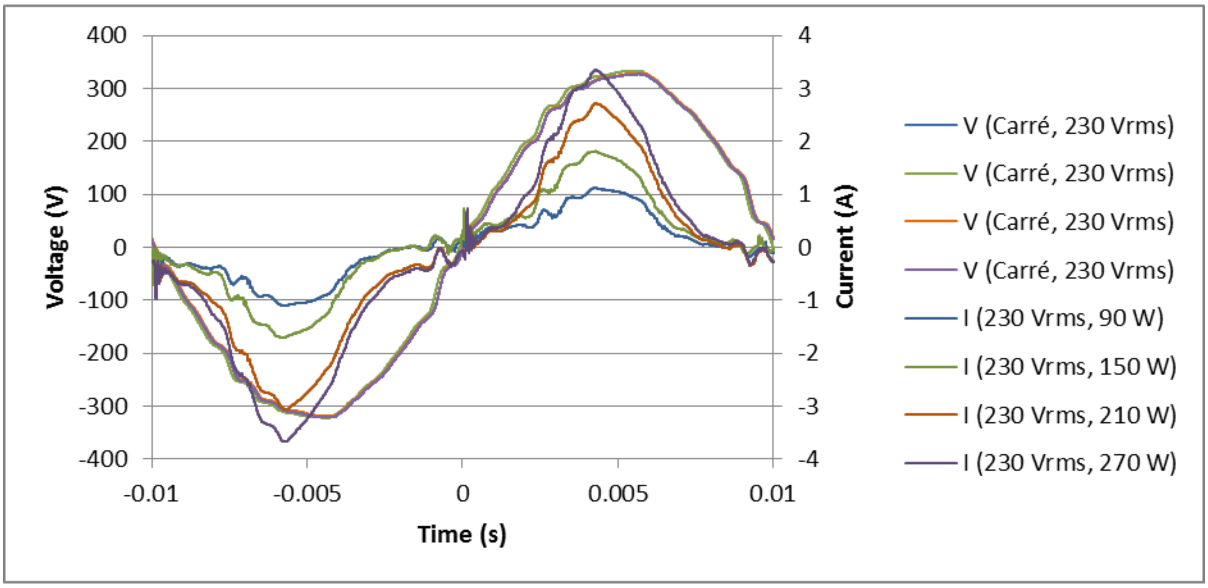

Figure 56: Behavior SMPS when excited by reconstructed Carré voltage for different loads (230 V_{RMS}, filtered)

8 Model Validation: Gray-Box Models

In this chapter the gray-box models developed in this work are checked for accuracy and if they competent in achieving the goals for this work. However before this can be done in a meaningful way, first the measurement setup needs to be looked into. After all, you cannot make a good model based on measurement, if the measurement setup influences the behavior of the DUM in an unpredictable or undocumented way. In other words, in order to get a simulation of a DUM to resemble a measurement, the measurement setup needs to be modeled as well. After that, the accuracy of the *Rectifier without PFC* model is looked into, as well as the accuracy of the MATLAB script for parameterizing this model. The Active PFC model is analyzed next. Various other DUMs are modeled using either model, following the procedure in the Manual (Chapter 9). Their accuracy of the models for these DUMs is explored as well.

8.1 Measurement Setup Validation

In this section we will look into how well the measurement setup is represented in the SPICE models, and what needs to be done to let the SPICE model perform realistically. This will be done by comparing the output of the *Rectifier without PFC* model to the measurements on the CFL bulb, in particular with the distorted voltage waveforms. The data processing is explored that needs to be performed to come to a good agreement between simulation and measurement. The match that is achieved in this section also validates the *Rectifier without PFC* model to a large extent.

The programmable power supply used in the measurement is designed to be low impedance for frequencies of up to several tenths of kilohertz. The first thought is then to model the power supply as an ideal voltage source. The gray-box model however is very sensitive to distortions in the voltage wave from. This is simply because the same is also true for the actual DUM. This means that when a measured voltage waveform is used as the input of the gray-box model, the measured voltage waveform data needs to meet some requirements. In the following section it is first shown what happens when the requirements are not met and after that the requirements are presented and the improved results are shown.

8.1.1 Averaging and Filtering of the Voltage

Figure 57 shows the current response of the SPICE model to the voltage waveform measured at the Thales EMC lab, together with the measured response. In this figure, the voltage waveform is directly imported from the scope without any averaging on the scope or filtering done afterwards. Figure 57 shows a great deal of noise on the *simulated* current. It was thought that this might be to do with the noise in the voltage measurement that was serving as input waveform for the simulation. To verify this, another measurement was performed, where the scope averaging function was set to its maximum, and the data was not saved until the waveforms stopped changing on the screen. When this measurement was used as input, the situation improved somewhat, as can be seen in Figure 58.

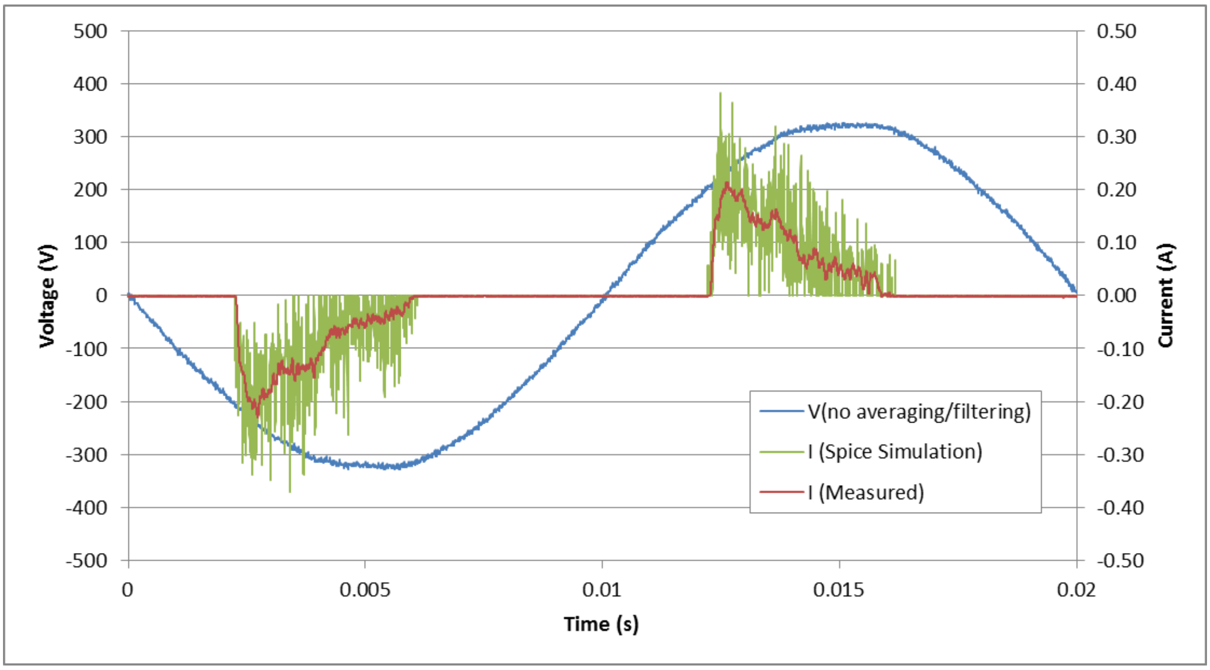

Figure 57: Comparison: SPICE simulation (with unfiltered/averaged voltage waveform as input) vs. measurement using power supply - Thales voltage waveform

But even in Figure 58, there is still too much noise on the simulated current. Closer inspection on the voltage waveform however reveals what looks a little bit like quantization noise. The solution to this is to apply a moving average filter, with an averaging window of 38 µs (N = 19 taps). This can easily be done in Excel as is explained in Section 9.3. The result is shown in Figure 59. The choice of 19 taps appears to be a good value in combination with the equipment that was used, as a longer filter (i.e. with more taps) makes the current waveform look as if it has been low-pass filtered compared to the measurement, and a shorter filter still leaves too much noise.

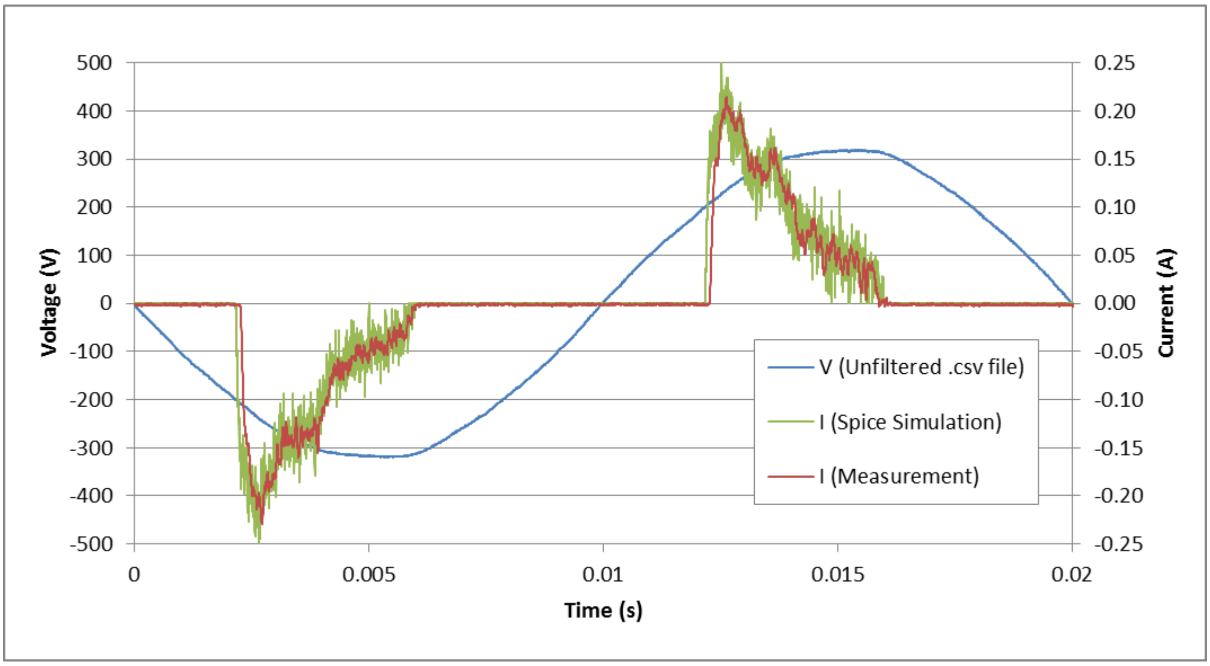

Figure 58: Comparison: SPICE simulation (with averaged but unfiltered voltage waveform as input) vs. measurement using power supply - Thales voltage waveform

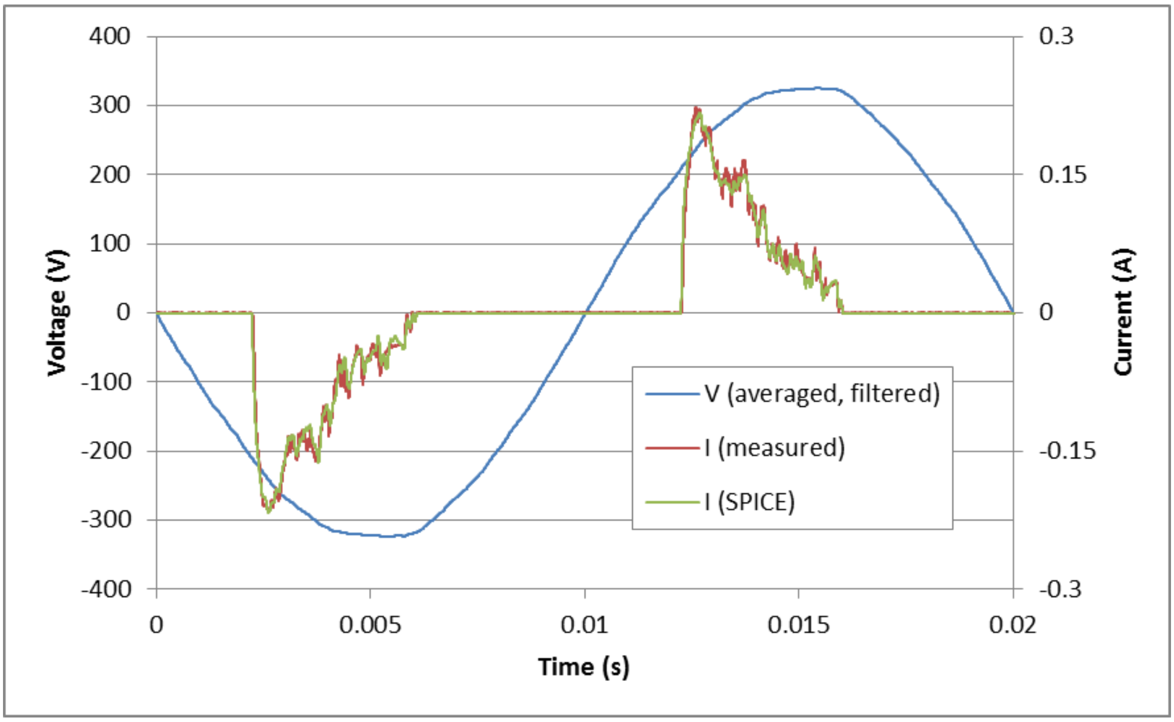

Figure 59: Comparison: SPICE simulation (with averaged and filtered voltage waveform as input) vs. measurement using power supply - Thales voltage waveform

In Figure 59, it can be seen that the simulation comes fairly close to the measurement, when the measurement is considered where the CFL bulb is fed by the Power supply. The simulation matches the measurement with the power supply more closely than the measurement performed directly to the power outlet, which is shown in Figure 60. This suggests that the source in the spice model more closely resembles the power supply than the power outlet.

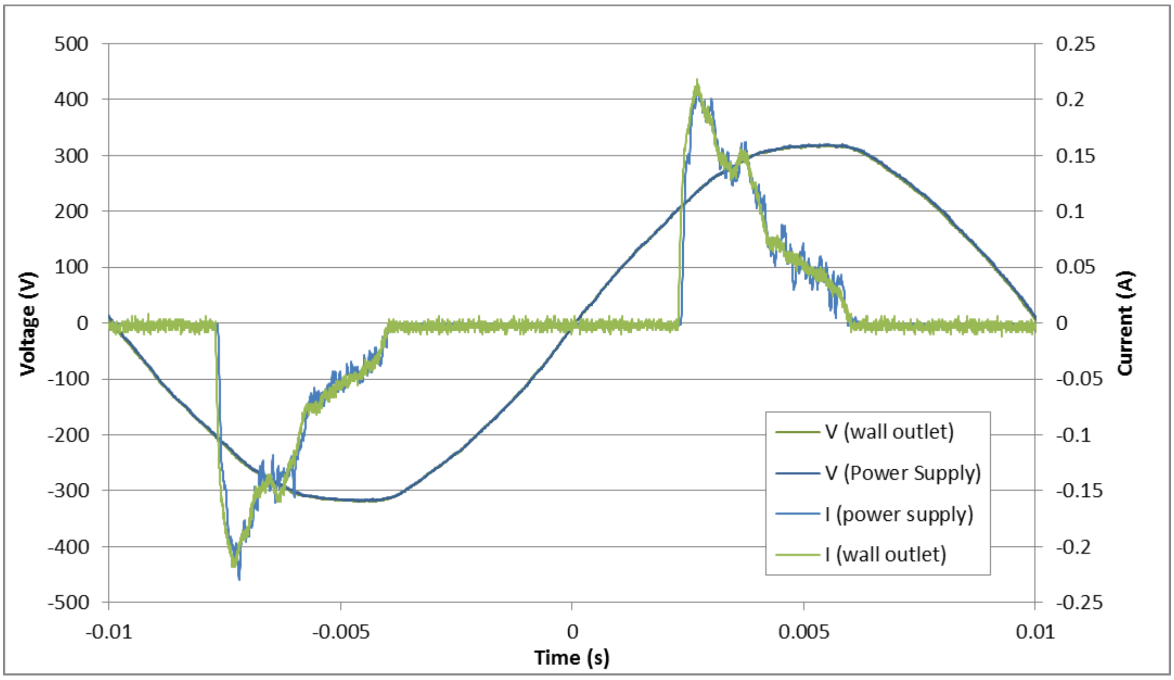

Figure 60: Comparison of CFL behavior: plugged directly into the wall outlet, vs. connected to the power supply. (Same plot as in Figure 40)

In Figure 61 the measurement with the reconstructed Carré voltage waveform is shown, together with the SPICE simulation. The voltage waveform has been averaged during measurement and filtered, just like before. Again, the simulated current waveform agrees to a large extent with the measurement, albeit that the simulation still has a little bit more noise.

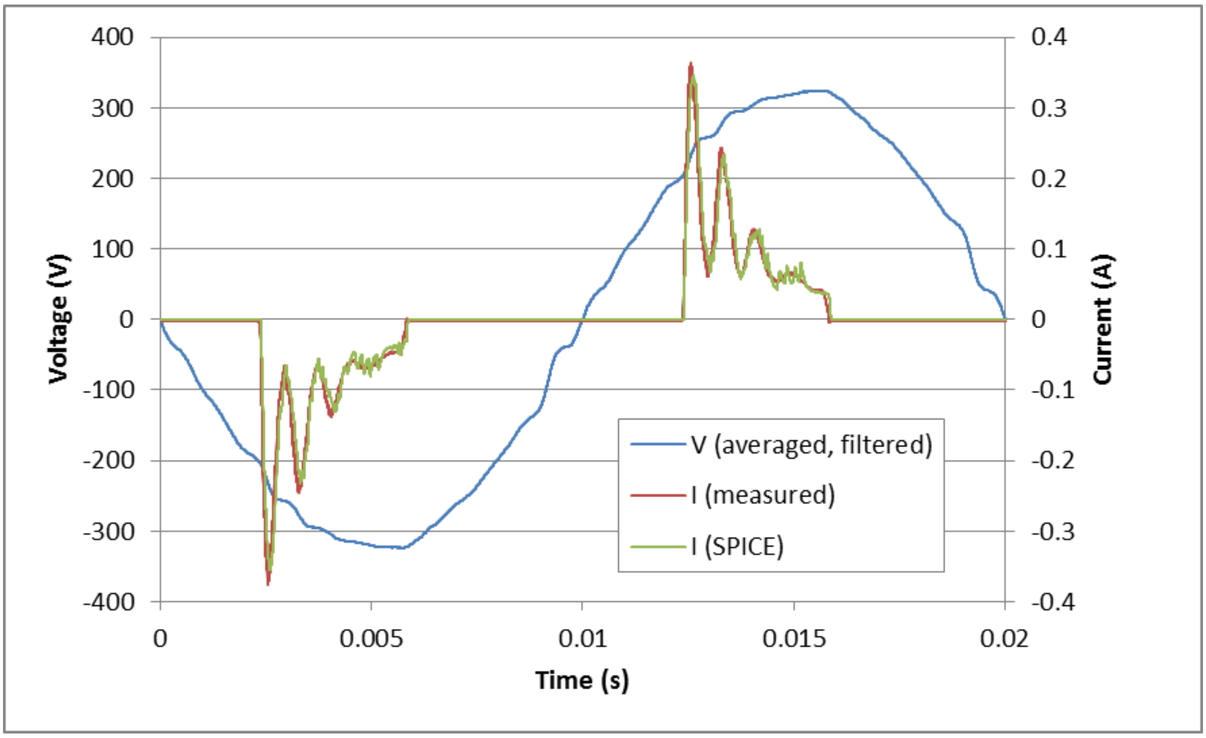

Figure 61: Comparison: SPICE simulation (with averaged and filtered voltage waveform as input) vs. measurement using power supply - Carré voltage waveform

8.1.2 DC Voltages

For the SPICE model, it is very important that the input voltage has no DC offset. A DC offset mainly influences the moment in time when the current peaks start. With a positive DC voltage, the positive pulse will start sooner, and the negative pulse will start later, and vice versa.

8.2 Rectifier without PFC Model

In this section the accuracy of the *Rectifier without PFC* model is checked as well as the accuracy of the parameterization script, when presented with different kinds of measurement. In the previous section however, the accuracy of the model with respect to the voltage distortion is already shown in Figure 59 and Figure 61, where very good agreement with measurement is shown. The responses to over- and under voltages are shown in Figure 62. The model shows good agreement in both plots. Figure 63 shows how the model responds to variations in frequency. Also in this situation the model is in good agreement with measurement.

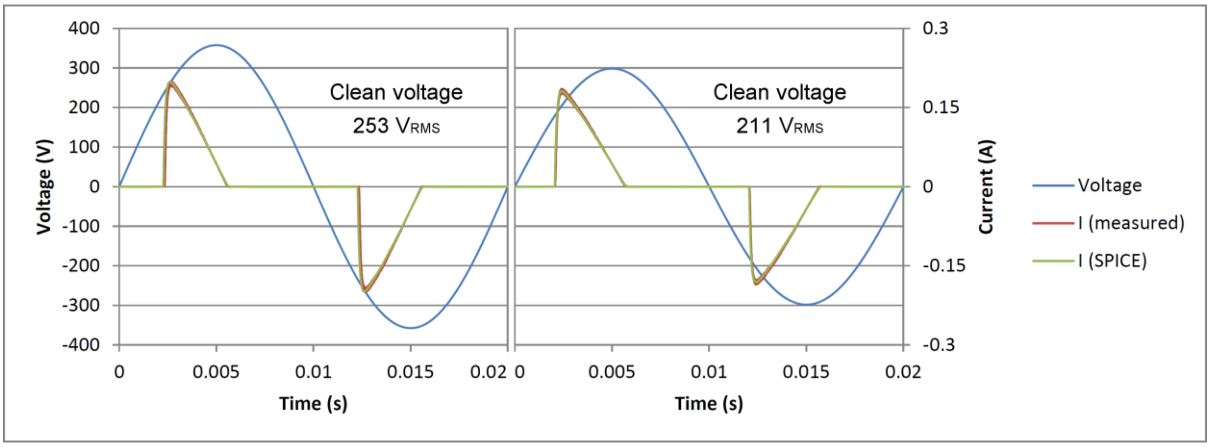

Figure 62: CFL bulb simulation vs. measurement: Over- and under voltage

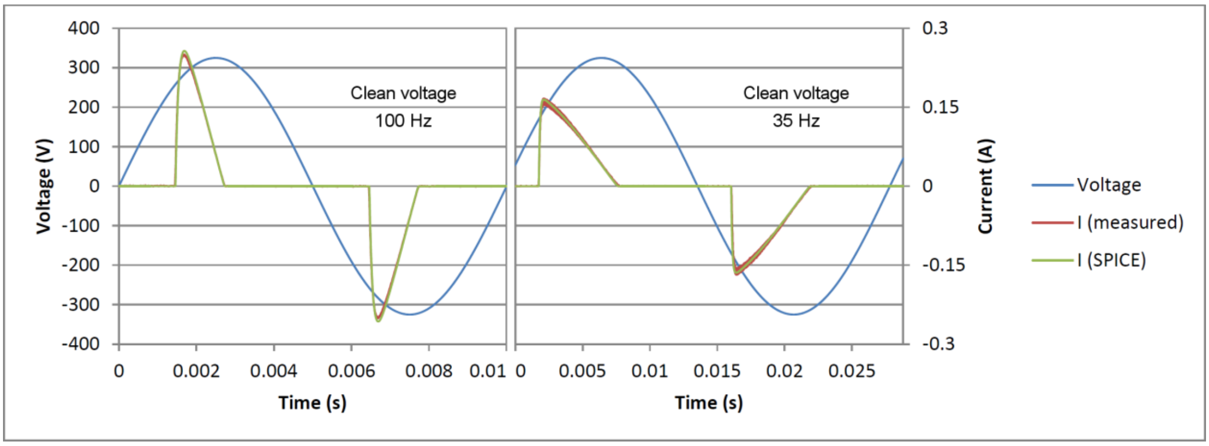

Figure 63: CFL bulb simulation vs. measurement: 100 Hz and 35 Hz sine voltages

Computational Complexity of the *Rectifier without PFC* model

To get an idea of how computationally intensive the *Rectifier without PFC* model is, several longer simulations have been performed.

The computer used for this test is a Toshiba Portégé M700 tablet PC laptop, with a Core2Duo T8100 CPU (2 cores) at 2.10 GHz, 2 GB of RAM, running Windows 7 (32 bit version) and LTspice IV (version 4.16h). The laptop was running in high performance mode, and had its power supply connected. This laptop is a business model that was sold until the end of 2009.

Where the simulation is run using the Carré voltage, at the start of the simulation the voltage waveform needs to be expanded by LTspice, i.e. the data in the file the voltage is read from needs to be repeated to extend the simulated time. When LTspice does this, it says “Expanding repeating PWL()” in the status bar. The time taken for this step has been recorded separately and is not included in the ‘*simulation run time’*, since it is not part of the model. In LTspice, the alternate solver was used, and the maximum time step in the simulation was 0.01 ms. The results are summarized in Table 2. It is interesting to note that the time taken to expand the measured waveform scales very nonlinear with the increase of simulated time.

It should also be noted that when the voltage source is a simple sine function, and LTspice is not reading a measured waveform from file, the simulation is much faster. 10 seconds simulated time is done only a second or two, which is much faster than real-time. This means that reading the voltage waveform from a file is by far the most time consuming part of this simulation.

Table 2: Simulation speed *Rectifier without PFC* model

Simulated time	Simulation run time	Simulation speed	Time taken to expand repeating PWL
0.25 s	15 s	17 ms/s	4 s
0.5 s	31 s	16 ms/s	13 s
1.0 s	64 s	16 ms/s	49 s
10 s	2 s	5 s/s	< 1 s *

* ideal sine voltage instead of measured voltage

Parameterization Script in MATLAB

To assess the accuracy and flexibility of the MATLAB script that was developed for the *Rectifier without PFC* model, a variety of measurements of the CFL bulb have been analyzed by the script. The results are presented in Table 3. The most difficult calculations for the script are the estimation of R_{in}, and the capacitor. Note that the CFL bulb has a load that behaves most like a current source. This can be seen in in Table 3, by the fact that the current calculated by the script is much more consistent than the power and resistance calculations.

Table 3: Parameterization by MATLAB scripts from steady operation measurement. Component value printed on the capacitor found inside the DUM is 2.2 µF.

Measurement	R_{in} Ohm	C uF	I_{load} mA	P_{load} Watt	R_{load} kOhm
* 115V	31	1.79	47.8	5.97	2.37
211V	23	2.14	36.8	9.21	6.66
'Ideal'	44	2.15	38.5	10.5	6.97
253V	42	2.15	35.9	11.0	8.41
* 15Hz	31	1.92	37.4	9.32	5.91
35Hz	20	2.13	38.0	10.0	6.70
'Ideal'	44	2.15	38.5	10.5	6.97
100Hz	36	2.14	37.6	11.0	7.75
ideal	44	2.15	38.5	10.5	6.97
Thales (power supply)	36	2.17	38.6	10.7	7.10
Carré (power supply)	42	2.11	37.2	10.3	7.36
Thales (wall outlet)	40	2.11	38.7	10.5	6.89
Carré (wall outlet)	32	2.05	33.6	9.74	8.51

* possibly a local optimum

As can be seen in Table 3, most values for the capacitor *C* and the current thought the load I_{load} are close together, and the values for R_{in} are mostly in the same ball park as well. The values that are out of line have been highlighted. These only seem to occur when the DUM is operating outside of its design specifications and in the measurement done with the CFL bulb plugged directly into the wall outlet in the Carré building. The latter inaccuracy is thought to be due to the somewhat higher output impedance of the wall outlet on this location. The high value for I_{load} with the 115 V_{RMS} measurement was expected from the VI curve of the CFL bulb load (See Figure 45, in Section 7.2.1), and is accurate.

It is also interesting to note that the values obtained from measurements with distorted sine voltages appear to be almost as accurate as the clean measurements, even with the measurement where the DUM was plugged in the wall directly at the Thales EMC lab. This confirms that the script can be used to parameterize the DUM using measurements performed on site, and not only using measurements performed in a lab with a clean power source. This is however only under the condition that the output impedance of the wall outlet isn't too high. So even though it is possible, the most reliable results are still obtained with a lab setup.

8.3 Active PFC, PC Power Supply

In this section we will look into the performance of the *Active PFC* model in modeling the PC power supply. The performance is checked for accuracy in the case of distorted voltages, over- and under voltages, various values for the load and some combinations thereof. All measured currents are filtered.

The first simulation looked at here are the clean and Carré voltages, with the 150 W load. Since the parameterization of the model is based on these measurements, it is expected that the model performs best under these circumstances. The plots are in Figure 64, and indeed show excellent agreement.

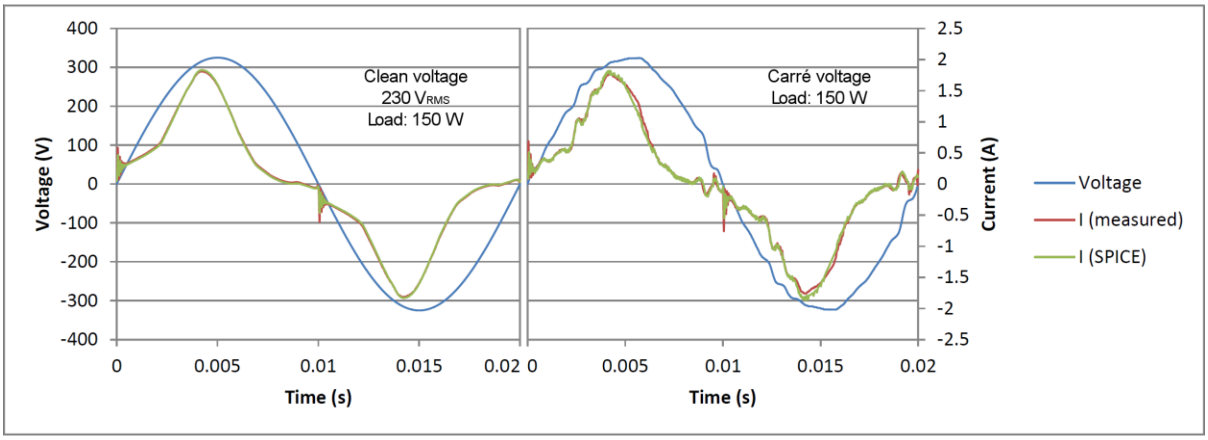

Figure 64: PC power supply simulation vs. measurement: Ideal and Carré voltages (Load: 150 W)

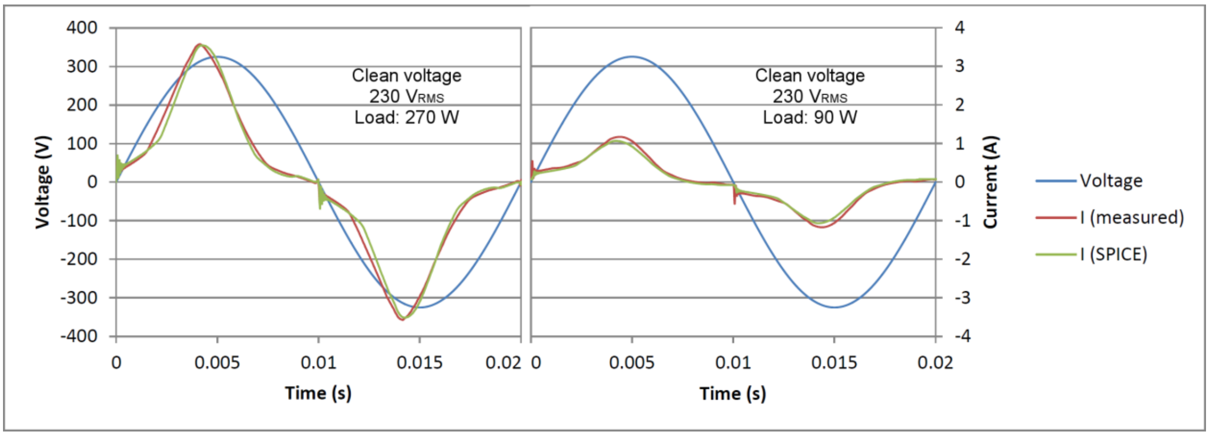

Figure 65: PC power supply simulation vs. measurement: Varying load (270 W and 90 W)

It is more interesting to see what happens when the simulation circumstances no longer match the circumstances of the prototype current measurement. Figure 65 shows what happens if the load is changed. The shape of the current waveforms has changed a little, but the match is still fair. Especially with the 90 W load, the efficiency of the DUM seems to have gone down a little compared to simulation, as the model draws a little less current than the DUM.

In Figure 66 the effect of over- and under voltages are shown, but still with the same 150 W load from the prototype measurement. Here it seems that the current waveform has changed shape somewhat more than with the varying load. In addition, in order to keep the power consumption constant, the model compensates the change in voltage by drawing extra current more than the actual DUM does. The error if this has been analyzed in Table 4.

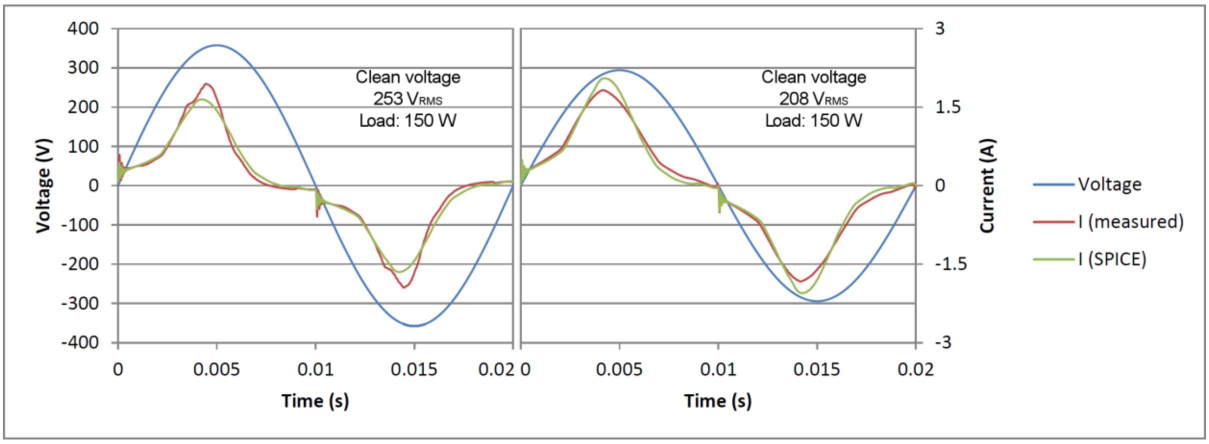

Figure 66: PC power supply simulation vs. measurement: Over- and under voltages (Load: 150 W)

Table 4: Analysis of how the PC power supply adapts to RMS voltage vs. the model

Conditions:	% change in RMS current compared to 230 V_{RMS}		% Error in RMS current, simulation vs. measurement
	Measured	Simulation	Resulting error
10% overvoltage	-4%	-10%	-6%
10% under voltage	6%	12%	5%
230 V_{RMS}			0.3%

Computational Complexity of the Active PFC model

To get an idea of how computationally intensive the *Active PFC* model is, several longer simulations have been performed.

The computer used for this test is a Toshiba Portégé M700 tablet PC laptop, with a Core2Duo T8100 CPU (2 cores) at 2.10 GHz, 2 GB of RAM, running Windows 7 (32 bit version) and LTspice IV (version 4.16h). The laptop was running in high performance mode, and had its power supply connected. This laptop is a business model that was sold until the end of 2009.

The simulations were run once using the Carré voltage, and once using an ideal sine voltage generated by LTspice. In the case of the Carré voltage, at the start of the simulation its repeating waveform needs to be expanded by LTspice, in addition to the prototype current waveform, that will always need expanding. When it does this, it says "Expanding repeating PWL()" in the status bar. The time taken for these startup tasks was recorded separately and is not included in the '*simulation run time'*. It may be part of the model in the case of the prototype current, but it is relevant to note how the time taken for this step changes with the simulated time separately. Thus '*Simulation run time'* is only the time during which the simulation itself is running. In LTspice, the alternate solver was used, and the maximum time step in the simulation was 0.01 ms. The results are shown in Table 5 and Table 6. It is interesting to note that the time taken to expand the measured waveform scales very nonlinear with the increase of simulated time.

Table 5: Simulation speed *Active PFC* model, measured Carré voltage used

Simulated time	Simulation run time	Simulation speed	Time taken to expand repeating PWL
0.25 s	26 s	9 ms/s	6 s
0.5 s	54 s	9 ms/s	23 s
1.0 s	115 s	9 ms/s	86 s

Table 6: Simulation speed *Active PFC* model, ideal sine voltage used

Simulated time	Simulation run time	Simulation speed	Time taken to expand repeating PWL
0.25 s	27 s	9 ms/s	4 s
0.5 s	54 s	9 ms/s	15 s
1.0 s	108 s	9 ms/s	48 s

8.4 Different DUMs with the Same Model

In this paragraph several different DUMs are modeled using the models and parameterization techniques developed in previous chapters. The manual (Chapter 9) will be used as a guide for parameterizing the models and the steps outlined in the manual will be referenced in this Section. First we will look at a small DC adapter, that fits in the *rectifier without PFC* category, and after that we will look at two SMPSs with active PFC, in this case a laptop power supply and a fluorescent tube.

8.4.1 DC Adapter (Rectifier without PFC)

A small DC adapter (5 V, 2 A max, brand: DVE, model: DSA-0101F-05) that shipped with an ASUS wireless router is the DUM. This is only a 10W power supply, so it does not have a PFC. It *is* however a SMPS. Because of this it is expected that the load will draw a constant power, regardless of input voltage. To make the measurements repeatable, a resistor has been used as a load, instead of the router that the DUM shipped with. A resistance of 3 Ω was used, which should draw about 1.6 A, well within specifications of the adapter.

Figure 67 and Figure 68 show the slow triangle measurement and the power versus voltage plot that results from this measurement. This confirms the expectation that the load would be a constant power load, across normal operating voltages. This is the conclusion from Step 1 in the manual.

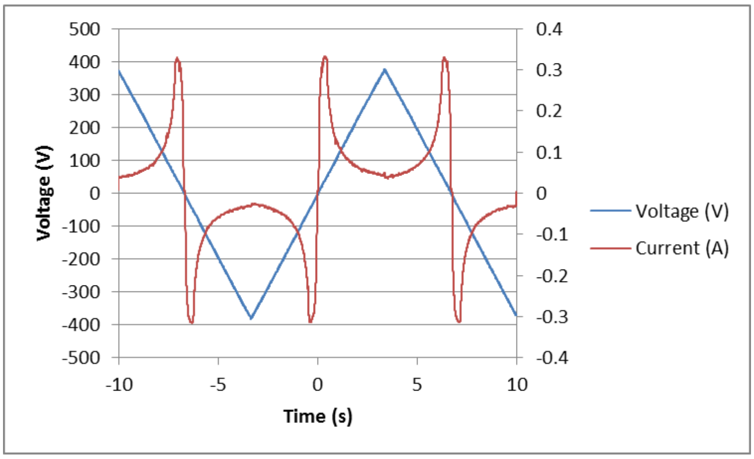

Figure 67: Triangle measurement DC adapter

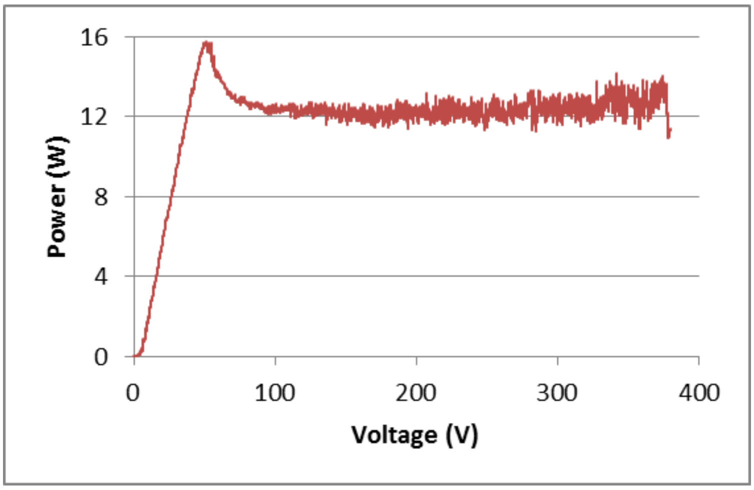

Figure 68: DC adapter, power vs. DC voltage

The MATLAB script analyzed the dirty Carré voltage measurement (Step 2), and found the following relevant values: R_{in} = 74, C = 10.5 µF and P_{load} = 12.1 W. When it came to R_{in} however, two very different values were found for the clean sine voltage waveform case and Carré voltage waveform case. For the former 74 Ω was found, and for the latter 44 Ω. Therefore, the average value of 59 Ω was taken. With these values, the results were obtained shown in Figure 69 and Figure 70.

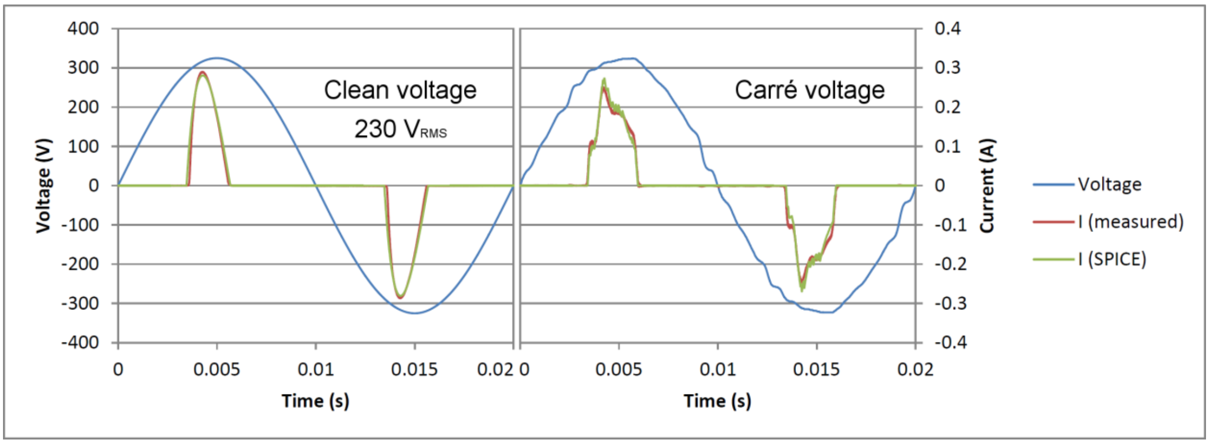

Figure 69: DC adapter simulation vs. measurement: 'ideal' and Carré voltages

In Figure 69 the clean 230V_{RMS} and Carré measurements are shown. With this value for R_{in}, it can be seen that the current peaks in the simulation (green) are not quite as sharp as in the measurement (red) in the clean voltage case, which indicates a too high value for R_{in}. On the other hand, in the Carré voltage waveform case, the simulated current peaks are a bit too sharp, indicating a too low value for R_{in}.

Figure 70 shows the simulation and measurement with clean sine voltages of different RMS value. The DUM is seen to adapt its current accurately to small changes in RMS voltage, making the reason visible for choosing the constant power load for this DUM.

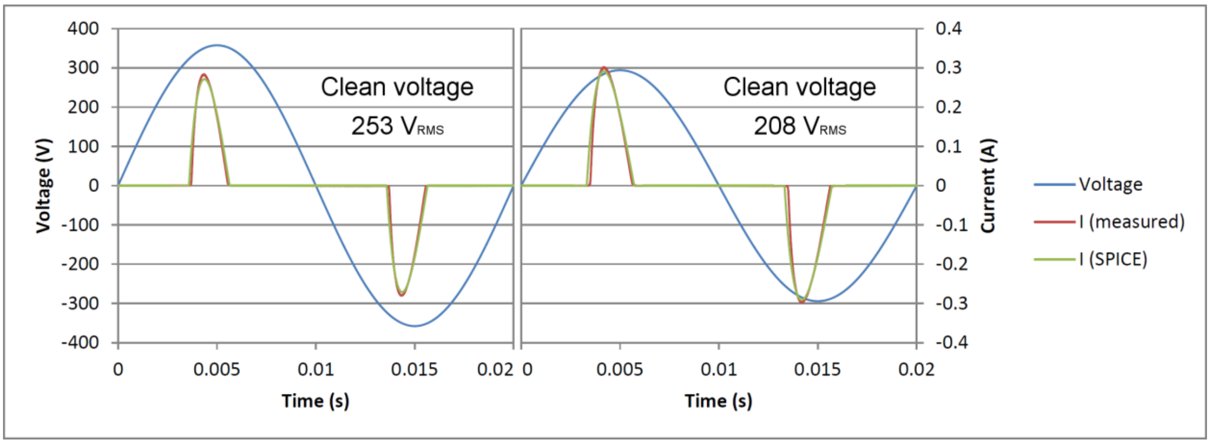

Figure 70: DC adapter simulation vs. measurement: over- and under voltages

8.4.2 Laptop Power Supply (Active PFC)

In this section we look at a laptop power supply. During the course of the analysis of this DUM some improvements to the model have been made, and this DUM is also used to make example plots in the manual (Chapter 9). Note that all the measured currents in this section have been filtered.

The measured half-wave and the prototype current initially made for this model in Step 1 is shown in Figure 71.

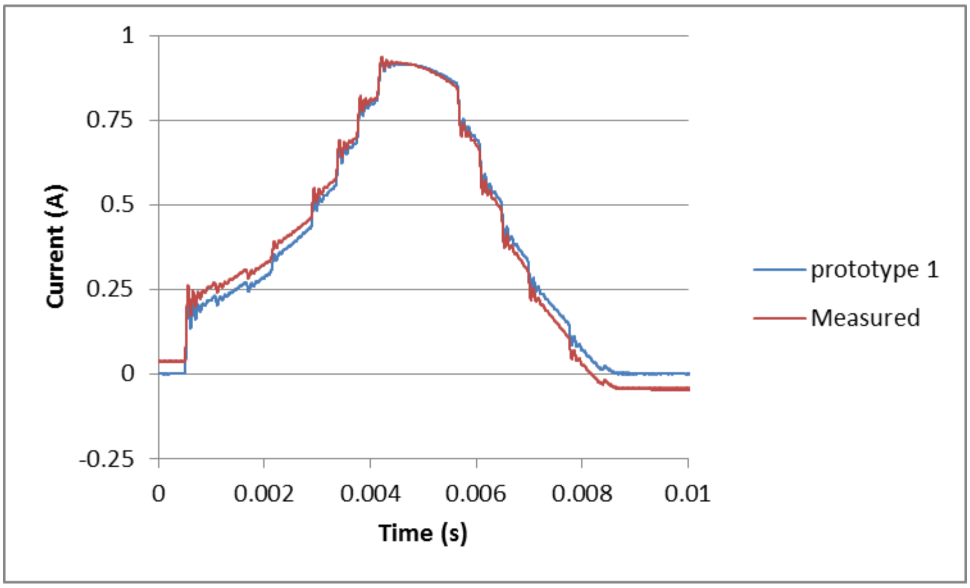

Figure 71: Laptop power supply: Measured half-wave and preliminary prototype current waveform

The line capacitor current had an amplitude of about 40 mA, which equates to 0.4 µF line filter capacitance. The prototype current was measured with a 100 W load. With the load in the simulation set to this value, the amplification factors for the prototype current sources were estimated to be 0.2 for the vertical source, and 0.8 for the horizontal source (Step 2). With these values, the simulation current best matched the measured current.

When looking at the simulation with the distorted voltages in Step 3, the best match in was obtained with C_1 = 1.5 µF. The simulation together with the measurement is shown in Figure 72. At this stage the model accuracy is still poor, but the goal at this stage is to match the amplitude of the *distortions* away from the voltage zero crossings. And as is illustrated by the highlighted detail in the figure, this amplitude matches.

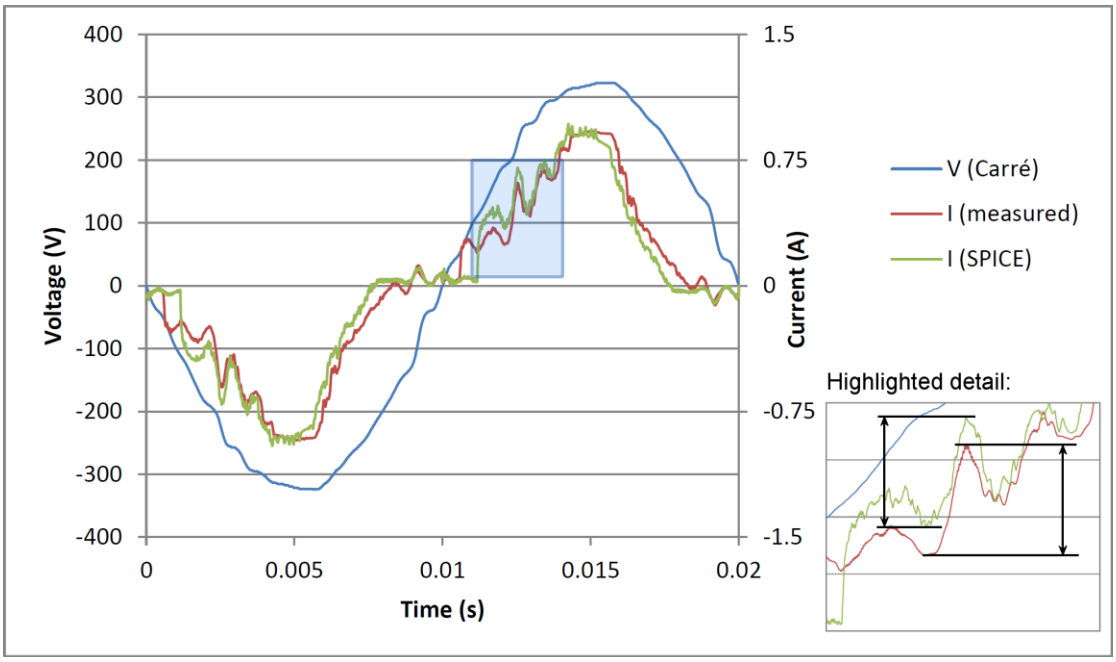

Figure 72: Laptop power supply: Estimating C_1 from distortion amplitude

With the size of C_1 now known, the final prototype current can be made (Step 4). The result is plotted in Figure 73. The simulation and measurements with the 'ideal' and Carré voltage are plotted in Figure 74. The effect of the last change in the prototype current is evident when compared to Figure 72, above.

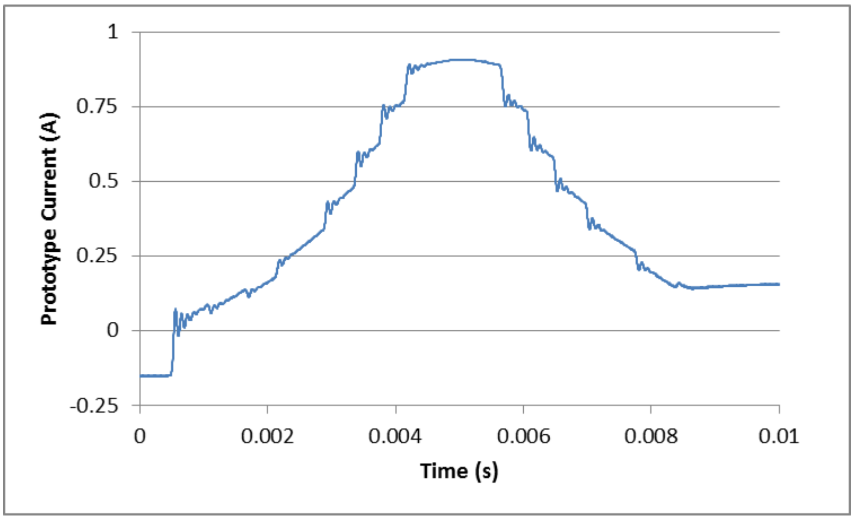

Figure 73: Laptop power supply: final prototype current waveform

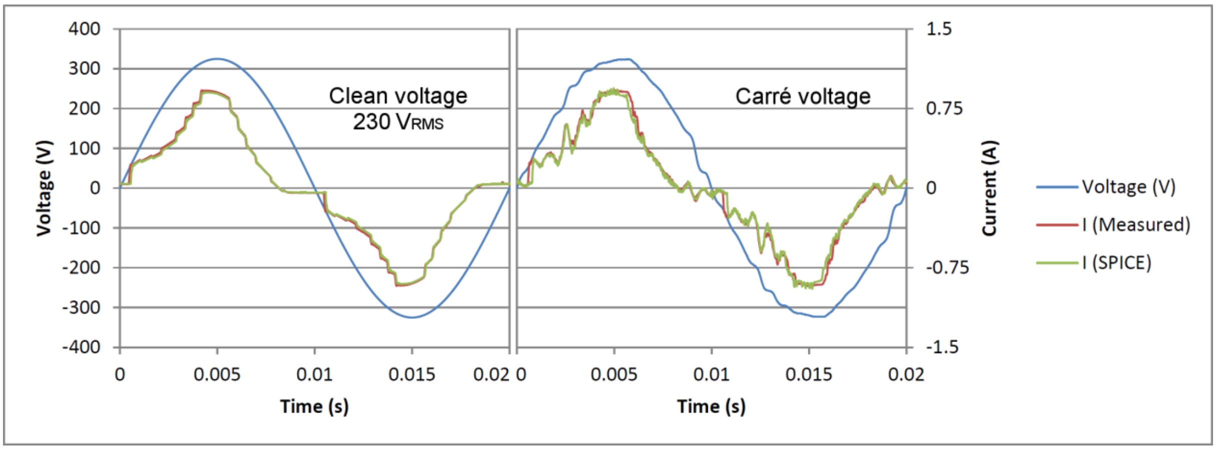

Figure 74: Laptop power supply simulation vs. measurement: 'ideal' and Carré voltages (Load: 100W)

Both plots in Figure 74 are still with the same load as with the prototype current measurement and with the same 230 V_{RMS} voltage, albeit with distortion in the case of the Carré voltage. Under these circumstances, the model is very accurate. However when the RMS voltage or load is changed, the simulation starts to differ more from the measurement. This can be seen from Figure 75, where the RMS voltage is varied ± 10%.

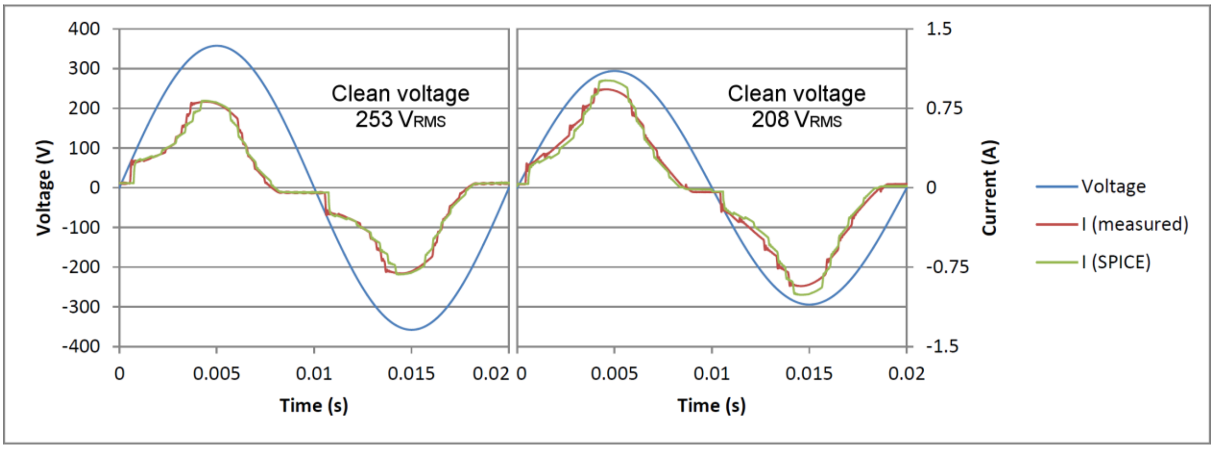

Figure 75: Laptop power supply simulation vs. measurement: 10% over- and under voltages (load: 100W)

It becomes even more obvious when also the load is varied. To illustrate this, in Figure 76 first only the load is increased to 124 W (left) and then the voltage is increased as well (right).

In the Figure 76 it can be seen that, aside of their shape, the total current also differs between the simulation and measurement. This is because the model assumes the DUM has the same efficiency for every load, which is not the case. The load parameter will need to be adjusted to compensate for the change in efficiency, if this inaccuracy is a problem.

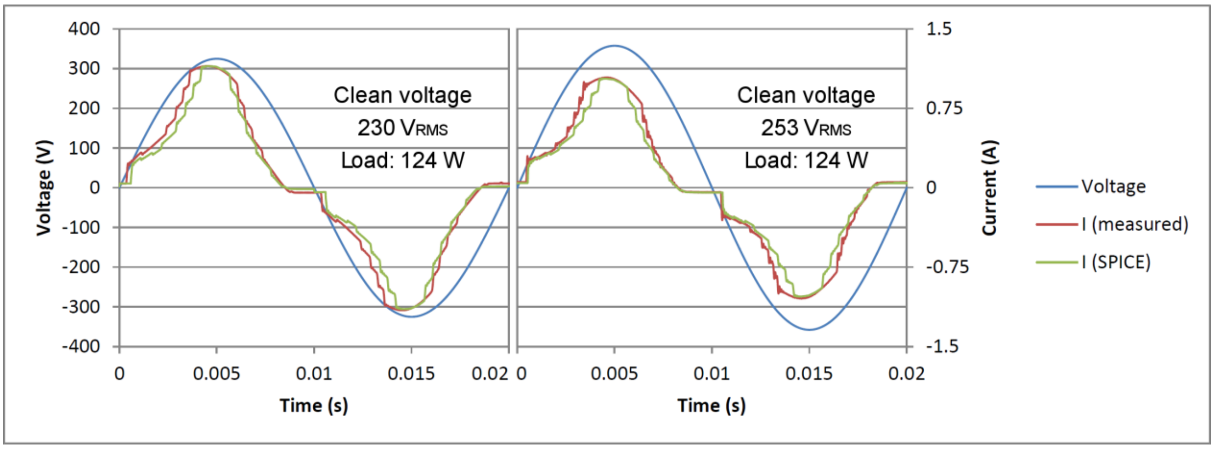

Figure 76: Laptop power supply simulation vs. measurement: Higher load, 'ideal' voltage and overvoltage

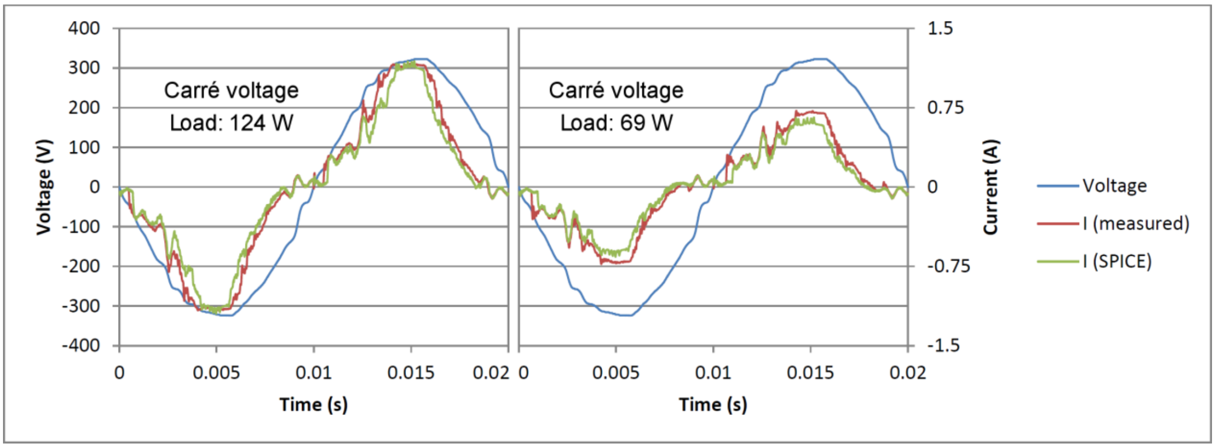

Figure 77: Laptop power supply simulation vs. measurement: Higher load and lower load, Carré voltage

As mentioned before, the shape of the current waveform changes when the load changes. However what does remain accurate is the reaction of the current to voltage distortions, as can be seen from Figure 77, where in both graphs the same 230 V_{RMS} Carré voltage is used, but with different loads. The basic shapes of the current waveforms are different as expected, but the way they are distorted looks very similar.

8.4.3 Fluorescent Tube (Active PFC)

Another DUM that was analyzed was a fluorescent tube (PHILIPS Electronic Ballast, HF-Regulator II, HF-R TD 154 TL5 EII, rated 54 W). This DUM has a SMPS with active PFC. It was measured to consume about 60 Watt of power, which for lighting means a PFC is mandatory. In this case, the load was always the same (the DUM is an armature for a single tube) which made modeling it a little less work. Note that all the measured currents in this section have been filtered.

The measured half-wave and the preliminary prototype current made for this model in Step 1 is shown in Figure 78. Note that the prototype current starts and ends at zero ampere, while the measured current, due to the capacitive current though the line filter, does not.

Since the load in this case is part of the DUM itself (the fluorescent tube), rather than a parameter of its environment, the value of the load does not have to reflect the actual power the fluorescent tube consumes, as long as the current amplitude matches.

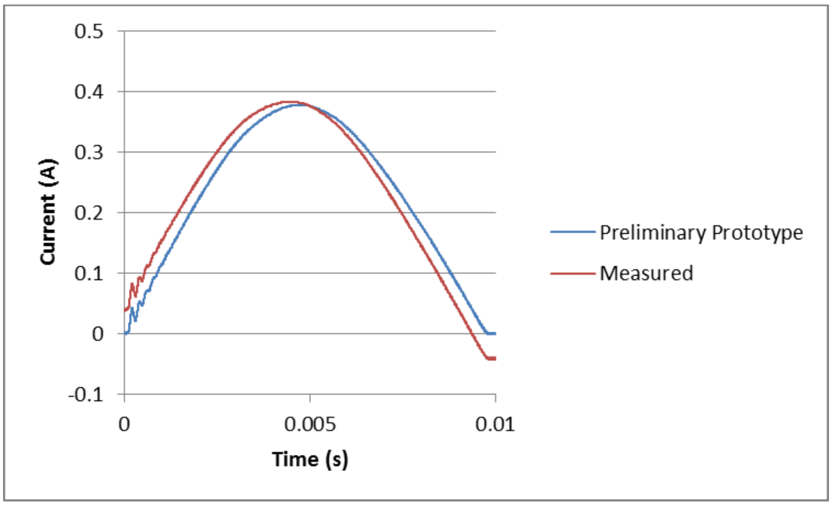

Figure 78: Fluorescent tube: Measured half-wave and preliminary prototype current waveform

For this reason, in Step 2 we can just put the amplification factors of both prototype current sources to 0.5 (default value), and tune the load value to get a match in current amplitude. This match is found to be at 39 Watt, though this number has very little to do with the power drawn from the mains or consumed by the fluorescent tube.

In Step 3 it is observed that the line filter capacitive current had an amplitude of about 41 mA, which equates to 0.4 µF line filter capacitance. The simulation is run using the Carré voltage and the preliminary prototype current, and the result is compared to measurement. The value of C_1 was varied to find the best match in the amplitude of the current distortion. The value found for C_1 was 0.3 µF, which equates to a current amplitude of about 32 mA through this component. This simulation can be seen in Figure 79, with the preliminary prototype current and the value for C_1 that was found, together with the measurement.

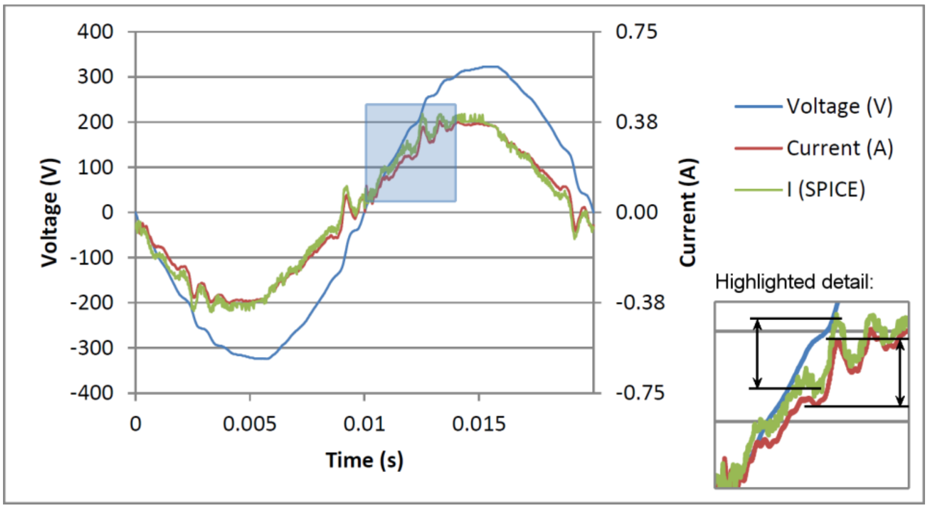

Figure 79: Fluorescent tube: Estimating C_1 from distortion amplitude

Adjusting the prototype current for the found value of C_1, makes the final prototype current look as shown in Figure 80 (Step 4). Note the prototype current pulse does not begin or end at zero, or even at the same current. This implies there will be a step in the prototype current as it is repeated. This is correct however, because there is also such a step in the capacitor current of C_1, because the derivative of the voltage across C_1 (V_{pulse}) has a step also.

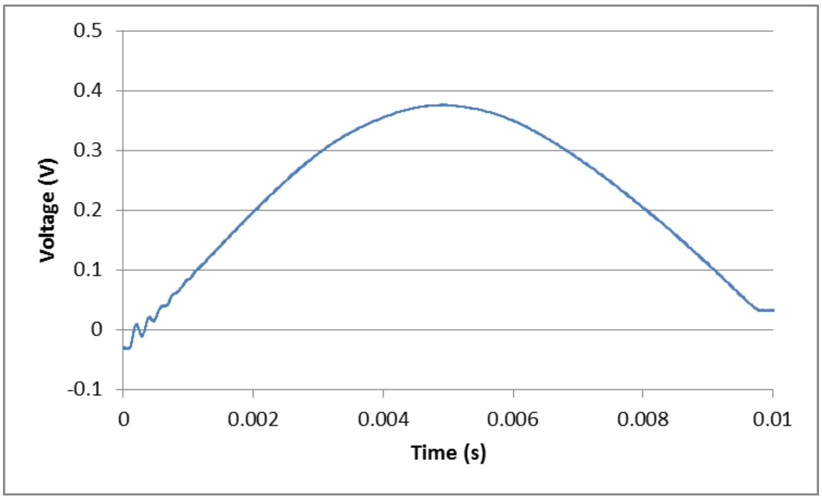

Figure 80: Fluorescent tube: final prototype current waveform

The simulation results obtained with the final prototype current for the 'ideal' and Carré voltages are compared to measurement in Figure 81. The match can be seen to have very good accuracy.

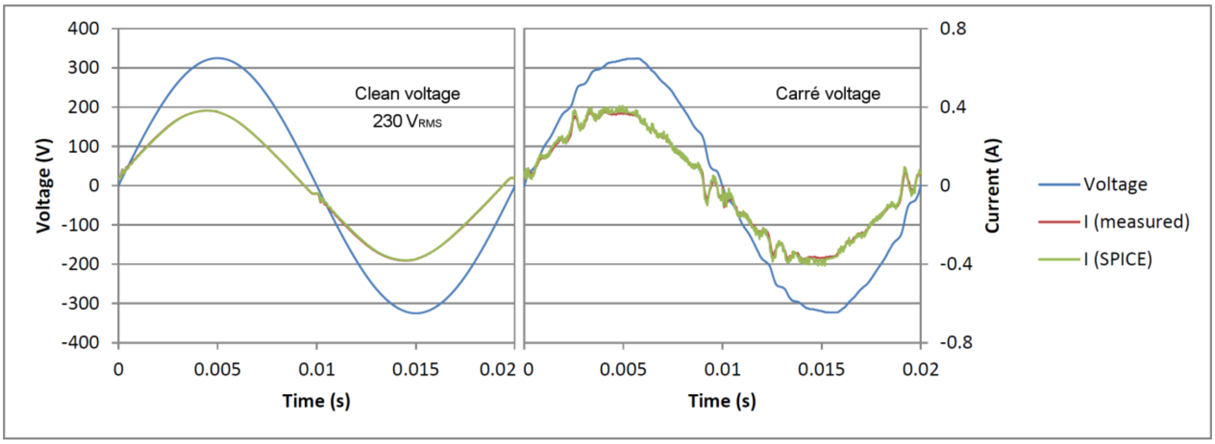

Figure 81: Fluorescent tube simulation vs. measurement: 'ideal' and Carré voltages

Figure 82 shows over- and under voltage simulation and measurement, also showing good agreement. In Figure 83 the Carré voltage is scaled to a 10 % under voltage (208 V_{RMS}), in which case still an good match is seen. This DUM appears to lend itself exceptionally well to be represented by this model.

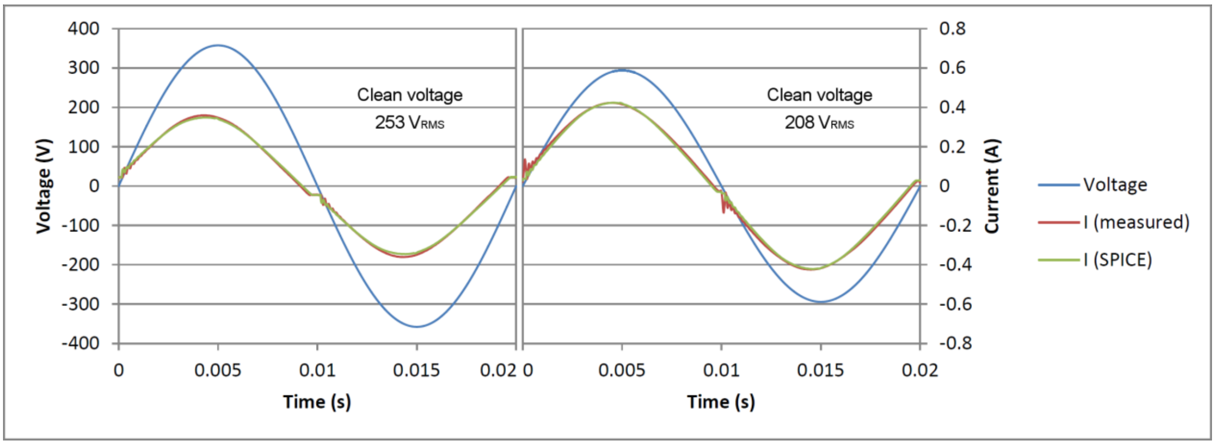

Figure 82: Fluorescent tube simulation vs. measurement: 10% over- and under voltages

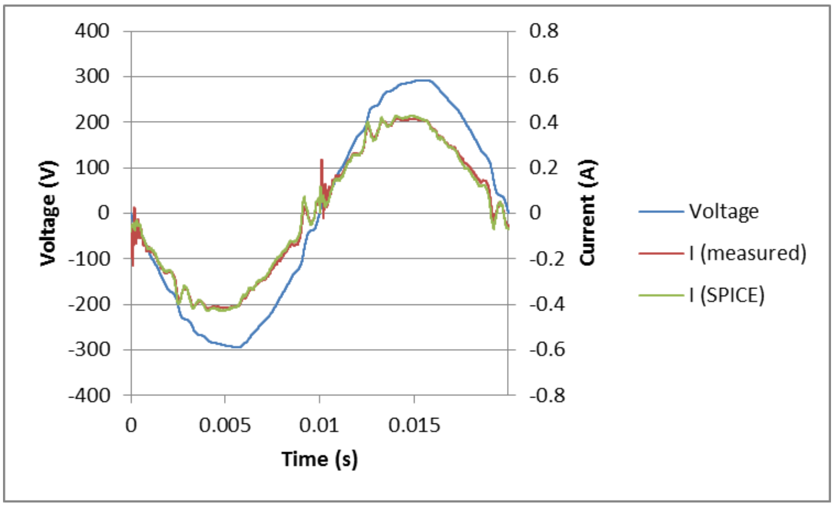

Figure 83: Fluorescent tube simulation vs. measurement: Carré voltage scaled to 208 V_{RMS}

8.5 Model Limitations and Considerations

The models developed in this work have been developed with a specific purpose, as has been outlined in the introduction (Chapter 0). The models are meant to be part of a simulation of the power network of a building, to aid in predicting the power quality and making design choices for these networks. The requirements for these models that come forth of this goal have been defined in Section 5.1. The choices that have been made in order to meet these requirements come at the cost of some limitations that the user of the model will need to take into account. In this section, these limitations and how to deal with them is are explained, and some general considerations are provided as well.

Diversity of Models

Do not simulate a whole network with only one distinct model per category. Use at least several different models of loads without PFC, (CFL bulb, phone chargers, etc.), because when the value of the DC voltage and its ripple are different, the timing of the current peaks will change as well. Using only one kind of CFL bulb in a simulation of a building and nothing else in that category, will probably not yield realistic results.

For the active PFC model, this is even more important, as the prototype current waveform is fixed. The reason for this is that the model will respond inaccurately if the conditions during simulation (RMS voltage and load) are very different from when the prototype current waveform was measured. The exact shape of the current waveform changes when these conditions change in the real DUM. But because of the prototype current principle, they do not change in simulation. In spite of the inaccuracies, the response is probably still realistic, because there is a wide variety in SMPSs and there might well be another SMPS that responds in the same way the model does in those circumstances. But when simulations are carried out with several SMPS models using the same prototype current waveform under different load conditions, the result will no longer be realistic, because their current waveforms will be too similar to each other. It will already be better if several prototype currents are used measured from the same DUM, but under different conditions. But even then, it is still very important to use models of at least several different DUMs.

Fixed Frequency in the Active PFC Model

In the Active PFC model, the frequency is fixed because the prototype current file will have a fixed time span. However, this is not expected to be a problem, because power quality will not be significantly influenced if the net frequency drifts by one or two Hertz. This means that fixing the frequency in simulation to an exact value is no problem, even if the actual power network represented in the simulation is an electrical island (e.g. a ship) where the local generator might drift in frequency somewhat. Problems with instantaneous jitter in the frequency with these models are in general not expected (though it is unknown how realistically the model will respond) as long as the average over several periods remains accurate.

9 Manual

In this chapter the way to use the SPICE models and how to parameterize them using measurements and the tools developed in this work is explained. Microsoft Excel™ or a similar software package will be required, and preferable also MATLAB. Basic knowledge of how to use SPICE, Excel and MATLAB is assumed. First we will look into the *rectifier without PFC* model, then the *Active PFC* model. At the end of this chapter it is explained how to apply a moving average filter in Excel, and how to import a (measured) waveform into SPICE.

9.1 Usage of the *Rectifier without PFC* Model

Parameterizing the *Rectifier without PFC* model is done by measuring the response of the DUM using a scope and with an active current probe that can accurately measure the current waveforms, including when there are periods of zero current (or DC) in the waveform. A MATLAB script is then used to analyze the measurements and it will extract all parameters: R_{in}, C, and three values for the load, I_{load}, R_{load} and P_{load}. If for any reason the MATLAB script fails to give an accurate or complete result, parameterization can be done manually as well.

First the measurements that are required or useful for parameterizing the model are presented, along with a brief description of what they are used for and what the main requirements for the measurements are. After that, the parameterization procedure is explained step-by-step.

Measurements:

- Required: Distorted sine voltage
  - Output impedance of the outlet or power source needs to be low, otherwise it will influence the current that the DUM draws.
  - Distortion must be severe enough to observe significant distortion in the current peaks
  - Distortion must not be so severe that individual current peaks are split in two, or it will confuse the MATLAB script. In that case, an additional measurement with a clean voltage will be required.
  - This measurement enables R_{in}, C and load estimation through the MATLAB script, if the above criteria are met.
  - This measurement also enables manual R_{in} estimation
- Optional: Clean sine measurements
  - Enables manual parameterization or parameterization by the MATLAB script, for instance useful if the distorted voltage measurement is not adequate. The results for C and the load should also be slightly more accurate; however, the result for R_{in} will be less accurate.
  - Not as suitable for manual estimation of R_{in}, though it is possible.
- Optional: Measurements at various RMS voltages
  - In case the behavior of the load is unknown, this enables estimation of whether it behaves like a constant DC current load, resistor or a constant power load. This knowledge also improves the accuracy of the initial parameter estimation of the MATLAB script significantly, and can be used to improve the voltage range over which the model is valid.

- Optional: Slow triangle voltage, or a series of DC-measurements
    - Can be used to obtain a V-I characteristic of the load
    - In case the behavior of the load is unknown, this enables determination of whether it behaves like a DC current source, resistor or a constant power load. This knowledge also improves the accuracy of the initial parameter estimation of the MATLAB script significantly, and can be used to improve the voltage range over which the model is valid.

With all measurements (except the slow triangle) the scope should be set to average at least 100 times.

Step 1) Parameterization: Load Type

Either of the first two measurements can be used for analysis by the MATLAB script. But before we use the script, we need to know a bit about the behavior of the load. This can be done by looking at the measurements of either of the last two bullets above, and looking at how the current behaves as a function of voltage. If neither measurement is available, some common sense needs to be applied, which will be discussed a little further on.

The slow triangle voltage measurement is the easiest to interpret, though low-pass filtering the current as described in Section 9.3, might help to improve the readability of the plot. An example of the CFL bulb triangle measurement is shown in Figure 84. It is not necessary to convert it into a V-I plot, when you know what to look for. Look at the parts of the measurement, where the absolute value of the voltage goes down, or in other words, where voltage moves towards the x-axis of the graph (highlighted). This part of the measurement is not affected by startup effects. The most relevant part of the plot is where the DC voltage is likely to be behind the rectifier, which is usually above 230 V. So you need to look at the behavior of the current in those parts.

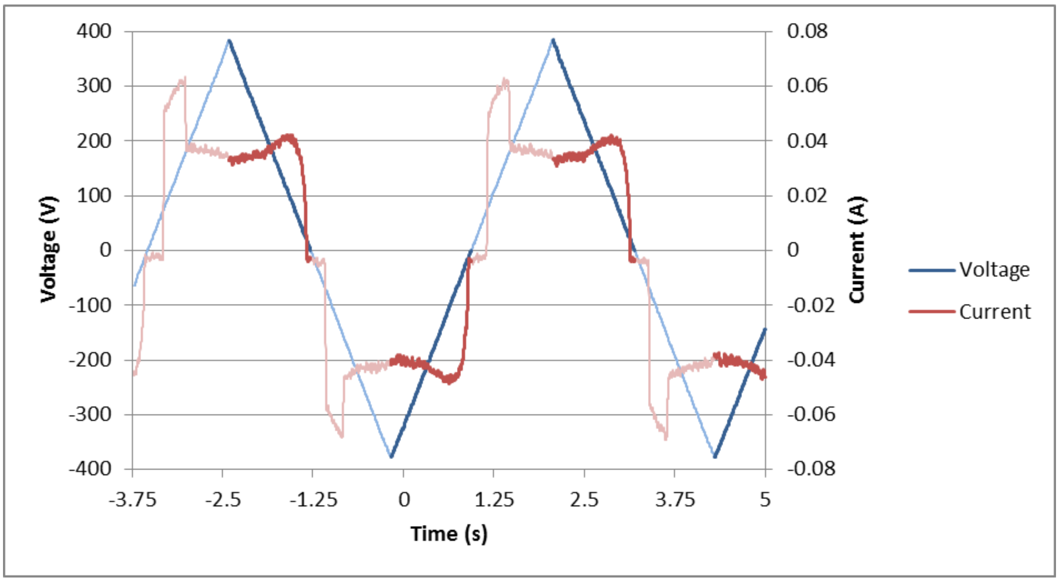

Figure 84: Slow Triangle Measurement (filtered) with DUM with a Rectifier without PFC. (The DUM is the CFL bulb – DC current load in this example, see also Figure 45.) Relevant parts of the plot are highlighted. Same plot as Figure 44.

If you performed measurements with sinusoidal voltage with several RMS values, then you need to plot the average current against the voltage. You don't need to know the value; you just need to know the type of behavior. Get the average current by taking the absolute value, integrating over one period, and then dividing it by the period time (0.02 seconds in case of 50 Hz). Note that the parameterization script in MATLAB does this as well while determining the initial guess values, so it can be used in this step to get the average current.

The question to answer is: how does then the current behave? Is it proportional to the voltage? Then the load is resistive. Is it approximately constant? Then it is a constant current source. Does it appear to go up quadratically as the voltage goes down? Then it is probably a constant power load. In the latter case, if you multiply the current and the voltage to get the power, you should get a horizontal line. You don't need to know the value of the current, resistance or power, you just need to know which *kind* of load most closely resembles the measurement.

If neither measurement is available, then some rules of thumb might help. A CFL light bulb is usually a constant current source, because it is the current that excites the atoms and lights up the fluorescent material. In the case of a modern phone charger (not the old-fashioned kind that contains a linear transformer) it will be a constant power load. This is because while it has no PFC, it is still an SMPS that maintains a constant DC output voltage regardless of input voltage. Off course, the load at its output needs to be constant during the measurements.

Step 2) Parameterization: R_{in}, Capacitor and Load Values

With the information from Step 2, you have everything you need to configure the MATLAB script (see part I in the code, Appendix A. An explanation of how to configure the script is provided in the code, read it carefully). Preferably use the dirty sine voltage measurement for the script. Note that the .csv file that MATLAB reads should *not* contain column headers. Whether the columns are separated by commas, tabs, or semicolons etc., is however not important. The script will generate values for the load, expressed in DC current, resistance and power. Just copy whichever load value is relevant to the SPICE model (in step 4). The model will also generate a value for the capacitor and R_{in}.

The voltage (and in some cases the current) should be filtered before analysis in MATLAB to improve accuracy. This can be done manually in Excel (see Section 9.3), but the same filter is also built-in in the script.

In some cases however the value for R_{in} gives a large error in the clean voltage simulation. In that case, the average can be taken between the R_{in} found with the dirty voltage analysis, and the R_{in} found with the clean voltage analysis.

Step 3) Alternative Parameterization Method in Case Step 2 Fails

In most cases, the MATLAB script should provide accurate values for the model. If however an error occurs that cannot be solved by properly configuring the scripts, or the optimization routine becomes stuck in a local optimum and is generating inaccurate values, there are still alternate ways to perform the parameterization.

The MATLAB script first generates initial guess values for *C* and Load, before starting the optimization routine. If these initial guess values are still generated properly, then these values could be used in the model, as they are usually fairly accurate already. If more accuracy is desired, they can be used as a starting point for the manual parameterization.

If the initial guess parameters are available, the only parameter still to be found is R_{in}. Even if you want to further refine the values for C and load manually, it is recommended to start with R_{in}. Fill in the initial guess parameters in the model (See: Step 4). If R_{in} is completely unknown, 40 Ω is a good value to start with. Run the simulation with the dirty voltage that you captured during measurement. Note that this voltage waveform needs a bit of processing (filtering, averaging) to meet a few requirements, as outlined in Section 8.1.1. As illustrated in Figure 85, the distortion in the current waveform is heavily dependent on R_{in}, so the dirty voltage is the easiest analysis to find R_{in} with. To easily compare the simulation with measurement, follow the steps outlined in Section 9.4.

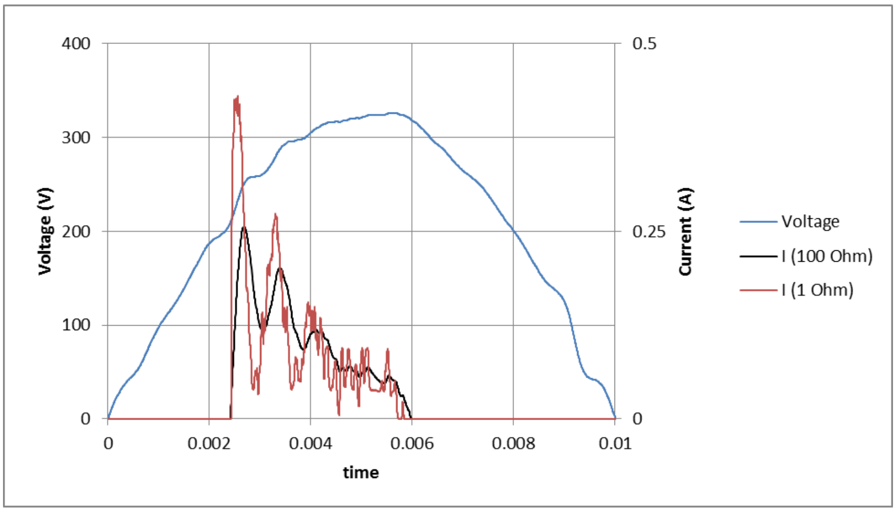

Figure 85: Illustration of how R_{in} influences the current in case of a distorted voltage. Same plot as Figure 30.

To find the values for C and the load from scratch, or to further refine them, it is easiest to use the clean voltage simulation and measurement for the analysis. Refer for the plots in Section 6.1.1, as they will give insight into how varying the various parameters will influence the current waveform. When finding the values for C and load from scratch, you can calculate an initial guess for the load value from the rated power of the DUM. A good place to start with C might be 5 µF.

Step 4) Inserting the Model in SPICE

When all the parameters have been obtained, the model needs to be inserted as a hierarchical block in SPICE. The easiest way to do this is to copy the model files into the working directory of your SPICE project (`Rect_no_PFC.asc` and `Rect_no_PFC.asy`). Then insert the block by opening the *Component* dialog (press <F2>), selecting the working directory at the *Top Directory* drop-down list, and selecting the *Rect_no_PFC* model. The result is illustrated in Figure 86, where the test circuit for the *Rectifier without PFC* model is shown (`test_cirquit_Rect_no_PFC.asc`).

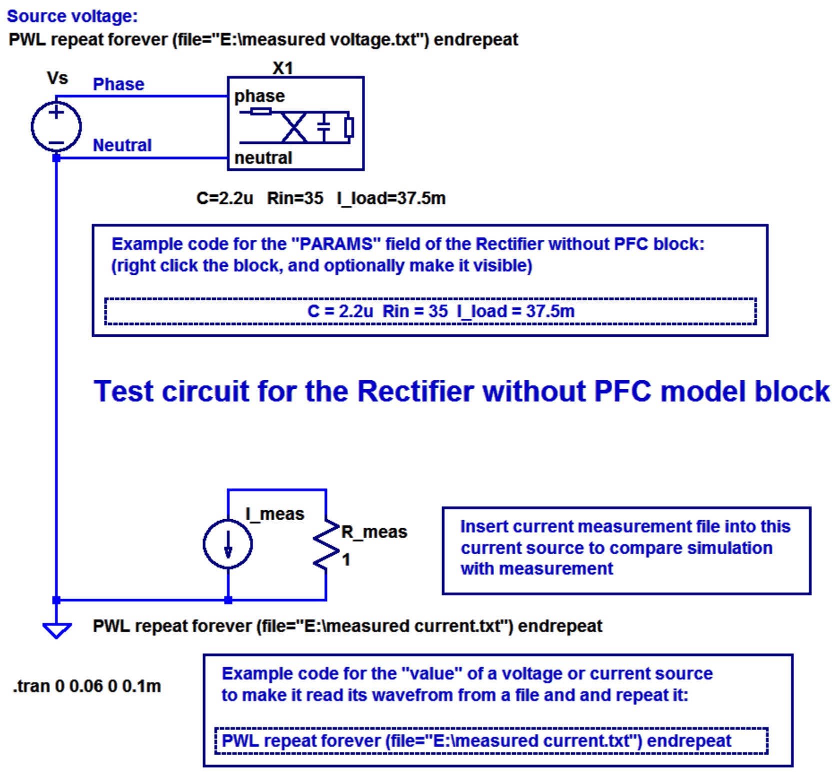

Figure 86: Test circuit for the *Rectifier without PFC* model block

Parameterizing the model is done by passing the parameters to the block. Right-click the block, and in the dialogue that appears, fill in the parameters in the *PARAMS* field. You can optionally make the parameters visible by selecting the check box next to it as is illustrated in Figure 87.

Parameters are typed into the *PARAMS* field simply as '*Parameter=value*', and each parameter should be separated by one or more spaces. Spaces around the '=' sign are allowed as well. Example:

```
C = 2.2u    Rin = 35    I_load = 37.5m
```

All the parameters are listed below.

- `C`: capacitor behind the rectifier (Required. Default: 2.2 µF)
- `Rin`: input resistor (Required. Default: 35 Ω)
- At least one of the following load parameters are required:
  - `P_load`: constant power load (Default: 0 W)
  - `R_load`: resistive load (Default: 10 MΩ)
  - `I_load`: DC current load (Default: 0 A)

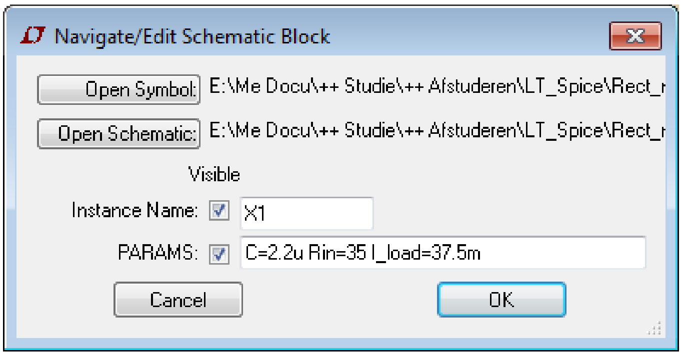

Figure 87: Passing parameters to the *Rectifier without PFC* model

9.2 Usage of the Active PFC Model:

Being more complex than a device without PFC, parameterizing the Active PFC model to a new DUM is more difficult. The process is illustrated with plots from the parameterization of the laptop charger discussed in Section 8.4.2, where also an assessment of the performance of this model for this DUM is made.

The parameterization process for the *Active PFC* model is performed manually. First a scope measurement is done with a clean, undistorted voltage that mimics an ideal power network. This measurement will form the basis for the model, as the prototype current waveform will be extracted from it. After that, other measurements are used that allow the manual estimation of the other relevant parameters.

Make sure that when manipulating measurement data during this procedure in Excel, you always keep a copy of the workbook in Excel format with all the equations. This will save a lot of time as sometimes the accuracy can be improved by doing some additional tweaking of parameters after finishing this manual, and because the prototype current is made in at least two iterations and a mistake is easily made.

First the measurements that are required or useful for parameterizing the model are presented, along with a brief description of what they are used for and what the main requirements for the measurements are. After that, the parameterization procedure is explained step-by-step.

Measurements:

- Required: Clean sine voltage measurement (usually 50 Hz, 230 V_{RMS}, mimicking an ideal power network).
    - The load on secondary side as well as the input voltage amplitude should be close to what will be used in simulation or should otherwise be typical for the DUM.
    - Frequency should be exactly what will be used in simulation.
    - The prototype current will be constructed from this measurement, in steps 1 and 4.
    - In most cases the capacitance in the line filter (C_{line}) can be estimated from this measurement.
- Required: Distorted sine voltage measurement
    - Enables estimation of C_1 (behind the rectifier)
    - If you were unable to estimate the line filter capacitance C_{line} from the clean measurement, then it can be estimated from this measurement as well.

- Optional: Measurements at various RMS voltages or slow triangle voltage.
    - This measurement enables the determination of how the DUM responds to varying input voltages: like a constant power load, constant current load, or constant linear resistance.
    - Note that, given that the control loop in an active PFC/SMPS usually regulates itself to achieve a constant DC voltage, the most likely behavior is that of a constant power load. If this measurement is unavailable, this is the best assumption.

With all measurements (except the slow triangle) the scope should be set to average at least 100 times.

Step 1) Making the Preliminary Prototype Current

First a preliminary prototype current should be made. With this prototype current, values can be estimated for the various components in the SPICE model in step 3, including the capacitors near the rectifier (C_{line} and C_1). After these capacitances are estimated, the final prototype current can be made. In the following it is assumed that *exactly* one period is contained in the measurement file from which the prototype current is to be made:

- Low-pass filter the current, for instance using a moving average filter, as is explained in Section 9.3. In this work, the filter had the amount of taps equivalent to 38 µs (19 taps), though it might depend on the measurement equipment what length of filter is required. Filtering removes the high-frequency switching behavior in which we are not interested, and this should also decrease simulation time, as well as make the following steps easier to perform. The effect of the filter can clearly be seen in Figure 88.

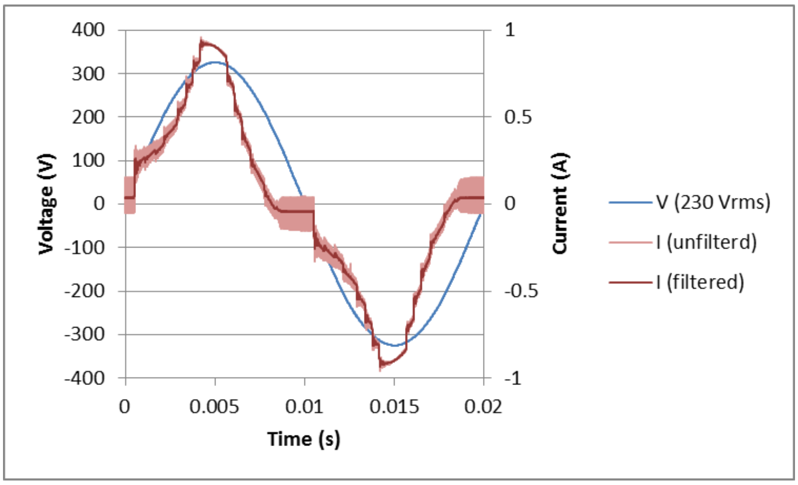

Figure 88: Effect of filtering the current measurement

- Determine a possible DC element in the current *and* voltage, by taking the average over a period, and remove it.
- Remove a time offset if present (make the voltage cross zero exactly between the first and last data point of the measurement file, but make sure any DC component is removed first!)
- Remove the current element due to the line filter capacitance, (represented by C_{line} in the model.) The line filter capacitive current is proportional to the derivative of the input voltage (i.e. it is a cosine, assuming input voltage is a sine) and the amplitude can often be seen from

the offset in the current near where the voltage crosses zero, as is illustrated in Figure 89. If the amplitude can be seen, this is the Excel equation that can be used:

```
=Amplitude*COS(A1*2*PI()*50)
```

Where `Amplitude` is the observed amplitude, `A1` is the cell in the *time* column at the same row, `PI()` simply means π, and 50 Hz is assumed. Keep a column with this equation in it, because you will need to change the prototype current in a similar way again later. Figure 89 plots the above equation together with the filtered measurement.

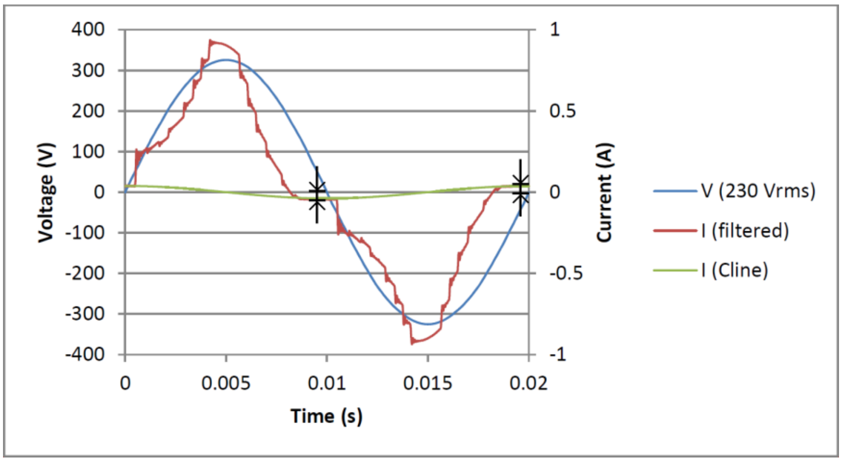

Figure 89: Plot of the line filter current equation (green line)

The resulting value needs to be *subtracted* from the measured current, the result of which is visible in Figure 90 for the first half-wave. Write down the amplitude, because it will be used again later. If this amplitude cannot be seen, then it might well be small and you can initially skip this step.

- Make sure the time axis starts at 0.
- Take the absolute value of the current and cut off the second half of the waveform so the prototype current becomes a single current peak. Note that the last point should be 0.01 seconds *exactly*, in case of 50 Hz. The resulting prototype current is shown in Figure 90.
- Before you prepare the file for SPICE, you should save your work in excel format, because you will have to change the prototype current again later.
- Prepare the Prototype current to be imported into SPICE as is explained in Section 9.4

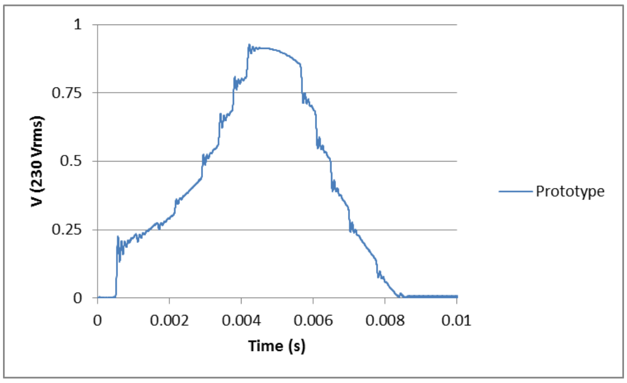

Figure 90: Preliminary prototype current

Step 2) Parameterization: R_{in}, Load and Prototype Current Sources

The value of R_{in} is not very critical. It could be for instance 10 Ω. Making the value higher will suppress noise on the current waveform a little that is due to noise in the voltage. However, a high value for R_{in} will cause the start-up effects of the model to last longer. Increasing R_{in} will also cause a larger voltage drop across it, causing in turn the control loop of the model to compensate by drawing more current. Therefore it is recommended to choose R_{in} to be below 20 Ω, and proceed to tune the load and prototype current sources after choosing R_{in}.

After the prototype current has been made and R_{in} is chosen, the load and the prototype current sources need to be looked at. If you have done the triangle voltage or measurements at several RMS voltages, then you can determine the type of load behavior in the same way as was explained in Step 1, for the *rectifier without PFC* model (Section 9.1). It should be noted however, that a SMPS generally generates a DC voltage that is regulated to maintain the same value, regardless of input voltage or load. This means, that it is reasonable to expect an SMPS to always behave approximately as load that dissipates a constant power, regardless of input voltage, (assuming of course, a constant load.) Therefore this is assumed in the rest of this text.

As explained in Section 0, part of the current should go to the buffer capacitor C2 and part should flow directly to the negative DC line. Whether this ratio needs to be explicitly determined depends on the kind of DUM and what you need the model for.

- If you are not planning to vary the load during the simulations or the load value is fixed or unknown, it is enough to simply adjust the load value so that the magnitude of the current that the model draws from the mains matches with the measurement. Run the simulation with the same circumstances (clean sine, same RMS voltage) under which the prototype current waveform was measured. Refer to Step 5 on how to do that. Then adjust the load value until the best possible match is obtained. (See also Section 9.4.)
- If the Power parameter (`P_load`) should reflect reality then the ratio between the two current sources should be determined. Do note that, even when the current sources are tuned, the power parameter will only be a rough approximation, because the efficiency of an SMPS is generally not constant when the load varies. Run the simulation with the same circumstances (clean sine, with the same load and RMS voltage) under which the prototype current waveform was measured. Refer to Step 5 on how to do that. Then, tweak the ratio until the simulated current amplitude matches with the measurement. (See also Section 9.4.) It is desirable that the sum of the amplification of both voltage controlled current sources is unity, so that here is no hidden amplification in this part of the model. So if the horizontal source has amplification A_{hor}, then the vertical source should have $A_{vert} = 1 - A_{hor}$, where $0 < A_{hor} < 1$. Note that in the model, only A_{hor} needs to be specified.

Note that a perfect match between the simulated and measured current cannot be obtained yet at this stage, because the values of the capacitors are still undetermined. Section 9.4 explains how a measured waveform can be imported into SPICE so that it can easily be compared with simulation.

Step 3) Parameterization: Capacitors C_{line} and C_1

You can estimate the value of the line filter capacitance C_{line} by the amplitude of the capacitive current determined in Step 1. If this amplitude was not observable, another solution is provided further down in this section. Calculating capacitance from a measured amplitude is done as follows. Starting from the constitutive relation of the capacitor:

$$\begin{aligned}
i(t) &= C\frac{\mathrm{d}}{\mathrm{d}t}v(t) \\
&= C\frac{\mathrm{d}}{\mathrm{d}t}\{230\sqrt{2}\sin(2\pi 50\, t)\} \\
&= C \cdot 2\pi 50 \cdot 230\sqrt{2}\cos(2\pi 50\, t) \\
&= \hat{I}\cos(2\pi 50\, t)
\end{aligned}$$

Where $v(t)$ is the input voltage and $\hat{I}$ is the observed amplitude. A 50 Hz, 230 V_{RMS} sine voltage is assumed. The cosines cancel, and rearranging we find the relationship between $\hat{I}$ and C:

$$\hat{I} = C \cdot 2\pi 50 \cdot 230\sqrt{2}$$

$$C = \frac{\hat{I}}{2\pi 50 \cdot 230\sqrt{2}}$$

When C_{line} is known, put its value into the model. C_1 Can then be estimated as follows. Run the simulation with the distorted input voltage waveform, and compare this to measurement. Then simply find the value of C_1 for which you get the best match in the distortion of the current. The simulation accuracy is still poor, but the goal at this stage is to match the amplitude *of the distortions* away from the voltage zero crossings, as is illustrated by the highlighted detail in the Figure 91.

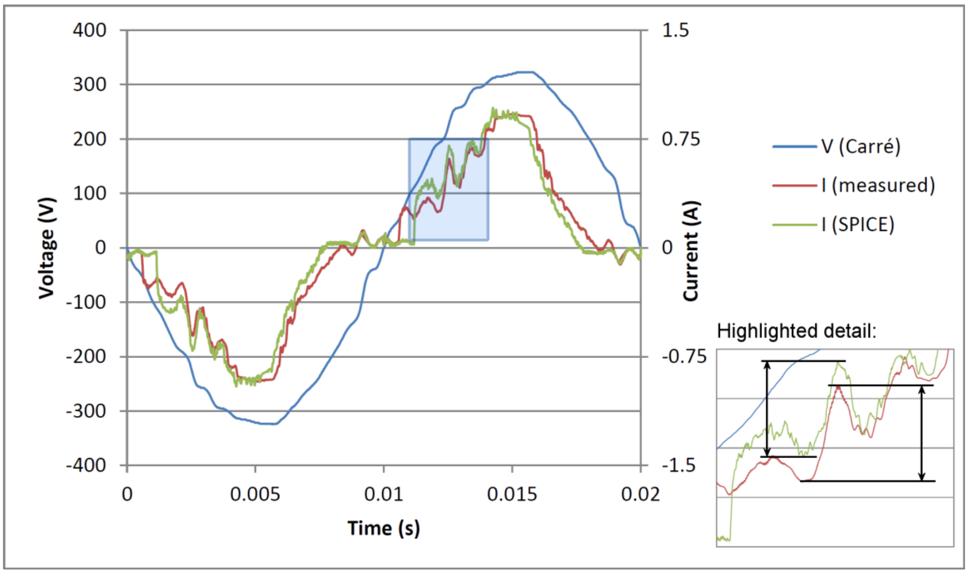

Figure 91: Estimating C_1 by looking at the current distortion

If the line filter capacitance is not known from the clean measurement, proceed as follows:

- Keep the line filter capacitance C_{line} zero, and find a value for C_1 where the simulated current distortion best matches the measurement far away from the zero crossings as illustrated in Figure 91.

- Move capacitance from the C_1 to C_{line}, so that the total capacitance in the model remains constant, until you get the best match near the zero crossings as possible.
- If deemed necessary, calculate the capacitive current in the line filter, and compensate the prototype current for it as explained in Step 1. This should improve the simulation accuracy near the zero crossings.

Step 4) Making the Final Prototype Current

As explained in Section 0, the prototype current waveform needs to be compensated for the capacitor current in C_1. To find the amplitude of the current that you need to compensate for, you can either look in the SPICE simulation at the current magnitude that goes in and out of the C_1 capacitor (clean voltage simulation), or calculate the amplitude using the equation from Step 3.

This current magnitude again goes into the equation:

```
=Amplitude*COS(A1*2*PI()*50)
```

But this time use a new column for the equation, and subtract this column from the preliminary prototype current that you have made before. This means that part of the prototype current will now be negative, and that when the prototype current waveform is repeated there will be a step in the current, because the prototype starts and ends on a different current value. This however is as it should be, because the C_1 capacitor current displays a similar step, when the derivative of V_{pulse} changes sign at 0 volt. The result is shown in Figure 92.

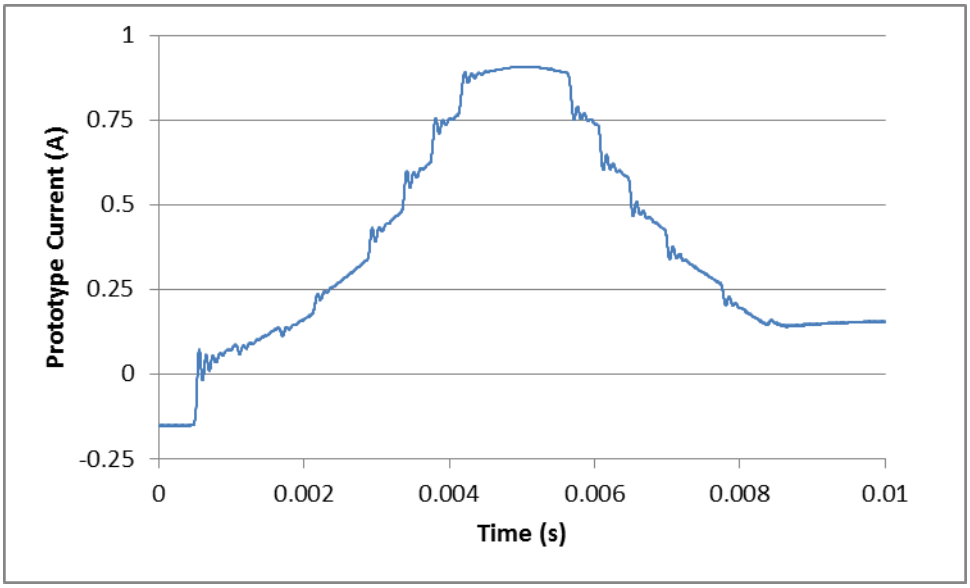

Figure 92: Final prototype current: half-wave does not start and end on the same value

Step 5) Inserting the Model in SPICE

Now that you have the prototype current ready and all the parameters, the model needs to be inserted as a hierarchical block in SPICE. The easiest way to do this is to copy the model files into the working directory of your SPICE project (`Active_PFC.asc` and `Active_PFC.asy`), as well as the prototype current file. Then insert the block by opening the *Component* dialog (press <F2>), selecting the working directory at the *Top Directory* drop-down list, and selecting the Active_PFC model. Attach a current source to the *Proto_out* and *Proto_in* pins of the model, and make it repeat the prototype current as explained in Section 9.4. This is illustrated in Figure 93, where the test circuit for the *Active PFC* model is shown (`test_circuit_Active_PFC.asc`). Note that the current should flow from `Proto_out` to `Proto_in`.

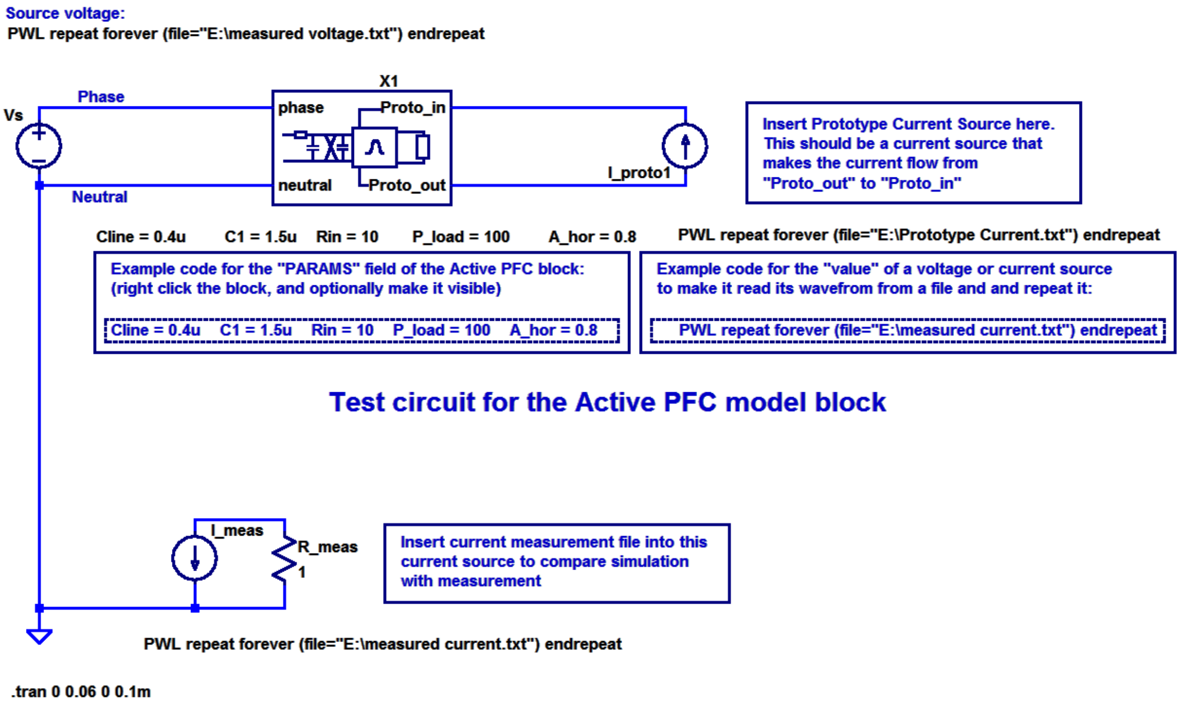

Figure 93: Test circuit for the *Active PFC* model block

Parameterizing the model is done by passing the parameters to the block. Right-click the block, and in the dialogue that appears, fill in the parameters in the *PARAMS* field. You can optionally make the parameters visible by selecting the check box next to it as is illustrated in Figure 94.

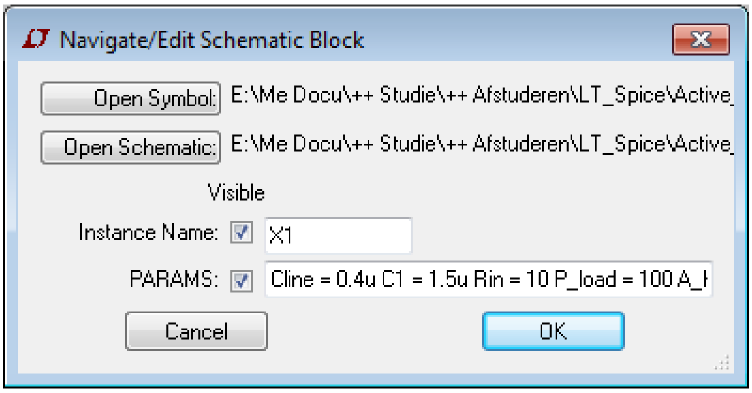

Figure 94: Passing parameters to the *Active PFC* model

Parameters are typed into the PARAMS field simply as '*Parameter=value*', and each parameter should be separated by one or more spaces. Spaces around the '=' sign are allowed as well. Example:

```
Cline = 0.4u    C1 = 1.5u    Rin = 10    P_load = 100    A_hor = 0.8
```

All the available parameters are listed below, categorized as ‘required’, ‘optional’ and ‘normally not used’.

Required parameters:

- `Cline`: line filter capacitance (Default: 0.75 μF)
- `C1`: capacitor behind the rectifier (Default: 0.75 μF)
- `Rin`: input resistor (Default: 10 Ω)
- At least one of the following load parameters:
    - `P_load`: constant power load (Default: 0 W)
    - `R_load`: resistive load (Default: 10 MΩ)
    - `I_load`: DC current load (Default: 0 A)

Optional parameter:

- `A_hor`, amplification factor for the horizontal prototype current source (Default: 0.5)

Parameters not normally used:
These parameters should in most cases be omitted so they stay at their default value:

- `A_vert`, amplification factor for the vertical prototype current source (The default value is `1 – A_hor`, so only `A_hor` needs to be specified)
- `C_lpf, R_lfp`: define the RC time of the low-pass filter in the control loop. (Default: 1 μF and 10 kΩ, respectively)
- `C_maxhold, R_maxhold`: define the RC time of the max-hold circuit. (Default: 1 μF and 10 MΩ, respectively)
- `A_ref`: Amplification for the reference voltage V_{REF}. V_{REF} will be `A_ref` times the amplitude of the input voltage. (Default: 1.1)
- `Control_a, Control_b`: these are the factors a and b respectively in the equation $A_{SC} = a + b\ V_{ERR}$ that the prototype current is scaled with in the control loop (see Section 0). (Default: a = 1 and b = 0.05)
- `C2`: Buffer capacitor behind the current sources. (Default: 120 μF)

9.3 Applying a Moving Average Filter in Excel

This section explains how a signal can be filtered by a moving average filter in Excel. We will assume that column A has the time, and column B is the data to be filtered, and column C is the first column that is empty. Furthermore in this text it is assumed the columns have no headers so row 1 contains data. The filter will be of length N, which is an odd integer. Before you begin, it is advisable to make a backup of your file, so you don’t lose your original data if you do something wrong.

The filter is implemented in column C. Select cell number (N + 1)/2 in column C. (e.g. in case of N = 19, select cell C10.) There you type the equation:

```
=AVERAGE(B1:B19)
```

Note that the cell you selected is in the row in the middle of the averaging range, which avoids causing a delay in the filtered data. Now you can double click the bottom right corner of the selected cell, to fill the column down, resulting in a column with the filtered data. However, this leaves the first (N - 1)/2 points unfiltered (the first 9 points in case of N = 19). However, if the measurement data exactly covers one or an integer multiple of periods, then there is a way to filter these too. Just copy the first N data points in column B, and attach it to the end of column B. Then double click the bottom-left corner of the cell with the averaging equation, so the extended data is filtered as well. Then copy the first (N – 1)/2 of the *extended* filtered data points (= 9 points if N = 19), and paste them, *values only*, at C1, to fill the gap.

To prepare the file for SPICE, copy column C, and paste it, again *values only*, to column B, to replace the original data. Then delete column C, as well as any extensions at the bottom of the columns that you might have made. Then follow the steps outlined in Section 9.4, below.

9.4 Import a Measured Signal into SPICE

To make use of a prototype current, or to compare a measured response with the SPICE response, you need to import a measured waveform into SPICE and plot it. In this section it is explained how the file with measurement data is properly prepared in Excel to be read by LTspice. Basic knowledge of how to use Microsoft Excel and LTspice is assumed.

- Before you prepare the file for SPICE, you should save your work in Excel format, because some information will be lost in this process.
- Delete everything in the Excel sheet that you do not need, until it is reduced to two columns:
  - Column A containing the time values and
  - Column B containing the signal (voltage or current) of interest
- Also delete the column headers
- Make sure the time column starts at 0, and ends at T (the period time), and not T-ΔT, where ΔT is the time step in the measurement data. This is because SPICE does not assume a constant time step in the input file, so when it repeats the waveform it will put the first and the last data point on top of each other, taking the value of the last data point in the file, and hence ignoring the first data point of the file upon repeat. This means that if the last data point is in the file is T-ΔT, the measured plot will move out of synch with the rest of the simulation by ΔT every period, which is likely to become significant after only a few periods. If the last point already is T-ΔT, then this can be corrected by simply copying the first data point and paste it at the end and giving it time stamp T.
- Both columns should have the same length
- Format the two remaining columns as ‘scientific’ and make sure they contain enough accuracy in the data, *as displayed on screen*, because that is how it will be saved. This means you may have to increase the width of the columns.
- Then save to the “Text (MS-DOS) (*.txt)” file format.

Now that we have the file, it needs to be imported in SPICE, and in case of a periodic waveform we need to get SPICE to repeat the waveform. This is done as follows. Take a voltage or current source. In the field where you would normally put the DC value or waveform parameters, you put the following line:

`PWL repeat forever (file="E:\Measurement File.txt") endrepeat`

Where `E:\Measurement File.txt` should be replaced by the proper file name. This can be the complete path as shown in the example, or only the file name, if the file is in the same directory as the SPICE project files. In the case of a current source you will need a resistor in parallel to have the current go somewhere, as shown in Figure 95. Hint: in Windows Explorer (Vista/7) when you hold down <Shift> while right-clicking a file, the option “Copy as Path” will appear in the in the pop-up menu, which lets you copy the path and filename as text, so you can paste it in the SPICE field.

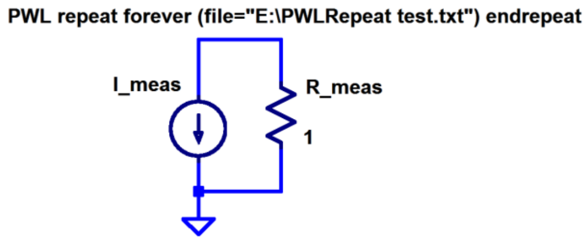

Figure 95: How to plot a measured waveform in SPICE

10 Conclusions

In this chapter the results and conclusions drawn from this project are presented, for both the modeling efforts for the rectifier without PFC load and the active PFC. In addition, a brief look into future work is taken, that still needs to be performed in order to achieve the goal of predicting and preventing power quality issues on a power network through simulation.

10.1 Rectifier without PFC model

The gray-box model for the rectifier without PFC shows very good agreement with the measured response of the DUM, and the model is computationally light. The model can be parameterized using measurements performed during steady state operation of the DUM. These measurements can then be analyzed automatically by a MATLAB script, producing results with good accuracy. The script can even produce a decent result when the measurement is performed on site by connecting the DUM to a wall outlet, though the output impedance of the outlet should not be too high. Measurements obtained through a lab setup do however provide a more reliable result. Good accuracy can also be obtained through manual parameterization, though this is more labor intensive.

Dr.ir. I. Stievano of Turin has attempted to make a black-box model of the Rectifier without PFC as well. The model he came up with was essentially the same as the gray-box model, because every component in that model represents an essential equation that cannot be replaced without changing an essential part of the dynamic behavior of the model. Only the rectifier was implemented differently, which turned out to be a big advantage, as it made the model much more numerically stable in LTspice. A variation of the rectifier has therefore also been used in both Gray-box models.

10.2 Active PFC model

The Gray-box model for the Active PFC is also accurate, however due to the complexity of the Active PFC, there are more restrictions to its applicability than with the *Rectifier without PFC* model. The *Active PFC* model is computationally light, though not nearly as light as the *Rectifier without PFC* model.

The primary restriction of the *Active* PFC model is that the more the simulated RMS voltage and load conditions differ from those of the prototype current measurement, the less accurate the model becomes. This is because the current waveform will change shape somewhat in the actual DUM, while in the model it merely scales. To mitigate the problem, multiple prototype currents under different RMS voltage and load conditions can be made, and the prototype current can then be selected that most closely matches the expected simulation conditions. It should be noted that even under inaccurate conditions, the model still behaves realistically, just not accurate for that specific DUM. This does however mean that it is important to use a variety of models of different DUMs to get a realistic simulation of a complete power network.

Another restriction is that the net frequency needs to be fixed to the same value as is assumed in the prototype current. However, for the simulations that these models are designed for, this is not expected to be a problem, since the power quality is not expected to change significantly if the net frequency drifts with one or two Hertz. So for the purpose of the simulation, fixing the frequency to an exact value is not a problem.

Because of the complexity of the DUM, parameterization has to be performed manually. A specific step-by-step method for this has been developed. In the case of the *Active PFC* model, a clean measurement is required to make the prototype current waveform out of, so parameterizing it through on-site measurements is not possible.

10.3 Future Work

The models developed in this work only model the loads themselves. They do not model the power network, or the impedance of the wall outlet. In order to make meaningful predictions of power quality based on simulations, the rest of the power network needs to be modeled as well. This includes the source, which could be for instance a 10 kV transformer or an emergency power generator.

It should also be investigated if a group of the same loads that are located close together can be modeled by a single load that simply has its current multiplied by the number of loads in the group. A group of loads could be for instance all the CFL bulbs that light a single room. Whether or not this can be done, will also depend on the properties of the network that connects these loads. So to answer this question, the network needs to be characterized and modeled first. If this grouping of loads is possible, it would be convenient because it would allow to model and simulate a much larger power network using the same computational power.

References

[1] Basu S.; Bollen, M.H.J.; M.Undeland, T.M.; , “PFC Strategies in light of EN 61000-3-2”, *EPE PEMC 2004 Conference*, 1-3 Sept. 2004, Riga, Latvia

[2] Timens, R.B.; Buesink, F.J.K.; Cuk, V.; Cobben, J.F.G.; Kling, W.L.; Leferink, F.B.J.; , "High harmonic distortion in a new building due to a multitude of electronic equipment," *Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on* , vol., no., pp.393-398, 14-19 Aug. 2011

[3] Timens, R.B.; Buesink, F.J.K.; Cuk, V.; Cobben, J.F.G.; Kling, W.L.; Leferink, F.B.J.; , "Large number of small nonlinear power consumers causing power quality problems," *EMC Europe 2011 York* , vol., no., pp.592-596, 26-30 Sept. 2011

[4] Stievano, I.S.; Maio, I.A.; Canavero, F.G.;, “Accurate and Efficient Parametric Macromodeling of IC Drivers via Sigmoidal Basis Functions” *Proc. of 7th IEEE Workshop on Signal Propagation on Interconnects*, pp 57-60, 2003

[5] Stievano, I.S.; Canavero, F.G.; Maio, I.A.; , "Behavioural macromodels of digital IC receivers for analogue-mixed signal simulations," *Electronics Letters* , vol.41, no.7, pp. 396- 397, 31 March 2005, doi: 10.1049/el:20058186

[6] Stievano, I.S.; Grivet-Talocia, S.; Maio, I.A.; Canavero, F.G.; , "Linear and nonlinear macromodels for power/signal integrity," *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, vol., no., pp. 5754- 5757 Vol. 6, 23-26 May 2005, doi: 10.1109/ISCAS.2005.1465945

[7] Stievano, I.S.; Maio, I.A.; Canavero, F.G.; , "Mπlog, macromodeling via parametric identification of logic gates," *Advanced Packaging, IEEE Transactions on* , vol.27, no.1, pp. 15- 23, Feb. 2004, doi: 10.1109/TADVP.2004.825475

[8] Stievano, I.S.; Maio, I.A.; Canavero, F.G.; , "Parametric macromodels of digital I/O ports," *Advanced Packaging, IEEE Transactions on* , vol.25, no.2, pp. 255- 264, May 2002, doi: 10.1109/TADVP.2002.803260

[9] Kahoul, R.; Azzouz, Y.; Marchal, P.; Mazari, B.; , "New Behavioral Modeling for DC Motor Armatures Applied to Automotive EMC Characterization," *Electromagnetic Compatibility, IEEE Transactions on* , vol.52, no.4, pp.888-901, Nov. 2010

[10] Bishnoi, H.; Baisden, A.C.; Mattavelli, P.; Boroyevich, D.; , "Analysis of EMI Terminal Modeling of Switched Power Converters," *Power Electronics, IEEE Transactions on* , vol.27, no.9, pp.3924-3933, Sept. 2012

[11] Crebier, J.-C.; Ferrieux, J.-P.; , "PFC full bridge rectifiers EMI modeling and analysis-common mode disturbance reduction," *Power Electronics, IEEE Transactions on* , vol.19, no.2, pp. 378- 387, March 2004, doi: 10.1109/TPEL.2003.823190

[12] Paul, C.R., “Introduction to Electromagnetic Compatibility”, 2d ed. New Jersy: John Wiley & Sons, Inc., 2006, pp. 67-73.

[13] Ross, B., “Practical Issues with IBIS Models”, *website article*, Interconnectix Unit of Mentor Graphics Corporation, URL: http://www.eda.org/ibis/articles/pcbeas97.htm , Accessed April 24, 2013

[14] Mercedes Casamayor, M.; , “A First Approach to IBIS Models:What They Are and How They Are Generated”, *Application note AN-715,* Analog Devices, URL: www.analog.com

[15] Mutnury, B.; Swaminathan, M.; Libous, J.; , "Macro-modeling of nonlinear I/O drivers using spline functions and finite time difference approximation," *Electrical Performance of Electronic Packaging, 2003* , vol., no., pp.273-276, 27-29 Oct. 2003, doi: 10.1109/EPEP.2003.1250048

[16] Sjöberg, J.; Zhang, Q.; Ljung, L.; Benveniste, A.; Delyon, B.; Glorennec, P.Y.; Hjalmarsson, H.; Juditsky, A.; , “Nonlinear black-box modeling in system identification: a unified overview,” *Automatica*, Volume 31, Issue 12, December 1995, Pages 1691-1724, ISSN 0005-1098, 10.1016/0005-1098(95)00120-8.

[17] Verspecht, J.; Schreurs, D.; Barel, A.; Nauwelaers, B.; , "Black-box modelling of hard nonlinear behavior in the frequency domain," *Microwave Symposium Digest, 1996., IEEE MTT-S International* , vol.3, no., pp.1735-1738 vol.3, 17-21 Jun 1996, doi: 10.1109/MWSYM.1996.512277

[18] Maksimovic, D.; Stankovic, A.M.; Thottuvelil, V.J.; Verghese, G.C.; , "Modeling and simulation of power electronic converters," *Proceedings of the IEEE* , vol.89, no.6, pp.898-912, Jun 2001, doi: 10.1109/5.931486

[19] R. W. Erickson, “Fundamentals of Power Electronics - accompanying slides chapter 6”, New York: Chapman and Hall, May 1997, ISBN 0-412-08541-0
URL: http://ecee.colorado.edu/copec/book/slides/Ch6slides.pdf , Accessed April 24, 2013

Appendix A: MATLAB Script to Parameterize CFL Bulb Model

In this appendix the MATLAB script is presented that analyses a measurement (or simulation) and estimates the parameters for the gray-box model presented in Section 5.4, which models the *Rectifier without PFC* load category. Some key features of the script are highlighted and an example output is given with some comments, and the structure and general operation of the optimization routine is presented.

This appendix accompanies Section 6.1.3

Features

The MATLAB script the estimates the parameters for the *Rectifier without PFC* model in two phases. In the first phase, estimates are made for the capacitor and load, which will function as initial guess parameters for the second phase, the optimization routine. This first phase relies on the fundamental equations for the various components inside the model, and the second phase runs the simulation using the measured voltage and compares the result with measurement. The script is therefore capable of analyzing measurements performed with a distorted voltage, which even results in a more accurate value for R_{in} than when a clean measurement is used. Just as long as the voltage waveform is available and individual the current peaks are not cut into two parts so that they are detected as separate peaks, the script should give an accurate result.

As already mentioned, the second phase is an optimization routine. The model has been implemented in MATLAB by Dr.Ir. Stievano. The optimization routine uses that implementation to compare simulation with measurement. The optimization routine varies the values for R_{in}, C and R_{load} and runs the simulation to find the best possible fit. To avoid local optima, C and R_{load} are always varied together, while either keeping their product constant (R_{load} x C) or their ratio constant (R_{load} / C). As can be seen from Figure 27 in Section 6.1.1, keeping (R_{load} x C) constant changes only the height of the current peaks, while keeping their timing exactly the same. By contrast, Figure 28 shows that keeping (R_{load} / C) constant has a very large effect on the timing.

The MATLAB script can cope with noisy data, however filtering the voltage sometimes produces a more accurate result. For the estimation of the initial guess parameters, the biggest challenge with noise is that the script needs to find the start and stop times of the current peaks with the greatest possible accuracy. Excessive noise will influence the accuracy of finding these start and stop times of the peaks, which in turn influences the initial guess values. To minimize this problem, the script first roughly finds the areas where the current is zero, using $I_{measured}$ < `Ith`, (these areas are marked in black In Figure 97, on the right). The average of the current in these areas is the DC-current offset, which is a measurement error. The offset is removed from the measurement data, and a new estimate is made of the smallest `Ith` that will not result in current noise being incorrectly interpreted as current peaks, while still missing as little of the actual current peaks as possible.

Another feature is that the script makes no assumptions about the time steps in the input data. This is because when curves are imported from SPICE, the time steps between data points vary a great deal. The maximum time step should however be set to a small value in the transient simulation command (e.g. to 0.01 ms), otherwise the current peaks will not start at a realistic time.

Output of the Script

The primary output of the MATLAB script are the values that can be used to parameterize the gray-box model. First the results of the initial guess phase are displayed in the command window. These are:

- `Rin`: Input resistor value
- `C`: Value of the buffer capacitor
- `I_load`: DC current though the load, in case the load is modeled as a DC current source
- `R_load`: Estimation of the load resistor, in case the load is modeled as a resistor
- `P_load`: Estimation of the power dissipated in the load, in case the load is modeled as a constant power load
- `Idc_offset`: The DC offset in the current measurement (could be interesting for various purposes)

Figure 96 shows what the output looks like.

```
Frist phase: Initial guess estimation of C and load
===================================================

Idc_offset =
   2.2557e-04
I_load =
    0.0409
R_load =
   7.3462e+03
P_load =
   12.2679
C =
   9.8161e-06
```

Figure 96: Output in the MATLAB Command Window of the initial guess routine (First phase)

In the first part of the script, a couple of settings need to be set so that the measurement is analyzed correctly. What they are and how to set them is explained in the code, so read carefully. The graphs produced by the script help the user verify that these settings are all filled in correctly, and give clues as to what the problem is when they are not. Usually, incorrect settings result in a MATLAB error that halts execution, but the graph giving a clue as to what caused the error should already be shown when the error occurs.

In Figure 97 the graphs that the script makes in the first phase are shown. The measurement used in this figure is from the DC adapter from Section 8.4.1, with the Carré voltage. This is how the figures are supposed to look when the script runs successfully. The graph on the left is to see if,

1) the script starts analyzing data when the CFL bulb is already in steady state and
2) if at the left most point of the graph (y = 0), both voltage and current are approximately zero. If either isn't the case, then some initial data needs to be discarded. The variable `nsteady` denotes the first data point index the script will analyze, so `nsteady` will need to have a value > 1 if data needs to be discarded. (see x-axis in the plot)

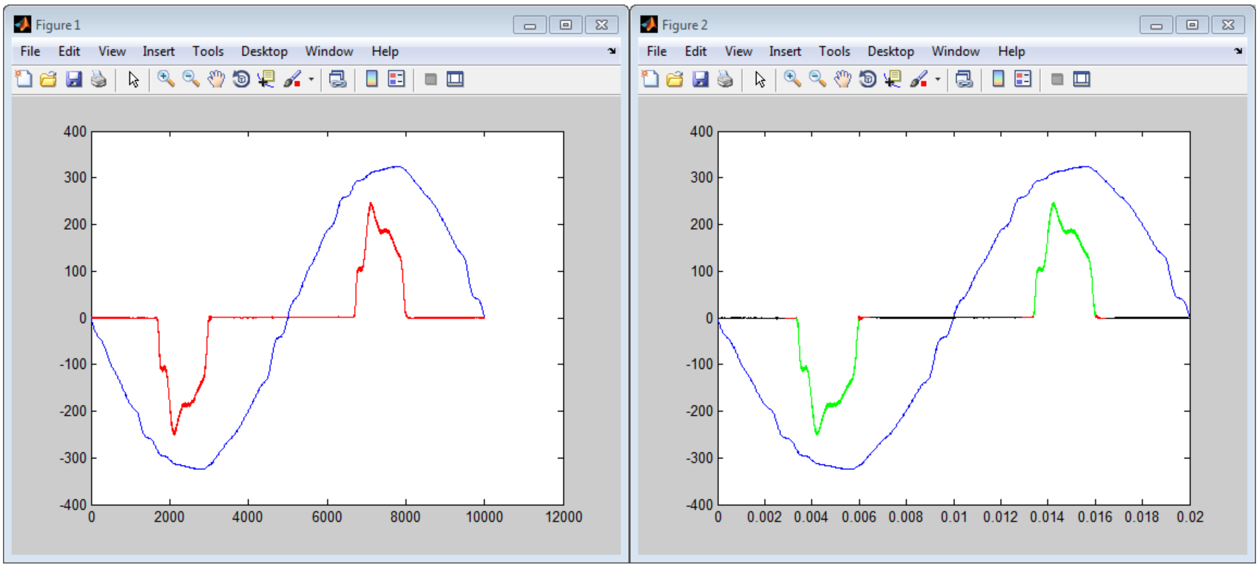

Figure 97: Graphs generated by the initial guess routine in MATLAB

The graph on the right shows how the data is used. The current peaks are supposed to be marked in green, and the areas of zero current are supposed to be marked in black, as is shown correctly in the figure. If anything is not correct in this graph, chances are you need to increase `Tnoise` or, if that fails, `Ith`. These variables are noise tolerances in the time and current domain, respectively.

The second phase of the script also displays its results in the output window. The output is shown in Figure 98. A large chunk of the output has been removed for brevity. The most important output is a complete set of model parameters including a value for R_{in}. These optimized parameters are found at the bottom line.

```
Second phase: Optimization routine
==================================

Starting search for optimum...
Initial guess: Rin = 40, C = 9.8161e-06, R_load = 7346.1958
Rin Optimization (LsQ), initial Error value 0.039619, Adjustment factor 0.4
Rin Optimization (LsQ), Iteration 1, Error value 0.012284, Adjustment factor 0.4, local max 0
Rin Optimization (LsQ), Iteration 2, Error value 0.0034141, Adjustment factor 0.4, local max 0
Rin Optimization (LsQ), Iteration 3, Error value 0.0034141, Adjustment factor 0.2, local max 0
Rin Optimization (LsQ), Iteration 4, Error value 0.0034141, Adjustment factor 0.1, local max 0

[...~]

RC Optimization (LsQ), Iteration 1, Error value 0.0011745, Adjustment factor 0.003125, local max
0

[...~]

R/C Optimization (LsQ), Iteration 1, Error value 0.0011745, Adjustment factor 0.003125, local
max 0

[...~]

Rin Optimization (LsQ), Iteration 1, Error value 0.0011745, Adjustment factor 0.01, local max 0
Rin Optimization (LsQ), Iteration 2, Error value 0.0011745, Adjustment factor 0.005, local max 0
Result so far: Rin = 74.475, C = 1.051e-05, R_load = 7486.2029, No_change? -1- last Acc:0.01
Final result:
Rin = 74.475, C = 1.051e-05, R_load = 7486.2029, I_load = 0.040218, P_load = 12.1195
>>
```

Figure 98: Output in the MATLAB Command Window of the optimization routine (Second phase)

The information in the output lines are mostly for debugging purposes. The most important information is:

- `XXX Optimization (YYY)`: XXX denotes the parameters being varied and optimized, and YYY denotes the error criterion:
  - `LsQ`: Least squares
  - `time`: timing of the current peaks
  - `Irms`: RMS current
- `Iteration 1`: counts how many times the parameters are varied during the optimization
- `Error value 0.0011745`: currently best error value (smaller is better).
- `Adjustment factor XXX`: the parameters are varied by dividing or multiplying the parameter value with a factor (1 + XXX).
- `local max X`: if X = 1 then varying the parameter either way is an improvement. When this occurs, there is a chance that the optimization routine ends in a local optimum.
- `No_change? -X-`: If X = 1 then in the last optimization attempt, the no better value for the parameter was found.
- `last Acc: 0.01`: the last value of the adjustment factor with which was searched.

The optimization script also produces several plots in two windows, as is illustrated in Figure 99. In each window, the top plot shows the voltages in the simulation, and the bottom plot shows the simulated and measured current. The red part of the measured current is the area of the plot that is analyzed and that the optimization routine tries to match with the simulated current. The first window (left) shows the simulation with the initial guess parameters, while the second window (right) shows the simulation using the optimized parameters from the final result.

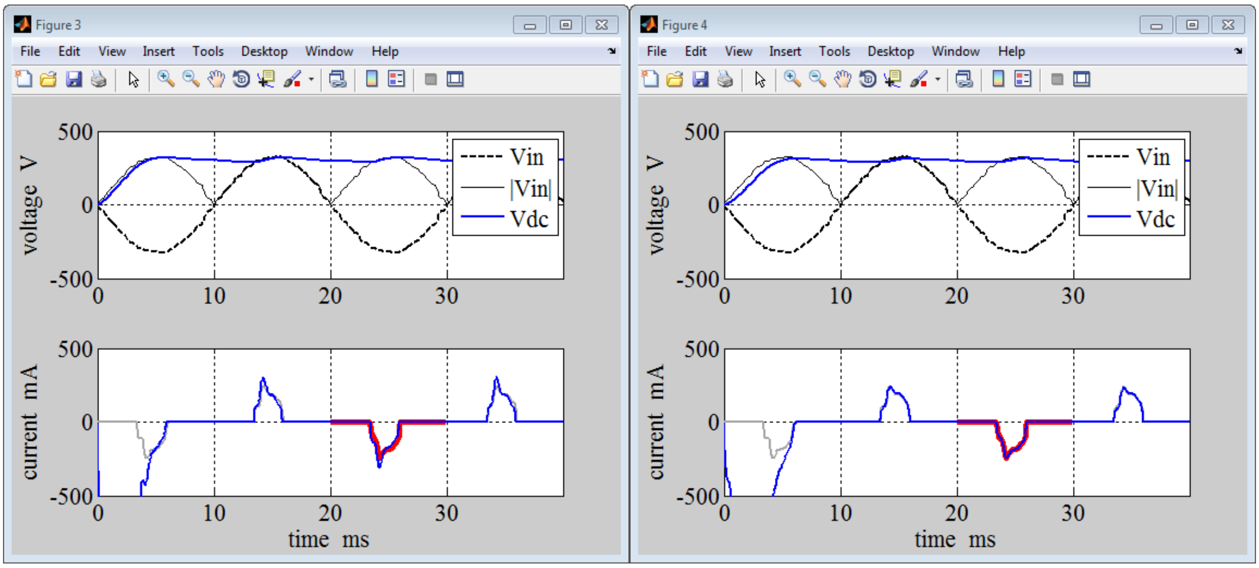

Figure 99: Graphs generated by the optimization routine in MATLAB

Implementation

The initial guess phase is implemented in a single .m file (`runme.m`), but the second phase, the optimization routine, consists of a hierarchy of .m files. Figure 100 gives an overview of the .m files and a brief description of their purpose and what they do.

`Search_optimum.m` coordinates the optimization routine. It controls which parameters are to be optimized in what order, and to which error criterion. The way it does this is illustrated in the figure. Note that 'R' in the optimization routine means R_{load}. It starts with optimizing R_{in}, as there is no initial guess for this parameter at the start. Then it varies RC and R/C to optimize the timing and RMS current, respectively, and then repeats the R_{in} optimization again. After that it repeats a sequence of RC, R/C, R_{in}, until none of the parameters change anymore. To avoid an endless loop, the sequence is repeated no more than 5 times. This routine also controls how coarse the search for the optimal parameters should be.

The .m files in the "*Vary parameter to find optimum"* column in Figure 100, perform a specific optimization to a specific error criterion. They take the parameters passed to them from `search_optimum.m` as a starting point, and vary their specific parameters to see if it results in a smaller error. The parameters to be varied and the criteria are:

- R_{in}, optimizing for least square current error (`Optim_Rin_LsQ.m`)
- RC, optimizing for least square current error (`Optim_RtimesC_LsQ.m`)
- R/C, optimizing for least square current error (`Optim_RoverC_LsQ.m`)
- RC, optimizing for best match in current peak timing (`Optim_RtimesC_time.m`)
- R/C, optimizing for best match in RMS current (`Optim_RoverC_Irms.m`)

The .m files in the "*Caculate error variable to be minimized"* column run the simulation by calling `odet23t(.)`,compare the result with the measurement data and calculate the error. There are three different error criteria:

- The squared current error signal (`Calc_Err_LsQ.m`)
- The number of samples that the start and stop times of the current peaks differ (`Calc_Err_time.m`)
- The difference in RMS current (`Calc_Err_Irms.m`)

The .m files in this column are modified versions of an .m file that was written by Dr.ir. Stievano.

The routines in the left most column, "*Model simulation*" contains the actual model and runs the simulation. `odet23t(.)` is a standard MATLAB routine, but the rest of this column has also been written by Dr. Stievano.

Note that the MATLAB model and hence the optimization routine assumes the load to be resistive, meaning the value for R_{load} is optimized. To obtain a value for I_{load} and P_{load}, `Vdc_waveform.m` is called, which returns the V_{DC} waveform from the simulation. Together with the value for R_{load}, the current waveform through the load is calculated. After that the power dissipated in the load, as well as the average current are calculated, obtaining P_{load} and I_{load}.

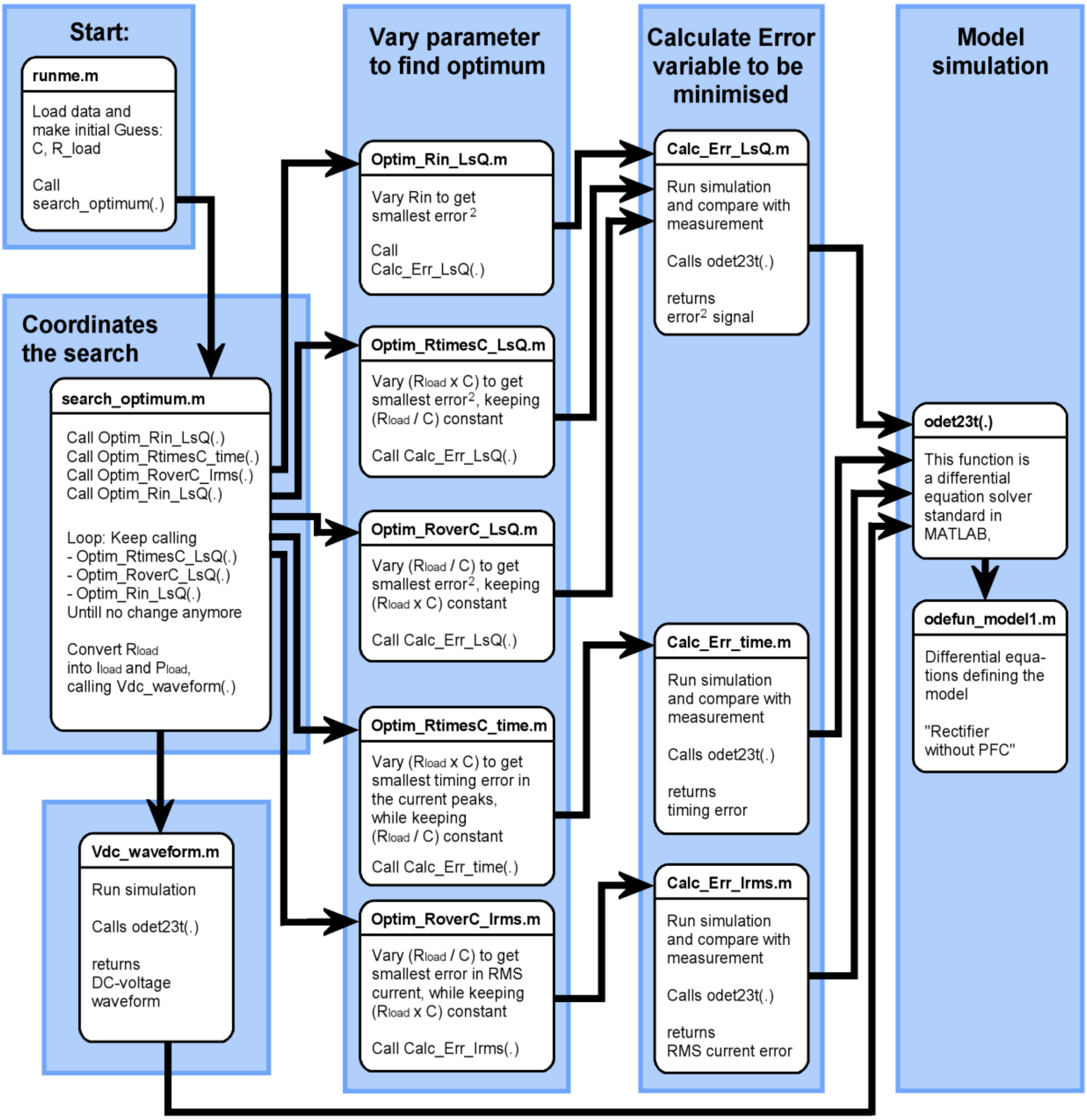

Figure 100: Hierarchy structure of the optimization routine in MATLAB