ANALYSIS AND DESIGN OF A LOW POWER ADC

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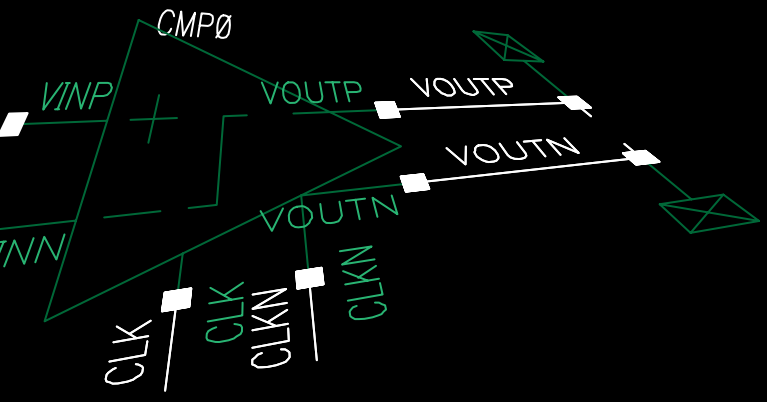

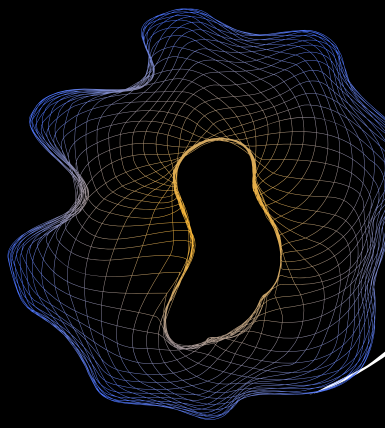

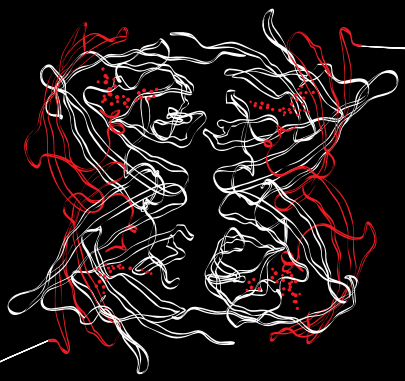

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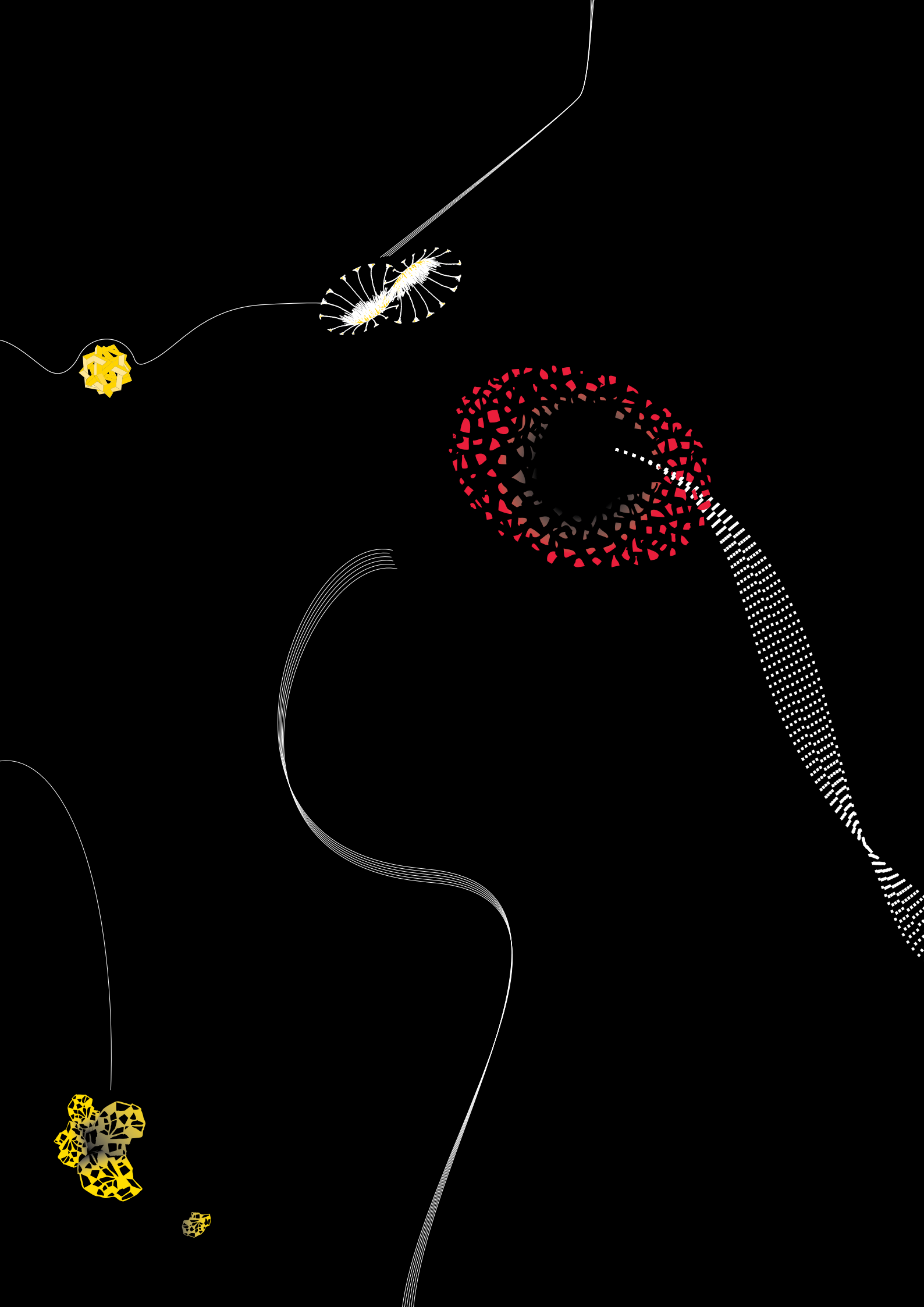

ABSTRACT

The main goal of this thesis is to design an ADC for the use in a low power spectrum analyzer (SA) aiming for cognitive radio applications. The receiver of the SA should operate power efficient because of the intended use in mobile applications. It should also have a high SFDR to detect weak signals in the spectrum.

For the power efficiency, a successive approximation ADC is implemented using a charge redistribution DAC. To reduce the overall power consumption of the SA, an amplification step in the signal path of the SA receiver is eliminated by creating a small input range for the ADC. This small input range introduced offset problems for which a new calibration procedure is developed. The calibration reduces the offset to under 1 LSB.

The SA uses digital cross-correlation to filter noise digitally and acquire a high SFDR. Because of this the primary focus on the design of the SA and its ADC is a high linearity to prevent harmonics and inter-modulation products in the output, limiting the SFDR. The linearity of the ADC is mainly influenced by mismatch between capacitors in the charge redistribution DAC. A new calibration architecture and procedure is introduced to increase the matching of the capacitors in the DAC.

The result is a 7-bit ADC consuming only 38.2 µW at 40 MS/s having a supply voltage of 1 V. The input range is 63 mV and it has a SFDR of 72 dB. With the new calibration method a higher SFDR can be achieved at the cost of a slight increase in power consumption.

CONTENTS

INTRODUCTION

Nowadays electronics and especially integrated circuits play an important role in modern society. Markets for electrical devices are growing rapidly as well as the number of new technologies being developed. Recent developments show a strong trend towards more mobile applications. Energy consumed by these applications can be harvest from the environment, but most mobile devices still depend on a battery as power source. Nevertheless both of them bring a demand for low power consumption to the electronics. The objective of this thesis is to design a low power analog to digital converter in CMOS.

The terms ‘low power’ and ‘ultra low power’ are widely used for a long time, while technology develops and becomes more advanced. Therefore these terms are slowly losing their credibility and it is more appropriate to look at the most energy efficient ADCs available today. A recent benchmark will be the ADC from M. van Elzakker which is a 10-bit ADC consuming only 1.9 µW at a sample speed of 1 MS/s [6]. With an ENOB of 8.75 bits this ADC has a power efficiency of 4.4 fJ per conversion step.

During the thesis some new ideas were investigated in order to create a new design which can compete with the benchmark described above. First of all the Träff comparator [16] was examined for the use in a low power current ADC. The reasons for this were the energy efficient properties of this comparator and earlier attempts made [17] seemed to become more energy efficient when scaled to newer and smaller technologies. The results of using the Träff comparator in a current ADC can be found in chapter 2.

The second idea investigated was an improvement for the voltage ADC of M. van Elzakker [4]. In this ADC, charge from the input is loaded onto a sample capacitor after which it is locked and modified for comparisons to a reference voltage. After the analog to digital conversion is completed, the same charge is still available on this sample capacitor. The idea of the improvement was to consume this sample charge for the conversion, instead of only measuring it and consuming the power from a supply. This idea resulted in a ‘discharging ADC’ from which the architecture and conclusions can be found in chapter 2.

The third and last idea investigated came from a more practical point of view. In a lot of applications, for instance radio receivers, a weak incoming signal has to be amplified before it can be converted by an ADC. The power consumption is then often dominated by the amplifier instead of the analog to digital conversion. By creating an ADC with a small input range, lots of amplifier power can be saved reducing the overall power consumption.

During the thesis, intermediate results led to the decision to further develop this last idea. The idea came originally as a result of a practical RF-receiver application where low power consumption was needed. This application is a spectrum analyzer for cognitive radio applications [1]. The low power consumption is needed because of the intended implementation in mobile devices. In this thesis a complete ADC is designed for this application, giving the ADC more requirements like a needed high linearity. The requirements for the ADC are derived in chapter 3, the application will be described next.

1.1 A SPECTRUM ANALYZER FOR COGNITIVE RADIO

The radio frequency spectrum refers to the part of the electromagnetic spectrum with an rate of oscillation in the range of 3 kHz to 300 GHz. Nowadays this spectrum is widely used for radio communication. To combat interference of radio transmitters, the spectrum is in most countries strictly regulated by government. Often licences are sold, which allows a buyer to exclusively transmit into a specific part of the spectrum. In practice not all buyers make use of there reserved spectrum at all times, making the usage of the RF-spectrum very inefficient. A measurement of the spectrum at one day illustrates the inefficiency (see Figure 1-1).

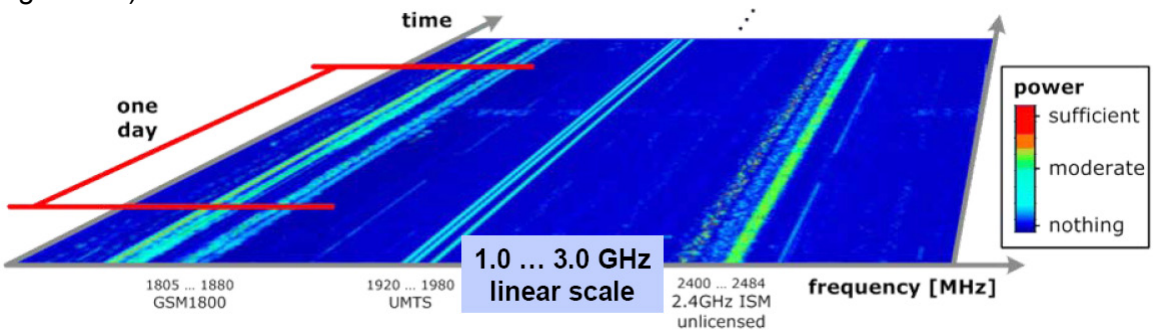

Figure 1-1, Usage of the spectrum between the band 1 GHz to 3 GHz [2], illustrating the inefficient usage

Cognitive radio is a technique which tries to make use of the unused parts of the spectrum without interfering with for instance licensed or other users. A cognitive radio transceiver detects which part of the spectrum is unused. The transceiver will then use such a part for communication. When the transceiver detects an interferer during transmission it will quickly switch to another unused part of the spectrum.

For this task the transceiver needs flexible hardware to be able to switch fast to other frequencies. Also a spectrum analyzer needs to be present, which continuously monitors the spectrum looking for unused parts and interferers. A global architecture for such a spectrum analyzer was developed in [1]. The ADC needed for this analyzer was investigated in [5], where different architectures where compared, specifications for the ADC where drawn up and recommendations for the ADC architecture were given.

In this thesis the ADC for the spectrum analyzer will be designed. A short overview of the complete spectrum analyzer is given in chapter 3, following the signal path up to the ADC. Also the chosen ADC architecture for our design is presented there and the ADC requirements are derived. Innovations to the designed ADC are the small input range which eliminates amplifier power and a calibration procedure which improves the linearity of the ADC drastically and reduces the ADC's offset.

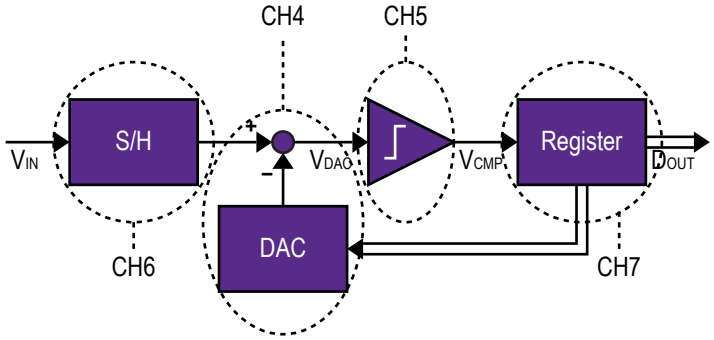

Figure 1-2, Parts of the ADC designed and the chapter where they are described

In chapter 4, 5, 6 and 7 each part of the designed ADC is treated according to Figure 1-2. In each chapter the element is described first and its novelties are introduced. Secondly the implementation of the part is discussed and calculations are done which lead to a final design. After this, the part is simulated and the results are given and discussed leading to a conclusion.

In chapter 8 the overall conclusions are drawn. The performance of the complete ADC is discussed and compared with the requirements given in chapter 3. Afterwards recommendations are given.

ANALOG TO DIGITAL CONVERTERS

An analog to digital converter has to convert an continuous analog signal to a discrete binary code. This analog signal can be an electrical voltage or a current. Over the years many techniques are developed to perform this task. Each technique having their own properties and drawbacks making them optimal for a certain task.
The goal of this thesis is to develop a low power ADC. As mentioned in the introduction three new ideas were investigated in order to develop an ADC which can compete with the least power consuming ADC available today [6]. The first two ideas are described in this chapter. Starting with the investigation of the Träff comparator and its possible application in a current ADC. After this the possibility of a discharging ADC is discussed.

2.1 LOW POWER CURRENT ADC

The first idea investigated during the thesis is the Träff comparator [16]. In [17] this comparator was used to create an analog to digital converter. The energy efficient properties of the comparator were the reason to look into the possibility to use it in an ADC. In the first part of this section the comparator is introduced. Afterwards the possibility of using it in an ADC is discussed followed by a conclusion.

2.1.1 THE TRAFF COMPARATOR

The Träff comparator is a current comparator which structure is shown in Figure 2-1.

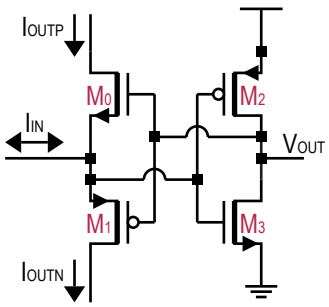

Figure 2-1, The Träff Comparator

It consists of four transistors forming an input stage (M_0 and M_1) and an inverter as output stage (M_2 and M_3). A feedback is present between the output and the gates of the input transistors. The comparator measures the direction of the current at the input. Current flowing into the comparator will raise the voltage at the input of the inverter resulting in a low output voltage. This low output voltage will open the gate of transistor M_1 which will let the input current flow through this transistor to the output I_{OUTN}. A negative input current will result in an opposite situation, drawing current from node I_{OUTP}. Next to the advantage of the

simple architecture, the main advantage of this structure is that input stage is completely driven by the input current and therefore consuming no power at all. The second advantage of the input stage is that the current flowing into the comparator will completely be available at one of the outputs of the comparator, making the same current reusable for another conversion. Also the input stage is able to handle a wide range of input currents.

2.1.2 ADC ARCHITECTURES

In [17] the comparator was used in a flash-like current ADC. The idea of this current ADC is illustrated in Figure 2-2.

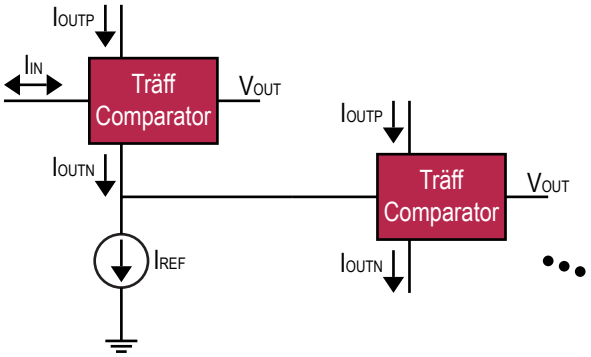

Figure 2-2, The Träff comparator in a flash-like ADC. One stage consists of a reference current source and a comparator.

In the architecture 2^N stages are used for an N bit converter. Each stage consists of a Träff comparator and a current source representing a LSB current. All the stages are placed in series. In each stage a LSB current is subtracted from the input current before the current flows into the comparator. At a certain stage the resulting current is less then zero and the LSB current source will start drawing current from the comparator. The stage where this happens can be located by looking at the outputs of the comparators. The outputs before this flipping point give a logic low while the outputs after this point output a logic high.
The are several drawbacks of this architecture. The input capacitance of the comparator sets a limit to the speed of the ADC. Since the architecture consists of 2^N stages the structure will have a (very) large input capacitance when a high resolution ADC is wanted. This input capacitance makes the ADC performing very slow.
Another disadvantage is the leakage current in the second stage (inverter) of each comparator. Especially when the input current is small the voltage at the input node of the comparator (see Figure 2-1) will be around half the supply voltage, resulting in a high leakage current in the inverter. This unwanted effect is intensified by the number of comparators needed in the architecture. In [17] the leakage is reduced by redesigning the inverter, but the leakage current still dominates the consumption of the complete ADC.
For this reason several other architectures are investigated. Using the same architecture of Figure 2-1 a pipelined SAR like architecture can be created by making binary weighted current references (which can be turned on or off). Using this architecture reduces the leakage current since only N comparators are needed for a N-bit converter. Nevertheless this architecture introduces the need of a current sample and hold. Because of this, the input current of the ADC will be drawn from the supply voltage instead of being input driven.

2.1.3 CONCLUSION

The Träff comparator is investigated for its use in a current ADC. The conclusion is that the comparator is not very suitable for this purpose when a low power consumption is required. The input capacitance makes the comparator slow compared to other solutions. Speed is an important property for a low power consumption, especially when a current sample and hold is used drawing current from a supply.
The low gain of the comparator is also a problem since it causes a leakage current in the inverter stage of the comparator. The feedback coming from the inverter causes a low voltage swing at the input node reducing its own gain. Because of this the output of the comparator will not be a digital signal, so additional inverters are needed to amplify the signal. Each consuming extra power.
The gain can be increased by adjusting the dimensions of the transistors in the input stage. Nevertheless this reduces the current input range of the comparator and causes large voltage swing at the current output. The voltage swing at the output results in accuracy problems for the reference current source used after each comparator.

When using a current sample and hold, a more efficient solution can be made when the input stage of the Träff comparator is removed and just an inverter is used. A solution can be seen in Figure 2-3.

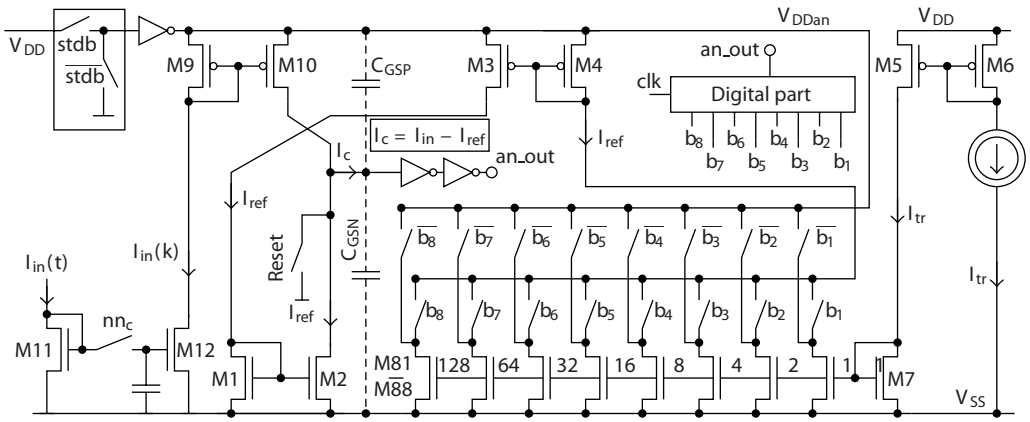

Figure 2-3, A current ADC solution using the SAR algorithm and an inverter as comparator

The ADC shown in the figure comes from [20] and consumes only 560 nW of power for an 8-bit resolution at a speed of 2 MS/s. It is a current SAR-ADC using binary weighted current sources and an inverter as comparator.

2.2 LOW POWER DISCHARGING ADC

The second idea which was investigated was based on the SAR-ADC of [6]. In this ADC an amount of charge is sampled onto a sample capacitance by a sample switch. After the switch is closed the charged is locked. The ADC uses a charge redistribution DAC to adjust the voltage on the sample capacitance in order perform comparisons used for the SAR algorithm. The sample charge is still available on the capacitor when the sample switch opens again. The idea of the improvement is to use the 'free' obtained sampled charge for performing a conversion. This resulted in a discharging ADC which is described in the second part of this section. Conclusions are drawn afterwards.

2.2.1 CHARGE REDISTRIBUTION ADC

The ADC of [6] uses a charge redistribution DAC with a split capacitor architecture which is described in chapter 4. The basic charge redistribution DAC is shown in Figure 2-4.

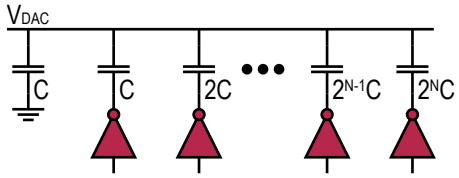

Figure 2-4, A basic charge redistribution DAC

It consists of a binary weighted capacitor array driven by inverters. A sample charge is loaded onto the array by a sample switch. After the switch is closed the voltage at V_{DAC} is adjusted by the inverters following the SAR algorithm, using a binary search. The voltage at V_{DAC} is compared to a reference voltage after each adjustment. As example, raising the voltage of V_{DAC} means switching an inverter output from low to high, charging the bottom plate of the capacitor connected to it. This charging consumes power.

2.2.2 DISCHARGING ADC

To prevent this charging and thus reduce the consumption, an alternative DAC architecture is developed which is shown in Figure 2-5.

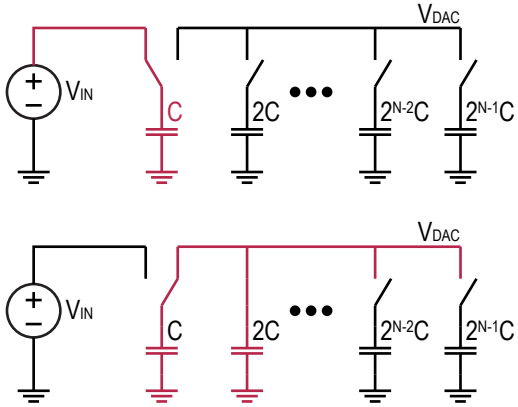

Figure 2-5, Architecture of the discharging ADC. Top: sampling phase of the DAC. Bottom: conditional discharging by coupling the sample capacitance to empty capacitors

The DAC consists of one sampling capacitor and a binary weighted array of empty capacitors. The input is sampled on the smallest capacitor. The voltage at V_{DAC} is compared with a reference voltage. The outcome of a comparison determines which empty capacitor is coupled to the sample capacitance to lower the voltage at V_{DAC}. When this voltage is lower than the reference voltage the reference voltage will be lowered. This means, when implementing the discharging DAC in differential form, the outcome of a comparison determines which of the 2 sample capacitors should be discharged.

Due to the fact only energy is needed for the switches, large capacitors can be used. This reduces the effect of charge injection by the capacitors. Instead of the switches shown in Figure 2-5 also bottom plate sampling can be used, which prevents charge injected during operation.

2.2.3 CONCLUSION

The architecture as presented in this section has several drawbacks which were reason to stop the development during this thesis. The drawbacks of the DAC itself were the charge injection during the reset phase (where the capacitor array is emptied) and the large chip area needed due to the large capacitors used.
Nevertheless the largest drawbacks were the requirements on the comparator needed for the use with the discharging DAC. These requirements on the comparator were a very low offset, which is important because the gain of the ADC changes during operation. Also a very small input voltage should be detectable by the comparator, since the voltage differences become very small while discharging. Next to this the common mode of the input changes, which is not the case in [6]. So a large common mode range should be available.
These requirements made the use of the energy efficient comparator used in of [6] not possible. Using another comparator to overcome the drawbacks increased the power consumption, cancelling the power consumption saved by using the discharging DAC.

ANALOG TO DIGITAL CONVERTERS

LOW POWER RF-RECEIVER ADC

As mentioned in the introduction, three ideas for the design of a low power ADC were investigated. The first two are described in chapter 2, their conclusions were reason to continue with a third idea which came from a more practical point of view. The objective of this third idea is to develop an ADC with a small input range to save amplifier power.
In applications like antenna receivers, a weak input signal has to be amplified before it can be converted by an ADC. The often dominant power consumption of this amplification can be eliminated when an ADC with a small input range is present.
In this thesis an ADC will be designed for a spectrum analyzer aiming for cognitive radio applications. The main focus for this ADC will be on the small input range and a low power consumption of the ADC itself. Next to this, the application gives more important requirements to the ADC. For instance a needed high linearity and noise requirements.
In the first part of this chapter the spectrum analyzer application is described which is based on the design of [1]. This leads to a choice of an ADC architecture and the needed specifications for the ADC which are described in section 3.2 and section 3.3.

3.1 THE SPECTRUM ANALYZER

The task of a spectrum analyzer (SA) in a cognitive radio application is to continuously monitor the usage of a wide band of spectrum. A receiver for this task is developed in [1], and the structure of this receiver is shown in Figure 3-1. The goal of the thesis is to design the ADC for this receiver. A short overview of each element in the SA will be given in this section, leading to the needed specifications for the receiver's ADC.

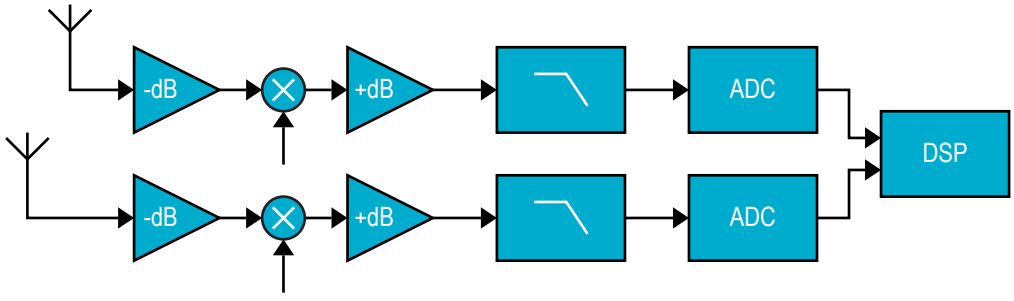

Figure 3-1, Overview of the spectrum analyzer. Two signal paths are present containing signal attenuation, a mixer, amplification, a low-pass filter and an ADC followed by a digital signal processor.

For the SA the strength of the signals in the spectrum are of importance rather than the information being transmitted. To be able to detect weak signals in the spectrum, it is important for the receiver to have a high spurious-free dynamic range (SFDR). A harmonic from a strong input signal or noise cannot be distinguished from a weak input signal when they occur at the same frequency. This is illustrated in Figure 3-2.

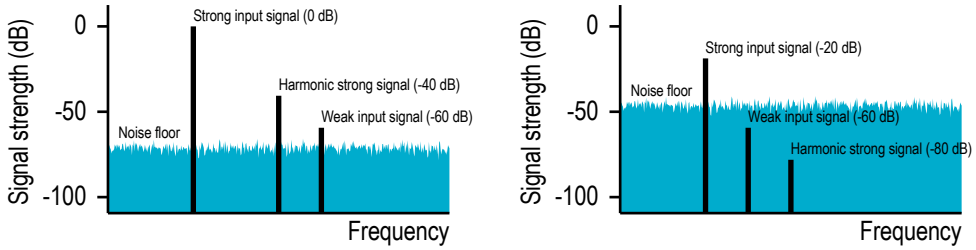

Figure 3-2, Examples of a SA output, illustrating the importance of a high SFDR. Left: A distortion component from a strong input signal is indistinguishable from a weak input signal. Right: Noise makes a weak input signal undetectable.

The SFDR is limited by the generated noise in the receiver and the linearity of the receiver (non-linearities will create harmonic- and intermodulation distortion in the output). As described in [1] there is a trade-off between both, limiting the SFDR. Increasing linearity of the components in the receiver results in an increasing noise floor, while lowering the noise floor of the components results in a decrease of linearity. So the limit of the SFDR is the technology where the SA is produced in.
As illustrated in the receiver overview in Figure 3-1, two signal paths are present with two different antennas. This makes it possible for the spectrum analyzer to filter noise digitally by a cross-correlation technique described in [1]. In this way the noise floor can be decreased without having the trade-off with the linearity of the system while using the same technology. Filtering noise digitally means that linearity becomes the first priority in the receiver design in order to increase the SFDR. The requirement for the SFDR of the SA is determined in [5] and set to 70 dB.

3.1.1 ANTENNA AND ATTENUATION

The antenna/external filter and the signal attenuation are the first two elements in the receiver as shown in Figure 3-1. According to [1] the intended bandwidth of the spectrum analyzer is 0 GHz - 6 GHz. The maximum expected power of the input signal coming from the antenna/external filter is 0 dBm, which is estimated as the strongest signal which a mobile device will receive [5]. In general the signal coming from the antennas is first amplified by an LNA. But because of the wide bandwidth and the high linearity needed for the application an architecture without LNA is used at the cost of noise [1].
To increase the linearity of the mixer, variable signal attenuation is applied before the mixer. This is done with a R-2R ladder network circuit which is able to attenuate the signal in steps of 6 dB, consuming virtually no power from the supply. The attenuation applied in the SA has 5 branches able to attenuate the input signal up to approximately 24 dB. Details of the signal attenuation can be found in [1] and an overview of the attenuation for each branch is given in Table 3-1.

f_{LO}	Conversion gain [dB] for each attenuation branch				
[GHz]	1	2	3	4	5
0.4	0.42	-5.26	-11.25	-17.37	-23.63
6.0	0.26	5.45	11.45	-17.58	-23.84

Table 3-1, Conversion gain of each branch at two different input frequencies

3.1.2 MIXER

Because of the large bandwidth of the spectrum analyzer, the signal cannot be converted directly to the digital domain. Therefore a mixer is added in the signal path which brings a part of the spectrum to DC. The mixer used in the SA is shown in Figure 3-3. This mixer is extensively discussed in [3]. It has a high IIP3 and low noise figure which makes it ideal for the use in the SA. The mixer works like a sample and hold circuit and is implemented as a quadrature sampling mixer. The duty cycle of the switches is 25% and the period time is determined by the mixer frequency.

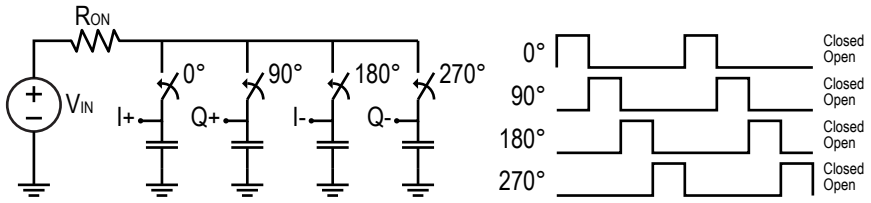

Figure 3-3, The mixer and the state of the switches in time, R_{ON} represents the on-resistance of the switches

The bandwidth of the mixer is limited to approximately 20 MHz [3], which limits the bandwidth of the SA and gives a speed requirement to our ADC of 40 MS/s.
The mixer contributes to the non-linearity of the SA. The linearity of the mixer is determined in [1] and shown in Figure 3-4 expressed in the third-order intercept point (IIP3) as function of the input frequency.

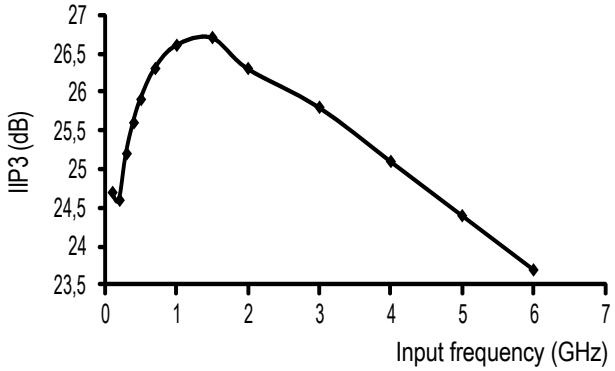

Figure 3-4, IIP3 of the mixer as function of the input frequency

With this information and the SFDR requirement of 70 dB the needed input range of our ADC can be determined. This is done in [5] for the maximum input signal of 0 dBm and a mixer IIP3 of 22 dB.

$$P_{att} = IIP3 - \frac{HD_{3,dB}}{2} = 22dB - \frac{70dB}{2} \approx -13dB$$

So an attenuation of the input signal of minimal -13 dB is needed to meet the 70 dB SFDR requirement. Like in [5] an attenuation of 20 dB is assumed, since the 70 dB SFDR is needed for the complete receiver and not only up to the mixer.
The maximum output voltage of the mixer can be determined with the 20 dB attenuation, an input signal of 0 dBm and R = 50 Ω.

$$P_{dBm} = -20dBm = 0.01mW$$

$$V_{out,RMS} = \sqrt{0.01mW \cdot 50\Omega} \approx 22.4mV$$

$$V_{out,peak-peak} \approx 31.6mV$$

So for the ADCs measuring the two quadrature mixer signals, a differential input range of approximately 63 mV is required.

3.1.3 AMPLIFICATION AND ANTI-ALIASING

Normally the signal is amplified after the mixer, followed by an anti-alias filter as shown in Figure 3-1. Amplification is needed to get the signal in the input range of the ADC and filtering is needed to prevent aliases in the output of the ADC. The idea of this thesis is to eliminate this amplification by designing an ADC with a small input range. This will save power and prevents extra non-linearities in the signal path. As described above the maximum differential output voltage of the mixer is approximately 63 mV. Assuming a power supply of 1 V the signal needs to be amplified approximately 30 dB to get it in the range of a full scale differential ADC. Furthermore the SFDR of the amplifier should be more than 70 dB to meet the requirements. The power consumption of such amplifiers [9][10][11][12] vary between approximately 1 mW to 50 mW.
This amplifier power gives a power consumption restriction to our ADC. Possible extra power consumed by our ADC used to acquire the small scale input range, should not be higher than this amplifier power in order to reduce the overall power consumption of the receiver.
Still an anti-alias filter needs to be present in the signal path. The filtering is investigated and discussed in [5]. The mixer used in the design has already a first order low pass filter characteristic [3], which relaxes the anti-alias filter requirement by approximately one order. The ADC architecture which will be chosen in section 3.2 has also a low pass filter characteristic. This relaxes the filter requirement again by approximately one order.
The coupling between the mixer and the ADC is also described in [5], it requires impedance matching and leaves room for one or more analog filters (like simple Butterworth filters). Other solutions suggested in [5] are time interleaving using multiple ADCs in parallel or a time discrete filter which is possible because of the mixer's discrete time output. The time interleaving method is the least preferable since it reduces the saved power consumption by the elimination of the amplifier.

3.2 ADC ARCHITECTURE

The ADC which should be used for in the SA is investigated in [5]. A successive approximation register (SAR) ADC is recommended using a charge redistribution DAC. The architecture of a SAR-ADC is shown in Figure 3-5.

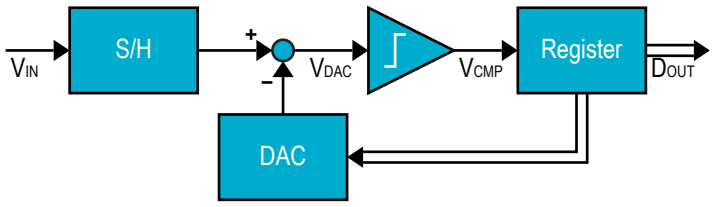

Figure 3-5, The architecture of a successive approximation register ADC

The SAR-ADC consists of a sample and hold (S/H), a digital to analog converter (DAC), one comparator and a digital register. In the SAR algorithm the output of the DAC will approximate the input of the ADC via a binary search. First the input is sampled by the S/H. After this it will be compared to the output of the DAC by the comparator. The input of the DAC will be adjusted according to the comparator output, starting with the MSB working towards the LSB of the DAC. This is illustrated with an example as shown in Figure 3-6.

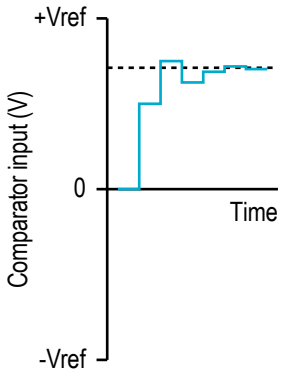

Figure 3-6, Example of one conversion using the SAR algorithm in a 8-bit ADC. Dotted line indicates an example of an input voltage. The blue line indicates the DAC output.

Starting at the most significant bit the DAC output will approximate the sampled voltage. After a conversion is completed the input of the DAC will be equal to the output of the ADC. There are only n comparisons needed for a n-bit converter, making the SAR algorithm power efficient compared to other architectures.
The DAC used in our ADC will be a charge redistribution DAC. This DAC will be described in chapter 4. For now the important property of the charge redistribution DAC is the fact that it behaves just like a sample capacitor connected to a switch during the sampling phase of the SAR algorithm. This property makes it ideal for cooperation with the used mixer or a time discrete anti-alias filter.
Direct coupling would be even more likeable (where the mixer is part of the ADC). Nevertheless this is not possible since some impedance matching and anti-alias filtering are needed [1][5].

3.3 REQUIREMENTS FOR THE ADC

The requirements needed for the design of the ADC will be summarized in this section.

3.3.1 TECHNOLOGY AND SUPPLY VOLTAGE

The ADC will be produced in a 65 nm process from ST-microelectronics. This is done because SA design of the first stages are also designed in 65 nm [1]. The supply voltage used is 1 V.

3.3.2 RESOLUTION AND BANDWIDTH

The resolution of the ADC is determined in [5]. A 7-bit resolution of the ADC is required to achieve a SFDR of 70 dB. Although, to achieve this 70 dB SFDR, the 7 bit resolution has to be increased. This is done by applying a dithering technique [1]. This technique will replace the distortion caused by the quantization error of the ADC with random noise in the output. Therefore dither noise will be added to the signal in the ADC. The added noise will eventually be filtered out of the signal again by the digitally applied cross-correlation technique.
The bandwidth of the ADC is determined by the bandwidth of the mixer which is 20 MHz. So a sample frequency of 40 MS/s is required.

3.3.3 NOISE

The intention of the cross-correlation is to digitally remove noise produced in the receiver. This relaxes the noise requirement of the ADC. The noise produced by the ADC is mainly caused by the sample switch, the DAC and the comparator. The comparator is expected to be the largest noise contributor. Lowering this noise means a higher power consumption of the comparator. To make the SA power efficient, this increase in consumption should be lower than the amount of power consumption saved with the elimination of the amplifier.
As mentioned in the previous part, noise should be added to the signal by the ADC to be used for dithering. In [5] the needed amount of this noise is determined to be 0.64 LSB bit for a 7-bit converter.

3.3.4 INPUT RANGE

The differential input range of the ADC is determined in the first section of this chapter and is set to approximately 63 mV.

3.3.5 LINEARITY

The SFDR of the ADC is set to 70 dB according to [5]. This sets a requirement to the linearity of the ADC. Non-linearities in the ADC are mainly caused by non-linearities in the charge redistribution DAC. The DAC as well as a new developed technique to increase the linearity is treated in chapter 4. Guideline here is the required 70 dB SFDR.

3.3.6 POWER CONSUMPTION

The overall power consumption should be kept as low as possible because of the intended use of the SA in mobile applications. An absolute maximum for the power consumption of the ADC is set in the first section of this chapter. The power consumption of the designed ADC should not exceed the consumption of an amplifier in combination with a regular ADC.

3.4 CONCLUSIONS

In the thesis an ADC will be developed for the application of a spectrum analyzer. The requirements for the ADC are derived from the requirements of the SA in this chapter. A successive approximation register is chosen as the ADC's architecture, because of its power efficiency. The DAC used in the ADC will be a charge redistribution DAC, which will be treated in 4.
The expected main challenges will be the SFDR requirement of 70 dB. Also the required small input range is expected to be a challenge since it will set high demands on the comparator and the noise produced in the ADC.

DIGITAL TO ANALOG CONVERSION

The complete ADC architecture is shown in Figure 4-1. The digital to analog converter part of the ADC is highlighted and will be discussed in this chapter. The DAC is used to adjust the sampled input voltage of the ADC. The design of the DAC is focussed on low power consumption as well as high linearity required for the spectrum analyzer application. Due to the small input range of the ADC, the DAC should have a small output range.

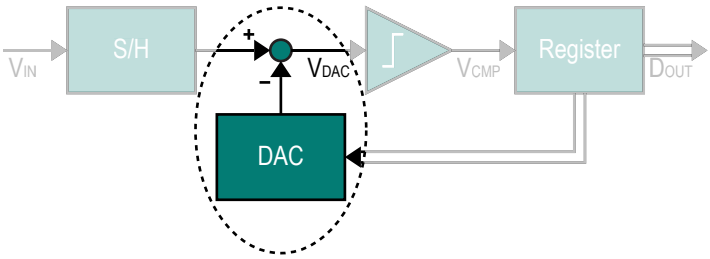

Figure 4-1, The DAC will be treated in this chapter

The architecture of the used DAC is discussed in the first section of this chapter. Several improvements are applied to the DAC which are also described in this first section. In the second section the implementation of the DAC is described. Calculations are done which are needed for the design. In the third section the DAC is simulated and the performance is discussed. In the last section conclusions are drawn.

4.1 THE CHARGE REDISTRIBUTION DAC

The DAC in our successive approximation ADC is used to add or subtract reference voltages to or from the sampled voltage. The DAC used for our ADC is a charge redistribution DAC. The architecture and operation of a standard charge redistribution DAC is shortly described in the first part of this section.
Three improvements are added to this standard DAC, these are described in the last three parts of this section. First the split-capacitor technique is shortly described, which is applied for a faster and more power efficient operation. Secondly a new method to reduce the output range of the DAC is presented. This is needed because of the ADC's required small input range. In the last section a new calibration technique is introduced, which is applied to improve the linearity of the DAC drastically and reduce power consumption.

4.1.1 BASIC ARCHITECTURE

The basic architecture of a charge redistribution DAC is shown in Figure 4-2. It consists of a binary weighted capacitor array with N capacitors for an N-bit converter. The shared node V_{DAC} is connected to the sample switch and the comparator of the ADC. The capacitors are driven by inverters and a dummy capacitor is present which is connected to GND and has a size equal to 1 unit capacitor (C).
During the sampling phase of the ADC, a sample charge is loaded onto the capacitors in the array by the sample switch (discussed in chapter 6). The inverters make it possible to switch one plate of each capacitor between VDD and GND, this adjusts the voltage at the shared node V_{DAC} after the sample switch is closed. The dummy capacitor of 1C is present to influence the total DAC capacitance making the voltage adjustments binary weighted parts of the reference voltage VDD (1/2 VDD, 1/4 VDD etc.)

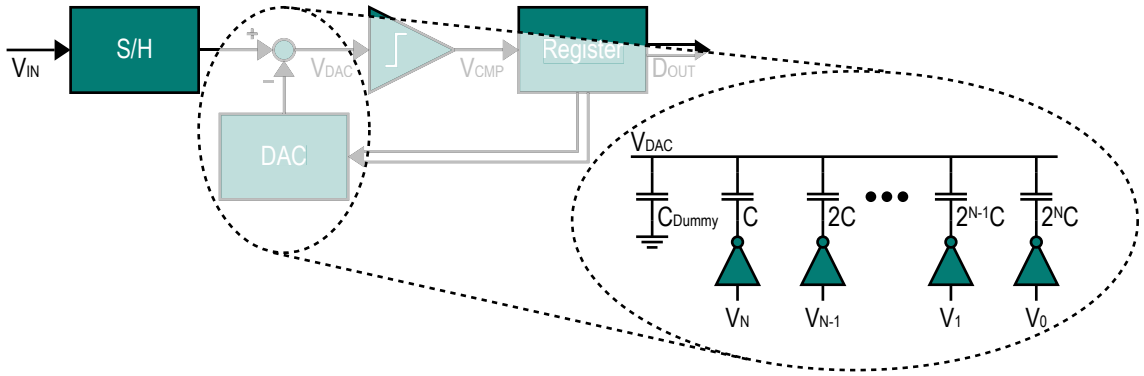

Figure 4-2, A basic charge redistribution DAC

During the sampling the bottom plates of all capacitors are connected to GND except for the largest capacitor which bottom plate is connected to VDD. This makes it possible to either add or subtract voltages to or from the sampled voltage. The voltage at V_{DAC} as function of the state of each inverter (binary array expressed as integer with V_0 as MSB) is plotted in Figure 4-3.

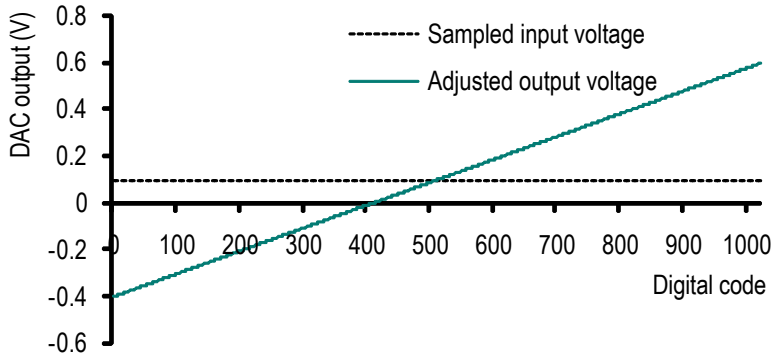

Figure 4-3, Example of the in- and output voltage in an 10-bit DAC with a VDD of 1V. The digital code represents the state of each inverter.

4.1.2 SPLIT CAPACITOR ARRAY

To reduce the power consumption of the basic DAC, a split capacitor technique is applied [8]. For this technique the basic DAC architecture of Figure 4-2 is replaced with the symmetric architecture shown on the left in Figure 4-4. As can be seen the largest capacitor in the basic array (representing half the capacitance of the total array) is split into a second array creating a symmetric structure. During the sampling, the bottom plates of the lower array are connect to GND and the bottom plates of the upper array to VDD. This makes it possible

to add or subtract different voltages directly to or from the sample voltage at V_{DAC}.

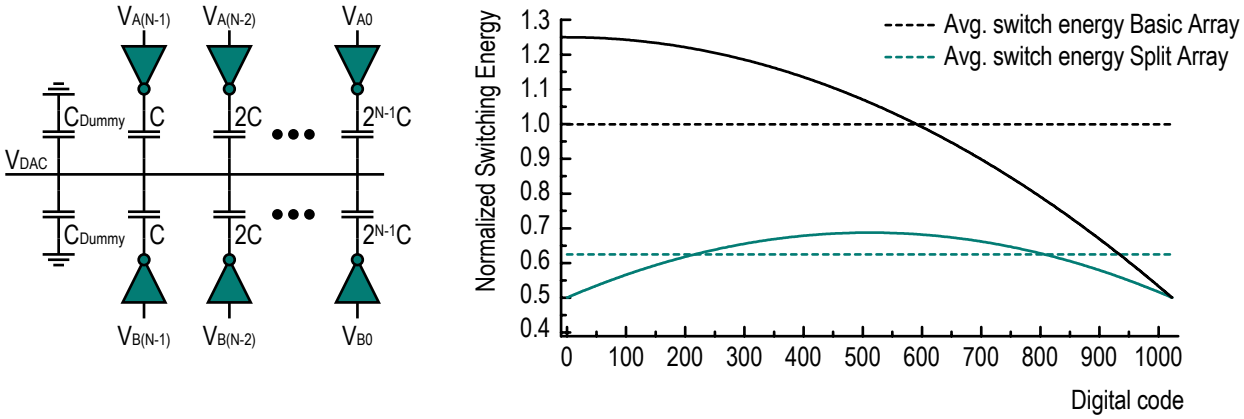

Figure 4-4, Left: the split capacitor array which replaces the basic array. Right: Switching energy of a 10-bit ADC applying the SAR algorithm. The basic array (black) and the split capacitor array (green) as function of the ADC's digital output.

The split capacitor architecture is because of this more power efficient than the basic array, where some voltages can only be subtracted indirectly. This will be illustrated by an example where VDD/4 needs to be subtracted from the sample voltage.
To accomplish this with the basic array two actions should be taken. First the bottom plate of the largest capacitor (2^NC in size) should be discharged to GND. Secondly the bottom plate of the second largest capacitor (2^{N-1}C in size) should be charged to VDD. Subtracting the voltage with the split capacitor architecture means that there is only one action, the bottom plate of a capacitor with size 2^{N-1}C should be discharged to GND. In general the split capacitor architecture prevents unnecessary charging and discharging of capacitors, making it less power consuming and faster.
The power consumption of both architectures are shown on the right side in Figure 4-4. In this figure both DAC architectures are applied in a 10-bit ADC using the SAR-algorithm. The overall power consumption is approximately reduced by 33 % compared to the basic charge redistribution DAC. Details of the split capacitor architecture and different switching algorithms can be found in [8].

4.1.3 INPUT RANGE AND GAIN

One of the targets for our ADC used in the spectrum analyzer (SA) application, is a small input range. A small input range of the ADC eliminates the need of an amplifier in the signal path which results in power reduction for the SA.
The input range of the SAR-ADC is normally reduced by adjusting the reference voltage in the charge redistribution DAC. With the use of inverters in the DAC, the VDD acts as reference voltage. Using a lower voltage will result in smaller voltage steps in the DAC, leading to a smaller input range of the ADC. However doing this brings the disadvantage of the required new reference voltage and more complex driving circuitry than the simple inverter.
Another way of making smaller voltage steps in the DAC is increasing the size of the dummy capacitances from Figure 4-4. This will increase the input capacitance and therefore the sampling time of the ADC. For this the reason, this method is normally not applied. Nevertheless for the application of the SA, a larger capacitance can be valuable. It reduces the kT/C noise, which will become more of an issue when reducing the input range. Another advantage is that fluctuations in the reference voltage (VDD) will have less effect on the sampled voltage. In Figure 4-5 the input range of the ADC is plotted against the size of the dummy capacitance in the DAC.

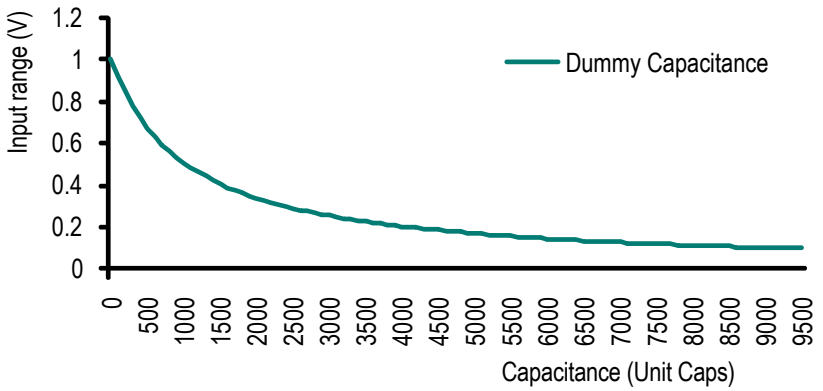

Figure 4-5, The input range of the ADC as function of the dummy capacitance in a 10-bit ADC with a 1 V supply. The capacitance is expressed in unit caps, where 1 unit cap represents the smallest capacitor in the capacitor array.

As can be seen in the figure, the size of the dummy capacitor needs to increase exponential to reduce the input range of the ADC. The total input capacitance of the ADC will increase with the same rate. The actual size of the total capacitance depends on the size of a unit capacitor (C).
Usually this size is determined by the mismatch between the capacitors in the array (which have sizes 1C, 2C etc.) rather than the noise produced by them [4]. For the application of the SA, good matching is needed to accomplish a high SFDR. This means the size of a unit capacitor, and therefore the size of the total input capacitance, will increase even further when a standard split capacitor array is used.
To prevent this increase in capacitance and increase the matching between the capacitors, a calibration technique is developed. This technique is introduced in the next part (4.1.4 on page 30). The technique makes use of the larger dummy capacitor, while it reduces the size of a unit capacitor. Due to the calibration, the total capacitance can even be reduced until it is limited by the kT/C noise on it. This will result in a small input range, high linearity and only a slight increase in input capacitance compared to the increase illustrated in Figure 4-5. The slight increase in capacitance will limit the disadvantage of the larger sampling time. And since the size of the unit capacitor determines the power consumption and the speed of the DAC, the smaller unit capacitor will make the ADC faster and more power efficient.

4.1.4 CALIBRATE TO REDUCE MISMATCH

Mismatch between the capacitors in the DAC will result in non-linearities in the ADC. Non-linearities in the ADC will generate harmonic distortion in the output of the ADC, lowering the SFDR. For the SA a high SFDR is required. Therefore a new calibration technique is developed which reduces the mismatch in the DAC, without increasing the size of the capacitors. It will make use of the larger dummy capacitance introduced in the previous part.

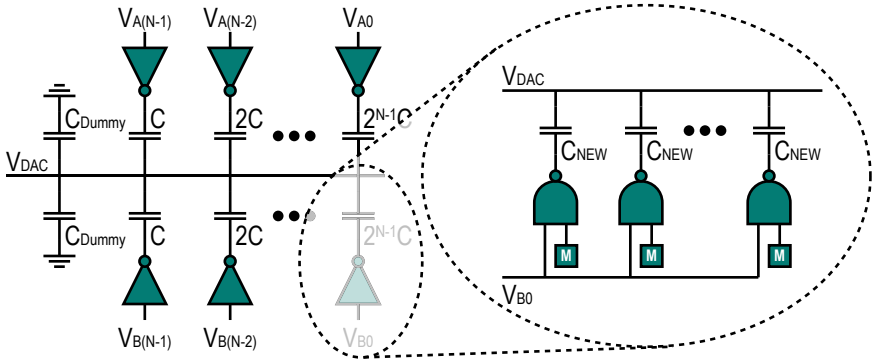

Figure 4-6, Each capacitor in the array driven by an inverter will be replaced by a group of capacitors each driven by NAND-gates

For the calibration technique the split capacitor architecture is adjusted as illustrated in Figure 4-6. Each capacitor in the array is replaced by a group of capacitors. Each capacitor in such a group will be driven by a NAND-gate instead of an inverter. One input of each NAND-gate is connected to a memory cell which determines if the control signal to the capacitor is blocked or not.
The capacitors in a group which control signals are blocked (passive part) will act as part of the large dummy capacitor. The capacitors in a group which signals are not blocked (active part) will act together as the replacement of the original capacitor.
The contents of the memory cells is determined by a calibration procedure. This procedure will select one or more capacitors out of a group (depending on the capacitor sizes in a group) as active part. The selected active part will form the best matched replacement for the original capacitor.
The number of capacitors inside each group and the size of each capacitor will be determined by the technology (mismatch parameters), the minimum input capacitance of the ADC (now limited by noise) and the linearity requirements of the DAC.

Calibration
Since capacitor mismatch is a constant error, it is enough to calibrate the DAC only once after fabrication. During the calibration procedure the size of each capacitor in a group should be determined in order to decide which capacitors should participate to replace the original capacitor.
The size of each capacitor can be determined very accurately by using statistics and the noise already present in the ADC causing digital noise at the output (present in the LSB bit(s) of the ADC). The noise is normal distributed around an average value. This average can be determined very accurately by measuring the noise at the output over a longer amount of time. In this way the capacitors sizes can be measured, starting with the smallest capacitors which size information is needed to determine the size of the larger capacitors. Instead of exact sizes, the outcome of the measurement are capacitor sizes expressed in ratios between each other. This ratio information is enough to acquire the best matching sum of capacitors in each group.
The calibration can even be performed when the comparator has an offset. Before the calibration starts, the offset can be compensated by subtracting it from the sample with the non-calibrated DAC. This can be done by a binary search, reducing the offset to a maximum of approximately 1 LSB (bringing the noise towards the decision point of the comparator).
After the calibration is done, accurate information is available about the capacitors used to compensate the offset. This gives the calibrator access to accurate information about the offset of the comparator (needed for the offset compensation in the comparator 5.1.3).
The output of the calibration procedure will be an static array of bits, which will fill the memory cells before all the NAND-gates driving the capacitors as in Figure 4-6. An efficient algorithm for the calibration should be developed to shorten the calibration time.

4.2 IMPLEMENTATION

An overview of the implemented charge redistribution DAC with all the improvements is given in Figure 4-7.

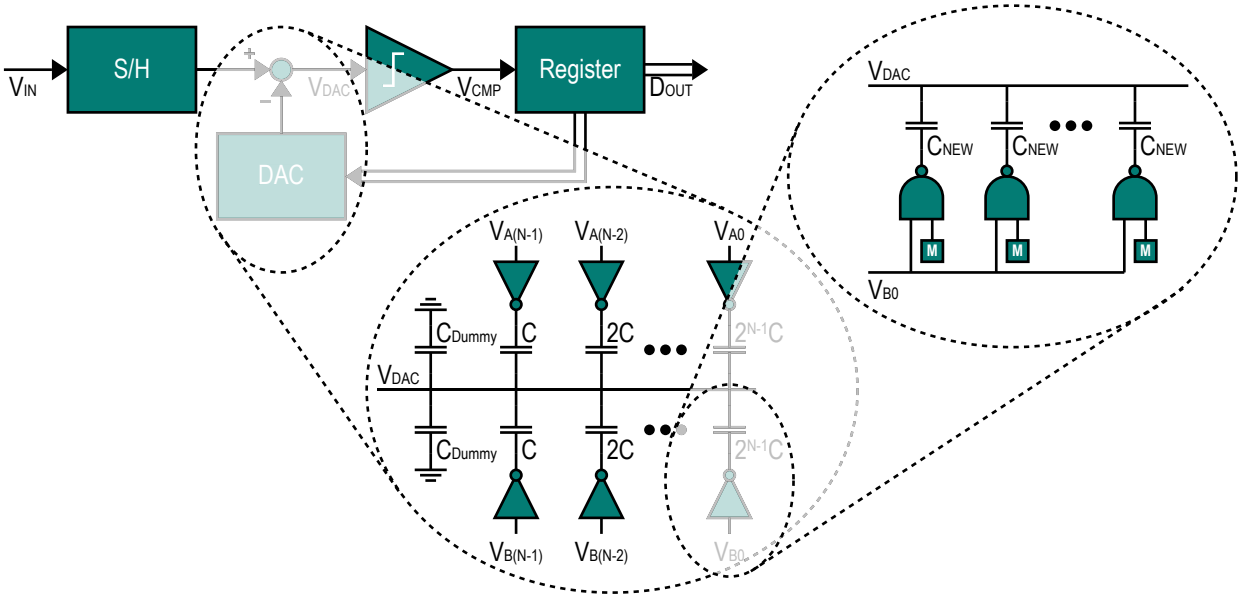

Figure 4-7, The complete ADC, the split-capacitor array, and a capacitor replacement

In this section the amount of capacitors and their sizes will be determined. In the first part the ratio between the size of the total DAC capacitance and a single unit capacitor is calculated. This is done with the specifications of the ADC's input range. After this the exact size of a single unit capacitor will be calculated, which is limited by the noise requirement of the DAC. The information is enough to build a normal split capacitor architecture.
For the calibration, the capacitors are replaced by groups of capacitors. The specifications of these groups, will be determined by the linearity requirements of the ADC. The amount of capacitors in each group and the size of each capacitor in a group will be calculated in the second part.
In the third part the NAND-gate driving each capacitor will be discussed shortly.

4.2.1 CAPACITORS SIZES FOR ORIGINAL DAC

The ADC will have a resolution of 7 bit (ADC requirements can be found in chapter 3). With the split capacitor architecture applied, 12 capacitors and 1 (combined) dummy capacitor are needed in the DAC. When the supply voltage (1 V) and the input range of ADC (63.2 mV differential) are known, the ratio between a single unit capacitor and the total DAC capacitance can be calculated.

$$\frac{C_{UNIT}}{C_{DAC}} = \frac{V_{diff\_input\_range}/2}{V_{supply}\,2^N} \approx \frac{1}{4050}$$

The ADC design will be implemented with a differential input, therefore the differential input range is divided by a factor of two to get the single input range. As can be seen the total capacitance of the DAC will be 4050C (unit capacitors).
The minimum total capacitance is limited by the kT/C noise as mentioned earlier. A certain level of random noise in the ADC is allowed and even needed for dithering. The total (differential) input referred noise wanted is around 0.64 LSB bit, which corresponds to approximately 223 µV rms [5]. The main noise contributors in the ADC are the sample switch, the comparator and the kT/C noise from the DAC. Now a trade-off arises between the places

where noise should be produced. Since the focus of the ADC is on low power consumption, the consumption should be the guide in this trade-off to find an optimum. Lower kT/C noise in the DAC means larger capacitors which increases the power consumption. Lower noise produced in the comparator means also an increase of the power consumption. Literature shows that the comparator will be the expected dominant power consumer [6]. Leaving most of the noise contribution to the comparator a unit capacitor size of 336.2 aF is chosen, which is the minimum capacitor size in the 65 nm technology used for the ADC design (1 µm x 1µm).
With the size of a unit capacitor known, the total capacitance can be calculated. The thermal noise in the DAC, as well as the input referred noise and the power consumption for a single conversion of the DAC can be calculated/approximated afterwards.

$$C_{DAC} = M_{unit}\, C_{unit} \approx 1.36\, pF$$

$$v_{n\_DAC} = \sqrt{k_B T / C_{DAC}} \approx 55.15\, \mu V$$

$$v_{n\_input} = v_{n\_DAC}\sqrt{2} \approx 78.00\, \mu V$$

$$E_{conversion} = 2\sum_{i=0}^{5} \frac{\left(C_{total} - C_{unit}\, 2^i\right) C_{unit}\, 2^i}{C_{total}} {V_{supply}}^2 \approx 42.14\, fJ$$

Where M_{unit} is representing the number of unit capacitors in the DAC (4050). Because of the differential implementation of the ADC, the noise has to be multiplied by √2 to acquire the input referred noise. Also the energy consumption for a single conversion is multiplied by a factor of 2.
Table 4-1 gives an overview of the capacitor sizes of each capacitor in the array starting with the smallest capacitor. Note that capacitor with numbers 5-0 occur twice because of the symmetric structure in the split capacitor architecture.

Capacitor size in the split capacitor DAC								
Cap in array	5	4	3	2	1	0	Dummy	Total
Size in Unit Caps	1C	2C	4C	8C	16C	32C	3924C	4050C
Size in fF	0.34	0.67	1.34	2.69	5.38	10.76	1319.25	1361.61

Table 4-1, Capacitances of the capacitors in the 7-bit DAC array. Capacitors with numbers 5-0 represent the capacitors driven by the inverter, all of them are used twice in the split capacitor array.

4.2.2 CAPACITOR GROUPS

The capacitors and their inverter are replaced by capacitor groups driven by NAND-gates to implement the calibration. The number of capacitors in each group and the size of the capacitors in a group, are calculated in this part. They are determined by the linearity requirements of the ADC.
The linearity of an ADC is expressed in the differential non-linearity (DNL) and the integral non-linearity (INL). The error between each quantization level and the ideal quantization level is given by the INL. The DNL indicates the error between each quantization step and an ideal quantization step. Both are illustrated in Figure 4-8.

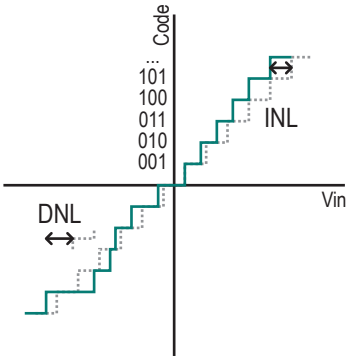

Figure 4-8, Differential non-linearity and integral non-linearity

Mismatch between the capacitors in the DAC will cause these non-linearities. The integral non-linearity will cause harmonic distortion at the output of the ADC. For example an INL with a second order shape will result in second order distortion in the output.
Because our ADC will be implemented as a differential design, the 3rd harmonic will in most cases be the largest distortion component. As described in chapter 3 the SFDR of the ADC should be at least 70 dB. So the 3rd order harmonic should be at least 70 dB lower than the input signal. At first the maximum allowed INL will be determined to acquire the 70 dB SFDR. With the INL requirements known, the number of capacitors in each capacitor group and their size will be determined.

The maximum allowed 3rd order deviation in the INL will be calculated by looking at the Taylor expansion of the ADC output.

$$y_{output}\ (t) = \propto_1 x(t) + \propto_3 x^3(t)$$

Taking the input

$$x_{input}\ (t) = Acos(\omega t)$$

Leads to the following output

$$y_{output}\ (t) = \propto_1 Acos(\omega t) + \propto_3 A^3 cos^3(\omega t)$$

$$y_{output}\ (t) = \propto_1 Acos(\omega t) + \frac{\propto_3 A^3}{4}[3cos(\omega t) + cos(3\omega t)]$$

The ratio between the amplitudes of the 3rd and 1st harmonic is given by

$$HD_{3,\%} = \frac{(\propto_3 A^3/4)^2}{(\propto_1 A + 3 \propto_3 A^3/4)^2} \cdot 100(\%)$$

As can be seen only the 1st and 3rd order terms are used, and the 2nd and higher order terms are ignored because they are not of interest. Taking an amplitude of 1 (A = 1, full input scale of the ADC) and a gain of 1 (α_1 = 1) leads to a maximum 3rd order harmonic distortion of approximately

$$HD_{3,\%} \approx (\propto_3/4)^2 \cdot 100(\%)$$

in dB

$$HD_{3,dB} \approx 10 \cdot log((\propto_3/4)^2)$$

$$\propto_3 \approx 4\sqrt{10^{HD_{3,dB}/10}}$$

The 3rd harmonic is caused by 3rd order deviation in the INL. The linear part of the quantization curve is given by

$$y_{linear} = \frac{\alpha_1 x_{max} + \alpha_3 x^3{}_{max}}{x_{max}} x = (\alpha_1 + \alpha_3 x^2{}_{max})x$$

The slope of the curve is calculated using the output at maximum input range (which is the sum of the linear and 3rd order component) divided by the input. The y_{linear} at $x = x_{max}$ represents the maximal digital output (all ones). The minimal digital output (all zeros) is represented by y_{linear} at $x = -x_{max}$. The difference with this linear line is the INL and is caused by the 3rd order deviation given by

$$y_{3rd} = \alpha_1 x + \alpha_3 x^3$$

The difference (taking $x_{max} = 1$ and $\alpha_1 = 1$)

$$\Delta y = y_{3rd} - y_{linear} = \alpha_3 x^3 - \alpha_3 x$$

The maximum INL can be found by taking the derivative, resulting in equation for Δy as function of α_3

$$0 = \frac{\partial \Delta y}{\partial x} = \alpha_3(3x^2 - 1), x = \frac{1}{\sqrt{3}}$$

$$\Delta y = \frac{2\alpha_3}{3\sqrt{3}}$$

The input range is approximated which leads to the maximum allowed 3rd order INL for 70 dB SFDR. Just like with the calculation of the maximum allowed 3rd order distortion, the maximum input scale is taken applying $A = x_{max} = 1$, leading to the 3rd order distortion.

$$y_{peak-peak} = 2A(\alpha_1 + \alpha_3) \approx 2$$

$$INL_3 = \frac{2^N \Delta y}{y_{peak-peak}} = \frac{2^7 \alpha_3}{3\sqrt{3}} = \frac{2^7 4\sqrt{10^{HD_{3,dB}/10}}}{3\sqrt{3}} \approx 0.031\ LSB$$

This maximum allowed INL gives a restriction to the matching of the capacitors in the DAC. Simulations show that the used unit capacitor of 336.2 aF has a standard deviation of 4.81 aF in the 65 nm technology. When no calibration technique is applied and a normal split capacitor array is present, the maximum INL will be calculated like shown below.

First average capacitance and the standard deviation of each capacitor in the array is calculated using

$$\mu_{cap} = \mu_{unit}\, n_{unit\_caps}$$

$$\sigma_{cap} = \sigma_{unit} \sqrt{n_{unit\_caps}}$$

The results are shown in Table 4-2.

Capacitor size in the split capacitor DAC							
Cap in array	5	4	3	2	1	0	Total
Size in Unit Caps	1C	2C	4C	8C	16C	32C	4050C
Mean Capacitance μ (fF)	0.336	0.672	1.345	2.690	5.379	10.76	1361.61
Standard Deviation σ (aF)	4.813	6.806	9.625	13.61	19.25	27.22	306.27

Table 4-2, Mean capacitances and standard deviation of the capacitors in a standard split capacitor DAC.

Now the average voltage step and their standard deviation can be calculated for each capacitor in the array using

$$V_{step\_mean} = \frac{C_{mean}}{C_{total\_mean}} V_{supply}$$

$$V_{step\_std} = \sqrt{\left(\frac{C_{mean}}{C_{std}}\right)^2 + \left(\frac{C_{total\_mean}}{C_{total\_std}}\right)^2} \frac{C_{mean}}{C_{total\_mean}} V_{supply}$$

The results are shown in Table 4-3.

Capacitor size in the split capacitor DAC						
Cap in array	5	4	3	2	1	0
Size in Unit Caps	1C	2C	4C	8C	16C	32C
Mean Voltage Step (mV)	0.247	0.494	0.988	1.975	3.951	7.901
Standard Deviation (μV)	3.535	5.000	7.073	10.01	14.17	20.07

Table 4-3, Mean voltage step and its standard deviation for each capacitor in a single DAC

The 7 bit ADC will have 2^7-1 quantization levels. The levels with the largest uncertainty will be the uneven ones, where half of the capacitors in the split-capacitor array are in use. It will be assumed (to simplify calculation) that these levels will determine the largest INL. The standard deviation of the INL at these levels will be

$$V_{INL\_std\_diff} = V_{INL\_std}\sqrt{2} = \sqrt{\sum_{i=0}^{5} {V_{step\_std\_i}}^2} \approx 39.78\,\mu V \approx 8.06E^{-2}\,LSB$$

For one conversion 64 of these levels will be present. For a 3σ-design the maximal expected INL can be calculated solving d from (μ = 0 and σ is determined above)

$$P(-3\sigma < X < 3\sigma) = \sqrt[64]{\int_{-3\sigma}^{3\sigma} \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2} dx} = \int_{-d}^{d} \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2} dx$$

$$d \approx 162.9\,\mu V \approx 0.3299\,LSB$$

Offset in the ADC will not introduce harmonics affecting the SFDR, so the INL curve can be adjusted to 'best fit' around zero. This is done by subtracting the mean value of the maximum and minimum INL in the curve from the complete curve. Note that the gain of the ADC in not adjusted. For a 3σ-design the maximal expected INL can now be calculated solving d from

$$P(-3\sigma < X < 3\sigma) = \sqrt[64\ nCr\ 2]{\int_{-3\sigma}^{3\sigma} \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2} dx} = \int_{-d/2}^{d/2} \frac{1}{\sqrt{2}\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)^2} dx$$

$$d \approx 136.0\,\mu V \approx 0.2753\,LSB$$

The 0.28 LSB is larger than the maximum allowed value of 0.031 LSB. The calibration is applied to increase the matching and lower the maximal INL.

The capacitors in the original DAC are each replaced by a group of capacitors. The calibration can choose capacitors in the group which will be used as a replacement of the original capacitor. The number of options where the calibration procedure can choose from is determined by the number of capacitors in each group and the size of each capacitor in the group.
As can be seen in Table 4-3 the largest contributors to the INL are the largest capacitors in the array with a size of 32 unit capacitors (32C). This capacitor will be taken as example. The 32C capacitor will be replaced by a group of 12 capacitors with each a size of 8C. The calibration procedure can choose 4 of these 8C capacitors which together will form the 32C capacitor. This creates 495 possibilities (binomial coefficient of 12 and 4) for the calibration procedure to make the 32C capacitor. Decreasing the standard deviation of the capacitor with a factor $\sqrt{(495)}$. This is done for all capacitors in the array and the results are shown in Table 4-4. As can be seen only multiples of the unit capacitor are used and the largest capacitors are replaced by groups having most selection possibilities.

The original capacitors and the specifications of the capacitor group replacing them						
Cap in array	5	4	3	2	1	0
Original cap size	1C	2C	4C	8C	16C	32C
Number of caps in group	8	8	8	8	12	12
Size of each cap	1C	1C	1C	2C	4C	8C
Possibilities to choose from	8	28	70	70	495	495
	Results of calibration					
Mean Voltage Step (mV)	0.247	0.494	0.988	1.975	3.951	7.901
Standard deviation (μV)	1.566	0.952	0.874	1.276	1.093	1.993

Table 4-4, Specifications of the capacitors in the original array and the results after they are replaced with capacitor groups

The group and capacitor sizes are chosen in such a way that the maximum expected INL after calibration for a 3σ-design will be 0.03098 LSB (with the best fit method applied). This value meets the required value of 0.031 LSB. Larger groups are not required for the specification. Simulation results in section 4.3.1 verify this. With the number capacitors and their sizes know, a short look will be taken at the NAND-gates driving the capacitors.

4.2.3 DRIVING CIRCUITRY

Each capacitor in the DAC will be driven by a NAND-gate. The capacitor sizes which will vary from 1C, 2C, 4C and 8C. The NAND-gate used is shown in Figure 4-9. One of the inputs is static (determined by calibration). The transistors used for this input have a high threshold voltage to prevent leakage.

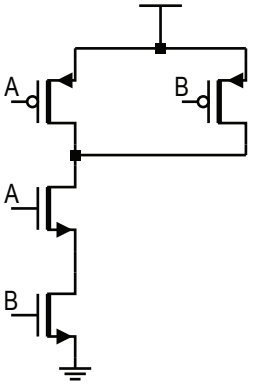

Figure 4-9, NAND-gate driving capacitors

4.3 PERFORMANCE

The DAC is built in a 65 nm ST-process, it is simulated and the performance is discussed in this section.

4.3.1 LINEARITY

The linearity is one of the most important properties of the developed ADC. The harmonics present at the output of the ADC are reduced with a lower INL. The calibration technique developed is capable of reducing the INL and DNL of the converter to a level needed for operation. In the previous section the needed capacitances in the DAC are calculated and here the test results are presented and compared with the calculated values.
The DNL and INL of the ADC are simulated with a Monte Carlo simulation of 5000 runs. In the simulation, all the circuitry around the DAC is replaced by ideal components. In Figure 4-10 the DNL of the ADC is plotted before and after the calibration is applied. The measured standard deviation of the largest DNL (equal to the standard deviation of the INL) before calibration is 8.12E-2 LSB which corresponds approximately with the calculated value of 8.06E-2 LSB. The standard deviation of the largest DNL after calibration is 0.50E-2 LSB.

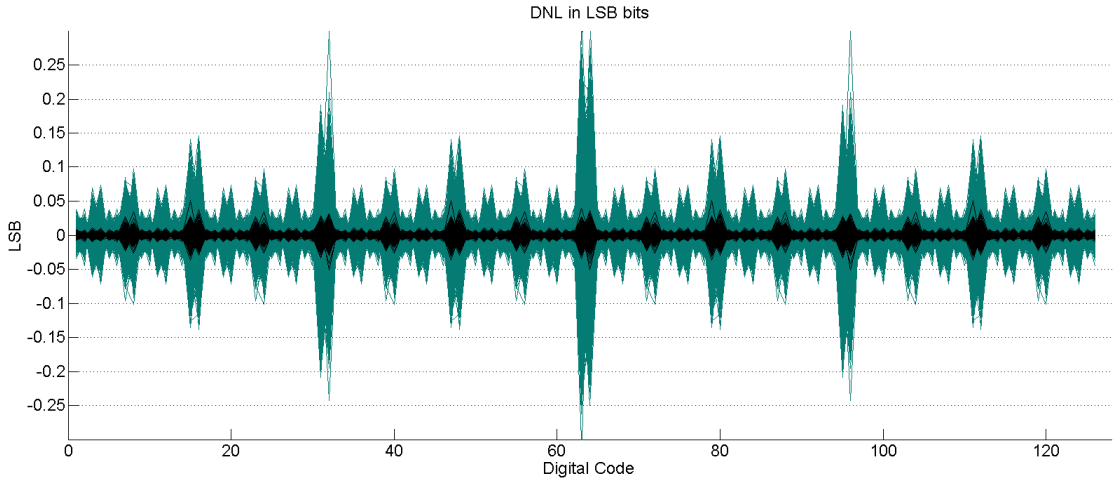

Figure 4-10, The DNL of the ADC in LSB bits (green is the non calibrated ADC, black is the calibrated ADC)

The INL and the ‘best fit‘ INL before and after calibration are shown in Figure 4-11 and Figure 4-12. The maximum ‘best fit‘ INL is 0.27 LSB without calibration. With calibration applied the maximum INL is 3.06E-2 LSB. Both correspond approximately with the expected values calculated before (0.28 LSB and 3.098E-2).

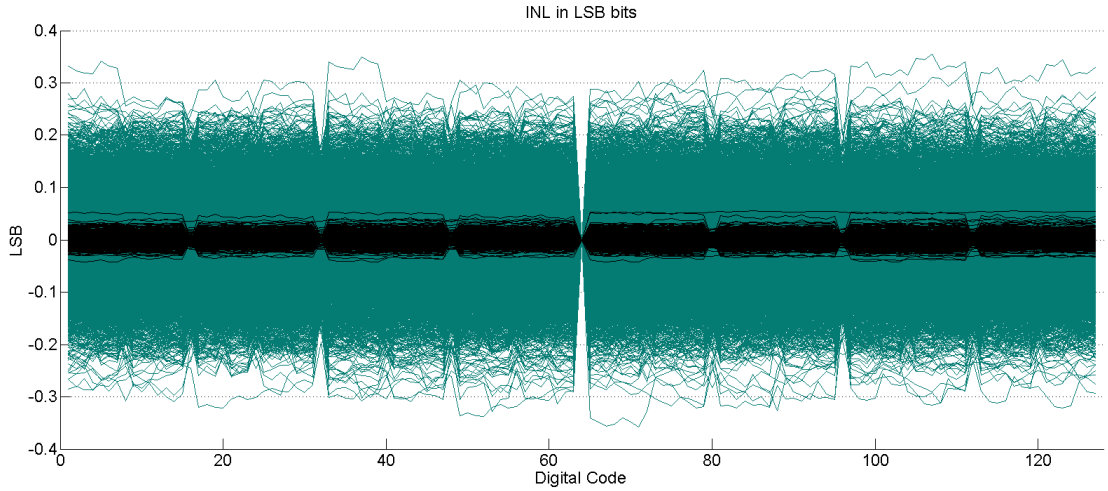

Figure 4-11, INL without best fit method applied (green not calibrated, black calibrated)

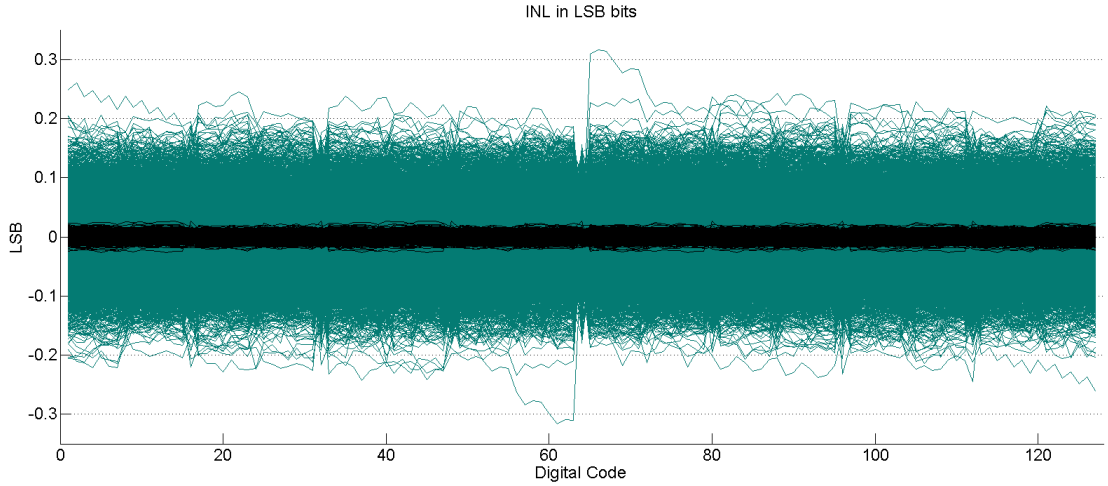

Figure 4-12, INL with best fit method applied (green not calibrated, black calibrated

To test if the required SFDR is achieved a sinus is applied at the input of the ADC and a fast Fourier transform is applied on the output and shown in Figure 4-13. The largest harmonic (3rd order) before and after calibration are measured. Before calibration the difference with input was 65 dB after calibration it is 72 dB meeting the requirement of 70 dB.

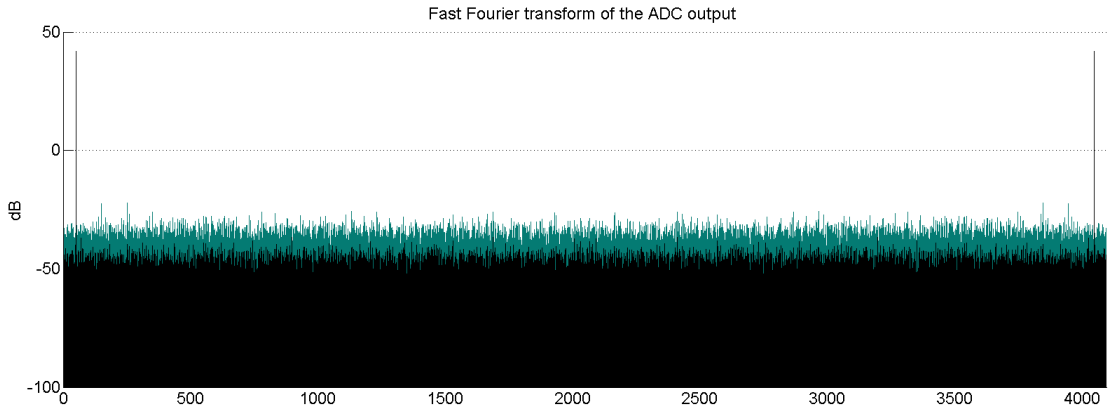

Figure 4-13, Fast Fourier transform of the ADC output

4.3.2 NOISE

The input referred noise of the ADC caused by the capacitor array corresponds with the calculated value of v_n = 78 µV approximately 0.158 LSB.

4.3.3 OFFSET AND GAIN

The standard deviation of the offset from 0 is increased because of the ‘best fit‘ method applied to the INL curve. The measured standard deviation of the offset is 0.0527 LSB for the non-calibrated ADC and 0.0033 LSB for the calibrated ADC.
This offset will be added to the offset which will be introduced by the comparator. In the comparator an offset reduction circuit will be present, which will be calibrated and will reduce the offset of the ADC, this will include the offset introduced by the DAC. The comparator is described in chapter 5.

4.3.4 POWER CONSUMPTION AND SPEED

The power consumption is simulated and shown in Figure 4-14.

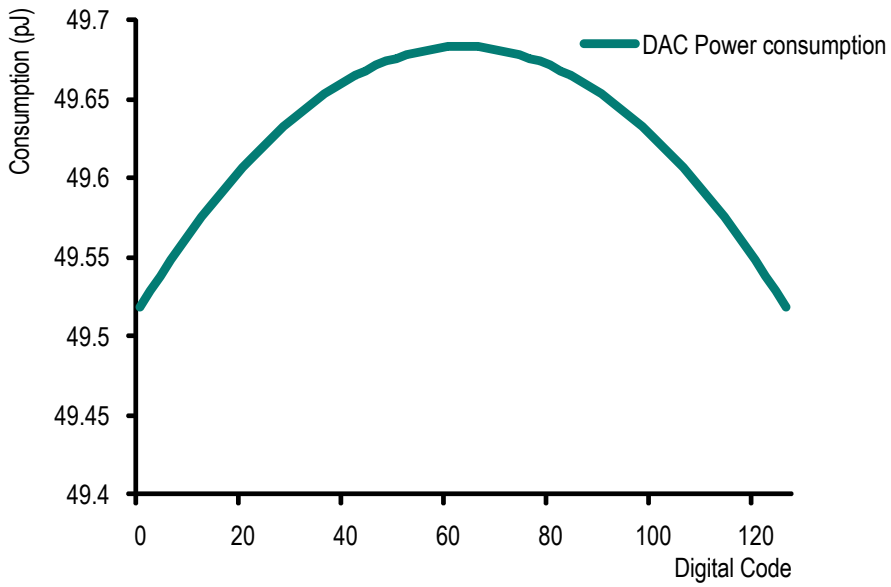

Figure 4-14, Power consumption of the DAC for one conversion as function of the ADC’s output

The average power consumption is 49.63 pJ per conversion.

This includes the power consumed for charging the DAC's capacitors as well as the driving NAND-gates. The charging speed of capacitors in the DAC is also simulated and the results are shown in Figure 4-15.

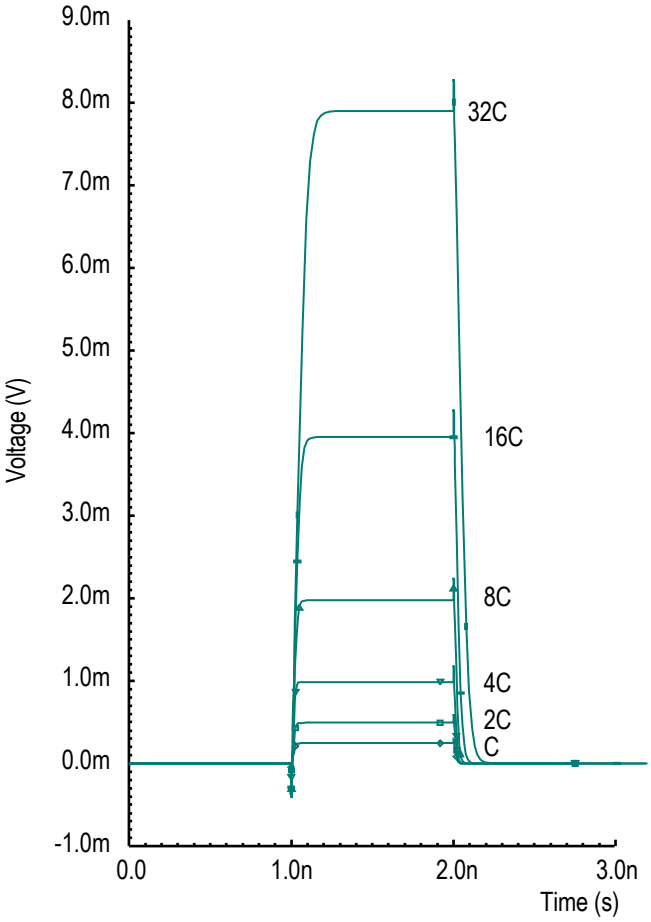

Figure 4-15, Output response of the DAC as result of switching a capacitor in the array. The size of the switched capacitor is indicated.

As can be seen the response of the DAC is within 0.2 ns for charging and discharging. In chapter 5 the comparator will be described which has a reset time of 1.5 ns. The DAC's output should settle during this time. The error in the output should at least be smaller than the 9-bit accuracy needed for the application. The 9-bit requirement comes from [5] and is acquired by the use of dithering as discussed in chapter 3. After 1.5 ns the error is << 1/16 LSB, so the DAC is fast enough. More about the timing in the ADC can be found in chapter 7 where the control logic is described.

4.4 CONCLUSIONS

In this chapter the DAC part of the ADC was treated. The DAC was simulated and the results were compared to the requirements given to the DAC. A charge redistribution DAC is implemented and three improvements were applied.
First of all a split capacitor architecture is applied to reduce the DAC's power consumption. The power consumption of the DAC is approximately 49.63 pJ per conversion. This consumption can be reduced further by reducing the size of an unit capacitor. This reduces the DAC's array capacitance which is limited by the noise requirement of the ADC.
The second improvement applied is the output range of the DAC, and therefore the input range of the ADC. It is decreased to approximately 63.2 mV, by placing a larger dummy capacitor in the DAC. The value meets the requirement of 63 mV, which was set in chapter 3.
The last improvement applied is a newly introduced calibration architecture and algorithm increasing the linearity by decreasing the INL from 0.27 LSB to 3.06e-2 LSB. It is important to note that the calibration architecture was determined with the use of the specification of the spectrum analyzer. It is possible to increase the linearity further by increasing the number of capacitors in a calibration group. This will be possible at the cost of a slight increase in power consumption (more NAND-gates are driven in parallel) and a longer calibration procedure (more capacitor sizes need to be determined).

THE COMPARATOR

The complete ADC architecture is shown in Figure 5-1. The comparator part is highlighted and will be treated in this chapter. The comparator is used to compare the sampled input voltage which is adjusted by the DAC discussed in chapter 4. As with the rest of the ADC design, the primary focus during the comparator design will be on low power consumption.

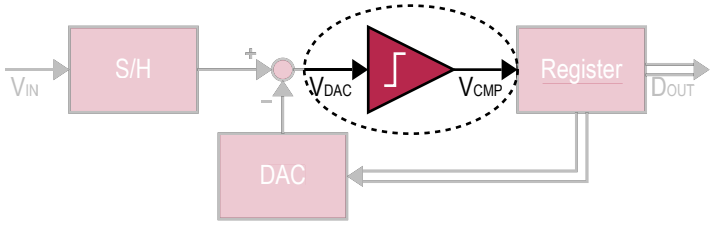

Figure 5-1, The comparator will be treated in this chapter

In the first section of this chapter the architecture of the used comparator will be discussed. The small input range of the ADC led to the need of a new offset compensation method for the comparator, which is introduced in the last part of this first section. In the second section, the comparator elements are dimensioned in order to meet the requirements for operation (noise, offset, speed etc.). In the third section the comparator is simulated and the performance is discussed.

5.1 THE LATCHED COMPARATOR

The task of the comparator is comparing its input signals and give the result as a digital output signal. In Figure 5-2 the different elements of the used comparator are shown. A two stage comparator is used consisting of an amplifier stage and a latch circuit. At the input of the comparator an offset compensation circuit will be present, needed for proper operation of the ADC. The architecture and operation of the two stage comparator are discussed first, followed by the new offset compensation method.

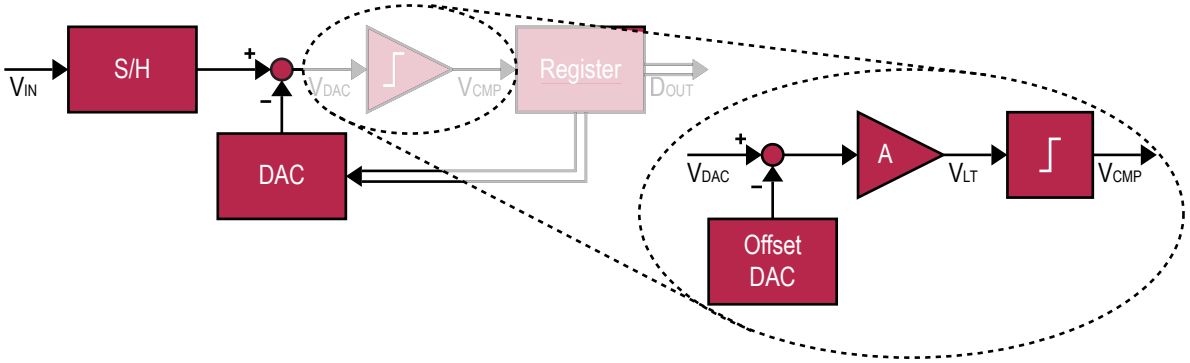

Figure 5-2, Comparator parts as used in the ADC

5.1.1 ARCHITECTURE

There exist two types of comparators, continuous and clocked comparators. Continuous comparators measure their inputs continuously and update their output quickly when their inputs change. An example of such a comparator is a huge gain amplifier with a clipping output. Clocked comparators make only a decision when they are triggered by an external clock signal. This results most of the time in higher accuracy in combination with a lower power consumption. Therefore clocked comparators are commonly used in ADCs, where there is no need for continuous comparison.
Often latched comparators are used consisting of a latch circuit with strong positive feedback. The latch is brought into a metastable position during a reset phase of the comparator. The inputs of the comparator bring an unbalance in the circuit causing the latch to flip to one of its two stable positions.
The accuracy and the low-power consumption make such a latched comparator ideal for the use in our ADC. The comparator which will be used is shown in Figure 5-3. This two stage latched comparator is selected for its energy efficient operation. It is also used in [6] and has some similarities with the comparator used in [7]. The focus in [7] is on speed rather than low power consumption. In [6] the focus is also on low power consumption. Nevertheless the small input range, noise requirement and higher speed of our ADC lead to extra requirements (discussed in 5.2).

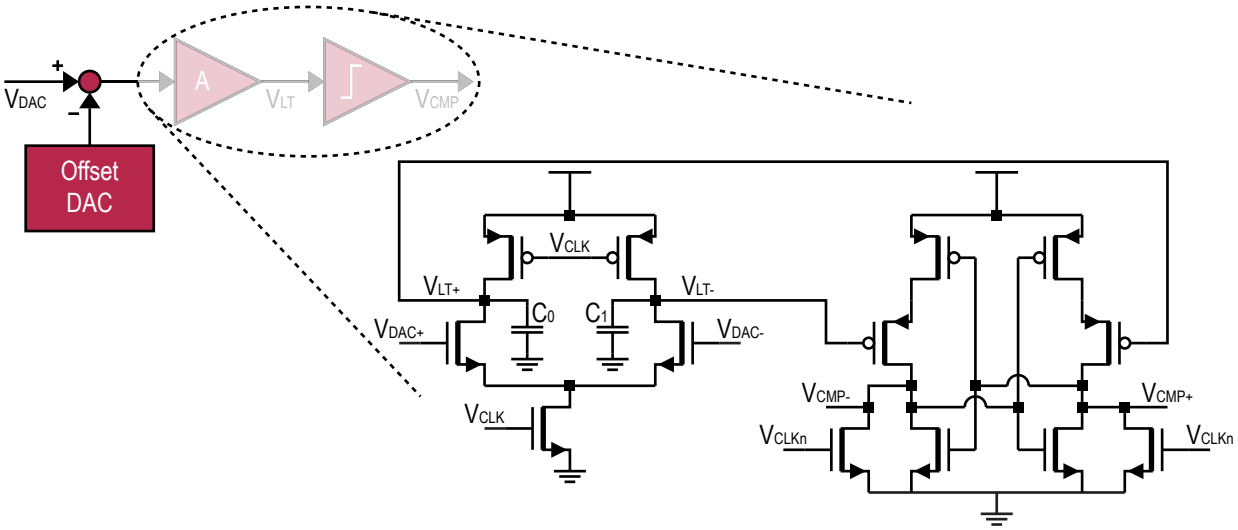

Figure 5-3, The architecture of the two-stage comparator

5.1.2 OPERATION

The two stage comparator is shown in Figure 5-3. The first stage consists of a differential input pair which will discharge two capacitors during the comparison phase of the comparator, creating a voltage amplification with V_{LT}+ and V_{LT}- as differential output. The second stage consists of voltage amplifier and a positive feedback amplifier (latch circuit) creating the differential rail-to-rail output voltage of the comparator.
In Figure 5-4 an example is given of the voltages and power usage in the comparator during one comparison. Before every comparison the comparator gets into the reset phase (V_{CLK} will be connected to GND and V_{CLKn} to VDD). All nodes are then pre-charged. The capacitors C_0 and C_1 are charged to VDD and the output nodes V_{CMP}+ and V_{CMP}- are connected to ground. After the reset, the comparator gets into the comparison phase (V_{CLK} is connected to VDD and V_{CLKn} to GND). In this phase the capacitors C_0 and C_1 are discharged by the input pair, amplifying the input voltage at the nodes V_{LT}+ and V_{LT}-. These nodes form the input of the second stage. When the threshold voltage of the input pair of the second stage is reached,

the voltage amplification in the second stage becomes dominant. After the threshold voltage of one of the NMOSTs in the latch is reached, the positive feedback in the second stage takes over and delivers the rail-to-rail output. As can be seen, virtually no power is consumed by the comparator once a decision is made, making the comparator very energy efficient.

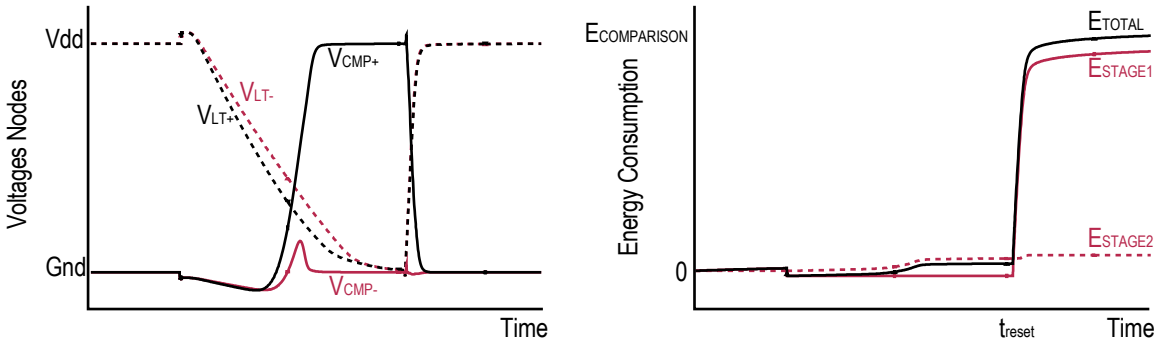

Figure 5-4, Example of one comparison of the comparator, left the output of the first stage (dashed) and output second stage (solid), right the energy consumption from each stage during the conversion. The increase in power consumption is at the time where the reset phase starts and the capacitors C_0 and C_1 are charged.

5.1.3 COMPENSATE FOR OFFSET

Mismatch between components of the comparator causes an offset at the output. This comparator offset will directly be translated into an offset for the complete ADC. For most applications the offset of an ADC is a minor issue. It will only affect the input range of the ADC and will not introduce extra harmonics or noise. For the comparator used in [6] the offset will vary between -30 mV to approximately 30 mV. The input range of the ADC is only affected by a couple of LSB bits, since the total input of the 10 bit ADC will vary from -1 V to 1 V. In the ADC needed for the spectrum analyzer the complete input range is only 63.2 mV. An offset of 30 mV will then heavily affect the operation of the ADC. For proper operation the offset needs to be reduced to one or a couple of LSB bits.
The offset of the comparator can be reduced by increasing the size of its components. Drawback of this is the increase in power consumption. Bringing the offset to an acceptable level for our ADC means a huge increase in power consumption. This is undesirable and therefore a new offset compensation method is introduced. It shows similarities with the calibration used for the DAC.

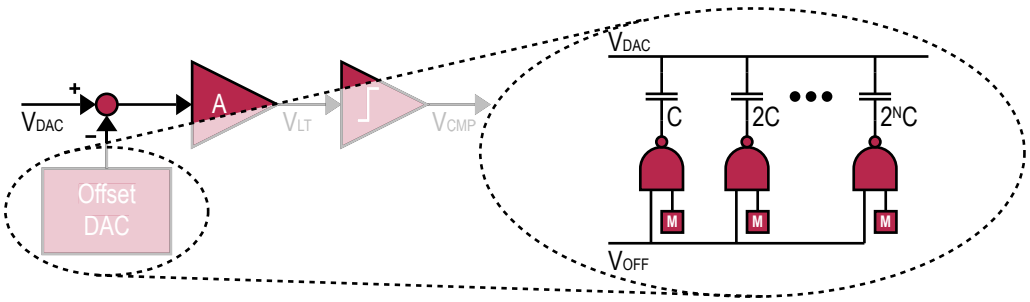

Figure 5-5, Offset reduction circuitry

The principle is shown in Figure 5-5. As can be seen, instead of reducing the offset of the comparator, the offset is compensated by subtracting a fixed voltage from the input. This will be done directly after the sample switch of the ADC is closed. The voltage is subtracted by an extra DAC, which forms an extension to the main DAC. It is possible to do this because the comparator is coupled directly to the output of the main DAC and thus to the common node of the capacitor array in the main DAC. The extra offset DAC is a simple weighted capacitor array. The capacitance used for this array is subtracted from the dummy

capacitance in the main DAC. In this way, the total input capacitance of the ADC stays equal as well as the voltage steps created by the main DAC. The capacitors are driven by a NAND gate and a memory cell which select the capacitors needed for compensation.
After fabrication the offset of the comparator is already measured as a result of the calibration procedure for the main DAC (see chapter 4). This offset will be approximated and stored digitally in the memory cells as shown in Figure 5-5. The maximum offset for a 3σ-design determines the maximal needed amount of capacitors in the DAC array, to be able to reduce the offset to one or a couple of LSB-bits.

5.2 IMPLEMENTATION

In this section each part of the comparator is treated in detail, leading to the design parameters. First the amplification stage of the comparator is described followed by the latch stage of the comparator. The offset compensation part is described last. The specifications for the comparator can be derived from the needed ADC specifications given in chapter 3.
The comparator should be able to perform at least 7 comparisons for one conversion at 40 MS/s. Therefore a comparator period of 3 ns is chosen (333 MHz). Furthermore noise used for dithering can be added by the comparator without exceeding the maximum total input referred noise of 0.64 bits (shared with the noise introduced by the DAC and the sample switch). The offset should be limited to a couple of bits for proper operation. This will be accomplished by the offset compensation DAC introduced in the previous section.

5.2.1 AMPLIFICATION STAGE

The amplification stage is the first stage of the comparator and is shown in Figure 5-6. The target of this stage is the amplification of the comparator input before it is further amplified by the second stage. A larger input voltage at the second stage, means that the latch gets faster to one of its stable positions. This results in a lower power consumption.

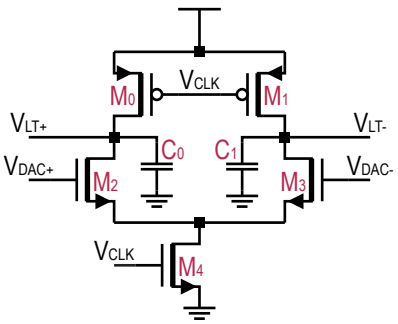

Figure 5-6, Amplifier stage of comparator

Reset and memory effect
During the reset phase of the comparator V_{CLK} is low. This means the tail transistor M_4 is closed and the capacitors C_0 and C_1 are charged to VDD by transistors M_0 and M_1. Possible residual charge from a previous measurement left on capacitors C_0 and C_1 give them a different starting voltage before they are being charged. Therefore the on-resistance of transistors M_0 and M_1 should be able to charge both capacitors to VDD within 1.5 ns (reset phase) and with a minimal error (V_{memory} << 0.5 LSB).

$$V_{memory} = \frac{V_{\text{diff\_old}} \cdot \left(1 - e^{-t_{reset}/R_{mosfet\_on} C_0}\right)}{A}$$

Where V_{diff_old} is the worst case voltage difference left before reset, t_{reset} is the reset time and A is the amplification of the first stage which is calculated next.

Gain
After the reset phase V_{CLK} will become high, closing transistors M_0 and M_1 and opening the tail transistor M_4. From this point the capacitors C_0 and C_1 start discharging through the input pair formed by M_2 and M_3. The tail transistor and the input pair are dimensioned in such a way that the input pair will operate in weak inversion. In this way the input transistors achieve a low equivalent input noise (higher *gm* per current than in strong inversion) and the amplification stage becomes more power efficient.

The gain of the stage is determined by the size of the capacitors C_0 and C_1, the *gm* of the input pair and the time available to discharge the capacitors. The time available for amplifying the input (by discharging C_0 and C_1) starts after the reset phase and ends at the point where one of the capacitor voltages has reached the threshold voltage of an input transistor of the second stage.

The gain will be calculated as follows

$$A = \frac{gm_{mosfet} \cdot t_{discharge}}{C_0}$$

$$t_{discharge} \approx \frac{V_{\text{threshold\_2nd\_stage}} \cdot 2C_0}{I_{M4}}$$

For our design the gain of the 1st stage will be approximately 11.

Noise
The total noise produced in the ADC should be limited to 0.64 LSB (see chapter 3) in order to be useful for dithering. This noise limit is shared with the DAC and the sample switch of the ADC. The largest expected noise contributor in the comparator is the input pair of the amplification stage [6], followed by the capacitor noise on C_0 and C_1. Noise introduced in the second stage will be a minor contribution to the total input referred noise because of the amplification in the first and second stage, this noise will therefore be neglected.

The input equivalent noise of the input pair can be estimated with [6]

$$V_{n\_inputpair} = \sqrt{2} \sqrt{4 \cdot k \cdot T \cdot \frac{\gamma}{gm_{mosfet}} \cdot NBW}$$

Because the noise is integrated over an amount of time ($t_{discharge}$) the noise bandwidth is replaced with the effective noise bandwidth (NBW) according to [13][14]:

$$NBW = \frac{1}{2 \cdot t_{discharge}}$$

The input equivalent noise of the capacitors is estimated with

$$V_{n\_capacitor} = \frac{\sqrt{2}\sqrt{\frac{k \cdot T}{C}}}{A}$$

Where C represents the capacitance of C_0 and C_1.

The input referred noise for the largest noise contributors of our comparator is estimated as (gm = 110E-6 A/V, C_0 = 5.6 pF, $t_{discharge}$ = 0.8 ns):
Input referred input pair noise: ~434 uV
Input referred capacitor noise: ~54 uV

These values give just an indication of the ratio between the noise sources. It does not give the real input referred noise since the noise is integrated a second time in the second stage of the comparator. Because of this the bandwidth of the noise is reduced further leading to a lower input equivalent noise.
For an exact estimation the frequency dependent transfer function of the complete comparator is needed, making the calculation very complex. The values calculated above are sufficient for design.

Kickback
The gate capacitance of the input pair will give a kickback charge into the capacitance of the DAC during a comparison. This charge will influence the voltage present at the output of the DAC. The cause of this kickback charge are the capacitors of the first comparator stage (C_0 and C_1), which are being discharged. Another cause is the kickback charge from the second comparator stage which is injected into the capacitors of the first stage. After which it is injected by the input pair of the first stage into the DAC.
The amount of kickback charge depends on the input voltage of the comparator and the size of the components in the comparator causing the kickback charge. Since the ADC will be implemented in differential form, the kickback will not influence the outcome of a comparison (assuming perfectly matched components in the ADC). The kickback will mostly influence the common mode of the input signal. The input voltage dependence of the kickback will have influence on the input signal but will not change the outcome (it will just make the input voltage smaller).
When mismatch is present, kickback will introduce an offset for the comparator. This will be compensated with offset DAC described in section 5.2.3.
The memory effect of the kickback also create an error. This effect should be maximal when the maximal input signal is applied to the ADC. This will create the maximum error between the differential inputs of the comparator. The memory effect is simulated for 7 comparisons (number of comparisons during one ADC conversion). It shows that the memory effect of the kickback under these conditions is very small (~1 uV) so it will be neglected.

Mismatch
Component mismatch in the first stage of the comparator will contribute to the offset of the comparator. This offset will be determined during a calibration procedure after fabrication. During operation the offset will be compensated by the method described in 5.2.3.

Power consumption
The power consumed by the first stage is mainly determined by the size of capacitors C_0 and C_1. These capacitors are charged during the reset phase and are therefore kept as small as possible, limited by the noise requirements given earlier.

5.2.2 LATCH STAGE

The latch stage is the second stage of the comparator and is shown in Figure 5-7. Before each comparison the comparator gets a reset. During the reset phase the input nodes of the latch are connected to VDD by the first stage and the output capacitance of the latch is connected to ground by M_9 and M_{12}. The output capacitances are formed by the gate and parasitic capacitances of the transistors connected to these nodes.

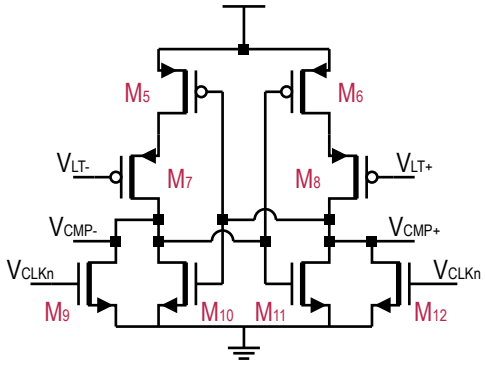

Figure 5-7, Latch stage of the comparator

Input pair

After the reset phase the amplifier stage begins to discharge the input nodes of the latch. This continuous until one of the inputs reaches the threshold voltage of the input pair in the latch (M_7 and M_8). As can be seen in the calculations of the amplifier stage, it is beneficial for the amplification as well as the noise figure to increase the discharging time in stage one. For this reason the transistors of the input pair of the latch are replaced by transistors with a higher threshold voltage (~0.45 V instead of ~0.34 V). The input pair amplifies the input by charging the gate capacitors of the transistors M_5, M_6, M_{10} and M_{11}. These MOSFETs form the positive feedback latch.

Noise

As mentioned in the description of the amplifier stage, the input referred noise introduced by the components of the latch will be a small compared to the first stage. This is caused by the amplification in the first stage combined with the voltage amplification by the input pair of the second stage. Therefore is noise contributors in the second stage will be neglected.

Mismatch

Mismatch between the components in the latch will have influence on the output. It will contribute to the offset of the comparator. This offset will be compensated for proper operation of the ADC as will be described in 5.2.3.

5.2.3 OFFSET COMPENSATION

The offset of the comparator is caused by the mismatch between the components in the comparator. As mentioned in the first section, offset of the comparator needs to be reduced to a maximum of several LSB bits for proper operation of the ADC.
During the calibration of the DAC the offset of the comparator is already determined (chapter 4). In our ADC this offset will be compensated by adjusting the inputs of the comparator. This will be done by an offset DAC which will subtract a fixed voltage each time after the sample switch of the ADC closes. This offset DAC is a simple binary weighted capacitor array (shown in Figure 5-8) which replaces a part of the dummy capacitances of the main DAC. In this way the total capacitances in the main DAC stay equal as well as the voltage steps made by these DAC.

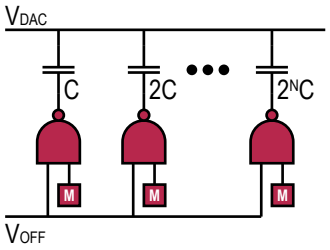

Figure 5-8, Offset compensation DAC

The amount of capacitors needed in the offset DAC (N) depends on the maximal expected offset of the comparator. The offset of the comparator is determined by a Monte Carlo simulation of the comparator with mismatch. The result is shown in Figure 5-9.

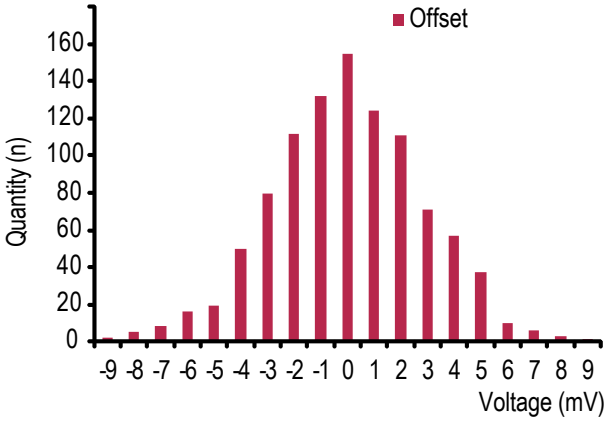

Figure 5-9, Offset comparator after Monte Carlo simulation (1000x)

The 3σ offset is 8.56 mV. This means the needed amount of capacitors in the array is N=5. According to

$$\frac{V_{\max offset}}{V_{LSB}} = 2^N$$

This enables the calibration to handle offsets up to 15 mV. Note that the offset DAC can be used for subtracting as well as adding voltages depending on the state of the DAC during the sampling phase of the ADC.

Power consumption

The extra power consumption for compensating a 15 mV offset can be calculated with the equation from chapter 4.2.1, taking C_{total} = n * C_{unit}. Where n = 4050C and C_{unit} = 336.2 aF (equal to the capacitances in the main DAC as given in Table 4-1).

$$E_{conversion} = 2\sum_{i=0}^{4}\frac{\left(C_{total} - C_{unit}\,2^{i}\right)C_{unit}\,2^{i}}{C_{total}}V_{supply}{}^{2} \approx 20.79\,fJ$$

This extra power consumption is small compared to one comparator comparison (~80 fJ, see 5.3) and very small compared to a comparator with less than ~500 µV offset (1 LSB of our ADC) designed by area upscaling.

To bring for instance the 8.56 mV offset towards 500 µV will require approximately 300 comparators in parallel (8.56 * √300 ≈ 500 µV) leading to a power consumption of 172.2 pF per ADC conversion (see chapter 5.3.5 about the power consumption of the comparator).

5.3 PERFORMANCE

The comparator is built in a 65 nm ST process and simulated. The results are shown in this section.

5.3.1 NOISE

The noise of a latched comparator is difficult to simulate as mentioned in [4]. To acquire accurate simulation results, our comparator is tested with transient simulations. With SPECTRE, noise can be added to a transient simulation. The outcome of the comparisons are monitored during a Monte Carlo simulation while giving the comparator a fixed voltage at the input. This is done for several applied voltages at the input of the comparator. Doing this gives the probability of a good comparison performed by the comparator as function of the input voltage. The probability reaches from 0.5 (where the input voltage is zero) to 1 where the input voltage exceeds the noise.
The probability density function of the input referred noise can be derived from this information. This is done by subtracting the probability of a good decision at an input voltage is from the probability of a good decision at the next measured input voltage. The result is the input referred noise distribution of the comparator as shown in Figure 5-10.

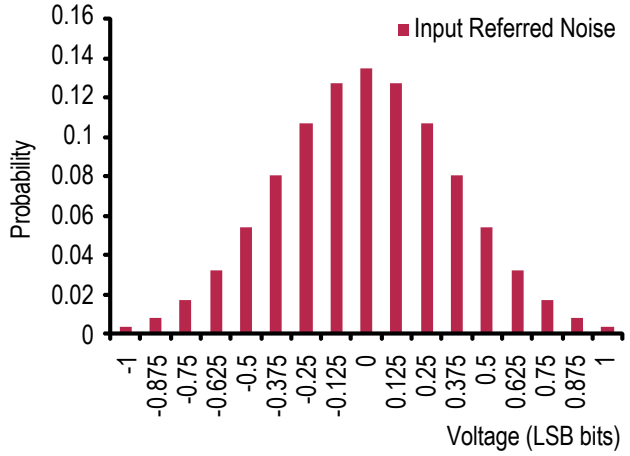

Figure 5-10, Input referred noise distribution of the comparator

As can be seen, the noise is normal distributed with a standard deviation of 182.84 µV which corresponds to 0.37 LSB. The simulations are performed with noise frequencies up to 100 GHz. So almost all the relevant noise is taken into account according to the low-pass filter characteristic of the first stage in the comparator.

Summing the input referred noise of the DAC together with the comparator leaves an allowed noise level for the sample switch.

$$\sigma_{sample} = \sqrt{\sigma_{allowed}{}^2 - \left(\sigma_{DAC}{}^2 + \sigma_{comparator}{}^2\right)} \approx 101\ \mu V$$

Where $\sigma_{allowed}$ is the allowed noise of 0.64 LSB (requirement described in chapter 3.3.3), $\sigma_{comparator}$ the comparator noise of 0.37 LSB and σ_{DAC} the DAC noise of 0.16 LSB (simulated in chapter 4.3.2).

5.3.2 SPEED AND GAIN AMPLIFIER STAGE

A periodic steady state analysis with different input voltages is used to test the speed performance of the comparator. The results are shown in Figure 5-11.

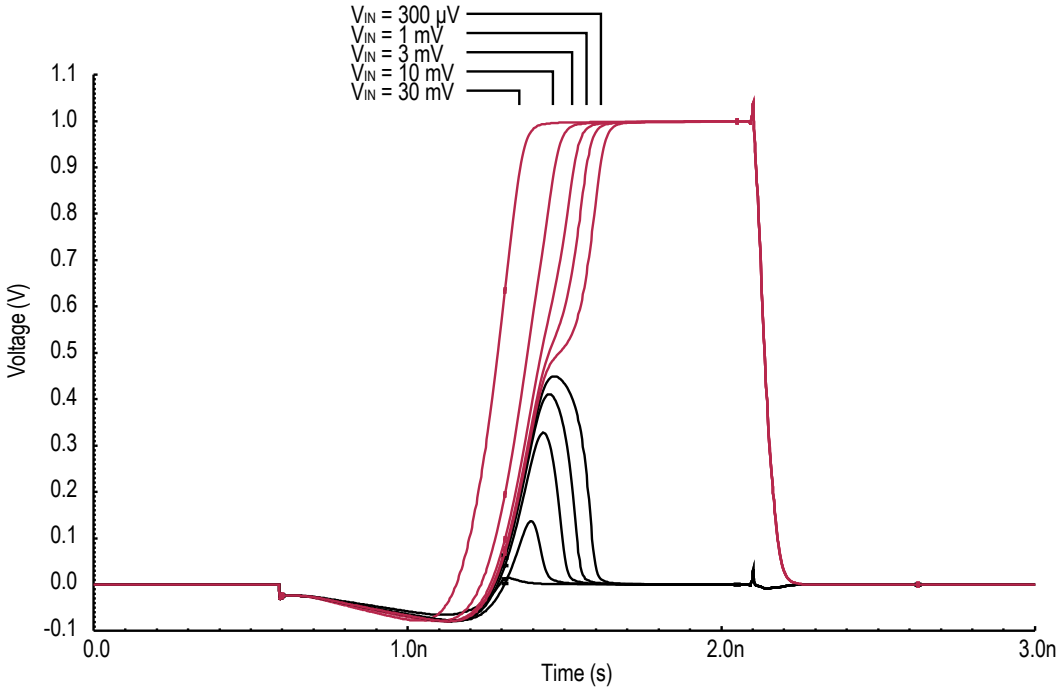

Figure 5-11, Outputs of the comparator as function of time for different input voltages

As can be seen even for small input variations (smaller than an LSB bit ~500 µV) the output of the comparator is settled in time before the reset phase of the comparator starts.
Also the gain of the first stage of the comparator is tested by using the periodic steady state (PSS) analysis. This is done to evaluate the time-dependant gain of the amplifier stage. It is simulated for different input voltages. The results are shown in Figure 5-12.

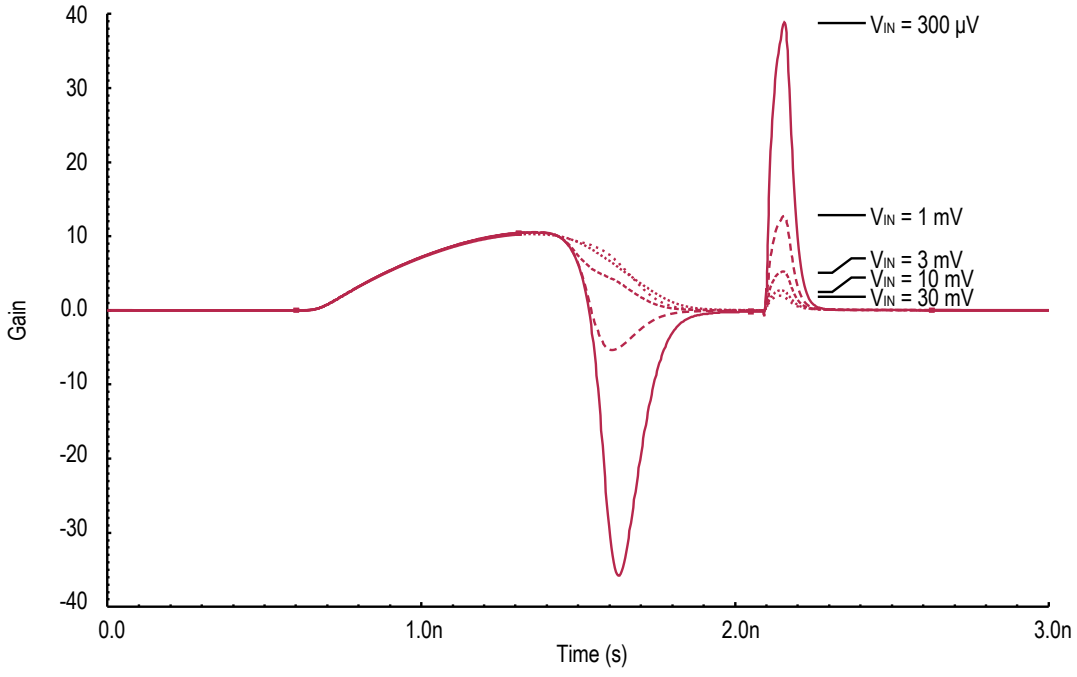

Figure 5-12, Gain of the amplifier stage of the comparator

At the point where the second stage starts amplifying (at approximately 1.4 ns) the gain of the amplifier stage corresponds with the calculated value A = 11. After this point the latch stage takes over and charge of the input transistors of the second stage is injected into the capacitors of the first stage. This explains the negative gain afterwards. The gain during the start of the reset after 2.1 ns can be neglected.

5.3.3 OFFSET

The offset of the comparator without the offset compensation is shown in already presented in Figure 5-9. The offset after calibration is reduced to a maximum of 500 µV (1 LSB + capacitor mismatch).

5.3.4 MEMORY EFFECT

The memory effect caused by residual charge at the capacitors in the amplifier stage of the comparator is tested by performing again a periodic steady state analysis with different input voltages. The voltage difference between the capacitors is determined shortly after the reset phase (indicated in Figure 5-13). This voltage is larger after a comparison with a larger input voltage. The voltage difference is approximately 210 µV after a comparison with an input voltage of 30 mV. Dividing this by an amplification factor of A=11 leads to a voltage difference of 19.1 µV, which is small enough for the required 9-bit accuracy of the ADC (<< 1/8 LSB bit). The 9-bit requirement comes from [5] and is acquired by the use of dithering as discussed in chapter 3.

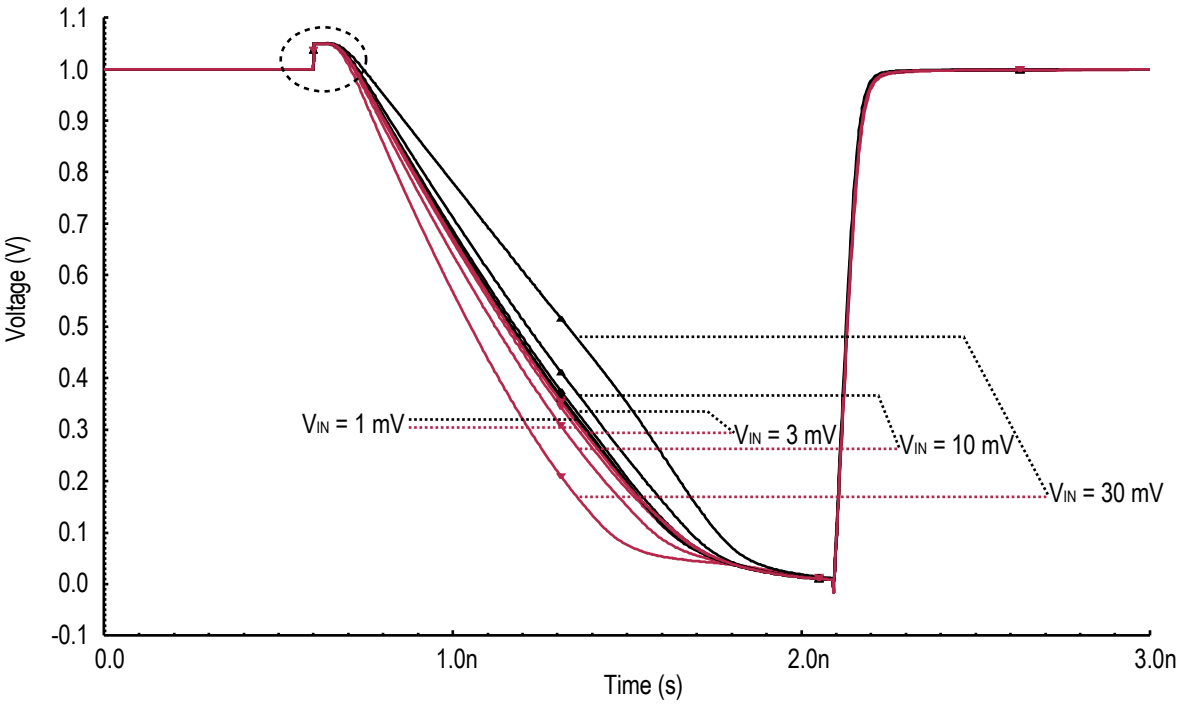

Figure 5-13, Capacitor voltages of the comparator's amplification stage for different input voltages, the circle indicates the moment after reset.

5.3.5 POWER CONSUMPTION

The power consumption of one conversion is shown in Figure 5-14.

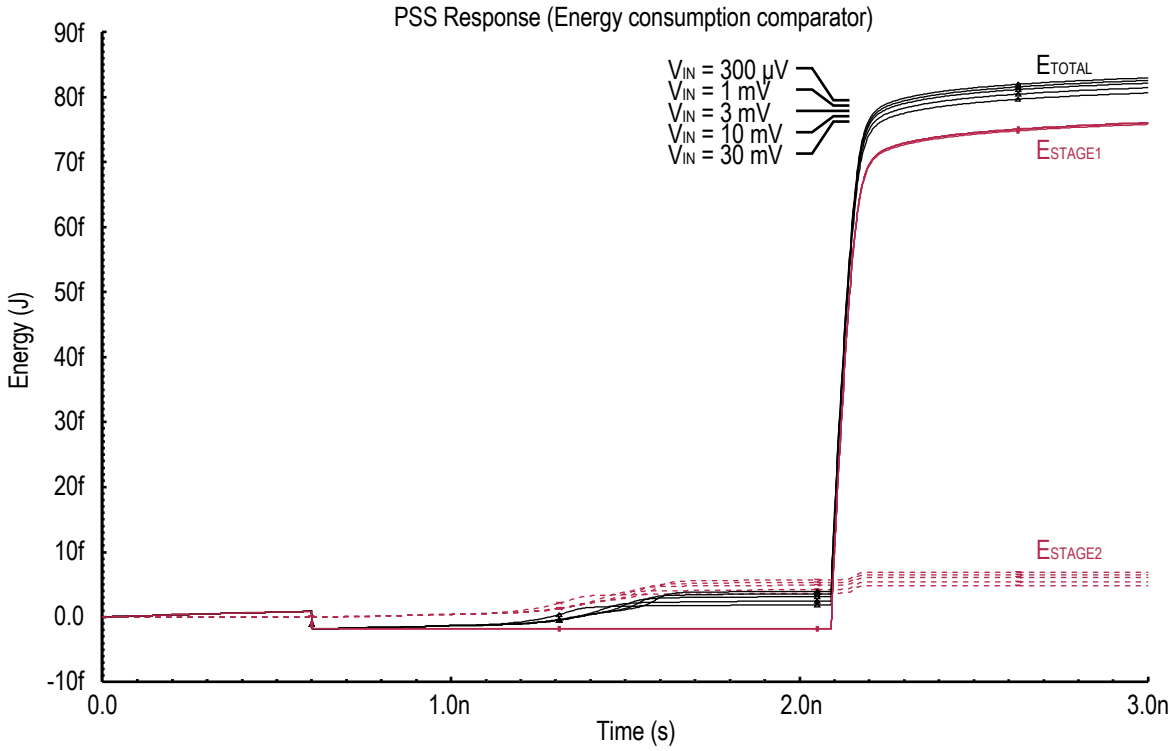

Figure 5-14, Power consumption of the comparator for one conversion with different input voltages, the red graphs indicate the power consumption per stage.

The power consumption for one conversion is shown for each stage and the total. As can be seen the power consumption in the second stage for a comparison with a small input voltage is slightly larger than the ones with a larger input voltage. The reset phase of the comparator starts at approximately 2.1 ns, at this point the discharged capacitors of the first stage are filled again. The total power consumption for one comparison can be estimated as 82 fJ.

5.4 CONCLUSIONS

The comparator is designed in this chapter and a new offset compensation method it introduced.

The result is a comparator which handles the small input range operating at the required speed of 333 MHz (see section 5.2). The power consumption for one comparison is 82 fJ, introducing an input equivalent noise with a standard deviation of 0.37 LSB bit. This is slightly larger than the comparator used in [6], while operating at a higher speed and introducing less noise.

The offset of the comparator was too large for proper operation, due to the small input range of the ADC. The calibration introduced to compensate for this offset, reduced the offset from a maximum of ~ 8.56 mV to less than 1 LSB bit (~500 µV). Extra power is consumed while compensating for this offset, with a maximum of approximately 20 fJ per ADC conversion. This is small compared to the power consumed by the comparator itself: 82 fJ * 7 = 574 fJ for a complete ADC conversion.

SAMPLE AND HOLD

The ADC designed is shown in Figure 6-1, the sample and hold part is highlighted and will be discussed in this chapter. It consists of a switch and its control circuit. The switch is used to load a sample charge onto the capacitor array of the DAC which forms the hold capacitor (discussed in chapter 4). In this chapter the DAC will be treated as a simple hold capacitor with the capacitance equal to the capacitor array of the DAC.
As with all the other elements in the ADC the power consumption of the switch and its control circuit should be kept as low as possible. Also the switch's contribution to noise, non-linearity and offset of the ADC should be taken into account.

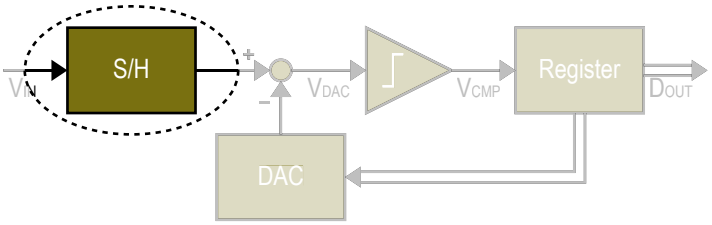

Figure 6-1, The sample and hold switch will be treated in this chapter

In the first section of this chapter the used switch is discussed as well as its requirements which are important for our ADC. The implementation of the switch is described in the second section. In the third section the performance of the switch is discussed and its influence on the performance of the ADC. In the last section conclusions are drawn.

6.1 THE SAMPLE AND HOLD SWITCH

The sample and hold switch used in our ADC is a bootstrapped NMOS transistor. The main reason for using this type of switch is its high linearity compared to other solutions like for instance a complementary NMOST/PMOST switch [15]. Also the low power consumption [6] is beneficial for using it in our ADC.

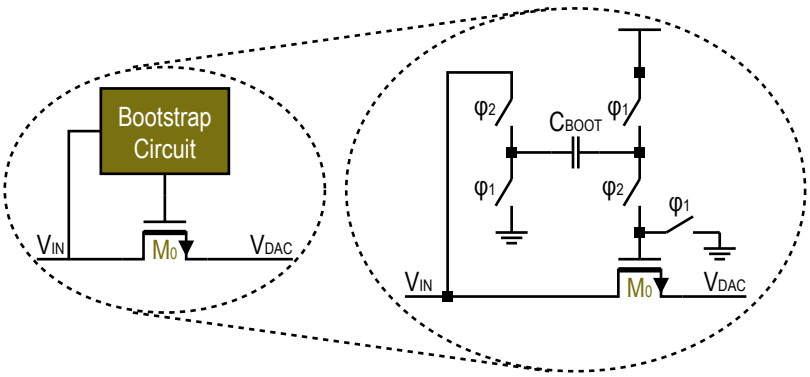

Figure 6-2, Architecture of the bootstrap NMOS transistor φ_1 represents the hold phase, φ_2 represents the sampling phase

6.1.1 ARCHITECTURE

The idea of the bootstrap NMOS transistor is illustrated in Figure 6-3, using the architecture of Figure 6-2. The bootstrap circuit controls the gate voltage of the NMOS transistor which acts as the switch. It applies a zero gate-bulk voltage to the transistor, when the switch should be open (in the hold phase φ_1 of our ADC). When the switch should be closed (during the sampling phase φ_2 of our ADC) the circuit will apply a fixed gate-source voltage to the gate of the transistor. This fixed offset voltage between the gate and the input voltage of the ADC is obtained by the use of a pre-charged capacitor. This capacitor is charged during the hold phase φ_1, as illustrated in Figure 6-2.

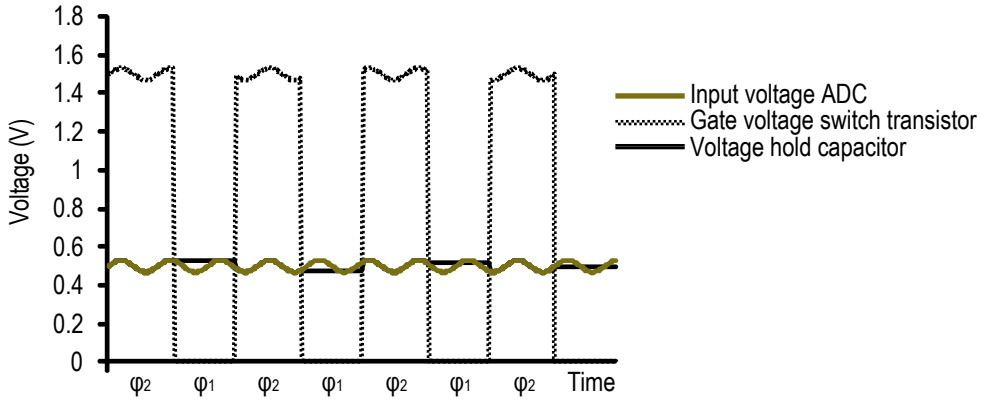

Figure 6-3, Voltages around the bootstrapped NMOS transistor during the sample and hold phase φ_1 and φ_2.

An advantage of a fixed gate-source voltage is an more or less fixed on-resistance of the switch. As mentioned in chapter 3 the on-resistance of the switch in combination with the capacitance of the DAC forms a low-pass RC-filter. The fixed on-resistance is preferable, when using this filter characteristic as part of the anti-alias filter in the spectrum analyzer.
Another effect of the fixed gate-source voltage is that the amount of charge injected into the DAC while closing the gate of the switch transistor becomes less dependent on the input voltage. This is important for the linearity of the switch and thus for the linearity and SFDR of the complete ADC.

6.1.2 REQUIREMENTS

There are some requirements on the sample switch which are important for the design of the ADC. As mentioned in chapter 3 the noise of the complete ADC should have a standard deviation of 0.64 LSB. The noise is mainly contributed by the DAC, the comparator and the sample switch. The design of the DAC and the comparator left an available amount of noise which can be sampled by the sample switch. As calculated in chapter 5 this amount of noise is equal to 0.20 LSB or 101 µV.
As mentioned in the previous part of this section the charge injected into the DAC when the sample switch is closed can cause non-linearities and therefore influence the SFDR of the ADC. It is important the non-linearity caused by the DAC and the sample switch together is small enough to keep the SFDR of the ADC above the required 70 dB as discussed in chapter 3.
Since the ADC will be implemented in differential form, two sample switches will be present. Mismatch between these switches can cause an offset in the ADC. The offset of the ADC is reduced by a calibration as described in chapter 5. Part of the offset measured for this calibration will be the offset introduced by the sample switches. So this offset will be of less importance since it will also be reduced by the calibration.

The on-resistance of the bootstrapped NMOS transistor is of importance for the speed of the ADC. A conversion speed of the ADC of 40 MS/s is required as determined in chapter 3. The comparator will use most of the available 25 ns conversion time, since 7 comparisons are needed consuming 3 ns of time each (see chapter 5). This leaves approximately 3.5 ns of time left for the sampling phase of the ADC (leaving 500 ps for resetting the ADC). For normal operation the on-resistance of the switch should be low enough to fill the DAC's capacitance over the complete input range within this amount of time. The on-resistance can be increased when using the ADC's RC-filter characteristic as part of the anti-alias filter. The required cut-off frequency is 20 MHz.

6.2 IMPLEMENTATION

The CMOS implementation of the sample switch and its control circuit are shown in Figure 6-4. It is a commonly used bootstrap circuit [15][18]. Transistor M_0 represents the sample switch. During the hold phase φ_1 of the ADC, the transistors M_1 and M_2 will bring the gate voltage of M_0 to zero. M_1 is implemented to protect the gate-oxide of M_2. Meanwhile transistors M_3 and M_4 pre-charge the bootstrap capacitor C_{BOOT}. The gate of M_3 is driven by a boost circuit which is also shown in Figure 6-4.

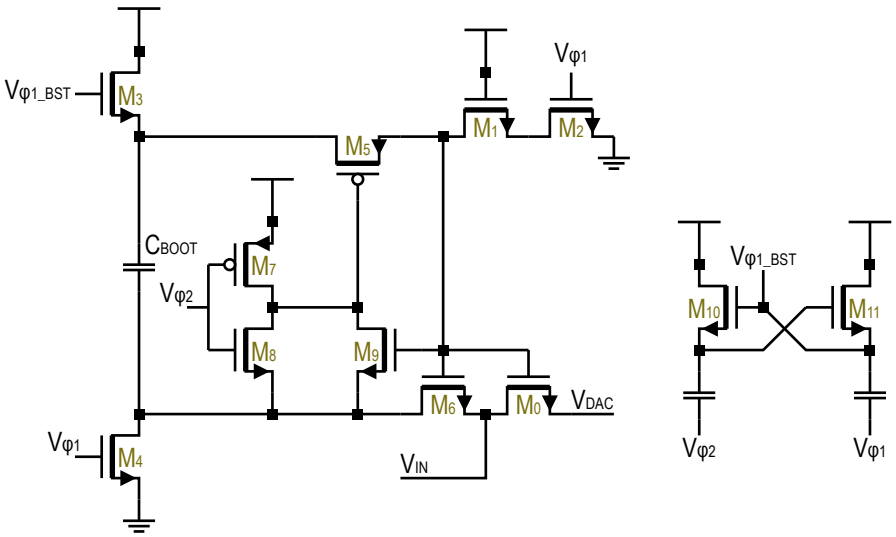

Figure 6-4, Implementation of the bootstrapped NMOS switch. Vφ1 is high during the hold phase while Vφ1 high during the sampling phase. Vφ1_BST is twice the supply voltage during the hold phase and equal to the supply during the sampling phase.

During the sampling phase φ_2, the transistor M_6 will couple the bottom plate of the pre-charged bootstrap capacitor C_{BOOT} to the input V_{IN}. The gate of M_0 will be coupled to the top plate of C_{BOOT} by M_5, creating the wanted offset voltage with the input voltage. Transistor M_7 is used to close the gate of M_5 during the hold phase. Transistors M_8 and M_9 are used to open the gate of M_5, where M_8 is only used during start-up of the sampling phase.
For the operation of the ADC the characteristic of the switch transistor M_0 is most important.

6.2.1 SWITCH TRANSISTOR

The switch transistor M_0 determines the on-resistance of the switch. As mentioned in chapter 3, the ADC is created in a 65-nm ST-process with a supply voltage of 1 V. With the bootstrap circuit of Figure 6-4 this means the gate-source voltage will be fixed at 1 V during the sampling phase. The on-resistance of the switch can now only be adjusted by changing the size of M_0.

The on-resistance of the sample switch forms an RC-filter with the capacitance of the DAC in the sampling phase. Because of this, the noise which will be sampled onto the DAC will be equal to the thermal noise √(k*T/C) of the DAC capacitance and will not depend on the on-resistance of the switch. So the size of the switch transistor can be determined by looking at the speed requirement of the ADC.
As mentioned in the previous section each sample should be taken in 3.5 ns. The minimum transistor size available in the technology is chosen which resulted in a simulated on-resistance of approximately 4129 Ω. This on-resistance in combination with the 1.36 pF DAC capacitance (see chapter 4) gives an RC cutoff frequency of 1 / 2πRC = 28.3 MHz. This frequency is high enough to let all the input signals up to the required 20 MHz through. Meanwhile RC-filter characteristic functions as a part of the anti alias filter; it relaxes the anti-alias filter requirement in the spectrum analyzer by one order.

6.3 PERFORMANCE

The comparator is built in a 65 nm ST process and simulated. The results are shown and discussed in this section.

6.3.1 LEAKAGE

Important for the sample and hold switch is that it will preserve the charge on the sample capacitor during the hold phase. Because of the small-input range of our ADC in combination with the small sample capacitor (DAC capacitance) it is appropriate to look at the leakage of the switch when it is opened. In the 65 nm technology most of the leakage will be present between the sample and the gate (gate-leakage). The leakage current is simulated by replacing the sample capacitor by a DC voltage source. The leakage is simulated varying the voltage source over the input range of the ADC. The leakage current varies between 458 fA and 561 fA. With a hold phase of 21.5 ns (25 ns - 3.5 ns) and a sample capacitance of 1.36 pF this results in a (differential) voltage drop of approximately ((561 fA - 458 fA) * 3.5 ns) / 1.36 pF = 2.65E-7 mV. This is low enough to neglect the leakage.

6.3.2 LINEARITY

The charge injected by the sample switch is dependent on the input voltage of the ADC. Therefore it will influence the linearity of the ADC. The bootstrap NMOS transistor was used to make the injected charge less dependant on the input voltage of the ADC.
The charge injection can be seen in Figure 6-5 where an example of the sampling is shown.

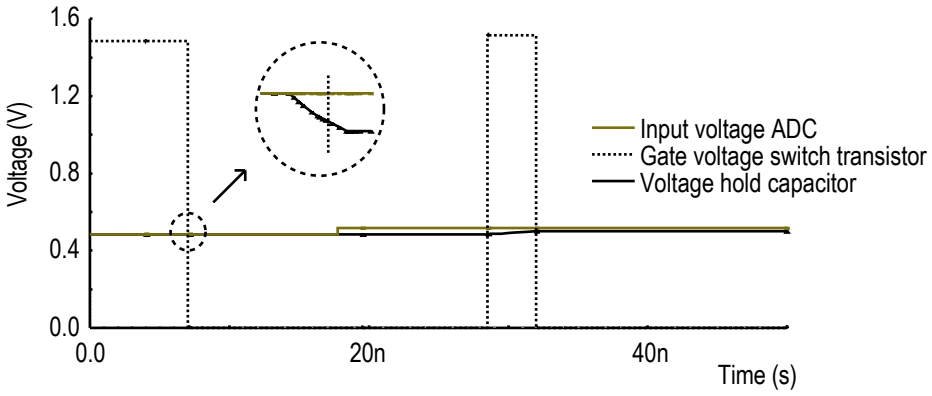

Figure 6-5, Two sample and hold cycles. Charge is injected into the DAC after closing the switch transistor.

Since the ADC is implemented in differential form, the injected charge will mainly change the common mode of the input. Since it will depend on the input voltage, it will influence the gain and introduce non-linearities. The INL caused by the sample switch is simulated and shown in Figure 6-6. There is mainly a 3rd order non-linearity with a value which can be neglected compared to the non-linearity introduced by the DAC of 3.06E-2 LSB.

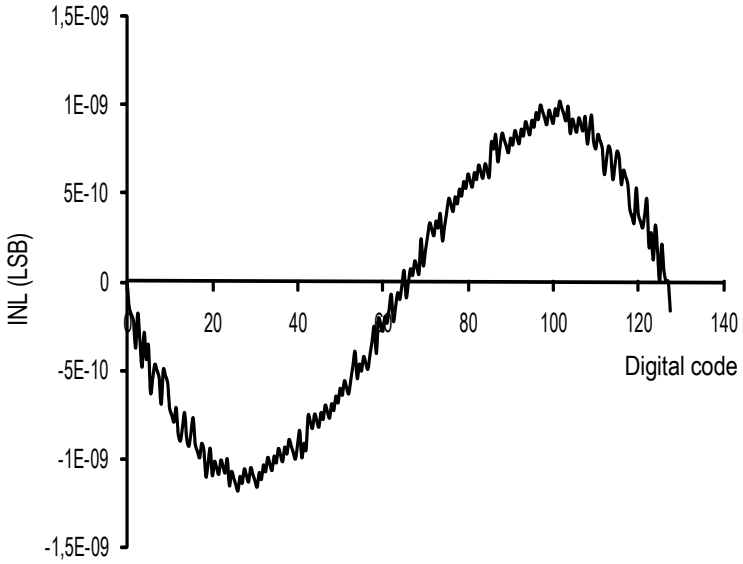

Figure 6-6, INL of the ADC caused by the sample switch

6.3.3 NOISE

The noise which is sampled by the sample switch into the DAC capacitance is simulated, using a transient simulation with noise. The standard deviation of the input referred noise is simulated as 80.4 μV. This is equal to 0.16 LSB, lower than the required 0.20 LSB. Nevertheless for the total required noise of 0.64 LSB this will be accurate enough.

6.3.4 POWER CONSUMPTION

The power consumption of the sample and hold switch and its driving circuitry is simulated. The results can be found in Figure 6-7, which shows 3 sample and hold cycles. The consumption of the S/H is determined at 2.54 fJ per sample cycle.

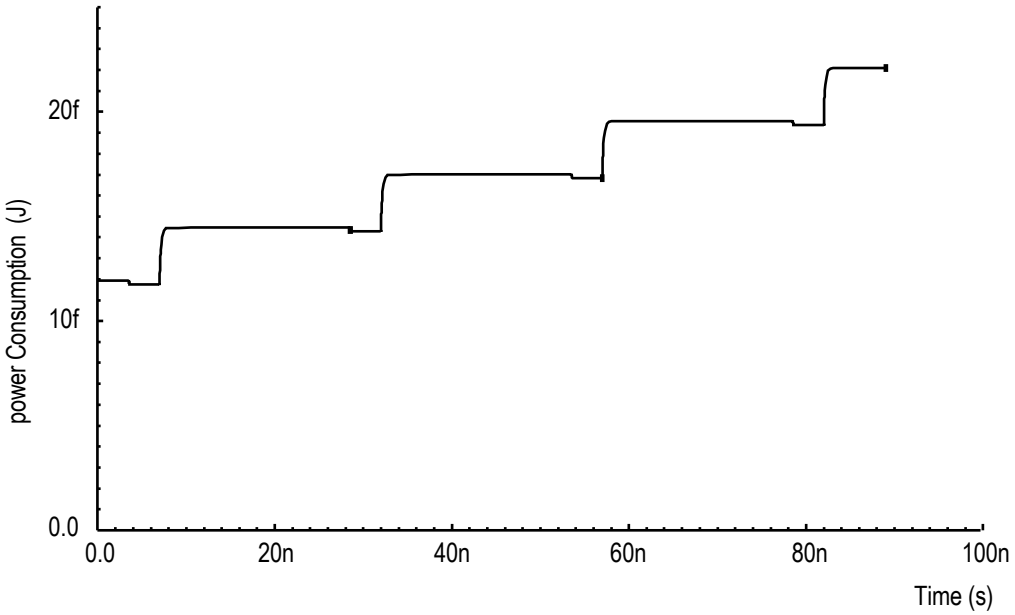

Figure 6-7, Power consumption of the S/H switch and its driving circuitry (for 3 sample and hold cycles)

6.4 CONCLUSIONS

The sample and hold switch used is a bootstrapped NMOS transistor. The results show that the designed switch has less influence on the performance of the complete ADC. The leakage and the introduced non-linearity can be neglected. Even the power consumption with 2.54 fJ per sample is small compared to for instance the 574 fJ consumed by the comparator for 7 comparisons (see chapter 5.3).
The size of the sample switch influences the on-resistance of the switch and therefore input characteristic of the ADC. The RC-filter characteristic is used to relax the specification of the alias-filter in the spectrum analyzer by approximately one order.

CONTROL LOGIC

The complete ADC structure is shown in Figure 7-1. In this chapter the register part of the ADC will be described. This part is completely digital and will control the DAC (treated in chapter 4) and give the output of the ADC. More control logic will be needed to get the ADC working. The clocked sample switch and the clocked comparator need control signals to operate. This controlling part of the ADC will also be treated in this chapter.

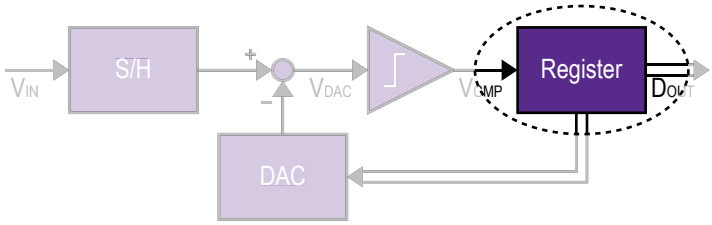

Figure 7-1, The complete ADC structure, the register part and the logic will be described in this chapter

In the first section the used control mechanism is shortly introduced as well as the register logic. In the second section the implementation of the logic is described followed by the simulation results in section three. The conclusions can be found in the last section.

7.1 THE DIGITAL PART

The task for the digital part of the ADC is creating control signals which operate the sample switch, the DAC and the comparator. Next to that the logic should handle in control input of the ADC and delivering the output of the ADC. The important requirements are the timing and the power consumption. The comparator needs a period time of 3 ns (see chapter 5), while the sample switch needs a sampling time of 3.5 ns (see chapter 6). The total available time for one conversion is 25 ns, since the ADC requires a sampling speed of 40 MS/s (see chapter 3). The power consumption needs to be as low as possible, like with all the other elements in the ADC.

7.1.1 CONTROL DELAY LINE

The ADC will be controlled with an inverter delay line [19], which is also used in the ADC of [6]. Because of this delay line the ADC requires no external clocking. The principle is explained in Figure 7-2, where a part of the delay line is shown. The even inverters are supplied with a long channel NMOST, while the uneven inverters have a long channel PMOST. Connecting NAND gates to the line will create timed pulses which can be used as control signals for logic in the ADC. Other than in [6] also NOR gates will be connected to the line in between the NAND gate like shown in Figure 7-2.

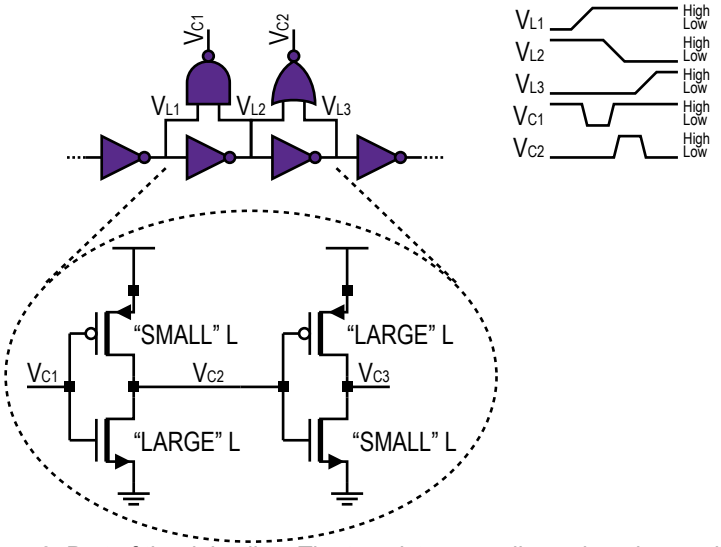

Figure 7-2, Part of the delay line. The transistors are dimensioned according to the figure. A NAND and NOR gate will create pulses which can be used to trigger parts in the ADC.

7.1.2 REGISTER

The register of the ADC is basically an array of memory cells which contains the output of the ADC. Before every conversion the ADC gets a reset and the contents of the memory array is cleared. During the conversion, a bit is added to this array every time a comparison is completed. Meanwhile the contents of the array forms directly the input for the DAC. After the conversion is completed (before the next conversion start with a reset), the contents of the register is shifted into an output buffer for readout.

7.1.3 SAMPLE SWITCH AND COMPARATOR

The sample switch discussed in chapter 6, and the comparator discussed in chapter 5 are both clocked elements. Both will be driven by a memory cell (latch) which is placed before them. The state of these latches (the clock of the switch and the comparator) are controlled by pulses from the control line.

7.2 IMPLEMENTATION

The logic and delay line are implemented in CMOS. The ADC is triggered by a external pulse which will come from the spectrum analyzer logic. After this pulse the sample switch is opened and closed after the required time. Then the first comparison starts and the DAC is input is changed. These last two actions are a repeating cycle (N-times for an N-bit converter) and will be discussed below.

7.2.1 ONE COMPARISON

A part of the delay line is a repeating element. It starts with the triggering of the comparator which starts a comparison. When the comparison is completed, the result will be read out. This will adjust in the input of the DAC. After the result is read out the comparator will get a reset. This cycle will repeat itself until the 7 comparisons of our ADC are completed. The control signals used for these repeated actions are coming from the control delay line and are shown in Figure 7-3. As can be seen the pulse used for reading out the comparator is shorter in time than the pulses used to control the comparator. This is done because the comparator needs an amount of time after it is triggered to make a decision. What can be

seen in Figure 5-11. The duty cycle of the pulses are changed by adjusting the channel lengths of the inverters in the delay line. To acquire the pulses shown in the figure a W/L ratio of 0.135/4.00 µm is used for the NMOS transistors in the uneven inverters and a ratio of 0.135/0.4 µm is used for the PMOS transistors in the even inverters.

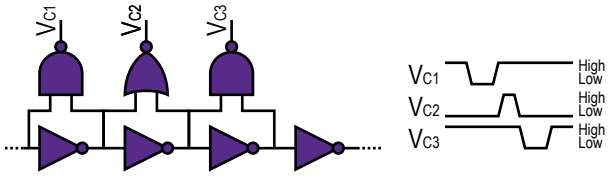

Figure 7-3, Repeating element of the delay line. Vc_1 will be used to start a comparison. Vc_2 will be used to read out the comparator result. Vc_3 will reset the comparator.

The last part of the delay line shifts the contents of the register into an output buffer after which it resets the ADC.

7.3 PERFORMANCE

The delay line and the control logic is built in a 65 nm ST process and simulated. The results will be shown and discussed in this section. The most important properties of the logic are the speed/timing and the power consumption.

7.3.1 SPEED AND TIMING

As described in the previous section most of the control delay line is a repeating element which is shown in Figure 7-3. The signals shown in this figure are also shown in Figure 7-4, which are the simulation results of the ADC. As can be seen the duty cycle of the comparator control pulses are longer than the pulse which triggers the readout.

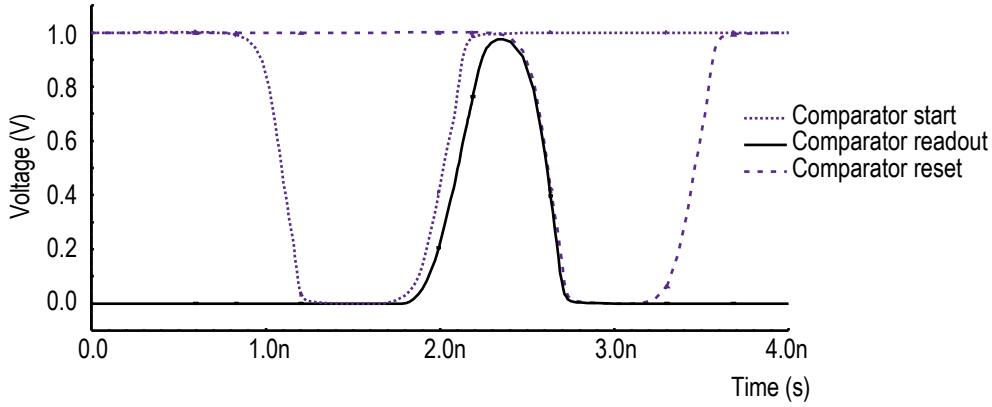

Figure 7-4, Simulated repeating part of the delay line with the output pulses controlling the ADC

Also the total timing of a complete ADC conversion is simulated and the results can be found in Figure 7-5. As can be seen the conversion starts with a sample period after which the cycles with comparisons start. A complete conversion takes 23.84 ns which is faster than the required 25 ns. The sampling phase takes 3.3 ns which is shorter than the 3.5 ns estimated in chapter 6.

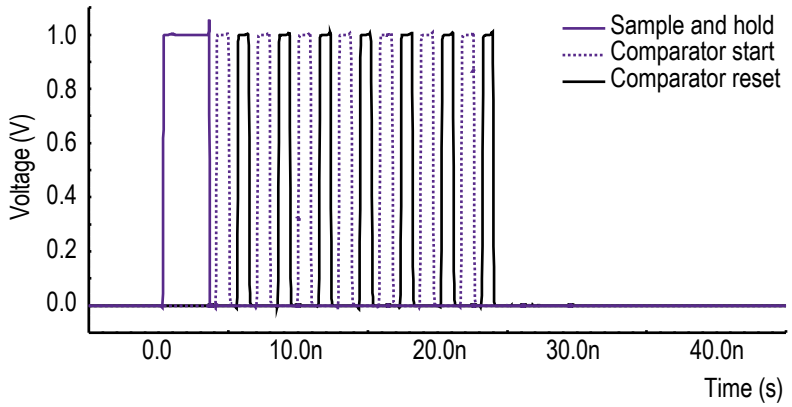

Figure 7-5, Control signals for one ADC conversion

7.3.2 POWER CONSUMPTION

The power consumption of the logic and the delay is simulated for one ADC conversion and the results are shown in Figure 7-6.

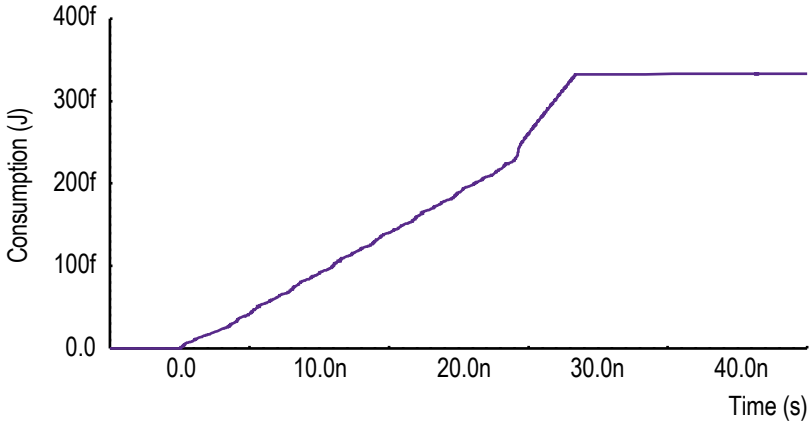

Figure 7-6, Power usage of the logic and delay line during one ADC conversion

The logic and delay consume together 332 fJ during a complete conversion of the ADC.

7.4 CONCLUSIONS

The control logic implemented in the ADC consists of an inverter delay line which takes care of the timing and control of different parts of the ADC. Other elements of the logic are memory cells holding the state of for instance the sample switch, the comparator and the DAC.
The power consumed by the digital part of the ADC is 332 fJ per conversion.

CONCLUSIONS AND RECOMMENDATIONS

The goal of the thesis was to design a low power analog to digital converter competing with the most energy efficient ADCs available today. Three ideas were investigated. First of all the Träff comparator was investigated for the use in a current ADC. Due to its large leakage current and bad speed performance, the conclusion is that this comparator is not suitable for an ADC when a low power consumption is required. Other, more simple, solutions perform better.
The second idea investigated was a discharging ADC which uses the charge sampled from the input to perform a conversion. This resulted in a SAR-ADC where the DAC consumes very little power. Nevertheless the discharging DAC gave high requirements on the comparator for offset and common mode range. These requirements increased the power consumption of the comparator cancelling the saved consumption in the DAC.
The third idea investigated consisted of the elimination of amplifier power for weak input signals. This amplifier power is consumed prior to the ADC and can be saved by making a small input range for the ADC. This was done for a receiver from a spectrum analyzer used for cognitive radio applications. The application gave other important requirements to the ADC. A high linearity was required resulting in a minimal SFDR of 70 dB. The application uses dithering to increase the SFDR, which also gives a noise requirement to the ADC.

8.1 CONCLUSIONS

The designed ADC for the SA is a successive approximation register (SAR) ADC, because of the energy efficient operation of the SAR algorithm. In the architecture a charge redistribution DAC is applied making it easy to implement the ADC in the existing SA architecture, consisting of a time-discrete output prior to the ADC.
The ADC is designed with a 7-bit resolution. For the application of the spectrum analyzer the required resolution is 9-bit [5], the additional 2 bits are acquired by dithering. For this case noise has to be added in the ADC which can be used as dither noise.
The main challenges for the design were the small-input range and the required linearity resulting in a SFDR of 70 dB. For this purpose several new techniques were developed which will be discussed next.

8.1.1 NEW TECHNIQUES

Basically three new techniques are introduced for the new ADC architecture. The input range is reduced by increasing a dummy capacitor in the charge redistribution DAC instead of adjusting reference voltage (chapter 4.1.3). Furthermore a calibration architecture and procedure are introduced (chapter 4.1.4), bringing the mismatch of capacitors in the charge redistribution DAC to a lower level. The calibration needs a larger dummy capacitor in the DAC which make the new techniques an ideal combination. The third new technique

introduced is an offset compensation method (chapter 5.1.3) which makes also use of the larger dummy capacitor in the DAC. The compensation of the offset (mainly introduced by the comparator) is needed because of the small input range of the ADC. The offset is too large in relation with the input range, introducing problems for operation.

8.1.2 ACHIEVED ADC PERFORMANCE

The specifications of the designed ADC are summarized in Table 8-1.

Property	Required	Performance ADC
Supply voltage	1 V	1 V
Input range	63 mV	63.2 mV
SFDR	70 dB	72 dB
Noise contribution	0.64 LSB	0.43 LSB
Resolution	7 bit	7 bit
Power consumption @ 40 MHz	< 1 mW - 50 mW	38.33 µW
Speed	40 MS/s	~41.9 MS/s

Table 8-1, Power consumption of the ADC for each element. The comparator can consume up to 20 fJ more due to the compensation for offset

As can be seen most of the requirements which were drawn up in chapter 3 are met. The input range is reduced to 63.2 mV. This makes any amplification in the signal path of the SA receiver not necessary.
The new calibration method makes it possible to meet the linearity requirement, resulting in a SFDR of 72 dB. The linearity can be even higher by adjusting the architecture for calibration (see chapter 4). The guideline of a SFDR of 70 dB was used because a higher linearity resulted in a higher power consumption and a more complex (longer) calibration.
The noise introduced by the ADC corresponds to 0.43 LSB which does not meet the requirement of 0.64 LSB set in chapter 3. Cause of this is a calculation error during design. The noise produced by the comparator can be increased to meet the requirement. This will even reduce the power consumption of the comparator. The different noise contributors in the ADC are listed in Table 8-2. The variances are summed to get the total noise in the output of the ADC. The total noise of 213.67 µV represents the 0.43 LSB for the 7-bit ADC.

Part	Noise contribution
DAC	78 µV
Comparator	183 µV
Sample switch	78 µV
Total	**213.67 µV**

Table 8-2, Noise produced in ADC sorted by contributor

The power consumed by the ADC is approximately 968 fJ per conversion. The power consumption per part of the ADC is listed in Table 8-3.

Part	Consumption
DAC	49.6 fJ
Comparator	584 fJ (+/- 10 fJ)
Sample switch	2.54 fJ
Logic	332 fJ
Total	**968 fJ (+/- 20 fJ)**

Table 8-3, The energy consumption of the ADC for one complete conversion. The consumption is ordered by the different parts of the ADC.

The power consumption for the ADC at the required speed of 40 MS/s is simulated as 38.33 µW. The consumption of the required amplification before the ADC was approximately 1 mW - 50 mW (see chapter 3). By the elimination of this amplifier the overall power consumption of the SA (amplification + ADC) is reduced by a factor of ~500.

8.2 RECOMMENDATIONS

Recommendations for further work are increasing the noise production in the comparator, which will make the ADC meet it requirements and will most likely reduce the power consumption of the ADC further.
Furthermore the anti-alias filtering before the ADC in the spectrum analyzer needs to be investigated. A discrete time filter would be a recommendation, because of its discrete in- and output.
Another recommendation would be a new solution for the delay line as control mechanism. Simulations show that the line itself consumes more than 90% of the total power used by the logic. A more energy efficient solutions can be looked for.

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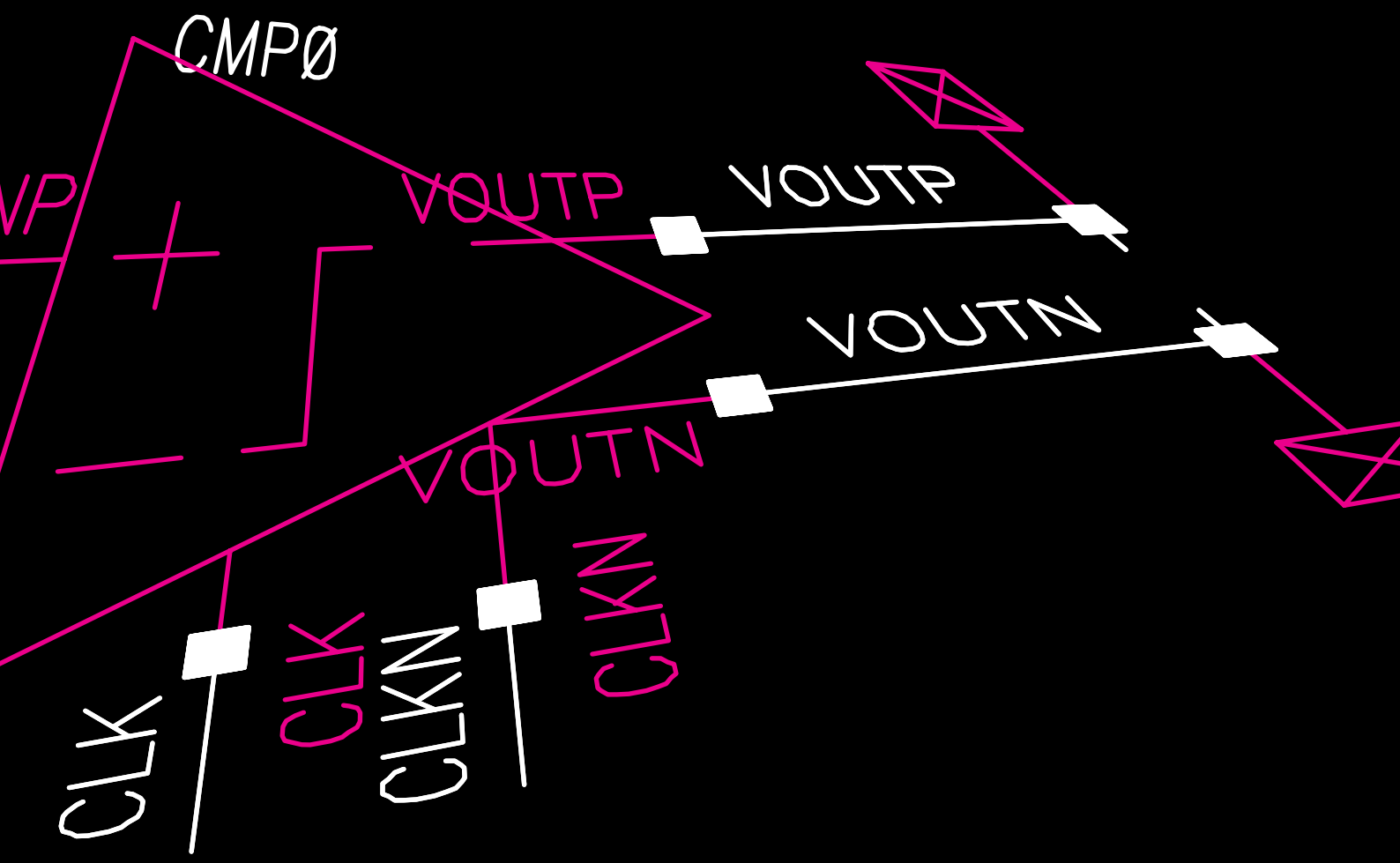
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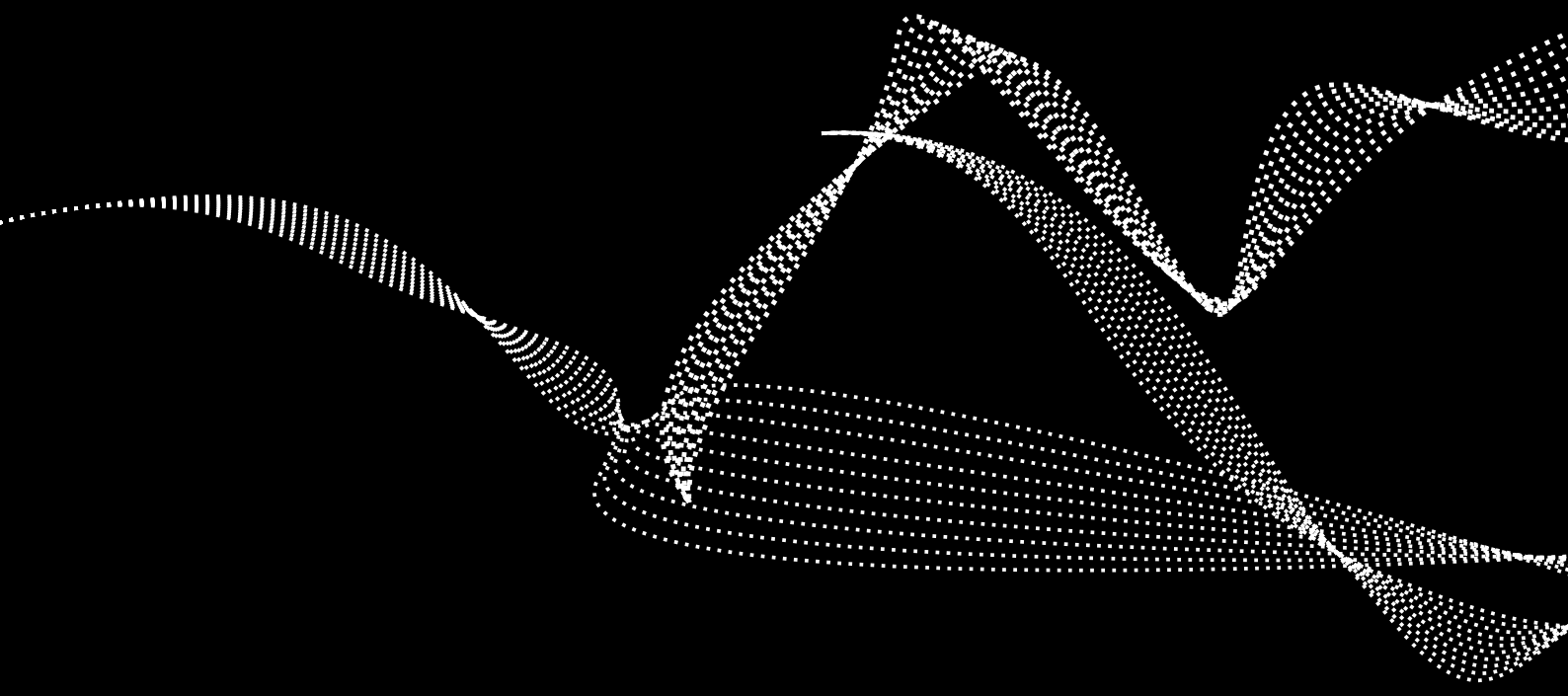

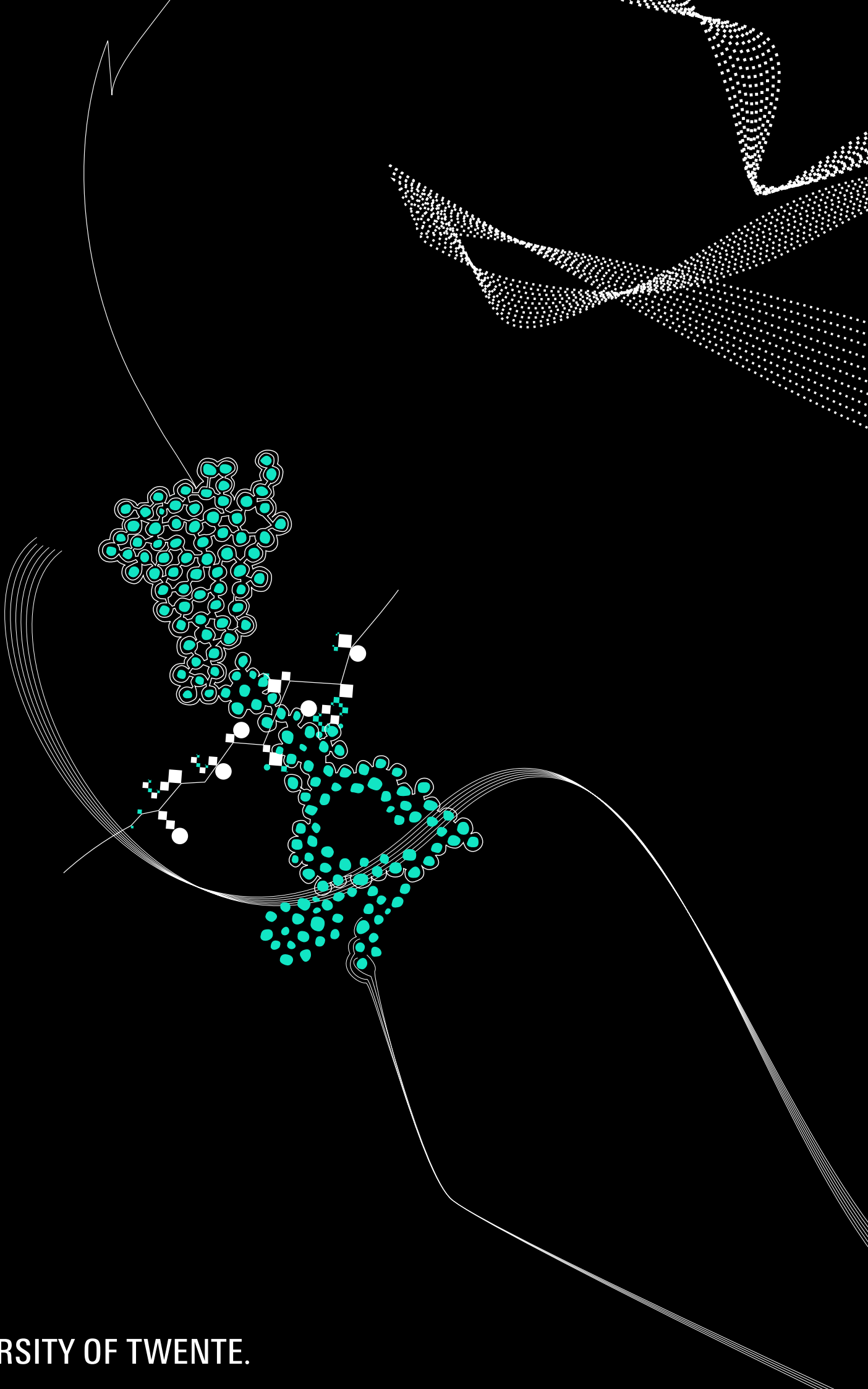

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