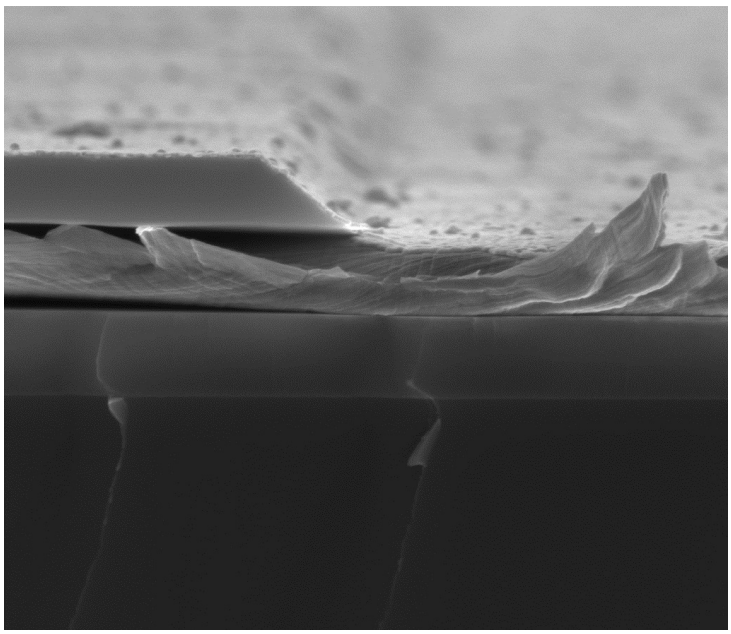
Spintronic devices based on the graphene-nickel(111) interface



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Abstract

Because of possible applications in next generation electronics, there is a lot of interest in research on carbon-based spintronics. An interesting development in this field is a theoretical study done by Karpan et *al.*, which predicts perfect spin filtering at the interface between Ni(111) and graphene. A spin filter like this could, for example, enhance the on/off ratio in a magnetic random access memory. This thesis presents the results of a MSc project performed at the NanoElectronics group at the University of Twente. The goal of this project is the fabrication and characterization of spintronic devices based on the graphene-nickel(111) interface. The initial focus of the project was on the fabrication of a proper insulating layer out of sputtered SiO_2 which is employed in the production of new spintronic devices. A recipe has been developed for sputtering a 200 nm layer which has a resistance in the order of 10 GΩ when cooled down to temperature below 150 K. A spintronic junction can be fabricated by using a lithography step and a buffered hydrofluoric acid etching of 95 s. With this SiO_2 layer, spintronic devices have been successfully fabricated.

Subsequently, initial characterization has been performed by doing transport measurements at room- and cryogenic temperature. At ambient temperature an ohmic behaviour is observed while the measurement at 10 K shows a tunnelling like characteristic. Also these devices can be used to study spin-orbit coupling (SOC) at this interface by performing magnetoresistance measurements, in which electrical characterization is performed under influence of a high magnetic field. By rotating the field, magnetic anisotropies in the density of states can be probed (tunnelling anisotropic magnetoresistance, TAMR). Initial magnetoresistance measurements have been performed by applying a 9 T magnetic field in-plane and out-of-plane of the sample surface. A difference of about 5% in resistance between these two configurations has been observed in the range $-0.05\,\mu A$ and $0.05\,\mu A$. This non-zero magnetoresistance might be an indication of SOC at the interface between Ni(111) and graphene. However, further measurements are required before firm conclusions can be drawn.

Furthermore, the predicted spin filtering effect can be examined by doing Tedrow-Meservey measurements. Therefore, a tunnelling experiment needs to be performed using a counter electrode of superconducting Al, under influence of a high magnetic field. From the conductance versus applied bias characteristic, the spin polarization of the tunnelling current can be derived. It has been attempted to induce and detect superconductivity in a top electrode consisting of Al_2O_3(3.5 nm)/Al(8 nm)/Cu(10 nm). Four-point measurements over the electrode, at a temperature of 314 mK, have been performed. This tests did not shown any sign of superconductivity. The explanation of this might lie in the fact that the underlying layers have a very large surface roughness, which might avoid the formation of a continuous Al layer thereby destroying superconductivity already at low bias current.

Image front cover: SEM image of graphene on nickel, on which an patterned SiO_2 layer and aluminium are applied. On the right the aluminium makes direct contact with the graphene. Image made by Johnny Sanderink.

Contents

Chapter 1

Introduction

Since the first personal computers where introduced in the 1970s until the introduction of smartphones and tablets recently the market for computer memories has been growing at a rapid pace. Also the storage capacity of these memories has increased dramatically. Where the IBM 3340 from 1973 had a storage capacity of 70 megabytes[1], by now, hard disks can have a storage capacity of multiple terabytes, which is an increase of about a factor 10,000. In the future, the capacity of computer memories is expected to increase even further. This development is a result of miniaturisation of electrical components and development of new storage concepts.

A promising field of research in this regard is that of spintronics. The word "spintronics" is a portmanteau of spin and electronics. In conventional electronics the charge of electrons is used for performing storage and logic operations. The field of spintronics focuses on using the charge as well as the spin magnetic moment (which results from the spin angular momentum) of the electrons for these purposes. This makes it possible to build devices in which logic operations, storage and communication can be combined[2]. Because electron spin can have two possible orientations relative to a reference axis, spin-up or spin-down, it is in principle possible to store binary information in a material by controlling the spins of its electrons. The spins of electrons can be manipulated by using ferromagnetic materials, in which electrons have a tendency to align their spin and create a net spin polarization. Information can be transported by sending a spin polarized current from a ferromagnet through a non-magnetic material. However, in such a material the current loses its spin polarization over a certain characteristic length, limiting the distance over which spin information can be transported. A major success of the spintronics field is the development of the magnetoresistive random-access memory (MRAM). This is a type of non-volatile random-access memory which is currently only used in niche applications. MRAM's are for example used in satellite electronics because of their permanence when exposed to radiation and extreme temperature[3].

An important development in spintronics is the emerging field of organic spintronics, in which carbon based materials are used as a medium to transport and control spin polarized signals. This opens the way to cheap, low weight, chemically interactive and bottom up fabricated spintronic devices. Also some high mobility carbon bases materials offer potentially very long spin relaxation times as a result of low spin-orbit coupling and hyperfine interactions. This makes it possible for current to be kept spin polarized over a longer distance than would be the case for inorganic materials.[2]

An material which is very promising for spintronic applications is the carbon allotrope graphene. This material, which was successfully isolated for the first time in 2004 by Andre Geim and Konstantin Novoselov[4], consists of a single layer of carbon atoms in a honeycomb structure. This material has some very remarkable properties. It is a so-called zero-gap semiconductor with a linear dispersion around the Fermi energy and very high mobilities which can

get as high as $16\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$[5].

This project focusses on the spintronic properties of the interface between graphene and the (111) plane of nickel on which it is deposited. This interface is known to exhibit a strong Rashba spin orbit coupling (SOC)[6]. Within a magnetic tunnel junction (MTJ) this may cause a non-zero tunnelling anisotropic magnetoresistance (TAMR). Another remarkable characteristic of graphene is that, as a result of its band structure, conduction through it is solely governed by electrons with a wave vector at the K and K' points of reciprocal space. A theoretical study by Karpan et *al.*[7][8] predicts that, exploiting this effect, perfect spin filtering can be achieved at a nickel(111)-graphene interface. This is because minority spin electrons in nickel can have a wave vector at the K and K' points while this is not possible for majority spin electrons. This way only minority spin electrons are able to conduct through the graphene. To achieve a complete spin filtering five or more layers of graphene are needed because tunnelling of majority spin electrons needs to be suppressed. A spin filter like this can be used to create current with a very high spin polarization. This for example could enhance the on/off ratio of MRAM devices.

Experimental research on this predicted effect is done in the context of a MSc project for the program of Applied Physics at the University of Twente. The project is performed at the NanoElectronics group which is also part of this university. The direct supervisors are ir. E. van Geijn and dr.ir. M.P. de Jong. Other members of the graduation committee are prof.dr.ir. W.G. van der Wiel and prof.dr.ir. A. Brinkman.

The goal of the project is the fabrication and characterization of spintronic devices based on the graphene-nickel(111) interface. These devices can be used to explore the SOC at this interface by performing TAMR measurements. Here a strong magnetic field is applied to the MTJ so the magnetization becomes saturated. The resistance as function of the magnetization direction reveals the influence of SOC, and in particular the anisotropy of that SOC, on the density of states (DOS). Also the predicted spin filtering effect can be examined, by using the method of Tedrow and Meservey[9][10], in which a tunnelling experiment is performed with a counter electrode of superconducting aluminium. Under influence of a magnetic field, Zeeman splitting occurs in the DOS of the aluminium, making it spin dependent. From the IV-characteristic the spin polarization of the current from the Ni and graphene into the Al can be determined.

The devices in this project will be made with a Ni bottom electrode, approximately five layers of graphene and an Al top electrode. On Ni, graphene grows in patches of varying thickness. Because the patches of the right thickness are small and because the used measurement techniques require a smooth junction, the Ni-graphene-Al stack cannot have an area larger than a few square micrometers. Therefore optical lithography as well as electron beam lithography (EBL) are used to create micrometer scale devices.

Previous research in this topic was done by J.M. Boter BSc.[11] and K. van der Zouw [12] in the context of a MSc project and a BSc project respectively. The fabrication process used in these studies provide the basis for the production of devices in this project. The biggest difference is that in these studies polymethyl methacrylate(PMMA) is used to form an insulating layer to avoid conduction over the whole Ni surface except for a few square micrometers where the Ni-graphene-Al stack is located. This layer however has proven to be inadequate for proper spintronic experiments because of poor insulating properties at low temperatures. Therefore, in this project devices with a sputtered silicon dioxide (SiO_2) insulating layer are fabricated and characterized. The first part of this project will be aimed at creating SiO_2 layers on top of graphene that are properly insulating, can be patterned and can withstand multiple cooling cycles to cryogenic temperatures. After that, devices will be designed and fabricated and the first experiments on them will be performed.

The rest of this thesis will start with a discussion on the relevant theoretical background. Then a chapter will be dedicated to the experimental methods in which the used fabrication,

characterization and measurement techniques are discussed. This is followed by a chapter describing the design, fabrication and experimental results on the development of SiO_2 as an insulating layer for the device. Subsequently, design, fabrication and results are discussed for chips which contain actual Ni-graphene-Al devices. In the final chapter the conclusions and recommendations will be given.

Chapter 2

Theory

This chapter discusses the theoretical concepts on which the experimental work of this project is based. The first section describes the phenomenon of ferromagnetism. Then various types of magnetoresistance are discussed. Also background information about the carbon allotropes graphite and graphene is given. Finally the theoretical prediction of perfect spin filtering in graphene is discussed.

2.1 Ferromagnetism

A peculiar property of bulk iron (Fe) is that it can have a net magnetic moment even when there is no external magnetic field applied. Other elemental materials that show this behaviour are, for example, cobalt (Co) and nickel (Ni). This effect is called ferromagnetism, after the Latin word ferrum, which means iron. These elements have in common that they have their 3d-states partially filled according to Hund's rules. Because the filling of the 3d-states is not complete, the electrons in this states have the freedom to adopt different spin configurations. Ferromagnetism in these materials is caused by the exchange interactions between electrons, which is a direct consequence of the Pauli exclusion principle. This principle requires the wave functions of fermionic particles like electrons to be antisymetric. The exchange interactions can be described by the Heisenberg exchange Hamiltonian:

$$\hat{H}_{ex} = -2J_{ex}\hat{S}_1\hat{S}_2 \tag{2.1}$$

This gives an energy term, called exchange energy, as a result of the interaction between electron 1 and 2. $\hat{S}_1$ and $\hat{S}_2$ are the spin operators for electron 1 and 2 respectively. These return $\frac{\hbar}{2}$ if the electron is spin up and $-\frac{\hbar}{2}$ if the electron is spin down. The factor J_{ex} is the exchange integral which depends on the separation between atoms and the overlap of electron clouds. If this term is negative, the energy can be minimized by having the spatial electron wave functions symmetric and the spins anti-aligned. In this case the material is a so called anti-ferromagnet. If the exchange integral is positive, the energy can be minimized by symmetrising the spatial wave function and aligning the spins. In this case the bulk material will acquire a net magnetization and it will be ferromagnetic. The alignment of the spins can also be seen in the density of states (DOS). The exchange interaction gives an energy penalty to the electrons which are not aligned with the majority spin direction. This shifts the DOS of the minority spin electrons up in energy. In figure 2.1a and b this effect is schematically indicated. In figure 2.1c, the spin dependent DOS of ferromagnetic Ni is shown, featuring similar bands for majority and minority spin electrons that are energetically shifted.

According to this theory, every piece of Fe, Co or Ni should have a net magnetization. But from practical experience it is well known that is not the case. This is because there are effects

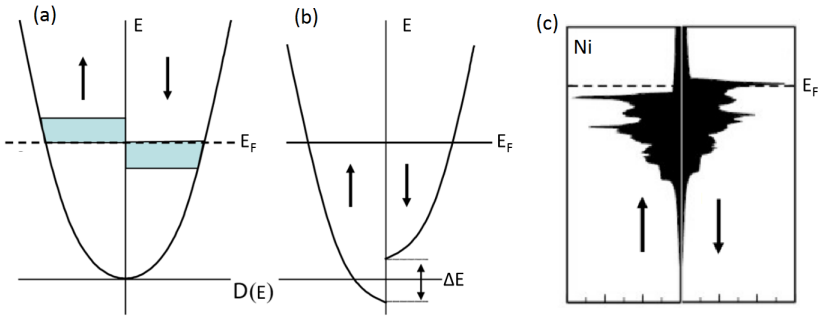


Figure 2.1 – Density of states ($D(E)$) versus energy (E) for majority spin (spin-up) and minority spin (spin-down). (a) A schematic DOS. The blue area on the left represents the added spin up electrons and the blue area on the right represents the subtracted spin-down electrons as a result of the exchange interaction. (b) A schematic DOS. Indicated is the relative shift in energy (ΔE) between majority and minority spins due to exchange interaction. (c) DOS for ferromagnetic Ni calculated from first principles. Note the shift in energy of the spin-down electrons with respect to the spin-up electrons. Adapted from lecture notes on magnetic materials by Geert Brocks [13].

counteracting the alignment of spins. The most important if these is the magnetostatic energy. This term arises from the fact that setting up a magnetic field, like is done when a material gets a net magnetization, cost energy because there is energy stored in the field. The energy stored in a magnetic field is given by[14]:

$$U_m = \frac{1}{2} \iiint \frac{1}{\mu(\vec{r})} |\vec{B}(\vec{r})|^2 dV \tag{2.2}$$

This integration should be done over the whole magnetic field, which is divided in infinitesimal volumes dV. In this expression U_m is the stored energy in Joule, $\vec{B}(\vec{r})$ is the magnetic field in Tesla and $\mu(\vec{r})$ is the material permeability in H/m at the position $\vec{r}$. The magnetostatic energy in ferromagnetic materials is usually reduced by forming magnetic domains as indicated in figure 2.2. If neighbouring domains anti-align their magnetization, the stray magnetic field is lowered, which decreases the amount of energy stored in field (figure 2.2b). By forming even more domains, it is possible to have no magnetic flux on the outside of the material which reduces the magnetostatic energy even more (figure 2.2c).

The magnetization of a ferromagnet can be altered by applying an external magnetic field, which is larger than the so called coercive field (H_c), to align the domains in the preferred direction. When this magnetic field is removed the material keeps a certain remanent magnetization (M_r). The response of a ferromagnetic material to an external field can be pictured by plotting the magnetization versus the magnetic field, as is done in figure 2.2d. As a result of the nonzero value of H_c and M_r a hysteresis loop will be visible in this diagram. At really high magnetic fields all domains will be aligned and the magnetization is at its maximum value, which is called the saturation magnetization (M_s).[15]

2.2 Spin-orbit coupling

Spin-orbit coupling (SOC), also called spin-orbit interaction, is the interaction of a particle's spin with its motion. It is a relativistic effect which originates from the fact that an electric field, when observed from the frame of reference of a moving electron, transforms into a magnetic field. This causes a splitting between the spin-up and spin-down states of the electron. A well known example of this is the spin-orbit coupling within atomic energy levels, which is usually described in introductory textbooks on quantum mechanics[16]. In a crystalline solid, the periodic electric

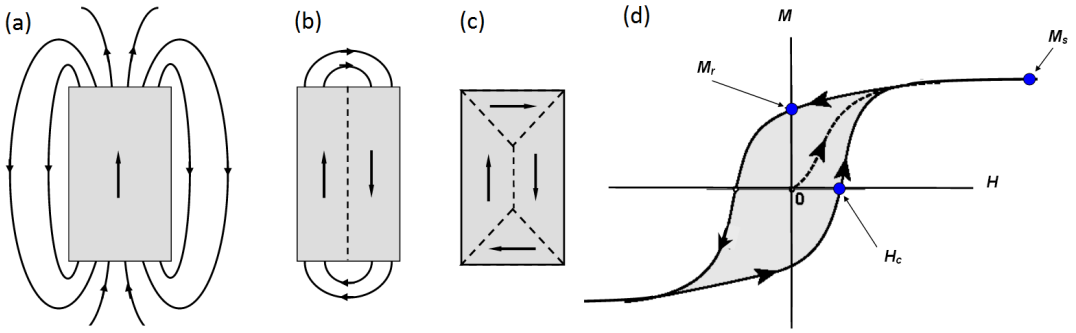


Figure 2.2 – (a) The magnetic field lines of a material with a single domain. Note that energy is stored in the stray magnetic field, which increases the net magnetization energy. (b) A material with two domains. It can be seen that the amount of field lines and thus the magnetostatic energy are already lower than in picture (a). (c) A material with a flux closure domain. In this case, no field lines are visible on the outside anymore and the magnetostatic energy is reduced even further. (d) The magnetization of a ferromagnetic material versus the external applied magnetic field. Note the coercive field (H_c), remanent magnetization (M_r) and the saturation magnetization (M_s). Adapted from Compendium NanoElectronics by Michel de Jong[15].

field of the ionic lattice translates to an effective SOC field ($\boldsymbol{w}_n(\boldsymbol{k}) = [w_{nx}(\boldsymbol{k}), w_{ny}(\boldsymbol{k}), w_{nz}(\boldsymbol{k})]$) in the electrons frame of reference. The interaction of this field with the spin of the electron can be described by the following Hamiltonian[17]:

$$\hat{H}_{SO} = \boldsymbol{w}_n(\boldsymbol{k}) \cdot \boldsymbol{\sigma} \tag{2.3}$$

In this equation $\boldsymbol{\sigma}$ represents the Pauli vector whose components are the Pauli matrices.

Dresselhaus SOC occurs within crystals which show a bulk inversion asymmetry, typically zinc-blende structures. This creates an inversion asymmetric electric field within the material. In this case the spin-orbit Hamiltonian becomes[18]:

$$\hat{H}_D = -\gamma(k_x\sigma_y + k_y\sigma_x) \tag{2.4}$$

In this equation k_x and k_y are the components of $\boldsymbol{k}$ perpendicular to the electric field and γ is a parameter characterizing the SOC strength. Because this Hamiltonian depends on the k-vector, a momentum dependent Zeeman-splitting occurs.

Bychkov-Rashba SOC is a result of structural inversion asymmetry at an interface or a surface. This causes a net electric field perpendicular to the surface/interface. The spin-orbit Hamiltonian for this interaction is given by[18]:

$$\hat{H}_{BR} = \alpha(k_x\sigma_x - k_y\sigma_y) \tag{2.5}$$

In this equation α is the parameter characterizing the SOC strength. When this spin-orbit Hamiltonian is added to the description for a free electron the energy spectrum becomes[19]:

$$E(k) = \frac{\hbar^2 k^2}{2m_e} \pm \alpha|k| \tag{2.6}$$

The $\pm$ refers to the splitting of the spin-up and spin-down electrons within the k_x-k_y plane. Figure 2.3a shows a sketch of the modified energy spectrum. In figure 2.3b (Bychkov-Rashba) and 2.3c (Dresselhaus), arrows are used to indicate the orientation of the spin along lines of equal energy.

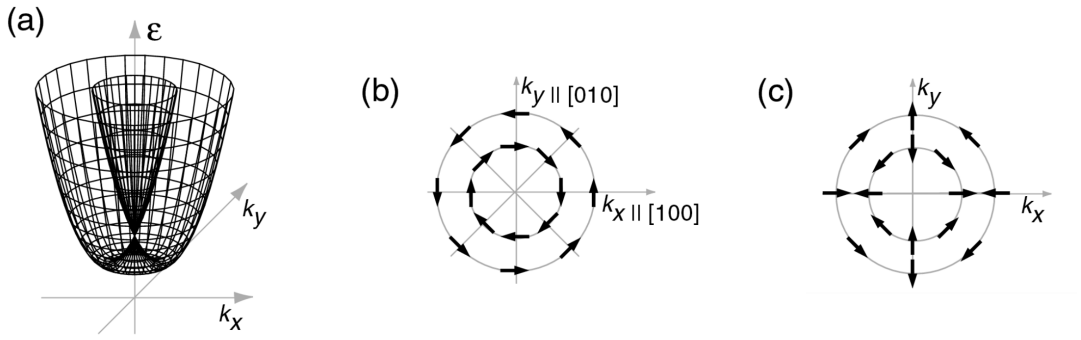


Figure 2.3 – (a) Schematic 2D band structure for an otherwise free electron which is influenced by Dresselhaus or Bychkov-Rashba SOC. Arrows in (b) and (c) indicate the orientation of the spins along lines of equal energy for Bychkov-Rashba and Dresselhaus respectively. Adapted from Ganichev et. *al.*[18]

2.3 Magnetoresistance

Certain devices have the property that the value of their electrical resistance changes as a result of an externally applied magnetic field. This effect is called magnetoresistance. There exist multiple types of magnetoresistance which originate from very different physical origins. In this section giant magnetoresistance (GMR), tunnelling magnetoresistance (TMR) and tunnelling anisotropic magnetoresistance (TAMR) will be discussed.

2.3.1 Giant magnetoresistance

When two ferromagnetic contacts are separated by a thin non-magnetic metal layer giant magnetoresistance (GMR) may occur. This effect causes the electrical resistance to depend on the relative orientation of the magnetization of the two ferromagnetic layers. A schematic representation of such a device can be found in figure 2.4(a). When the magnetization of the two layers are parallel the stack has a lower resistance than in the case when he magnetization of the two layer are anti-parallel.

This effect can be explained by the two-current model. Because of the exchange energy, ferromagnetic materials have a different DOS for majority spin and minority spin electrons. This means that also the current which is carried by electrons at the Fermi-level behaves different for majority and minority spin electrons. As a result of increased scattering probability for minority spin electrons, the current of a ferromagnet is mainly carried by majority spin electrons. Since scattering events in which electron spins flip are very rare, the flow of electrons can be modelled as a circuit with two parallel resistances. One of these channels is representing the flow of majority spin electrons while the other represents the minority spin electrons. Since the current of majority spin electrons is larger, this current can be modelled with a lower resistance than that of minority spin electrons. When the magnetization of the two layers are parallel, the situation can be modelled by figure 2.4(b). Majority spin electrons on one electrode are also majority spin electrons when they are transported to the other electrode and can therefore be modelled by two small resistances in series. Minority spin electrons on the other hand, can be modelled by two larger resistance in series. When the magnetization of the two layers in anti-parallel, the situation can by modelled by figure 2.4(c). Majority spin electrons on the left electrode become the minority spin when they are transported to the other side and vice versa. This means that both currents can be modelled by a large and a small resistance in series. A straightforward calculation of the equivalent resistance in both cases, which can be found in the literature[15],

shows that the the total resistance in the anti-parallel configuration is indeed higher than when the magnetization of the two layers are parallel. The difference in resistance between these configurations depends on various parameters like material properties and the geometry of the device. This difference is usually expressed using the MR-ratio:

$$MR = \frac{R_{AP} - R_P}{R_{AP}} \times 100\% \tag{2.7}$$

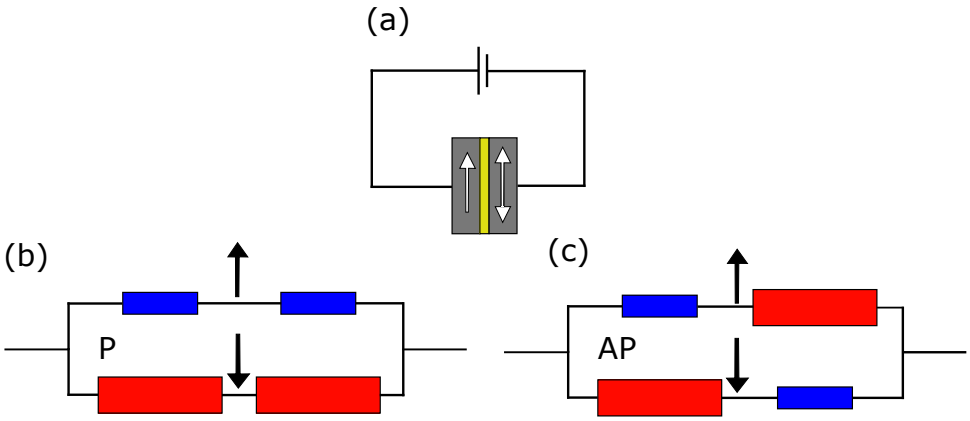


Figure 2.4 – (a) Two ferromagnetic electrodes separated by a small non-magnetic metal. When a voltage is applied perpendicular to the stack the GMR effect can be observed. (b) Resistor network modelling the stack when the magnetization of the two layers are parallel. (c) Resistor network modelling the stack when the magnetization of the two layers are anti-parallel.

2.3.2 Tunnelling magnetoresistance

Another magnetoresistance effect occurs when the two ferromagnetic contacts are separated by a thin insulating layer instead of a conductive layer. This effect is called tunneling magnetoresistance (TMR). In measurements GMR and TMR appear quite similar, however the underlying mechanisms are different. In the case of TMR, transport from one contact to another happens by quantum mechanical tunnelling trough this insulating layer. Such a device is called a magnetic tunnel junction (MTJ)[1]. As a result of TMR, the resistance of this junction depends on the relative orientation of the magnetization of the two contacts. The difference in resistance is caused by the difference in DOS at the Fermi level, between majority and minority spin electrons. It can be explained by a simple model which is sketched in figure 2.5. Note that the DOS at the Fermi level is higher for majority spin electrons (yellow) than for minority spin electrons (green). It is assumed that the electron spin is conserved during tunnelling. Therefore this model contains two tunnelling rates, one for spin-up electrons and one for spin-down electrons. The tunnel rate of electrons of a certain spin polarization is proportional to the product of the DOS at the Fermi level at the donating electrode (density of electrons that can tunnel) and that of the receiving electrode (density of states that can be tunnelled to). Figure 2.5a represents the DOS of both electrodes in the case of parallel magnetization. In this scenario, the majority (minority) spin electrons that tunnel to the other electrode are also majority (minority) spin electrons there. This means that there is a high tunnelling rate for majority spins and a low tunnelling rate for minority spins. Figure 2.5b represents the DOS of both electrodes in the case of anti-parallel magnetization. In this scenario, the majority (minority) spin electrons that tunnel to the other

[1] For measuring TMR, the MTJ requires two ferromagnetic electrodes. For measuring TAMR (section 2.3.3) at least one electrode needs to be ferromagnetic.

electrode are minority (majority) spin electrons there. This means that there is a moderate tunnelling rate for spin-up as well as spin-down electrons. As a result the total tunnelling rate in the parallel configuration is higher than in the anti-parallel configuration. This causes the resistance of the MTJ to depend on the relative orientation of the two electrodes.

Also in this type of magnetoresistance the MR ratio defined in equation 2.7 is used to express the difference between the two configurations. The value of this ratio depends strongly on the used materials for the ferromagnetic contacts as well as the insulating layer. This is a result of ferromagnetic material having a different band structure at the Fermi level for minority and majority spin electrons. The decay length of the electron wavefunction inside the insulator, depends on the overlap between the band structures of the ferromagnet and the insulator. This makes that the tunneling probability for many MTJ's is spin dependent. By a proper choice of materials for the ferromagnet and insulator, MTJ with a very high TMR-ratio can be achieved.[15]

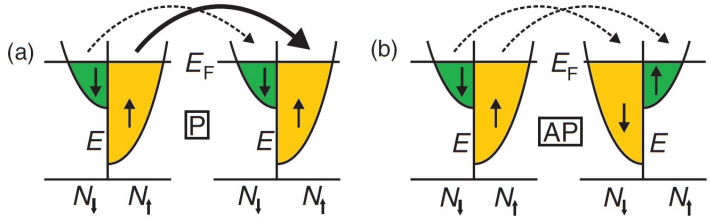


Figure 2.5 – The DOS for both contacts is shown for parallel (a) and anti-parallel (b) magnetization. The green area represents the DOS of the minority spin electrons while the DOS of the majority spin electrons is represented by the yellow area. The arrows indicate the tunnelling rates in both situations. Adapted from Naber et *al.*[2]

2.3.3 Tunnelling anisotropic magnetoresistance

In contrast to TMR and GMR, which require two ferromagnetic electrodes, tunnelling anisotropic magnetoresistance (TAMR) can cause similar behaviour in systems with just one ferromagnet. This is a result of spin-orbit coupling which makes the DOS of a material depend on its magnetization direction relative to its crystallographic axes.

TAMR can be measured by applying a strong magnetic field to a MTJ such that its magnetization saturates. By measuring the dependence of the resistance on the direction of the magnetization, with respect to a reference axis x, the in- and out-of-plane TAMR can be calculated. The in-plane TAMR is defined as:

$$TAMR^{in}_{[x]}(\phi) = \frac{R(\theta = 90°, \phi) - R(\theta = 90°, \phi = 0)}{R(\theta = 90°, \phi = 0)} \times 100\% \tag{2.8}$$

While the out-of-plane TAMR is given by:

$$TAMR^{out}_{[x]}(\theta) = \frac{R(\theta, \phi = 0) - R(\theta = 0, \phi = 0)}{R(\theta = 0, \phi = 0)} \times 100\% \tag{2.9}$$

The angles ϕ and θ, as indicated in figure 2.6, represent the direction of the magnetization with respect to the reference axis and the normal of MTJ respectively.

TAMR effects are caused by SOC-effects (see section 2.2) within the MTJ. Because the momentum and the spin orientation of an electron are coupled, Zeeman splitting by an magnetic field also affects the dispersion relation of the electron. This causes the DOS and thus the

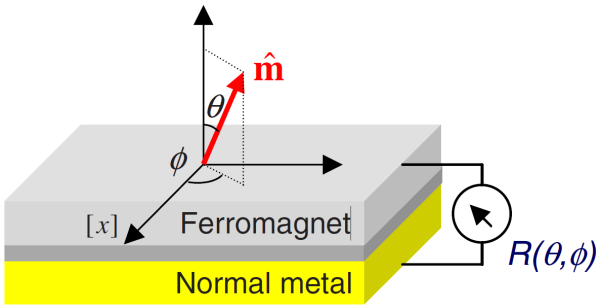


Figure 2.6 – Schematic representation of an MTJ for measuring TAMR. A normal metal and a ferromagnet are separated by a tunnel barrier. The vector $[x]$ represents the chosen reference axis. The angles θ and ϕ are used to indicate the magnetization direction of the ferromagnet. Source: Matos-Abiague et. *al.*[17]

tunnelling rate of a ferromagnetic MTJ electrode, to depend on its magnetization. By analysing the TAMR ratio as function of applied bias and the angles ϕ and θ, the SOC in the MTJ can be explored.

2.4 Graphite and graphene

An isolated carbon atom has the electron configuration $1s^2 2s^2 2p^2$. The $2s$ and the $2p$ electrons have similar binding energy and are the valence states that make up chemical bonding. Chemical bonds are caused by so called hybrid orbitals, which are a linear combination of different valence states. Graphite and graphene bond via the so called sp^2-hybridization. This hybridization gives three orbitals which are a linear combination of the $2s$, $2p_x$ and $2p_y$ orbitals. These orbitals lie in the same plane and make an angle of 120° with each other, while the remaining p_z orbital lies perpendicular to this plane (see figure 2.7). The sp^2 orbitals can form σ-bonds with neighbouring carbon atoms while the p_z orbitals make π bonds. These sp^2-hybridized carbon atoms can form flat sheets of carbon in a hexagonal lattice.[20]

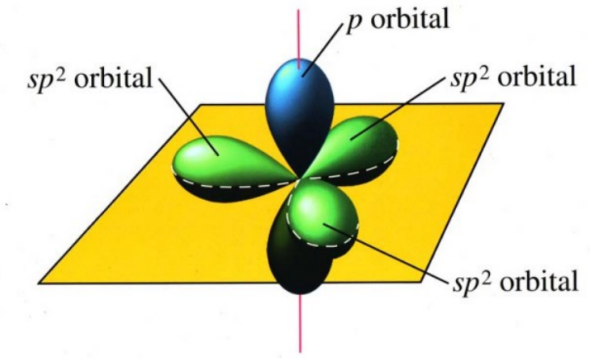


Figure 2.7 – Electron wave functions of an sp^2-hybridized carbon atom. The green lobes are sp^2 orbitals that cause σ-bonding. The blue lobes are p_z orbitals that undergo π-bonding. Source: Lecture notes on graphene by Geert Brocks[20].

Graphite is the most stable allotrope of carbon. Its structure is sketched in figure 2.8a. Graphite consists of sheets of carbon atoms. These sheets have a honeycomb lattice composed of sp^2-hybridized carbon atoms which are covalently bonded. The sheets themselves are held together via van der Waals bonds. The tip of a pencil, for example, consists of graphite.

Another allotrope of carbon is graphene. This is a 2 dimensional material in which there is only a single sheet of sp^2-hybridized carbon atoms in a honeycomb lattice. The structure of graphene is schematically depicted in figure 2.8b. Because the real space lattice is hexagonal, the reciprocal space lattice of graphene is also hexagonal. The first Brillouin zone of the reciprocal lattice is sketched in figure 2.9a. In this figure also the high symmetry points Γ, M, K, K' are indicated.

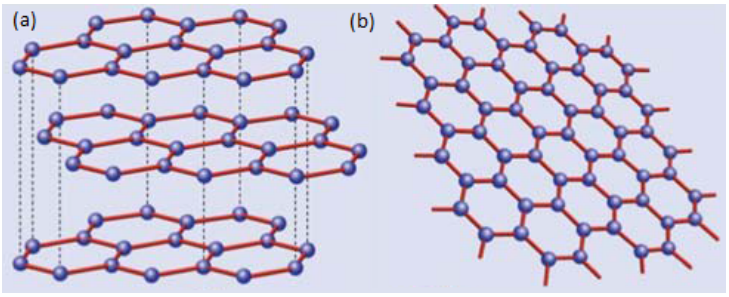


Figure 2.8 – Schematic representation of (a) graphite, which consists of multiple layers of carbon sheets, and (b) graphene, which consists of a single layer of carbon atoms. Adapted from Castro Neto et *al.*[21]

The 2D lattice structure of graphene gives rise to a very interesting band diagram. The sp^2 orbitals are completely filled, while the p_z orbitals are half filled. As a result, the electronic transport in graphene occurs only in the π-bonded p_z bands. Because the p_z-orbitals lie out of the graphene sheet plane, and thus have no overlap with any other orbitals than the p_z orbitals ot the neighbouring atoms, the band structure can be calculated easily using the tight binding approach. The details of this calculation can be found in the lecture notes on graphene by Geert Brocks[20].

This calculation yields the band structure as is plotted in figure 2.9b. At the zoom on the right the so called Dirac cones are shown. They are located at the K and K' points. at these points, the conduction and the valence band touch each other. Because for charge neutral graphene the p_z band is half filled, the Fermi energy is located exactly where the two cones meet. This means that at the Fermi energy, there are only states available at the K and K' points. Since the current through a material is carried by the electrons at the Fermi energy, the current through graphene is solely governed by electrons with wave vectors at the K and K' points. The dispersion relation close to the K and K' points is linear, resembling that of massless particles (e.g. photons). Therefore the behaviour of free electrons in graphene can be described by considering them as massless particles (so called Dirac fermions).[20]

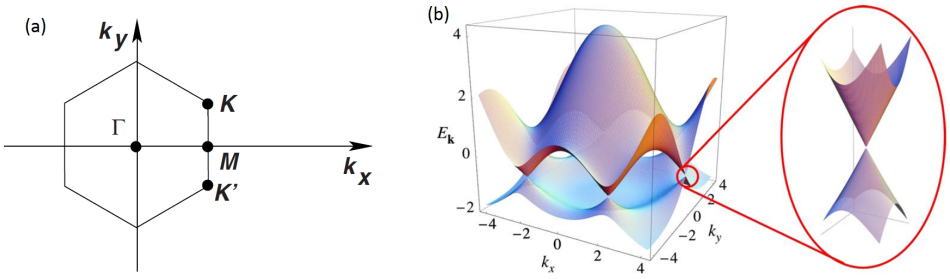


Figure 2.9 – (a) The first Brillouin zone of a 2D hexagonal lattice (e.g. graphene), indicating the high symmetry points. (b) Band structure of graphene with a zoom of the Dirac cones. Adapted from Castro Neto et *al.*[21]

2.5 Spin filtering using graphene

In order to maximize the TMR, different concepts have been investigated theoretically and experimentally. For example crystalline MgO between two CoFeB electrodes has shown to have a TMR of up to 86%[2] at room temperature [22]. Another configuration which might lead to very high magnetoresistance has been theoretically predicted by Karpan et *al.* in 2007[7] and in more detail in 2008[8]. These papers predict perfect spin filtering to occur in a stack of multiple layers of graphene sandwiched between the (111) planes of ferromagnetic Ni or Co. This prediction is based on the shape of the Fermi surface of Ni, Co and graphene. Also the lattice mismatch between graphene and Ni(111) or Co(111) is very small, so they share a common two dimensional reciprocal space. As explained in section 2.4, the band structure of graphene only crosses the Fermi energy at the K and K' points. Disregarding tunnelling, which will be addressed further below, this means that conduction through the multilayer graphene is only possible by electrons at these points. We now look at the projection of the Fermi surface of Ni on the plane perpendicular to the [111] direction (figure 2.10). Because Ni is ferromagnetic, the Fermi surface looks different for majority spin electrons and minority spin electrons. The most important difference is that majority spin electrons have no states at the Fermi energy residing at the K and K' points, while minority spin electrons do have states there. As a result, the conduction electrons at the K and K' points of Ni only carry minority spin. When graphene is deposited on Ni(111), only minority spin electrons should conduct through the graphene layer.

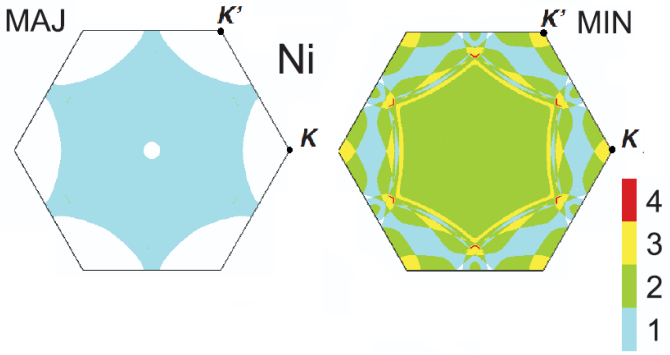


Figure 2.10 – Projections of the Fermi surface of Ni onto the plane perpendicular to the [111] axis, for majority spin (left) and minority spin (right). The colour bar indicates the amount Fermi surface sheets. Note the difference around K and K' between majority and minority. Adapted from Karpan et *al.* [7]

In practice there might be interactions disturbing the spin filtering. For example, the deposition of graphene onto Ni might change the energy landscapes around the C atoms such that the two atoms in the unit cell are no longer equivalent. This would open an energy gap between the valance and conduction band at the K and K' points. In this case, conduction trough the graphene layer could be hampered. To test how interactions like these affect the spin filtering, numerical calculations where made by Karpan et *al.*[7][8]. These calculations shows that interactions like this do not reduce the spin filtering effect.

This study also shows that only a monolayer of C atoms would not be enough to achieve perfect spin filtering. This is mainly because for such a thin layer the tunnelling probability for majority spin electrons is to high. However the calculations show that using around five layers

[2] the publication mentions a TMR of 604% in the optimistic definition $(R_{ap} - R_p)/R_p \times 100\%$. In this thesis the pessimistic definition of magnetoresistance$(R_{ap} - R_p)/R_{ap} \times 100\%$ is used.

of graphene[3] should suppress the tunnelling of majority spins and still give a good transmission for minority spins. In figure 2.11, the transmission is shown throughout the first Brillouin zone for majority and minority spins. It can be seen that for one layer of graphene there is a lot of transmission for minority spins as well as majority spins. But for five layers of graphene there is no transmission for majority spins, while for minority spins there is transmission around the K and K' points. This matches the earlier made prediction based on the shape of the Fermi surface.

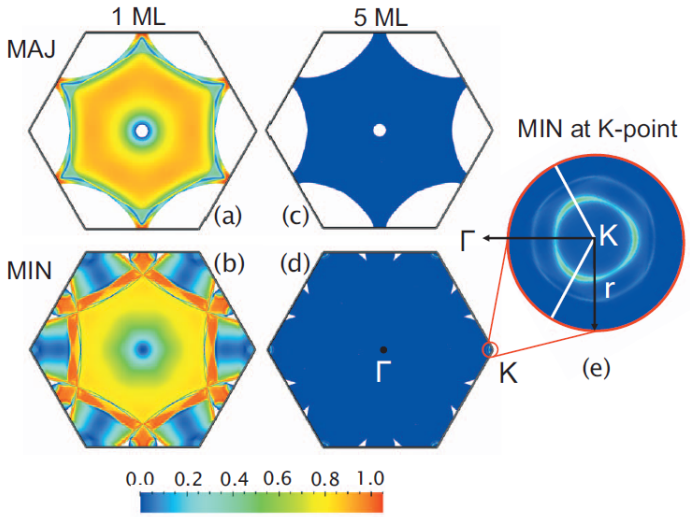


Figure 2.11 – Transmission through (multilayer) graphene as function of the wave vector perpendicular to the [111] direction. For one monolayer, the transmission is large for both the majority (a) and minority (b) spin. For five monolayers, there is no transport of majority spins through the graphene(c), while for the minority spins(d) there is transmission around the K and K' points (e). Source: Karpan et *al.* [8]

According to the theoretical predictions made by Karpan et *al.*[8], the spin polarisation is for all intents an purposes complete when using five layers of graphene. In figure 2.12 (circles) the effect of the number of layers on the magnetoresistance is indicated. This prediction is based on a perfect Ni graphene interface without any lattice mismatch, interface roughness or interface disorder.

To investigate the influence of the 1.3% lattice mismatch between Ni and graphene, Karpan et *al.* repeated their calculation for 19×19 unit cells of Ni and 20×20 unit cells of graphene, corresponding to a lattice mismatch of 5%. Calculating a smaller lattice mismatch would require more unit cells and therefore an unacceptable high computation time. Calculating the spin polarization for this scenario gives a good upper limit for the effect of lattice mismatch. This calculation yields that in the worst case scenario the magnetoresistance, for five layers of graphene, decreases from 100% to 90%.

To model the effect of interface roughness, the calculation was done with 50% of the atoms in the top layer removed. As a result of the interface roughness, the magnetoresistance decreases from 100% to about 70% for five graphene layers, as can be seen in figure 2.12(squares).

The interface disorder is modelled by considering the top layer to consist of $Ni_{50}Cu_{50}$ random alloy. In this case the magnetoresistance in predicted to decrease to 90% for five monolayer. This is indicated by the diamonds in figure 2.12.

[3] There is discussion whether multiple layers of carbon atoms can still be called graphene. In this thesis, less that ten layers of carbon atoms will be referred to as graphene.

From this analysis it can be concluded that even with the presence of lattice mismatch, interface roughness and disorder, this configuration is promising for achieving very high TMR values. This makes it a promising system for spintronics applications.

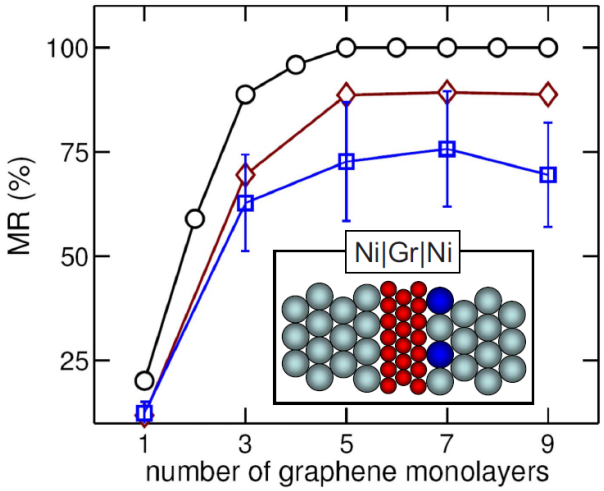


Figure 2.12 – The magnetoresistance for the Ni-graphene-Ni stack as a function of the number of graphene layers, for the ideal case (circles), the analysis of interface roughness (squares) and the analysis of interface disorder (diamonds). This graph shows that even with the presence of interface roughness and interface disorder, high TMR values can be achieved when using about five layers of graphene. Inset: Schematic representation of the Ni-graphene-Ni stack in the case of the analysis on disorder (roughness). The blue spheres represent Cu (missing) atoms. While the gray and red spheres represent Ni and C atoms respectively. Source: Karpan et *al.* [8]

2.6 Tedrow-Meservey method

The spin polarization of a tunnelling current can be determined by using superconducting Al as the counter electrode of a MTJ. This can be done by measuring the bias dependence of the out-of-plane conductance, under influence of a high in-plane magnetic field. This technique is developed by P.M. Tedrow and R. Meservey who used it to determine the spin polarized current of Fe, Co, Ni and Gd electrodes [9] [10].

In a junction in which a ferromagnet is separated from an Al electrode by a thin insulator, a spin polarized tunnelling current into the counter electrode can be induced. Al has a very smooth DOS with sharp edges of the superconducting energy gap of 2Δ, separating the electron-like from the hole-like quasiparticles (figure 2.13a). In a MTJ, this gives a conductance versus voltage relation as sketched in figure 2.13c.

When a magnetic field is applied Zeeman splitting occurs in the DOS of the Al. The quasiparticle energies are shifted by $\pm\mu H$, where μ is the magnetic moment of the electron. This creates a spin dependent DOS in which the energy bands for spin-up and spin-down quasiparticles are separated by $2\mu H$, as is sketched in figure 2.13d. When a spin polarized tunnelling current is applied, a conductance characteristic occurs with four distinct peaks (σ_1 to σ_4). From this, the spin polarization of the tunnelling current P can be calculated as:

$$P = \frac{n_\uparrow - n_\downarrow}{n_\uparrow + n_\downarrow} = 2a - 1 \tag{2.10}$$

Where a is given by:

$$a = \frac{\sigma_4 - \sigma_2}{\sigma_4 - \sigma_2 + \sigma_1 - \sigma_3} \tag{2.11}$$

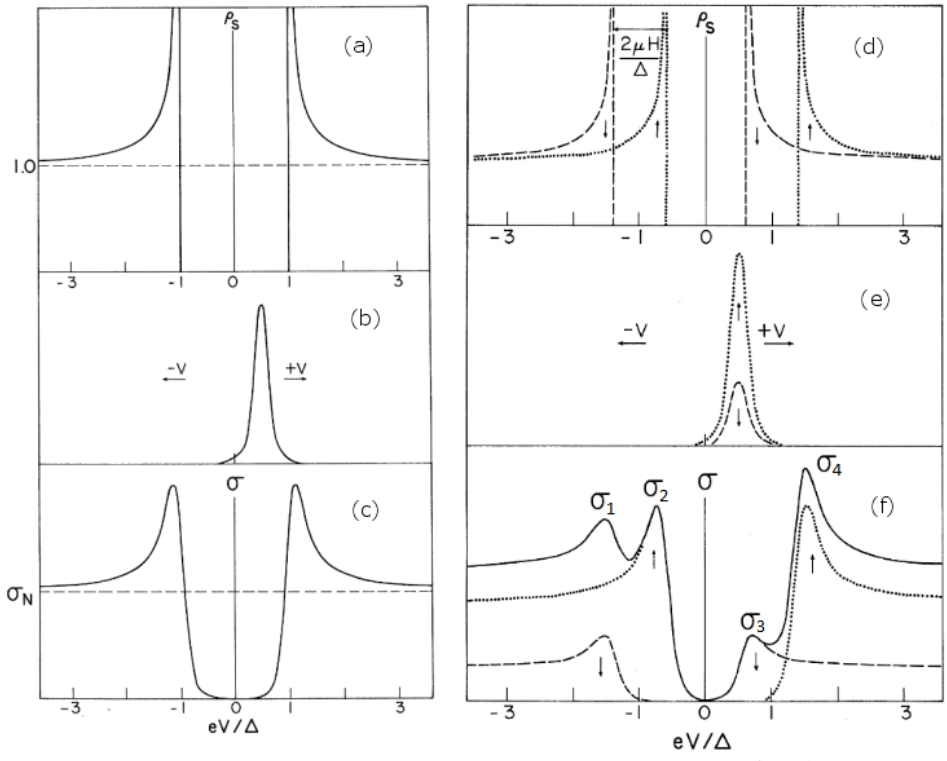


Figure 2.13 – Characteristics of a MTJ with an electrode of superconducting Al. (a) DOS of superconducting Al without external magnetic field. (b) Temperature-dependent kernel of the tunnelling current. (c) Theoretical conductance characteristic without external magnetic field. (d) Spin dependent DOS of superconducting Al under influence of a high magnetic field. (e) Kernel of a spin polarized current. (f) Theoretical conductance characteristic under influence of a high magnetic field, showing four distinct peaks from which the spin polarization can be determined. Adapted from Tedrow et *al.*[10].

To clearly resolve the four different conductance peaks, a large Zeeman splitting is needed which requires a high magnetic field of about 3 T. Usually this is higher than the critical field of Al above which superconductivity is lost. However in thin films, the critical in-plane field can be increased by making the layer much thinner than the London penetration depth. The amplification of the critical field is caused by the fact that for these layers, a parallel magnetic field penetrates the film almost completely, thereby reducing the films diamagnetic moment per unit volume. This causes the critical parallel field to be inversely proportional to the thickness of the layer[23].

Chapter 3

Experimental methods

This chapter discusses the experimental methods which are used in this project. The first section describes the techniques which are used in the production of samples, including lithography, etching and film deposition. In the second section, the methods used to characterize the samples are discussed. This includes scanning electron microscopy for imaging and transport measurements for electrical characterisation.

3.1 Fabrication

Fabrication of devices is this project is performed in the cleanroom of the MESA+ institute at the University of Twente. This is a 1000 m^2 laboratory in which the concentration of environmental pollutants like dust and airborne particles is kept as low as possible. This is done to enable the production of micro/nanoscale devices without contamination. The cleanroom of the MESA+ institute can be quantified as a class 10000 cleanroom. In this section the fabrication techniques which are used in project are discussed.

3.1.1 Photolithography

Photolithography is a technique which is commonly used to create micro-scale structures on a chip. It employs light for transferring a pattern from a photomask to a light sensitive photoresist. The process of photolithography is depicted in figure 3.1. The material which needs to be patterned is applied as a film over the whole substrate. This can for example be done by sputter deposition or electron beam evaporation which are discussed in section 3.1.4 and 3.1.5 respectively. Then a layer of photoresist is spin coated on top. This resist can be either a positive or a negative type.

In the next step a mask alignment machine is used to place a patterned photomask over the sample. This mask is basically a glass plate on which a pattern is applied using a non-transparent coating. The photomask can either make a direct contact or can be held at a certain distance above the sample. Then a light source is used to expose the sample through the mask, creating a shadow of the pattern onto the chip. In the MESA+ cleanroom an EVG620 bond aligner (figure 3.3(a)) is available, which uses a Hg lamp to do exposure with radiation in the 350-400 nm range. The minimum feature size that can be achieved with photolithography is in the same order as the wavelength of the used light[24]. Below this limit, diffraction of the light becomes too strong to write clear structures. Therefore, often UV-light is used for lithographic exposure. Next generation lithography systems employ extreme ultraviolet (EUV) radiation for writing even smaller features[25]. The light sensitive photoresist undergoes a chemical change at the places which are illuminated by the light source. In the case of a positive resist, the exposed

area becomes better soluble to the chemical which is used as developer. When a negative resist is used, the solubility to the used developer decreases.

After the sample is held into a bath of developer for a certain amount of time, positive (negative) photoresist only remains at the unexposed (exposed) areas. Next, uncovered parts of a film underneath the resist may be etched away. This can be done using wet etching or dry etching. In wet etching a liquid is used which chemically reacts with the material which is to be removed. An example of this is Buffered Hydrofluoric acid (BHF) which etches silicon dioxide (SiO_2) but does not react with organic polymers. By using an organic polymer as a photoresist it is possible to selectively etch a pattern into a material. An alternative technique is dry etching in which no liquid chemicals are used. An important type of dry etching is ion beam etching (IBE) which is discussed in section 3.1.3. After etching, the remaining photoresist is removed using a chemical which dissolves the resist but leaves the rest of the chip unharmed. This leaves the film with the same pattern as was written on the mask.

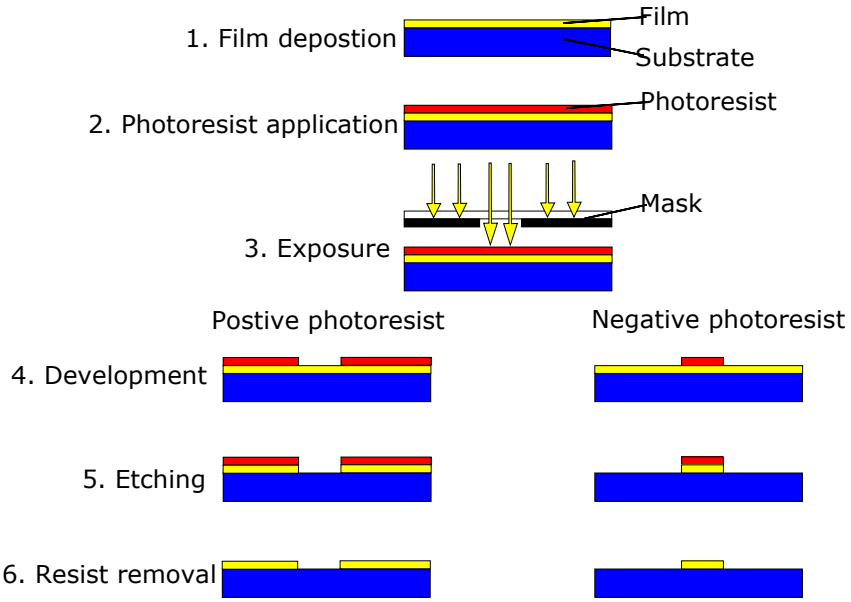


Figure 3.1 – Schematic representation of the photolithography process. 1. Deposition of a thin film of the material which needs to be patterned. 2. Application of photoresist on top of the chip. 3. Parts of the resist are selectively exposed to light using a photomask. The exposed resist undergoes a chemical transition. 4. Development of the photoresist. In the case of positive (negative) resist the exposed (unexposed) areas are removed. 5. Etching of the film which is not protected by resist. 6. Removal of the remaining photoresist using a solvent.

It is also possible to perform photolithography without an etching step by using an alternative process called lift-off. This process is schematically depicted in figure 3.2. In the first step a layer of photoresist is spin coated onto the substrate. Then lithographic exposure is done in the same way as described above. Subsequently, the resist layer is developed, leaving a pattern which is the negative of the final pattern. The film is applied after development, adhering to the uncovered substrate as well as the photoresist which is still there. Finally, the lift-off step is performed. In this step, a solvent is applied to the sample which dissolves all remaining photoresist. This detaches the film from the sample at the locations where there used to be photoresist and leaves it unharmed where it adhered directly to the substrate, creating the pattern that was also written on the mask. Lift-off is generally used when etching can damage the underling layer. Although this technique might give some problems with retention of material at unwanted places and poorly defined edges.

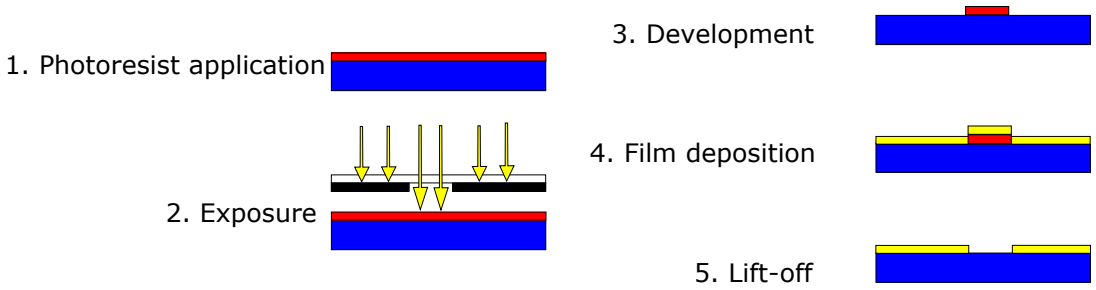


Figure 3.2 – Schematic representation of the photolithography process by lift-off using a negative photoresist. 1. Application of photoresist on top of the chip. 2. Parts of the resist are selectively exposed to light using a photomask. The exposed resist undergoes a chemical transition. 3. Development of the photoresist. 4. Deposition of a thin film of the material which needs to be patterned. 5. Lift-off of undesired material. A solvent is applied which dissolves the remaining photoresist and detached the material on top of it leaving the same pattern as written on the mask.

3.1.2 Electron beam lithography

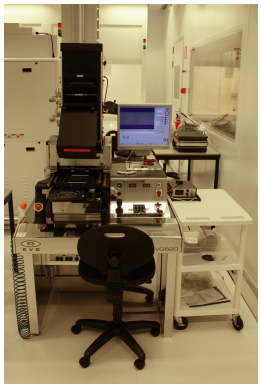
An alternative to photolithography is electron beam lithography (EBL). Instead of light, it uses a beam of electrons for exposure. Because the wavelength of an electron, according the de Broglie relation ($\lambda = \frac{h}{p}$), is much smaller than that of UV or x-ray photons, much smaller details can be achieved using EBL than with photolithography. Another difference is that, in EBL, no mask is used. Instead it uses a focused beam of electrons to write a pattern into the resist. Because of this method the process time per wafer is generally much higher. On the other hand, no expensive mask is needed. This makes that EBL is more cost efficient then photolithography when small numbers of custom design chips need to be produced, but when it comes to mass production photolithography is the best choice[26].

The process flow of EBL is comparable to that of photolithography. Also for EBL positive and negative resists are available, which usually consist out of polymers. In positive resist, the electrons break the polymers chains which makes it better soluble. While in negative resist, the electrons create crosslinks between the chains which decreases the solubility. In the MESA+ cleanroom EBL can be performed using a RAITH150-TWO (figure 3.3(b)). This system accelerates electrons with a voltage of maximum 30 kV and can write structures down to 10 nm. The electron gun can also be used to do scanning electron microscopy as is described in section 3.2.1. This is generally used for aligning the electron beam with the sample.

3.1.3 Ion beam etching

As already mentioned, etching is an important step in a lithographic process, in which excess material of a film is removed while the rest of the wafer is protected by a layer of resist. Ion beam etching (IBE) is a type of dry etching, which means that no liquid etchant is used. Instead it uses a plasma of noble gas ions to remove surface material from a wafer. This plasma is produced in a low pressure discharge chamber where a high frequency AC voltage is applied to the gas (usually argon). This field accelerates charged particles that then strip away outer electrons from the gas atoms, creating a plasma. Outside the discharge chamber, positive ions from this plasma are accelerated towards the sample, using a negatively charged grid. A neutraliser adds electrons to the plasma, turning it into a beam of neutral atoms before reaching the film. On impact, these atoms dislodge material from the surface. This creates a very uniform etching process with a high reproducibility[27].

In the MESA+ cleanroom, an Ionfab 300Plus system produced by Oxford instruments is available (figure 3.4). This system also has the capability to use reactive gasses, like oxygen, for



(a) EVG620 bond aligner for photolithographic exposure.

(b) RAITH150-TWO for electron beam exposure.

Figure 3.3 – Photos of lithography tools in MESA+ cleanroom. Source: MESA+ equipment database.

reactive ion beam etching.

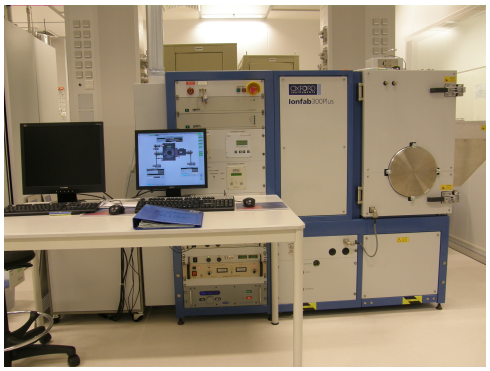


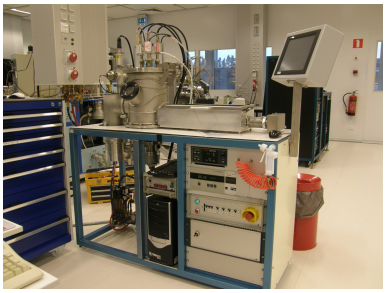
Figure 3.4 – Ionfab 300Plus for (R)IBE, in the MESA+ cleanroom. Source: MESA+ equipment database.

3.1.4 Sputter deposition

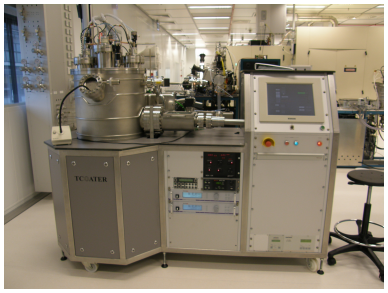
Sputter deposition is a commonly used technique for thin film deposition. The material to be sputtered is put into the process chamber in a solid form which called a target. The process chamber is kept at a low pressure of gas (usually Ar, O_2 or N_2). From this gas, a plasma is generated by applying a voltage to the target relative to the wall of the chamber. This accelerates charged particles which ionize the gas in the chamber. For electrically conductive targets the plasma is usually generated using a DC voltage while for insulating materials a high frequency AC voltage is used to prevent charging of the target. The positive ions in the plasma then accelerate towards the target. These ions erode atoms from the target which consists out of the material which needs to be sputtered. Often a magnetic field from a permanent magnet is used to confine the charged particles to a "race track" near the target (magnetron sputtering), which increases the sputtering efficiency. Part of the ejected target atoms will land on the substrate which is located at the other side of the process chamber. This creates a thin film of the target material on the substrate.[28]

In the MESA+ cleanroom multiple sputter deposition systems are available. In this project two of them are used. The first one is the Sputterke system, shown in figure 3.5(a). This machine

has one 200 W DC power supply which can be used for depositing conductive films. An other system which is called TCOater is shown in figure 3.5(b). It has two DC and two AC power supplies, which enable the system to also apply thin films of insulating materials like SiO_2. The TCOater is also able to heat up the substrate to about 400 °C during the sputtering. Both systems have been made by the TCO department of the University of Twente.



(a) The Sputterke system.



(b) The TCOater system.

Figure 3.5 – Photos of sputter deposition tools in MESA+ cleanroom. Source: MESA+ equipment database.

3.1.5 Electron beam evaporation

Another method for depositing thin films is electron beam evaporation (EBE). This process is performed in a chamber which is at ultra high vacuum ($<10^{-9}$ mbar). Here electrons are emitted from a heated filament, accelerated by a strong electric field and curved towards a target by a magnetic field. This beam of electrons locally heats the target, creating a vapour of the material which is to be deposited. The sample is mounted so that it faces the target and is exposed to the vapour. The material condensates on the sample leaving a thin film.

In EBE, the particles have less kinetic energy when they strike the sample then sputtered particles would have. This means that in EBE there is generally less island formation and that it is better suitable for lift-off. On the other side, the adhesion of a layer deposited by EBE is generally worse than that of a sputtered layer.[28]

Because of the low kinetic energy of the evaporated atoms, it is possible to create structures on the sample by using shadow mask evaporation. In this technique a shadow maks, which is basically a metal plate with holes in the desired pattern, is suspended above the sample. By evaporation this pattern is transferred to the sample.

In this project, electron beam evaporation is done using the DCA Metal-600 system (figure 3.6) which is property of the NanoElectronics group and located in the MESA+ cleanroom. With this system various materials can be evaporated including Al and Cu. The thickness of the layer can be controlled using a quartz microbalance growth rate monitor.

3.2 Characterization

Once samples have been produced, they are characterized using various methods. This can be done to understand and improve the production process or to explore the properties of the interface between Ni(111) and graphene. This section discusses the characterization techniques used in this project. First the imaging of samples using scanning electron microscopy is discussed. Then some information is given about the techniques used to do electrical characterization of the samples using transport measurements.

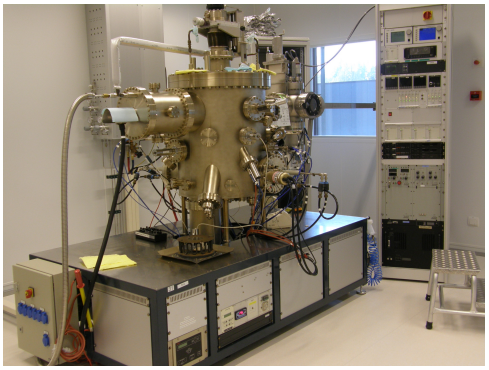


Figure 3.6 – The DCA Metal-600 system for electron beam evaporation, in the MESA+ cleanroom. Source: MESA+ equipment database.

3.2.1 Scanning electron microscopy

Because of diffraction, micro/nano structures with features smaller than a few hundred nanometre cannot be imaged properly using optical microscopy. As an alternative the scanning electron microscope (SEM), which uses electrons to image the structure, has been developed. Because the wavelength of electrons is much lower than that of the photons used in optical microscopy, features in the order of a nanometre can be distinguished. A beam of electrons is created by thermionic emission from a heated filament and acceleration by an electric field. Electromagnetic lenses are used to focus the electron beam to a spot on the sample. The interaction of electrons with the material leads to back-scattered electrons and emission of secondary electrons and X-rays that can be detected using various sensors on the SEM. With the electromagnetic lenses, the electron spot can be directed over the surface so that a scan of a certain area is made. By detecting the products of the electron-material interaction, an image of the surface can be constructed. This can give high resolution information about the sample topography or composition.[28]

In the analysis lab of the MESA+ institute electron microscopy can be performed with the NOVA 600 Nanolab (figure 3.7). This machine is also equipped with a focused ion beam (FIB) which can be used to etch the sample. This technique is not used in this project. Also the RAITH150-TWO EBL machine can use its electron gun to do scanning electron microscopy.

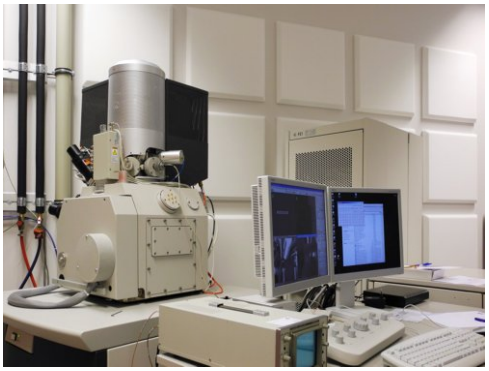


Figure 3.7 – The NOVA 600 Nanolab FIB/SEM, in the MESA+ analysis lab. Source: MESA+ website.

3.2.2 Transport measurements

When developing novel electronics it is important that the electrical transport properties of the device are well understood. To do electrical characterization, the usually micro- or nanoscale structure needs to be electrically contacted to macroscale instrumentation. Also very low temperatures and high magnetic fields are often needed. These requirements make that transport measurements in nano electronic devices is less straightforward than it sounds. First the chip on which the device is fabricated needs to be connected to a PCB (Printed Circuit Board). This is done with the West Bond Luxury II wire bonder, which can be used to connect bond pads on the chip and the PCB using thin Al (or Au) wires. Then the PCB can be further connected to instrumentation like voltage sources and multimeters. To minimize thermal broadening of energy levels, measurements are usually done at low temperature. Therefore multiple cryostat's which are available in the labs of the university are used.

One of the systems which is utilized is a tabletop cryostat produced by Oxford Instruments (figure 3.8(a)). This device can cool down samples to temperatures of about 10 K and can apply magnetic fields up to 0.04 T. Another cryostat is the physical property measurement system (PPMS) owned by the IMS research group (figure 3.8(b)). This machine can cool to a temperature of about 5 K. It is equipped with superconducting magnet which can create magnetic fields up to 9 T. When an even lower temperature is required, the Heliox system (figure 3.8(c)) is used, which can cool down to about 250 mK. It also has superconducting magnets which can apply a magentic field of about 8 T.

(a) Oxford **(b)** PPMS **(c)** Heliox

Figure 3.8 – Photos of cryostat's used in this project.

To do more accurate transport measurements often the 4-point probes method is used. In this technique four wires are attached to the sample as sketched in figure 3.9. Between the outer two, a current is sources while the inner ones act as voltage probes. This way, the resistance present in the leads and contacts is cancelled out. This is especially useful in measuring effects like superconductivity in which the resistance in comparable or lower than that of the leads.

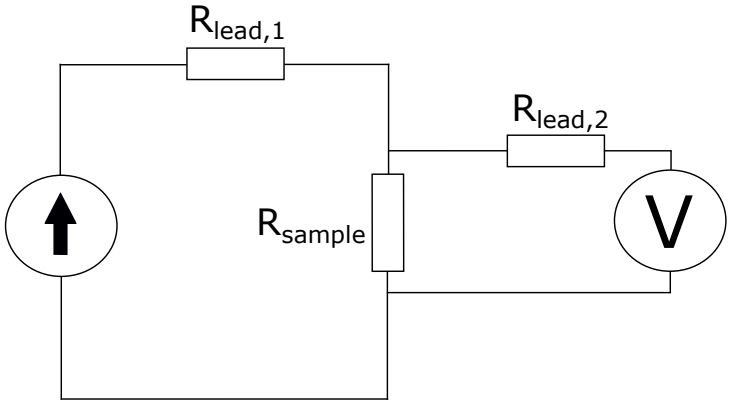


Figure 3.9 – Simple resistor network showing a 4-point probe method. This configuration allows measuring R_{sample} without unwanted contribution from $R_{lead,1}$ or $R_{lead,2}$.

Chapter 4

SiO_2 as an insulating layer

Previously Ni-graphene-Al stacks have been studied by J.M. Boter BSc.[11] and K. van der Zouw[12]. A schematic representation of their devices is shown in figure 4.1. Because the graphene patches of the right thickness are small and because a smooth surface is required to achieve a good spin-filtering, the stack cannot have an area larger than a few square micrometers. This junction is then placed at a location with a thick graphene layer and a flat plane in the underlying Ni. To avoid conduction through the sample, except the few square micrometers area where the aforementioned requirements are met, an electrically insulating layer is used.

Unfortunately previous studies could not draw firm conclusions about the spintronic properties of the Ni-graphene interface. One of the main causes for this is that the used devices contain an insulating layer out of polymethyl methacrylate(PMMA) which breaks when cooling the sample to cryogenic temperatures. This creates other conduction paths through the sample, making a potential spin filtering by the junction impossible to detect. To avoid this problem in a new series of experiments, new devices are designed and fabricated with a insulating layer of sputtered silicon dioxide (SiO_2), which should have a better resistance against temperature change.

The goal of the experiments described in this chapter is to find out how to properly create an insulating layer out of SiO_2 which can be used for fabricating devices as indicated in figure 4.1. First the resistance of the layer should be very high, preferably in the order of 1 GΩ at temperatures of around 10 K. The SiO_2 must also be able to withstand large sweeps in temperature (between 300 K and 10 K) without degradation of the resistive properties. Besides this, it is also important that it is possible to etch a hole the layer, at the location where the graphene needs to be top contacted with Al. Then it should be possible to deposit Al into this contact hole, creating a Ni-graphene-Al stack.

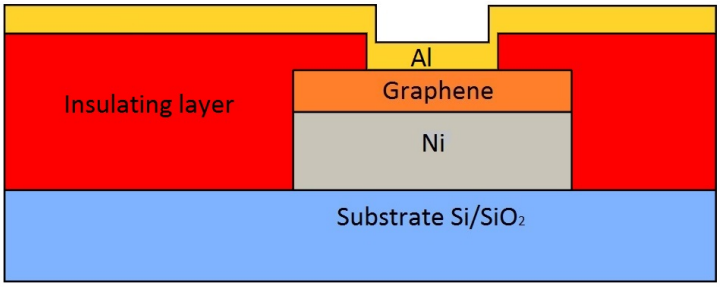


Figure 4.1 – Typical device layout used in this study. A current can be sourced between the Ni and the Al electrode. The insulating layer constrains the flow of current to a selected small area with advantageous properties. Adapted from MSc thesis J.M. Boter [11].

The thickness of the layer should be carefully chosen. If the SiO_2 layer is too thin, the insulating properties will not be good enough. When it is too thick, the step at the edge of the contact hole will be too high to form a well-connected layer of thin Al on top of the graphene. The thickness is chosen by finding the thinnest layer which still given good insulating properties. During the sputtering process of SiO_2 it is possible to add extra O_2 to the reaction chamber. This can be done to avoid the formation of SiO_x with $x < 2$. Such a layer would have worse insulating properties than a stoichiometric SiO_2 layer. Therefore also the influence of O_2 inflow during sputtering on the insulating properties is investigated. When the right SiO_2 thickness and oxygen inflow are determined, it needs to be tested how a contact hole can be etched and if the graphene can be properly top contacted. This is done by varying the etch time and analysing the sample by optical and electron microscopy. By applying a thin film of Al before analysis by electron microscopy it can be verified if it is possible to top contact the graphene using Al.

In the next section of this chapter the design and fabrication of samples for testing the SiO_2 layer is discussed. This is done by first describing the supply of wavers from which the further fabrication processes start. Then the production of samples for doing transport measurement through a SiO_2 layer is discussed. Also the design and fabrication for the etch tests is discussed in this section. In the subsequent section the results of the performed tests are discussed. These tests include transport measurements to determine the quality of the insulating layer and etch tests to determine the correct etch time. In the final section of this chapter, the conclusions about using SiO_2 as an insulating layer will be summarized.

4.1 Design and fabrication

For this part of the project, two different designs are used. The first one is used to produce samples that can be used for transport measurements to test the insulating properties of the SiO_2 layer. This design, which is described in section 4.1.2, includes the formation of bottom and top contacts so a voltage difference can be applied over the layer. The second design is used to test how etching of the SiO_2 layer can be performed. This design, which is described in section 4.1.3, defines multiple shapes which can be etched into the layer using buffered hydrofluoric acid (BHF). This way the processes of etching SiO_2 with underlining layers of graphene and Ni can be understood. The production of samples starts with 4 inch Si wafers with native SiO_2. On top of this a layer of Ni and graphene is already applied. Details of the supplied wafers can be found in section 4.1.1. These wafers are diced into samples of 11mm×11mm on which the described designs are applied.

4.1.1 Wafer supply

The fabrication of devices starts with 4 inch Si wafers on which Ni, graphene and a protective resist layer are already applied. For this project, the wafers of two different suppliers are used. Part of the wafers is externally bought from graphene-supermarket.com, a web shop from Graphene Laboratories, Inc., a company which produces various graphene products. Other wafers are produced by Derya Ataç (post-doc in the NE-group) in the cleanroom of the MESA+ institute. The production processes used by both suppliers are comparable. They both use a Si wafer on which a film of Ni is deposited. The graphene is deposited using chemical vapour deposition (CVD). In this process, the sample is heated to about 950 °C and exposed to a mixture of hydrogen and methane gas. The Ni layer acts as a catalyst which causes the methane to decompose and the C atoms to be absorbed into the Ni. When the sample is cooled down again, the C atoms migrate to the surface, leaving typically between 1 and 7 layers of graphene. The graphene arranges itself in patches with different thickness. The size of each patch is about 3-10 microns. Finally

a layer of protective photoresist is spin coated before dicing the sample in chips of 11×11 mm. This resist layer is applied to protect the graphene surface against wafer fragments during the dicing step. [29] [30]

4.1.2 Transport measurements

To test the insulating properties of the SiO_2 layer, bottom and top contacts which can be connected to a PCB need to be defined. A schematic representation of the chip layout can be found in figure 4.2. This design was made by Elmer van Geijn. The size of the bottom electrode is 3×11 mm and the three top electrodes are 1.2×7.2 mm. These dimensions are large compared to structures that are previously made in this research[11][12]. This is because having a large overlap area between the top and the bottom electrode gives statistically better information about possible leakage through the SiO_2 layer (if there is no conduction for a large overlap area, then it is very unlikely that there will be conduction in a sample with a much smaller overlap area). The bottom electrode is defined by photolithography with a positive resist. At the exposed parts, the Ni and graphene are etched away. Then a layer of SiO_2 is sputtered, covering the whole sample. Finally, the top electrodes are deposited using electron beam evaporation with a shadow mask. These electrodes consist of an Al layer with a layer of Cu on top. The reason that Al as well as Cu are applied is that, for the final devices described in chapter 5, a thin Al layer can be used for Tedrow-Meservey measurements when it is made superconducting. This layer needs to be very thin to be able to withstand high magnetic fields while retaining its superconducting state. Because the top electrode also needs to be a good conductor when there it no superconductivity an extra layer of Cu is applied. This layer also protects the Al against oxidation and makes ensures that there are no gaps in the film (especially at step edges). The top and bottom electrodes can be connected to a PCB chip using Al wires which are attached using a wirebonder. To contact the bottom electrodes the wirebonder needs to pierce through the SiO_2 layer. This is generally not very hard because this layer is relatively thin.

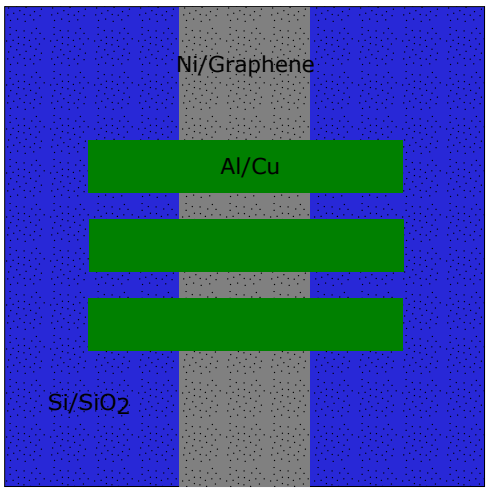


Figure 4.2 – Layout of a chip for testing the SiO_2 layer. The sample consists of a bottom electrode (grey) out of Ni covered with graphene. Over the whole sample, a SiO_2 layer is applied (dotted in black). Finally three top electrodes (green) are deposited. The resistive behaviour of the SiO_2 layer can be tested by applying a voltage difference between a top and the bottom electrode.

The fabrication starts with removing the protective photoresist layer using acetone. Then a layer of positive OiR 907/17 photoresist is spin coated onto the sample. To define bottom electrodes, photolithography is performed. For simplicity a printed overhead sheet was used

in stead of a glass mask. After exposure, the sample is baked on a 120 °C hotplate for one minute and developed in OPD-4262, leaving the resist only at the unexposed parts. Then ion beam etching is performed to etch away the Ni and graphene around the bottom electrodes. The bombardment of the photoresist with Ar during this step, cuts the length of the polymer chains. This makes the top layer of the photoresist less sensitive to solvents like acetone. This layer is removed by a 30 second oxygen plasma treatment in the TePla 300E. The remaining resist is removed by cleaning the sample with acetone. The sputtering of the SiO_2 is done using the TCOater. The thickness of the deposited layer can be determined using ellipsometry. The thickness of this layer is varied as well as the amount of O_2 that is added to the chamber during the sputtering. Finally, the top electrodes are applied by electron beam evaporation. In this machine the sample is covered with a shadow mask in which the top electrodes are defined. A layer of Al and Cu are evaporated onto the sample to form these electrodes. The finished sample is placed on a PCB chip and wires are bonded to the electrodes.

4.1.3 Etch tests

In the production process of the final device, holes need to be etched into the SiO_2 layer using a BHF solution. In this hole, Al can be deposited so that a Ni-graphene-Al stack is created. To find the optimal etch time test samples with a different design than the final samples are used.

In the final devices, EBL will be used to define contacts holes. To save time, a first estimate of the optimal etch time was determined using photolithography. This set of tests uses square contact holes of 8×8 µm. After etching, optical microscopy is used to judge if the etch time was sufficient or not. When the etch time using photolithography is estimated, a second test using EBL is done. Besides squares, also lines are etched into these samples. This makes it possible to cleave the sample through the etched lines and use SEM to look at the cross-section. This way, it can be determined if the used etching time was sufficient or not. Before cleaving, a layer of Al is applied to the sample. This is done because a sample needs to be conducting in order to be analysed by SEM and because it needs to be tested if the graphene can be properly top contacted with an Al layer. The EBL design for these tests can be found in figure 4.3.

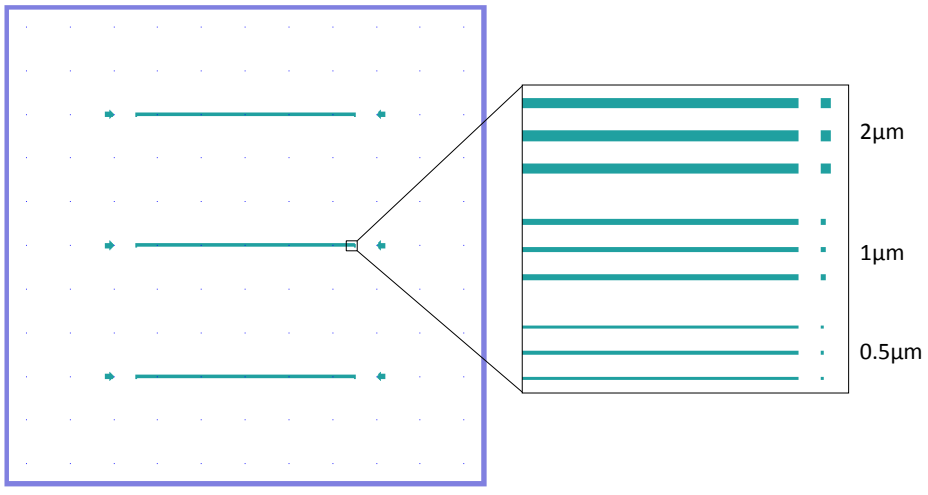


Figure 4.3 – EBL design for determining the correct etch time. The coloured lines represent the regions which receive a dose of electron beam radiation. Here the SiO_2 will be etched. Lines of 0.5 µm, 1 µm and 2 µm width are written. The lines are 5 mm long so it is possible to cleave through them and investigate the etching using SEM. Design made by Elmer van Geijn.

Also for these tests, the production starts by removing the protective layer of resist from a 11 mm×11 mm sample. Then a SiO_2 layer is sputtered onto the sample using the TCOater. The thickness of the layer and the oxygen content during sputtering depend on the results of the transport measurements.

For the tests using photolithography, a layer of positive OiR 907/17 photoresist is spin coated onto the sample. Then photolithography is performed. After exposure, the sample is baked on a hotplate for one minute at 120 °C and developed in OPD-4262, leaving 8 µm×8 µm holes in the photoresist. Then the sample is etched in a BHF solution. The etch time is varied experimentally. The remaining photoresist is removed using acetone before the sample can be examined using optical microscopy.

For the test using EBL, a layer of PMMA is spin coated onto the sample. Then EBL is performed using the design as indicated in figure 4.3. The sample is developed in 1:3 MIBK/IPA developer. After that the SiO_2 layer is etched in BHF solution. After removing the remaining photoresist using acetone, the samples are examined using optical microscopy. Samples that seem to have been well etched, are further processed to be imaged using SEM. Therefore 10 nm of Al is deposited by electron beam evaporation. Then the samples are cleaved across the etched lines, so the cross-section of these lines can be imaged using the SEM of the Nova 600 dual FIB.

4.2 Results

4.2.1 Transport measurements

Before the spin filtering at the Ni-graphene interface can be investigated, the insulating quality of the SiO_2 layer has to be checked. Therefore transport measurements are done to test the resistive properties of this layer without the presence of a contact hole. The design of these samples is discussed in section 4.1. The samples are tested at room temperature in open air in the lab, and at various temperatures in a He atmosphere inside the Oxford cryostat.

Used samples

For the transport measurements 10 samples are used. All of them are pieces from the same commercially bought wafer from the graphene supermarket. Bottom and top electrodes are fabricated as described in section 4.1.2. As can be seen in figure 4.2, every sample contains three junctions between the bottom- and top electrodes. The thickness of the SiO_2 layer of the samples is varied between 100 nm and 200 nm. During sputtering some O_2 is added to the gas inside the chamber. To test the influence of this on the resistive properties of the insulating layer, the flow of O_2 during sputtering is varied between 1 sccm and 10 sccm.[4] An overview of the applied SiO_2 thickness and used O_2 flow for every sample can be found in table 4.1.

Table 4.1 – Overview of SiO_2 thickness and O_2 inflow for the used samples.

Sample	Approximate SiO_2 thickness (nm)	O_2 inflow (sccm)
S1 & S2	100	1.0
A1 & A2	150	1.0
B1 & B2	100	5.0
C1 & C2	100	10.0
D1 & D2	200	5.0

[4] The abbreviation sccm stands for standard cubic centimetres per minute, which is a unit for gas flow.

The effect of O_2 inflow

During the sputtering of the SiO_2, some oxygen is added to the reaction chamber. To test the influence of O_2 inflow on the resistive properties of the layer, samples with a SiO_2 thickness of 100 nm are used. The oxygen inflow during sputtering is 1 sccm (sample S1 and S2), 5 sccm (sample B1 and B2) and 10 sccm (sample C1 and C2). Transport measurements on these samples have been done in air at room temperature. In the analysis of these measurements no significant influence of the O_2 inflow on the IV characteristics of the SiO_2 layer has been found.

The effect of insulator thickness

To test the effect of the thickness of the layer on its insulating properties, SiO_2 layer thicknesses of 100 nm, 150 nm and 200 nm are measured at room temperature in air. A very notable effect occurs in samples with a SiO_2 thickness of 100 nm. Most of the junctions of these samples show abrupt transitions between high and low resistance. The voltages at which this switching occurs are seemingly random and are even different for repeated measurements of the same junction. A typical measurement of the current through a 100 nm SiO_2 layer is shown in figure 4.4.

The behaviour can be explained by nanoscale filamentary switching. This effect occurs in many metal-insulator-metal systems and causes switching between high and low resistance. Wang et *al.*[31] show that this effect also occurs in oxide materials like SiO_2. The switching behaviour is mainly attributed to the formation and rupture of nanoscale conductive filaments within the oxide. These filaments could be composed of electrode metal that is transported into the oxide. Another possibility is the formation of a pathway of nano-crystals by voltage-driven reduction of the SiO_2 into Si[32]. Nanoscale filamentary switching is extensively studied because of the possible application in resistive random access memory (RRAM). Techniques exist to control the switching so that bits can be stored represented by high resistance (0) and low resistance (1). Unstable switching, like is observed in these samples, is also known to occur[33]. [34]

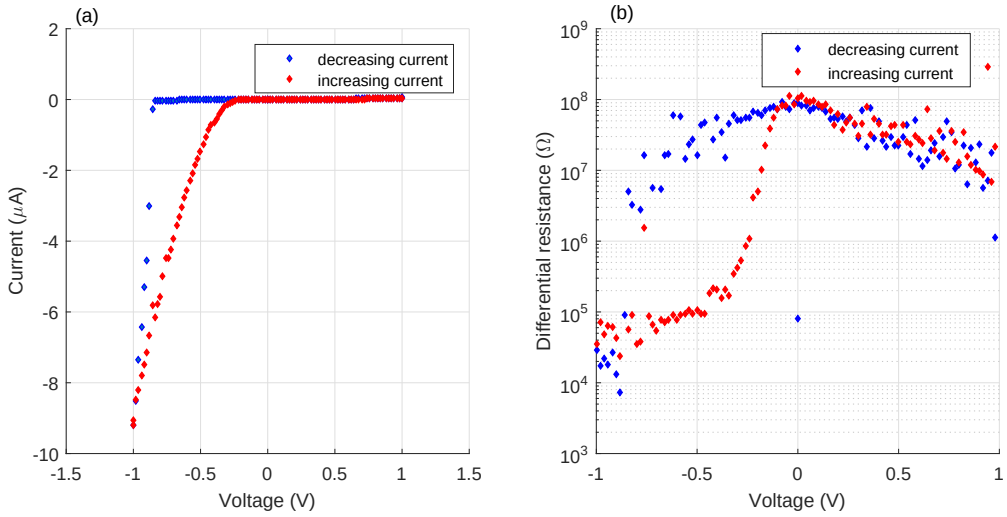


Figure 4.4 – Typical measurement of the current through a 100 nm SiO_2 layer for increasing as well as decreasing voltage. Measured on sample S2, junction 3. (a) The measured current versus voltage on a linear scale. (b) The differential resistance versus voltage on a logarithmic scale. Note: the abrupt transition in resistance of about 3 orders of magnitude at an increasing voltage around −0.25 V. This transition can be explained by nanoscale filamentary switching.

This switching behaviour almost only occurs in samples with a SiO_2 thickness of 100 nm and

not in the 150 nm and 200 nm layer samples [5]. This is probably because in a thicker layer it is harder for switchable filaments to form. Also the electric field is lower than in a thinner SiO_2 layer when the same voltage is applied over it. Because resistive switching within a layer, which is supposed to be insulating, is clearly not wanted, one of the thicker layers of SiO_2 should be used.

The IV curves of the samples with 150 and 200 nm thick SiO_2 can be sorted in two types based on their overall shape. The first type has a linear characteristic and a resistance of the order of 10 to 100 MΩ. The second type gives a non-linear asymmetric IV curve with a low current around zero and positive bias (top electrode positive and bottom electrode negative) and a much higher current for negative bias (bottom electrode positive and top electrode negative). The differential resistance for this type of IV characteristic varies between 1 to 100 MΩ. Typical measurements of both kinds of conduction can be found in figure 4.5. For the linear characteristic (figure 4.5a), it can be seen that an increasing voltage gives a larger current than a decreasing voltage. This is probably a result of capacitative charging between the top and bottom electrode. In combination with the relatively fast voltage sweep, this creates a charging and discharging, which is visible in the measurement.

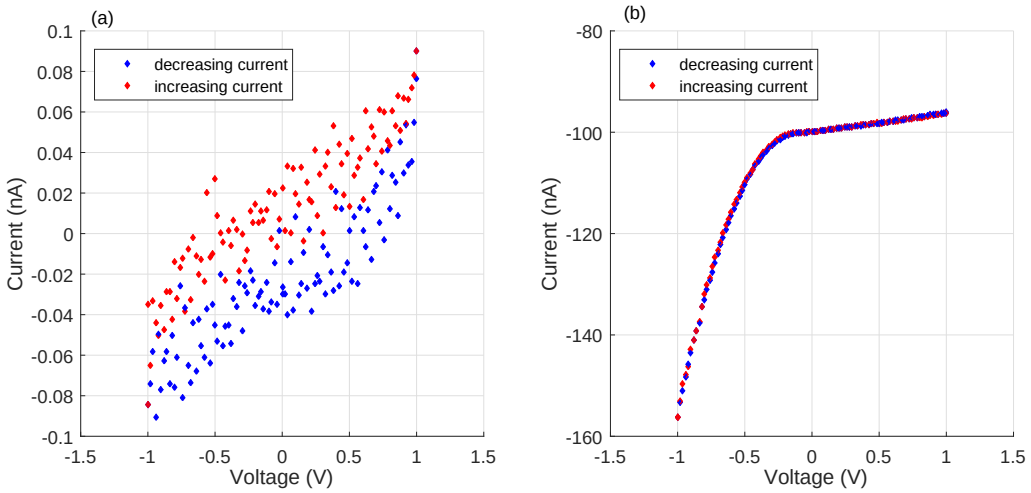


Figure 4.5 – Typical measurements of the current through a 150 nm or 200 nm SiO_2 layer for increasing as well as decreasing voltage. (a) Linear characteristic with high resistance, measured at sample A1, junction 2. (b) Non-linear asymmetric characteristic with a much lower resistance, measured at sample A2, junction 1.

Both types of conduction occur in about equal amounts of junctions. It is observed that the resistance of the 200 nm layers is generally higher than that of 150 nm layers. Therefore samples with a 200 nm layer of SiO_2 are used in further research.

Temperature dependence

Is has been shown that two typical shapes of IV curves occur in 150 nm and 200 nm SiO_2 layers. To get more insight in this behaviour, the temperature dependence of these IV characteristics is analysed. This measurement is performed in the Oxford cryostat, which is described in section 3.2.2. Sample D1 (200 nm SiO_2) was cooled down to 11 K. Next, the temperature was raised to 300 K in steps of 50 K and at each step an IV curve was measured. To reduce the effects of

[5] Resistive switching only once appeared in one of the six junctions with 200 nm SiO_2. But this junction probably damaged because the sample fell out of the sample holder.

noise, all measurements are repeated three times and averaged. A systematic offset of 50 pA at zero bias, attributed to the measurement equipment, is subtracted from all curves.

The IV curves of junctions 1 and 3 on sample D1 are roughly linear with a high resistance at low temperatures (figure 4.6). The resistance of junction 1 shows no temperature dependence, whereas the resistance of junction 3 strongly increases with temperature above 200 K.

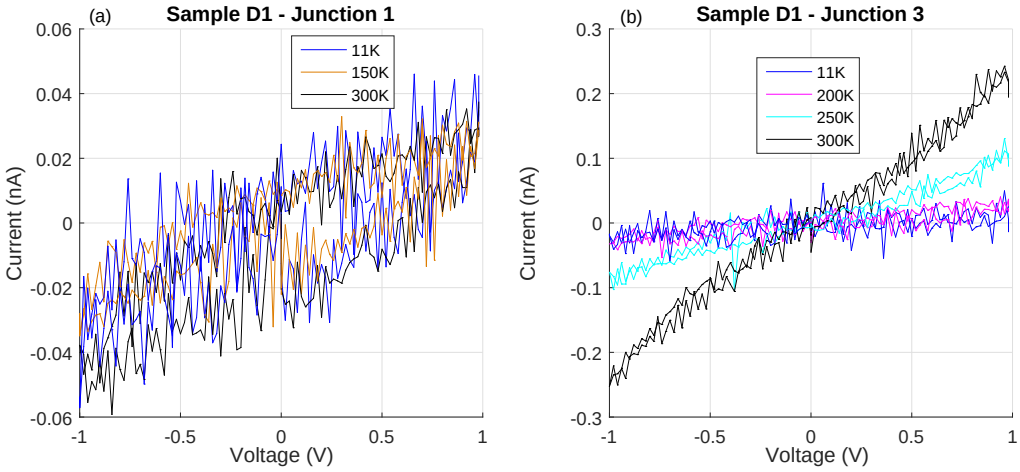


Figure 4.6 – IV curves at different temperatures for junction 1 (a) and junction 3 (b) of sample D1. Both junctions have a seemingly linear IV curve and a high resistance at low temperature. For junction 1, no temperature dependence is observed. For junction 3 however, a temperature dependence is observed in the range between 200 K and 300 K.

Junction 2 on sample D1 has an asymmetric non-linear IV characteristic at room temperature. In figure 4.7, the IV curves for this junction at different temperatures are plotted. Here it can be seen that the behaviour of the junction has a strong dependence on temperature. When the temperature decreases the resistance increases and the IV curve becomes more and more symmetric. At a sufficiently low temperature, the asymmetric behaviour disappears completely and the junction gets a high resistance (~10 GΩ) and a seemingly linear IV curve. This is the case for all IV curves up to 150 K which are shown in part c of figure 4.7. The resistance in this regime is independent of temperature.

To obtain a better understanding of the temperature dependence of this junction, we compare the conductance ($G = I/V$) at a bias of -0.95 V for different temperatures (figure 4.8). This value can be interpreted as a measure for the charge carrier concentration in the SiO_2. The static conductance is taken instead of the more commonly used differential conductance, because due to high noise it is hard to extract an accurate value for the differential conductance. The current is sampled at -0.95 V because negative voltages give a higher value of the current for asymmetric junctions. Measuring a larger current gives a smaller relative error due to noise. In figure 4.8 the natural logarithm of the conductance is plotted versus in inverse temperature. Also in this plot the two regimes that were earlier mentioned can be distinguished. In the high temperature asymmetric regime (150 K or higher), the data is in good agreement with the plotted linear fit. Meanwhile, the conductance at -0.95 V seems to be independent of temperature when the temperature gets low (colder that 150 K).

The graph in figure 4.8 provides the basis for a possible theoretical explanation of the results. In insulators defects typically introduce levels in the band gap[35]. For oxides like SiO_2 common defects are oxygen vacancies which can give rise to states close to the conduction band edge. These levels can act similar to the donor states in a n-type semiconductor[36]. The temperature dependence of the conductance in this regime, resembles that of a doped semiconductor in the

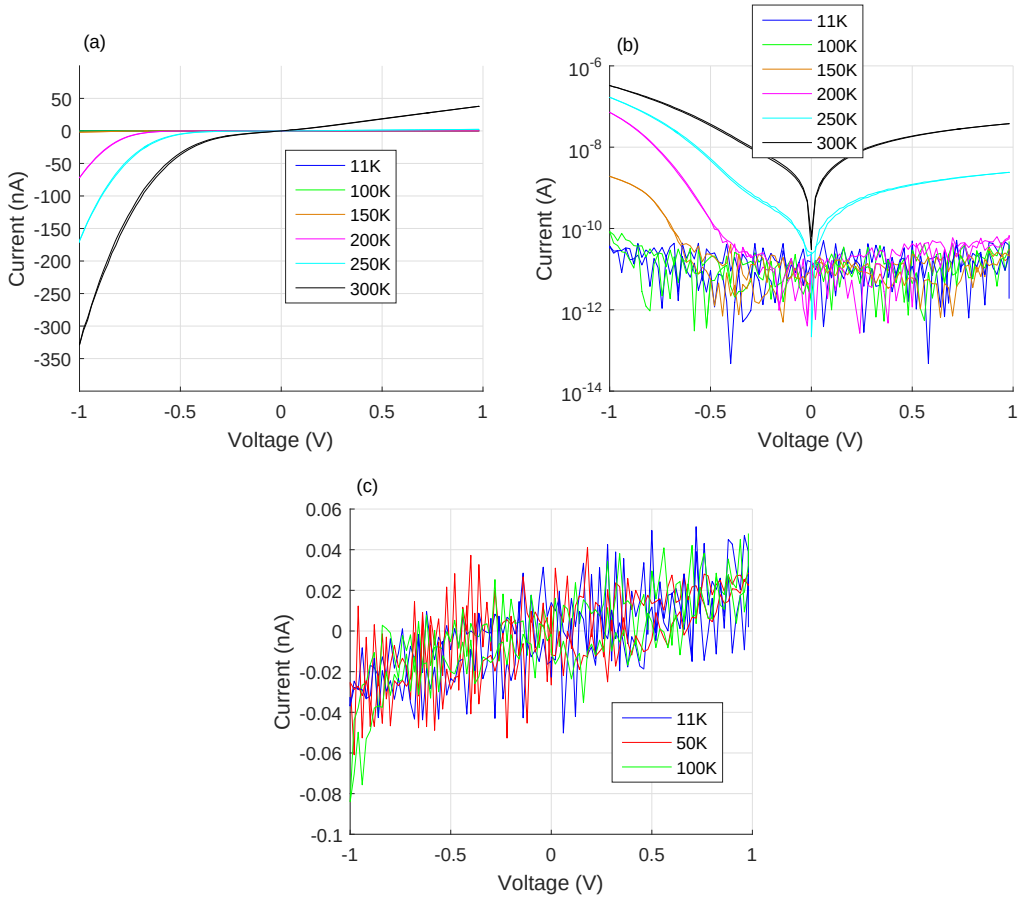


Figure 4.7 – IV curves at different temperatures of junction 2 of sample D1. (a) The current plotted on a linear scale. (b) The absolute value of the current plotted on a logarithmic scale. (c) Only the low temperature measurements showing linear IV curves are shown on a linear scale. All IV measurements up to 150 K have an high resistance, are seemingly linear and independent of temperature. At higher temperatures, the resistance decreases with temperature and the IV curves become asymmetric.

freeze-out range. Therefore, it is expected that defect induced levels cause the conductance in the asymmetric non linear regime. In the freeze-out range, the charge carrier concentration for n-type is given by[37]:

$$n(T) = \sqrt{N_D N_C} e^{-E_d/2k_bT} \tag{4.1}$$

Where n is the number of free electrons. N_D and N_C are the donor concentration and the effective density of levels in the conduction band respectively. E_D is the energy difference between the impurity and the bottom of the conduction band. It is assumed that the static conductance is proportional to the concentration of charge carriers. Therefore it can be written that:

$$G_{\text{stat}} \propto e^{-E_d/2k_bT} \rightarrow \ln(G_{\text{stat}}) = \text{constant} - \frac{E_d}{2k_b}(\frac{1}{T}) \tag{4.2}$$

Using the relation above it is possible to determine E_d from the linear trend line in figure 4.8. This way E_d is estimated to be about 0.3 eV. This means that the defects cause donor states about 0.3 eV below the conduction band. The bandgap for high quality amorphous or crystalline SiO_2 is about 9 eV[38]. The bandgap for the sputtered SiO_2, which is used in this project, is

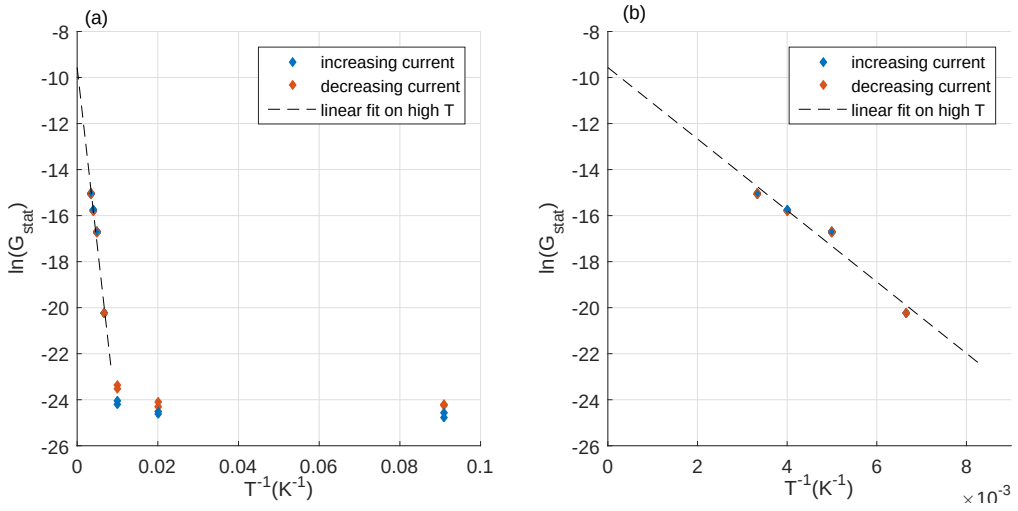


Figure 4.8 – Natural logarithm of the static conductance at $-0.95\,\mathrm{V}$ versus the reciprocal temperature. (a) In this plot it can be seen that for high temperature this gives a linear dependence while for low temperature, the temperature dependence seems to disappear. A linear fit is applied to the high temperature regime (150 K to 300 K). In (b) a zoom-in on this high temperature regime is shown. It can be seen that the linear trend line is a good approximation to the data.

assumed to be in the same order of magnitude. In a bandgap of this order, a E_d of about 0.3 eV is a plausible scenario.

From this analysis some possible explanations for the observed behaviour can be pointed out. However to draw any firm conclusions, more experiments would be needed. For the sake of time, this is not done in this project. From this analysis of the temperature dependence, it is likely that the conduction in the asymmetric regime is caused by defect induced levels within the SiO_2 band gap. The non-linear and asymmetric IV characteristic in these measurements can be explained by a Schottky-barrier at the interface between SiO_2 and Ni. In Junction 1 and 3 the density of defects is probably too low to form a band of impurities inside the SiO_2 bandgap. The linear IV characteristic seen in these junctions and at low temperature at junction 2 of sample D1, can be explained by ohmic leakage probably through a metallic filament in the SiO_2 layer. This conduction mechanism has a relatively weak (junction 3, sample D1) or no (junction 1, sample D1) temperature dependence and a high resistance. This leakage is probably also present in junction 2 of sample D1 at room temperature, but not visible because the conduction from the defect induced levels is much larger. Only at low enough temperature, this contribution freezes out and the linear IV characteristic with a resistance in the order of 10 GΩ becomes visible. This fact is very important when it comes to the further production of a device, because a high resistance of the insulating layer (at least at low temperature) is needed in the final experiment.

Effect of temperature cycles

It has now been shown that the resistance of the SiO_2 layer gets very high when it is cooled down to low temperatures. Because it would be convenient if samples could be cooled down and heated up again without damaging them, it is important to know if the layer keeps its good insulating behaviour after going through multiple temperature cycles. Therefore both samples with a 200 nm SiO_2 layer (D1 and D2) are cooled down from room temperature to 11 K, then heated up again to 300 K, before cooling down and heating up one more time to 11 K and 300 K

respectively. [6] Just like in the temperature dependence analysis, also these measurements are repeated at least three times, so the IV-curves can be averaged for noise reduction and compared to each other to check reproducibility. Also these measurements are performed using the Oxford cryostat and a Keithley 2401 sourcemeter.

In figure 4.9 the effect of temperature cycles on the IV-characteristic of junction 1 and 3 of sample D1 can be seen. As already discussed before junction 1 shows no temperature dependence while junction 3 does. However, it is visible that for both junctions it does not matter if there already have been one or two temperature cycles before. This is an indication that the sample has not suffered any damage caused by cooling down and warming up again.

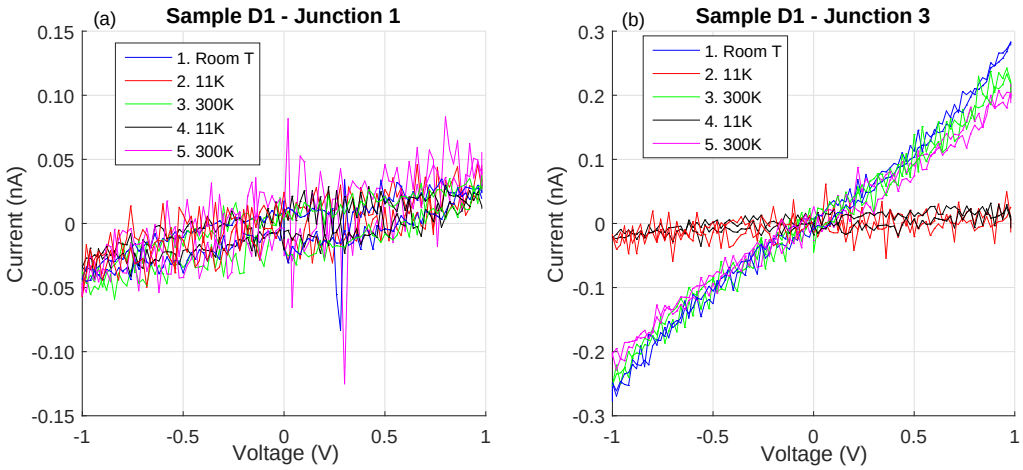


Figure 4.9 – IV curves taken at different temperatures within a temperature cycle test, in which the sample has been cooled down an heated up twice. (a) Junction 1 of sample D1. (b) Junction 3 of sample D1. It can be seen that for both junctions the IV curves do not significantly change after one or two temperature cycles. This indicates that the samples are not damaged by the temperature cycles.

This test also has been done for junctions which show an asymmetric IV-curve. The result of this is shown for junction 2 of sample D1 in figure 4.10. It has already been shown before that the temperature dependence of this junction is very strong. To also keep the low temperature results clear, the current has also been plotted on a logarithmic scale, as well as on a linear scale showing only low temperature results. The figure shows that also junctions showing an asymmetric IV curve do not seem to be influenced by temperature cycles.

This test has also been performed at sample D2, showing similar results, with a resistance in the order of 10 GΩ for temperatures below 150 K and no significant influence of the cycles. This means that out of six measured junctions, none of them show any influence of the temperature cycles on the IV characteristic of the junction. From this it can be concluded that, for all observed junctions, cooling down and heating up does not significantly influence the insulating properties of the SiO_2 layer.

4.2.2 Graphene damage by SiO_2 sputtering

From the transport measurements performed at SiO_2 layers with thicknesses 100 nm, 150 nm and 200 nm, it can be concluded that a thickness of 200 nm gives the best insulating properties.

[6] For sample D1, the temperature cycle test where combined with the temperature dependence test (which has already been discussed). So the first time this sample was heated up from 11 K to 300 K, this was done in steps of 50 K.

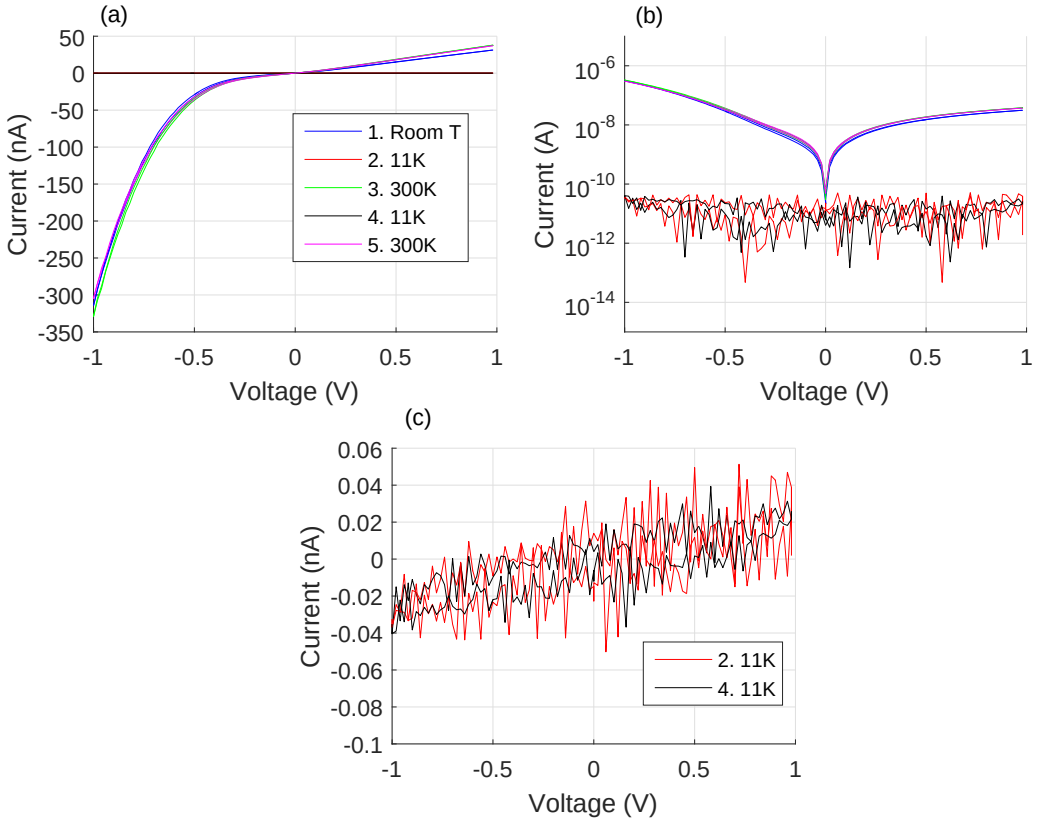


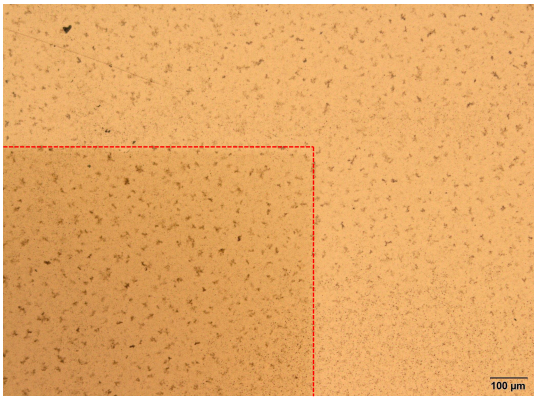
Figure 4.10 – IV curves taken during a temperature cycle test, in which junction 2 of sample D1 has been cooled down an heated up twice.(a) Linear plot showing curves taken at low as well as high temperature. (b) Logarithmic plot showing curves taken at low as well as high temperature. (c) Linear plot only showing curves taken at low temperature. These graphs show that also a junction with an asymmetric IV curve does not show seem to be influenced by the temperature cycles.

Although no significant influence of O_2 inflow during SiO_2 sputtering has been found, it has been decided that an O_2 inflow of 5 sccm should be used in producing the final device. This decision is based on the theoretical predication that a higher O_2 content during sputtering should avoid the formation of SiO_x with $x < 2$.

However, it turns out that the graphene flakes are damaged by the oxygen which is let into the sputtering chamber. This is tested by using a shadow mask while sputtering, so that at a part of the sample no SiO_2 is deposited. In figure 4.11, the result of this test is shown for (a) 1 sccm of O_2 inflow and (b) 5 sccm of O_2 inflow. The darker coloured regions in these images indicate where the SiO_2 is deposited. It can be seen that in this case of 5 sccm O_2 inflow, the graphene flakes in the exposed areas are largely removed, while this is not the case with a O_2 inflow of 1 sccm. From this it can be concluded that the removing of the graphene flakes during sputtering is caused by the O_2 flow into the chamber.

To avoid damage to the graphene flakes, the SiO_2 layer is applied in two steps. In the first step a layer in sputtered for 5 minutes without adding O_2 to the chamber. This creates a thin SiO_2 layer which protects the graphene flakes from O_2 damage. Then the second layer is applied by sputtering for 70 minutes in which 5 sccm of O_2 is added to the chamber. This results in a total SiO_2 thickness of about 200 nm.

(a) 1 sccm of O_2.



(b) 5 sccm of O_2.

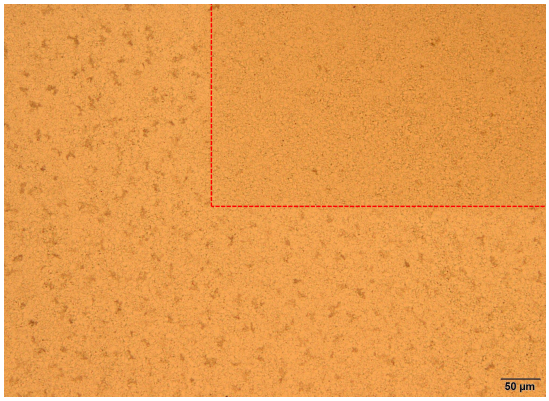


Figure 4.11 – Optical microscopy images of SiO_2 deposited onto a plain Ni-graphene sample using a shadow mask for 1 sccm(a) and 5 sccm(b) of O_2 inflow during sputtering. The framed regions indicate where the SiO_2 has been deposited. It can be seen that for 5 sccm of O_2 the graphene flakes in the sputtered area are largely removed while this is not the case at the sample with 1 sccm of O_2. These samples are produced and imaged by Elmer van Geijn.

4.2.3 Outbaking procedure prior to SiO_2 sputtering

At some of the SiO_2 layers which are sputtered onto a Ni-graphene surface, blue spots appear with a diameter between 5 µm and 10 µm. Within these spots, also some rings are visible (figure 4.12). These spots are presumably caused by gas bubbles that form between the SiO_2 and the graphene. This hypothesis is supported by the rings which can be explained by so called Newton's rings formed by interference of light reflected from a flat surface and an adjacent spherical surface. In this case, they are probably formed by reflection from the Ni/graphene surface and the curved inner surface of the SiO_2 layer. The gas that fills the bubbles is expected to be desorbed from the Ni. After SiO_2 sputtering gas cannot escape any more and gets trapped under the SiO_2 layer. It is expected that this gas is H_2 which originates from the decomposition of absorbed water, while the O atom binds to non-stoichiometric SiO_x.

It is unknown if these spots have a negative influence on the insulating properties of the SiO_2. However it is likely that when a contact hole is etched onto such a spot, under-etching occurs leading to poorly defined junctions. Therefore it is desirable to avoid the formation of "blue spots" as much as possible.

An approach which is used to avoid the formation of spots is outbaking the samples in vacuum before the deposition of SiO_2. In this step, all the gas would be desorbed from the sample so no bubbles can be formed after applying SiO_2. It is important that the sample stays in vacuum between outbaking and sputtering, so no new contaminations can be absorbed. To accomplish this, the outbaking step is performed in the TCOater system which is also used in the subsequent sputtering step. In the vacuum of this system (10^{-6} mbar), the sample is heated to 170 °C so it can bake for at least 90 minutes. Then cooling gas is let into the chamber for about three hours to cool the sample back to room temperature. Finally the SiO_2 sputtering is done with the recipe described in section 4.2.2. New samples that have been produced with this outbaking procedure do not show blue spots anymore. This also supports the idea that these spots are bubbles of gas.

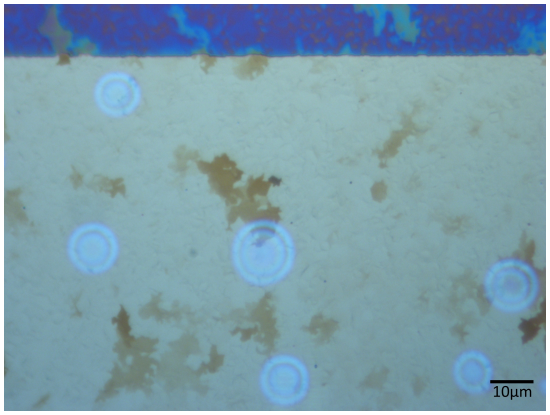
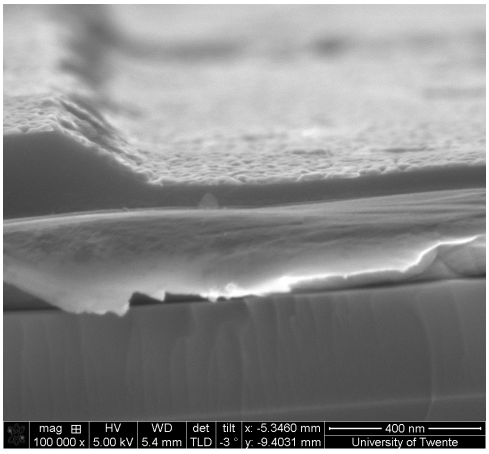


Figure 4.12 – Optical microscopy image of SiO_2 deposited onto a Ni-graphene bottom electrode. The blue spots that are visible are probably gas bubbles that have formed under the SiO_2. Inside the spots, circles are visible which are likely to be Newton's rings.

4.2.4 Etching of contact holes

To properly top contact the graphene, holes need to be etched in the SiO_2 layer. The BHF etching time is optimized by tests using optical lithography and EBL as described in section 4.1.3. The tests using optical lithography estimated the time to etch away all the SiO_2 to be around 70 s. The required etch time is determined more exactly using EBL with the design of figure 4.3. After etching the samples are coated with 10 nm of Al and cleaved so that the cross-section can be analysed using SEM. In figure 4.13a, the SEM image of a line which is etched for 70 s is shown. It can be seen that the SiO_2 (dark grey) is not etched away completely. Therefore a longer etch time is needed. In figure 4.13b, the SEM image of a line which is etched for 95 s is shown. This image shows that in the etched area, the SiO_2 is completely removed and that the Al, which has a flake-like pattern, seems to lie directly on top of the graphene. From this, it can be concluded that an etch time of 95 s is probably sufficient to create holes in the SiO_2 layer, in which top contacts can be applied to the graphene.

(a) 70 s of etching.



(b) 95 s of etching.

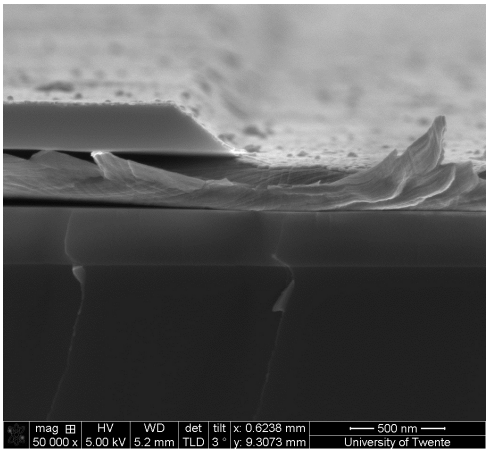


Figure 4.13 – SEM images of a cross-section of an EBL patterned SiO_2 layer after 70 s (a) and 95 s (b) of BHF etching. (a) 70 s of etching still leaves some SiO_2 on the patterned area. The etch time is not sufficient. (b) 95 s of etching leaves no SiO_2 is the patterned area. As a result, the Al is applied directly to the graphene in this region. (Images by Johnny Sanderink)

4.3 Conclusions

The goal of the experiments described in this chapter was to find out how to create an insulating layer out of SiO_2, which can be used to fabricate a device for investigating the spintronic effects at the interface between Ni and graphene. In SiO_2 layers with a thickness of 200 nm, resistances in the order of 10 GΩ have been measured when the samples are cooled down to temperatures below 150 K. This resistance is high enough for the fabrication of devices. Also the effect of temperature cycles (i.e. cooling down to around 10 K and heating up again to 300 K) on these layers has been tested. For all six measured junctions, no influence of the temperature cycles on the IV characteristic was seen.

Examination of the samples after SiO_2 sputtering with different O_2 inflow, using optical microscopy shows that graphene is damaged by O_2 which is inserted into the chamber during sputtering. Therefore an alternative recipe is chosen in which first a very thin layer of SiO_2 (5 minutes of sputtering) is applied without additional O_2. Then the rest of the 200 nm SiO_2 (70 minutes of sputtering) is applied while 5 sccm of O_2 is flowing into the chamber. Also an in situ outbaking procedure is added prior to SiO_2 deposition to avoid the formation of blue spots, which are likely to be caused by gas bubbles trapped between the Ni and SiO_2 layer.

After the recipe for SiO_2 has been determined, the etching of contact holes and the deposition of Al has been tested. It turns out that an etch time of 95 s is sufficient to etch a contact hole into 200 nm SiO_2 in which the graphene can be contacted using Al. Considering the experiments described in this chapter, it can be concluded that SiO_2 when sputtered according previously described recipe, seems a promising candidate for providing the insulating layer in spintronic devices based on the graphene-Ni(111) interface.

Chapter 5

Fabrication of spintronic devices

In this chapter, the fabrication and initial characterization of spintronic devices based on the graphene-Ni(111) interface are discussed. Because the graphene patches of the desired thickness are small, a microscale device is produced which employs a SiO_2 layer to avoid conduction through the sample except through the few square micrometers where the contact is defined. In chapter 4, a recipe for sputtering SiO_2 has been determined which seems promising for fabricating these kind of devices. On the basis of this recipe, devices with a contact hole are produced, which can be used to measure conduction through a Ni-graphene-Al stack. This can give valuable information about the spintronic properties of the graphene-Ni(111) interface. The next section in this chapter discusses the design and fabrication of these devices. Then the results of device fabrication and transport measurements are presented. Finally, some conclusions about the fabrication and performance of spintronic devices based on the Ni(111)-graphene interface will be discussed.

5.1 Design and fabrication

To create a micro scale Ni-graphene-Al stack, the chip layout as indicated in figure 5.1 is used. This design (made by Elmer van Geijn) defines six devices on one sample. The production starts with a 11 mm×11 mm chip containing a film of Ni and graphene on a Si substrate. These chips are diced from a 4 inch wafer produced by Derya Ataç as described in section 4.1.1. The bottom electrode is defined by photolithography with a positive resist. At the exposed parts, the Ni and graphene are etched away. Then a layer of SiO_2 is sputtered, covering the whole sample. To do a proper experiment on the properties of the Ni(111)-graphene interface, a contact needs to be created on a thick graphene flake and smooth part of the surface. This is done by creating a hole using EBL and BHF etching of the SiO_2 layer. To properly aim the electron beam, alignment markers are sputtered next to the bottom electrode and at the corners of the sample (zoom-in of figure 5.1). By optical microscopy a suitable location for the contact hole is chosen before doing EBL and BHF etching. Finally, the top electrodes are deposited using electron beam evaporation. These consist of an Al layer with a layer of Cu on top. The Al layer can be used to do Tedrow-Meservey measurements if it is $<$10 nm thick and kept at sufficiently low temperature to maintain a superconducting state under application of a magnetic field of a few Tesla. The Cu is included to ensure electric contact over step edges and prevent oxidation of Al. To do transport measurements trough the contact hole, the top and bottom electrodes are connected to a PCB chip using Al wires. To contact the bottom electrodes the wirebonder needs to pierce through the SiO_2 layer. This is generally not very hard because this layer is relatively thin. A detailed recipe for the production of these samples can be found in appendix A.

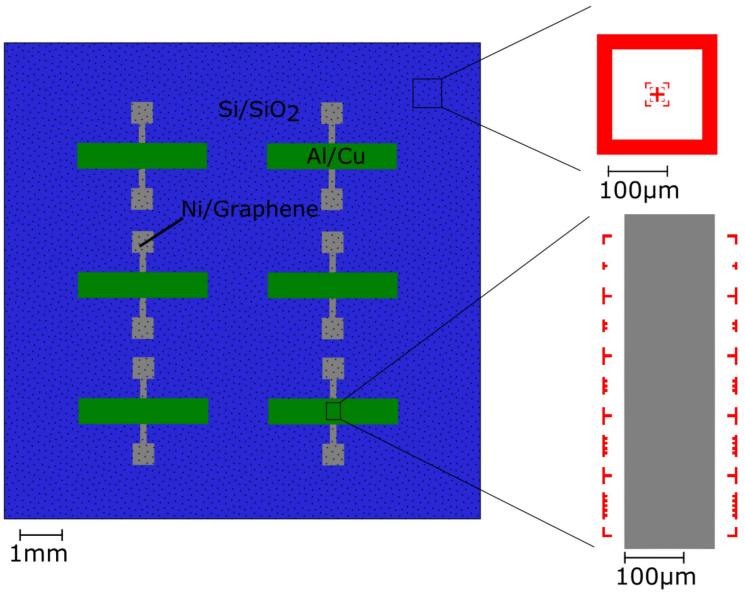


Figure 5.1 – Layout of a 11 mm×11 mm chip containing six devices. The sample consists of bottom electrodes (grey) made of Ni covered with graphene. Over the whole sample a SiO_2 layer is applied (dotted in black). Next to the bottom electrode and at each corner of the sample, alignment markers are sputtered (shown in red, in the zoom on the right). A small contact hole is etched into the SiO_2 so the graphene can be top contacted (not shown). Finally top electrodes (green) are deposited. A current can be sent trough the contact hole and Ni(111)-graphene interface by applying a voltage difference between the top and bottom electrode.

5.1.1 Bottom electrodes

The fabrication starts with removing the protective photoresist using acetone. Then a layer of positive OiR 907/17 photoresist is spin coated onto the sample. To define bottom electrodes photolithography is performed. A description of the used mask can be found in appendix C. This mask contains three different designs for bottom electrodes with widths of 150 µm, 100 µm and 60 µm. After exposure, the sample is developed in OPD-4262 for 29 seconds, leaving the resist only at the unexposed parts. Then ion beam etching is performed for 55 minutes to etch away the Ni and graphene around the bottom electrodes. The bombardment of the photoresist with Ar during this step damages the polymer chains and leads to crosslinking. This makes the top layer of the photoresist less sensitive to solvents like acetone and DMSO. This layer is removed by a 30 second oxygen plasma treatment in the TePla 300E. The remaining resist is removed by cleaning the sample in a ultrasonic bath of 80 °C DMSO for 30 seconds. A schematic cross-section of the chip before and after fabrication of the bottom electrode can be found in figure 5.2. In between fabrication steps, the sample is placed on a hotplate to remove any residual water from the surface. Details of these steps can be found in the recipe of appendix A.

5.1.2 SiO_2 layer and contact holes

After the bottom electrodes have been fabricated, the SiO_2 insulating layer is sputtered using the TCOater. This is done according to the recipe described in chapter 4, for sputtering of a 200 nm layer. First the outbaking procedure is performed at 170 °C to avoid the formation of

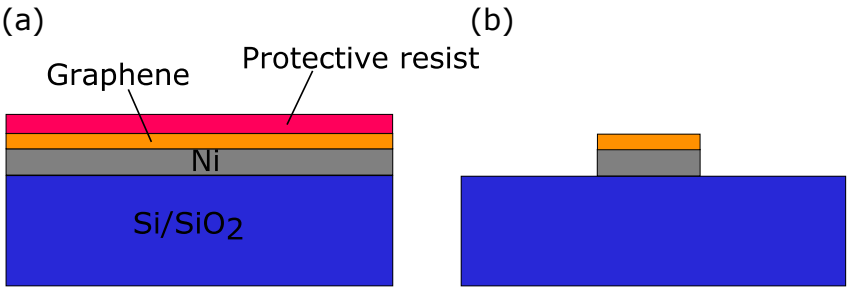


Figure 5.2 – Schematic representation of the sample cross-section. (a) The chip as supplied by Derya Ataç, consisting of a Si wafer with native SiO_2 on which a Ni film is applied. On this film graphene in grown. The chip is covered with a layer of protective photoresist. (b) The chip after the first fabrication steps in which the bottom electrodes are fabricated.

blue spots which are probably gas bubbles. Then the first few nanometres are sputtered without adding O_2, the rest of layer is applied while 5 sccm of O_2 is added to the chamber.

After the SiO_2 layer is deposited, markers for aligning the EBL are applied. This is done using photolithography with a lift-off procedure using positive resist. Because these markers are important for positioning the contact hole, effort is done to define well located alignment markers with edges which are as sharp as possible. Therefore hexamethyldisilazane (HMDS) is spin coated onto the sample before spin coating OiR 907/17 photoresist. HMDS makes the sample surface more hydrophobic which improves adhesion of the photoresist. Then another lithographic exposure is done using the mask shown in appendix C. This mask contains three designs for alignment markers, in which the separation between the two rows of markers is 225 µm, 200 µm or 125 µm. After exposure, the sample is developed in OPD-4262 for 29 seconds, leaving the resist as a negative of the alignment markers. Then two layers of Ti(2 nm) and Pd(18 nm) are sputtered using the Sputterke system. The markers are completed by doing lift-off using a bath of 80 °C DMSO. This removes all the photoresist and the Pd and Ti which is on top of it, leaving the metals only where the alignment markers are defined.

Subsequently, the location for the contact hole is chosen. This is done using optical microscopy. This hole is usually a square of a few μm^2. According to the publications by Karpan *et al.*[7][8], which are described in section 2.5, there are some requirements to get good spin filtering. The first is that the graphene should be thick enough. At 5 layers or more the spin filtering is predicted to be complete. In the work of J.M. Boter[11], images made by optical microscopy have been compared to Raman spectroscopy measurements. This comparison confirmed that darker flakes in optical images correspond to thicker layers of graphene. Also a rough estimation of the number of graphene layers of a flake, based on how dark it is, is made. This indicates that the darkest spots on a typical wafer should be thick enough. Another requirement to achieve good spin filtering is that the interface should be as smooth as possible. This is because according to the numerical calculations by Karpan et *al.* interface roughness can decrease the spin filtering effect. Furthermore, a smooth surface also gives a higher change of being located at a single Ni grain with a good lattice match between the Ni and the graphene. As shown in previous research[12], the surface structure of the Ni can be imaged by quenching the aperture of the optical condenser of the microscope. This decreases the angular divergence of the light exposing the sample, leading to an increased contrast of the surface morphology. Figure 5.3 shows a graphene flake imaged using an optical microscope with (a) and without (b) aperture quenching. By imaging the surface structure, the contact hole can be located at a location where no ridges appear, so the substrate is likely to be smooth. Here it is also more likely that, as assumed in the calculation, the contact is created at a single Ni grain where the graphene well

matches the Ni surface. When a suitable location for the contact hole is determined, an image is taken which shows the location of the flake relative to the alignment markers.

Then an EBL step is performed which begins with spin coating a layer of PMMA resist. On this resist, electron beam exposure is done. The sample is aligned with its design by using the integrated SEM of the RAITH150-TWO. Because the alignment markers give good contrast in an optical microscope as well as a SEM, they are used to locate the spot where the exposure for the contact hole needs to be done. After the exposure is done, the sample is developed in 1:3 MIBK/IPA developer for 33 seconds, leaving the PMMA everywhere except the few square micrometers where the contact hole will be located. Then holes are etched into the SiO_2 by doing 95 seconds of BHF etching. The remaining PMMA is removed with 80 °C DMSO. In figure 5.4(a), a schematic cross-section of the sample after these fabrication steps is shown.

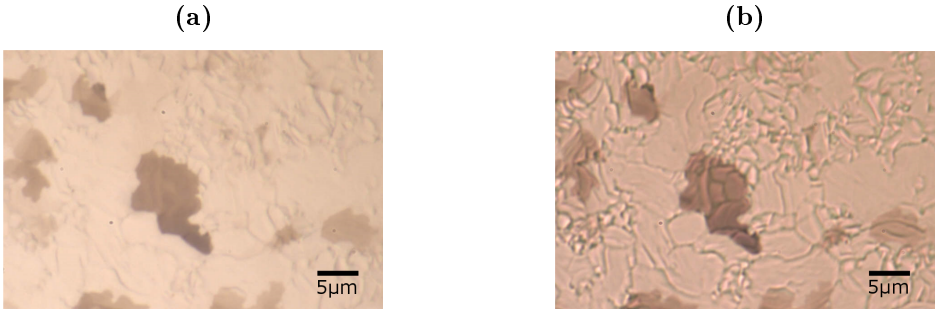


Figure 5.3 – Optical microscopy images of a graphene flake by using normal settings (a) and by quenching the aperture (b) which reveals the surface structure of the Ni.

5.1.3 Top electrodes

To make electrical contact with the graphene layer trough the contact hole, a top electrode is deposited using another lithography step with a lift-off procedure. In the general recipe, as described in appendix A, photolithography is used. In addition, also an alternative procedure employing EBL, has been developed.

The photolithography procedure starts with spin coating a layer of OiR 907/17 photoresist. Exposure is again done with the mask shown in appendix C, using one of the three designs for top electrodes. This mask contains designs for top electrodes of 300 µm, 600 µm and 900 µm width. The sample is developed in OPD-4262 for 29 seconds leaving the resist as a negative of the top electrodes. Using electron beam evaporation ~10 nm of Al and Cu are deposited onto the sample. Finally the lift-off step is performed using acetone. This dissolves all remaining photoresist and leaves the metal film only where the top electrodes are defined. This is schematically shown in figure 5.4(b). With this step, the fabrication of this sample is completed.

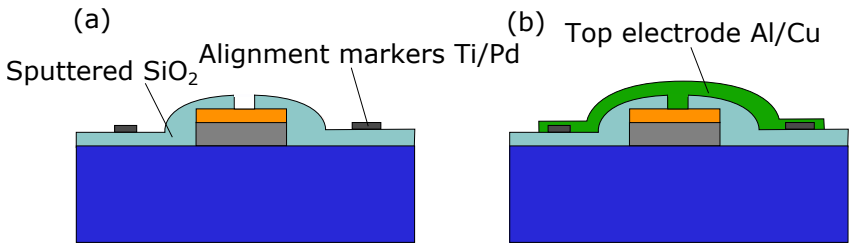


Figure 5.4 – Schematic representation of the sample cross-section. (a) The chip after sputtering of SiO_2 and etching of the contact holes. The alignment markers are used for aligning the EBL-machine. (b) The chip after deposition of top electrodes.

Another method of producing top electrodes is developed, using EBL to do a lift-off procedure. This enables the production of narrower top electrodes. Thereby reducing the area of overlap between the bottom and top electrode making unwanted conduction through defects in the SiO_2 layer less likely. A disadvantage is however that it is more time consuming to do EBL than photolithography, increasing the total production time of the devices. These electrodes have a designed width of 10 µm, are 600 µm long and have bonding pads of 200 µm×200 µm. This decreases the area of overlap between the top and bottom electrode by a factor of 30 compared to the smallest photolithography design.

Based on the design for the contact holes, locations for the top electrodes are chosen. Then PMMA is spin coated onto the sample and the electron beam exposure is performed. After developing the sample with 1:3 MIBK/IPA, the top electrode is deposited by electron beam evaporation. The sample is finished by performing the lift-off using hot DMSO and acetone, leaving the metal only where the top electrodes are defined.

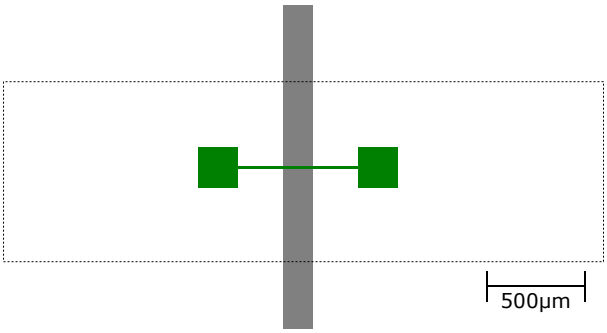


Figure 5.5 – Layout of an EBL defined top electrode (green) with respect to a bottom electrode (grey). For comparison the dimensions of a photolithography defined top electrode with a width of 900 µm are indicated by the dashed line.

5.2 Results

5.2.1 Device fabrication

The production process for bottom electrodes is similar to the recipe developed in previous research [11]. Therefore this part of the process is relatively straightforward. A problem which does occur sometimes is the retention of resist after oxygen plasma treatment and the DMSO cleaning step (see figure 5.6(a)). This can be a result of insufficient plasma or DMSO treatment. Doing another plasma treatment is not possible because this would damage the graphene. It is expected that a device which is located on top of a layer of resist shows a very high resistance and probably no physically interesting effects. Therefore, retention of resist is an effect which can lower the yield of good devices from the production process.

The SiO_2 layer is applied using the recipe described in chapter 4. The fabrication of Ti and Pd alignment markers using lift-off has not been used on these kind of samples before. For the alignment of the EBL machine, it is important that the markers are clearly visible and have their intended shape with preferably sharp edges. An optical microscopy image of the alignment markers compared to their design can be found in figure 5.6(b). This image shows that the edges of the shapes are somewhat rounded compared to their design. This was expected because defining sharp edges using photolithography with lift-off is not straightforward. However, because the contact holes are aimed at relatively large Ni grains, some misalignment is acceptable as long as this is within about 1 µm of the intended location. For this purpose, the

shape of the makers is sufficient for proper alignment of the EBL machine.

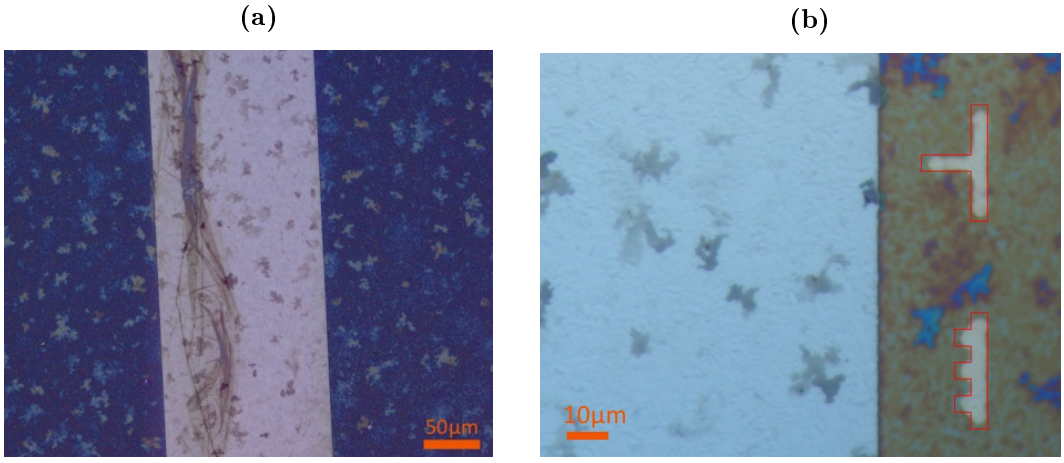


Figure 5.6 – Optical microscopy images of the device fabrication. (a) Image of a bottom electrode showing remains of resist. (b) Image of alignment markers next to a bottom electrode. The red frames show the design of the markers.

In a computer program called KLayout, a design is made defining the location of the contact holes with respect to the alignment markers. With this design, the EBL machine can be programmed. The markers at the corners of the sample are used to correctly align it with the EBL design. After e-beam exposure, the sample is developed and etched, creating the designed holes in the SiO_2. The etching of the contact holes is a critical step in the production process. Because graphene is a inert material, to which SiO_2 does not have a good adhesion, underetching is likely to occur. In optical microscopy, this can be seen as a blue area around the contact hole (see figure 5.7(b)). When a top contact is applied to an underetched hole, this may cause a larger area than the intended square to be contacted. When this area contains a too thin or non-uniform graphene layer or a too large Ni roughness, interesting effects like spin filtering may be strongly hampered. Therefore, underetching of contact holes is also an effect which will lower the fabrication yield of good devices.

Finally the device is completed by applying a electron beam evaporated top electrode, using the previously described lift-off procedure with photolithography or EBL. This metal layer should make direct contact with the graphene inside the contact hole, as was the case for the tests described in section 4.2.4.

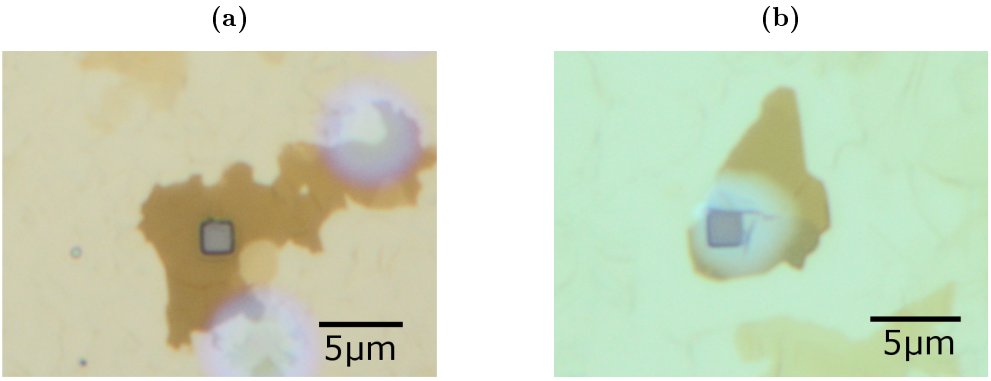


Figure 5.7 – Optical microscopy image of the contact hole after BHF etching of the SiO_2. (a) A contact hole that is etched correctly. (b) A contact hole that is surrounded by a blue area, indicating underetching of the SiO_2.

5.2.2 Towards TAMR measurements

In the PPMS cryostat transport measurements have been performed (by Elmer van Geijn) as exploration towards doing a extensive analysis of the TAMR effect. The used sample contained four devices with a 1.5×1.5 µm contact hole and top electrodes consisting of Al(20 nm)/Cu(30 nm). The device, which is located on the flake of figure 5.8, is measured in detail. This flake has a smooth region where the graphene layer, based on its colour, must be relatively thick. The measurement is performed using a four probe method in which the current is sourced between the ends of the top and bottom electrodes. The voltages are measured between the other ends of the same electrodes. This way only the voltage drop over the contact hole is detected. In every measurement, the bias current is swept back an forth multiple times, resulting in eight data-points for every positive bias current and ten data-points for every negative current. In the following graphs, the averaged curves are plotted.

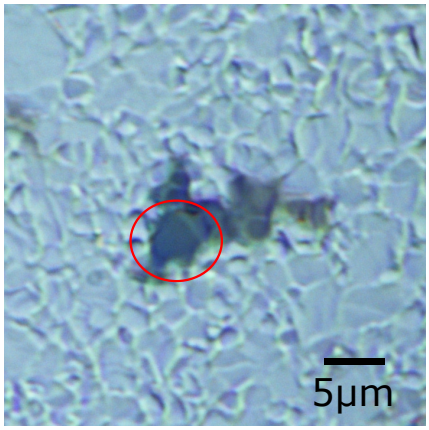


Figure 5.8 – Optical image of the contacted graphene flake. The red circle marks the plane at which the contact hole is aimed.

Figure 5.9 shows the measured voltage and the resistance of the junction at room temperature and 10 K. At room temperature, an ohmic behaviour is observed with a resistance of about 75 kΩ. When the temperature is 10 K, the junction shows a tunnelling-like non-linear behaviour. There are reports that claim that a transferred monolayer of graphene acts as a tunnel barrier[39][40]. However, it is unknown if this also holds for multilayer graphene grown on Ni(111). From these measurement, no firm conclusions can be drawn about the occurring transport mechanisms. In future research, transport measurements should also be performed at intermediate temperatures. Also multiple devices should be characterized to exclude the possibility that these characteristics are a result of defects within the junction.

As a first step towards a full analysis of TAMR effects in these devices, a 9 T magnetic field is applied in-plane and out-of-plane of the surface of the sample. Again transport measurements are performed while the sample is kept at a temperature of 10 K. The voltage over the junction and the corresponding resistance are plotted in figure 5.10. Around zero bias current, a clear difference in resistance can be observed, which could indicate a nonzero TAMR-ratio if statistically significant.

To show the spread of the measurements at low bias, the average resistance for in-plane and out-of-plane field is plotted together with the corresponding standard deviation in figure 5.11. When assuming a normal distribution and the samples standard deviation to be correct, this would indicate a 68% confidence interval. Around zero bias current, a clear difference between the two orientations of the external field can be seen. These results show a TAMR-ratio of around −5 %, however more measurements are needed to confirm the reproducibility of these

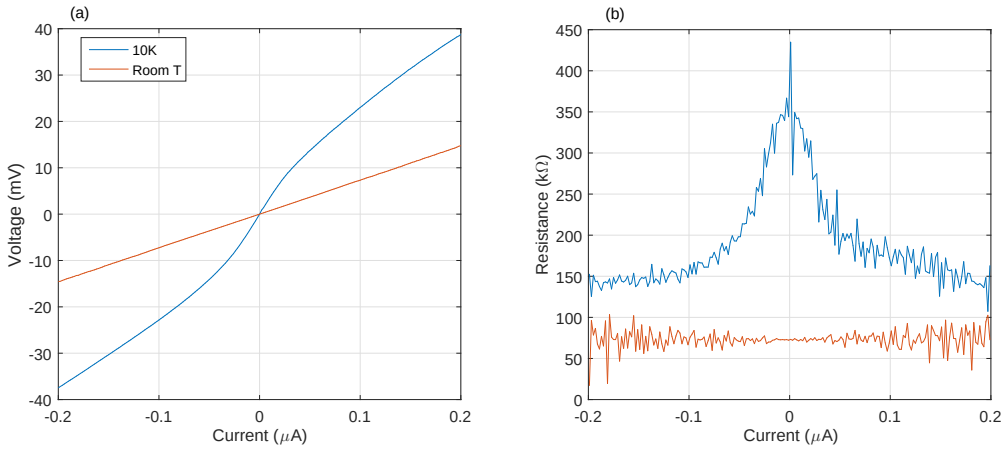


Figure 5.9 – (a) Voltage plotted versus the applied bias current over the junction, without external magnetic field at room temperature and 10 K. (b) Corresponding resistance versus applied bias current.

effects. Such an effect could be the result of SOC at the interface between Ni(111) and graphene described in literature[6]. These result offer a promising prospect for further measurements in which a high resolution 360° scan can be performed, providing information about the magnetic anisotropy of the device.

5.2.3 Towards Tedrow-Meservey measurements

The experimental confirmation of the existence of spin filtering at the interface between Ni(111) and graphene is one of the main motivations for this research. A very unambiguous method of measuring spin polarization is performing Tedrow-Meservey measurements, in which a current is sent through a tunnel barrier into an electrode of superconducting Al, under influence of a high magnetic field. As a result of Zeeman splitting in the DOS of the Al, the spin polarization of the tunnelling current can be determined from conductance measurements. To withstand the high in-plane magnetic field required for creating sufficient spin splitting, an Al layer is needed with a thickness which is much smaller than the London penetration depth of about 50 nm[23]. On the other hand, for really thin layers, it is possible that the metal does not form a continuous top electrode which fails to make electrical contact between the tunnel junction and the leads. Previous research within the NanoElectronics group has proven that Tedrow-Meservey measurements are possible using a top electrode of about 7 nm of e-beam evaporated Al[43].

An attempt is made to induce and confirm superconductivity in the top electrode of these devices. For this test, samples have been made with EBL defined top electrodes consisting of Al_2O_3(3.5 nm)/Al(8 nm)/Cu(10 nm). The Al_2O_3 would act as the tunnel barrier required when performing Tedrow-Meservey measurements. The Cu top layer ensures proper electric contact over step edges where the underlying Al layer might be discontinuous. The sample is cooled to 314 mK using the Heliox cryostat. This is well below the 1.175 K critical temperature of Al. The occurrence of superconductivity is tested by performing a four-point measurement over the top contact, in which the current is sourced and the voltage is probed. When the applied bias is lower than the critical current there should be no voltage drop over the Al layer, while at the critical point a sudden transition to ohmic behaviour should be observed. Based on the dimensions of the Al layer, a critical current in the order of a 1 mA is expected.

The tested top electrode shows an ohmic behaviour of about 300 Ω and no sign of a super-

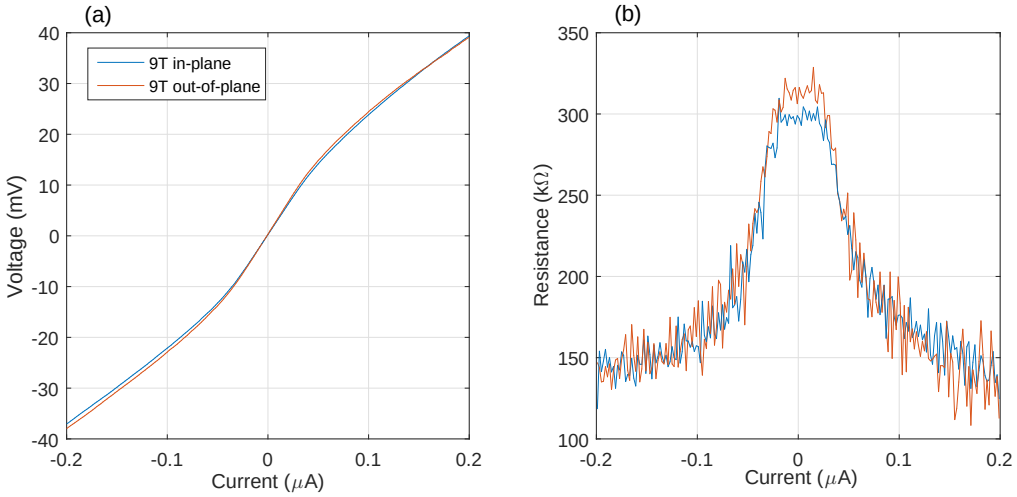


Figure 5.10 – (a) Voltage plotted versus the applied bias current over the junction, at a temperature of 10 K and a 9 T in-plane (blue) and out-of-plane (red) magnetic field. (b) Corresponding resistance versus applied bias current.

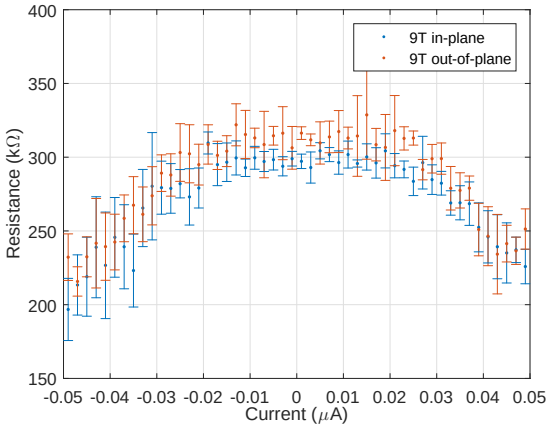


Figure 5.11 – Resistance versus applied bias current for the in-plane (blue) and out-of-plane (red) external field, showing also the standard deviation per data point.

conducting phase transition in the range between 5 nA and 0.6 mA. The fact that no superconductivity is observed in the top electrode might be a result of a discontinuous Al layer. In contrast to the devices produced in previous research [43], the underlying layers of these devices have a large surface roughness. Because the e-beam evaporation is performed under an angle, ridges on the surface might cast a shadow over other parts of the substrate, thereby avoiding the formation of a continuous Al layer. This might have led to current being forced to flow largely trough the overlying Cu layer creating Joule heating which locally raises temperature and destroys superconductivity.

5.3 Conclusion

The work described in this chapter aimed at the fabrication and initial characterization of spintronic devices based on the graphene-Ni(111) interface. The production of devices, with the recipe described in appendix A, has been successful. However there are some issues in the

production process, like retention of photoresist and the underetching of contact holes which lower the production yield. Some successful transport measurements have been performed in the PPMS cryostat. These show that the measured junction gives an ohmic behaviour at room temperature while at 10 K a tunnelling like characteristic is observed. When applying a magnetic field in-plane and out-of-plane to the sample, a difference in resistance is observed in the range between $-0.05\,\mu A$ and $0.05\,\mu A$. This could be a result of SOC at the interface between Ni(111) and graphene. Although for firm conclusions further TAMR measurements are required. Also an attempt has been made to induce and confirm superconductivity in these devices. Therefore a device, with a top electrode consisting of $Al_2O_3(3.5\,nm)/Al(8\,nm)/Cu(10\,nm)$, has been cooled down to 314 mK. A four-point measurement has been performed to find a superconducting phase transition when crossing the critical current. The tested top electrode does not show any sign of superconductivity. This might be caused by the surface roughness of the underlying layers of the device, which can avoid the formation of a continuous Al layer, thereby suppressing any superconductivity.

Chapter 6

Conclusions and recommendations

During this master assignment some steps have been made concerning the fabrication and characterization of spintronic devices based on the graphene-nickel(111) interface. First, research has been done on how to use sputtered SiO_2 as an insulating layer in new devices. The conclusions, concerning the production of this layer, are summarized below.

- SiO_2 layers with a thickness of 200 nm have been sputtered, which show a resistance in the order of 10 GΩ when cooled down to temperatures below 150 K. These films maintain their good insulating properties after two temperature cycles (i.e. cooling down to around 10 K and heating up again to 300 K).
- Adding extra O_2 to the chamber while sputtering SiO_2 is shown to damage the graphene. Therefore an alternative recipe is determined in which first SiO_2 is sputtered for 5 minutes without adding O_2. The rest of the layer is sputtered in 70 minutes while adding 5 sccm of O_2 to the chamber. This leaves the graphene unharmed and should create a layer with better stoichiometry than if no O_2 would have been added.
- After the sputter step, blue spots have been observed. These are likely caused by gas bubbles trapped underneath the SiO_2 layer. To prevent this, an outbaking procedure has been added in which the sample is heated to 170 °C and cooled down again, before doing the sputter deposition.
- For the etching of contact holes in this layer, using a BHF solution, an etching time of 95 s has been determined. This enables the fabrication of contact holes in which an Al top contact can be applied to the graphene.

This recipe for sputtering an insulating SiO_2 layer is then used in the fabrication of spintronic devices based on the Ni(111)/graphene interface. The development of this fabrication process is successful, although there are some issues like retention of photoresist and the underetching of contact holes which lowers the yield of this process.

With a junction of a finished devices, transport measurements have been performed in the PPMS cryostat. At room temperature, an ohmic behaviour is observed. At 10 K however, the junction shows a tunnelling like characteristic. Also a 9 T magnetic field has been applied in-plane and out-of-plane of the sample, while performing transport measurements. Between these two field directions, a difference in the junction's resistance is observed in the range between −0.05 µA and 0.05 µA. This might be caused by SOC effects at the interface between Ni(111) and graphene. However further TAMR measurements are required for drawing firm conclusions.

Attempts have been made to induce and confirm superconductivity in a device with a top electrode consisting of Al_2O_3(3.5 nm)/Al(8 nm)/Cu(10 nm). At a temperature of 314 mK, a

four-point measurement has been performed. Current sweeps have been applied to find a superconducting phase transition when crossing the critical current. However the tested top electrode did not show any sign of superconductivity. A possible explanation of this might be that this is a result of the surface roughness of the underlying layers of the device. This might avoid the formation of a continuous Al layer thereby suppressing superconductivity.

The transport measurement performed in the PPMS cryostat have given some promising results. Therefore, it is recommended to perform extensive TAMR measurements, using multiple devices for proper statistics. Especially the out-of-plane TAMR-ratio should be mapped using a high resolution 360° scan, because this, when combined with proper modelling, can give valuable information about SOC at the Ni(111)/graphene interface. Also the in-plane TAMR-ratio might be interesting. This measurement can only show a observable effect if the junction is located at a single Ni grain, which is possible using this fabrication process. This can give information about magnetic anisotropies within the hexagonal planes of Ni(111) and/or graphene.

It is hypothesised that the absence of superconductivity is a result of a discontinuous Al layer, leading to joule heating in the shunting Cu layer and thereby destroying superconductivity at currents mush smaller than the critical current. The voltage drops at these low current are probably to low to detect a possible superconducting phase transition. An alternative way of detecting superconductivity would be to conduct a tunnelling experiment by applying a very small bias current over the tunnel junction. In the case of superconductivity this would yield a tunnelling characteristic showing a energy gap of 2Δ. This energy gap should become less and eventually disappear when applying a magnetic field.

Review and acknowledgements

After almost a year of working in the NanoElectronics group, my project is almost finished. The work related to the development of new devices using a SiO_2 layer started prosperous. However, as usual in scientific research, there were some unforeseen setbacks like blue spots in the oxide layer and damage to graphene by oxygen. This taught me the importance of perseverance when doing research, which is something you cannot learn from a textbook. The project also gave me the chance to gain a lot of practical experience. I got the opportunity to do fabrication in the MESA+ cleanroom, which involved working with high vacuum systems and wet chemistry. For characterization, I worked with cryostats and sensitive electronics, which was also a completely new experience for me. When it comes to the literature I studied, it amazes me that I read about so many different topics ranging from RRAM's in SiO_2 to Rashba at the Ni(111)-graphene interface. My background in material physics proved very useful here.

This thesis work, which is now finished, would not have been possible without the help several people. First I would like to thank Elmer van Geijn and Michel de Jong who were my direct supervisors and gave me a lot of support while working on this project. I also want to thank Wilfred van der Wiel for offering me the possibility of working in the NanoElectronics group and for valuable discussions we had during our meetings. My graduation committee is completed by Alexander Brinkman to whom I also owe my thanks for taking time to read and asses my thesis as an external committee member.

The practical work I did could also not have been done without the help of several people. First I thank Derya Ataç who produced the graphene on Ni wafers used in this project. I also want to thank the cleanroom staff, when doing fabrication of samples, I could always rely on their support when I had questions or problems. Then I would like to thank Johnny Sanderink for the help with the DCA and SEM. When doing electrical characterization in one of the cryostats, I could count on the help of Thijs Bolhuis and Joost Ridderbos for which I am very grateful. Finally I would like to thank the NanoElectronics group as a whole for the pleasant atmosphere and the nice social activities.

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Appendix A

Recipe

Below the detailed recipe for the final process is given. Some parts of this description are copied from the master thesis of J.M. Boter[11], who used a similar recipe in his project. The recipe consists of six main steps (preparation, bottom electrodes, SiO_2 deposition, alignment markers, contact holes and top electrodes), which contain several sub steps.

0. Preparation (this step only has to be done once for a new wafer)
   (a) Dice the 4 inch wafer in smaller samples of 11 mm by 11 mm.
1. Define bottom electrodes
   (a) Strip the layer of protective resist with acetone in WB11, rinse with isopropanol (IPA) and dry the samples with the nitrogen gun.
   (b) Bake the samples on the 120 °C hotplate for five minutes.
   (c) Spin coat OiR 907/17 photoresist in WB21. Use the 4000 recipe.
   (d) Bake the samples on the 95 °C hotplate for 90 seconds.
   (e) Pre-align the metal 4 inch sample holder with 20 sample positions in the EVG620 Bond Aligner.
   (f) Place a sample at the correct position for the desired width of the bottom electrodes in the sample holder, align the sample and expose it for 4 seconds. Use the Topside recipe in hard contact mode with a separation distance of 60 µm and the 'Bottom contacts'. Repeat this step for all samples.
   (g) Bake the samples on the 120 °C hotplate for one minute.
   (h) Develop in OPD-4262 for 29 seconds in WB21, rinse thoroughly with water and dry with the nitrogen gun.
   (i) Bake the samples on the 120 °C hotplate for five minutes.
   (j) Prepare treatment with DMSO. Heat the DMSO in the ultrasonic bath of WB1 to 80 °C. Let it warm up so it can be used in step o.
   (k) Place the samples in the 4 inch sample holder for ion beam etching. Use the one marked RIBE and be sure to not use the holders marked TCOater or BAK.
   (l) Load the sample holder into the Oxford Ionfab300Plus for etching with standard settings. Let the platen rotate at 5.0 rpm at an angle of 0°, add 5 sccm of argon gas to both neutralizer and beam and set the cool gas at 5.0 Torr. Etch away the complete nickel layer. Generally 55 minutes of etching in enough. After checking with a microscope some additional etching may be done.

(m) Unload the sample holder and remove the samples.

(n) Place the samples in the TePla 300E for a 30 seconds treatment in oxygen plasma to strip the top of the resist layer. The oxygen flow should be 50% (200 sccm) and the power should be 500 W.

(o) Clean the samples in hot DMSO at level 3 ultrasonic for 30 seconds.

(p) Clean with acetone and IPA and dry the samples with the nitrogen gun in WB11. If necessary, repeat treatment in oxygen plasma and cleaning until all photoresist is removed. Do not expose the samples to oxygen plasma too long, because it can damage the graphene.

2. Apply SiO_2

(a) Make sure there is a SiO_2 target inside gun of the TCOater.

(b) Place the samples in the 4 inch sample holder for film sputtering. Use the one marked TCOater.

(c) Load the sample holder into the TCOater.

(d) Warm up chamber.

i. Temp to 170 °C

ii. At "HT/VAT", put heater on

A. Heater on

B. Setpoint T to 170 °C

iii. At "Basics", manually make thermal contact.

A. Press "Chuck process (rotate)"

iv. Set gas flow.

A. At "HT/VAT", set "chuck[mbar]" to about 3.5 (make sure the flow is between 3 sccm and 5 sccm).

B. At "HT/VAT", set "wafer[mbar]" to about 3.0 (make sure the flow is between 3 sccm and 5 sccm).

C. At "manual", put on manual control.

D. At "manual", put "He" on.

(e) Wait for at least 90 minutes

(f) Cool chamber

i. Turn gasses off.

ii. Turn heater off.

iii. Press "chuck process(rotate)" twice.

iv. Bring chuck to load position.

v. At "Process", set Temp to 20 °C.

vi. Cool chuck.

(g) Wait for about three hours

(h) Start sputtering

i. Base Pressure: 1×10^{-6} mbar.

ii. Distance: 44 mm.

iii. Temperature: 20 °C.

iv. Rotation: 5 rpm.

v. Backside cooling: off.
vi. Cool after process: off.
vii. Process pressure: 7×10^{-3} mbar.
viii. Sputter time: 75:00
ix. Ar: 30 sccm
x. O_2: 0 sccm
xi. Use gun 4 on RF mode.
xii. Forward power: 500 W
xiii. Do not add gasses to the gun.

(i) After 5 minutes of sputtering, at "PLC I/O", set O2R to 5 sccm

(j) During the process check the reflected power. If this gets higher than 5 W, switch to manual and reduce the reflected power by pressing the button “Cr<”. Then switch back to automatic.

(k) Unload the sample holder and remove the samples.

3. Define EBL alignment markers

(a) Bake the samples on the 120 °C hotplate for five minutes.

(b) Spin coat primer (HMDS) in WB21. Use the 4000 recipe.

(c) Spin coat OiR 907/17 photoresist in WB21. Use the 4000 recipe.

(d) Bake the samples on the 95 °C hotplate for 90 seconds.

(e) Pre-align the metal 4 inch sample holder with 20 sample positions in the EVG620 Bond Aligner.

(f) Place a sample at the correct position for the desired the alignment markers in the sample holder, align the sample and expose it for 4 seconds. Use the Topside recipe in hard contact mode with a separation distance of 60 µm and the "Allignment markers". Repeat this step for all samples.

(g) Bake the samples on the 120 °C hotplate for one minute.

(h) Develop in OPD-4262 for 29 seconds in WB21, rinse thoroughly with water and dry with the nitrogen gun.

(i) Prepare treatment with DMSO. Heat the DMSO in the ultrasonic bath of WB1 to 80 °C. Let it warm up so it can be used in step k.

(j) Sputter metal using sputterke.
i. Make sure there are Ti and Pd targets inside sputterke.
ii. Load the samples. No sample holder required.
iii. Set the power supply to 100 W.
iv. Use the argon flow to regulate the pressure to 6.6×10^{-3} mbar.
v. Apply Ti for 1:20 min.
vi. Apply Pd for 1:00 min.
vii. Unload the samples.

(k) Perform lift-off in hot DMSO.

(l) Clean with acetone and IPA and dry with the nitrogen gun.

(m) Bake the samples on the 120 °C hotplate for five minutes.

4. Define contact holes

   (a) Make images of the bottom electrodes with an optical microscope in which suitable graphene flakes (both large and thick enough) are visible.

   (b) Define an EBL pattern with square contact holes of 1.5 µm by 1.5 µm by using these images in the EBL software.

   (c) Clean the samples in WB11 with acetone and IPA and dry with the nitrogen gun.

   (d) Bake the samples on the 120 °C hotplate for two minutes.

   (e) Cover the spin coater in WB23 with tinfoil.

   (f) Spin coat PMMA A4 in WB23 using the 4000 recipe.

   (g) Put samples at 160 °C hotplate for two minutes.

   (h) Write the EBL pattern in the RAITH150-TWO with an aperture of 10 µm, an acceleration voltage of 20 kV and a dose of 450 µC/cm^2.

   (i) Prepare treatment with DMSO. Heat the DMSO in the ultrasonic bath of WB1 to 80 °C. Let it warm up so it can be used in step l.

   (j) Develop in WB23. Use 1:3 MIBK/IPA developer for 33 seconds, rinse in IPA and dry with the nitrogen gun.

   (k) Do etching in WB9. Use BHF for 95 seconds, rinse in water and dry using the dry spinner. Use plastic beakers.

   (l) Remove PMMA in hot DMSO.

   (m) Clean with acetone and IPA and dry with the nitrogen gun.

5. Deposit top electrodes

   (a) Spin coat OiR 907/17 photoresist in WB21. Use the 4000 recipe.

   (b) Bake the samples on the 95 °C hotplate for one minute.

   (c) Pre-align the metal 4 inch sample holder with 20 sample positions in the EVG620 Bond Aligner.

   (d) Place a sample at the correct position for the desired width of the top electrodes in the sample holder, align the sample and expose it for 4 seconds. Use the Topside recipe in hard contact mode with a separation distance of 60 µm and the 'Top contacts'. Repeat this step for all samples.

   (e) Bake the samples on the 120 °C hotplate for one minute.

   (f) Develop in OPD-4262 of 29 seconds, rinse thoroughly with water and dry with the nitrogen gun.

   (g) Do E-beam evaporation

      i. Start the cooling of the DCA by opening the liquid nitrogen valve and placing the turning knob in the "Fill" position.

      ii. Stop the turbo pump to aerate the load lock of the DCA.

      iii. Place the samples in the 4 inch sample holder. Use the holder marked TCOater or BAK and be sure to not use the holder marker RIBE.

      iv. Place the sample holder on the wafer holder and together place them in the load lock.

      v. Start the turbo pump to evacuate the load lock.

vi. When the pressure in the load lock is sufficiently low, transfer the wafer holder to the deposition chamber and place it at a height of 57 cm.

vii. Wait for at least six hours, so the sample can cool down to the temperature of the deposition chamber.

viii. Place the crucible in the correct position for the material to be deposited.

ix. Start the e-gun and the corresponding rate monitor. Gradually increase the emission current to the correct value.

x. Check the deposition rate with the rate monitor and, if it is sufficient and stable, open the shutter to start the deposition. At the same time, set the rate monitor to zero.

xi. Close the shutter as soon as the desired thickness is obtained on the rate monitor. Keep in mind the tooling factor.

xii. Gradually decrease the emission current and switch off the e-gun.

xiii. Repeat steps viii-xii for all layers.

xiv. After deposition of the final layer, place the wafer holder in the load position and transfer it to the load lock.

xv. Aerate the load lock and wait for about an hour to avoid condensation. Get the screw off the door to avoid overpressure.

xvi. Unload the wafer holder and evacuate the load lock.

xvii. Remove the samples from the sample holder.

xviii. Stop the cooling by placing the turning knob in the "off" position and closing the liquid nitrogen valve.

(h) Perform lift-off in acetone in WB11. Clean with IPA and dry with the nitrogen gun.

(i) Bake the samples on the 120 °C hotplate for five minutes.

Appendix B

Workflow

The images below represent the fabrication process of the devices used in the experiments described in chapter 5. Note that in these images only one device per chip is shown, while in reality every sample contains six devices.

Bottom electrode

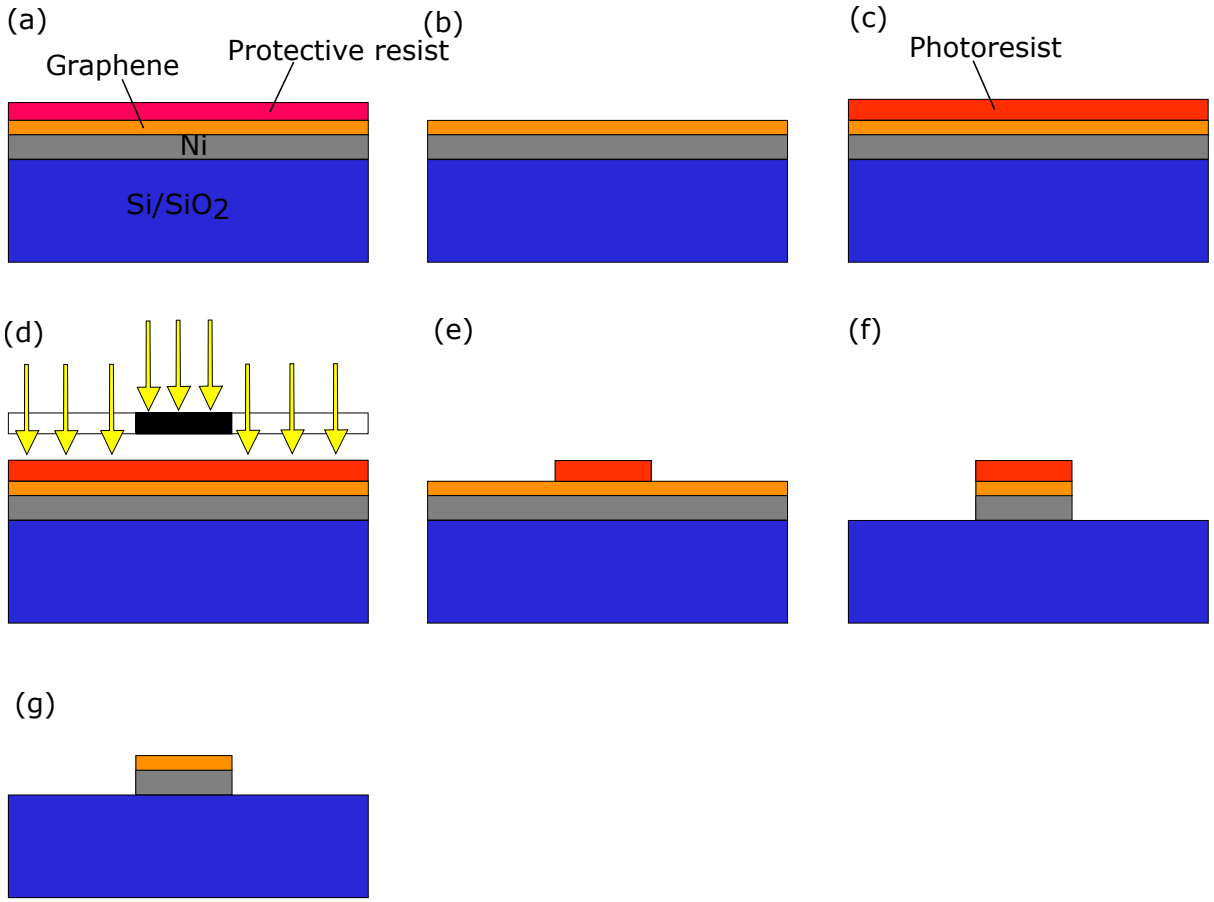


Figure B.1 – The fabrication of bottom electrodes. (a) Sample as supplied. (b) Stripping protective resist. (c) Spin coating photoresist. (d) Photolithographic exposure. (e) Development of photoresist. (f) Ion beam etching of graphene and Ni layer. (g) Removing the remaining photoresist.

Sputtering SiO_2

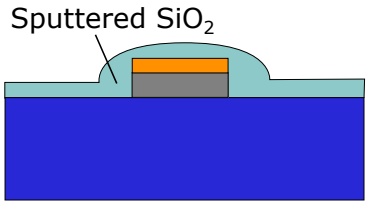


Figure B.2 – Sputtering of the SiO_2 layer.

Alignment markers

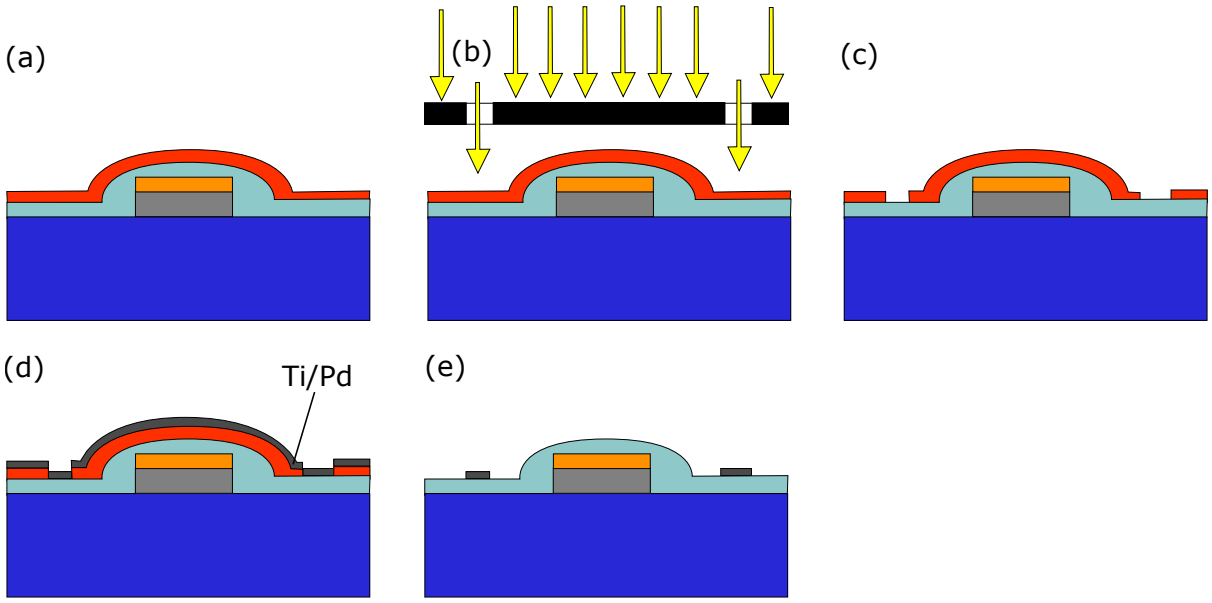


Figure B.3 – Fabrication of alignment markers for EBL. (a) Spin coating photoresist. (b) Photolithographic exposure. (c) Development of photoresist. (d) Sputtering a layer of Ti and Pd. (e) Lift-off of photoresist leaving the Ti and Pd only where the markers are defined.

Contact hole

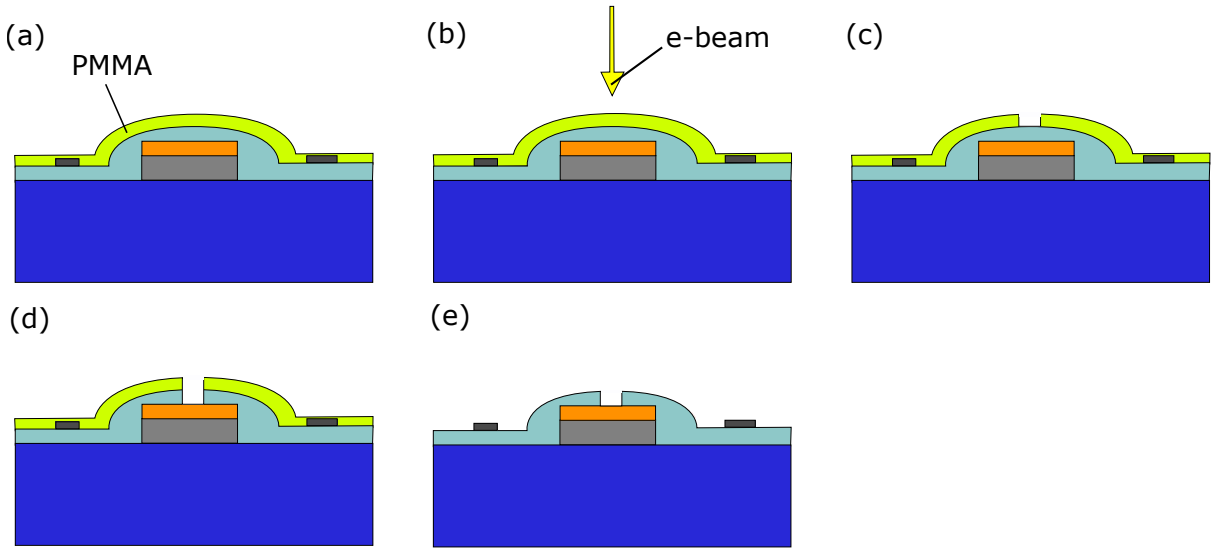


Figure B.4 – Fabrication of contact holes. (a) Spin coating PMMA resist. (b) Electron beam exposure. (c) Development of PMMA resist. (d) Etching of the SiO_2. (e) Removing the remaining PMMA.

Top electrode

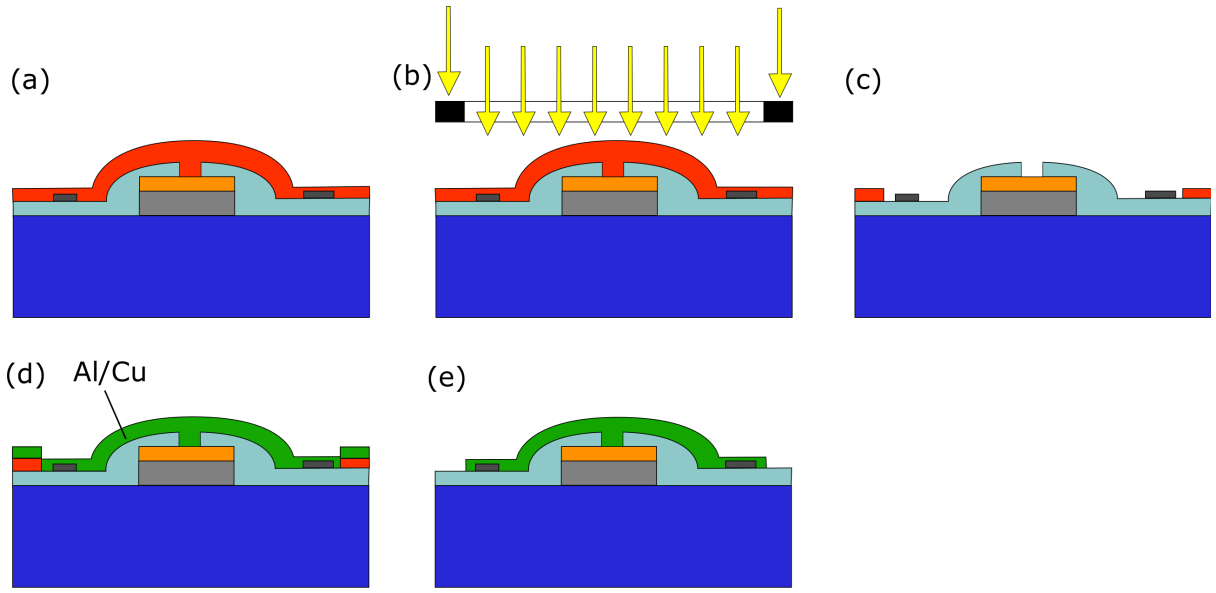


Figure B.5 – Deposition of top electrodes. (a) Spin coating photoresist. (b) Photolithographic exposure. (c) Development of photoresist. (d) electron beam evaporation of a layer of Al and Cu. (e) Lift-off of photoresist leaving the Al and Cu only where the top electrodes are defined.

Appendix C

Mask

In figure C.1, the photolithography mask used in this project is shown. The pink regions indicate where the non-transparent coating is applied so the photoresist does not get exposed at these locations. the mask consists out of 20 designs of 11 mm×11 mm each (although 5 have been left empty). The black frame contains the three bottom electrodes designs. A zoom in of such a design is shown in figure C.2(a). In the green frame the designs for the alignment markers are shown, while the blue frame contains the designs for the top electrodes. A zoom-in of the alignment markers and the top electrodes can be found in figure C.2(b) and figure C.2(c) respectively.

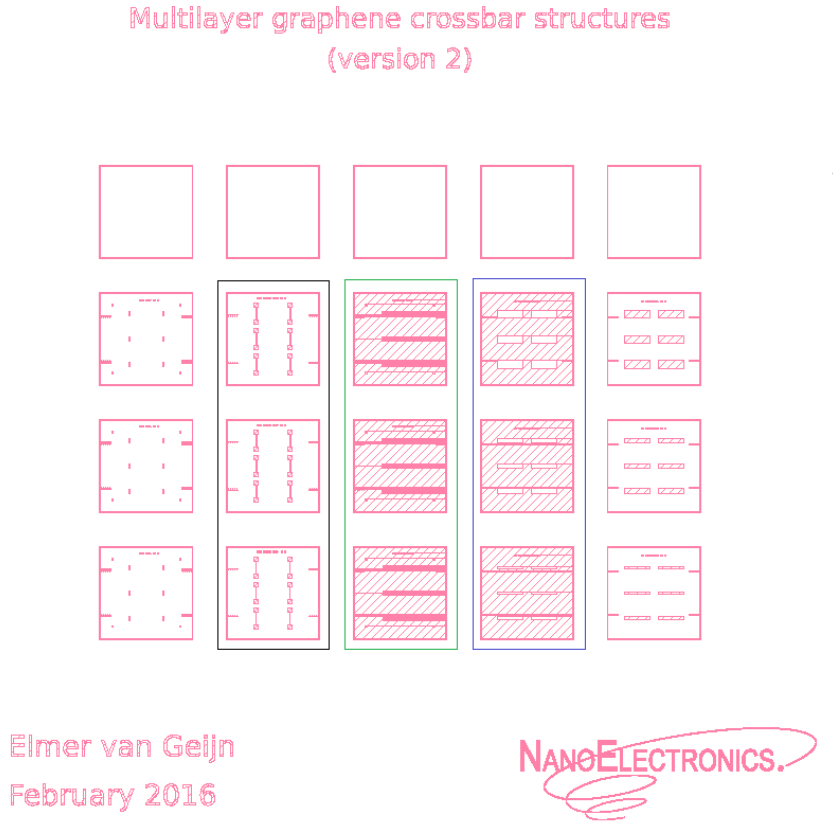
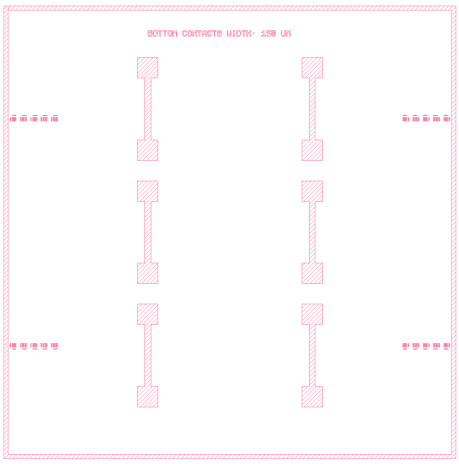
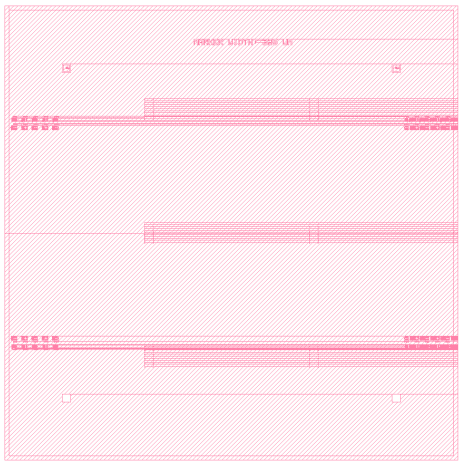


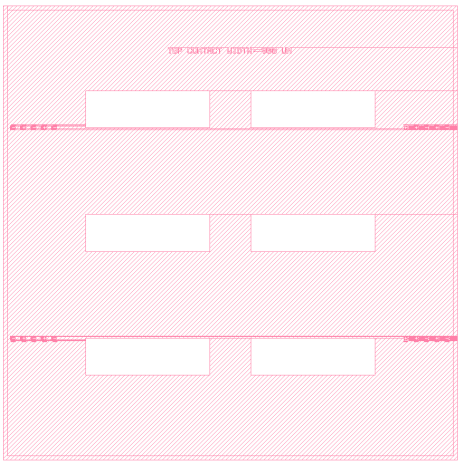
Figure C.1 – The used photolithography mask. The black, green and blue frames contain the bottom electrodes, alignment markers and top electrodes respectively.



(a) Mask for bottom electrodes with a width of 150 µm. Designs for 100 µm and 60 µm are also available.



(b) Mask for alignment markers with a separation distance of 225 µm. Designs for 200 µm and 125 µm are also available.



(c) Mask for top electrodes with a height of 900 µm. Designs for 600 µm and 300 µm are also available.

Figure C.2 – Three of the used mask designs used in this project.

In the mask design some horizontal lines appear. These are a result of the computer program, called KLayout, in which this design is made. In this program mask designs are made out of polygons. the horizontal lines are edges on of these polygons, but do not represent any artefact present on the actual mask.