Experimental investigation of new device test structures for determining the lifetime in solar cells

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***Abstract*— Octagonal ring-shaped test structures have been developed for experimental investigation of charge carrier flows in p-type regions configured as the emitter of a vertical pnp transistor. An I-V characterization of the test structures is performed to evaluate their suitability for investigating the electrical performance of emitters for n-type crystalline solar cell in terms of surface recombination and minority carrier lifetimes. The emitter regions in this study are formed by using pure boron (PureB) depositions under different processing conditions. The base current, ideally formed by injection of electrons into the emitter, is found for the region of interest by using a differential measurement technique. For solar cells, the emitter should preferably be designed to suppress the injection of electrons as much as possible. Differences in the emitter efficiency between the fabricated emitters are identified and related to the method of processing.**

***Index Terms*— c-Si solar cells; surface recombination; bipolar transistor test structure; PureB diodes; emitter efficiency; sheet resistance**

I. INTRODUCTION

As worldwide energy demands increase, conventional energy resources such as fossil fuels, will be exhausted within the next century. Therefore development and usage of alternative energy resources is important, especially if we could use the long-term natural resource of the Earth-the sun. Solar cells are considered to be a major candidate for obtaining energy from the sun, since they can convert light to electricity [1]. The figure of merit for conversion performance of a solar cell, built using a semiconductor photodiode, is efficiency, which depends on the minority carrier lifetime. This is basically the average time that a carrier can spend in an excited state after electron-hole generation before recombining.

In silicon, photodiode solar cells consist of highly-doped p- or n-type emitter, an n- or p-type base as junction layers, metallic contacts, dielectric layers as silicon surface-passivation and anti-reflection coatings [2]. The interfaces between the silicon and contacting/passivation layers have in common that they are a major source of interface states for generation/recombination of charge carriers. In bulk impurities and other defects of the crystal structure can be a source of generation/recombination of carriers but often the surface effects dominate. Characterising the carrier losses in the solar cell is considered to be complicated task, as it is generally not possible to disentangle its two main components, recombination in the bulk and at the surface.

Surface recombination and lifetime in silicon devices have been studied and lots of different approaches have been proposed [3]-[7]. However, in the proposed measurement techniques, the presence of carrier trapping and surface recombination can have a strong effect on the measured response time, causing it to be much larger that the actual lifetime and therefore unable to give accurate values for calculating the efficiency [8].

In this study, new test structures are investigated with the objective of separately measuring the hole and electron current flows in p-type emitter regions to evaluate the influence of surface recombination on the lifetime of the carriers. Additionally, in this work a pure boron (PureB) layer was used for creating the p^+region and a number of different processing procedures are examined that may be of interest for fabricating c-Si solar cells. PureB has already been extensively studied as a means of creating the p^+ region of ideal p^+n diodes with junction depths down to a few nanometers [9], [10]. The advantage of these diodes is that despite having a shallow junction depth, reverse currents in the diodes are the same low level as for conventional deep junction diodes. This low-leakage property has been accorded to the fact that a high effective hole concentration is created at the PureB-to-Si interface, thus giving an efficient suppression of electron injection from the n-region and a correspondingly low saturation current [11],[12].

In the present test structures, the PureB is incorporated as the emitter in a bipolar transistor structure. The design allows to study both emitter contact regions where metal is placed directly on the p^+ region and emitter passivation regions in which dielectric is deposited on the p-region. By using different test-structure geometries and a differential measurement technique, the minority carrier electron injection into the emitter can be determined for each region of interest. In a solar cell, the electron injection must be minimized since only holes should be collected at the anode and all electrons should travel through thick n-region to the cathode, which requires an electron lifetime that is as long as possible. The bipolar test structures allow to separately optimise the electron injection in each region of the emitter, something that is not possible with only a simple diode structure.

II. TEST STRUCTURES

The basic p^+np bipolar structures studied in this work are shown in Fig. 1. The starting substrates were <100> 1-10

Ohm p-type Si wafers that were first thermally oxidized to a silicon-dioxide (SiO_2) layer thickness of 200nm. Through this layer, the n-type base region and the n^+ contacts regions were formed by implantation and thermal activation. Windows to the Si were then opened where the PureB deposition was to be performed. Before this deposition, shallow p^+-regions were implanted and activated at 700°C as an initial part of the PureB deposition cycle. Four different types of devices with a variety of deposition temperatures, deposition times and metallization methods are studied here. Two approaches were taken for metallization of the diodes. In the first approach, shown in Fig. 1a, a 0,6μm PECVD SiO_2 was deposited on top of the PureB. Contact windows to the n^+ and p^+ regions were then etched on this oxide and Al/1%Si was sputtered and patterned to form the metal contact pads. In this way, an emitter region that is covered with oxide is formed in the region between contacts. This resembles how an emitter region passivated by a dielectric could be made in solar cell as shown in Fig. 2. Fig.1b illustrates second metallization approach where the devices are metalized by contacting the whole PureB emitter region with the deposited Al/Si. This resembles the emitter contacting regions of solar cell also indicated in Fig. 2. The processing parameters of the four PureB emitter types studied in this work are listed in Table I.

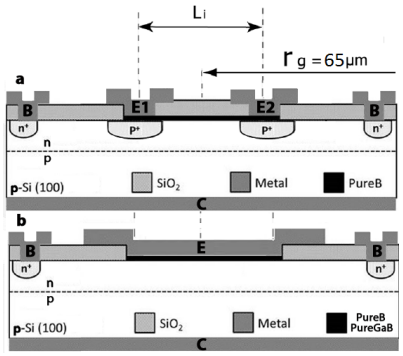

Fig. 1. Cross section of the test structures with two different metallization methods: (a) fabrication of the central oxide window by Al-contacting the diode through a ring-shaped window to the PureB at the perimeter of the diode, and (b) contacting the whole emitter region by depositing Al directly on the PureB.

TABLE I

PROCESSING PARAMETERS FOR THE 4 PUREB EMITTER REGIONS.

Device Name	PureB Deposition		Anneal/ oxidation at 950°C	Deposition of 0.6μm PECVD	Simulated junction depth(nm)
	Temp(°C)	Time(min)			
HT6	700	6	no	yes	5
HT20	700	20	yes	yes	400
LT20	400	20	no	no	0
LT40	400	40	no	no	0

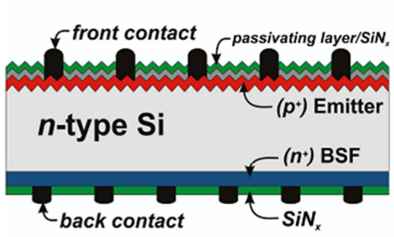

Fig. 2. Schematic cross-section of a typical concept of an n-type silicon based solar cell with a front emitter. The indicated emitter passivating layer and front contact can be studied using the test structures of respectively Fig.1a and Fig.1b [13].

Octagonal-ring shaped bipolar structures are designed with the purpose of extracting parameters related to the laterally uniform part of the emitter region by subtracting peripheral contributions, associated with the collector and base regions, from the measurements. Sets of octagon-shaped structures were designed with a fixed 65μm radius to the center of the emitter ring, so that total perimeter is always fixed independent of the length of the octagon rings. Sets of each 8 octagon ring structures are designed as in Fig. 3. with the ring width L equal to 23,7μm, 24μm, 25μm, 26μm, 28μm, 30μm, 34μm and 64μm. This gives a fixed perimeter of 2x431μm.

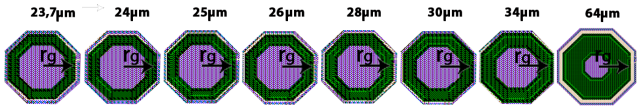

Fig. 3. Octagon-ring shaped structures with ring width.

The PureB layer that is used here to form the p emitter can have two functions in this respect. As a more conventional function, the layer acts as a source of a boron dopants, which diffuse into silicon up to the solid solubility, which is about $2 \cdot 10^{19}/cm^3$ at 700°C [14].

The test structures HT6 and HT20 have two p^+ rings (inner and outer contacts) which are connected together by a thin PureB layer that dopes the Si at 700°C. In HT20 the PureB layer was oxidized after deposition at a temperature of 950°C. The oxidation cycle was designed to completely consume the pure boron layer and give a doping of the Si with a peak value of $2 \cdot 10^{20}/cm^3$ at the surface [10]. In this device the central emitter region is therefore expected to be oxide covered p-Si.

The function of the PureB is less conventional for LT20 and LT40 devices. The p-type region is not formed by doping of the Si, since the deposition temperature of 400°C is too low for this. Nevertheless, a p^+-region is formed due to an interface reaction between the pure boron and the Si surface. In this reaction, it has been proposed that a monolayer of fixed acceptor is formed that attracts a monolayer of holes to the interface[15]. This layer of holes has been shown to be as efficient in suppressing the electron injection as a deep p^+ diffused region.

The implanted p^+ region is expected to have a deeper junction depth than the PureB-only region. This means that the depletion of the n-type base will be larger under the p^+ region, which in turns means that the base width is smaller. The smaller the width the higher the resistance. This is indicated in Fig. 4.

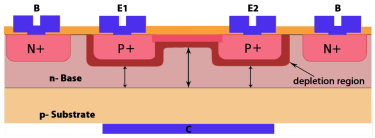

Fig. 4. A schematic cross section of the *pnp* test structure. The width of the base region is narrowed as a result of change in depletion region caused by implanted p^+ contact regions.

III. METHOD

PureB diodes are known for property of functioning as *pn* junctions with very low saturation current despite junction depths down to a few nanometers [10]. This is attributed to the formation of a monolayer of holes at the PureB-to-Si interface [15]. Without this hole layer, the total hole concentration from B-doping of the Si, equivalent to a shallow diffused junction, is limited at 700°C and the B-doped region forms an almost transparent layer for electron injection from the n-substrate [9], [11]. Therefore, when the metal covers the diode's surface, the IV characteristics are determined by the electron injection into the metal [16]. Moreover, imperfections at the interface with the metal will often be a source of generation-recombination (g-r) currents that deteriorate both electrical and optical performance. The PureB diodes give a way of avoiding these problems while still maintaining a nm-shallow junction.

The best way to experimentally study the electron and hole currents through a diode is to separate them by using a bipolar structure. In our case, p^+np structures with the PureB depositions used to form the emitter allow us to do that. In such structures, a forward voltage is placed over the emitter-base junction so that high electron and hole currents flow through the junction. The holes are injected from the emitter into the base that is so narrow that practically all the holes are swept to the collector by electric field over the reverse-biased collector-base junction depletion region as shown in Fig. 5.

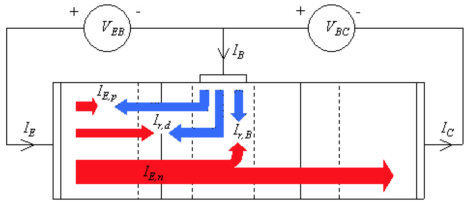

Fig. 5. Electron (blue) and hole (red) current flow in an *pnp* transistor biased to operate in the active mode. The base current is the sum of the hole diffusion current $I_{E,p}$, the base recombination current, $I_{r,B}$ and the base-emitter depletion layer recombination current, $I_{r,d}$.

If there are defects in the base region, some of the injected holes may recombine there. For each hole that recombines in the base region, another electron enters the base as base current ($I_\mathbf{B}$). This gives the parasitic g-r base current indicated in Fig. 5. Since the p^+np bipolar structure is designed to have a high collector current and low base current, even a small g-r current can be observed as an increase in base current. Eventually, the I-V characteristics of the test structures were studied using Gummel plots, where the base current I_B was observed. Three different measurements were performed on the HT6 and HT20 devices. Basic cross section of the devices and the schematic of the measurements are illustrated in Fig. 6. Fig. 6a depicts biasing over two emitters, while measuring base ($I_\mathbf{B}$) and collector ($I_\mathbf{C}$) currents. $I_{\mathbf{B}_{\mathbf{E}_2}}$ and $I_{\mathbf{B}_{\mathbf{E}_1}}$ base currents are measured while outer E_2 and inner E_1 emitters are biased respectively.

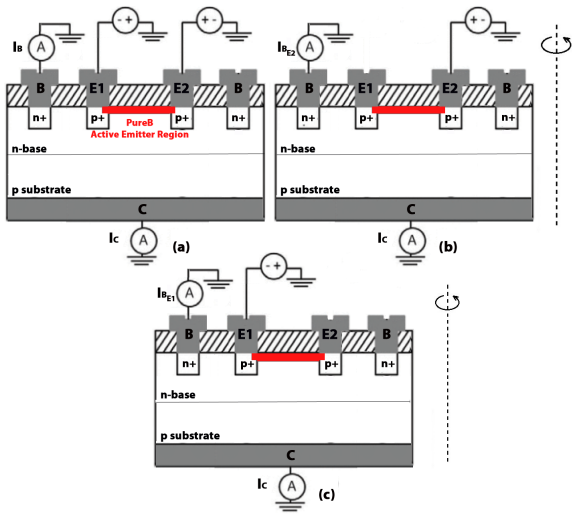

Fig. 6. Schematic cross section of HT20 and HT6 devices with (a) both emitters connected, (b) only inner emitter E_2 is connected and (c) outer emitter E_1 is connected. The base current(I_B, $I_{B_{E2}}$, $I_{B_{E1}}$) is in all cases measured under forward bias.

Another parameter that may be extracted out of the structures and contribute to the characterization is the sheet resistance (R_{sh}). R_{sh} may be extracted out of the resistance measurements of outer and inner octagonal ring structures which later on have to be corrected by radial correction factor.

A. Gummel Number

To gain insight in the current flows in the different types of junction we first look at the ideal case, disregarding defect-induced currents. The electron and hole currents over a junction can be expressed as [1]:

$$I = qn_{\mathbf{i0}}^2 A \cdot \left(\frac{1}{G_\mathbf{D}} + \frac{1}{G_\mathbf{A}}\right) \cdot \left(e^{\frac{qV}{kT}} - 1\right) \tag{1}$$

$$I_h = \frac{qn_{\mathbf{i0}}^2 A}{G_\mathbf{D}} \cdot \left(e^{\frac{qV}{kT}} - 1\right) \tag{2}$$

$$I_e = \frac{qn_{\mathbf{i0}}^2 A}{G_\mathbf{A}} \cdot \left(e^{\frac{qV}{kT}} - 1\right) \tag{3}$$

where q is elementary charge, n_{i0} is the intrinsic carrier concentration, A is the diode area, $G_{\mathbf{D}}$ and $G_{\mathbf{A}}$ are Gummel numbers of the n and p-doped regions and kT/q is the thermal voltage.

The electron injection into the emitter region is governed by the Gummel number $G_{\mathbf{A}}$ of the region. In general formulation this can be defined as [1]:

$$G_{\mathbf{A}} = \int_{W_{QNA}} \frac{N_E(z)\cdot n_{i0}^2}{D_n(z)\cdot n_{ie}^2} dz + \frac{N_A}{S_A}\frac{n_{i0}^2}{n_{ie}^2} \tag{4}$$

where W_{QNA} is the width(or depth) of the p-type doped region, $n_{ie}(z) = n_{i0}e^{(\frac{-\triangle E_G(Z)}{2kT})}$ is the effective intrinsic carrier concentration, $\triangle E_G(z)$ is the bandgap difference with respect to the c-Si, N_A is the active p-type doping concentration, $D_n(z)$ is the electron diffusion coefficient in the p-region as a function of depth z from Si surface, and S_A is the surface recombination velocity.

In first instance, it can be useful to consider the ideal case, but many diodes will have I-V characteristics that deviate from the ideal case due to, e.g., defect-related parasitic currents and series resistance. To stretch the applicability of the basic Eq. (1), the 'ideality factor' was introduced in the denominator of the exponential term.

B. Ideality Factor

For actual non-ideal diodes, the expression for the I-V behaviour is often written as in Eq. (5). The parameter n in this equation is the ideality factor.

$$I = I_o \cdot (e^{\frac{qV}{nkT}} - 1) \tag{5}$$

Having Gummel plots and knowing the values of k, T and q, the ideality factor may be easily calculated. Typically, Si diodes have an n between 1 and 2, the latter being seen when $g-r$ currents dominate [1],[17]. PureB diodes can be fabricated with high ideality and often have an n below 1.02 [18].

C. Sheet Resistance of the Emitter Regions

To determine the sheet resistance $R_{\mathbf{sh}}$, a differential measurement technique is applied as described in [20]. In this method the resistance associated with the contacts are eliminated and the real value of sheet resistance of the layer of interest can be extracted. Sets of octagonal ring structures are designed with the basic design illustrated in Fig. 7. Each octagonal ring structures has a fixed perimeter length, therefore only two variables are important for the sheet resistance extraction. These are the measured resistance, $R_{\mathbf{mi}}$ of each measured structure and the ring length $L_{\mathbf{i}}$, where the indices $\mathbf{i} = 1,...,\mathbf{n}$ refer to each specific test structure in the given set of n structures (section II). Since the structures are octagon-ring shaped, the radial spreading must be taken into account [19].

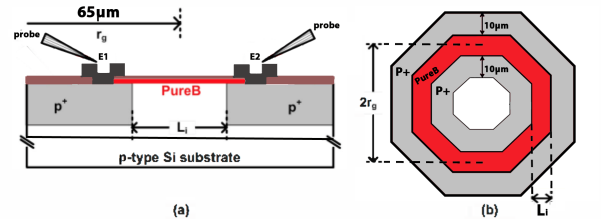

Fig. 7. Schematic cross section (a) and layout (b) of the octagonal ring sheet resistance measurement structure. The perimeter of the PureB-only region is constant and equal to $2x431\mu m$ while the length of the octagonal ring has varying values $L_{\mathbf{i}}$.

If the length of the ring is very small compared to radius $r_{\mathbf{g}}$, $r_{\mathbf{g}} >> L_{\mathbf{j}} \approx L_{\mathbf{i}}$ the $R_{\mathbf{sh}}$ can be determined as

$$R_{\mathbf{ij}} = R_{\mathbf{mj}} - R_{\mathbf{mi}} = R_{\mathbf{sh}} \cdot \frac{L_{\mathbf{j}} - L_{\mathbf{i}}}{W} \tag{6}$$

When the $L_{\mathbf{i}}$ is of the same order as $r_{\mathbf{g}}$, then the radial spreading of the current from the inner contact to outer contact of the ring must be taken into account. For an octagonal ring a radial correction factor can be calculated as,

$$R_{\mathbf{mj}} - R_{\mathbf{mi}} = R_{\mathbf{sh}} \cdot \alpha_{\mathbf{ij}} \tag{7}$$

and

$$\alpha_{\mathbf{ij}} = \frac{1}{6,627} ln[\frac{(r_g - 0.5\cdot L_{\mathbf{i}})(r_g + 0.5\cdot L_{\mathbf{j}})}{(r_g + 0.5\cdot L_{\mathbf{i}})(r_g - 0.5\cdot L_{\mathbf{j}})}] \tag{8}$$

where $\alpha_{\mathbf{ij}}$ is the proportionality that relates $R_{\mathbf{ij}}$ to $R_{\mathbf{sh}}$.

Plotting $R_{\mathbf{ij}}$ versus the calculated values of radial correction factors must provide a linear relation and the value of the extracted sheet resistance [19].

D. Sheet Resistance of the Base Regions

Another important limitation of the bipolar transistors comes from the design of the structures, which is shown in Fig. 8, in which the emitter (p^+-region), base (n-region), collector (p-region), and the contacts are presented. For such a design, the base current flows in the lateral direction and the so called base-spreading resistance associated with such a current path becomes important.

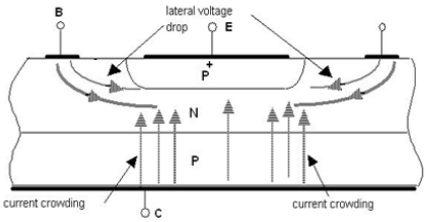

Fig. 8. Current (emitter) crowding of BJT device.

The voltage drops non uniformly in the lateral direction along the base which leads to a nonuniform voltage difference between the emitter region and base regions. Small variations in $V_{\mathbf{BE}}$ will give rise to large current variations since $I_{\mathbf{C}}$ and $I_{\mathbf{B}}$ depend exponentially on $V_{\mathbf{BE}}$ [1]. Base

spreading resistance results in the so-called emitter-current crowding at the edges of the emitter region and reduces conduction at the center of the emitter region.

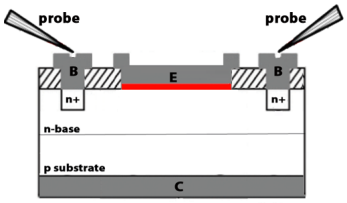

Fig. 9. Schematic cross section of the LT40 and LT20 devices used for the base resistance measurements.

A different set of test structures were available for measuring the sheet resistance of the base in the HT6 and HT20 devices in the regions, where (1) no emitter, (2) a PureB-only region emitter, and (3) a p^+ region is formed. The base sheet resistance of the LT20 and LT40 devices can be determined by I-V measurements over two base contact regions illustrated in Fig. 9. Eventually, a differential measurement technique is applied to correct measured resistance with radial proportionality factor as described in [20].

IV. RESULTS

A. I-V Characteristics

The I-V characteristics of the HT6 device with an emitter area of 26x431μm^2 are plotted on a semi-logarithmic scale as indicated in Fig. 10. The hole injection ($\sim I_C$) from the p^+ PureB emitter region is separated from the electron current ($\sim I_B$) by collecting the hole current at the collector terminal. The diode displays uniformly low reverse current and an ideality factor n=1. The collector current increases exponentially in the range 0.2V to 0.7V. Below 0.2V the reverse current dominates and above the 0.7V the series resistance in either the base or emitter attenuates the exponential trend. Along with collector current, the base current at low voltages below about 0.2V is dominated by a leakage current that could originate from g-r effects at defects in the emitter-base space-charge or base regions. The leakage current is low at intermediate voltages, slope shows that $n \approx 1$ just as it is for the collector current. At higher voltages the curve deviates from exponential growth due to series resistance.

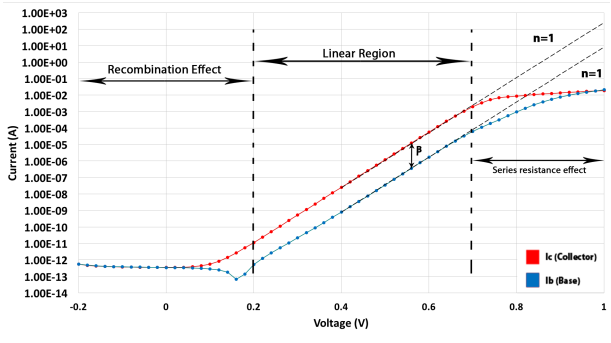

Fig. 10. Gummel plots of HT6 26x431μm^2 (L= 26μm) device showing the effects of emitter-base space charge region recombination($n \approx 1,5-2$), quasi-neutral region recombination($n \approx 1$), and series resistance.

The I-V characteristics of HT20 device structure is compared to the nonanneled device HT6 in Fig. 11. Base currents $I_{B_{E_2}}$ and $I_{B_{E_1}}$ are measured on HT20 and HT6 devices and plotted in Fig. 11. Both base currents of HT20 and HT6 devices display low reverse current and an ideality factor $n =$ 1. Below 0.2V the reverse current dominates and above 0.7V the series resistance determines the current. Base currents of HT6 device $I_{B_{E_2}}$ and $I_{B_{E_1}}$ identically increase exponentially in the range 0.2V to 0.7V. Distinction of these base currents above 0.7V could be explained by the difference in series resistance, which is attributed to the difference of emitter perimeters, as outer emitter has larger perimeter that the inner one. On the other hand, base currents measured for annealed HT20 device were observed to be different over whole measurement range. In order to observe this strange effect, differential $I_{B_{E_2}}$ and $I_{B_{E_1}}$ for HT20 device were plotted against different emitter lengths(Fig. 12).

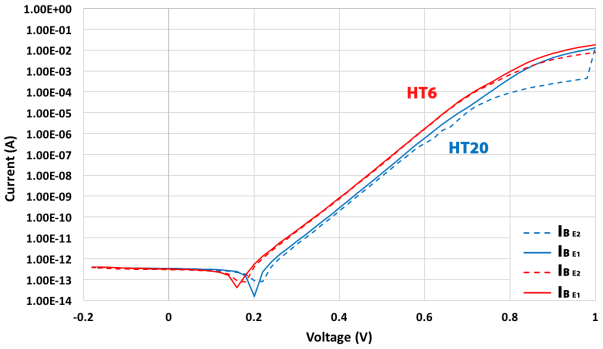

Fig. 11. Gummel plots of $I_{B_{E2}}$, $I_{B_{E1}}$ and I_B as a function of forward bias for HT6 device (red) and a HT20 (blue). The area of measured emitter is 30x431μm^2 (L= 30μm).

The linear growth of differential $I_{B_{E_2}}$ and linear decline of differential $I_{B_{E_1}}$ in Fig. 12, illustrate that the measurements were performed over the whole perimeter and that in the PureB-only region there was no p-type region to be found. This could be explained by an excessive oxidation of the PureB region during the oxidation/anneal step. This, however, is in contrast to the results obtained in reference [10] where the procedure is shown to deliver a highly-doped p-region of about $0,3\mu m$ deep as shown in Fig. 13.

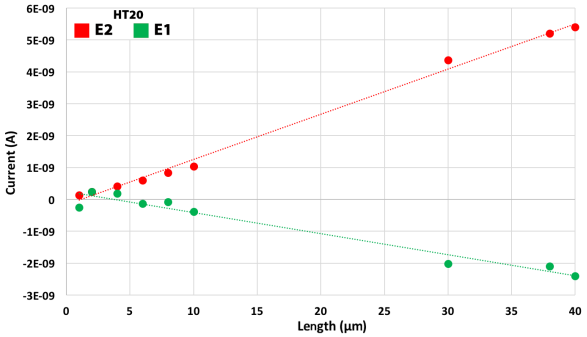

Fig. 12. Measured $I_{B_{E2}}$ and $I_{B_{E1}}$ of HT20 device for various active emitter lengths.

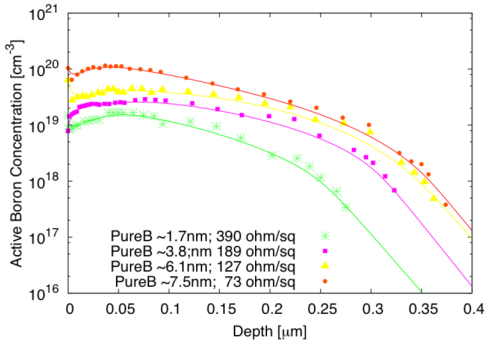

Fig. 13. ECV-measured active boron concentration profiles of various initially deposited PureB layers, followed by thermal annealing at 950°C for 10-min in 14% O_2 concentration [10]. Sheet resistance of these profiles are also included in the legend.

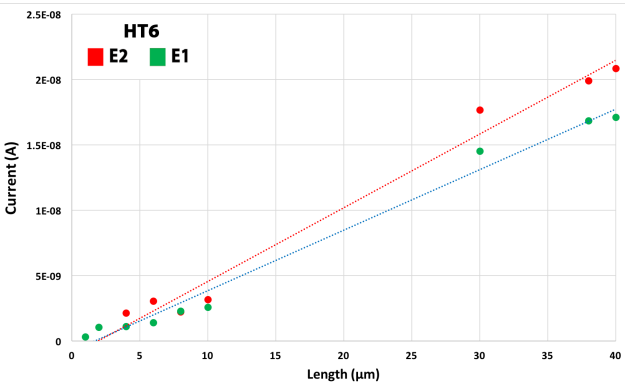

Fig. 14. Measured $I_{B_{E2}}$ and $I_{B_{E1}}$ of HT6 device for various active emitter lengths.

Fig. 14 illustrates differential $I_{B_{E_2}}$ and $I_{B_{E_1}}$ for HT6 device plotted against different emitter lengths. The minor difference between $I_{B_{E_2}}$ and $I_{B_{E_1}}$ is observed for small values of L. With the increase in length of active emitter region, the difference in base currents increases. This could be explained by the radial spreading of the current in the octagonal-ring structures.

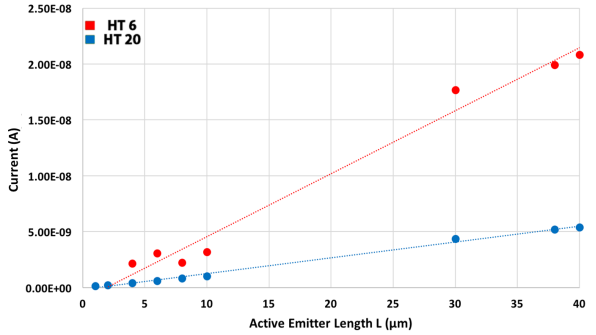

Fig. 15. $I_{B_{E2}}$ at 450mV forward bias for HT6 and HT20 diodes measured for various active emitter lengths.

In order to compare the HT6 and HT20 over the active emitter region, differential $I_{B_{E_2}}$ currents at 0.4V were plotted versus different emitter lengths. The HT6 devices resulted in higher base current that HT20 devices. Higher base current of the nonannealed HT6 device can be explained by surfaces with an interfaces containing a large number of recombination centers because of the abrupt termination of the semiconductor crystal forming efficient recombination centers.

Typical Gummel plots measured on the LT20 and LT40 devices are shown in Fig. 16. At low processing temperatures, the lack of a high-temperature anneal step is often a problem because defects introduced during processing are not removed by thermal diffusion processes. In the two LT devices the shorter deposition time of 20 min for the LT20 devices resulted in about 3 decades higher base current than the LT40 devices. Moreover, as shown in Fig. 17, there is a decade higher spread of the base current measured at 0.4 V forward bias for the LT20 devices. These differences between the two device types do not show any geometry dependence as is demonstrated by Fig. 17 where the I_B is compared for devices with L = 1, 2, 4, 6, 10 and 40 μm.

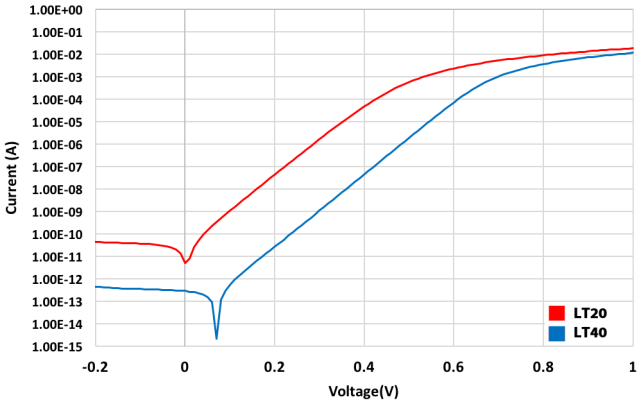

Fig. 16. Gummel plots of the base current as a function of forward bias for LT20 (red) and LT40 (blue). The area of the measured emitter is 10x431μm^2 (L= 10μm).

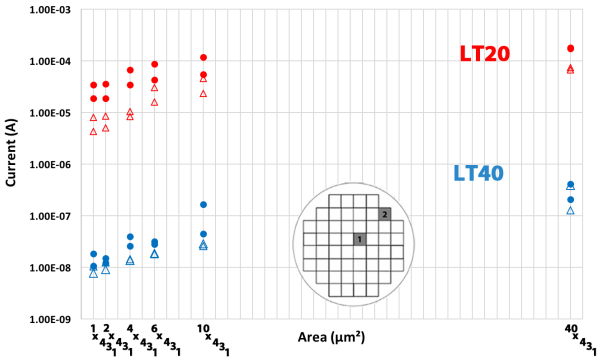

Fig. 17. Diode current spread at 0.4V forward bias for LT20 and LT40 diodes with different areas. Measurements are performed on dies 1 and 2 (shown inset) and 2 diodes per area are measured per die.

Base currents of three different emitters contacted directly by metal were compared with respect to their efficiency for suppressing the electron injection (Fig. 18). In order

to observe injection of currents in the region of interest, differential base currents illustrated in Fig. 18 are plotted against active emitter length. $\triangle I_B$ of HT6 is the lowest among compared devices, which means that Gummel number of the HT6 emitter is the lowest one (section III A). This is expected since, emitter region of the LT20 and LT40 devices is covered with the metal. The suppression of electron injection in LT40 is found to be more efficient than LT20 devices. This shows that different emitter processing may affect the injection of electrons into the emitter region. Due to an experimental misfortune, emitters with dielectric passivation were not available so the effect of recombination along the dielectric interface could not be studied.

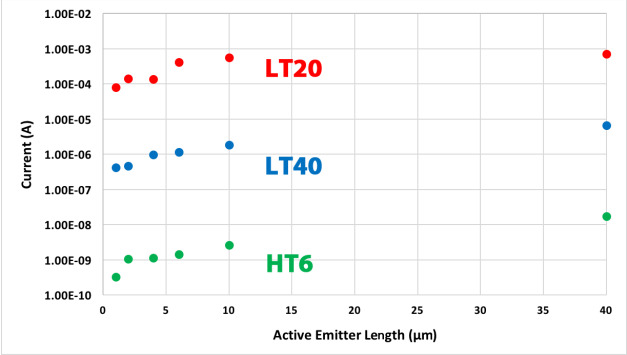

Fig. 18. $\triangle I_B$ of LT20, LT40 and HT6 devices at 0.5V bias plotted versus active emitter length.

B. Sheet Resistance of the Emitter Regions

The sheet resistance of the central emitter region of the HT6 structure was extracted from resistance measurements of a set of octagon-ring structures as shown in Fig. 3. The differential measured resistance values taken between structures with different emitter lengths are plotted in Fig. 19 and they display a linear relation between resistance and length. This indicates that a correct extraction of the PureB emitter R_{sh} can be made. In Fig. 20 the α_{ij} are plotted against Eventually, in order to extract R_{sh} of the PureB, calculated α_{ij} were plotted against R_{ij}. The R_{ij} and α_{ij} are seen to be linearly correlated, and an R_{sh} equal to 17,5kΩ/□ is extracted.

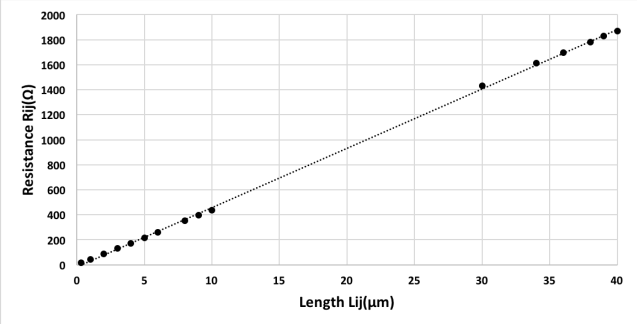

Fig. 19. Subtracted resistance R_{ij} plotted against subtracted active emitter layer length L_{ij}.

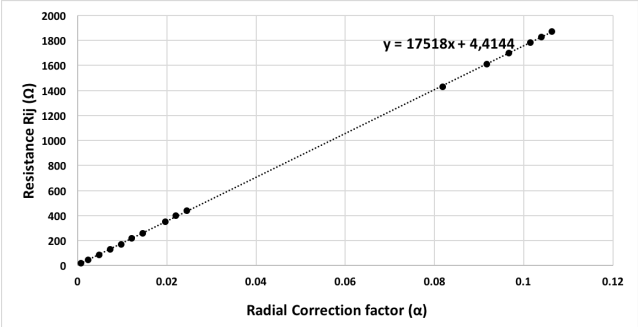

Fig. 20. Subtracted resistance R_{ij} plotted against radial correction factor α_{ij}.

For the HT20 structures, it was not possible to measure the resistance between E_1 and E_2. I-V measurements of the current through E_1 and E_2 also indicated that there was no p-type region to be found Fig.12.

C. Sheet Resistance of the Base Regions

The base sheet resistance values measured for the LT20 and LT40 devices are listed in Table II. The only difference between these structures is the way the emitter is processed. There is no boron doping in the Si, therefore it is not expected that the neutral base width is different.

TABLE II
MEASURED BASE RESISTANCE FOR DIFFERENT TEST STRUCTURES.

Test Structure	Base Resistance
LT20	2,98kΩ/□
LT40	2,96kΩ/□

The sheet resistance of the base region of the HT6 is shown in Table III for the case of with the central PureB-only emitter and the peripheral p+-region. At about 2,4kΩ/□, the values are slightly higher than those of LT devices which is expected since that the PureB-only emitter is slightly deeper for the 700°C deposition. The R_{sh} of the p^+-region has been well-chosen and does not cut off the central base region. Table III also includes the sheet resistance of the base region without any PureB emitter deposition. This gives a base R_{sh} of 1,8kΩ/□, which is slightly lower that the HT6 base R_{sh}. This underlines that the PureB emitter is very shallow.

TABLE III
MEASURED BASE RESISTANCE FOR HT6 DEVICE.

Test Structure	Base Resistance
no PureB emitter	1,78kΩ/□
PureB-only emitter	2,38kΩ/□
p^+ emitter region	2,43kΩ/□

As for the emitter sheet resistance, the base R_{sh} could not be measured for the HT20 device. This suggests that the whole central base region has been cut off from the n^+-contact regions by the anneal/oxidation of the PureB deposition.

V. CONCLUSION

In this paper, *pnp* bipolar test structures were used to evaluate several types of emitters fabricated using PureB depositions with respect to their efficiency in suppressing electron injection from the base region. By using different test-structure geometries and a differential measurement technique the minority carrier electron injection into the emitter was determined for each region of interest. Three different emitters contacted directly by metal were compared with respect to their efficiency for suppressing the electron injection from the base and base leakage currents. Due to an experimental misfortune, emitters with dielectric passivation were not available so the effect of recombination along the dielectric interface could not be studied. So, future studies may be focused on this structures and more detailed analysis may be performed. Additionally, the differential measurement technique was performed on test structures in order to extract the sheet resistance of the PureB-only emitter and the base region. Eventually, experimental investigation on the new test structures provided insights on the surface recombination of solar cell and eventually proved that they are suitable for analysing the efficiency of solar cells.

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