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Faculty of Electrical Engineering,
Mathematics & Computer Science

Electrical measurement method and test structures for determining continuity of ultra-thin conducting or insulating films.

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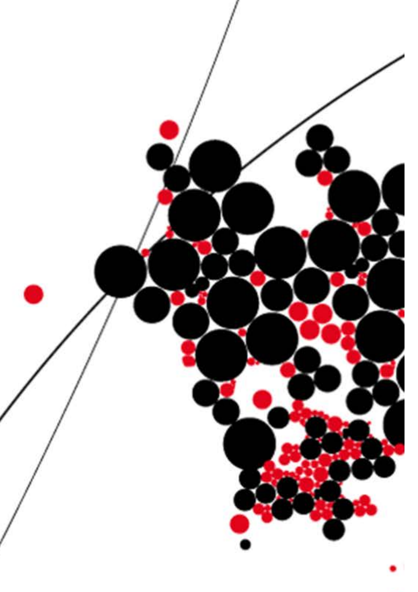

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Abstract

Ultra-thin films can be used for many interesting new applications in the field of microelectronics. The thickness of ultra-thin films ranges from sub-nanometer to a few tens of a nanometer. The various new applications require either discontinuous, percolated (almost continuous) or continuous ultra-thin films. Therefore it is critical to know the continuity of the deposited ultra-thin film. Currently there are no standard methods or test structures to determine the continuity of an ultra-thin film. The goal of this project is to design a methodology and corresponding test structures, to determine the closure point of conducting or insulating ultra-thin films.

The established methodology for determining the continuity for conducting ultra-thin films is a combination of two methods. The first method is to look at the conduction mechanism of the film by measuring the I-V characteristics. Continuous conducting ultra-thin films have an ohmic conduction mechanisms, whereas discontinuous conducting ultra-thin films have non-ohmic conduction. The two conduction mechanisms can be distinguished by analyzing the I-V characteristics of the film. When the conduction mechanisms goes from non-ohmic to ohmic, the film is expected to become continuous. The second method is a method proposed by Maroof and Evans. They state that the minimum value in the Rt^2 vs thickness plot is the onset of a continuous film, where R is the resistance and t is the thickness of the film. The continuity of insulating ultra-thin films can also be determined by measuring the I-V characteristics of the film. The film is sandwiched between two electrodes. When the film is discontinuous the conduction mechanism is ohmic, the two electrodes are in contact. When the film is continuous the conduction mechanism is non-ohmic, the current has to tunnel through the continuous insulating film.

During this project test structures for both the conducting and the insulating ultra-thin films are designed, keeping the chosen methodologies in mind. Masks are designed to be able to fabricate the structures in the MESA+ nanolab of the University of Twente. During this project tungten (W) and aluminium nitride (AlN) are used as a conducting and insulating material respectively, to show the effectiveness of the methodologies and corresponding test structures. Two process flows are composed, one for the conducting and one for the insulating films. Measurements of 6 W ultra-thin films and 4 AlN ultra-thin films, with different thicknesses, are done. Both of the methods for the conducting ultra-thin films indicate that the W film becomes continuous between 1.3 and 2.2nm. The method for the insulating ultra-thin films indicates that the AlN film becomes continuous between 4 and 11nm.

The drawn conclusions are compared to SE measurements done during the deposition of the films. The SE measurements of the W films show a sharp increase, caused by an incorrect model at this point. It is speculated that the incorrectness of the model is related to the change from a discontinuous to a continuous film. Interpreted in terms of film thickness this change falls in the same range as for the electrically found closure points of the W films. The growth rate of the AlN films becomes constant when the substrate is completely covered. The growth is no longer influenced by the substrate. For AlN films constant growth rate was established in the same range as the electrically found closure points of the films. This proves that the designed methodologies and corresponding test structures can be used to determine the closing point of conducting or insulating ultra-thin films.

Abbreviations

a-Si Amorphous silicon.

ALD Atomic layer deposition.

AlN Aluminium nitride.

CTLM Circular transfer length model.

CVD Chemical vapor deposition.

FM Frank-van der Merwe.

HF Hydrogen fluoride.

NCNV Nano-crystalline non-volatile.

Pt Platinum.

PUF Physical unclonable functions.

R Film resistance.

SE Spectroscopic ellipsometry.

SiO_2 Silicon oxide.

SK Stranski-Krastanov.

t Film thickness.

VW Volmer-Weber.

W Tungsten.

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Chapter 1

Introduction

Ultra-thin films can be used for many interesting new applications in the field of micro-electronics. The thickness of ultra-thin films ranges from sub-nanometer to a few tens of a nanometer. Applications that can be made using ultra-thin films are for example: nano-crystalline non-volatile (NCNV) memories, physical unclonable functions (PUF) or field effect devices. NCNV memories make use of a discontinuous ultra thin film, whereas PUF are made with so-called percolated (almost continuous) films. Field effect devices make use of continuous ultra-thin films. The differences of the ultra-thin films in the three examples of applications show that it is very important to know if the deposited ultra-thin film is continuous or discontinuous. Currently there are no standard methods or test structures to determine the continuity of an ultra-thin film.

The goal of this project is to design a methodology and corresponding test structures to determine the closure point of conducting or insulating ultra-thin films. Aluminium nitride (AlN) and tungsten (W) are used, as an insulating and conducting material respectively, to show the effectiveness of the designed methodologies and the designed test structures. With the designed methodologies and corresponding test structures, designed during this project, it should be possible to determine the continuity of conducting or insulating ultra-thin films.

This report starts with background information about ultra-thin films, in chapter 2. The growth modes of ultra-thin films, deposition method for ultra-thin films and applications of ultra-thin films are discussed. Chapter 3 explains the conduction mechanisms in continuous or discontinuous conducting ultra-thin films. With this in mind the methodology of determining the continuity of conducting or insulating ultra-thin films is established. In chapter 4 the test structures corresponding the previous discussed methodologies are designed. In order to prove that the methodologies and test structures work, the test structures have been fabricated. The fabrication process of the designed structures is explained in chapter 5. Chapter 6 shows the measurement results of the fabricated wafers. The measurement results are analyzed and some conclusions are drawn in this chapter. This work is concluded in chapter 7. Some recommendations for further research are done in chapter 8.

Chapter 2

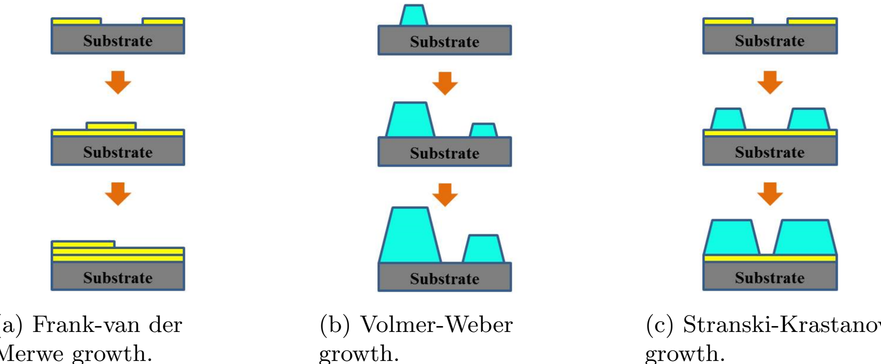
Ultra-thin films

In this chapter ultra-thin films are discussed in more detail. Ultra-thin films can grow in different manners, so-called modes. The different growth modes of ultra-thin films can be utilized in interesting new applications. In this chapter three examples of these applications are elaborated, each using a different type of ultra-thin film. For these applications the ultra-thin films have to be deposited with well-controlled thicknesses. The deposition technique used during this project is discussed. With this deposition technique the tungsten (W) and aluminium nitride (AlN) films studied during this project are deposited. During deposition of the films the thickness is monitored in-situ by spectroscopic ellipsometry (SE). This measurement technique is discussed briefly in this chapter.

2.1 Growth modes

Ultra-thin films can grow epitaxial in one of three growth modes. Epitaxial means that the crystals of one material grow onto another material while keeping the same crystal orientation. The theory explaining these growth modes is originally proposed by Bauer, and is nowadays generally accepted [1, 2]. The three growth modes can be seen in figure 2.1. The growth depends strongly on the interaction strength between adatoms (an adatom is an atom that lies on a crystal surface) and the substrate. With Frank-van der Merwe (FM) growth (shown in figure 2.1a), the adatoms-surface interactions are stronger than the adatoms-adatoms interactions. This induces the growth of a complete layer before the next layers are grown. Thus a continuous film is formed in the early stages of the film growth. With Volmer-Weber (VW) growth (shown in figure 2.1b), the interactions between the adatoms is stronger than the interaction with the surface leading to the growth of clusters or islands. While growing a film in VW mode the islands increase in size and number, and finally interconnect. This point is called the percolation threshold. The film is called a percolated film at this point. After this the film will gradually close and form a continuous layer. Stranski-Krastanov (SK) growth (shown in figure 2.1c) is an intermediate growth mode where the initial growth start is in a layer by layer fashion, after a certain thickness the growth changes to island-based growth. This thickness depends on various properties, such as surface energies and lattice parameters.

An important observation that can be seen in figure 2.1 is that none of these growth modes immediately enables a continuous film.



(a) Frank-van der Merwe growth.

(b) Volmer-Weber growth.

(c) Stranski-Krastanov growth.

Figure 2.1: Growth modes of ultra-thin films [1].

2.2 Applications

A lot of applications can be improved with, or depend on the use of an ultra-thin films. The previously explained growth modes of ultra-thin films and their different stages (discontinuous,percolated and continuous) can be exploited for these applications. Three examples are shown below. For each of these examples a different type of film is required (discontinuous, percolated and continuous, respectively). This shows that precise control of the deposition (i.e. thickness) of the ultra-thin film is very important. It is crucial to know the morphology and properties of the deposited film.

Nano-crystalline non-volatile (NCNV) memories make use of discontinuous ultra-thin films. Conventional nonvolatile memories are made with a MOS structure in combination with a polycrystalline floating gate which is used as the memory element. Data is stored by charge injection to the floating gate. The tunnel oxide must be thick enough to prevent charge loss to the contacts, but thicker oxides requires high injection voltages. Claims are made that replacing the continuous polycrystalline floating gate by discrete silicon nano-crystals embedded in a dielectric matrix (see figure 2.2) can reduce the leakage current. To allow the use of thinner tunneling oxides, lowering the voltage needed for charge injection [3, 4].

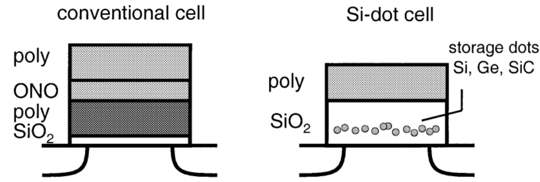


Figure 2.2: Schematic representation of a conventional and NCNV memory [4].

Physical unclonable functions (PUF) make use of the so-called percolated films. Figure 2.3 shows such a percolated film. A PUF is practically impossible to duplicate, even given the exact manufacturing process. It was first introduced by Pappu et al as a physical one-way function [5]. The PUF exploits the fact that a percolated film is actually just a number of randomly grown resistors, forming a PUF circuit. These circuits can be used to electronically secure a device. A signal can be put in to such a system and the response will be different for every PUF, because of the randomly generated resistors network.

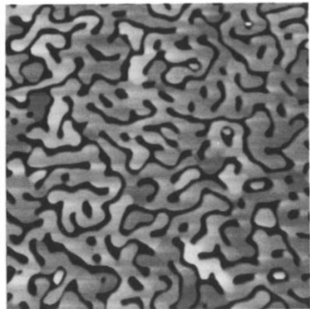


Figure 2.3: Atomic force microscope image of a percolated Ag film (bright = conducting, dark = isolating) [6].

Field effect devices make use of continuous ultra-thin films. Field effect is the ability to manipulate the electrical conductivity of a material by applying an external electric field. In semiconductors the number of carriers (electrons and holes) that can respond to the applied field is relatively low. Therefore the field can penetrate quite far into the material. Redistribution of the carriers is caused and this changes the conductivity of the semiconductor near the surface. In metals, where the electron density is much higher, when an electric field is applied, a surplus of charges is created which blocks the penetration of the electric field into the material [7]. Therefore, to be able to observe field effect in metals the film thickness must be comparable to the penetration depth of the field. When ultra-thin metallic films are deposited, the conductivity of these films can possible be manipulated by the field effect.

2.3 Atomic layer deposition

Ultra-thin films can be deposited by various methods. Historically thin films are deposited by chemical vapor deposition (CVD) and sputtering. The problem with these two deposition techniques for deposition of ultra-thin films is the conformality, further it is difficult to control the growth down to sub-nanometer range. The deposition method used in this project to deposit the ultra-thin films is atomic layer deposition (ALD). ALD is an ideal tool for achieving the deposition of ultra-thin films due to its fundamental property of self-limiting surface reactions. This fundamental property of ALD allows for a precise control of thickness. ALD will be discussed in more detail below, followed by a description of the deposition cycles for the tungsten (W) and AlN films used during this project.

ALD is a deposition method that is considered as a subclass of CVD. ALD is based on the sequential use of gases that react with the surface of the substrate. A schematic illustration of the ALD process is shown in figure 2.4. This is a self-limiting process; when the whole surface has reacted the reaction would stop. In between of giving the reactive gases the reaction chamber is purged. Then, the next gas is introduced in the system. This gas will react with the newly formed surface. By sequencing this process a thin film will be grown on the substrate. The materials grown during this project are W and AlN. These materials are chosen because within the Semiconductor Components group there is already experience in the ALD deposition of these materials.

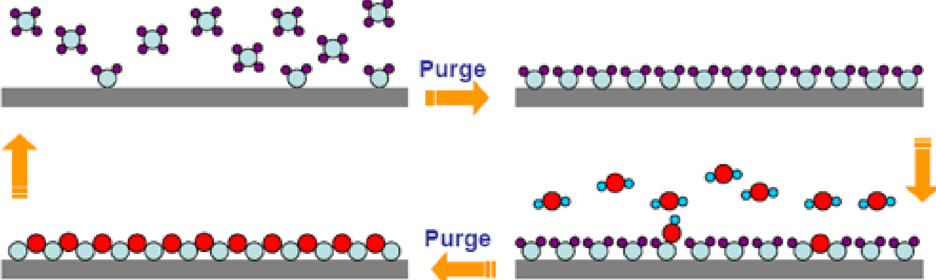


Figure 2.4: Schematic illustration of the ALD process [8].

2.3.1 Tungsten (W)

To note, the actual deposition of the W films during this project is done by PhD student M. Yang. A summary of the process is described below, details are provided in the paper of M. Yang [9]. The W film needs a seed layer to start the initial growth. The seed layer is made by depositing approximately 0.6nm of amorphous silicon (a-Si) on the substrate. This a-Si is converted to W by introducing WF_6 gas in the system. Upon this W seed layer the film is deposited. First WF_6 gas is introduced in the system, the system is purged and after that atomic H is used as the subsequent gas. These two gases are sequenced and the W film will be grown. The atomic H is generated from H_2 by catalytic thermal dissociation on a heated filament (or hot-wire).

2.3.2 Aluminium nitride (AlN)

The actual deposition of the AlN films in this work is done by PhD student S. Banerjee. ALD of AlN, opposite to the ALD of W, does not need a seed layer for the film to start growing. The first gas introduced in the system is trimethylamine (TMA) this gas reacts with the functional groups of the silicon oxide substrate. The system is purged and then the second gas is introduced in the system. The second gas used is NH_3. This gas reacts with the newly formed surface. By sequencing these two gases and purging the system, the AlN film can be grown.

2.4 In-situ thickness measurements by spectroscopic ellipsometry (SE)

During this project several ultra-thin films of various thicknesses are deposited. To ensure the right thickness is deposited onto the wafer it is important to monitor the thickness of the ultra-thin films during deposition. These measurements are done by spectroscopic ellipsometry (SE). SE is an optical technique for characterization of thin films, which uses polarized light. Figure 2.5 shows a schematic setup of a SE measurement. The light source irradiates polarized light on the surface. SE measures the change in polarization of the light that is reflected from the material. Thickness of individual materials and optical properties determine the change in polarization. Therefore SE is mostly used to determine the thickness of films and the optical constants.

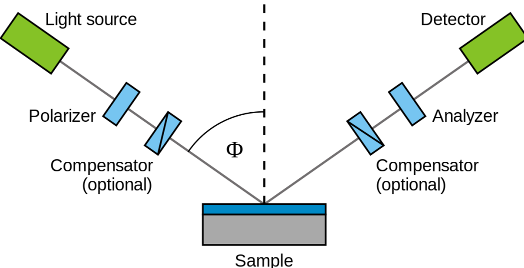


Figure 2.5: Schematic of a spectroscopic ellipsometry (SE) setup [10].

It is important to note that, the measured thicknesses are average within the optical beam area, as the light source has a certain light beam width. When a film grows in island fashion, the islands might be smaller than the diameter of the beam. This results in a "quasi effective" thickness of the film instead of the real thickness of the islands. When the film is continuous, the measured thickness corresponds better to the real thickness.

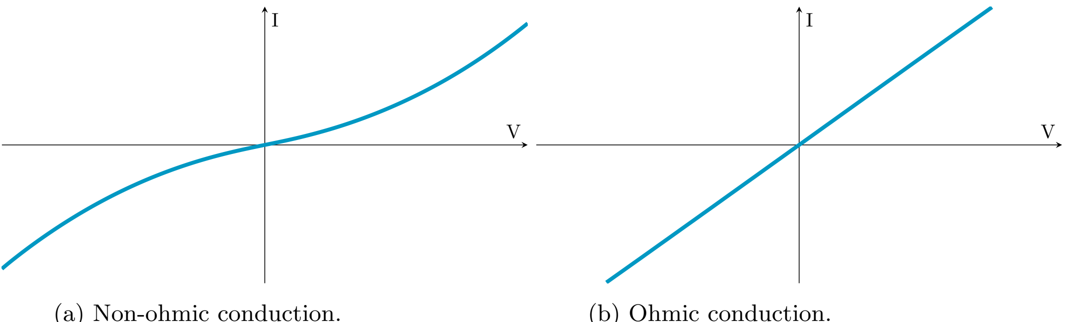
Chapter 3

Methodology

The goal of this project is to design a methodology and corresponding test structures for determining the continuity of conducting or insulating ultra-thin films. In this chapter the designed methodologies are discussed. These methodologies make use of the differences between the conduction mechanisms in a discontinuous and continuous conducting ultra-thin film. The conduction mechanisms in discontinuous and continuous ultra-thin films are discussed first in this chapter. With the difference of the conduction behavior in mind the methodologies are developed.

3.1 Conduction mechanisms

In the different stages of the conducting ultra-thin film growth the conduction mechanism of the film differs. When the film is discontinuous, the conduction mechanism exhibits a non-ohmic conduction behavior. The electrons hop or tunnel from one island to another. The typical I-V curve can be seen in figure 3.1a. There are several types of non-ohmic conduction mechanisms; the dominant mechanism is determined by the voltage applied to the film [11, 12]. All of these non-ohmic conduction mechanisms rely on the fact that electrons will pass through a barrier. The non-ohmic current is not linearly proportional to the voltage, as the latter influences the barrier height or shape. While the islands grow in size and number, some of the islands will interconnect. The conduction mechanism in these films is a combination of ohmic conduction, through the network of connected islands, and non-ohmic conduction at the closely spaced, but not connected, islands. Meaning that the distance between islands is still small enough to enable tunneling, the barrier width can however vary dependent on the distance. When the film becomes continuous the conduction mechanism in the film will become ohmic. The electrons can freely flow trough the material and the current becomes linearly proportional to the voltage applied to the film. This ohmic conduction can be seen in figure 3.1b.



(a) Non-ohmic conduction.

(b) Ohmic conduction.

Figure 3.1: Non-ohmic and ohmic conduction.

3.2 Methodology for conducting films

The conduction mechanisms in continuous and discontinuous conducting ultra-thin films significantly differ. They have a very different I-V characteristic as shown in chapter 3.1. Because of this a distinction between the continuous and discontinuous films can be made. When the conduction mechanisms changes from non-ohmic to ohmic, the ultra-thin film is expected to become continuous. This is the first method used to determine whether a conducting film is continuous or not. The second method is described below.

For conducting films several studies have been preformed to find the closure point [13, 14]. One general method was developed and proofed to be effective, proposed by Maroof and Evans [15]. They plot the measured resistance (R) times the thickness squared (t^2) as a function of the approximate thickness of the film (Rt^2 vs t). An example of such a graph can be seen in figure 3.2. Maroof and Evans state that the minimum in this plot is the thickness at which the film becomes continuous. As the resistance of the film is very high in the discontinuous region, it is comparable to the resistance of the insulating substrate. With continued deposition the islands grow in size and these islands will interconnect. In this region the resistance of the film drops drastically. The resistance of the film will keep decreasing with increasing film thickness. At a certain point the film will become continuous and the resistance will reach its bulk value; this will appear as the minimum value in the $Rt^2(t)$ graph. After reaching the bulk value R remains independent on t, leading to a gradual increase of $Rt^2(t)$.

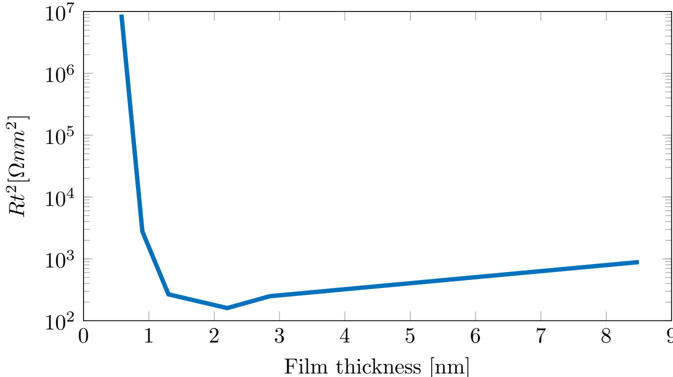


Figure 3.2: Graph shows $Rt^2(t)$, so that the onset of a continuous film can be identified.

In this project the continuity of the conducting ultra-thin films will be examined, by (i) monitoring the conduction behavior (i.e. ohmic/non-ohmic conduction) and (ii) analyzing the $Rt^2(t)$ curve.

3.3 Methodology for insulating films

Insulating films do not conduct current when sufficiently thick, therefore the methods for conducting films do not work for insulating films. A different method is needed to determine the continuity of insulating films. For a thin insulating film, electrons can still tunnel through it, which will result in a tunneling current and non-linear I-V curves [11, 12]. To enable such a tunneling cunduction, the films should be sandwiched between to electrodes. The typical expected I-V characteristic of a continuous insulating ultra-film, sandwiched between two electrodes, can be seen in figure 3.3.

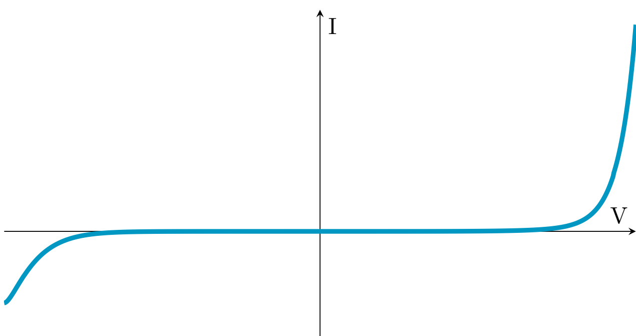
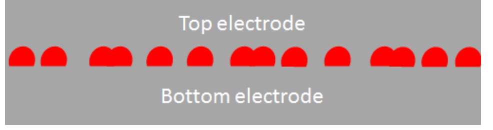
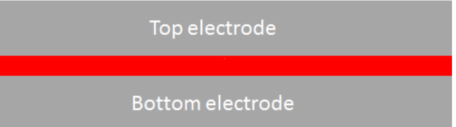


Figure 3.3: Non-ohmic I-V characteristic of a continuous insulating film sandwiched between two electrodes.

The above described I-V characteristics can be used for determining the continuity of an insulating ultra-thin film, by measuring the I-V characteristics. When the film is discontinuous the top and bottom metal electrode are in direct contact (figure 3.4a). This results in an ohmic I-V characteristic giving linear I-V curves. When the film is continuous the top and bottom electrode are no longer in contact (figure 3.4b) and electrons will tunnel through the insulating film. This results in a non-ohmic conduction mechanism giving non-linear I-V curves. When the conduction mechanism changes from ohmic to non-ohmic conduction the ultra-thin film is expected to become continuous. This method can be used to determine whether an insulating ultra-film is continuous or not.



(a) Discontinuous film, the top and bottom electrodes are in contact. Resulting in linear I-V curves.



(b) Continuous film, electrons can tunnel through the film. Resulting in non-linear I-V curves.

Figure 3.4: Discontinuous and continuous insulating film sandwiched between two metal electrodes.

3.4 Conclusion

In this chapter the methodology of determining the continuity of conducting or insulating ultra-thin films is described. The continuity of conducting ultra-thin films will be determined by performing I-V measurements. When the conduction mechanism changes from non-ohmic to ohmic behavior the film is expected to become continuous. For conducting films, the method of Maroof and Evans will also be used to determine film continuity. The insulating ultra-thin film is sandwiched between two electrode. When the conduction mechanism changes from ohmic to non-ohmic the film is expected to become continuous.

Chapter 4

Test structure lay-out and mask design

In the previous chapter the methodology for determining the continuity of conducting or insulating ultra-thin films is established. Based on this methodology test structures are designed. For I-V measurements it is necessary to have a structure consisting of two conductive electrodes and the film of interest in between. In this chapter the designs are further elaborated.

4.1 Test structures

For both the conducting and the insulating ultra-thin films, test structures are designed. The designs are discussed below.

4.1.1 Conducting ultra-thin films

For conducting films the test structures can be relatively simple. Two types of measurement structures are designed, the so-called circular transfer length model (CTLM) structures [16, 17] and linear bar structures.

CTLM structures

Figure 4.1 shows a schematic representation of a CTLM structure. The ultra-thin film is deposited on top of this structure. The main benefit of a CTLM structure, compared to other structures, is that the current path is confined by the outer ring. No extra patterning step of the ultra-thin film is needed to confine the current path for these structures. The gap spacing (S) between the inner and outer circle(s) is varied, from 2.5 μm to 300 μm. These variations in gap spacing are used to extract the resistivity of the films and the contact resistance.

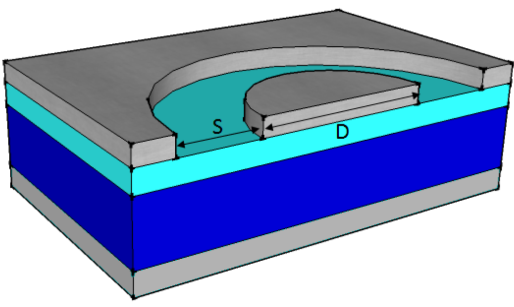


Figure 4.1: Schematic representation of a CTLM structure.

Bar structures

In figure 4.2 the linear bar structures can be seen. The bar structures are designed to further compare the measurement results of the CTLM structures and these bar structures. Because the ultra-thin film is deposited onto the entire wafer, the ultra thin film is also on the edges of the electrodes. Therefore it is expected that current will also flow from the edges of the bar structures. The current path is not confined compared to the CTLM structures. To further investigate the impact of this design on the I-V characteristics, several variations of these structures are designed. The length of the bars (L) is varied, to see if the ratio of the length of the bars compared to the gap between the bars (S) can influence the results of the measurements.

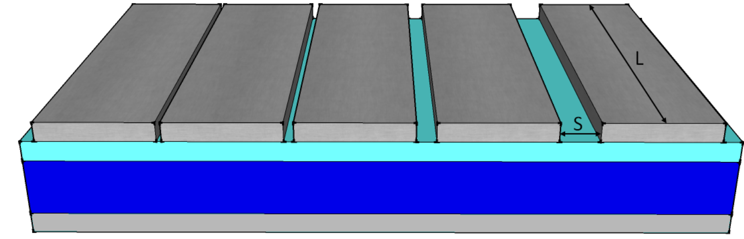
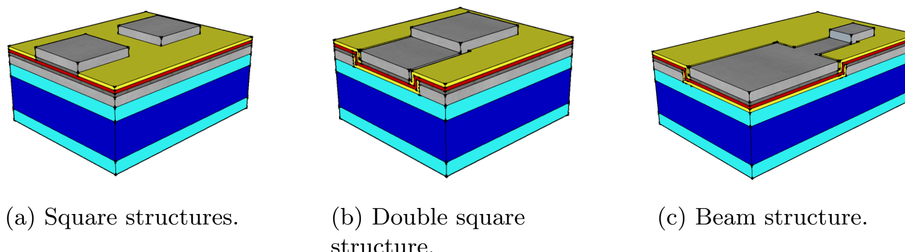


Figure 4.2: Schematic representation of the linear bars structures.

4.1.2 Insulating ultra-thin films

The methodology for determining the continuity of insulating ultra-thin films is also based on I-V measurements, as described in chapter 3.3. Three variations of structures are designed, they can be seen in figure 4.3. The design details are discussed below.



(a) Square structures.

(b) Double square structure.

(c) Beam structure.

Figure 4.3: Schematic representation of the three test structures designed for insulating films.

Figure 4.3a shows the first type of the test structures. In this structure the top electrode is a square ranging in surface area from 100 x 100 μm^2 to 500 x 500 μm^2. A possible problem with this structure is that for the I-V measurements the electrodes have to be probed by applying a force to the top electrode and possibly affecting the unerlying film. The films are fragile because of there thickness, also AlN is a piezoelectric material. Piezoelectric materials are materials that physically shrink or expand when an electric field is applied. On the other hand, the material produces an electric field when a force is applied on the film. The latter can be the case for this type of test structure. The possible damage of the film and the piezoelectric properties of the material could possibly influence the measurements.

Due to these reasons, a second type is designed, see figure 4.3b. It is designed in such a way that the force of the probing needle is not applied on the same place as where the

current is flowing. These structures consist of two squares as a top electrode. Underneath one of the squares there is no bottom electrode and under the other square there is a bottom electrode. The absence of the bottom electrode underneath one of the squares makes it possible to probe the structure without influencing the film. The effective area of the test structures again ranges from 100 x 100 μm^2 to 500 x 500 μm^2.

Areas much smaller than 100 x 100 μm^2 cannot physically be probed with the probing station used for the measurements. The last type of the test structures is designed to be able to measure effective areas smaller than 100 x 100 μm^2. This test structure can be seen in figure 4.3c. The square that is probed has a surface area of 100 x 100 μm^2 which can still be probed. The effective areas of these structures ranges from 2.5 x 2.5 μm^2 to 100 x 100 μm^2.

4.2 Mask Design

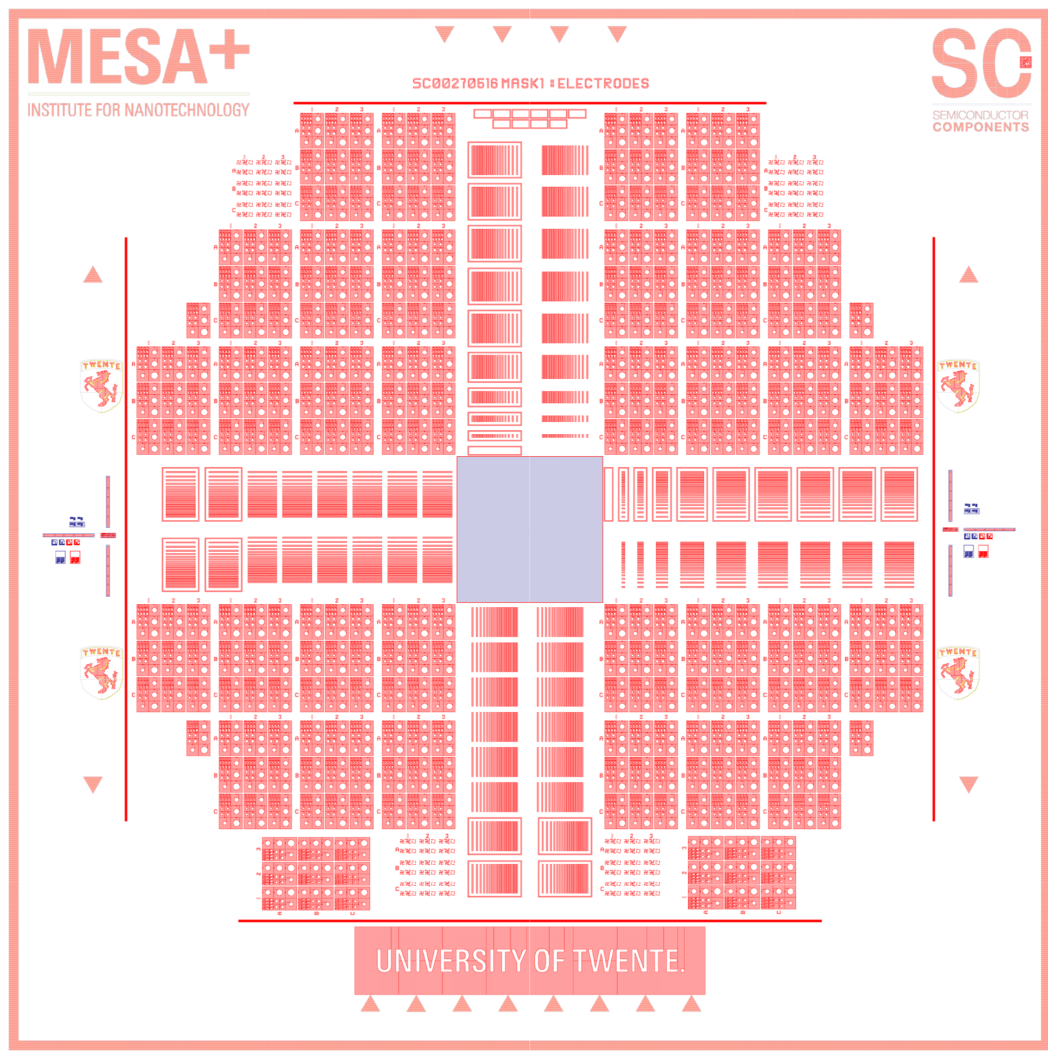
For the realization of the designed structures, patterned electrodes are made. This is done by a so-called lift-off process, which will be further described in chapter 5.1. A mask is required in order to use the lift off process. The design of these masks is discussed in this chapter. The masks are designed with Cadence software.

The structures designed for measuring the metallic ultra-thin films can be fabricated with one mask, as there is only one metal layer that has to be patterned. The structures designed for measuring the insulating ultra-thin films have to be fabricated with two masks as both the top and bottom electrode have to be patterned in 2 separate processes. Several variations of the test structures are included on the masks, allowing for a variety of measurements. Also some structures that are not discussed are included in the mask designs, for possible future research. These structures are not discussed further in this report because they are not used in this project. The extra structures can be seen in appendix A. Images of the full mask designs are shown in figure 4.4 and 4.6, these designs are further discussed below.

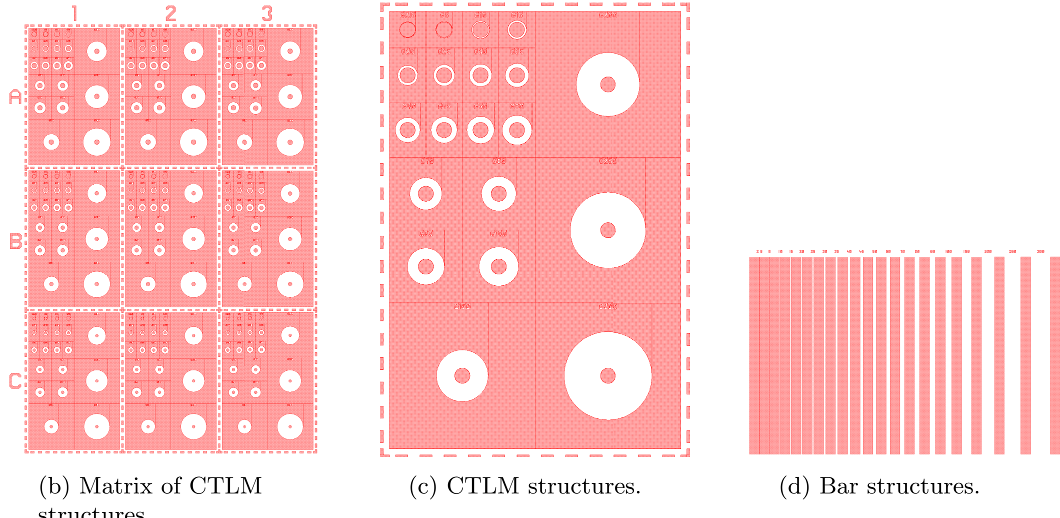
4.2.1 Conducting ultra-thin films

The wafer layout for the metallic ultra-thin films can be seen in figure 4.4a. The CTLM structures are arranged in a matrix (see figure 4.4b). This allows to distinguish the individual test structures, each of the entries in the matrix consists of 20 CTLM structures with gaps ranging from 2.5 µm to 500 µm (see figure 4.4c). For each of the three rows in the matrix the diameter of the inner circle differs. Row A contains CTLM structures with an inner circle diameter of 125 µm. Row B contains CTLM structures with an inner circle diameter of 100 µm and row C contains CTLM structures with an inner circle diameter of 75 µm.

The linear bar structures can be seen in figure 4.4d, spacing between the bars ranges from 2.5 µm to 500 µm. The spacing between the bars is the same as the spacings of the CTLM structures, this allows for a comparison of the measurement results of the two types of structures. The length of the bars is varied between 100 µm and 3000 µm, this allows for an investigation of the side effects compared to the length of the bars and the gap spacing.



(a) Complete mask layout.



(b) Matrix of CTLM structures.

(c) CTLM structures.

(d) Bar structures.

Figure 4.4: Wafer layout and groups of individual test structures for metallic ultra-thin films.

4.2.2 Insulating ultra-thin films

The masks designs for insulating ultra-thin films are depicted in figure 4.6. As mentioned, 2 masks are designed for these structures. For the bottom electrode the mask is designed in such a way that the structures drawn on this mask, are the holes in the bottom electrode. No metal is present at these areas after lift-off. For the top electrode the mask design is reverse; meaning that the areas drawn are the areas where metal is present after lift-off. An example of this is shown in figure 4.5, the blue mask is the mask for the bottom electrode and the red mask is the mask for the top electrode.

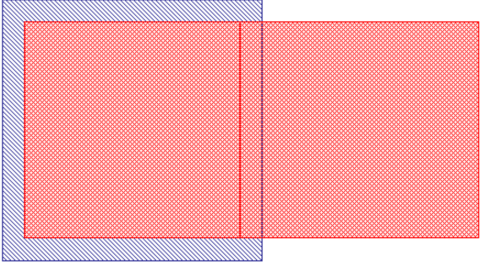
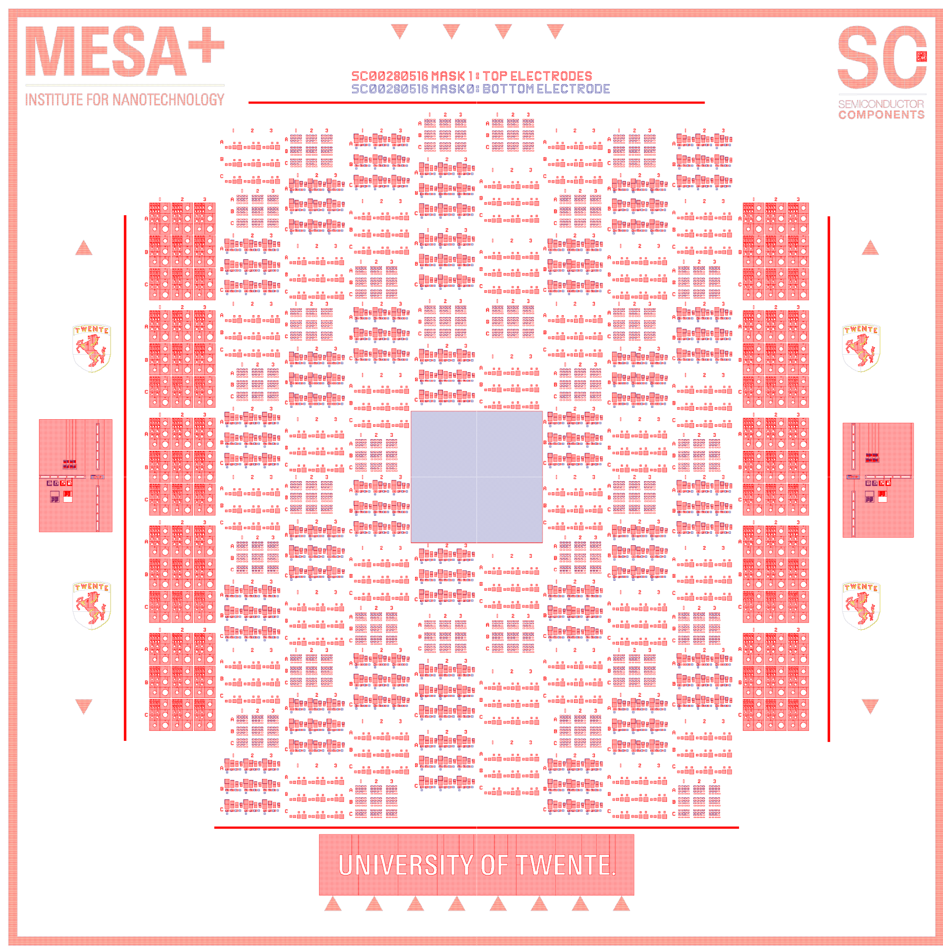
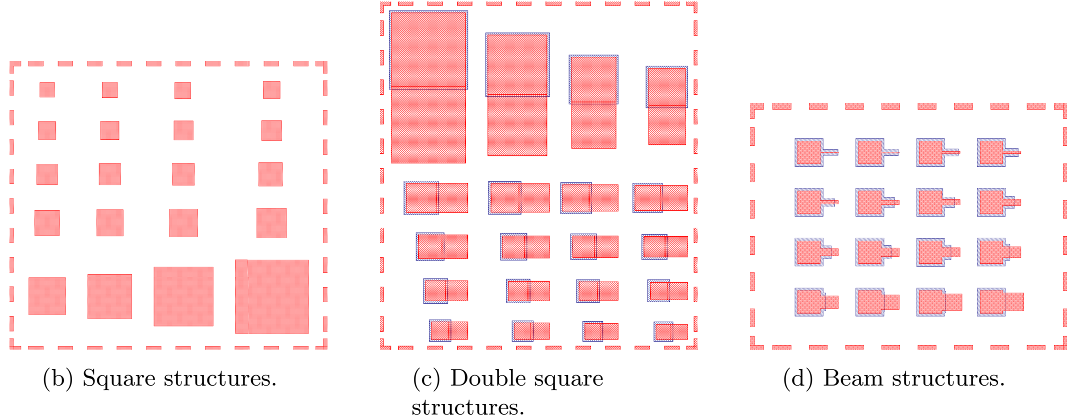


Figure 4.5: Example of the mask design with bottom area (blue) where no metal is present and the top area (red) where metal is present after lift-off.

Three types of structures are present on the masks for the insulating films, as discussed previously (section 4.1.2). For easy finding, the structures are grouped in blocks. Each block contains several test structures of the same type with changing effective area's. Figures 4.6b, 4.6c and 4.6d show the first, second and third type of the structures respectively.



(a) Complete mask layout.



(b) Square structures. (c) Double square structures. (d) Beam structures.

Figure 4.6: Wafer layout and groups of individual test structures for insulating ultra-thin films.

Chapter 5

Fabrication of test structures

In this chapter the fabrication process of the test structures is discussed. The patterning of electrodes is done via a so-called lift-off process, which will be explained briefly. The process flows for fabricating both types of test structures are explained and the key steps in these processes are discussed in more detail. During this project the designed test structures are made, using the developed process flow, in the MESA+ nanolab of the University of Twente. During the fabrication of the test structures observations are made and problems are solved, the findings are discussed in this chapter.

5.1 Lift-off

During this project the electrodes are patterned by a lift-off process. Lift-off is chosen because platinum (Pt) (which is used for the electrodes) is a material which, due to its chemical inertness, is hard to pattern by chemical means. The general lift-off process can be seen in figure 5.1 and is explained below.

The lift-off process starts by spin coating of photoresist on the substrate. This photoresist is exposed to UV light with the use of a mask and a mask aligner. In the MESA+ nanolab, typically positive photoresist is used. Positive photoresist that is exposed to light becomes soluble in the photoresist developer. Developing the photoresist, creates a pattern on the substrate. The material that has to be patterned is then deposited onto the entire wafer. The last step is dissolving the photoresist in acetone, the material that is on top of this photoresist is washed off together with the photoresist. Dissolving of the photoresist can be aided by putting a beaker with the wafer in acetone, in an ultrasound bath. After this, only the material that is in direct contact with the substrate remains on the substrate. This concludes the lift-off process.

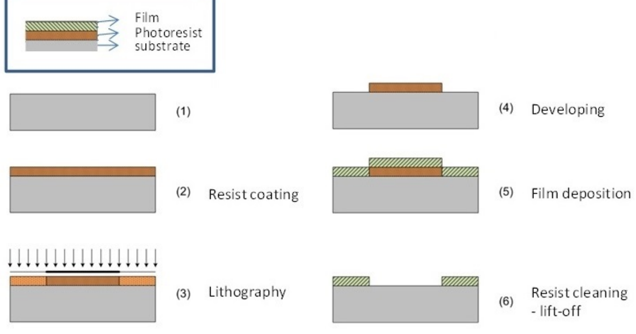


Figure 5.1: Graphical overview of the lift-off process. [18]

5.2 Process flows

For this project two process flows are developed, namely for the conducting and insulating ultra-thin film test structures. Both the process flows are described below and a graphical flow chart is depicted in table 5.1 and table 5.2. Detailed process flows are included in appendix B and appendix C. The detailed process flows are important because they contain the precise steps that are preformed in the nanolab. Crucial parameters such as time and temperatures are specified here.

5.2.1 Conducting ultra-thin films

The graphical overview of the process flow for the conducting ultra-thin film test structures can be seen in table 5.1. The steps mentioned in this table correspond to the steps of the detailed process flow in appendix B.

The substrate used in this process is a p++ silicon wafer. The wafer is p++ because in a subsequent step, a gate electrode will be deposited on the backside of the wafer for possible field effect measurements. If the wafer was not highly doped it would not be conductive enough to act as a gate for the field effect measurements. First the wafer is cleaned. Then 100 nm silicon oxide (SiO_2) is grown on the wafers. This SiO_2 acts as the gate oxide for the field effect measurements and isolates the metallic electrodes from the conducting wafer. The oxide is thermally grown in the furnace, therefore the oxide will automatically be grown on both sides of the wafer.

The next step is to deposit and pattern the Pt electrodes. The mask used for patterning is discussed in chapter 4.1.1. Patterning is done by a standard lift-off process as described in section 5.1. To enhance the lift off process the SiO_2 substrate is etched slightly by 1% hydrogen fluoride (HF) after developing the photoresist. This causes bad step coverage during Pt sputtering and therefore ensures that the acetone, used to dissolve the photoresist, can actually reach the photoresist. On top of the entire wafer a Pt layer is then sputtered. First a few nanometers of titanium is sputtered on the wafer to improve the adhesion to SiO_2 and then 20 nm of Pt. Pt does not have good adhesion with the thermally grown oxide and therefore a titanium adhesion layer is needed.

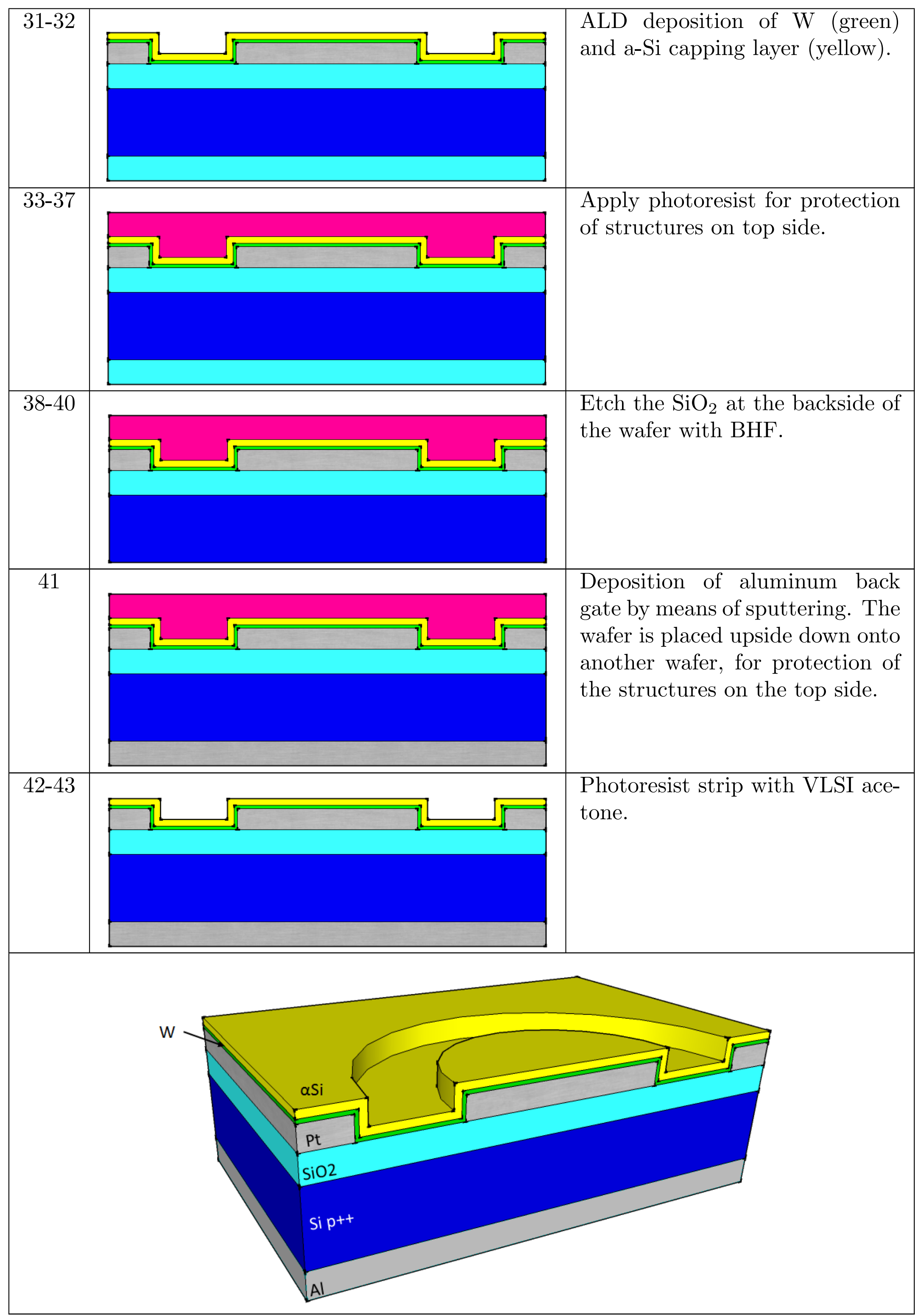
The next step of the process flow is the ALD step. In this project the chosen conducting material is W. The process of W deposition is discussed in chapter 2.3.1. The W is deposited onto the entire wafer. Next, without breaking vacuum 10 nm of a-Si is deposited onto the tungsten film. This a-Si is used to protect the tungsten from oxidation as it is very thin. The thicknesses of the W films deposited during this ranges from 0.6 nm (which is only the seed layer) to 8.5 nm including the seed layer.

After the ALD step only making the backside contact is left. First, the oxide thermally grown on the backside of the wafer (grown in the first step of the process) is stripped. This is done by etching the oxide in buffered HF. To protect the structures on the topside of the wafer, the topside is coffered with a layer of photoresist before etching. After etching the thermal oxide, 100 nm of aluminum is sputtered on the backside of the wafer. The last step of this process is to remove the photoresist on the topside of the substrate. The wafers are then finalized and ready for measurements.

The above described process is shown graphically in table 5.1.

Table 5.1: Simplified graphical overview of the process flow for the test structures for metallic ultra-thin films.

Steps	Graphic wafer status	Explanation of the steps
1		Start with a highly (p++) doped silicon wafer.
2-7		A thermal SiO_2 layer of 100 nm is grown on the front and back side of the substrate.
8-13		1.7 µm of photoresist is applied by means of spin coating.
14-19		Exposure of the photoresist by means of UV light and development of the exposed parts.
20-22		1% HF dip to ensure good lift-off results. The under etch decreases the subsequent Pt step coverage.
23-24		Deposition of titanium adhesion layer and 50 nm Pt electrode.
25-30		Photoresist lift off, removal of the photo resist and the Pt on top of the photoresist. Followed by a cleaning step.



Step		Description
31-32		ALD deposition of W (green) and a-Si capping layer (yellow).
33-37		Apply photoresist for protection of structures on top side.
38-40		Etch the SiO_2 at the backside of the wafer with BHF.
41		Deposition of aluminum back gate by means of sputtering. The wafer is placed upside down onto another wafer, for protection of the structures on the top side.
42-43		Photoresist strip with VLSI acetone.

5.2.2 Insulating ultra-thin films

This section describes the process flow for ultra-thin insulating film test structures. The graphical overview of this process flow is shown in table 5.2. The steps mentioned in this table correspond to the steps of the detailed process flow in appendix C.

The substrate used in this process is a p+ doped silicon wafer. The first seven steps of this process flow are the same as those of the conducting ultra-thin films, meaning until the ALD step.

Next, the film under study is deposited by means of ALD. For this project AlN, is used as the insulating film. The deposition process of this material is described in chapter 2.3.2. On top of this AlN film a capping layer of a-Si is deposited, to protect the ultra-thin film in all the subsequent steps, including its oxidation in air.

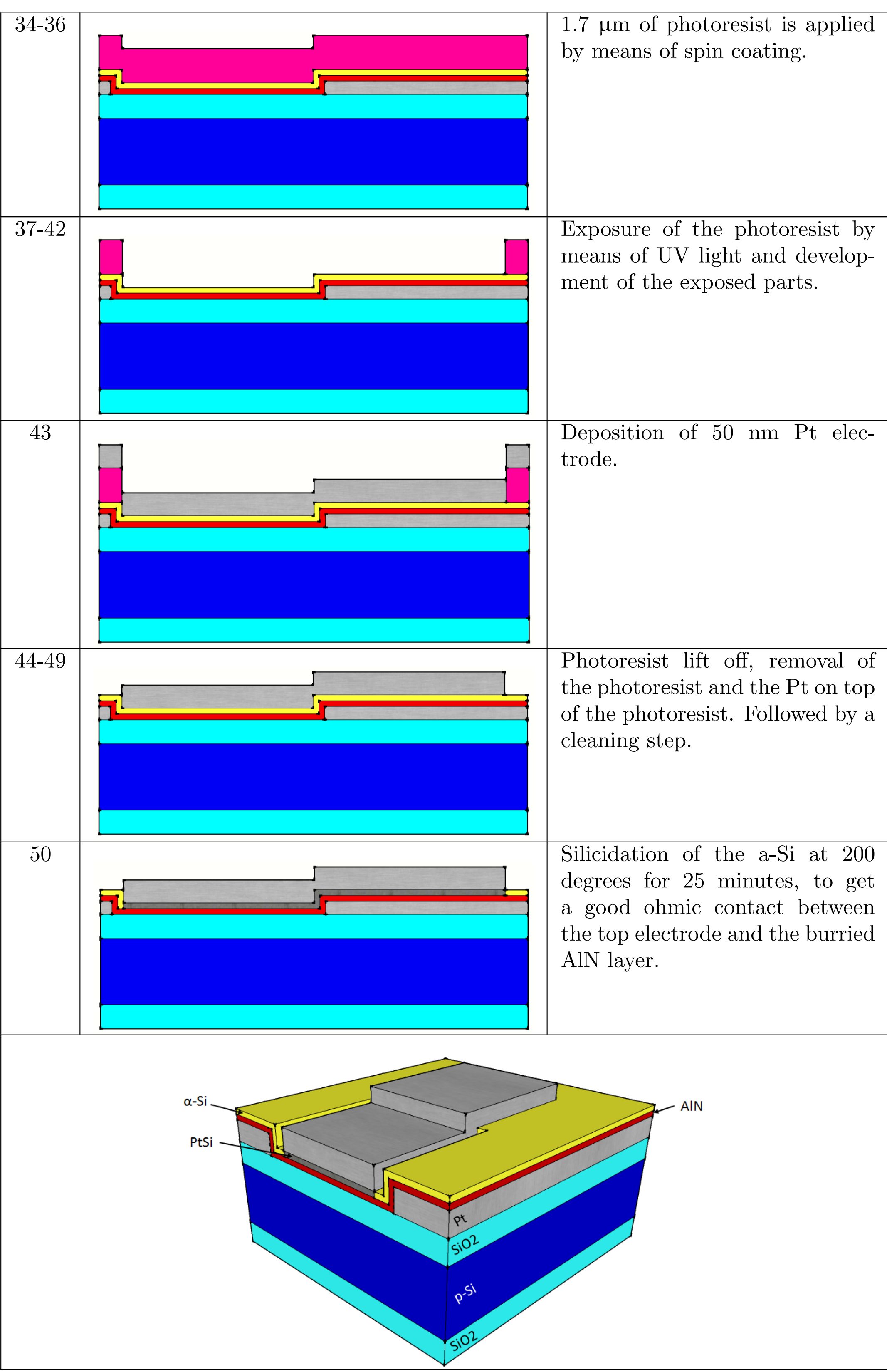
After the ALD step the top Pt electrode is deposited. This electrode is again patterned by lift-off. There is no titanium adhesion layer needed because Pt adheres well to a-Si.

At this point the insulating film is sandwiched between two electrodes but has the highly resistive a-Si on top of the AlN. To lower resistivity of the layer stack, a silicidation step is done. Silicidation is an anneal process that results in a silicon-metal alloy formation. Silicides are known for their lower resistivity, improving the contact resistance. The silicidation is done at a temperature of 200 degrees Celsius for 25 minutes. This results in an ohmic contact to the buried AlN film [19]. The wafers are then finalized and ready for measurements.

The above described process is shown graphically in table 5.2.

Table 5.2: Simplified graphical overview of the process flow for the test structures for insulating ultra-thin films.

Steps	Graphic wafer status	Explanation of the steps
1		Start with p+ doped wafer.
2-7		A thermal SiO_2 layer of 100 nm is grown on the substrate back and front side.
8-13		1.7 µm of photoresist is applied by means of spin coating.
14-19		Exposure of the photoresist by means of UV light and development of the exposed parts.
20-22		1% HF dip to ensure good lift-off results. The under etch decreases the subsequent Pt step coverage.
23-24		Deposition of titanium adhesion layer and 50 nm Pt electrode.
25-30		Photoresist lift off, removal of the photo resist and the Pt on top of the photoresist. Followed by a cleaning step.
31-33		ALD deposition of AlN (red) and a-Si capping layer (yellow).



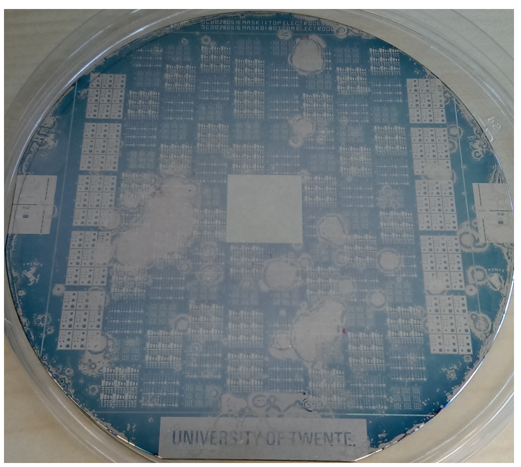
Step	Cross-section	Description
34-36		1.7 μm of photoresist is applied by means of spin coating.
37-42		Exposure of the photoresist by means of UV light and development of the exposed parts.
43		Deposition of 50 nm Pt electrode.
44-49		Photoresist lift off, removal of the photoresist and the Pt on top of the photoresist. Followed by a cleaning step.
50		Silicidation of the a-Si at 200 degrees for 25 minutes, to get a good ohmic contact between the top electrode and the burried AlN layer.

5.3 Findings

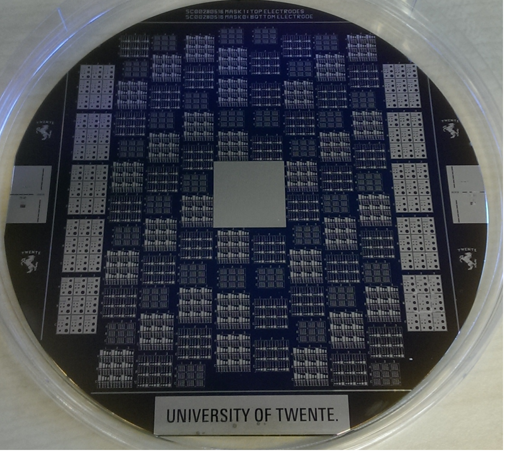
Using the developed process flow, the designed structures are made, in the MESA+ nanolab of the University of Twente. During the fabrication steps some effects are observed, which will be discussed below.

5.3.1 Adhesion of AlN to platinum

In the process of making the test structures for insulating ultra-thin films, the AlN film is originally deposited onto the Pt electrodes. On top of the AlN the a-Si is further deposited. In the post-ALD step it is observed that the films started to peel off from the substrate, as seen in figure 5.2a. It was assumed that the adhesion between the AlN film and the Pt electrodes is poor. This assumption is based on the observation that there is no "peeling off" for the reference wafer with no AlN layer present. This means that the adhesion of a-Si to Pt is good. Therefore the decision is made to slightly adjust the process. Before the AlN film is deposited by ALD, a thin film of a-Si is deposited. On top of this a-Si the AlN film is deposited and this AlN is again protected by an a-Si capping layer. The added a-Si film now acts as an adhesion layer, having good adhesion to the Pt underneath and to the AlN op top. By adding this step to the process the problem of "peeling off" films has been solved (figure 5.2b).



(a) Photograph of the "peeling off" observed during fabrication.



(b) Photograph of a wafer with the 2nd a-Si layer, solving the "peeling off" problem.

Figure 5.2: Photographs of two wafers, with and without the "peeling off" problem.

5.3.2 Silicidation of amorphous silicon during ALD

In the process of making the test structures for insulating thin films silicidation of the a-Si films (i.e. a reaction between a-Si and Pt) is done at a temperature of 200 degrees Celsius for 25 minutes. This results in an ohmic contact to the buried AlN film [19].

The depositions of AlN film and the a-Si capping layer are done at a temperature of 350 degrees Celsius and take more than half an hour in total. There is already an a-Si film present on the substrate before the AlN is deposited. This a-Si film might react with underlying Pt during the deposition of the AlN film and the subsequent capping layer. The temperature is enough to enable silicidation, as well as the time duration. This phenomena is further discussed in chapter 6.3.1, where it is used to explain the measurement results and draw some conclusions.

Chapter 6

Measurements

Several measurements have been done on the fabricated wafers, the measurement results are analyzed and conclusions are drawn. In this chapter the measurement setup is explained, the results are shown and are analyzed. Furthermore the results are compared with in-situ SE measurements, showing good agreement.

6.1 Measurement setup

The wafers are measured using one of the probe stations available in the lab of the Semiconductor Components group. Figure 6.1 shows an image of this probe station. The measurements are conducted by using two probes to force a voltage to the contacts and measure the current. In these measurements the current is limited to 100 mA, this is the compliance of the probe station. The test structures for the metallic ultra-thin films are probed by puncturing the a-Si capping layer. This can easily be done because the capping layer is only 10 nm. Probing the electrodes for insulating films can be more challenging. The top electrode for the test structures can be easily reached because there is no film on top of this electrode. To reach the bottom electrode the a-Si/AlN/a-Si films stack has to be punctured. This can be done as long as the entire film stack is not too thick. During this project film stacks with a thickness of $\approx$ 30 nm and less could be measured successfully. For the film stack including a 35 nm AlN film the "peeling off" problems occurred (discussed in section 5.3.1). The film stack just "peeled off" the bottom electrode while probing, making it easy to reach the bottom electrode.

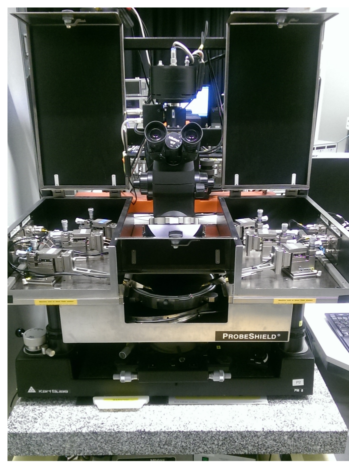


Figure 6.1: Probe station used for measurements during this project.

6.2 Metallic films

During this project 6 wafers with a W ultra-thin film and a reference wafer were fabricated. W films with a thickness of approximately 0.6 nm (this is only the seed layer, as discussed in chapter 2.3.1), 0.9 nm, 1.3 nm, 2.2 nm, 2.9 nm and 8.5 nm are deposited and measured. The first wafer made is the reference wafer, and does not contain any W. After that wafers with a continuous and a discontinuous film are made. The thicknesses are 8.5 nm and 0.6 nm for a continuous and discontinuous film, respectively. This information resulted from the previous studies of M. Yang. More thicknesses were further obtained for a comparison. All these wafers were measured. The results are discussed on the next pages and conclusions are drawn. To enable comparison, the measurements were preformed on the same CTLM structures at the same positions on the wafer. The legend in the graphs shows the gap spacings (S) of the CTLM structures.

6.2.1 I-V characteristics

This paragraph shows the I-V characteristics of the wafers made during this project. Using the method previously established conclusions are drawn.

Reference wafer

A reference wafer is made without a W film, to verify that the deposited capping layer of a-Si is highly resistive. The measurement results can be seen in figure 6.2. The measurement results indicate non-ohmic conduction of the a-Si capping layer, as expected. The capping layer does exceed 0.05 µA. Only the structures with a relatively small gap spacing conduct more current at higher applied voltages, at these voltages the non-ohmic conduction mechanisms are enhanced.

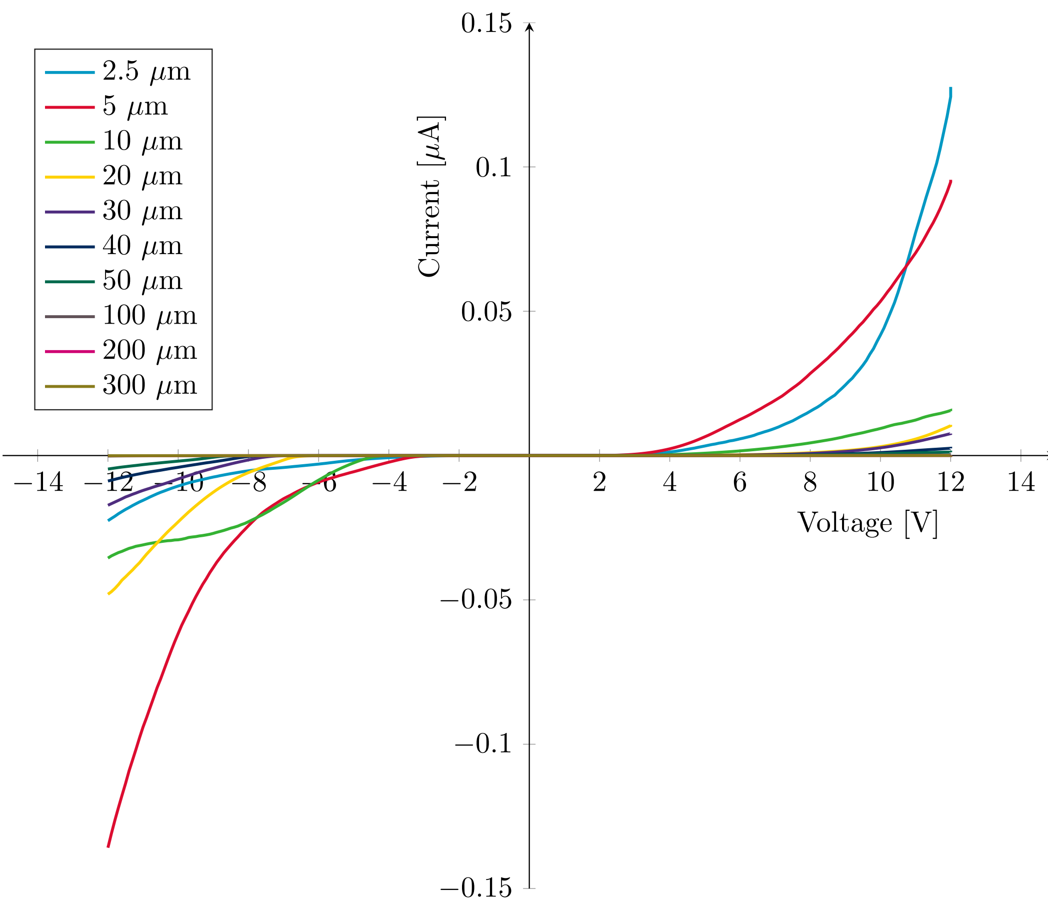


Figure 6.2: Measurements of CTLM structures on the reference wafer without ALD W film.

0,6 nm W film

For further measurements, 0.6 nm of W is formed on a wafer, which is only the seed layer for growing W. This film is expected to be discontinuous, figure 6.3 shows that the measurement results support this expectation. The current has increased compared to the reference wafer, but is still very low. In the measurement results the non-ohmic conduction is clearly visible. This wafer represents a discontinuous film.

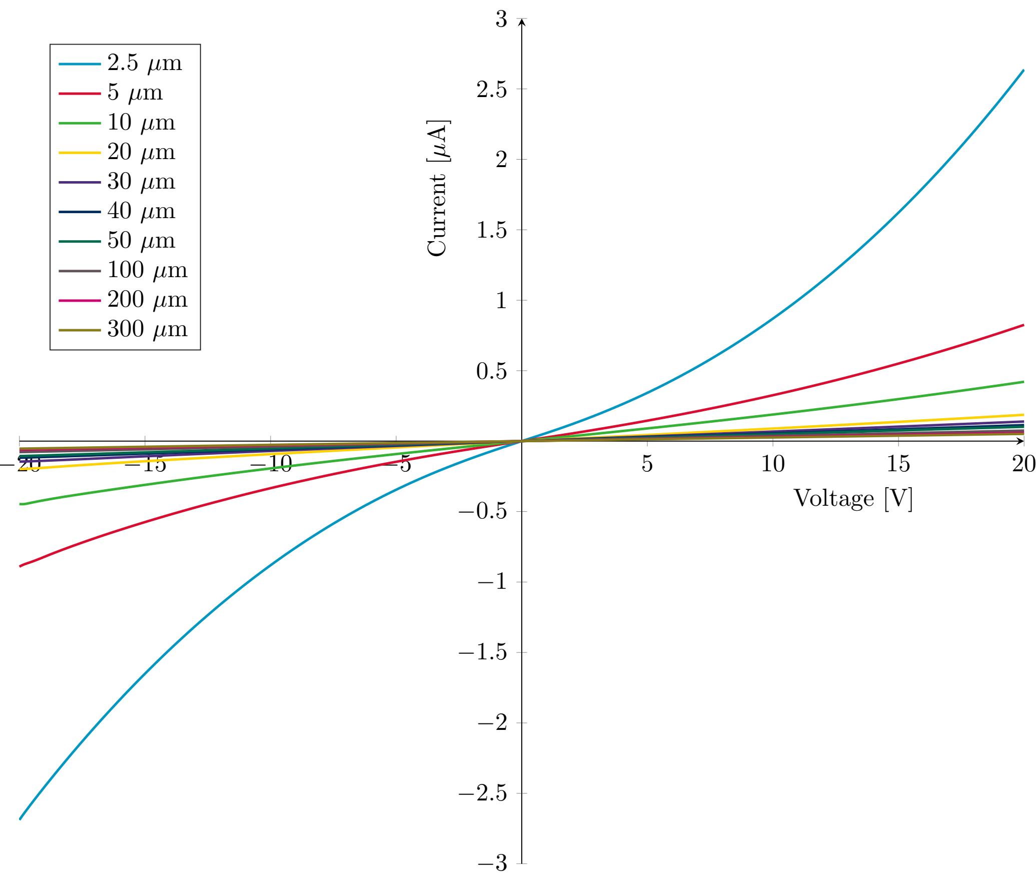


Figure 6.3: Measurements of CTLM structures on the wafer with 0.6 nm thick W film.

8.5 nm W film

For the next step a W film of 8.5 nm was deposited. From the previous studies of M. Yang it is expected to be continuous at this thickness. Therefore the measurement results of this film can be used as a reference to a continuous film. The measurement results are shown in figure 6.4. The conduction mechanism is clearly highly ohmic, therefore this film is indeed continuous as expected.

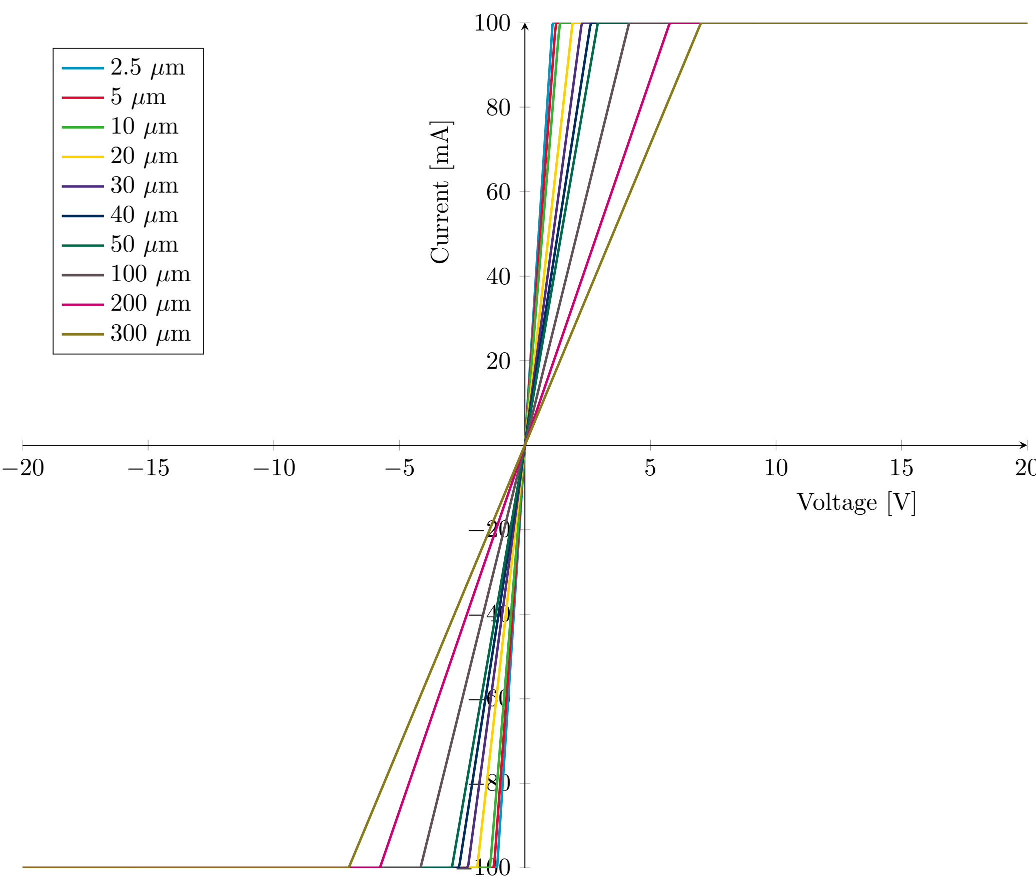


Figure 6.4: Measurements of CTLM structures on the wafer with 8.5 nm thick W film.

Now the I-V behavior of the continuous and discontinuous films is confirmed. Two new wafers with a thickness of 0.9 nm and 2.9 nm are made, to verify if the closure point of the film can be found.

0,9 nm W film

Figure 6.5 shows the measurement results of the 0.9 nm W film. The current is increased significantly compared to the previous film of 0.6 nm. This is as expected, due to the further formation of the resistance network. It is also quite clear that the non-ohmic conduction is still dominant, indicating a still discontinuous film.

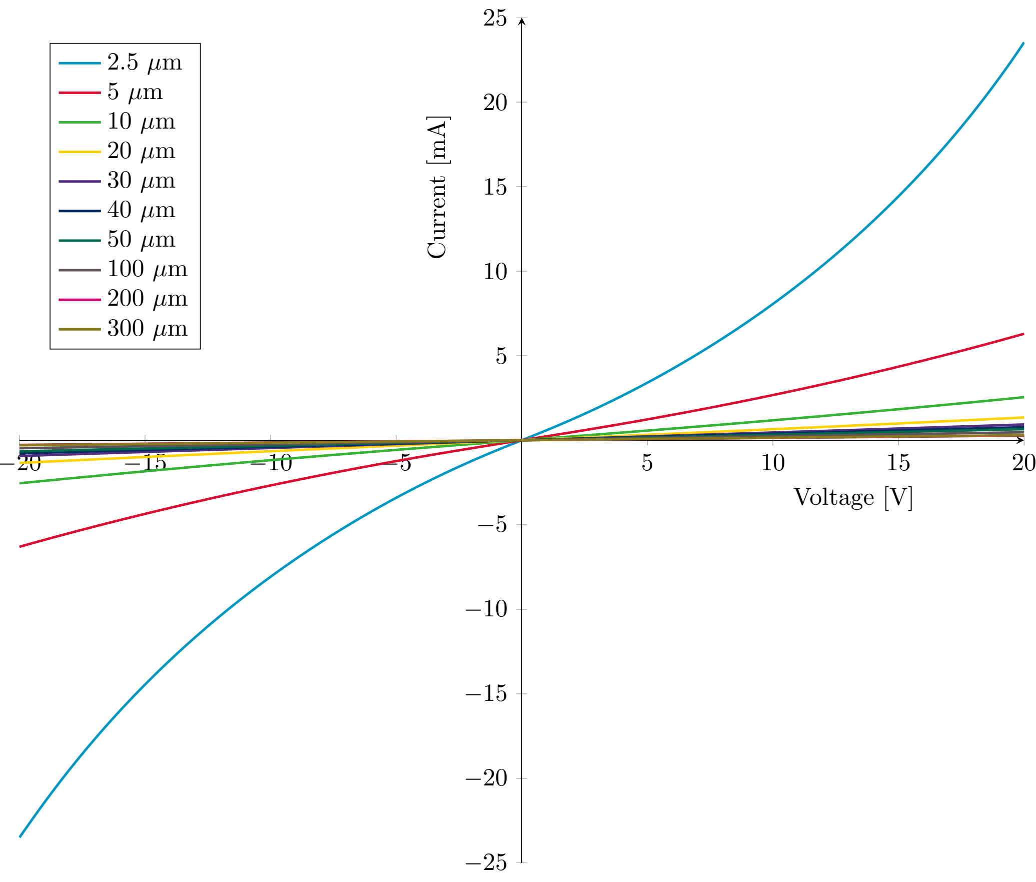


Figure 6.5: Measurements of CTLM structures on the wafer with 0.9 nm thick W film.

2.9 nm W film

In figure 6.6 the measurement results of the 2.9 nm W film are shown. Compared to the 8.5 nm film the resistance is increased, which results in a lower current (the I-V characteristics are less steep). Ohmic conduction is still dominant in this film, indicating its continuity.

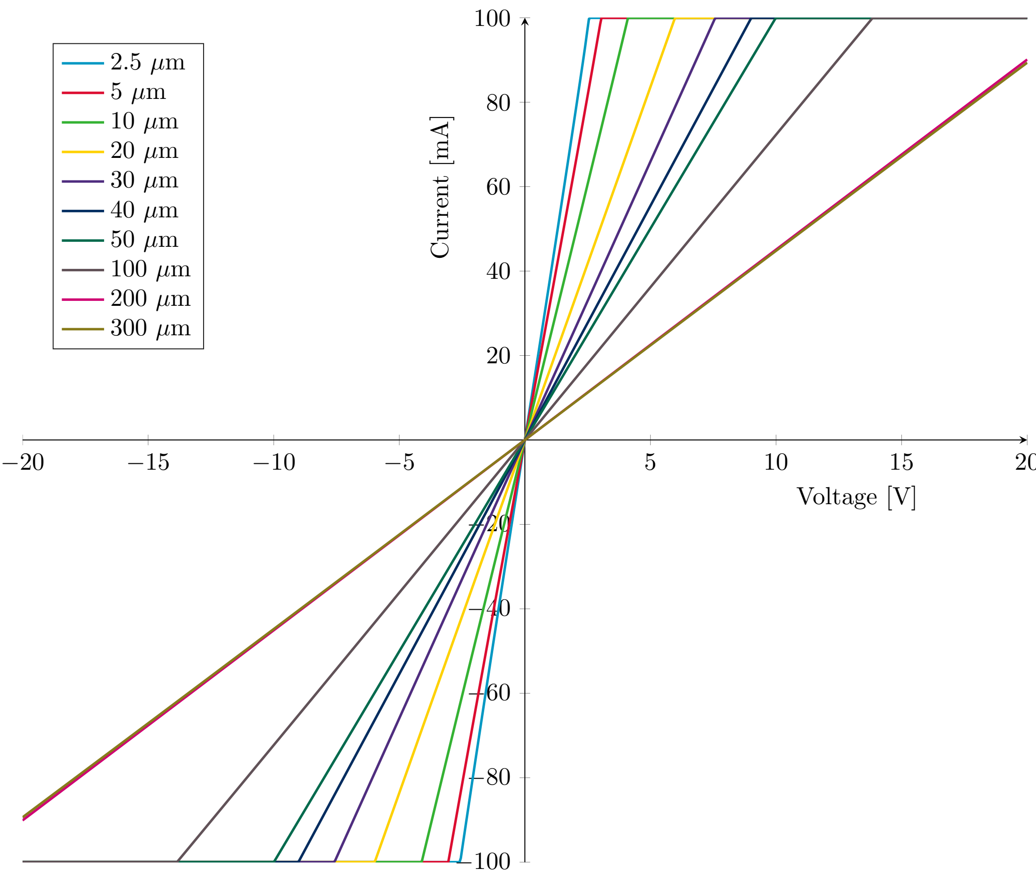


Figure 6.6: Measurements of CTLM structures on the wafer with 2.9 nm W film.

It can be concluded that the W films become continuous between 0.9 nm and 2.9 nm. Therefore two new wafers were made containing films with a thickness of 1.3 nm and 2.2 nm.

1.3 nm W film

The measurements of the 1.3 nm W film are shown in figure 6.7. The current has increased compared to the 0.9 nm film. The I-V curves show a slight non-linearity pointing to the vanishing of non-ohmic conduction. This indicates that the film is in the transition regime from discontinuous to continuous. That would explain the prevailing ohmic conduction in these results, because many islands of the film are now interconnected.

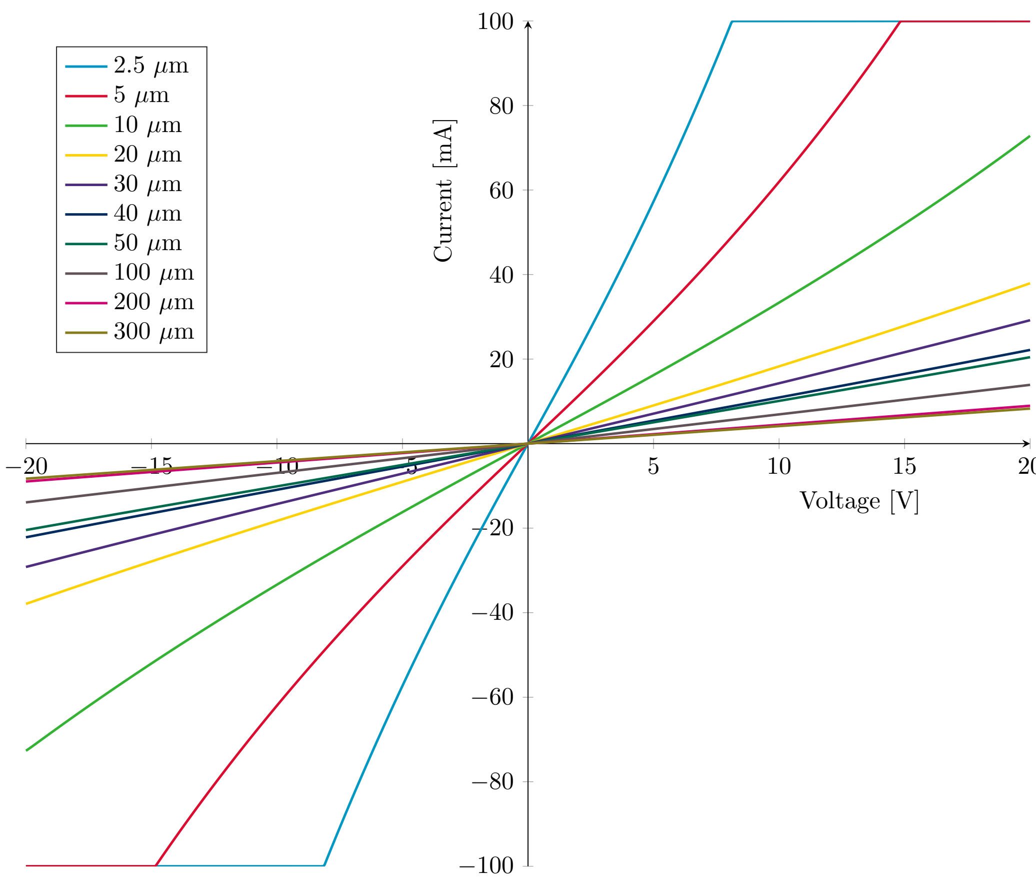


Figure 6.7: Measurements of CTLM structures on the wafer with 1.3 nm thick W film.

2.2 nm W film

Figure 6.8 shows the results of the 2.2 nm film. The I-V curves indicate an ohmic conduction, pointing to a continuous film.

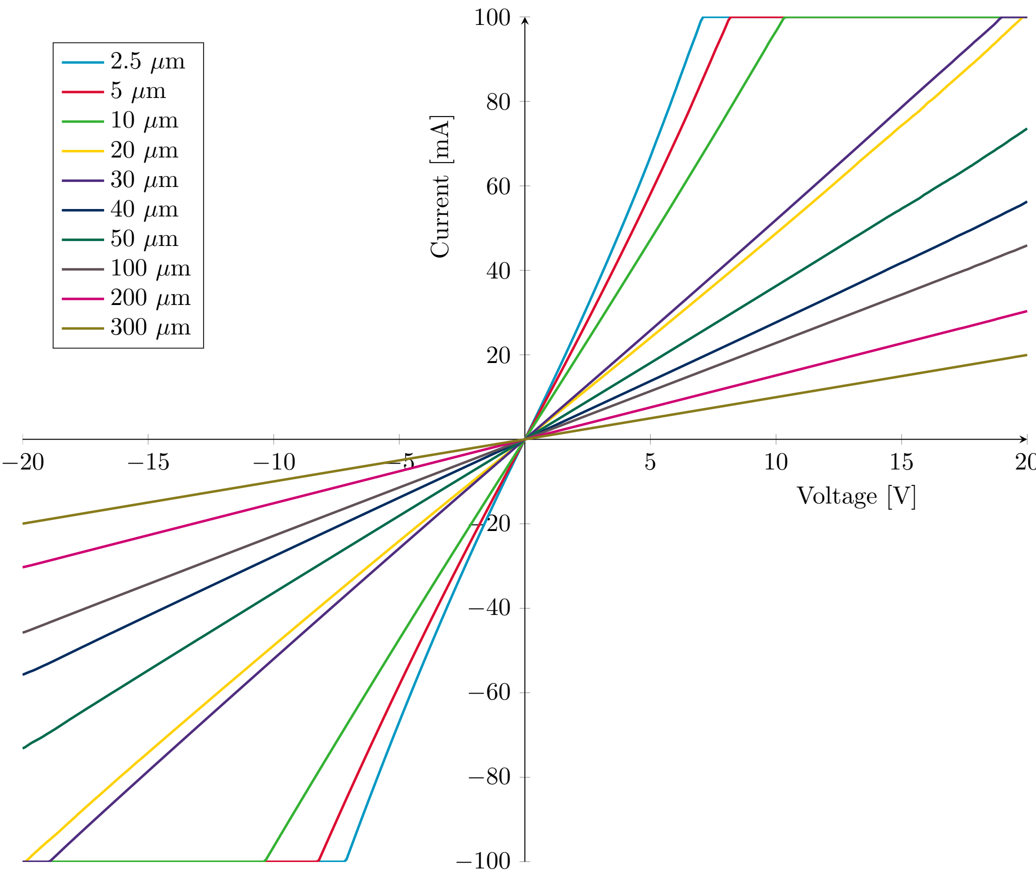


Figure 6.8: Measurements of CTLM structures on the wafer with 2.2 nm thick W film.

By comparing the I-V characteristics of all the wafers measured, the closure point of the W films can be expected between 1.3 and 2.2 nm. For the 1.3 nm film, non-ohmic conduction mechanisms can still be observed. For the 2.2 nm film, the conduction mechanisms has become purely ohmic. To verify this preliminary conclusion about the closure point, the $Rt^2(t)$ curves are further analyzed.

6.2.2 Rt^2 vs thickness

The second method to determine the continuity of an ultra-thin film is the method of Maroof and Evans, as mentioned in chapter 3. The resistance of the films is calculated and multiplied by the square of the thickness. These results are plotted against the thickness, showing a graph with a minimum. This minimum indicates the onset of a continuous film.

The resistance of the film is calculated by fitting a line trough the I-V measurements; the slope indicates the resistance of the film. For the calculation of film resistivity the CTLM structures are used. To account for the non-linear structures, a correction factor c has to be applied [16], given by:

$$c = \frac{R_1}{s} ln(\frac{R_1 + s}{R_1}) \tag{6.1}$$

In which R_1 is the radius of the inner circle of the CTLM structure and s is the distance between the inner and outer circle of the CTLM structure. The linear resistance is calculated by formula (6.2), and consists of the resistance of the W film and two times the contact resistance between the electrodes and the film (formula (6.3)) of the probes with the electrodes. R_W is the resistance of the W film and can be calculated by formula (6.4).

$$R_L = \frac{R_m}{c} \tag{6.2}$$

$$R_L = R_W + 2R_c \tag{6.3}$$

$$R_W = \frac{R_{sh}}{2\pi R_1} s \tag{6.4}$$

Plotting the R_L versus the gap spacings should result in a linear fit. The slope determines the sheet resistance (R_{sh}) and the intercept with the y axis gives two times the contact resistance. Such a plot is shown in figure 6.9. From the slope, the sheet resistance can be extracted using formula (6.5) and using the sheet resistance the resistivity of the W film can be calculated using formula (6.6) where t is the thickness of the film.

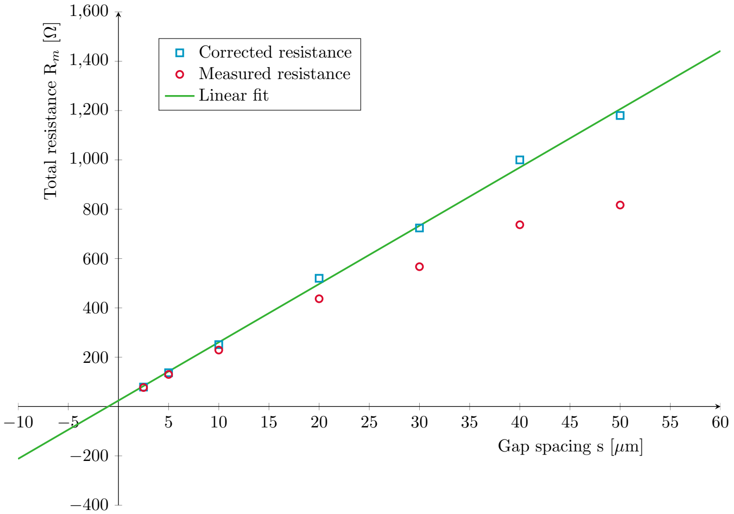
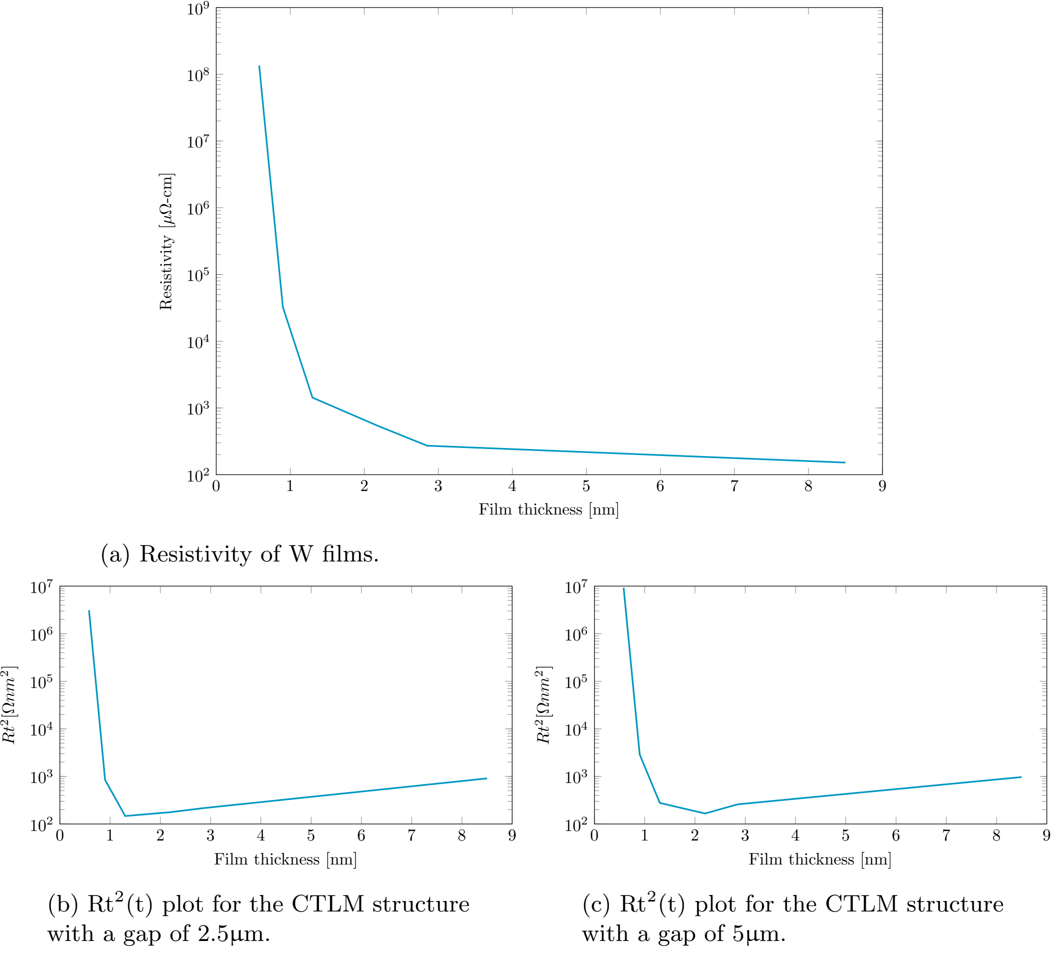


Figure 6.9: Linear fit obtained after correction of CTLM to linear TLM.

$$Slope = \frac{R_{sh}}{2\pi R_1} \tag{6.5}$$

$$\rho = \frac{R_{sh}}{t} \tag{6.6}$$

Figure 6.10 shows the $Rt^2(t)$ plot results and the calculated resistivity of the W film for various thicknesses. The two $Rt^2(t)$ plots in figure 6.10b and 6.10c indicate similar minimum values, between 1.3 nm and 2.2 nm. The resistivity plot (figure 6.10a) shows that with increasing film thickness the resistivity of the film decreases, as expected. This confirms the I-V characteristics of the deposited films. Concluding, the film is expected to become continuous between 1.3 nm and 2.2 nm.



(a) Resistivity of W films.

(b) $Rt^2(t)$ plot for the CTLM structure with a gap of 2.5µm.

(c) $Rt^2(t)$ plot for the CTLM structure with a gap of 5µm.

Figure 6.10: Resistivity of the W film and $Rt^2(t)$ plots of two CTLM structures.

6.2.3 Conclusion

Both methods indicate that ALD W film becomes continuous between 1.3 nm and 2.2 nm. This is confirmed by the change in conduction mechanism and the minimum in the $Rt^2(t)$ plot. For the 1.3 nm film, non-ohmic conduction is still present, indicating that electrons hop or tunnel from one island to another. This corresponds to a not fully closed film. For the 2.2 nm film, the conduction mechanism is ohmic, indicating a continuous film.

6.3 Insulating films

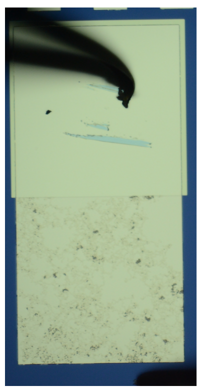
During this project 4 wafers with an AlN ultra-thin film, with thicknesses of 4, 11, 15 and 35 nm, and a reference wafer were measured. The reference wafer does not contain an AlN film. A wafer with an AlN film of 35 nm is fabricated to ensure a continuous film, to verify if the idea of the test structures works. The measurement results are discussed in this chapter. For analysis the double square structures are used. While measuring the wafers some findings have been obtained which are discussed below.

6.3.1 Findings during the measurements

Breakdown of the films

While measuring the AlN film of 11 nm, 15 nm and 35 nm, cracking of the films is observed. This cracking of the films is probably due to the piezoelectric nature of the layers. With increasing electric field applied to AlN, the film starts to shrink or expand, which probably causes the physical damage of the film. This is shown in figure 6.11, namely the appeared black spots are attributed to the film damage. Electrically, after the appearance of the spots the I-V characteristics of the film are changed irreversibly. The damage can be avoided by first finding the voltage at which the film is damaged for one of the structures, and then not exceeding those voltages for the rest of the measurements.

(a) Before voltage stress of the AlN film.



(b) After voltage stress of the AlN film.

Figure 6.11: Images before and after applying a voltage stress to the film, the black spots attributed to damage are clearly visible.

Measurements before and after silicidation

The bottom layer of a-Si might become silicidated by reacting with underlying Pt during the deposition of both the AlN film and the capping layer, as mentioned in chapter 5.3.2. During the measurements it was found that the I-V characteristics of the 4 nm films were ohmic even before the final silicidation step. This ohmic behavior was unexpected, because the last silicidation (i.e. the reaction between the top a-Si/Pt stack) step has not been done yet; the a-Si should still behave as an insulating material as shown for the reference wafer for the W films. The only explanation for the ohmic conduction is that the AlN film is indeed discontinuous and therefore silicidation of the top Pt/a-Si stack could occur by diffusion of Pt from the layers below the AlN. As indicated in chapter 5.3.2, the temperature and duration of the deposition of the a-Si could allow for its in-situ silicidation. When the AlN film is discontinuous, there are places where the bottom silicide is in contact with the top a-Si film. At these places silicidation of the top a-Si film can further occur during the deposition of the 2nd a-Si layer. This phenomena can be used as an extra tool to determine the continuity

of the ultra-thin films. The wafers can be measured before and after silicidation; when the results are ohmic even before the silicidation step the film is expected to be discontinuous. After the silicidation step, the ohmic behavior increases, because not all a-Si might have become in-situ silicidated during the deposition.

6.3.2 I-V characteristics

The 4 wafers with the different thicknesses of the AlN films are measured. To determine the continuity, the I-V characteristics will be analyzed. First, the reference wafer has been made and measured. Then, a 35 nm film is made and measured, which is expected to be continuous and can be used as a reference for a continuous film. After that, the other wafers are made and measured to further clarify the closure point.

Reference wafer

Figure 6.12 shows the measurement results of the reference wafer, exhibiting a clear ohmic conduction. This means that the silicidation process was successful and the a-Si was fully silicidated. This also shows that if the AlN film was discontinuous ohmic I-V characteristics would be expected.

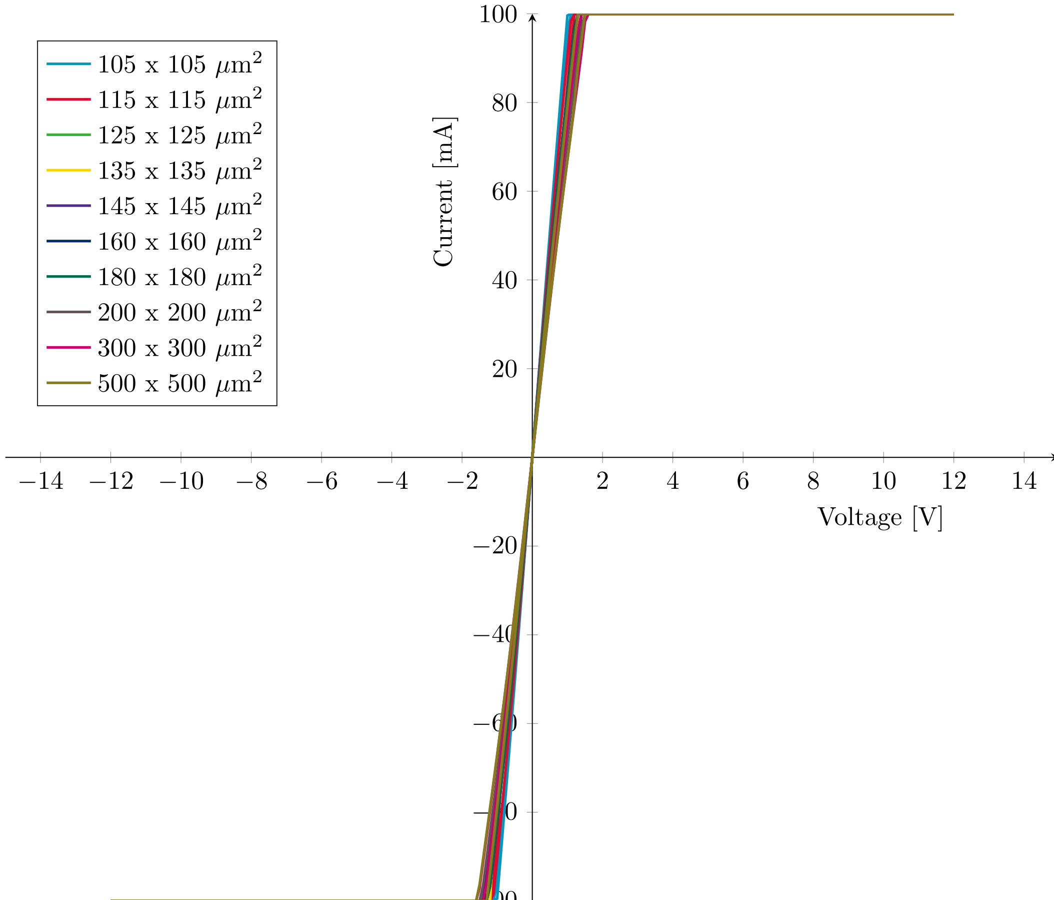


Figure 6.12: Measurements of double square structures on the reference wafer for AlN films.

35 nm AlN film

A wafer with a 35 nm AlN film is made and measured. The results (figure 6.13) show a clear non-ohmic I-V characteristic. The bigger the effective measurement area the higher the current, caused by the lower resistance for bigger contact areas. The results clearly indicate that the AlN film is continuous, as expected. Therefore the measurement results of this film can be used as a reference to a continuous film.

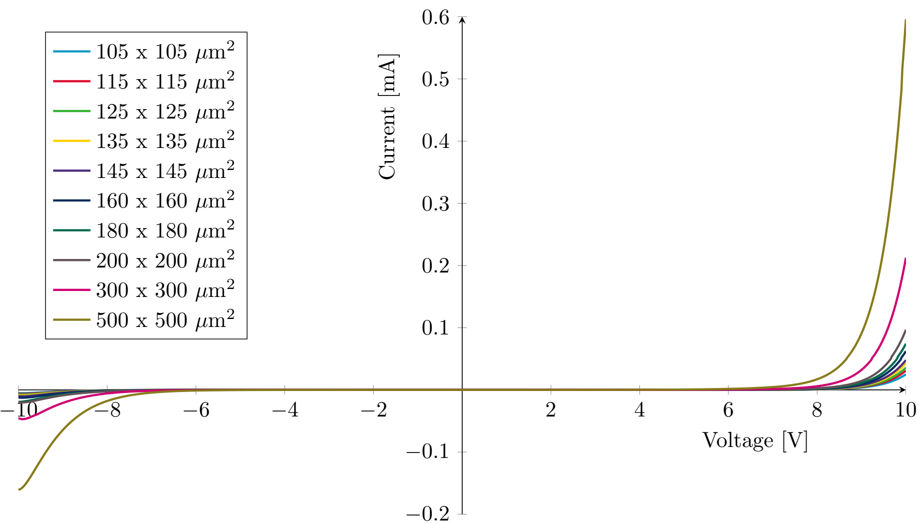


Figure 6.13: Measurements of double square structures on the wafer with 35 nm of AlN.

The current density in these structures has been calculated (figure 6.14). Current density is defined as the electrical current per unit area. The results show that the whole effective area of the structures was used, the current scales with the effective area.

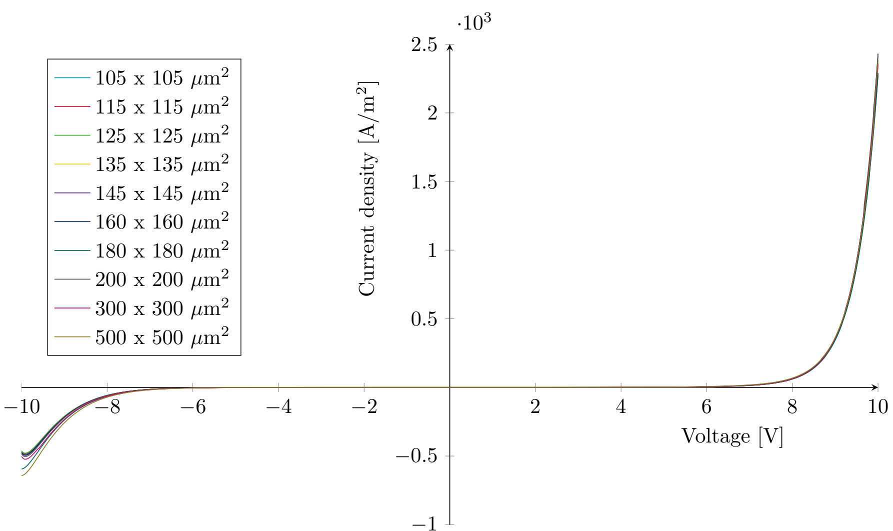


Figure 6.14: Current density in the structures of the 35 nm film.

15 nm AlN film

Further, a 15 nm AlN was examined for its continuity. The results are shown in figure 6.15. Several observations can be made. First of all, the measurements are done from -1.5 V to 1.5 V. This is due to the previous explained cracking of the AlN films. For the 15 nm AlN the films are damaged at low voltages and therefore the voltages applied to the film could not exceed the -1.5 V/1.5 V range. The noise on the measurement data is due to the fact that the film is probably already physically changing at the -1.3 V/1.3 V range, even though cracking of the films is not observed during these measurements. The last and most important observation is the conduction mechanism is still non-ohmic. This indicates that the AlN film is still continuous at 15 nm.

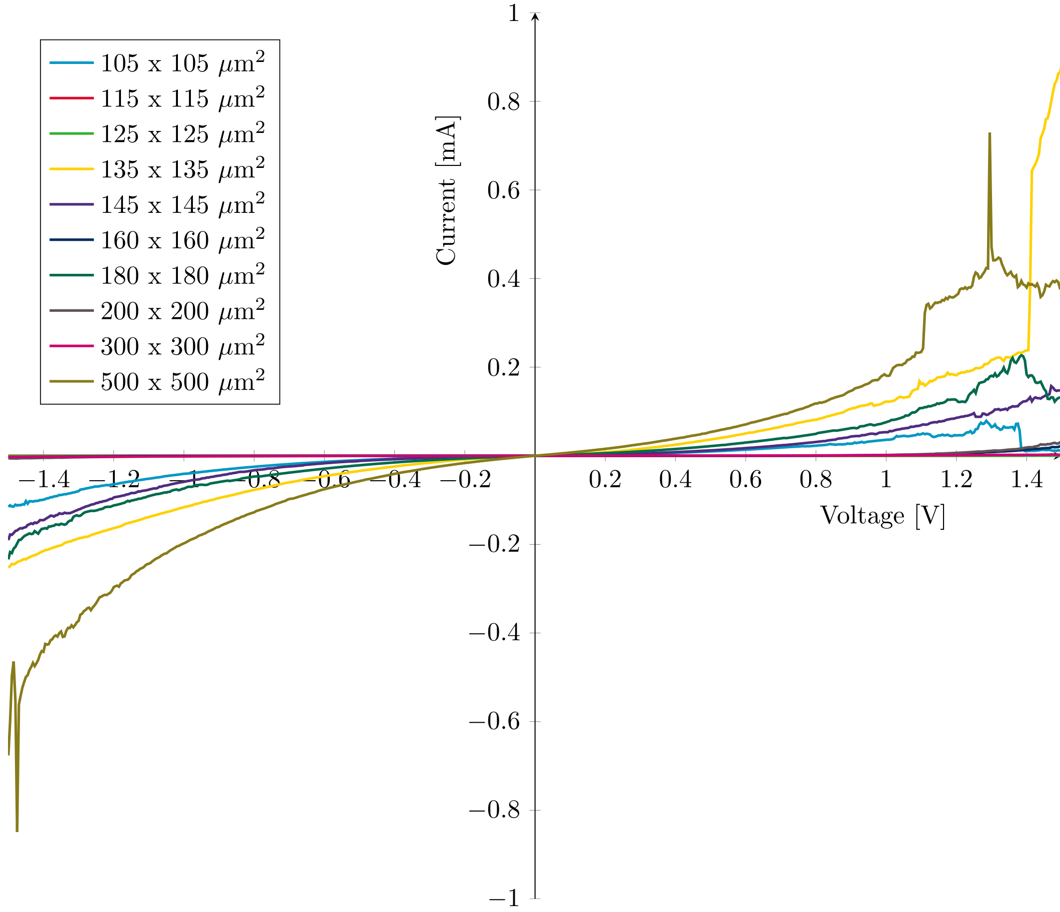


Figure 6.15: Measurements of double square structures on the wafer with 15 nm of AlN.

4 nm AlN film

After testing the 15 nm film the decision was made to fabricate a wafer with an AlN film of approximately 4 nm, to verify if the film is continuous at this thickness. The results contribute to finding the closure point of the AlN film. This wafer was also measured before annealing the wafer, the results are shown in figure 6.16. The measurements show ohmic behavior even before annealing. This is unexpected but can be explained by the previously discussed silicidation of the 2nd a-Si layer during its deposition, indicating that the 4 nm AlN film is discontinuous.

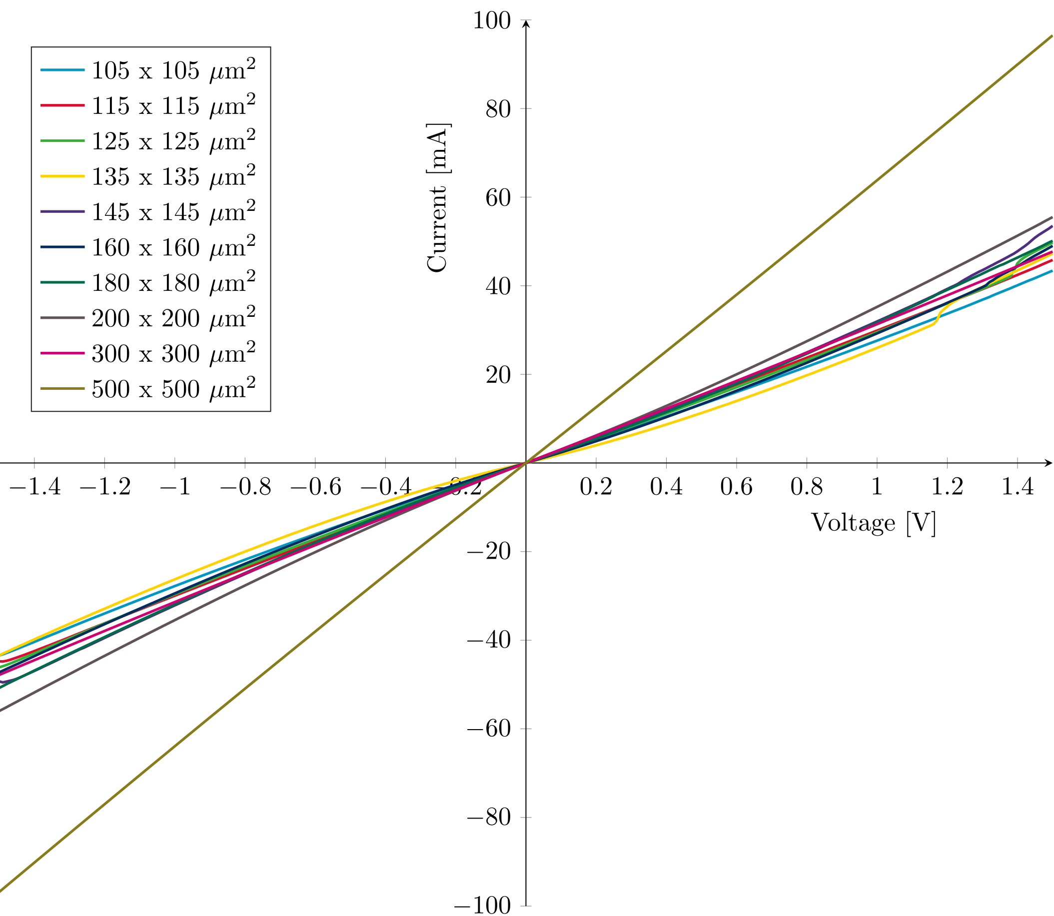


Figure 6.16: Measurements of double square structures on the wafer with 4 nm of AlN before annealing.

The wafer is also measured after final annealing, at 200 degrees for 25 minutes. A decrease of the resistance may be expected as well as an improved linearity of the I-V curves. When the I-V's after silicidation are more linear than before that would indicate that not all of the a-Si was silicidated during the deposition. Figure 6.17 shows the measurement results after annealing, indeed indicating a better ohmic conduction and a lower resistance. The I-V behavior before and after annealing confirms that the AlN film is discontinuous at 4 nm.

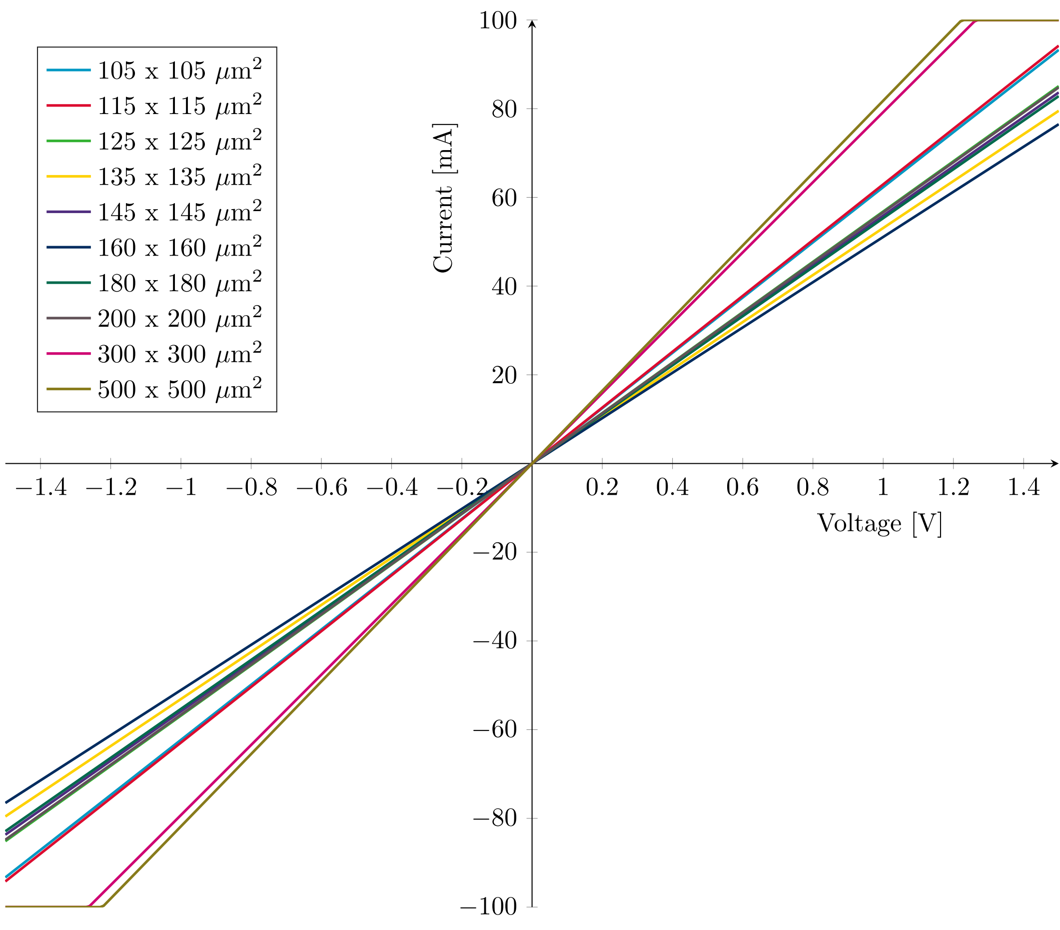


Figure 6.17: Measurements of double square structures on the wafer with 4 nm of AlN after annealing.

11 nm AlN film

The last wafer with AlN made during this project is a wafer containing 11 nm of AlN. Again, this wafer is measured before and after annealing. Figure 6.18 shows the measurement results before annealing. The measurements are done from -1.5 V to 1.5 V, because of the damage of the AlN film when higher voltages are applied. As can be seen the conduction mechanism is non-ohmic. The top a-Si layer is not yet silicidated and the conduction through this a-Si dominates the I-V characteristics. The current is in the same range as for the reference wafer of the W films, where conduction through the a-Si film is measured as well (figure 6.2). These two situations are of course not completely comparable but this indicates that the 2nd a-Si film is not yet silicidated. This may indicate that the AlN film is already closed or continuous at this thickness.

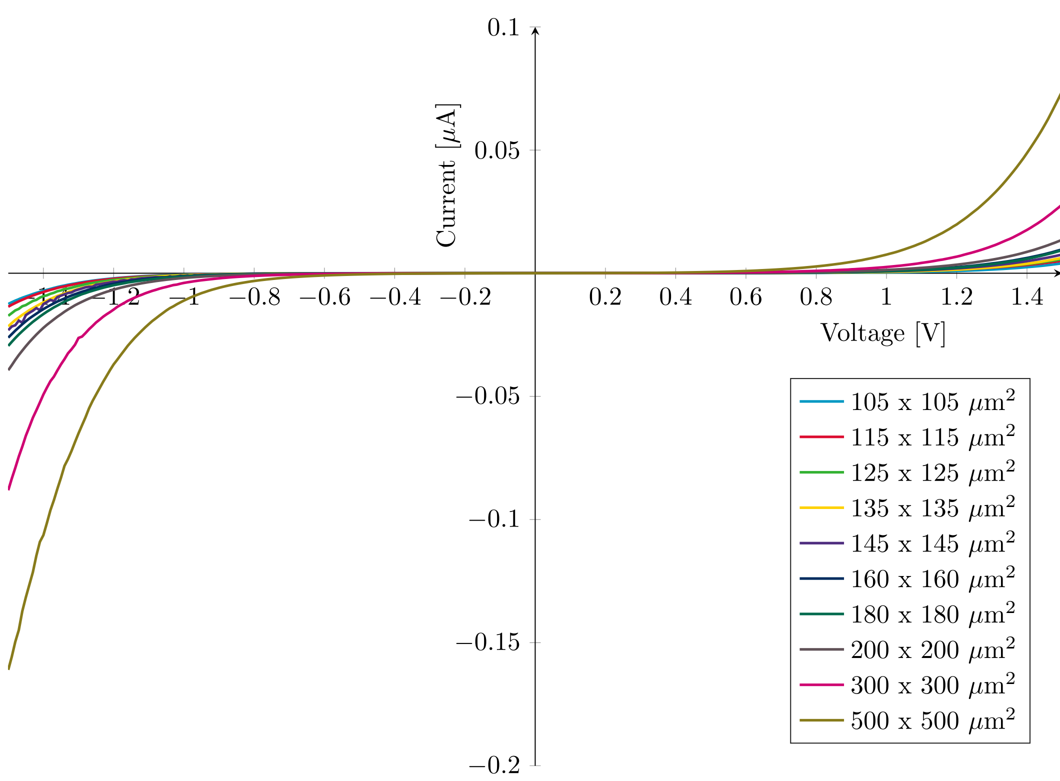


Figure 6.18: Measurements of double square structures on the wafer with 11 nm of AlN before annealing.

Figure 6.19 shows the measurement results for the 11 nm AlN film after final annealing. Unfortunately something went wrong during the annealing step in the cleanroom. Due to the technical difficulties the wafer is annealed for one and a half hour instead of 25 minutes. When the wafer is annealed for such a long time, one can expect a diffusion of Pt to occur through the AlN layer. This diffusion can take place via defects in the AlN film or along the grain boundaries (interface where the individual grains of the film meet each other). This diffusion can explain the observed ohmic conduction after the over-annealing step.

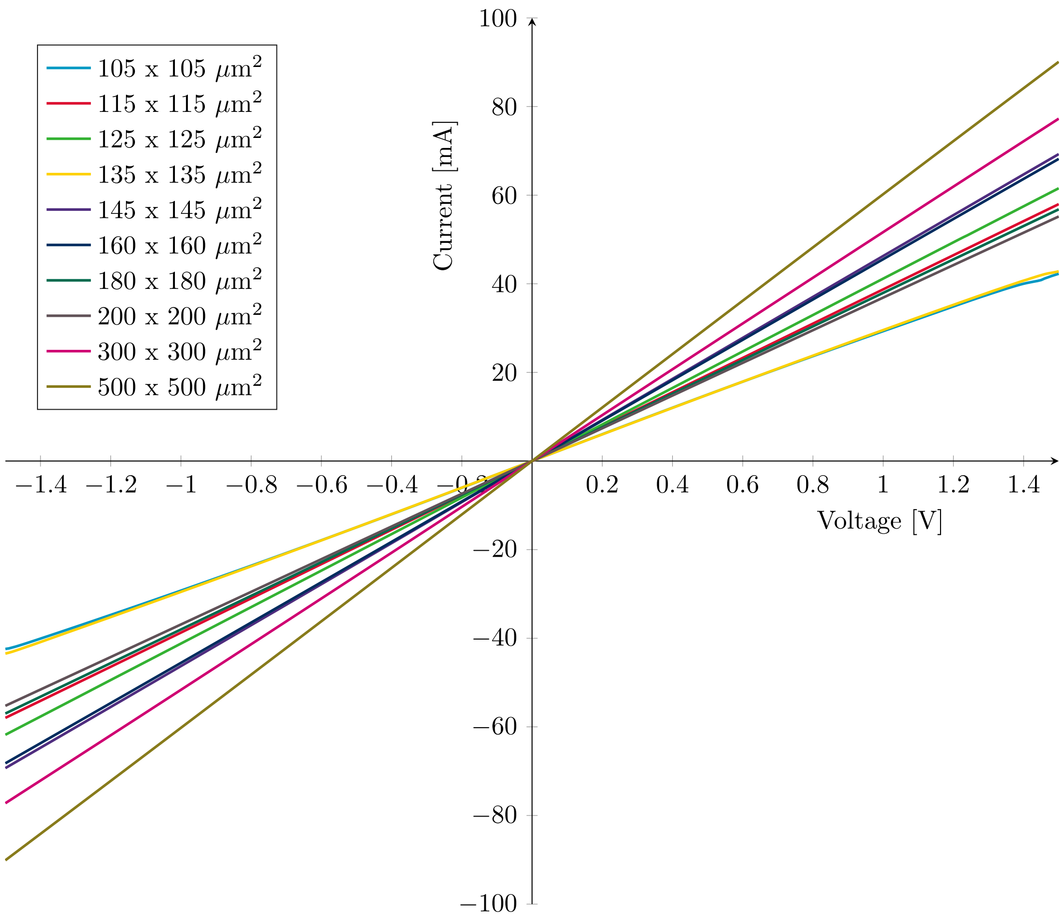


Figure 6.19: Measurements of double square structures on wafer with 11 nm of AlN after annealing.

6.3.3 Conclusion

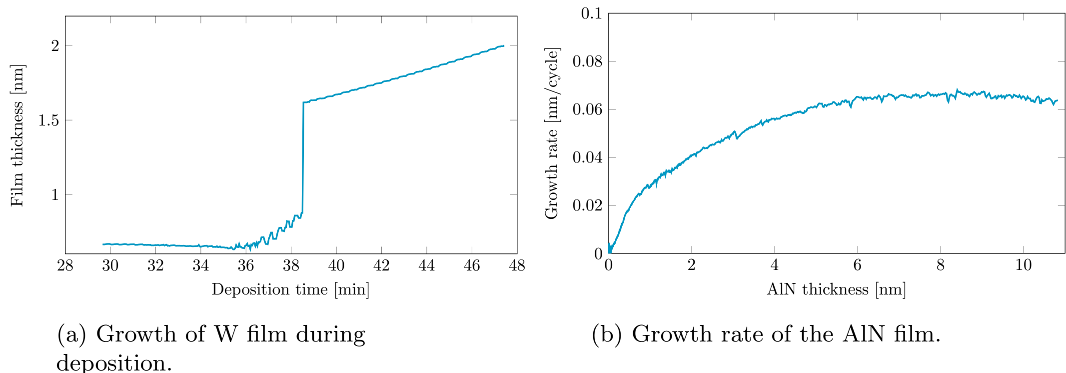
From the previous measurement results the conclusion can be drawn that the AlN film becomes continuous between 4 and 11 nm. The conduction mechanism at 4 nm is ohmic, before and after annealing. The conduction mechanism at 11 nm is non-ohmic before annealing and after over-annealing it becomes ohmic. The non-ohmic conduction before annealing indicates that the film probably is continuous, therefore the top a-Si film is not silicidated during its deposition. The appearance of ohmic conduction after over-annealing can be explained by diffusion through the AlN layer.

6.4 Comparison between electrical and SE measurements

The conclusions drawn from electrical measurements can be supported by the SE measurements done during deposition of the films, shown in figure 6.20

For the W films, the in-situ thickness measurements are shown in figure 6.20a. At a certain time during deposition the SE signal suddenly sharply increases. This increase is not truly happening with the thickness of the film. The model used to calculate the thickness of the film becomes no longer correct at this point. It is speculated that the incorrectness of the SE model occurs due to the transition from discontinuous to continuous film coverage of the surface. Interpreted in terms of film thickness, this sudden SE signal increase falls in the range of 1 and 1.6 nm. In other words the W becomes continuous between 1 and 1.6 nm according to the SE measurements. This confirms the earlier drawn conclusion based on the electrical measurements.

The growth rate of the AlN film is in-situ measured and a conclusion can be drawn from this data (figure 6.20b). The growth rate saturates at a thickness of approximately 8 nm. The growth rate saturates when the growth is no longer influenced by the substrate. Therefore, the constant value of the growth rate may indicate that the film is continuous around 8 nm, which falls in the same thickness range based on the conclusion drawn from the electrical measurements. Therefore it is proposed that the closure of the AlN films occurs between 4 nm and 11 nm.



(a) Growth of W film during deposition.

(b) Growth rate of the AlN film.

Figure 6.20: SE measurements of W and AlN films, measured during deposition.

Chapter 7

Conclusions

Ultra-thin films can be used for many interesting new applications in the field of micro-electronics. These various applications require either continuous or discontinuous, conducting or insulating ultra-thin films. The goal of this project is to design a methodology and corresponding test structures to determine the continuity of conducting or insulating ultra-thin films.

By measuring the I-V characteristics of conducting and insulating ultra-thin films the continuity of the films can be determined. For conducting ultra-thin films the continuity can be determined by a combination of two methods. The first method makes use of the different conduction mechanisms in continuous and discontinuous films. The conduction is ohmic in continuous films and non-ohmic in discontinuous films. This difference can be seen by measuring the I-V characteristics of the film. The second method is proposed by Maroof and Evans, where they plot the measured resistance of the film multiplied by the film thickness squared against the film thickness. This graph results in a minimum value which indicates the onset of a continuous conducting ultra-thin film. For the insulating ultra-thin film also the I-V characteristics of the films are used. This time the film is sandwiched between two electrodes. When the insulating film is discontinuous the two electrodes are in direct contact with each other and the conduction is ohmic. When the insulating film is continuous the two electrodes are separated and the conduction will be non-ohmic.

Test structures are designed for the conducting and insulating ultra-thin films, keeping the chosen methodologies in mind. CTLM structures and linear bar structures are designed for the conducting ultra-thin films. For the insulating ultra-thin films, three comparable test structures are designed. Two of these structures are designed in such a way that the piezoelectric nature of the chosen insulating material, used in this project, could not influence the measurement results. Masks are made to enable fabrication of the test structures in the MESA+ nanolab of the University of Twente. Process flows for both types of ultra-thin films are composed and several wafers are made.

W and AlN are chosen as a conducting and insulating material respectively, to show the effectiveness of the established methodology and corresponding test structures. Measurements of six W films and four AlN ultra-thin films, with different thicknesses, are performed. The W films with a thickness of 2.2 nm and higher showed ohmic conduction in the I-V characteristics. The W films with a thickness of 1.3 nm and lower showed non-ohmic behavior. The method of Maroof and Evans has also been used, suggesting to the closure points between 1.3 and 2.2nm. Both methods indicate that the W films become continuous between 1.3 and 2.2 nm. For the AlN ultra-thin films, the I-V characteristics of the 35 and 15 nm films are non-ohmic. The 4 nm film shows ohmic conduction even before annealing the wafer. The 11 nm film shows non-ohmic conduction before annealing. Further

processing resulted in over-annealing of this wafer, showing ohmic conduction. The films of 11, 15 and 35 nm are assumed to be continuous because of there non-ohmic conduction mechanism. The ohmic conduction of the 11 nm film after over-annealing is explained by diffusion through the continuous AlN film. The film of 4 nm is assumed to be discontinuous, which explains the ohmic conduction even before annealing. Because of the change in the conduction behavior, the conclusion has been drawn that the AlN films become continuous between 4 and 11 nm of their thickness.

The drawn conclusions are compared to the SE measurements of both film types done during depositions. The W film closes, according to the SE measurements, between 1 and 1.6 nm. This corresponds with the range found by the electrical measurements. For the AlN film, the film closes around 8 nm. This is also in accordance with the found thickness range by the electrical measurements. The good agreement between the SE and electrical measurements confirms that the designed methodology and corresponding test structures can be used to determine the closure point of the conducting and insulating ultra-thin films.

The results presented in this report are accepted for an oral presentation, at the international conference on microelectronic test structures (ICMTS) 2017. **"Electrical test structures for verifying continuity of ultra-thin insulating and conducting films"** by *S. Banerjee, R. van der Velde, M. Yang, J. Schmitz and A. Y. Kovalgin.*

Chapter 8

Recommendations

For the masks several different structures were designed. During this project, only one or two types of the structures have been measured. A lot of different effects can still be investigated with the remaining structures. For the metallic ultra-thin films, the edge effects of the bar structures in comparison to the CTLM structures can be investigated. For the insulating ultra-thin films, the difference between the structures with and without a bottom electrode can be investigated, in the sense of affecting the result by the piezoelectric nature of AlN.

The process flow for the conducting ultra-thin films includes the deposition of a gate electrode on the backside of the wafer. Due to the limited time, this gate electrode was not implemented on the wafers. Still this can be done relatively easy on the already fabricated wafers. Using this gate electrode interesting field effect measurements on the conducting ultra-thin films can be done.

Unfortunately for the 11 nm AlN film, some technical difficulties interfered with the annealing process. Even tough conclusions could be drawn from the measurement results, it would be better to keep the same process conditions for each wafer. Therefore, the recommendation is to remake the 11 nm film and measure it again before and after annealing. When the process is done correctly the measurement before annealing will show non-ohmic behavior, it is expected that the measurement after annealing will also show non-ohmic behavior. This would confirm the conclusions drawn in this work. To further narrow the thickness range for the closure point of the AlN films, some additional wafers could be made. At this moment it is concluded that the film closes between 4 and 11 nm. The SE growth rate measurements indicate that the film closes around 8 nm. This should be investigated by making one or several additional wafers with film thicknesses of around 8 nm. Such electrical measurements can possibly confirm the conclusions of the SE measurements.

In this report, W and AlN are used to show the effectiveness of the designed methodology and the test structures. The proposed methodology and structures are designed for any conducting or insulating material. Therefore ultra-thin films of different insulating and conducting materials might be examined accordingly. This can prove that the methodology and the test structures work for a broad range of materials.

Chapter 9

Acknowledgments

I would like to thank Sourish Banerjee and Mengdi Yang for there help doing the deposition of the AlN and W respectively. I would also like to thank them for the fruitful discussions we had during this project.

I would like to thank Sander Smits for helping me getting acquainted with the cadence software for the mask designs. And I would like to thank Tom Aarnink for helping by revising the process flows for the wafers made during this project.

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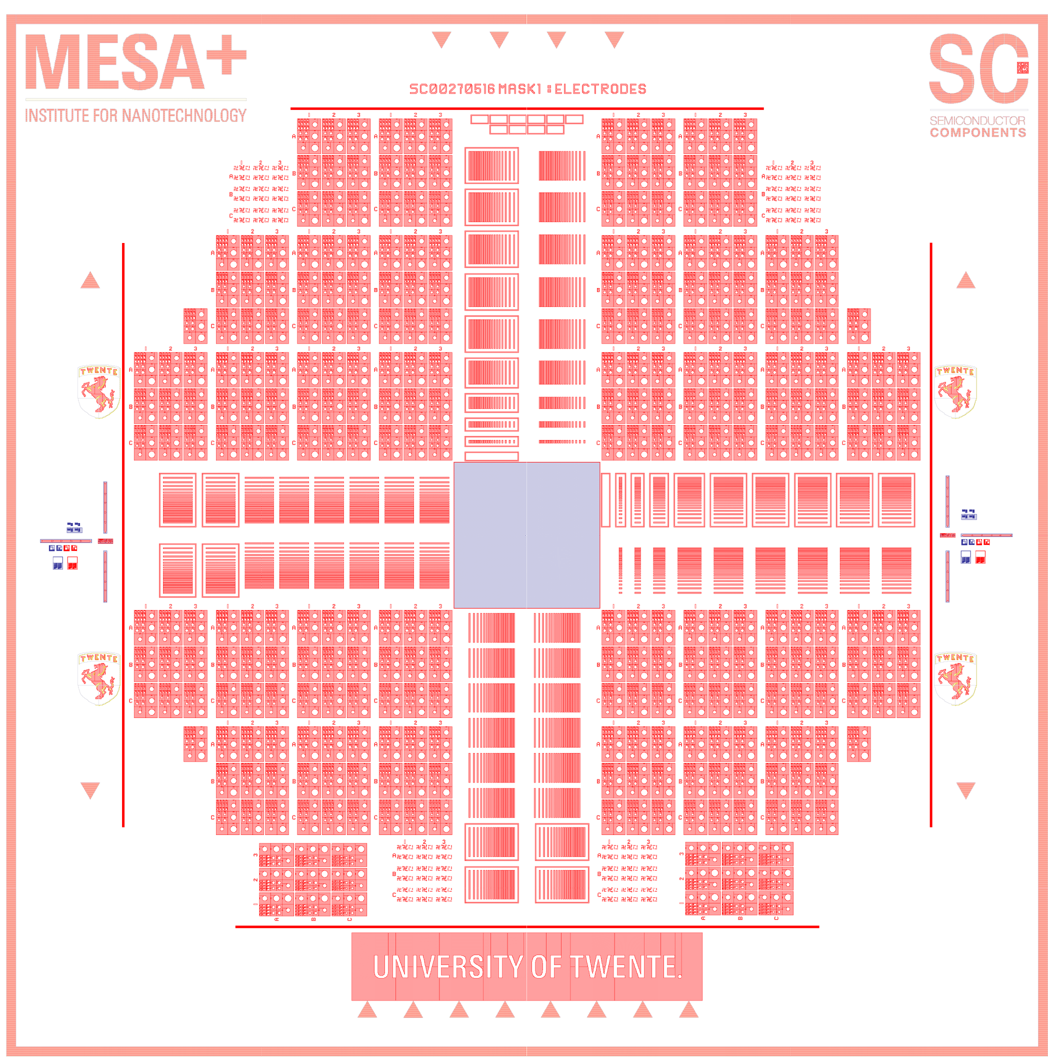
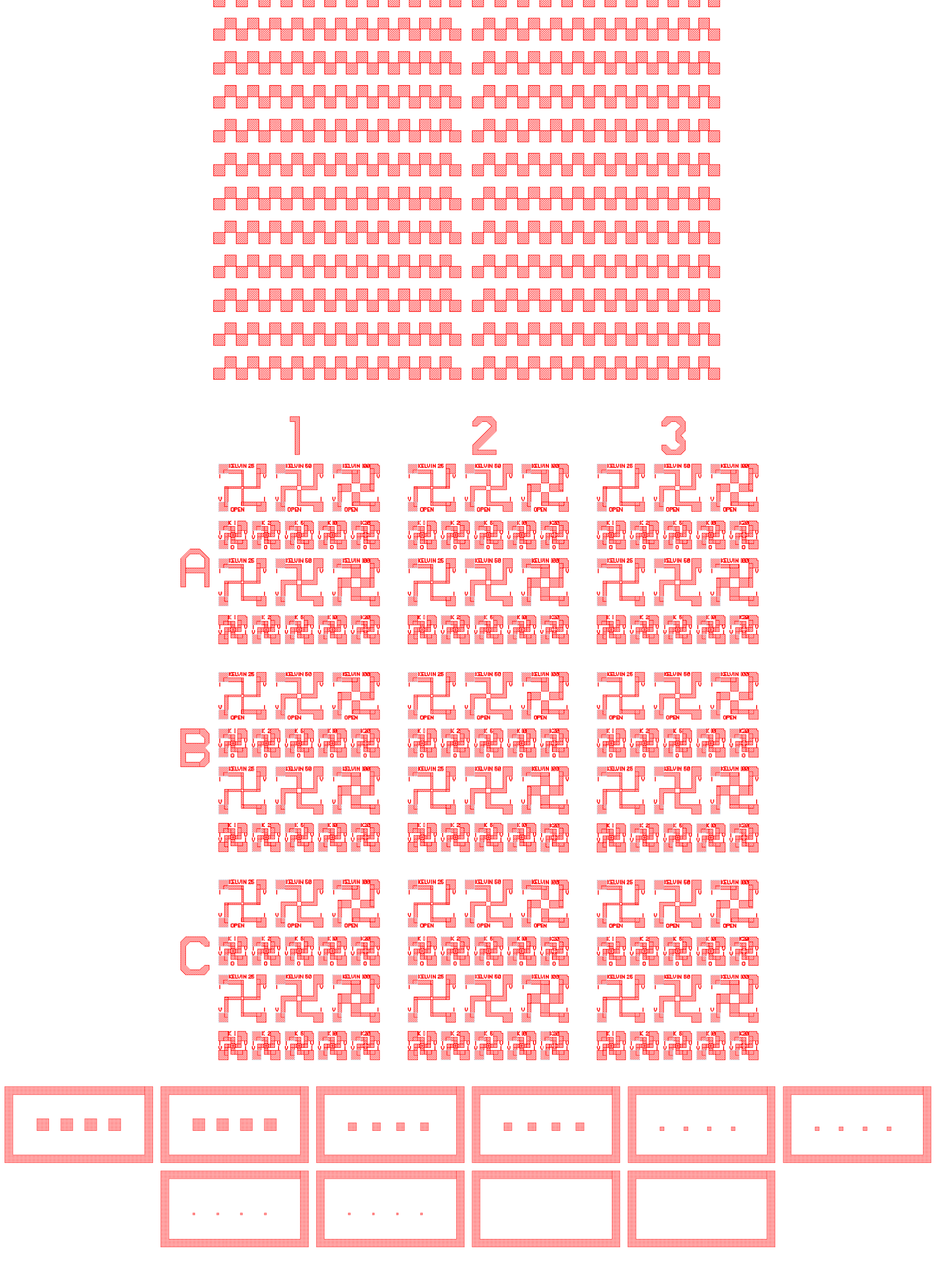
Appendix A

Mask designs

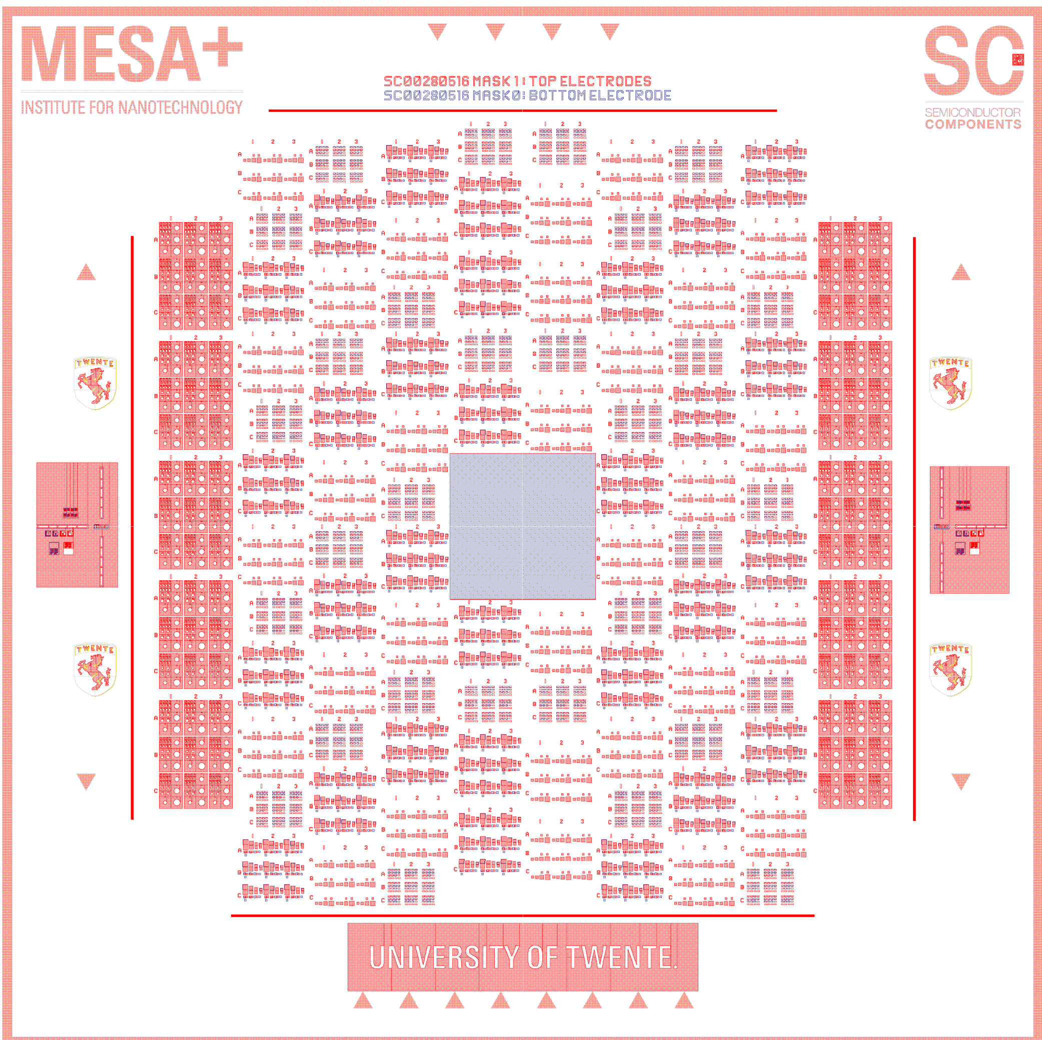
Conducting films



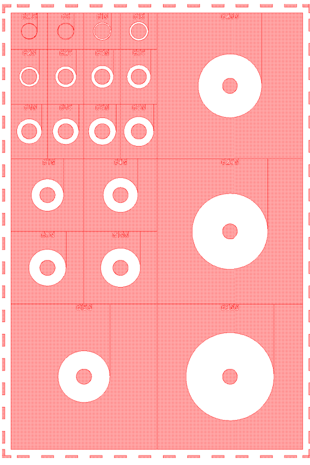
Conducting films, extra structures



Insulating films



Insulating films, extra structure



Appendix B

Process flow test structures for metallic ultra-thin films.

Print date: 2016-11-08

Name of process flow:	Wafer for metal film
Platform:	Electronics
Creation date:	2016-06-08
Personal information	
User name:	Velde, F.J. van der
Email address:	f.j.vandervelde@student.utwente.nl
Company/Chair:	Masterstudenten
Function:	Student
Project:	Test structures for measuring continuity of metal ultra-thin films
Name of supervisor:	Alexey Kolvagin
Process planning	
Process start:	2016-05-30
Process end:	2016-06-17
Status	
Name of advisor:	Bruinink, C.M.
Last revision:	2016-06-09
Approval:	
Approval date:	
Expiration date:	

ILP: In-line Processing	MFP: Metal-free Processing	UCP: Ultra Clean Processing	Removal of Residues

Step	Level	Process/Basic flow		User comments
1		**Substrate Silicon** (#subs103)	NL-CLR-Wafer Storage Cupboard Orientation: <100> Diameter: 100mm Thickness: 525µm +/- 25µm Polished: Single side (OSP) Resistivity: xxx Ωcm Type: p+/boron	
		film1901: Dry Oxidation of Silicon (A2-UCP)		
2	UCP	**Cleaning in Ozone Steam (UCP)** (#clean100)	NL-CLR-WB12 Purpose: removal of organic and inorganic traces. Settings: 2 cycles (overall time: 40:20 min, clean time: 22:50 min)	
3	UCP	**Etching in HF (1%)** (#etch217)	NL-CLR-WB12 Purpose: strip the native SiO_2 after cleaning the silicon substrates in Ozone Steam. Beaker 2: HF 1% Time = 1 min	Obligatory for the silicon monitor wafer of the furnace (if applicable).

			This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	
4	UCP	**Quick Dump Rinse (QDR)** (#rinse121)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
5	UCP	**Substrate drying** (#dry122)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
6	UCP	**Clean TLC furnace cleaning** (#film195)	**NL-CLR- A-stack:** FurnacesA2,A3,A4 Before use contact adminstrator Applications: UCL gate-oxide • Temp.: 1150°C • Gas: 02, 4 liter • TLC: 115 sccm • Ramp: 10°C/min • Cooldown: 7,5°C/min	Optional
7	UCP	**Dry Oxidation of Silicon (UCP)** (#film175)	NL-CLR-Tempress-furnace A2 Standby temperature: 700°C • Temp range.: 800 up to 1100°C • Gas: O_2 • Flow: 4l/min • Ramp: 10°C/min • Cooldown: 7.5 °C/min • Standard programs: UCL-2 950 °C (time variable) UCL-1 1100 °C (time variable)	100nm
		clean1003: In-line cleaning (WB13-UCP)		
8	UCP	**Cleaning in 99% HNO_3** (#clean008)	NL-CLR-WB13 Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	
9	UCP	**Quick Dump Rinse (QDR)** (#rinse121)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
10	UCP	**Substrate drying (WB13)** (#dry158)	NL-CLR-WB13 **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm)	

			• Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
	litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)			
11	ILP	**Dehydration bake** (#litho001)	NL-CLR-WB21/22 Dehydration bake at hotplate • Temp.: 120°C • Time: 5min	Continue immediately with priming the step!
12	ILP	**Priming HMDS (liquid)** (#litho600)	NL-CLR-WB21/22 Primer: HexaMethylDiSilazane (HMDS) Use spincoater: • program: 4000 (4000rpm, 30sec)	
13	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec) Prebake: hotplate • Time: 90 sec • Temp.: 95 °C	
14	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec	
15	ILP	**Development of Olin OiR resists** (#litho200)	NL-CLR-WB21 After exposure bake : hotplate • Temperature: 120°C • Time: 60sec Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
16	ILP	**Quick Dump Rinse (QDR)** (#rinse119)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
17	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
18	ILP	**Postbake of Olin OiR resists** (#litho006)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
19	ILP	**Inspection by optical microscope** (#metro101)	NL-CLR- Nikon Microscope • dedicated microscope for lithography inspection	
	etch1219: Etching in 1% HF (WB13)			

Step	Module	Process	Details	Comments
20	UCP	**Etching 1% HF** (#etch238)	NL-CLR-WB13 Use Beaker HF with 1% • Time variable, 1 min for native SiO_2 strip	
21	UCP	**Quick Dump Rinse (QDR)** (#rinse121)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
22	UCP	**Substrate drying** (#dry122)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		film1531: Sputtering of Titanium (TCOathy)		
23	ILP	**Sputtering of Ti** (#film901)	**NL-CLR-T´COathy** Ti Target • Use Ar flow to adjust process pressure. • Base pressure: < 1.0 e-6mbar • Sputter pressure: 6.6 e-3mbar • power: 200W • Deposition rate = 12.9 nm/min	
		film1534: Sputtering of Platinum (TCOathy)		
24	ILP	**Sputtering of Pt** (#film624)	**NL-CLR-T´COathy** Pt Target • Use Ar flow to adjust process pressure. • Base pressure: < 1.0 e-6mbar • Sputter pressure: 6.6 e-3mbar • power: 200W • Deposition rate = 24.0 nm/min	
		litho1500: Lift-Off with positive resist (WB11)		
25	ILP	**Lift-Off** (#litho500)	NL-CLR-WB11 Purpose: removal of resist and excess metal from the surface of the substrate by ultrasonication in Acetone. Use the ultrasonic bath in WB11. • Beaker 1: Acetone • Time = 10 min **Single wafer processing:** Spray the wafer with Acetone for 30 sec and immediately spray with isopropanol (IPA) for 30 sec. **Batch wafer processing:** • Beaker 2: Acetone • Time = 10 min • Beaker 3: Isopropanol • Time = 10 min	Times are not fixed!
26	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		xclean10042: In-line cleaning of silicon substrates with metallic structures		

		(WB16-ILP)		
27	ILP	**Cleaning in 99% HNO_3** (#clean005)	NL-CLR-WB16 Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	
28	ILP	**Cleaning in 99% HNO_3** (#clean006)	NL-CLR-WB16 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
29	ILP	**Quick Dump Rinse (QDR)** (#rinse119)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
30	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		film1001: ALD of AlN with aSi capping (Clustersystem)		
31	UCP	**ALD of W** (#film001)	NL-CLR-Clustersystem (reactor-2)	Thickness= 1-10nm
32	UCP	**ALD of aSi** (#film002)	NL-CLR-Clustersystem (reactor-2)	Thickness= 10nm
		litho1804: Spincoating of Olin Oir 907-17 (positive resist - ILP)		
33	ILP	**Dehydration bake** (#litho001)	NL-CLR-WB21/22 Dehydration bake at hotplate • Temp.: 120°C • Time: 5min	Continue immediately with priming the step!
34	ILP	**Priming HMDS (liquid)** (#litho600)	NL-CLR-WB21/22 Primer: HexaMethylDiSilazane (HMDS) Use spincoater: • program: 4000 (4000rpm, 30sec)	
35	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec) Prebake: hotplate • Time: 90 sec • Temp.: 95 °C	
36	ILP	**Postbake of Olin OiR resists** (#litho006)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
37	ILP	**Inspection by optical microscope** (#metro101)	NL-CLR- Nikon Microscope • dedicated microscope for lithography inspection	

etch1208: BHF etch (WB10-private use)

Step	Module	Process	Description	Remarks
38	ILP	**Etching SiO2 BHF (1:7)** (#etch125)	NL-CLR-WB9 or 10 Use private beaker with BHF (1:7) Temp.: room temperature Etchrates: • thermal SiO2: 60-80nm/min • PECVD Si02: 125/nm/min • TEOS SiO2: 180/nm/min • TEOS **H3 (new):** 242 nm/min • Pyrex #7740: 20nm/min • Borofloat BF33: 20-25 nm/min • Si3N4-H2: 0.64 nm/min	Backside etching
39	ILP	**Quick Dump Rinse (QDR)** (#rinse119)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
40	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	

film1603: Sputtering of Al at 700W for lift-off processing (Oxford PL400-UCP)

Step	Module	Process	Description	Remarks
41	UCP	**Sputtering of Al (700W)** (#film601)	NL-CLR-Oxford PL400 Purpose: lift-off process using resist as the mask. Select magnetron gun2 (Al) using the manual switch in front of the apparatus. General settings: Power: 700W Pressure: 10mTorr Rotation: 5rpm **Static sputtering (single wafer processing)** Recipe: Al 100 nm pos 1 (700W) Sputter time: 1min 13sec for 100nm **Dynamic sputtering** Al 100 nm dynamic (700W) Recipe: Sputter time: 6min 13sec for 100nm Adjust the sputter time and/or power for obtaining the desired layer thickness. System restrictions: max. sputter time = 15 min; power range = **500-700W**; max. layer thickness = 2 micrometer per run.	

residue1202: Removal of organic residues after lithography by ultrasonication in organic solvents (WB11 - ILP)

Step	Module	Process	Description	Remarks
42	Rem Res	**Removal of organic residues after lithography** (#residue202)	NL-CLR-WB11 Purpose: removal of organic residues by ultrasonication in acetone. Use the ultrasonic bath in WB11. • Beaker 1: Acetone • Time = 10 min	

			• Beaker 2: Isopropanol • Time = 10 min
43	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)

Appendix C

Process flow test structures for insulating ultra-thin films.

Print date: 2016-11-16

Name of process flow:	Wafer for insulating film
Platform:	3D-nanoshaping
Creation date:	2016-06-09
Personal information	
User name:	Velde, F.J. van der
Email address:	f.j.vandervelde@student.utwente.nl
Company/Chair:	Masterstudenten
Function:	Student
Project:	Test structures for measuring continuity of insulating ultra-thin films
Name of supervisor:	Alexey Kolvagin
Process planning	
Process start:	2016-06-12
Process end:	2016-07-08
Status	
Name of advisor:	Bruinink, C.M.
Last revision:	2016-11-16
Approval:	
Approval date:	
Expiration date:	

ILP: In-line Processing	MFP: Metal-free Processing	UCP: Ultra Clean Processing	Removal of Residues

Step	Level	Process/Basic flow		User comments
1		**Substrate Silicon** (#subs101)	NL-CLR-Wafer Storage Cupboard Orientation: <100> Diameter: 100mm Thickness: 525µm +/- 25µm Polished: Single side (OSP) Resistivity: 5-10Ωcm Type: p/boron	
		film1901: Dry Oxidation of Silicon (A2-UCP)		
2	UCP	**Cleaning in Ozone Steam (UCP)** (#clean100)	NL-CLR-WB12 Purpose: removal of organic and inorganic traces. Settings: 2 cycles (overall time: 40:20 min, clean time: 22:50 min)	
3	UCP	**Etching in HF (1%)** (#etch217)	NL-CLR-WB12 Purpose: strip the native SiO_2 after cleaning the silicon substrates in Ozone Steam. Beaker 2: HF 1% Time = 1 min	Obligatory for the silicon monitor wafer of the furnace (if applicable).

			This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	
4	UCP	**Quick Dump Rinse (QDR)** (#rinse121)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
5	UCP	**Substrate drying** (#dry122)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
6	UCP	**Clean TLC furnace cleaning** (#film195)	**NL-CLR- A-stack:** FurnacesA2,A3,A4 Before use contact adminstrator Applications: UCL gate-oxide • Temp.: 1150°C • Gas: 02, 4 liter • TLC: 115 sccm • Ramp: 10°C/min • Cooldown: 7,5°C/min	Not necessary
7	UCP	**Dry Oxidation of Silicon (UCP)** (#film175)	NL-CLR-Tempress-furnace A2 Standby temperature: 700°C • Temp range.: 800 up to 1100°C • Gas: O_2 • Flow: 4l/min • Ramp: 10°C/min • Cooldown: 7.5 °C/min • Standard programs: UCL-2 950 °C (time variable) UCL-1 1100 °C (time variable)	100nm
		clean1003: In-line cleaning (WB13-UCP)		
8	UCP	**Cleaning in 99% HNO_3** (#clean008)	NL-CLR-WB13 Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	
9	UCP	**Quick Dump Rinse (QDR)** (#rinse121)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
10	UCP	**Substrate drying (WB13)** (#dry158)	NL-CLR-WB13 **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm)	

			• Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
		litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)		
11	ILP	**Dehydration bake** (#litho001)	NL-CLR-WB21/22 Dehydration bake at hotplate • Temp.: 120°C • Time: 5min	Continue immediately with priming the step!
12	ILP	**Priming HMDS (liquid)** (#litho600)	NL-CLR-WB21/22 Primer: HexaMethylDiSilazane (HMDS) Use spincoater: • program: 4000 (4000rpm, 30sec)	
13	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec) Prebake: hotplate • Time: 90 sec • Temp.: 95 °C	
14	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec	
15	ILP	**Development of Olin OiR resists** (#litho200)	NL-CLR-WB21 After exposure bake : hotplate • Temperature: 120°C • Time: 60sec Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
16	ILP	**Quick Dump Rinse (QDR)** (#rinse119)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
17	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
18	ILP	**Postbake of Olin OiR resists** (#litho006)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
19	ILP	**Inspection by optical microscope** (#metro101)	NL-CLR- Nikon Microscope • dedicated microscope for lithography inspection	
		etch1219: Etching in 1% HF (WB13)		

Step	Type	Process	Description	Remarks
20	UCP	**Etching 1% HF** (#etch238)	NL-CLR-WB13 Purpose: etching of native SiO2 • Beaker: 1% HF • Time = 1 min (for native SiO2 strip)	
21	UCP	**Quick Dump Rinse (QDR)** (#rinse121)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
22	UCP	**Substrate drying** (#dry122)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		film1531: Sputtering of Titanium (TCOathy)		
23	ILP	**Sputtering of Ti** (#film621)	**NL-CLR-T´COathy** Ti Target • Use Ar flow to adjust process pressure. • Base pressure: < 1.0 e-6mbar • Sputter pressure: 6.6 e-3mbar • power: 200W • Deposition rate = 12.9 nm/min	
		film1534: Sputtering of Platinum (TCOathy)		
24	ILP	**Sputtering of Pt** (#film624)	**NL-CLR-T´COathy** Pt Target • Use Ar flow to adjust process pressure. • Base pressure: < 1.0 e-6mbar • Sputter pressure: 6.6 e-3mbar • power: 200W • Deposition rate = 24.0 nm/min	
		litho1500: Lift-Off with positive resist (WB11)		
25	ILP	**Lift-Off** (#litho500)	NL-CLR-WB11 Purpose: removal of resist and excess metal from the surface of the substrate by ultrasonication in Acetone. Use the ultrasonic bath in WB11. • Beaker 1: Acetone • Time = 10 min **Single wafer processing:** Spray the wafer with Acetone for 30 sec and immediately spray with isopropanol (IPA) for 30 sec. **Batch wafer processing:** • Beaker 2: Acetone • Time = 10 min • Beaker 3: Isopropanol • Time = 10 min	Lift off step did not show while using database with coatings
26	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	

clean1002: In-line cleaning (WB16-ILP)

Step	Lab	Process	Details	Comments
27	ILP	**Cleaning in 99% HNO_3** (#clean005)	NL-CLR-WB16 Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	
28	ILP	**Cleaning in 99% HNO_3** (#clean006)	NL-CLR-WB16 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
29	ILP	**Quick Dump Rinse (QDR)** (#rinse119)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
30	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
31				Deposition of aSi adhesion layer
32				ALD of AlN
33				Deposition of capping layer of aSi

litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)

Step	Lab	Process	Details	Comments
34	ILP	**Dehydration bake** (#litho001)	NL-CLR-WB21/22 Dehydration bake at hotplate • Temp.: 120°C • Time: 5min	Continue immediately with priming the step!
35	ILP	**Priming HMDS (liquid)** (#litho600)	NL-CLR-WB21/22 Primer: HexaMethylDiSilazane (HMDS) Use spincoater: • program: 4000 (4000rpm, 30sec)	
36	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec) Prebake: hotplate • Time: 90 sec • Temp.: 95 °C	
37	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec	
38	ILP	**Development of Olin OiR resists** (#litho200)	NL-CLR-WB21 After exposure bake : hotplate • Temperature: 120°C • Time: 60sec	

			Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec
39	ILP	**Quick Dump Rinse (QDR)** (#rinse119)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
40	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
41	ILP	**Postbake of Olin OiR resists** (#litho006)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min
42	ILP	**Inspection by optical microscope** (#metro101)	NL-CLR- Nikon Microscope • dedicated microscope for lithography inspection

film1502: Sputtering of Platinum (Sputterke)

43	ILP	**Sputtering of Pt** (#film118)	NL-CLR-nr. 37 / Sputterke Pt Target (gun #: see mis logbook) • use Ar flow to adjust sputter pressure • base pressure: < 1.0 e-6mbar • sputter pressure: 6.6 e-3mbar • power: 200W depositionrate = 22-27 nm/min

litho1500: Lift-Off with positive resist (WB11)

44	ILP	**Lift-Off** **(**#litho500)	NL-CLR-WB11 Purpose: removal of resist and excess metal from the surface of the substrate by ultrasonication in Acetone. Use the ultrasonic bath in WB11. • Beaker 1: Acetone • Time = 10 min **Single wafer processing:** Spray the wafer with Acetone for 30 sec and immediately spray with isopropanol (IPA) for 30 sec. **Batch wafer processing:** • Beaker 2: Acetone • Time = 10 min • Beaker 3: Isopropanol • Time = 10 min
45	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)

clean1002: In-line cleaning (WB16-ILP)

46	ILP	**Cleaning in 99% HNO_3** (#clean005)	NL-CLR-WB16 Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	
47	ILP	**Cleaning in 99% HNO_3** (#clean006)	NL-CLR-WB16 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
48	ILP	**Quick Dump Rinse (QDR)** (#rinse119)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
49	ILP	**Substrate drying** (#dry120)	NL-CLR-WB **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
50				Silicidation of aSi in reactor of ALD system, at 200 degrees Celsius for 30 minutes