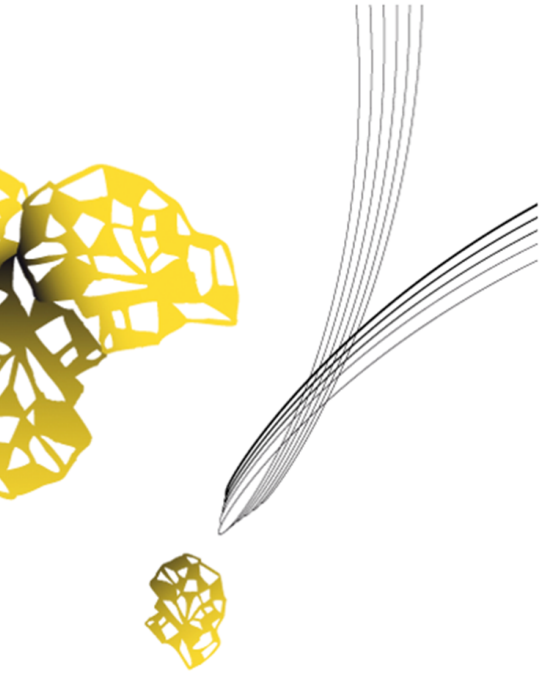
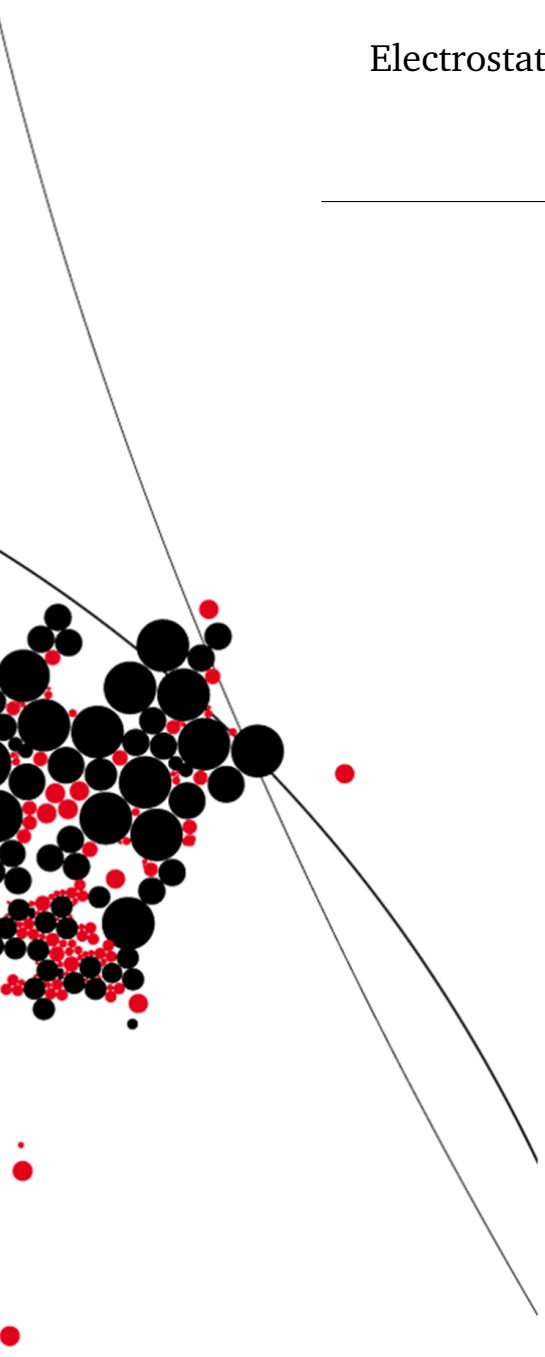


Electrostatically defined quantum dots in a two dimensional electron/hole gas at the Si and SiO_2 interface

M.W.S. Vervoort



April 12, 2017

University of Twente

Department of Electrical Engineering
Institute for Nanotechnology
Nano Electronics

Electrostatically defined quantum dots in a two dimensional electron/hole gas at the Si and SiO_2 interface

M.W.S. Vervoort

1. Supervisor PhD S.V. Amitonov
Group: Nano Electronics
University of Twente

2. Supervisor dr.ir. F.A. Zwanenburg
Group: Nano Electronics
University of Twente

3. Supervisor prof.dr.ir. W.G. van der Wiel
Group: Nano Electronics
University of Twente

Reviewer prof.dr. J. Schmitz
Group: Semiconductor Components
University of Twente

April 12, 2017

M.W.S. Vervoort

Electrostatically defined quantum dots in a two dimensional electron/hole gas at the Si and SiO_2 interface

April 12, 2017

Supervisors: PhD S.V. Amitonov, prof.dr.ir. W.G. van der Wiel, dr.ir. F.A. Zwanenburg and prof.dr.ir. W.G. van der Wiel

Reviewer: prof.dr. J. Schmitz

University of Twente

Nano Electronics

Institute for Nanotechnology

Department of Electrical Engineering

Drienerlolaan 5

7522 NB and Enschede

Abstract

In this thesis electrostatically defined quantum dots formed in a two dimensional electron/hole gas are investigated. Until now, only quantum dots have been made in intrinsic silicon by accumulating charge carriers while in this project the main focus is on defining a quantum dot by means of depletion.

The devices used in this thesis are made from a $Si - SiO_2 - Al_2O_3$ layer stack with a metal gate on top. At the interface of $SiO_2 - Al_2O_3$ negative fixed charge is present attracting free holes at the $Si - SiO_2$ interface, acting as a two dimensional hole gas. These holes are spatially confined into a quantum dot with the use of metal gates. By making use of literature, device iterations and a finite element method simulation, a close to optimal depletion hole dot design is presented. This depletion hole dot made from palladium is shown to be stable with transport measurements up to the possible few hole regime.
As an alternative to palladium this thesis addresses the possible implementation of titanium as a gate metal. Where titanium has the advantage of being more robust during processing thereby increasing device yield, but on the contrary it is found to affect the negative fixed charge in the system.
Additionally a charge sensor is implemented by fabricating a double layer device made entirely from titanium. This sensor is a single electron dot shown to be stable over more than 30 charge transitions. This, and the fact that titanium is not found to oxidize after a cumulative time of 95 minutes at 160 $^{\circ}$C indicates that titanium is a good alternative for palladium.
Furthermore this thesis shows that it is possible to define both a depletion hole dot and single electron dot simultaneously in gate space allowing the device to be pushed even further by using charge sensing.
Lastly it is found that the exposure of a sample to ultraviolet and ozone can be used to manipulate the fixed charge present in the system.

1 Acknowledgments

First of all I would like to thank Floris Zwanenburg and Wilfred van der Wiel for the lectures during my masters in the subject of nanoelectronics, the intriguing field and their combined enthusiasm convinced me to pursue this field during my thesis. Their devotion is shared by my day to day supervisor Sergey Amitonov, who I would like to thank for his extensive knowledge, guiding and helping hand in the cleanroom, as well as in the lab. Following him like a shadow in the first phase of my thesis was very interesting and made me learn a lot about processing. Additionally to the cleanroom work he supported me like a call center on Slack, and even when he was not at the office he out-competes my girlfriends response speed.

Besides this already great team of supervisors I would like to thank Chris Spruijtenburg for joining when the original project came to a standstill due to the failure of an essential machine in the cleanroom. You helped me in search for a new topic and showed me the way to electrostatically define quantum dots.

Furthermore I would like to thank Floris and Matthias for their involvement in the keeping students slim and fit policy called: "NE football team". It was a pleasure to defend the honors of NE against others. Besides my direct supervisors I would like to thanks my fellow students and other PhD's for giving me a helping hand when needed with EBL sessions, measurements, sharp remarks and mental support. Of course also many thanks to Thijs and Joost for their help with the Oxford Heliox setup.

Many thanks also go to Jurrian Schmitz who was has made major contributions for my master program by arranging not only an internship at Philips Research but also being the external member of my graduation committee. I learned a lot from his feedback and enthusiasm regarding projects.

For the support throughout this thesis and for the delighted talks about what the hell I am actually doing I would like to thank my family, friends and Lotte who were a major support throughout this thesis.

To conclude all other members of the Nanoelectronics group who made the stay all the more enjoyable, many thanks to you all!

Contents

Tab. 1.1.: Abbreviations used in this thesis.

Symbol	Description
2DEG	Two-Dimensional Electron Gas
2DHG	Two-Dimensional Hole Gas
AFM	Atomic Force Microscope
BG	Barrier Gate
CI Model	Constant Interaction Model
DAC	Digital to Analog Converter
DMSO	DiMethylSulfOxide
DOS	Density Of States
EBL	Electron Beam Lithography
FEM	Finite Element Method
GPIB	General Purpose Interface Bus
IPA	IsoPropyl Alcohol
LG	Lead Gate
MIBK	Methyl IsoButyl Ketone
NE	Nano Electronics
PCB	Printed Circuit Board
PMMA	PolyMethyl MethAcrylate
QTLab	Quantum Transport Laboratory
SD	Source drain
SET	Single Electron Transistor
SHG	Second-Harmonic generation
SHT	Single Hole Transistor
SMU	Source Measure Unit
UV	UltraViolet
ZIF	Zero Insertion Force

Tab. 1.2.: Constants used in this thesis.

Symbol	Description	Value	Unit
e	Elementary charge	$1.602 \cdot 10^{-19}$	C
k_B	Boltzmann constant	$1.38 \cdot 10^{-23}$	$\mathrm{m^2\ kg\ s^{-2}\ K^{-1}}$
h	Planck constant	$6.626 \cdot 10^{-34}$	$\mathrm{m^2\ kg\ s^{-1}}$

Tab. 1.3.: Symbols used in this thesis.

Symbol	Description	Unit
C	Capacitance of the dot	F
C_D	Drain capacitance of the dot	F
C_G	Gate capacitance of the dot	F
C_S	Source capacitance of the dot	F
E_add	Addition voltage	eV
E_c	Conduction band	eV
E_C	Orbital level energy	eV
E_F	Fermi level	eV
E_Fi	Intrinsic Fermi level	eV
E_v	Valance band	eV
ΔE	Charging energy	eV
I_SD	Source drain current	A
R_t	Tunneling Resistance	Ω
T	Temperature	K or °C
V_SD	Source drain voltage	V
μ_S	Electrostatic potential of the source	eV
μ_D	Electrostatic potential of the drain	eV
μ_dot	Electrostatic potential of the dot	eV

2 Introduction

The prediction of Gordon Moore in 1965 that the number of transistors in a dense integrated circuit would continue to double every two years led to a business model of miniaturizing in the semiconductor industry [1]. When these transistors cramp up closer to the fundamental limits of physics it becomes interesting to note that after being scaled down a couple orders of magnitude in size no major changes in behavior occur. However, this behavior does change when sizes become in the order of the electron wavelength and physics as we experience it in daily live changes. A new and novel concept is needed to gasp these changes and to apply them for new technology. To do this physicist leap into the field of quantum mechanics where the behavior of matter and its interactions with energy on the scale of atoms and subatomic particles is investigated. As Feynman already noted in 1959: "There is plenty of room at the bottom" [2].
In the field of quantum mechanics one could think of an atom connected by source and drain contacts where the quantization of charge in units of "e" becomes important, a so called quantum dot. A quantum dot is an artificially fabricated device in a solid, typically consisting of $10^3 - 10^9$ atoms and a comparable number of electrons. These electrons are virtually all tightly bound to the nuclei of the material, however some free electrons between one and a few hundred can reside on the dot [3].

To form a quantum dot the energy spectrum has to be confined in all three directions leading to quantum effects that strongly influence the electronic transport at low temperatures. In particular it leads to the formation of a discrete energy spectrum. The atomic state of a quantum dot can be probed by attaching current and voltage leads enabling movement of electrons on or off the dot at the cost of the charging energy required to overcome the Coulomb repulsion between electrons [4]. Whenever a single quantum dot is properly understood one could look into systems of coupled dots, a so called artificial molecule. Two quantum dots can be coupled by weak ionic bonds or strong covalent bonds where the two dots are quantum-mechanically coupled. This coupling allows an electron to tunnel between the states of both dots, thereby creating a coherent wave that is delocalized over the two dots, hence a superposition state. A so called qubit [5].
A qubit behaves fundamentally different from a classical bit (0 or 1) and was first posed by Yuri Manin in 1980 [6]. It makes use of the superposition of two eigenstates in a linear combination as depicted in Equation 2.1. Realization of a qubit is possible

in many ways as in principle any quantum two-level system can be used, as for example nuclear spin [7], single photon by using the polarization of light [8], by using electron spin or hole spins. At the moment these realizations of qubits are unfortunately less stable than regular bits due to scattering effects causing loss of spin coherence.

$$|\psi >= \alpha|0 > +\beta|1 > \tag{2.1}$$

Advances in silicon qubits are being made by using isotropically purified silicon 28 containing zero magnetic spin limiting the effect of hyperfine interactions and spin orbit coupling [9], [10]. Whenever these qubits are better understood and spin coherence times are further improved they are a good candidate for building blocks of a quantum computer.
A quantum computer makes it possible to efficiently solve certain computational problems which have no efficient solution on a classical computer, e.g. prime factorization of an integer [11]. Another example that demonstrates the power of the quantum computer is the search through unsorted data [12].
To fabricate these computers better understanding of quantum effects and possible ways to define quantum dots are however required for which this thesis will deliver a small building block.

2.1 Aim of this research

The aim of this thesis is to measure the few or even single hole regime of a lateral depletion hole dot in intrinsic silicon. These dots are electrostatically defined artificial quantum dots in a two dimensional electron gas at the Si-SiO_2 interface. The devices are are fabricated in the MESA+ cleanroom at the University of Twente. A possible confirmation of the few or even single hole regime can be done by making use of a single electron transistor in the vicinity to act as a charge sensor.

2.2 Thesis outline

The outline of this thesis is as follows, sorted per chapter with a brief description:

Chapter 3, Theory
This thesis starts with the important properties of silicon for quantum applications followed by electron and hole transport in traditional semiconductor devices. Secondly the concept of a quantum dot is addressed involving spacing of the energy levels, Coulomb interactions, tunneling rates, excited states, capacitive coupling and fixed charge.
Chapter 4, Simulation
This chapter addresses the setup and results from the finite element method simulations made by using Comsol Multiphysics. Additionally import straight from KLayout into Comsol Multiphysics as well as importing atomic force microscope scans are discussed.
Chapter 5, Device layout
In this chapter the layout of several samples that were fabricated during the iterative process in this thesis are discussed.
Chapter 6, Experimental methods
Experimental methods including cleanroom techniques such as the electron beam lithography, cold development, lift off, ultraviolet ozone exposure, measurement preparation and the experimental setup are discussed.
Chapter 7, Results
In this chapter the results presented for the different types of devices as well as measurements about the fixed charge in the system, and possible implementation of palladium and titanium as a gate metal.
Chapter 8, Conclusion and discussion
In this chapter the results from this thesis are discussed and conclusions are drawn.
Chapter 9, Outlook
To conclude an outlook is presented addressing new insights and questions arisen during this thesis. These statements and ideas can act as a guideline for further work and hopefully lead to the publication of a paper in the near future.

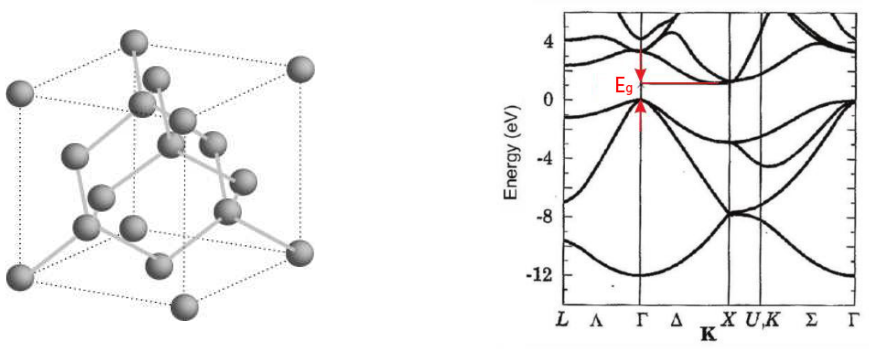
3 Theory

In this section the theory concerning this thesis is discussed starting with classical semiconductor physics such as silicon devices and band structures to quantum mechanical behavior including Coulomb interactions, quantum dots, excited states and charge sensing. To conclude the origin of fixed and mobile charge in the system are discussed.
It is noted that the measured devices mainly address transport of holes while some graphical representation in the theory section address transport of electrons. These representations are more intuitively and therefore it will be clearly stated whether an illustration applies to either hole or electron transport.

3.1 Silicon

The most common material in the world of solid state physics and second most abundant on earth, after oxygen [13], is silicon which has a wide variety of uses due to its properties as a semiconductor material.
Silicon orientates itself as a diamond cubic crystal structure since it crystallizes in the same pattern as a diamond, hence Figure 3.1a [14]. Purified silicon consists of three stable isotopes: ^{28}Si, ^{29}Si, ^{30}Si, respectively being 92.2, 4.7 and 3.1 % of the total amount of atoms [15]. From these stable isotopes, ^{29}Si has a natural $+\frac{1}{2}$ nuclear spin creating an inhomogeneous and randomly fluctuating background of spins decreasing coherence times and offering less control of the system. To overcome this problem enriched ^{28}Si wafers beyond 99.9998 % are being fabricated for semiconductor quantum devices [16].

In intrinsic silicon the number of holes and electrons available for transport are equal (p = n) because silicon has no overall net charge. This results in the intrinsic Fermi level (E_{Fi}) being equally spaced between the valence (E_{v}) and conduction band (E_{c}) where the band gap is determined by the lowest point of the conduction band and the highest point of the valence band. Monocrystalline silicon is an intrinsic semiconductor with an indirect band gap between the valence band and the conduction band of $E_{\mathrm{g}} = 1.12$ eV at $T = 300$ K as depicted in Figure 3.1a. The band gap differs from material to material and is largest for insulators where almost no charge transport is possible because electrons are tightly bound to the nuclei, up till



(a) (b)

Fig. 3.1.: a) Face-centered cubic structure of a silicon unit cell [17]. b) Energy band diagram of monocrystalline silicon, E_g is the energy band gap [18]

metals where the conduction and valence band overlap enabling charge transport between atoms.

With a semiconductor material such as silicon these bands can be tuned by doping the intrinsic silicon with a substitutional atom that has nearly the same size and a unit valence of plus one (n-type/Arsenic) or minus one (p-type/Boron). These substitutional atoms act as dopants shifting the Fermi level closer to the valance (p-type) or conduction (n-type) band. Due to this valence difference free electrons or holes become available in the valence band allowing an electron/hole to move from one atom to another. The amount of electrons available for charge transport is not only influenced by doping but also due to thermal energy ($k_\mathrm{B}\ T$) allowing electrons and holes to move from one energy state to another. The probability of occupying an available state can be calculated from the Fermi-Dirac distribution as depicted in Equation 3.1 [19]. Some electrons occupy an energy state higher than the Fermi energy ($E > E_\mathrm{F}$) due to thermal energy creating free electrons in the conduction band allowing the metal to conduct. When the thermal energy is decreased by using for example a cryostat, the electrons redistribute under the Fermi energy ($E < E_\mathrm{F}$) disabling transport between atoms, because the conduction band is empty and the valence band completely filled at zero temperature. Besides the Fermi energy the free carrier concentration depends on the Density of States (DOS) describing the number of states per interval of energy at each energy level is allowed.

$$f(E) = \frac{1}{e^{\frac{E-E_\mathrm{Fi}}{k_\mathrm{B}T}} + 1} \tag{3.1}$$

3.2 Quantum dot

A quantum dot is an artificially structured system that can be filled with electrons or holes by confining the energy spectrum in all dimensions. A particle that can move freely in two directions, but is confined in one direction is called a quantum well. Accordingly a particle that is confined in two directions is called a quantum wire and a particle that is confined in all directions a quantum dot. It leads to the formation of a discrete (0D) energy spectrum.
A quantum dot typically consisting of $10^3 - 10^9$ atoms and a comparable number of electrons/holes tightly bound to their nuclei has however some free electrons/holes (between one and a few hundred) that can reside on the dot or so called island [3]. This island is coupled to a source and drain through tunnel junctions and capacitively to one or more gate electrodes as schematically depicted in Figure 3.2a. By tuning these tunnel junctions and gates into the Coulomb blockade regime electrons and holes can tunnel on or of the dot in units of 'e' allowing for the formation of a single-electron or single-hole transistor (respectively SET, SHT) [9].

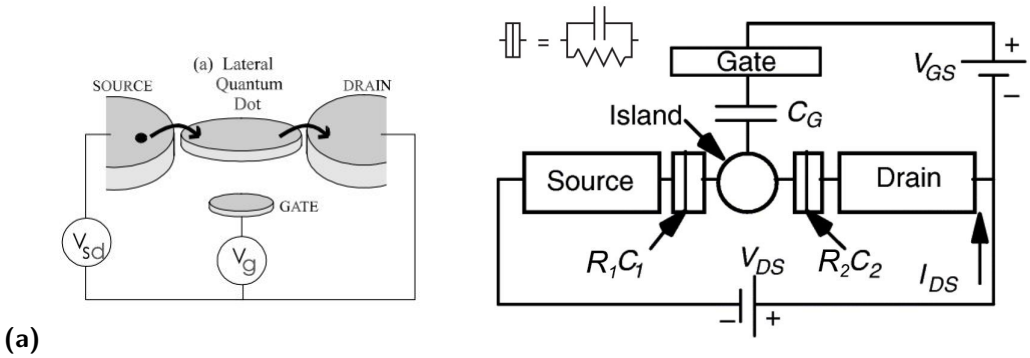


Fig. 3.2.: a) Schematic representation of a lateral quantum dot in the shape of a disk connected to source and drain, and capacitively coupled to the gate [3].
b) Simplified electrical equivalent of a lateral quantum dot system with source and drain contacts connected by a tunnel junction to the island, and a gate capacitively coupled to the dot. The tunnel junction is equivalent to a resistor and capacitor in parallel as depicted at the left top [20].

3.3 Coulomb interactions

Transport in a quantum dot takes place due to Coulomb interactions describing the force that interacts between static electrically charged particles present on the island and the source/drain. This indicates that a certain Coulomb repulsion (preventing an electron to flow) has to be overcome in order for an electron to tunnel on or off the dot. In literature this effect is known as Coulomb blockade since no current can flow through the device and was already first noticed in 1987 by Fulton et

al. [21]. Coulomb blockade can be represented by drawing the energy levels of the source (μ_S), drain (μ_D) and dot (μ_{dot}) schematically as depicted in Figure 3.3a where the energy potential of the dot does not align with the bias window. The blockade can be overcome by increasing the potential between the source and drain or alternatively by changing the voltage on the gate. Due to capacitive coupling of the gate the potential landscape alters and the available state (μ_N) allows an electron to tunnel in and out of the dot as depicted in Figure 3.3b.

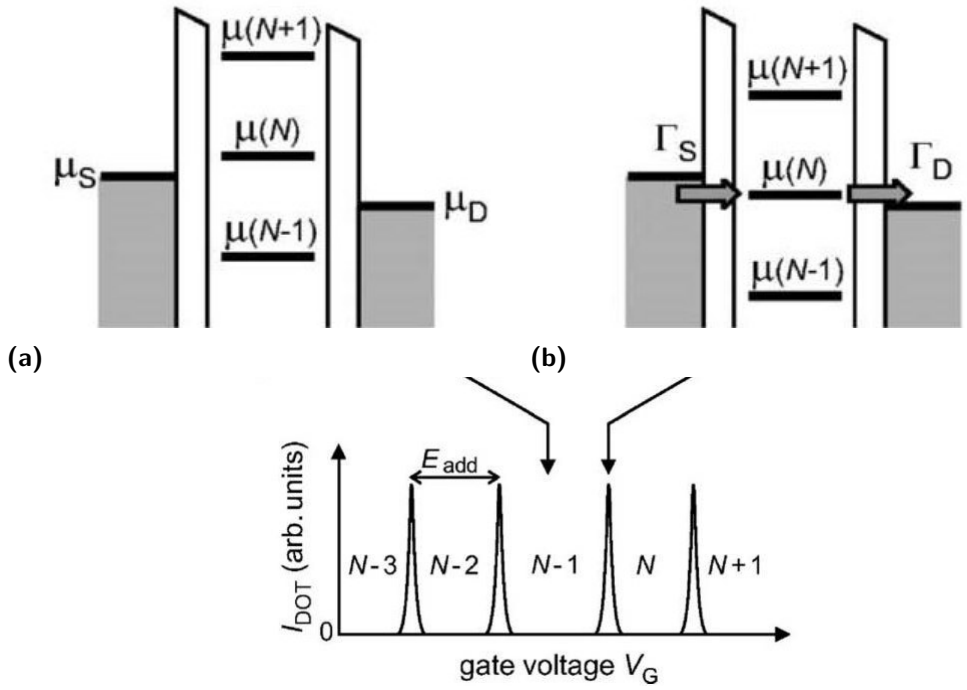


Fig. 3.3.: Schematic representation of the electrochemical potential levels of a quantum dot in the low bias regime regime for the case of electron transport. a) No energy level of the dot falls between the bias window, meaning an electron can tunnel into the N-1 state when empty but cannot tunnel off the dot to the drain, hence Coulomb blockade. b) The energy level of the dot falls between the bias window allowing an electron to tunnel into the N state and tunnel forwards onto the drain, so the number of electrons can alternate between N-1 and N, resulting in a single-electron tunneling current. The magnitude of the current depends on the tunnel rate between the dot and the reservoir on the left τ_S and on the right τ_D. c) Schematic representation of the current through the dot as a function of gate voltage V_G. The gate voltages where the level alignments of (a) and (b) occur are indicated by the arrows [9].

A quantum dot can be described in the electrical domain by using the constant-interaction (CI) model. This model assumes that Coulomb interactions between an electron occupying the dot and all other electrons (inside and outside the dot) are parametrized by a constant capacitance C. This model is hold valid if given that the quantum dot is an almost isolated system and secondly, the energy levels of the dot are independent of the number of electrons on the dot [22]. The total capacitance of the dot is a combination of all capacitances connected to it, hence $C = C_G + C_D + C_S$.

The energy potential of a quantum dot can be described by Equation 3.2 where E_{N} is the sum over the occupied single particle energy levels. And the left part is the continuous classical potential due to capacitive coupling of a bias voltage applied from the source/drain and the gate to the dot [23].

$$U(N) = \frac{[-|e|(N - N_0) + C_{\mathrm{S}}V_{SD} + C_{\mathrm{G}}V_{\mathrm{G}}]^2}{2C} + \sum_{n=1}^{N} E_{\mathrm{N}} \tag{3.2}$$

$$\mu_{\mathrm{dot}}(n) = (N - N_0 - 1/2)E_{\mathrm{C}} - e(C_{\mathrm{G}}/C)V_{\mathrm{G}} + E_{\mathrm{N}} \tag{3.3}$$

This discrete behavior due to Coulomb blockade is depicted in Figure 3.3c where the addition energy (E_{add}) has to be paid to add an additional electron to the dot. In general the addition energy is equal to the charging energy (E_{C}) except for when an extra penalty has to be paid whenever a shell is filled and the electron has to go into a new orbital. Each orbital state can be occupied by a certain number of electrons following Hunds rule and the Pauli exclusion principle. This means that in case of adding an electron to a new orbital both the charging energy and the orbital level spacing (ΔE) have to be provided, hence Equation 3.4.

$$E_{\mathrm{add}} = E_{\mathrm{C}} + \Delta E = \frac{e^2}{C} + \Delta E \tag{3.4}$$

This indicates that to overcome Coulomb blockade the bias voltage moving an electron on or off the dot must be higher than the elementary charge divided by the self capacitance of the island, hence $V_{\mathrm{bias}} > \frac{e^2}{C}$. Besides this, two other requirements to form a quantum dot have to be met:

1. As a first requirement the electron should be able to reside on the dot, therefore the charging energy (E_{c}) must be larger than the thermal energy: $k_{\mathrm{B}}T$, where k_{B} is the Boltzmann's constant and T the temperature in Kelvin. This first requirement is met by lowering the temperature close to absolute zero by using a cryogenic setup. The temperature has to be low enough such that the energy separation of these levels (typically 2-6 meV) is larger than the thermal energy of the free charge carriers $E_{\mathrm{th}} = k_{\mathrm{B}}\ T$ (26 meV @ 300 K).

$$E_{\mathrm{C}} = \frac{e^2}{C} > k_{\mathrm{B}}T \tag{3.5}$$

2. The second requirement states that the tunneling resistance (R_t) of a quantum dot has to be larger than the resistance quantum $\frac{h}{e^2} = 25.812\ \mathrm{k\Omega}$. This implies that an electron has to be either located on the source, drain or the island. Charging the island with an additional charge takes time, hence the RC-time of the quantum dot: $\Delta t = R_\mathrm{t} C$.
   The charging energy $\Delta E_\mathrm{c} = e^2/C$ of the system with respect to Heisenberg's uncertainty relation $\Delta E_\mathrm{c}\ \Delta t > h$ states that the more precisely the position of some particle is determined, the less precisely its momentum can be known, and vice versa. This leads to the condition: $R_\mathrm{t} >> \frac{h}{e^2}$ as depicted in Equation 3.6 [24]. This requirement can be achieved by making use of materials with a good dielectric constant. High k dielectrics are used nowadays to prevent electrons from tunneling to allow even further improvement in the finFET technology [25]. Furthermore the temperature has to be as low as possible and the dot has to be shielded from electromagnetics [3].

$$\begin{aligned} &\frac{e^2}{C} \cdot R \cdot C > h \\ &R_t >> \frac{h}{e^2} \end{aligned} \tag{3.6}$$

The rate an electron tunnels onto the dot can be described by a tunneling rate (τ_S) and the tunneling off the dot by the rate (τ_D) as depicted in the Figure 3.3b. These rates determine the total current that can flow through the dot limited by the slowest tunneling rate. The current can be calculated as a parallel combination of τ_S and τ_D where in case of one dominant tunneling rate, hence slow, the equation can be simplified as depicted in Equation 3.7.

$$I = e\frac{\tau_\mathrm{S}\tau_\mathrm{D}}{\tau_\mathrm{S} + \tau_\mathrm{D}} \approx e\frac{\tau_\mathrm{S}\tau_\mathrm{D}}{\tau_\mathrm{dominant}} \tag{3.7}$$

Transport through a quantum dot is not only possible due to ground states, but at certain bias voltages a so called excited state contributes to the current. An excited state is a quantum state of the system that has a higher energy than the lowest available potential energy state, hence ground state. It can form due to its movement to a different orbital allowing transport of an additional electron as depicted in Figure 3.4a. In addition to an excited state the bias voltage can be increased to exceed the addition voltage to open up a second ground state for transport as depicted in Figure 3.4b.

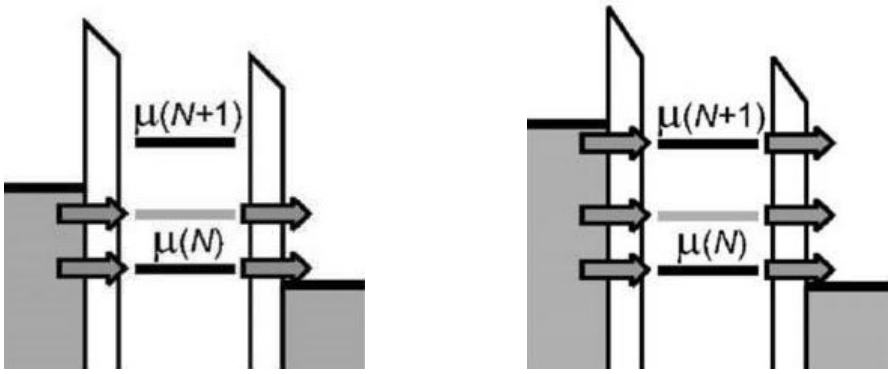


Fig. 3.4.: Schematic representation of the electrochemical potential levels of a quantum dot in the high-bias regime for the case of electron transport. a) The level in gray corresponds to a transition involving an excited state making an extra state available through which an electron can tunnel. b) The applied bias voltage exceeds the addition energy for N electrons, leading to a third path to tunnel through [9].

3.4 Coulomb diamond

A quantum dot can be characterized visually by a so called Coulomb diamond plot where diamond like structures represent the current in the system. In this measurement source-drain sweeps are taken over a rage of gate voltages while the source-drain current is measured and mapped as differential conductance $\mathrm{d}I_{\mathrm{SD}}/\mathrm{d}V_{\mathrm{SD}}$. As an example a Coulomb diamond plot is depicted in Figure 3.7 for transport of holes where Coulomb blockade is established within the diamond while outside a current flows between the source and the drain. The amount of energy states in a dot is indicated and a vertical line cut of the 3D Coulomb diamond plot can be taken as a line cut at V_{SD}=0 V to show Coulomb peaks as depicted in Figure 3.3c indicating alignment within the bias window of ground states. On top of these ground states excited states are expressed as diagonal lines parallel to the ground state indicating a local increase in current as depicted in Figure 3.6 with red arrows.
This allows for a stable configuration with N holes on the dot. Besides changing the gate voltage the source drain voltage can be manipulated changing the electrochemical potential between the source ($\mu_{\mathrm{S}} = \mu_0 + eV_{\mathrm{SD}}$) and the drain ($\mu_{\mathrm{D}} = \mu_0$) where μ_0 is the ground potential. Whenever the potential of the dot does not align within the bias window ($\mu_{\mathrm{S}} - \mu_0$) no conduction is possible. Solving these boundary conditions for Equation 3.8 and 3.9 [5] in the top of the diamond results in addition energy of $E_{\mathrm{add}} = \frac{e^2}{C} + \Delta E$ as depicted in Figure 3.7. The difference in peak height between the N and N+1 level, ΔE corresponds to a new orbital level. The slope of the Coulomb diamonds can also be used to calculate the capacitances of individual gates to the quantum dot, hence $\mathrm{C_G}, \mathrm{C_D}, \mathrm{C_S}$ and C. Furthermore an alpha factor can be defined to describe the coupling between the gate and the dot; $\alpha = C_{\mathrm{g}}/C$. A high

alpha factor indicates that it becomes easier to change the electrochemical potential of the dot without changing the tunnel barriers.

$$0 = (N - N_0 - 1/2)E_C - e(C_G/C)V_G + E_N - \mu_0 \tag{3.8}$$

$$eV_{SD} = (N - N_0 + 1/2)E_C - e(C_G/C)V_G + E_{N+1} - \mu_0 \tag{3.9}$$

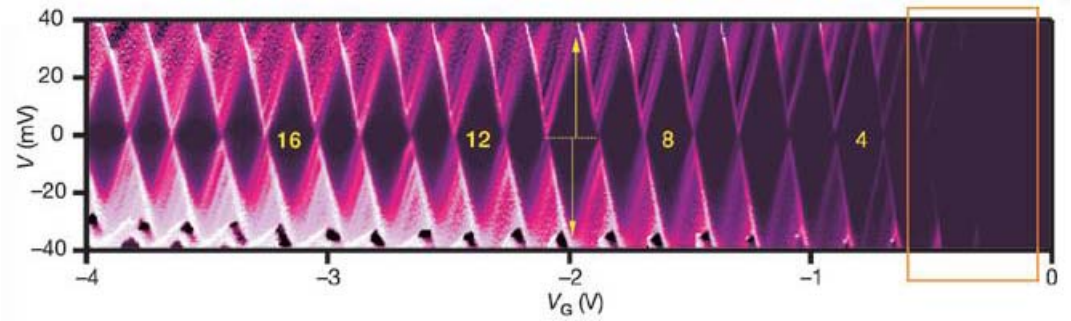


Fig. 3.5.: Two-dimensional color plot of the differential conductance or the case of hole transport, dI/dV versus V and negative V_G at $T = 4$ K (black is zero, white is 3 μS) f. In the black diamond-shaped regions, the number of holes (indicated) is fixed by Coulomb blockade. The orange frame at the right side indicates the few hole regime [26].

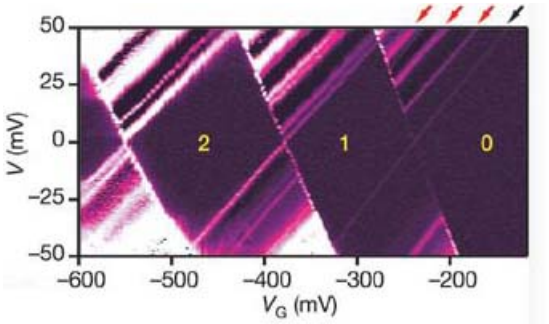


Fig. 3.6.: Few hole regime: Zoom-in, taken at 0.3 K of the region with 0, 1 and 2 holes (black is zero, white is 10 nS). Lines outside the diamonds running parallel to the edges correspond to discrete energy excitations (the black arrow points at the one-hole ground state; the red arrows at the one-hole excited states) [26].

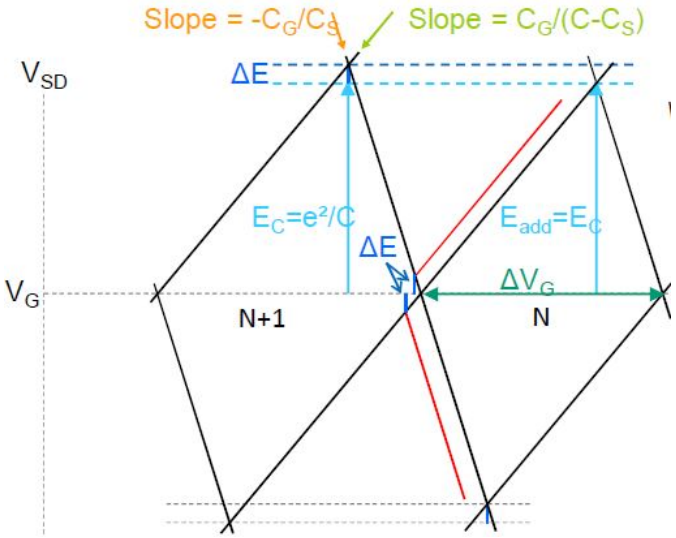


Fig. 3.7.: Schematic representation of a Coulomb diamond for the case of electrons. The addition energy can be extracted from the height of the Coulomb diamond as well as the charging energy, and energy required to fill an additional shell (ΔE). From its slopes the capacitive coupling to the source, drain and gate terminals can be extracted [27].

3.5 Double quantum dot

A single quantum dot system behaves as described in the previous section, when however a second dot is present in the system this behavior changes and the system can be represented electrically as depicted in Figure 3.8. The second dot can be formed intentionally by changing the design or unintentionally by defects in the system, exotic gate designs, bad annealing, lift off or lithography during fabrication. A two or more dot system opens up new area's to research in the areas of spin manipulation and quantum computing.

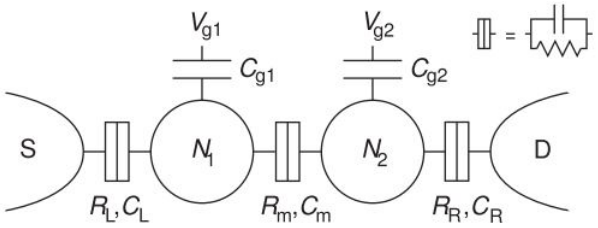


Fig. 3.8.: Schematic representation double quantum dot with tunnel barriers represented as a parallel combination of a capacitor and resistor, and capacitive coupling to the gate. [5].

The constant interaction model used for the single quantum dot structure is also applicable for the double quantum dot structure when one assumes that the cross

capacitances are neglectable. The electrochemical potential of a dot is than described by Equation 3.10[5]:

$$U(N_1, N_2) = [N_1^2 E_{C_1} + N_2^2 E_{C_2}]/2 + N_1 N_2 E_{C_M} + f(V_{G_1}, V_{G_2}), \tag{3.10}$$

Where:

$$\begin{aligned} f(V_{G_1}, V_{G_2}) = &\frac{1}{-|e|}[C_{G_1} V_{G_1}(N_1 E_{C_1} + N_2 E_{C_M}) + C_{G_2} V_{G_2}(N_1 E_{C_M} + N_2 E_{C_2})] \\ &+ \frac{1}{e^2}[(C_{G_1}^2 V_{G_1}^2 E_{C_1})/2 + (C_{G_2}^2 V_{G_2}^2 E_{C_2})/2 + C_{G_1} V_{G_1} C_{G_2} V_{G_2} E_{C_M}] \end{aligned} \tag{3.11}$$

Here $N_{1(2)}, E_{C_{1(2)}}, C_{G_{1(2)}}$ and $V_{G_{1(2)}}$ are the occupation number, charging energy, gate capacitance and gate voltage for the first (second) dot, respectively. E_{C_M} is the coupling energy of one dot when an electron is added to the other dot [5]. These coupling energies between the source, drain and inter-dot can be described in combination with their self capacitance as represented by Equation 3.12. Here the total capacitance is the sum of the capacitances connected to an island, hence $C_1 = C_L + C_{G_1} + C_M$ and $C_2 = C_R + C_{G_2} + C_M$.

$$E_{C_1} = \frac{e^2}{C_1} \frac{1}{1 - \frac{C_M^2}{C_1 C_2}};\ E_{C_2} = \frac{e^2}{C_2} \frac{1}{1 - \frac{C_M^2}{C_1 C_2}};\ E_{C_M} = \frac{e^2}{C_M} \frac{1}{\frac{C_1 C_2}{C_M^2} - 1} \tag{3.12}$$

3.6 Charge stability diagram

The mutual capacitance between the two dots influences the electrochemical potential of the dots and can be described as a weak, intermediate or strong interaction depending on the coupling between the two dots. Whenever the mutual capacitance is low, hence no coupling between the dots $C_M \approx 0$ drops out. Reducing Equation 3.10 into an expression for two single dot energies. This weak coupling between two dots represents itself in a barrier vs. barriers sweep as depicted in Figure 3.9a where oscillations represented by the black lines are coupled to one barrier at a time. When however the mutual capacitance between the two dots is non-zero a double dot system can be observed as depicted in Figure 3.9b where the energy levels of each dot are coupled to both of the dots indicated by the slightly slanted lines.
A high mutual capacitance is expressed by the formation of one big dot equally coupled to both barriers where electrons can tunnel from one dot to another as depicted in Figure 3.9c by the dashed lines. New states become available whenever the gate voltage on one of the gates is increased.
These schematic representations are represented by their electrochemical potentials

as depicted in Equation 3.13 and 3.14. The energy $\mu_{1(2)}$ required to add the $N_{1(2)}$th electron to the dot 1(2) while having $N_{2(1)}$ electrons on the dot 2(1) [5]:

$$\begin{aligned}\mu_1(N_1, N_2) &\equiv U(N_1, N_2) - U(N_1 - 1, N_2) \\ &= (N_1 - 1/2)E_{\mathrm{C_1}} + N_2 E_{\mathrm{C_M}} - (C_{\mathrm{G_1}} V_{\mathrm{G_1}} E_{\mathrm{C_1}} + C_{\mathrm{G_2}} V_{\mathrm{G_2}} E_{\mathrm{C_M}}/|e|)\end{aligned} \tag{3.13}$$

$$\begin{aligned}\mu_2(N_1, N_2) &\equiv U(N_1, N_2) - U(N_1, N_2 - 1) \\ &= (N_2 - 1/2)E_{\mathrm{C_2}} + N_1 E_{\mathrm{C_M}} - (C_{\mathrm{G_1}} V_{\mathrm{G_1}} E_{\mathrm{C_M}} + C_{\mathrm{G_2}} V_{\mathrm{G_2}} E_{\mathrm{C_2}}/|e|)\end{aligned} \tag{3.14}$$

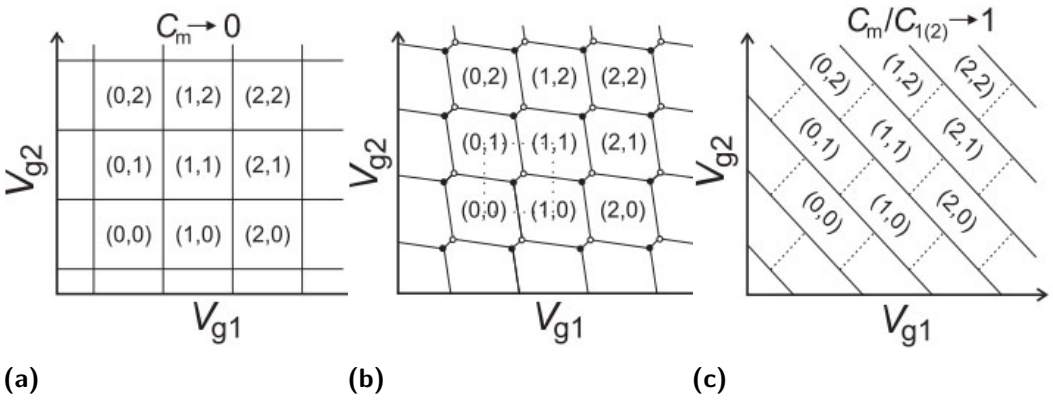


Fig. 3.9.: Schematic charge stability diagram for a double quantum dot system coupled to two gates. a) small, b) intermediate, and c) large inter-dot coupling. Each cell indicates the occupancy of the states, hence (N_1, N_2) [5].

The capacitive coupling from both gates to the dot is given by Equation 3.15 where the coupling of dot 1 to gate 1 and 3 is represented in the case of intermediate or strong coupling. One can rewrite these equations into a single equation describing the ratio of coupling between the dot and both barriers as depicted in Equation 3.16.

$$e = C_{\mathrm{G_3-D_1}} \Delta V_{\mathrm{B_3}}; \qquad e = C_{\mathrm{G_1-D_3}} \Delta V_{\mathrm{B_1}} \tag{3.15}$$

$$\frac{C_{\mathrm{G_1}}}{C_{\mathrm{G_3}}} = \frac{\Delta V_{\mathrm{B_3}}}{\Delta V_{\mathrm{B_1}}} \tag{3.16}$$

3.7 Charge sensing

The constant-interaction model assumes that the total capacitance of the system is constant which can be hold valid when a large amount of electrons or holes are present on the dot. When however this number decreases (N < 10) due to confinements this leads to discrepancies in the model. When only a handful of electrons or holes are left on the dot the Coulomb peaks become embedded into the noise level of the measurement, because the energy associated with these last states (N < 10) are small, limiting the signal to noise ratio. A way to resolve this is to use charge sensing where a second dot is placed in the vicinity of the first to sense electrostatically if a charge transition takes place [28], [29].
Non-invasive charge sensing is an invaluable tool for the study of electron or hole charge and spin states in nanostructured devices. It has been used to identify electron occupancy down to the single electron regime [30], [31] and has made possible the single-shot readout of single electron spins confined in both quantum dots [32].

To be most sensitive the sensor dot is tuned at a place with high transconductance as depicted in Figure 3.10a. Charge sensing can be done in either static or dynamic mode. In static mode the lead is swept through different states on the measured dot while in the sensor dot a slow change in current can be observed with on top the charging/de-charing events in the measured dot as depicted in Figure 3.10b. The downside of this measurement setup is that at a low transconductance, hence a low slope of the dI/dV curve the charge upsets are less clear as depicted in Figure 3.10b.

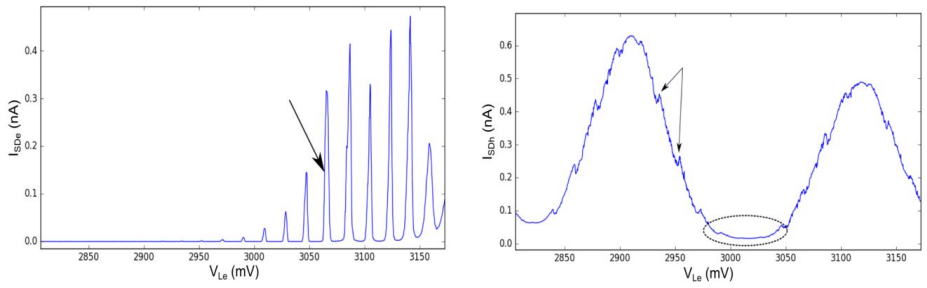


Fig. 3.10.: For the case of electrons. a) Coulomb peaks of a SET as the lead is swept, the arrow indicates example point of high transconductance. b) Example measurement where the charge upsets are visible in the SHT current as the electron lead is swept. Image adopted from F. Bruijnes [20]

A way to resolve this is to use charge sensing with a dynamic feedback loop where the sensor dot is tuned at a place of high transconductance as depicted by the arrow in Figure 3.10a. Here a current $I_{SD} = I_0$ flows and when a charge transition occurs in the measured dot the feedback loop readjusts the sensor dot to its initial position

with high transconductance by changing the sensor dot plunger voltage to pull I_S to its operating point I_0. A plot of the current for both static and dynamic feedback is depicted in Figure 3.11 where it is clear that the the signal to noise ratio in the case of fixed compensation is better than for the uncompensated I_S.
This feedback system can be described by the Equations 3.17 and 3.18 where the parameters used for the feedback system have to be in correspondence with the measured physical properties of the device. [33].

$$V_{SD}[x+1] = V_{SD} - \beta I_{SD} - \Delta V_{MD} A_C[x] \tag{3.17}$$

$$A_C[x+1] = A_C[x] + \frac{\gamma}{\Delta V_{MD}} I_{SD}[x] \tag{3.18}$$

Where ΔV_{SD} is the step size in the gate voltage of the measured dot and $A_C = \frac{C_{MD}}{C_{SD}}$ is the ratio of the capacitance between the gates of the two dots. This value is extracted from a gate versus gate scan. β controls the first order feedback, which governs the decay rate of the error current $I_{SD} - I_0$ and γ controls the decay rate of the A_C back to its steady state value as used by [33].

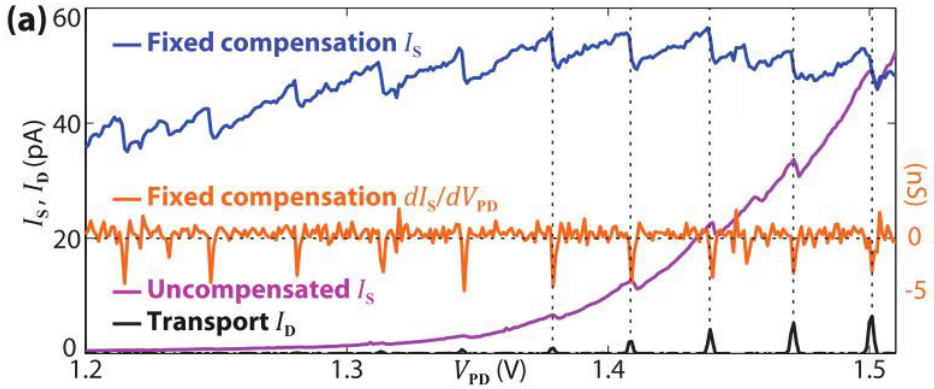


Fig. 3.11.: SET sensor current I_S without compensation (magenta) and dot transport current I_D (black). Fixed compensation is applied by linearly adjusting the sensor gate potential V_{PS} and the compensated I_S (blue) then operates within a fixed range with a corresponding transconductance dI_S/dV_{PD} (orange) [33].

3.8 Fixed charge

The devices in this thesis are based on electrostatically defining a dot in the two-dimensional hole gas (2DHG) between intrinsic silicon and SiO_2 at the interface. The origin of these charges is due to a shielding effect (like a capacitor) of negative charges present at the SiO_2-Al_2O_3 interface as depicted in Figure 3.12a.

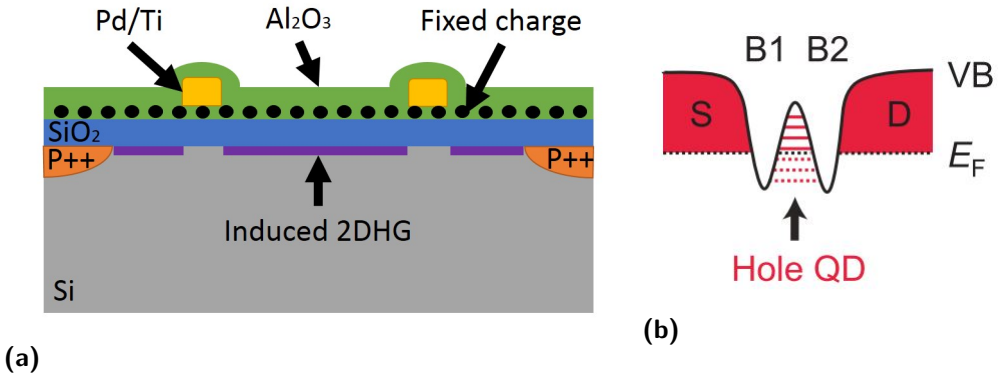


Fig. 3.12.: a) Layout of a sample with a layer stack of Si-SiO_2-Al_2O_3. Fixed charges are represented by closed black circles indicating that they are fixed and unable to move, and two-dimensional hole gas at the Si-SiO_2 interface indicated in purple. The Pd/Ti gates can be used to locally deplete the 2DHG. b) Formation of a quantum dot by the confinement of holes due to a potential on the barriers [22].

In literature several studies can be found with different explanations about the origin of these fixed charges at the SiO_2-Al_2O_3 interface [34], [35]. It could be due to the formation of negatively charged Al-OH bonds as residuals of the ALD process [36] or Al-O- groups, caused by insufficient reaction [37]. It is however expected that during annealing any open bond or oxygen radical will react or will be terminated by hydrogen in case of forming gas treatment [38].

Furthermore Bansall et al. [34] suggest a shift in the ratio between tetrahedrally and octahedrally coordinated Al atoms near the interface due to the formation of aluminum silicate [39]. They support their claim by an electron localized function (ELF) simulation where at the interface there is a decrease in the tetrahedrally coordinated Al atoms and an increase of the average charge on Al atoms indicated by the abundance of O near the interface as depicted in Figure 3.13.

Although charges in our system are usually labeled “fixed charges” some papers report that not all charges are fixed, but some are however mobile. Gielis et al. [40] observed a continuous rise of negative fixed charge during second-harmonic generation (SHG) experiments. This rise in charge is depicted in Figure 3.14a where a laser with an average power of 100 mW is used to induce charge trapping by photons from Si into Al_2O_3. After 61 min the laser was shut off for 32 minutes after which some of the charges became de-trapped indicating recombination. This procedure

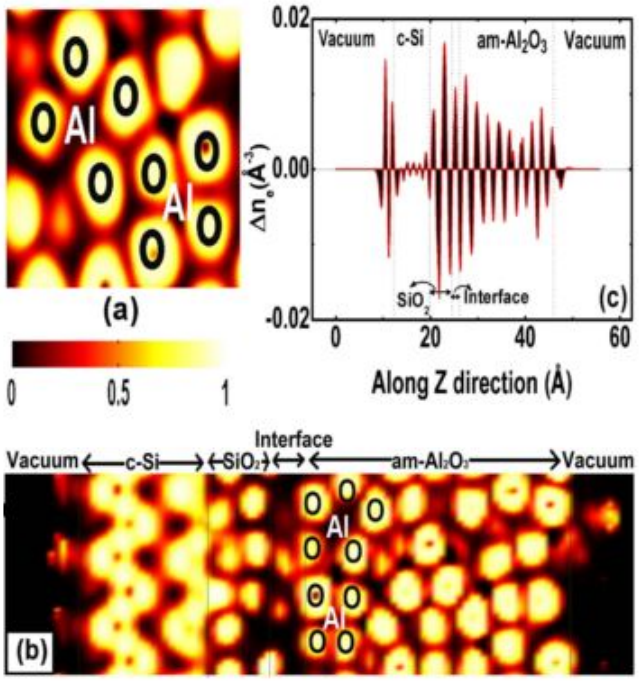


Fig. 3.13.: a) Electron localized function (ELF) of the am-Al_2O_3 structure. (b) ELF of the c-Si-SiO_2-Al_2O_3 structure indicating the coordination of Al and O atoms. (c) Electron difference density for interface along the z-direction [34].

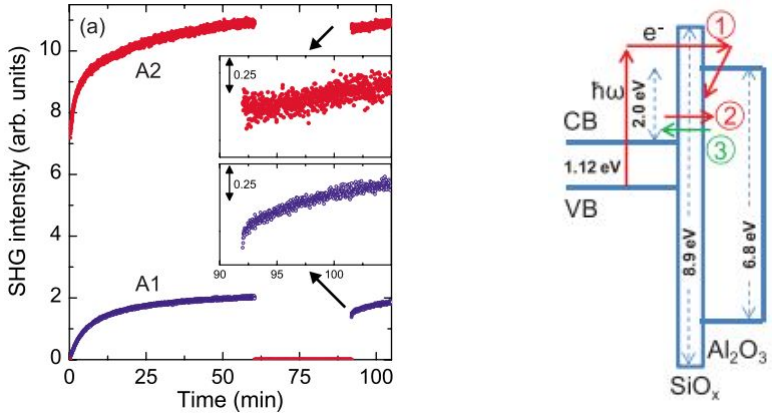
was done both before annealing and with a second sample after 425 °C N_2 annealing showing similar behavior to photon induced charge.

These measurements are supported by Liao et al. [41] who also observed an increase in charge density after illumination of Al_2O_3 with Air Mass 1.5. Air Mass 1.5 is similar to direct sunlight under an angle of 42° with the horizon [42]. While these samples were stored in the dark, charge injection partly reverses and the measured charge density reduced towards the initial value [43].

In order for a photon to form additional charge the generated electron can use two mechanisms to get to the $Al_2O_3 - SiO_2$ interface where they are trapped as depicted in Figure 3.14b:

1. from the valence band of Si into the conduction band of Al_2O_3 and then subsequently diffuse into trap sites located at the $SiO_2 - Al_2O_3$ interface (path 1 in Figure 3.14b).
2. the electron can either tunnel through the SiO_2 layer and then be captured by trap sites located at the $SiO_2 - Al_2O_3$ interface (path 2 in Figure 3.14b)

De-trapping is suspected to take place via recombination of holes and electrons tunneling through the SiO_2 (path 3 in Figure 3.14b).



(a) **(b)**

Fig. 3.14.: a) Time-dependent SHG intensity for 11 nm Al_2O_3 on Si-100 before annealing (blue) and after annealing 425 °C N_2 (red). A fundamental photon energy of 1.71 eV, and an average laser power of 100 mW. Between t=60–92 min the laser beam was blocked. The insets show the SHG intensity during the second period of illumination in greater detail. [40] b) Energy band diagram for $Si - SiO_x - Al_2O_3$ interface. The electron trapping and de-trapping transport are indicated in red and green respectively [41].

4 Simulation

In this chapter the electrostatic model made by using a finite element method (FEM) simulation tool called Comsol Multiphysics 5.1 is discussed. For this simulation the layer stack is build similar to the real device as depicted in Figure 4.1a. Here the substrate layer of silicon is taken as an arbitrary large thickness compared to the other materials similar to the real sample. For the other layers SiO_2, Al_2O_3 and Pd their actual thicknesses are used. Fixed charge present at the boundary between SiO_2 and Al_2O_3 is depicted in black and a ground plate, hence a zero potential is applied to the bottom of the silicon slab. The red plane represents the location of the 2DHG at the Si-SiO_2 interface and is used as a 2D plot plane.
The fixed charge is taken to be $Q_f = -2 * 10^{12}$ cm^{-2} $= -3.2$ mC m^{-2} [44]. For all other parameters the standard values Comsol provides out of the material library are used.

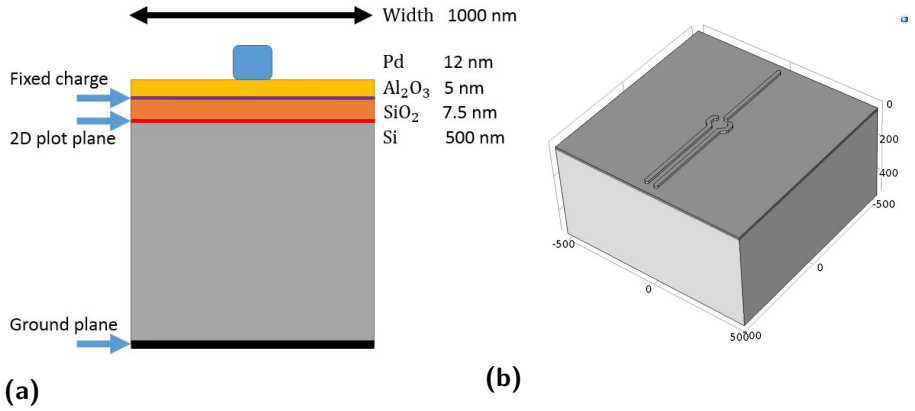
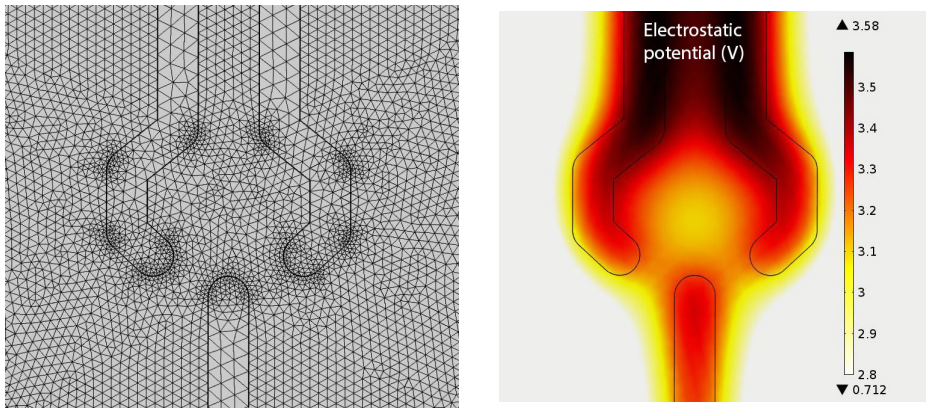


Fig. 4.1.: a) Layer stack for the finite element method simulation in Comsol Multiphysics, the substrate layer of Silicon is taken as an arbitrary large thickness compared to the other materials similar to the real device. SiO_2, Al_2O_3 and Pd represent actual thicknesses measured for the devices. Fixed charge present at the boundary between SiO_2 and Al_2O_3 is depicted in purple and a ground plate is added as a reference at the bottom. The red plane represents the location of the 2DHG at the Si-SiO_2 interface. b) Isometric representation of the Comsol model build with the dimensions in nm and gates on top.

Definition of the gate electrodes can be done by hand in Comsol or by importing a .GDS file which is commonly used for layout editing tools such as KLayout. A .GDS layout file from KLayout can be imported via the Geometry import drop down menu in Comsol by selecting the ECAD file (.GDS) as depicted in Figure A.2 in Appendix

A.3. For a 3D simulation setup in Comsol the layer has to become 3D by setting the type of import to 'full 3D' while additionally its thickness has to be chosen. To ease selection of gates a 'Cumulative Selection 1' can be created from a single import, without this cumulative selection all boundaries (top,bottom and sides etc.) of the gate have to be selected manually.
The use of the cumulative selection function removes the possibility to apply different gate voltages to different gates out of the same .GDS file. The most suitable solution found so far is to split the gates in multiple .GDS files using the same layer and a second import feature in Comsol. If the import function return an error, removing all excess layers out of the .GDS file might pose a solution.
When the gates are imported a potential of 5 V is applied to all barrier gates and the electrostatic potential at the red interface, hence $Si-SiO_2$ interface can be simulated. For the simulation an extremely fine mesh is used as depicted in Figure 4.1b resulting in a computational time of three minutes (i7-3630QM @ 2.40 GHz). The ability to be able to change and simulate the effect of different gate designs poses a powerful and versatile tool for further research.
Besides the capability of importing .GDS files, additionally an AFM scan can be imported to get an indication about the actual gate performance of the fabricated device as discussed in Appendix A.3.
Multilayer design is possible but it poses difficulties in correct covering of complex 3D topologies. Besides this, a second layer to accumulate charges is found to be limited by the in real life dielectric layer of devices rather than the layout.



(a) **(b)**

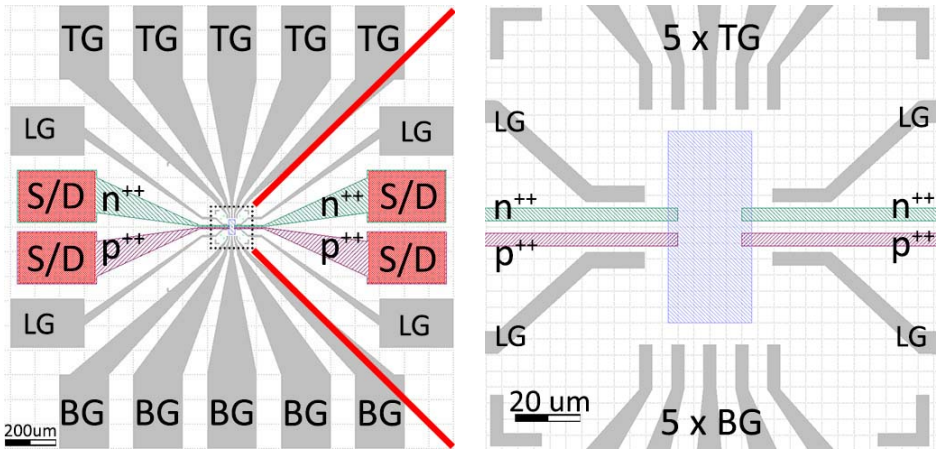
Fig. 4.2.: a) Extra fine mesh used for the simulation. b) Slice of the electric potential at the location depicted in Figure 4.1a as "2D plot plane". A thermalequidistant colorplot is used with the formation of the dot clearly visible between the barrier hands.

5 Device layout

In this section the layout of the samples that were fabricated in this thesis will be discussed. It starts with the difference between microscale and nanoscale devices and continues to discuss the way the design iterated during the course of this thesis.

5.1 Microscale device

The macroscale device is used as a starting point for all nanoscale devices with its layout depicted in Figure 5.1. By using this microscale standard design big structures can be patterned with photo-lithography while small nanoscale features connecting to these contact pads can be written with Electron Beam Lithography (EBL). This cooperation of two lithography techniques increases process speed. A total of five bottom/top gates (BG/TG) and four lead gate (LG) contacts pads are available to be used as a break out connection for the nanoscale devices. The starting point for the EBL lithography can be seen in Figure 5.1b where the p^{++} and n^{++} implanted regions act as a charge reservoir for holes and electrons.



(a) (b)

Fig. 5.1.: a) Overview of the microscale device fabricated with photo-lithography, the bottom S/D channel p^{++} doped, and the top S/D n^{++} doped. b) Zoom in of the area indicated figure (a) by the dotted lines where the nanoscale device is fabricated by using EBL. The top, bottom and lead gates are depicted as TG, BG and LG respectively.

5.2 Ten gate depletion dot

As a start of the depletion dot topic ten fingered gated nanostructes with a pitch of 70 nm between the barriers and 50 between the plungers are designed. by making use of five top and bottom barriers made from 15 nm of Pd in a single layer as depicted in Figure 5.2a. By tuning the voltages on the barriers, area's can be depleted allowing for the formation of a dot between two barriers with a third to act as a plunger as depicted in Figure 5.2b. Two lead gates (LG) were incorporated to allow accumulation of holes to the active region of the depletion dot. The small lines indicate single pixel lines and are used with the EBL machine to reach minimal feature size.

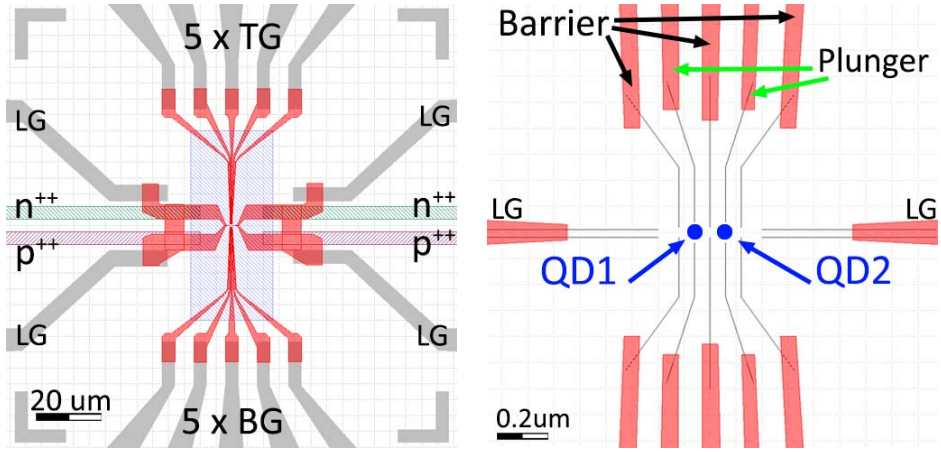


Fig. 5.2.: a) Ten fingered depletion dot design with lead gates to ease hole transport to and from the quantum dot. b) Zoom in of the double quantum dot structure where the outer and middle barriers act as tunnel barriers while the 2nd and 4th barrier act as plungers for the dots. The small lines indicate single pixel lines.

5.3 Ciorga design

A design proven to work for the few electron regime in a GaAs layer stack is adopted from Ciorga et al. [45] as shown in Figure 5.3b. The design makes use of two big barriers (B1 and B3) highly coupled to the dot and a bottom gate electrode to define the barriers. A plunger is spaced in between B1 and B3 to adjust the electrochemical potential on the dot without changing the resistance of the tunnel barriers. The main idea behind the Ciorga design is that a bean shaped like quantum dot is formed around the bottom barrier. This shape should allow tunneling of holes on or off the dot even when it decreases in size.

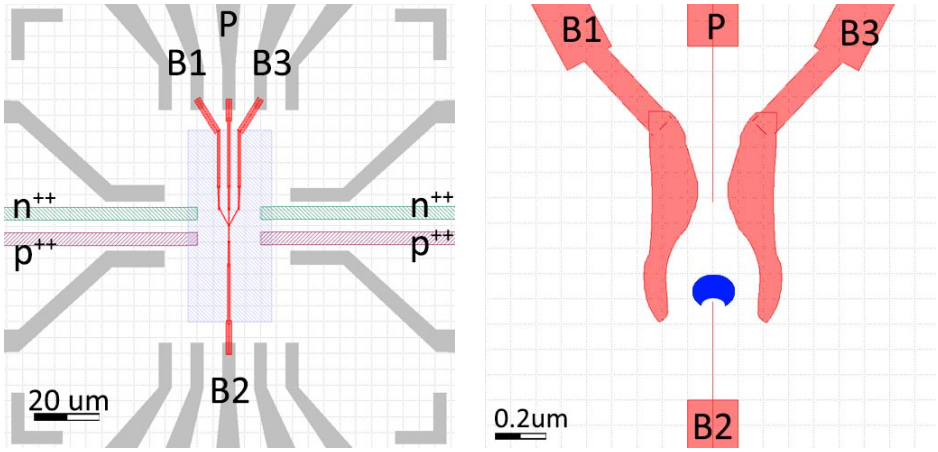


Fig. 5.3.: Single layer Ciorga depletion dot design. a) General layout with gate connections indicated. b) Zoom in on the location of interest with SET indicated in blue and single pixel lines visible as plunger and bottom gate electrode.

5.4 Single hole and single electron dot

As an alternative on the Ciorga design [45] and due to the proof of concept with the ten gated device a double layer device is made to be able to apply charge sensing to the depletion dot by using a SET. This SET will be induced by the second layer lead gate and makes use of the two top barriers. Additionally two bottom barriers and one plunger gate are used to define the depletion hole dot as depicted in Figure 5.4.

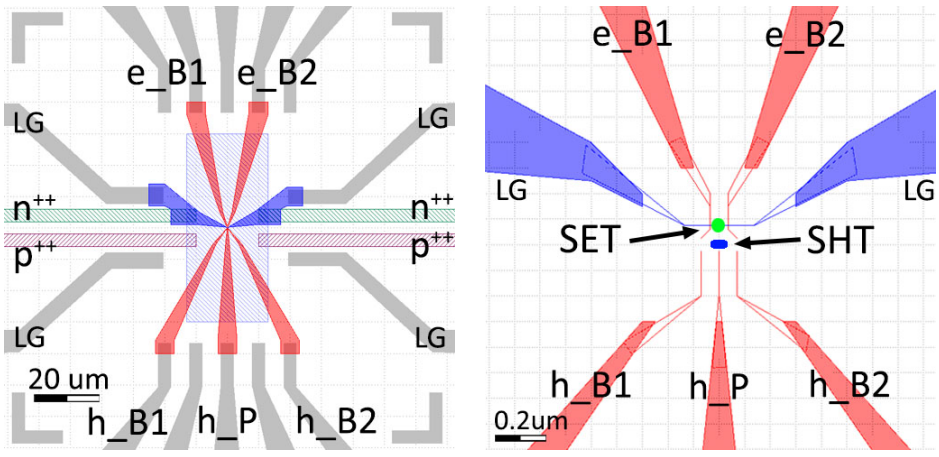


Fig. 5.4.: Two layer depletion dot design with first layer in red with 15 nm palladium gates and second layer 25 nm palladium lead gate. a) General layout with gate connections indicated. b) Zoom in on the location of interest with SET and SHT indicated.

5.4.1 Minimal Design single hole and single electron dot

As a combination the Ciorga design and the previous double layer design are combined into a minimal design as depicted in Figure 5.5b. It makes use of a lead gate to accumulate electrons from the n^{++} regions to the SET where B1 and B3 are used to define the electron dot. The depletion hole dot is than tuned into place by making use of a combination of all barriers. This device should allow for both transport measurements as well as charge sensing to be able to reach the single or few hole regime.

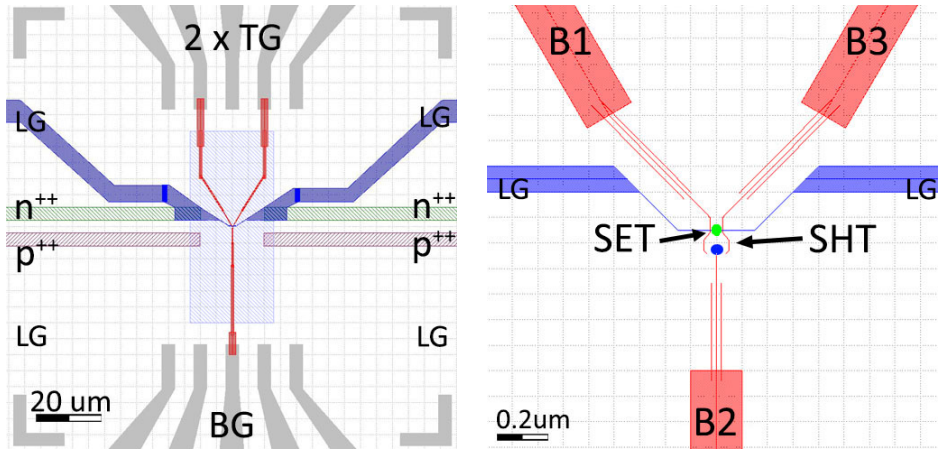


Fig. 5.5.: Double layer depletion dot and single electron transistor design. a) General layout with gate connections indicated. b) Zoom in where both the depletion dot in blue and electron dot in green are indicated. Note that the single pixel lines have become triple pixel lines to broaden the gate in some regions.

6 Experimental methods

The samples in this thesis were fabricated in the MESA+ Nanolab Facility at the University of Twente. The most important steps along with the experimental setup will be discussed.

6.1 Electron beam lithography

Electron beam lithography (EBL) is a technique that uses the beam of a scanning electron microscope with a certain energy, typically 10 to 100 keV for the exposure of resist. The most common positive resist is polymethyl methacrylate, or polymethyl-2-methylpropanoate (PMMA). In positive resists chemical bonds are cracked by the impinging electrons making the exposed region more soluble. In negative resists exposure leads to a strong cross-linking of the molecules and as a result to a lower solubility. The advantage of using an EBL machine is that no mask is required due to the ability to write structures by precise control of the beam. The EBL machine used in the MESA+ cleanroom is the Raith 150-TWO. After exposure the PMMA is developed in an isopropyl alcohol-water (IPA-water) solution of a ratio of 1:10 for one minute or alternatively by using so called cold development.

6.2 Cold development

To reach even smaller feature sizes, higher acceleration voltages, thinner resist and cold development can be used. A higher acceleration voltage leaves a more direct imprint in PMMA due to a decrease in the spread of the backscattered electrons that can overexpose neighboring resist. Additionally a thinner layer of resist will leave a more direct imprint on the sample due to an improvement in aspect ratio. Furthermore, cold development has been shown to improve the EBL resolution and line roughness by using Methyl IsoButyl Ketone (MIBK) with an optimal temperature of approximately -15 °C [46],[47].
A possible downside of using cold development is that development of multiple samples after on another yields different results due to the rapid warm-up of the developer in the cleanroom environment. Secondly if the sample is not properly blow dried afterwards the PMMA starts to overdevelop.

6.3 Metal deposition

The pattern written into PMMA is transfered into metal by evaporation of palladium (Pd) or titanium (Ti). The evaporation of a metal layer is generally done by using the BIOS evaporator were the system is pumped down to vacuum after which a Pd/Ti source is heated with an e-gun to start evaporating. This metal layer is used to define the gates on top of the sample and is usually in the order of tens of nanometers.

6.4 Lift off

After metal has been evaporated, the excess on top of the PMMA is removed by using a lift off procedure. A beaker filled with dimethylsulfoxide (DMSO) as a solvent for the PMMA is placed in an ultrasonic bath and heated to 80 °C. Ultrasonic power can be used moderately to enhance the lift of process when required.

6.5 UV ozone

For the exposure of a device to Ultraviolet (UV) radiation and Ozone (O_3) the PR-100 UV-ozone photo-reactor was used for exposure of samples as depicted in Figure A.1a. To expose a sample to ozone but not to UV an improvised aluminum "roof" can be used as depicted in Figure A.1b in Appendix A.1. Before each exposure a 5 min warm-up of the lamp is performed to make sure exposure in orders of seconds behaves the same as minutes.

6.6 Experimental setup

In this subsection the experimental setup used for the electrical characterizations of the devices at low temperatures will be discussed in detail.

6.6.1 Measurement preparation

After a sample is taken out of the cleanroom it is glued to the PCB by using PMMA/copolymer and a hotplate at 80 °C for 30 minutes to evaporate solvents. After gluing, the contact pads of the chip are wire bonded to the channels on the PCB allowing for a total of 22 interconnects between the sample and the measurement setup. This is done by using the ultrasonic power of the the wire bonder (WestBond 7476E Wedge-Wedge Wire bonder) to "weld" aluminum wires to both the sample and the PCB. The channels on the PCB can than be connected to the measurement setup and individually addressed by putting the connector into the zero insertion force (ZIF) socket. This PCB can be reused by cleaning it with acetone to dissolve the PMMA after which it is rinsed with IPA and blow dried with a nitrogen gun.

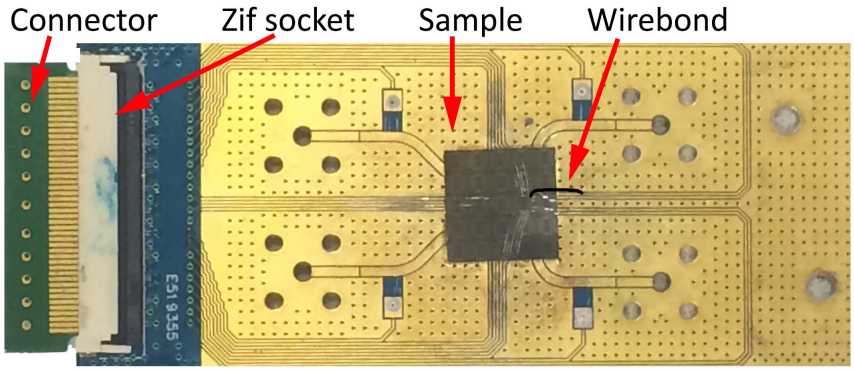


Fig. 6.1.: Custom PCB with 22 break out connections that can be wire bonded to the connections in the ZIF socket. A so called grounding connector shorts all pins to avoid static discharge by keeping them at the same potential. The sample is glued to the PCB by using PMMA.

6.6.2 Dipstick

After the sample has been glued to the PCB it can be loaded into one of the low-temperature setups. Firstly the sample is loaded into the so called "Dipstick" where the PCB is mounted with screws on the end of a long movable rod (Figure 6.2a) after which it is loaded into the liquid helium dewar (Figure 6.2b). The movable rod can be pushed through the lid of the dewar and thereby be lowered into the liquid helium. The benefit of using this setup is that loading and unloading of a sample can

be done within half an hour. The downside is that it goes down to 4.2 K whereas other cryogenic setups are able to reach lower temperatures

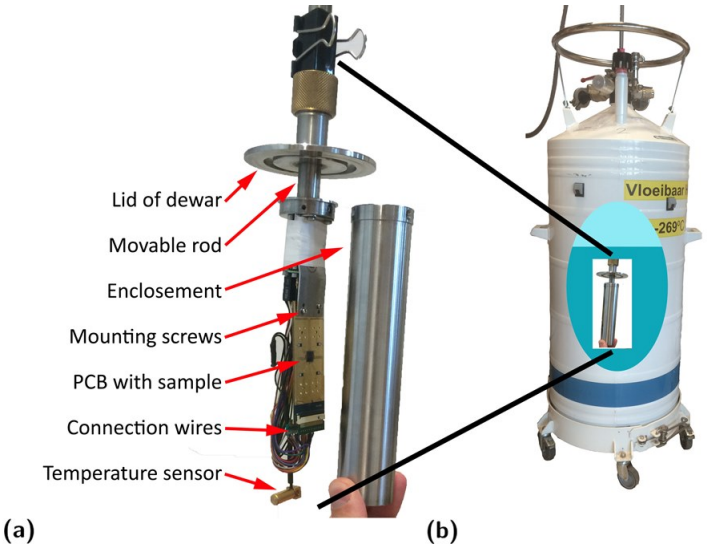


Fig. 6.2.: a) Image of the end of the dipstick where the PCB is mounted with screws and connected with the use of a ZIF connector. The temperature sensor below the sample is used to ensure that the sample is immersed into the liquid helium. b) 100 liter liquid helium dewar into which the sample is immersed to let it cool down to a temperature of 4.2 K.

6.6.3 Heliox

For samples that show good characteristics at 4.2 K temperatures can be decreased even further to decrease the amount of thermal energy ($k_B\ T$) present in the system by using the Oxford Heliox Helium3 fridge which is able to go down to 250 mK. A decrease of thermal energy makes electrical transport phenomena more prominent and enables lower currents to be measured due to the decrease of thermal noise in the system. Additionally a vector magnet is present which can be used to apply a magnetic field to measure effects like Zeeman splitting.

6.6.4 Source Measure Unit/ beeper

To apply a voltage on the gates the source measure unit (SMU) can be used. The SMU can be set to limit the current while applying a voltage to keep the current low and thereby the device alive. The SMU is mostly used for turn on/pinch off measurements in combination with the Beep-R, a custom build device that measures channel resistance. The general advantage of using the SMU and the beeper is that setup is relatively easy and it allows for testing of leakages in the system before controlled measurements are done with the IV/VI rack is possible. The drawback is

that it lacks flexibility in applying different potentials to different gates. It is a fast method to get an indication about which devices can be promising.

6.6.5 IV/VI

The connections wire bonded to the PCB are directly connected to the pins on the so called IV/VI rack, as depicted in Figure 6.3. This rack is custom-built at the Delft university and consists of digital to analogue converters (DAC), multiple measurement, source and routing modules. The setup is controlled from a computer running QTlab software connected by an optical fiber connection and is battery powered to reduce noise from the power grid. Additionally, current measure, voltage source amplifying and summing modules are used and read out is done by using multimeter's connected to the computer via General Purpose Interface Bus (GPIB). The advantage of using the IV/VI rack is that all DACs and thereby hence gates/barriers can be controlled individually and that actual measurements can be done precisely and stored onto the computer.

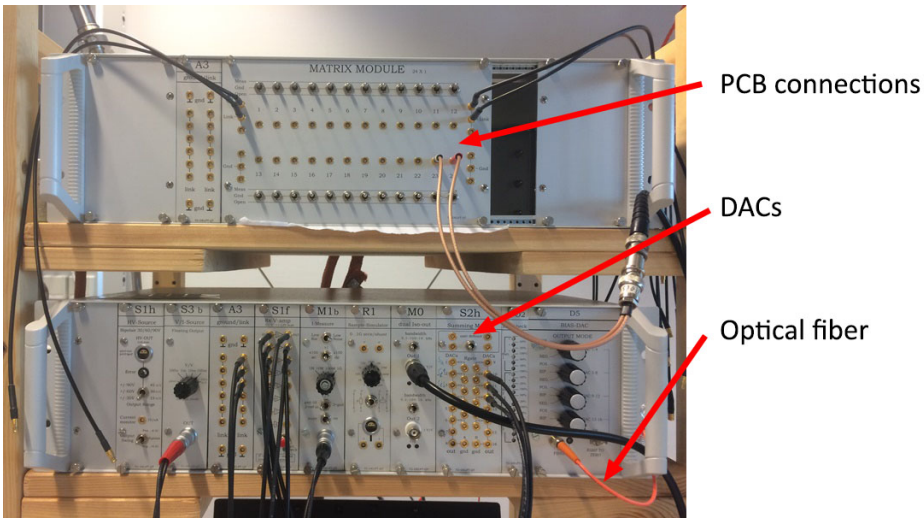


Fig. 6.3.: IVVI rack with on to the matrix module allowing to individually address each pin and to be able to ground, connect and open them. Below the measurement module connected to the PC by an optical fiber connection, and operated from batteries to prevent noise from the grid.

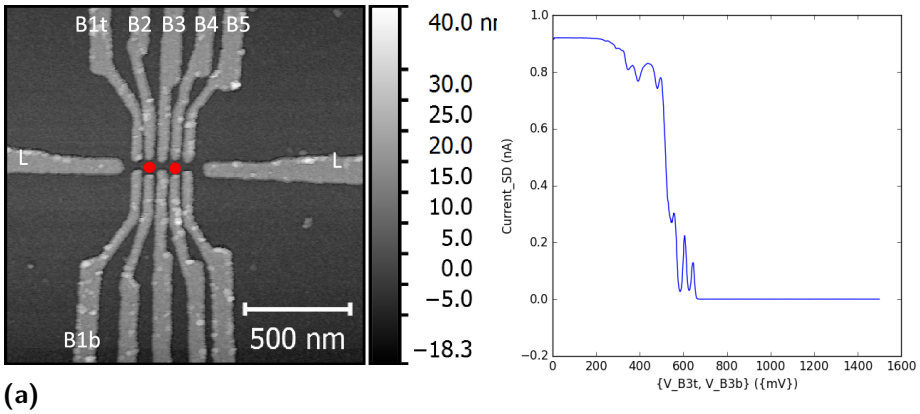
7 Results

In this chapter the results from the electrical characterization of the fabricated devices are discussed. Based on these results multiple device iterations were made with design specifications as described in the device layout section. Lastly a brief look is taken into manipulation of fixed charge in the system by making use of the UV-ozone photo-reactor, and the possible implementation of titanium gate electrodes is discussed.
It is important to note that the samples were annealed at different temperatures ranging between 350 and 500 °C in different combinations of gases involving N_2, Ar and H_2. Additionally gates are indicated by letters: B indicates a barrier, L indicates a lead gate and P indicates a plunger. Numbers are added when multiple barriers are in use.

7.1 Ten gate depletion dot

As a proof of concept a double dot design was realized by making use of ten gates as depicted in Figure 7.1a to deplete the 2DHG at the $Si - SiO_2$ interface [48]. The lead gates (LG) can be used to accumulate holes to the structure from the highly doped p^{++} regions by applying a negative voltage.

To form a depletion dot, firstly both top and bottom barrier finger gates are used to pinch the source-drain channel. A typical pinch-off curve can be seen in Figure 7.1b for the left top (B3t) and left bottom (B3b) barriers. This measurement is repeated for all top and bottom barrier combinations where the formation of a single dot between B1 and B3 was found to be most optimal with B2 to act as a plunger gate. By parking the plunger gate (B2) on a voltage just before pinch off, one makes sure that the dot is formed between the ends of the top and bottom barrier as depicted in Figure 7.1a (red dots). The barriers (B1 and B3) are swept around their pinch off regime, hence 300-700 mV (B3) and 700-1100 mV (B1) to form a dot as depicted in Figure 7.2a. The formation of a dot is visible by the diagonal lines, and additionally a resonance coupled to B1 can be seen at 1020 mV. By making a top vs. bottom barrier scan it can be seen where this unintentional resonance coupled to B1 is most pronounced. The initial sweep ratio of B1t and B1b is indicated by the blue line in Figure 7.3a and is moved around the defect by applying an offset of 150 mV to

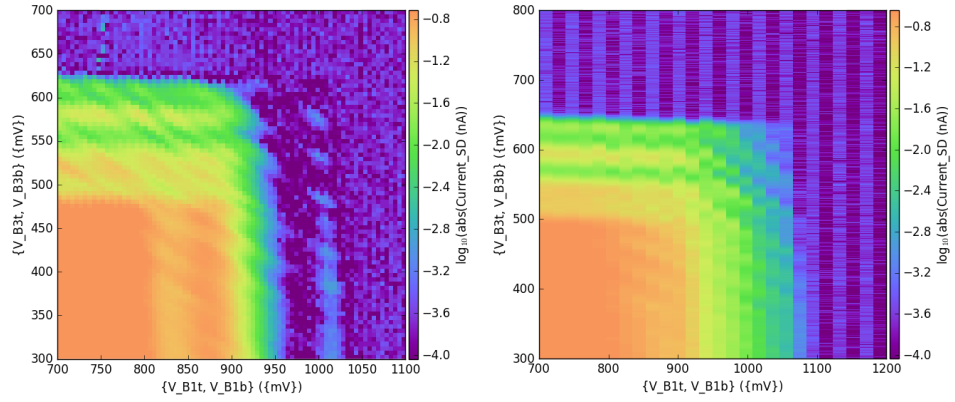


(a) (b)

Fig. 7.1.: a) Typical AFM image of the ten gated depletion dot design with 15 nm palladium gates. Here B1,B2,B3,B4 and B5 indicate the barriers where a 't' or 'b' is added to indicate top and bottom barriers respectively. L indicates the lead gate. b) Pinch off graph for B3. Resonances around pinch off at 600 mV could be due to the formation of an unintentional dot between both barriers or a defect in the lattice. *Here* $V_{SD} = 1$ *mV,* $B2 = B3 = B4 = B5 = 0$ *mV.*

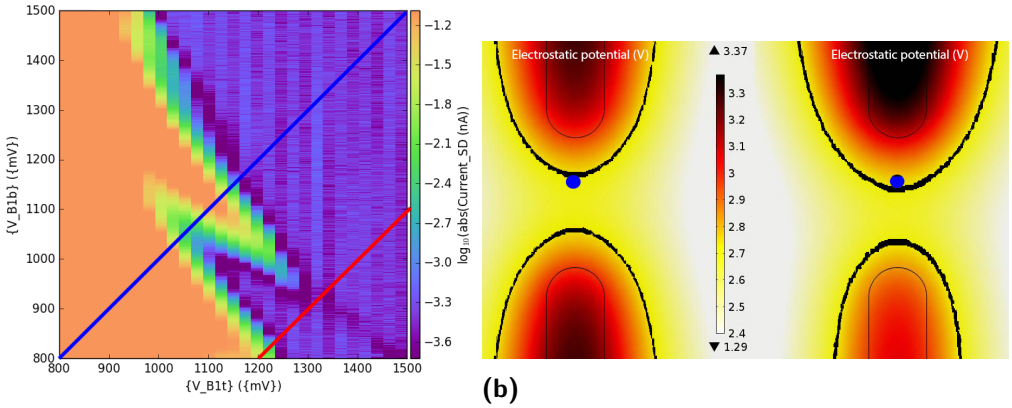
B1t as indicated by the red line. Additionally this shift can be visualized with a simulation of the electrostatic field where the blue dot represents the defect and black lines are used as a guide to the eye to indicate the shift in field as depicted in Figure 7.3b. A defect can be a dangling bond, lattice defect or interstitial, and can be decoupled as indicated in Figure 7.2b where the dot behavior is less because gate space was not optimized and a low resolution scan is made.

The lead gate incorporated into this design turned out to be not required for the formation of a depletion dot indicating that a proper 2DHG is present in the system and no additional bias is required to accumulate holes.



(a) (b)

Fig. 7.2.: a) Quantum dot formed between B1 and B3 indicated by the diagonal lines. A resonance coupled to B1 can be seen around 1020 mV. *Here* $V_{SD} = 0.4$ *mV,* $B2 = 100$ *mV,* $B4 = B5 = 0$ *mV.* b) Quantum dot formed between B1 and B3 where the resonance (a) is decoupled by sweeping B1b and B1t-150 mV. *Here* $V_{SD} = 0.4$ *mV,* $B2 = 100$ *mV,* $B4 = B5 = 0$ *mV.*



(a) (b)

Fig. 7.3.: a) B1b vs. B1t scan with in blue the original B1t and B1b scan ratio, and depicted in red the adjusted ratio to tune around the defect. *Here* $V_{SD} = 0.4$ *mV,* $B2 = B3 = B4 = B5 = -200$ *mV.* b) Color plot of the electric potential (V) in a Comsol simulation with a defect indicated as a blue dot, and black guides to the eye to indicate tuning around a defect.

7.2 Electron accumulation and hole depletion dot

As discussed in the theory section, charge sensing is a powerful tool for measuring down to the few or even single hole regime. For this purpose a double layer device is fabricated with a second layer lead gate to accumulate electrons for the single-electron dot between both top barriers to act as a sensor dot, recall Figure 5.4b. For the depletion dot an additional set of bottom barriers in incorporated, and a plunger gate is used to tune the electrochemical potential of the depletion dot without changing the tunnel barriers.

A typical AFM image of the first write test is depicted in Figure 7.4a where it can be seen that the bottom center barrier is a bit wider than the other two due to proximity effect of the EBL. Furthermore the two fingers at the top are slightly close to one another, leaving a small region available for the SET.

Firstly an electron dot is defined by accumulating electrons from the n^{++} regions by using the lead gate with approximately 3.0 V, and the two top barrier gates (e_B1 and e_B2). An approximate 1.4 V is required for the electron barriers at 3.0 V lead gate voltage which lowers when the lead voltage increases as also clear from the oscillations to the lead vs. barrier scan in Figure 7.4d. This indicates that the lead gate can be used to tune the barrier voltages in correspondence with both the electron and hole dot simultaneously. A main requirement is a good dielectric between the first and second layer to allow high voltages on the lead gate without leakage.

After defining the SET, secondly a hole dot is formed with initial starting conditions as indicated by the black dot as depicted in Figure 7.4c. The performance of this device was however limited since h_B1 was broken, so a depletion dot without a

plunger is formed between h_B2 and h_P as depicted in Figure 7.4b. Resonances of a performance limited intentional dot can be seen devoted to both the design, small region for the SET and the formation of the depletion dot with the plunger gate as a barrier.

Due to the limited performance of both dots charge sensing is not implemented and device iteration continues. It is however demonstrated that an electron accumulation and hole depletion can be formed simultaneously in gate space within the same device.

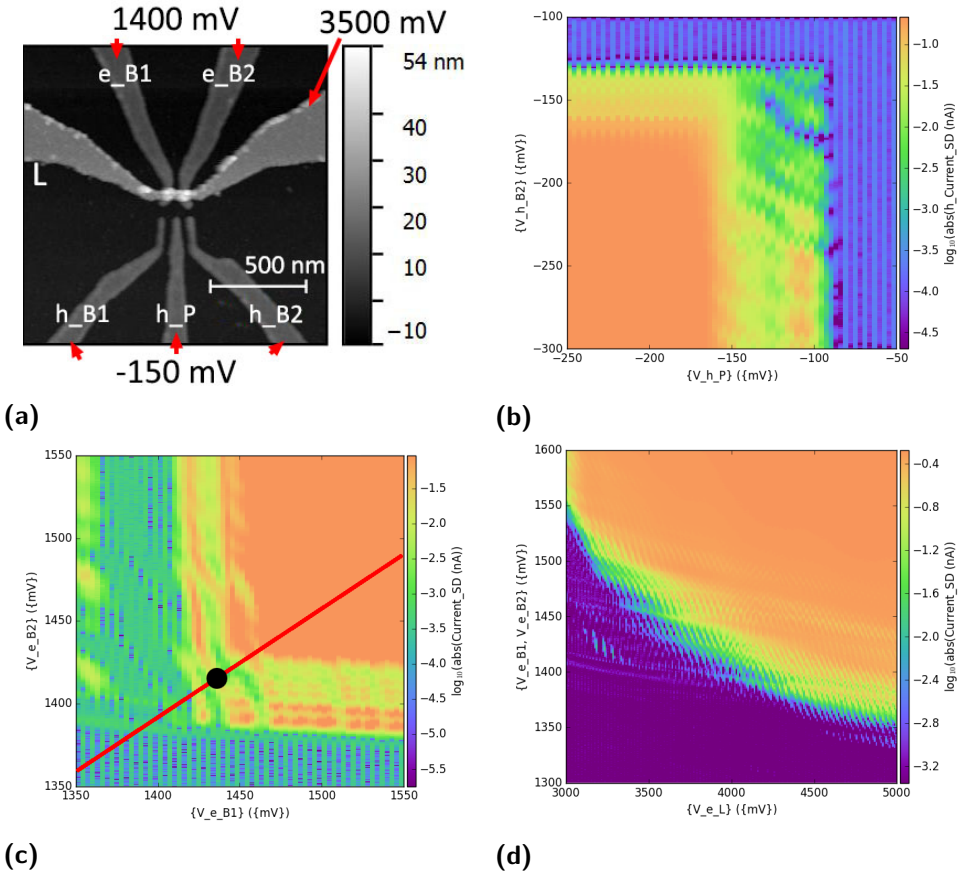
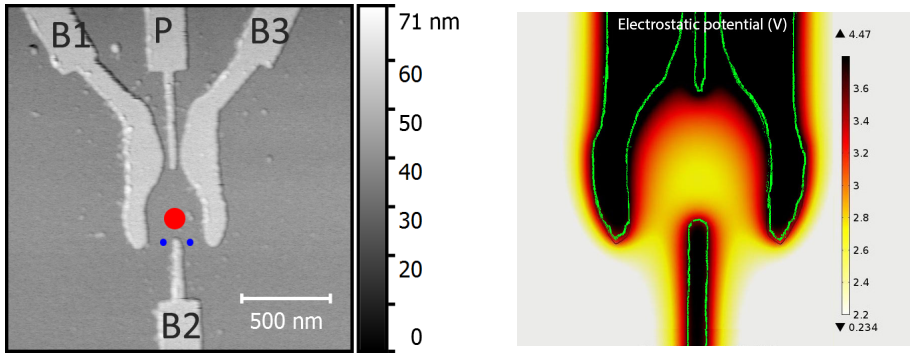


Fig. 7.4.: a) AFM image of the first and second layer with voltages to indicate the operating regime and barriers indicated.
b) Hole dot formed with electron leads at the parking spot at the black dot in (c). *Here* $V_{SD} = 0.4$ *mV,* $e\_B1 = 1440$ *mV,* $e\_B2 = 1410$ *mV,* $L = 3650$ *mV,* $h\_B1 = -500$ *mV.*
c) Electron dot formed between e_B1 and e_B2. The red line indicates the ratio e_B1 and e_B2 for the scan in (d) and the black dot shows the parking spot for the scan in Figure (b). *Here* $V_{SD} = 0.4$ *mV,* $h\_B1 = 0$ *mV,* $h\_B2 = 0$ *mV,* $h\_P = 0$ *mV,* $L = 3650$ *mV.*
d) Lead vs. e_B1&e_B2 scan where the most optimal location for the lead can be found by looking at the resonance peaks. *Here* $V_{SD} = 0.4$ *mV,* $h\_B1 = 0$ *mV,* $h\_B2 = 0$ *mV,* $h\_P = 0$ *mV.*

7.3 Ciorga design

As it turned out from the first two generation of devices a slightly different approach might improve the behavior of the depletion dot, after which charge sensing could be implemented into the design. As an advantage only a single layer device has to be fabricated to define a depletion dot allowing faster fabrication and thereby device iterations. A design proven to be capable of reaching the single-electron regime in a GaAs structure was adapted from Ciorga et al. [45]. The main difference is that Ciorga used a GaAs stack which has a lower effective mass allowing for a bigger spacing between energy states making them easier to probe.
A typical AFM scan of the Ciorga design is depicted in Figure 7.5a where the colored dots can be ignored for the moment. The formation of a quantum dot by the Ciorga design made from palladium can be seen in Figure 7.6a where clear resonances coupled equally to both barrier B1 and B3 are visible as depicted by the black line. On top of the intentional quantum dot the behavior of two unintentional dots coupled each to one of the barriers can be seen as indicated by the red and white lines.



(a) (b)

Fig. 7.5.: a) AFM scan after metal lift off with in red the intentional dot and in blue two unintentional dots depicted, and gates indicated. b) Comsol simulation with the Ciorga gate design as shown in (a) and the color-plot indicating the amount of fixed charge at the 2DHG layer noted in electric potential (V). The shape of the gate electrodes is indicated in green.

The capacitive coupling of these unintentional dots to the barriers can be extracted to get a quantitative indication of the location of these dots. For this, the constant interaction model is hold valid with Equation 3.15 and 3.16 to describe mutual capacitances between the barriers.
When extracted out of the B1 vs. B3 scan: C_{g1}/C_{g3}=2.74 indicating that dot 1 couples 2.74 times stronger to B1 than B3, and vise versa for dot 3: C_{g3}/C_{g1} = 2.92 with B2=1100 mV. By changing the potential on B2 the tunnel barriers move in the 2DHG and thereby the location of the unintentional dots coupled to B1 and B3. With B2=3000 mV the dots tend to move further from B2 and closer to B1

and B3 as indicated by the coupling ratio's being respectively: C_{g1}/C_{g3}=6.36 and C_{g3}/C_{g1} = 6.43, thereby shifting them a factor of 2.8 closer to the big barriers. It is noted from these numbers that coupling to both gates is highly symmetrical which can be explained due to the well defined symmetrical gate structures. To see whether these unintentional dots form in complete gate space or between two barriers, a B3 vs. B2 scan is made as depicted in Figure 7.7. From this no optimal position for both barriers could be found since unintentional resonances stays present as more clear in the close-up. The expected location of both the intentional and unintentional dots are depicted in the AFM scan in Figure 7.5a as red and blue dots respectively.

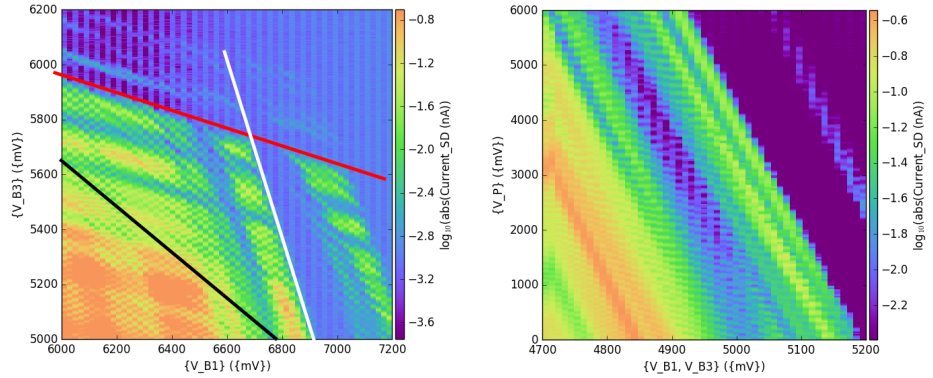


Fig. 7.6.: a) B1 vs. B3 plot where the formation of the intentional quantum dot can be seen by the diagonal lines indicated by the blue line with on top unintentional quantum dots forming coupled unequally to B1 and B3 as indicated by the red and white lines. *Here* $V_{SD} = 0.4$ *mV,* $B2 = 1100$ *mV,* $P = 4000$ *mV.* b) B1&B3 vs. P plot in which it can be seen that the dot couples weakly to the plunger compared to the barriers. *Here* $V_{SD} = 0.4$ *mV,* $B2 = 2250$ *mV.*

In Figure 7.8 it can be seen that the coupling between the plunger and B1 and B3 is a factor of 24, indicating that the plunger is lowly coupled to the dot and the barriers highly. This can be explained by the fact that the plunger is relatively small and far away from the dot as compared to the barriers B1 and B3.

As discussed in the theory section a bias spectroscopy can be made where the voltage on the plunger or in this case B1 and B3 is increased to deplete the dot due to the low coupling of the plunger to the dot. At a first glance it can be seen that the charging energy of the dot increases overall which can be attributed to shrinking of the dot and thereby a larger capacitance. On top of this an alternating pattern as an envelope around the diamonds is visible indicating additional coupling of the main dot to another secondary dot as is most probable due to the unintentional dots forming between B1 and B2, and B3 and B2, or a defect nearby. When looked at the shape of the diamond it is clear that it is slightly slanted indicating unequal coupling of the main dot to the source and the drain.

A possible solution for the unintentional dots might be found when a look is taken at the Comsol simulation where a possible solution might be moving the bottom barrier down to decrease overlap between barriers, thereby decreasing the space for an unintentional dot to form. This device was fabricated but showed however similar behavior. It was therefore concluded that the Ciorga design was too big for good pinch off also indicated by the high pinch off voltages (>5 V). Leading the device onwards to devices with a smaller pitch and minimal structural design.

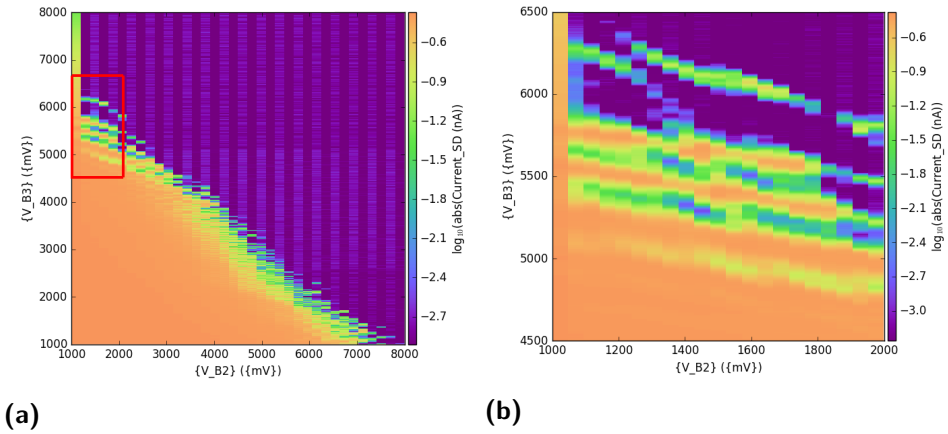


Fig. 7.7.: a) B2 vs. B3 plot with many resonances visible from the unintentional dot forming between B2 and B3. *Here* $V_{SD} = 0.4$ *mV,* $B1 = 500$ *mV,* $P = 500$ *mV.* b) Higher resolution plot of the left top area of (a). *Here* $V_{SD} = 0.4$ *mV,* $B1 = 0$ *mV,* $P = 0$ *mV.*

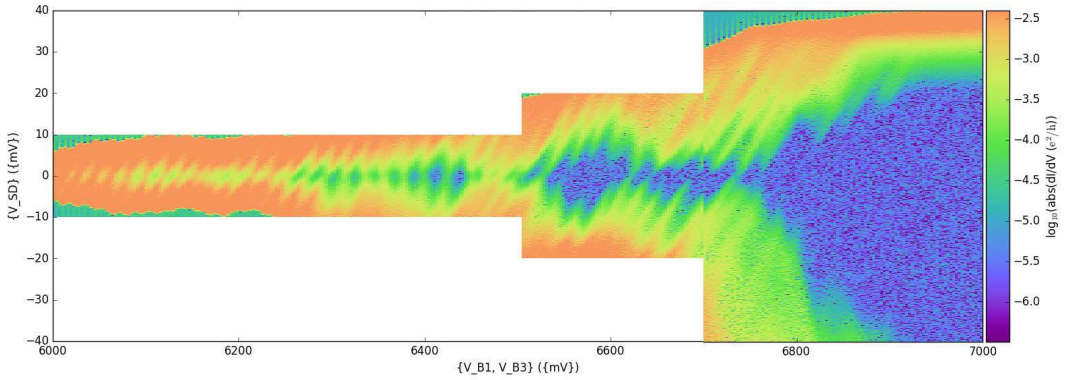


Fig. 7.8.: Combination of three bias spectroscopies with different source-drain bias voltages. Resonances on top of the dot in the form of an envelope can be seen attributed to the unintentional dots. *Here* $B2 = 1100$ *mV,* $P = 4000$ *mV.*

7.4 Minimal single hole and single electron dot

Reaching the single hole regime requires lowering the levels of the quantum dot to the last level. In previous devices this regime was unreachable mainly due to the formation of unintentional quantum dots between two barriers. Implementing smaller pitch gates with current technology available at the MESA+ nanolab, hence 28 keV, cold development and PMMA spun at 6000 rpm. This decreases the spacing between barriers leaving less space for an unintentional dot to form. In this subsection the minimalistic single hole and single electron dot design is described. Due to their difference in nature, and different devices that were used to demonstrate the results for both dots, this section is divided into two. A start is made with the single layer depletion hole dot followed by the double layer electron dot.

7.4.1 Depletion dot

For the depletion dot design small pitch gates and barriers inspired by the Ciorga design are used. A typical AFM image is depicted in Figure 7.9a with a finite element simulation accordingly in Figure 7.9b where clear formation of a dot can be seen.

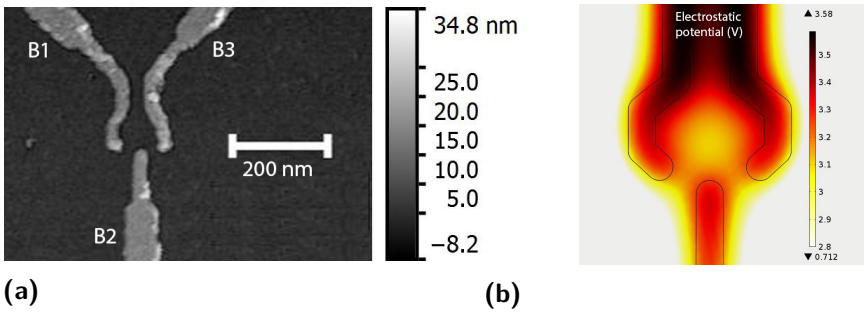
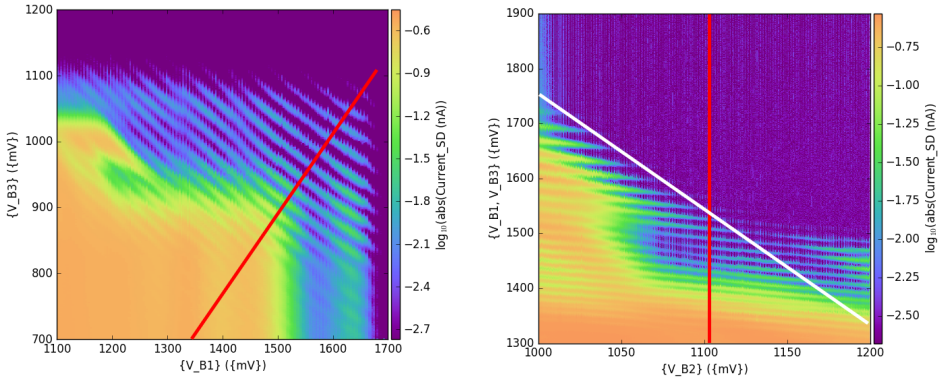


Fig. 7.9.: a) Typical AFM image of first generation depletion dot design, first layer. B1,B2 and B3 indicate the barriers. b) Electrostatic potential (V) in optimized Comsol design for the depletion dot where an excess of charge is present in a spherical shape indicating the dot.

In electrical behavior it is clear that when compared to the Ciorga design, pinch off curves look cleaner and optimal as depicted in Figure 7.13 where no resonances between both barriers are observed. Tuned into an optimal place in gate space the depletion dot becomes clear as depicted in Figure 7.10a with equal coupling to both barriers. An oscillation coupled to B1 at 1650 mV can be seen attributed to the formation of an unintentional dot between B2 and B1 as depicted in Figure A.5a in Appendix A.4.2. Or by the presence of a defect in the vicinity of the depletion dot as also visible at left middle of the figure at B3=1000 mV.
Coupling of B2 to the dot can be seen by a B1&B3 vs. B2 as depicted in Figure 7.10b

with the ratio of B1&B3 perpendicular to the oscillations of the dot as indicated by the red line in Figure 7.10a. The slope of these oscillations indicates a high coupling of B1&B3 compared to B2 attributed to the area of the barriers touching the dot, hence Figure 7.9b. The coupling has a ratio of approximately one to four which is about the difference in perimeter of the dot closer to B2 than to B1 and B3 combined.



(a) **(b)**

Fig. 7.10.: a) B1 vs. B3 scan where a depletion quantum hole dot is formed equally coupled to both barriers. The red line indicates the ratio between B1 and B3 for the scan in (b). *Here* $V_{SD} = 0.4\ mV$, $B2 = 1105\ mV$. b) B1&B3 vs. B2 scan with the ratio of B1 and B3 corresponding to the red line in (a) The formation of a dot is visible with high coupling to B1&B3 and low to B2. The white line indicates the scan direction to keep resistance of the tunnel barriers constant. *Here* $V_{SD} = 0.4\ mV$.

A bias spectroscopy is taken as depicted in Figure 7.11 where clear and closing diamonds are visible up to 1650 mV. The charging energy increases do to emptying of the dot and is in the order of a few up to 15 mV in the possible few hole regime. It can be seen that at high source drain voltages current starts leaking underneath the metal gates from source to drain due to the current being forced underneath. Furthermore the single hole regime is not reached in this device, clear from the charge upset at a negative bias voltage at 1680 mV. Another indication is that the last transition does not fully open into a Coulomb blockade diamond. A possible solution to increase the potential on the bottom barrier since its potential is just above pinch off, this however pushes the dot more upwards and thereby increasing the size of the dot making the few hole regime harder to reach.

Additionally a possible explanation for not being able to reach the few/single hole regime is that the barriers used to plunger the electrochemical potential of the dot also influence the tunnel barriers. A way to keep the tunnel barriers constant is to decrease the voltage on B2 while increasing the voltage on B1&B3. This method will however make B2 transparent when the voltage of B1&B3 becomes too high, and consequently B2 too low as depicted in Figure 7.10b by the white line. A transparent B2 means that current starts flowing underneath the barrier from source to drain and not through the dot. The corresponding bias spec is depicted in Figure 7.12

where at high B1&B3 (1700 mV) and correspondingly low B2 (1000 mV) leakage starts as can be seen in Figure A.5b in Appendix A.4.2.
A way to resolve this is to increase the width of the barriers thereby increasing the region where the 2DHG is depleted, recall the large Ciorga B1 and B3 barriers. These devices were fabricated but were however not successfully functioning due to a combination of problems with lift off, ALD and annealing procedures.

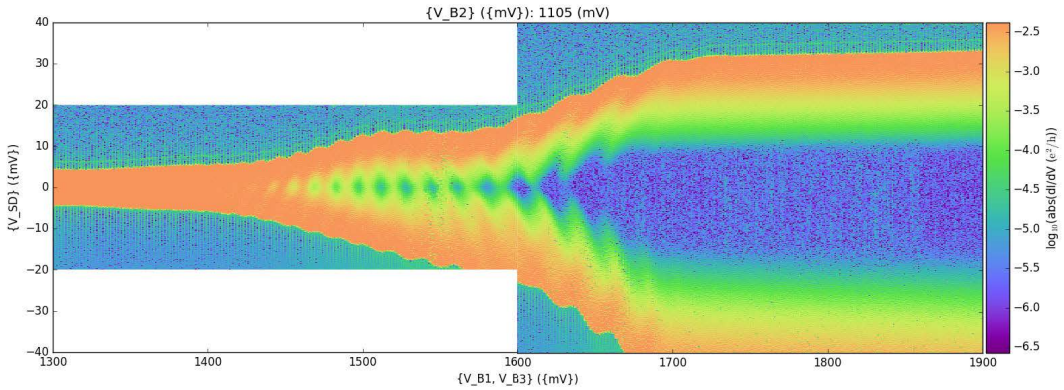


Fig. 7.11.: Bias spectroscopy taken along the line as depicted in Figure 7.10a where the formation of an intentional dot between B1 and B3 is visible. At high source drain voltages current is pushed underneath the barriers. *Here* $B2 = 1105$ *mV.*

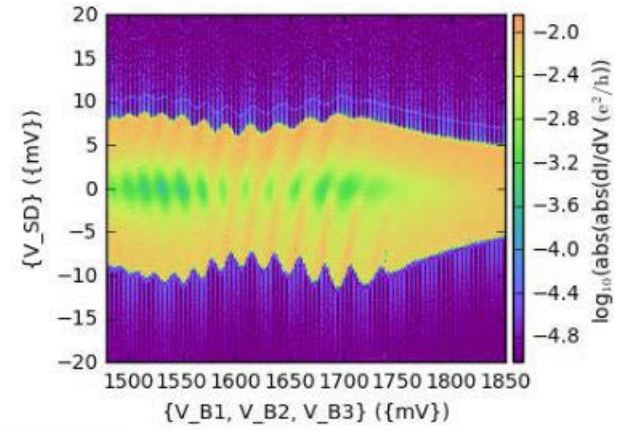


Fig. 7.12.: Bias spectroscopy where the voltage for B1 and B3 is increased while the voltage on B2 is decreased to keep a constant tunnel barrier resistance visualized by the white line in Figure 7.10b. An envelope can be seen around the Coulomb diamonds indicating coupling to a secondary unintentional dot or a defect.

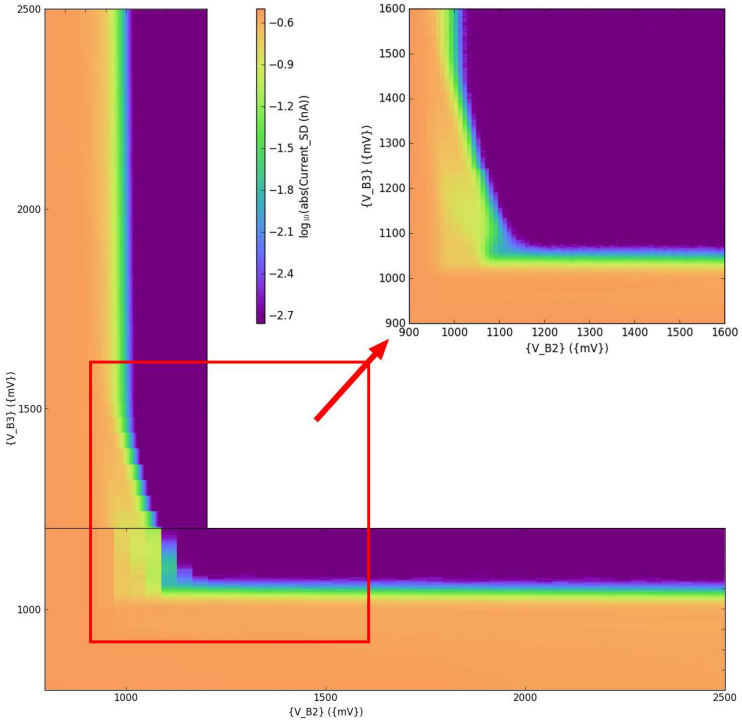
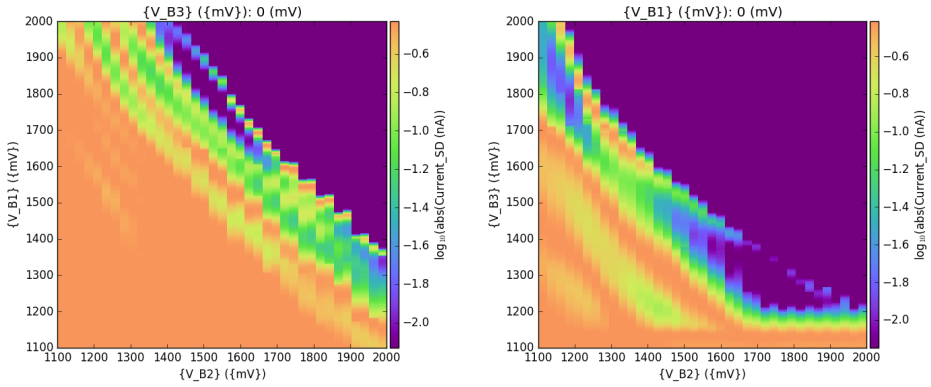


Fig. 7.13.: Color scale applies to entire figure. Three images stitched together where clear and sharp pinch off between the barriers can be seen without the formation of an unintentional dot. Right top inset is an increased resolution plot of lower barrier voltages. *Here* $V_{SD} = 0.4$ *mV,* $B1 = 0$ *mV.*

Additionally to the results for the depletion dot device at liquid helium temperature, this device was cooled down in the Oxford Heliox setup as discussed in the the experimental section for lower temperatures of approximately 280 mK.
Loading of the device did not go as smooth as planned requiring additional thermal cycles and exposure to external stimuli to the device. This is expected to be the main cause of the shift in pinch off voltage to 1,5 V as depicted in Figure 7.14 where it used to be 1,0 V. Compared to the results at liquid helium temperature the formation of unintentional resonances between both barriers can be seen, expected to be due to a combination of thermal cycles and a lower base temperature. This expected to be the main reason why the pinch off region between B2 and B3 referred to as optimal in Figure 7.13 does not behave as ideal in the Oxford Heliox setup.



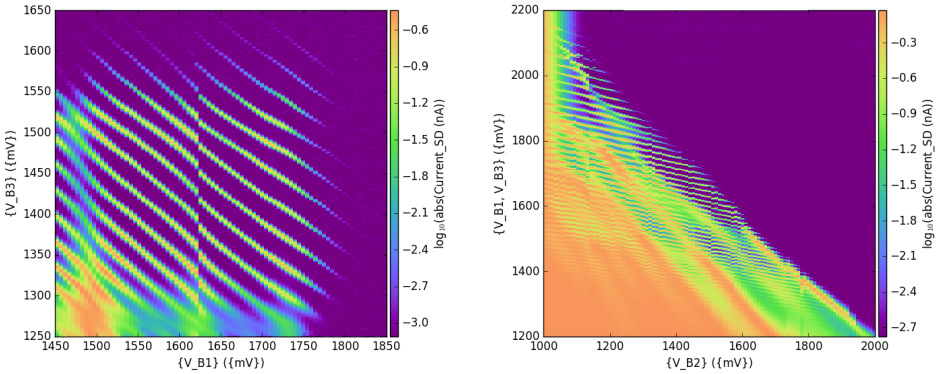
(a) **(b)**

Fig. 7.14.: a) B2 vs. B1 scan where the formation of unintentional resonances coupled to both barriers can be seen. *Here* $V_{SD} = 0.4$ *mV,* $B3 = 0$ *mV.* b) B2 vs. B3 scan where the formation of unintentional resonances coupled to both barriers can be sen. *Here* $V_{SD} = 0.4$ *mV,* $B1 = 0$ *mV.*

By making use of B1 and B3 an intentional dot is formed as depicted in Figure 7.15a. On top of this dot, unintentional resonances coupled to either B1 or B3 are visible as seen by the local increase in current of the intentional dot behavior. On top of this, a switch can be seen at B1=1625 mV devoted to the presence of a nearby charge trap under B1 or close to it.
To find the coupling of B2 to the dot and most optimal position for B1&B3, a scan is made as depicted in Figure 7.15b. The formation of an intentional quantum dot can be seen by the horizontal lines, slightly slanted indicating a coupling of B2 of 1:4 compared to B1&B3. As was noted before, devoted to the surface area of the barriers close to the dot. These unintentional resonances are expected to be due to the formation of dots between the barriers as they can also be found in Figure 7.14.

A bias spectroscopy is made with B1&B3 perpendicular to the oscillations of the intentional dot. In figure 7.16 it can be seen that the dot opens up before the

last transition is reached which is expected to be due to an increase of tunneling resistance due to an increase of B1&B3 while B2 stays the same. Thereby blocking the current at small source drain voltages. Additionally an envelope can be seen on top of the diamonds corresponding to the unintentional resonances between the barriers. A possible way to resolve this is to add a plunger either in the first or second layer.



(a) **(b)**

Fig. 7.15.: a) B1 vs. B3 scan where the formation of an intentional depletion dot can be seen. The switch visible at B1=1625 mV is expected to be due to a charge trap nearby. *Here* $V_{SD} = 0.4$ *mV,* $B2 = 1425$ *mV.* b) B2 vs. B1&B3 scan perpendicular to the oscillations of the quantum dot, it can be seen that unintentional resonances between the combination of barriers are formed. *Here* $V_{SD} = 1$ *mV.*

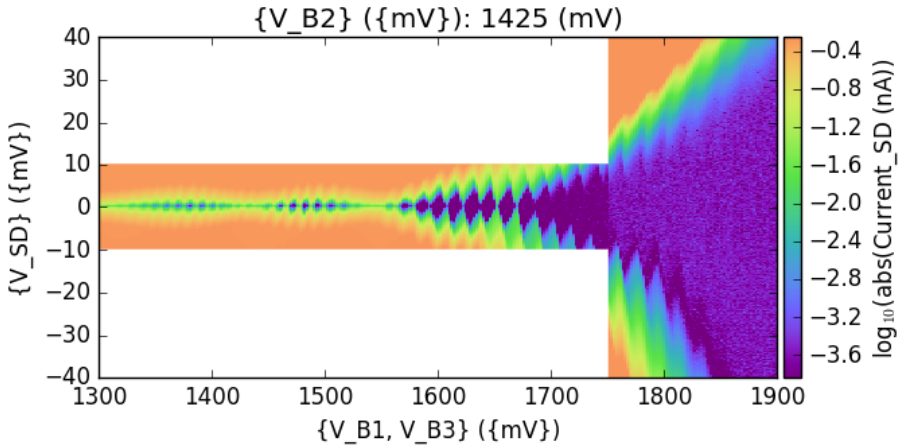
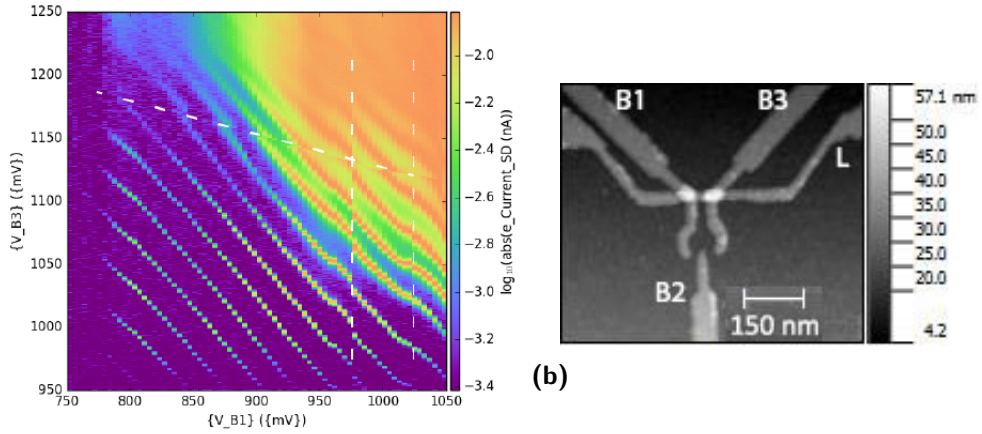


Fig. 7.16.: Bias spectroscopy taken perpendicular to the oscillations of Figure 7.15a. The opening of the quantum dot can be seen before the few hole regime is reached and an oscillation on top of the spectroscopy is visible attributed to the oscillations between the barriers. *Here* $B2 = 1425$ *mV.*

7.4.2 Single electron dot

To be able to verify if the depletion dot reached the single hole regime a new device is fabricated with a second layer lead gate used to define a SET by using the top two barriers: B1 and B3. It is noted that this device is fabricated from 15 nm titanium barriers and is depicted in Figure 7.17b. These measurements are done at a base temperature of approximately 280 mK in the Oxford Heliox setup as discussed in the experimental section.
A dot is formed with a lead voltage of 3000 mV to accumulate electrons from the n^{++} region while B1 and B3 are used to define tunnel barriers as depicted in Figure 7.17a. These oscillations are more narrow than the ones shown before, attributed to the lower temperature and consequently lower thermal energy which broadens the peaks. Oscillations clearly visible and equally coupled to both barriers are visible with a horizontal charge transition around B3=1175 mV and vertical around B1=975 mV. These transitions are attributed to a hole moving out of the depletion dot to the coupling of B1 and B3 to both dots. However only one transition can be seen whereas multiple holes are expected in the dot. Alternatively these switches can be a defect explained by the transition solely coupled to B1 at 975 mV. Since a hole dot is expected to be coupled to both B1 and B3 as is the case for the slanted transition for B3 at 1175 mV indicating that it is coupled to both B1 and B3.



(a) (b)

Fig. 7.17.: a) B1 vs. B3 measurement with clear resonances of the SET and a vertical and horizontal shift visible as indicated by the white lines expected to be due to either a hole moving out of the depletion dot or a defect. *Here* $e\_V_{SD} = 0.4$ *mV,* $h\_V_{SD} = 0$ *mV,* $B2 = 0$ *mV,* $L = 3000$ *mV.* b) Typical AFM scan of the double layer device with first layer barriers and second layer lead gate made from 15 nm titanium. B1,B2,B3 and L indicate the barriers and lead respectively.

To find the most optimal region for the lead gate in gate space and to see whether the lead gate can be used to push holes out of the depletion dot a lead gate vs. B1&B3 scan is made as depicted in Figure 7.18.
At the left top the voltage on the lead gate becomes too low to accumulate charges as can be seen by the disappearance of the orange region. On contrast at high bias voltages switches can be seen indicated by the white arrows expected to be instantaneous switches of nearby states as they were not reproducible. Additionally a charge transition indicated by the white line couples approximately 20 times stronger to the barriers. This resonance is in agreement with the transitions found in Figure 7.17a leaving it for debate whether it is coupling to the hole dot or a defect nearby. Also more transitions are expected to be visible when it would concern a transition from the hole dot. As an additional indication that the SET couples to the dole dot another charge transition is visible as indicated by the black line. This dot couples three times stronger to the lead gate in comparison to the white line indicating that its location is closer. A possible explanation for both lines is that the lowly coupled white line translates to the vertical line in Figure 7.17a while the black line is represented by the horizontal line in Figure 7.17a. If assumed that the black line indicates coupling to the hole dot one can define the mutual coupling energy E_{m} indicating that the electrochemical potential of the one dot depends on the charge state of the other[5]. This means that the SET has two potential ladders shifted by E_{m}.

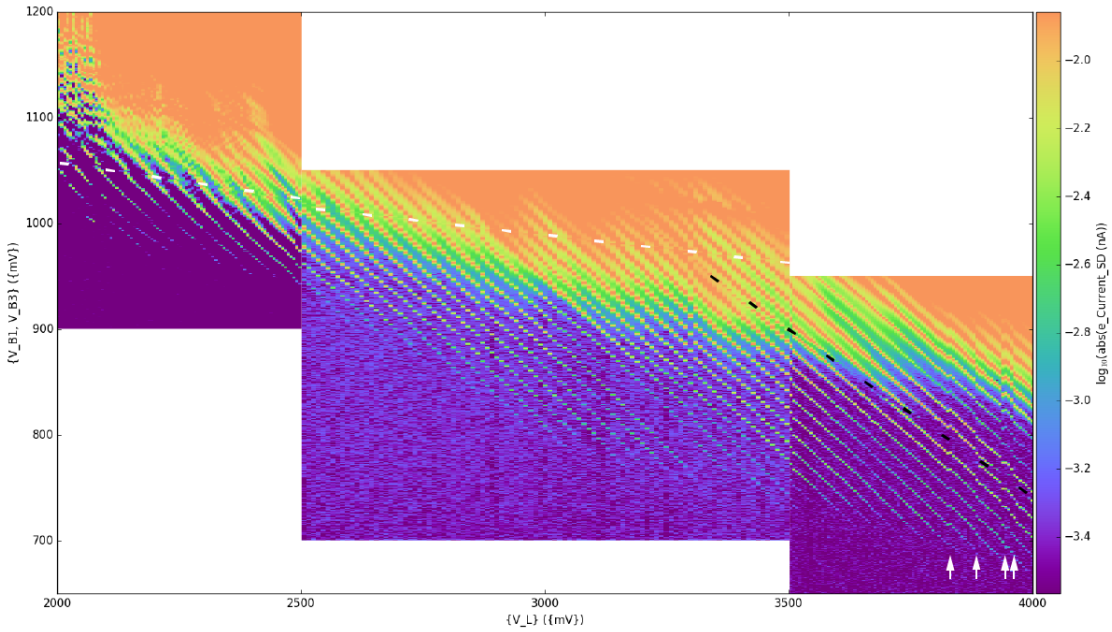


Fig. 7.18.: Combination of three deinterlaced scans where lead gate vs. B1&B3 is plotted. Stippled lines are used as a guide to the eye for charging events and arrows indicating instantaneous switches. The difference in background current is expected to be due to a different resolution. *Here* $e\_V_{SD} = 0.4$ *mV,* $h\_V_{SD} = 0$ *mV,* $B2 = 0$ *mV.*

In Figure 7.18 it can be seen that there are many charge transitions on the SET indicating many levels moving along the bias window. This becomes more clear when a bias spectroscopy is taken through these oscillations. A clear SET is visible with a total of 39 transitions up to 4000 mV on the lead gate as depicted in Figure 7.19. The dot looks stable with a constant charging energy of around 5 mV. This is also confirmed by a minimal envelope on top of the diamonds indicating limited coupling to additional dots. A defect can be seen around 3800 mV which is most likely a defect in the vicinity of the SET coupling to it. With a constant charging energy one can assume the constant interaction model is valid from which an approximate size of the dot can be calculated: C=$8\epsilon_0\epsilon_r d$, $d \approx 39$nm. This size is in correspondence with the area available for the SET between the top two barriers.

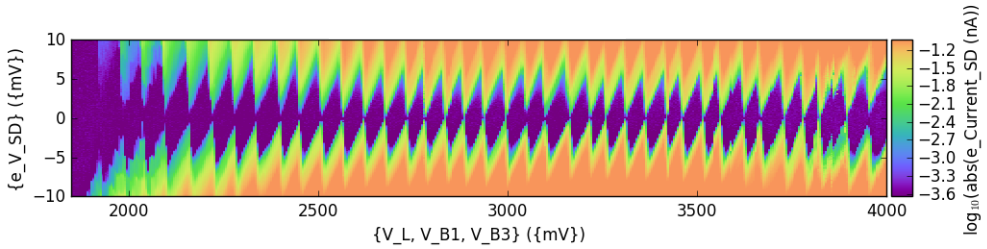


Fig. 7.19.: Bias spectroscopy measurement with al total of 39 transitions visible and a defect visible around 3800 mV. Overall constant charging energies of around 5 mV indicating a stable electron dot. *Here* $h\_V_{SD} = 0$ *mV,* $B2 = 0$ *mV.*

A bias spectroscopy is taken perpendicular to the oscillations of the quantum dot as depicted in Figure 7.20 where closing diamonds are clearly visible due to the ground states. A charging energy in the order of 7 mV is indicated by the dashed lines with the orbital excited state energy of 3.5 mV as indicated by the excited state in red. A second excited state is clearly visible around 800 mV with an orbital energy of 3.5 mV. Here the total gate potential required to add an extra electron to the dot is approximately 21 mV.
An attempt is made to use the bottom barrier, B2 as a plunger for the depletion dot as depicted in Figure 7.21. B2 is swept from -600 mV where for lower voltages current starts leaking from source to drain, up to 500 mV where the depletion dot should be depleted in combination with B1 and B3. As can be seen only one horizontal switch around B1&B3=770 mV occurs, but since it is a single event it is not clear if this is from the depletion dot. Additionally small switches can be seen vertically expected to be caused by defects nearby.

Due to the results during charge sensing the main hypothesis is that the depletion dot was not successfully formed due to confinements of the titanium barriers, therefore firstly the depletion dot should be functional with these metal gates. Alternatively palladium can also be used when taken into account that lift off and annealing

procedures might pose a difficulty. This design has shown however that it is capable of successfully defining a depletion hole dot and single electron hole dot with stable performance. Therefore with further optimization of the layout without major modifications should allow the device to be pushed even further.

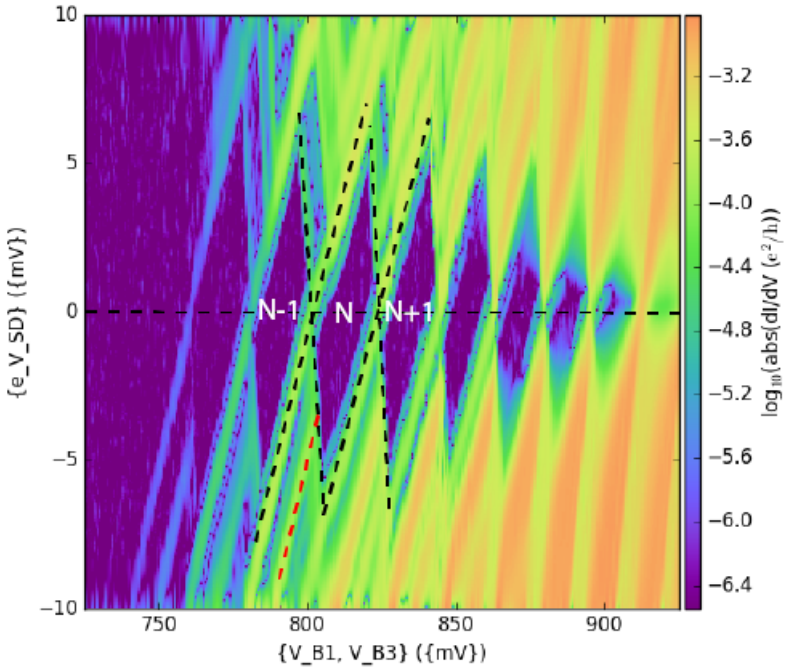


Fig. 7.20.: Bias spectroscopy with B1 and B3 perpendicular to the oscillations and clear ground states and excited states visible. A charging energy around 7 mV and orbital excited state energy of 3.5 mV visible around B1&B3=820 mV. *Here* $B2 = 0$ *mV,* $L = 3000$ *mV.*

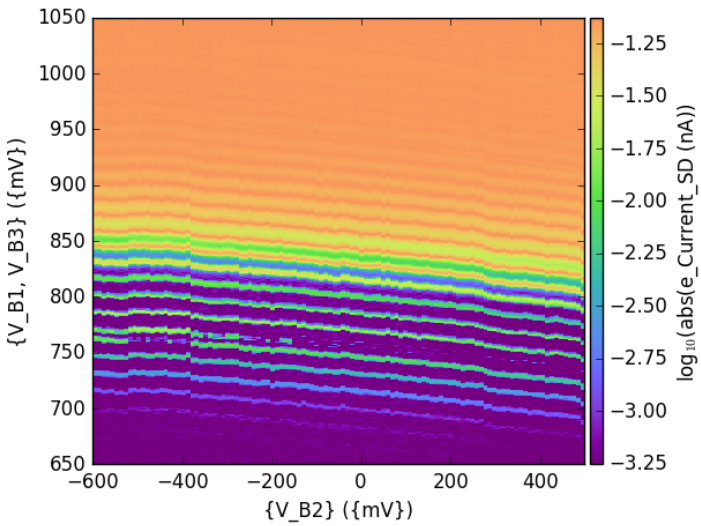


Fig. 7.21.: B1&B3 vs. B2 plot where the electron current is measured and no clear sign of charge sensing from the depletion dot can be seen. *Here* $e\_V_{SD} = 2$ *mV,* $h\_V_{SD} = 0$ *mV,* $L = 4000$ *mV.*

7.5 Fixed charge

In this subsection the influence of UltraViolet (UV) and ozone (O_3) on the fixed charge at the $SiO_2 - Al_2O_3$ and thereby indirectly the conductance of the 2DHG is presented. As discussed in the experimental section two sample were glued to the same PCB and exposed to a combination of UV and O_3 by using the setup as depicted in Figure A.1 in Appendix A.1. These samples have been Ar annealed at 400 °C for 30 minutes.

As can be seen in Figure 7.22 the resistance of the sample exposed to UV and O_3 first drops which can be explained by filling of charge traps by UV light at the $SiO_2 - Al_2O_3$ interface. After this the resistance saturates around 50 seconds resistance and increases due to the oxidation effect of O_3 which diffuses in filling oxygen vacancies at the Al_2O_3 interface. When however compared to the sample protected by the aluminum roof and only exposed to O_3 a difference in behavior is found. In this sample the slow decrease of resistance is attributed due to reflections of the UV light reaching the surface and thereby inducing charges at the interface. While minimal exposure to UV, the sample remains subjective to O_3 diffusing towards the sample, and an increase in resistance is expected. In Figure 7.22 it can be seen that the resistance is minimally effected. This can be due to O_3 not being able to diffuse under the aluminum roof and thereby not reaching the sample or that oxygen radicals do not diffuse into the substrate without UV to assist oxidation of the negative charge traps.

As for accumulation dots, fixed charge is not of the essence and by making use of UV and O_3 removal of fixed charge is possible. This decrease in fixed charge lowers pinch off voltages as depicted in Figure 7.23a which is advantages since a lower pinch off and thereby makes a sample less subjective to leakage. Whereas for the sample being under the roof no shift in pinch off voltage was observed.

As briefly mentioned in the theory section fixed charge can be induced by photons after which this charge slowly reduces when stored in the dark. In the devices used in this thesis no change in charge density was found after being stored in the dark for over 30 days. Indicating that the fabricated depletion dot devices pose a useful alternative for stable planar quantum dots in silicon.

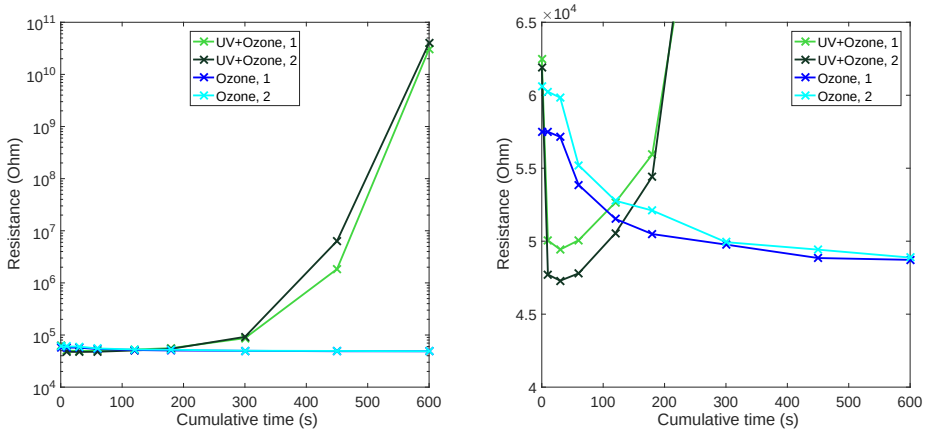


Fig. 7.22.: Test of the exposure to UV Ozone for a total of four devices. a) Logarithmic scale. b) Linear scale.

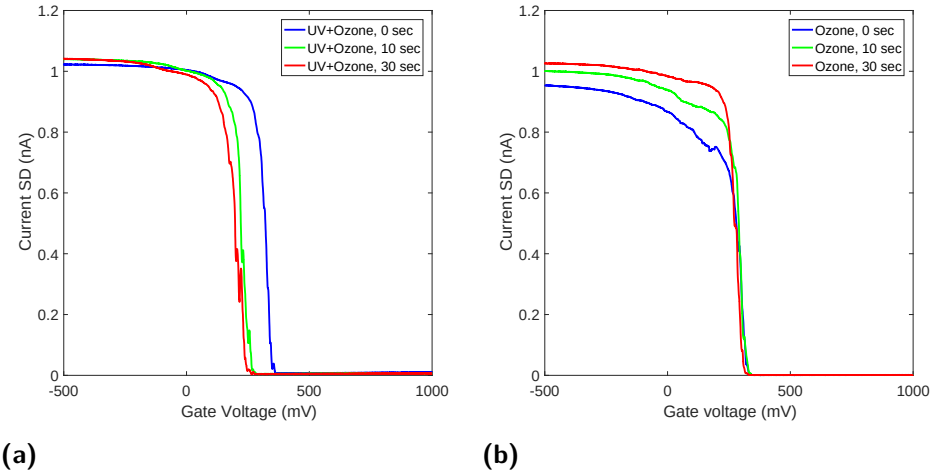
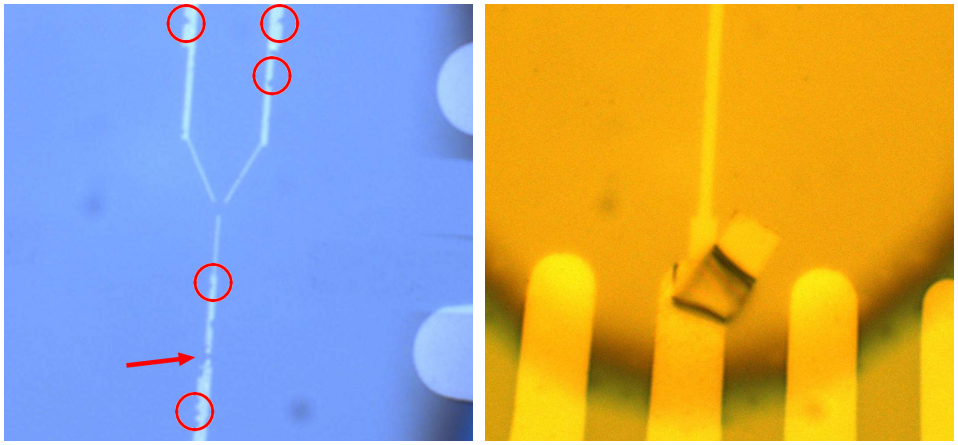


Fig. 7.23.: Test for the UV Ozone treatment, blue 0 sec, green 10 sec and red 30 sec. a) Sample exposed to UV and O_3. b) Sample exposed to O_3.

7.6 Palladium and Titanium gates

During the iteration process palladium as well as titanium devices were fabricated. An initial start was made with palladium, but as it turned out small features (<40 nm), called single pixel lines were on occasion shaken off during the lift off procedure due to ultrasonic power. This drastically decreased yield for some palladium batches. Additionally some devices of palladium de-wetted during the annealing procedure as depicted in Figure 7.24a. It is not yet clear why this happens since it occurs non consistent at different annealing temperatures (350-500 °C) and gas treatments (N_2, Ar and H_2). It was also noted that two different chips part of one annealing run came out differently, indicating that it is an effect not only linked to the annealing procedure, but may be influenced by earlier processing steps.
As an alternative titanium is posed as a gate metal to resolve the issue of de-wetting and removal of the small features during lift off, since titanium is known for its good adhesion properties. The fabricated titanium structures however did not stick properly to the micro sized photo-pads made from palladium and titanium. A solution to this problem is to fabricate the top layer of the sample entirely out of titanium, meaning that no photo lithography is used for the micro sized contact pads but solely EBL is used to define the gates. A downside of this approach is that it required more EBL time. A second concern of using titanium instead of palladium is that it oxidizes through when exposed for long periods to the ambient. In the layer stack in this thesis the metal layer is capped with a 5 nm Al_2O_3 layer before exposure to the ambient. In a thermal oxidation test the sample was exposed to a cumulative time of 95 minutes on a hotplate at 160 °C as shown in Table 7.1. Here no significant shift in pinch off voltage for the devices of the minimal depletion dot design were observed indicating constant functioning of the barriers (B1,B2 and B3) and thus no noticeable oxidation of titanium. Additionally no large difference in channel resistance of the 2DHG was observed. The slight difference in resistance is due to the usage of the Beep-R which has a limited step size. And the fact that every time a sample is cooled to 4.2 K the behavior slightly changes.
A disadvantage of using titanium gates for depletion dot structures is that either a proper 2DHG or proper gates were present. Indicating that the gates already limit the source drain conduction. A negative voltage on these barriers lifts this restriction indicating that a 2DHG is present since there are no lead gates to accumulate charge. A possible explanation is found when assumed that the unoxidized titanium gates suck out the negative fixed charges present as oxides at the SiO_2-Al_2O_3 interface during annealing, consequently leaving no fixed charge at these locations.
It is unclear at this moment how these mechanisms operate, but if the behavior of the titanium gates on fixed charge is found to be consistent this mechanism can be used to define barriers without applying gate voltages. This implies that a quantum dot could be formed by precise patterning of the barriers and only an external plunger

gate is required to sweep to the electrochemical potential of the dot. This would allow for an array of quantum dots links to one another, hence "sacrificing tuneability for scalability". Additionally the electrochemical state of the depletion dot can be altered by using a second layer lead gate, or by making use of the open structure of the depletion dot by using external sources of light.



(a) (b)

Fig. 7.24.: a) Palladium gates de-wetted during annealing indicated by the circles and with bottom barrier broken at the red arrow. b) Titanium device where the pad peeled of the microstructures bondpads.

Tab. 7.1.: The data in the table is an average of two samples for pinch off voltages, and three for the conduction of the 2DHG from source to drain.

Time (min)	0	10	20	35	95
2DHG conduction (kΩ)	-	100	20	100	73
Pinch off voltage (mV)	88	200	135	160	160

8 Conclusion and discussion

As a start of this thesis it was shown that the fixed charge present in the system is sufficient to accumulate holes from the highly doped p^{++} regions without making use of a lead gate. Thereby decreasing device complexity and improving overall yield since there are less gates to pattern. Additionally the absence of a lead gate makes the depletion dot an open design where no gates are present on top of the dot meaning that no defects can be induced by electron beam lithography. The removal of a lead gate decreases however the flexibility in gate space.

The next step towards the few hole regime for depletion hole dots was made by showing that it is possible to fabricate a double layer device with both a functioning depletion hole and single electron dot simultaneously in gate space. This device however showed a non optimal behavior for both dots. Out of main interest of improving the depletion dot, the Ciorga et al. [45] design known to work for a GaAs stack up to the single electron regime was adopted. This design showed clear signs of a depletion dot with on top unintentional resonances between the barriers. This behavior is devoted to the large structural design of the barriers also evident from the high barriers pinch off voltages (>5 V).

To limit the amount of unintentional resonances it is found useful to decrease the spacing between barriers to a minimum. To do this 28 keV and cold development were used to achieve smaller feature sizes in the order of 40 nm. In combination with a finite element method simulation software: Comsol Multiphysics 5.1 gate designs could be imported and analyzed both from layout editing tools as well as atomic force microscope scans. In means of flexibly and optimization these simulations have proven to be a valuable tool for future this and research.

Furthermore by using these techniques a stable and well defined intentional depletion dot made from palladium has been shown. Transport measurements indicate limited formation of unintentional dots as has been shown to be a key factor for reaching the few hole regime. Additionally it is found that using the same barriers to define tunnel barriers and deplete the island limits the behavior of the depletion dot in the possible few hole regime. A solution might pose to implement a second layer lead gate to be keep the small dot geometries while still being able to change the electrochemical potential of the dot.

As for the second dot used for charge sensing a clean and stable SET has been successfully fabricated by using titanium barriers with a total of 39 transitions. The influence of titanium on the 2DHG might pose a useful feature to find the few hole regime due to a local depletion under the barriers of the fixed charge. Alternatively titanium gates might be used to create a depletion dot without using external bias voltages, by making use of this mechanism allowing for scalability and external excitation. Opposed to palladium, titanium improved adhesion to the substrate improving yield when small feature sizes and ultrasonic power are used. Additionally, titanium can better withstand annealing temperatures leaving the gates intact. Titanium shows promising results when covered with Al_2O_3 and performs stable after thermal oxidation for 95 minutes at 160 °C. The expression of these unintentional dots might change for a titanium device requiring optimization of the size and spacing of the barriers indicating that optimization might push the depletion dot even further.

Therefore it is concluded from this thesis that the few hole regime in depletion hole dot structures should be achieved with the right architecture and an SET to allow for charge sensing. It poses a good alternative for accumulation dots due to its possibilities for scalability and open design.

9 Outlook

In this thesis the foundation for a depletion hole dot in combination with a single electron dot is shown to be feasible. The concept is not yet pushed to its limits and some more iterations have to be made to find the few or even single hole regime. The hole depletion dot made from palladium as presented as best device so far shows pinch offs within the operating regime of both the depletion hole as well as the electron dot. Therefore the dimensions used in these devices are assumed to be close to optimal and one should focus on improving device yield by means of lift off and annealing procedure.

Alternatively the project can continue with titanium devices as has been shown to work. For these devices spacing between the barriers of the depletion dot should increase to allow source drain conduction without bias voltages, and consequently pinch off in the positive voltage regime. Additionally it may be interesting to fabricate a device with pinch off voltages around 0 V to instantaneously define a depletion dot without using external bias. A second layer plunger can be used to tune the electrochemical potential of the dot.

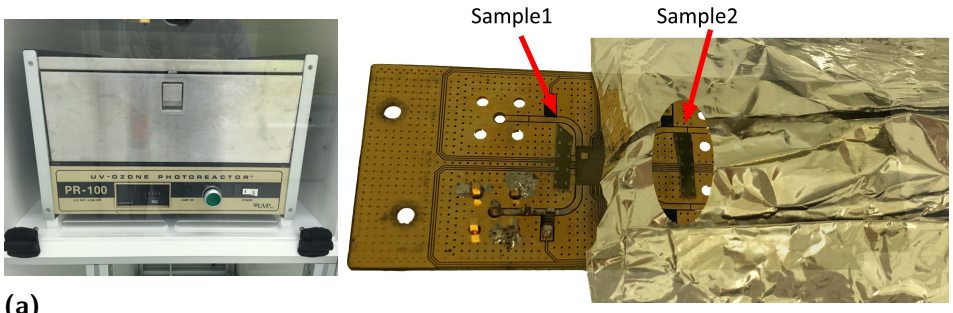
As shown in this work the origin of the fixed charge is still under debate. It might pose useful to get a better understanding of this mechanism by exposing a sample to either ultraviolet or ozone in dedicated clean room equipment. It would also be interesting to see whether the polarity of the fixed charge can be of a positive nature giving rise to depletion electron dots.

Assuming a depletion hole dot can successfully be fabricated for the single hole regime one knows how these charges occupy orbitals in this quasi one-dimensional artificial atom. Additionally interesting effects like Zeeman splitting could be investigated or one could think of a double depletion hole dot.

Appendix

A

A.1 Experimental Methods



(a) (b)

Fig. A.1.: a) PR-100 UV-Ozone photoreactor in the cleanroom where the sample can be loaded by opening the door and placing it on a holder. A UV lamp generates both UV light and thereby O_3. b) Sample for in the reactor. At the left sample 1 exposed to both UV and Ozone while sample 2 is shielded by an aluminum roof to avoid exposure by UV (opening and transparency of aluminum for graphical purposes made with photoshop).

A.2 Process flow

Standard fabrication steps performed in the MESA+ cleanroom on top of the pre-processed wafer pieces are listed in detail in Table A.1. The fabrication steps for the standard am-bipolar quantum dot design can be found the Phd thesis of F. Muller [22]. All steps are performed by the author excluding ALD to grow Al_2O_3, and the annealing procedure, performed by S. Amitonov.

Tab. A.1.: Process flow for the single and double layer designs.

Process	**Material**	**Settings**	**Remarks**
First Layer			
Clean sample	VLSI Acetone	10 min soak	
	IPA	rinse & blow dry	
Spin resist	PMMA A2	6000 RPM / 45 sec	
Bake resist		160 °C / 3 min	Hotplate
Expose resist			RAITH150-TWO
Develop resist	MIBK/IPA	30 sec dip	Develop at -15 °C
		blow dry	
AFM			Quality check
Evaporate metal	Pd/Ti - 13 nm	P $\approx 10^{-7}$ mbar	BIOS Evaporator
Lift-off	DMSO	80 °C, low ultrasonic power	sonic bath
			use sonic power conservatively
AFM			Quality check
ALD	Al_2O_3 - 5 nm		
Annealing	300-400 °C	H_2 / Ar / N_2	If last layer
Second Layer			
Spin resist	PMMA A2	6000 RPM / 45 sec	
Bake resist		160 C / 3 min	Hotplate
Expose resist			RAITH150-TWO
Develop resist	MIBK/IPA	30 sec dip	Develop at -15 °C
		blow dry	
AFM			Quality check
Evaporate metal	Pd/Ti - 25 nm	P $\approx 10^{-7}$ mbar	BIOS Evaporator
Lift-off	DMSO	80 °C, low ultrasonic power	sonic bath
			use sonic power conservatively
AFM			Quality check
ALD	Al_2O_3 - 5 nm		
Annealing	300-400 °C	H_2 / Ar / N_2	If last layer

A.3 Simulation

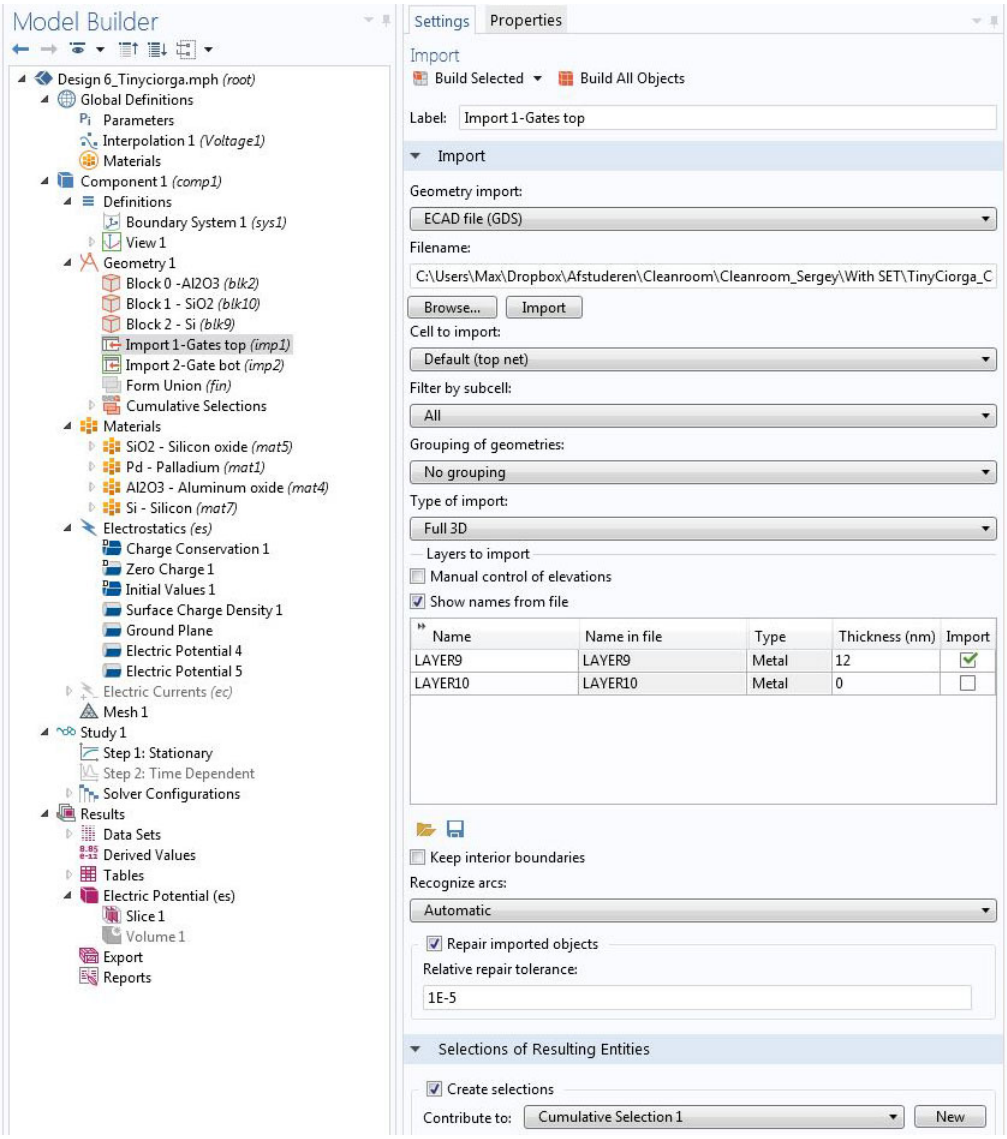


Fig. A.2.: Part of the graphical user interface of Comsol Multiphysics 5.1. The model builder is depicted at the left with at the right the menu of the import function found under 'Geometry 1' tab. This tab is used to setup the dimensions of the model, hence the Block 0,1 and 2 elements used for the Si, SiO_2 and Al_2O_3 layers.

To import an AFM scan into Comsol the following steps have to be taken with Figure A.3 as a graphical guideline. Firstly open the AFM scan file with Gwyddion 2.45 and select option: "Mark grains by threshold" to mark the metal layer in a different color. Use a distinct color such as red (255,0,0 RGB values) with an opacity of 255 and save file as .png while disabling: value scale, draw mask legend and rulers. And adjust color range under: "Sketch color range" to part of data" to create a completely black background. Convect the image to .dxf to be imported into Klayout which can for example be done by using http://www.autotracer.org/ [49]. For a more detailed conversion the .png file can be smoothed by using for example photoshop before converting it into .dxf. Another option is to take a higher resolution AFM scan of a smaller region, effectively getting more pixels into the area of interest.

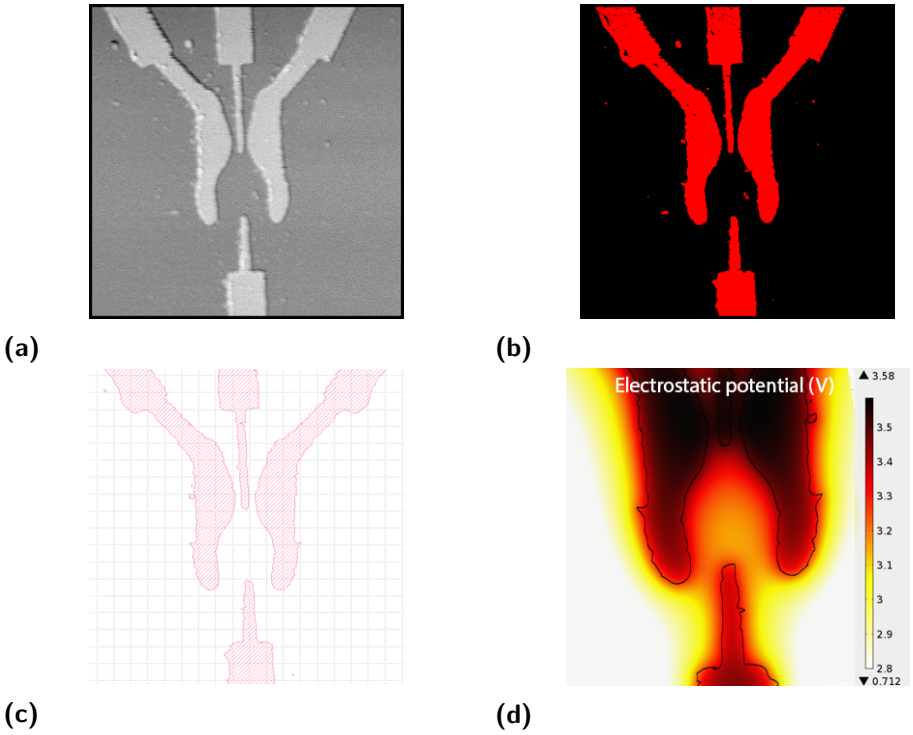
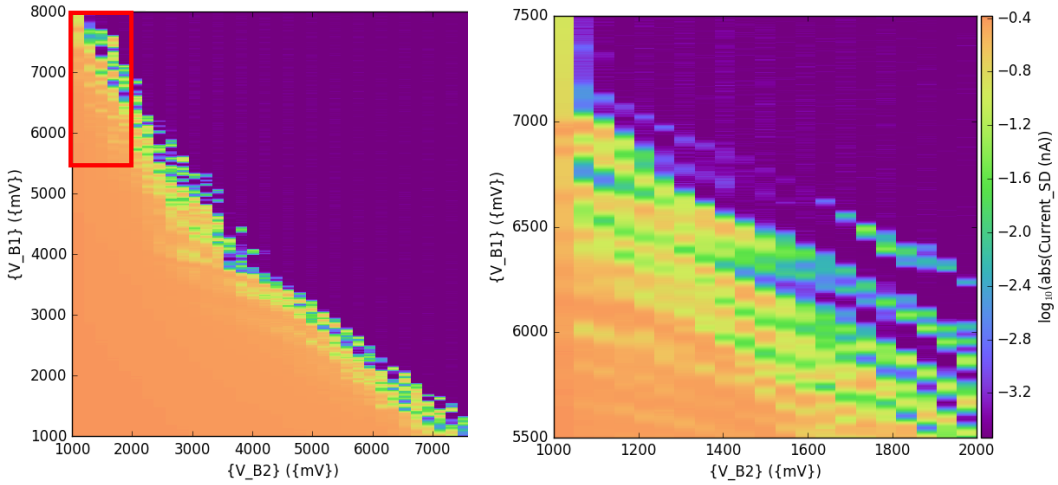


Fig. A.3.: Import from AFM scan into Comsol Multiphysics. a) Start with normal AFM scan opened in Gwyddion b) Set offset for color range such that the topography sticks out c) Convert to .GDS image and open in KLayout. d) Simulation run in Comsol for the fabricated device.

A.4 Results

In this section of the appendix the additional results for the devices are presented.

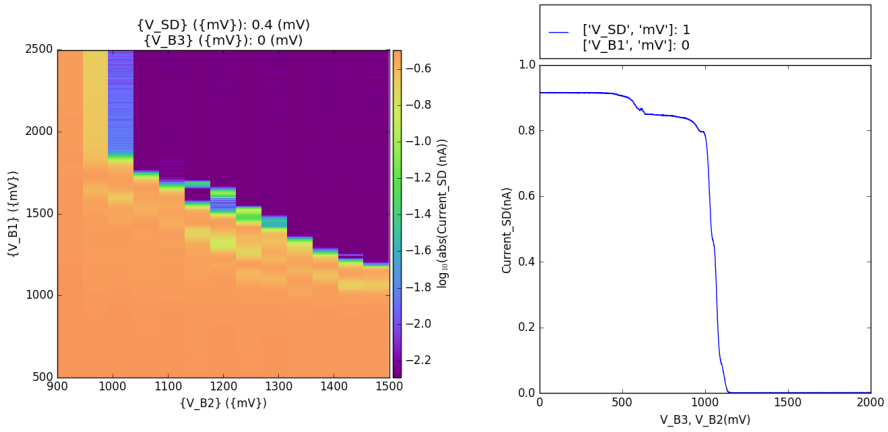
A.4.1 Ciorga Design



(a) **(b)**

Fig. A.4.: a) B2 vs. B1 plot with many resonances visible from the unintentional dot forming between B2 and B1. *Here* $V_{SD} = 0.4$ *mV,* $B3 = 500$ *mV,* $P = 500$ *mV.* b) Higher resolution plot of the left to area of (a). *Here* $V_{SD} = 0.4$ *mV,* $B3 = 0$ *mV,* $P = 0$ *mV.*

A.4.2 Minimal single hole and single electron dot



(a) **(b)**

Fig. A.5.: a) B2 vs. B1 plot showing the region of pinch off where resonances between both barriers can be seen. *Here* $V_{SD} = 0.4$ *mV,* $B3 = 0$ *mV.* b) Pinch off graph of B2&B3 to deplete the source drain channel around 1000 mV. *Here* $V_{SD} = 1$ *mV,* $B1 = 0$ *mV.*

Bibliography

[1] Brock D. C. *Understanding Moore's law: Four Decades of Innovation*. Chemical Heritage Foundation, 2006 (cit. on p. 3).

[2] Feynman R. P. „Plenty of Room at the Bottom". 1959 (cit. on p. 3).

[3] Kouwenhoven L. P. „Electron transport in quantum dots". In: *Mesoscopic Electron Transport* Kluwer (1997), pp. 105–214 (cit. on pp. 3, 9, 12).

[4] Averin D. V., Korotkov A. N., and Likharev K. K. „Theory of single-electron charging of quantum wells and dots". In: *Physical Reviewd* 44.12 (1991), pp. 6199–6211 (cit. on p. 3).

[5] van der Wiel W. G., De Franceschi S., Elzerman J., et al. „Electron transport through double quantum dots". In: *Reviews of Modern Physics* 75.1 (2002), pp. 1–22 (cit. on pp. 3, 13, 15–17, 49).

[6] Yu. M. „Computable and Uncomputable (in Russian)". In: *Sovetskoye Radio* (1980) (cit. on p. 3).

[7] Morton J.J. L., Tyryshkin A.M., Brown R.M., et al. „Solid-state quantum memory using the 31P nuclear spin". In: *Nature* 455.7216 (2008), pp. 1085–1088 (cit. on p. 4).

[8] Clemmen S., Farsi A., Ramelow S., and Gaeta A. L. „Ramsey interference with single photons". In: *Physical Review Letters* 223601.117 (2016), pp. 1–6 (cit. on p. 4).

[9] Hanson R., Kouwenhoven L. P., Petta J. R., Tarucha S., and Vandersypen L. M. K. „Spins in few-electron quantum dots". In: *Reviews of modern physics* 79.4 (2007), pp. 1217–1265 (cit. on pp. 4, 9, 10, 13).

[10] Zutic I., Jaroslav F., and Das Sarma S. „Spintronics: Fundamentals and applications". In: *Rev. Mod. Phys.* 76 (2004), pp. 323–410 (cit. on p. 4).

[11] Shor P. W. „Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer". In: *Society for Industrial and Applied Mathematics* 26.5 (1997), pp. 1484–1509 (cit. on p. 4).

[12] Grover L. K. „Quantum Computers Can Search Arbitrarily Large Databases by a Single Query". In: *Physical Review Letters* 79.23 (1997), pp. 4709–4712 (cit. on p. 4).

[13] Nave R. `http://hyperphysics.phy-astr.gsu.edu/hbase/tables/elabund.html`. Georgia State University. retrieved: juli 4, 2016 (cit. on p. 7).

[14] Shin-Etsu Chemical Co. *Semiconductor Materials Division*. `https://www.shinetsu.co.jp/en/products/semicon.html`. retrieved: juli 4, 2016 (cit. on p. 7).

[15] Sonzogni A. A. and NNDC contributors. *Chart of Nuclides*. https://en.wikipedia.org/wiki/Silicon. Upton (NY): National Nuclear Data Center, Brookhaven National Laboratory. retrieved: 2008-09-13 (cit. on p. 7).

[16] Dwyer K. J., Pomeroy J. M., Simons D. S., Steffens K. L., and Lau J. W. „Enriching 28 Si beyond 99.9998 % for semiconductor quantum computing". In: *Journal of Physics D: Applied Physics* 47.34 (2014) (cit. on p. 7).

[17] Kittel C. *Introduction to Solid State Physics*. John Wiley & Sons, Inc, 2005 (cit. on p. 8).

[18] Cohen M. L. and Chelikowsky J. R. *Electronic structure and optical properties of semiconductors*. Ed. by Springer-Verlag. 2nd. 1988 (cit. on p. 8).

[19] Datta S. *Quantum transport*. Ed. by Cambridge University Press. Cambridge University Press, 2005 (cit. on p. 8).

[20] Bruijnes F. „Capacitively coupled single-electron and single-hole transistors in silicon". MA thesis. 2016 (cit. on pp. 9, 18).

[21] Fulton T. A. and Dolan G. J. „Observation of single-electron charging effects in small tunnel junctions". In: *Phys. Rev. Lett.* 59 (1987), pp. 109–112 (cit. on p. 10).

[22] Muller F. „Single-charge Tunneling in Ambipolar Silicon Quantum Dots". PhD thesis. 2015 (cit. on pp. 10, 20, 61).

[23] van der Wiel W. G. *Electron transport in quantum dots*. 2008 (cit. on p. 11).

[24] Heisenberg W. „Über den anschaulichen Inhalt der quantentheoretischen Kinematik und Mechanik". In: *Zeitschrift fur Physik* 43 (Mar. 1927), pp. 172–198 (cit. on p. 12).

[25] Waldrop B. Y. M. „More Than Moore". In: *Nature* 530 (2016), p. 145 (cit. on p. 12).

[26] Jarillo-Herrero P., Sapmaz S., Dekker C., Kouwenhoven L. P., and Van Der Zant H. S. J. „Electron-hole symmetry in a semiconducting carbon nanotube quantum dot." In: *Nature* 429.6990 (2004), pp. 389–92 (cit. on p. 14).

[27] Zwanenburg F. „Session 7 Quantum NanoElectronics 2". 2014 (cit. on p. 15).

[28] David Berman. „Single-electron transistor as a charge sensor for semiconductor applications". In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* 15.6 (1997), p. 2844 (cit. on p. 18).

[29] Field M., Smith C. G., Pepper M., et al. „Measurements of Coulomb Blockade with a Noninvasive Voltage Probe". In: 70.9 (1993), pp. 1311–1314 (cit. on p. 18).

[30] Simmons C. B., Thalakulam M., Shaji N., et al. „Single-electron quantum dot in SiSiGe with integrated charge sensing". In: *Applied Physics Letters* 91.21 (2007), pp. 1–4. arXiv: 0710.3725 (cit. on p. 18).

[31] Elzerman J. M., Tarucha S., and Kouwenhoven L. R. „Few-electron quantum dot circuit with integrated charge read out.pdf". In: *Physical Review B* 161308 (2003), pp. 9–12. arXiv: 0212489 [cond-mat] (cit. on p. 18).

[32] Andrea Morello, Jarryd J Pla, Floris a Zwanenburg, et al. „Single-shot readout of an electron spin in silicon." In: *Nature* 467.7316 (2010), pp. 687–91. arXiv: 1003.2679 (cit. on p. 18).

[33] Yang C. H., Lim W. H., Zwanenburg F. A., and Dzurak A. S. „Dynamically controlled charge sensing of a few-electron silicon quantum dot“. In: *AIP Advances* 1.4 (2011). arXiv: 1107.1557 (cit. on p. 19).

[34] Bansal A., Mishra H., Bhattacharya S., and Singh R.S. „First Principles Calculations of Bonding and Charges at the Al 2 O 3 Interface in a for the Surface Passivation of“. In: *IEEE Trans. Electron Devices* 63.2 (2016), pp. 544–550 (cit. on pp. 20, 21).

[35] Knaut M. and Bartha J. W. „Investigation of the c-Si / Al2O3 Interface for Silicon Surface Passivation“. In: October (2014) (cit. on p. 20).

[36] Jakschik S., Schroeder U., Hecht T., et al. „Physical characterization of thin ALD-Al2O3 films“. In: *Applied Surface Science* 211.1-4 (2003), pp. 352–359 (cit. on p. 20).

[37] Hoex B., Gielis J. J. H., Van De Sanden M. C. M., and Kessels W. M. M. „On the c-Si surface passivation mechanism by the negative-charge-dielectric Al2 O3“. In: *Journal of Applied Physics* 104.11 (2008) (cit. on p. 20).

[38] Naumann V., Otto M., Wehrspohn R. B., Werner M., and Hagendorf C. „Interface and material characterization of thin ALD-Al 2 O 3 layers on crystalline silicon“. In: *Elsevier Ltd. Selection* 27 (2012), pp. 312–318 (cit. on p. 20).

[39] Kimoto K., Matsui Y., Nabatame T., et al. „Coordination and interface analysis of atomic-layer-deposition Al2O3 on Si(001) using energy-loss near-edge structures“. In: *Applied Physics Letters* 83.21 (2003), pp. 4306–4308 (cit. on p. 20).

[40] Gielis J. J. H., Hoex B., Van De Sanden M. C. M., and Kessels W. M. M. „Negative charge and charging dynamics in Al2O3 films on Si characterized by second-harmonic generation“. In: *Journal of Applied Physics* 104.7 (2008) (cit. on pp. 20, 22).

[41] Liao B., Stangl R., Mueller T., et al. „The effect of light soaking on crystalline silicon surface passivation by atomic layer deposited Al2O3“. In: *Journal of Applied Physics* 113.2 (2013) (cit. on pp. 21, 22).

[42] Riordan C. and Hulstron R. „What is an air mass 1.5 spectrum? solar cell performance and calculations“. In: *IEEE Conference on Photovoltaic Specialists* (1990), pp. 1085–1088 (cit. on p. 21).

[43] Jordan P. M., Simon D. K., Mikolajick T., and Dirnstorfer I. „Trapped charge densities in Al2O3-based silicon surface passivation layers“. In: *Journal of Applied Physics* 119.21 (2016) (cit. on p. 21).

[44] Dingemans G. and Kessels W. M. M. „Status and prospects of Al2O3-based surface passivation schemes for silicon solar cells“. In: *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* 30.4 (2012), p. 040802 (cit. on p. 23).

[45] Ciorga M., Sachrajda A., Hawrylak P., et al. „Addition spectrum of a lateral dot from Coulomb and spin-blockade spectroscopy“. In: *Physical Review B* 61.24 (2000), pp. 16315–16318 (cit. on pp. 26, 27, 39, 57).

[46] Cord B., Lutkenhaus J., and Berggren K. K. „Optimal temperature for development of poly(methylmethacrylate)“. In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* 25.6 (2007), p. 2013 (cit. on p. 29).

[47] Ocola L. E. and Stein A. „Effect of cold development on improvement in electron-beam nanopatterning resolution and line roughness“. In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* 24.6 (2006), p. 3061 (cit. on p. 29).

[48] P.C. Spruijtenburg. „Imperfection holes and defects in silicon quantum dots“. PhD thesis. 2017 (cit. on p. 35).

[49] Maklabu GmbH. `http://www.autotracer.org/` (cit. on p. 64).