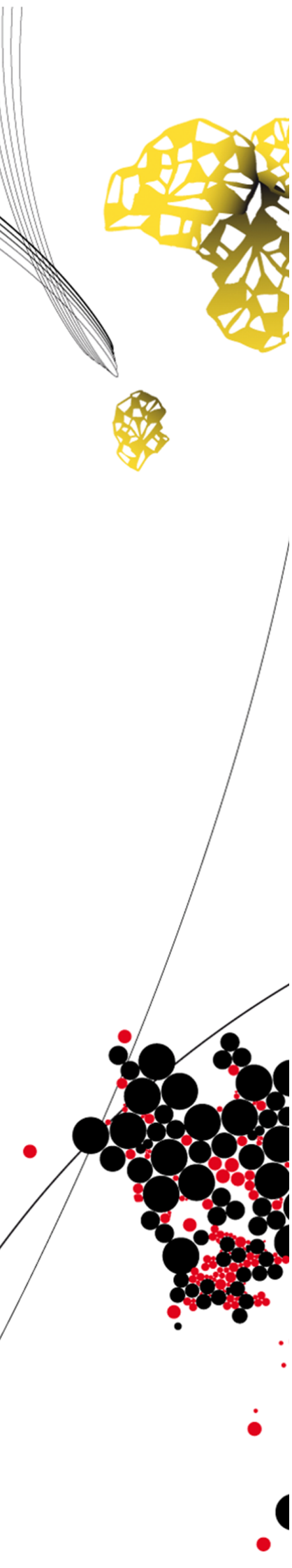

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A Charge Biased Delay Element

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Abstract

In most modern electronic devices a wireless transmission link is available. The RF power amplfier(RFPA) of the transmitting part is a dominant source of power dissipations. To increase the efficiency of the RFPA, class E amplifiers are used. These amplifiers are prone to process, voltage, temperature and environmental changes. In self-healing RF amplifiers, the RFPA is characterized to obtain information about its performance after production and during operation. The information obtained by the characterization system is used to tune the RFPA in such way that it becomes more robust. To characterize the RFPA, the output is sampled at 8 equidistant phases of its operating frequency. These phases are obtained by a delay locked loop(DLL) driven by the local oscillator(LO) used by the up-conversion mixer preceding the RFPA. The DLL plays an essential role in the accuracy and power consumption of the characterization system. Especially jitter on the outputs of the DLL is an important contributor of inaccuracy in the measurement system.
This master assignment focusses on delay elements within the DLL. An overview and a comparison is given for conventional delay elements for the specified speed, power and jitter. These specification are directly linked to the accuracy and power consumption of the PA characterization system. Furthermore, the application of charge biasing in delay element is investigated with the objective to reduce power dissipation in the voltage controlled delay line.
A charge biased delay element is proposed for which an analytic model is derived to obtain insight in power consumption, speed and jitter. With the model is shown that compared to the current starved inverter, the charge biased delay element consumes less power, but has a considerable increase in jitter and delay time. Escpecially for large delay times the jitter of the charge biased delay element becomes orders of magnitude larger than the conventional delay element.
An analysis is done on the optimal number of cascaded delay elements for power and jitter performance to obtain a certain delay. From the analysis could be concluded that more delay elements results in better jitter and power performance. This conclusion excludes delay elements that dissipate static power.

Contents

Chapter 1

Introduction

1.1 Motivation

Within the last decade, wireless communication has experienced a revolution. The majority of the people has a mobile device and it has become an integrated part of our lives. Because battery performance improves at a slower pace, a lot of effort is put into making applications low power. In a transceiver, the power amplifier (PA) is by far the most power hungry component. Class E amplifiers are the most efficient solution for low power applications, with an ideal efficiency of 100%. Under ideal conditions, these amplifiers are really robust and efficient. However, due to process, voltage, temperature and environmental changes (PVT-E), these amplifiers prove fragile and less efficient. Self-healing amplifiers correct for the PVT-E after production and during operation. To apply corrections, characterization of the PA is required. The PA could be adequately characterized by phase and amplitude information of the fundamental tone and its second and third harmonic. These are obtained by doing a discrete Fourier transform(DFT). The samples for the DFT are obtained by a down mixing the PA signal with an N-phase mixer and applying the signal to an N-input ADC. The N-phase mixer requires multi-phase equally spaced clocks which are obtained by a delay-locked loop (DLL). The voltage-controlled delay line (VCDL) used in this DLL proves to be the most power consuming component of the PA characterization system. The current delay elements in the VCDL employ power hungry current steering logic. In applications like clock and data recovery and comparators, charge biasing is proven to be a low power replacement for current steering techniques. The purpose of this assignment is to explore ways to reduce the power consumption in a VCDL, especially by using the concept of charge biasing.

1.2 Research Topics

- A comparison of conventional delay elements.
- The applications of charge biasing in voltage controlled delay lines.
- A comparison of charge biasing delay element to conventional delay elements.

1.3 Thesis Outline

In chapter 2 the system in which the delay element is applied is explained. Chapter 3 will elaborate on the specifications related to chapter 2. Trade-offs between the specifications will be explained as well. From here, an overview on conventional delay elements is given in chapter 4. A comparison is made between the conventional delay elements. Chapter 5 introduces the charge biased delay elements and is divided in three parts, describing respectively the concept of charge biasing applied to delay elements, an analysis on the specifications described in chapter 3 and a comparison against the current starved inverter. Chapter 6 treats the optimal number of delay elements with respect to specifications described in chapter 3. Chapter 7 gives an overview of conclusions and has recommendations for future research.

Chapter 2

PA Characterization System

Most modern electronic devices have a wireless transmission link. These links consist of transmitters and receivers. For the transmitter, an electromagnatic wave is transmitted and the power of the signal delivered to the antenna is amplified by the radio frequency power amplifier(RFPA). The power amplifier is one of the most power consuming components of a transmission link. Therefore, the efficiency of the power amplifier has a large impact on the efficiency of the system as a whole. A RFPA has to meet certain criteria:

- Life-time, so it does not break down before a specified amount of uses.
- Linearity, non-linearity might cause corruption of data, reduce the efficiency and interfere with other devices.
- Efficiency, all electronic devices have bounds on their power consumption due to cost or battery life.

Analog components are far more sensitive than digital components. Small variations during processing, variations on the power supply, changes in output impedance of the antenna and changes in temperature (PVT-E) all influence the efficiency, life time and linearity of the amplifier. These sensitivities put harsh demands on the design and fabrication on amplifiers. Usually this requires a design margin for RFPA to guarantee a circuit life time and linearity at the cost of area efficiency and price.

2.1 Self Healing

To minimize design margin and to reduce the fragility of a RFPA, self-healing is proposed. The errors in the amplifier due to PVT-E are monitored after fabrication and during operation. This is information is used to vary the parameters of the RFPA to correct for errors in a feedback configuration. This is shown in figure 2.1.

PA Characterization

The system for characterizing the RFPA is shown in figure 2.2. The RFPA is designed to operate in the range from 1GHz to 10GHz. A delay locked loop (DLL) is used, that is locked to the local oscillator(LO) used by up-conversion

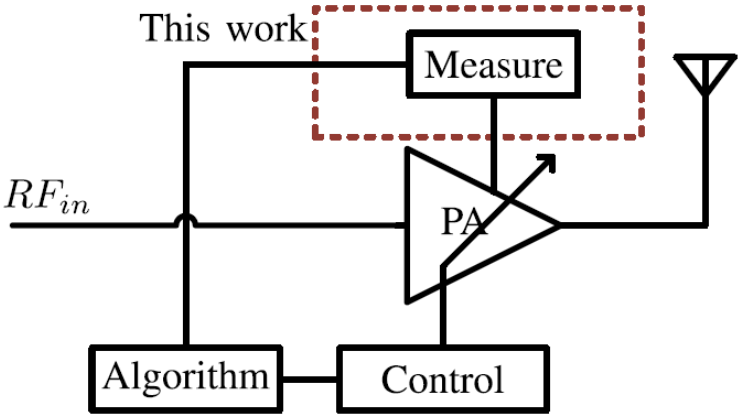


Figure 2.1: System overview for a self-healing power amplifier [1]

mixer preceding the RFPA. Ideally, the DLL generates N equally spaced over one LO period. These N outputs are fed to N sampling mixers, which sample the signal and mix it to DC. This makes the analog-to-digital converter(ADC) succeeding the sampling mixers feasible for low power consumption[2]. The sampled signal is translated to the digital domain by the ADC and processed by the baseband processor and could be used to correct the RFPA.

Discrete Fourier Transform(DFT)

It is assumed that the output of the RFPA can be described sufficiently accurate by the fundamental tone and the second and third harmonic, which are obtained by doing the DFT. The DFT is carried out in the digital domain, requiring sampled data. To obtain information up to the third harmonic, at least seven sample points equally distributed over one period of the RF signal are required. These samples are obtained by the passive sampling mixer shown in figure 2.2. The ADC provides the quantization. The discrete Fourier transform(DFT) is given by:

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi kn/N} \tag{2.1}$$

Here n is the sample number and k is the frequency normalized to the sample frequency. N is the total number of samples. X_k is complex and contains amplitude and phase information. The amplitude and phase are obtained by the following equations:

$$|X_k| = \sqrt{Re\{X_k\}^2 + Im\{X_k\}^2}/N \tag{2.2a}$$

$$arg(X_k) = atan\left(\frac{Im\{X_k\}}{Re\{X_k\}}\right) \tag{2.2b}$$

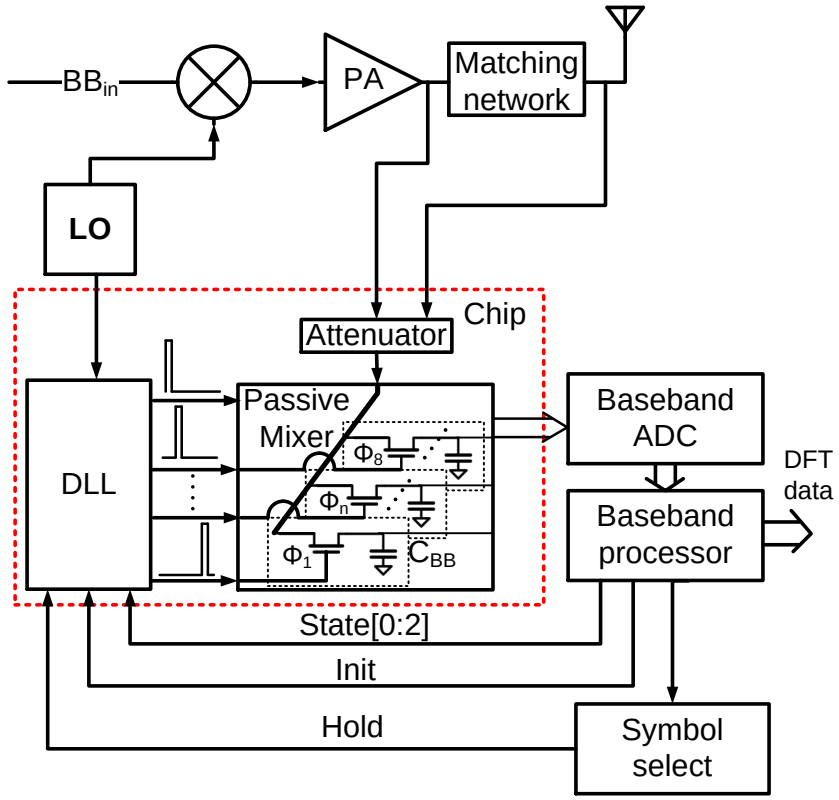


Figure 2.2: Measurement system for a self healing PA, including an attenuator and a passive N-phase sampling mixer [1]

It is important to note the that DFT assumes samples equally distributed over one period of the RF signal. Therefore, the DLL has to be very precisely locked to the LO and the phases should be equally spaced over one RF period. If this is not the case, the output of the DFT does not correspond to the actual spectral components at the output of RFPA and therefore compromises accuracy. Care should be taken to make sure that the samples taken at the output of the RFPA are accurate in time.

N-phase Sampling Mixer

The RF output signal is mixed down to dc by using a passive sampling mixer in the mixer region [3]. The use of the mixer region requires multiple periods of the RFPA-output to settle on the sampling capacitor, but does not present a significant load to the PA, ensuring that matching to the antenna is not compromised. Because PVT-E changes are static or relatively slow processes, the increased settling time due to the mixing region is not a problem. However, the RF-signal's phase or amplitude should not change within the period required for settling.

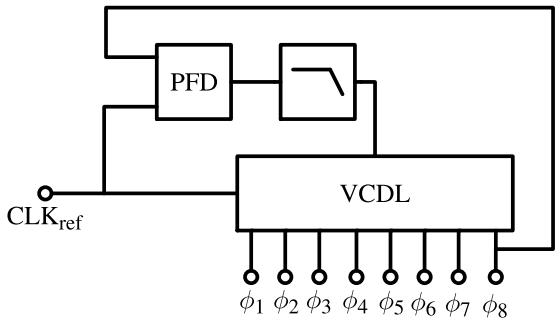


Figure 2.3: High level overview of a delay locked loop using a phase-frequency detector(PFD), a loop filter and a voltage controlled delay line

Doing this for N phases, one period of the signal could be reconstructed, assuming that the signal to be measured is periodic and the settling time is smaller than the low frequency variation of the RF signal. This requires N clock signals running at f_{LO} that have a phase difference of $2\pi/N$ relative to each other as is shown in figure 2.2.

2.2 Delay Locked Loop

In [1] the reason for using a delay locked loop(DLL) to create a multiphase clock is explained. A DLL uses a voltage controlled delay line to delay a reference clock. A phase-frequency detector is used to obtain the phase difference between the reference and the output of the VCDL. Using negative feedback, the output of the PFD is used to correct the total delay of the VCDL by using a loop filter. A system overview of a DLL is given in figure 2.3.

Voltage Controlled Delay Line

The voltage controlled delay line(VCDL) is a cascade of delay elements. If N phases are required, usually N elements are cascaded. To make sure that the phases are equally distributed over one period, the delay elements should be as identical as possible. Dynamic power increases with frequency, therefore the VCDL, which is operated at RF, is assumed the most power hungry part of the DLL and should therefore be the main focus of power reduction. The specifications of these elements and their relations to power is explained in chapter 3.

2.3 Conclusions

In this chapter an overview is given on the system in which the delay elements are applied. The delay locked loop operates at RF and therefore the delay elements dissipate a considerable portion of power. The different phases of the

DLL have to be equally spaced over one period of the RF-signal to obtain a reliable characterization.

Chapter 3

Delay Element Specifications

This chapter gives on overview of the specifications which are relevant for delay elements in the context of a characterizer for self-healing PAs.

3.1 Power

The main reason for choosing a class E amplifier is to make power gain at RF with high power efficiency. Due to the high sensitivity of PVT-E, these amplifiers are the ideal candidate for self-healing. However, if the measurement system consumes a considerable amount of power, design margins may prove more power efficient than self-healing. Therefore measurement circuit's power consumption should be orders of magnitude smaller than the power consumption of the PA itself. Power consumption in general could be described by the following equation:

$$P = C_L f_{sw} V_{DD}^2 + V_{DD} I_{static} \tag{3.1}$$

From the first part of equation (3.1) is seen that the power is linearly proportional to the switching frequency. Depending on the topology, delay elements draw mostly current from the supply when switching, or draw a constant current. However, the amount of constant current drawn is usually depends on the required delay(chapter 4). Because the multiphase clock circuit has to operate at RF, the voltage controlled delay line takes a considerable portion of the total power consumption of the measurement system.

3.2 Speed

The RFPA is supposed to work at an operating frequency between 1GHz and 10GHz. The speed or delay time of a single delay element depends on the LO and the number of delay elements. If N phases are required, the delay time for a single element should be:

$$T_D = T_{LO}/N \tag{3.2}$$

If a the number of elements is assumed to be 8, this would require a minimum individual delay of 12.5 pico seconds.

3.3 Jitter

The precision of a measured signal is usually expressed in signal-to-noise ratio (SNR). If the signal is below the noise level, measured values are not accurate any more.
Time deviation from an ideal sampling clock is called jitter. In sampled systems, the moment of sampling is of importance to the SNR. Sampling at the wrong time instant could be expressed as an error in amplitude and phase, which in turn translates in a lower SNR. Relating jitter to SNR can be done by using a first order Taylor approximation on the input signal which is assumed to be a sinusoid with frequency f. The following equation expresses the SNR due to jitter[2]:

$$SNR \approx 20log_{10}\left(\frac{1}{2\pi f \sigma_t}\right) \tag{3.3}$$

It is estimated that minimally 8 bits is required. The SNR corresponding to 8 bits is ($\approx 50dB$)[2], requires a standard deviation jitter of more than two order of magnitude smaller than the period of the sampled signal. This makes a first order approximation sufficient. The SNR could be improved in the digital domain by averaging, and in the analog domain by filtering, however this is out of the scope of this thesis. The remainder of this section will treat different origins of jitter and their relevance.

Thermal Jitter

Thermal jitter originates from thermal voltage noise. This noise originates from FETs and resistive elements inside the delay element itself.

1/f Jitter

1/f Jitter originates from flicker noise, or 1/f noise. Flicker noise exists due to traps present in the FET channel. These traps result in noise behavior that is non-uniform distributed over frequency and has a 1/f shape. Differential delay elements have 1/f noise due to their tail bias source. Other delay elements might have 1/f noise due to their bias circuitry [4].

Power supply variation

Due to the non-zero output impedance of the power supply, the current drawn by neighboring circuits might cause the ripple and fluctuations locally on the supply lines. Depending on the delay element, this ripple might modulate delay time. Supply regulation and decoupling are possible solutions to reduce this effect.

Substrate Noise

Fast switching of high swing digital circuits couple signal into parasitic capacitances to the substrate. This coupling causes voltage fluctuations in the substrate and might modulate the threshold voltage of analog circuits. Modulation of the threshold voltage causes some delay elements to deviate from

their ideal zero-crossing. Substrate noise could be avoided by shielding and separating the delay element and the noise coupling source.

Mismatch Jitter

Two transistors designed for the same values might have a relative deviation in values after production. This is called mismatch. As a result, the delay elements are not identical to each other and produce a different delay. This kind of jitter is deterministic after the chip is fabricated, but could be estimated a priori[5]. Most of the time, mismatch jitter is the most dominant source of jitter in DLLs, however calibration can be used to reduce this effect at the cost of complexity.

Relevance

Power supply variation and substrate noise are highly relevant if the delay elements are used within a digital environment, for example to reduce clock skew, as mentioned by [6]. However, in the context of chapter 2 it is possible to separate the analog circuitry and the digital circuitry. Decoupling the supply with large capacitances is deemed adequate. Low frequency jitter is reduced heavily by the loop filter and is therefore considered less relevant. Hence the main focus is on thermal jitter. Mismatch jitter could be solved by calibration.

3.4 Trade-offs

Power, accuracy and operating frequency(speed) all influence each other. Although the reduction of power is the main objective, it is important to compare power constrained by speed and accuracy to obtain an objective view on performance and meet the specifications for jitter and speed. Equation (3.1) states the trade-off between operating frequency and power. Thermal jitter and power consumption have an important trade-off: thermal jitter could always be reduced by admittance scaling [7] at the cost of power. To fairly compare different delay element topologies, the jitter is normalized to power[8]:

$$\sigma_{tnorP}^2 = \frac{\sigma_t^2 P}{1mW} \tag{3.4}$$

The calculation of σ_{tnorP} for a fully differential delay element (chapter 4) reveals that the normalized jitter variance is linear proportional to the delay time[8]. This relation holds as well for other delay element topologies (chapter 4). Because of the linear proportionality, we could write:

$$\sigma_{tnorP}^2 = cT_D \tag{3.5}$$

Where c is a constant which could be determined if σ_{tnorP}^2 for its corresponding T_D is known. From chapter 2 follows that the signal to be sampled has the frequency of the local oscillator, f_{LO}. Using this in equation (3.3) together with equation (3.2) and equation (3.5). We can obtain the SNR normalized to power:

$$SNR_{norP} = 10log_{10}\left(\frac{N}{4\pi^2 c f_{LO}}\right) \tag{3.6}$$

From equation (3.6) we can see that the SNR for a given power could be increased by using a lower value for f_{LO}, or a lower value of c. Equation (3.6) gives the SNR_{norP} due to the jitter at the first tap of the voltage controlled delay line. The second tap has the jitter variance of the first tap plus its own jitter variance. This repeats at every succeeding tap, in other words: jitter accumulations through the VCDL (chapter 6). The SNR_{norP} at the n-th tap of the VCDL is:

$$SNR_{norP,n} = 10log_{10}\left(\frac{N}{4\pi^2 ncf_{LO}}\right) \tag{3.7}$$

For completeness we can obtain an equation that would give us the SNR due to jitter on the n-th tap as a function of operating frequency, power and number of elements:

$$SNR_n = 10log_{10}\left(\frac{N}{4\pi^2 ncf_{LO}}\right) + 10log_{10}\left(\frac{P}{1mW}\right) \tag{3.8}$$

From equation (3.8) we can deduce that given a constrain on f_{LO} and SNR at the N-th tap, the only free variable to reduce the power is c, which depends on the delay element topology. Therefore, jitter normalized to power will be the focus in this thesis.

3.5 Conclusions

In this section specification and their relevance in the context of chapter 2 are treated. Furthermore, the trade-offs between jitter, power and speed are treated. Literature shows that to fairly compare jitter and power of different delay element topologies a FoM should be used.

Chapter 4

Voltage Controlled Delay Element Topologies

This chapter presents an overview of conventional delay elements. The treated specifications are thermal jitter, delay time and power consumption. The delay elements treated in this chapter are shown in figure 4.1. Most of the available other topologies are derived from one of the topologies mentioned in this chapter, except for the Park-Kim differential delay element[9] and its derivatives.
The delay elements could be roughly divided in two categories: Single ended and differential. In some applications, a differential delay element is required. An example is a PLL which VCO generates a quadrature clock. A quadrature clock requires 4 phases with 90 degrees offset. Because of the even amount of phases, the voltage controlled delay line output should be cross coupled to its input, ensuring 360 degrees phase shift.

4.1 Single Ended Voltage Tuning

The delay of an inverter can be tuned by varying the supply voltage (figure 4.1a). Tuning of the supply changes the transconductance of the PFET and NFET and changes the g_m/C time. The inverters draw a considerable current and cannot be driven by the loop-filter of the DLL. A common way to obtain V'_{tune} is shown in figure 4.2. Level-shifters at the output shift the voltage to V_{DD} to interface the VCDL with switches. At the input a level-shifter is required to shit the rail-to-rail reference clock from V_{DD} to V'_{tune} The regulator is within the control loop of the DLL and should be designed not to compromise the stability of the loop or reduce its bandwidth [10] [11] [12]. An advantage of the regulator is that it provides moderate rejection against power supply variation.
A readable closed form expression for delay time can be obtained with the following assumptions[13]:

- The delay time T_D is the time instance for which V_{out} crosses the logic threshold.
- The logic threshold is $V_{tune}/2$.
- The input signal V_{in} has zero rise/fall time when switched between V_{tune} and ground.

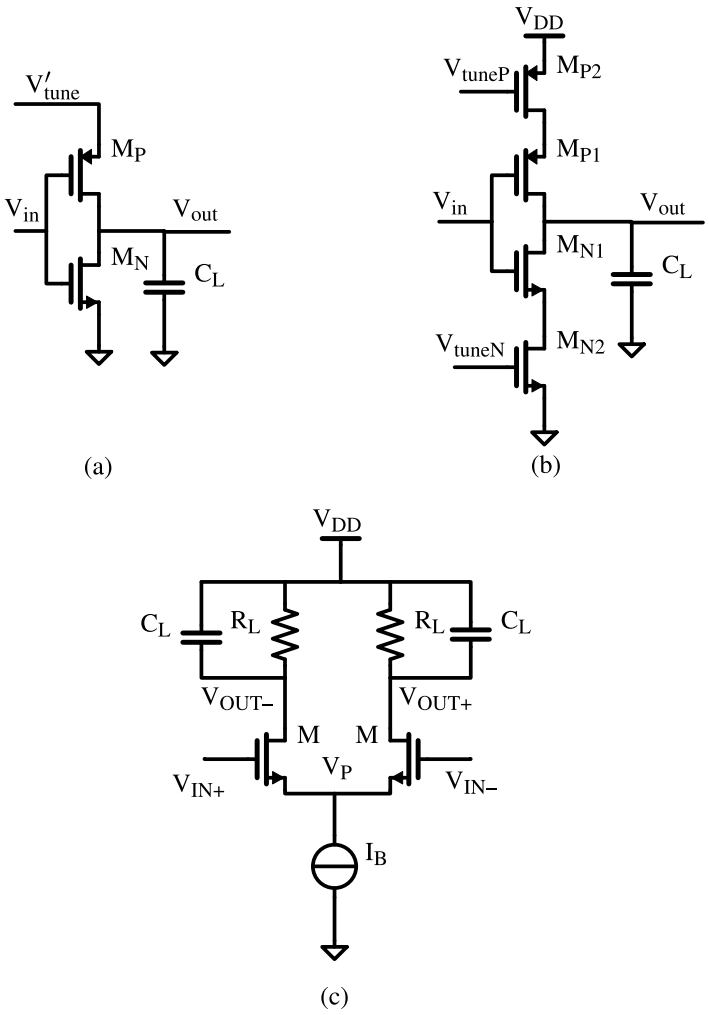


Figure 4.1: a) Voltage tuning b) Current starved inverter c) Fully differential

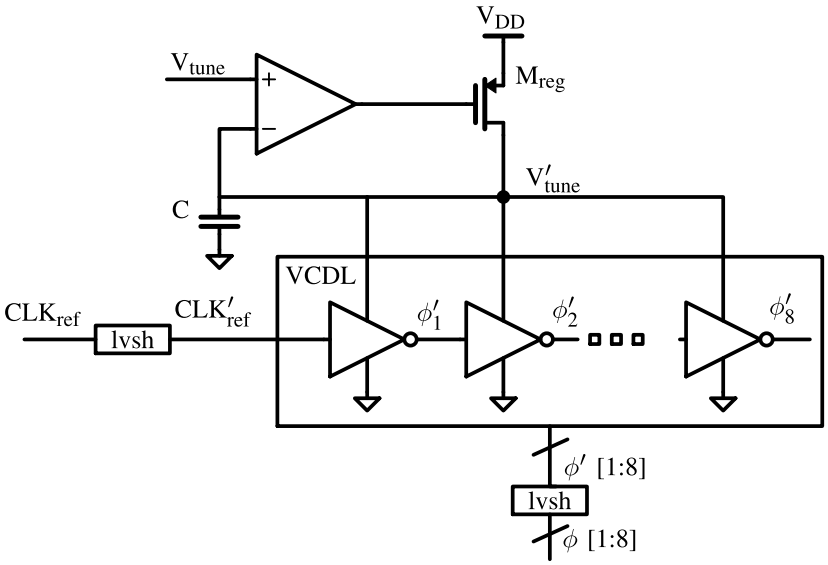


Figure 4.2: Regulator and levelshifter in a VCDL employing voltage tuned inverters

- At the time instance that V_{in} switches, the current drawn by M_P or M_N immediately reaches its peak value until V_{out} crosses the logic threshold.

A more accurate model is presented in [14], but does not have closed form expressions. The delay time for a voltage tuned inverter is [13]:

$$T_D = \frac{V_{tune} C_L}{2 I_{peak}} \tag{4.1}$$

Where C_L is the load capacitance and I_{peak} is the peak current.
The power could be obtained from equation (3.1). The inverter has no static power consumption, because the complementary FETs prevent a direct path to ground. If the DLL is locked, all the capacitances in the VCDL are charged and discharged within T_{LO}. Resulting in:

$$P_{VCDL} = N \frac{V_{tune}^2 C_L}{T_{LO}} \tag{4.2}$$

Where N is the number of elemens in the VCDL. The power consumption of the regulator is dominated by the power dissipated in M_{reg} (figure 4.2). The power dissipation of the opamp is neglected for now. The average current through M_{reg} is equal to the charge per LO period required to charge NC_L to V_{tune}:

$$I_{mreg,avg} = \frac{N V_{tune} C_L}{T_{LO}}$$

The power dissipated in M_{reg} is:

$$P_{mreg} = V_{ds,mreg} I_{mreg,avg} = (V_{DD} - V_{tune}) \frac{N V_{tune} C_L}{T_{LO}} \tag{4.3}$$

Adding (4.2) and (4.3) results in:

$$P_{total} = \frac{NV_{DD}V_{tune}C_L}{T_{LO}} \tag{4.4}$$

If the DLL is locked, $T_{LO} = NT_D$, the power as a function of the delay of a single delay element is:

$$P_{DE} = \frac{V_{DD}V_{tune}C_L}{T_D} \tag{4.5}$$

The thermal jitter of an voltage tuned delay element is [13]:

$$\sigma_t^2 = \left(1 + \gamma\frac{V_{tune}}{V_{tune} - V_T}\right)\frac{2kTC_L}{I_{peak}^2} \tag{4.6}$$

Where γ is the excess noise factor, V_T is the threshold voltage of the FET, k is the boltzmann constant and T is the temperature in kelvin. Jitter normalized to power is obtained by substitution of (4.5) and (4.6) into (3.4):

$$\sigma_{tnorP}^2 = \left(1 + \gamma\frac{V_{tune}}{V_{tune} - V_T}\right)\frac{2kTC_L^2V_{DD}V_{tune}}{I_{peak}^2T_D \cdot 1mW} \tag{4.7}$$

Equation 4.1 is rewritten to:

$$\frac{C_L^2}{I_{peak}^2} = \frac{4T_D^2}{V_{tune}^2}$$

and substituted into (4.7):

$$\sigma_{tnorP}^2 = \left(1 + \gamma\frac{V_{tune}}{V_{tune} - V_T}\right)\frac{8kTV_{DD}}{V_{tune} \cdot 1mW}T_D \tag{4.8}$$

4.2 Single Ended Current Starved Inverter

A current starved inverter (figure 4.1b) uses transistors M_{N2} and M_{P2} to reduce, or starve, the current available to charge or discharge the load capacitor. Hence the name current starved inverter. The minimum delay time is greater than that of the voltage tuned inverter because two transistors are stacked on top of each other. It is possible to obtain a rail-to-rail output and is therefore easily interfaced with switches. Examples are given in [4] and [15]. The logic threshold is $V_{DD}/2$ and with the other assumptions the same as the previous subsection the delay time can be obtained. The analysis for delay time, power and jitter normalized to power is follows the same procedure as the previous subsection. The delay time is:

$$T_D = \frac{V_{DD}C_L}{2I_{peak}} \tag{4.9}$$

The power dissipation of a VCDL employing current starved inverters is:

$$P_{VCDL} = N\frac{V_{DD}^2C_L}{T_{LO}} \tag{4.10}$$

The power in terms of delay time for a single delay element:

$$P_{DE} = \frac{V_{DD}^2 C_L}{T_D} \tag{4.11}$$

And just as in the previous subsection, the normalized jitter is deduced from [13].

$$\sigma_{tnorP}^2 = \left(1 + \gamma \frac{V_{DD}}{V_{tune} - V_T}\right) \frac{8kT}{1mW} T_D \tag{4.12}$$

In this analysis is assumed that M_{N2} and M_{P2} are the primary noise contributors, the contribution of M_{N1} and M_{P1} neglected.

4.3 Fully Differential

A fully differential delay element(figure 4.1c), sometimes called current mode logic(CML) or current steering logic, is based on a differential pair. The drain nodes are either discharged by the tail current or charged via the load resistance. The load resistance is realized by a PFET in triode, or by a symmetric load[6]. This circuit performs well under heavy power supply variation and substrate noise[6].
The delay time is once again obtained from [13]. The assumption are the same as for the voltage tuned delay element except the logic threshold. The logic threshold is $V_{OUT} = V_{OUT+} - V_{OUT-} = 0$. The delay time is:

$$T_D = \ln(2) R_L C_L \tag{4.13}$$

Tuning is done by varying the load. The voltage swing on V_{OUT+} and V_{OUT-} is $V_{sw} = R_L I_B$. For a tuning range of 1GHz to 10GHz this would result in a tenfold variation in voltage swing. Usually servo control on the current source is used to keep V_{sw} constant[6]. In this case (4.13) could be rewritten:

$$T_D = \ln(2) \frac{V_{sw} C_L}{I_B} \tag{4.14}$$

The delay time could be decreased by using a larger I_B, while keeping C_L and V_{sw} constant. However, the V_P in figure 4.1c should be high enough to keep the current source in saturation.
Due to the differential property of a fully differential delay element, a VCDL with N output phases, only requires N/2 fully differential delay elements. The negative output of a fully differential delay element is "free". The power dissipation of the VCDL is:

$$P_{VCDL} = \frac{N}{2} V_{DD} I_B \tag{4.15}$$

To obtain the power as a function of T_D, equation (4.14) is substituted in equation (4.15):

$$P_{DE} = \ln(2) \frac{N}{2} \frac{V_{DD} V_{sw} C_L}{T_D} \tag{4.16}$$

The factor N in equation (4.16) is intuitively caused by the static power dissipation of a fully differential delay element. For the single ended topologies this

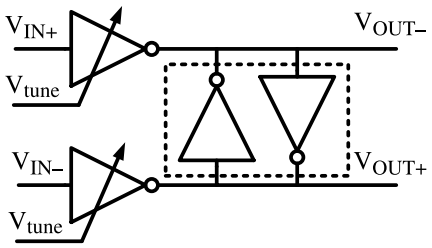


Figure 4.3: Reduction of skew between the positive and negative output by using cross coupled inverts that are weak in comparison to the delay elements.

factor is absent because they only dissipate power while switching.
The jitter is obtained from [13]:

$$\sigma_t^2 = \left(1 + \gamma + \frac{V_{sw}}{V_B - V_T}\right) \frac{2kTC_L}{I_B^2} \tag{4.17}$$

Where $V_B - V_T$ is the overdrive voltage of the NFET used as current source. Using equation (4.17), (4.16), (4.14):

$$\sigma_{tnorP}^2 = \left(1 + \gamma + \gamma \frac{V_{sw}}{V_B - V_T}\right) \frac{kTV_{DD}}{\ln(2) V_{sw} \cdot 1mW} T_D \tag{4.18}$$

4.4 Pseudo Differential

When two single ended delay elements are used to make a differential delay element, this is called a pseudo differential delay element. This delay element does not have the benefits of a reduced common mode effects like power supply variation and substrate noise [13]. Due to process variation, the drive strength of PFETs and NFETs are hard to match. To match the rising and falling edge at the output of the pseudo differential delay element more closely, weak cross coupled inverters are inserted between the positive and negative output as shown in figure 4.3[12]. The cross coupled inverters should be small enough that no regenerative latching occurs. A thorough analysis is not deemed necessary, because the analysis is already done on the single ended inverters. The weak cross-coupled inverters add some additional power dissipation and jitter as price to obtain some differential properties. A larger design margin should suffice.

4.5 Comparison

Jitter and Power

In table 4.1 the normalized jitter for different topologies are summarized. More or less the same conclusion could be made as is done in [13]: The current starved inverter has the best jitter performance for a given power budget, with the reasonable assumption that $V_{tune} < V_{DD}$ and $V_{sw} < V_{DD}$. This could

Topology	σ^2_{tnorP}
Voltage Tuning	$\left(1+\gamma\frac{V_{tune}}{V_{tune}-V_T}\right)\frac{8kTV_{DD}}{V_{tune}\cdot 1mW}T_D$
Current Starved	$\left(1+\gamma\frac{V_{DD}}{V_{tune}-V_T}\right)\frac{8kT}{1mW}T_D$
Fully Differential	$N\left(1+\gamma+\gamma\frac{V_{sw}}{V_B-V_T}\right)\frac{kTV_{DD}}{\ln(2)V_{sw}\cdot 1mW}T_D$

Table 4.1: Summary of the σ^2_{tnorP} of mentioned topologies

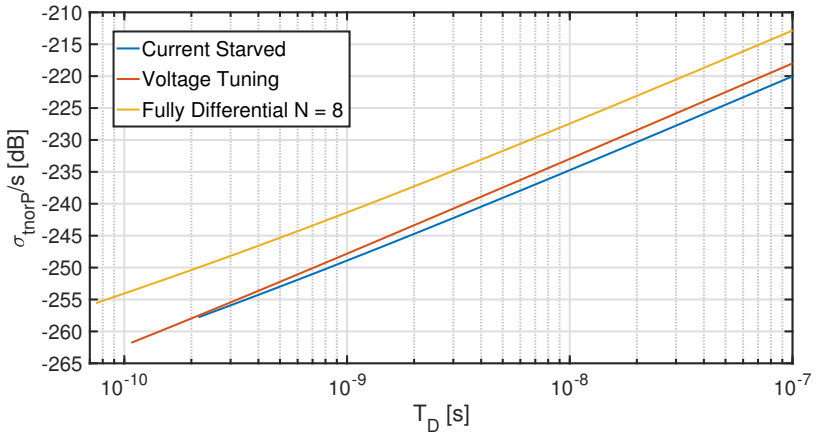


Figure 4.4: Normalized jitter

be attributed to the reduced swing of a voltage tuned inverter and the fully differential delay element. The foremost reason that the fully differential delay element has worse normalized jitter performance, is the dependency on the amount of required delay elements in the VCDL.

Speed

From the treated topologies, the current starved inverter has the least speed. This is due to the stack of four transistors that effectively lengthen the gate length. The voltage tuned inverter does not have this drawback and is therefore faster. For the fully differential topology, I_B is steered which allows high speeds.

Total

Table 4.1 is used to plot figure 4.4. The same parameters are used for fair comparison. The parameters are extracted from 22nmFDSOI. The following parameters are used: $C_L = 20fF$, $V_T = 0.38V$, $V_{DD} = 0.8V$, $T = 297K$, $\gamma = 3/2$, $W/L = 6$, $\mu C_{ox} = 0.7\mu A/V^2$, $V_{sw} = 0.4V$ and $V_B = V_{tune} = 0.39V..0.8V$. The reason that the fully differential delay element is plotted for N = 8, is because the characterization system requires 8 phases.
The reason that the fully differential delay element has significantly more normalized jitter, is due to the dependency on the number of phases. This dependency in turn is due to the static power dissipation. The foremost reason for using the fully differential delay element, is because it is the most immune to power supply variation and substrate noise.
If high speed and moderate thermal jitter and power supply rejection are required, it may be worth the increased complexity to chose the voltage tuned inverter. The circuits shown in figure 4.4 are not optimized for speed. As seen in figure 4.4, the speed requirements mentioned in chapter 3 are not met.
It should be noted that the delay in figure 4.4 T_D is varied by tuning voltage. It is also possible to tune the delay by increasing the load capacitance. Plotting this would not give us any additional information, because the normalized jitter is only indirectly dependent on C_L by T_D. Because the normalized jitter is plotted against T_D, the result would be a line with a slope of 10dB/decade.

4.6 Conclusion

If the speed allows it, current starved inverters should be used because of their high jitter performance. For fast operation and moderate power supply rejection and thermal jitter performance, the voltage tuned inverter could be chosen. For a large amount of delay elements, the fully differential topologies normalized jitter performance is severely degraded and should only be used if high immunity against supply variation and substrate noise is required.

Chapter 5

Charge Biased Delay Element

Charge biasing has proven to be more energy efficient for circuits employing differential pairs, like comparators, amplifiers and latches[16]. Charge biasing has been used in a delay interpolator[17], which claims an order of magnitude in power reduction but does not present any jitter performance. This chapter will treat the application of charge biasing in delay elements and their performance in terms of power, delay and jitter.

5.1 Fully Differential to Charge Biased Inverter

Charge Biased Differential Pair

An example of a charge biased circuit is shown in figure 5.1. The name "charge biased" probably originates from the replacement of the current source in figure 4.1c by a switched capacitor. Opinions on the pertinence of the name differ, since there is no actual bias point. Other names are charge steering and dynamic biasing[18].
There are two modes in which the circuit operates. If the circuit is used as com-

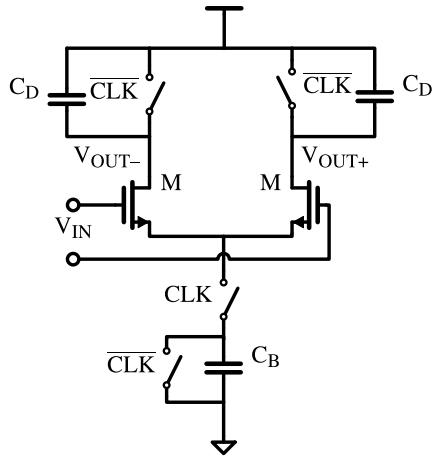
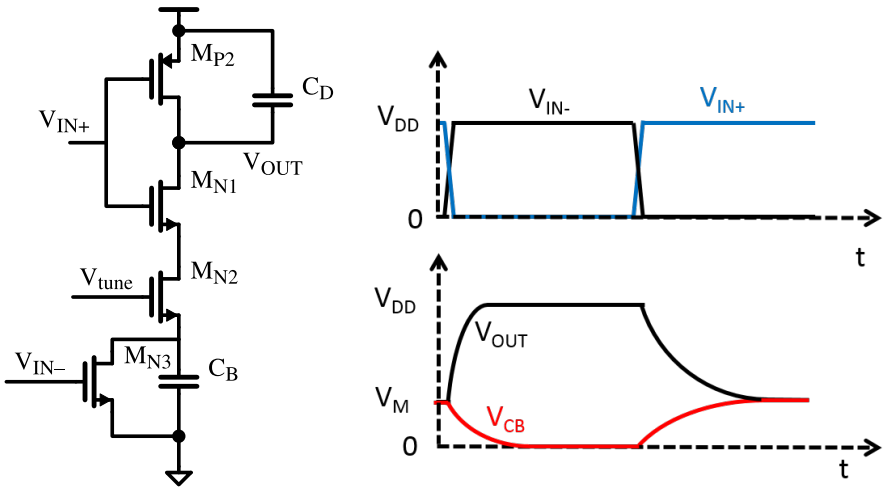


Figure 5.1: An example of a charge biased circuit



(a) (b)

Figure 5.2: Charge Biased Inverter a) circuit b) waveform

parator, these phases are called amplification mode and reset mode[16]. During the reset phase, the V_{OUT} nodes are charged to V_{DD} and C_B is discharged to ground. During the amplification phase, the V_{OUT} nodes are discharged at a rate depending on either differential and common mode of V_{IN} and results in a growing differential output voltage. The charge from C_D is moved to capacitor C_B, which quenches the differential input transistors. The current flowing through the differential pair reaches zero when V_{CB} reaches V_{CD}. Or the current becomes very small because the differential pair goes into weak inversion, $V_{GS} < V_T$. In both cased, the current reaches zero before V_{CD} becomes zero, generating no rail-to-rail signal.

Charge Biased Inverter

The property that makes a fully differential delay element popular, is its immunity against common mode variations, such as power supply variation and substrate noise. This property is achieved by the combination of a differential input and a differential output. The amplifier of figure 5.1 only satisfies these properties during the amplification phase. It is difficult to make a circuit based on charge biasing with the same differential properties as a fully differential delay element. It would likely require a lot of overhead which probably negates any reduction of power consumption. To investigate the properties of charge biasing in delay elements, a single ended approach is chosen. The circuit is made single ended and a tuning FET is added which result in the circuit in figure 5.2. There are a couple of difficulties associated with the circuit in figure 5.2 for application in a delay line.

- In deep sub-micron technologies, transistors M_{N1} and M_{N3} require a V_{GS} of zero to prevent the transistors from creating a conducting path to ground. Therefore V_{IN+} and V_{IN-} require a rail-to-rail swing.

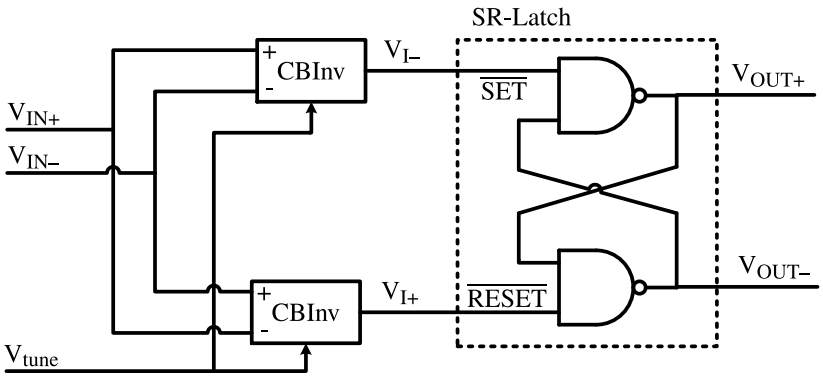


Figure 5.3

- The circuit requires a differential input clock and should therefore produce a differential output clock as well to allow cascading of multiple delay elements. Because the charge biased inverter only has a single ended output, a negative clock should be created somehow.
- The capacitors C_D and C_B require a reset before every clock edge.
- Only the high to low transition is delayed. This might be enough for some applications, for example time-to-digital converters. In this case it leads to problems, which are explained in chapter 6.

Most of the problems could be solved by time interleaving two charge biased delay elements followed by an SR-latch (figure 5.3). The implementation of the SR-latch is shown in figure 5.4. Assume an initial condition of $V_{OUT+} = 0$ and $V_{OUT-} = 1$. A positive edges arrives on V_{IN+} and a negative edge on V_{IN-}. V_{I+} goes high fast, but the latch retains the state due to the feedback from V_{OUT+} and M_{P4}. Then the delayed edge of V_{I-} pulls V_{OUT+} up by weaking the pull down network M_{N1} and increasing the pull up by M_{P1}. V_{OUT+} pulls V_{OUT-} down by M_{N4}. In this way, the SR-latch generates a differential output rail-to-rail output that could drive the next delay element. Furthermore, the latch is immune to the fast positive edges that reset C_D and C_B.

5.2 Charge Biased Inverter: A Quantitative Analysis

To compare the system in figure 5.3 against an existing system, a quantitative analysis is done. The idea is to obtain readable expressions for delay, power and jitter to gain insight in the performance of the charge biased inverter. If V_{IN+} and V_{IN-} switch infinitely fast at $t = 0^-$ and if its assumed that the output crosses the logic threshold within one period of V_{IN}, than the circuit of figure 5.2 could be stripped down to figure 5.5a. The initial conditions assumed are:

- $V_{out,cb}(0) = V_{DD}$

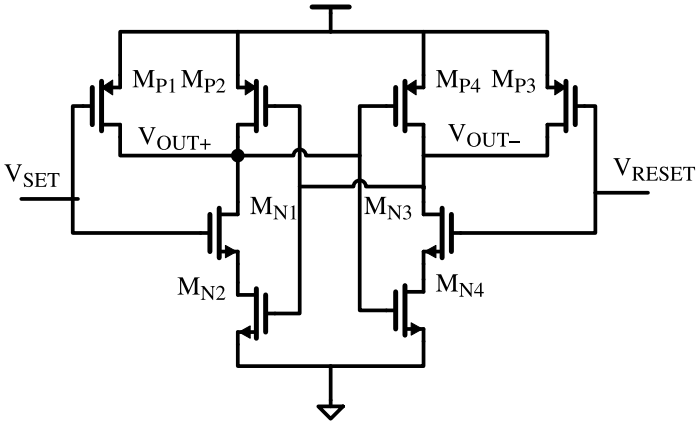


Figure 5.4

- $V_{IN}\,(0) = V_{DD}$
- $V_s\,(0) = 0$

Furthermore, it is assumed that M_{N1} and M_{N2} operate in saturation and strong inversion for $t < T_D$ for ease of calculations. M_{N1} is assumed as a cascode device of M_{N2} and does not influence the current through M_{N1} and M_{N2}. The charge biased inverter should be benchmarked against another delay cell. In this case is chosen for a current starved inverter because of the obvious similarities (figure 5.5b), for this circuit the same assumptions hold as mentioned for the charge starved inverter. Verification of this model based on simulations are shown in appendix A.

Output Voltage

In [19] calculation are done on a NFET with a capacitor between the source terminal and the ground like the combination of M_{N2} and C_B in figure 5.5a. Assuming no parasitic capacitances for a first order approximation, the drain current of M_{N2} and M_{N1} is the only current flowing from the power supply to ground. It is assumed that M_{N1} act as a cascode device and that the current is determined by M_{N2} From [19] (5.1) is obtained.

$$I_D(t) = \frac{K}{2}\left(\frac{(V_{tune} - V_{TH})}{\frac{(V_{tune}-V_{TN})Kt}{2C_B} + 1}\right)^2 \tag{5.1}$$

Here K is a constant depending on dimension and technology and $(V_{tune} - V_{TN})$ is the gate voltage minus the threshold voltage of the NFET. The output voltage V_{out} is given by:

$$V_{out,cb}(t) = V_{DD} - \frac{1}{C_D}\int_0^t I_D(\tau)d\tau \tag{5.2}$$

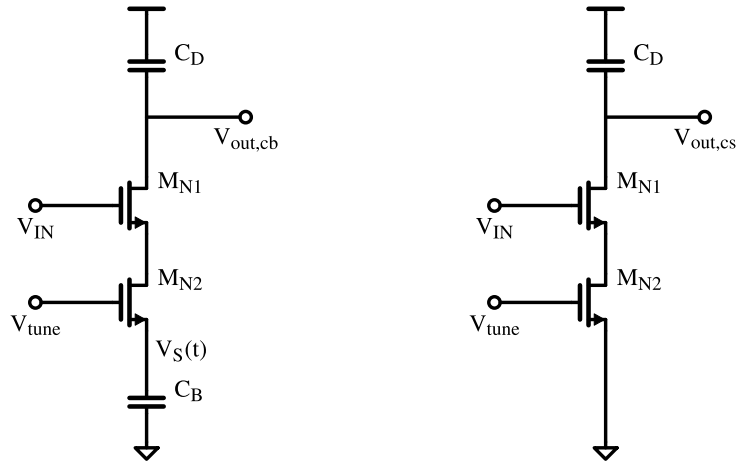


Figure 5.5: Circuits used in the quantitative analysis

Substition of (5.1) in (5.2) results in:

$$V_{out,cb}(t) = V_{DD} - \frac{1}{C_D}\int_0^t \frac{K}{2}\left(\frac{(V_{tune}-V_{TN})}{\frac{(V_{tune}-V_{TN})K\tau}{2C_B}+1}\right)^2 d\tau \tag{5.3}$$

By solving the integral and substitution of the initial condition $V_{out,cb}(0) = V_{DD}$ the following equation is obtained:

$$V_{out,cb}(t) = V_{DD} - \frac{K\left(V_{tune}-V_{TN}\right)^2 t}{2C_D\left(\frac{(V_{tune}-V_{TN})Kt}{2C_B}+1\right)} \tag{5.4}$$

Writing the term $\frac{K}{2}\left(V_{tune}-V_{TN}\right)^2$ as current $I_D(0)$ simplifies comparison with the current starved inverter:

$$V_{out,cb}(t) = V_{DD} - \frac{I_D(0)t}{C_D}\frac{2C_B}{\left(V_{tune}-V_{TN}\right)Kt+2C_B}. \tag{5.5}$$

The rightmost term in equation (5.5) is due to the quenching of transistor M_{N2}, this is seen by the time dependency of the denominator.

Delay Time

The delay time is calculated from (5.5) for the crossing of a certain threshold voltage $V_{DD}-V_{TP}$. Here V_{TP} is the threshold voltage of the PFET of the next stage.

$$V_{out,cb}\left(T_D\right) = V_{DD} - V_{TP}$$

After some manipulation:

$$V_{TP} = \frac{2I_D(0)T_DC_B}{K\left(V_{tune}-V_{TN}\right)C_DT_D+2C_DC_B}$$

Solving this equation for T_D leads to:

$$T_D = \frac{V_{TP}C_D}{I_D(0)} \frac{1}{1 - \frac{C_D V_{TP}}{2C_B(V_{tune} - V_{TN})}}$$

It is convenient to write the right term in the following way:

$$\rho = \frac{1}{1 - \frac{C_D V_{TP}}{C_B(V_{tune} - V_{TN})}} \tag{5.6}$$

Resulting in:

$$T_D = \rho \frac{V_{TP}C_D}{I_D(0)} \tag{5.7}$$

In equation (5.7) ρ is larger than one, because the denominator of (5.6) is always smaller than one and non-negative. In the limit of C_B to infinity ρ becomes one, the delay time equation reduces to that of a current starved inverter. This is a intuitive result, because C_B acts as a short for high frequencies.

Power

The power consumed by the circuit in figure 5.5a depends on drain capacitance C_D, the voltage swing on C_D and the clock period. From figure 5.3 follows that a chrage biased delay element requires two charge biased inverters. Because the delay element is differential, there is one "free" phase per element, doubling the power. Therefore, if N phases are required the power required by the VCDL (ignoring the latch[1]) is:

$$P_{VCDL} = N \frac{C_D V_{sw} V_{DD}}{T_{LO}} \tag{5.8}$$

Here T_{LO} is the period of V_{IN} and N is the number of required phases. The voltage swing V_{sw} is given by:

$$V_{sw} = \frac{C_B}{C_B + C_D} V_{DD} \tag{5.9}$$

Substitution of (5.9) into (5.8) yields:

$$P_{VCDL} = N \frac{C_D V_{DD}^2}{T_{LO}} \frac{C_B}{C_D + C_B} \tag{5.10}$$

The power per delay element is obtained by $T_{LO} = NT_D$:

$$P_{DE} = \frac{C_D V_{DD}^2}{T_D} \frac{C_B}{C_D + C_B} \tag{5.11}$$

Depending on the operation of the charge biased circuit, M_{N2} may go into weak inversion before an equilibrium between C_B and C_D is obtained. In this case V_{OUT} and V_s may not converge before the reset, depending on the

[1] In chapter 6 is explained that other delay elements require a buffer. The power of the latch is considered about equal to the power of a buffer, therefore the comparison to the current starved inverter still holds.

value of V_{tune}, reducing power consumption. However, care should be taken to not enter the weak inversion for the minimum value of V_{tune} if $t < T_D$. This greatly reduces the slope when $V_{out,cb}$ crosses the logic threshold and drastically increases jitter (later this chapter). The boundary condition for not entering weak inversion is given by:

$$V_{tune} - V_s(T_D) > V_{TN} \tag{5.12}$$

Where V_{TN} is the threshold voltage of M_{N2}. By conservation of charge:

$$V_s(t) = \frac{C_D}{C_B}\left(V_{DD} - V_{out,cb}(t)\right) \tag{5.13}$$

Substitution of $t = T_D$:

$$V_s(T_D) = \frac{C_D}{C_B} V_{TP} \tag{5.14}$$

Substitution of (5.14) into (5.12) and rewriting gives the boundary condition of V_{tune}:

$$V_{tune} > V_{TN} + \frac{C_D}{C_B} V_{TP} \tag{5.15}$$

The minimum voltage swing at $V_{out,cb}$ for proper operation dependents on the threshold voltage of the next stage. If the output voltage swing is too small, M_{P1} and M_{N2} (or M_{P3} and M_{N4}) in figure 5.4 will not overpower the positive feedback and fail to toggle the latch. Increasing the sizes of the PFET will result in an increase in capacitance C_D. The output voltage swing of the charge biased inverter is therefore limited by the SR-latch.

Jitter

In [13] a strategy is proposed to determine the jitter from different noise sources in a delay element. The jitter is obtained by:

$$\sigma_t = \frac{\sigma_v(T_D)}{S(T_D)} \tag{5.16}$$

Here, $S(T_D)$ is the slope of $V_{out,cb}$ evaluated at T_D, and σ_v is the voltage noise on $V_{out,cb}$.

$$S(t) = \frac{dV_{out,cb}}{dt} = -\frac{I_D(0)}{C_D}\left(\frac{2C_B}{K\left(V_{tune} - V_{TN}\right)t + 2C_B}\right)^2 \tag{5.17}$$

Substitution of (5.7) into (5.17) and some manipulation:

$$S(T_D) = -\frac{I_D(0)}{C_D}\left(1 - \frac{C_D V_{TP}}{2C_B\left(V_{tune} - V_{TN}\right)}\right)^2 \tag{5.18}$$

Noting that the term inside the square is equal to $1/\rho$, with (5.6) this yields:

$$S(T_D) = -\frac{I_D(0)}{\rho^2 C_D} \tag{5.19}$$

The reset switch parallel to C_D "samples" V_{DD}. This changes the initial voltage on the onset of discharging C_D and is directly translated to jitter. The standard deviation of the noise on C_D due to the switch parallel to C_D is given by:

$$\sigma_{v,sw} = \sqrt{\frac{kT}{C_D}} \tag{5.20}$$

Here k is the Boltzmann constant and T is temperature in kelvin. By substitution of (5.19) and (5.20) into (5.16), the jitter is calculated:

$$\sigma_{t,sw} = \frac{\rho^2\sqrt{kTC_D}}{I_D(0)} \tag{5.21}$$

The voltage noise due to M_{N2} (figure 5.5a), is obtained by a time domain analysis. The noise current is approximated by a pulsed sample and hold waveform with a period dt and a gaussian distributed amplitude with standard deviation σ_i and zero mean. Time instances are uncorrelated[13].

$$\sigma_i^2 = \frac{i_n^2}{2dt} \tag{5.22}$$

Equation (5.22) could be rewritten to give variance of the charge uncertainty:

$$\sigma_q^2 = \frac{i_{no}^2 dt}{2} \tag{5.23}$$

No constant is flowing through M_{N2} because of the charging capacitor C_B which quenches M_{N2}. Therefore, the associated noise current, i_n^2, is time dependent:

$$\frac{i_n^2(t)}{2} = 2g_m(t)\gamma kT \tag{5.24}$$

Because the noise is uncorrelated over time, $g_m(t)$ can be evaluated for every dt with the following equation:

$$g_m(t) = K\left((V_{tune} - V_{TN}) - V_S(t)\right) = K\frac{(V_{tune} - V_{TN})}{\frac{K(V_{tune}-V_{TN})t}{2C_B} + 1} \tag{5.25}$$

The total noise variance is obtained by substitution of (5.25) into (5.24) and substitution of that result into (5.23), which is integrated from $t = 0$ to $t = T_D$:

$$\sigma_{q(TOTAL)}^2(T_D) = 2\gamma kTK\left(V_{tune} - V_{TN}\right)\int_0^{T_D} \frac{dt}{\frac{K(V_{tune}-V_{TN})t}{2C_B} + 1} \tag{5.26}$$

Solving the integral and doing some manipulations result in:

$$\sigma_{q(TOTAL)}^2(T_D) = 4\gamma kTC_B \ln(\rho) \tag{5.27}$$

(5.27) is the total integrated noise charge on capacitor C_D. The voltage noise is obtained by:

$$\sigma_{v,cs} = \frac{\sigma_{q(TOTAL)}(T_D)}{C_D} = \frac{\sqrt{4\gamma kTC_B \ln(\rho)}}{C_D} \tag{5.28}$$

Dividing the voltage noise by the slope to obtain the jitter:

$$\sigma_{t,cs} = \frac{\rho^2 \sqrt{4\gamma kTC_B \ln(\rho)}}{I_D(0)} \tag{5.29}$$

The noise sources are uncorrelated and add up by root-mean-square:

$$\sigma_t = \sqrt{\sigma_{t,sw}^2 + \sigma_{t,cs}^2} \tag{5.30}$$

$$\sigma_t = \frac{\rho^2}{I_D(0)} \sqrt{kTC_D \left(1 + \frac{4C_B\gamma \ln(\rho)}{C_D}\right)} \tag{5.31}$$

Substitution of equation (5.31) and (5.11) into equation (3.4) and using $f = N/T_D$, were N is the number of elements, results in:

$$\sigma_{tnorP}^2 = \frac{\rho^4}{I_D^2(0)} kT \left(1 + \frac{4C_B\gamma \ln(\rho)}{C_D}\right) \frac{V_{DD}^2 C_D^2 C_B}{(C_D + C_B) T_D \cdot 1mW} \tag{5.32}$$

Rewriting equation (5.7) in the following way:

$$\frac{\rho^2 C_D^2}{I_D^2(0)} = \frac{T_D^2}{V_{TP}^2} \tag{5.33}$$

Substitution of equation (5.33) in equation (5.32) is done to obtain the form of (3.5):

$$\sigma_{tnorP}^2 = \frac{\rho^2}{V_{TP}^2} kT \left(1 + \frac{4C_B\gamma \ln(\rho)}{C_D}\right) \frac{C_B V_{DD}^2}{(C_D + C_B) \cdot 1mW} T_D \tag{5.34}$$

5.3 Comparison to Current Starved Inverter

By carrying out the same analysis on the current starved inverter, the following equations are obtained:

$$T_D = \frac{V_{TP} C_D}{I_D} \tag{5.35}$$

$$P_{VCDL} = N \frac{V_{DD}^2 C_D}{T_{CLK}} \tag{5.36}$$

$$P_{DE} = \frac{V_{DD}^2 C_D}{T_D} \tag{5.37}$$

$$\sigma_t = \frac{1}{I_D} \sqrt{kTC_D \left(1 + \frac{4\gamma V_{TP}}{V_{tune} - V_{TN}}\right)} \tag{5.38}$$

$$\sigma_{tnorP}^2 = \frac{kT}{V_{TP}^2} \left(1 + \frac{4\gamma V_{TP}}{V_{tune} - V_{TN}}\right) \frac{V_{DD}^2 N}{1mW} T_D \tag{5.39}$$

These equations differ slightly from the equations in section 4.2 because the logic threshold voltage in section 4.2 is chosen as $V_{DD}/2$. To compare the charge biased inverter more fairly to the current starved inverter, the logic threshold voltage in this section is chosen $V_{DD} - V_{TP}$.

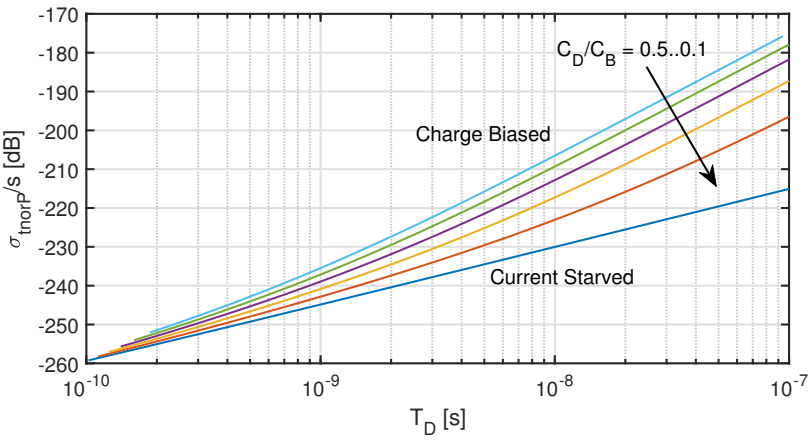


Figure 5.6: Normalized jitter for the charge biased inverter for different ratios of C_D/C_B and normalized jitter for the current starved inverter

Delay Time

Because the overdrive voltage on the tuning FET is quenched, the delay time of a charge biased inverter is intuitively always greater than the delay time of a current starved inverter. This is seen as well when equation (5.7) and (5.35) are compared. Recalling equations (5.6) and (5.7):

$$T_D = \rho \frac{V_{TP} C_D}{I_D(0)}$$

$$\rho = \frac{1}{1 - \frac{C_D V_{TP}}{C_B (V_{tune} - V_{TN})}}$$

For the circuit to operate properly, $\rho > 1$. As a result, $T_{D,cb} < T_{D,cs}$.

Power and Jitter

Since power and jitter are related, they can be compared by the jitter normalized to power. If the normalized jitter is lower than that of the current starved inverter, by impedance scaling the power of the charge biased invert could be reduced to obtain the same amount jitter.
In figure 5.6 the normalized jitter for different ratios of C_D/C_B is plotted along the normalized jitter of the current starved inverter. For a greater T_D, the charge biased inverter becomes considerably worse than the current starved inverter. For smaller ratios of C_D/C_B, the normalized jitter of the charge biased inverter starts approaching that of the current starved inverter. This is because in the limit of $C_B \to \infty$ the charge biased inverter behaves similar to the current starved inverter. The intuitive reason for the increase in jitter, comes from the definition of jitter (equation (5.16)). Due to the quenching of the transistors, the slope decreases considerably, resulting in more jitter. Figure 5.6 indicates that it is better to decrease the power consumption of a current starved inverter by impedance scaling than to use charge biased inverter.

5.4 Conclusion

Possibilities are analyzed to apply charge biasing in a voltage controlled delay line, resulting in the charge starved inverter. An analytic analysis is done to benchmark the charge starved inverter to a current starved inverter in terms of power, delay time and jitter. From the analysis and simulation is concluded that a charge biased delay cell is performing worse on all mentioned aspect, especially for jitter.

Chapter 6

Optimal Number of Delay Elements

This chapter treats some considerations on the design of a VCDL. Firstly, a short section is dedicated to the behavior of jitter in a VCDL. Secondly, the need for buffer between delay elements is explained and the power dissipated by the buffer is treated. In the last section, the aforementioned sections are used to argue what number of elements is best to obtain a certain delay in terms of jitter and power.

6.1 Thermal Jitter Accumulations

Thermal jitter is described by its standard deviation. At every delay element, jitter is added to clock edges that propagates through the VCDL (figure 6.1). Assuming that the thermal noise in each delay cell is uncorrelated, jitter adds with the variance. Therefore the jitter at the Nth cells is equal to:

$$\sigma_{t,N} = \sqrt{\sigma_{t,1}^2 + \sigma_{t,2}^2 + ... + \sigma_{t,N}^2} = \sqrt{\sum_{n=1}^{N} \sigma_{t,n}^2} \tag{6.1}$$

Where $sigma_{t,N}$ is the jitter at the output of the N-th tap of the delay element and $\sigma_{t,n}$ is the individual jitter contribution of the n-th element. If the delay elements are assumed identical, the standard deviation of jitter of jitter added

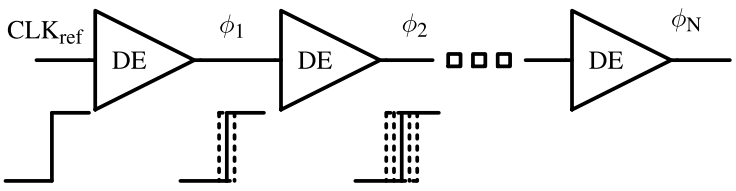


Figure 6.1: Jitter accumulation in a VCDL

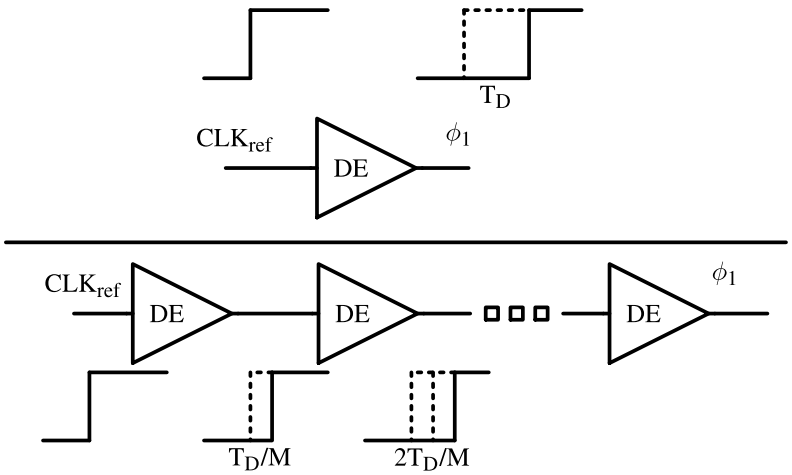


Figure 6.2: One delay element with a large delay time, or M delay elements with a short delay time

by each element is the same as well, resulting in:

$$\sigma_{t,N} = \sqrt{N}\sigma_{t,i} \tag{6.2}$$

Where $\sigma_{t,i}$ is the standard deviation of jitter for a single delay element.

6.2 Number of Elements

If a certain amount of delay is desired, this could be obtained by cascading multiple fast delay elements, or by just making one slow element. The freedom in this decision depends on the application and technology. This section explains the impact on thermal jitter if the same power budget is assumed (figure 6.2). To compare the thermal jitter of a cascade of M delay elements to one delay element, the capacitive load of the individual cascaded elements is divided by M. Since the power is linear depended on C, the power of M elements with a load of C/M remains the same. The jitter equation for a current starved inverter is[13]:

$$\sigma_t = \frac{1}{I_{peak}}\sqrt{kTC_L\left(1+\gamma\frac{V_{DD}}{V_{GS}-V_T}\right)} \tag{6.3}$$

Where I_{peak} is the peak current in the current starved inverter, k is the Boltzmann constant and T is the temperature in Kelvin. Using equation (6.3) with a load capacitance of C_L/M, the thermal jitter of an individual element in the cascade of a current starved inverter becomes:

$$\sigma_{t_i} = \frac{1}{I_{peak}}\sqrt{\frac{kTC_L}{M}\left(1+\gamma\frac{V_{DD}}{V_{GS}-V_T}\right)} \tag{6.4}$$

Where M is the number of delay elements. Substitution of equation (6.4) into equation (6.2) results in:

$$\sigma_{t_M} = \frac{\sqrt{M}}{I_{peak}} \sqrt{\frac{kTC_L}{M} \left(1 + \gamma \frac{V_{DD}}{V_{GS} - V_T}\right)} = \sigma_t \tag{6.5}$$

The left most M is due to jitter accumulation and the rightmost M comes from the fact the capacitive load is divided by M. The factor M cancels and equation (6.5) reduces to equation (6.3). This assumption is based on the scaling of area, W*L: $W \rightarrow W/\sqrt{M}$ and $L \rightarrow L/\sqrt{M}$. Where W is the the width of the device and L is the length of the device. If a square law model is used the voltage to current relation is described by:

$$I_{peak} = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{tune} - V_T\right)^2 \tag{6.6}$$

Where μC_{ox} is a technology constant. Instead of decreasing W and L. Only W could be reduced and $V_{GS} - V_T$ should be increased to compensate for the reduction in I_{peak}. In this case: $W \rightarrow W/M$ and $V_{GS} - V_T \rightarrow (V_{GS} - V_T)\sqrt{M}$. The rightmost term of equation (6.3) equation becomes:

$$\sigma_{t_{N,cs}} = \frac{\sqrt{M}}{I_{peak}} \sqrt{\gamma \frac{C_{load} V_{DD}}{M\sqrt{M}\left(V_{GS} - V_T\right)}} \tag{6.7}$$

The $\sqrt{M}$ falls out. Resulting in the following relation:

$$\sigma_{t_{M,cs}} \propto \frac{1}{\sqrt[4]{M}} \tag{6.8}$$

From this derivations follows that it is better for in terms of jitter to use more delay elements with higher overdrive voltage, than one delay element which is tuned to a large delay by decreasing the overdrive voltage. This observation excludes the fully differential implementation, because the normalized jitter increases with the number of elements.
A graphical interpretation could be obtained from figure 6.3. By cascading M elements, the delay time increases by M. For $M = 10$ this corresponds to the horizontal arrow shown in figure 6.3. According to equation (6.2), the jitter increases with $\sqrt{M}$. Using M more elements increases the power by M and since $\sigma^2_{tnorP} = \sigma_t^2 P/1mW$, the total increase in jitter is M. This corresponds to the vertical arrow shown in figure 6.3. The log-log scale of figure 6.3 simplifies graphical representation of the multiplication, because it is a linear shift in the plot. From figure 6.3 it is easily seen that it is better to cascade N delay elements than to increase the delay of one element, if the slope of the normalized jitter is larger than 10dB/decade. The normalized jitter for a fully differential element increases with M^2, because the normalized jitter itself is already linearly dependent on N. This requires the slope of the normalized jitter to be larger than 20dB/decade. In figure 6.4 and figure 6.5 the slope is plotted, none of the slopes is smaller than 10dB/decade, therefore it is advantageous to cascade more delay elements, instead of reducing the delay time of one element. Especially the charge biased inverter hugely benefits from reducing the delay and cascading multiple elements. This could be seen from figure

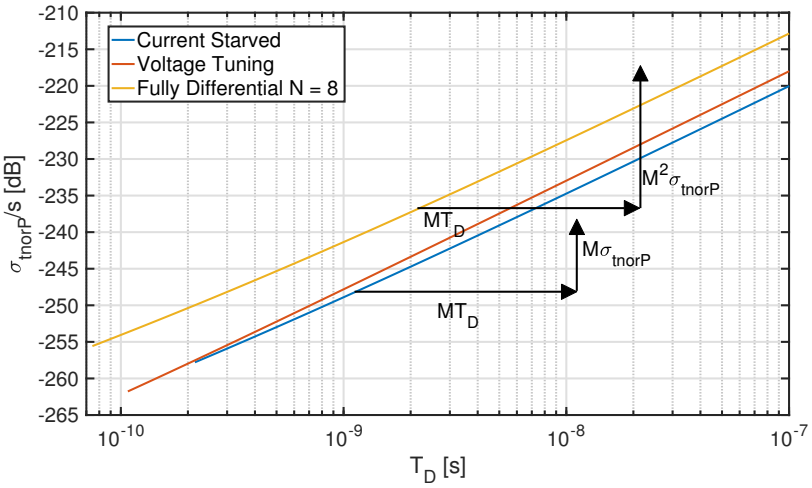


Figure 6.3: Cascading N elements

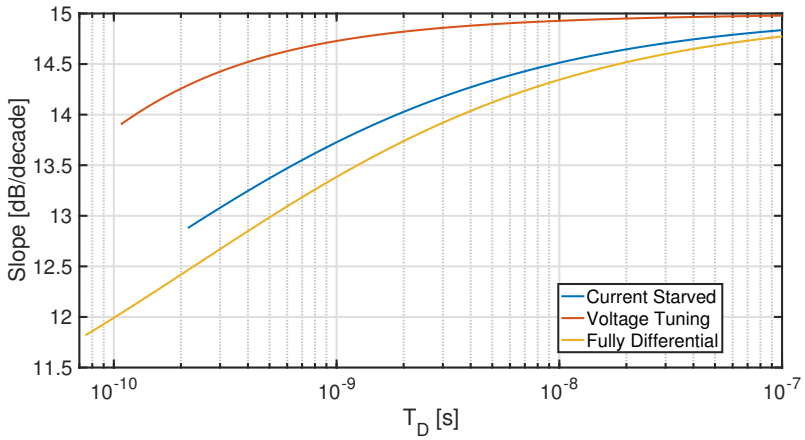


Figure 6.4: Slope of the normalized jitter for different topologies

6.5 where especially the at large delay times the slope goes to 30dB/decade. However, the charge biased inverter has a relatively long minimum delay time. Therefore the amount of cascaded elements possible for specified speed is less than that of the current starved inverter.

6.3 Duty-Cycle

Due to process variations, NFETs and PFETs are difficult to match. As a result, the current starved inverter and the voltage tuned inverter do not have a 50% duty-cycle. The deviation of the 50% duty-cycle is called duty-cycle error. This is illustrated in figure The problem with the buffered delay elements, is that the duty-cycle error accumulates through the VCDL. If too many elements

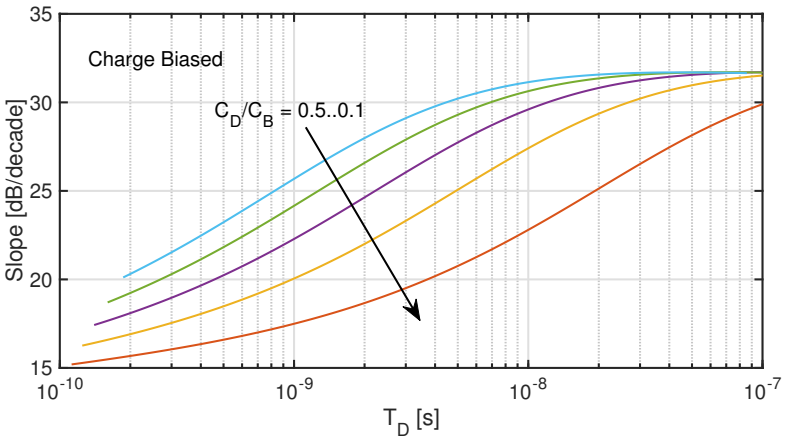


Figure 6.5: Slope of the normalized jitter of a charge biased inverter for different value of C_D/C_B.

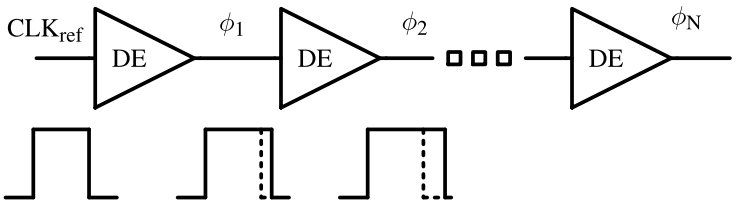


Figure 6.6: Duty cycle error due to different drive strength of NFET and PFET

are cascaded, the duty-cycle approaches 0% or 100% where no switching occurs any more. If the VCDL is pseudo-differential, the weak cross-coupled inverters will reduce the duty-cycle error.
In case of a current starved inverter, current mirrors could be used to make the charge and discharge current equal. However, second order effects like channel length modulation and parasitic capacitances at the drain nodes of the current sources result in a duty-cycle error which becomes more severe at higher operating frequencies.
If the accumulated duty-cycle error is too high, it poses a limit on the maximum amount of delay elements that could be used (figure 6.6).
The charge biased delay element does not suffer from duty-cycle error, because rising edge and falling edge both depend on the delay of an NFET.

6.4 Conclusion

This chapter shows that jitter for a given power becomes better for cascaded delay elements than a reduced delay of a single delay element. This applies for the voltage tuned inverter, current starved inverter and especially for the

charge biased inverter. For the fully differential delay element the optimum is at the least amount of delay elements: N/2, where N is the amount of desired phases. The maximum number of delay elements for the voltage tuned inverter and current starved inverter depends on the minimum possible delay and the tolerated duty-cycle error. The charge biased delay elements does not suffer from accumulated duty-cycle error, however its maximum number of delay elements depends on the minimum possible delay, which is relatively large.

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

Literature research has been done to look at the jitter, power and speed specifications of different delay element topologies.
It is shown that the current starved inverter has the least jitter for a given power consumption, but is slow in comparison to a fully differential topology an voltage tuned inverters. Furthermore, the complexity to implementing a current starved inverter could be designed with rail-to-rail output and is therefore easily interfaced with switches, the voltage tuned inverter and the fully differential topology require level shifters. The tuning of the voltage tuned inverter is usually done by a linear regulator, which increases the complexity and may reduce the bandwidth of the DLL.
A delay element based on charge biasing is investigated. The first thing to investigate was finding a way to apply charge biasing in a delay element. This resulted in the charge biased inverter. This inverter is only capable of delaying either negative or the positive edge, therefore two are required in parallel follow by an asynchronous SR-latch. The SR-latch generates a pseudo-differential rail-to-rail signal, which is needed to drive the charge biased inverter and ensures a 50% duty-cycle at the output of the delay element. The charge biased inverter does not dissipate static power.
The delay of delay elements is slope dependent, as a result the delay compared to the delay of the previous element increases. To restore the slope after a delay element, buffers are inserted between the elements. In case of the charge biased delay element, the SR-latch could act as buffer.
It turns out that the jitter for a given power for a charge biased delay element is greater than the jitter of a current starved inverter and that the speed of a charge biased delay element is less than that of a current starved inverter. No level shifters are needed, which is a advantage with respect to the fully differential delay element and the voltage tuned inverter.
From chapter 6 follows that it is advantageous for jitter normalized to power, to cascading delay elements instead of reducing the delay of a single element. This only holds if the delay element does not dissipate static power and is therefore not applicable to fully differential delay elements.

7.2 Recommendations

No jitter specification is given for the system in chapter 2. A worse case scenario is easily estimated, but is presumably far too conservative. The sampling mixer has a kind of build-in averaging and the DLL might reduce some of the jitter in certain topologies. Also digital averaging might increase the tolerated amount of jitter. In other words, there are a lot of system considerations that might increase the toleration to jitter in this system. If the tolerated jitter for a certain effective number of bits is known, the increase in jitter would reduce the power consumption of the delay elements. This could be done either by a mathematics or by simulations.
For specific ultra-low power cases where the supply voltage is minimized, the speed of a charge biased inverter could be increased beyond that of a current starved inverter, by resetting the bias capacitance to a negative voltage. In this case, the SR-latch is likely the bottleneck for speed, therefore other ways should be investigated to delay the positive and the negative edge.

Appendix A

Charge Biased Delay Element Model Verification

The purpose of this appendix is to verify that the charge biased delay element model is correct and applicable in practical situations. This is done by limit checks, a proof and simulations.

A.1 Limit Checks

If the bias capacitor C_B goes to infinity, it effectively acts as a short and should obtain the same result as the current starved inverter. The equations for voltage, delay and jitter are checked. Most of the limit checks are really straightforward and are listed below.

$$V_{out,cb}(t) = V_{DD} - \frac{I_D(0)}{C_D} \frac{1}{\frac{(V_{tune}-V_{TN})Kt}{2C_B} + 1} \tag{A.1}$$

$$\lim_{C_B \to \infty} V_{out,q}(t) = V_{DD} - \frac{I_D t}{C_D} = V_{out,i}(t) \tag{A.2}$$

$$T_{D,q} = \frac{1}{1 - \frac{C_D V_{TP}}{C_B(V_{tune}-V_{TN})}} \frac{V_{TP} C_D}{I_D(0)} \tag{A.3}$$

$$\lim_{C_B \to \infty} T_{D,q} = \frac{V_{TP} C_D}{I_D(0)} = T_{D,i} \tag{A.4}$$

$$\sigma_{t,cb} = \frac{\rho^2}{I_D(0)} \sqrt{kTC_D \left(\frac{4\gamma C_B \ln(\rho)}{C_D} + 1 \right)} \tag{A.5}$$

$$\rho = \frac{1}{1 - \frac{C_D V_{TP}}{C_B(V_{tune}-V_{TN})}} \tag{A.6}$$

Part of the limit check for the jitter FOM, equation (A.10) is self-evident:

$$\lim_{C_B \to \infty} \rho = 1 \tag{A.7}$$

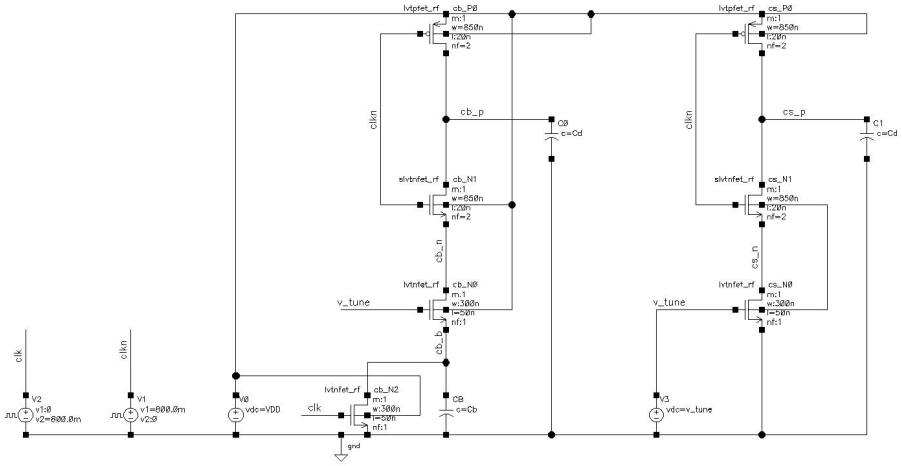


Figure A.1: Simulation Setup

The not so self-evident part is obtained by wolfram alpha:

$$\lim_{x\to\infty} x \ln(\frac{1}{1-\frac{a}{x}}) = a \tag{A.8}$$

using this in the equation (A.5)

$$\lim_{C_B\to\infty} C_B \ln(\rho) = \frac{C_D V_{TP}}{V_{tune} - V_{TN}} \tag{A.9}$$

$$\lim_{C_B\to\infty} \sigma_{t,cb} = \frac{1}{I_D(0)} \sqrt{kTC_D \left(\frac{4\gamma V_{TP}}{V_{tune} - V_{TN}} + 1 \right)} = \sigma_{t,cs} \tag{A.10}$$

A.2 Simulations

Simulation Setup

The validation circuit is shown in figure A.1. The parameters used are:

- $V_{DD} = 0.8V$
- $V_{tune} = 0.7V \to 0.8V$
- $T_{clk} = 1ns$
- $C_D = 15fF$
- $C_B = 30fF$
- $V_{TP} = 0.42V$
- $V_{TN} = 0.36V$

	Charge Starved	**Current Starved**
Analysis	$6.4\mu W$	$9.6\mu W$
Simulation	$7\mu W$	$10.7\mu W$

Table A.1: Analysis compared to simulations of power consumption

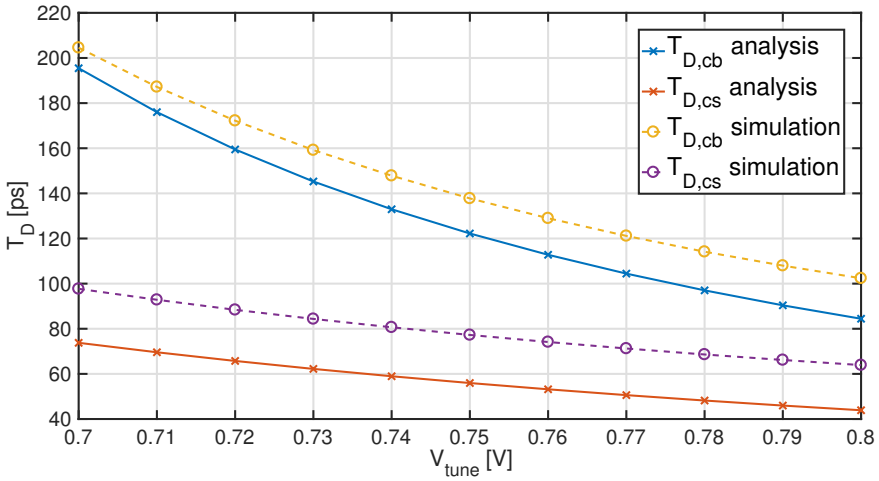


Figure A.2: Analysis compared to simulations of the delay time

Simulation Results

In table A.1, figure A.2, figure A.3 and figure A.3, the simulation results are plotted alongside the predicted results from the chapter 5. Errors are expected, because a quadratic model is not accurate for deep sub-mircon technology. From the previous mentioned figures is concluded that the analytic model is accurate enough to provide insight in the performance of a charge biased inverter. In figure A.3 and figure A.3 the jitter contributions not taken into account in the analysis are also shown. The analysis provides an optimistic result, therefore designs based on this analysis should always be checked by simulations.

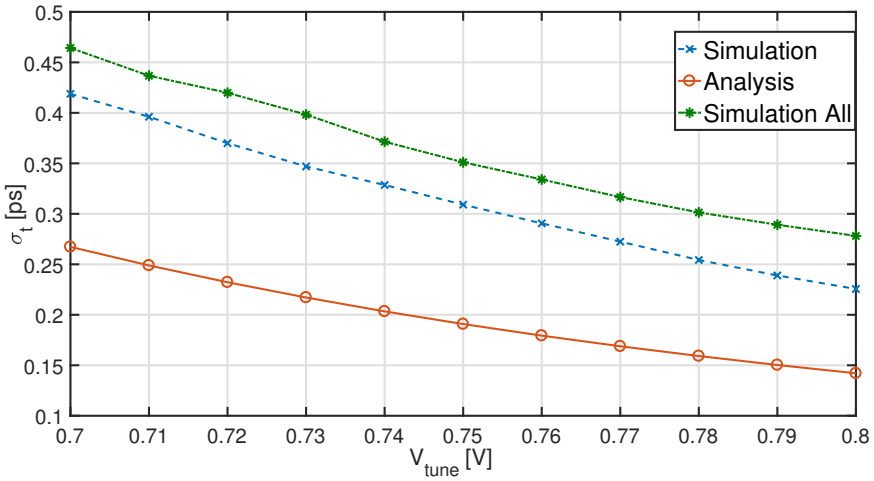


Figure A.3: Analysis and simulations of jitter from the current starved inverter; With only noise contributions of the current source and the reset switch and with all noise sources.

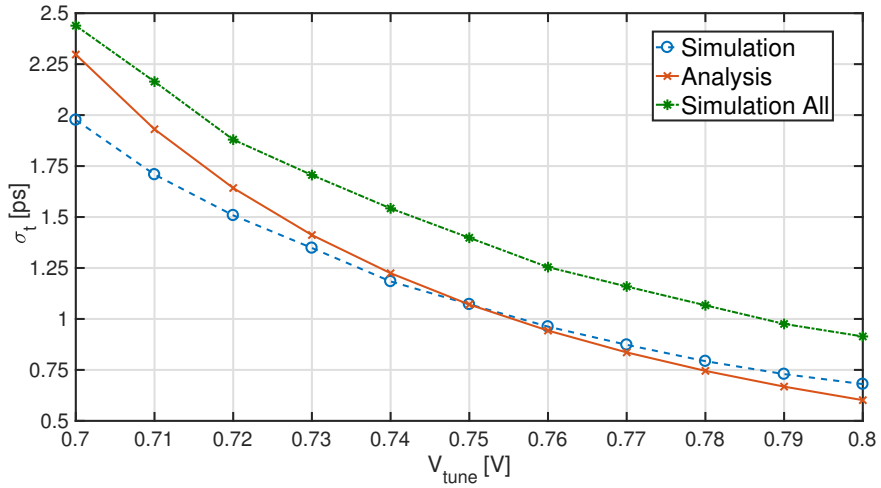


Figure A.4: Analysis and simulations of jitter from the charge biased inverter; With only noise contributions of the current source and the reset switch and with all noise sources.

A.3 Conclusion

The simulations show that the model is good enough for the purpose of insight. Furthermore, some limit checks are done to verify the validity of the model.

Appendix B

Buffers

B.1 Delay Modulation

Up until now, all calculations done on delay elements assume a infinitely sharp input edge. Moreover, it was assumed that the peak current is reached instantly. When directly cascading delay elements, this is not the case. Directly cascading elements will not work if equidistant phases are required. This is because the delay of a delay element depends on slope as well. As an example, a low to high transition in a current starved inverter is considered. First of all, when the threshold voltage of the NFET is crossed, it takes finite time to reach the voltage corresponding to the peak current. Secondly, until the input voltage reaches the threshold voltage of the PFET, the PFET supplies current from V_{DD}, effectively reducing the current flowing out of the load capacitance; increasing delay and power consumption. Cascading multiple elements results in a accumulation of the delay error, which is visualised in figure B.1.

B.2 Buffer

To resolve the problem of slope dependent delay, buffers are inserted between delay elements as shown in figure B.2. These buffers restore the lowered input slope to a steep output slope. Because for all the treated topologies in chapter 4 buffers are required, the buffers are not taken into account in the comparison.

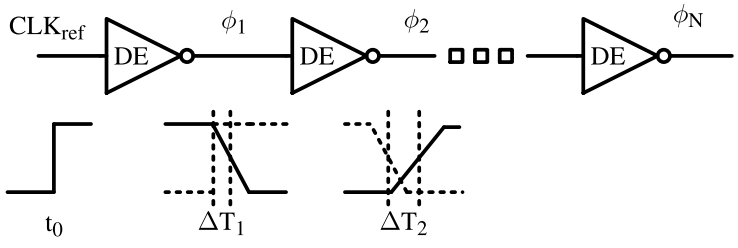


Figure B.1: The effect of the slope of the input on the delay time

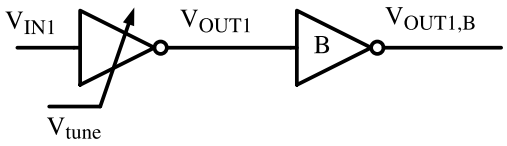


Figure B.2: Bufferd delay element

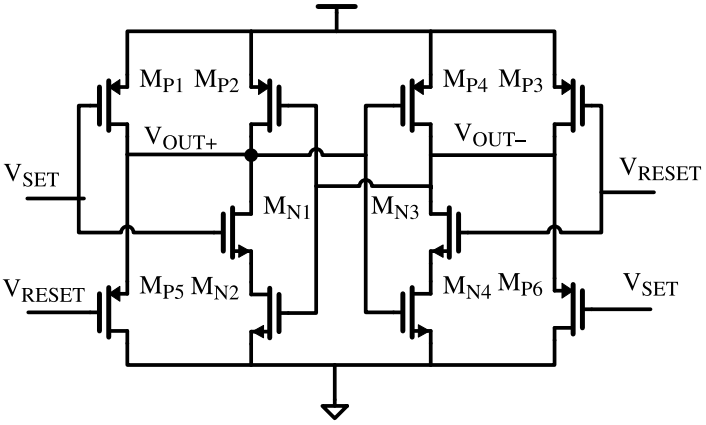


Figure B.3: PFET parallel to the pull down network of a SR-latch

However, when designing a VCDL for a given power budget, they should be taken into account because of their considerable power consumption due to their short circuit current [20].

B.3 Latch

A buffer is not needed in the case a charge biased inverter is used, because the latch acts as buffer. Generally the latch has worse driving capability compared to an inverter buffer due to the self-loading of the cross coupled inverters.
Between the positive and negative phase of the latch is some skew. This is because the high to low transition is initiated by the opposite phase of the latch. This skew could be reduced by putting a PFET parallel to the pull-down network as shown in figure B.3.

B.4 Jitter

The inherent function of the buffer is to make the edges of the output of the delay element more steep. Because jitter is inversely proportional to the slope,

it is assumed that jitter added by the buffer is negligible compared to the delay element.

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