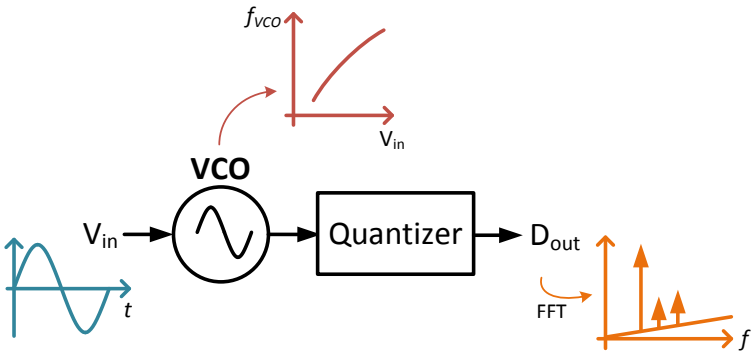
UNIVERSITY OF TWENTE.

Faculty of Electrical Engineering,
Mathematics & Computer Science

Distortion analysis of Voltage-Controlled Oscillator-based Analog-to-Digital Converters



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I Abstract

In this work, Analog-to-Digital Converters (ADCs) based on a Voltage-Controlled Oscillator (VCO) were analyzed on distortion performance. It is widely known that the performance of these ADCs is limited by the VCO nonlinearity. Since this is the most limiting factor, this MSc project was focused on the linearity of VCOs, at which a distinction was made between static distortion and dynamic distortion. The static distortion was determined from the actual (nonlinear) VCO control characteristic, that was obtained by simulations at several fixed (static) input voltages. The dynamic distortion was determined from frequency spectra with a sinusoidal input voltage to indicate frequency dependent distortion. In order to cancel the VCO nonlinearity by digital calibration, the frequency dependent distortion also known as memory effects, should be lower than 0.1 dB to gain 40 dB in performance.

Before the VCO nonlinearity was analyzed and simulated on circuit level, high-level system simulations of VCO-based ADCs were performed. They show beside the desired operation of the system, an interesting aspect of this kind of ADCs, namely the inherent first-order noise shaping. Since the phase of the VCO is a continuous signal and sampled for the A/D conversion, the residual phase at a current sampling period becomes the initial phase of the next sampling period. This introduces the first-order noise shaping. With ideal building blocks on high-level it was shown that the VCO-based ADC generates no distortion. However, by adding a small amount of nonlinearity to the voltage-to-frequency gain K_{VCO} to the ideal ADC, the performance was significant decreased.

Regarding the static distortion on circuit level, the proposed ring VCO from former MSc project was analyzed and simulated. The mathematical analysis showed that the VCO nonlinearity was caused by the nonlinear V-I characteristics of the MOS transistors. Several alternative VCO circuits were treated and compared to the proposed ring VCO and the proposed ring VCO achieved the highest performance qua static distortion in comparison with the alternatives. Nevertheless, the proposed VCO needs an input buffer, which cannot be implemented easily without influencing the overall static distortion performance. The saw-tooth oscillator, which is a completely different oscillator, is an interesting alternative, because it rendered only 1.6 dB more static distortion than the proposed ring VCO while it does not need an input buffer.

The proposed ring VCO and the saw-tooth oscillator were also analyzed on frequency dependent (dynamic) distortion. Since determining the instantaneous VCO frequency by time periods rendered distortion issues, a frequency quantizer was implemented to investigate the dynamic distortion of VCOs. Single-tone simulations of the proposed ring VCO and the saw-tooth oscillator showed distortion results that correspond to the static distortion results. Two-tone simulations were performed with both circuits to indicate memory effects, where it turned out that the variations of the distortion terms cannot easily be related to these effects. Several other methods were explored to indicate memory effects, but without successful results.

II Preface

This report describes the results of the master thesis project, performed at the University of Twente. It is the final project of the master Electrical Engineering curriculum at the same university. It describes the results of my activities within the research group Integrated Circuit Design, the ICD group. This report includes the research objectives, methods, final results and conclusions.

The Integrated Circuit Design group does research on integrated transceivers in CMOS technology. These transceivers become more and more digital, however Analog-to-Digital Converters (ADCs) are still needed to communicate with the analog world. Therefore, this investigation provides more insight in the distortions of so-called Voltage-Controlled Oscillator-based ADCs (VCO-based ADCs), which might become one of the interesting ADCs in the future.

This report is dedicated to the supervising committee of my master thesis project. I would like to thank the head of the ICD group prof. dr. ir. B. Nauta for giving me the opportunity to graduate with a master's degree at his research group. The daily supervisor was dr. ing. E.A.M. Klumperink, and I am thankful for his great supervision. He made this project possible and his knowledge, practical insight and suggestions for improvements were of great value to me. Also I would like to thank dr. ir. A.J. Annema for the many interesting discussions about project issues.

M. Besselink
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III Table of Contents

1 Introduction

Analog-to-Digital Converters (ADCs) which are based on a Voltage-Controlled Oscillator (VCO) have attractive assets and might become one of the interesting converters in the future. The implementation of high-bandwidth and high-resolution ADCs becomes more challenging for circuit designers. The converters that have currently the best performance based on bandwidth and resolution are the sigma-delta (ΣΔ) ADCs and the pipeline ADCs [1]. However, the dynamic range of these converters is difficult to maintain when the power supply is decreasing by CMOS scaling. The reduction of technological dimensions has led to power supply reductions from 5 to currently 1 V. According to this trend the supply voltages will be extended towards 0.6 V in the year of 2020 [2]. On the other hand, new CMOS processes offer fast switching speed and higher density of transistors per unit area. Thus, we could lose some dynamic range, but instead gain some more operating speed and make circuits more digital. VCO based ADCs are therefore more attractive to future A/D conversion solutions, because they are largely digital!

1.1 Background

A VCO-based ADC is an Analog-to-Digital Converter which converts the analog voltage at first to time information and then quantizes it in time. The first step takes place by using a so-called VCO, that gives an output frequency which is proportional to the analog input voltage or current. Next, the output of the VCO can be quantized by using a digital time quantizer. On the other hand, conventional ADCs convert their signals in the voltage or current domain, where their input signals are sampled and quantized in the same domain by using analog processing. The basics of VCO-based ADCs are treated in recently published books [3] [4].

One of the first reported VCO-based ADCs was proposed more than 30 years ago in the superconducting industry [5]. The proposed ADC consists of a quantizer and bit scalers, and were made with superconducting materials. Nowadays, we have VCO-based ADCs that have corresponding building blocks, namely the quantizer, counter and register. Although the implementation of both converters are different in technology (superconductors versus CMOS), the overall architecture is almost the same.

Later in the year of 1997, a design of a second-order delta-sigma modulator was published, which uses frequency modulation [6]. The first integrator in that design was replaced by a frequency modulator, and had the modulating signal as input. The design resulted in a simple delta-sigma modulator with no need for feedback. It became clear that this design does also have the advantages of the delta-sigma noise shaping. It was mathematically proven that the truncation error at the end of a clock period was not lost, but was accounted in the following clock period. This could be seen as quantization noise of the modulator, that is first-order noise-shaped. The main disadvantage of the proposed circuit is the nonlinearity of the VCO. The relation from the analog input signal to the frequency of the VCO turns out not to be highly linear, and add distortions directly to the signal.

In 2006, a design of a time-based ADC was published, which used a multi-phase VCO to enhance the quantizer's resolution [7]. The design is based on a ring VCO to provide multi-phase outputs and a phase quantizer which consists of a counter and phase detector to improve the resolution. The counter quantized the input signal by π, and the phase detector quantized the residual phase with a

resolution of π/N, where N represents the number of stages of the ring VCO. The linearity of the VCO is still the main bottleneck in this design.

A time-based bandpass ADC was introduced in 2008, where the proposed architecture provides a bandpass function by time-interleaving first-order VCO-based ADCs [8]. By using time-interleaving, the noise transfer function of the ADC was modified from a high-pass to a bandstop characteristic. From this inherent characteristic, the operating speed of each VCO-based ADC is reduced with more interleaving. In addition, the SNR due to harmonic distortion can be increased by using a higher number of interleaving. The disadvantages of this design by using more interleaving are the increased complexity, more mismatch effects and more power consumption.

In the past, the VCO-based ADCs found also their application in the sigma-delta (ΣΔ) ADCs (or also called ΣΔ modulators). The quantizer in a ΣΔ ADC is replaced by a VCO-based ADC, which provides one more order of noise shaping to that of traditional ΣΔ ADCs [9]. The results of this design suffered from harmonic distortion caused by nonlinearity of the VCO, and there was still need of a Digital-to-Analog Converter (DAC) in the feedback path, which was quite critical and complex to design. One year later this circuit was redesigned to eliminate the DAC in the feedback path by using a frequency detector [10]. Despite the fact that the DAC with the static and dynamic component matching was eliminated, the nonlinearity of the VCO remained an issue in the degradation of the Signal-to-Noise-and-Distortion Ratio (SINAD). Even by using a loop filter with a high gain (50 dB) to suppress the VCO nonlinearity, it still remains the dominant distortion in continuous-time ΣΔ VCO-based ADCs [11].

In 2010, a digital calibration method was developed to enhance the dynamic range of VCO-based ADCs [12]. They generate a ramp signal once at the input of the VCO-based ADC and store the samples in a lookup table which, in fact, is the inverse transfer function of the VCO tuning curve. During operation the digital output is mapped in the lookup table to its corresponding address and the calibrated output is produced. After calibration, the dynamic range of small and large input signals was improved with 40 and 60 dB, respectively.

From that moment, many people used calibration techniques to improve the dynamic range of VCO-based ADCs. Digital calibration based on a least mean square algorithm was introduced [13]. To improve the resolution further, interpolation techniques were used at the same time with digital calibration [14] [15]. Also digital calibration with temperature compensation was developed [16]. An architecture was designed which makes the linearity of the whole ADC independent of the VCO linearity, by using Pulse Width Modulation (PWM) precoding [17]. Even calibration with self-cancelling dither techniques were used in continuous-time ΣΔ VCO-based ADCs [18] [19]. These converters obtain a Figure of Merit (FOM) of 123 fJ/conv. (depending on sampling frequency and bandwidth), which is quite state-of-the-art nowadays.

1.2 Research Scope

As it was discussed in previous paragraph, the performance of VCO-based ADCs is mostly limited by the nonlinearity of the VCO. The dynamic range can only be increased by implementing some kind of complex and power consuming calibration technique. On the other hand, the resolution of these ADCs is limited with current architectures. Therefore, many IC designers are working on new VCO-based ADC architectures to enhance its performance without the expenses of speed, power consumption, noise, etc.

Last year, the ICD research group of the University of Twente proposed an idea to improve the resolution of VCO-based ADCs. The idea was to generate a signal which is a linear representation of the instantaneous VCO phase. This can be seen as generating a signal which starts linearly to increase at the beginning of a VCO phase and resets to zero at the end (2π) of the VCO phase. In fact, such a signal has a saw-tooth shape and a period of 2π. At the sampling moments of the A/D conversion, that saw-tooth signal is sampled at a certain moment and the height of that signal represents a part of the VCO phase which belongs to previous A/D conversion. This approach makes it possible to increase the resolution substantially compared to conventional VCO-based ADCs which uses multiple phases with counters. By this new design the resolution is limited to the accuracy of generating and sampling the saw-tooth signal rather than the number of interleaved VCO phases.

This new design was investigated last year by a master student at the ICD research group. He worked on different techniques to generate linear phases of VCO-based ADCs [20]. The results of that MSc work was a high level design of a new VCO-based ADC, where certain building blocks were implemented on circuit level (but not all). This new design consists of a coarse path for the coarse A/D conversion and a fine path for the fine A/D conversion. The block diagram of the design is shown in Figure 1.

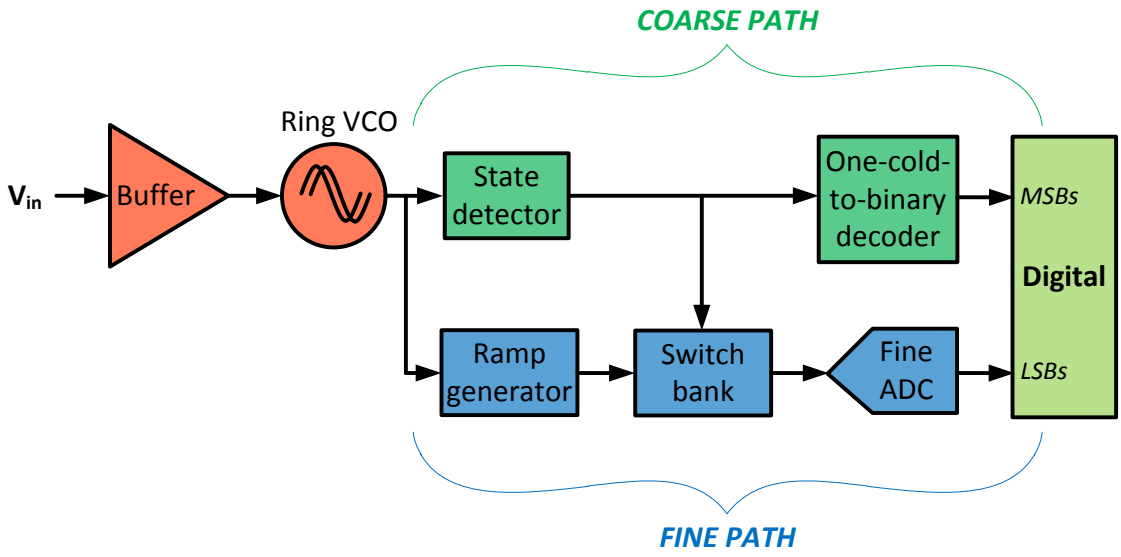

Figure 1: Block diagram of a new VCO-based ADC design with linear phase generation technique.

The Analog-to-Digital Converter is based on a ring VCO, which forms the essence of this converter. By using a ring VCO with multiple output signals, the coarse path counts the number of full VCO phases during sampling moments. It represents a rough approximation of the input voltage. Due to implementation aspects of the ring VCO, an input buffer is needed to create power gain for the VCO.

The course path is based on a so-called “state detector” principle, which observes the state of the VCO at the sampling moments. It determines which VCO output signal had the last transition edge before the sampling moments, instead of counting the number of VCO periods. Also a so-called “One-cold-to-binary decoder” is implemented in the coarse path to converts an one-cold representation of the state detector output to binary for the digital domain (MSBs). The fine path is the new and promising idea behind this VCO-based ADC. It generates the linear ramp signals that represent the instantaneous VCO phase at every time moment. The ramp generator consists of two capacitor banks to charge capacitors interleaved in order to create conversion time for the fine A/D conversion. The correct capacitor is selected by using a switch bank, which passes a capacitor voltage (a linear representation of the VCO phase belonging to the A/D conversion) to a fine ADC. This ADC converts that information to the digital domain to obtain the LSBs of the whole A/D conversion.

1.3 Objectives

As it was mentioned in previous paragraph, the described VCO-based ADC architecture was not completely implemented on circuit level. In fact, only the building blocks ring VCO, state detector and ramp generator of Figure 1 were designed on circuit level. At the start of this project it was the intention to finish the whole design on circuit level, and show via circuit simulations the desired operation of the ADC. However, after a couple of weeks it turned out that there were uncertainties about the design. The proposed ring VCO does not achieve high linearity performance, and the design still needs a buffer which should be more linear than the ring VCO. Otherwise the nonlinearity of the buffer will become more dominant over the nonlinearity of the VCO. It is not straightforward to design a high linear input buffer on circuit level, which operates at low supply voltage (1.2 V) and has little power consumption. In order to compete with state-of-the-art ADCs digital calibration is needed for the new VCO-based ADC design to increase the dynamic range. Without digital calibration the performance of this new design is limited by the nonlinearity of the ring VCO. It is not self-evident that the nonlinearity can be cancelled by using calibration. The digital calibration can only increase the performance if the distortion caused by the nonlinearity is frequency independent. Otherwise, the digital calibration will not increase the performance substantially, since input frequency dependent distortion cannot be cancelled by calibration. Therefore, this thesis is focusing on the ring VCO and the buffer of the new VCO-based ADC design, see Figure 2.

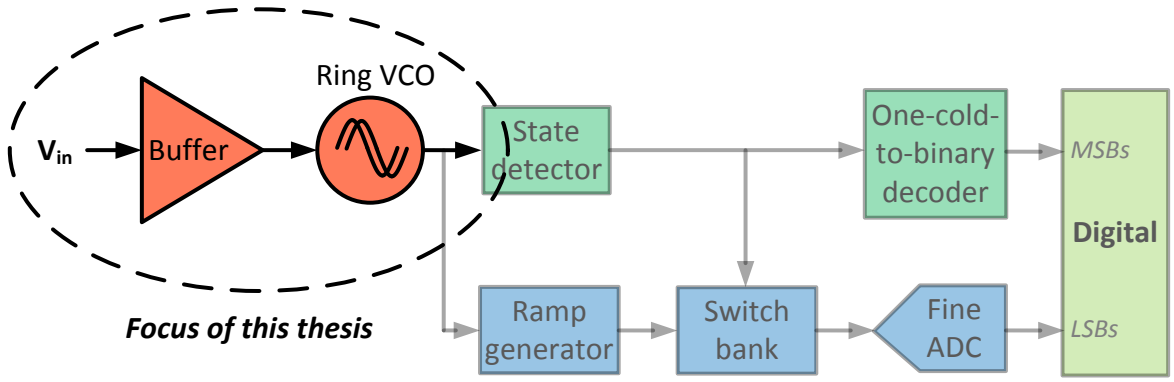

Figure 2: Block diagram of the VCO-based ADC with highlighted part indicating the focus of this thesis.

The objectives of this master thesis project are:

- Perform high-level system analysis to show desired system behavior.
- Investigate the linearity performance of the proposed ring VCO.
- Investigate if alternative VCOs achieve less distortion.
- Investigate the consequences of the input buffer on the linearity.
- Investigate frequency dependent distortion of VCOs, which influences the obtained performance if digital calibration will be used.

1.4 Thesis outline

Chapter 2 deals with the high-level system behavior of VCO-based ADCs. The first paragraph describes the operation of an ideal VCO. After that, different frequency quantization architectures are discussed, which is needed to perform an Analog-to-Digital conversion. It shows besides the mathematical performance also simulation results with ideal building blocks. The chapter is concluded with non-ideal effects that limits the performance of VCO-based ADCs.

In order to describe these limits in terms of distortion, chapter 3 describes the static distortion of VCOs on circuit level. After an introduction of the characterization method, the proposed ring VCO circuit is analyzed and simulated. The performance of the proposed VCO is compared to alternatives which are also tuned in frequency by the power supply V_{DD} and compared to alternatives which are tuned by the transconductance *gm* of a transistor. After that, the design aspects of an input buffer are treated. Since a saw-tooth oscillator is an appropriate alternative to the whole new ADC design, it will also be elaborated in this chapter. The end of chapter 3 is dedicated to compare the static distortion performance of the discussed oscillators.

The fourth chapter is focused on the dynamic distortion of the two preferred VCO circuits from chapter 3. It first describes the characterization method, after which the simulation results are treated. These simulations are subdivided into single-tone and two-tone simulations. The third paragraph of chapter 4 discusses briefly an alternative approach to investigate memory effects.

Finally, this thesis is concluded with conclusions in chapter 5, and recommendation in chapter 6.

2 High-level system analysis

This chapter will discuss the system analysis of VCO-based ADCs on a high-level. This gives more insight in the operation of this kind of ADCs, and shows how these converter behave ideally. Firstly, the ideal VCO operation will be treated by showing important mathematics. Secondly, several VCO-bases ADC architectures will be discussed theoretically and evaluated by system simulations with ideal building blocks. Since noise and distortion will limits the ADC's performance, the third paragraph will deal with the non-ideal effects of VCO-based ADCs.

2.1 Ideal VCO operation

A Voltage-Controlled Oscillator (VCO) is a system or circuit that generates an oscillating signal and can be controlled with an analog input voltage. It transposes an analog input signal into an oscillating output signal which can be interpreted by either frequency or phase. The instantaneous VCO frequency, f_{VCO} is ideally proportional to the input voltage, whereas the phase of the VCO, θ_{VCO} represents the integral of the VCO frequency [3] [4] [6]. This can be written in equations as:

$$f_{VCO}(t) = f_c + K_{VCO} \cdot V_{in}(t) \tag{1}$$

$$\theta_{VCO}(t) = 2\pi \int_{-\infty}^{t} f_{VCO}(\tau) d\tau = 2\pi \int_{-\infty}^{t} f_c + K_{VCO} \cdot V_{in}(\tau) d\tau \tag{2}$$

Here, f_c represents the free running center frequency and K_{VCO} denotes the "gain" or also called the "sensitivity" of the VCO expressed in [Hz/V]. Equation (1) gives a linear voltage-to-frequency transfer characteristic, which can be visualized graphically as shown in Figure 3. This figure shows easily that the slope of the transfer represents K_{VCO}, and thus the following equation holds:

$$K_{VCO} = \frac{df_{VCO}}{dV_{in}} \tag{3}$$

The voltage-to-phase relationship as shown in Equation (2) exhibits a notable operation, namely the integration. The VCO effectively behaves as a continuous-time voltage-to-phase integrator without having feedback. This is due to the output phase of a VCO accumulates continuously, and this results in an ideal voltage-to-phase integration with an infinite DC gain.

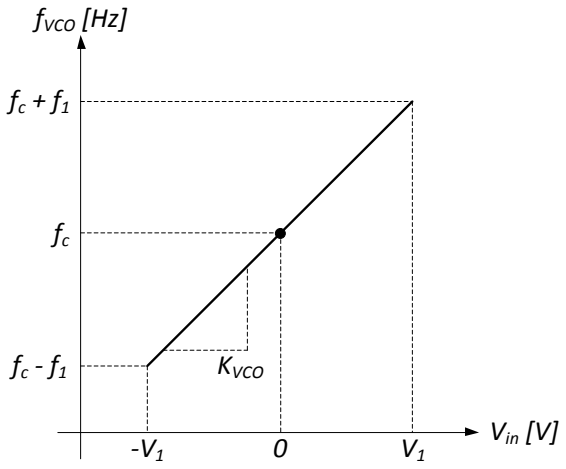

Figure 3: The voltage-to-frequency transfer characteristic of a VCO.

The output voltage of an ideal VCO can be expressed in time-domain as a sinusoidal signal with amplitude and phase by equation:

$$V_{VCO\_out}(t) = A_{VCO}\sin\left(\theta_{VCO}(t)\right) \tag{4}$$

Equation (4) can also be written as a function of the input voltage as shown in Equation (5).

$$V_{VCO\_out}(t) = A_{VCO}\sin\left(2\pi\int_{-\infty}^{t} f_c + K_{VCO}\cdot V_{in}(\tau)d\tau\right) \tag{5}$$

An ideal VCO can therefore be represented as a block diagram as shown in Figure 4. The integration is implemented in the Laplace-domain by 1/s. In order to generate a sinusoidal output, a sinus function block is needed where the argument of the sinus is formed by an input.

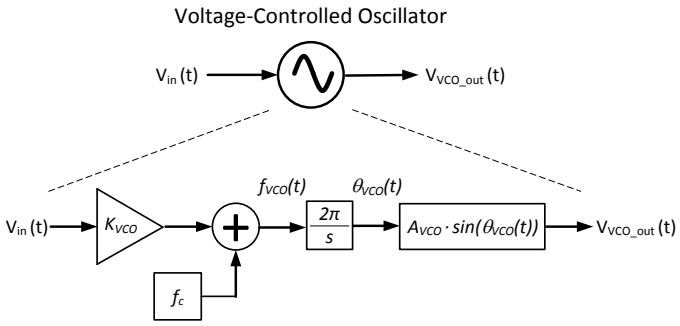

Figure 4: Block diagram of an ideal VCO.

2.2 Ideal Frequency quantization

In previous paragraph an ideal VCO was discussed, where its output frequency is linear related to the input voltage. In order to perform an analog-to-digital conversion a frequency quantizer is needed. This quantizer measures the phase difference between two sampling moments to derive the VCO frequency. It can be implemented in several ways.

2.2.1 Architecture with counter and reset

The first VCO-based ADCs were based on this architecture, and it consists of a counter and a sampling register as shown in Figure 5 [3].

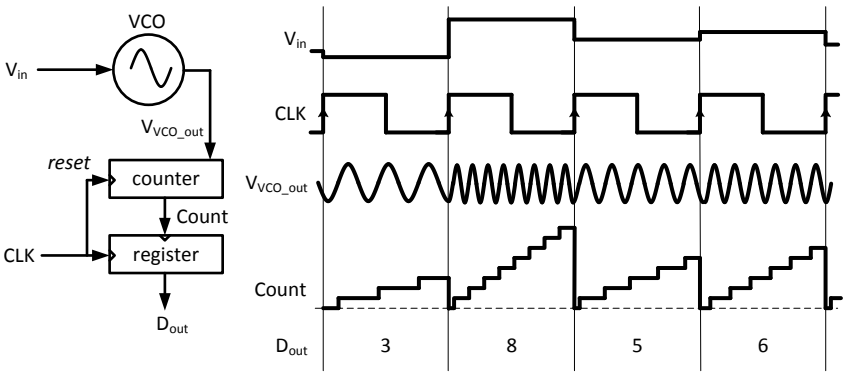

Figure 5: Block diagram of a VCO-based ADC with a counter and register as quantizer.

With this architecture it is possible to monitor the rising or falling edges of the VCO output by means of a counter, see the right-side of Figure 5. It accumulates the number of transition edges during a sampling period. Since the output phase is monitored in this case by counting the rising edges, the resulting phase is quantized with a resolution of 2π. On the sampling moments (rising CLK edges), the resulting count is sampled by a register and the counter is reset to zero. Note that the counter acts as a differentiator, because it defines the VCO phase difference between the current sampling moment and the previous sampling moment. Thus the counter value at the sampling moments is linear with the oscillation frequency of the VCO, and therefore linear to the input voltage.

It should be stressed that this mechanism introduces an important aspect of VCO-based ADCs. Since the output phase of the VCO is continuous, the residual phase at the current sampling period becomes the initial phase of the VCO of the next sampling period. This introduces first-order noise shaping of the counter's quantization noise. To elaborate this principle further, an example is given as shown in Figure 6.

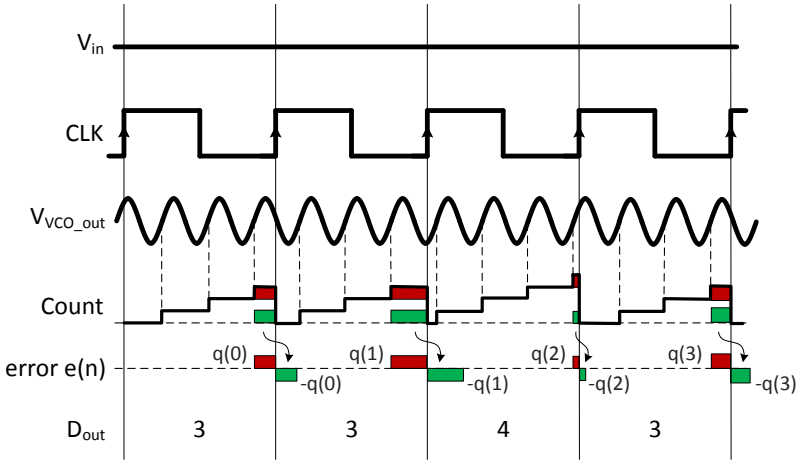

Figure 6: Principle of first-order noise shaping in VCO-based ADCs.

Figure 6 shows a simple example of the counting process with a constant input voltage. During a rising edge of the VCO, the counter increase its count value by one. On the sampling moments, i.e. at the rising edge of the CLK, the final count is passed through to the output and the counter is reset to zero. On that moment, the VCO period is truncated and results in an additional truncation error of sample *n* denoted by *q(n)*. Consequently this truncation error also called the residual phase at sample *n*, becomes the initial phase at the next sample *n+1*. Moreover the resulting phase error per sample *e(n)* consists of the difference of the truncation error of current sample with the truncation error of previous sample. The accumulation of the phase error from sample to sample is then limited to a single quantization level (1 LSB). This is visualized in Figure 6 by the extra count in the third sample of the sequence [3 3 4 3]. Thus, the resulting phase error of n^{th} sample, *e(n)* can be stated as:

$$e(n) = q(n) - q(n-1) \tag{6}$$

The digital output, stated with *y(n)*, represents the quantized version of the VCO phase difference and can be expressed as [8]:

$$y(n) = \frac{1}{2\pi}\left(\phi(n) + e(n)\right) \tag{7}$$

where $\phi(n)$ represents the phase difference in terms of full VCO periods (measured by the counter), and $e(n)$ represents the resulting phase error due to the truncation of a VCO period at the sampling moments.

Transforming Equation (6) to the z-domain results in the following expression:

$$E(z) = Q(z) - Q(z) \cdot z^{-1} = Q(z)(1 - z^{-1}) \tag{8}$$

Here we see that the quantization error signal, or also called the quantization noise, E(z) is first-order high-pass noise-shaped. By high-pass noise-shaping we mean that the noise energy at lower frequencies is shifted to higher frequencies. The quantization noise will be first-order shaped, hence an increase of 20 dB per decade. This noise-shaping mechanism is equivalent to another type of A/D converters, the well-known first-order sigma-delta (ΣΔ) converters. Therefore the same reasoning can be used to deduce the resolution and the Signal-to-Quantization-Noise Ratio (SQNR) of the quantizer. For a VCO-based ADC, both the resolution and SQNR depend on the phase resolution of the VCO during the sampling period. The resolution also called the effective number of quantization bits of the quantizer, can be defined as:

$$M_Q = \log_2\left(\frac{\Delta f_{VCO}}{f_s}\right) \tag{9}$$

where Δf_{VCO} represents the full-scale tuning range of the VCO and f_s represents the sample frequency of the quantizer. Note that Δf_{VCO} is equal to the difference of the maximum and minimum oscillation frequency, and it is not equal to half of the tuning range. Thus Δf_{VCO} can also be expressed as:

$$\Delta f_{VCO} = 2 \cdot K_{VCO} \cdot A_{in} \tag{10}$$

Here, A_{in} represents the maximum input voltage of the VCO. It is very remarkable that the resolution of the quantizer depends on the sample frequency. As a matter of fact, for other A/D converter types this is not the case. Only for VCO-based ADCs this holds, and the resolution as function of sample frequency is even a potential advantage. Moreover, the resolution of these kinds of converters is exchangeable with time. The reason for the f_s dependent resolution is probably due to the smallest Δf_{VCO} that the counter can distinguish, should correspond to an additional count during a sampling period. Thus in other words, the quantizer should be able to distinguish $\Delta f_{VCO}/f_s$ with $(\Delta f_{VCO}+f_s)/f_s$. As a matter of fact this is true, because it results indeed in an addition count. Since VCO-based ADCs have a much higher sampling frequency compared to the input bandwidth, the SQNR depends on the Nyquist bandwidth $f_s/2$ compared to the signal bandwidth BW. This ratio also known as the oversampling ratio OSR, is defined as:

$$OSR = \frac{f_s}{2 \cdot BW} \tag{11}$$

Hence, with the known resolution and oversampling ratio, the SQNR can be represented as the following equation [8]:

$$SQNR = 6.02 \cdot M_Q - 3.41 + 30 \cdot \log_{10}(OSR) \tag{12}$$

It is a known formula, because it is also applicable to first-order sigma-delta (ΣΔ) ADCs. The factor 30 for the OSR in the equation arises from two different factors. Firstly a factor 10 due to the oversampling principle (Equation (11)), and secondly a factor 20 due to the noise shaping of the quantizer. Equation (12) shows that by doubling the full-scale tuning range (Δf_{VCO}) results in 6 dB

improvement of the SQNR, while by doubling the sampling frequency (f_s) results in an effective improvement of 3 dB. This latter improvement is equal to 3 dB, because the 9 dB benefit due to the oversampling is degraded by a 6 dB increase of the quantization noise. In other words, the improvement of the SQNR by increasing f_s is limited, because the quantizer counts less VCO transitions within a sample period. Thus for VCO-based ADCs it is possible to increase the SQNR by increasing f_s, but the benefit is much less than in comparison with conventional sigma-delta converters with noise shaping.

Although the VCO-based quantizer shown in Figure 5 shows the essentials of this kind of analog-to-digital conversion, its performance may not be as good as expected. There is a significant probability that that a VCO edge falls simultaneously with reset edge, because the VCO frequency is much higher than the sampling frequency (reset operation). The effects of this will be investigated in more detail with simulations in the second coming paragraph. Firstly, an alternative architecture will be introduced.

2.2.2 Architecture with modulo-N counter

This architecture is basically the same as preceding architecture, but is uses a different counting mechanism. The counter in this architecture is represented by a modulo-N counter, which does not have the reset function. The block diagram of this architecture is shown in Figure 7.

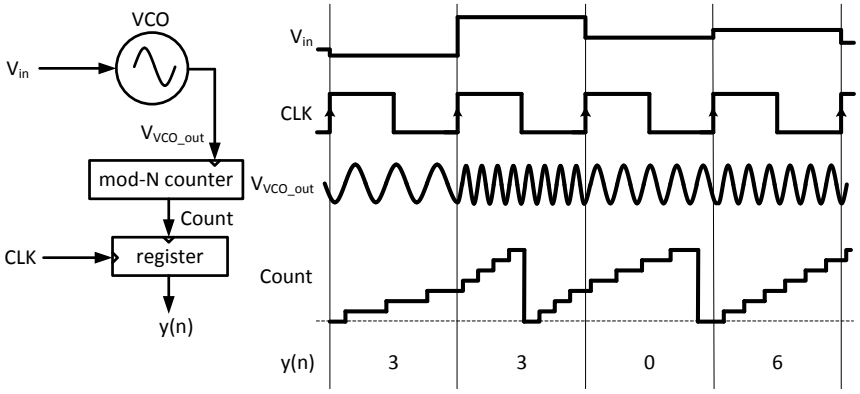

Figure 7: Block diagram of a VCO-based ADC with modulo-N counter and register as quantizer.

The counter is implemented as such that it flows over at a certain maximum count, because infinite counters do not exist. When the counter reaches the maximum count, the next count will be zero. This way of counting is also known as modulo-*N* counting, where *N* represents here the maximum count number. The resolution of the counter should be higher than or equal to the maximum number of counts that could occur during one sampling interval. Otherwise, the counter may flow over twice during a sampling interval, which will not be detected. That is because the quantizer's output is represented by a count number between 0 and *N.* If more than 1 overflow occur during a sampling period, then the second overflow is not counted, a phenomenon that is referred to as aliasing. The number of counts that could occur depends on the frequency deviation Δf of the VCO and the sampling frequency f_s of the quantizer. Therefore, the minimum resolution of the counter expressed in a number of bits can be calculated by equation (9).

The output of the quantizer does not represent the phase difference from sample to sample anymore. Therefore, it is not a representation of the VCO frequency, because the counter is not reset at the sampling moments. In order to determine the phase difference between two sampling moments, or in other words to derive the VCO frequency, a difference in count number has to be determined. That can be performed at the output of the quantizer in the digital domain.

When the counter flows over the phase difference between two sampling moments, it is not represented by the difference in count number, but by that difference plus the full-scale count number *N*. Thus, the digital output of the VCO-based ADC can be formulated in digital domain from the quantizer output by the following equations:

$$D_{out} = \begin{cases} y(n) - y(n-1) & if \;\; y(n) > y(n-1) \\ y(n) - y(n-1) + 2^{M_Q} & if \;\; y(n) \le y(n-1) \end{cases} \tag{13}$$

where *y(n)* represents the quantizer output at sample *n*, and M_Q represent the quantizer's resolution calculated by equation (9).

2.2.3 Simulations of the single phase architectures

To verify the theory in previous described paragraphs, both architectures are simulated with ideal function blocks in Matlab/Simulink. Simulink was used to simulate the VCO-based quantizer in continuous time, while Matlab was used to perform FFT calculations on the time signals. With focus on the application of this A/D converter, the parameters and simulation settings that were used are listed in Table 1.

Parameter	***Symbol***	***Value***	***Unit***
Input signal frequency	f_{in}	1	[MHz]
Input signal bandwidth	BW	10	[MHz]
Input signal amplitude	A_{in}	1	[V]
VCO free-running frequency	f_c	12	[GHz]
VCO gain	K_{VCO}	4	[GHz/V]
Sampling frequency	f_s	1	[GHz]
Simulation step size	T_{step}	1	[ps]
Simulation duration time	T_{sim}	10.1	[µs]
Part of simulation time to take FFT	T_{FFT}	0.06-10.06	[µs]

Table 1: Parameters and simulation settings of Matlab/Simulink simulations.

The expected SQNR can be calculated using equation (12), and results with the parameters from Table 1 in 65.6 dB. Note that this number represents the ratio of the signal power to the quantization noise power within the input bandwidth. Thus in this case, only the quantization noise power in 10 MHz bandwidth is included. The simulation results of both architectures are shown in Figure 8.

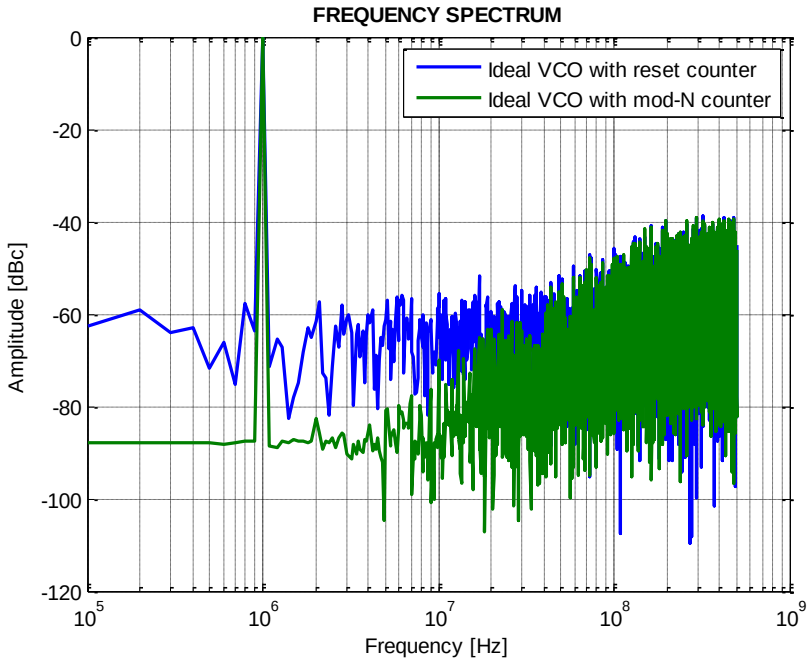

Figure 8: Simulation results of the two ideal VCO-based quantizer architectures.

From Figure 8 we can observe that the ideal VCO-based quantizer with reset have a substantial higher quantization noise level at lower frequencies compared to the quantizer with the modulo-N counter. The performance is limited due to the reset operation of the counter. In cases where a VCO edge occurs at the same time as the reset signal, the measured edge count is not necessarily included. Since the VCO frequency is much higher than the sampling frequency (reset operation), there is a significant probability that a VCO edge falls at the same time as a reset edge. Thus, some counts are not included, and eventually limits the performance of VCO-based ADCs with this architecture.

The simulated SQNR turned out to be 43.0 dB for the architecture with reset and 64.3 dB for the architecture with the modulo-N counter. This last value corresponded to a large extent to the theoretical SQNR of 65.6 dB, however a small error still remained. Figure 8 shows in case of the second architecture also the first-order high-pass noise-shaping over the full frequency range. It agrees with the first-order noise-shaping, which renders a 20 dB per decade increase of the quantization noise floor. Note that the noise-shaping is the result of counting the VCO phase continuously, whereby the residual phase at the current sampling period becomes the initial phase at the next sampling period. Thus, the phase error is differentiated.

2.2.4 Multiphase architecture with counters

The previous described architecture works fine, but the resolution is rather low for practical applications. To improve the resolution of the VCO-based ADC, the VCO needs to generate more edge transitions during a sampling period. This can be accomplished by implementing a ring-oscillator structure to generate multiple VCO output signals [8]. The block diagram of a three-stage ring oscillator-based VCO is shown in Figure 9.

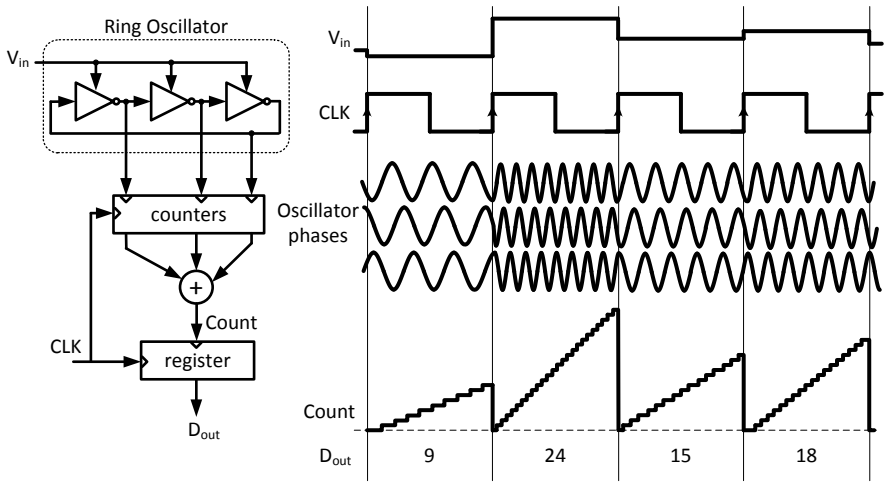

Figure 9: Block diagram of a 3-stage VCO-based ADC with a ring-oscillator to improve resolution.

From Figure 9 it is visible that the ring oscillator-based VCO has three outputs, and each output drives a single counter. All oscillator output signals have the same shape, but are only shifted in time. Thus mutually, they have 120 degrees phase difference. The output of the counters are subsequently added together and sampled with a register. This produces a total count with a higher resolution by a factor N_{ph} compared to the single-output VCO-based ADC as described in preceding paragraphs. Here, the factor N_{ph} represents the number of VCO output signals, and is in this example equal to three. Hence, instead of Equation (9), the resolution of a multiple output ring oscillator-based VCO can be represented as the following equation:

$$M_Q = \log_2\left(\frac{\Delta f_{VCO} \cdot N_{ph}}{f_s}\right) \tag{14}$$

where Δf represents the full-scale tuning range of a single output of the VCO and f_s represents the sample frequency of the quantizer. In fact, the frequency range corresponds to the single phase architectures, but using multiple VCO output signals that results in an increase of phase resolution.

The output of this VCO-based ADC architecture represents the VCO phase difference from sample to sample, similarly as the first treated architecture in this chapter. Thus, the digital output value is proportional to the input voltage. However, due to the reset operation of the counters, the performance of these VCO-based ADCs is strongly limited. An improved ring oscillator-based VCO architecture will be treated in the next paragraph.

2.2.5 Multiphase architecture with a state detector

From preceding paragraph it turned out that the resolution of VCO-based ADCs can be improved by using a multistage ring oscillator as VCO. In order to achieve good performance, edge transitions of the VCO outputs should be detected without using a counter with reset function. There are a variety of alternative VCO-based quantizer structures that do not use counters with a reset function, but here we treat a new non-published architecture [20]. It makes use of “state detector” instead of counting edges during a sampling period. By state detection we mean, observing the level of all VCO outputs at fixed sampling moments, and determine which output had the last edge transition. When, the output which had the last edge transition at a certain sampling moment and which output had

the last edge transition at the previous sampling moment are known, the difference between them can be used as a measure for the phase difference. In order to clarify this concept, we analyze the ring oscillator in more detail.

A ring oscillator consists of a number of sequential delay stages, and uses feedback to create a loop. If it then satisfies the Barkhausen's criterion, i.e. the open loop gain is unity and the open loop phase shift is a multiple of 2π (or zero), the circuit will oscillate. In ICs, the delay stages are normally buildup from CMOS inverters, because of its simple structure. The output signal of an inverter stage represents the inverted version of the input signal but with some delay equal to τ_d. This delay is a consequence of the signal propagation through the inverter, and is a dynamic property. A block diagram of a three-stage single-ended ring oscillator and the corresponding waveforms are shown in Figure 10.

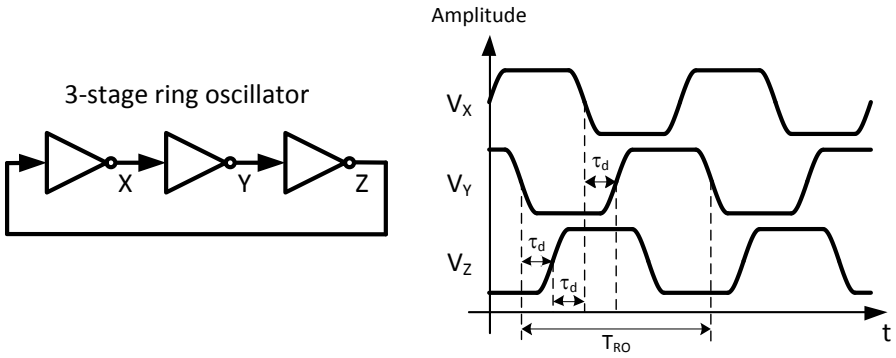

Figure 10: Block diagram (left) and waveforms (right) of a three-stage single-ended ring oscillator.

At a certain moment in time, one output of the ring oscillator is in a transition state, i.e. between the two supply voltages, while the other outputs are fixed at one of the two supply voltages (either negative (often a ground) or positive supply voltage). In case of a three-stage single-ended ring oscillator (see Figure 10), one output has a transition, while the first of the two other outputs is low (ground) and the second is high (V_{DD}). The amount of transitions of a ring oscillator before it is in its initial state is therefore equal to twice the number of stages. This encloses for each output one transition from the negative to the positive supply voltage and one from the positive to the negative supply voltage. The time that has elapsed during both transitions for each inverter output is known as the oscillator period, and is equal to twice the number of stages times the inverter delay per stage. Thus, the instantaneous frequency of a single VCO output of the ring oscillator can be expressed as:

$$f_{VCO} = \frac{1}{T_{RO}} = \frac{1}{2N\tau_d} \tag{15}$$

where N represents the number of inverter stages of the ring oscillator. Note that the number of stages N may by definition not be equal to the number of ring oscillator output signals N_{ph}. This is clarified later on, when differential ring oscillator stages will be used.

In order to determine which output signal of the ring oscillator had the last edge transition, a so-called "state detector" observes the level of all output signals. The architecture of a N-stage ring oscillator with the state detector is shown in Figure 11.

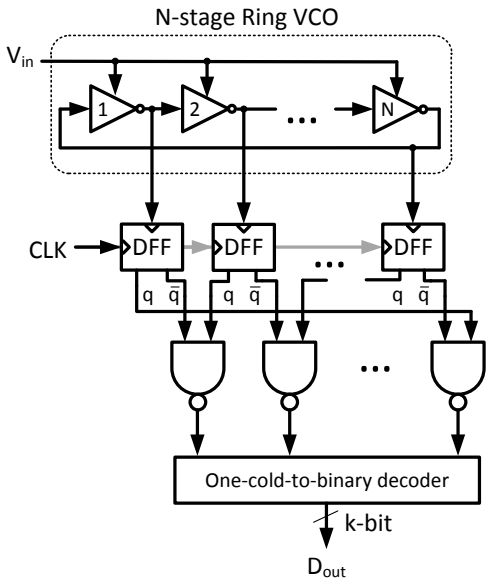

Figure 11: Block diagram of a N-stage ring oscillator with state detector and decoder.

The architecture as shown in Figure 11 consist of a *N*-stage Ring VCO, *N* Data Flip-Flops, *N* NAND gates and a one-cold-to-binary decoder. The output signals of the ring oscillator are captured with a Data Flip-Flop (DFF), at which each output signal is quantized to one bit, i.e. quantization to logical "0" or logical "1". By using a NAND gate between the complementary DFF output of VCO output "i" and the DFF output of VCO output "i+1", it determines if VCO output "i" had the last edge transition. When the NAND output of VCO output "i" becomes "0", it means that this output had the last edge transition. The output of the other NAND gates, are then "1", due to the structure of the DFF with the NAND gates. The implementation of such a multi-bit signal in which all bits are "1" except one "0" is referred to as one-cold representation. The decoder converts this *N*-bit signal to a binary representation which consists of *k*-bits. Note that it should satisfies the following expression:

$$N = 2^k \tag{16}$$

Since the outputs of the NAND gates indicates which VCO output had its last edge transition (by a "0"), a decoder maps the VCO output number to a digital number. In order to derive the VCO frequency (which is a linear representation of the input voltage), the difference should be taken in the digital domain in the same manner as described in section 2.2.2. This is because the output of the decoder does not represents the phase difference from sample to sample, similarly as with the architecture with the modulo-N counter. Therefore, Equation (13) should be implemented in the digital domain, where the resolution M_Q is here equal to *k*.

This mechanism of frequency quantization works only properly if the VCO frequency f_{VCO} is bounded. We would like to ensure that each ring oscillator output makes at least one positive and one negative edge transition during one sampling period. Thus in other words the VCO frequency should be higher than or equal to the sampling frequency. On the other hand, the VCO frequency may not exceed twice the sampling frequency, because the state detector cannot make a distinction of the VCO frequency between one or twice the sampling frequency. If it otherwise exceeds twice the sampling frequency aliasing will then occur. Thus the maximum VCO frequency should be lower than twice the sampling frequency, and depends on the number VCO output signals N_{ph}. This is because the number

of N_{ph} signals determines the number of detection states between one and twice the sampling frequency. The VCO frequency of a single VCO output should therefore be limited to:

$$f_s \leq f_{VCO} \leq \left(2 - \frac{1}{N_{ph}}\right) f_s \tag{17}$$

The simulation results of this architecture will be treated in the following paragraph.

2.2.6 Simulations of the multiphase architecture with a state detector

The architecture with multiple phases and a state detector is also simulated with ideal function blocks in Matlab/Simulink. The same procedure is used here as described in section 2.2.3. In order to perform a simulation of the VCO as a whole with the same parameters as described before, the VCO free-running frequency and the VCO gain needs to be adapted. Both parameters are scaled with the number VCO output signals N_{ph}. For our application we are aiming at a VCO with 8 output signals. Thus the minimum and maximum frequency of a single VCO output f_{VCO} were defined as 1 and 1.875 GHz, respectively (Equation (17)). The simulation settings as well as the used parameters are listed in Table 2.

Parameter	*Symbol*	*Value*	*Unit*
Input signal frequency	f_{in}	1	[MHz]
Input signal bandwidth	BW	10	[MHz]
Input signal amplitude	A_{in}	1	[V]
Number of outputs VCO	N_{ph}	8	[1]
VCO free-running frequency	f_c	1.4375	[GHz]
VCO gain	K_{VCO}	437.5	[MHz/V]
Sampling frequency	f_s	1	[GHz]
Simulation step size	T_{step}	1	[ps]
Simulation duration time	T_{sim}	10.1	[µs]
Part of simulation time to take FFT	T_{FFT}	0.06-10.06	[µs]

Table 2: Parameters and simulation settings of Matlab/Simulink simulations.

The expected SQNR of the ideal quantizer can be calculated by using Equations (12) and (14). This results with the parameters from Table 2 to a SQNR equal to 64.5 dB. Comparing it to a single phase VCO (as discussed in section) renders theoretically 1.16 dB less SQNR. This is due to the fact that the tuning range Δf_{VCO} is decreased from 8 GHz (single phase VCO) to 8 times 875 MHz (8-stage ring VCO). The mathematical prove can be expressed as:

$$\Delta SQNR = 6.02 \cdot \Delta M_Q = 6.02 \cdot \left(\log_2\left(\frac{8\ GHz}{1\ GHz}\right) - \log_2\left(\frac{8 \cdot 875\ MHz}{1\ GHz}\right)\right) = 1.16\ dB \tag{18}$$

The simulation results are shown in Figure 12.

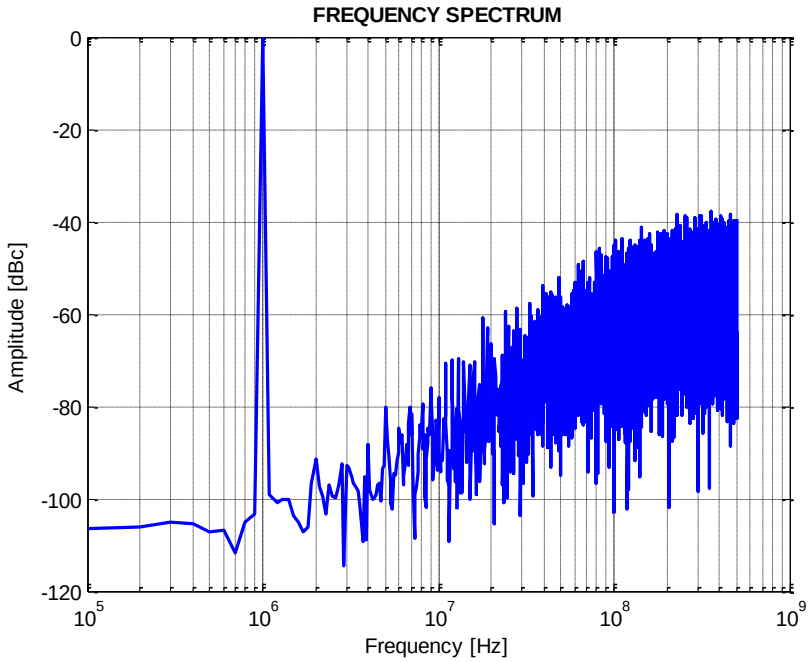

Figure 12: Simulation results of the ideal 8-stage ring VCO architecture with a state detector.

As can be seen from Figure 12, this quantizer maintains the first-order noise-shaping. The increase of the quantization noise is approximately 20 dB per decade, which corresponds to first-order behavior. It turned out that the simulated SQNR within the 10 MHz input bandwidth equals 65.7 dB, and that corresponds nearly with the calculations (64.5 dB).

2.3 Non-ideal effects

There are many non-idealities which influence the overall performance of VCO-based ADCs. Until now, we saw in the output spectra of the aforementioned systems that it does not generates distortion terms. The performance of the previous ADC architectures was only limited by the quantization noise of the frequency quantizer. This is one of the many non-ideal effects of VCO-based ADCs. From previous work it turned out that there are several non-idealities with respect to noise on the ADC's performance [20]. These different types of noise will now be discussed briefly.

- Quantization noise.
  As it was shown in previous paragraphs, the quantization noise from the frequency quantizer is first-order high-pass noise shaped. That is a consequence of the fact that the residual phase of the VCO at the current sampling period becomes the initial phase of the next sampling period.

- Circuit noise added before the VCO.
  This type of noise is present by physical components, such as resistors and capacitors. Since this noise follows the same path as the input signal, this noise will not be shaped. Therefore, it is crucial to reduce the amount of noise as much as possible at the input stage of the VCO-based ADC, during the circuit design.

- Circuit noise added after the VCO.
  This type of noise is injected on the system after the integration of the VCO. It turned out that this noise will also be first-order shaped, similar to the quantization noise.

- Phase noise of the VCO.
  Phase noise is a noise which limits the accuracy of the oscillation frequency of the VCO. This is for oscillators a non-ideal effect that limits the performance. Since this type of noise does not depend on the input signal, it can be seen as noise injected after the integration of the VCO. Thus, this noise is first-order shaped before it is present on the output of the ADC.

Now the important noise sources are discussed, it is time to investigate the most dominant non-ideal effect of VCO-based ADCs, namely the nonlinearity of VCO control characteristic. From the first VCO-based ADCs, this is still the most limiting factor of the ADC's performance. In fact, it is a result of the nonlinear voltage-to-frequency characteristic of the VCO, which limits the performance. This nonlinear transfer function distorts the input signal, and generates distortion terms in the output spectrum of the ADC. On high system level, this nonlinearity can be modeled by a cubic function at the input of the VCO-based ADC, which is in fact a third-order polynomial. This is shown in Figure 13 in case of the ADC architecture with a ring VCO and state detector as discussed in section 2.2.5.

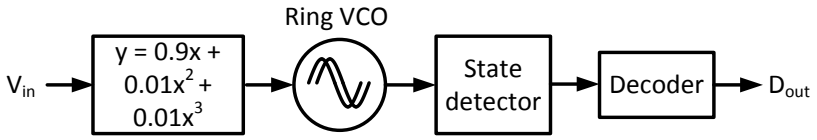

Figure 13: Block diagram of the VCO-based ADC, where the VCO nonlinearity is modeled by a Taylor polynomial.

The VCO nonlinearity is modeled as a third-order polynomial with amplitudes for the quadratic and cubic terms equal to 1%. The linear term is slightly decreased to prevent that the VCO will exceed the detectable tuning range of the frequency quantizer (state detector). The same simulation settings were used as stated in Table 2, described in section 2.2.6. The simulation results of this architecture with the modeled nonlinearity is shown in Figure 14.

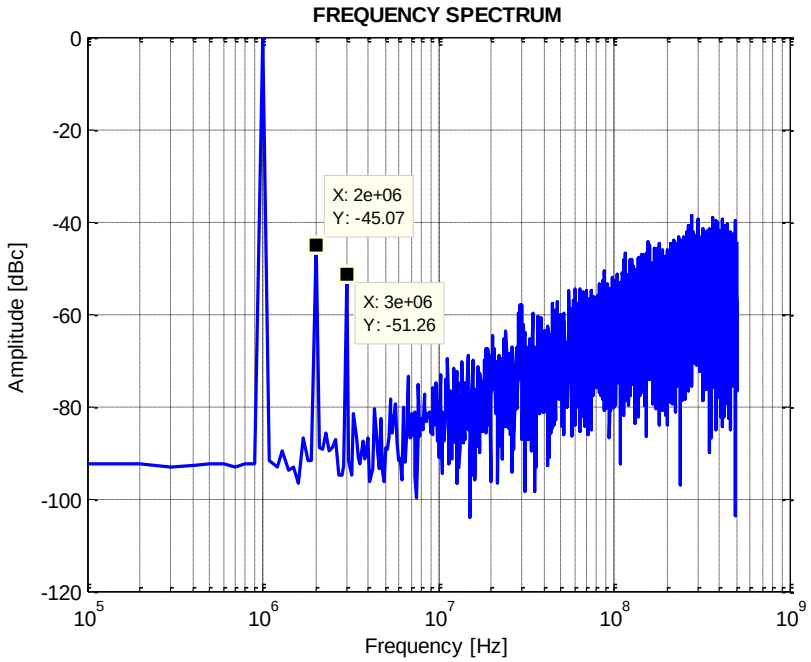

Figure 14: Simulation results of the 8-stage nonlinear ring VCO architecture with a state detector.

The figure shows that the second and third harmonic distortion numbers are equal to -45.1 dB and -51.3 dB, respectively. The simulated SINAD within the 10 MHz input bandwidth turned out to be 44.1 dB, which is a decrease in performance caused by the second and third harmonics. Furthermore, the simulated Signal-to-Noise ratio (SNR) within the 10 MHz input bandwidth turned out to be 63.8 dB. This value is in close agreement with the SQNR of the ideal architecture as discussed in section 2.2.6. The small difference is due to the fact that the amplitude of the input signal in this simulation is decreased by a factor 0.9. It can be concluded that a small VCO nonlinearity degrades the performance of VCO-based ADCs significantly. The next chapter will deal with the distortion analysis of VCOs on circuit level.

3 Static distortion analysis on circuit level

Static distortion is a measure of the distortion without taking frequency dependent memory effects into account. It was discussed in previous chapter that the performance of VCO-based ADCs is mainly limited by the nonlinear control characteristic of the VCO. This nonlinear characteristic is often determined by measuring the frequency at several fixed (static) input voltages. From that, a control characteristic *frequency = f(V_{in})* can be formed, where harmonic distortion numbers like HD_2 and HD_3 can be deduced. These numbers show to a large degree the static distortion of the VCO. As from now, this will also be mentioned as the static performance of VCOs. Note that it is the distortion determined at static input values, and not the static behavior of the VCO. The VCO is inherently a dynamic circuit, since it has internal a dynamic behavior (oscillation). The performance of VCOs based on static distortion will be elaborated in more detail in the first following paragraphs.

3.1 Characterization method

The static performance of VCOs can be analyzed by characterizing the control characteristic of the VCO. The nonlinearity originates from a nonlinear characteristic, i.e. the VCO gain, K_{VCO} is not constant. As we want to analyze frequency modulation, we will evaluate the control characteristic around a so-called quiescent point. At that point, the VCO is said to oscillate at a free-running frequency. This is the frequency at which the signal input amplitude is zero. A nonlinear control characteristic is shown in Figure 15.

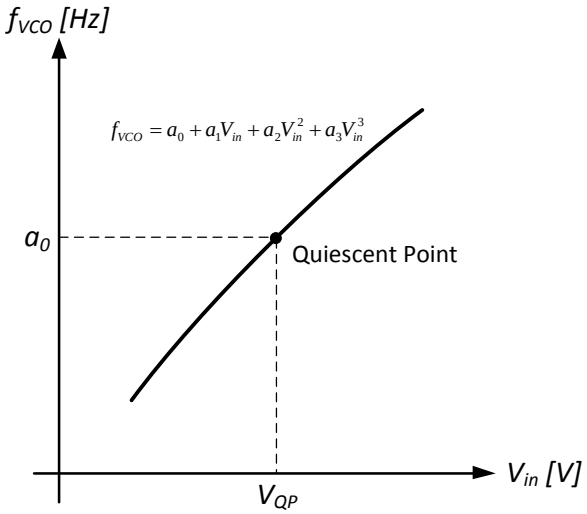

Figure 15: Nonlinear control characteristic around the Quiescent Point of a VCO.

The actual (nonlinear) control characteristic of a VCO as shown in Figure 15, is determined by performing multiple circuit simulations with a constant input voltage V_{in}. A transient (time) analysis is needed, since only then the circuit will oscillate. By using a transient simulation the average VCO frequency f_{VCO} can be determined, which corresponds to the fixed input voltage. The transient simulation will be repeated for different input voltages to compose a complete control characteristic. This results in a nonlinear transfer curve which can be approximated by using Taylor series. The Taylor series represents a function that consist of an large but finite sum of higher order polynomial terms. A third-order polynomial is sufficient to approximate the deviation from the linear control

characteristic, because a weakly nonlinear behavior is expected. Hence, the control characteristic of the VCO can be approximated by Equation (19):

$$f_{VCO} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 \tag{19}$$

where a_n represent the Taylor coefficients with n from 0 to 3 inclusive. The first coefficient a_0 is the DC term of the polynomial which corresponds to the free-running frequency of the VCO. The second coefficient a_1 represents the small-signal gain, and is the linear gain of the input voltage to VCO frequency transfer with the dimension Hz/V. The coefficients a_2 and a_3 are the second- and third-order distortion terms, respectively. They indicate the presence of even and odd nonlinearity in the VCO transfer curve.

For any nonlinear transfer curve, the coefficients from a_0 to a_3 can easily be found by taking derivatives in the quiescent point [21]. Coefficient a_0 is simply the DC value, which is reached for an input signal V_{in} equal to the quiescent point voltage V_{QP}. Coefficient a_1 is the first derivative of the output frequency f_{VCO} with respect to V_{in} at the quiescent point. The coefficients a_2 and a_3 are respectively the second and third derivatives of the output frequency at the quiescent point. However, the coefficients needs to be corrected by factors that arise from the derivation, giving the following equation [21]:

$$a_n = \frac{1}{n!} \frac{d^n f_{VCO}}{dV_{in}^n}\bigg|_{Vin=VQP} \tag{20}$$

Once the nonlinearity has been described by a power series, i.e. Equation (19), the harmonic distortion can be calculated. They give a measure of distortion at the second and third harmonic if a sinusoidal input signal is applied. This input signal can be formulated by Equation (21).

$$V_{in} = V_{QP} + A_{in} \cdot \sin(2\pi \cdot f_{in} \cdot t) \tag{21}$$

Note that V_{in} represents the signal applied to the input of the VCO, while A_{in} represents the amplitude of the input signal at the signal frequency f_{in}. Due to the nonlinear transfer curve distortion arises at $2 \cdot f_{in}$ and $3 \cdot f_{in}$. The ratio of the component at $2 \cdot f_{in}$ to the fundamental f_{in} is by definition the second Harmonic Distortion (HD_2). On the other hand, the ratio of the component at $3 \cdot f_{in}$ to the fundamental f_{in} is by definition the third Harmonic Distortion (HD_3). These distortion numbers depend on the input amplitude A_{in} and the Taylor coefficients a_n, and can be calculated as follows [21]:

$$HD_2 = \frac{1}{2}\left|\frac{a_2}{a_1}\right| A_{in} \tag{22}$$

$$HD_3 = \frac{1}{4}\left|\frac{a_3}{a_1}\right| A_{in}^2 \tag{23}$$

3.2 Proposed VCO circuit

As it was discussed in the introduction, this project is a continuation of a former MSc project. The outcome of that work was that a ring VCO achieves a more linear voltage-to-frequency transfer than in comparison to the current-to-frequency transfer of the saw-tooth oscillator [22]. A new design of a

ring VCO was recommended for the implementation of a VCO-based ADC with linear phase generation techniques. In this section, the proposed ring VCO circuit will be analyzed and simulated.

3.2.1 Circuit design

The proposed VCO circuit consists of a four-stage differential ring VCO as shown in Figure 16. A single stage is represented by a differential delay block. The positive outputs are connected to the negative inputs, and the negative outputs are connected to the positive inputs. Only the last stage is connected without inversion to the first stage in order to meet an odd number of signal inversions. The circuit of each delay cell is also shown in the figure below. This circuit is inspired by an previously published paper [23], although some small differences were made.

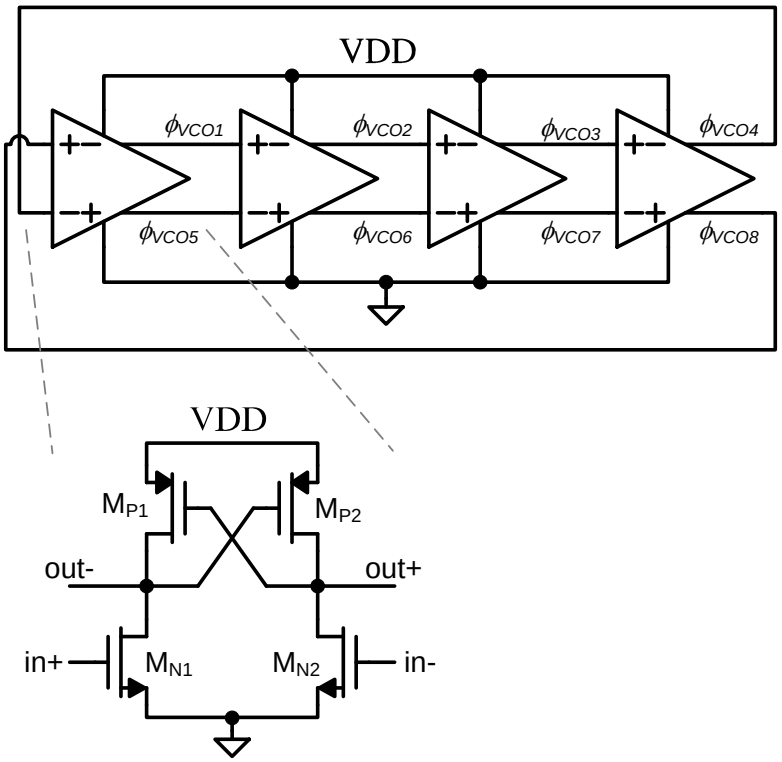

Figure 16: Proposed 4-stage differential ring VCO.

The delay cell consists of one NMOS differential input pair (M_{N1} and M_{N2}) and one PMOS cross-coupled load (M_{P1} and M_{P2}). The PMOS pair can also be interpreted as positive feedback. This structure was chosen, because it consists of only four transistors, thus it is more attractive for future CMOS scaling. It can operate at high frequencies, since only parasitic capacitors of the MOS devices are utilized. Ring oscillators has also a wide frequency-tuning range, which is desirable for our application. In this design, frequency tuning is achieved by means of controlling the power supply V_{DD}.

The author of [23] claimed that his VCO circuit has better linearity performance in comparison with alternative delay cells published in [24] [25] [26]. Two of the three alternatives do not use V_{DD} tuning, and all three have more nonlinear frequency tuning. Note that these VCO circuits are not intended for ADC applications.

The oscillation frequency is determined by the signal delay τ_d in each stage. The oscillation signal will propagate through the stages and forces a signal inversion. Since all stages are identical, the oscillation frequency is equal to:

$$f_{osc} = \frac{1}{2N\tau_d} \tag{24}$$

where in our case the number of stages *N* equals four. Alternatively the oscillation frequency can also be determined by performing linear frequency analysis. Then, by using Barkhausen's criterion it can be determined when a circuit will oscillate. This mathematical criterion can be translated to requirements of gain and phase characteristics of the circuit. To derive the oscillation frequency of proposed circuit (see Figure 16), a half-circuit of the delay cell is considered. That half-circuit (NMOS N1 and PMOS P1) is converted to a small-signal model as shown in Figure 17.

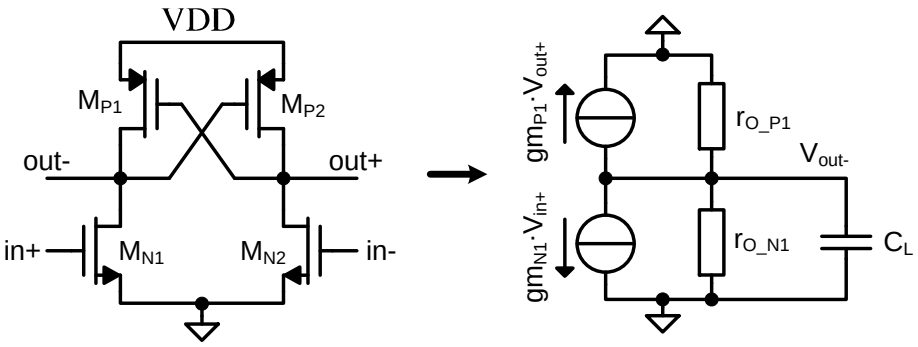

Figure 17: Small-signal model of half-circuit of the delay cell.

Both N1 and P1 are represented by a voltage-controlled current source and an output resistance r_O. Furthermore, all parasitics on the output node are combined into one single capacitance C_L. This capacitance consists of the output parasitics of the first stage followed by the input capacitances of the second stage, and can be expressed as the following equation:

$$C_L = C_{GS\_N} + 2C_{GD\_N} + C_{DB\_N} + C_{GS\_P} + 2C_{GD\_P} + C_{DB\_P} \tag{25}$$

where the subscripts G, S, D and B correspond to the capacitance between the Gate, Source, Drain and Bulk, respectively. The transfer function of the delay cell *H(s)* can be determined by using simple mathematics giving the following expression:

$$H(s) = \frac{V_{out+}}{V_{in+}} = \frac{-gm_N}{\left(r_{O\_N}^{-1} + r_{O\_P}^{-1} - gm_P\right) + sC_L} \tag{26}$$

where gm_N, gm_P, r_{O_N} and r_{O_P} represent the transconductance of the NMOS and PMOS, and the output resistance of the NMOS and PMOS, respectively. The output resistance is a consequence of the channel-length modulation effect. Based on the Barkhausen's criterion, the VCO circuit will sustain steady-state oscillations only at frequencies for which the loop gain is equal to unity and the phase shift around the loop is zero or a multiple of 2π. This means that each delay cell provides a π phase shift and maintains a gain of unity at the oscillation frequency. By equating the transfer function of the delay cell (Equation (26)) to unity, the oscillation frequency of the ring VCO can be expressed as:

$$f_{osc} = \frac{1}{2\pi} \cdot \frac{\sqrt{gm_N^2 - \left(r_{O\_N}^{-1} + r_{O\_P}^{-1} - gm_P\right)^2}}{C_L} \tag{27}$$

From Equation (27) it can be concluded that the oscillation frequency depends on several parameters. It is desired to design the circuit in such a way that the term within the brackets of Equation (27) are close to zero. In other words, the transconductance gm_P should have a similar value as the sum of the two inverse output resistances. Then, the oscillation frequency is maximized, and can be approximated by:

$$f_{osc} \approx \frac{1}{2\pi} \cdot \frac{gm_N}{C_L} \propto \sqrt{I} \propto V_{GS\_N} - V_{TH\_N} \tag{28}$$

Equation (28) shows that the oscillation frequency is proportional to the transconductance *gm* of the NMOS and inverse proportional to the node capacitance. If the capacitance of the input/output node does not change significantly with the V_{DD} swing, as is often the case, the oscillation frequency is also proportional to the square root of the current through the NMOS and proportional to the overdrive voltage of the NMOS. Thus, the gate-source voltage of the NMOS is linearly related to the oscillation frequency, as shown by Equation (28). In order to derive the relation of the oscillation frequency to the V_{DD}, the DC operation point of the delay cell must be formulated. This results in the following equation:

$$V_{DD} = V_{GS\_N} + V_{GS\_P} \tag{29}$$

This equation is only valid when the four delay cells are interconnected to form a ring oscillator. Otherwise, the voltage V_{GS_N} needs to be replaced by the voltage V_{DS_N}. By substituting Equation (29) into Equation (28), the following expression can be derived:

$$f_{osc} \propto V_{DD} - V_{GS\_P} - V_{TH\_N} \tag{30}$$

From Equation (30) it is visible that the f_{osc} is linear related to the V_{DD}. In fact, this is desirable for making a linear voltage-to-frequency function. However, the gate-source voltage of the PMOS V_{GS_P} also depends on V_{DD}, and probably it will decrease the linearity of the relationship of $f_{osc} = f(V_{DD})$. It is hard to describe this nonlinearity, because equations of device physics will come up. A large-signal analysis may provide a more accurate oscillation behavior of oscillators as compared to the small-signal analysis as discussed in this paragraph. Therefore a large-signal approach of this VCO will be elaborated later in this chapter. First, the circuit simulations will be discussed, assuming that the V_{GS_P} dependence on f_{osc} can be neglected. In that case the oscillation frequency of the VCO can linearly be tuned by V_{DD}.

3.2.2 Simulation results

The ring VCO as shown in Figure 16 is simulated on circuit level by using the design tool Cadence. This circuit and all coming circuits are build up in the 65 nm technology of UMC. All transistors in the proposed circuit (Figure 16) are designed at the minimal gate length, which is 60 nm in order to achieve the highest speed. The width of each gate-finger was also chosen at the minimal width of 500 nm. The total width of the transistor is changed by adapting the number of gate-fingers. From Equation (26) it is shown that the open loop gain of a single-stage is dominated by the *gm* of the NMOS. Since the *gm* of a transistor is proportional to the width *W*, the width of the NMOS was

chosen to be 4 times wider than the PMOS. With focus on the tuning linearity, the best results were achieved with the number of gate-fingers being equal to 16 and 4 for the NMOS and PMOS, respectively. The dimensions of the transistors are also shown in Table 3.

Transistor	$M_{N1} = M_{N2}$	$M_{P1} = M_{P2}$
W/L	8/0.06 µm	2/0.06 µm

Table 3: Transistor dimensions of the circuit as shown in Figure 16, .

The eight VCO output signals of a transient simulation with V_{DD} equals 1 V is shown in the figure below:

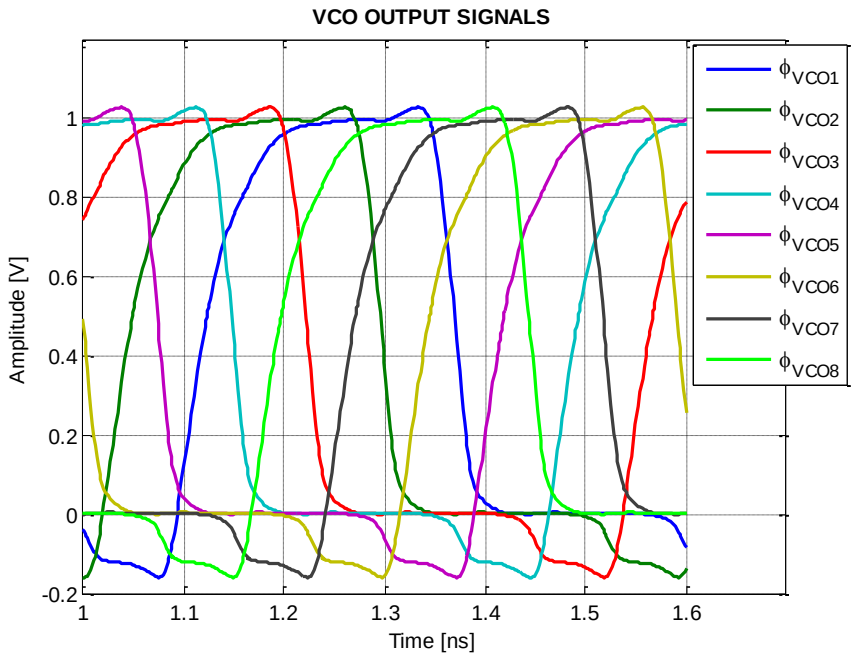

Figure 18: The eight VCO output signals of a transient simulation of proposed circuit.

From Figure 18 it can be seen that the eight VCO output signals are shifted in phase with 45 degrees. The signals 5, 6, 7 and 8 are the inverse of the signals 1, 2, 3 and 4 respectively. The figure shows also that the time period of each signal can be approximated to 0.59 ns, which is equal to an oscillation frequency of 1.69 GHz.

Figure 18 shows the behavior of the circuit during oscillation, which is as expected, but it does not give any information about the start-up behavior of the VCO. The start-up behavior of oscillators is an important aspect when designing these kinds of circuits. The proposed circuit as shown in Figure 16 is more susceptible to settle in a non-oscillating state, because it does not have a current source in the tail of the differential pair. In order to guarantee that the oscillator will always start-up, the open loop gain of the oscillator must be larger than unity. Since that cannot be guaranteed for the proposed circuit by a simple gain expression, since there are active nonlinear devices. Some small simulations were performed to see if the oscillator will start-up. One way to simulate that, is by observing the VCO output signals from the start when it is brought in a worst case scenario at initial condition. The worst case scenario for the proposed 4-stage differential VCO is shown in Figure 19.

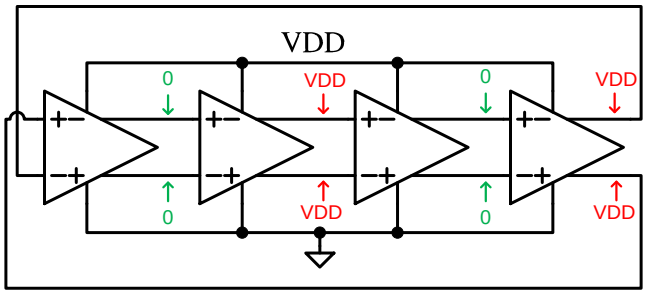

Figure 19: 4-stage VCO with the output node voltages in worse case as initial condition.

The figure shows that four VCO output signals have an initial voltage equal to V_{DD}, while the other four signals have an initial voltage equal to zero. By simulations it turned out that the VCO does not stay in a fixed non-oscillating state, and starts to oscillate after 6.3 µs. By putting all VCO output signals to zero, it will bring the VCO in oscillation after 1 ns. Most likely, the open loop gain of the VCO is higher than unity, which ensures oscillation.

The static distortion of the proposed VCO can be determined by analyzing the linearity of the VCO transfer curve. The basics of this linearity analysis is described in section 3.1. In order to compose the control characteristic of the VCO, 11 transient simulations were performed at different V_{DD} voltages. The constant f_{VCO} at each simulation was determined accurately by using the standard function *frequency* within Cadence. For the desired ADC, a VCO is needed which is tunable between 1 and 2 GHz. With the proposed circuit, this is possible with a V_{DD} power supply of 0.835 V to 1.075 V. This means that the quiescent point of 1.5 GHz is located at a V_{DD} equal to 0.955 V. The full-scale input amplitude is equal to 120 mV. The simulation data was analyzed by using the software tool Matlab, and the results are shown in Figure 20.

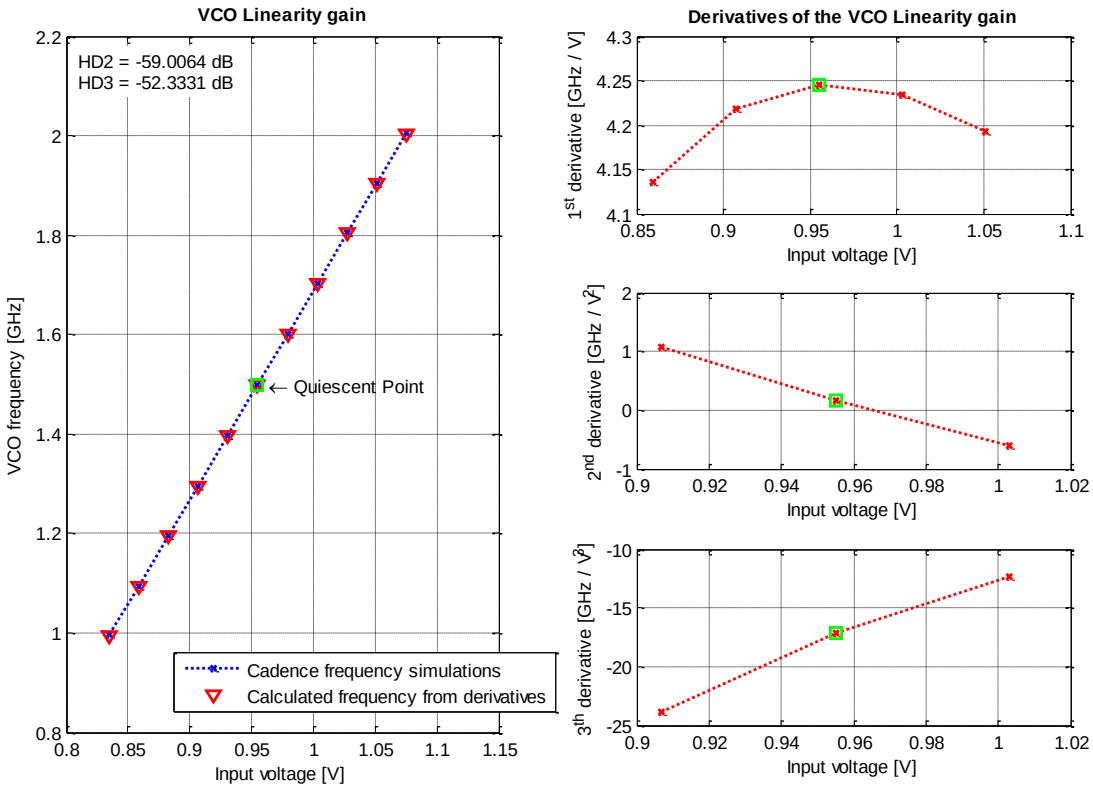

Figure 20: VCO linearity gain and their derivatives of the proposed circuit as shown in Figure 16.

The determined frequencies of the different simulations are shown with the blue crosses at left-side of Figure 20. These simulation points are necessary to determine the derivatives at the quiescent point. The derivation was performed numerically and symmetrically at that point. The first three derivatives of the VCO frequency simulations are shown at the right-side of Figure 20. The derivatives at the quiescent point represent the values of the coefficients of the Taylor approximation (see Equation (19)), excluding the multiplication factor due to the derivation. These coefficients are used to deduce the static distortion, i.e. HD_2 and HD_3 by the Equations (22) and (23), assuming a full-scale amplitude equal to 120 mV. These two numbers are shown for this circuit in the upper left-corner of Figure 20, and are stated to HD_2 = -59.0 dB and HD_3 = -52.33 dB.

The first derivative as shown in Figure 20 does also represent the small-signal gain. It shows a quadratic curve, which indicates a strong even order behavior in the first derivative. This can be translated to the VCO gain curve (left-side of Figure 20) by a stronger odd order nonlinearity. This was confirmed a higher HD_3 with respect to HD_2.

The determined coefficients a_0 to a_3 are also used the calculate the expected f_{VCO} by means of Equation (19). These calculated frequencies are shown in Figure 20 at the left-side by the red triangles. They match well with the simulations, which indicated that the distortion numbers are reliable.

The linearity performance of the whole ADC will be limited by the nonlinearity of the VCO. If this circuit will be used for the ADC, its SINAD will be limited to -52 dB. This number is rather poor when it needed to be focused on a 15 bit ADC. ADCs with this kind of resolution are hard to design. An ADC with a 15 bit resolution corresponds to a SINAD equal -92 dB. Thus 40 dB should be gained in order to compete with other state-of-the-art ADC architectures. From a recent published paper [12] it was shown that the performance of a VCO-based ADC can be increased with 40 dB by using calibration techniques. By implementing such a calibration, it will not necessarily mean that it gains 40 dB of performance. This is only possible when the so-called memory-effects are small. These effects are dynamic effects which depend on the signal frequency and are caused by energy elements like capacitors and inductors. If memory effects are relatively high, then they create distortion which is frequency dependent, and it will decrease the gained performance of the calibration. The consequence of these effects on the performance of the VCO will be elaborated in detail in the next chapter concerning dynamic distortion. The next paragraph will introduce an alternative approach to investigate the static distortion of VCOs.

3.2.3 Large-signal approach

The small-signal analysis as described earlier in this chapter gives some insight into the origin of the static distortion. It turned out that the frequency is almost proportional to the voltage V_{DD} and proportional to the square root of the current. In order to elaborate the origin of the distortion even further, a so-called Piecewise Linear Model (PLM) of an oscillator will be introduced here. This model is an general model and is not only restricted to oscillators [27]. The behavior of every oscillator can be approximated in pieces, at which each piece can be represented by a linear function. With this model the parameters that determine important properties of the oscillation frequency f_{osc} can be found. The waveform of the node voltages of every 4-stage differential ring oscillator can be approximated with a waveform as shown in Figure 21.

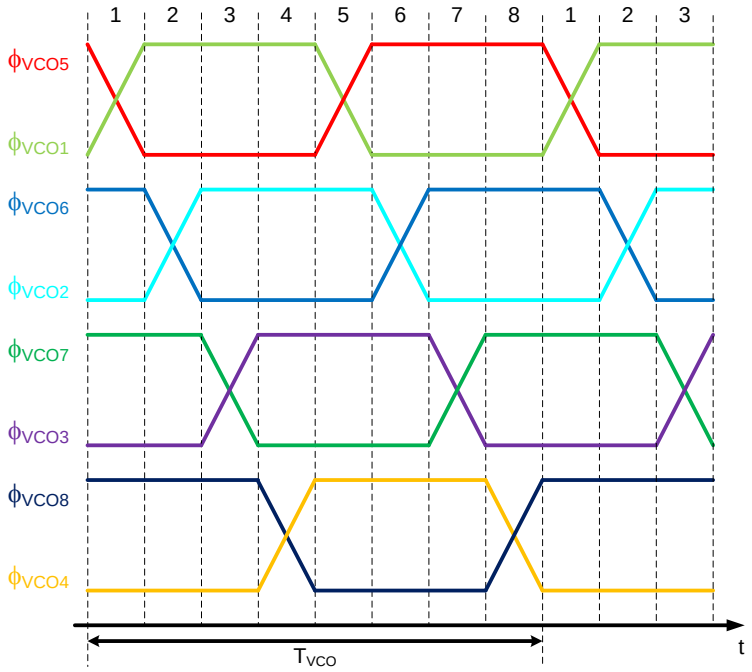

Figure 21: Piecewise Linear approximation of the node voltages of proposed circuit.

Figure 21 shows that one oscillation period can be divided in 8 equal parts (pieces). In each part two VCO node voltages have a transition between the two supply voltages, i.e. between the ground and V_{DD}. One of the two voltages has a rising edges, while the other node voltage has a falling edge. During the rising edge the capacitance present at the output node is charged with the PMOS transistor. For the proposed circuit (Figure 16) this is shown in Figure 22 with the red arrow. The capacitance is on later moment discharged with the NMOS transistor, as shown with the green arrow in Figure 22.

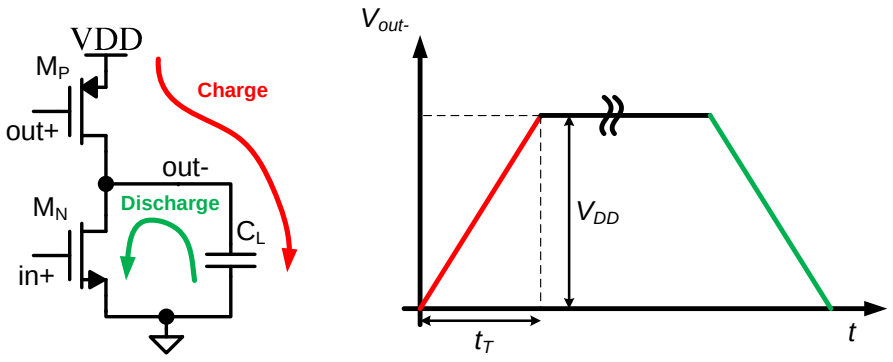

Figure 22: Half-delay cell of the proposed circuit during charging and discharging, and the belonging output node voltage.

The right-side of this figure shows the linear approximation of the output node voltage during both charge and discharge time intervals. The actual delay of a single oscillator stage (τ_d) can be approximated with this model to a transition time t_T, which represents the charging and discharging time of the node capacitance as shown in Figure 22. Hence, the oscillation frequency can be approximate by the following equation:

$$f_{osc} = \frac{1}{2N\tau_d} \approx \frac{1}{2N\eta t_T} \tag{31}$$

where η represents a proportionality constant, which is typically close to one, due to the linearization of the actual charge and discharge slope of the output node voltage. In reality, the output voltage of an inverter starts already decreasing before its input voltage has reached V_{DD}. This can be seen in the real time simulation results of the proposed VCO as shown in Figure 18.

During the charging time interval the output node is charged with a current from V_{DD}. Assuming the PMOS transistor behaves as an ideal current source, i.e. the transistor is always in saturation, the charge current can be expressed as Equation (32). This current can be equated to a capacitor charge current with the derivative of the charge voltage over time as shown in the equation below.

$$I_{D\_P} = \frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}\left(V_{GS\_P} - \left|V_{TH\_P}\right|\right)^2 = C_L\frac{dV_C}{dt} \tag{32}$$

The voltage step dV_C and the gate-source of the PMOS V_{GS_P} can be represented with this piecewise linear model to the voltage swing equal to V_{DD}, whereas the time step dt can be represented by the transition time t_T. Therefore, Equation (32) can be rewritten to the following expression:

$$t_T = \frac{2C_L L_P V_{DD}}{\mu_p C_{ox} W_p\left(V_{DD} - \left|V_{TH\_P}\right|\right)^2} \tag{33}$$

Now, the oscillation frequency can be rewritten by filling in Equation (33) into Equation (31) to the following expression:

$$f_{osc} \approx \frac{\mu_p C_{ox} W_p\left(V_{DD} - \left|V_{TH\_P}\right|\right)^2}{4\eta N C_L L_p V_{DD}} \tag{34}$$

This equation shows the dependencies of the oscillation frequency of the proposed circuit. It is shown that the frequency is proportional to the physical parameters of the PMOS (excluding the length L_P), while it is inverse proportional to equivalent output node capacitance C_L. However, more importantly, it also shows the relation to the power supply V_{DD}. As it can been seen the V_{DD} is nonlinear related to the oscillation frequency, because $(V_{DD}-|V_{TH\_P}|)^2/V_{DD}$ term is definitely not proportional to V_{DD}. Thus by tuning V_{DD}, it will result in a nonlinear change of the oscillation frequency of the VCO. It can be noted that the nonlinearity of the VCO is mainly caused by the nonlinear V-I characteristics of the MOS transistors!

In order to verify this piecewise linear model, analysis of the approximated oscillation frequency can be compared with the simulated frequencies from Cadence. To calculate the frequency, the physical parameters of the PMOS were found by performing a DC-simulation of one delay stage in Cadence. The output node capacitance was found by performing an AC-simulation at that node and observing the resulting AC-current. Then, the output node capacitance can be calculated by Equation (35).

$$C_L = \frac{\left|i(f_{AC})\right|}{2\pi f_{AC}} \tag{35}$$

The results of this analysis is shown in Figure 23 which is compared with the simulation results of the proposed circuit as shown in Figure 20. The proportionality factor η was determined by trial and error, and was set to 0.84 in order to match the formula with the simulation results.

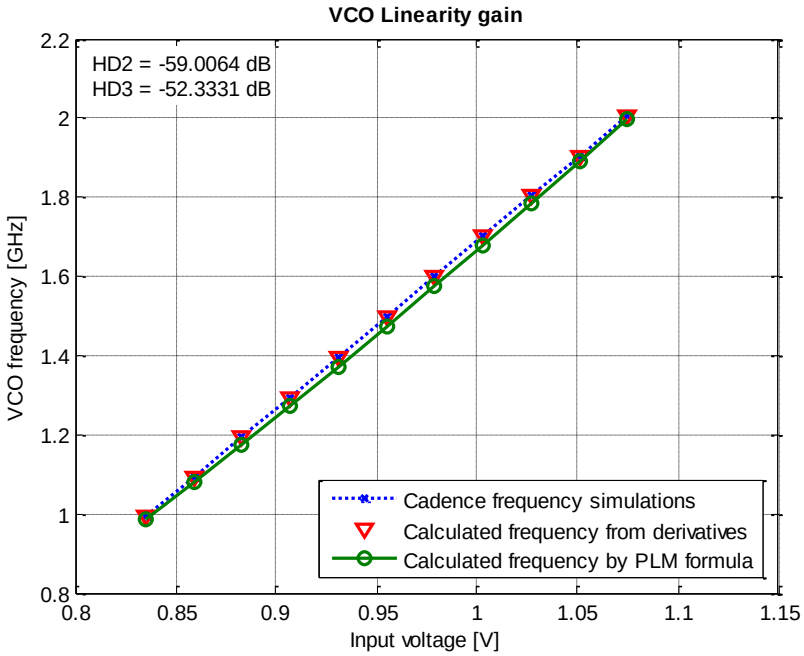

Figure 23: VCO Linearity gain of the proposed circuit with a comparison with the PLM formula.

From Figure 23 it can be concluded that the PLM formula expressed by Equation (34) corresponds with the simulation results from Cadence. There is only a very small difference between the calculated frequencies and the simulated frequencies from Cadence. Therefore, the analysis of the large-signal approach is sufficient to approximate the oscillation frequency and to determine the dependencies of that frequency.

3.3 Comparison with other VCO circuits

It became clear in previous paragraphs that the static linearity performance of the proposed circuit is limited to -52 dB caused by the third harmonic. This paragraph deals with alternative VCO circuits in order to see if they achieve less static distortion. First some alternatives are treated which are tuned by *gm*, after which alternatives are presented which are tuned by V_{DD}.

3.3.1 VCO circuits with *gm* tuning

The proposed circuit, which was discussed in previous paragraphs, was inspired by paper [23] from 2010. In that paper the presented VCO circuit was compared to an alternative, which is not tuned by the supply V_{DD}. It was stated that their performance on frequency tuning range, power efficiency and linearity was limited, but no simulation results were attached to that. In order to make a fair comparison with the proposed circuit, the alternative circuit is simulated in the same 65 nm CMOS process. In addition, an another VCO circuit was found in [12] which is also an interesting alternative, because the author claimed that it has a substantial VCO linearity. Therefore two alternatives without V_{DD} tuning will be simulated and compared in this section with the proposed circuit with V_{DD} tuning.

The first circuit was published in 2001 and was designed for the integration of many wireless transceiver building blocks on a single chip [26]. The two-stage VCO was designed to run at a 900 MHz operating frequency with a power supply of 2.5 V. For our application this design was extended to a four-stage VCO and was implemented in Cadence for simulations. The circuit of a single-stage is shown in Figure 24.

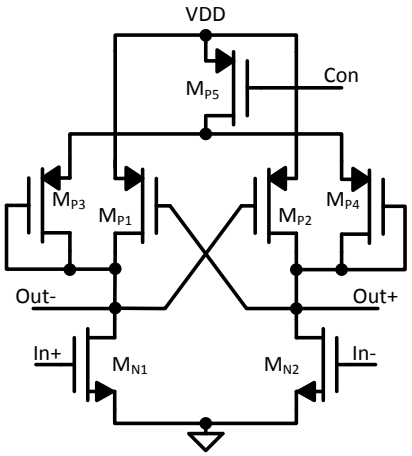

Figure 24: Circuit implementation of the presented VCO stage in [26], tuned by the PMOS M_{P5}.

The presented circuit as shown above consist of one differential input pair (M_{N1} & M_{N2}), one positive feedback pair (M_{P1} & M_{P2}), one diode-connected PMOS pair (M_{P3} & M_{P4}), and one PMOS transistor (M_{P5}) for frequency tuning. In comparison with the proposed circuit only the transistors M_{P3} to M_{P5} are added. With this design it is possible to tune the transconductance *gm* of the diode-connected transistors M_{P3} & M_{P4} by controlling the gate-source voltage of transistor M_{P5}. This will in turn alter the load of the PMOS transistors, and tune the oscillation frequency.

The transfer function of this VCO stage can be expressed as [26]:

$$H(s) = \frac{V_{out+}}{V_{in+}} = \frac{gm_{N1}}{\left(r_{O\_N1}^{-1} + r_{O\_P1}^{-1} + r_{O\_P3}^{-1} + gm_{P3} - gm_{P1}\right) + sC_L} \tag{36}$$

where the output node capacitance C_L represents in this case all capacitances to ground, i.e. the capacitances of M_{N1}, M_{P1} and M_{P3}. Therefore Equation (25) will hold if the capacitances of M_{P3} are also be included. In order to maintain oscillation the transconductance gm_{P1} should be higher than the total output load conductance. Thus the following expression should be considered:

$$gm_{P1} > r_{O\_N1}^{-1} + r_{O\_P1}^{-1} + r_{O\_P3}^{-1} + gm_{P3} \tag{37}$$

This design was simulated in Cadence with the 65 nm UMC technology. All transistors in this circuit (Figure 24) has a minimal length equal to 60 nm for maximum speed. Since the width of a CMOS transistor is proportional to the transconductance *gm*, the width of M_{P1} (and M_{P2}, due to symmetry) should be higher than M_{P3} (and M_{P4}). The best VCO performance in the desired frequency range from 1 to 2 GHz was found with the transistor dimensions as shown in Table 4. In order to achieve that frequency tuning range, the control voltage has a range from 0.34 V to 0.52 V, see Table 4.

Transistor	$M_{N1} = M_{N2}$	$M_{P1} = M_{P2}$	$M_{P3} = M_{P4}$	M_{P5}		Control range
W/L	4/0.06 µm	16/0.06 µm	8/0.06 µm	4/0.06 µm		0.34 – 0.52 V

Table 4: Transistor dimensions and the control voltage to achieve a full-scale tuning range from 1 to 2 GHz of the circuit as shown in Figure 24.

The linearity of this VCO circuit was analyzed on the same manner as the proposed VCO circuit as described in section 3.2. The results of this analysis is shown in Figure 25. First the VCO frequencies are determined in the Cadence simulations at different input voltages, after which the derivatives are taken with Matlab to calculate the second and third harmonic distortion numbers HD_2 and HD_3. The determined coefficients from the derivatives are also used to calculate the frequencies, which is also shown in the figure below.

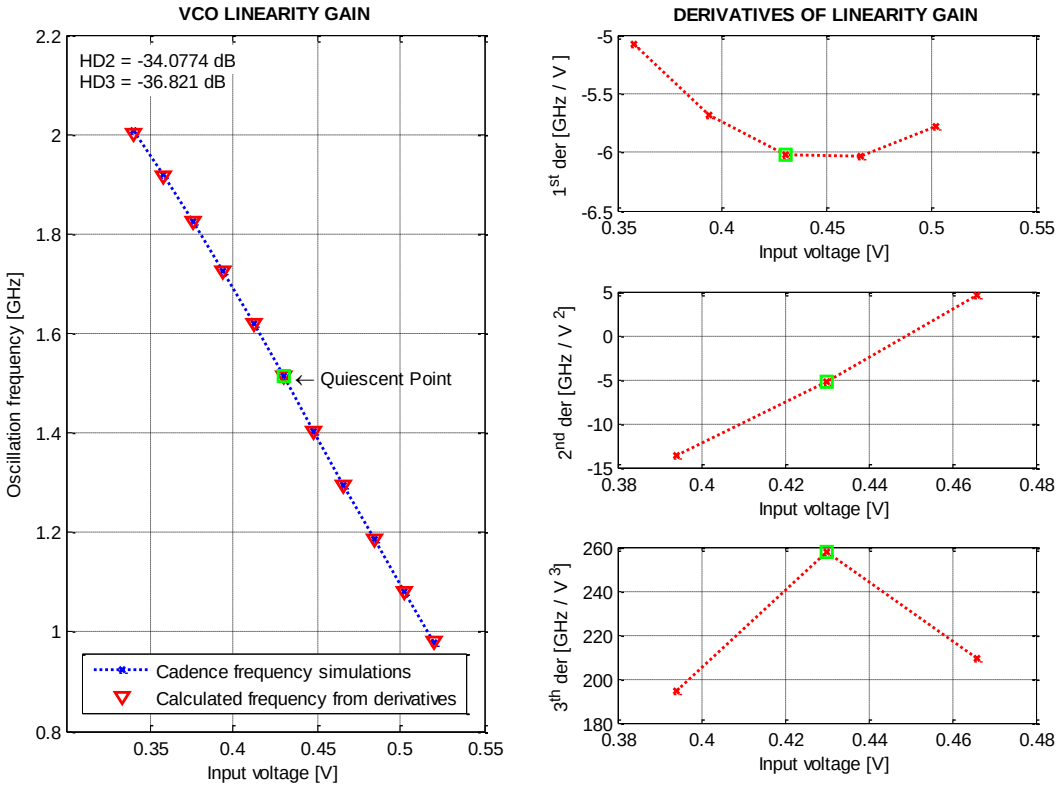

Figure 25: VCO linearity gain and their derivatives of the circuit as shown in Figure 24.

As it can be seen from Figure 25, the first derivative shows a local minimum near the quiescent point, while the second derivative is rather linear. The second- and third-order distortion numbers turned out to be -34.1 and -36.8 dB, respectively. Since the calculated frequencies from the derivatives matches the simulated frequencies, the distortion numbers give a good indication of the static distortion of both circuits.

The second alternative was found in a recently published paper referenced to a VCO-based Analog-to-Digital Converter [12]. In that design a 32-stage VCO was used in a conventional VCO-based ADC architecture, which also makes use of digital calibration techniques to enhance the dynamic range degraded by the nonlinearity of the VCO. For our purpose only a four-stage VCO was considered. The circuit design of a single stage is shown in Figure 26.

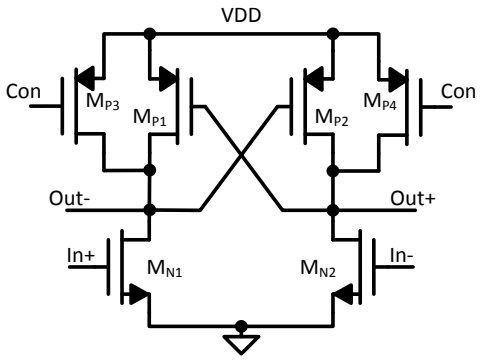

Figure 26: Circuit implementation of the presented VCO stage in [12], tuned by the transistors M_{P3} and M_{P4}.

The circuit as shown in Figure 26 is quite identical to the first presented alternative as shown in Figure 24. The main difference is that the second PMOS pair (M_{P3} & M_{P4}) is here not diode-connected and controlled by the drain-current from a third PMOS, but controlled directly via the gate-source voltage. In this way the *gm* of M_{P3} and M_{P4} can be tuned via a single-ended voltage in order to tune the oscillation frequency of this VCO. Also this circuit was simulated in the 65 nm UMC technology, where the length of all transistors were set on the minimal length for the maximum speed. In order to operate this circuit at a frequency range from 1 to 2 GHz, the best results were achieved by having the transistors dimensions as shown in Table 5. This table shows also the control voltage range to a achieve the desired frequency range. The linearity analysis of this circuit is shown in Figure 27.

Transistor	$M_{N1} = M_{N2}$	$M_{P1} = M_{P2}$	$M_{P3} = M_{P4}$		Control range
W/L	8/0.06 µm	16/0.06 µm	1/0.06 µm		0.07 – 0.37 V

Table 5: Transistor dimensions and the control voltage to achieve a full-scale tuning range from 1 to 2 GHz of the circuit as shown in Figure 26.

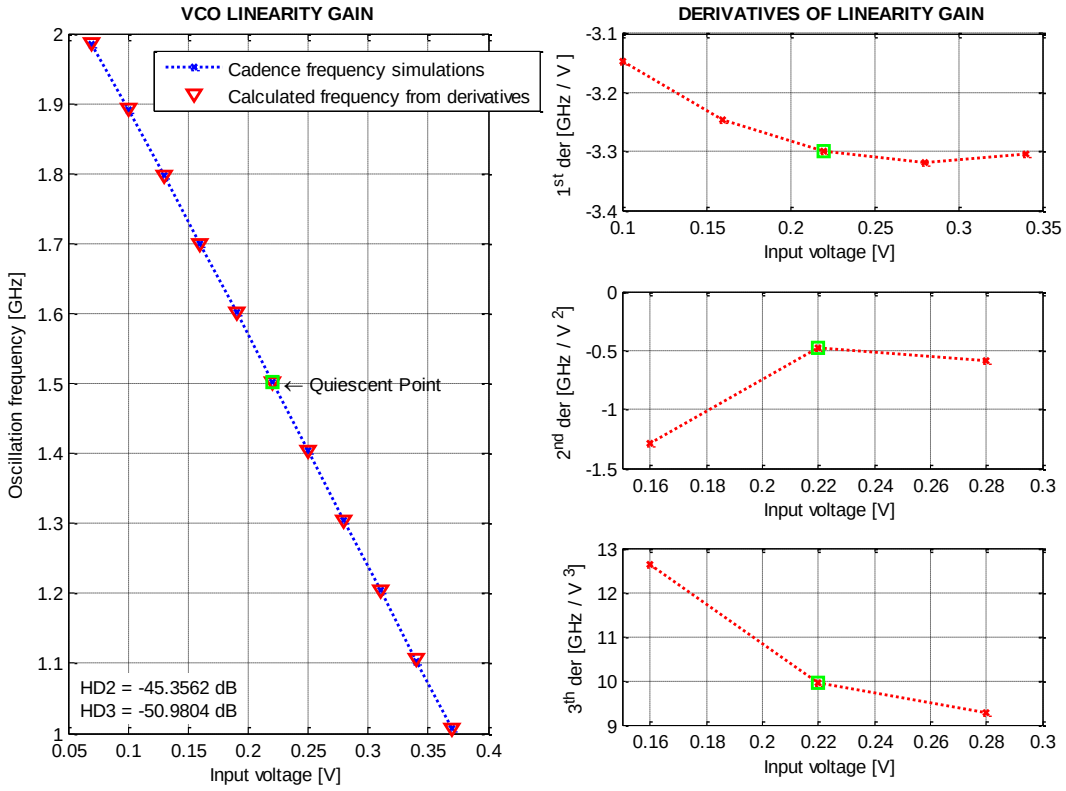

Figure 27: VCO linearity gain and their derivatives of the circuit as shown in Figure 26.

Figure 27 shows the linearity gain and their derivatives of the circuit presented in Figure 26, from what it turned out that the linearity is limited to HD_2 and HD_3 equal to -45.4 dB and -51.0 dB, respectively. The first derivative shows a higher order behavior, which determines the overall linearity performance. The second and third derivatives are not linear and do not pass zero crossings within the operating range.

In order to compare both alternatives with *gm* tuning, it can be concluded that the second alternative is more linear than the first alternative, because the distortion numbers are lower. Another point of interest is the fact that the second alternative has a much wider input voltage range compared to the first alternative. To achieve a frequency range from 1 to 2 GHz, the first alternative has an input voltage range equal to 0.34 V to 0.52 V, while the second alternative has a input voltage range equal to 0.07 V to 0.37 V. This means that the full-scale amplitudes, which are used for the calculation of the harmonic distortion numbers, are equal to 90 mV and 150 mV, respectively. The second alternative shows even with a larger input amplitude lower distortion numbers compared to the first alternative. Lowering that amplitude will result in even less static distortion.

3.3.2 VCO circuits with V_{DD} tuning

As it was mentioned before the proposed circuit as discussed in paragraph 3.2 was inspired by paper [23]. Since the presented VCO circuit in that paper shows promising results concerning low-power and linear-tuning aspects, this circuit seems to be an interesting alternative to investigate. To make a comparison also another VCO circuit with V_{DD} tuning was found in a recently released MSc thesis report within the ICD research group.

The first alternative VCO circuit was published in a paper in 2010, and can be tuned in frequency by controlling the V_{DD} [23]. It was designed to operate at a high frequency range from 1 to 9 GHz for radar applications. A 2-stage differential ring oscillator was presented to obtain quadrature outputs I and Q. For our purpose this design was extended to a 4-stage VCO in order to achieve 8 phase-shifted oscillation signals. The circuit implementation of one differential stage is shown in Figure 28.

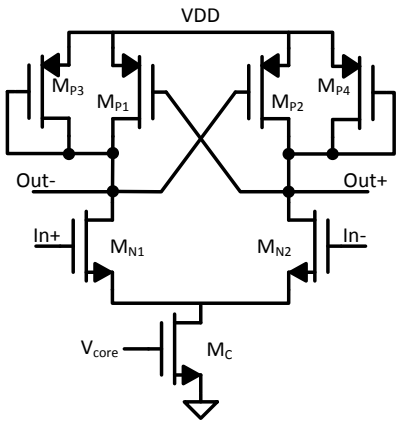

Figure 28: Circuit implementation of the presented VCO stage in [23], tuned by V_{DD}.

This design is rather similar to previous described VCOs, but there are differences. The stage as shown in Figure 28 consist of a NMOS differential input pair (M_{N1} & M_{N2}), a PMOS cross-coupled load (M_{P1} & M_{P2}), a PMOS diode pair (M_{P3} & M_{P4}) and an NMOS transistor M_C. The main difference is the

addition of the NMOS M_C in the tail of the stage. This transistor was designed by the author to operate in deep triode region. Then it consumes little headroom for the output voltage swing.

The single stage as shown in Figure 28 included in a 4-stage VCO was simulated in Cadence by using the 65 nm UMC technology. The length L of all transistors were set to its minimum length equal to 60 nm in order to achieve maximum speed. In order to operate the transistor M_C in deep triode the gate-source voltage of that transistor (V_{core} as shown in Figure 28) was set on 0.8 V. That was even the voltage where the best linearity performance was achieved. The transistor dimensions belonging to that performance and the V_{DD} range to achieve a VCO frequency from 1 to 2 GHz is listed in Table 6.

Transistor	$M_{N1} = M_{N2}$	$M_{P1} = M_{P2}$	$M_{P3} = M_{P4}$	M_C		V_{DD} range
W/L	16/0.06 µm	4/0.06 µm	1/0.06 µm	32/0.06 µm		0.775 – 0985 V

Table 6: Transistor dimensions and the V_{DD} voltage to achieve a full-scale tuning range from 1 to 2 GHz of the circuit as shown in Figure 28.

The VCO linearity gain of the presented VCO circuit, which is tunable by V_{DD}, is shown in Figure 29. The VCO frequencies are determined in Cadence at different V_{DD} voltages, while the derivatives are taken with Matlab afterwards. The determined linearity coefficients by Matlab are also used to calculate the frequencies of both alternatives, which is also shown in the figure below.

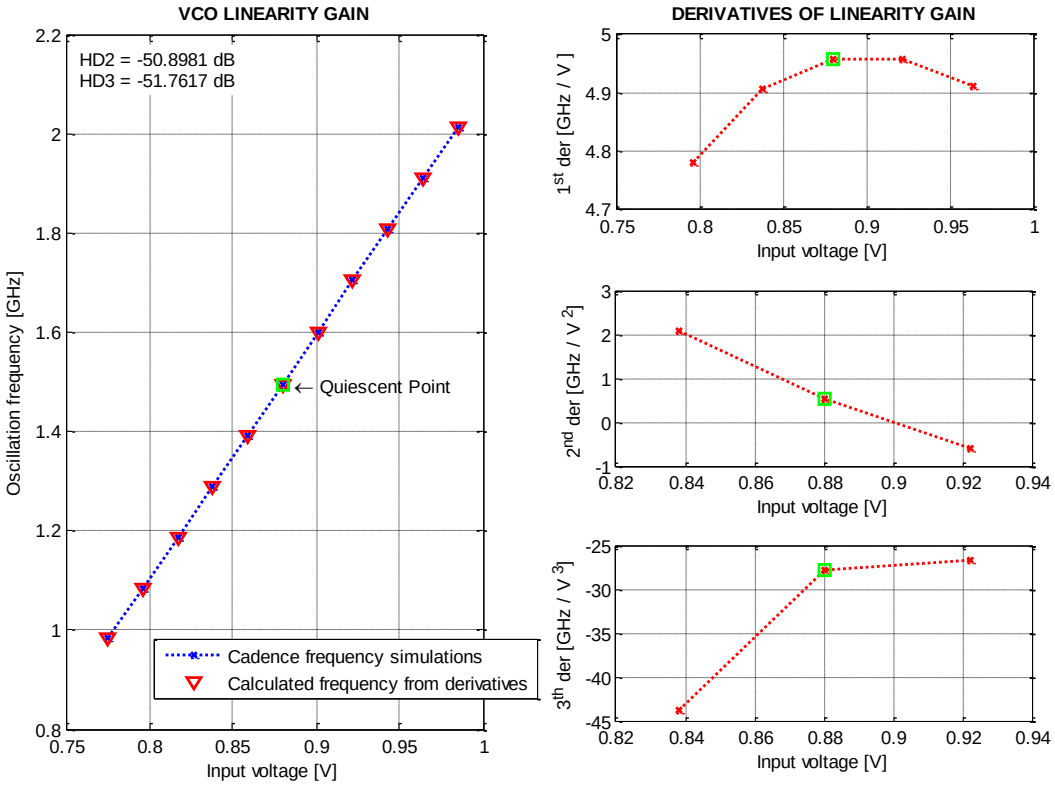

Figure 29: VCO linearity gain and their derivatives of the circuit as shown in Figure 28

It turned out that the presented circuit achieves static distortion numbers HD_2 and HD_3 equal to -50.9 dB and -51.8 dB, respectively. The second derivative shows a zero crossing at approximately 0.9 V, which indicates that the linearity will be improved by setting the quiescent point to that voltage.

The second alternative of a VCO circuit which can be tuned by V_{DD} was found in a recently released MSc thesis report and came originally from a paper published in 2009 [28]. That paper presents an ultra-low power analog front-end architecture for radio receivers. They implemented a two-stage VCO for the generation of the clock signals. Here, the design is implemented in a 4-stage VCO to generate eight VCO output signals. The circuit implementation of a single stage of this design is shown in Figure 30.

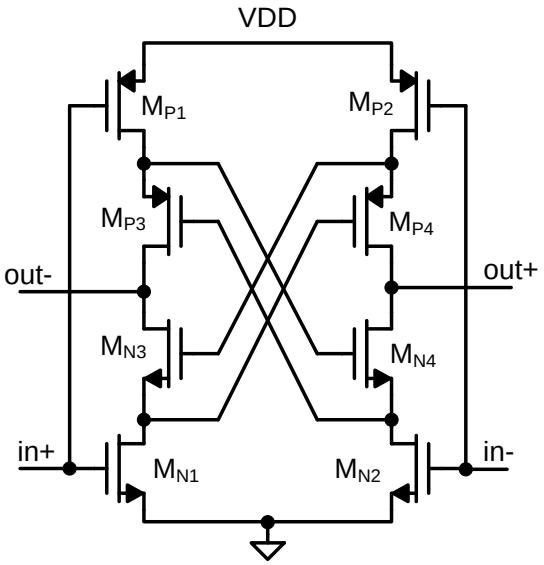

Figure 30: Circuit implementation of the presented VCO stage in [28], tuned by V_{DD}.

As it can be seen from Figure 30 this design is completely different from previous described VCOs. It consist, in fact, of two inverters (M_{N1} with M_{P1} & M_{N2} with M_{P2}) with four positive cross-coupled transistors to ensure oscillation. These inner cross-coupled transistors (M_{N3}, M_{N4}, M_{P3} and M_{P4}) prevent the outputs of this stage from changing if the inputs are not switched between the ground and V_{DD} at the same time. This structure has also a full rail-to-rail output swing and no DC current source, which saves power consumption.

This design was implemented in a 4-stage VCO in Cadence (UMC 65 nm), assuming minimal length (60 nm) to achieve maximum speed. The best linearity performance was achieved with the transistor dimension as stated in Table 7. This table shows also the V_{DD} range to achieve the VCO frequency range from 1 to 2 GHz.

Transistor	**M_{N1} = M_{N2}**	**M_{N3} = M_{N4}**	**M_{P1} = M_{P2}**	**M_{P3} = M_{P4}**		**V_{DD} range**
W/L	8/0.06 µm	4/0.06 µm	8/0.06 µm	4/0.06 µm		0.835 – 1.095 V

Table 7: Transistor dimensions and the V_{DD} voltage to achieve a full-scale tuning range from 1 to 2 GHz of the circuit as shown in Figure 30.

The linearity analysis of this circuit is shown by their VCO linearity gain and derivatives in Figure 31.

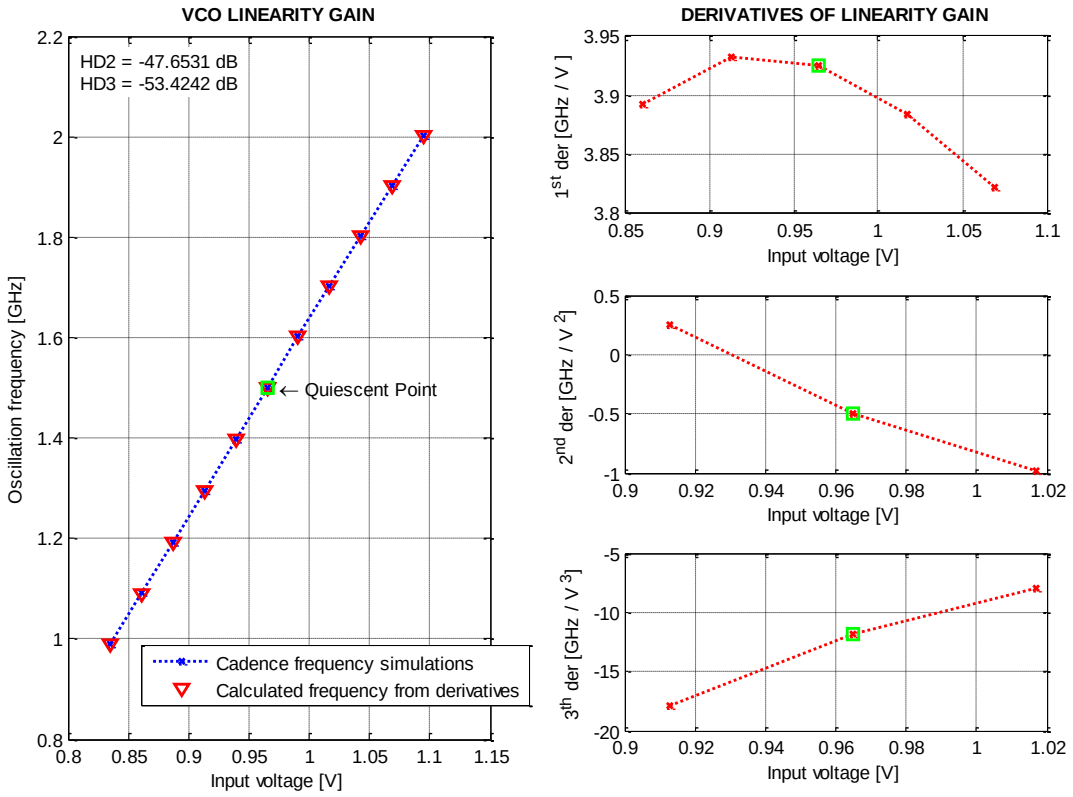

Figure 31: VCO linearity gain and their derivatives of the circuit as shown in Figure 30.

As it can be seen from Figure 31, the first derivative has a local maximum near the quiescent point, while the second derivative has a zero crossing near the quiescent point. This indicates that the linearity can be improved by setting the quiescent point to approximately 0.93 V. Both second and third derivatives show a rather linear behavior. It turned out that the static distortion of this circuit is limited to HD_2 equals -47.7 dB and HD_3 equals -53.4 dB.

In order to compare both alternative with frequency tuning by V_{DD}, the first alternative has less static distortion compared to the second alternative. The first alternative achieves approximately 3 dB lower HD_2 and approximately 2 dB higher HD_3 in comparison with the second alternative. If a comparison is made with the proposed circuit as discussed in paragraph 3.2, it can be concluded that both presented alternative circuits discussed here have worse linearity performance compared to the proposed circuit. Therefore the proposed ring VCO circuit (Figure 16) can be chosen for the implementation of the ADC over the presented alternatives discussed here. But, still an input buffer is needed for the proposed circuit in order to tune the oscillation frequency by the power supply V_{DD}. The design of this buffer be the subject of the next paragraph.

3.4 Design aspects of the input buffer

The proposed VCO circuit as shown in Figure 16 achieves less static distortion in comparison with the preceding alternative VCO circuits. However, this circuit still needs an input buffer, because its VCO frequency is tuned by V_{DD}. This section will investigate first if it is possible to control the proposed VCO by a current instead of a voltage, after which a voltage buffer implementation will be treated.

3.4.1 Controlling the VCO with a current

The easiest way to control the VCO by a current, is by implementing a voltage-controlled current source (VCCS). That can even be done by using a single PMOS transistor between the V_{DD} and the V_{DD} connection of the VCO circuit. In this way the input voltage is transformed to a current to supply the VCO. Two simple architectures are shown in Figure 32. In the first architecture (left-side of the figure) the input voltage is directly transformed to a supply current, while in the second architecture (right-side of the figure) the input voltage is transformed to a supply current via a NMOS as a current source and PMOS current mirror.

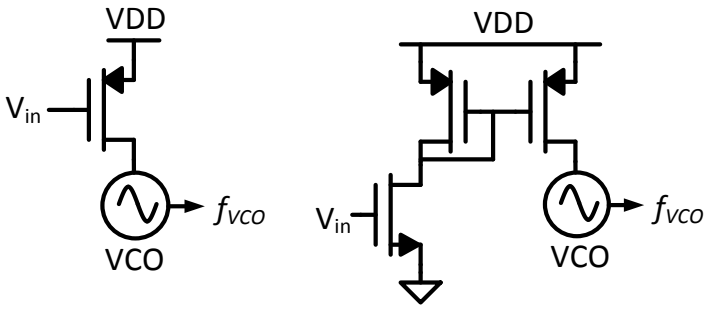

Figure 32: Two simple architectures to control the VCO by a current.

In order to investigate if this manner of controlling is sufficiently linear, the frequency versus input current behavior of the proposed VCO needs to be known. The proposed VCO circuit as shown in Figure 16 was first simulated with a voltage source as input, as described in section 3.2. The average current consumption of the input source during these simulations are shown in Figure 33 by the green dotted line with crosses. The belonging distortion numbers HD_2 and HD_3 are also plotted in that figure, and turns out to be rather high, i.e. the highest distortion of approximately -27.9 dB. The second simulation that was considered, is simulating the proposed VCO circuit as shown in Figure 16 by a current source as input. These simulated frequencies versus input current are shown in Figure 33 by the bleu dotted line with crosses. The distortion numbers of these simulations are also shown, and correspond nearly with the simulations with the voltage source as input. Note that both simulation results are plotted in one graph, they are simulated independent of each other.

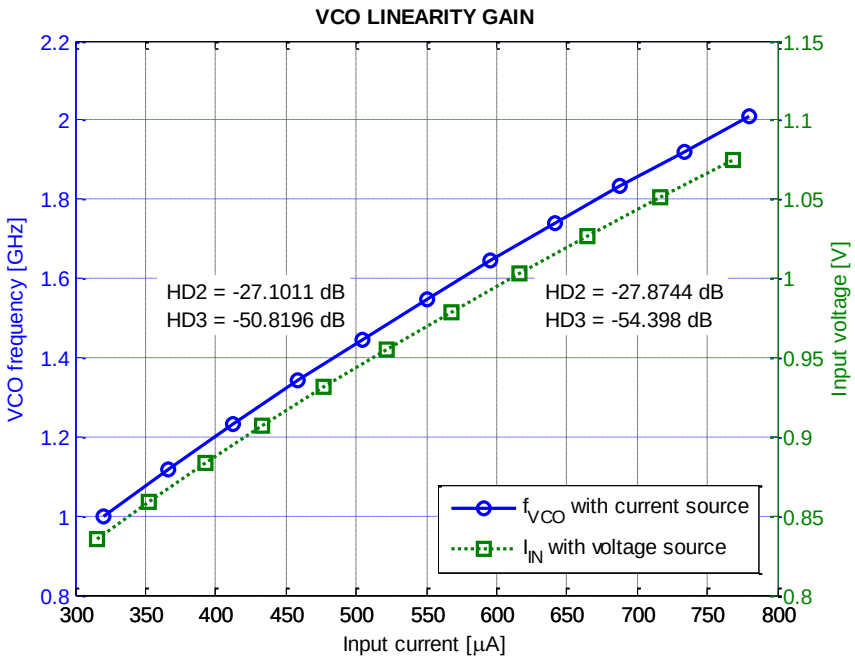

Figure 33: Linearity gain of the proposed VCO (Figure 16) with: 1) simulated VCO frequency f_{VCO} with a current source as input, and 2) simulated input current I_{IN} with a voltage source as input.

By simulations it turned out that the proposed VCO stage has a more linear f_{VCO} as a function of V_{in} than f_{VCO} as a function of I_{in}. Thus in other words, controlling the VCO by a current source will give more static distortion than controlling it by a voltage source. This is also confirmed by Equation (28), where it is stated that the oscillation frequency of the proposed VCO circuit is proportional to the square root of the current. The presented architectures as shown in Figure 32 have a voltage V_{DD} of the VCO which is not regulated by the input voltage. The input voltage is in fact transformed to a supply current, while a voltage buffer is needed.

The simple architectures with a VCCS as shown in Figure 32 were simulated, and the results confirm this reasoning. The static distortion becomes worse when the VCO is controlled by a current. Therefore a regulated voltage buffer is needed in order to let the distortion of the VCO be dominated over the distortion of the input buffer.

3.4.2 With a voltage buffer

Since a voltage input buffer is needed, probably an architecture with an OPAMP would be a good solution. There are many possibilities for designing a voltage buffer, but one thing should be kept in mind that the linearity of the voltage buffer should be higher than the linearity of the VCO. Otherwise the buffer will decrease the linearity performance of the ADC even more than by the already existing nonlinearity of the VCO. Then also all linearity improvements by designing a good VCO will be useless.

If the VCO will be buffered directly with a source follower, then simulations are useful to investigate the effects of the buffer on the VCO nonlinearity. Source follower stages or also known as common-drain stages, are attractive as a voltage buffer, because of its low output resistance and high input resistance. Furthermore, such stages can have a unity voltage gain and a high current gain, which is

essential for a voltage buffer. The implementation of a source follower as buffer connected to the VCO is shown in Figure 34.

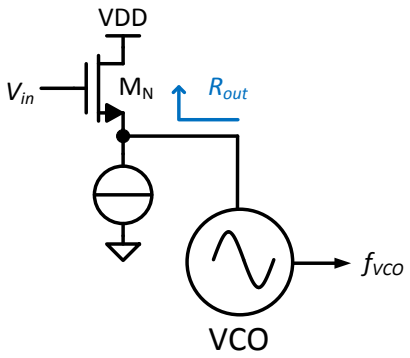

Figure 34: Implementation of a source follower as voltage buffer.

The output resistance of the presented source follower is equal to the inverse of the transconductance *gm* of the NMOS. This can be written in mathematical form as Equation (38).

$$R_{out} = \frac{1}{gm_N} \tag{38}$$

Assuming that the NMOS operates in strong inversion, the *gm* can be determined with the following expression:

$$gm = \frac{2I_D}{(V_{GS} - V_{TH})} \tag{39}$$

where the term within the brackets represents the overdrive voltage of the transistor. This value could typically have a value around 100 mV. The two aforementioned equations show that the transconductance *gm* is proportional to the drain current I_D, and the output resistance inverse proportional to I_D. From Figure 33 it turned out that the input current range of the VCO is equal to 320 µA to 760 µA. Since that current will flow through transistor M_N, the output resistance can be approximated between 160 Ω and 70 Ω. Using a rather midscale solution, the source follower can be modeled for simulation purposes by a resistor of 120 Ω. Then, by performing a voltage sweep of V_{DD}, the effects of the VCO nonlinearity can be monitored. The results of this simulation as well as the belonging distortion numbers are shown in Figure 35.

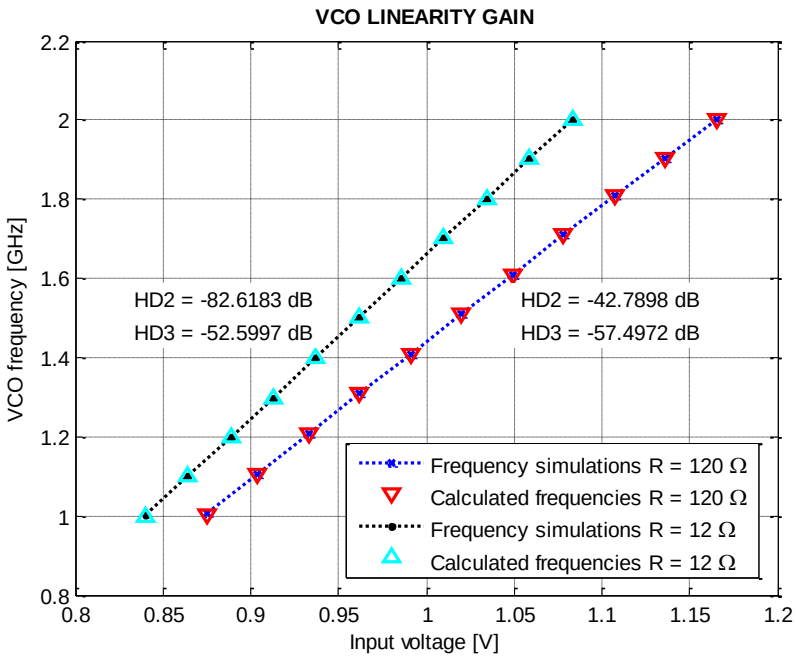

Figure 35: Linearity gain of the proposed VCO with a series resistance R between the V_{DD} connection of the VCO and a voltage source, representing the output resistance of the transistor (Figure 34).

As it can be seen from Figure 35 when the series resistance is equal to 120 Ω, the dominant static distortion is degraded from -52.33 dB without resistance (Figure 20) to -42.78 dB with resistance (equal to 120 Ω). This is almost a decrease of 10 dB in dynamic range, which is quite a lot. The second derivative of this simulation result (not shown in the figure) showed that it did not cross the zero line in derivative value, whereas the second derivative of the proposed circuit (see Figure 20) does. Besides that, the third derivative is more fluctuating compared to proposed circuit. Thus using a straightforward source follower as input buffer will degrade the VCO linearity transfer even more than the already existing nonlinearity of the VCO itself. The distortion coming from the source follower can only be less dominant if the output resistance of the transistor M_N is low. A good way to achieve that is by using an OPAMP, which controls the gate-voltage of the transistor and senses the V_{DD} voltage of the VCO. The described implementation is shown in Figure 36. With this structure the OPAMP ensures that the input voltage V_{in} is equal to the V_{DD} voltage of the VCO.

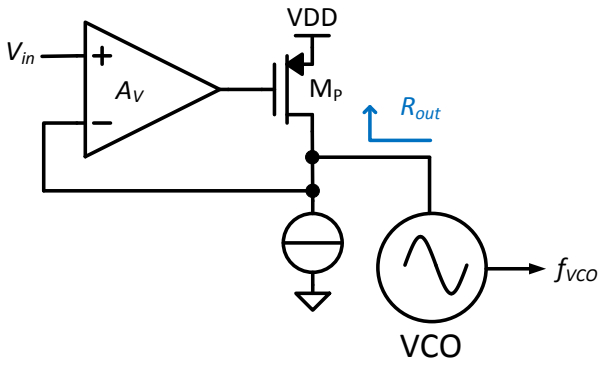

Figure 36: Implementation of a source follower with OPAMP to decrease output resistance.

Note that in this configuration a PMOS is preferred over a NMOS, since the PMOS has less voltage-drop over the drain and source connections of the transistor. It can mathematically be proven that

the output resistance of the buffer implementation with OPAMP (Figure 36) can be calculated by Equation (40). The parameter A_V represents the closed-loop voltage gain of the OPAMP.

$$R_{out} = \frac{1}{A_V gm_P} \tag{40}$$

This equation shows by adding a OPAMP circuit with feedback to the source follower, the output resistance of the transistor M_P will be reduced proportional with the voltage gain of the OPAMP. Note that this only holds at low frequencies. If the OPAMP gain drops as a function of frequency, the output resistance starts to increase. Assuming a 10 times closed-loop voltage gain, the output resistance of this implementation is reduced to 12 Ω. The consequence to the nonlinearity of the VCO transfer can easily investigated, if a simulation sweep is performed with a series resistor equal to 12 Ω. The results of this sweep including the distortion numbers are also shown in Figure 35. The derivatives of this simulation correspond to a large degree with the derivative from the proposed circuit as shown in Figure 20. Figure 35 shows that the dominant distortion in case of a 12 Ω series resistor is in close agreement with the already existing dominant distortion from the VCO itself, i.e. HD_3 = -52.33 dB (proposed circuit) versus HD_3 = -52.60 dB (proposed circuit with a 12 Ω series resistor). It can be concluded that the proposed circuit with a low series resistor (12 Ω) will not add additional distortion to the overall voltage-to-frequency transfer. An interesting observation can be drawn if we look at the second-order distortion. This HD_2 is improved from -59.0 dB without buffer implementation to -82.6 dB with 12 Ω series resistor implementation. It turned out that the second derivative (in case of 12 Ω series resistor) was determined to zero at the quiescent point. This cancels the second-order distortion of the VCO linearity gain, which results in a sufficient low HD_2.

3.5 Saw-tooth oscillator circuit

Until now, several voltage-controlled ring oscillators were treated in order to find the oscillator with the highest linearity. That ring oscillator can then be used to control linear ramp circuits that represent the continuous phase of the oscillator. With this mechanism a new VCO-based ADC can be developed with a high resolution compared to convention VCO-based ADCs. The ring oscillator and the linear ramp circuit can also be combined together, which results in a saw-tooth oscillator. This type of oscillator was the subject of a PhD work at the ICD group at the University of Twente in 1999 [22]. At the beginning of this project by the former MSc student, this oscillator was the first interesting implementation to look at. It is in fact all we need: a controllable oscillator with linear ramp signals (and no need of an input buffer). However, from the work of the former MSc student the control nonlinearity and the power consumption of the saw-tooth oscillator was relatively high [20]. Therefore, an alternative solution with a ring VCO and a linear ramp circuit appear to be less power consuming and more linear compared to the saw-tooth oscillator. The outcome of previous work was that the ring VCO with ramp circuit is a better solution for the ADC than the saw-tooth oscillator. Since the proposed ring VCO (section 3.2) turned out to be limited to the third harmonic distortion of approximately -52 dB, it is not self-evident that it is the best solution for the new VCO-based ADC design. Since dynamic distortion of oscillators become also of interest, a completely different oscillator design like this is worthy to investigate. Especially, if another 40 dB of dynamic range should be gained by using digital calibration for the desired 15 bit ADC. Hence, the saw-tooth oscillator is still an interesting alternative, which is the subject of this paragraph.

The saw-tooth oscillator presented in the PhD work is interesting, but not dimensioned for our purpose. It is designed in a 0.8 µm CMOS process and it has only a full-scale frequency tuning range of 1MHz. On the other hand, it achieves static distortion numbers equal to approximately -70 and -90 dB for the HD_2 and the HD_3, respectively. Our attention will first go to the latest version of the saw-tooth oscillator presented in previous MSc work, because it was already designed in the 65 nm process and achieves better saw-tooth waveforms and higher linearity results compared to previous versions in the 65 nm process. In order to control the saw-tooth oscillator conveniently a four-stage oscillator is preferred. The circuit implementation of a single stage is shown in Figure 37.

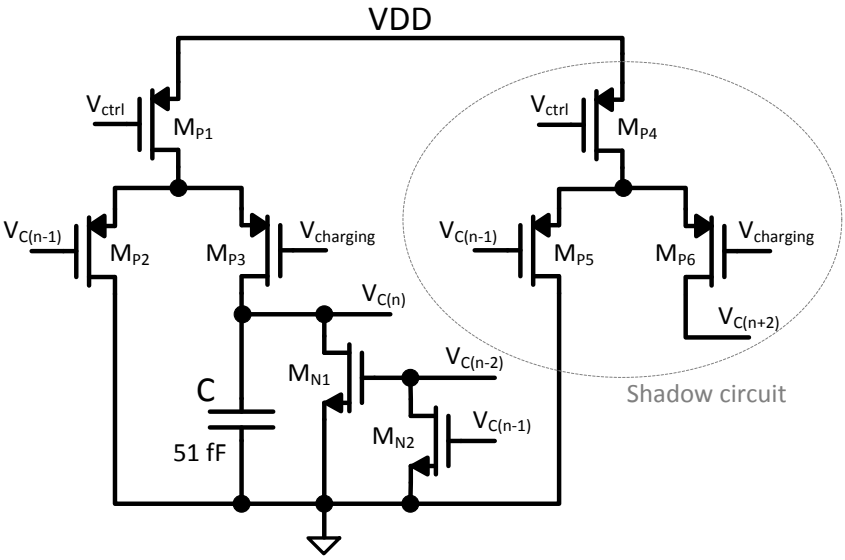

Figure 37: Implementation of a single stage saw-tooth oscillator.

A single saw-tooth oscillator stage as shown in Figure 37 is based on the principle of charging the capacitance *C* with a constant current. The current source that delivers that current is represented by the transistor M_{P1}, which makes controlling the frequency of the oscillator possible by adapting the gate-source voltage that transistor. Note that the 4-stage saw-tooth oscillator will be controlled by an ideal current source connected to a PMOS current mirror, at which the second-half of that mirror is represented by the transistors M_{P1} and M_{P4} of all four stages. When charging a capacitance with a constant current, will result in a linear increase of the capacitance voltage. That is exactly what is needed in order to represent the continuous phase of the oscillator. The ideal waveforms of the 4-stage saw-tooth oscillator is shown in Figure 38.

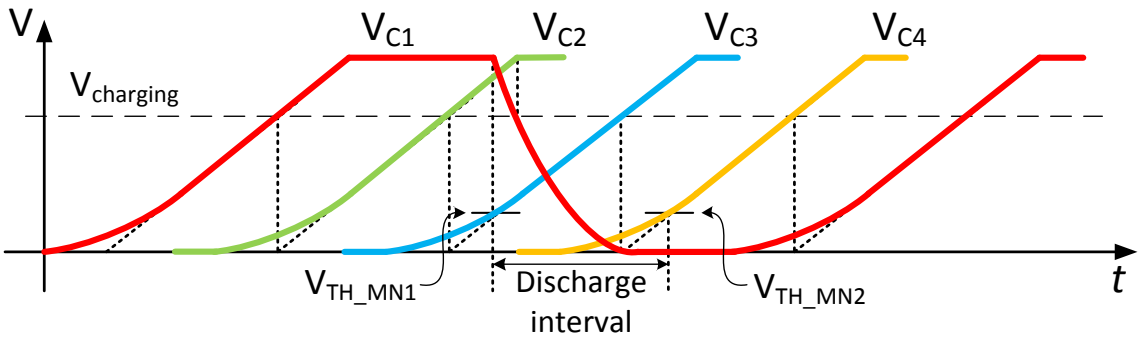

Figure 38: Ideal waveforms of the 4-stage saw-tooth oscillator.

The transistors M_{P2} and M_{P3} decide if the current will be used to charge the capacitor or flow directly to the ground. That decision depends on the capacitance voltage of previous stage $V_{C(n-1)}$. If that voltage is higher than the fixed voltage level $V_{charging}$, the current will flow into the capacitor resulting a linear growth of $V_{C(n)}$. The voltage $V_{C(n)}$ will stop increasing by bypassing the current to the ground via M_{P2}, when the capacitor voltage of previous stage ($V_{C(n-1)}$) falls below $V_{charching}$. This is represented in Figure 37 for the second stage, showing a stop of V_{C2} when V_{C1} falls below $V_{charging}$. Consequently, the capacitor starts to discharge when $V_{C(n-2)}$ exceeds the threshold voltage of transistor M_{N1}. To ensure the capacitor can be charged again in the new cycle, the transistor M_{N2} stops the discharge time interval by switching the transistor M_{N1} off. Otherwise the current in the next cycle will be flowing to ground via M_{N1}. To turn off M_{N1}, the gate of transistor M_{N1} will be put to ground by M_{N2} when the capacitor voltage of previous stage $V_{C(n-1)}$ exceeds the threshold voltage of M_{N2}. The timing of this discharge mechanism is also shown in Figure 37 for the first stage V_{C1}.

The former MSc student added a shadow circuit in each stage as shown in Figure 37, in order to improve the linearity of the oscillator. It is a copy of the main oscillator stage and serves as an elimination of the frequency dependent capacitance of transistor M_{N1}. It turned out that without the shadow circuit the transistor M_{N1} creates more nonlinearity in the control characteristic [20].

The saw-tooth oscillator was simulated in Cadence in the 65 nm UMC technology, and all the transistor lengths were set to its minimal length for the maximum speed. As a good starting point, the transistor widths were take over from the previous MSc work. Simulations show corresponding distortion results compared to previous work, i.e. the dominated second-order distortion is equal to -37.6 dB. However, by increasing the transistor widths of M_{P2} and M_{P3} by 1.5 times, the oscillator control linearity is improved significantly. The dimensions of the saw-tooth oscillator used for the simulations are shown in Table 8. The power supply V_{DD} was as usual set to 1.2 V and the fixed charge voltage $V_{charging}$ to 0.5 V. Table 8 list also the control range of the input current to achieve a frequency tuning range from 1 to 2 GHz.

Transistor	**M_{P1}**	**$M_{P2} = M_{P3}$**	**M_{N1}**	**M_{N2}**	**M_{P3}**	**$M_{P4} = M_{P5}$**	**Control range**
W/L	40/0.06 µm	30/0.06 µm	2/0.06 µm	4/0.06 µm	30/0.06 µm	15/0.06 µm	360 – 780 µA

Table 8: Transistor dimensions and the control current to achieve a tuning range from 1 to 2 GHz of the saw-tooth circuit as shown in Figure 37.

The results of the linearity simulations of the saw-tooth oscillator are presented in the figure below (Figure 39). The input current controls the charge current of each stage via PMOS current mirrors. In order to sweep the oscillator between 1 and 2 GHz the input current range is determined at 360 µA to 780 µA. This results in a quiescent point of 570 µA, which will be used to calculate the static distortion via the derivatives.

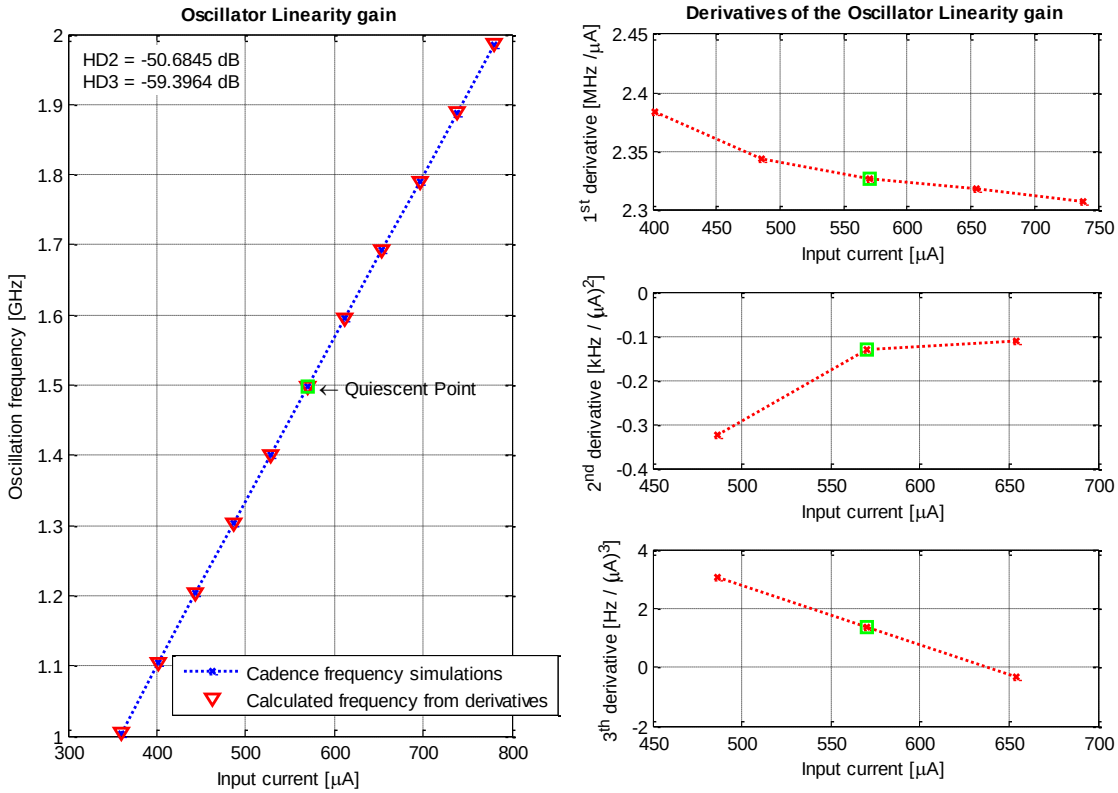

Figure 39: Oscillator linearity gain and their derivatives of the saw-tooth oscillator.

As it can been seen from Figure 39 the control characteristic is quite linear and achieves lower distortion numbers, i.e. HD_2 equal to -50.68 dB and HD_3 equal to -59.4 dB. This is an improvement of more than 13 dB of the second-order distortion compared to the saw-tooth oscillator designed in previous work. With the small modification of the transistor widths of M_{P2} and M_{P3}, this oscillator is qua distortion in closeness with the proposed ring oscillator as presented in section 3.2. The dynamic range of this oscillator is limited by the second-order distortion equal to -50.68 dB, while the dynamic range of the proposed ring oscillator is limited by the third-order distortion equal to -52.33 dB. Figure 39 shows also that higher linearity results can probably be obtained, if the quiescent point is increased with approximately 100 µA to create a zero in the third derivative.

3.6 Comparison between the different oscillators

In order to compare the different oscillators, Table 9 summarizes the static distortion numbers of the presented oscillators treated in this chapter. They are calculated at a full-scale input amplitude to achieve an oscillation frequency range from 1 to 2 GHz. The belonging input ranges and amplitudes for the different oscillators are also shown in the table below.

Oscillator type	***Input range for 1-2 GHz***	***Full-scale Amplitude***	***Static Distortion***	
			HD_2 [dB]	***HD_3 [dB]***
Oscillator with still the need of an input buffer				
Proposed VCO [20]	0.835 - 1.075 V	120 mV	-59.01	-52.33
Alternative 1 with V_{DD} tuning [23]	0.775 - 0.985 V	105 mV	-50.90	-51.76
Alternative 2 with V_{DD} tuning [28]	0.835 - 1.095 V	130 mV	-47.65	-53.42
Oscillator with buffered input				
Alternative 1 with *gm* tuning [26]	0.34 - 0.52 V	90 mV	-34.08	-36.82
Alternative 2 with *gm* tuning [12]	0.07 - 0.37 V	150 mV	-45.36	-50.98
Proposed VCO with 120 Ω series R	0.875 - 1.165 V	145 mV	-42.79	-57.50
Proposed VCO with 12 Ω series R	0.84 - 1.08 V	120 mV	-82.62	-52.60
Saw-tooth [22]	360 - 780 µA	210 µA	-50.68	-59.40

Table 9: Static distortion summary of the different treated oscillators.

From the table it can be concluded that the proposed VCO achieves less static distortion compared to the alternatives with V_{DD} tuning. In addition, the proposed VCO is also more linear than in comparison with the alternatives with *gm* tuning. However, these last two alternatives do not need an input buffer, while the proposed VCO does. If the proposed VCO will be connected to an input buffer with a certain output resistance, this resistance should be low enough to prevent an increase of the static distortion. It even turned out that there is an optimum in series resistance, since both distortion numbers HD_2 and HD_3 are lower in case of a 12 Ω series resistor than compared to the proposed VCO without resistor. The saw-tooth is a proper alternative, because the static distortion numbers are reasonably close to the proposed VCO and it does not need an input buffer. Note that the saw-tooth oscillator even has the desired saw-tooth shape, which represents linearly the phase of the oscillator.

In order to determine which oscillator is appropriate for the ADC application, the dynamic distortion of an oscillator is another important objective. This is the subject of the next chapter, where the proposed ring VCO will be compared to the saw-tooth oscillator.

4 Dynamic distortion analysis on circuit level

Dynamic distortion is a measure of the distortion which depends on the input frequency. It is often characterized as a function of input frequency, where so-called memory effects can be identified. What these effects are and how they can be analyzed, is the subject of the next paragraph. In the second paragraph are the simulation results discussed. The end of this chapter is dedicated to an alternative approach to determine memory effects.

4.1 Characterization method

In general, memory effects are defined as changes in amplitude and phase of distortion components caused by changes in input frequency. They become in particular important when these components need to be cancelled by some manner of calibration. If the distortion components varies over frequency, they cannot be cancelled entirely by using calibration techniques.

The dynamic distortion of analog circuits are usually determined in the frequency domain by using the FFT. This is a commonly used procedure for characterizing analog circuits, such as A/D converters, amplifiers, etc. This procedure will also hold to characterize the dynamic distortion of VCOs. The characterization can be distinguished between single-tone en two-tone simulations, which correspond to applying one pure sinusoidal signal or applying two sinusoidal signals at the input, respectively. When one sinusoidal signal is applied at the input, it will give the distortion numbers HD_2 and HD_3. On the other hand, two sinusoidal signals at the input will give second-order and third-order intermodulation distortion terms, IM_2 and IM_3 respectively.

If one sinusoidal signal with a certain frequency f_{in} is applied to the input of the VCO, the oscillation frequency of the VCO will have the same sinusoidal shape over time. In other words, a sinusoidal input voltage will give an oscillation frequency f_{VCO} which changes sinusoidally over time with a frequency equal to f_{in}. This principle is shown in Figure 40.

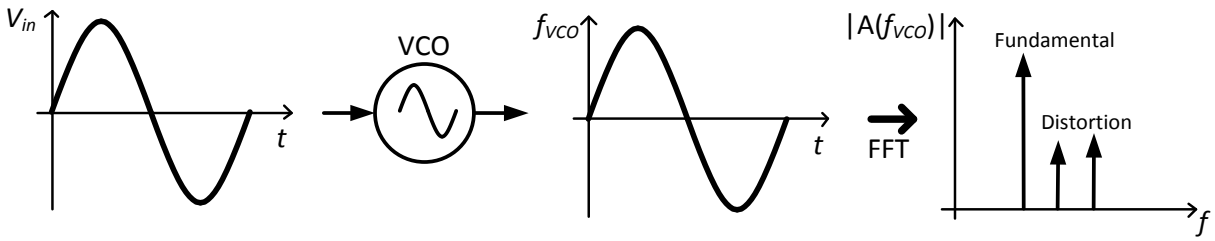

Figure 40: Dynamic characterization of a nonlinear VCO at single-tone (one input frequency).

To determine the dynamic distortion of the VCO, an FFT of the VCO's output signal will give a frequency spectrum where harmonic distortion terms can be deduced. The spectrum shows the contribution of noise and distortion by the VCO as function of frequency. It is called dynamic distortion, because the simulated distortion terms may depend on the input signal frequency. The distortion at low input frequencies should correspond to the static distortion performance (treated in previous chapter). By changing the frequency of the single-tone input at different simulations, the frequency dependent distortion of the VCO can be characterized.

The two-tone simulations are also of interest when characterizing the dynamic distortion of VCOs. By applying two input frequencies, intermodulation terms (IM) of both tones appear near the input frequencies in the frequency domain. In particular, the third-order distortion terms $2 \cdot f_{in1} - f_{in2}$ and $2 \cdot f_{in2} - f_{in1}$, will arise at a tone spacing distance of Δf (being the distance between the two input frequencies) adjacent to the fundamental input tones. That is undesired, since the distortion terms exist within the signal band. The two-tone simulations with varying tone spacings will show how the distortion responds to changes in frequency (indicating memory effects).

However, a problem arises when determining the oscillation frequency f_{VCO} continuously over time. Figure 40 shows that a continuous f_{VCO} is needed in order to determine the distortion terms by using an FFT. An usual method could be to identify the time period of the VCO output signal, and take the reciprocal to obtain the oscillation frequency. This method and its consequences will be discussed in the next section.

4.1.1 Identify time period of the VCO

As it was discussed in section 2.1, the VCO output can be expressed in the time domain by the following expression:

$$V_{VCO\_out}(t) = A_{VCO} \sin\left(2\pi \int_0^t f_c + K_{VCO} \cdot V_{in}(\tau) d\tau \right) \tag{41}$$

If a pure sinusoidal input voltage equal to $A_{in} \cdot \sin(2\pi \cdot f_{in} \cdot t)$ is assumed, the VCO output becomes:

$$V_{VCO\_out}(t) = A_{VCO} \sin\left(2\pi \cdot f_c \cdot t - \frac{K_{VCO} \cdot A_{in}}{f_{in}} \cos(2\pi \cdot f_{in} \cdot t) \right) \tag{42}$$

which can be simplified to the following expression:

$$V_{VCO\_out}(t) = A_{VCO} \sin(\omega_c t - \beta \cos(\omega_{in} t)) \tag{43}$$

where ω_c and ω_{in} represent the angular free running and angular input frequencies expressed in rad/s, respectively. The variable β is known as the modulation index, which indicates the maximum frequency deviation. It is a normalized measure of how rapidly the instantaneous VCO frequency varies around the free running frequency. Thus, the modulation index which is dimensionless, is defined by:

$$\beta = \frac{K_{VCO} \cdot A_{in}}{f_{in}} \tag{44}$$

Equation (43) shows that a cosine function is located within a sine function. In order to investigate the behavior of this equation, so-called Bessel functions of the first kind will arise. These functions are inconvenient to solve, since they represent solutions of the Bessel's differential equation. Bessel functions may be expanded as the coefficients of a theoretically infinite Fourier series. This means that these functions create sidebands in the frequency spectrum which contain energy of the frequency modulated input signal. Note that the amount and power of these sidebands strongly depends on the modulation index β. It can be said that Bessel functions itself are nonlinear, and ensures that observing the linearity of the VCO output will be difficult. The analysis will not be

discussed further, since mathematical analysis about Bessel functions are already described in books over Frequency Modulation (FM) [29].

In order to determine the time period of the VCO, zero crossings of the VCO's output signal as described by Equation (43) need to be located. In other words, the VCO's time period can be found when the continuous phase of the VCO θ_{VCO} is a multiple of π. Then, the average VCO frequency over the zero-cross interval is equal to the reciprocal of twice the time interval. To see how the VCO phase behaves over time, simple simulations have been performed which is shown in Figure 41. It is just a simulation of the VCO phase θ_{VCO} as function of time t, with fixed frequencies f_c and f_{in}. For the actual VCO phase β is equal to 50 and for the VCO phase without FM modulation β is equal to zero.

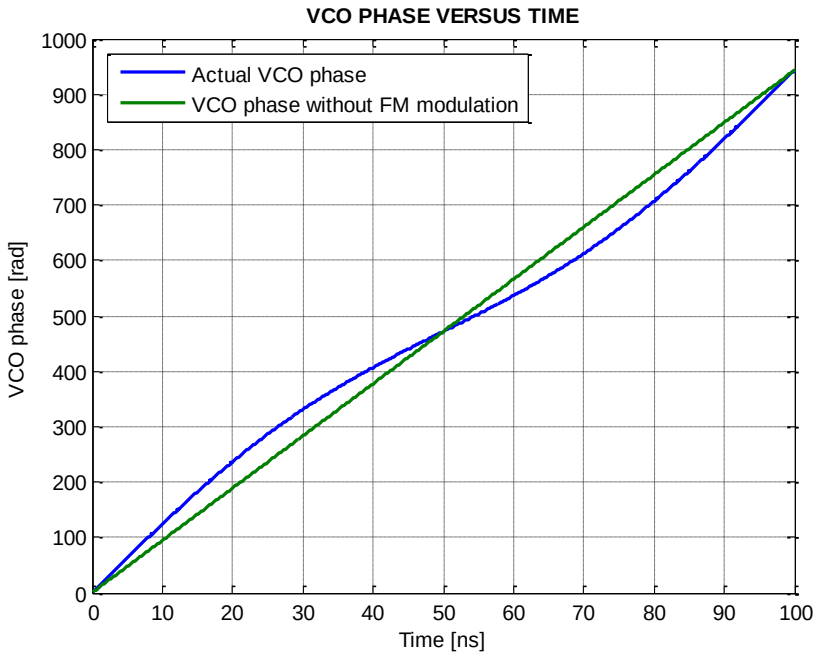

Figure 41: Simulation of the actual VCO phase as described by Equation (43) with β = 50, as well as the simulation without FM modulation (β = 0), assuming f_c = 1.5 GHz, f_{in} = 10 MHz.

As it can be seen from Figure 41, the actual VCO phase has a nonlinear increase of the phase, which results in unequally spaced zero crossings. On the other hand, the VCO without frequency modulation has a constant frequency, i.e. the free running frequency f_c, which results in a linearly growth of the VCO phase. The frequency of the actual VCO phase can be found by taking the difference in time of two zero crossings, and it will represent the frequency on the center of the time interval. If next time intervals calculate the frequency on the same manner and are interpolate linearly with each other, it will not perfectly match a sine function. This can eventually cause additional distortion in the linearity characterization the of VCO.

The VCO circuits were simulated in Cadence, by using the build-in plot function "freq". This function plots the instantaneous frequency versus time, by calculating the time between signal crossings. Thus, the output is a waveform f_{VCO} versus t, which is exactly what is needed. By different simulations it turned out that the obtained distortion does not correspond to the static distortion behavior as described for different VCOs in chapter 3. This confirms the aforementioned reasoning, that determining the VCO frequency by zero crossings will introduce additional distortion. Therefore, an

alternative approach in needed to determine the instantaneous VCO frequency. This is the subject of the next paragraph.

4.1.2 Use a frequency quantizer

As it was discussed in previous paragraph, determining the instantaneous VCO frequency by locating zero crossings for the time period is not an option. We need a way to determine the frequency which is in fact a linear representation of the input voltage. Thus, why not using a frequency quantizer? That would be a proper solution, since it quantizes the frequency to an integer which indicates the amount of VCO periods within a sampling period. In fact, it represents the actual coarse path of the proposed VCO-based ADC. Since the distortion terms coming from the nonlinear VCO will be higher than the first-order shaped quantization noise, this mechanism should be suitable to determine the dynamic distortion of the VCO. In addition, it is assumed that the frequency quantizer will not add additional distortion to its output, since it does not influences the voltage-to-frequency transfer.

For characterizing the VCOs, the state detector as described in section 2.2.5 will be used as frequency quantizer. It is a new and non-published manner of frequency quantization and is appropriate, because it generates not any distortion by itself (see section 2.2.6). An overview of the characterization method with frequency quantizer is shown in Figure 42.

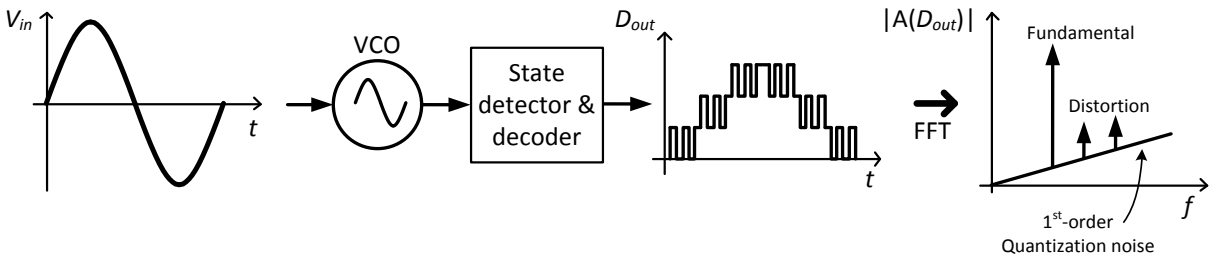

Figure 42: Dynamic characterization of the VCO by using the state detector as frequency quantizer.

The so-called “one-cold-to-binary decoder” is attached to the state detector, to obtain a binary value of the last VCO edge. By taking the differences of these values in the digital domain, a quantized version of the input signal can be obtained. The frequency dependent distortion of that signal is analyzed by taking an FFT. This FFT show besides the fundamental tone and harmonics also the first-order quantization noise. The used FFT settings correspond the settings used for the system simulations in chapter 2, i.e. 10.1 µs simulation time and 10 µs for the FFT calculations (neglecting start-up behavior of the quantizer). Since the Cadence simulation data was resampled to a fixed simulation step size of 1 ps, the number of FFT points were 10 million and resulted in a frequency bin of 100 kHz. This ensured that fundamental tones, harmonics and intermodulation distortion terms fell in a single FFT bin in the frequency domain.

4.2 Simulation results

In order to compare the proposed ring VCO with the saw-tooth oscillator on dynamic distortion, both circuits are simulated as described in previous paragraph. The circuit of the proposed ring VCO was already represented in Figure 16 and the circuit of the saw-tooth oscillator in Figure 37. Both

architectures consist of four stages. The state detector is shown in Figure 11, where it can be seen that it consists of only digital blocks, i.e. Data Flip-Flops (DFFs) and NAND gates. The state detector and decoder are for simulation purposes implemented in Cadence by ideal Verilog A building blocks. This results in significant less simulation time compared to simulations with these digital blocks implemented on transistor-level. In this section, first the single-tone simulations are discussed, after which the two-tone simulation will be treated.

4.2.1 Single-tone simulations

The proposed VCO circuit build in the 65 nm CMOS technology (Figure 16), was simulated with the Verilog implemented frequency quantizer by using the transient analysis. In order to prevent frequency aliasing in the digital domain, the VCO frequency needs to be bounded, because the state detector is used as frequency quantizer. This was elaborated in detail in section 2.2.5. The boundaries of the f_{VCO} are stated by Equation (17), and it is repeated here by Equation (45).

$$f_s \leq f_{VCO} \leq \left(2 - \frac{1}{N_{ph}}\right) f_s \tag{45}$$

For the proposed four-stage VCO, the number of VCO output signals N_{ph} is equal to 8. Since the sampling frequency f_s is fixed to 1 GHz, the VCO frequency should be bounded between 1 GHz and 1.875 GHz. This means that the free running frequency is now positioned in the center of that range at 1.4375 GHz. To achieve that desired frequency range, the DC input voltage is equal to 0.94 V (instead of 0.955 V) and the input amplitude is equal to 0.105 V (instead of 0.12 V). To preserve a small safety margin, the amplitude of the single-tone simulations was set to 0.1 V. A simulation was performed with an input frequency equal to 1 MHz, and the results were analyzed with an FFT which is shown in Figure 43.

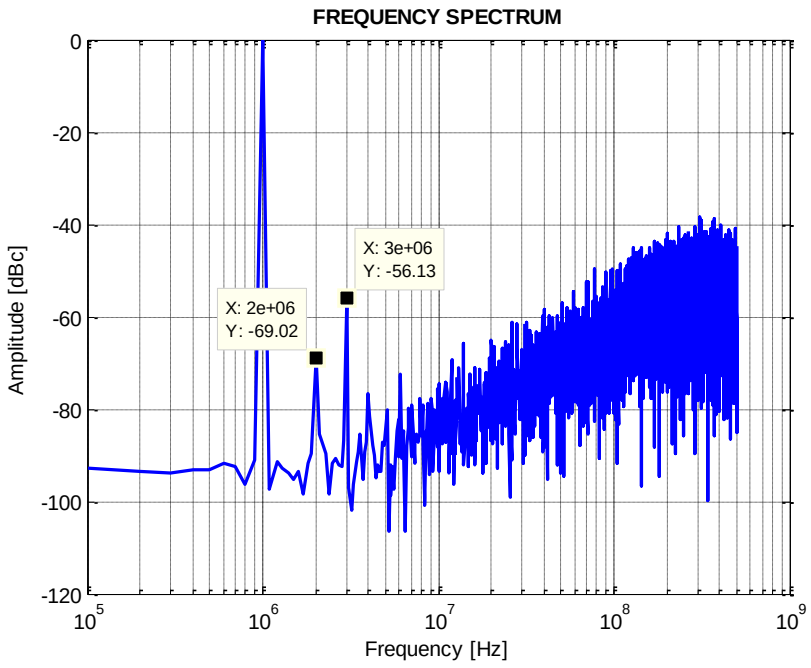

Figure 43: FFT simulation result of the proposed VCO with state detector at f_{in} = 1 MHz and f_s = 1 GHz.

Figure 43 shows clearly the presence of the fundamental tone at 1 MHz and the second and third harmonics at 2 MHz and 3 MHz, respectively. The most dominant distortion is the third-order at -56.1 dB, while the second-order distortion limits the performance at -69.0 dB. If we would compared these numbers to the static distortion numbers, the static distortion numbers need to be recalculated with an amplitude equal to 0.1 V. This results for the proposed circuit in a static distortion of HD_2 = -61.5 and HD_3 = -55.8 dB. This shows that recalculated HD_3 from the static distortion corresponds to the simulated dynamic distortion and have only a difference of 0.3 dB, while there is a difference of approximately 7.5 dB between both HD_2. That difference is most probably due to the different characterization techniques (static input versus sinusoidal input). The FFT as shown in Figure 43, shows also the expected first-order noise shaping. The simulated SINAD within the 10 MHz input bandwidth turned out to be 55.4 dB. This degradation is a consequence of the nonlinear VCO, and are mainly caused by second and third harmonics, since higher-order distortion terms fall in the quantization noise floor. It turned out that the simulated SNR within the 10 MHz input bandwidth is equal to 64.7 dB. This value is in close agreement to the ideal (linear) VCO with state detector as described in section 2.2.6 (SQNR = 64.5 dB).

The saw-tooth oscillator was characterized in the same manner as the proposed VCO. Since this oscillator consists of a four-stage architecture with single-ended outputs, the total number of output signals N_{ph} is equal to 4. This means that the quantization noise level is 6 dB higher than the previous discussed VCO (by Equation (14)). This is simply a reduction of the phase resolution by a factor 2. By using Equation (45), the frequency range for the saw-tooth oscillator is bounded between 1 GHz to 1.75 GHz. In order to achieve that frequency range, the quiescent point is set with an input current of 510 µA, while its input amplitude is equal to 150 µA. The simulation result of the saw-tooth oscillator with an input frequency of 1 MHz is shown in Figure 44.

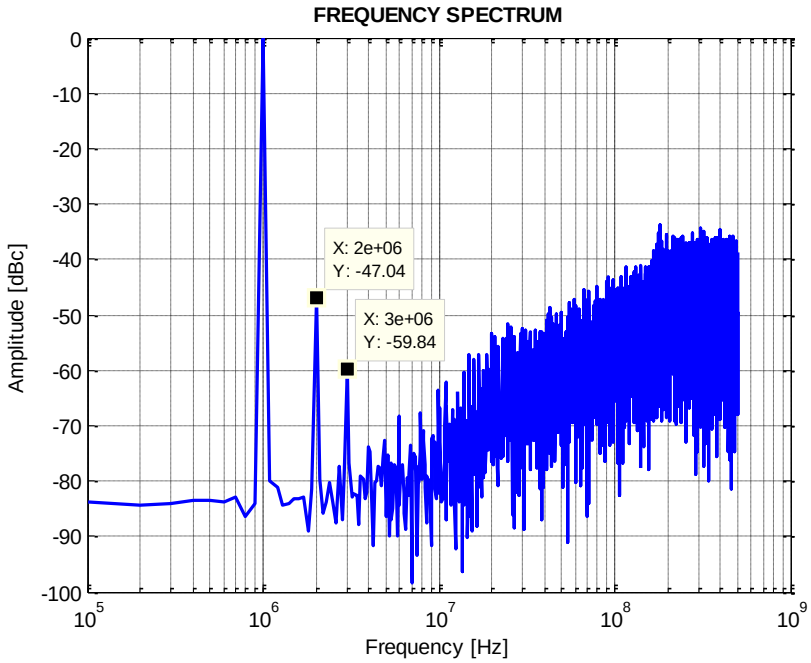

Figure 44: FFT simulation result of the saw-tooth oscillator with state detector at f_{in} = 1 MHz and f_s = 1 GHz.

As it can be seen from Figure 44, the second- and third-order distortions are equal to -47.0 and -59.8 dB, respectively. Also the expected first-order noise shaping is visible in the FFT plot. The recalculated static distortion numbers HD_2 and HD_3 with the corresponding amplitude (which was used in this simulation) turned out to be -46.9 and -59.2 dB, respectively. It shows that both HD_2 and HD_3 from the static distortion simulations are in close agreement with HD_2 and HD_3 from the dynamic distortion simulations (Figure 44). The SINAD from the FFT as shown in Figure 44 turned out to be 46.4 dB for an input bandwidth of 10 MHz. This ratio is limited due to the presence of the second and third harmonics, which arises within the input bandwidth. Theoretically, the maximum achievable SQNR for this oscillator with 750 MHz tuning range Δf_{VCO} can be determined by Equations (12) and (14), and is equal to 57.1 dB (see Equation (46)).

$$SQNR = 6.02 \cdot \log_2\left(\frac{\Delta f_{VCO} \cdot N_{ph}}{f_s}\right) - 3.41 + 30 \cdot \log_{10}(OSR) = 57.1\ dB \tag{46}$$

The nonlinearity of the saw-tooth oscillator renders almost 10 dB decrease of dynamic range assuming a 10 MHz input bandwidth. It turned out that the simulated SNR within the desired bandwidth is equal to 56.8 dB. This value corresponds nearly to the theoretically maximum value of 57.1 dB as shown by Equation (46).

4.2.2 Two-tone simulations

In order to investigate memory effects of circuits, often two-tone simulations are performed with fixed input amplitudes and at different input frequencies. Since two input frequencies are applied for this kind of simulation, intermodulation distortion terms arise in the output frequency spectrum due to the VCO nonlinearity. The second-order intermodulation distortion terms fall on the frequencies $f_{in1}+f_{in2}$ and $f_{in2}-f_{in1}$, while the important third-order distortion terms fall on the frequencies $2 \cdot f_{in1}-f_{in2}$ and $2 \cdot f_{in2}-f_{in1}$. By shifting the frequencies of both input tones, the potentially frequency dependent dynamic distortion effects of the VCO can be analyzed by observing the distortion levels of the IM terms. This is often characterized as a function of the tone spacing Δf. Note that the distortion itself is not a memory effect, but any non-constant distortion behavior at different modulation frequencies (tone spacings) can be regarded as one. In order to do a correct comparison between different simulations, the input frequencies are chosen as such that the lower IM_3 term ($2 \cdot f_{in1}-f_{in2}$) always falls on 1 MHz. This mechanism is shown in Figure 45.

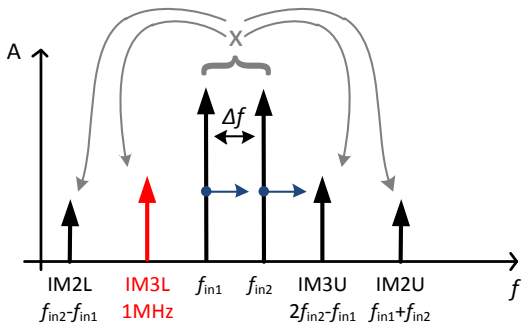

Figure 45: Dynamic characterization at two-tone simulations, where both input tones are shifted in frequency to obtain a fixed lower IM_3 (IM3L) at 1 MHz.

Figure 45 shows that two input frequencies create two second-order and two third-order IM terms in the frequency spectrum. Note that in practice more than four intermodulation terms arise, but here only the four mentioned terms are of interest. In particular, the lower IM_3 is important, because it falls for different simulations on 1 MHz. By looking at the level of that IM term, deviations as function of tone spacing can be monitored to indicate memory effects.

In case of the proposed VCO, multiple two-tone simulations were performed in Cadence. The input amplitudes of both tones were decreased by half in comparison with single-tone simulations to prevent that the VCO frequency will exceed the desired range. Furthermore the simulation settings were increased on resolution with a factor 10 as compared to the single-tone simulations. After each two-tone simulation, the data was analyzed in Matlab by using an FFT. The results of multiple simulations are for the proposed VCO shown in Figure 46.

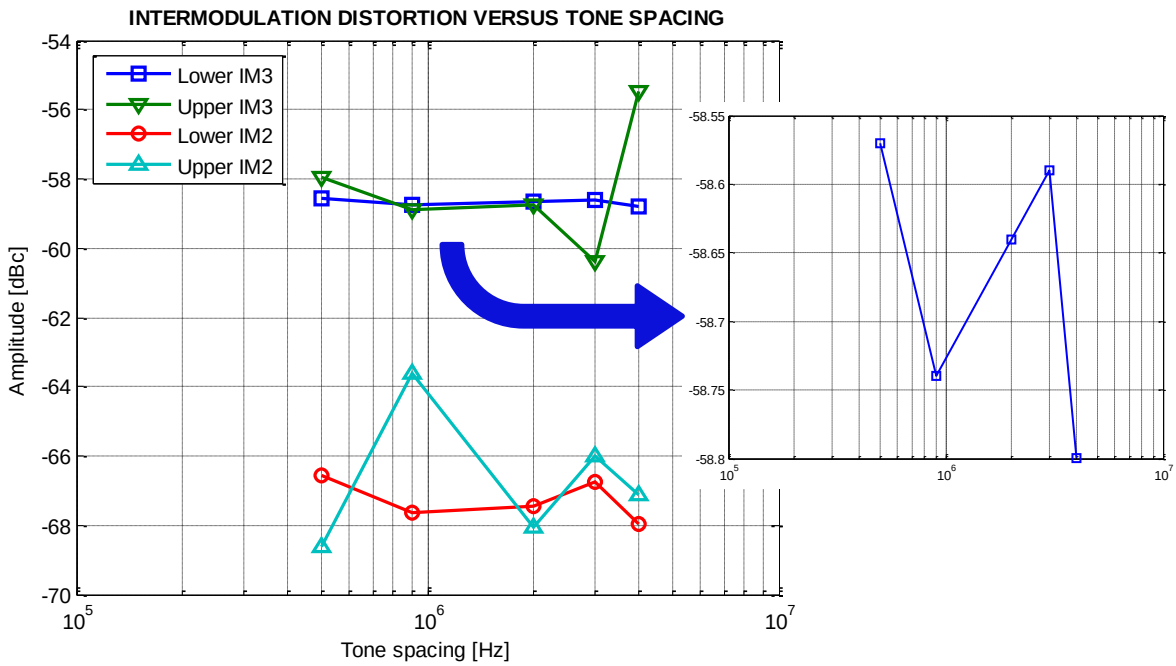

Figure 46: Two-tone simulation results of the proposed VCO, where the lower IM_3 always fell on 1 MHz. The inlet shows the amplitude of the lower IM_3 in detail.

Figure 46 shows for the proposed VCO circuit the levels of the four intermodulation distortion terms as a function of tone spacing, where the lower IM_3 term fell constantly on 1 MHz. As it can be seen this third-order term is much more flat over tone spacing compared to the other IM terms. That is a consequence of the different positions of these IM terms in frequency for different simulations. Both upper IM_2 and upper IM_3 exhibit more amplitude variation compared to both lower ones, and that could be probably caused by more frequency dependent behavior at higher frequencies. Regarding memory effects, the most important information can be found in the deviation of the lower IM_3. If memory effects are negligible, then the IM term at the fixed frequency should be constant over tone spacing. It turned out that in this case the lower IM_3 term has a maximum deviation of 0.23 dB (see inlet of Figure 46). What the effect of this deviation is, will be discussed in the next paragraph. First, the saw-tooth oscillator will be treated on dynamic distortion.

The same procedure as described for the proposed VCO will be used to characterize the dynamic distortion of the saw-tooth oscillator. The same simulation settings were used, and only the

amplitudes of both input tones are decreased by a halve to 75 µA. The results of the different two-tone simulations are shown in Figure 47.

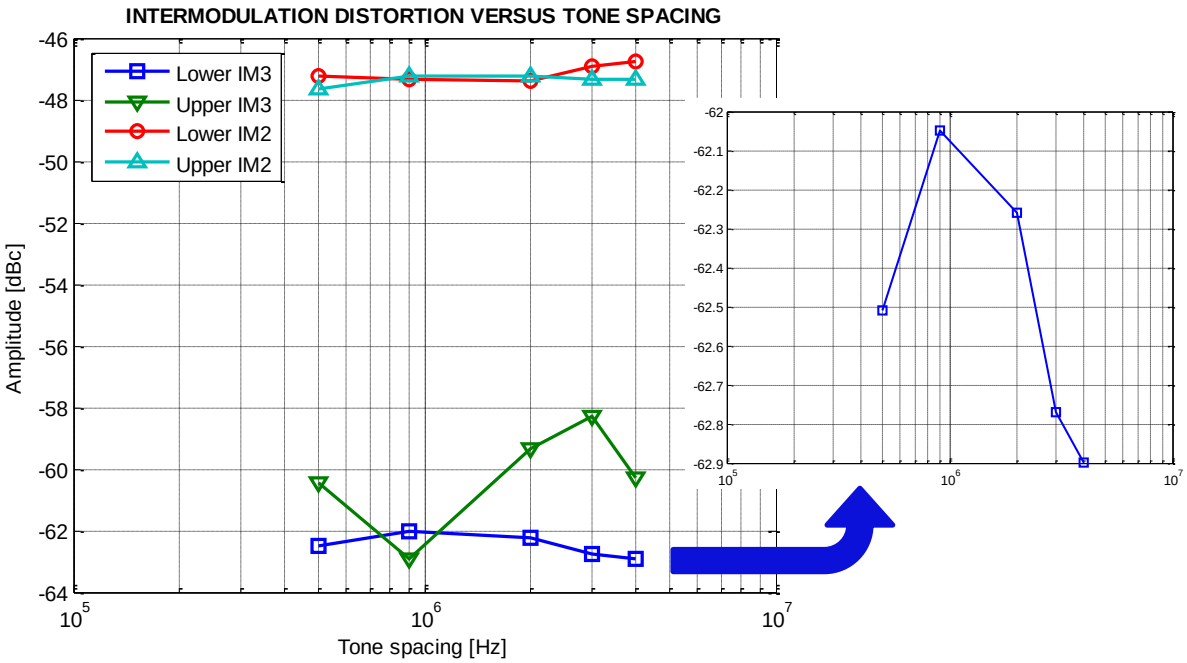

Figure 47: Two-tone simulation results of the saw-tooth oscillator, where the lower IM_3 always fell on 1 MHz. The inlet shows the amplitude of the lower IM_3 in detail.

Figure 47 shows for the saw-tooth oscillator the levels of the four intermodulation distortion terms as a function of tone spacing, where the lower IM_3 term fell constantly on 1 MHz. This figure shows that the lower IM_3 at 1 MHz is flatter than the upper IM_3, and that both IM_2 terms show small deviations of approximately 0.6 dB as function of tone spacing. It can be concluded that large part of the deviations come from the frequency dependent behavior of the oscillator, since the terms upper IM_3, lower IM_2 and upper IM_2 fell for the individual simulations at different locations in the FFT spectrum. Note that this does not necessarily mean that these IM terms have more memory effects than the lower IM_3. It turned out that this lower IM_3 has a maximum deviation of 0.85 dB (see inlet of Figure 47). This is a higher IM_3 deviation compared to proposed VCO. The consequences of this IM_3 deviation will be the subject of the next paragraph.

4.2.3 Comparison based on dynamic distortion

As it was discussed in previous paragraph, both oscillator architectures achieve a certain deviation in the lower IM_3 versus tone spacing. From the literature it is known that memory effects will degrade the linearity performance at higher frequencies. In fact, if memory effects are present, it will increase the intermodulation distortion terms at high frequencies (tone spacings). However, the lower IM_3 terms of both oscillators (see the inlets of Figure 46 and Figure 47) does not confirm this reasoning. The IM terms of both oscillators alternate randomly as function of tone spacing. It does not show an increase in the distortion, which can be dedicated to memory effects. The lower IM_3 term of the saw-tooth oscillator shows even a decrease of the distortion as function of tone spacing, which is quite strange. The simulation results as shown in previous paragraph were already obtained with a significant low simulator tolerance. The accuracy settings of the simulator were set to conservative,

and the absolute voltage and current tolerances were set to 0.1 µV and 0.1 pA, respectively. By increasing the tolerance of the simulator with a factor 10, it did not change the amount of the deviation of the IM_3 versus tone spacing of previous simulations. Decreasing the simulator tolerance even more is not possible, because the simulator is almost limited to the available computational memory and an individual simulation takes almost 18 hours to complete. Since still large deviations are visible in the aforementioned figures of the intermodulation distortion, it is probably not a result of the simulator tolerances. Most likely the deviations of the lower IM_3 term of both oscillators are a consequence of the quantization noise of the frequency quantizer. The quantization noise is a randomly behavior, and could affect the amplitude of the distortion terms.

Another way to characterize memory effects, is by observing the phase instead of the amplitude of the lower IM_3 terms [30]. If circuits have memory, the phase of the intermodulation term will increase as function of tone spacing (frequency). In order to express the phase of the IM_3 term, it is necessary to have a reference to the phase of the fundamentals. It is known that the phase of both fundamentals are at some point in time equal, since they are both generated with an initial phase of zero. Therefore, a so-called pseudo delay τ_p can be defined as shown by Equation (47) [31].

$$\tau_p = \frac{\angle F_2 - \angle F_1}{2\pi \cdot \Delta f} \tag{47}$$

In this equation $\angle F_1$ and $\angle F_2$ correspond to angle (phase) of the first (lower) and second (upper) fundamental tones obtained from an FFT of the output signal. The variable Δf represents the tone-spacing. The phases of the fundamental tones and IM_3 terms can be compensated for the pseudo delay. Firstly it is subtracting the phase shift caused by the pseudo delay, and secondly subtracting the remaining phase of the two fundamental tones. Note that after these subtractions, the phase of the two fundamental tones will be zero. This reasoning gives the phase of the lower IM_3 (IM3L) relative to the fundamental tones as shown by Equation (48) [31].

$$\varphi_{IM3L} = \angle F_{IM3L} + 3\pi \cdot \Delta f \cdot \tau_p - \left(\angle F_1 + \pi \cdot \Delta f \cdot \tau_p\right) \tag{48}$$

The variable $\angle F_{IM3}$ represents the angle of the lower IM_3 term obtained from an FFT. Performing these phase analysis to the aforementioned two-tone simulations of the proposed VCO and the saw-tooth oscillator, will obtain the relative phase of the lower IM_3 term as shown in Figure 48.

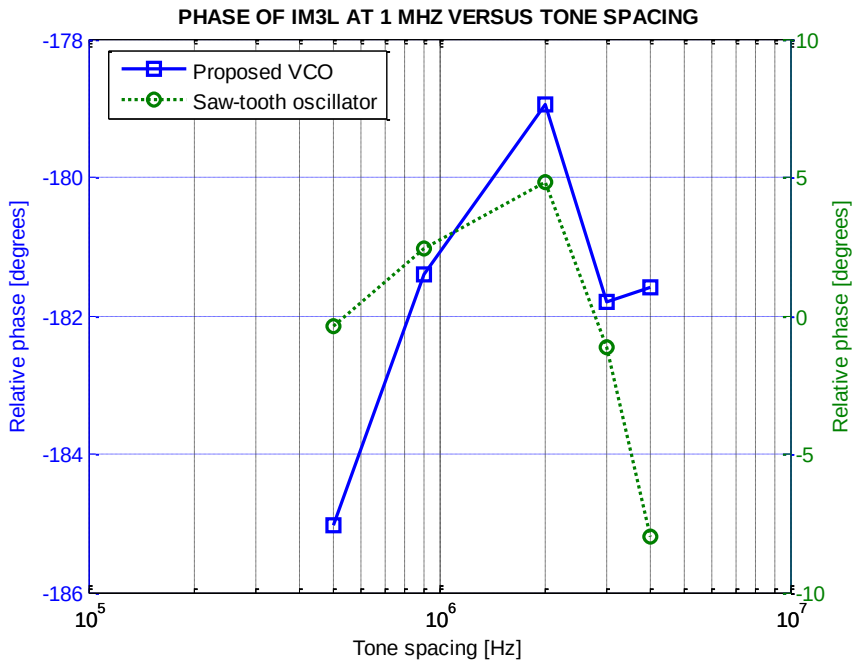

Figure 48: The relative phase of the lower IM_3 term, in case of the proposed VCO and the saw-tooth oscillator, and obtained by the FFT of two-tone simulations.

As it can be seen from Figure 48, the proposed VCO achieves a maximum phase deviation of 6°, while the saw-tooth oscillator achieves a maximum phase deviation of 13°. Both phases show a rather randomly behavior, which cannot easily be related to memory effects. These effects are often localized by an increase of the phase as function tone spacing [30]. It seems that also the deviation of the phase is a consequence of quantization noise, similar to the amplitude deviations as shown in Figure 46 and Figure 47.

It can be concluded that memory effects are rather difficult to determine, because the VCO frequency cannot be observed as a continuous function over time. Since calibration is needed to increase the performance of VCOs, it is necessary that the distortion terms, like IM_3, can be predicted accurately. If an extra tone is added to the output signal in the frequency domain, and that tone has the same frequency and amplitude of an IM_3 term but opposite phase, that IM_3 term will completely vanish at the output. However, this will not be the case in practice, since mismatch occur in the phase and amplitude of the IM_3 term. The amount of amplitude mismatch and phase mismatch is a direct measure of the obtained suppression by calibration. The obtained suppression for different amplitude and phase mismatch is shown in Figure 49 [32].

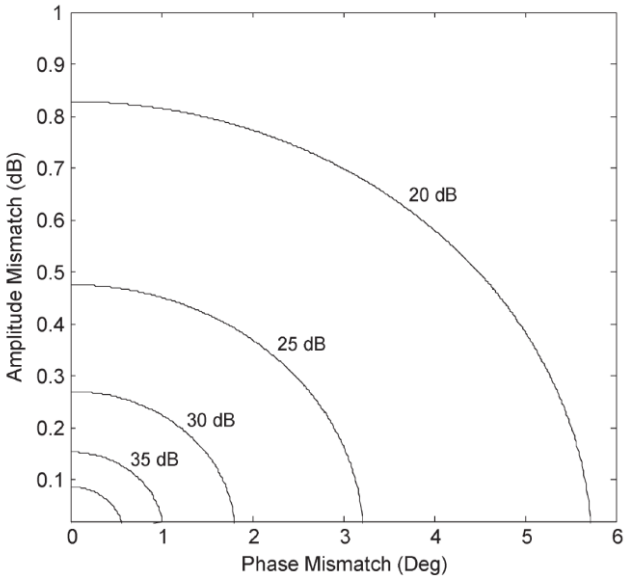

Figure 49: Amplitude and phase mismatch for different amounts of suppression, source: [32].

From Figure 49 it can be seen that 40 dB performance can be gained if the amplitude mismatch is smaller than 0.1 dB or the phase mismatch smaller than 0.6°. Thus, if both amplitude and phase mismatch are present, the requirements are even stronger. This figure gives an indication how low the memory effects should be if calibration will be applied. Since the aforementioned amplitude and phase deviations of both oscillators are not dedicated to memory effects, it does not tell anything about the obtained suppression of the distortion terms.

4.3 Alternative approach to determine memory effects

Since previous performed simulations did not indicate memory effects of VCOs, an alternative approach is needed to determine the frequency dependent distortion. The drawback of the previous used characterization method is the VCO frequency cannot be obtained as a continuous function over time. Therefore, another approach is needed without observing the VCO frequency. Since a ring VCO is in fact a delay cell, the delay per stage could be observed to investigate memory effects. In case of a four-stage ring VCO with frequency tuning by V_{DD}, a possible alternative approach is presented in Figure 50.

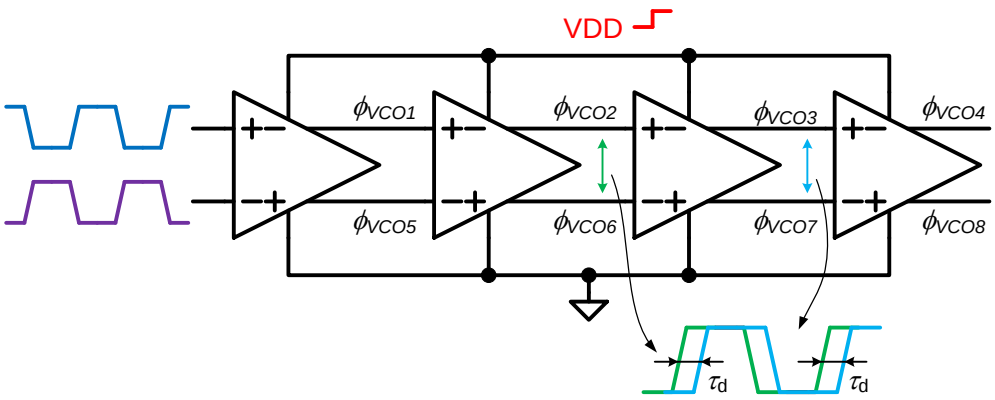

Figure 50: Four-stage open-loop ring VCO with some signal representations to investigate memory effects.

Figure 50 shows that the delay τ_d between two differential VCO output signals is represented in an open-loop configuration with two pulsed input signals (one in the opposite phase than the other) at the first stage. The input and output signals of the third stage are chosen to be observed, since the input and the output of that stage are loaded in a ring configuration. Note that the first two stages also adapt the ideal pulsed input signals to a more practical shape, ensuring that the signals have the same shape as in a closed-loop configuration. If the ring VCO will be supplied with a certain fixed voltage V_{DD}, the obtained delay will be constant over time. In order to investigate memory effects, it is necessary to observe the delay differences versus time when the control voltage (V_{DD}) makes a small voltage step. These differences indicate how fast the delay cell adapt their delay as a response of the voltage step. Thus, by performing multiple simulations with V_{DD} voltages at the extremes of the desired frequency range, will result in delay differences at different V_{DD} levels. For example, a V_{DD} voltage step to achieve a delay from 125 ps to 110 ps (1 GHz to 1.1 GHz) could be compared with a V_{DD} voltage step to achieve a delay from 65 ps to 62.5 ps (1.9 GHz to 2 GHz). Since the delay differences may depend on the input signal (V_{DD}), they can probably indicate memory effects.

The described method will give delay differences at different V_{DD} voltages in case of the four-stage differential ring VCO. However, to make a comparison with the saw-tooth oscillator, the same procedure is required. This will be a problem in case of the saw-tooth oscillator, because it consists of four single-ended stages that are not delay cells. In fact, the saw-tooth oscillator is designed as such that the behavior of a current saw-tooth stage does not only depends on previous stage but also on the second last stage. This will increase the complexity of investigating memory effects on the described approach, and due to time limits that was not further investigated.

5 Conclusions

Analog-to-Digital Converters (ADCs) which are based on a Voltage-Controlled Oscillator (VCO), are limited in performance by its VCO nonlinearity. This MSc project focused on the achievable performance, firstly on system high-level perspective and secondly on circuit level perspective.

High-level system simulations with ideal building blocks have shown that a VCO-based ADC generates no distortion. However, by adding 1% nonlinearity to the voltage-to-frequency gain K_{VCO} of the ideal ADC, the performance was limited to a SINAD equal to 44 dB (HD_2 dominant).

The circuit level analysis was subdivided into static distortion analysis to investigate the distortions originating from the nonlinear VCO gain, and into dynamic distortion analysis to investigate the feasibility of digital calibration of the nonlinear VCO gain. Small- and large-signal analyses of the ring VCO showed that the VCO nonlinearity is due to the nonlinear V-I characteristics of the MOS transistors.

The ring VCO achieved less static distortion (more than 1.4 dB) than the discussed alternative VCO circuits with the same VCO frequency range. However, the ring VCO needs an input voltage buffer, which is not easy to design with the requirement that the output resistance should have a value of approximately 12 Ω. The saw-tooth oscillator is an appropriate alternative, since the static distortion is only less than 1.6 dB compared to the ring VCO and it does not need an input buffer.

In order to cancel out the nonlinearity of the VCO by using digital calibration, the frequency dependent dynamic distortion (memory effects) should be lower than 0.1 dB to be able to gain 40 dB in performance. The dynamic distortion cannot be determined by measuring the time of each VCO period to obtain an instantaneous VCO frequency, because complex Bessel functions arise in the time domain due to frequency modulation of the input signal. When the number of VCO periods per sampling clock were observed (frequency quantization), the dynamic distortion results with a single-tone input of the ring VCO and the saw-tooth oscillator (within 10 MHz input bandwidth) were not significant different from the static distortion results.

In case of two-tone simulations it turned out that the variations of the amplitude (and phase) of the lower IM_3 term versus tone spacings were substantial higher than 0.1 dB (and 0.6^o), and cannot be related to memory effects. Since the VCO frequency cannot be observed as a continuous function over time, it is difficult to determine memory effects of VCOs by means of an FFT, and due to time limits that was not further investigated.

In conclusion, the ring VCO achieves higher linearity performance than the saw-tooth oscillator (based on static distortion analysis), and it cannot be concluded which oscillator has the lowest dynamic distortion (memory effects).

6 Recommendations

- To be sure that frequency dependent distortion will not degrade the gained performance by calibration significantly, memory effects of VCOs may still be investigated. An alternative approach was already proposed in section 4.3, and could be validated with circuit simulations on the ring VCO. In case of the saw-tooth oscillator, this approach may not be valid and could be verified in correctness, since the saw-tooth oscillator is completely different from the ring VCO.
- In chapter 3 it was shown that VCOs achieve high linearity results if the second and third derivatives of the VCO linearity gain is located with the quiescent point around zero. Thus for the final VCO-based ADC design, the transistors of the VCO could be dimensioned as such that the desired tuning range is achieved while the second and/or third derivatives of the VCO linearity gain fall with the quiescent point around zero.
- Since this project only focused on non-ideal effects from circuit behavior such as noise and nonlinearity, the non-ideal effects from IC manufacturing are not well-known and could be investigated. Temperature dependencies and mismatch of the transistors will influence the circuit behavior of the VCO, and may degrade the linearity performance.
- To complete the new VCO-based ADC design, several blocks need still to be designed on circuit level. The one-cold-to-binary decoder in the course path does not need much effort, since it only consists of digital logic. However, the switch bank and the fine ADC in the fine path of the new ADC design have still to be designed. The switch bank could be critical, since capacitor voltages of the ramp generator need to pass through to the fine ADC, without losing the accuracy of these voltages. On the other hand, the implementation of the fine ADC should not be too difficult, because an already designed flash ADC would be sufficient. The ADC reported by Veldhorst et al. [33] achieves state-of-the-art performance and the design is already available within the ICD group of the University of Twente.

7 References

[1] M. Pelgrom, Analog-to-Digital Conversion, Springer, 2010.

[2] ITRS, "International Technology Roadmap for Semiconductors," 2011. [Online]. Available: http://www.itrs.net.

[3] M. Straayer and M. Perrott, "Chapter 9 Oversampled ADC Using VCO-based Quantizers," in *Multi-Mode/Multi-Band RF Transceivers for Wireless Communications*, John Wiley & Sons, 2011, pp. 247-276.

[4] S. Yoder, M. Ismail and W. Khalil, VCO-Based Quantizers Using Frequency-to-Digital and Time-to-Digital, Springer, 2011.

[5] J. Hurrell, D. Pridmore-Brown and A. Silver, "Analog-to-Digital Conversion with Unlatched SQUID's," *IEEE Transactions on Electron Devices,* vol. 27, no. 10, pp. 1887-1896, 1980.

[6] M. Høvin, A. Olsen, T. S. Lande and C. Toumazou, "Delta-Sigma Modulators Using Frequency-Modulated Intermediate Values," *IEEE Journal of Solid-State Circuits,* vol. 32, no. 1, pp. 13-22, 1997.

[7] J. Kim and S. Cho, "A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage-Controlled Oscillator," *IEEE ISCAS,* pp. 3934-3937, 2006.

[8] Y.-G. Yoon, J. Kim, T.-K. Jang and S. Cho, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," *IEEE Transactions on Circuits and Systems - I,* vol. 55, no. 11, pp. 3571-3581, 2008.

[9] A. Iwata, N. Sakimura, M. Nagata and T. Morie, "The Architecture of Delta Sigma Analog-to-Digital Converters Using a Voltage-Controlled Oscillator as a Multibit Quantizer," *IEEE Transactions on Circuits ans Systems II,* vol. 46, no. 7, pp. 941-945, 1999.

[10] R. Naiknaware, H. Tang and T. Fiez, "Time-Referenced Single-Path Multi-Bit ΣΔ ADC using a VCO-Based Quantizer," *IEEE Transactions on Circuits and Systems II,* vol. 47, no. 7, pp. 596-602, 2000.

[11] M. Straayer and M. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time ΣΔ ADC With a 5-bit, 950-MS/s VCO-Based Quantizer," *IEEE Journal of Solid-State Circuits,* vol. 43, no. 4, pp. 805-814, 2008.

[12] J. Kim, T.-K. Jang, Y.-G. Yoon and S. Cho, "Analysis and Design of Voltage-Controlled Oscillators Based Analog-to-Digital Converter," *IEEE Transactions on Circuits and Systems I,* vol. 57, no. 1, pp. 18-30, 2010.

[13] H. Venkatram, "Least Mean Square calibration method for VCO non-linearity," *IEEE International Conference on Microelectronics,* vol. 22, no. 12, pp. 1-4, 2010.

[14] J. Daniels, W. Dehaene and M. Steyaert, "All-Digital Differential VCO-based A/D Conversion," *IEEE Circuits and Systems,* no. 5, pp. 1085-1088, 2010.

[15] T.-K. Jang, J. Kim, G.-Y. Yoon and S. Cho, "A Highly-Digital VCO-based Analog-to-Digital Converter Using Phase Interpolator and Digital Calibration," *IEEE TRansactions on VLSI Systems,* vol. 20, no. 8, pp. 1368-1372, 2012.

[16] M. Negreiros, L. Carro and G. Cassel, "All Digital ADC with Linearity Correction and Temperature Compensation," *IEEE Instrumentation and Measurement Technology Conference,* no. 5, pp. 147-152, 2010.

[17] L. Hernández, S. Patón and E. Prefasi, "VCO-based sigma delta modulator with PWM precoding," *IEEE Electronic Letters,* vol. 47, no. 10, pp. 1-2, 2011.

[18] G. Taylor and I. Galton, "A Mostley-Digital Variable-Rate Continuous-Time Delta-Sigma Modulator ADC," *IEEE Journal of Solid-State Circuits,* vol. 45, no. 12, pp. 2634-2646, 2010.

[19] G. Taylor and I. Galton, "A Reconfigurable Mostly-Digital ΣΔ ADC with a Worst-Case FOM of 160dB," *IEEE Symposium of VLSI Circuits Digest of Technical Papers,* no. 12, pp. 166-167, 2012.

[20] B. Behroozpour, "VCO Based ADC Exploiting Linear Phase Genration Techniques," MSc. Thesis, University of Twente, Enschede, 2012.

[21] W. Sansen, "Distortion in elementary transistor circuits, Chapter 18," in *Analog design essentials*, Dordrecht, Springer, 2006, p. 519.

[22] S. Gierkink, "Control Linearity and Jitter of Relaxation Oscillators," Phd thesis, Enschede, 1999.

[23] C. Li and J. Lin, "A 1–9 GHz Linear-Wide-Tuning-Range Quadrature Ring Oscillator in 130 nm CMOS for Non-Contact Vital Sign Radar Application," *IEEE Microwave and Wireless components letters,* vol. 20, no. 1, pp. 34-36, 2010.

[24] B. Fahs, M. Ali-Ahmed and P. Gamand, "A Two-Stage Ring Oscillator in 0.13-um CM OS for UWB Impulse Radio," *IEEE Transactions on Mircrowave Theory and Techniques,* vol. 57, no. 5, pp. 1074-1082, 2009.

[25] Y. Eken and J. Uyemura, "A 5.9-GHz Voltage-Controlled Ring Oscillator in 0.18-um CMOS," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 1, pp. 230-233, 2004.

[26] W. Yan and H. Luong, "A 900-MHz CMOS Low-Phase-Niose Voltage-Controlled Ring Oscillator," *IEEE Transactions on Circuits and Systems II,* vol. 48, no. 2, pp. 216-221, 2001.

[27] S. Blaakmeer, "Design of RF-CMOS Ring Oscillator," MSc. Thesis, University of Twente, Enschede, 2001.

[28] N. v. Helleputte and G. Gielen, "A 70 pJ/Pulse Analog Front-End in 130 nm CMOS for UWB

Impulse Radio Receivers," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 7, pp. 1862-1871, 2009.

[29] A. Carlson, Communication Systems, An Introduction to Signals and Noise in Electrical Communication, New York: Mcgraw-Hill Inc, 1986.

[30] J. Vuolevi, T. Rahkonen and J. Manninen, "Measurement Technique for Characterizing Memory Effects in RF Power Amplifiers," *IEEE Transaction on Microwave Theory and Techniques,* vol. 49, no. 8, pp. 1383-1389, 2001.

[31] D. Wisell, B. Rudlund and D. Rönnow, "Characterization of Memory Effects in Power Amplifiers Using Digital Two-Tone Measurements," *IEEE Transactions on Instrumentation and Measurement,* vol. 56, no. 6, pp. 2757-2766, 2007.

[32] N. Pothecary, Feedforward Linear Power Amplifiers, London, U.K.: Artech House, 1999.

[33] P. Veldhorst, G. Goksun, A.-J. Annema and B. Nauta, "A 0.45pJ/conv-step 1.2Gs/s 6b full-Nyquist non-calibrating flash ADC in 45nm CMOS and its scaling behavior," *IEEE ESSCIRC,* pp. 464-467, 2009.