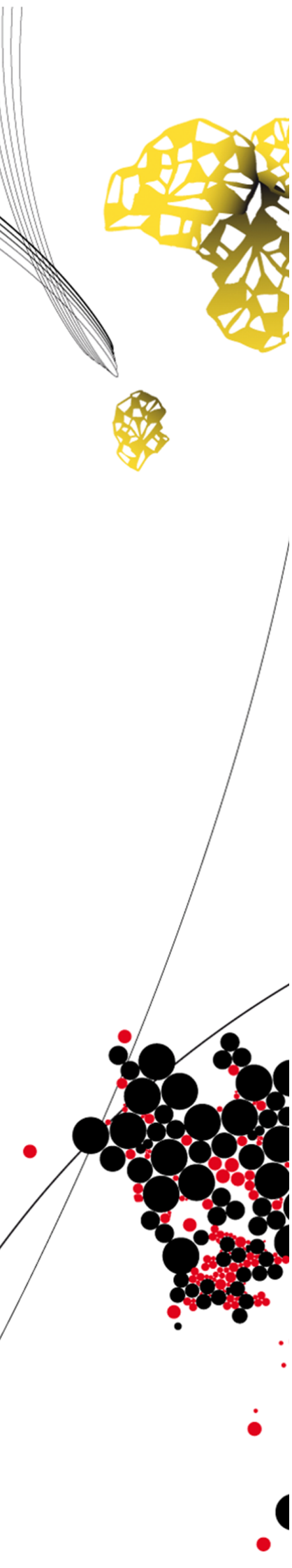

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Design of an Energy Efficient 12-bit 100MS/s SAR ADC in 22nm FD-SOI

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Abstract

Current state-of-the-art high-frequency SAR ADCs challenge the technological limits of CMOS. The focus of this thesis is on the design of analog sub-circuits of such a state-of-the-art SAR ADC in 22nm FD-SOI. The target SAR ADC has a 12-bit resolution at a sample frequency of 100Ms/s. The parasitic effects in a charge-redistributing digital-to-analog converter are modelled, and a custom unit-cell capacitor is made that minimizes the effect of parasitics. A fully differential 12-bit DAC with 4-bit thermometer code is made, consuming $969fJ$ per conversion. A dynamic bias comparator is implemented. Simulations of the comparator show an average energy consumption of $58fJ$ per comparison and $145\mu V$ input-referred noise. A track and hold circuit, that utilizes the absence of latch-up and smaller parasitic capacitance in the FD-SOI technology, is implemented with a SINAD of 74.35dB and a very low energy consumption of $15fJ$ per conversion. The energy consumption for the full 12-bit SAR ADC is estimated to be $2.3pJ$ per conversion.

Abbreviations

ADC	Analog-to-Digital Converter
BOX	Buried Oxide
CMOS	Complementary Metal-Oxide-Semiconductors
DAC	Digital-to-Analog Converter
DFT	Direct Fourier Transform
DNL	Differential nonlinearity
ENOB	Effective Number Of Bits
FD-SOI	Fully Depleted Silicon On Insulator
FOM	Figure Of Merit
HVT	High Threshold
INL	Integral nonlinearity
NBW	Noise Bandwidth
PMOS	P-channel Metal-Oxide-Semiconductor
SAR	Successive Approximation Register
SLVT	Super Low Threshold

Contents

Chapter 1

Introduction

Analog signals are continuous in both time and amplitude. To use analog signals in digital devices the amplitude is limited to a finite number of levels, and is converted to a time discrete signal by sampling the analog signal at a fixed interval. The conversion of an analog signal to a digital signal is done by an analog-to-digital converter (ADC). Figure 1.1 shows a graphical representation of the analog-to-digital conversion.

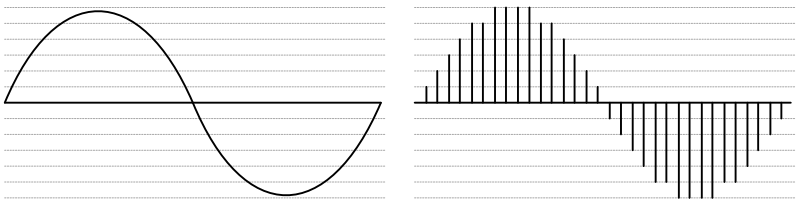

Figure 1.1: Graphical representation of analog-to-digital conversion.

1.1 Analog-to-digital converters

The continuous increase in digital processing speed and accuracy, triggers the demand for more accurate high-speed ADCs. Research on ADCs is therefore focused on the three main requirements: speed, resolution and energy efficiency. Different converter topologies are subject of research and target to increase the speed and accuracy while decreasing the energy consumption. This research focusses on successive approximation register (SAR) ADCs.

1.2 SAR ADC

A SAR ADC, as shown in figure 1.2 is a recursive system wich comprises of a comparator and a digital-to-analog converter (DAC). The input signal V_{in} is sampled by the track-and-hold circuit. The sampled value of V_{in}, at the positive input of the comparator, is compared to the initial voltage generated by the DAC. The comparison result is then used to modify the first bit in the successive approximation register and with that the DAC output. This comparison and modification is repeated until the last bit is computed.

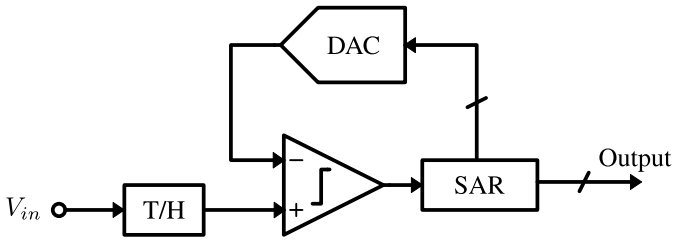

Figure 1.2: Block diagram of a single-ended SAR ADC.

1.3 Track-and-hold circuit

The track-and-hold circuit can be seen as a sampling switch, as shown in figure 1.3, which samples the input signal V_{in} on the capacitor C_{hold}. To maintain a high effective number of bits (ENOB), the switch should not add significant noise or distortion to the system. Non-linear on-resistance, parasitic capacitance and incomplete settling, due to insufficient settling time for the RC circuit, reduces the ENOB.

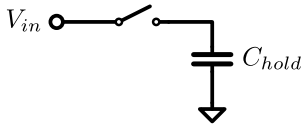

Figure 1.3: Sampling switch.

1.4 Comparator

The comparator is at the core of the SAR ADC. The comparator has to differentiate between its two inputs. Noise effects the accuracy of this decisions and is therefore the main concern in the comparator. A two stage dynamic comparator structure [1] [2] is used in this SAR ADC. A dynamic comparator has two stages, a pre-amplifier and a regenerative latch. The pre-amplifier is a low noise amplifier that is used to amplify the input. After sufficient amplification the regenerative latch secures the comparator output. Energy efficiency is important because the comparator is often one of the main contributors to the total energy consumption of a SAR ADC.

1.5 Digital-to-analog converter

The DAC is used to generate an analog reference signal for the comparator as shown in figure 1.2. The input of the DAC is a digital word $DN \cdots 1$ and is converted to an analog signal as depicted in 1.4. DACs in SAR ADCs are mostly binary-scaled capacitor arrays. Capacitive charge-redistribution DACs, as depicted in figure 1.5, generate an analog voltage V_{out} by redistributing

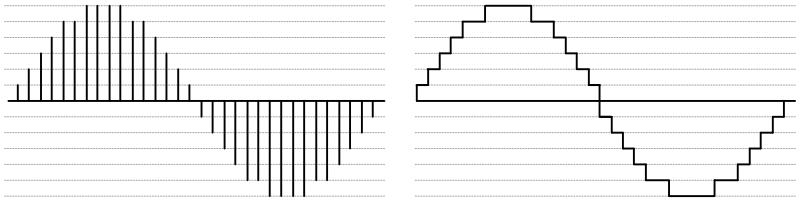

Figure 1.4: Graphical representation of digital-to-analog conversion.

charge according to equation (1.1). The nonlinearity of the DAC is one of the aspects that defines the ENOB.

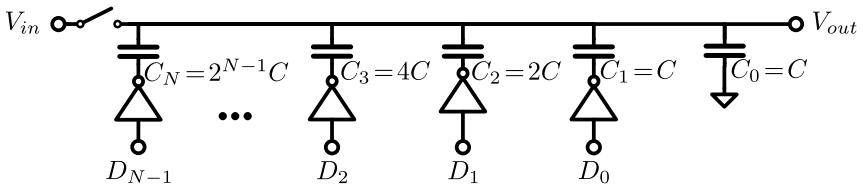

Figure 1.5: Capacitive charge-redistribution DAC.

$$V_{out} = V_{in} + V_{ref} \frac{\sum_{i=1}^{N} \overline{D_{i-1}} \cdot C_i}{C_{total}} \tag{1.1}$$

1.6 22nm FD-SOI technology

The SAR ADC will be implemented in 22nm Fully Depleted Silicon On Insulator(FD-SOI) CMOS technology. Unlike conventional bulk CMOS, FD-SOI uses a buried-oxide(BOX) layer as depicted in figure 1.6. This BOX-layer separates the channel from the silicon substrate. On top of this BOX-layer a very thin silicon film is placed to make the channel.

In an attempt to reduce the energy consumption of bulk CMOS circuits, the supply voltage is lowered. However this decreases the maximal overdrive voltage of the transistors and therefore the switching speed and current driving capability. To maintain performance at lower supply voltages the threshold voltage is lowered by doping the channel [3]. Because the channel in FD-SOI is very thin, there is often no doping required or the channel is only lightly doped.

FD-SOI offers a lot of advantages for digital circuits like a sharp subthreshold slope, high current drive, high transconductance, less parasitic capacitance and absence of latch-up. FD-SOI is not only beneficial for digital circuit design, but offers nice properties for analog applications as well [4]. FD-SOI has a higher transconductance to drain current ratio compared to bulk CMOS, resulting in a higher gain. The smaller parasitic capacitances result in less power consumption and higher speed.

Similar to body bias in CMOS[3], FD-SOI has this ability, but can further exploit this because the BOX-layer prevents forward diode conduction,

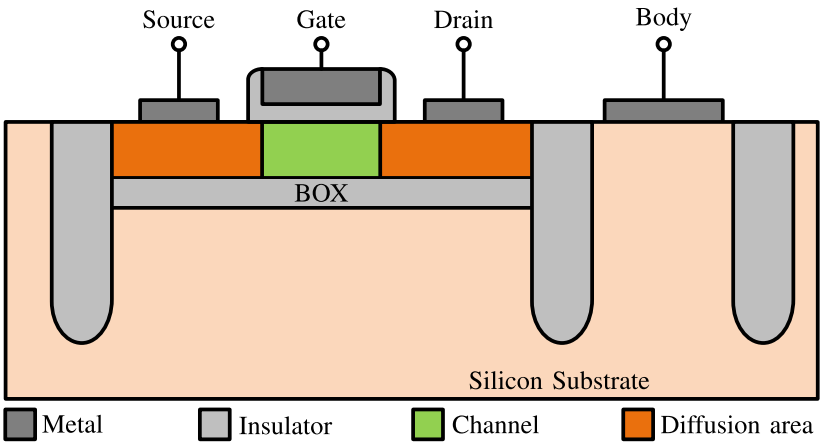

Figure 1.6: FD-SOI MOSFET structure.

and therefore voltage range for the body bias is larger, allowing for a better tunability of the threshold voltage.

Chapter 2

System requirements and block specifications

The target specifications are to challenge the technological limits of 22nm FD-SOI for state-of-the-art performance. An example of a state-of-the-art high-frequency SAR ADC is the 100Ms/s 12-bit SAR-assisted digital slope ADC[5]. The design specifications for this high-frequency SAR ADC are listed in table 2.1. The SAR ADC uses a 0.8V power supply, a differential architecture allows an input swing of $1.4V_{pp}$. The target effective resolution(ENOB) is > 10.5 bits.

Table 2.1: Design specifications.

Specifications	
Process type	GF 22nm FD-SOI
Supply voltage	0.8V
Input voltage swing	$1.4V_{pp}$
Resolution	12 bits
Effective resolution	>10.5 bits
Speed	100Ms/s

2.1 Noise

The noise of a SAR ADC is mainly depends on three noise sources. First of all, the quantization noise. Quantizing a signal introduces an error of maximal $\frac{V_{LSB}}{2}$. The quantization noise power $\overline{v_{n,q}^2}$ is given by equation (2.1).

$$\overline{v_{n,q}^2} = \frac{1}{V_{LSB}} \int_{-\frac{1}{2}V_{LSB}}^{\frac{1}{2}V_{LSB}} x^2 \, \mathrm{d}x = \frac{V_{LSB}^2}{12} \tag{2.1}$$

Sampling noise is another noise source in a SAR ADC. Sampling noise, also called kTC noise, is the thermal noise on the sampling capacitor after sampling. The sampling noise power, $\overline{v_{n,kTC}^2}$, is given by:

$$\overline{v_{n,kTC}^2} = \frac{kT}{C}$$

The comparator is the third contributor to the total ADC noise. The total noise power, $\overline{v_{n,total}^2}$, is given by equation (2.2). Note that because the ADC is a differential structure, and uses two sampled inputs, the sampling noise power is doubled.

$$\overline{v_{n,total}^2} = \overline{v_{n,q}^2} + 2 \cdot \overline{v_{n,kTC}^2} + \overline{v_{n,comp}^2} \tag{2.2}$$

For the sampling noise power, $2 \cdot \overline{v_{n,kTC}^2}$, not to be dominant it needs to be smaller than the quantization noise power $\overline{v_{n,q}^2}$.

$$\overline{v_{n,q}^2} > 2 \cdot \overline{v_{n,kTC}^2} \Rightarrow \frac{V_{LSB}^2}{12} > \frac{2kT}{C} \Rightarrow C_{tot} > \frac{24 \cdot kT}{V_{LSB}^2}$$

For $V_{LSB} = \frac{1.4V_{pp}}{2^N}$, k being the Boltzmann constant and $T = 300K$, The minimum for C_{tot} is:

$$C_{tot} > 850fF \tag{2.3}$$

The capacitive DAC uses 2^N unit capacitors so the minimum capacitance of an unit capacitor, C_0, is given by:

$$C_0 > \frac{C_{tot}}{2^N} = 208aF$$

By taking a larger capacitor than the minimum required, the system will not be limited by the sampling noise, and the DAC design becomes mismatch limited as described in chapter 3. For this SAR ADC design, the sampling capacitors C_{tot} will 1.5 times the minimum of equation (2.3), resulting in a 1.2pF capacitor. This gives an unit capacitor, C_0 of $293aF$.

2.2 Timing

The sampling frequency is 100MS/s as specified in table 2.1. The sampling period, T_s, is 10ns. To give the track and hold circuit sufficient time for precise settling and a still allow a practical value for the switch resistance, described in chapter 5, the track an hold is given 20% of T_s. For a 12-bit ADC, 12 comparisons are required. The DAC updates 11 times, and once during the reset phase. By taking twice the time budget of a comparison and DAC update for reset, the remaining 8ns are divided by 13, resulting approximately 600ps for comparison time and DAC update. The DAC is assigned 5 times more than the comparator, resulting in the timing budget depicted in figure 2.1.

The comparator gives a ready signal after its comparison is finished and

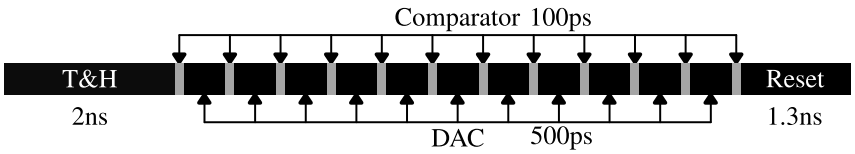

Figure 2.1: Timing of a conversion cycle.

triggers the delay line of the DAC. This asynchronous comparator timing allows the comparator to compensate slow comparisons with fast comparisons. The ADC will work at 100MS/s as long as the total time of all the comparisons combined does not exceed the given total 1.2ns allocated to the comparator.

Chapter 3

Digital-to-analog converter

The DAC capacitor array is also the sampling capacitor, C_{hold}, of the track and hold circuit as illustrated in figures 1.3 and 3.1. The output of the comparator is used to update the DAC state. With the conventional SAR algorithm, V_{in}^{+} and V_{in}^{-} converge to common-mode in N cycles, where N is the ADC resolution in bits. Fundamental aspects for the DAC accuracy are discussed in this chapter and the design choices based on these aspects are clarified.

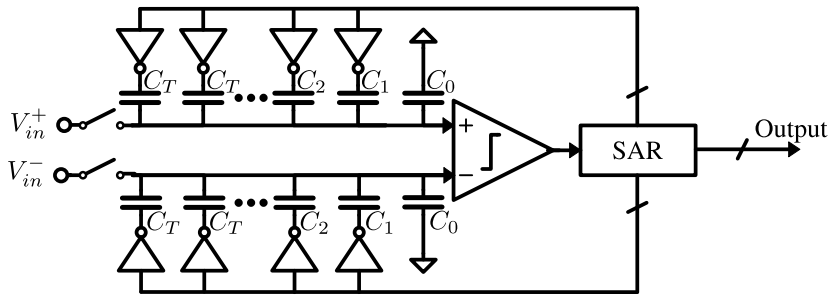

Figure 3.1: Block diagram of a differential partially thermometer-coded SAR ADC.

3.1 Noise

The total capacitance of the DAC, C_{tot}, is the sampling capacitor of the track and hold circuit, C_{hold}. The minimum size for C_{tot} is derived in section 2.1. C_{tot} is sized 1.5 times larger than the calculated minimum to, $1.2pF$, therefore the DAC can only limit the ADC accuracy by its mismatch. The total unit cell capacitance C_0 is $293aF$.

3.2 Mismatch

Nonlinearity of a digital-to-analog converter is expressed in differential nonlinearity(DNL), and integral nonlinearity(INL). DNL in a DAC is defined as the output voltage difference between two consecutive digital input codes minus

the ideal voltage difference. INL is defined as the difference between the actual analog output and the ideal output for a specific digital input code. Both DNL and INL are normalized to V_{LSB}.

$$DNL(k) = \frac{V(k+1) - V(k)}{V_{LSB}} - 1, \quad \{k \in \mathbb{Z} \,|\, 0 \leq k \leq 2^{N-1} - 2\}$$

$$INL(k) = \frac{V(k) - k \cdot V_{LSB}}{V_{LSB}}, \quad \{k \in \mathbb{Z} \,|\, 0 \leq k \leq 2^{N-1}\}$$

The maximum absolute value is taken to express the nonlinearity in a single positive number.

$$DNL = max|DNL(k)|, \quad \{\forall k \in \mathbb{Z} \,|\, 0 \leq k \leq 2^{N-1} - 2\}$$

$$INL = max|INL(k)|, \quad \{\forall k \in \mathbb{Z} \,|\, 0 \leq k \leq 2^{N-1} - 1\}$$

Nonlinearity in a charge-redistribution DAC is caused by capacitor mismatch. Like mismatch in MOS transistors [6][7], capacitors have similar mismatch behaviour. Their variance is given by:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{W \cdot L}} \; or$$

$$\sigma(C) = C\frac{A_C}{\sqrt{W \cdot L}}$$

Capacitor mismatch has a square-root dependence on area. This implies e.g. that if capacitor $C_1 = 2 \cdot C_0$, the standard deviation $\sigma(C_1)$ is $\sqrt{2}$ times larger than $\sigma(C_0)$

$$\sigma(C_1) = 2 \cdot C_0 \frac{A_C}{\sqrt{2 \cdot W \cdot L}} = \sqrt{2} \cdot \sigma(C_0) \tag{3.1}$$

The maximal $DNL(k)$ typically occurs at the MSB transition where $k = 2^{N-1}-1$, at this transition C_{MSB} is switched on while the capacitors $\sum_{i=LSB}^{MSB-1} C_i$ are switched off. In this transition the maximum number of capacitors switch. Equation (3.1) shows that the larger capacitors have a higher variance, at MSB transitions the switched capacitance is maximal resulting in a larger DNL. Equation (3.2) gives the DNL for the MSB transition.

$$\frac{DNL_{MSB}}{V_{LSB}} = \frac{V(2^{N-1}) - V(2^{N-1} - 1)}{V_{LSB}} - 1 \tag{3.2}$$

Substituting equation (1.1) in (3.2) gives the DNL expressed in capacitor ratios:

$$\frac{DNL_{MSB}}{V_{LSB}} = \frac{C_N - \sum_{i=1}^{-1} C_i}{2^{-N} \cdot C_{TOTAL}} - 1 = 2^N \cdot \frac{C_N - \sum_{i=1}^{N-1} C_i}{\sum_{i=0}^{N} C_i} - 1$$

This formula can be written in the following form[8]:

$$Y = 2^n \cdot \frac{X_1 - X_2}{X_1 + X_2 + C_0} - 1 \tag{3.3}$$

Where the mean and standard deviation of both X_1 and X_2 are given by:

$$E(X_1) = 2^{N-1} \cdot C_0, \qquad \sigma(X_1) = \sqrt{2^{N-1}} \cdot \sigma C_0$$

$$E(X_2) = 2^{N-1} - 1 \cdot C_0, \qquad \sigma(X_2) = \sqrt{2^{N-1} - 1} \cdot \sigma C_0$$

The left hand side in equation (3.3) does not correspond to a normal distribution, due to the non-linear relation. A Taylor expansion is used in [8] to approximate the standard deviation:

$$\frac{\sigma(DNL_{MSB})}{V_{LSB}} = \frac{\sigma(C)}{C}\sqrt{2^N - 1 - 2^{-N}} \approx \frac{\sigma(C)}{C}2^{N/2}$$

To decrease the mismatch at MSB transitions, the MSB capacitor can be split in two equally sized capacitors, making a partially thermometer-coded DAC with 1 thermometer-coded bit. This halves the switched capacitance at the MSB transition, which decreases the standard deviation at the MSB transition by $\sqrt{2}$, resulting in the same deviation as a fully binary coded DAC with (N-1)-bit resolution [8].

3.3 Energy

In a SAR ADC as shown in figure 3.1, the two DACs do complementary operations. After every comparison one DAC increases its output where the other DAC decreases its output. In a binary-coded DAC the output is increased by charging C_{MSB-1}. The output in the other DAC is decreased by discharging C_{MSB} and charging C_{MSB-1}. In both cases C_{MSB-1} is charged. This operation is visualized in table 3.1. Going from 2 to 3 or 1 for binary coding, requires charging of the LSB-bit in both directions. For thermometer coding,

Table 3.1: Binary and thermometer coding.

Decimal	Binary	Thermometer
1	01	001
2	10	011
3	11	111

going from 2 to 3 requires the same energy as the binary-coded equivalent because one bit is charged, however, going from 2 to 1 only requires discharge of a bit. Therefore a thermometer-coded DAC saves energy compared to a binary coded DAC.

3.4 Unit-cell

An unit-cell capacitor and its parasitics can be modelled as depicted in figure 3.2 [9]. Where C_u is the unit capacitor, C_{pT} is the top-plate parasitic, C_{pB} is the bottom plate parasitic and $C_{p\Delta}$ is the parasitic coupling from the top plate to the bottom plate, the deviation of to C_u. The $C_{p\Delta}$ parasitic is mainly defined by coupling to routing wires. C_{pS} is the non-linear output capacitance of the inverter switch. Including the parasitic effects equation, (1.1) from chapter 1 can be written as equation (3.4). Equation (3.4) gives the output voltage, V_{out} of the DAC depicted in figure 1.5, and illustrates the effect of the parasitics depicted in figure 3.2.

$$V_{out} = V_{in} + V_{ref}\frac{\sum_{i=1}^{N}\overline{D_{i-1}}\cdot(C_i + C_{i,p\Delta})}{C_{total} + C_{pT}} \tag{3.4}$$

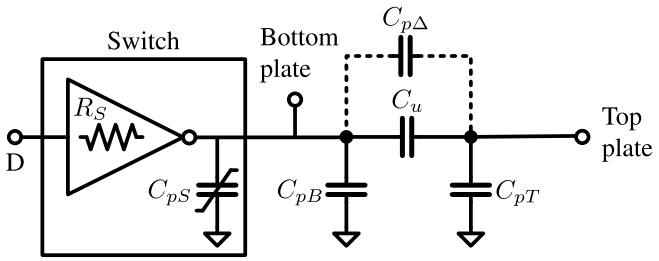

Figure 3.2: (MOM) unit capacitor model.

From equation (3.4) it is clear that C_{pT} will give a gain error, but C_{pT} will not affect the linearity of the DAC. In the system specifications $V_{ref} = 0.8V$ while the input voltage swing is $1.4V_{pp}$ which means that the DAC output is allowed to be $0.7V_p$. The gain of the DAC should be $\frac{7}{8}$ and therefore C_{pT} is dimensioned, by putting dummy unit-cells between TP and ground, to be $\frac{C_{total}}{7} = \frac{2^N}{7}C_0$. C_{pB} and C_{pS} only have an impact on the settling time and energy consumption. This should be taken into account when designing the switch with switch resistance R_S. From equation (3.4) it is clear that $C_{p\Delta}$ directly affects the linearity, therefore it is beneficial to design a unit-cell capacitor that minimizes this effect. Figure 3.3 shows the parasitics in a cross-sectional view of the layout.

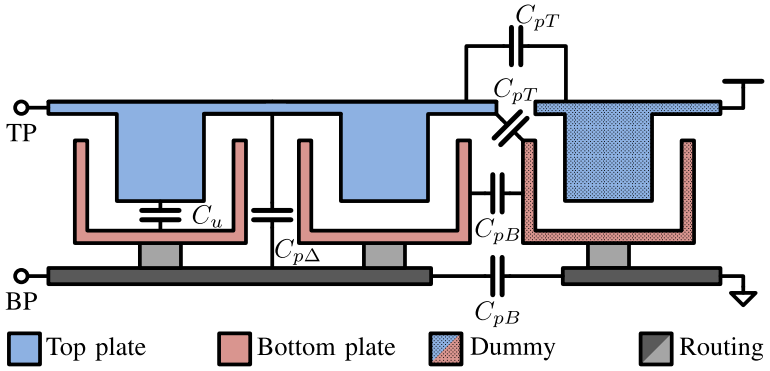

Figure 3.3: cross section of the DAC showing parasitics.

Layout

The unit-cell layout features a pillared top plate enclosed by a box-shaped bottom plate. In this design the top plate is isolated by the bottom plate, away from the substrate and routing wires, minimizing $C_{p\Delta}$. The design as depicted in figure 3.4 and 3.5 is based on [10], with a few changes to adapt it to the 22nm FD-SOI technology. Figure 3.4 shows how the unit cell is build up using 5 metal layers. The first two metal layers are used for routing. Figure 3.5 shows the top view of the unit-cell design. The top-plate is cross shaped to

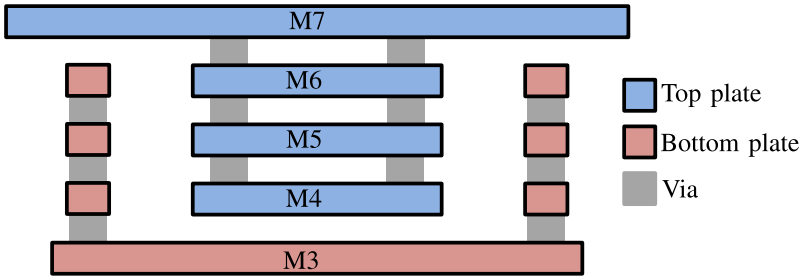

Figure 3.4: Cross-sectional view of proposed MOM capacitor.

interconnect with bordering unit-cells, creating a unit-cell matrix of capacitors. The first metal layer above the capacitor bank is connected to V_{SS} to shield the top plate. The unit cell is $750nm$ by $750nm$, occupying $0.56\mu m^2$.

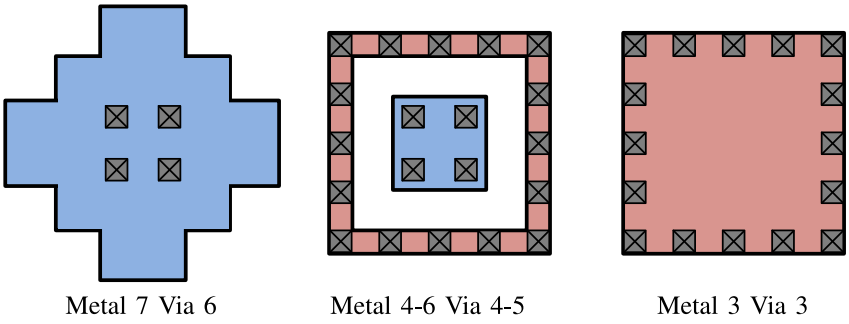

Figure 3.5: Top view of proposed MOM capacitor.

3.5 DAC layout

As discussed in the previous section, the routing wires define $C_{p\Delta}$ and therefore the linearity of the DAC. In order to minimize this, the proposed floor plan in figure 3.6 uses only one routing wire underneath each unit-cell capacitor. The label denotes the connection to the corresponding set of unit-capacitors. The DAC is implemented in a rectangle shape. Dummy-cells are added to minimize edge effects. One row of dummy-cells is added above the DAC, and two rows on either side and beneath the DAC. These dummies are connected to the top plate and V_{SS} to meet the required gain and input swing of $1.4Vpp$. Additional dummies, connected as decoupling capacitors between V_{DD} and V_{SS}, are placed around this structure to further reduce possible process variations. An overview of the DAC layout is given in appendix E.

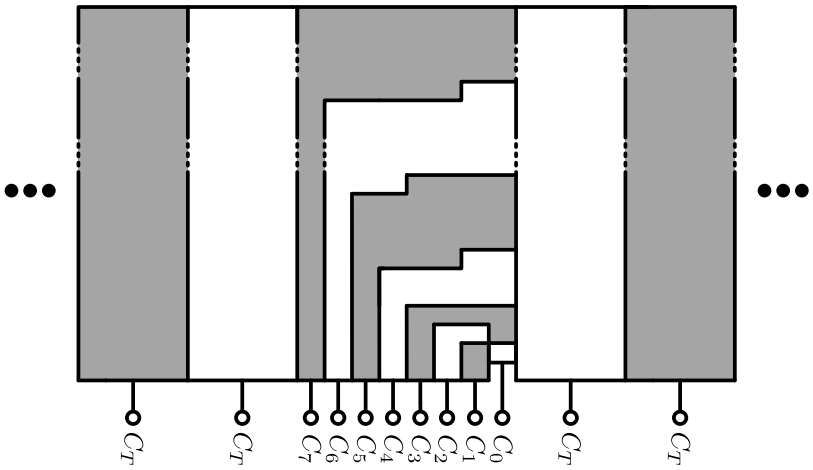

Figure 3.6: Floor-plan of proposed DAC.

3.6 Switches

The switches(figure 3.7) switching the different sets of the capacitor matrix need to settle within $\frac{1}{2}V_{LSB}$ accuracy in a 500ps time-frame as described in chapter 2. The settling of a RC circuit is given by equation (3.5).

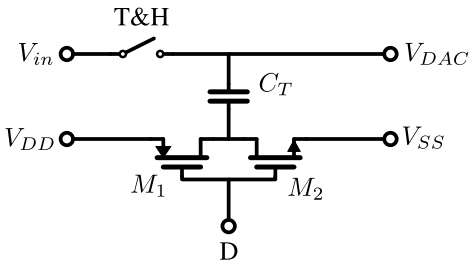

Figure 3.7: DAC capacitor inverter switch.

$$Settling = 1 - e^{-\frac{T}{\tau}} \tag{3.5}$$

The settling accuracy requirement can be written as follows:

$$Settling_i = 1 - \frac{\frac{1}{2}V_{LSB}}{2^{i-1}V_{LSB}} = 1 - \frac{1}{2^i} \tag{3.6}$$

Substitution of equation (3.5) and (3.6) gives:

$$\left(\frac{T}{\tau}\right)_i > -\ln\left(\frac{1}{2^i}\right) \tag{3.7}$$

With a budget of 500ps for DAC settling the maximal switch resistance can be calculated.

$$R_{S_i} = \frac{500ps}{\left(\frac{T}{\tau}\right)_i \cdot C_i} \tag{3.8}$$

The switches are implemented as inverters as depicted in figure 3.7 and scaled to have a smaller on-resistance than required(table 3.4). Promost shows an

Table 3.2: Maximal values for the on-resistance of DAC switches.

i	C	bit	settling [%]	$\left(\frac{T}{\tau}\right)$	$R_S[\Omega]$
12	$16 \cdot C_T$	MSB	99.976	8.32	1.60k
11	$8 \cdot C_T$	MSB-1	99.951	7.62	1.75k
...	...	...	...	...	...
7	$64 \cdot C_0$	7	98.438	4.85	5.50k
...	...	...	...	...	...
2	$2 \cdot C_0$	LSB+1	75.000	1.39	614k
1	C_0	LSB	50.000	0.69	2.47M

on-resistance for a minimum size NMOS of $2.0k\Omega$ and a minimum size PMOS of $5.9k\Omega$. Therefore a minimum size inverter switch is sufficient for the first 6-bits.

3.7 Results and conclusion

The DAC capacitor array is used as the C_{hold} capacitor for the track and hold circuit. By switching a set of DAC capacitor bottom plates to V_{DD} or V_{SS} the voltage on the top plate is changed, generating a new reference voltage for the comparator. The dimensions of the DAC layout are given by table 3.3. To validate the DAC design for capacitor mismatch, it is compared with

Table 3.3: Dimensions DAC.

post-layout single DAC	
A_{C_u}	$0.56\mu m^2$
C_u	282aF
A_{total}	$4250\mu m^2$
C_{total}	1.16pF
$C_{pT_{total}}$	153fF

a 12-bit ADC[11] that uses 3 thermometer-coded bits and has a unit-cell area of $0.8\mu m^2$ in 65nm CMOS. Since the 22nm FD-SOI technology is likely to be more precise, but the unit-cell area is smaller, the mismatch will be in roughly in the same order. Because this design uses one more thermometer-coded bit the mismatch of this design is expected to be superior to the design in[11].

Promost is used to size the switches to achieve the required on-resistance. The switches are designed with two times less on-resistance to compensate for

process variation and the parasitic capacitance. PMOS and NMOS transistors have the same size. The switch dimensions are given in table 3.4.

Table 3.4: Dimensions of DAC switches.

N	Capacitor	$\frac{W}{L}[nm]$
8-12	C_T	400/20
7	$64 \cdot C_0$	200/20
1-6	$C_0 - 32 \cdot C_0$	80/20

Chapter 4

Comparator

The comparator in the ADC has to differentiate between its two inputs within $< 0.5LSB$ accuracy, and therefore is one of the sub-circuits that defines the precision of the ADC. The challenge is to achieve good accuracy, high speed and low energy consumption.

4.1 Implementation

The comparator as proposed by [1] is depicted in figure 4.1. The pre-amplifier uses dynamic biasing[12]. The regenerative latch is based on the latch in the comparator presented in [2].

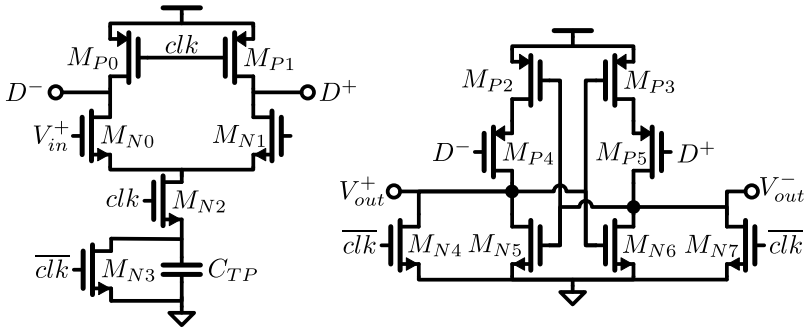

Figure 4.1: Dynamic bias comparator.

4.2 Pre-amplifier

The pre-amplifier, depicted in figure 4.2, has two phases of operation. The reset-phase, where the parasitic drain capacitors of the differential pair are charged to the supply voltage, and a comparison-phase where the parasitic drain capacitors are discharged into the tail capacitor generating a differential output voltage at the drain nodes. The benefit of the tail capacitor is that it, especially for high differential input voltages, quenches either M_{N0} or M_{N1} as

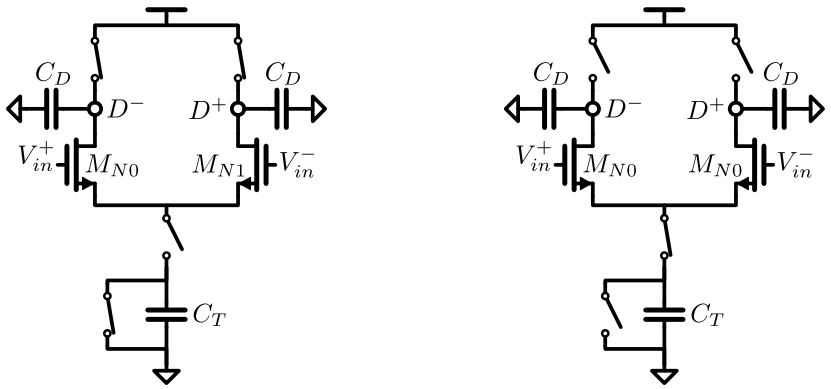

Figure 4.2: Pre-amplifier: Left: Reset-phase. Right: Comparison-phase.

the voltage over C_T rises. Thereby freezing the voltage on either node D^+ or D^- and saving energy in the next reset phase.

4.3 noise

The SNR is lowest for small ΔV_{in}. For a small ΔV_{in}, V_{in}^+ and V_{in}^- are close to the common mode of 350mV and both M_{N0} and M_{N1} will operate in weak inversion since $V_{gs} < V_{th}$. For weak inversion the drain current I_d is given by equation (4.1).

$$\begin{aligned} I_d &= I_0 \frac{W}{L} e^{\frac{V_{gs}}{\zeta V_t}} \left(1 - e^{-\frac{V_{ds}}{\zeta V_t}}\right) \\ I_0 &= \mu_n C_{ox} (\zeta - 1) V_t^2 \cdot e^{-\frac{V_{TH}}{\zeta V_t}} \end{aligned} \tag{4.1}$$

The thermal voltage V_t is constant for a fixed temperature as shown in equation (4.2).

$$V_t = \frac{kT}{q} \approx 26mV@300K \tag{4.2}$$

Because $\left(1 - e^{-V_{ds}/V_t}\right) \approx 1$ for $V_{ds} \geq 100mV$, saturation will occur. Under this condition equation (4.1) can be simplified to (4.3)

$$I_d = I_0 \frac{W}{L} e^{\frac{V_{gs}}{\zeta V_t}} \tag{4.3}$$

For weak inversion, the g_m of M_{N0} and M_{N1} is given by equation (4.4).

$$g_m = \frac{\delta I_d}{\delta V_{gs}} = I_0 \frac{W}{L} e^{\frac{V_{gs}}{\zeta V_t}} \cdot \frac{1}{\zeta V_t} = \frac{I_d}{\zeta V_t} \tag{4.4}$$

Where ζ is the body factor given by equation (4.5). C_{dep} is the depletion layer capacitance, and C_{ox} is the capacitance of the gate oxide.

$$\zeta = 1 + \frac{C_{dep}}{C_{ox}} \tag{4.5}$$

Due to the BOX isolation layer in the structure of a FD-SOI MOSFET the depletion capacitance C_{dep} is smaller than for normal bulk CMOS, therefore FD-SOI MOSFET's have superior G_m/I_d compared to conventional CMOS[4]. The input-referred noise is given by equation (4.6).

$$\overline{v_{n,i}^2} = \frac{4kT}{g_m} \cdot \Delta f \tag{4.6}$$

However, I_d in equation (4.4) is dependent on V_{gs} and therefore V_S, which is time dependent as shown in appendix A, therefore g_m changes over time. From [13] and [14] the noise bandwidth(NBW) or Δf of similar systems depends the noise integration time, and whether it reaches steady state. In the case of a dynamic bias comparator the NBW time is given by:

$$NBW = \frac{1}{2t}$$

In order to reduce $v_{n,i}$ it is beneficial to maximize the integration time within the given budget of chapter 2.2. The integration time increases when the threshold voltages of M_{P4} and M_{P5} of the latch are higher. Therefore high threshold(HVT) PMOS transistors are used for M_{P4} and M_{P5}. To give the pre-amplifier maximal integration time, the regenerative latch stage should require less time of the given budget.

4.4 latch

The second stage, or regenerative latch stage, turns on after the pre-amplifier has build up an adequate amount of gain. This is done using PMOS transistors that activate the latch when the drain nodes of the pre-amplifier have dropped below the V_{TH} of the PMOS transistors. The PMOS transistors, M_{P4} and M_{P5}, are place in the current path of the cross coupled inverters. The differential signal of D^+ and D^- results in a differential current in the cross coupled inverters, initiating the latching operation. The moment the latch turns on, the overdrive of the M_{P4} or M_{P5} is very low, so the regeneration of the latch is slow as well. In order to increase the latch regeneration speed, the voltage of D^+ and D^- needs to decrease further, in order to increase the overdrive of M_{P4} and M_{P5}. Therefore the discharge rate of D^+ and D^- is proportional to the speed of the latch. To achieve a high discharge rate, the quenching point of the pre-amplifier has to be significantly lower than the threshold voltage of M_{P4} and M_{P5}. The quenching point of the pre-amplifier is depends on the size of C_T.

4.5 Results

Taking all the described trade-offs in to account, the comparator was sized according to table 4.1. This simulation results are described in chapter 6.

Table 4.1: Dimensions comparator implementation.

Transistor	type	W	L
$M_{N0,N1}$	slvt	80μm	50nm
M_{N2}	slvt	4μm	20nm
M_{N3}	slvt	500nm	20nm
$M_{N4,N7}$	slvt	80nm	20nm
$M_{N5,N6}$	slvt	1μm	20nm
$M_{P0,P1}$	slvt	1μm	20nm
$M_{P2,P3}$	slvt	2μm	20nm
$M_{P4,P5}$	hvt	2μm	20nm

Capacitor	Capacitance
C_T	300fF

Chapter 5

Track-and-hold

The track-and-hold circuit can be seen as a switch that freezes an input voltage on a hold capacitor, as described in chapter 1. The track-and-hold circuit should not limit the effective resolution(ENOB) of the ADC by either noise or non-linearity. The noise is defined by the kT/C noise and does not limit the performance of the ADC since C_{hold} is larger than required for 12-bit resolution, as described in chapter 2. This chapter focusses on the linearity of the switch in the track and hold circuit.

Switch

The track and hold circuit is essentially an RC circuit where the switch resistance defines the settling precision within the given time budget(section 2.2). To maintain sufficient linearity the settling needs to be $\frac{V_{LSB}}{2}$ accurate within the allocated time. The required settling precision for half-LSB-accuracy, as a factor, is given by equation (5.1).

$$settling = \left(1 - \frac{1}{2^{N+1}}\right) \tag{5.1}$$

The T&H circuit can be seen as a first order RC circuit, and hence settles according to equation (5.2).

$$T_s = \left(1 - e^{-\frac{T}{\tau}}\right) \tag{5.2}$$

The required number of time constants can be obtained by substituting equation (5.1) and (5.2), resulting in:

$$\frac{T}{\tau} > \ln(2) \cdot (N+1)$$

For half-LSB accuracy in a 12-bit ADC, the minimum number of RC time-constants $\frac{T}{\tau} > 9.01$.
C_{hold} is defined by the noise and mismatch requirements of the ADC in chapter 2.1. The maximum on-resistance of the switch is therefore limited by the timing budget that is given to the track and hold in chapter 2.2.

$$r_{on} < \frac{\tau}{C_{hold}} = \frac{T_{budget}}{C_{hold} \cdot \left(\frac{T}{\tau}\right)};$$

With $C_{hold} = 1.2pF$, $\frac{T}{\tau} = 9.01$ and $T_{budget} = 2ns$ the maximum resistance for r_{on} becomes 185Ω.

5.1 Implementation

A single transistor or transmission gate is a simple way to implement a switch, however such an implementation limits the input swing and does not allow for rail-to-rail inputs[15]. In order to avoid this, the bootstrap circuit of Dessouky[15] is used. Although bootstrapping is mainly known from the work of Abo and Gray [16], the design of Dessouky[15]is favoured because it uses less transistors, since is has no clock multiplication. The bootstrap circuit is depicted in figure 5.1. The on-resistance of M_{N6} is given by equation (5.3).

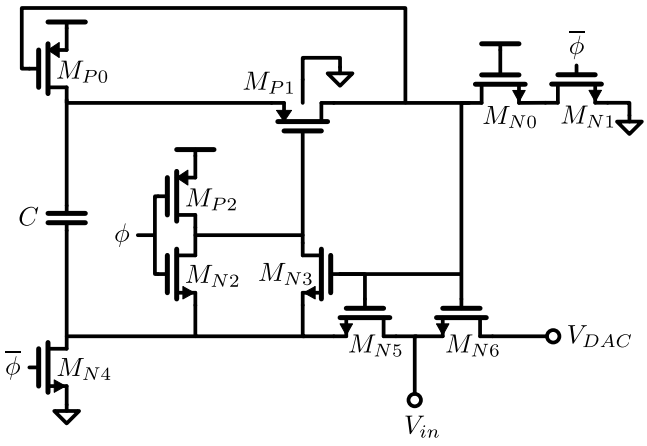

Figure 5.1: Bootstrap circuit implementation.

$$r_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})} \tag{5.3}$$

With the property of the bootstrap switch,$V_{gs} = V_{dd}$, the on-resistance is mainly dependent on $\frac{W}{L}$. The *Promost*-tool shows that on-resistance of a $100nm/20nm$ transistor is equal to $1.75k\Omega$ which means that a ten times larger device with 10 fingers will meet the required 185Ω. To limit the distortion even further, and compensate process variations, the $\frac{W}{L}$ of M_{N6} is set on $2\mu m/20nm$ with 20 fingers.

FD-SOI

The bootstrap switch in [15] has the bulk of M_{P1} connected to source terminal to suppress latch-up. In FD-SOI however, the PN-junctions, that result in intrinsic body diodes, are separated by an isolation layer. This isolation eliminates the latch-up problem. Figure 5.1 shows the body connection of M_{P1} to *gnd* which has less parasitic capacitance, allowing a smaller bootstrap capacitor[16].

Results

The bootstrap switch transistor, M_{N6}, is sized to meet the required on-resistance. All other transistors are kept small as possible in order to limit the parasitic capacitance that degrades the linearity. All transistors are super low V_T(SLVT) to maximize current driving capability and minimize on-resistance, while keeping roughly the same parasitic capacitances. The bootstrap capacitor size is

Table 5.1: Dimensions of the bootstrap switch implementation.

Transistor	$\frac{W}{L}[nm]$
M_{N0}	100/20
M_{N1}	300/20
M_{N2-5}	100/20
M_{N6}	2000/20
M_{P0-1}	100/20
M_{P0-1}	200/20

mainly dependent on the total parasitic capacitance at the gate of M_{N6}, this parasitic capacitance limits the voltage swing of V_{gs} due to charge sharing. The bootstrap capacitor size is 66fF and is determined by simulation.

Chapter 6

Simulations and Results

Testbenches are used to verify the functionality of the ADC subsystems. This chapter describes the three testbenches used to verify the behaviour of the DAC, comparator and track & hold circuit.

6.1 DAC

The testbench for the DAC, depicted in figure 6.1, contains a VerilogA implementation of an ADC with a partially thermometer-coded output. The VerilogA description of the ADC is given in appendix B. The sample rate of the ADC is set by the clock source connected to the ADC. The output code of the ADC depends on the input of V_{ref}. To simulate the linearity of the DAC,

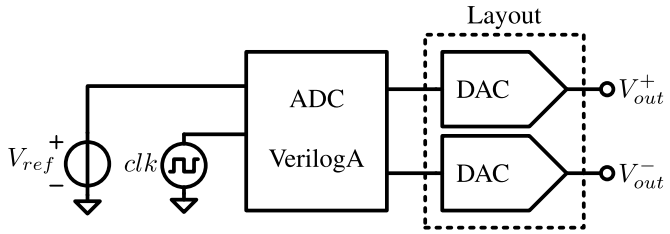

Figure 6.1: Testbench for the DAC linearity simulation in *Spectre/Cadence*.

the testbench is used with voltage ramp for V_{ref} and a clock of 1GHz. The ramp function is chosen such that every clock cycle the digital ADC output is incremented with one LSB. The VerilogA ADC also generates a complementary output to test the differential DAC structure. This creates an ideal digital staircase signal used as an input for the DAC. The differential DAC block itself is an extracted C+CC netlist of the DAC layout including switches, using *Calibre xACT* $3D$. It is important to use a 3-dimensional field solver like *Calibre xACT* $3D$ because complex fringe capacitance have an important share in the total capacitance of both the unit cell and the total capacitor bank. Non-3D extractions show 35% less capacitance. Extractions also show that the highest accuracy(*Accuracy mode* = 600) is required to achieve realistic results, the lower accuracy(*Accuracy mode* = 200) showed approximately 0.5% difference in capacitance for identical cells, resulting in a DNL of $0.6LSB$. Therefore

low accuracy is not sufficient to validate whether $C_{p\Delta}$(from the model in chapter 3) is small enough to not have a significant effect on the linearity of the DAC. The analog output of the differential DAC is used to plot the DNL as shown in figure 6.2. Note that this simulation only takes layout mismatch, $C_{p\Delta}$, into account and not the process variance. The process variance is not know at this point, a comparison with an existing DAC is made to verify the rough sizing, however real mismatch data can only be measured after the tape-out. The maximum simulated DNL occurs at a thermometer bit transition and is 0.13LSB, the maximum INL is also 0.13LSB. The signal swing of the simulated DAC is $1.37V_{pp}$. The energy consumption of the DAC in a SAR ADC de-

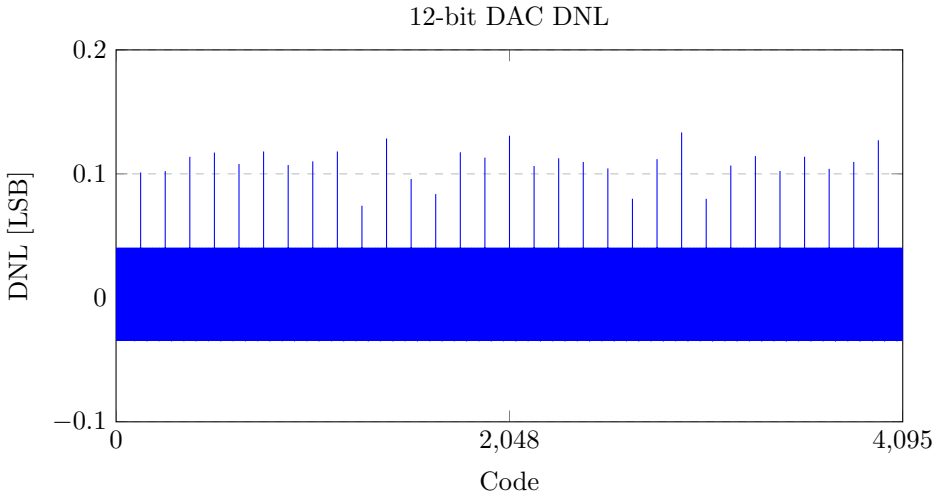

Figure 6.2: DAC DNL simulation result.

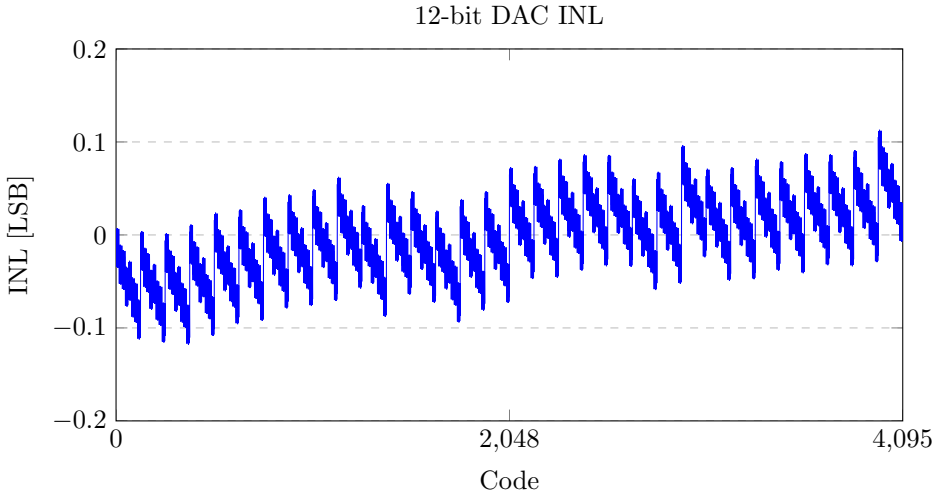

Figure 6.3: DAC INL simulation result.

pends on the input, and therefore the output of the DAC. Figure 6.4 shows the simulation results of the energy consumption of the DAC with $V_{ref} = 0.8V$. The energy consumption is simulated by using a VerilogA implementation of a comparator and SAR algorithm both for the partially thermometer-switched DAC, shown in appendix C, and for the same DAC using full binary switching, shown in appendixD. Simulations show an energy saving of 14.5%.

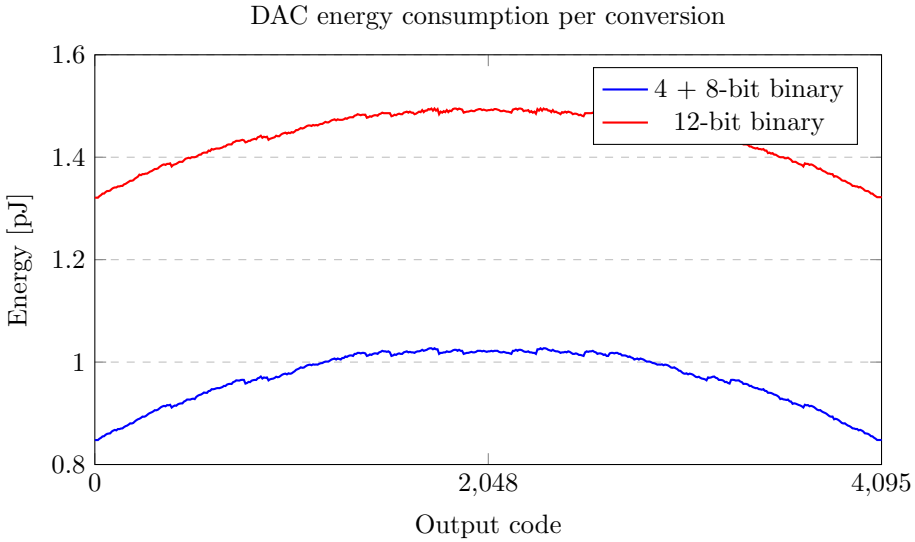

Figure 6.4: DAC energy simulation result.

6.2 Comparator

The testbench for the comparator is depicted in figure 6.5. The differential input is generated using an ideal balun. Since the noise performance of the comparator is most important for LSB comparisons, V_{DM} is $150\mu V$ for transient and $PSS/PNOISE$ noise simulations. V_{CM} is $350mV$ and the clock frequency of clk is 1GHz. The capacitance of the C_{load} capacitors is $10fF$ to model the additional digital circuitry behind the comparator. Both $PSS/PNOISE$ and transient simulations are used to simulate the noise performance and power consumption of the comparator. Figure 6.6 shows the output nodes of the pre-amplifier and the latch. The comparison time, or clk to Q delay is dependent on the input, and so is the power consumption. Table 6.1 give the performance for four different differential inputs. All simulations use the model parameter pre_layout_sw = 1 to estimate layout parasitics that will be included post-layout. The noise of the comparator is simulated using a transient simulation and a $PSS/PNOISE$ simulation. The result of both simulations do not map, the transient simulation results in $145\mu V$ input-referred noise and the $PSS/PNOISE$ simulation results in approximately $100\mu V$ input-referred noise. The transient simulation is favoured over the $PSS/PNOISE$ simulation because the $PSS/PNOISE$ seems to be less consistent when the noise analysis is done at a different time point. More research is required to see whether

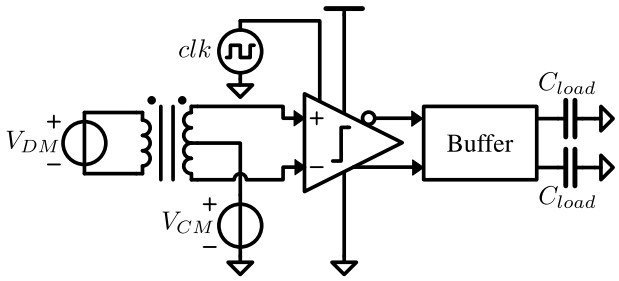

Figure 6.5: Testbench for comparator simulation in *Spectre/Cadence*.

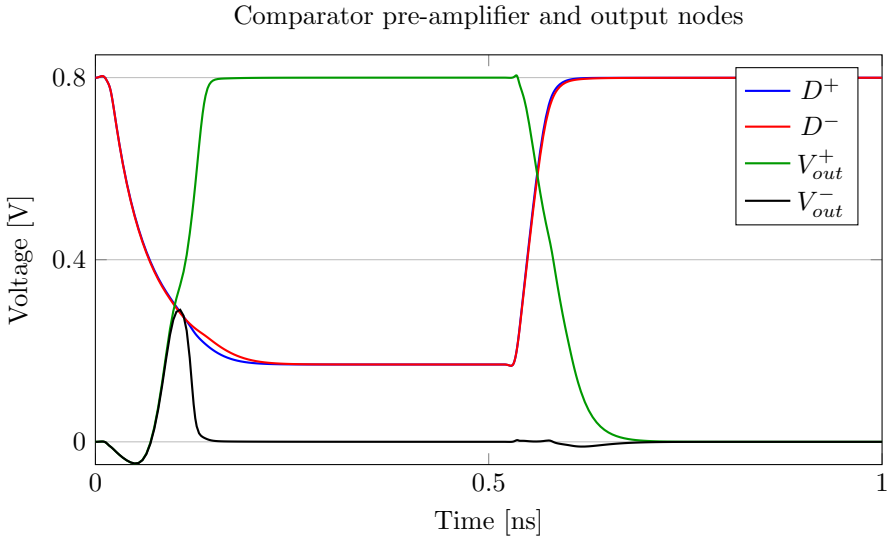

Figure 6.6: Pre-amplifier and output signals for $V_{DM} = 300\mu V$.

the $PSS/PNOISE$ simulation method is valid for this particular comparator architecture.

Table 6.1: Comparator performance at different V_{DM}.

V_{DM} [mV]	*clk to Q*[ps]	Energy [fJ]
0.1	145	60.5
1	132	57.8
10	113	55.2
100	70	48.0

6.3 Track and hold

The testbench for the track and hold circuit is depicted in figure 6.7. The differential input is generated using an ideal balun. The capacitance of the C_{hold} capacitors is 1.2pF to model the DAC capacitor array. $v_{CM} = 350mv$ and V_{DM} is a sine wave at $\frac{255}{512} \cdot f_{sample}$ with $V_{pp} = 1.4V$. The ideal balun converts this in to two signals with $0.7V_{pp}$ and 180° phase shift in one signal. Both signals have the same frequency as V_{DM}. Since this frequency is very close to the Nyquist frequency it also takes the settling accuracy into account because at some point it needs to make the maximum signal swing of $0.7V$ on the C_hold capacitor. The clock signals are at 100MHz with a duty cycle of 2ns corresponding to the timing budget allocated to the subcircuit in chapter 2. Results

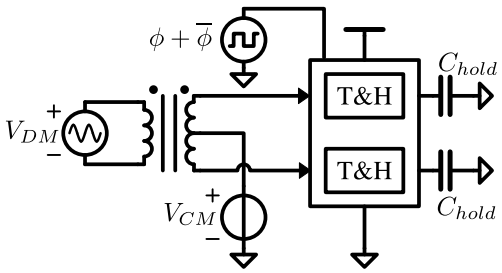

Figure 6.7: Testbench for track and hold linearity simulation in *Spectre/Cadence*.

of the transient schematic simulation, with pre_layout_sw = 1, are measured using the spectrum tool of the measurement tab in $Virtuoso/Cadence$. Taking 512 samples within a 50MHz spectrum ensured that the harmonics of the input frequency are exactly at one of the calculated frequencies in the direct Fourier transform(DFT). The resulting plot is shown in figure 6.8. The result of this simulation is summarized and shown in table 6.2 giving both the noise and distortion of the system. The track and hold circuit has an ENOB larger than 12-bit and has therefore only very little effect on the total system. The average power consumption for the differential track and hold circuit, simulated over 5000 samples, is $15fJ$.

Table 6.2: Summary of the track and hold linearity simulation.

N	Capacitor
ENOB	12.05
SINAD	74.35
SNR	76.45
SFDR	78.53

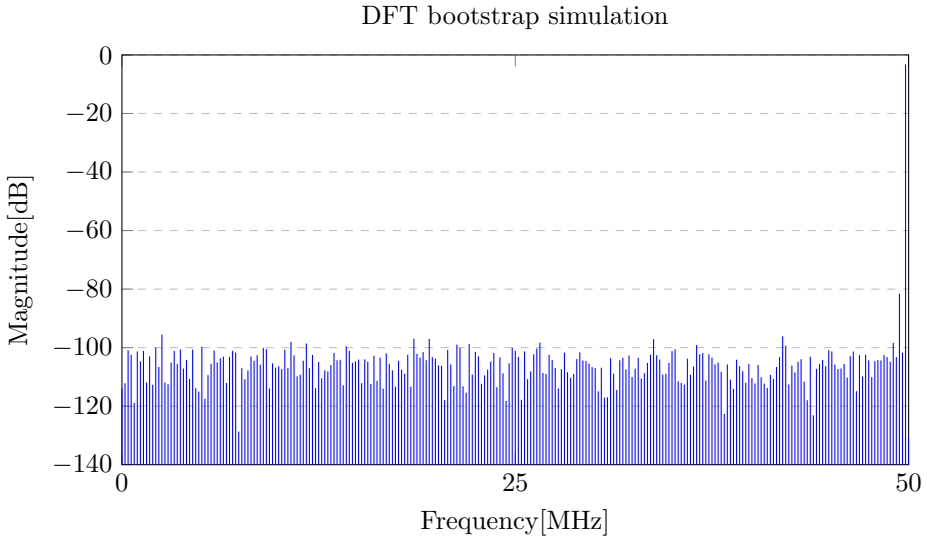

Figure 6.8: DFT of track and hold simulation

6.4 Power

An estimated figure of Merit (FOM) is used to compare the power efficiency of this ADC with other ADCs. Assuming that the effective resolution does not change significantly up to the Nyquist frequency $f_s/2$. The Walden FOM [17] can be simplified to:

$$FOM = \frac{P}{2 \cdot BW_{eff} \cdot 2^{ENOB}} = \frac{E_{conv}}{2^{ENOB}}$$

The energy consumption per conversion is the sum of the energy consumptions of the different subcircuits per conversion. $E_{control/comv}$ is the energy consumption of the control logic and delay line.

$$E_{conv} = E_{comp/conv} + E_{T\&H/conv} + E_{DAC/conv} + E_{control/conv}$$

The energy consumption of the comparator $E_{comp/conv}$ is the average energy

Table 6.3: Energy dissipation per conversion for every subcircuit.

Subcircuit	Energy/conv
Comparator	$670fJ$
DAC	$969fJ$
Track and hold	$15fJ$
Control	$670fJ$

consumption per comparison multiplied by the resolution. The energy consumption of the DAC is the average energy consumption of the simulation result in figure 6.4. The power of the control circuitry is estimated, based on

other ADC designs, to be in the same order as the comparator, taking into account that the 22nm FD-SOI technology offers great possibilities to reduce the power consumption in digital logic. Equation (4.6) from chapter 2 gives the total noise. Using the simulation results of the comparator, the total noise is:

$$\begin{aligned}\overline{v_{n,total}^2} &= \overline{v_{n,q}^2} + 2 \cdot \overline{v_{n,kTC}^2} + \overline{v_{n,comp}^2} \\ &= \frac{V_{LSB}^2}{12} + 2 \cdot \frac{2kT}{C} + 145\mu V^2 \\ &= 194\mu V^2\end{aligned}$$

The signal to noise ratio therefore is:

$$\begin{aligned}SNR &= 10 \log \frac{P_{signal}}{P_{noise}} \\ &= 10 \log \frac{V_p^2}{2 \cdot 194\mu V^2} \\ &= 68.1dB\end{aligned}$$

This SNR gives an ENOB of 11.03 bits when nonlinearity is neglected. However if the SFDR is similar to SNR, due mismatch in the DAC, the ENOB is reduced to 10.5 bits, resulting in a FOM of $1.6fJ/conversion - step$.

Chapter 7

Improvements & Optimization

7.1 DAC linearity

The DAC suffers from nonlinearity as described in chapter 3. But since this design is partially thermometer-coded, the DAC has a one-to-many relation for every digital input larger than one thermometer-bit. Therefore there are many ways to generate a specific analog output. The DAC in this SAR ADC has 38 switches which can be represented in an array as shown in figure 7.1. In a SAR

Figure 7.1: DAC representation

structure the DAC is reset to mid-code as depicted in figure 7.2. After the first comparison, the MSB is either 1 or 0. For MSB=1 the DAC switches on half of the bits dedicated to MSBm, as shown in figure 7.2. For MSB=0 the DAC

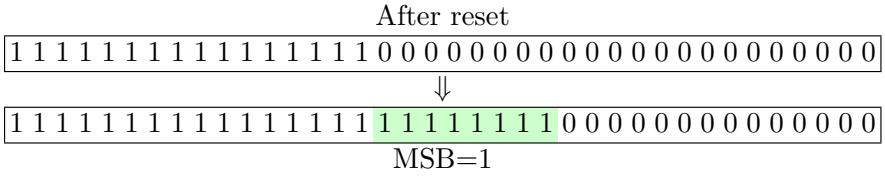

Figure 7.2: DAC after reset and first comparison, MSB = 1.

switches off half of the bits dedicated to MSB. as shown in figure 7.3. After

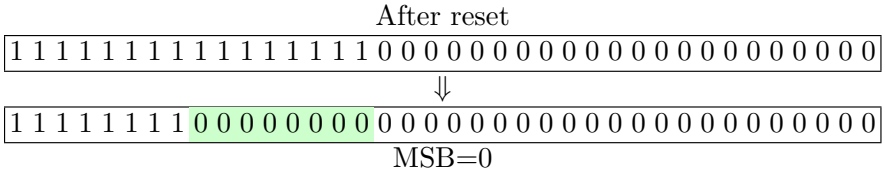

Figure 7.3: DAC after reset and first comparison, MSB = 0.

the complete SAR conversion, the output is given by 7.4. From this figure it is

easy to see that the MSB-bit is represented by 16 separate thermometer sets. Because the thermometer sets are identical in layout, and thanks to its many to one relation, it is possible to interchange thermometer units and thereby change the set for a particular bit. This property offers benefits for DAC matching.

MSB-4	MSB-3	MSB-2	MSB-1	MSB	MSB	MSB-1	MSB-2	MSB-3	MSB-5	LSB+5	LSB+4	LSB+3	LSB+2	LSB+1	LSB
T	T	T	T	T	T	T	T	T	T	B	B	B	B	B	B

Figure 7.4: DAC after each conversion

Since all the thermometer bits are the largest capacitors in the DAC capacitor array, the thermometer bit have the highest variance as described in chapter 3. The capacitor mismatch is mapped on a normal distribution in 7.5. By combining the most extreme negative and positive case into a single bit, the mismatch is averaged and therefore partially cancelled. This mechanism is visualized in figure 7.5. This mismatch cancellation technique requires extra

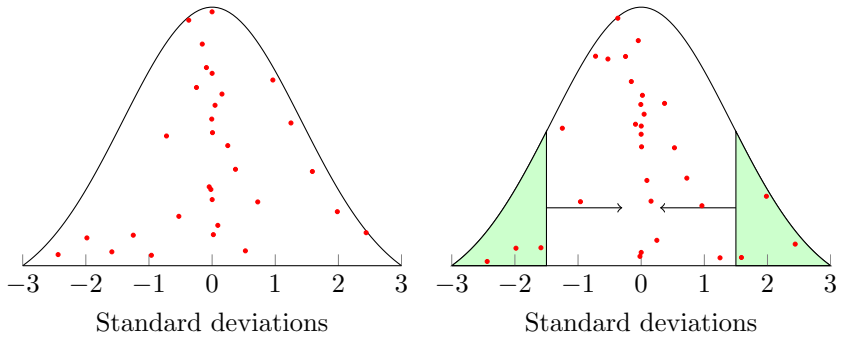

Figure 7.5: Left: Conventional. Right: After mismatch cancellation.

circuitry to route the SAR logic to different DAC switches. Further research is required on possibilities of this calibration.

Chapter 8

Conclusions & Recommendations

The main analog subcircuits of a SAR ADC are implemented in layout or schematic. A DAC design is proposed in chapter 3, based on a unit capacitor model. The DAC layout is validated by simulations of the extracted netlist in chapter 6 and show a INL and DNL of 0.13LSB due to parasitic coupling. Simulations of the DAC including inverter switches show a average energy dissipation of $969fJ$ per conversion. Process capacitor mismatch information is not yet available for similar capacitor structures in the Global Foundries 22nm FD-SOI technology. In order to minimize the mismatch effect, 4-bit thermometer coding is used, reducing the effect of mismatch effectively from a 12-bit to an 8-bit DAC[8]. Another way to reduce the mismatch effect is proposed in chapter 7.

A low power dynamic bias comparator [1] is implemented in the 22nm FD-SOI technology, schematic simulations with parasitic estimation show a noise level of $145\mu V$, an energy dissipation of $60fJ$ per comparison and a *clk to Q* delay of $145ps$ at an input of $100\mu V$. Because the process capacitor mismatch information is not yet available for the DAC it is recommended for a tape-out to also design a comparator with less noise, that in case of good mismatch results the ADC performance is not severely degraded by the comparator noise. Further research on the optimization and modelling of the comparator for speed, noise and energy consumption is recommended.

A track and hold circuit with a bootstrap switch[15] is implemented in the the 22nm FD-SOI technology. Schematic simulations with parasitic estimation show 12-bit ENOB and a very low energy consumption of $15fJ$ per conversion. This implementation reduces the parasitic capacitance in the bootstrap circuit by utilizing the FD-SOI properties.

If an ENOB of 10.5-bits is assumed and the energy consumption of the control circuitry is assumed to be the be equal to the energy consumption of the comparator, a FOM of $1.6fJ$/conversion step is obtained. The closest ADC in figure 8.1 is a SAR-assisted digital slope ADC and has a FOM of $2.6fJ$/conversion step at a sampling frequency of 100MS/s[5]

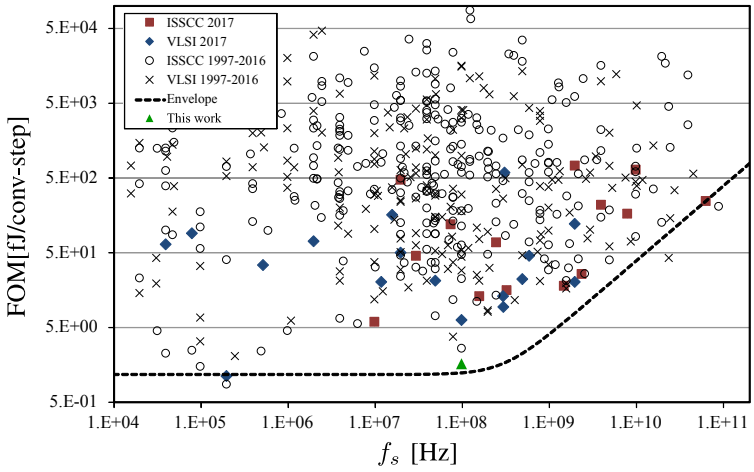

Figure 8.1: Comparison of the FOM versus effective sampling frequency of ADCs published at ISSCC and VLSI[18].

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Appendix A

Comparator pre-amplifier tail capacitor voltage

$$\begin{aligned} I_d &= I_0 \frac{W}{L} e^{\frac{V_{gs}}{\zeta V_t}} \\ I_0 &= \mu_n C_{ox} (\zeta - 1) V_t^2 \cdot e^{-\frac{V_{TH}}{\zeta V_t}} \end{aligned} \tag{A.1}$$

Taking:

$$K = I_0 \frac{W}{L} \tag{A.2}$$

$$I_d = K \cdot e^{\frac{V_{gs}}{\zeta V_t}} = C \frac{dV_S}{dt} \tag{A.3}$$

$$K \cdot e^{\frac{V_G - V_S}{\zeta V_t}} = C \frac{dV_S}{dt} \tag{A.4}$$

Resulting in the following first order non-linear differential equation:

$$\begin{aligned} \int \frac{K \cdot e^{\frac{V_G}{\zeta V_t}}}{C} dt &= \int e^{\frac{V_S}{\zeta V_t}} \cdot dV_S \\ \frac{K \cdot e^{\frac{V_G}{\zeta V_t}}}{C} t &= \int e^{\frac{V_S}{\zeta V_t}} \cdot dV_S \\ &= \zeta V_t \cdot e^{\frac{V_S}{\zeta V_t}} + Constant \end{aligned} \tag{A.5}$$

For $V_S(0) = 0$:

$$Constant = -\zeta V_t \tag{A.6}$$

rewriting the equation:

$$\frac{K \cdot e^{\frac{V_G}{\zeta V_t}}}{C \cdot \zeta V_t} t + 1 = e^{\frac{V_S}{\zeta V_t}} \tag{A.7}$$

$$V_S(t) = \zeta V_t \cdot \ln \left(\frac{K \cdot e^{\frac{V_G}{\zeta V_t}}}{C \cdot \zeta V_t} t + 1 \right) \tag{A.8}$$

Note: for this analysis the differential pair transistors are merged into one single transistor.

Appendix B

VerilogA DAC testbench

```
`include "constants.vams"
`include "disciplines.vams"
module veritest (outp, outn, in, clk);
parameter real td = 0;           //Delay = 0s
parameter real tt = 1f;          //transition time = 1fs
parameter real thresh = 0.8/2;   //Threshold = .5vdd
parameter real lsb = 0.8/4095;   //Lsb voltage
input in, clk;
output [0:37] outp;
output [0:37] outn;
voltage in, clk;
voltage [0:37] outp;
voltage [0:37] outn;
real sample, midpoint;
integer resultp[0:37];
integer resultn[0:37];
genvar i;
analog begin
  @(cross(V(clk) - thresh, +1) or initial_step) begin
    sample = V(in);
    midpoint = 64 * lsb;
    for (i = 37; i >= 0; i = i - 1 ) begin
      if ( i >= 7) begin       //Thermometer part
        if (sample > (128 * (i-6) * lsb)) begin
          resultp[i] = 0.8;
          resultn[i] = 0.0;
          sample = sample - (128 * lsb);
        end else begin
          resultp[i] = 0.0;
          resultn[i] = 0.8;
        end
      end else begin           //Binary part
        if (sample > midpoint) begin
          resultp[i] = 0.8;
          resultn[i] = 0.0;
          sample = sample - midpoint;
        end else begin
          resultp[i] = 0.0;
          resultn[i] = 0.8;
        end
        sample = 2.0*sample;
      end
    end
  end
```

```
  for (i = 0; i < 38; i = i + 1) begin     //Set outputs
    V(outp[i]) <+ transition(0.8 * resultp[i], td, tt);
    V(outn[i]) <+ transition(0.8 * resultn[i], td, tt);
  end
end
endmodule
```

Appendix C

VerilogA thermometer-coded DAC energy testbench

```
`include "constants.vams"
`include "disciplines.vams"
module veritest2(outp, outn, in, clk);
parameter real td = 0;          //Delay = 0s
parameter real tt = 1f;         //transition time = 1fs
parameter real thresh = 0.8/2;  //Threshold = .5vdd
input in, clk;
output [0:37] outp;
output [0:37] outn;
voltage in, clk;
voltage [0:37] outp;
voltage [0:37] outn;
real sample;
integer resultp[0:37];
integer resultn[0:37];
integer i = 0;
genvar j;
genvar k;
analog begin
  @(cross(V(clk) - thresh, + 1) or initial_step) begin
    sample = V(in);
    if(i == 0)begin
      for(j = 37; j >= 0; j = j - 1 ) begin
        if(j>=22)begin
          resultp[j]=0.8;
          resultn[j]=0.8;
        end else begin
          resultp[j]=0.0;
          resultn[j]=0.0;
        end
      end
    end else if(i==1)begin
      for(j = 29; j >= 14; j = j - 1 ) begin
        if(sample > 0.0)begin
          resultp[j]=0.0;
          resultn[j]=0.8;
        end else begin
          resultp[j]=0.8;
          resultn[j]=0.0;
        end
      end
    end else if(i==2)begin
```

```
      for (j = 33; j >= 30; j = j - 1 ) begin
        if(sample > 0.0)begin
          resultp[j]=0.0;
        end else begin
          resultn[j]=0.0;
        end
      end
      for (j = 13; j >= 10; j = j - 1 ) begin
        if(sample > 0.0)begin
          resultn[j]=0.8;
        end else begin
          resultp[j]=0.8;
        end
      end
    end else if(i==3)begin
      for (j = 35; j >= 34; j = j - 1 ) begin
        if(sample > 0.0)begin
          resultp[j]=0.0;
        end else begin
          resultn[j]=0.0;
        end
      end
      for (j = 9; j >= 8; j = j - 1 ) begin
        if(sample > 0.0)begin
          resultn[j]=0.8;
        end else begin
          resultp[j]=0.8;
        end
      end
    end else if(i==4)begin
      if(sample > 0.0)begin
        resultp[36]=0.0;
        resultn[7]=0.8;
      end else begin
        resultn[36]=0.0;
        resultp[7]=0.8;
      end
    end else if(i==5)begin
      resultp[6]=0.8;
      resultn[6]=0.8;
      if(sample > 0.0)begin
        resultp[37]=0.0;
      end else begin
        resultn[37]=0.0;
      end
    end else if(i==6)begin
      resultp[5]=0.8;
      resultn[5]=0.8;
      if(sample > 0.0)begin
        resultp[6]=0.0;
      end else begin
        resultn[6]=0.0;
      end
    end else if(i==7)begin
      resultp[4]=0.8;
      resultn[4]=0.8;
      if(sample > 0.0)begin
        resultp[5]=0.0;
      end else begin
        resultn[5]=0.0;
      end
    end else if(i==8)begin
```

```
      resultp[3]=0.8;
      resultn[3]=0.8;
      if(sample > 0.0)begin
        resultp[4]=0.0;
      end else begin
        resultn[4]=0.0;
      end
    end else if(i==9)begin
      resultp[2]=0.8;
      resultn[2]=0.8;
      if(sample > 0.0)begin
        resultp[3]=0.0;
      end else begin
        resultn[3]=0.0;
      end
    end else if(i==10)begin
      resultp[1]=0.8;
      resultn[1]=0.8;
      if(sample > 0.0)begin
        resultp[2]=0.0;
      end else begin
        resultn[2]=0.0;
      end
    end else if(i==11)begin
      resultp[0]=0.8;
      resultn[0]=0.8;
      if(sample > 0.0)begin
        resultp[1]=0.0;
      end else begin
        resultn[1]=0.0;
      end
    end
    i = i + 1;
    if(i == 12)begin
      i=0;
    end
  end
  for (k = 0; k < 38; k = k + 1) begin          //Set outputs
  V(outp[k]) <+ transition(0.8 * resultp[k], td, tt);
  V(outn[k]) <+ transition(0.8 * resultn[k], td, tt);
  end
end
endmodule
```

Appendix D

VerilogA binary-coded DAC energy testbench

```
`include "constants.vams"
`include "disciplines.vams"
module veritest3(outp, outn, in, clk);
parameter real td = 0;          //Delay = 0s
parameter real tt = 1f;         //transition time = 1fs
parameter real thresh = 0.8/2;  //Threshold = .5vdd
input in, clk;
output [0:37] outp;
output [0:37] outn;
voltage in, clk;
voltage [0:37] outp;
voltage [0:37] outn;
real sample;
integer resultp[0:37];
integer resultn[0:37];
integer i = 0;
genvar j;
genvar k;
analog begin
  @(cross(V(clk) - thresh, + 1) or initial_step) begin
    sample = V(in);
    if(i == 0)begin
      for(j = 37; j >= 0; j = j - 1 ) begin //reset
        if(j>=22)begin
          resultp[j]=0.8;
          resultn[j]=0.8;
        end else begin
          resultp[j]=0.0;
          resultn[j]=0.0;
        end
      end
    end else if(i==1)begin
      for(j = 21; j >= 14; j = j - 1 ) begin
        resultp[j]=0.8;
        resultn[j]=0.8;
      end
      for (j = 37; j >= 22; j = j - 1 ) begin
        if(sample > 0.0)begin
          resultp[j]=0.0;
        end else begin
          resultn[j]=0.0;
        end
```

```
    end
  end else if(i==2)begin
    for(j = 13; j >= 10; j = j - 1 ) begin
      resultp[j]=0.8;
      resultn[j]=0.8;
    end
    for (j = 21; j >= 14; j = j - 1 ) begin
      if(sample > 0.0)begin
        resultp[j]=0.0;
      end else begin
        resultn[j]=0.0;
      end
    end
  end else if(i==3)begin
    for(j = 9; j >= 8; j = j - 1 ) begin
      resultp[j]=0.8;
      resultn[j]=0.8;
    end
    for (j = 13; j >= 10; j = j - 1 ) begin
      if(sample > 0.0)begin
        resultp[j]=0.0;
      end else begin
        resultn[j]=0.0;
      end
    end
  end else if(i==4)begin
    resultp[7]=0.8;
    resultn[7]=0.8;
    for(j = 9; j >= 8; j = j - 1 ) begin
      if(sample > 0.0)begin
        resultp[j]=0.0;
      end else begin
        resultn[j]=0.0;
      end
    end
  end else if(i==5)begin
    resultp[6]=0.8;
    resultn[6]=0.8;
    if(sample > 0.0)begin
      resultp[7]=0.0;
    end else begin
      resultn[7]=0.0;
    end
  end else if(i==6)begin
    resultp[5]=0.8;
    resultn[5]=0.8;
    if(sample > 0.0)begin
      resultp[6]=0.0;
    end else begin
      resultn[6]=0.0;
    end
  end else if(i==7)begin
    resultp[4]=0.8;
    resultn[4]=0.8;
    if(sample > 0.0)begin
      resultp[5]=0.0;
    end else begin
      resultn[5]=0.0;
    end
  end else if(i==8)begin
    resultp[3]=0.8;
    resultn[3]=0.8;
```

```
      if(sample > 0.0)begin
        resultp[4]=0.0;
      end else begin
        resultn[4]=0.0;
      end
    end else if(i==9)begin
      resultp[2]=0.8;
      resultn[2]=0.8;
      if(sample > 0.0)begin
        resultp[3]=0.0;
      end else begin
        resultn[3]=0.0;
      end
    end else if(i==10)begin
      resultp[1]=0.8;
      resultn[1]=0.8;
      if(sample > 0.0)begin
        resultp[2]=0.0;
      end else begin
        resultn[2]=0.0;
      end
    end else if(i==11)begin
      resultp[0]=0.8;
      resultn[0]=0.8;
      if(sample > 0.0)begin
        resultp[1]=0.0;
      end else begin
        resultn[1]=0.0;
      end
    end
    i = i + 1;
    if(i == 12)begin
      i=0;
    end
  end
  for (k = 0; k < 38; k = k + 1) begin          //Set outputs
    V(outp[k]) <+ transition(0.8 * resultp[k], td, tt);
    V(outn[k]) <+ transition(0.8 * resultn[k], td, tt);
  end
end
endmodule
```

Appendix E

DAC layout

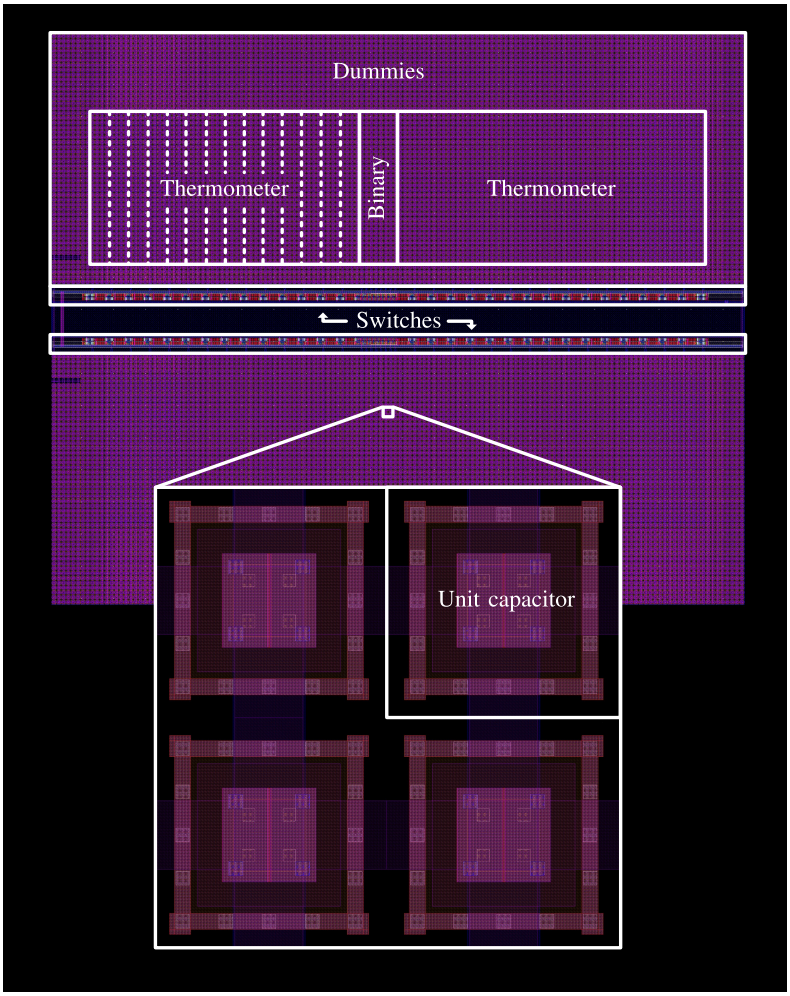

Figure E.1: DAC layout

Bibliography

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