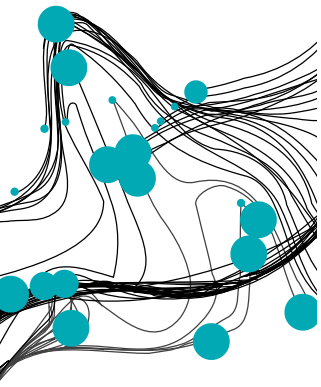

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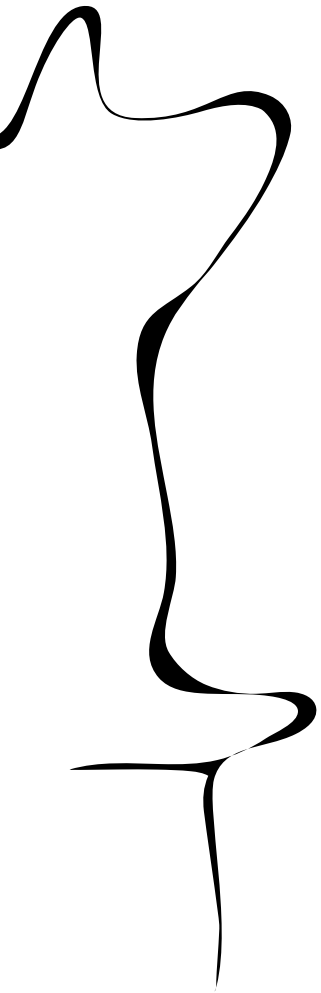

Analysis Of Sub-Sampling Phase-Locked Loop Dynamic Behaviour

MSc. Thesis
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1. Introduction

Since the beginning of civilisation timekeeping has been essential for its functioning. Working together is not very productive if one person turns up a year after the other.

The notion of when something should happen is also very important in electronics. The periodic signal that is used for this timing reference is either called a clock signal or Local Oscillator (LO). Digital circuits rely on this clock to time when an operation is done and the next one can begin. Analog circuits like a mixer, can use an LO to select which channel to receive.

Because the function of the circuit relies on this timing, the accuracy of the timing signal partly determines the circuit's performance. In the field of frequency synthesis jitter or phase noise gravely impact that accuracy. Jitter being the time deviation of the zero-crossings of the timing signal, as compared to an ideal version of that timing signal. Phase noise is the frequency domain equivalent of jitter. Both therefore, say something about the accuracy of the zero-crossings of the timing signal.

But, as is often the case in electronics there are many circuit parameters as can be seen in figure 1.1, each representing a possible performance metric. Depending on the application a different parameter can be the performance limiting factor.

In the case of Phase-Locked Loops (PLL) there is usually a focus on jitter and power consumption parameters.
For instance, when using a PLL for the clock in a digital circuit it should have low jitter to allow for high speed operation. It should also consume little power so that it can last

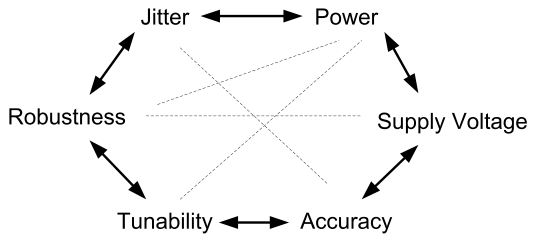


Figure 1.1.: A few circuit parameters that can be a measure of quality.

longer on a battery.
However, if a PLL is used to select the channel for a radio application like Bluetooth it also important how fast it can change its output frequency. Bluetooth may change its channel 1600 times per second meaning it stays tuned to one frequency for only 625 µs. In order to have as much time as possible to send data the channel switching time of the PLL must be much shorter than 625 µs [1]. That means the required channel switching time is in the order of 10 µs.

1.1. Phase-Locked Loops

The previous section explained that there is a need for an electronic timing signal and that applications can have performance requirements for any circuit parameter. Now it is time to take a closer look at the most employed synthesizer timing signal architecture, called the Phase-Locked Loop (PLL). A basic schematic for a PLL is shown in figure 1.2. A PLL can either be used to synchronize its output frequency with its input frequency or to synthesize a new output frequency from a fixed frequency source. This thesis focusses on using a PLL as a frequency synthesizer.

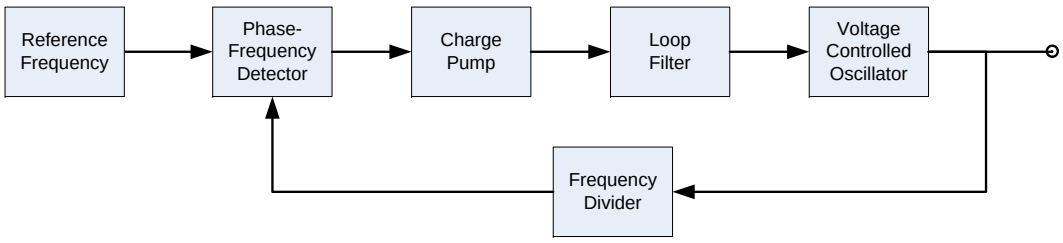


Figure 1.2.: Block schematic for a basic PLL.

In the case of frequency synthesis the "reference frequency" from figure 1.2 comes from a high fidelity timing reference. Commonly used as this reference are piezoelectric materials. Usually these are quartz crystals and have therefore come to be known as crystal oscillators (XO). The jitter of an XO can be very low at for example 124.9 fs when integrated from 100 Hz to 200 kHz [2]. The absolute frequency accuracy of an XO is also very good and usually in the order of 10 to 50 ppm [2]. The biggest down side of using crystals without a PLL is that the available output frequencies are only up to tens-of-megahertz and without the PLL cannot be changed over a wide range.
Firstly, for modern day applications these frequencies are quite low, as applications using frequencies of multiple gigahertz are commonplace. Secondly, most applications that use a timing signal no longer operate on just one frequency, like radio-frequent communication, analog-to-digital converters and digital circuits. Instead, mixers switch frequencies to select a different channel and digital circuits vary their clock frequency to conserve

power.

Thus, an XO is a good reference to start from. However, a functional block in series is needed that converts the high fidelity signal from the XO into a tunable high output frequency. This functional block is either called a Clock Multiplier Unit, Frequency Synthesizer or Frequency Multiplier depending on whether the output signal is used as a time or frequency reference.
There are various known frequency synthesizer architectures of which the most important ones are outlined in [3, Chapter 1.3]. That thesis builds the case for the Phase-Locked Loop (PLL) as being the best choice for a high-speed low jitter frequency synthesizer.

Looking at PLL publications, more often than not the jitter and power consumption are the key performance metrics and therefore focus of the publication. In order to objectively compare PLL implementations with respect to jitter and power consumption, a Figure-Of-Merit (FOM) was derived in [4]. This FOM indicates how far from ideal a PLL is with respect to jitter versus power dissipation. A lower FOM indicates a better design.
Currently, the lowest published FOM is held by the Sub-Sampling Phase-Locked Loop (SSPLL) developed by Gao et al. [5] at the Integrated Circuit Design group of the University of Twente.

However, jitter and power dissipation are only two of many performance measures.
For example tunability, is an area where the SSPLL could be improved. A big downside of the traditional PLL is that the output frequency is always stepped by an integer multiple of the reference frequency. These PLLs are therefore called integer-N PLL. The SSPLL in [5] is also of this type.
For instance, this integer stepping of the output frequency directly determines how close adjacent channels can be in a communication link. In modern communication links many closely spaced channels are used to increase the link capacity. To build such a link using an integer-N PLL would require a very low reference frequency to match the channel spacing. For instance, in the GSM-900 standard the channels are spaced only 200 kHz apart [6]. The reference frequency is usually at least ten times higher than the loop bandwidth. This results in a trade-off between channel spacing and the switching time between channels, which is proportional to the loop bandwidth.
To break this trade-off fractional-N PLLs were introduced. A fractional-N PLL can also have an output frequency in between the usual integer steps. A very innovative method to make a fractional-N SSPLL was published in [7].

A publication by Hsu et al. [8] focusses on the SSPLL robustness to perturbations. In this paper it is shown that the SSPLL from [9] loses lock after a perturbation is injected into the loop and then takes several microseconds to recover lock. As mentioned before and illustrated with the example of bluetooth, in a lot of applications this is too long. Before the publication of [8] the dynamic behaviour of the SSPLL was not properly considered, but has been of growing interest ever since because of its crucial role in

practical applications.

1.2. Research Questions

The paper by Hsu et al. [8] opened up an internal discussion around the topic of SSPLL dynamic behaviour. Furthermore, in the recommendations of the PhD thesis by Gao [10] a related comment is found: "In some applications, the PLL settling time is an important specification. In the current design, a classical PLL with dead zone function as the FLL. Having a dead zone during frequency acquisition slows down the PLL settling, which may be problematic. It is worthwhile to investigate the settling behaviour of the SSPLL further."

The discussion and newly found information led to the following research questions:

> What is the influence of the dead zone in the phase frequency detector on the sub-sampling phase-locked loop dynamic behaviour?

> Can the robustness to perturbations of the SSPLL design from [9] be improved without removing the dead zone in the phase frequency detector?

> Can the dynamic behaviour of the SSPLL design from [9] be improved by optimizing its configuration?

1.3. Thesis Outline

Before going deeper into the analysis of SSPLL dynamic behaviour some general information about PLLs and specifically SSPLLs will be presented in chapter two. The chapter closes with a discussion of some issues of SSPLLs.

Chapter three and four focus on finding answers to the research questions of the SSPLL design. Chapter three starts with loop filter design and loop stability. After that come simulations and analysis related to channel switching. Chapter four continues the simulations, but focusses on lock perturbation instead. The results from these two chapters are used to answer the research questions.

The thesis ends with a summary of the important conclusions from the thesis followed by recommendations for future work.

2. Phase-Locked Loop

This chapter will briefly describe some concepts concerning Phase-Locked loops (PLL) in general. Later on about the specific implementation called Sub-Sampling Phase-Locked Loop (SSPLL) that is the subject of this thesis will be discussed.

The simplest way of describing a PLL to an electrical engineer is by saying it is a voltage buffer for the phase domain. Like a voltage buffer a PLL is a feedback loop, where the output tracks the input. However, the quantity of interest is the phase of the signal instead of the voltage. By setting the feedback ratio the relation between the in and output of the loop can be defined. When moving on to study the inner working of a PLL things become more tricky. Depending on the node under inspection the quantity of interest may change from phase to current, voltage or frequency. Despite being difficult to analyse, many have studied and written about the PLL because of its usefulness in electronics. An important application for PLLs is as a frequency synthesizer, which is also the focus of this thesis.

The basic buildings blocks for a PLL are shown in figure 2.1. The reference frequency is usually a crystal oscillator (XO) whose jitter can be very low at for example 124.9 fs when integrated from 100 Hz to 200 kHz [2]. The absolute frequency accuracy of an XO is also very good and usually in the order of 10 to 50 ppm [2]. The biggest down side of using crystals without a PLL is that the available output frequencies are only up to tens-of-megahertz and cannot be changed over a wide range. The application area for PLL frequency synthesizers is very wide from the audio range all the way to the gigahertz range.
The Phase Frequency Detector (PFD) modulates the width of its output current as a measure for the phase difference between the reference and the divided VCO output.
The Charge Pump (CP) converts this voltage to a current to be fed into the loop filter and theoretically provides infinite gain. The total charge going into the loop filter is called a charge packet and is expressed by $I_{CP} * T_{on}$. Where T_{on} denotes the on time of the charge pump transconductance and adds a degree of freedom for possible gain control. A schematic of the PFD followed by a charge pump and its characteristic are shown in figure 2.2. The PFD-CP characteristic shows a linear relation between the average output current $\overline{i_{CP}}$ on the y-axis and the phase difference between the reference and the divided VCO output $\Delta\phi_{div}$ on the x-axis. At a phase difference of 2π the average output current reaches its maximum. For a bigger phase difference the characteristic repeats itself, due to the periodic nature of the compared signals. What is very important, is that the sign of the average output current is positive for all positive phase differences and

negative for all negative phase differences. This property gives the PFD its frequency discrimination ability. The sign continuity means that the loop control action for a certain frequency difference is always in the same direction. If the characteristic would have additional zero-crossings, the loop control action would also be zero for multiple points. That would mean that there are multiple frequencies on which the PLL could lock. One of the things that makes PLLs useful is the ability to uniquely control the output frequency. Having multiple lock frequencies would mean a loss of this ability.
The loop filter suppresses high frequencies and gives the necessary degrees of freedom to stabilise the loop. Together with the PFD and CP an integrator is formed. This is important for the steady-state phase error, which will be discussed in section 2.1.
The Voltage Controlled Oscillator (VCO) is a tunable frequency synthesizer that can provide the desired gigahertz output range.
The frequency divider scales the output frequency by a factor N and in doing so sets the relation between the in and output frequency by the same factor.

The most common way to work with a PLL is to use a phase domain model which is presented in the next section.

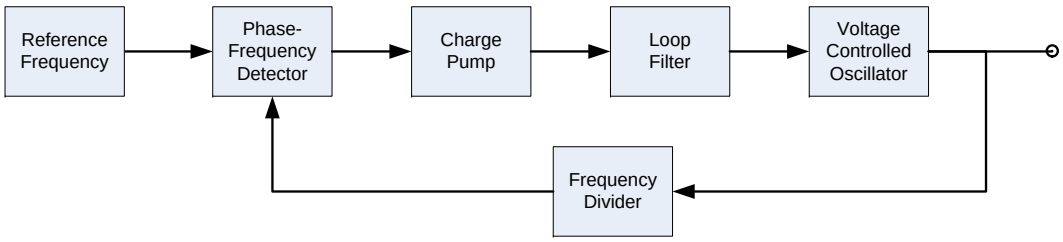


Figure 2.1.: Block schematic for a basic PLL.

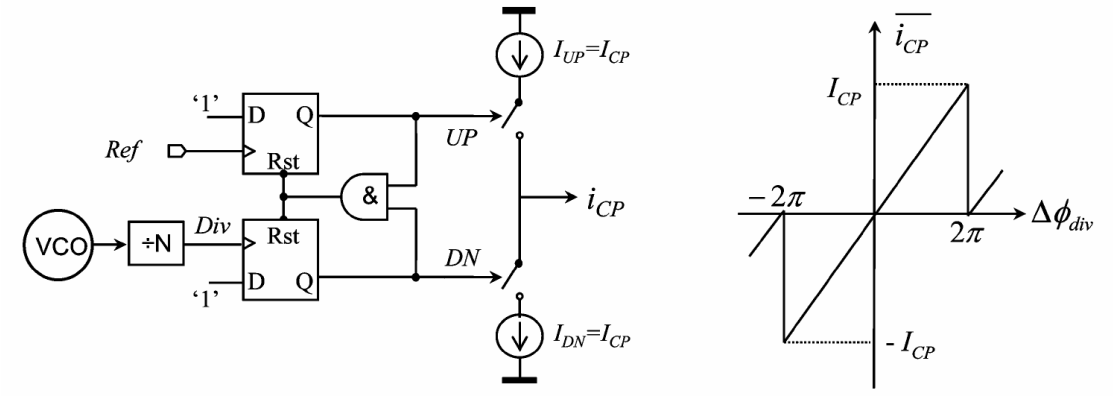


Figure 2.2.: Schematic of phase-frequency detector and charge pump and its characteristic. [9]

2.1. Phase-Locked Loop Phase Domain Model

PLLs are nonlinear, time-discrete circuits and are difficult to analyse and describe with mathematics. Therefore, a linear time-continuous model is often used and is competent provided that the loop bandwidth is much smaller than the reference frequency which acts as the sample frequency for the PFD. The rule of thumb for PLL design is that the loop bandwidth is at least ten times smaller than the reference frequency in order for the continuous time approximation to be good enough [11].

Figure 2.4 shows the phase domain model for a PLL. Most PLLs use a loop filter like the one shown in figure 2.3. This reduces the VCO output phase noise by adding extra suppression for high frequencies on the voltage that tunes the VCO (V_{tune}). The trans-impedance of this filter is given by:

$$Z_{lf}(s) = \frac{V_{out}}{I_{in}} = \frac{1}{C_2} \cdot \frac{(s + \frac{1}{R_1 C_1})}{s(s + \frac{C_1 + C_2}{R_1 C_1 C_2})} \tag{2.1}$$

Equation 2.1 shows that the filter has two poles and one zero. In the phase domain the VCO is modelled as K_{vco}/s as is shown in figure 2.4. This PLL is therefore a third order system, which is difficult to work with. However, this third order system can be approximated by a second order, by placing one pole at a much higher frequency than the others. This is done by making the second filter capacitance C_2 much smaller than the first. By doing this approximation the system is very similar to a standard second order system from control theory. In section 3.1 the loop filter and loop stability will be discussed further.
By doing the second order approximation the following equations describe the PLL transfer function:

$$H(s) = N \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.2}$$

$$w_n = \sqrt{\frac{K_{pd} K_{vco}}{C_1 N}} \tag{2.3}$$

$$\xi = \frac{R_1}{2} \sqrt{\frac{K_{pd} K_{vco} C_1}{N}} \tag{2.4}$$

$$K_{pfd} = \frac{I_{cp}}{2\pi} \tag{2.5}$$

Where N is the feedback frequency division factor, ξ the damping factor, ω_n the natural frequency, K_{vco} the VCO tuning gain, K_{pfd} the PFD gain and I_{cp} the charge pump current.

2.2. Phase-Locked Loop Figure-Of-Merit

When working on improving PLLs it is convenient to have a performance number with which to compare if progress has been made. For many circuits an equation for such a number exists. Often the number is called the Figure-Of Merit (FOM). Even though there are many possible measures of quality as was indicated in the introduction by figure 1.1, there are two that are most used for PLLs when trying to quantify performance. The first is the VCO output phase noise or jitter variance when viewed in the time domain. The second is the PLL power consumption.

In a paper by Gao et al. [4] the most used FOM for PLLs is derived:

$$FOM_{PLL} = 10 \cdot log10((\frac{\sigma_{t,PLL}}{1\text{s}})^2 \cdot \frac{P_{PLL}}{1\text{mW}}) \tag{2.6}$$

Where $\sigma_{t,PLL}$ is the PLL output jitter and P_{PLL} is the total PLL power consumption. The FOM increases with more power consumption and more output jitter. Because the goal is to create a PLL with as little power consumption and output jitter as possible, a lower FOM indicates a better PLL design.

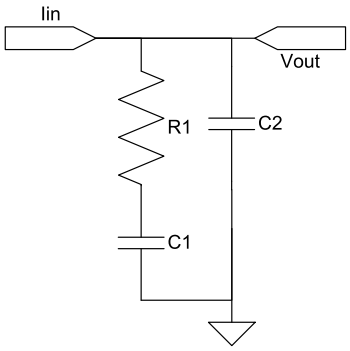


Figure 2.3.: The schematic for the two pole, one zero loop filter.

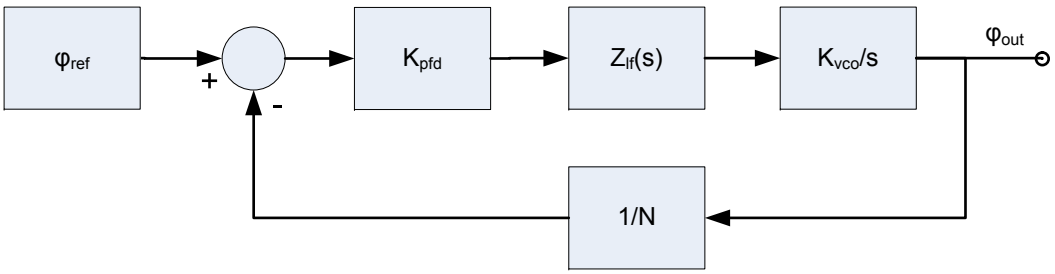


Figure 2.4.: The phase domain model of a PLL.

The derivation begins by analysing the propagation of noise sources through a typical PLL phase domain model such as in figure 2.2. From this an optimal PLL loop bandwidth is derived. The choice of PLL loop bandwidth minimizes the total PLL output phase noise when the phase noise contributions from the reference and loop equal that of the VCO. This also means that the loop and the VCO should be given an equal power budget.
The paper then goes on to show that the in and output frequency have no influence on the output jitter variance.
Lastly, if the assumption is made that all power consumption is dynamic power then it can be shown that the PLL output jitter variance is inversely proportional to the power consumption.

2.3. Sub-Sampling Phase-Locked Loop

With the goal of obtaining the lowest possible FOM, a PLL should have as little output jitter as possible while consuming as little power as possible.
Often the dominating noise source from the loop is the charge pump. If a feedback gain β_{CP} is defined from the PLL output to the charge pump output, it can be shown that the charge pump noise is suppressed by the square of this gain [9]:

$$\mathcal{L}_{in-band,CP} \approx \frac{S_{iCP,n}}{2\beta_{CP}^2} \tag{2.7}$$

Where $\mathcal{L}_{in-band,CP}$ is the single side-band noise power to carrier power ratio and $S_{iCP,n}$ the power spectral density of the charge pump current noise.
To obtain a low FOM the feedback gain should be increased with no additional power consumption.

This is the basis for using a different kind of phase detector with a higher gain instead of the traditional PFD. The Sub-Sampling Phase Detector (SSPD) shown in figure 2.5 is exactly that. The difference with the traditional PFD shown in figure 2.2 is that the SSPD directly samples the VCO output every reference period and outputs a voltage proportional to the phase difference between the reference and the VCO. This is illustrated in the SSPLL block schematic shown in figure 2.6.
Combined with a charge pump this gives the characteristic shown in figure 2.5. The characteristic shows a sinusoidal relation of the phase difference between the reference and the VCO $\Delta\phi_{VCO}$ and the average output current $\overline{i_{CP}}$. The maximum average output current is reached at a phase difference of $\pi/2$ modulo 2π. In contrast to the PFD, the SSPD characteristic has multiple zero-crossings. This means that the SSPD is not able to discriminate between different frequencies like the PFD can.
Because the VCO frequency is N times higher than the reference in frequency synthesizers, the VCO output has a very high slew rate. This translates to a very high phase

gain. In [9] the feedback gain for the traditional PFD and SSPD are given by:

$$\beta_{CP,PFD} = \frac{I_{CP}}{2\pi N} \tag{2.8}$$

$$\beta_{CP,SS} = A_{VCO} \cdot \frac{2I_{CP}}{V_{gs,eff}} \tag{2.9}$$

The equation for the ratio of the VCO output to PD output gain between a traditional PFD and SSPD is therefore given by:

$$\frac{\beta_{CP,SS}}{\beta_{CP,PFD}} = 4\pi \cdot N \cdot \frac{A_{VCO}}{V_{gs,eff}} \tag{2.10}$$

Where $N = \frac{f_{vco}}{f_{ref}}$, A_{VCO} is the VCO output amplitude, $V_{gs,eff}$ is the effective gate-source voltage of the MOS transistor. This ratio is much larger than 1, because 4π, $N \geq 1$ and usually $A_{VCO} > V_{gs,eff}$. Therefore the SSPD offers more charge pump noise suppression than a traditional PFD, resulting in a higher FOM.

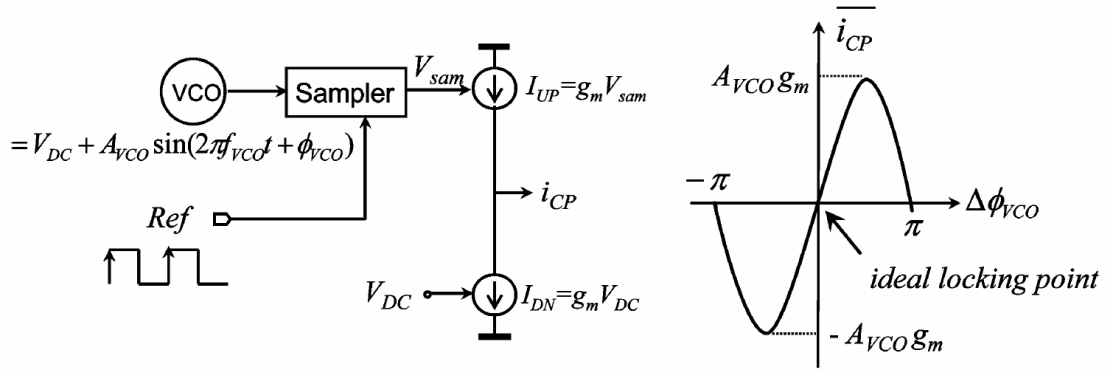


Figure 2.5.: Schematic of a sub-sampling phase detector and charge pump and its characteristic. [9]

One downside to using an SSPD is that it is frequency agnostic meaning it does distinguish between sampling $N \cdot f_{ref}$, $(N+1) \cdot f_{ref}$ or any other multiple. The way this was solved in [9] was to include a second loop that provides the frequency locking. This second loop was a traditional PLL with a Dead-Zone (DZ) added to the PFD. This enables the SSPLL to lock to the correct frequency. After that lock is made the traditional PFD is in its DZ and does not contribute to the phase noise.

Lastly, the feedback gain of the SSPD can actually be too high. Section 3.1 will explain that a higher feedback gain requires a larger loop filter capacitance for loop stability. The feedback gain should just be high enough to make the charge pump noise negligible. If the feedback gain becomes higher than that point, the loop filter capacitance must become very large for loop stability without gaining any noise benefit. The feedback

gain can then be said to be unnecessarily high and should be reduced. In [9] this was done by adding a Pulser block that only turns on the charge pump for a fraction τ_{pul} of the sampling period T_{ref}. This reduces the feedback by a factor $\frac{\tau_{pul}}{T_{ref}}$. The gain reduced feedback gain is given by:

$$\beta_{CP,SS} = A_{VCO} \cdot \frac{2I_{CP}}{V_{gs,eff}} \cdot \frac{\tau_{pul}}{T_{ref}} \tag{2.11}$$

The combined structure of sub-sampling and frequency loop is called a Sub-Sampling Phase-Locked Loop. A schematic of an SSPLL is shown in figure 2.6.

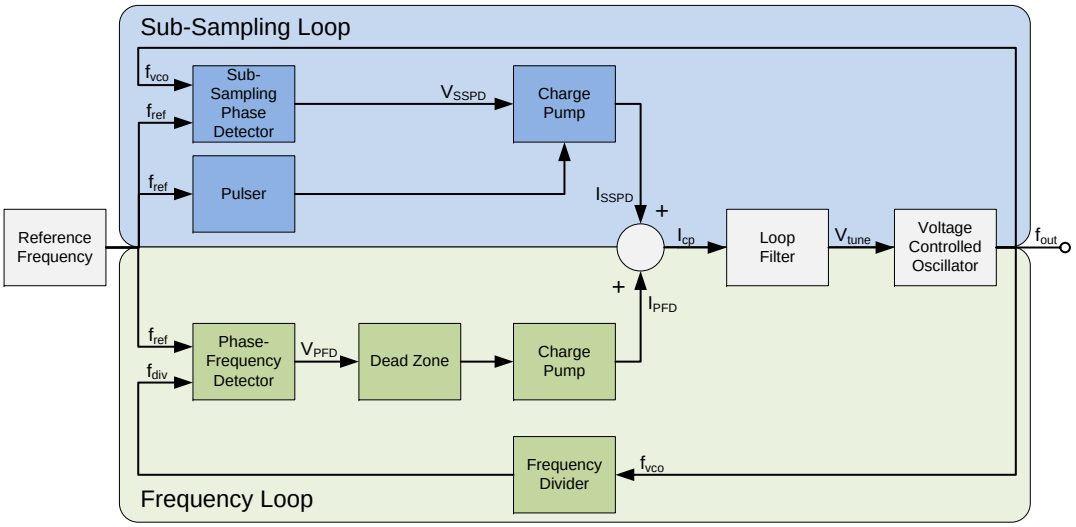


Figure 2.6.: Block schematic of an SSPLL.

2.3.1. Sub-Sampling Phase-Locked Loop Phase Domain Model

The phase domain model for an SSPLL is shown in figure 2.7. The frequency loop is basically a traditional PLL but with a DZ added to the PFD for the reasons mentioned in the previous subsection. The sub-sampling loop contains the SSPD which has the higher gain compared to the traditional PFD and does not require a divider in the feedback path. The loop filter can be the same as used before of which the trans-impedance is given by equation 2.1. Again the second order approximation is applied. The two loop

are simply superimposed to obtain the following transfer function:

$$H(s) = N\frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.12}$$

$$w_n = \sqrt{\frac{(\beta_{pfd} + \beta_{sspd})K_{vco}}{C_1}} \tag{2.13}$$

$$\xi = \frac{R_1}{2}\sqrt{(\beta_{pfd} + \beta_{sspd})K_{vco}C_1} \tag{2.14}$$

$$\beta_{pfd} = \frac{K_{pfd}}{N} = \frac{I_{cp}}{2\pi N} \tag{2.15}$$

$$\beta_{sspd} = K_{sspd} = A_{vco}\frac{2I_{cp}}{V_{od}} \cdot \frac{\tau_{pul}}{T_{ref}} \tag{2.16}$$

Where N is the feedback frequency division factor, ξ the damping factor, ω_n the natural frequency, K_{vco} the VCO tuning gain, β_{pfd} the PFD gain, β_{sspd} the SSPD gain, I_{cp} the charge pump current, A_{vco} the VCO amplitude and V_{od} the SSPD transconductance overdrive voltage.
Because this is a linearised model the DZ is not taken into account. The DZ could be added by making β_{pfd} dependent on the phase difference between the reference and the divided VCO output. The PFD feedback gain would then be as equation 2.8 for phase differences outside the DZ and zero for phase differences inside the DZ.

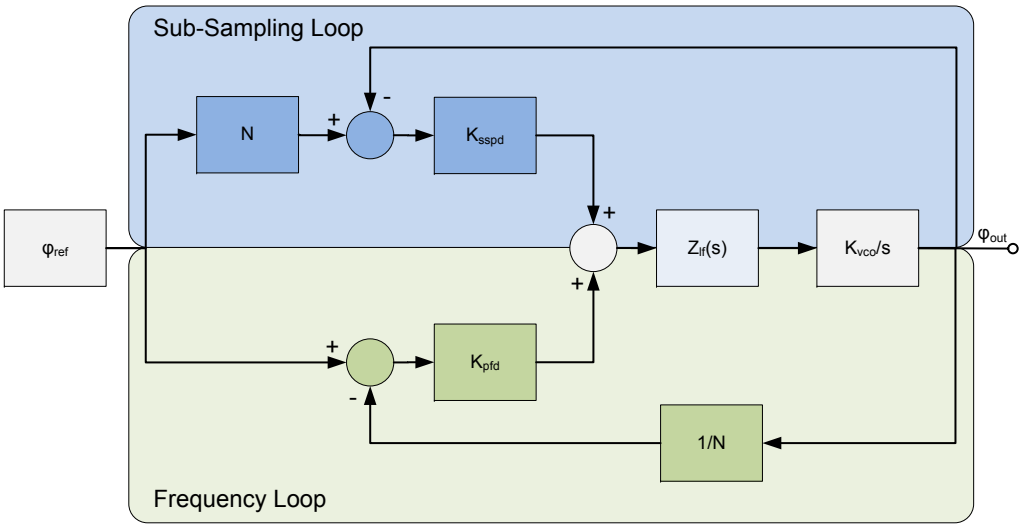


Figure 2.7.: The phase domain model of an SSPLL.

2.3.2. Research Questions About the Sub-Sampling Phase-Locked Loop

The original publication of the SSPLL in [9] reported the lowest PLL FOM at the time. Since then there have been many follow up designs all reporting very low FOMs.

A paper by Hsu et al. [8] suggests that the relock time after a disturbance of the SSPLL could use some improvement, because it "may not be acceptable in many clock synthesis applications". The paper suggest that the relock time after a disturbance of a PLL needs to be in the order of 1 µs though it never mentions a specific target. In one example the SSPLL took 2.5 µs to regain lock where a traditional PFD took 0.4 µs.

In the recommendations of the PhD thesis by Gao [10] a similar comment is found: "In some applications, the PLL settling time is an important specification. In the current design, a classical PLL with dead zone function as the FLL. Having a dead zone during frequency acquisition slows down the PLL settling, which may be problematic. It is worthwhile to investigate the settling behavior of the SSPLL further."

Combined with an internal discussion at the beginning of this thesis the following questions where raised:

> What is the influence of the dead zone in the phase frequency detector on the sub-sampling phase-locked loop dynamic behaviour?
> Specifically, in the event of channel switching or lock perturbation the size of the DZ could influence the PLL settling time.

> Can the robustness to perturbations of the SSPLL design from [9] be improved without removing the dead zone in the phase frequency detector?
> The big advantage of the original SSPLL was its high phase detector gain and therefore low output noise. By removing the PFD DZ the SSPLL robustness is improved at the cost of mitigating the noise advantage.

> Can the dynamic behaviour of the SSPLL design from [9] be improved by optimizing its configuration?
> It is not known whether the parameter value choices of the original SSPLL design took dynamic behaviour into account.

3. Channel Switching Simulations of a Sub-Sampling Phase-Locked Loop

This thesis started by explaining the growing interest in the Sub-Sampling Phase-Locked Loop (SSPLL) dynamic behaviour, because of its crucial role in practical applications. Specifically, a paper published by Hsu et. al. [8] raised the issue of the SSPLL's robustness to perturbations. The proposed solution was to remove the Phase-Frequency Detector (PFD) Dead Zone (DZ) present in the original design from [9]. However, removing the PFD DZ mitigates a large part of the noise benefits that the original SSPLL presented.

In this chapter the goal is to find out more about the dynamic behaviour of SSPLLs through simulation and analysis. The insight gained could lead to an SSPLL implementation that keeps all the noise benefits of the original design, but is also robust to perturbations.

The dynamic behaviour of the SSPLL will be examined in two practically relevant situations:

1. Channel Switching: the output frequency of an SSPLL can be electronically set by changing the feedback division ratio. If the SSPLL was previously locked on a different ratio the output is made to switch from one frequency to another, or one channel to another and it is called channel switching. As was illustrated with a bluetooth example in chapter 1 a PLL that can quickly switch between channels can be very useful.

2. Lock Perturbation: If any charge is injected into a phase-locked SSPLL that causes a loss of that lock, it is called lock perturbation. In case a perturbation is large enough to force the SSPLL out of lock it is of interest to know how fast the SSPLL is able to regain lock so that normal operation of integrated circuit can be resumed.

The reason for using simulations as a research tool instead of trying a fully analytical approach is that PLLs are non-linear time-discrete circuits and therefore difficult to handle mathematically. However, as presented in chapter 2 some approximations can be made to get a linear (SS)PLL model that can for instance be used in the lock situation alongside the simulations to gain insight.

The model used for the simulations will be presented in section 3.1. Section 3.2 will

cover the first channel switching simulations after which section 3.3 will present new analysis based on insight gained from [8] and the first simulations. Section 3.4 will present adjusted channel switching simulations, because of the new insight from section 3.3. There will be intermediate conclusions and the chapter will close with an overall conclusion.

3.1. Simulation Model

In order to find relations between the settling time, Loop BandWidth (LBW) and Loop Gain Ratio (LGR) a Simulink model of a PLL was created. The schematic of the model is shown in figure 3.1. It has been designed to be representative of the design published in [9]. The parameters are set by the script found in appendix A.

The following list clarifies the function of each block in the model:

- The "Reference" block represents the crystal oscillator source and outputs a sine wave with frequency f_{ref} and amplitude A_{ref}.
- The "SubSampling PD" block is a simple sample and hold function that samples "VCO" at the rising edge of "REF".
- The "gm" block is a transconductance equal to the gm.
- The "Pulser" is a block that only passes its I_{cp} input when PUL is high.
- The "Pulse Generator" makes pulses with a width equal to $\frac{\tau_{pul}}{T_{ref}}$ every T_{ref} seconds.
- The block "PFDwDZTrefo2_V1" is a Phase-Frequency Detector with a DZ of $T_{ref}/2$ based on figure 4.13 from [9]. Its implementation is shown in figure 3.2.
- The "Charge Pump" consist of two gain blocks equal to I_{cp} but of opposite sign.
- The "Loop Filter" represents a filter with two poles and a zero that are set by $z1$, $p2$ and $p2$. Subsection 3.1.1 describes the filter design.
- The "perturbation" block enables the injection of a perturbation with amplitude A_{pert}, length W_{pert} and time of occurrence T_{pert}.
- The "Vtune_init" block allows for the setting of an initial offset V_{tune_init} on V_{tune} representing an initial charge on the Loop Filter.
- The "VCOwNoise" block is a Voltage Controlled Oscillator with amplitude A_{vco}, free-running frequency f_{fr}, gain K_{vco} and possibility of adding band-limited white noise S_{vco}.

> The "Zero-Order Hold" block captures the VCO output and sends it to the Matlab workspace. It also sets the simulation step size T_{zoh}.

> The "Divider" block is a phase transparent frequency divider, that is set to divide its input frequency by N.

3.1.1. Design of the Loop Filter

The purpose of the loop filter is to suppress the current pulses coming out of the phase-frequency detector. The simplest implementation for this would be a single capacitor. This proves problematic however, because together with the pure integrator in the VCO the accumulated phase around the loop would be $-180°$ for all frequencies. The Barkhausen criteria say that in this situation loop stability would not be guaranteed.
Therefore a zero should be added to the filter to compensate the phase at the 0 dB open-loop gain crossing to ensure stability. This can be implemented by a resistor in series with the capacitor.

With the correct choice of capacitance and resistance the loop is now stable. However, the high frequency currents from the phase-frequency detector will again cause spikes on the VCO control signal (V_{tune}) due to the resistor, adding phase noise and even spurious tones at the PLL output.
By adding a second pole to the filter far away from the first one, the suppression of high frequencies is increased while only giving up a little phase margin. The resulting loop filter is shown in figure 3.3. The transimpedance of this filter is given by:

$$Z(s) = \frac{V_{out}}{I_{in}} = \frac{1}{C_2} \cdot \frac{(s + \frac{1}{R_1 C_1})}{s(s + \frac{C_1 + C_2}{R_1 C_1 C_2})} \tag{3.1}$$

Because of the expansive knowledge on second order systems and their behaviour, it is beneficial to approximate the PLL as second order instead of trying to analyse the full third order transfer function. This can be done by designing the second filter pole far away from the first by choosing $C_2 \leq \frac{C_1}{5}$.
The loop filter values can now be calculated by using the second order closed loop transfer function of the phase domain model for an SSPLL shown in figure 2.7.

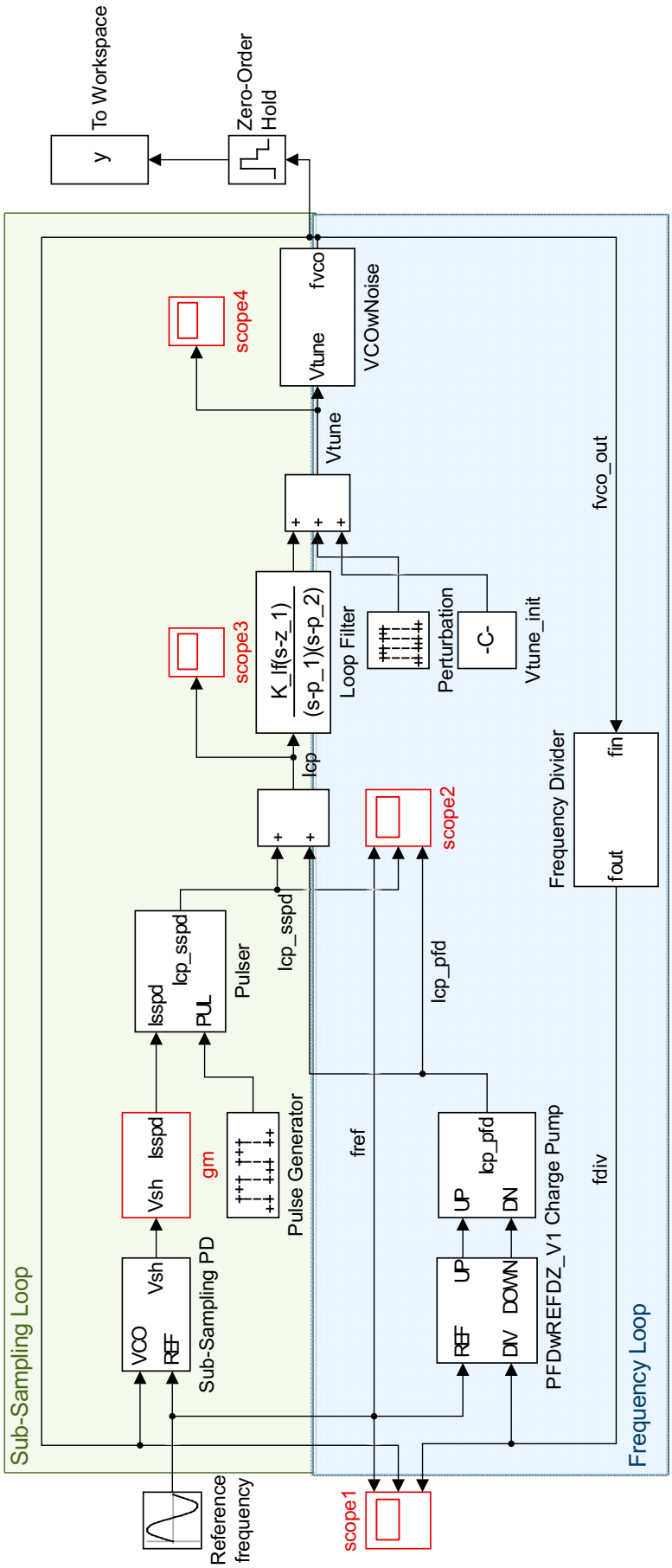


Figure 3.1.: The schematic for the Simulink model with a DZ of $T_{ref}/2$.

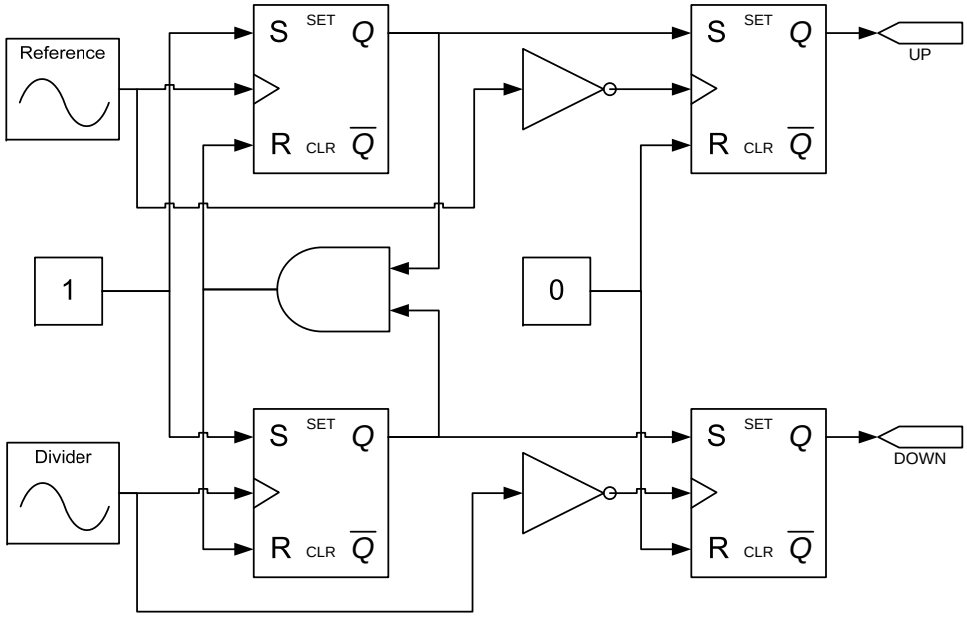


Figure 3.2.: The schematic for the PFD model with a DZ of $T_{ref}/2$.

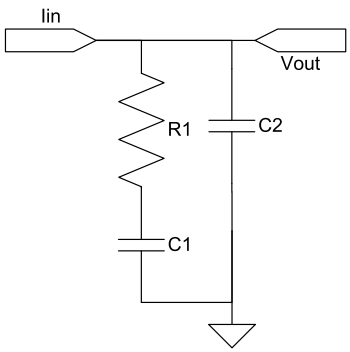


Figure 3.3.: The schematic for the two pole, one zero loop filter.

$$H(s) = N\frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.2}$$

$$w_n = \sqrt{\frac{(\beta_{pfd} + \beta_{sspd})K_{vco}}{C_1}} \tag{3.3}$$

$$\xi = \frac{R_1}{2}\sqrt{(\beta_{pfd} + \beta_{sspd})K_{vco}C_1} \tag{3.4}$$

$$\beta_{pfd} = \frac{I_{cp}}{2\pi N} \tag{3.5}$$

$$\beta_{sspd} = A_{vco}\frac{2I_{cp}}{V_{od}} \tag{3.6}$$

Where N is the feedback frequency division factor, ξ the damping factor, ω_n the natural frequency, K_{vco} the VCO tuning gain, β_{pfd} the PFD gain, β_{sspd} the SSPD gain, I_{cp} the charge pump current, A_{vco} the VCO amplitude and V_{od} the SSPD transconductance overdrive voltage.
K_{vco}, A_{vco} and N are assumed to be determined by the application and therefore not free to choose. Because there are more unknowns than equations β_{sspd}, I_{cp}, V_{od}, ξ and w_n are choices to be made by the designer based on desired performance.
β_{sspd} is chosen high enough for sufficient loop noise suppression. V_{od} is usually chosen to put the transistor comfortably in strong-inversion and saturation for the specific technology node. I_{cp} then results from the choice of β_{sspd} and V_{od}. For the damping factor ξ usually a value close to 1 gives good transient behaviour. For ω_n there is a condition that ensures that the continuous time approximation for the PLL remains valid. The condition is that the loop bandwidth should be much smaller than the input frequency: $2.5\omega_n << \omega_{in}$, where the $2.5\omega_n$ represents the $-3\,\text{dB}$ loop bandwidth of the second order transfer function. A derivation of this bandwidth can be found in section 9.6 from [12]. With these choices made C_1 and R_1 are given by:

$$C_1 = \frac{(\beta_{pfd} + \beta_{sspd})K_{vco}}{\omega_n^2} \tag{3.7}$$

$$R_1 = \frac{2\xi\omega_n}{(\beta_{pfd} + \beta_{sspd})K_{vco}} \tag{3.8}$$

At this point it should be noted that on could define the loop gain in an SSPLL in multiple ways leading to different values. In the phase domain model shown in figure 2.7 the two loop transfers are superimposed. A common way of defining the loop gain would be by taking the derivative of the loop transfer around the lock point. Following this definition the two loop gains around the lock point are simply added and its derivative is taken.
The characteristic of an SSPD is shown in figure 2.5. Due to the sinusoidal output of the VCO, the phase-current transfer of the sub-sampling loop is sinusoidal with a periodicity of 2π in the phase domain or T_{vco} in the time domain.

The phase-current transfer of a PFD without a DZ shown in figure 2.2, has sawtooth shape with a periodicity of 2π in the phase domain or T_{ref} in the time domain.
By combining these two characteristics and characteristic is shown in figure 3.4. After taking the derivative around the lock point a loop gain is obtained. The loop gain from other definitions may lead to more conservative estimates, possibly allowing for a design with better dynamic behaviour. However, by using this definition and resulting optimistic value for the loop gain, loop stability is ensured.

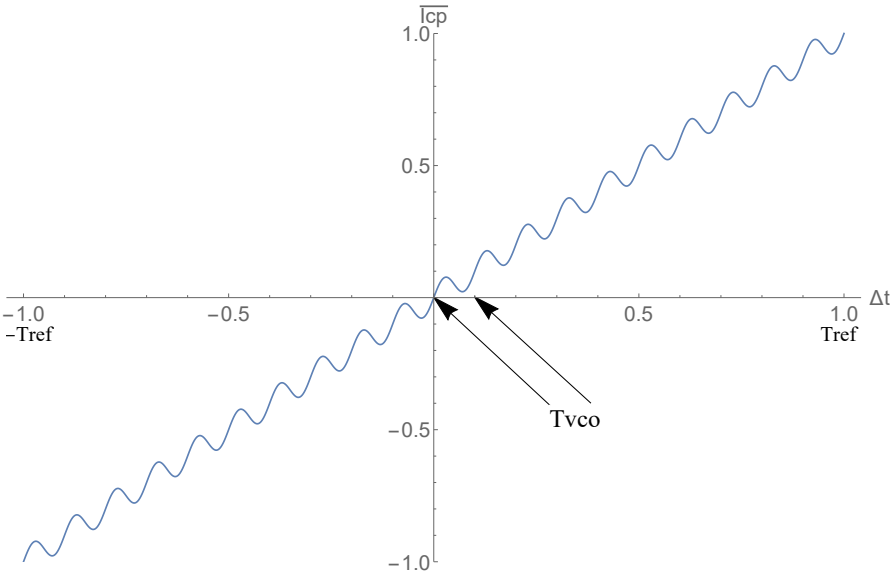


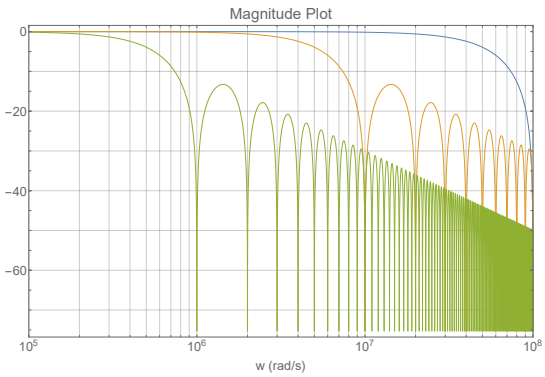
Figure 3.4.: The combined time-current transfer of the sub-sampling and frequency loops without a DZ.

A point that wasn't touched upon in the paper by Gao [9], is the influence of the gain reduction implementation on loop stability.
As explained in section 2.3, the feedback gain should just be high enough to make the charge pump noise negligible. If the feedback gain becomes higher than that point, the loop filter capacitance must become very large for loop stability without gaining any noise benefit. The feedback gain can then be said to be unnecessarily high and should be reduced.
In [9] this was done by adding a pulser block that only turns on the charge pump for a fraction τ_{pul} of the sampling period T_{ref}. This reduces the feedback by a factor $\frac{\tau_{pul}}{T_{ref}}$.
Other gain reduction techniques could be used, such as adjusting the gm. However, if a gain reduction technique is chosen that doesn't significantly shorten the output pulse of the sub-sampling phase detector, the Zero-Order Sample and Hold (ZOSH) effect becomes significant and should be added to the loop transfer. The following equation describes the ZOSH effect as a function of is the input angular velocity ω,

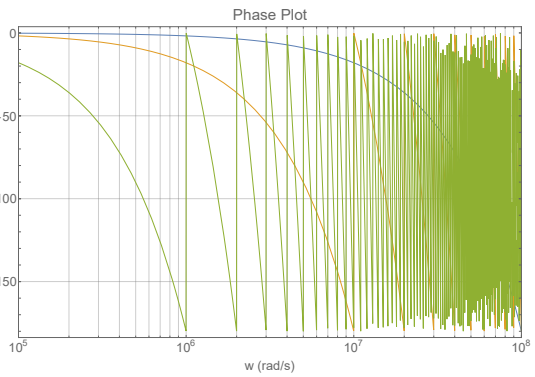
sample frequency $T_s = T_{ref}$ and the hold-pulse width-scaling factor ρ.

$$H_{zosh}(\omega) = \frac{1 - \exp\frac{-j\omega\rho T_s}{2}}{\frac{j\omega\rho T_s}{2}} = \frac{\sin\left(\frac{\omega\rho T_s}{2}\right)}{\frac{\omega\rho T_s}{2}} \cdot \exp\frac{-j\omega\rho T_s}{2} \tag{3.9}$$

For $\rho = 1$ the pulse width is equal to T_s. One can quickly deduce that the transfer function magnitude then contains zeroes at multiples of the sample frequency. This is illustrated by the Mathematica plots 3.5a and 3.5b in which the magnitude and phase are plotted from left to right for $\rho = 1, 0.1, 0.01$. The sample frequency for this example is 1×10^6 rad/s.
For the green plot $\rho = 1$ and the first zero occurs at 1×10^6 rad/s and gives a dip of which the magnitude is limited by the calculation accuracy. The subsequent zeroes are at every multiple of the sample frequency.
The Orange plot shows what happens when $\rho = 0.1$. By making the hold-pulse ten times narrower, the sample frequency is effectively increased by the same amount. This can be seen by observing that the first and subsequent zeroes for the orange graph are at ten times higher angular velocity compared to the green graph.
By increasing ρ again by ten times the blue graph is obtained. As before the sample frequency is effectively also increased tenfold making the zeroes move to ten times higher angular velocities.
All of this is a problem because the VCO output frequency that needs to be sampled is exactly an integer multiple of the reference frequency. Without any loop gain in the lock point there is no loop noise suppression, meaning increased phase noise at the SSPLL output. Because of this effect the gain reduction implementation as used in [9] is likely the best choice for achieving a low PLL FOM.



(a) Magnitude plot of the ZOSH transfer function for $\rho = 1, 0.1, 0.01$.



(b) Phase plot of the ZOSH transfer function for $\rho = 1, 0.1, 0.01$.

3.2. Channel Switching simulations

In this section simulations will be used in order to find out more about the dynamic behaviour of Sub-Sampling Phase-Locked Loops and more specifically the channel switching behaviour. Channel switching is when a PLL is tuned from one output frequency to another by changing the division ratio in the feedback.
The goal of these simulations is to find out how the following SSPLL parameters influence the channel switching behaviour, with an emphasis on the time it takes to regain phase lock:

> Size of the Dead-Zone (DZ): a distinct difference between a classic PLL using a Phase-Frequency Detector (PFD) and an SSPLL is the dual loop structure and the presence of a DZ in the frequency loop. The DZ ensures that in lock the phase noise is determined by the sub-sampling loop. In [8] it is shown that the DZ influences the SSPLL reaction to a perturbation, this section will examine if this is also the case for channel switching behaviour.

> Loop Gain Ratio (LGR): the presence of two loops in an SSPLL and therefore two loop gains, begs the question if there is an LGR that optimises channel switching behaviour. LGR is defined as the ratio between the sub-sampling and the frequency loop feedback gains: $\frac{\beta_{SSPD}}{\beta_{PFD}}$.

> Loop BandWidth (LBW): in most dynamic systems the LBW plays a role in the behaviour. Therefore the relation of the channel switching behaviour with respect to the LBW will be studied.

The simulation model that will be used was introduced in section 3.1. The block schematic and phase domain model of the SSPLL can be found in figures and 2.6 and 2.7.
The rest of the simulation setup will be explained in subsection 3.2.1, followed by the channel switching simulation results and a discussion in subsection 3.2.2. The section will close with a conclusion in subsection 3.2.3.

3.2.1. Channel Switching Simulation Setup

In these channel switching simulations the quantity of interest is the time it takes for the output frequency to settle to within a certain error from the pre-set division ratio. However, because V_{tune} is directly related to the output frequency and an instantaneous frequency is more difficult to determine than a voltage, V_{tune} will be evaluated and give the same information. Using the equation:

$$V_{tune} = \frac{f_{out} - f_{fr}}{K_{VCO}} = \frac{N \cdot f_{ref} - f_{fr}}{K_{VCO}} \tag{3.10}$$

the V_{tune} for a certain multiplication integer N is known. In this simulation $f_{ref} = 50$ MHz, $f_{fr} = 2.2$ GHz, $N = 45$ and $K_{vco} = 50$ MHz/V corresponding to a V_{tune} of 1 V.
The settling time will be the measured quantity and is defined as the time when V_{tune} falls within a chosen boundary of its final value. The maximum simulation time is 25 µs which is more than enough for the PLL to lock, given that the range of interest is sub-10 µs as was explained in chapter 1. If the PLL is not able to lock within that time a settling time of 25 µs will be recorded. By recording 25 µs instead of "no lock" the results can be included in numerical result graphs.
In classic control theory a 2% error limit from the theoretical steady-state value is often used. Due to the similarity of those applications and a PLL the same limit is maintained here.

To find the influence of the DZ on the dynamic behaviour two variations of the model are simulated. In the original model the DZ was $T_{ref}/2$, because this was how it was implemented in [9].
In the publication [8] it was proposed to remove the DZ, because of its negative effect on the robustness to perturbations of the SSPLL. Therefore, the second choice for the DZ is to reproduce the implementation of [8] and remove the DZ.

Proposed SSPLL Robustness Improvement

Although [8] showed that the robustness to perturbations was improved compared to [9], the output phase noise was higher. The idea behind the SSPLL is to use only the SSPD for the phase lock, because of its high detection gain giving lower output phase noise than a traditional PFD. A PFD is used to get the correct frequency lock, because the SSPD cannot distinguish between multiples of the frequency it samples. This means that on its own an SSPD doesn't correct the loop output towards the desired integer multiple of the reference frequency. The DZ is added so that when the correct frequency is locked the noise performance is not degraded by the PFD. Therefore, by removing the DZ entirely a core advantage of the SSPLL is lost.
A compromise between having a DZ of $T_{ref}/2$ and no DZ, is to reduce the size of the DZ without removing it. This should give both the noise benefit of the original SSPLL and

have similar robustness to perturbations as was shown by removing the DZ. Looking again at figure 2.5 shows that the next zero crossing after the lock point is at a phase difference of $T_{vco}/2$. Therefore, choosing the size of the DZ smaller than $T_{vco}/2$ only leaves the desired lock point. To change the size of the PFD DZ shown in figure 3.2 the "CLK" signal of the second flip-flops should be changed. For a DZ of $T_{vco}/2$ the "CLK" signal for the pair of flip-flops on the right-hand side should be changed to the inverted VCO output, instead of "!REF" and "!DIV". This PFD with a DZ of $T_{vco}/2$ is shown in figure 3.6. The changes compared to the PFD with a DZ of $T_{ref}/2$ from figure 3.2 are green. This solution both reduces the size of the DZ providing the mentioned benefits and can be implemented with no additional components using existing signals.

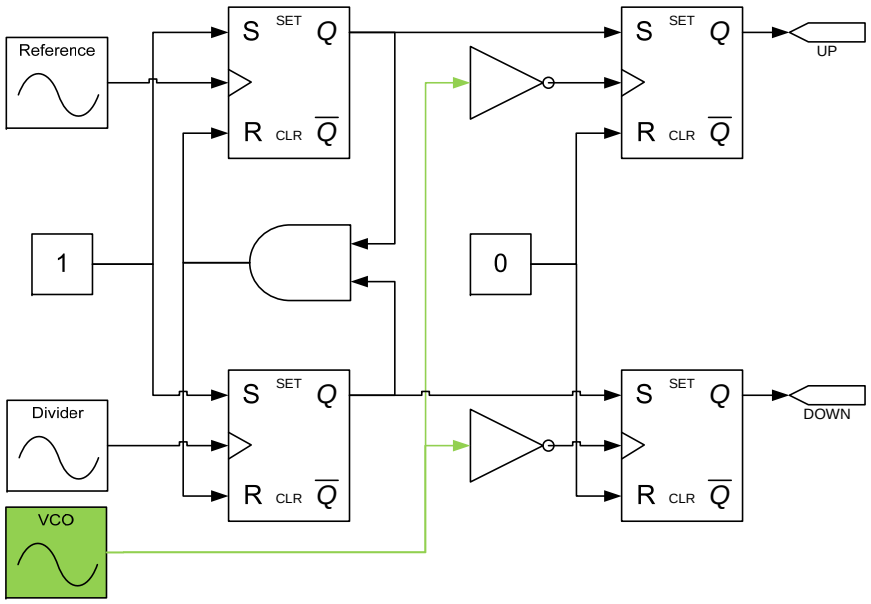


Figure 3.6.: Schematic of a PFD with a DZ of $T_{vco}/2$.

Expectations for the Simulations

Going into the simulations there where no expectations of what effect the DZ or LGR would have on the channel switching behaviour, because there was no theoretical description available or conceived beforehand. The LGR will be varied from 1 to 450 in course steps with the intent of revealing a pattern or relation to the settling time from the simulation results. The simulation will be run with the DZ removed and then with the DZ set to the size of $T_{ref}/2$ and $T_{vco}/2$.
For the effect of LBW a theoretical basis was found in [12] of which a summary is given here:
In [12, Chapter 10.3] an expression is derived that describes when the output frequency

of a PFD-PLL falls within an arbitrary boundary α that indicates a chosen relative frequency error, after switching from one division ratio "N1" to another "N2".:

$$|1 - \frac{N1}{N2}| \cdot (1 - g(t)u(t)) \leq \alpha \tag{3.11}$$

Where g(t) is the time domain closed loop transfer function and u(t) the unit step function. For a type-II integer-N PLL with $\xi \leq 1$, g(t) is given by:

$$g(t) = 1 - [\cos(\sqrt{1-\xi^2}\omega_n t_s) - \frac{\xi}{\sqrt{1-\xi^2}} \sin(\sqrt{1-\xi^2}\omega_n t_s)] \exp^{-\xi\omega_n t_s} \tag{3.12}$$

For the settling time, only the envelope of the signal is important resulting in the following expression for α:

$$|1 - \frac{N1}{N2}| \cdot \sqrt{2} \exp^{-\xi\omega_n t_s} \leq \alpha \tag{3.13}$$

This expression can be rewritten to an expression for the settling time t_s:

$$t_s = \frac{\sqrt{2}}{\omega_n} \log(\frac{\sqrt{2}(1 - \frac{N1}{N2})}{\alpha}) \tag{3.14}$$

Equation 3.14 reveals an inverse relation for t_s with the natural frequency ω_n and therefore with the LBW of the PLL defined as $2.5\omega_n$. A derivation of this bandwidth can be found in section 9.6 from [12].
Using equation 3.14 and substituting the values $N1 = 44$, $N2 = 45$, $LBW = 2\pi 2.50MHz$, $w_n = \frac{LBW}{2.5} = 2\pi 1e6 rad/s$ and $\alpha = 0.02$ the calculated settling time is $t_s = 0.1\mu s$.
The LBW is set to 0.63, 1.25, 2.50 and 5.00 MHz.

Tradional PFD Simulations Result for Comparison

To have a ground for comparison for the upcoming simulations a PLL with a regular PFD is simulated. The schematic of the PFD is shown in figure 3.7. The LBW is set to 2.50 MHz and the simulations were run using the script found in appendix A. This means that the expected tune voltage is 1 V.
The simulated V_{tune} voltage is shown in figure 3.8. The simulation result shows that the tune voltage settles to 1 V with an overshoot going to 1.5 V.

The simulated 2% settling time is 0.81 µs. It turns out that equation 3.14 gives rather optimistic values and that in practice settling times are longer.
It should also be noted that equation 3.14 does not take into account any SSPLL specific parameters like LGR or DZ. Therefore, the predictive value for an SSPLL is likely to be worse.

These results and figure 3.8 can be used as a reference for the result of the upcoming simulations done with the SSPLL.

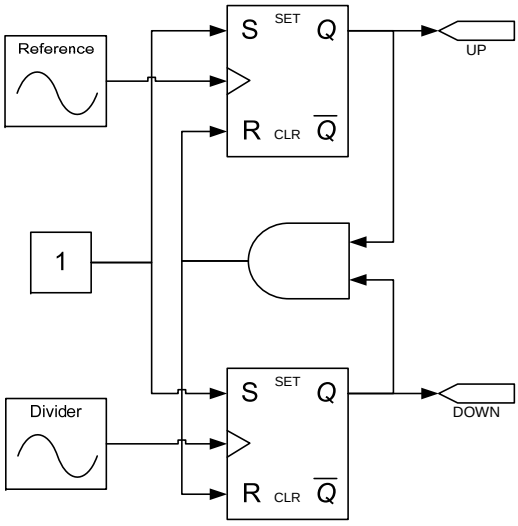


Figure 3.7.: Schematic of a standard PFD.

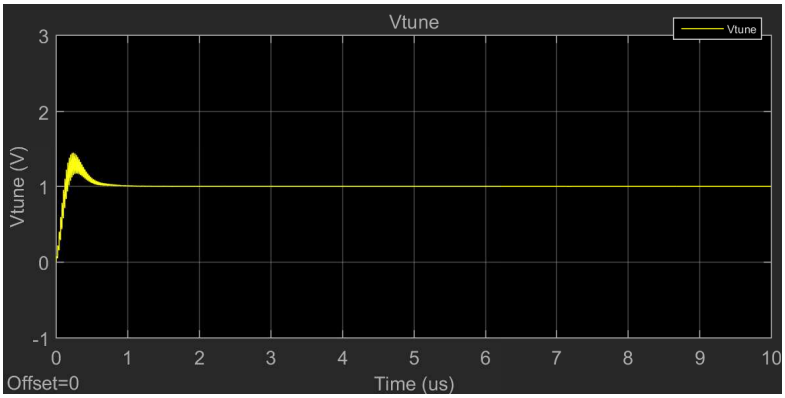


Figure 3.8.: Graph of V_{tune} for a PLL with an LBW of 2.50 MHz.

Simulation Setup Variables Table

The simulation parameters and values are shown in table 3.1.

Table 3.1.: Summary table of the channel switching simulation setup.

Parameter	**Value(s)**												
f_{ref} (Hz)	50e6												
A_{ref} (V)	0.5												
f_{fr} (Hz)	2.2e9												
A_{vco} (V)	0.5												
K_{vco} (Hz/V)	50e6												
N1	44												
N2	45												
f_{out} (Hz)	2.25e9												
V_{tune} (V)	1												
I_{cp} (A)	20e-6												
V_{od} (V)	200e-3												
ξ	1												
A_{pert} (V)	0.5												
Type of the DZ	linear	binary											
Size of the DZ	none	$T_{ref}/2$	$T_{vco}/2$										
LGR	1	25	50	75	100	125	150	200	250	300	350	400	450
LBW (Hz)	0.63e6	1.25e6	2.50e6										

3.2.2. Channel Switching Simulation Results and Discussion

The simulations were run using the script found in appendix A. The recorded settling times are shown in figure 3.9, 3.14 and 3.12.
The y-axis in the graphs indicates the settling time in µs. The x-axis covers the range of LGRs that were simulated. The various LBWs are indicated by different colors and shapes shown in the legend on the right of the graphs.
For reference, an example of the simulated V_{tune} for a correctly locking PLL is shown in figure 3.8.

Phase-Frequency Detector With a Dead Zone of $T_{ref}/2$

Looking at the simulation results shown in figure 3.9, the fastest settling times for an SSPLL with a DZ of $T_{ref}/2$ are at an LGR of 25.
For comparison to the traditional PFD, the simulated V_{tune} for an LGR of 25 and LBW of 2.50 MHz is shown in figure 3.10. Compared to figure 3.8 the response is a lot slower.

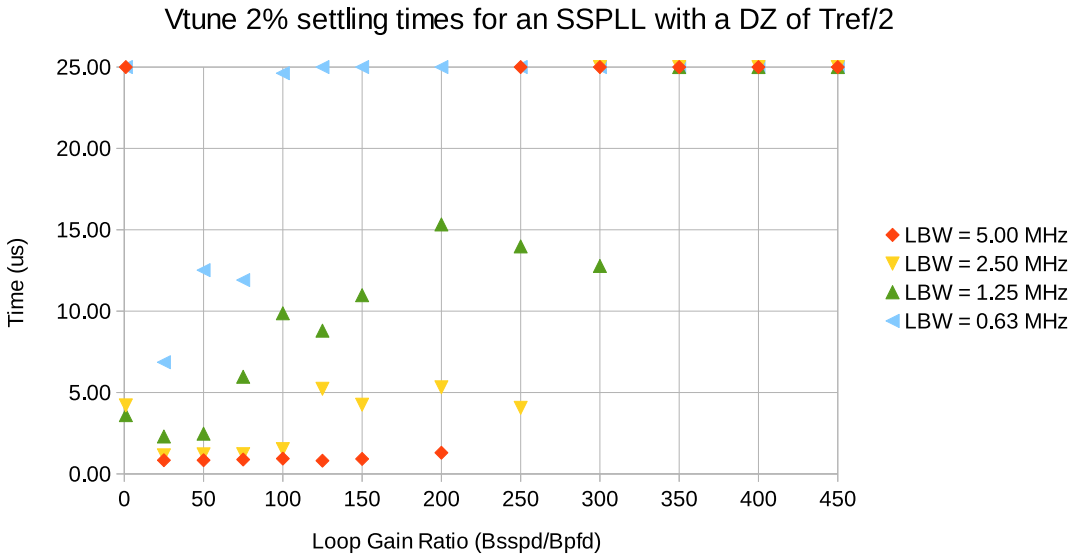


Figure 3.9.: The 2% V_{tune} settling times of an SSPLL with a DZ of $T_{ref}/2$ versus loop gain ratios.

For an LGR of 1 and LBW of 0.63 and 5.00 MHz the PLL does not achieve lock within 25 µs. The graphs of V_{tune} for LBW is 0.63 MHz is shown in figure 3.11. It can be seen that the loop overshoots the 1 V target. Looking closely at V_{tune}, after overshooting the target some sinusoidal activity can be seen. This activity comes from the sub-sampling loop that is unable to pull the loop to any nearby voltage corresponding to an integer

lock. The frequency loop takes a very long time react. When it finally does react, it overshoots the 1 V target again and the story repeats. The same goes for LBW is 5.00 MHz.

Looking again at figure 3.9 there is a trend for longer settling times as the LGR gets higher. The results also reveal that for an SSPLL with a DZ of $T_{ref}/2$ the LGR should at least be lower than 300, because the SSPLL then fails to lock at any LBW. In the region between LGR 1 and 100 the SSPLL locks with every LBW, though some results are almost 25 µs.

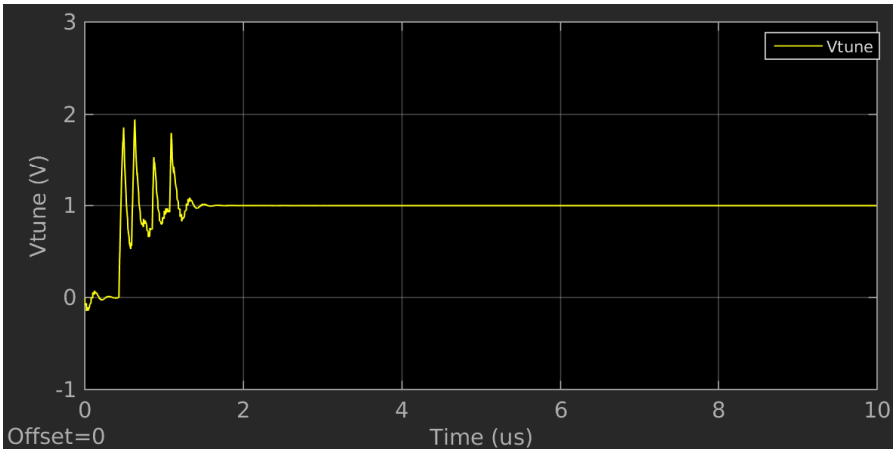


Figure 3.10.: Graph of V_{tune} for an SSPLL with a DZ of $T_{ref}/2$, LGR of 25 and LBW of 2.50 MHz.

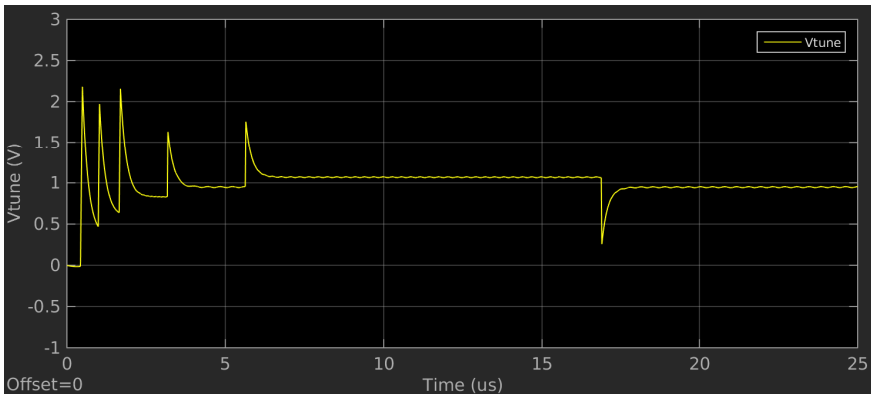


Figure 3.11.: Graph of V_{tune} for an SSPLL with a DZ of $T_{ref}/2$, LGR of 1 and LBW of 0.63 MHz.

Phase-Frequency Detector Without a Dead Zone

The channel switching simulation results for the PFD without DZ are shown in figure 3.12. For the SSPLL without a DZ the lowest settling times are at an LGR of 1.
Compared to 3.8 the simulated graph of V_{tune} shown in figure 3.13 is very similar. An important difference is that there are some minor ripples on the final voltage. The severity of these ripples became less after decreasing the simulation step time. It is therefore believed that these ripples are due imprecision if the simulation. By removing the DZ the lock point of both loops has to be exactly the same. Otherwise there could be a back and forth between two very similar, but not identical lock points. With more computing power this imperfection could be studied further.

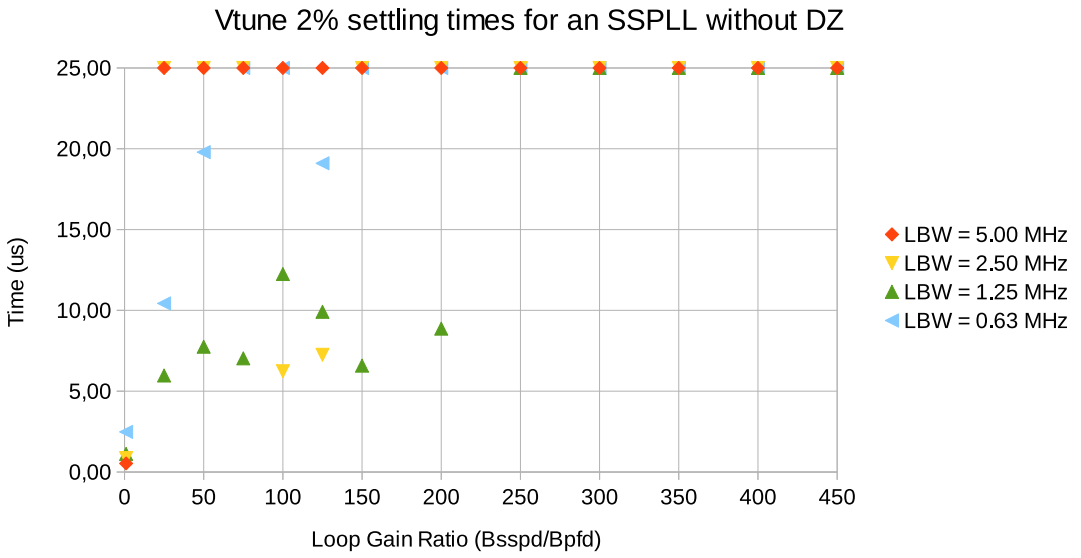


Figure 3.12.: The 2% V_{tune} settling times of an SSPLL without a DZ versus loop gain ratios.

Above LGR 1 the results are inconsistent, but unlike for the DZ of $T_{vco}/2$ it is hard to say whether those points represents situations where the SSPLL does not lock correctly. This is because the final V_{tune} already contains a lot of remaining activity due to the lack of DZ.

From the results in figure 3.12 it is concluded that for an SSPLL without a DZ the LGR should at least not exceed 200, because there are no more locked results above that. There is not a very clear trend visible from the results, because there are so many points were the SSPLL failed to lock within 25 µs. There is an optimum around LGR equal to 1.

Phase-Frequency Detector With a Dead Zone of $T_{vco}/2$

In figure 3.14 the results are shown for the SSPLL with a DZ of $T_{VCO}/2$. The lowest settling times are at an LGR of 1. The graph of V_{tune} for a LGR of 1 and LBW of 2.50 MHz is shown in figure 3.15.
Compared to figure 3.8 the response is slower, but again due to the DZ the final voltage has no remaining PFD activity. Compared to figure 3.10 the response is faster.

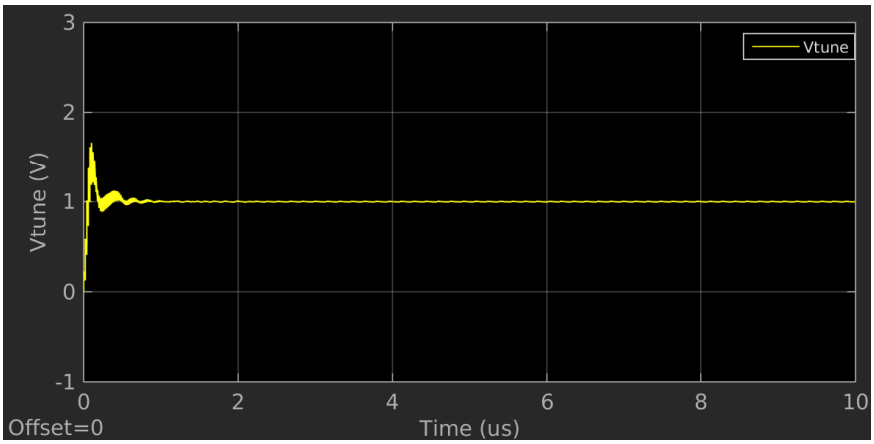


Figure 3.13.: Graph of V_{tune} for an SSPLL without DZ, LGR of 1 and LBW of 2.50 MHz.

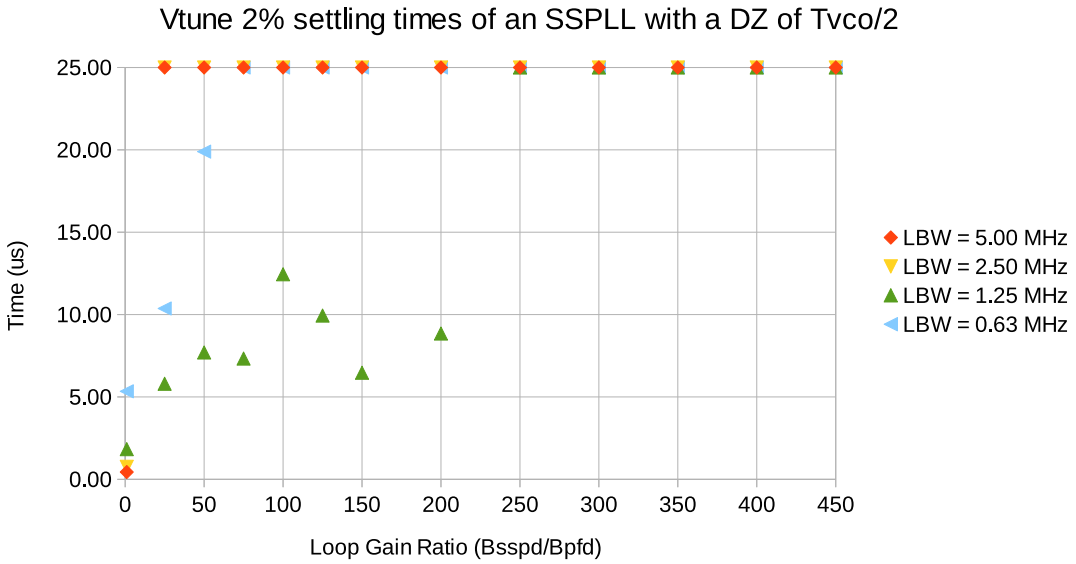


Figure 3.14.: The 2% V_{tune} settling times of an SSPLL with a DZ of $T_{vco}/2$ versus loop gain ratios.

Only for LBW equal to 1.25 MHz and 0.63 MHz there are results that lock within 25 µs for an LGR higher than 1. Zooming in on the final voltage for LGR is 50 and a LBW of 2.50 MHz shown in figure 3.16, it can be seen that the final voltage shows activity despite the presence of a DZ. This means that the SSPLL is not actually locked correctly. This also goes for all other points with LGR higher than 1.

For an SSPLL with a DZ of $T_{vco}/2$ only LGR 1 works for all frequencies and also shows the fastest settling times. There are so few correctly locked simulation results available that it is impossible to draw any meaningful conclusion about a trend.

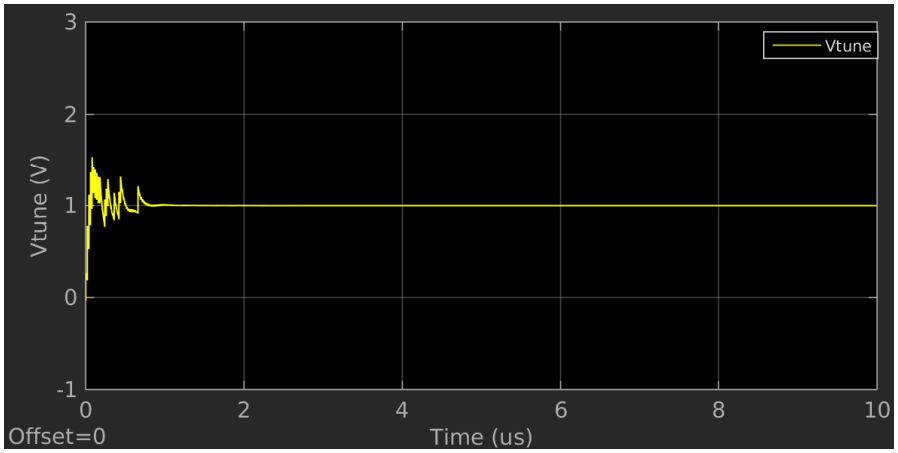


Figure 3.15.: Graph of V_{tune} for an SSPLL with a DZ of $T_{vco}/2$, LGR of 1 and LBW of 2.50 MHz.

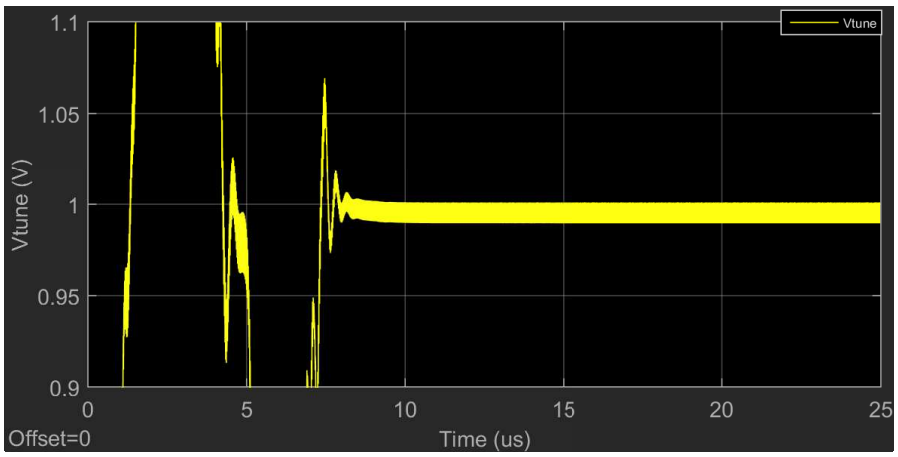


Figure 3.16.: Zoomed graph of V_{tune} for an SSPLL with a DZ of $T_{vco}/2$, LGR of 50 and LBW of 1.25 MHz.

3.2.3. Preliminary Conclusion About the Channel Switching Simulations

So far it has become clear that the LBW has an inverse relation with the settling time and that a higher LGR either breaks the SSPLL or makes the settling time longer. Only in the case of an SSPLL with a DZ of $T_{ref}/2$, an LGR higher than 1 lowered the settling time.
In figure 3.17 the fastest simulations settling times for the different DZs are shown. The graph seems to suggest that the relation between the DZ and settling time is that a bigger DZ has slower settling behaviour. The graph also shows the theoretical settling time that was discussed in subsection 3.2.1. As stated previously, the theory underestimates the settle time. The match to the simulation results without a DZ could be improved by multiplying equation 3.14 by 6.

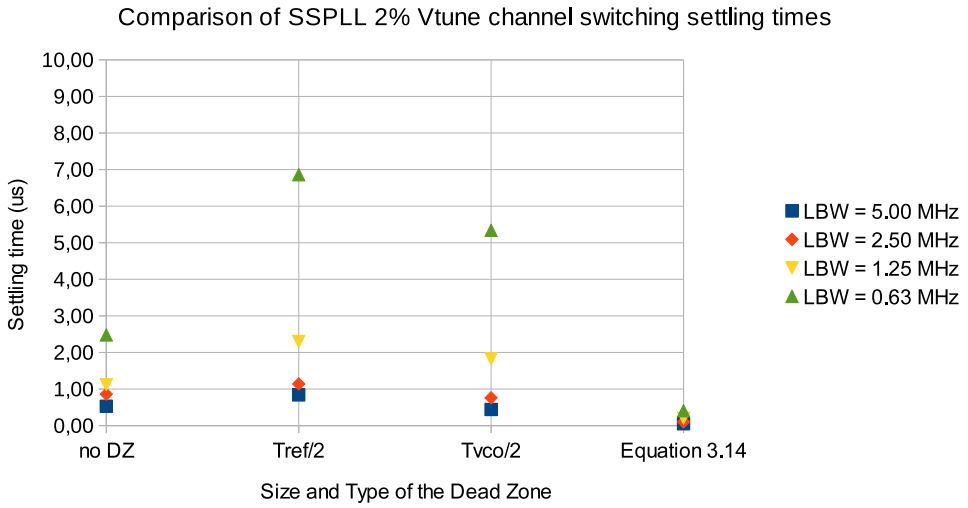


Figure 3.17.: Graph comparing the settling times for the different DZs.

The simulations showed that the 2% limit taken from classical control theory to measure the settling time turns out to be too big, because it doesn't exclude some wrong lock points. The settling limit needs to be adjusted for further simulations.

Upon further reading of [8], the paper also noted a maximum current relation between the two loops in an SSPLL. This next section will expand upon this to derive a maximum for the LGR.
Another insight was that the PFD with DZ as used by [9] and shown in figure 3.2 is not linear, but binary due to the second pair of flip-flops not being reset. The consequences of this will also be discussed in the next section. In section 3.4 a linear PFD with DZ will be proposed to see if it shows any benefits with regard to dynamic behaviour compared to the binary PFD with DZ used previously.

3.3. Loop Gain Ratio Analysis

From the results of the settling simulations a rough insight evolved into what the relations between LGR, LBW and DZ are. However a theoretical explanation is still lacking. The block schematic of an SSPLL can be found in figure 2.6 and its phase domain model in figure 2.7.

In [8] a relation between the average current of the sub-sampling and frequency loop is given to ensure proper control action of the combined loop. In the paper it is argued that the time-current transfer function of the sub-sampling and frequency loop has to be superimposed to get the combined transfer. While it is more common to look at the phase-current transfer of a PLL, in this case the time-current transfer gives the better picture. The SSPLL is unique in that it has two loops that operate with different frequencies. The frequency loop operates using the reference and divided VCO output. However, the sub-sampling loop operates using the reference and direct VCO output. This difference means that 2π has a different meaning in the two loops. The frequency loop defines 2π as a period of the reference T_{ref}. The sub-sampling loop defines 2π as a period of the VCO T_{vco}. Using the conventional phase-current transfer would be confusing because it would be unclear what the meaning of 2π phase difference would indicate. By going to the time domain this ambiguity is solved.
The time-current transfer of the individual linear PFD without DZ from figure 2.2 and SSPD from figure 2.5, are shown in figure 3.18 and 3.19. The combined time-current transfer is shown in figure 3.20. For the purpose of illustration the feedback division factor N is equal to 10 in this section.

The paper goes on to say that in order to ensure that only one lock point exists, this combined transfer should have positive average current output for positive time differences and negative average current output for negative time differences. In this way the combined characteristic is able to control the loop to the right integer frequency. As explained in chapter 2 the SSPD alone does not have this property, precisely because its characteristic does not have this sign continuity for positive or negative phase/time differences. Together with expressions for the average output currents of the SSPD and PFD $\overline{I_{sspd}}$ and $\overline{I_{pfd}}$ from [9], this results in the following equations that need to be satisfied to maintain the proper control action in an SSPLL:

$$\overline{I_{sspd}} + \overline{I_{pfd}} \geq 0 \tag{3.15}$$

$$-\overline{I_{sspd}} \leq \overline{I_{pfd}} \tag{3.16}$$

$$\overline{I_{sspd}} = A_{vco} \cdot \frac{2I_{cp}}{I_{cp}} \sin(\Delta\phi_{vco}) \frac{\tau_{pul}}{T_{ref}} \tag{3.17}$$

$$\overline{I_{pfd}} = \frac{I_{cp}}{2\pi} \Delta\phi_{div} \tag{3.18}$$

Where $\overline{I_{sspd}}$ and $\overline{I_{pfd}}$ are the average output currents of the SSPD and PFD, A_{vco} the VCO output amplitude, I_{cp} the charge pump current amplitude, V_{od} the transconduc-

tance overdrive voltage and τ_{pul} the gain reduction pulse duration.

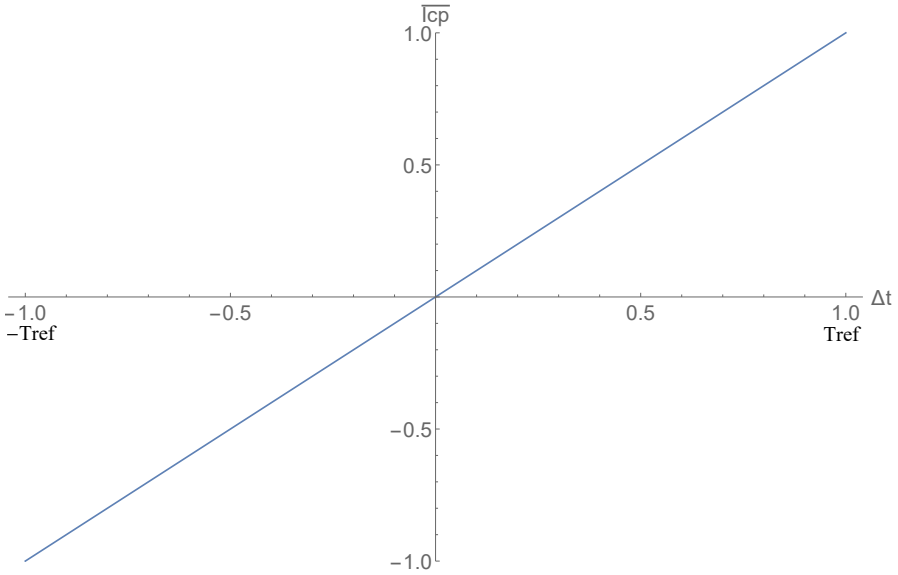


Figure 3.18.: The time-current transfer of the frequency loop without a DZ.

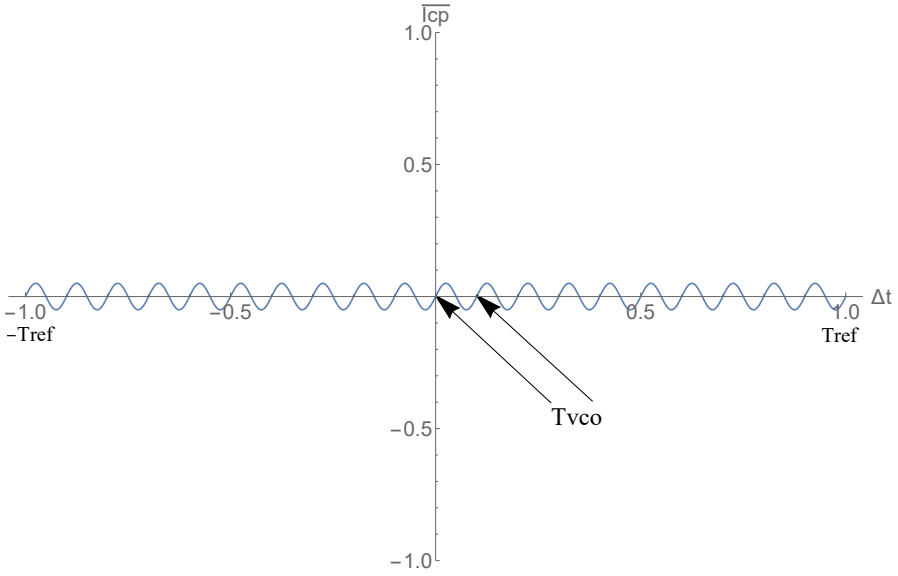


Figure 3.19.: The time-current transfer of the sub-sampling loop.

Using this information a theoretical limit for the LGR can be derived. Because in [8] there is no DZ this case will be treated first and then be expanded upon to the cases

with a DZ. For all analysis in this section it is assumed that:

$$T_{ref} = N \cdot T_{vco} \tag{3.19}$$

$$\Delta\phi_{div} = \Delta t \cdot \omega_{ref} = \Delta t \cdot \frac{2\pi}{T_{ref}} = \Delta t \cdot \frac{2\pi}{N \cdot T_{vco}} \tag{3.20}$$

$$\Delta\phi_{vco} = \Delta t \cdot \omega_{vco} = \Delta t \cdot \frac{2\pi}{T_{vco}} = \Delta t \cdot \frac{2\pi \cdot N}{T_{ref}} \tag{3.21}$$

Where $\Delta\phi_{div}$ is the phase difference and Δt the time difference between the zero-crossing of the reference frequency and divided VCO frequency, ω_{ref} the angular frequency of the reference, T_{ref} the reference period, ϕ_{vco} is the phase difference between the reference frequency and VCO frequency, ω_{vco} the angular frequency of the VCO and T_{vco} the VCO period.

3.3.1. Loop Gain Ratio Boundary for a linear PFD without a Dead Zone

For correct operation of the SSPLL the sign of the time-current characteristic of the combined loop, must be positive for a positive time difference and negative for a negative time difference. Looking at figure 3.20 it can be seen that for an SSPLL without a DZ the boundary of this condition is found when the time difference $\Delta t = \frac{3}{4}T_{vco}$. At that time difference the sinusoidal transfer of the SSPD is at its first minimum starting from

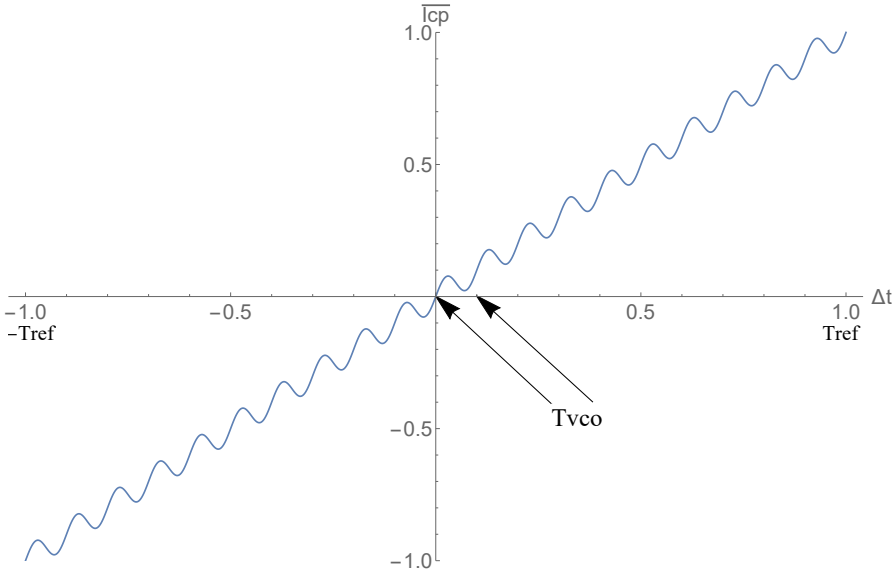


Figure 3.20.: The combined time-current transfer of the sub-sampling and frequency loops without a DZ.

the lock point. Using this data and equation 3.16 the following relations are derived:

$$\Delta t = \frac{3}{4}T_{vco} = \frac{3}{4N}T_{ref} \tag{3.22}$$

$$\Delta\phi_{div} = \frac{3}{4N}2\pi \tag{3.23}$$

$$\Delta\phi_{vco} = \frac{3}{4}2\pi \tag{3.24}$$

$$-\overline{I_{sspd}} \leq \overline{I_{pfd}} \tag{3.25}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{I_{cp}} \sin(\Delta\phi_{vco}) \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{2\pi}\Delta\phi_{div} \tag{3.26}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \sin(\frac{3}{4} \cdot 2\pi) \cdot \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{2\pi}\frac{3}{4N}2\pi \tag{3.27}$$

$$\frac{\tau_{pul}}{T_{ref}} \leq \frac{3V_{od}}{8NA_{vco}} \tag{3.28}$$

Equation 3.28 represents the maximum gain reduction factor for correct operation of the dual loop structure. With this equation the maximum LGR can be derived, where β_{sspd} and β_{pfd} represent the sub-sampling and frequency loop open loop gains from [9]:

$$\beta_{pfd} = \frac{I_{cp}}{2\pi N} \tag{3.29}$$

$$\beta_{sspd} = A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \frac{\tau_{pul}}{T_{ref}} \tag{3.30}$$

$$LGR = \frac{\beta_{sspd}}{\beta_{pfd}} = \frac{A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \frac{\tau_{pul}}{T_{ref}}}{\frac{I_{cp}}{2\pi N}} \tag{3.31}$$

$$LGR_{max} = \frac{A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \frac{3V_{od}}{8NA_{vco}}}{\frac{I_{cp}}{2\pi N}} = \frac{3\pi}{2} \approx 4.7 \tag{3.32}$$

3.3.2. A Linear Phase-Frequency Detector with Dead Zone of $T_{ref}/2$

Before moving on to analyse the LGR for a linear PFD with a DZ, its design is proposed as shown in figure 3.21. To make the binary PFD from figure 3.2 linear, a reset should be added to the second flip-flops. This reset should simply be the same as is used for the first pair of flip-flops. Like before, to make the DZ $T_{vco}/2$ the "CLK" signal of the second flip-flops should be the inverted VCO output. This is shown in figure 3.22 the changes are coloured green.

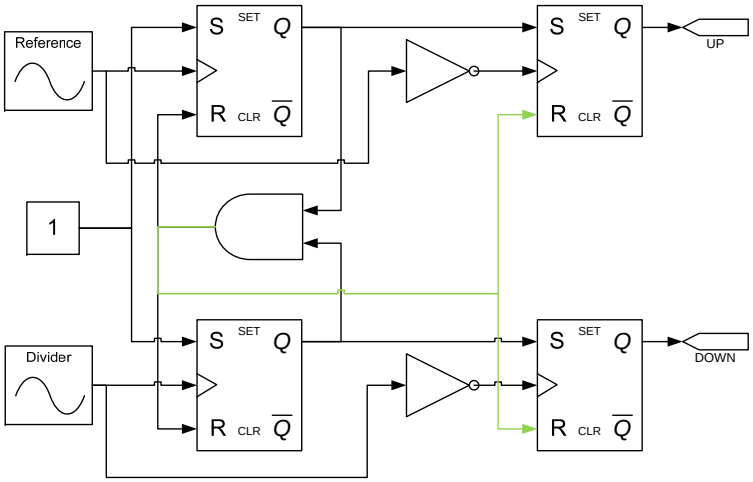


Figure 3.21.: Schematic of the linear PFD with DZ of $T_{ref}/2$.

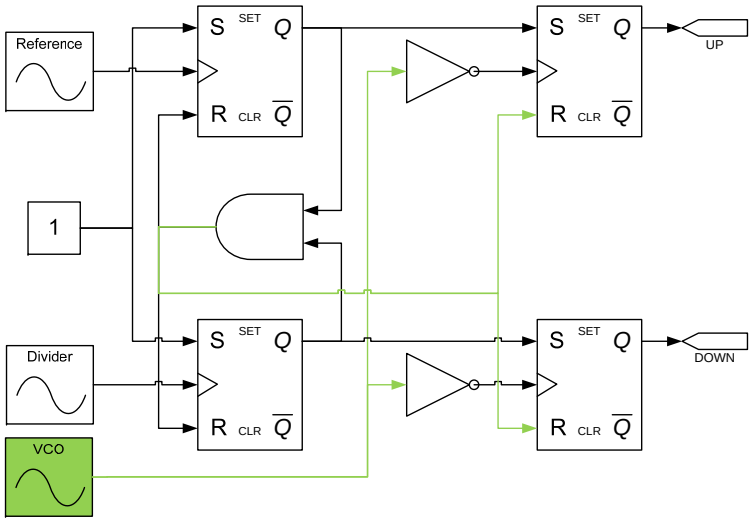


Figure 3.22.: Schematic of the linear PFD with DZ of $T_{vco}/2$.

3.3.3. Loop Gain Ratio Boundary for a linear PFD with a Dead Zone

Now the same derivation can be done using the linear PFD with DZ of $T_{ref}/2$ shown in figure 3.21. The introduction of a DZ of $T_{ref}/2$ changes the PFD time-current transfer as shown in figure 3.23.
The PFD now only produces an output current when the time difference is greater than $T_{ref}/2$. This also means that the PFD effectively loses half of its maximum average output current $\frac{I_{cp}}{2}$. Combining this new PFD transfer with the SSPD transfer from figure 3.19, the combined time-current transfer with a linear PFD DZ of $T_{ref}/2$ is shown in figure 3.24. This means that the time difference when the control condition from

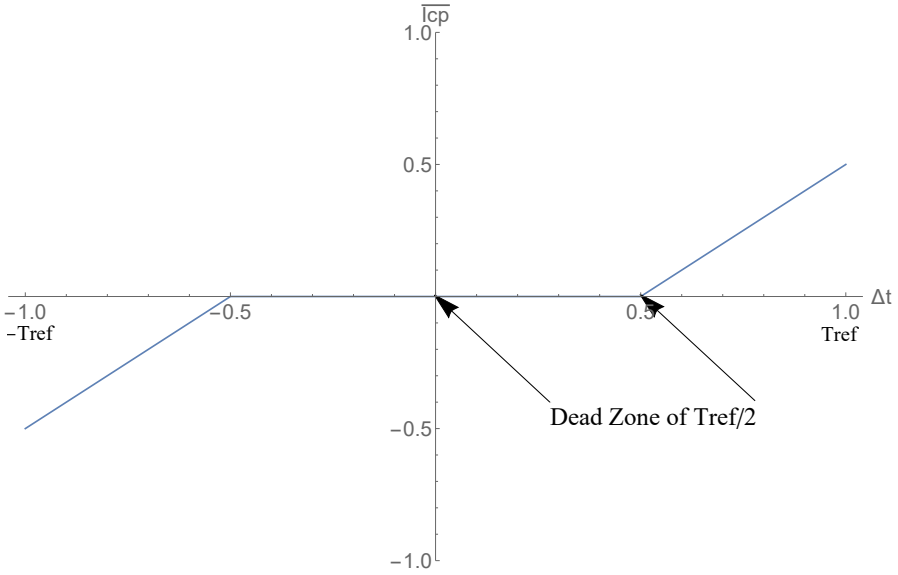


Figure 3.23.: The time-current transfer of the frequency loop with a linear PFD with DZ of $T_{ref}/2$.

equation 3.16 should be evaluated is now $\Delta t = \frac{3}{4}T_{vco} + \frac{T_{ref}}{2}$ when the division ratio N is even, because this time-difference is where the SSPD transfer has its first minimum outside of the DZ. The assumption is still that $T_{ref} = N \cdot T_{vco}$ leading to the following equations:

$$\Delta t = \frac{3}{4}T_{vco} + \frac{T_{ref}}{2} = T_{vco}(\frac{3}{4} + \frac{N}{2}) = T_{ref}(\frac{3}{4N} + \frac{1}{2}) \tag{3.33}$$

$$\Delta\phi_{div} = (\frac{3}{4N} + \frac{1}{2})2\pi \tag{3.34}$$

$$\Delta\phi_{vco} = (\frac{3}{4} + \frac{N}{2})2\pi \tag{3.35}$$

$$-\overline{I_{sspd}} \leq \overline{I_{pfd}} \tag{3.36}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \sin(\Delta\phi_{vco}) \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{2\pi}\Delta\phi_{div} - \frac{I_{cp}}{2} \tag{3.37}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \sin((\frac{3}{4} + \frac{N}{2}) \cdot 2\pi) \cdot \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{2\pi}(\frac{3}{4N} + \frac{1}{2})2\pi - \frac{I_{cp}}{2} \tag{3.38}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \sin(\frac{3}{4} \cdot 2\pi) \cdot \frac{\tau_{pul}}{T_{ref}} \leq \frac{3I_{cp}}{4N} \tag{3.39}$$

$$\frac{\tau_{pul}}{T_{ref}} \leq \frac{3V_{od}}{8NA_{vco}} \tag{3.40}$$

Where $\sin(\frac{N}{2}2\pi) = 0$ is used.
The value for the maximum gain reduction factor is the same results as in equation 3.28. Therefore the maximum LGR is also the same $\frac{3\pi}{2} \approx 4.7$ as equation 3.32.
For N is odd the time difference should be changed to $\Delta t = \frac{1}{4}T_{vco} + \frac{T_{ref}}{2}$, because of the sinusoidal nature of the SSPD. The $\overline{I_{pfd}}$ now becomes three times lower resulting in a three times lower maximum gain reduction factor $\frac{\tau_{pul}}{T_{ref}}$ and LGR $\frac{\pi}{2} \approx 1.6$.

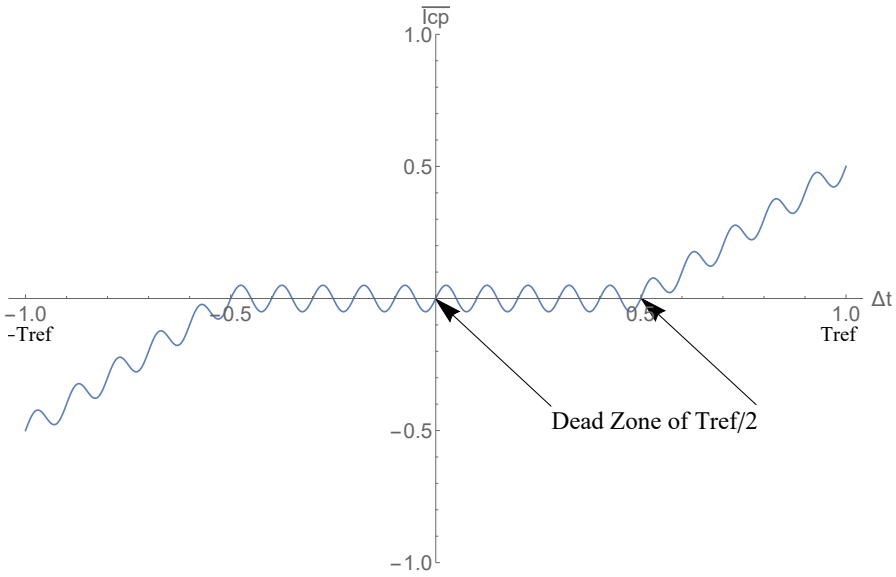


Figure 3.24.: The combined time-current transfer of the sub-sampling and frequency loops with a linear PFD with DZ of $T_{ref}/2$.

Dead Zone of $T_{vco}/2$

If the DZ is reduced to $T_{vco}/2$ as in figure 3.22, the PFD only produces an output current when the time difference is greater than $T_{vco}/2$. This means that the starting point for the analysis is now $T_{vco}/2$ instead of $T_{ref}/2$. The SSPD characteristic now has its first minimum outside of the DZ at $\Delta t = \frac{1}{4}T_{vco} + \frac{1}{2}T_{vco}$. The loss of average output current in the PFD due to the DZ of $T_{vco}/2 = T_{ref}/(2N)$ is now $\overline{I_{pfd}} = \frac{I_{cp}}{2\pi}\Delta\phi_{div} = \frac{I_{cp}}{2\pi}\frac{\pi}{N} = \frac{I_{cp}}{2N}$. This gives the following derivation of the maximum gain reduction factor:

$$\Delta t = \frac{1}{4}T_{vco} + \frac{1}{2}T_{vco} = \frac{3}{4}T_{vco} = \frac{3}{4N}T_{ref} \tag{3.41}$$

$$\Delta\phi_{div} = \frac{3}{4N}2\pi \tag{3.42}$$

$$\Delta\phi_{vco} = \frac{3}{4}2\pi \tag{3.43}$$

$$-\overline{I_{sspd}} \leq \overline{I_{pfd}} \tag{3.44}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \sin(\Delta\phi_{vco}) \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{2\pi}\Delta\phi_{div} - \frac{I_{cp}}{2N} \tag{3.45}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \sin(\frac{3}{4}2\pi) \cdot \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{2\pi}\frac{3}{4N}2\pi - \frac{I_{cp}}{2N} \tag{3.46}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \sin(\frac{3}{4}2\pi) \cdot \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{4N} \tag{3.47}$$

$$\frac{\tau_{pul}}{T_{ref}} \leq \frac{V_{od}}{8NA_{vco}} \tag{3.48}$$

This gain reduction factor is three times less than equation 3.28. The maximum LGR for a SSPLL with a linear PFD with a DZ of $T_{vco}/2$ is therefore $\frac{\pi}{2}$ for N is both even and odd.

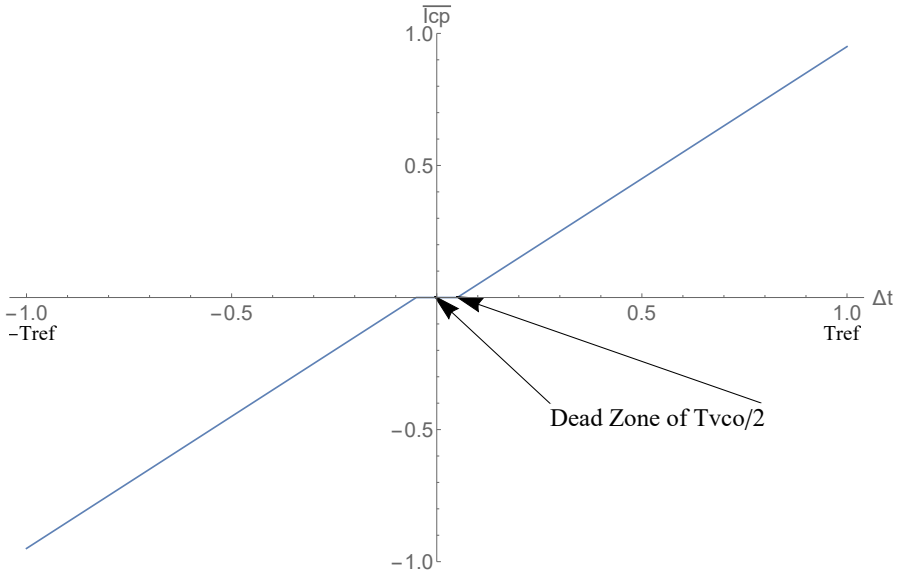


Figure 3.25.: The time-current transfer of the frequency loop with a linear PFD with DZ of $T_{vco}/2$.

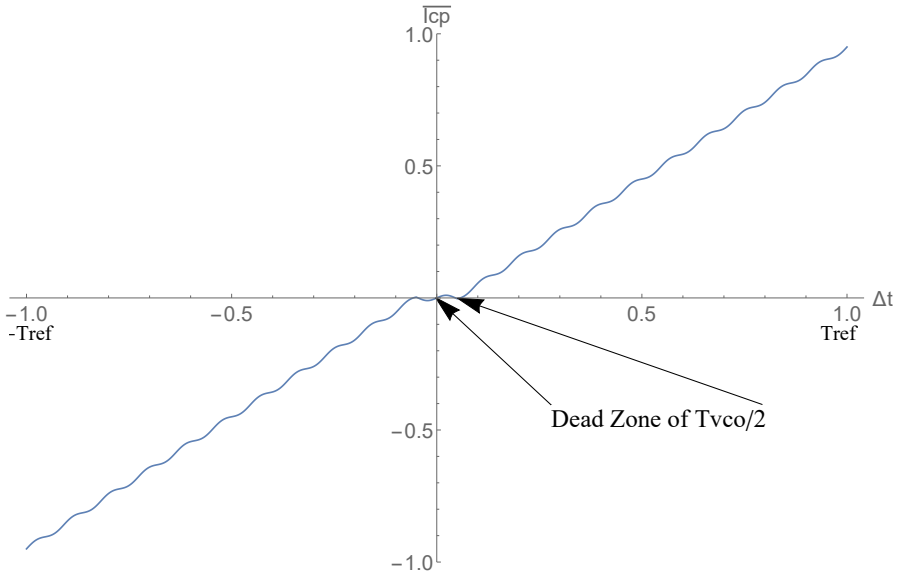


Figure 3.26.: The combined time-current transfer of the sub-sampling and frequency loops with a linear PFD with DZ of $T_{vco}/2$.

3.3.4. Loop Gain Ratio Boundary for a binary PFD with a Dead Zone

The PFD with DZ of $T_{ref}/2$ as described in [9] is not linear but binary as shown in figure 3.2, because the second flip-flops are never reset. This causes the current output to not increase linearly to its maximum of I_{cp} when the time difference is greater than $T_{ref}/2$. Instead the output current is maximum for all time differences greater than $T_{ref}/2$. The time-current transfer for this binary PFD is shown in figure 3.28.

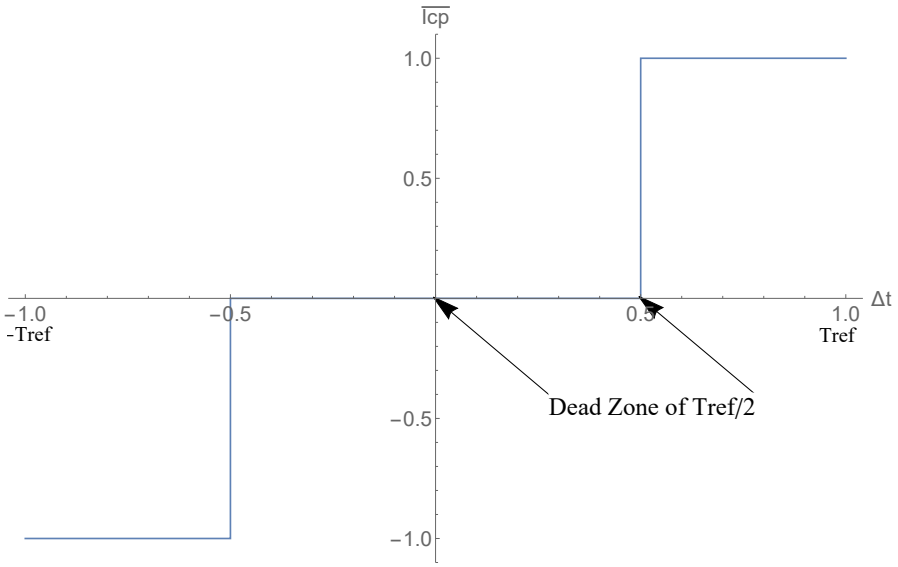


Figure 3.27.: The time-current transfer of the frequency loop with a PFD with binary DZ of $T_{ref}/2$.

To find the maximum gain reduction factor the right-hand side of equation 3.16 now changes to I_{cp}, instead of $\frac{I_{cp}}{2\pi}\Delta\phi_{div} - \frac{I_{cp}}{2}$ in case of the linear PFD with a DZ of $T_{ref}/2$ (eq. 3.37).
This also means that there is no more difference between even and odd N. That is, because no matter at what time difference the SSPD characteristic has its minimum outside of the DZ, the average current output of the PFD is maximum. Therefore, the time difference at which to evaluate the average output current from the SSPD remains the same at $\Delta t = \frac{3}{4}T_{vco} + \frac{T_{ref}}{2}$.

$$\Delta t = \frac{3}{4}T_{vco} + \frac{T_{ref}}{2} = T_{vco}(\frac{3}{4} + \frac{N}{2}) = T_{ref}(\frac{3}{4N} + \frac{1}{2}) \tag{3.49}$$

$$\Delta\phi_{div} = (\frac{3}{4} + \frac{N}{2})2\pi \tag{3.50}$$

$$\Delta\phi_{vco} = (\frac{3}{4N} + \frac{1}{2})2\pi \tag{3.51}$$

$$-\overline{I_{sspd}} \leq \overline{I_{pfd}} \tag{3.52}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \sin(\Delta\phi_{vco}) \frac{\tau_{pul}}{T_{ref}} \leq I_{cp} \tag{3.53}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \sin((\frac{3}{4} + \frac{N}{2}) \cdot 2\pi) \cdot \frac{\tau_{pul}}{T_{ref}} \leq I_{cp} \tag{3.54}$$

$$\frac{\tau_{pul}}{T_{ref}} \leq \frac{V_{od}}{2A_{vco}} \tag{3.55}$$

Because this result for $\frac{\tau_{pul}}{T_{ref}}$ is different from equation 3.28 the maximum LGR is also different:

$$LGR = \frac{\beta_{sspd}}{\beta_{pfd}} = \frac{A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \frac{\tau_{pul}}{T_{ref}}}{\frac{I_{cp}}{2\pi N}} \tag{3.56}$$

$$LGR_{max} = \frac{A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \frac{V_{od}}{2A_{vco}}}{\frac{I_{cp}}{2\pi N}} = 2\pi N \tag{3.57}$$

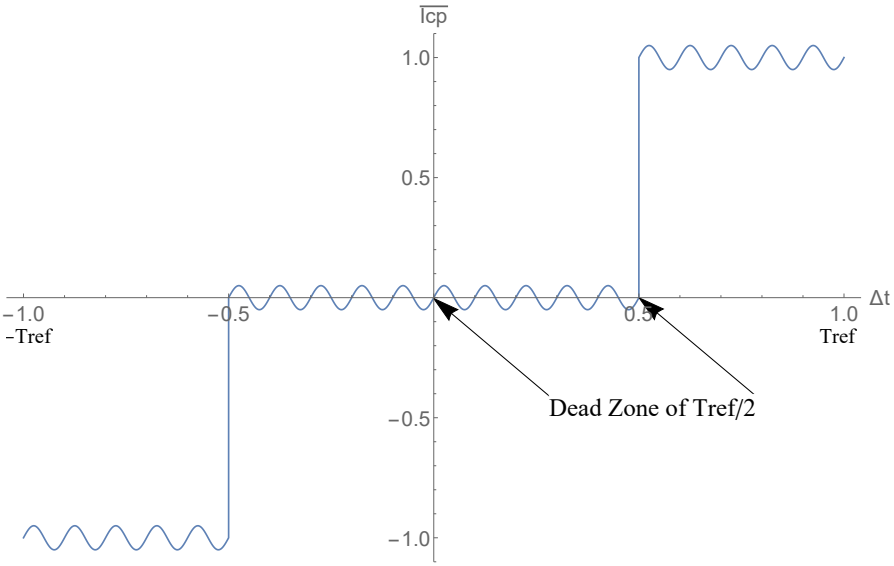


Figure 3.28.: The time-current transfer of the frequency loops with a binary PFD with DZ of $T_{ref}/2$.

Dead Zone of $T_{vco}/2$

The size of the DZ is decreased to $T_{vco}/2$ by clocking the right-hand side pair of flip-flops with the inverted VCO output in figure 3.2 as shown in figure 3.6. The changes are shown in green. The time-current transfer of the binary PFD with a DZ of $T_{vco}/2$ is shown in figure 3.29.
Because the second pair of flip-flops is not reset, the average output current of the PFD can now only change every T_{vco} seconds of time difference. Therefore if the time difference is only just longer than the DZ $T_{vco}/2$, the average output current will be $\overline{I_{pfd}} = I_{cp} \cdot \frac{T_{vco}}{T_{ref}}$. In other words, the time-current transfer is now a stair case with minimal step size $\frac{I_{cp}}{N}$ assuming $\frac{T_{vco}}{T_{ref}} = \frac{1}{N}$. The combined time-current transfer is shown in figure 3.30.

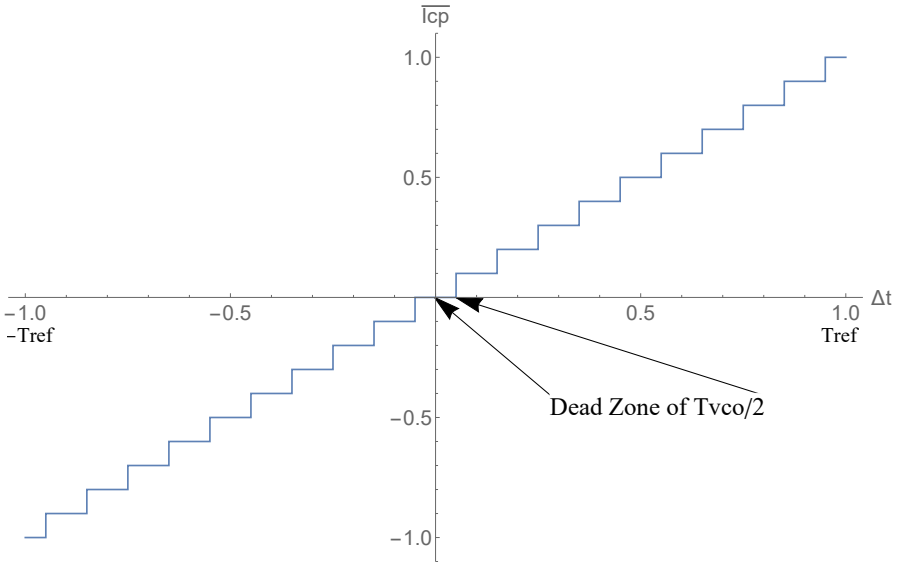


Figure 3.29.: The time-current transfer of the frequency loop with a binary PFD with DZ of $T_{vco}/2$.

The derivation for the maximum gain reduction factor then becomes:

$$\Delta t = \frac{1}{4}T_{vco} + \frac{1}{2}T_{vco} = \frac{3}{4}T_{vco} = \frac{3}{4N}T_{ref} \tag{3.58}$$

$$\Delta\phi_{div} = \frac{3}{4N}2\pi \tag{3.59}$$

$$\Delta\phi_{vco} = \frac{3}{4}2\pi \tag{3.60}$$

$$-\overline{I_{sspd}} \leq \overline{I_{pfd}} \tag{3.61}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \sin(\Delta\phi_{vco}) \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{N} \tag{3.62}$$

$$-A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \sin(\frac{3}{4}2\pi) \cdot \frac{\tau_{pul}}{T_{ref}} \leq \frac{I_{cp}}{N} \tag{3.63}$$

$$\frac{\tau_{pul}}{T_{ref}} \leq \frac{V_{od}}{2NA_{vco}} \tag{3.64}$$

From which the maximum LGR for a binary PFD with a DZ of $T_{vco}/2$ can be determined:

$$LGR = \frac{\beta_{sspd}}{\beta_{pfd}} = \frac{A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \frac{\tau_{pul}}{T_{ref}}}{\frac{I_{cp}}{2\pi N}} \tag{3.65}$$

$$LGR_{max} = \frac{A_{vco} \cdot \frac{2I_{cp}}{V_{od}} \cdot \frac{V_{od}}{2NA_{vco}}}{\frac{I_{cp}}{2\pi N}} = 2\pi \approx 6.28 \tag{3.66}$$

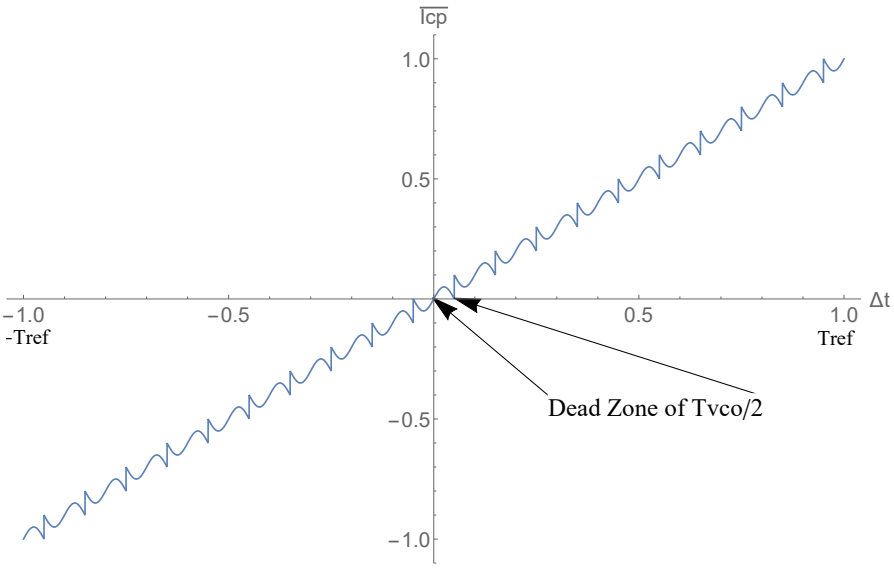


Figure 3.30.: The combined time-current transfer of the sub-sampling and frequency loops with a binary PFD with DZ of $T_{vco}/2$.

3.3.5. Summary of the Loop Gain Ratio Analysis

In this section the control loop current equation for an SSPLL (eq. 3.16) from [8], was used to derive an equation for the maximum Loop Gain Ratio of an SSPLL with and without a Dead Zone. To the author's knowledge, the important difference in the outcome of these equations between even and odd division ratios N was not mentioned in [8].

Table 3.2 summarizes the calculated maximum LGRs from this section.

Table 3.2.: Summary of the calculated maximum LGRs for an SSPLL.

Parameter	**Value**				
Type of DZ	Linear			Binary	
Size of DZ	none	$T_{ref}/2$	$T_{vco}/2$	$T_{ref}/2$	$T_{vco}/2$
LGR_{max} for even N	$\frac{3\pi}{2}$	$\frac{3\pi}{2}$	$\frac{\pi}{2}$	$2\pi N$	2π
LGR_{max} for odd N	$\frac{3\pi}{2}$	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$2\pi N$	2π

The analysis from this section suggests that an SSPLL with a binary PFD, correct locking is possible with a higher LGR than with a linear PFD. A possible benefit of this could be to reduce the power consumption of the frequency loop, achieving a lower PLL FOM with the frequency loop always turned on.
In [9] part of the reason for the low FOM, was that the frequency loop was turned off once the SSPLL was locked. In [8] it is noted that this is impractical, because it reduces the SSPLL robustness to perturbations.
Reducing the frequency loop power consumption allows for the frequency loop to remain on without affecting the PLL FOM too much.
However, so far the simulation results have shown that a high LGR does not benefit the channel switching speed of an SSPLL.

The next section will repeat the channel switching simulations, but with different parameters to check the theory presented in this section. It will also be interesting to see if using a linear or binary PFD makes a difference in the simulated settling times.

3.4. Channel Switching Simulations - Continued

With the new found theoretical basis for the LGR the simulations should be redone to check the predicted maximum LGRs from section 3.3. Also, the previous simulations intentionally had a big step size in the LGR, because it was unclear what the expected outcome would be. Now that there is a potential theoretical basis for the LGR, the LGR step size can be reduced.
With the new linear PFD the channel switching simulations will be redone in subsection 3.4.2. Like before the section will close with a comparison of the simulation results.

The goal of these simulations is the same as in section 3.2: to find out how the following SSPLL parameters influence the channel switching behaviour, with an emphasis on the time it takes to regain phase lock. An added goal is to confirm the proposed theory from section 3.3 and if using a linear or binary PFD makes a difference in the simulated settling times.

3.4.1. Channel Switching Simulation Setup - Continued

The simulations were run using the script found in appendix A.
This time the simulations are now run with five different PFD DZs: without a DZ, linear DZ of T_{ref}, linear DZ of T_{vco}, binary DZ of T_{ref} and a binary DZ of T_{vco}.
In order to zoom in on the proposed theoretical limit from section 3.3, the LGR is now varied from 1 to 20.
The LBW is set to 0.63, 1.25, 2.50 and 5.00 MHz.

Another change from before is the settling limit. The 2% was taken from classical control theory, but is actually way to big of a margin in the context of PLLs to have a correct indication of lock. This was a problem in the interpretation of the previous results, as there where some incorrect locking points among them. This was explained in subsubsection 3.2.2 and shown in figure 3.16. To avoid this the new reduced settling limit will be 0.1%.

Expectations for the Simulations

From the previous results the expectation is that a smaller DZ corresponds to faster settling times. The expectation for the LBW is still that it has an inverse relation to the settling time.
For the LGR the expectations can now be based on the theory proposed in section 3.3. The maximum LGRs for which the SSPLL has a single lock point are shown in table 3.2. The expectation here is that every simulation with an LGR higher than the corresponding value from table 3.2 has multiple lock points and could therefore fail to

lock to $V_{tune} = 1V$. If there are correctly locking results for LGR higher than the calculated maximum it does not directly disprove the theory presented in section 3.3. The prediction is that it only means the SSPLL configuration and simulation settings where such that it happened to lock to the correct integer. Even though according to the theory from section 3.3 there are multiple lock points. By changing the simulation condition slightly for these cases it could be shown that a different lock is achieved. An example of an easy small change, is to change the LGR by 1. Another possibility is to inject a voltage into V_{tune}. By following this approach it can be shown that the theory from section 3.3 is at least not wrong.

Simulation Setup Variables Table

The simulation parameters and values are shown in table 3.3.

Table 3.3.: Summary table of the channel switching simulation setup.

Parameter	**Value(s)**						
f_{ref} (Hz)	50e6						
A_{ref} (V)	0.5						
f_{fr} (Hz)	2.2e9						
A_{vco} (V)	0.5						
K_{vco} (Hz/V)	50e6						
N1	44						
N2	45						
f_{out} (Hz)	2.25e9						
V_{tune} (V)	1						
I_{cp} (A)	20e-6						
V_{od} (V)	200e-3						
ξ	1						
A_{pert} (V)	0.5						
Type of the DZ	linear	binary					
Size of the DZ	none	$T_{ref}/2$	$T_{vco}/2$				
LGR	1	2	3	4	5	10	20
LBW (Hz)	0.63e6	1.25e6	2.50e6	5.00e6			

3.4.2. Channel Switching Simulation Results and Discussion - Continued

The recorded settling times are shown in figure 3.31, 3.37, 3.38, 3.33 and 3.35.
The y-axis in the graphs indicates the settling time in µs. The x-axis covers the range of LGRs that were simulated. The various LBWs are indicated by different colors and shapes shown in the legend on the right of the graphs.
For reference, an example of the simulated V_{tune} for a correctly locking PLL is shown in figure 3.8.

Linear Phase-Frequency Detector Without a Dead Zone

The channel switching simulation results for an SSPLL with a linear PFD without a DZ are shown in figure 3.31. The calculated maximum LGR for this type and size of DZ is $3\pi/2$.
There are a number of data points with LGR higher than $LGR = 4.7$. The theory says that for these LGRs there exist multiple locking points including the correct one. It is possible that the correct locking point was entered by "accident" and that a change in simulation parameters or a perturbation can showcase other unwanted locking points. By changing the LGR by only 1, other lock points could be shown.
In figure 3.32 the zoomed graph V_{tune} is shown for LGR equal to 9 and LBW is 5.00 MHz. This is only 1 different from the simulation for LGR is 10 with the same LBW. By making this small change the SSPLL no longer locks to the correct integer. This shows that there is more than one lock point for LGR is 9. By making minor changes in simulation conditions, the same can be shown for the other points with LGR higher than 4.7.

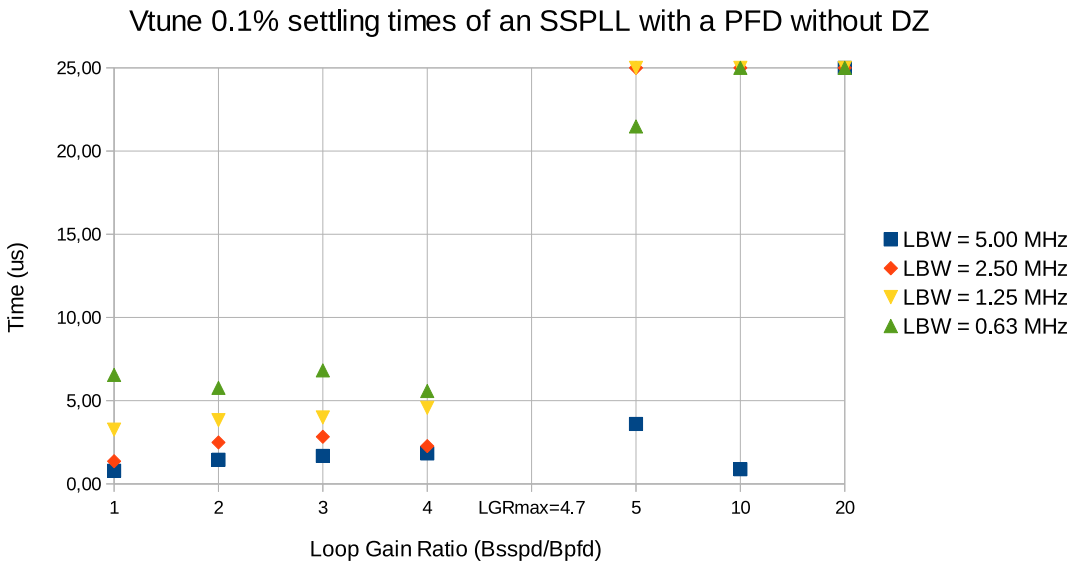


Figure 3.31.: The 0.1% V_{tune} settling times of an SSPLL without a DZ versus loop gain ratios.

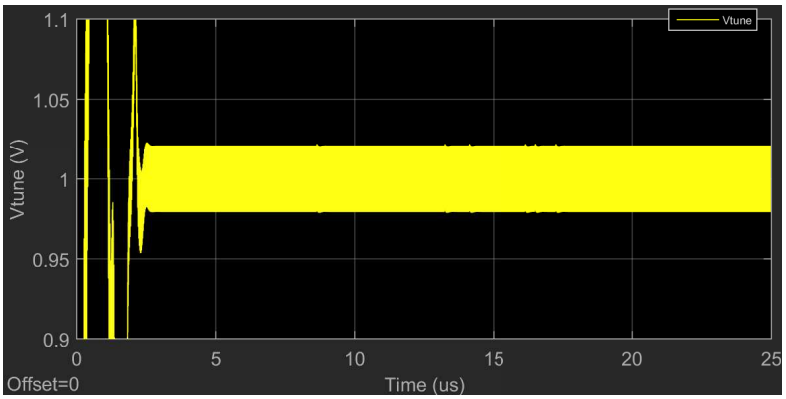


Figure 3.32.: The zoomed graph of V_{tune} for a PFD without DZ LGR 9 and LBW 5.00 MHz.

Linear Phase-Frequency Detector with a Dead Zone of $T_{ref}/2$

The channel switching simulation results for an SSPLL with a linear PFD with a DZ of $T_{ref}/2$ are shown in figure 3.33. The calculated maximum LGR for this type and size of DZ is $3\pi/2$ for N is even and $\pi/2$ for N is odd, with $N = 45$ for these simulations. Looking at figure 3.33 there are a couple of correctly locking results for LGR is 10 and 20. This time by injecting a disturbance an incorrect lock point can be exposed as is shown in figure 3.34 for LGR is 10 and LBW 1.25 MHz. Minor changes in simulation conditions can show the same for the other points with LGR higher than 1.6.

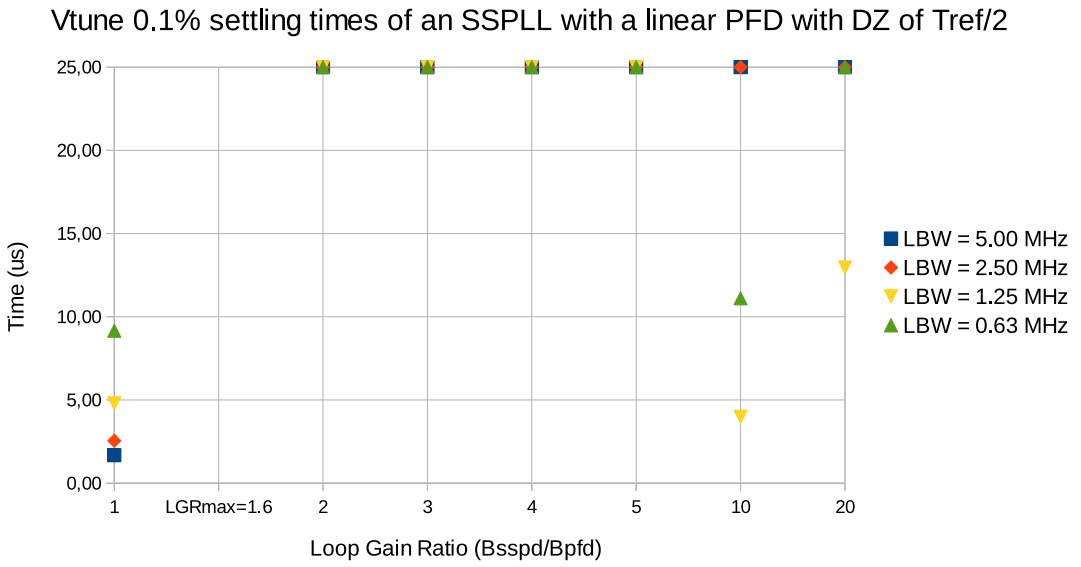


Figure 3.33.: The 0.1% V_{tune} settling times of an SSPLL with a linear PFD with DZ of $T_{ref}/2$ versus loop gain ratios.

Linear Phase-Frequency Detector with a Dead Zone of $T_{vco}/2$

The channel switching simulation results for an SSPLL with a linear PFD with a DZ of $T_{vco}/2$ are shown in figure 3.35. The calculated maximum LGR for this type and size of DZ is $\pi/2$.
The results in figure 3.35 show multiple points that fall outside the expectations. By injecting the same disturbance as before it can again be shown that these configurations do indeed suffer from multiple lock points. This is illustrated in figure 3.36 for an LGR of 2 and LBW 1.25 MHz.

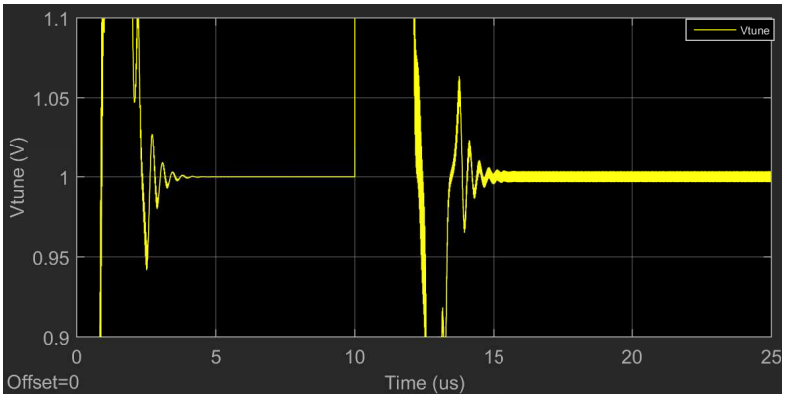


Figure 3.34.: The zoomed graph of V_{tune} for a linear PFD with DZ $T_{ref}/2$ LGR 10 and LBW 1.25 MHz.

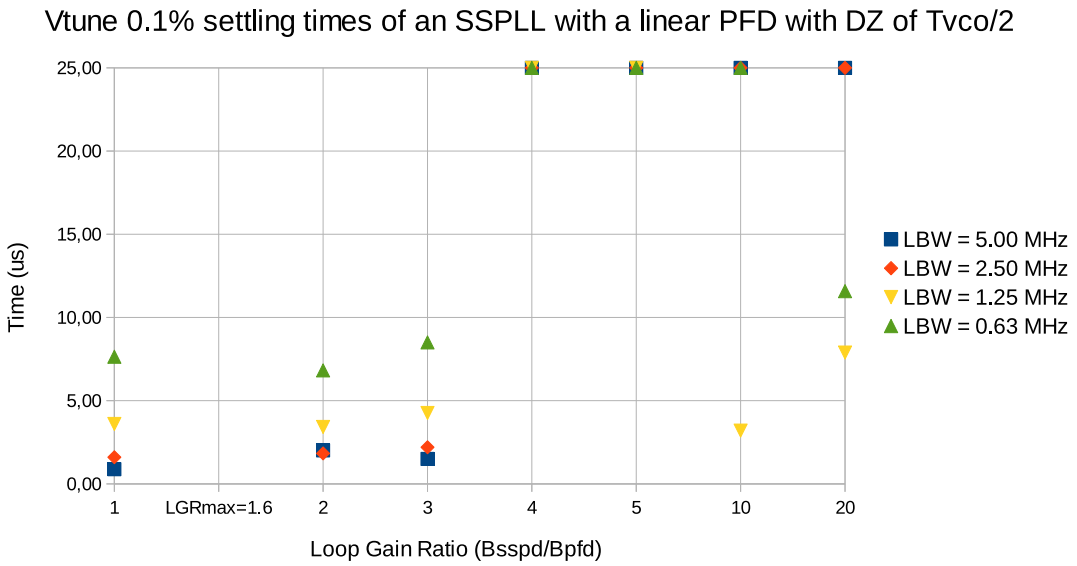


Figure 3.35.: The 0.1% V_{tune} settling times of an SSPLL with a linear PFD with DZ of $T_{vco}/2$ versus loop gain ratios.

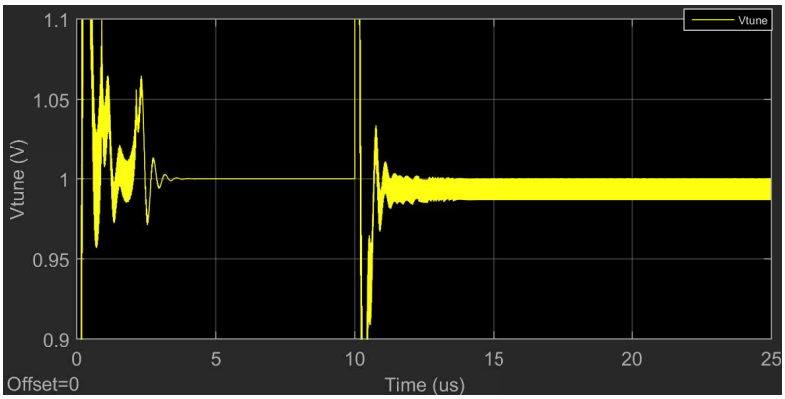


Figure 3.36.: The zoomed graph of V_{tune} for a linear PFD with DZ $T_{vco}/2$ LGR 2 and LBW 1.25 MHz.

Binary Phase-Frequency Detector With a Dead Zone of $T_{ref}/2$

The channel switching simulation results for an SSPLL with a binary PFD with a DZ of $T_{ref}/2$ are shown in figure 3.37. The calculated maximum LGR for this type and size of DZ is $2\pi N$.
The expected result is that there will be correct locking for every LGR in figure 3.37. There is a trend visible of decreasing settling times for higher LGR. This agrees with the observations from subsection 3.2.2.

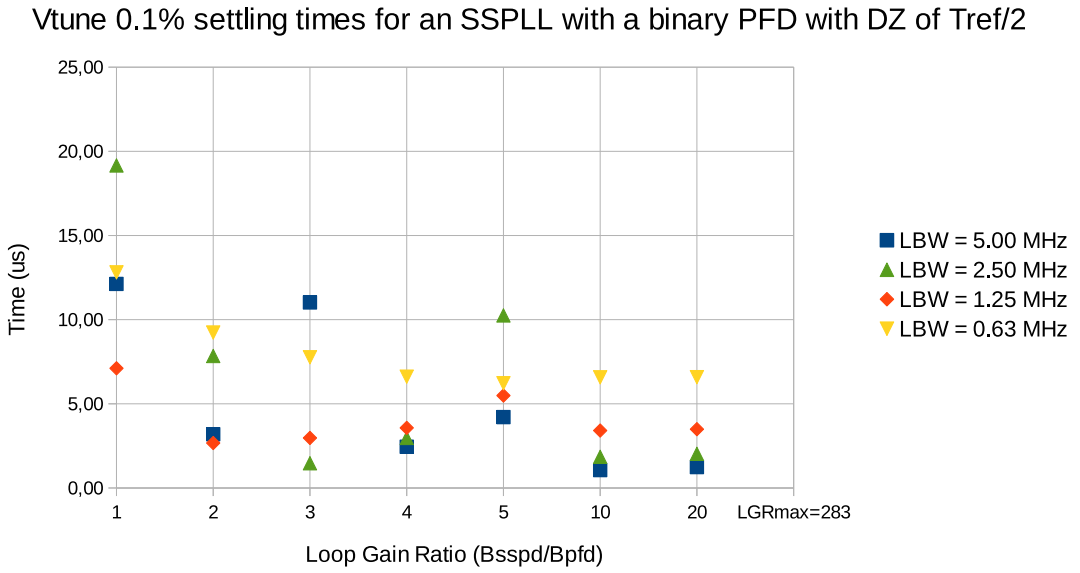


Figure 3.37.: The 0.1% V_{tune} settling times of an SSPLL with a binary PFD with DZ of $T_{ref}/2$ versus loop gain ratios.

Binary Phase-Frequency Detector with a Dead Zone of $T_{vco}/2$

The channel switching simulation results for an SSPLL with a binary PFD with a DZ of $T_{vco}/2$ are shown in figure 3.38. The calculated maximum LGR for this type and size of DZ is 2π.
Figure 3.38 shows that for LGR lower than 2π there is correct locking, there are also some points for higher LGR.
However, when the SSPLL is again injecting with a disturbance at $t = 10\mu s$ the incorrect lock points can be shown. Figure 3.39 illustrates this. By making minor changes in simulation conditions, the same can be shown for the other points with LGR higher than 2π.

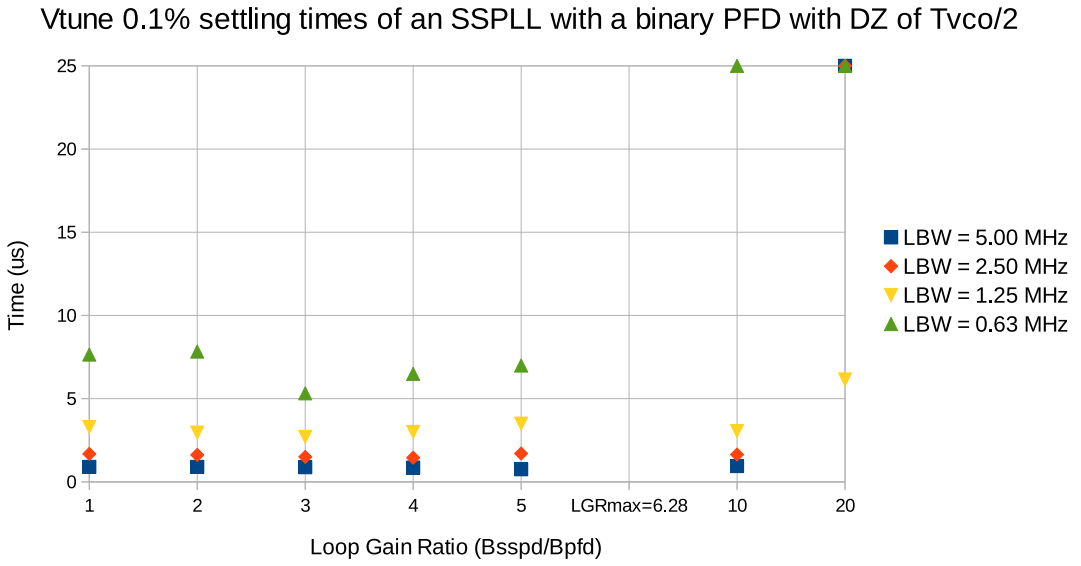


Figure 3.38.: The 0.1% V_{tune} settling times of an SSPLL with a binary PFD with DZ of $T_{vco}/2$ versus loop gain ratios.

3.4.3. Comparison of the Channel Switching Simulation Results

In this subsection the five DZs are compared based on their best simulation results. Figure 3.40 shows the recorded 0.1% settling times for all tested dead zones along with the calculated values using equation 3.14. The data points chosen for the comparison are at the LGR that gave the lowest settling times. The LGRs and corresponding DZs for which the fastest results were simulated are shown in table 3.4.

Table 3.4.: Lgrs and corresponding DZs for the fastest channel switching simulation results.

Parameter	**Value**				
Type of DZ	Linear			Binary	
Size of DZ	none	$T_{ref}/2$	$T_{vco}/2$	$T_{ref}/2$	$T_{vco}/2$
LGR with fastest results	1	1	1	20	3

Figure 3.40 shows the predicted inverse relation between LBW and settling time. Overall the fastest times where recorded with the binary PFD with a DZ of $T_{vco}/2$. The calculated values using equation 3.14 are about a factor 2 lower than the simulation results for the SSPLL without a PFD DZ. This accuracy is enough to use equation 3.14 as a first rough estimate of the channel switching settling time, but because of the non-linear time-discrete nature of PLLs simulations remain a necessary tool.

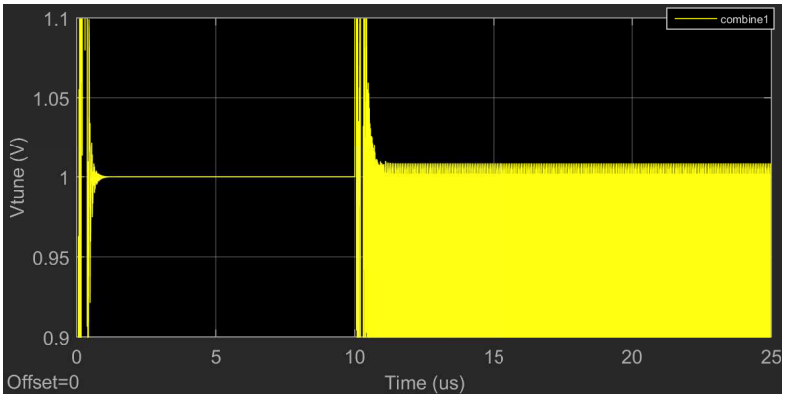


Figure 3.39.: The zoomed graph of V_{tune} for a binary PFD with DZ $T_{vco}/2$ LGR 10 and LBW 5.00 MHz.

3.5. Conclusion About the Channel Switching Simulations

The aim of this chapter was to find relations between the channel switching behaviour and the Loop Band Width, Loop Gain Ratio and size of the Phase Frequency Detector Dead Zone in Sub-Sampling Phase-Locked Loops. To this end a Simulink model was made. The LBW and LGR values were varied using a Matlab script shown in appendix A and tables 3.1 and 3.3.
In the original paper about the SSPLL [9] the DZ was equal to $T_{ref}/2$ and this therefore served as the starting point of the comparison.
In [8], a paper commenting on the slow dynamic behaviour of the SSPLL, it was proposed to remove the DZ to improve the SSPLLs robustness to perturbations. The paper indeed showed an improved response to disturbances and therefore the second choice for the DZ was to remove the DZ.
This thesis proposed a compromise between these two ideas by making the DZ as small as possible without removing it. This should give both the noise benefit of the original SSPLL and have similar robustness to perturbations as was shown by removing the DZ. The edge surrounding the lock point of the sub-sampling loop is $T_{vco}/2$ and therefore this was the third choice of DZ.

The time it took for the VCO control voltage (V_{tune}) to come within 2% of its final value was used as a measure of comparison.
The initial simulation results showed an upper limit of LGR is 300 for the DZ of $T_{ref}/2$

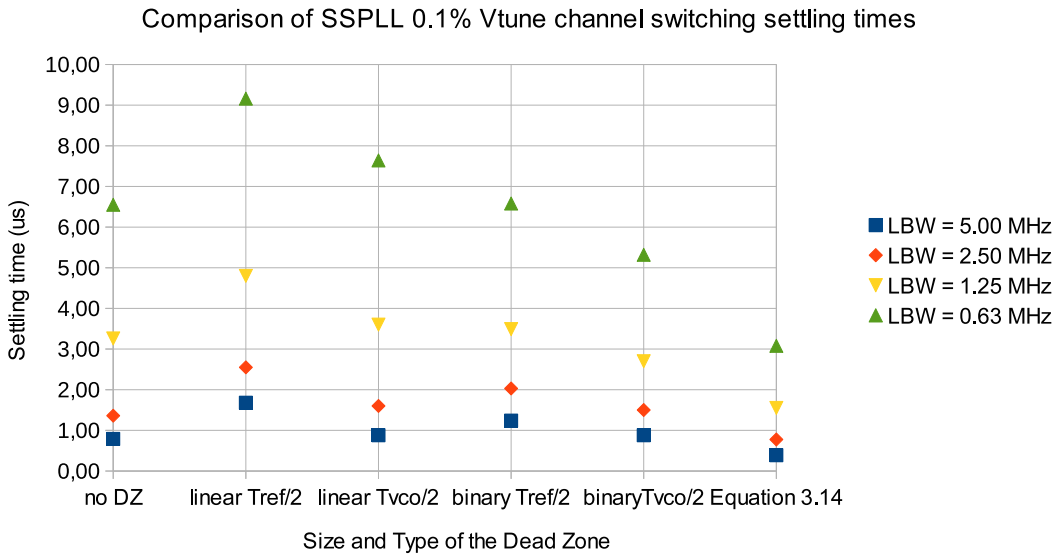


Figure 3.40.: A comparion of the 0.1% V_{tune} settling times of an SSPLL with different DZs for their optimal LGR.

and LGR is 1 for the DZ of $T_{vco}/2$. For the simulation without a DZ a clear limit could not be determined due to the inconsistent results.
The relation between the DZ and settling time seemed to be that a bigger DZ has slower settling behaviour. The calculated settling times given by 3.14 were about 6 times faster than the simulation results.
The 2% limit was taken over from classic control theory because the PLL structure strongly resembles the applications in that field. The first simulations showed this limit to be too big, because it didn't exclude some wrong lock points. Therefore it was adjusted to 0.1% for the next simulations.

Using information from [8] a theoretical basis for the LGR was derived. The theory agreed with the results from the first simulations, but more refined simulations were needed to make the theory plausible.

It was also discovered that the PFD proposed in [9] is binary (without reset) rather than linear as had been presumed up to this point. A linear PFD with DZ was proposed to compare against the binary PFD based on settling time.

For the next set of simulations the limit used to determine the settling time was reduced from 2% to 0.1%, to more clearly distinguish between correct and incorrect lock points. By reducing the range over which the LGR was varied for the simulations, the limits predicted by the new LGR theory were shown to be plausible. However, with more computing power more accurate simulations could be done to increase and reinforce the empirical evidence for the theory presented in section 3.3.
The author would also like to note that the use of a certain boundary around V_{tune} as a condition for phase lock does not seem totally unambiguous. For instance, if there is an unwanted interaction between the two SSPLL loops, but the LBW is low enough to suppress it within the chosen boundary a false positive would be recorded. It could be valuable to look into a different lock definition based instead on the current output of the two loops. It is likely however, that due to mismatch and other noise sources present in practical SSPLL implementations, this definition would only find use in the context of simulations.

To draw a conclusion about which DZ gives the fastest channel switching settling times the fastest simulation results for each DZ were compared in figure 3.40. Equation 3.14 was used as a theoretical reference and its calculated values deviated by a factor two. Though that is close keeping in mind that equation 3.14 was derived for traditional PLLs, it could be valuable to try to develop a settling time equation specifically for SSPLLs.
The fastest times where recorded with the binary PFD with a DZ of $T_{vco}/2$. For now it doesn't seem like the linear PFD has any advantage over the original binary PFD. An exact theoretical reason why the binary PFD shows faster simulated settling times is missing.

4. Lock Perturbation Simulations of a Sub-Sampling Phase-Locked Loop

In this section simulations will be used to find out what the relations are between Lock Perturbation settling time and Loop Band Width, Loop Gain Ratio and size of the PFD Dead Zone. Lock Perturbation means a situation where any charge is injected into the PLL from outside forcing the PLL out of lock.
The simulation model that will be used was introduced in section 3.1. The rest of the simulation setup and will be explained in subsection 4.1, followed by the lock perturbation simulation results and discussion in subsection 4.2 and a comparison in subsection 4.3.

4.1. Lock Perturbation Simulation Setup

In these lock perturbation simulations a voltage will be injected on the V_{tune} voltage while the PLL is locked. The voltage injection will need to be high enough to throw the PLL out of lock. A choice was made for a perturbation of 0.5 V.
The time it takes for the output frequency to again match the pre-set division ratio is the quantity interest. The expected V_{tune} is therefore simply 0 V.
The settling time will be the measured quantity and is defined as the time when V_{tune} falls within a 0.01% boundary of its final value. The maximum simulation time is 25 µs, because that is already much longer than the zero to ten micro seconds time scale of interest. If the PLL is not able to regain lock within that time a settling time of 25 µs will be recorded.

The simulations were run using the script found in appendix A. The choice for LBWs remains the same as with the channel switching simulations at 5.00 MHz, 2.50 MHz, 1.25 MHz and 0.63 MHz. Also remaining the same are the now five PFD DZ variations of binary $T_{ref}/2$ and $T_{vco}/2$, linear $T_{ref}/2$ and $T_{vco}/2$ and lastly no DZ.
Because of the theory developed in section 3.3 the choice for the LGR of the PFD without and linear DZ is limited to 1. For the PFDs with binary DZ of $T_{ref}/2$ and $T_{vco}/2$ there could be an optimal LGR different from the ones found from the channel switching simulations. A binary PFD with DZ $T_{ref}/2$ has a maximum LGR of $2\pi N$, which for $N = 45$ comes down to 283. For a DZ of $T_{vco}/2$ the maximum LGR is 2π. By running simulations at intermediate LGRs and reviewing the results an optimum may

be found for these two DZ variants.

4.1.1. Expectations for the Simulations

The expected result is that LBW will show an inverse relation with the LPS settling time, because in in subsection 3.2.1 it was shown that the closed loop transfer function has this relation. The same applies here, because a perturbation on V_{tune} can be referred back as a change of the input. Therefore, this injected change of the tune voltage can be modelled as a scaled change of the input frequency whose dynamic behaviour is modelled by the closed loop transfer function.

For the LGR it is expected that the theory of section 3.3 holds. The calculated maximum LGRs are shown in table 3.2. This means that for a linear PFD the maximum LGR with a unique lock point is $\pi/2$. For the binary PFD with a DZ of $T_{ref}/2$ this is $2\pi N$ and with a DZ of $T_{vco}/2$ this is 2π.
For the linear PFDs the LGR range is so small that it is assumed there will be no significant performance difference over the range. Therefore, the LGR in this case is set to 1.
For the binary PFDs the range is bigger such that there could be an optimum LGR. However, there is no theoretical basis for what this optimum should be. Therefore, the simulations will be run with varying LGR over its range to see if any optimum becomes visible.

The expected results from changing the size of the DZ if that smaller DZ will have a faster settling time. In [8] this was shown for removing the DZ. Also in that paper an equation for the reaction time T_r was derived depending on the size of the DZ in the phase domain ϕ_{dz} and the size of the perturbation V_{pert}:

$$T_r = \frac{N \cdot \phi_{dz}}{2\pi K_{vco} V_{pert}} \tag{4.1}$$

which shows that a smaller DZ will need less time to react and also a bigger perturbation will lower the reaction time. The reaction is of course not the entire settling time and depending on the size of the DZ, perturbation and LBW it may be more or less significant. For instance, if the perturbation is 0.5 V and the DZ $T_{vco}/2$ the reaction time will be 0.02 µs. If that is combined with a small LBW of say 100 kHz the expected settling time will still be in the order of (tens-of) µs. Therefore the relative contribution of the reaction time was small.

4.1.2. Simulation Setup Variables Table

The simulation parameters and values are shown in table 4.1.

4.2. Lock Perturbation Simulation Results

All lock perturbation simulations were run using the script found in appendix A. Because the linear PFDs with and without DZ share the same single LGR, those results are plotted in the same graph shown in figure 4.1. The settling times for the binary PFD with DZ of $T_{ref}/2$ and $T_{vco}/2$ are respectively shown in figure 4.7 and 4.5.
The y-axis in the graphs indicates the settling time in µs. The x-axis covers the range of LGRs that were simulated. The various LBWs are indicated by different colors and shapes shown in the legend on the right of the graphs.

4.2.1. Phase-Frequency Detector Without a Dead Zone

Based on equation 4.1 and the results from [8] it was expected that removing the DZ would give fast relock times. The results show sub 5 µs relock times for all but one LBW size. For the simulation with LBW equal to 5.00 MHz the remaining PFD activity causes voltage peaks that exceed the 0.1% limit around the final tune voltage. As an example of the simulation results the graph of V_{tune} for a LBW of 2.50 MHz is shown in figure 4.2.

Table 4.1.: Summary table of the channel switching simulation setup.

Parameter	**Value(s)**											
f_{ref} (Hz)	50e6											
A_{ref} (V)	0.5											
f_{fr} (Hz)	2.2e9											
A_{vco} (V)	0.5											
K_{vco} (Hz/V)	50e6											
N1	44											
N2	44											
f_{out} (Hz)	2.25e9											
V_{tune} (V)	1											
I_{cp} (A)	20e-6											
V_{od} (V)	200e-3											
ξ	1											
A_{pert} (V)	0.5											
Type of the DZ	linear	binary										
Size of the DZ	none	$T_{ref}/2$	$T_{vco}/2$									
LGR	1	2	3	4	5	6	10	20	50	75	100	200
LBW (Hz)	0.63e6	1.25e6	2.50e6	5.00e6								

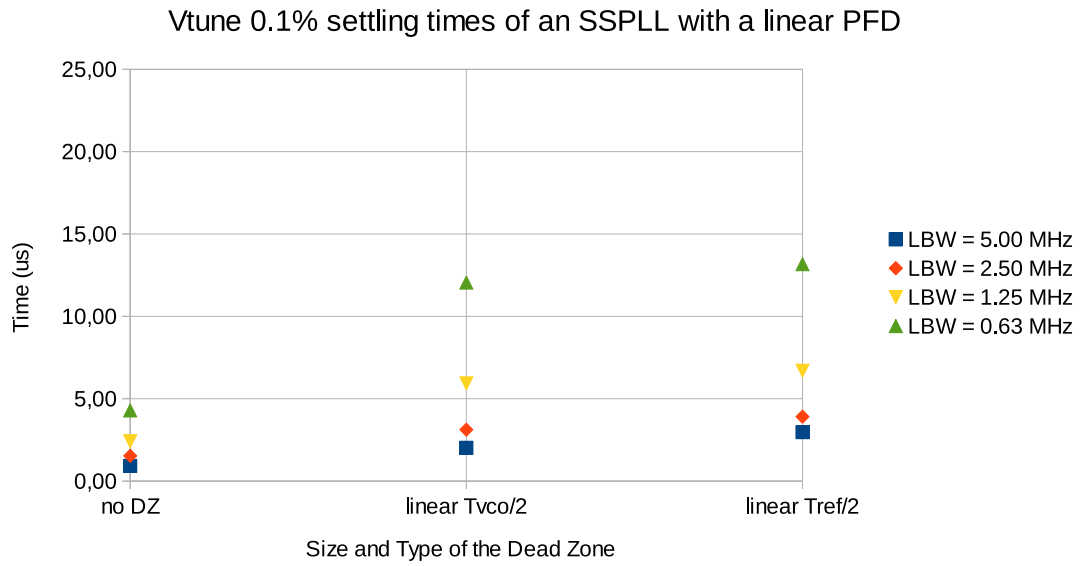


Figure 4.1.: Lock Perturbation settling times for an SSPLL with a linear PFD without DZ, DZ of $T_{ref}/2$ and $T_{vco}/2$.

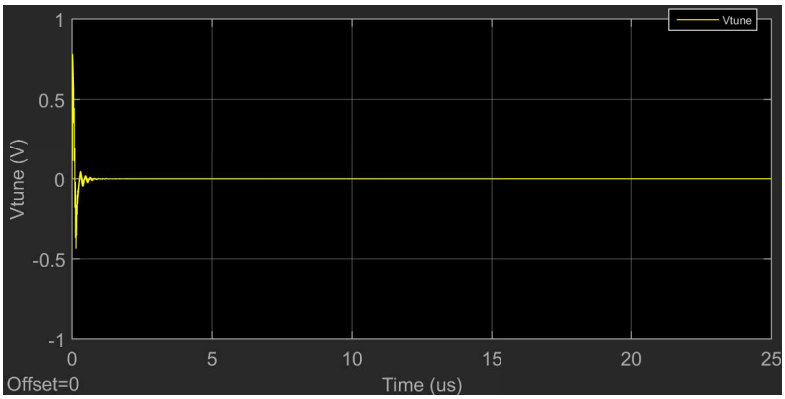


Figure 4.2.: Simulation result for an SSPLL with linear PFD without DZ, LGR 1 and LBW of 2.50 MHz.

4.2.2. Linear Phase-Frequency Detector With a Dead Zone of $T_{vco}/2$

Filling out equation 4.1 for a DZ size of $T_{vco}/2 = \pi/N$ gives an expected reaction time of 0.02 µs. Looking at the results for this DZ in figure 4.1 the settling times are significantly longer than the predicted reaction time. This indicates that the size of the DZ is not the main cause of the long settling times that were recorded. In this case it appears that the LBW and the linear implementation of the DZ have far more impact on the dynamic behaviour. The graph of V_{tune} for a LBW of 2.50 MHz is shown in figure 4.3.

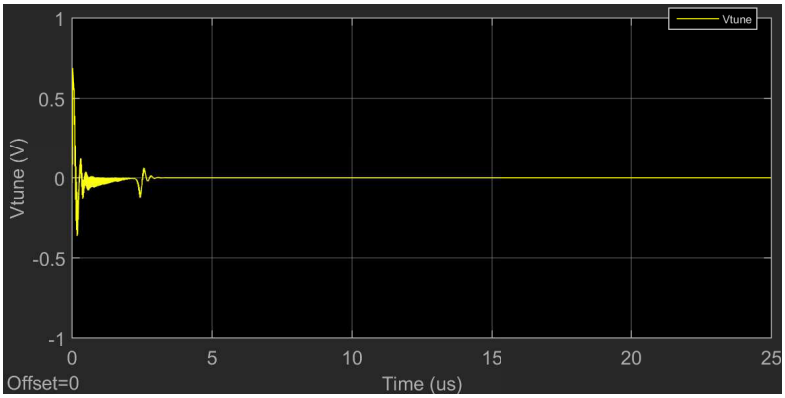


Figure 4.3.: Simulation result for an SSPLL with linear PFD with DZ of $T_{vco}/2$, LGR 1 and LBW of 2.50 MHz.

4.2.3. Linear Phase-Frequency Detector With a Dead Zone of $T_{ref}/2$

For a DZ of $T_{ref}/2 = \pi$ the reaction time given by equation 4.1 is 0.9 µs. In figure 4.4 this can be seen in the time the tune voltage stays at 0.5 V before the PFD reacts. The reaction time is now a more significant part of the overall dynamic behaviour.

4.2.4. Binary Phase-Frequency Detector With a Dead Zone of $T_{vco}/2$

From the results shown in figure 4.5 there is an optimum visible at LGR equal to 3. For this LGR and a LBW of 2.50 MHz the graph of V_{tune} is shown in figure 4.6. The reaction time of 0.02 µs is not a significant part of the settling time and is not clearly visible at the time scale of figure 4.6.

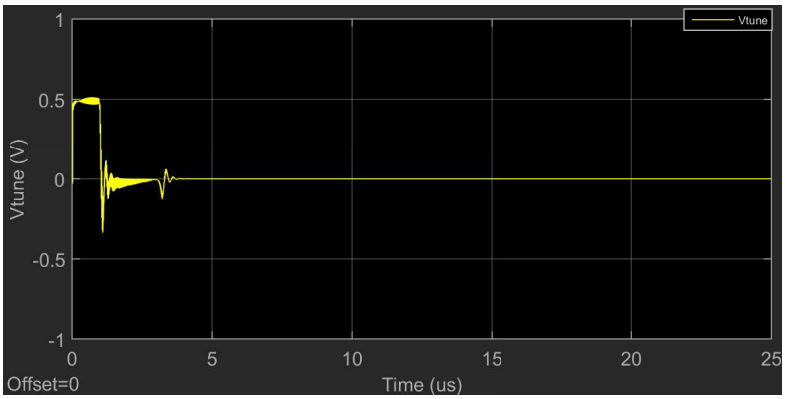


Figure 4.4.: Simulation result for an SSPLL with linear PFD with DZ of $T_{ref}/2$, LGR 1 and LBW of 2.50 MHz.

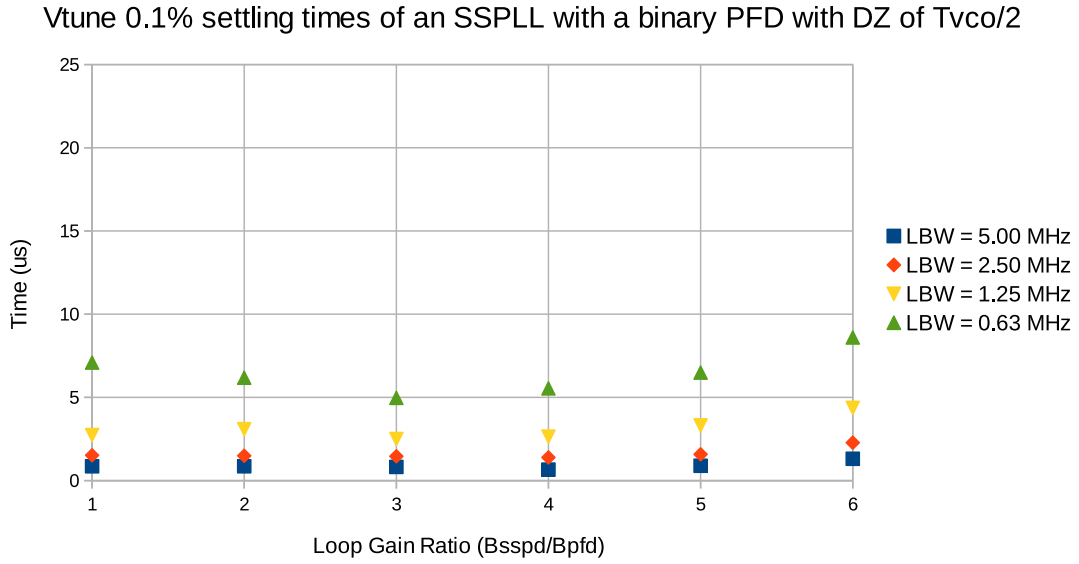


Figure 4.5.: Lock Perturbation settling times for an SSPLL with a binary PFD with DZ of $T_{vco}/2$.

4.2.5. Binary Phase-Frequency Detector With a Dead Zone of $T_{ref}/2$

Looking at the results in figure 4.7 the lowest settling times can be found at LGRs between 5 and 50. For a LBW of 0.63 MHz a trend can be seen. From the point of LGR higher than 50 onwards the settling times become significantly longer. Combining these results with that of the previous channel switching simulations an LGR of 20 is in both cases a good choice. In figure 4.8 the graph of V_{tune} is shown for an LGR of 20 and an LBW of 2.50 MHz. The reaction time of 0.9 µs can be seen in the part of the graph that is at 0.5 V.

For an LGR of 1 and a LBW of 5.00 MHz the simulation result of V_{tune} is shown in figure 4.9. In the figure it can be seen that the voltage keeps overshooting the zero volt target, due to the combination of the high LBW and binary PFD with the large DZ of $T_{ref}/2$. For LGR equal to 2 and a LBW of 1.25 MHz a similar situation occurs, leading to the tune voltage endlessly jumping over and under 0 volt.

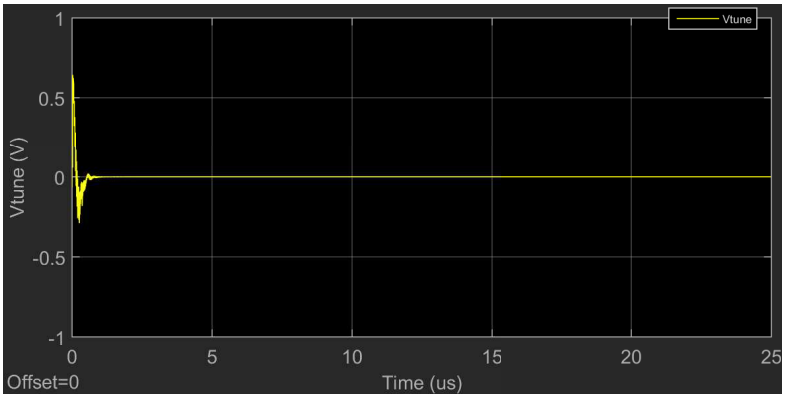


Figure 4.6.: Simulation result for an SSPLL with binary PFD with DZ of $T_{vco}/2$, LGR 3 and LBW of 2.50 MHz.

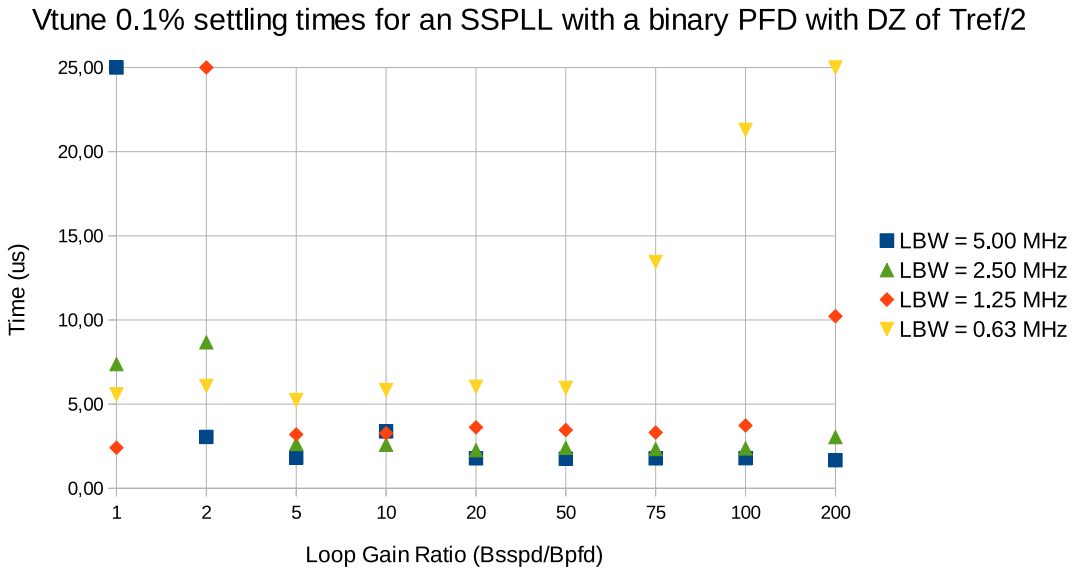


Figure 4.7.: Lock Perturbation settling times for an SSPLL with a binary PFD with DZ of $T_{ref}/2$.

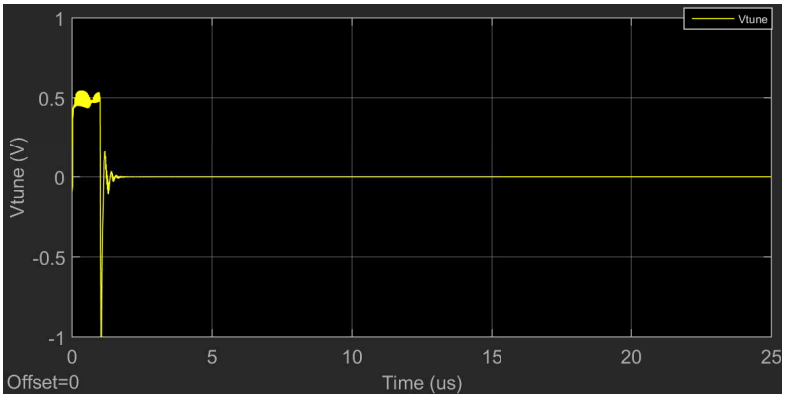


Figure 4.8.: Simulation result for an SSPLL with binary PFD with DZ of $T_{ref}/2$, LGR 20 and LBW of 2.50 MHz.

4.3. Comparison of the Lock Perturbation Simulation Results

In figure 4.10 the fastest lock perturbation simulation results for each DZ are shown together. On the x-axis is indicated the size of the DZ as well as the PFD type, linear or binary. On the y-axis is the time it took for the particular SSPLL configuration to regain phase lock.

For the PFD without DZ the LGR is 1. Its result with a LBW of 5.00 MHz is 25 µs because the remaining PFD activity causes voltage peaks that exceed the 0.1% limit

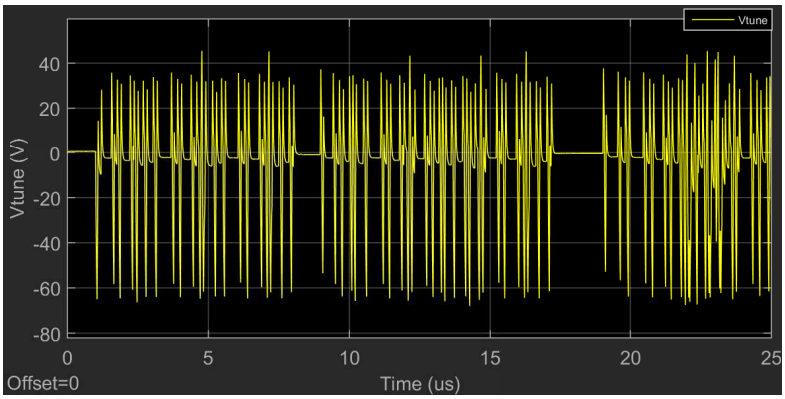


Figure 4.9.: Simulation result for an SSPLL with binary PFD with DZ of $T_{ref}/2$, LGR 1 and LBW of 5.00 MHz.

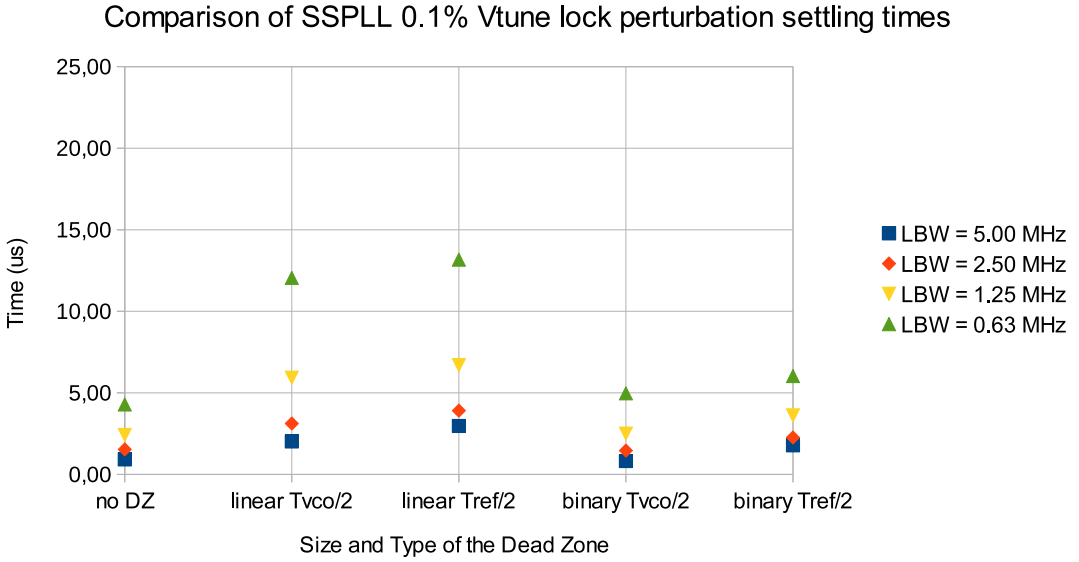


Figure 4.10.: Comparison of Lock Perturbation settling times.

around the final tune voltage. This result will be disregarded for the rest of the comparison.
For both linear PFDs the LGR is 1. The results of the binary PFD with DZ of $T_{vco}/2$ are at LGR equal to 3. The results of the binary PFD with DZ of $T_{ref}/2$ are at LGR equal to 20. These are the same LGRs as shown in table 3.4.

The results for the linear PFD without DZ and the binary PFD with DZ of $T_{vco}/2$ are the fastest. Both the binary PFDs recover lock faster than the linear versions.
The difference between the DZs of $T_{ref}/2$ and $T_{vco}/2$ is the reaction time as described by equation 4.1. This can be seen by comparing figure 4.3 and 4.4 for the linear PFDs and figure 4.8 and 4.6 for the binary PFDs. In those figures the reaction time can be seen as the width of the graph that is at 0.5 V from $t = 0s$ onwards. With a DZ of $T_{ref}/2$ this reaction time is clearly visible and was previously calculated to be 0.9 µs for the setup of these simulations.

4.4. Conclusion About the Lock Perturbation Simulations

In this section simulations were done with the goal of finding relations between lock perturbation settling time and LBW, LGR and size of the PFD DZ. A voltage perturbation was injected onto the V_{Tune} voltage to force the SSPLL out of phase lock and see how fast it would recover lock depending on varying parameters.

Because of the wider range of LGRs available for the binary PFDs based on the theory presented in section 3.3, the LGR was varied to identify any optimum that might exist. For the linear PFDs the available LGR range was not wide enough to warrant a similar investigation and their simulations were all run with LGR equal to 1.
For the binary PFD with DZ of $T_{ref}/2$ an optimum range was found for an LGR between 5 and 50. The binary PFD with DZ of $T_{vco}/2$ showed an optimum for LGR equal to 3.

From [8] equation 4.1 was found that expresses the time it takes the phase at the VCO output to accumulate to equal the PFD DZ for a given constant voltage perturbation at V_{tune}.
From the simulation results it was concluded that this reaction time is the difference between the settling times for a DZ of $T_{ref}/2$ and $T_{vco}/2$. The significance of this reaction time contribution to the total settling time, depends on how big the voltage perturbation is, the size of the DZ and the LBW. With the 0.5 V perturbation that was used for these simulations the effect of reaction time may have been understated in the results. By decreasing the size of the perturbation the reaction time could be accentuated more.
Equation 4.1 gives a reaction time of 0.9 µs for the DZ of $T_{ref}/2$ and 0.02 µs for the DZ of $T_{vco}/2$. If the voltage perturbation is decreased by a factor 5 to 0.1 V the reaction times increase to 4.5 µs and 0.1 µs. In many cases the reaction time of 0.1 µs for a DZ $T_{vco}/2$

would still be a minor part of the total settling time, which is in the order of several µs. However, in the case of a DZ of $T_{ref}/2$ the increase to a reaction time of 4.5 µs will likely have a huge impact on the total settling time, which is also in the order of several µs.

Comparing all results shows that the PFD without a DZ and the binary PFD with DZ of $T_{vco}/2$ give the fastest lock perturbation settling times. The binary PFD with DZ of $T_{ref}/2$ may still be good enough, but that depends on the expected perturbations and required maximum relock time. Both binary PFDs have faster settling times than their linear counterparts.
Finally, if noise performance is also considered the binary PFD with a DZ of $T_{vco}/2$ gains a big advantage over the PFD without DZ, because in lock its PFD is fully disabled and therefore does not influence the phase noise at the VCO output.

5. Thesis Conclusion

The goal of this thesis was to find out more about the dynamic behaviour of SSPLLs through simulation and analysis. A paper published by Hsu et. al. [8] raised the issue of the SSPLL's robustness to perturbations. The proposed solution was to remove the PFD DZ present in the original design from [9]. However, removing the PFD DZ turns out to negate a large part of the noise benefits that the original SSPLL presented. The insight gained has led to a proposed SSPLL implementation that keeps all the noise benefits of the original design and is also robust to perturbations. At the beginning of this thesis the following questions where raised:

> What is the influence of the dead zone in the phase frequency detector on the sub-sampling phase-locked loop dynamic behaviour?

> Can the robustness to perturbations of the SSPLL design from [9] be improved without removing the dead zone in the phase frequency detector?

> Can the dynamic behaviour of the SSPLL design from [9] be improved by optimizing its configuration?

Channel Switching Behaviour

The first step was to make a Simulink simulation model that could reproduce the known dynamic behaviour from [9]. In doing so the analysis for loop stability revealed a Zero-Order Sample and Hold effect (ZOSH) that was previously not included. This ZOSH effect was not significant in the original SSPLL design, because of the gain reduction implementation that was used. The hold pulses were made shorter, thereby reducing gain and coincidentally removing the ZOSH effect. If the gain reduction would be implemented without this shortening of the hold pulse, the ZOSH transfer function would make the loop gain zero at multiples of the reference frequency. Because of this effect the gain reduction implementation as used in [9] is likely the best choice for achieving a low PLL FOM.

The dynamic behaviour of PLLs was divided into three situations: start-up, channel switching and lock perturbation. The focus of this thesis was on robustness to perturbations, therefore only the latter two situations were analysed.

Next the simulation model was used to find relations between the channel switching behaviour and the Loop Band Width, Loop Gain Ratio and size of the Phase Frequency Detector Dead Zone in SSPLLs. To this end three variations of the Simulink simulation model were made, the difference between them being the size of the DZ of the PFD. The LBW and LGR are parameters whose value was varied using the Matlab script found in appendix A.
In the original paper about the SSPLL [9] the DZ was equal to $T_{ref}/2$ and this therefore served as the starting point of the comparison.
In [8], a paper commenting on the slow dynamic behaviour of the SSPLL, it was proposed to remove the DZ to improve the SSPLLs robustness to perturbations. The paper indeed showed an improved response to disturbances and therefore the second choice for the DZ was to remove the DZ.
This thesis proposed a compromise between these two ideas by making the DZ as small as possible without removing it. This should give both the noise benefit of the original SSPLL and have similar robustness to perturbations as was shown by removing the DZ. The edge surrounding the lock point of the sub-sampling loop is $T_{vco}/2$ and therefore this was the third choice of DZ.

Using results from some initial simulations together with information from [8] a theoretical basis for the LGR was derived. At the same time it was discovered that the PFD proposed in [9] is binary (without reset) rather than linear as had been presumed up to this point. A linear PFD with DZ was proposed to compare against the binary PFD on the point of settling speed.

The channel switching settling times for each DZ were compared in figure 3.40. The fastest settling times where recorded with the binary PFD with a DZ of $T_{vco}/2$. The linear PFD showed no advantage over the original binary PFD.

Lock Perturbation Behaviour

After the channel switching simulations, the goal was to find relations between lock perturbation settling time and LBW, LGR and size of the PFD DZ. A voltage perturbation was injected onto the V_{Tune} voltage to force the SSPLL out of phase lock and see how fast it would recover lock depending on varying parameters.

Because of the wider range of LGRs available for the binary PFDs based on the theory presented in section 3.3, the LGR was varied to identify any optimum that might exist. For the linear PFDs the available LGR range was not wide enough to warrant a similar investigation and their simulations were all run with LGR equal to 1.
For the binary PFD with DZ of $T_{ref}/2$ an optimum range was found for an LGR between 5 and 50. The binary PFD with DZ of $T_{vco}/2$ showed an optimum for LGR equal to 3.

From [8] equation 4.1 was found that expresses the time it takes the phase at the VCO

output to accumulate to equal the PFD DZ for a given constant voltage perturbation at V_{tune}. From the simulation results it was concluded that this reaction time is the difference between the settling times for a DZ of $T_{ref}/2$ and $T_{vco}/2$. The significance of this reaction time contribution to the total settling time, depends on how big the voltage perturbation is, the size of the DZ and the LBW.

Comparing all results shows that the PFD without a DZ and the binary PFD with DZ of $T_{vco}/2$ give the fastest lock perturbation settling times. The binary PFD with DZ of $T_{ref}/2$ may still be good enough, but that depends on the expected perturbations and required maximum relock time. Both binary PFDs have faster settling times than their linear counterparts. Finally, if noise performance is also considered the binary PFD with a DZ of $T_{vco}/2$ gains a big advantage over the PFD without DZ, because in lock its PFD is fully disabled and therefore does not influence the phase noise at the VCO output.

Dynamic Behaviour

Combining the information obtained in this thesis leads to the conclusion that removing the PFD DZ improves the SSPLL dynamic behaviour as was shown in [8]. However, this is at the cost of added phase noise at the VCO output with respect to the original SSPLL design from [9].
By reducing the size of the PFD DZ to $T_{vco}/2$ a similar improvement in robustness is obtained, while retaining the noise benefits of having a PFD DZ. The SSPLL FOM will be worse though by the extra power consumption of the DZ flip-flops in the PFD that are now clocked at f_{vco} instead of f_{ref}. Also, in the original SSPLL paper the frequency loop was turned off, further improving the FOM at the cost of robustness.
The fastest dynamic behaviour is obtained by using a binary implementation of the DZ of $T_{vco}/2$. The linear PFD with DZ presented in this thesis has shown no advantage over the binary version when applied in an SSPLL. An exact theoretical explanation for this is not known. However, for now it is valuable to know the distinction between these two implementation with regard to the LGR theory developed in this thesis.

Lastly, it should not be forgotten that the choice of LBW also has a high influence on dynamic behaviour. Usually though, its choice is based on reducing the VCO output phase noise instead of dynamic behaviour.

5.1. Recommendations for Future Work

The conclusions in this thesis are based on behavioural simulations done in Mathworks' Simulink. Great effort was taken to make the simulation model behave as the published SSPLL reference. However, it is possible that there are unforeseen issues. To this end a good next step would be to validate the model behaviour by using more computational precision and more scenarios.

The use of a certain boundary around V_{tune} as a condition for phase lock does not seem totally unambiguous. It could be valuable to look into a different lock definition based instead on the current output of the two loops.

Equation 3.14 was derived for traditional PLLs and its predicted values came within a factor two or more from the simulations results. Therefore, it could be valuable to try to develop a settling time equation specifically for SSPLLs.

If there is enough confidence in the competency of the Simulink model and the conclusions from this thesis an SSPLL should be made with the proposed reduced size of the DZ. The novelty of that SSPLL would be combining the already published levels of low PLL FOM with a more robust design.

Another big step forward for the SSPLL concept would be to improve its tunability by making it fractional-N. A very promising way of doing this was published in [7].

A. Matlab Simulation Script

```
% This script sets the PLL simulation parameters
```

Reference

```
f_ref = 50e6;                          % reference frequency
T_ref = 1/f_ref;                       % reference period
A_ref = 0.5;                           % amplitude of the reference
ref_bias = 0;                          % reference bias Voltage
S_ref = 1e-20;                         % reference noise power

%display('reference set')
```

Divider

```
N = 45;                                % feedback division ratio
f_set = f_ref*N;                       % intended PLL output frequency

%display('divider set');
```

Voltage Controlled Oscillator

```
A_vco = 0.5;                           % VCO output amplitude in Volts
f_fr = 45*f_ref;                       % Free-Running VCO frequency in Hz
K_vco = 50e6;                          % VCO sensitivity in Hz/V
V_tune_set = (f_set-f_fr)/K_vco;       % intended Vtune voltage
S_vco = 1e-20;                         % VCO noise power

%display('VCO set');
```

Output to Workspace and Simulation Sample Time

```
T_zoh = 1e-12;                         % zero order hold sample time

%display('Sampling time set');
```

Phase Detector, Pharge Pump and Loop Gain

```
I_cp = 20e-6;                          % the Charge Pump current
V_od = 200e-3;                         % the effective Vgs of the SS CP gm
gm = -2*I_cp/(V_od);                   % the SSCP gm
tau_pul = 1*0.7074*T_ref/1000;         % the pulse duration for the SSPD gain control

B_pfd = I_cp/(2*pi*N);                 % Gao eq. 4.3
B_sspd = abs(A_vco*gm*tau_pul/T_ref);  % Gao eq. 4.8

B = B_pfd+B_sspd;                      % superimposed loop gain
LGR = B_sspd/B_pfd;                    % Loop Gain Ratio

%display('CP set');
```

Loop Filter

```
xi = 1;                                % set the damping factor of the open-loop transfer
w_n = 2*pi*f_ref/50;                   % set the natural frequency of the open-Loop transfer

C_1 = B*K_vco/(w_n^2);                 % first pole cap
C_2 = C_1/(2*(4*xi^2-1));              % second pole cap
C_eq = C_1*C_2/(C_1+C_2);              % equivalent cap
R_1 = 2*xi*w_n/(B*K_vco);              % resistance that give a zero

z_1 = -1/(R_1*C_1);                    % first Loop Filter zero
p_1 = 0;                               % first Loop Filter pole
p_2 = -1/(R_1*C_eq);                   % second Loop Filter pole
K_lf = 1/C_2;                          % Loop Filter gain

%display('filter set');
```

Perturbation

```
A_pert = 0.5;                          % perturbation amplitude in Volt
T_pert = 100e-6;                       % perturbation period in seconds
W_pert = 100e-6;                       % perturbation width in seconds
Delta_pert = 0.02e-6;                  % perturbation delay in seconds
V_tune_init = 0;                       % initial Vtune voltage

%display('perturbation set');
```

finished setting parameters

```
%display('end of line');
```

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