Temperature Independent, Low Reference voltage

Jelle Bakker, June 28, 2018

Abstract—The change in bandgap of a silicon diode, due to applied strain, was experimentally studied for a wide temperature range (5 K to 473 K). The strain was then estimated, and a simulated change in bandgap was leveraged in a new bandgap reference circuit which should result in a lowered reference voltage. Such a circuit could then potentially be utilised in modern circuits. The estimated bandgap difference was found to be between 1.3 mV to 8.0 mV depending on the type of diode and the assumption that the strain is not temperature dependent. The corresponding strain was found to be between −0.007% to −0.054% and the simulated reference voltage did indeed become lower. The new bandgap reference circuit has a strong potential, also for cryogenic ambient, however the way to apply strain should first be understood completely and optimised.

Index Terms—Bandgap reference, low reference voltages, strain, diode, temperature.

1 INTRODUCTION

Modern integrated circuits require low voltage, stable reference voltages, in order to work properly. Currently the bandgap reference circuit is used quite often [1]. In principle, this bandgap reference circuit gives a temperature independent reference voltage. This voltage is made by summing the voltage over a single diode, which decreases for higher temperatures, and the voltage difference over two diodes that are biased at a different current density. The latter voltage is linear with temperature. There is however a problem. The reference voltage that is created by this circuit is around the bandgap voltage of silicon (~1.1 V) while today's supply voltage may be smaller (~0.6 V). It is known that the bandgap of silicon depends on strain [2]. So the diode current will also change by strain because it is exponentially dependent on the bandgap. This implies that by taking the difference between two diodes with different current densities, and different amounts of strain, a linearly increasing voltage with an offset dependent on the difference in bandgap could be made. This offset can then be multiplied and then subtracted from the reference voltage in order to obtain a lower reference voltage.

Strain changes the bandgap, however it is unknown how diodes with strain will behave for a wide temperature range, and it is also unknown whether the strain that is applied to a set of manufactured diodes is sufficient to measure a difference in bandgap. Furthermore the strain can only be predicted once the essential manufacturing steps are known. These steps are unknown because the diodes are made by an external manufacturer.

The current hypothesis is that the strain applied to a diode, if it is large enough, would cause a measurable change in bandgap which then theoretically could be used to make a temperature independent, low reference voltage. The main objective of this report is to investigate whether this hypothesis is correct. This will be done by answering the following research questions.

- What is the achieved strain on the diodes and how does the difference in bandgap [eV], of the strained silicon, between two diodes behave, for a temperature range between 5 K to 473 K?
  - How to determine the (ambient) temperature?
  - How to determine the difference in bandgap between two diodes?
  - How to determine the strain?
- Could the difference in strain induced bandgap be used to make a new bandgap reference circuit with a lower reference voltage then the original circuit?
  - How does the original bandgap reference circuit work?
  - How would the new bandgap reference circuit work?

The "Temperature" section discusses how the temperature of a diode can be determined using the $I-V$ curve of the previously mentioned diode. The "Bandgap Difference" section discusses how the difference in bandgap can be found for diodes. The "Strain" section discusses how the strain can be calculated once the bandgap difference is known. The "Bandgap Reference Circuit" section

will explain the original and the new bandgap reference circuits and a couple of simulations will be done.

2 Temperature

One of the objectives is to plot the difference in bandgap caused by strain versus the (ambient) temperature. This means that the temperature has to be determined. The temperature could be measured with commercial measurement equipment. That is available for the high temperature range (245 K to 450 K) and the cold temperature range (10 K to 245 K). The temperature can however also be determined from the $I-V$ plot of a diode; this is useful to check if the temperature was measured correctly. The basic $I-V$ equation of a diode can be rewritten to give the temperature. Equation 3 shows that the temperature can be determined by taking one over the derivative of

$$I_\mathrm{D} = I_\mathrm{S} e^{\frac{V_\mathrm{D}}{u_T N}} \tag{1}$$

with respect to the voltage (V_D). Here $u_T = \frac{kT}{q}$, N is the ideality factor and I_S is the saturation current. This results in

$$\left(\frac{dI_\mathrm{D}}{dV_\mathrm{D}}\right)^{-1} = \left(\frac{I_\mathrm{S}}{u_T} e^{\frac{V_\mathrm{D}}{u_T N}}\right)^{-1} = \frac{u_T}{I_\mathrm{D}} N. \tag{2}$$

Multiplying this with I_D will result in the thermal voltage

$$\frac{u_T}{I_\mathrm{D}} N I_\mathrm{D} = u_T N. \tag{3}$$

multiplying this with $\frac{q}{kN}$ gives T. It should be noted that taking the derivative will be the same as multiplying with s in the s-domain. which is the same as a high pass filter which in turn increases the amount of noise. If the ideality factor N is not equal to unity it could be that the temperature can not accurately be found using this method because the ideality factor may be temperature dependent [3]. N will be approximately 1 for large forward biased voltage [4]. The ideality factor can also be estimated by trying to minimise the error between the measured and calculated temperature. A more detailed explanation, along with a different method that could be used to find the temperature without taking the derivative which increases the noise, can be found in appendix A. The symbols used in the equations can be found in appendix H.

3 Bandgap Difference

The difference in bandgap between strained and less strained or "relaxed" silicon, whose relation will be discussed in section 4, can be found using at least 4 different methods. The first is based on extracting the difference in bandgap by taking the difference between the voltage over two diodes with a constant current (method 1), or the difference in current with a fixed voltage is taken to find the difference in bandgap (method 2). The bandgap of each individual diode could be determined, from the $I-V$ curves at different temperatures, in order to find the difference in bandgap (method 3). The last method makes use of the fact that the energy of photons generated by the diode, equals the bandgap energy (method 4).

All four methods could be used however method 1 and 2 are the easiest to implement. Method 4 has the advantage that the bandgap is measured directly unlike method 1 and 2 where it is impossible to say if it is the bandgap that is temperature dependent due to thermal expansion of the diodes or that the diodes are simply not identical enough which would also result in a temperature dependent term. Calculating the bandgap is more work than simply using the difference in voltage between two diodes, and measuring the light of the diodes requires special measurement equipment which would also take extra time. This is why method 1 will be used to obtain the difference in bandgap and method 2 will be used to confirm method 1.

Method 1 depends on the fact that the diodes are identical with the only difference being the bandgap. This may not be completely true because there could be some differences between the diodes due to the production process and possibly at least one dimension is changed for each diode. The diodes were made on the same chip, so there will most likely not be a large error due to fabrication differences. To test this two identical diodes on separate chips were measured using the high temperature measurement setup. The results can be seen in appendix G. The difference in bandgap can then be found by rewriting the equation for the current of a diode,

$$I_\mathrm{D} = I_\mathrm{S} e^{\frac{V_\mathrm{D}}{u_T}} = n_\mathrm{i}^2 q A \left(\frac{D_n}{N_\mathrm{A} L_n} + \frac{D_p}{N_\mathrm{D} L_p}\right) e^{\frac{V_\mathrm{D}}{u_T}}, \tag{4}$$

where n_i^2 is equal to

$$n_\mathrm{i}^2 = N_\mathrm{c} N_\mathrm{v} e^{\frac{-E_g}{kT}}. \tag{5}$$

The names of all the used symbols can be found in appendix H table 25 [12]. Then the dif-

ference in voltage between two diodes is taken:

$$V_{D1} - V_{D2} = \frac{\Delta E_g}{q} \quad (6)$$

See appendix B for a more thorough explanation along with simulations adopting method 1. See appendix B for in depth explanations about method 2, 3 and 4.

4 STRAIN

Strain influences the bandgap. The problem is that the strain can not be calculated beforehand for the diodes that will be measured. This is because the exact production process is not known. This is why the strain will be determined from ΔE_g. ΔE_g can be calculated and it is also equal to

$$\Delta E_g = max(\Delta E_v) - min(\Delta E_c), \quad (7)$$

ΔE_c and ΔE_v are the difference between the conductance and valence band with and without strain and ΔE_c and ΔE_v are only dependent on the strain and a couple of constants,

$$\Delta E_{c,k} = \Xi_d(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \Xi_u \varepsilon_{kk}, \quad (8)$$

$$\Delta E_{v,k} = -a(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \quad (9)$$

$$\pm\sqrt{\frac{b^2}{2}((\varepsilon_{xx} - \varepsilon_{yy})^2 + (\varepsilon_{yy} - \varepsilon_{zz})^2 + (\varepsilon_{xx} - \varepsilon_{zz})^2)}.$$

This means that an equation can be found that translates ΔE_g to strain. Here Ξ_d, Ξ_u, a and b are the dilatational deformation potential, uniaxial deformation potential, valence band deformation potential and valence band shear deformation potential respectively. All symbols of the equations can be found in appendix H [2].

ε is the strain in the x, y and z direction. A compressive (negative) strain is applied in the x direction for diode types 1 and 2. This means that the strain in the z and y directions are equal to the Poisson's ratio $(-\sigma_{100})$ times the strain in the x direction. Diode type 3 has an equal compressive strain applied both in the x and y direction. This means that the strain in the z direction will be equal to -2 times the Poisson's ratio (σ_{100}) times the strain in the x direction.

Diode type 1, 2 and 3 can be seen in figures 1 to 3. The dimensions that are changed are indicated with the letters k d l for diode types 1, 2 and 3 respectively. The strain is created by either changing the width of the STI or the width of the diode itself. The legend and dimensions of the changed width can be seen in tables 1 and 2. See appendix B for a more detailed explanation of how the strain is made per diode type.

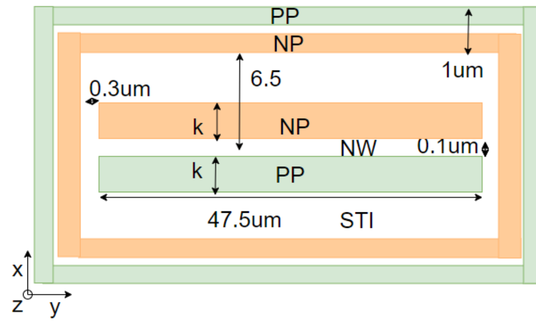

Figure 1. Diode type 1, top view, variants of diode type 1 have different k.

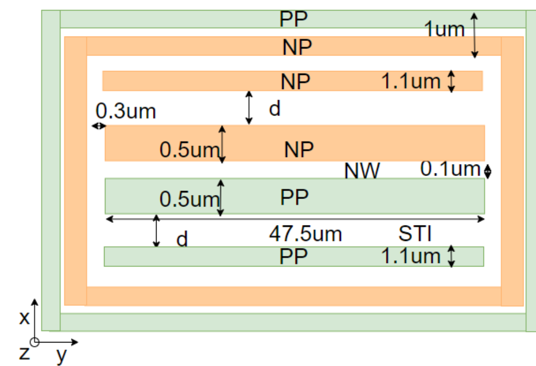

Figure 2. Diode type 2, top view, variants of diode type 2 have different d.

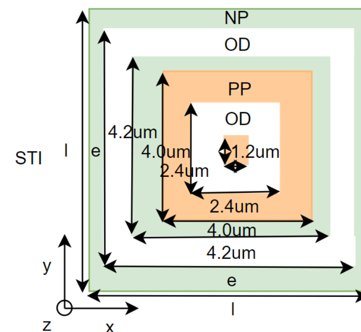

Figure 3. Diode type 3, top view, variants of diode type 3 have different e and l.

Table 1
Legend for figure 1 till 3

Symbol	Description
NP	n type silicon
NW	n well
PW	p well
PP	p type silicon
OD	active area
STI	Shallow trench isolation
k, d, l, e	dimensions that are varied

Table 2
Dimensions for figure 26 till 29

Type	Name	Length (μm)
Type 1	D_{11}	k=0.67
	D_{12}	k=2.1
Type 2	D_{21}	d=0.12
	D_{22}	d=2.0
Type 3	D_{31}	l=6.1 e=5.6
	D_{32}	l=8.0 e=7.5

$\varepsilon_{\mathrm{kk}}$ is the strain in the direction that will result in the minimum ΔE_{c}. This is the strain is in the x direction for all 3 diode types, because the strain in the x direction is compressive and will therefore always result in a lower ΔE_{c} than the tensile strain in the y and z direction for diode types 1,2 and the z direction for diode type 3 [2].

It is also known that ΔE_V has to be maximum. The $\pm$ in equation 9 represents the heavy and light hole bands. The light hole band will have an higher energy then the heavy hole band and that is in this case represented by the + sign. Hence, this + will give the maximum ΔE_V and determines the ΔE_{g} [18].

Equations 8 and 9 can now be rewritten to only be dependent on the strain in the x direction for all 3 types of diodes. The result can be seen in equations 65 to 68 in appendix C. These equations can then in turn be rewritten using the fact that $\Delta E_{\mathrm{g}} = max(\Delta E_{\mathrm{v,k}}) - min(\Delta E_{\mathrm{c,k}})$. The resulting equation translates ΔE_{g} to strain. The strain for diode type 1 and 2 then is

$$\varepsilon_{\mathrm{xx,D1,D2,LH}} = \frac{-\Delta E_{\mathrm{g,D1,D2,LH}}}{b - \Xi_{\mathrm{u}} - a - \Xi_{\mathrm{d}} + (2\Xi_{\mathrm{d}} + 2a + b)\sigma_{100}}. \tag{10}$$

The strain for diode type 3 will be

$$\varepsilon_{\mathrm{xx,D3,LH}} = \frac{-\Delta E_{\mathrm{g,D3,LH}}}{b - \Xi_{\mathrm{u}} - 2a + 2\Xi_{\mathrm{d}} + (\Xi_{\mathrm{d}} + a + b)\sigma_{100}}. \tag{11}$$

See appendix C for a more detailed explanation along with a description of the 3 different types of diodes and a plot of equations 10 and 11.

5 Bandgap Reference Circuit

The conventional bandgap reference circuit will first be explained after which a new bandgap reference circuit will be demonstrated, to show how the reference voltage could be lowered using a simulated bandgap difference.

Conventional Bandgap Reference Circuit

The conventional bandgap circuit is shown in figure 4 [6]. The voltage over diode D1 (see figure 4) decreases with an increase in temperature,

$$V_{\mathrm{D}}(T) = \frac{kT}{q} \ln\left(\frac{I_{\mathrm{D1}}}{I_{\mathrm{S}}(T)}\right). \tag{12}$$

$$I_{\mathrm{S}}(T) = qA\left(\frac{D_n}{N_{\mathrm{A}} L_n} + \frac{D_p}{N_{\mathrm{D}} L_p}\right) N_{\mathrm{c}} N_{\mathrm{v}} e^{\frac{-E_g}{kT}} \tag{13}$$

Here the saturation current I_{S} is dependent on the temperature. I_{S} increases for higher temperatures thereby lowering V_{D} at a constant current level [5]. The voltage over diode D1 is called Complementary To Absolute Temperature (CTAT) or V1 in the LTspice schematic in figure 4. V_{D1} and V_{D2} corresponds to the voltage over diode 1 and 2. The difference in voltage between diode D1 and D2 increases with an increase in temperature

$$V_{\mathrm{D1}} - V_{\mathrm{D2}} = \frac{kT}{q} \ln(Q) = PTAT. \tag{14}$$

Q is the ratio between the current density of diode 1 and diode 2. This increasing voltage is called Proportional To Absolute Temperature (PTAT). Q is chosen in such a way that it compensates for the the decreasing slope of CTAT(T).

The reference voltage is not a straight line. Instead it will have a maximum as can be seen in figure 5. The ratio Q decides where the maximum reference voltage can be found. The reference voltage should be maximum for the center operating temperature of a circuit in order to minimise the temperature dependence.

The opamp takes the difference in voltage between V_{D1} and V_{D2} plus the voltage over resistor R_2. There is a current I_1 and I_2 for which the difference between V_{D1} and $V_{\mathrm{D2}} + V_{\mathrm{R2}}$ is equal to 0. The currents are stable when the opamp has reached this point. The current through R_2 is

$$I_2 = \frac{V_{\mathrm{D1}} - V_{\mathrm{D2}}}{R_2} = \frac{\frac{kT}{q}\ln(Q)}{R_2}. \tag{15}$$

The current through R_1 will then be Q times higher then I_2. So PTAT can be found by taking R_1 to be equal to R_2/Q. This means the voltage over R_1 is equal to PTAT and V_{D1} (V1) is equal to CTAT. The sum of PTAT and CTAT will be the reference voltage if Q is chosen to compensate for the decreasing slope of V_{D1} for higher temperatures. V3 is the sum of CTAT and PTAT so it (see figure 4) has to be equal to the reference voltage (V_{ref}) [6].

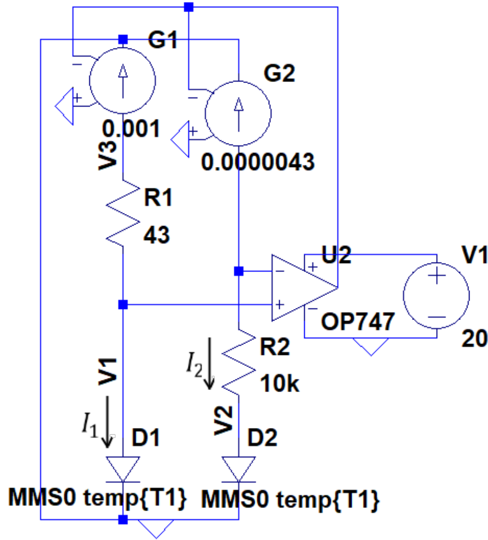

Figure 4. Conventional bandgap reference voltage circuit [6].

Figure 5 shows the simulation result of the circuit in figure 4. Here the center operating temperature (T_{center}) is equal to 273 K with a maximum voltage of 1.1996 V and the maximum deviation of the reference voltage between $T_{center} \pm 40$ K is 1.1 mV

The saturation current of the simulated diodes is made very low (0.005 nA) in the simulations so that the circuit will work over a large temperature region. The series resistance could also have been lowered to achieve the same result. If the saturation current is too high the series resistance of the diodes will start to give problems for low temperatures because V_{D1} will be larger for lower temperatures.

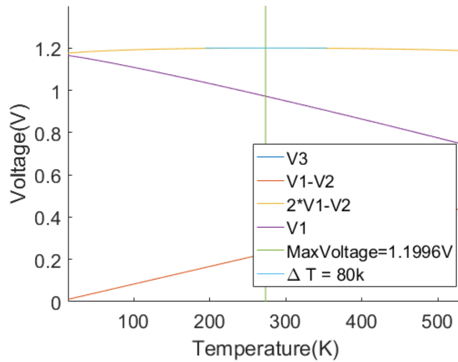

Figure 5. CTAT = V_{D1} = V1, PTAT = V1-V2, $V_{ref} \approx$ V3.

See appendix D for a more detailed explanation.

New Bandgap Reference Circuit

The used circuit is of the same design as the circuit shown in figure 4. The components will however have different values and the two diodes are replaced. D1 is under a higher amount of strain and hence has a smaller bandgap than D2. And the saturation current and ideality factor are changed in the way descried in subsection B. They are changed to make the difference in bandgap temperature independent. The PTAT voltage gets an extra term ($-\Delta E_g/Q$ here ΔE_g is in eV) This lowers the reference voltage. The effective PTAT which is equal to the voltage over R_1 is now

$$V_{R1} = \frac{R1\,Q}{R2} PTAT \tag{16}$$

$$= \frac{R1\,Q}{R2}\left(\frac{k}{q}\ln(Q)T - \frac{\Delta E_g}{q}\right) = PTAT_{eff}.$$

This can be different from PTAT, because PTAT was previously only dependent on Q because R_1 was chosen in such a way that the voltage over it would be equal to PTAT. However this is no longer the case. Now the reference voltage is dependent on a combination of Q and R_1 because the reference voltage is equal to $PTAT_{eff} + CTAT$ and Q will now also change the temperature range for which the circuit will work because PTAT has to be higher then 0V otherwise a negative current will go through the diodes.

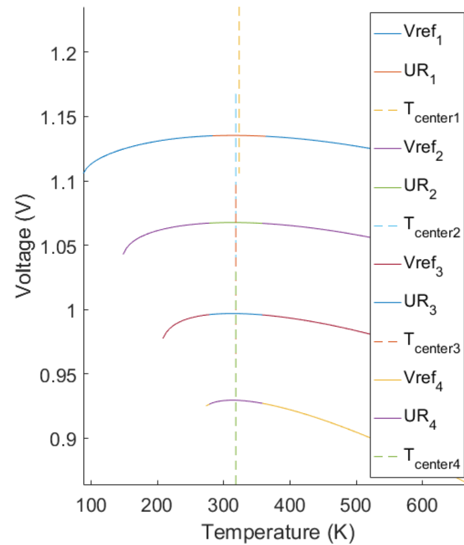

Figure 6. Close up of V_{ref} for 4 different temperatures for which the circuit is allowed to stop working. UR stands for usable range ($T_{center} \pm 40K$)

LTSpice simulations were done in order to validate the equations that were found and to demonstrate that the reference voltage could indeed be lowered. The results can be seen in figure 6. The

maximum voltage deviation in the usable range ($T_{center} \pm 40K$) is equal to 3.1 mV. This usable temperature range is found to be a reasonable expectation of the temperature range seen by consumer electronics [24]. The reference voltage is lowered by increasing the temperature (with steps of approximately 60 K) for which the circuit is allowed to to stop working and $T_{center} = 318K$. See appendix E for a more detailed explanation of the new circuit and the simulation.

6 Method/Materials

To demonstrate the effect of strain on the material bandgap and its applications in voltage references, ΔE_g vs temperature for the 3 different types of diodes, and the strain for the 3 different types of diodes as functions as a function of temperature were made. These two things have been created in two different phases. The $I-V$ curve has been determined for low (5 K to 233.15 K) and high (233.15 K to 473.15 K) temperatures. The $I-V$ curves from 5 K to 233.15 K have been measured using a cryostat, from 233.15 K to 473.15 K have been measured using a shielded wafer probe. The high and low temperature ranges both had a temperature sensor which was recorded. All 3 different types of diodes have been measured for the high temperature range. Only diode type 1 has been measured for the low temperature range. For each type of diode there is a variety with low and with high strain. The used materials of the high and low temperature range measurement setups, a step by step method of preparing the samples, taking the measurements and calculating the temperature, difference in bandgap and strain, and the real live setup can be found in appendix F. Figure 7 gives the graphical representation of the different sensors that are used. The chip containing the diodes is connected to a sample holder and the diodes are bonded to this sample holder. This is needed for the low temperature range setup and it reduces the time needed for the high temperature range measurements.

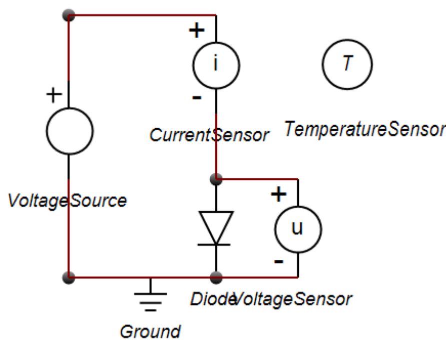

Figure 7. Graphical representation of the high and low temperature measurement setup

A 5th order polynomial fit was taken of all measured $ln(I_D/Z - V_D)$ curves. The error between the fitted and measured curves is voltage dependent because the error is expressed in ampere and the fit is taken over $ln(I_D/Z - V_D)$ which increases for higher voltages. This makes it difficult to give one final value for the error. Instead the average error of each diode is calculated and the average error of each diode type at low (o.4V) and high (The highest voltage of the measured data that was used to do the fitting) voltages is determined. These errors can be seen in appendix G, tables 16 to 19. The fitted curves for the extreme temperatures of the high and low temperature ranges can be seen in figures 8 to 11.

Temperature

The $I-V$ curves of all 6 diodes were measured using a Keithley 4200 semiconductor characterisation system. The temperature was set using a temperature test system which was connected to the chuck. This temperature test system also measured and displayed the temperature. The ideality factor was determined using the fitted values obtained from the $ln(I_D/Z) - V$ ($Z = 1$ A) curve and the measured temperature. The average error of the fitted values has been obtained by calculating the RMS (Root Mean Square) of the difference between the measured and fitted data. This was done for a couple of different voltages and all temperatures. It was decided to do the following steps to get the thermal voltage because it is easier to take a fit over the $ln(I_D/Z) - V$ curve then the $I-V$ curve

$$\frac{d(\ln(I_D/Z))}{d(V_D)} = (u_T N)^{-1} \tag{17}$$

It was found that N is indeed not equal to 1 and that it is temperature dependent. The differential of the 5th order polynomial fit is taken towards voltage. The temperature could then be found by taking the minimum value in the region where the differential was approximately constant. This minimum is then used to find the temperature. The temperature is calculated both under the assumption that the ideality factor is equal to 1 and using an estimated ideality factor. This estimated ideality factor is found by looking at which ideality factor results in the smallest error between the measured and calculated temperatures. It was found that the ideality factor was indeed close to 1 and therefore it gives a meaningful temperature indication. The average error for each diode can be seen in table 4 and each individually calculated temperature can be found in appendix G.

The temperature was also determined for the low temperature range, with the same method as

for the high temperature range. These results can be found in appendix G.

Bandgap difference

The voltage for a constant current has been found by using the polynomial fit of the $ln(I_D/Z)-V$ curve. The difference in voltage is then calculated for each temperature of each set of diodes using the roots function available in Matlab. The difference in bandgap, under the assumption that the strain is not temperature dependent, was calculated using method 1 and 2 described in appendix B. Method 1 finds ΔE_g by looking at the voltage difference at a specific current and method 2 finds ΔE_g by looking at the current ratio at a specific voltage. The result can be found in table 5. The bandgap was also calculated assuming the strain to be temperature dependent. This result can be found in appendix G figures 96 to 98. An attempt was made to find the bandgap difference using method 1 for the low and high temperature data of diode type 1. There is however a large discontinuity when the current vs the temperature vs the difference in bandgap is plotted. This means that a linear fit is not really an option. This discontinuity can be seen in appendix G, figure 120. This is also why the strain was not calculated by using the low temperature range measurements. The low temperature range measurements are discussed in more detail in the discussion.

Strain

The strain was obtained for the high temperature range of diode type 1, 2 and 3 using equations 10 and 11. The strain is dependant on the difference in bandgap. However a temperature dependent linear line is found if the difference in bandgap is plotted. This temperature dependence can be there either because the two diodes that are compared are simply not identical or because the strain is temperature dependent. This is why different results are obtained depending on what is assumed to be the case. It is very well possible that both assumptions are correct so the strain is temperature dependent and the diodes are not identical. This would make the calculations quite a bit more difficult so this is not assumed to be the case. The results for the temperature independent strain are summarised in table 6 and the results for the temperature dependent strain are summarised in appendix G. The strain has only been determined using the high temperature measurements. The reason for this will be given in the discussion.

Noise and bond wires

The sample holder has also been measured to determine if it might have influenced the measurements. These measurements were done with the high temperature range setup. The needles were placed on the sample holder and then the current was measured. The noise in the air was also measured by lifting the needles used to measure the sample holder inside the air so that they are not connected to anything else (floating). This was done for two temperatures in order to have a reference for the sample holder measurement. The results can be found in appendix G. The measurements of the sample holder and air are almost identical.

The effect of the bond wires was also measured by comparing the bonded diode d_{11} with it's own clones located on two other chips. These clones were measured by connecting the needles directly to the bond pads in the high temperature range setup. In this case the chips were glued to a wafer so they were not located on a sample holder. The results can be found in appendix G. It can be seen that the bond wires have a very large impact on the measurements because they are not the same as the measurements done without bond wires.

7 Results

Figures 8 to 11 show the fitted curves obtained from the measured ($ln(I_D/Z)-V_D$) curves for the extreme temperatures of both the high and the low temperature ranges. All the curves can be found in appendix G. The error of all individual curves can be found in tables 16 to 18, it should be noted that this is an average. The fit is taken over the $ln(I_D/Z)-V$ curve. This curve increases for an increase in voltage. This means that the error for lower voltages will be smaller then for higher voltage.

The average error for diode types 1, 2 and 3 at 0.4V and the highest voltage of each measured $I-V$ curve, for the high temperature range, can be seen in table 3. The highest voltages used to determine these errors can be seen in appendix G, figures 66 to 71. The error for the low temperature range can be seen in appendix G, table 24. D_{11}, D_{22} and D_{31} have maximum strain.

Table 3
Error of fitted curves, high temperature range.

Diode type	V=0.4V, error (A)	Highest voltage in the measured data set that was used for fitting, error (A)
1	0.071n	0.23m
2	0.030n	0.17m
3	0.216n	0.23m

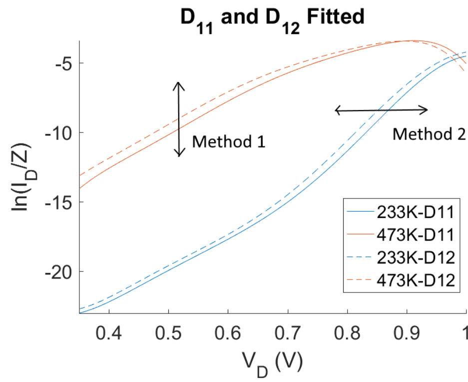

Figure 8. Forward biased ($ln(I_D/Z)-V_D$) curves of the high temperature range of diode type 1.

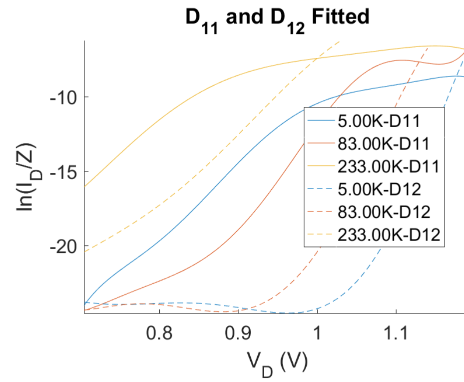

Figure 11. Forward biased ($ln(I_D/Z)-V_D$) curves of the low temperature range of diode type 1.

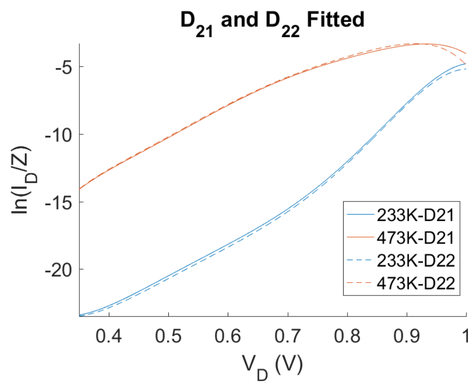

Figure 9. Forward biased ($ln(I_D/Z)-V_D$) curves of the high temperature range of diode type 2.

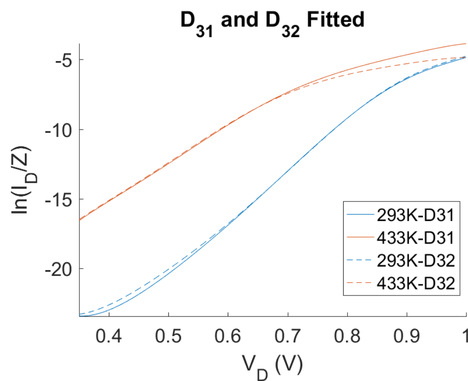

Figure 10. Forward biased ($ln(I_D/Z)-V_D$) curves of the high temperature range of diode type 3.

Figures 12 to 14 show the difference in bandgap for diode types 1, 2 and 3 if it is assumed that the difference in bandgap is caused by a temperature dependent strain. How the strain is influenced by temperature will be discussed more in the discusion. These graphs are also used by method 1, method 1 takes the difference in voltage at a specific current level. TThe point where the temperature is equal to 0 K is given in table 21. The corresponding strain can be found in appendix G

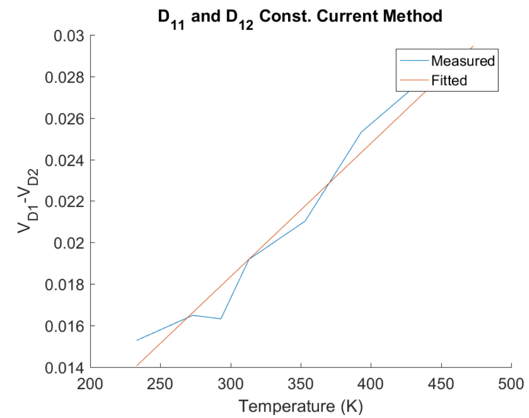

Figure 12. Difference in bandgap for diodes D_{11} and D_{12} for $I_D = 0.0025$

Figure 12 shows the fitted linear line which is equal to

$$\Delta V_D = 64\frac{\mu V}{K}T - 0.92 mV. \tag{18}$$

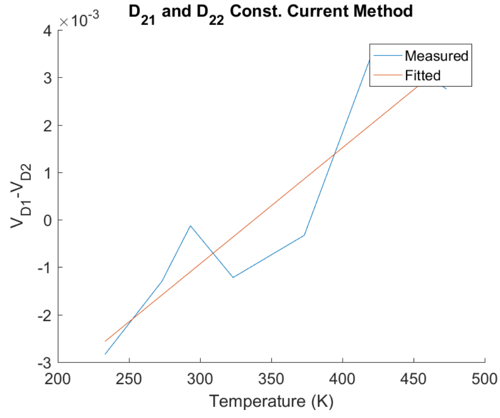

Figure 13. Difference in bandgap for diodes D_{21} and D_{22} for $I_D = 0.00012$

Figure 13 shows the fitted linear line which is equal to

$$\Delta V_D = 24.5\frac{\mu V}{K}T - 8.3mV. \tag{19}$$

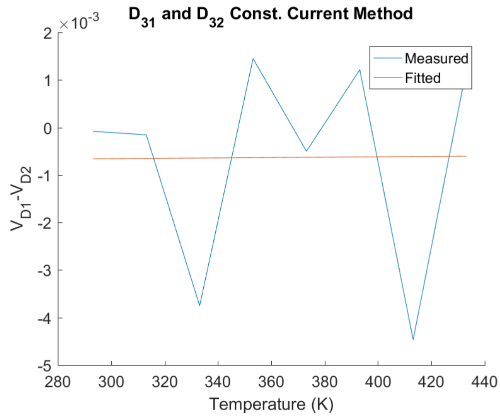

Figure 14. Difference in bandgap for diodes D_{31} and D_{32} for $I_D = 0.00012$

Figure 14 shows the fitted linear line which is equal to

$$\Delta V_D = 0.38\frac{\mu V}{K}T - 0.77mV \tag{20}$$

Table 4
Temperature results

Diode	Ideality factor	error (K)	Ideality factor	error (K)
D_{11}	1.0	30	1.10	9.4
D_{12}	1.0	27	1.10	14
D_{21}	1.0	21	1.10	10
D_{22}	1.0	25	1.10	5.3
D_{31}	1.0	5.7	0.99	3.8
D_{32}	1.0	2.5	1.00	2.5

Table 5 shows the calculated bandgap difference assuming that the strain is temperature independent. The corresponding strain can be found in table 6. The temperature dependent bandgap and corresponding strain which could be temperature dependent can be found in appendix G. Some rough calculations and guesses will show that the strain is most likely temperature dependent. This will be shown in the discussion.

Table 5
ΔE_g, results

Diode	Met 1 $I_D(mA)$	Met 1 ΔE_g (mV)	Met 2 ΔE_g (mV)	Avg ΔE_g (mV)	Error (mV)
D_{11} - D_{12}	2.49	-0.9	-2.9	-1.9	1.0
D_{21} - D_{22}	0.12	-8.3	-7.7	-8.0	0.3
D_{31} - D_{32}	0.12	-0.8	-1.8	-1.3	0.5

Table 6
Strain results

Diode	Method 1 *Strain* (%)	Method 2 *Strain* (%)	Avg Strain (%)	Error (%)
D_{11} - D_{12}	-0.006	-0.019	-0.013	0.006
D_{21} - D_{22}	-0.056	-0.052	-0.054	0.002
D_{31} - D_{32}	-0.004	-0.009	-0.007	0.002

8 Discussion

There were a couple of things which could have gone better or could have been done differently for a better result and some of the result were questionable. All of these things will be discussed here.

General

The creation of the sample holder caused almost a week delay which is about 10% of the total time, this could have been avoided by making it at the very beginning.

Chip design

The size of the bond pads on the chip gave some problems. These bond pads were about $50X50\,\mu m$ with a spacing between bond pads of about $5\,\mu m$. There were no bonding machines available that were able to bond such a size without problems. It is therefore advisable to let a company with better equipment do the bonding or to increase the spacing between and the size of the bond pads.

Diode type 1 and 2 have a ring surrounding them. This ring is meant to isolate the diodes. The problem however is that this ring is also made of NP and PP and the rings were connected to the diode itself. This is shown in figure 15. This construction means that the current can take a couple of different paths. It would have been better to have the diode disconnected from this

guard ring. This would remove a couple of the parasitic paths that the current can take.

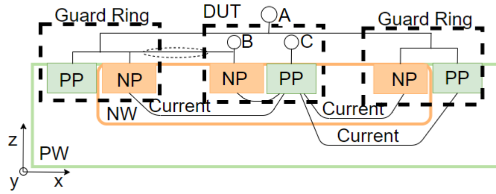

Figure 15. Graphical representation of the basic structure behind diode type 1 and 2. See table 12 for the legend. DUT stands for device under test.

Strain

The strain could have been higher if the structure of the diodes was chosen specifically to create strain and to do so in a optimal manner. This would mean that the width of the diodes is increased to make a diode with almost no strain and the width would have to be decreased to give more strain. The width of the diode is indicated by k in figure 1. There are some fabrication limits to the minimum width, however it is very likely that a diode with more strain can be realised.

An other thing is the way the strain is realised. It would perhaps be better to realise the strain by changing the width of the STI (indicated by R in figure 16) instead of the width of the diodes. This way the physical parameters of the diodes are not really changed. This can be achieved by making the diode with the layout given in figure 16. This diode is also not perfect however it might work better. The nwell indicated in figure 16 should not be made to short. This makes it so that there is less tunnelling.

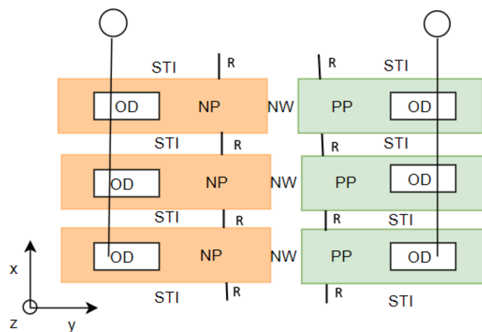

Figure 16. New diode layout. See table 12 for the legend.

An other thing that should be done differently is the structure of diode type 3 shown in figure 17. Here it was assumed that the strain is the same in the x and y directions because the STI is the same width on all sides of the diode. This is not true. 4 diodes are measured in parallel. The two diodes at the side will have a larger piece of STI bordering them (Indicated with A) and therefore experience more strain. The middle two diodes will also have a different strain in the x and y directions this is because the lengths B and C are not the same. This can be solved by changing the spacing between the diodes to be equal to the distance from the diodes to the bond pads and/or using an isolation ring to limit the STI width at the sides.

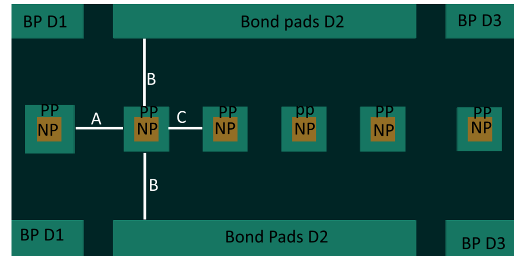

Figure 17. Diode type 3

The last thing that could be changed if the general structure of diode type 1 is going to be reused is to keep the width of the STI constant by increasing the size of the surrounding isolation boundary shown in figure 15, with the same amount as the increase in width of the diode. Currently the width of the STI and the width of the diode are both changed and both have influence on the strain.

A part of this temperature dependant strain could be due to the thermal expansion of the STI and or silicon of the the diode itself. The strain is equal to

$$\varepsilon = \frac{\Delta L}{L} \tag{21}$$

Here ΔL is the change in the width of the diode (L). Now ΔL can be calculated for diode type 2 by assuming that this change in calculated strain is purely because the strain is temperature dependent, and this temperature dependence is completely caused by thermal expansion of the STI.

The change caused by the thermal expansion would then be equal to the difference between ΔL_{233K} and ΔL_{473K}. This difference can be found in table 7

Table 7
Temperature dependent strain

Temp (K)	Strain	$\Delta L(m)$
233	-0.0227	-1.134e-10
473	0.0189	9.45e-11
Δ240	Δ0.0416	Δ2.08e-10

It is unknown what material the STI is made of, but a couple of possibly used materials are used to estimate the thermal expansion if those materials were chosen. To do this the difference

in thermal expansion of D_{21} and D_{22} will be calculated using the following equation

$$\Delta d = (d_2 - d_1)\Delta T \alpha \quad (22)$$

Here Δd is the change in d (width of the STI (m)) due to thermal expansion. ΔT is the change in temperature in Kelvin. α is the thermal expansion coefficient (K^{-1}).

The difference between the length of the STI of D_{21} and D_{22} $(d_2 - d_1)$ is taken because the only part that is of interest is the difference in expansion of d_1 and d_2. This is what could result in a temperature dependent strain. ΔE_g would not change if both d_1 and d_2 were to expand with exactly the same amount, which would mean that the difference in strain between D_{21} and D_{22} would also not change. For the other diode types the STI width is changed but also the width of the diodes themselves which is why diode type 2 is studied here.

Table 8 shows the thermal expansion of Si, SiO_2, Si_3N_4 and $C_8H_{20}O_4SI$ (TEOS). The silicon is only shown to get an idea of the expansion of the width of the diode. The initial width of the diode is 0.5 µm. $d_2 - d_1 = 2.0 \cdot 10^{-6} - 0.12 \cdot 10^{-6} = 1.88$ µm for the width of the STI and $\Delta T = 240K$.

Table 8
Temperature dependent strain

	$\alpha(10^{-6})(K^{-1})$	
Si [7]		$\Delta L(10^{-10}m)$
min	2.60	3.12
max	3.30	2.96
avg	2.95	3.54
SiO_2 [8]		$\Delta d(10^{-10}m)$
min	0.55	2.48
max	0.75	3.38
avg	0.65	2.93
Si_3N_4 [9]		$\Delta d(10^{-10}m)$
min	1.4	6.32
max	3.7	16.70
avg	2.05	9.25
$C_8H_{20}O_4SI$ (TEOS) [10]		$\Delta d(10^{-10}m)$
avg	0.4	1.8

It is very likely that the thermal expansion does in fact have a significant effect on the strain because the change in width of the diode is calculated to be 21 nm and the change in width of the diode and STI can be found in table 8 for a variety of materials.

Measurements

In the current measurements, compliance is set for the forward and reverse bias. The reverse current does not allow for the same magnitudes seen in the forward biased region. This means that the compliance has to be set lower than for the forward biased region. This means that two measurements had to be done: one for measuring the reversed bias region, the other one for measuring the forward bias region. This could be quite easily solved if the measurement program would allow for setting a lower and upper limit for the current or by measuring the diodes in multiple phases. This last one was the one that was used here. The current range was however set on best fixed for the forward biased region. This resulted in a lower current limit of 5 µA for this region, for the high temperature measurements.

The temperature could not accurately be measured for cryogenic temperatures because a room temperature thermocouple is used along with a separate sensor to monitor temperature close to the reference junction to compensate for the room temperature fluctuations. This is however not recommended for cryogenic work according to the manual [11]. This was why it was desired to get the temperature out of the $I-V$ curve.

The diodes that were measured showed behaviour that was not expected, mostly in the reverse biased region. The saturating current is for example positive and the point where it becomes negative changes with temperature. This could be due to a lot of reasons.

The first is that the diodes were simply not good (this is not very likely but it is possible see the paragraph under "Chip design").

The second possible reason could be that during the bonding some gold particles landed on the diode which make a conductive path between the two bonding pads or the bond wires are connected to two different diodes at the same time. The effect of the bond wires is checked for diode D_{11}. This diode was measured for 293 K and 473 K using the high temperature range measurement setup. The only difference was that the sample holder PCB is removed instead of the chip with the diodes that was placed on a silicon waver using PMMA (glue). The D_{11} was then measured using needles connected directly to the bond pads of the chip. The results can be seen in appendix G. Here it becomes clear that the bonding did have a large effect on the $I-V$ curves of the diodes. The "Not Bonded 2" diode shows for example a almost ideal $I-V$ curve. The "Not Bonded 1" does show some non-ideal behaviour. This could be because of current paths along the surface area. Because here the needle scratched the surface of the diode, this is however unlikely because there are quite a few protective layers on top of the diodes.

The third is that there was something wrong with the measurement equipment.

The fourth is that the PCB might conduct and that the conductance is temperature dependent. To rule this out the PCB was measured using the

high temperature range measurement setup. The result was then compared with a measurement of air. No significant difference was found. The results can be seen in appendix G.

Taking the measurements took a lot of time. This time can be reduced by writing a program that automatically takes the measurements. This is recommended especially if more then 6 different diodes have to be measured.

Simulations

A simulation tool used to see if it is possible to make a low reference voltage. LTspice crashed 2 times and some of the equations for the temperature dependence used by LTspice were not similar to the standard equation seen in [12]. And the ideality factor was also not temperature dependent. It is advised to use spectre for a more realistic result, pharps even TCAD. LTspice did not allow for changing all the settings necessary for the temperature models that should have been in the diode model. These settings are present in Hspice and it is assumed that the diode model is very similar in LTspice. It is unclear if those settings are selected automatically or if they are simply not there.

Results

The low temperature range measurements were not used because they showed behaviour that was very strange. The low temperature range gave three measurements (5K, 23K and 53K) in diode D_{11} where the forward biased current moved to the left instead of to the right. This might be because the temperature read out was completely wrong. Besides that there was the problem that the forward biased current became negative. This should not happen. An other thing that was strange was that the difference in voltage between the two diodes suddenly increased by almost a $100\,\mathrm{mV}$. This made any linear fit for the difference in voltage for different high and low temperature measurements practically useless because the data itself is not a straight line.

The main reason why it is assumed that something went wrong during this measurement is that the $I-V$ curve measured at $233\,\mathrm{K}$ in the low temperature setup was not the same as the $I-V$ curve measured at $233.12\,\mathrm{K}$ in the high temperature setup. The high temperature setup is used quite often and is known to give good results unlike the low temperature setup which was not used before in this specific configuration.

The difference in voltage for diode type 3 with a constant current for different temperatures was not a very straight line making the linear fit suspect which in turn removes quite a bit of the reliability of the difference in bandgap and strain that was calculated for this diode type.

9 Conclusion

The hypotheses said "The strain applied to a diode, if it is large enough, would cause a measurable change in bandgap which then theoretically could be used to make a temperature independent, low reference voltage". This was indeed correct. In the sections "Temperature", "Bandgap Difference" and, "Strain" the ways to determine the temperature, difference in bandgap and strain are given. These methods were then applied on three different diode types. The temperature could be determined with the maximum error being $7\,\mathrm{K}$ for D_{32} under the condition that the ideality factor is estimated. The difference in bandgap is determined to be $-2.9 \pm 1\,\mathrm{mV}, -7.7 \pm 0.4\,\mathrm{mV}$ and $-3.0 \pm 0.3\,\mathrm{mV}$ for diode types 1, 2 and 3. Under the assumption that the strain is not temperature dependent. The strain is also calculated under the same assumption and is determined to be $-0.019 \pm 0.007\%, -0.052 \pm 0.003\%$ and $0.02 \pm 0.002\%$ for diode types 1, 2 and 3. The temperature dependent ΔE_g and strain were also determined and those can be found in appendix G. These results are however only obtained by utilising the measured data obtained for the high temperature range.

It has been also discussed how the original bandgap reference circuit works and how the new bandgap reference circuit would work. It has been shown that a simulated ΔE_g can be used to lower the reference volt.

Appendix A
Temperature

Ideal I-V curve

The temperature can be found by focusing on the exponential region in the $I-V$ plot of a diode. This means that the series resistance seen at high forward bias and the recombination current or current caused by tunnelling at low forward bias are not taken in to consideration. The equation for the current through a diode is

$$I_{\mathrm{D}} = I_{\mathrm{S}}\left(e^{\frac{V_{\mathrm{D}}}{u_T}} - 1\right), \tag{23}$$

With I_{S} the saturation current and V_{D} the voltage over the diode. The -1 can be neglected when $e^{\frac{V_{\mathrm{D}}}{u_T}} >> 1$. One over the derivative towards the voltage can be taken. This is done to get the thermal voltage $u_T = \frac{kT}{q}$ hence,

$$\left(\frac{dI_{\mathrm{D}}}{dV_{\mathrm{D}}}\right)^{-1} = \left(\frac{I_{\mathrm{S}}}{u_T} e^{\frac{V_{\mathrm{D}}}{u_T N}}\right)^{-1} = \frac{u_T}{I_{\mathrm{D}}} = \frac{1}{g_{\mathrm{D}}}. \tag{24}$$

Multiplying the result with I_{D} will result in the thermal voltage

$$\frac{1}{g_{\mathrm{D}}} I_{\mathrm{D}} = u_T = \frac{kT}{q}. \tag{25}$$

T can now be calculated by multiplying the result by $\frac{q}{k}$. This is not the only way to calculate the temperature. One of the other methods would be to take the difference in voltage between two identical diodes with the only difference being the current density which ratio is also constant. This results in the following equation

$$\begin{aligned} V_1 - V_2 &= u_T \ln\left(\frac{QI_{\mathrm{D}}}{I_{\mathrm{S}}}\right) - u_T \ln\left(\frac{I_{\mathrm{D}}}{I_{\mathrm{S}}}\right) \\ &= u_T \ln(Q) = \frac{q}{k}\ln(Q)T. \end{aligned} \tag{26}$$

Here it also becomes clear that the temperature can be determined, because all parameters are known except for T. Q is the multiplier used to indicate a higher current density. The advantage of this method is that no derivative is taken. Taking the derivative increases the amount of noise. Both methods would work but for now the first method will be used. [6]

Non idealities

It is important to note that LTspice uses an extra term called emission coefficient (N) in its equations [13]. In literature, this N is called the ideality factor.

$$I_{\mathrm{D}} = I_{\mathrm{S}} e^{\frac{V_{\mathrm{D}}}{u_T \cdot N}} \tag{27}$$

The only change this gives is that T has to be calculated by multiplying by $\frac{q}{kN}$ instead of $\frac{q}{k}$ when using the first method described in the ideal I_V curve section. N is there because equation 27 assumes that no generation or recombination of electron-hole pairs takes place in the depletion region. There will be some recombination current caused by the carriers injected across the depletion region that will recombine. In addition, tunnelling either via traps (trap assisted) or phonons could also result in such non-idealities [12]. The recombination current also known as Shockley-Hall-Read current can be expressed in the following way

$$I_{\mathrm{rec}} = I_{\mathrm{ro}} e^{\frac{V_{\mathrm{D}}}{2u_T}}. \tag{28}$$

I_{ro} depends on the width of the depletion region, the recombination lifetime, and the intrinsic carrier concentration. The total current can be found by summing equation 28 and 23. Alternatively, the following approximation is used

$$I_{\mathrm{D}} = I_{\mathrm{S}}\left(e^{\frac{qV_{\mathrm{D}}}{NkT}} - 1\right) \tag{29}$$

N is approximately 1 for large forward-bias voltages when diffusion dominates, and 2 for low forward-bias voltages when recombination dominates [4], this means that the temperature has to be determined at a large forward-bias voltage. N for our experimental diodes is not known. This will give an error when determining the temperatures. This error can be minimised by using the part of the $I-V$ curve where N is close to 1. It should be noted that N could be dependent on temperature as well [3]. The -1 in equation 29 can again be neglected when the exponential term is a lot larger then -1, this means that the equation is very similar to equation 23. The following steps can then be performed to find the temperature and the ideality factor.

$$\left(\frac{d(I_{\mathrm{D}})}{d(V_{\mathrm{D}})}\right)^{-1} I_{\mathrm{D}} = \left(\frac{1}{u_T N}\right)^{-1} = \frac{NkT}{q} \tag{30}$$

Here Z is equal to 1A. Z is put there to remove the unit current because the

Simulations

A couple of simulations were done in LTspice in order to verify the equations that will be used to find the temperature. A custom diode was used for these calculations. The model for the diode was made by changing the model for the

MMSD4148 diode which was provided by LTspice. The datasheet of this diode can be found in [15].

The only changes that were made is that the bandgap is set to be equal to $1.17eV$. This is the default value for silicon in LTspice. The saturation current (I_S) is set to $0.005nA$. Originally it was $2.52nA$, it was changed because the leakage current will have to be lower in order to measure a wide temperature range. The exponential voltage dependent term in equation 23 is only dominant for a small voltage range for low temperatures. All other parameters of the diode model can be found in table 28 in appendix H.

It was decided to keep N equal to 1.752. It is expected that good diodes will be measured that have an N equal to 1 however that has to be confirmed. The LTspice circuit and the custom diode can be found in figure 18. The $\log(I_D)$ for different temperatures can be found in figure 19. The derivative of (I_D) for different temperatures can be found in figure 20. The only part of interest is between $0.2\,\mathrm{V}$ to $1.7\,\mathrm{V}$. The inverse of this part is taken and then multiplied with $\frac{qI_D}{kN}$ to get the temperature. Only the linear parts show the real temperature which is where the exponential term is dominant. Which is why those sections are shown in figure 21.

The measurement for T=273.15K was used to find N. In this case the measured temperature was assumed to be equal to the LTspice temperature. N is found to be equal to 1.752 which is equal to what N was set to be in the LTspice simulation. The calculated temperature is within $\pm 0.06\,\mathrm{K}$ to the temperature set in LTspice for all simulated temperatures. This means that N is not temperature dependent in LTspice, this is not expected to be the case in the real diodes.

```
.model Diode1 D(EG=1.17 XTI=3
+ Is=0.005n Rs=.168 N=1.752 Cjo=.64p
+ M=.4 tt=5n Iave=200m Vpk=100
+ mfg=Onsemi type=silicon)
.step param T2 -200 200 50
.dc V1 0 2 0.01
```

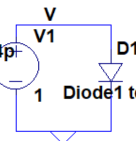

Figure 18. LTspice circuit used for the simulations.

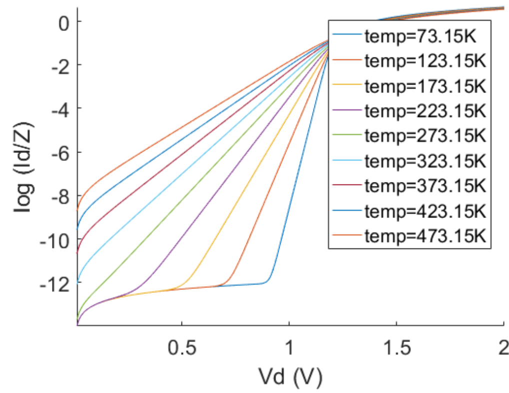

Figure 19. $\log(I_d/Z)$ for different temperatures. With $Z = 1\,\mathrm{A}$

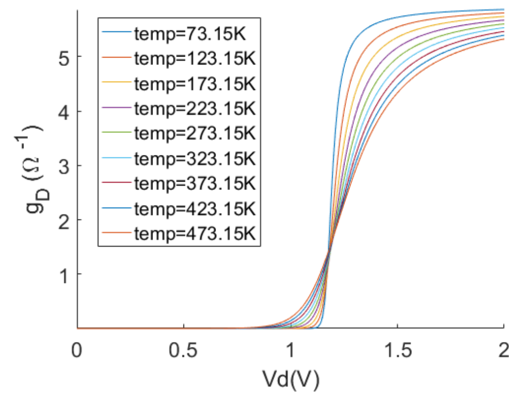

Figure 20. g_D for different temperatures.

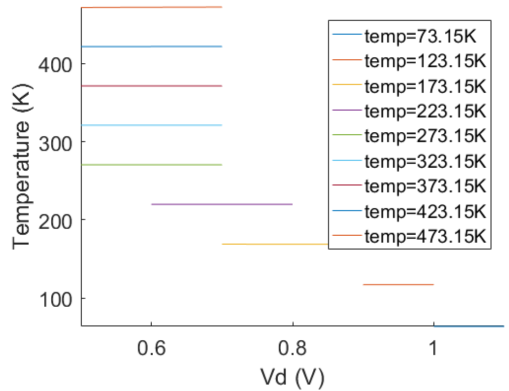

Figure 21. Temperature plots.

The final temperatures are found by finding the average temperature of the regions shown in figure 21. The error is found using equation 31.

$$error = \sqrt{(T_{LTspice} - T_{Calculated})^2} \quad (31)$$

The average error is found to be $\pm 0.02\,\mathrm{K}$. This error is found by taking the average of all the separate errors seen in table 9.

Table 9
Calculated temperature vs Temperature set in LTspice simulation

LTspice temp (K)	Calculated Matlab temp (K)	Error (K)
73.15	73.1593	0.0093
123.15	123.1529	0.0029
173.15	173.1821	0.0321
223.15	223.1609	0.0109
323.15	323.1496	0.0004
373.15	373.1442	0.0058
423.15	423.1280	0.0220
473.15	473.0890	0.0610

Appendix B
Bandgap Difference

Method 1, Voltage Difference

Theoretical

The current though the diode is given by the following equation [12]

$$I_\mathrm{D} = I_\mathrm{S} e^{\frac{V_\mathrm{D}}{u_T}} = n_\mathrm{i}^2 qA\left(\frac{D_n}{N_\mathrm{A} L_n} + \frac{D_p}{N_\mathrm{D} L_p}\right) e^{\frac{V_\mathrm{D}}{u_T}} \tag{32}$$

With u_T being equal to

$$u_T = \frac{kT}{q} \tag{33}$$

And n_i^2 is equal to

$$n_\mathrm{i}^2 = N_\mathrm{c} N_\mathrm{v} e^{\frac{-E_g}{kT}} \tag{34}$$

To simplify matter C is made equal to

$$C = qA\left(\frac{D_n}{N_\mathrm{A} L_n} + \frac{D_p}{N_\mathrm{D} L_p}\right) \tag{35}$$

The saturation current can then be described in the following way

$$I_\mathrm{S} = n_\mathrm{i}^2 C \tag{36}$$

equation 32 can be rewritten to give the voltage. The saturation current seen in equation 36 can then also be substituted.

$$V_\mathrm{D} = u_T \ln\left(\frac{I_\mathrm{D}}{I_\mathrm{S}}\right) = u_T \ln\left(\frac{I_\mathrm{D}}{C n_\mathrm{i}^2}\right) \tag{37}$$

The band gap and temperature are of interest so n_i^2 and μ_T will be expanded

$$V_\mathrm{D} = \frac{k}{q} \ln\left(\frac{I_\mathrm{D}}{C N_\mathrm{c} N_\mathrm{v}}\right) T + \frac{E_\mathrm{g}}{q} \tag{38}$$

Now the voltage over two diodes can be measured it is assumed that $CN_c N_v$ will almost be the same for both diodes. The difference in band gap can then be found by taking the difference in voltage over the two diodes. As seen in equation 39.

$$\begin{aligned} V_\mathrm{D1} - V_\mathrm{D2} = &\left(\frac{k}{q} \ln\left(\frac{I_\mathrm{D}}{C_1 N_\mathrm{c1} N_\mathrm{v1}}\right) T + \frac{E_\mathrm{g1}}{q}\right) \\ &- \left(\frac{k}{q} \ln\left(\frac{I_\mathrm{D}}{C_2 N_\mathrm{c2} N_\mathrm{v2}}\right) T + \frac{E_\mathrm{g2}}{q}\right) = \frac{\Delta E_\mathrm{g}}{q} \end{aligned} \tag{39}$$

It is however possible that there will be more differences between the diodes then only the bandgap if that is the case the difference in voltage will become equal to

$$\begin{aligned} V_\mathrm{D1} - V_\mathrm{D2} = &\left(\frac{k}{q} \ln\left(\frac{I_\mathrm{D}}{C_1 N_\mathrm{c1} N_\mathrm{v1}}\right) T + \frac{E_\mathrm{g1}}{q}\right) \\ &- \left(\frac{k}{q} \ln\left(\frac{I_\mathrm{D}}{C_2 N_\mathrm{c2} N_\mathrm{v2}}\right) T + \frac{E_\mathrm{g2}}{q}\right) \\ &= \frac{k}{q} \ln\left(\frac{C_2 N_\mathrm{c2} N_\mathrm{v2}}{C_1 N_\mathrm{c1} N_\mathrm{v1}}\right) T + \frac{\Delta E_\mathrm{g}}{q}. \end{aligned} \tag{40}$$

Now the difference in bandgap can be found by looking at the difference in voltage at 0 K

Voltage Difference Simulations

A couple of simulations were done in LTspice in order to validate the calculations. Figure 22 shows the used circuit. The used diode model is the same as in section A except for three different parameters. N is set to be equal to 1 for all diodes. The saturation current (IS) is also changed for each diode model and the bandgap is changed. ΔE_g is expected to be 0.05, 0.10, 0.15 and 0.20 eV for this simulation. Diode 1 represents the diode without strain and has therefore a bandgap of 1.17 eV. Figure 23 shows the voltage over diode 1 till 5. Figure 24 shows the difference in voltage between diode 1 and diode 2, 3, 4 and 5. Matlab is used to calculate the mean. The results of can be found in table 10.

It turns out there is a linear dependence between ΔE_g and the temperature in LTspice. This dependency was not predicted in the original equation. Which is why the LTspice models will have to be looked up. LTspice uses the following equations when working with temperature

$$egnom = EG - GAP1\Big(\frac{T_\mathrm{nom}^2}{T_\mathrm{nom} + GAP2}\Big), \tag{41}$$

$$eg(T) = EG - GAP1\left(\frac{T^2}{T + GAP2}\right). \tag{42}$$

egnom is the nominal bandgap. eg(T) is the temperature dependent gap. All the other parameters can be found in appendix H. Further,

$$facln = \frac{egnom}{u_T(T_{\text{nom}})} - \frac{eg(T)}{u_T(T)} + XTI \cdot \ln\left(\frac{T}{T_{\text{nom}}}\right) \tag{43}$$

$$I_S(T) = J_S e^{\frac{facln}{N}} \tag{44}$$

Equation 44 can then be substituted in the equation for the difference in voltage over two diodes,

$$\begin{aligned} V_{D1} - V_{D2} &= \left(\frac{k}{q}\ln\left(\frac{I_D}{I_{s1}}\right)T\right) - \left(\frac{k}{q}\ln\left(\frac{I_d}{I_{s2}}\right)T\right) \\ &= \frac{k}{q}\ln\left(\frac{I_{s2}}{I_{s1}}\right)T = \frac{k}{q}\ln\left(\frac{J_{s2}e^{\frac{facln_2}{N}}}{J_{s1}e^{\frac{facln_1}{N}}}\right)T. \end{aligned} \tag{45}$$

If the temperature independent saturation current J_{s1} and J_{s2} are both equal, then there will be a linearly temperature dependent term in the equation that gives the difference in voltage between two diodes as seen in equation 46

$$\begin{aligned} V_{D1} - V_{D2} &= \frac{k}{q}\left(\frac{facln_2}{N} - \frac{facln_1}{N}\right)T \\ &= \frac{kT}{qN}\left(\left(\frac{egnom_2}{u_T(T_{\text{nom}})} - \frac{eg_2(T)}{u_T(t)}\right.\right. \\ &\left.\left. + XTI\ln\left(\frac{T}{T_{\text{nom}}}\right)\right) - \left(\frac{egnom_1}{u_T(T_{\text{nom}})}\right.\right. \\ &\left.\left. - \frac{eg_1(T)}{u_T(T)} + XTI\ln\left(\frac{T}{T_{\text{nom}}}\right)\right)\right) \\ &= \frac{kT}{qN}\left(\frac{egnom_2 - egnom_1}{u_T(T_{\text{nom}})}\right. \\ &\left. + \frac{eg_1(T) - eg_2(T)}{u_T(T)}\right) = \frac{kT}{qN}\left(\frac{EG_2 - EG_1}{u_T(T_{\text{nom}})}\right. \\ &\left. + \frac{EG_1 - EG_2}{u_T(T)}\right) = \frac{kT}{qN}\left(\frac{-\Delta EG}{u_T(T_{\text{nom}})}\right. \\ &\left. + \frac{\Delta EG}{u_T(T)}\right) = \frac{-\Delta EG}{T_{\text{nom}}}T + \frac{\Delta EG}{N} \end{aligned} \tag{46}$$

This temperature dependent term is not what is expected so it will have to be removed an other thing that is not expected is the division by N. The division by N can be solved by making N equal to 1 which should be fine because it is expected that this will be the case and the low temperature range can not be determined if it is not equal to 1. However removing the linear temperature dependent term is a little bit more involved. This therm is caused by the egnom term in the exponent. It can therefore be removed by making $J_{s1} = xe^{-egnom_1}$ and $J_{s2} = xe^{-egnom_2}$. In the simulations this has to be done for all 5 diodes. egnom is dependent on EG, $GAP1$, $GAP2$, T and T_{norm}. EG and x are chosen, x is a multiplier and is equal for all diodes. x, $GAP1$, $GAP2$ and T_{norm} are constants and are respectively 100, $7.02e{-}4$eV/°, 1108eV°, 300.15K. The calculated values for J_s can be found in figure 22 and in table 11.

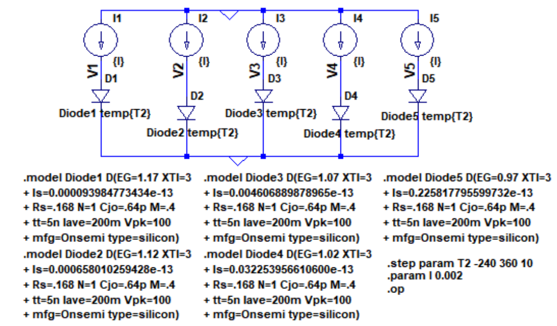

Figure 22. The circuit used for the simulation, Diode 1, 2, 3, 4, 5 have the bandgap 1.17, 1.12, 1.07, 1.02, 0.97 eV

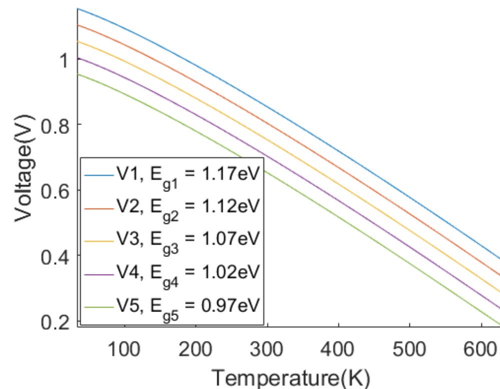

Figure 23. Plots showing the voltage over diode 1, 2, 3, 4 and 5

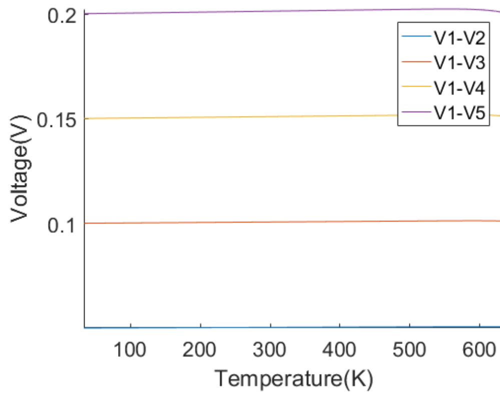

Figure 24. Plots showing the difference in voltage between diode 1 and diode 2, 3, 4, 5

Table 10
Results of the calculated values using the simulated values

$\Delta E_g(eV)$	ΔE_g LTspice (eV)	ΔE_g calculated (eV)
d1-d2	0.05	0.05
d1-d3	0.10	0.10
d1-d4	0.15	0.15
d1-d5	0.20	0.20

Table 11
Calculated values for J_S

J_S	Value 10^{-13} (A)
J_{s1}	0.000128469019975
J_{s2}	0.000887854687737
J_{s3}	0.006136000311147
J_{s4}	0.042406150847001
J_{s5}	0.293070654900693

Method 2, Current difference

This method does the opposite of method 1. Here the difference in current is taken in order to find the difference in bandgap. This method takes the difference in current,

$$\begin{aligned}\ln\left(\frac{I_{D1}}{Z}\right)-\ln\left(\frac{I_{D2}}{Z}\right)&=\ln\left(\frac{I_{S1}e^{\frac{V_d}{u_T}}}{Z}\right)-\ln\left(\frac{I_{S2}e^{\frac{V_d}{u_T}}}{Z}\right)\\&=\ln\left(\frac{I_{S1}}{I_{S2}}\right)=\ln\left(\frac{C_1 n_{i1}^2}{C_2 n_{i1}^2}\right)\\&=\ln\left(\frac{C_1 N_{c1} N_{v1} e^{\frac{-E_{g1}}{kT}}}{C_2 N_{c2} N_{v2} e^{\frac{-E_{g2}}{kT}}}\right)\\&=\ln\left(\frac{C_1 N_{c1} N_{v1}}{C_2 N_{c2} N_{v2}}\right)+\left(\frac{E_{g2}-E_{g1}}{kT}\right)\\&=\ln\left(\frac{C_1 N_{c1} N_{v1}}{C_2 N_{c2} N_{v2}}\right)-\frac{\Delta E_g}{kT}.\end{aligned}\quad(47)$$

Z is equal to 1A. This is needed because it is not allowed to take the natural logarithm of something with a unit. This method has as advantage that it does not assume that the two diodes are identical. Except for the difference in bandgap.

Method 3, Bandgap

Method three would involve calculating the bandgap of each diode individually and then taking the difference. This could be done using the following method. The saturation current is equal to:

$$I_S = n_i^2 C \quad (48)$$

With C being equal to:

$$C = qA\left(\frac{D_n}{N_A L_n}+\frac{D_p}{N_D L_p}\right) \quad (49)$$

The intrinsic carrier density is dependent on the bandgap as seen in the following equation

$$n_i^2 = N_c N_v e^{\frac{-E_g}{kT}} \quad (50)$$

$B = N_c N_v C$ in order to simplify the equation for the saturation current.

$$I_S = Be^{\frac{-E_g}{kT}} \quad (51)$$

This can be substituted in the ideal diode equation in the following way (This only holds if $\left(e^{\frac{qV_D}{kT}}\right) >> 1$)

$$I_D = I_S\left(e^{\frac{qV_D}{kT}}\right) = B\left(e^{\frac{qV_D}{kT}-\frac{E_g}{kT}}\right) \quad (52)$$

This equation can be rewritten to give the band gap for a constant current

$$V_D = \frac{k}{q}\ln\left(\frac{I_D}{B}\right)T - \frac{E_g}{q} \quad (53)$$

Here it is quite clear that a linear line will be obtained as a function of T (the current should be a constant). The bandgap can then be found at the point were the temperature is equal to 0K [21]. ΔE_g can be found by determining E_g for two identical diodes with one having more strain than the other and then taking the difference in bandgap between the two.

Method 4, Light

An other more direct method to determine the band gap difference is to measure the photons that are produced by the diodes. The energy of the photons can be expressed by the following equation:

$$E_p = \frac{hc}{\lambda} \tag{54}$$

This energy is equal to the bandgap $E_g = E_p$ (photonic bandgap) [20]. This method will not be used due to the fact that specialised measurement equipment is needed and all the data needed to find ΔE_g when using method 1 is already obtained because the same data was also used for determining the temperature. An other thing is that the effective photonic bandgap would be measured.

Appendix C
Strain

Relation between bandgap and strain

The strain, ε and bandgap E_g have a direct relation [14]. The strain is equal to the relative deformation of the silicon:

$$\varepsilon = \frac{\Delta L}{L}. \tag{55}$$

There are two possible strains. One is a shear type while the other is a deformation along the crystal axes. The shear type is not relevant because the deformation is caused by a force along the crystal axis. Usually all the valleys in the conductive band of silicon are at the same energy level but this changes when strain is applied. This strain will make it so that there will be two different band minima. The offset of the valleys can be calculated with the band deformation model using equation 56 and 57. k indicates one of the three valley pairs corresponding to a large momentum in the k direction. $\varepsilon_{xx}, \varepsilon_{yy} and \varepsilon_{zz}$ are the strain in the x, y and z direction. ε_{kk} is the strain in the direction k.

$$\Delta E_{c,k} = \Xi_d(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \Xi_u \varepsilon_{kk} \tag{56}$$

$$\Delta E_{v,k} = -a(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \pm \sqrt{\frac{b^2}{2}((\varepsilon_{xx} - \varepsilon_{yy})^2 + (\varepsilon_{yy} - \varepsilon_{zz})^2 + (\varepsilon_{xx} - \varepsilon_{zz})^2)} \tag{57}$$

Where $\Xi d, \Xi u, a$ and b are the deformation potentials. These constants can be found in table 14 [14]. ΔE_g can be calculated. It is also known that ΔE_g is equal to

$$\Delta E_g = -\Delta E_c + \Delta E_v \tag{58}$$

Diode types

Three different diodes will be studied. Each diode gets strain using a different method. The legend for figure 25 till 29 can be found in table 12 The amount of strain is unknown because the production method is unknown. This is unknown because the diodes are made by an external supplier. The general layout and direction of the applied strain will now be discussed. Diode type 1 can be seen in figures 25 and 26. Here the strain is applied in the x direction. The strain increases due to a decrease in length k while at the same time Δk also decreases because the trench isolation (STI) layer (which is responsible for the deformation) next to the NP and PP region becomes smaller. This will not have as much effect as the change in k because the STI layer is quite long, so a relative small change there will not influence the strain much. Diode type 1 has two variation (D_{11} and D_{12}) with the distance k being the only difference between the two, see table 13.

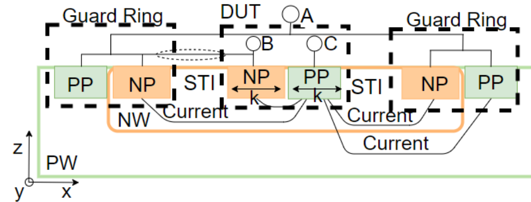

Figure 25. Diode type 1, side view, variants of diode 1 have different k.

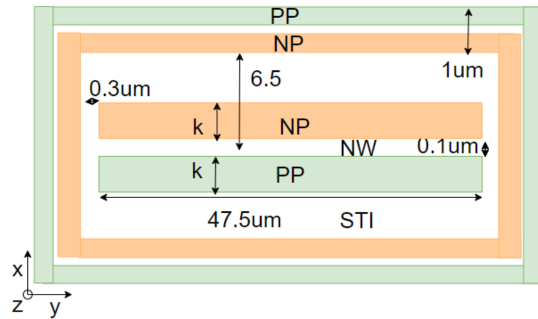

Figure 26. Diode type 1, top view, variants of diode type 1 have different k.

Diode type 2 can be seen in figures 27 and 28. This diode gets a different strain using a different method then diode 1. The STI is added by first etching some material away. The sides of the etched hole are then not completely straight if this etching is done on a very small stroke of material. The sides will become straighter when the thickness (d) is increased. This change in form will influence the strain applied to the material. It is expected that here the strain is applied mostly in the x direction.

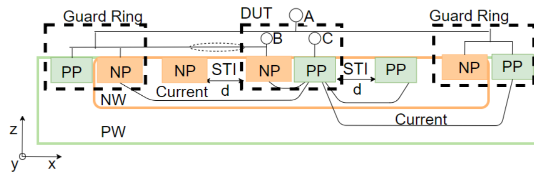

Figure 27. Diode type 2, side view, variants of diode type 2 have different d.

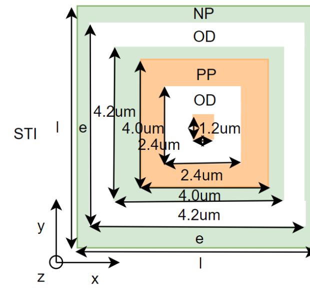

Figure 29. Diode type 3, top view, variants of diode type 3 have different e and l.

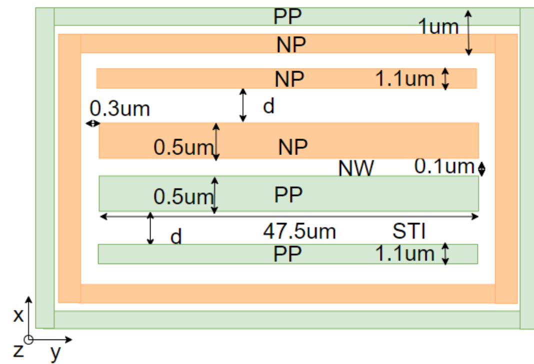

Figure 28. Diode type 2, top view, variants of diode type 2 have different d.

Table 12
Legend for figure 26 till 29

Symbol	Description
NP	n type silicon
NW	n well
PW	p well
PP	p type silicon
OD	active area
STI	Shallow trench isolation
k, d, l, e	dimensions that are varied

Table 13
Dimensions for figure 26 till 29

Type	Name	Length (μm)
Type 1	D_{11}	k=0.67
	D_{12}	k=2.1
Type 2	D_{21}	d=0.12
	D_{22}	d=2.0
Type 3	D_{31}	l=6.1 e=5.6
	D_{32}	l=8.0 e=7.5

Diode type 3 is shown in figure 29. This diode gets a different strain by changing the width l. When this width is increased the strain will become less. Because Δl stays almost the same (the change in the STI layer will lower it a bit but it should not be as much as the effect of the change in l) so $\frac{\Delta l}{l}$ will become less. The main difference between diode type 1 and 3 is that for the latter the strain originates from 2 directions. Namely the x and y directions. This diode also has one other length that changes namely e. This means that the active area increases in size. This diode type changes parameters in two dimensions this means that more things will change and that the assumption that they will almost be identical with the only difference being strain is no longer completely correct. In this case less can be said about the certainty that the difference in voltage between the two diodes is really only caused by the change in bandgap. Unless the second method explained in appendix B is used. Four of these diodes are connected in parallel.

Poisson's ratio

ΔE_c and ΔE_v are only dependent on the strain and a couple of constants. When a strain is applied in one direction, for example the x direction, it will also be known for all other directions. The strain in all other directions can be calculated using Poisson's ratio. This means that the strain in the y and z direction for diode type 1, 2 can be expressed in the following way for diode types 1 and 2:

$$\varepsilon_{yy} = -\sigma_{100} \cdot -\varepsilon_{xx} \tag{59}$$

$$\varepsilon_{zz} = -\sigma_{100} \cdot -\varepsilon_{xx} \tag{60}$$

The strain in the y and z direction will be positive (tensile), the strain in the x direction will be negative (compressive).

The strain in all directions can also be determined when an equal strain is applied in two directions, as is the case in diode type 3. In this

case the applied strain will be in the x and y directions. This means that the strain in the y and z direction can be found using the following equations:

$$\varepsilon_{yy} = -\varepsilon_{xx} \tag{61}$$

$$\varepsilon_{zz} = -2\sigma_{100} \cdot -\varepsilon_{xx} \tag{62}$$

ε_{kk} can be found by taking the strain which will give the minimal ΔE_c so minimal energy. The strains in the x and y direction are higher then the strain in the z direction and equal to each other. This is why the following relation is chosen for ε_{kk}

$$\varepsilon_{kk} = -\varepsilon_{xx} \tag{63}$$

The same reasoning also holds for diode type 3. In this case the highest strain will be the strain in the x direction.

$$\varepsilon_{kk} = -\varepsilon_{xx} \tag{64}$$

Equations 59 to 64 can be substituted in equations 56 and 57 to get the equations for ΔE_c and ΔE_v for diode type 1, 2 and diode type 3. Equations 65 and 66 give the equations for diode types 1 and 2. Equations 67 and 68 give the equations for diode type 3.

$$\Delta E_{c,D1,D2} = -\Xi_u \varepsilon_{xx} - \Xi_d \varepsilon_{xx}(1 - 2\sigma_{100}) \tag{65}$$

$$\Delta E_{v,D1,D2} = a\varepsilon_{xx}(1 - 2\sigma_{100}) \pm \sqrt{b^2 \varepsilon_{xx}^2 (1 + \sigma_{100})^2} \tag{66}$$

$$\Delta E_{c,D3} = -\Xi_u \varepsilon_{xx} - \Xi_d \varepsilon_{xx}(2 - \sigma_{100}) \tag{67}$$

$$\Delta E_{v,D3} = a\varepsilon_{xx}(2 - \sigma_{100}) \pm \sqrt{b^2 \varepsilon_{xx}^2 (1 + \sigma_{100})^2} \tag{68}$$

These equations in combination with equation 58 can then be used to find the relation between the strain and ΔE_g. There are two possible solutions (indicated with the $\pm$ sign) when the resulting equations are rewritten to get the strains as a function of ΔE_g for diode types 1, 2 and 3. This is due to the light and heavy hole bands. The light hole band will increase when strain is applied ($\pm$ will therefore be $+$) while the heavy hole band will decrease ($\pm$ will therefore be $-$). This in turn means that $max(\Delta E_v)$ will obtained by focusing on the light hole band [18]. The resulting equation that takes the light hole band in to consideration for diode type 1, 2 can be seen in equation 69. The equation for diode type 3 can be seen in equation 70. Figure 30 shows the plots of these equations. Ξ_u, Ξ_d, a, b are all deformation constants and can be found in table 14.

$$\varepsilon_{xx,D1,D2,LH} = \frac{-\Delta E_{g,D1,D2,LH}}{b - \Xi_u - a - \Xi_d + (2\Xi_d + 2a + b)\sigma_{100}} \tag{69}$$

$$\varepsilon_{xx,D3,LH} = \frac{-\Delta E_{g,D3,LH}}{b - \Xi_u - 2a + 2\Xi_d + (\Xi_d + a + b)\sigma_{100}} \tag{70}$$

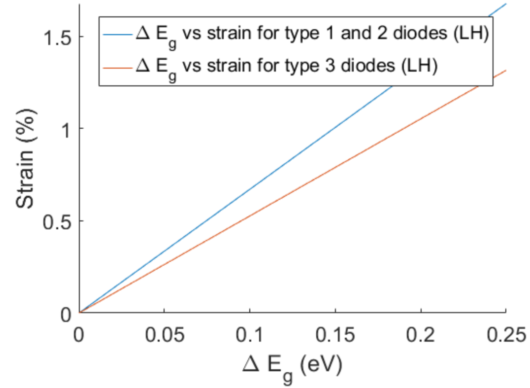

Figure 30. Strain of diode types 1, 2 and 3

Table 14
σ is obtained from [22]. All other constants are obtained from [19].

properties	Silicon
σ_{100}	0.2783
$\Xi_u(GPa)$	10.5
$\Xi_d\ (GPa)$	1.1
$a(eV)$	2.1
$b(eV)$	-2.33

Appendix D
Conventional Voltage Reference circuit

The voltage reference circuit is a quite commonly used circuit [1]. In this section the conventional bandgap voltage reference circuit will be explained and a couple of simulations will be done to see whether the explanation is correct.

Theoretical background

The bandgap reference circuit relies on the fact that the voltage over a diode decreases with higher temperature, this voltage is called the complementary to absolute temperature voltage (CTAT). While the difference in voltage between two diodes, one of which its active area is Q times larger, increases with temperature. This voltage increases linearly and is often called proportional

to absolute temperature voltage (PTAT). The sum of CTAT and PTAT will almost be constant for different temperatures. The voltage will not be completely linear due to CTAT. Figure 31 shows the circuit. V1 is equal to CTAT and the voltage over R1 is equal to PTAT. V3 is equal to the sum of CTAT and PTAT.

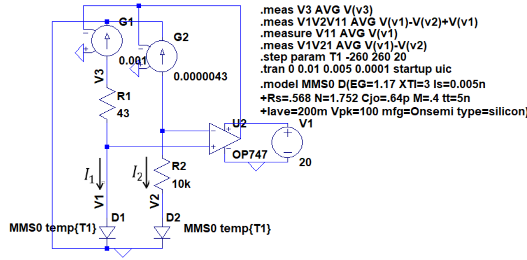

Figure 31. Conventional bandgap reference voltage circuit [6].

The current though diode 1 and 2 can be expressed using the following equation

$$I_D = I_S e^{\frac{V_D}{u_T}} \tag{71}$$

$u_T = \frac{kT}{q}$ can be substituted and the voltage can then be determined in the following way.

$$V_D = \frac{kT}{q} \ln\left(\frac{I_D}{I_S}\right) \tag{72}$$

The diodes are equal enough in dimensions that it is possible to say that the saturation current is equal in both diodes. The current though the diodes is not equal. The current though diode 2 is equal to

$$I_{D2} = \frac{I_{D1}}{Q}. \tag{73}$$

Q is in this case the amount of diodes that are put in parallel, the combination of all these diodes in parallel is called diode 2 (D2 shown in figure 31). So the current is equally divided over all diodes that are in parallel. An easier way to model this is to simply take one diode and give it Q times less current. The voltage over diode 1 and two can then be expressed in the following way

$$V_{D1} = \frac{kT}{q} \ln\left(\frac{I_{D1}}{I_S}\right), \tag{74}$$

$$V_{D2} = \frac{kT}{q} \ln\left(\frac{I_{D1}}{QI_S}\right). \tag{75}$$

V_{D1} is equal to V1 in figure 31. The difference between V_{D1} and V_{D2} is then

$$V_{D1} - V_{D2} = \frac{kT}{q} \ln\left(\frac{I_{D1}}{I_S}\right) - \frac{kT}{q} \ln\left(\frac{I_{D1}}{QI_S}\right) = \frac{kT}{q} \ln(Q) \tag{76}$$

This difference is equal to PTAT. The current going though R2 is determined using a feedback loop. A voltage controlled current source get a voltage from the opamp which in turn takes the difference between V1 and V2 plus the voltage over R_2. The voltage provided by the opamp becomes stable for the point where

$$V_{R2} + V_{D2} = V_{D1} \tag{77}$$

.

This condition also demonstrates that PTAT can be found over R2 in the following manner

$$V_{R2} = V_{D1} - V_{D2} = \frac{kT}{q} \ln Q. \tag{78}$$

This shows that the current does indeed become stable and that the voltage over R_2 is equal to PTAT. The current though R_2 is then equal to

$$I_2 = \frac{V_{R2}}{R_2} = \frac{V_{D1} - V_{D2}}{R_2} = \frac{\frac{kT}{q} \ln(Q)}{R_2} \tag{79}$$

The current that goes though R_1 is then equal to

$$I_{D1} = QI_{D2}. \tag{80}$$

In this case Q is equal to

$$Q = \frac{I_{D1}}{I_{D2}} = \frac{0.001}{0.0000043} \approx 233 \tag{81}$$

Q can be found by starting at 1 and then increasing it. Q is good the moment that the maximum reference voltage is found at the temperature at which the circuit is expected to work. This gives the least amount of deviation in the voltage for a change in temperature. The voltage over R_1 has to be equal to PTAT so it has to be equal to the voltage over R_2. The current though R_1 is Q times higher so R_1 can be determined if R_2 is known

$$R_1 = \frac{R_2}{Q} \approx \frac{10000}{233} \approx 43 \tag{82}$$

It is possible to not use this relation and instead simply choose R_1 such that it for example amplifies PTAT. So that It is possible to choose a smaller Q. Or the opposite could be done. So R_1 would then attenuate PTAT which would mean that Q has to become bigger. For this example it was decided not to do this in order to simplify the calculations.

a couple of conditions which have to be met in order for the circuit to function properly will now be discussed. The entire circuit is dependent on the fact that the diodes are operated in the exponential region of the $I-V$ curve. This means that the circuit will no longer work if they leave that region. This is more likely to happen for very low and very high temperatures due to the series resistor which plays a more important role at high temperatures and recombination current which takes a more important role at low temperatures.

Simulations

A couple of simulations were done in LTspice in order to verify the equations. A custom diode was used for these calculations. The model for the diode was made by changing the model for the MMSD4148 diode. This diode is provided in LTspice. The datasheet of this diode can be found in [15]. The only changes that were made is that the bandgap is set to be equal to 1.17V. This is the default value for silicon in LTspice. The saturation current is set to 0.005nA. It was 2.52nA, this is changed in order to make sure the circuit still works for low temperatures. The used opamp is the 747 opamp. The datasheet can be found in [16].

The simulation is performed by doing a transient simulation for 0.01 seconds. Then the average voltage is taken between 0.005 and 0.01 seconds for V1, V2, V3. This transient simulation is repeated for different temperatures. In this case the temperatures are between -260 and 260 degrees, the step size is 20 degrees. The results of these simulations are seen in figure 32. The reference voltage (V3) is set to be maximum for $T_{\text{center}} = 273.15\,\text{K}$. The voltage at this point is $1.1996\,\text{V}$. The interesting part is to see how much deviation there is in this voltage. Circuits are not normally used for extremely cold or warm environments which is why it was decided to focus on the voltage deviation between $T_{\text{center}} - 40$ and $T_{\text{center}} + 40$ kelvin. This is a range of $80\,\text{K}$ and is indicated in figure 31 by the name ΔT. This range is magnified in figure 33. This figure shows the reference voltage measured at V3 and the reference voltage that would have been obtained if CTAT and PTAT ware added without the use of R_1. They are almost identical, the small difference is most likely due to a rounding error. The difference between the highest and the lowest voltage in this range is determined to be $1.06\,\text{mV}$.

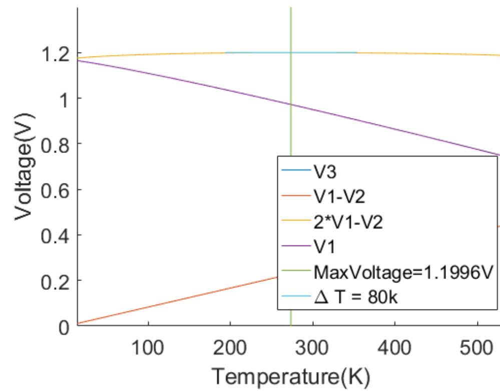

Figure 32. CTAT = V1, PTAT = V1-V2, $V_{\text{ref}} \approx$ V3.

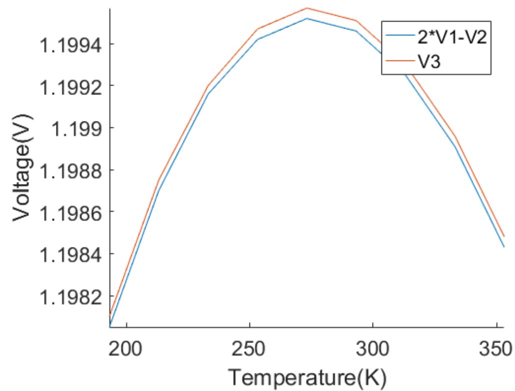

Figure 33. The deviation over the temperature at maximum voltage $\pm 40\,\text{K}$.

Appendix E
New Voltage Reference circuit

In this section the new and hopefully improved bandgap reference circuit will be explained and a couple of simulations are done in order to confirm the equations that should describe the circuit.

Theoretical background

The new bandgap reference circuit is identical to the original circuit seen in figure 31. The difference is in the diodes that are used in the simulation that can be found in figure 34. The diodes have been changed to give a temperature independent E_g when the difference in voltage is taken. The way to do this is described in appendix B. The diodes in this circuit do not have the same bandgap. This means that when the difference between diode 1 and 2 is taken there will be a offset plus a linear temperature dependent term caused by the different currents going through the diodes. As seen in equation 83. This equation uses the same assumptions as equation 39 and 80.

$$
\begin{aligned}
V_1 - V_2 &= \left(\frac{k}{q}\ln\left(\frac{I_{d1}}{C_1 N_{c1} N_{v1}}\right)T + \frac{E_{g1}}{q}\right) \\
&\quad - \left(\frac{k}{q}\ln\left(\frac{I_{d2}}{C_2 N_{c2} N_{v2}}\right)T + \frac{E_{g2}}{q}\right) \\
&= \left(\frac{k}{q}\ln\left(\frac{QI_{d2}}{C_1 N_{c1} N_{v1}}\right)T + \frac{E_{g1}}{q}\right) \\
&\quad - \left(\frac{k}{q}\ln\left(\frac{I_{d2}}{C_2 N_{c2} N_{v2}}\right)T + \frac{E_{g2}}{q}\right) \\
&= \left(\frac{k}{q}\ln(Q)T - \frac{\Delta E_g}{q}\right) = PTAT \qquad (83)
\end{aligned}
$$

It now becomes clear that the new circuit should work however it does have a couple of disadvantages. This first one is that the circuit will not work for temperatures when PTAT is negative

$$
\frac{kT}{q}\ln(Q) - \frac{\Delta E_g}{q} >= 0. \qquad (84)
$$

This means that

$$
T >= \frac{\frac{\Delta E_g}{q}}{\left(\frac{k}{q}\ln(Q)\right)} = \frac{\Delta E_g}{k\ln(Q)}. \qquad (85)
$$

So the minimal temperature can be decreased by increasing Q or decreasing ΔE_g. This also has an influence on the reference voltage because the reverence voltage is equal to CTAT plus PTAT. CTAT is the voltage over diode 1 and will be a little bit higher then an identical diode with the bandgap of relaxed silicon because the bandgap has been decreased by 0.05V. PTAT will now add $-\Delta E_g$ which will lower the reference voltage. An other problem is that Q now influences the usable temperature range so it can not be used to set $max(V_{ref})$ to the center operating temperature of the circuit in order to minimise the voltage swing of the temperature range for which a circuit is designed, without also changing the usable operating temperature range of the circuit. This is not desirable which is why resistor R1 will be used to set $max(V_{ref})$ to the center operating temperature of the circuit. The voltage over R1 is $V_{R1} = R1 I_{R1}$. The current though R1 is equal to QI_{R2} and $I_{R2} = (V_{D1} - V_{D2})/R2$ combining this will give the following equation for the voltage over R1

$$
\begin{aligned}
V_{R_1} &= \frac{R_1 Q}{R_2} PTAT = \frac{R_1 Q}{R_2}\left(\frac{k}{q}\ln(Q)T - \frac{\Delta E_g}{q}\right) \\
&= PTAT_{eff} \qquad (86)
\end{aligned}
$$

Simulations

Lets for the sake of argument assume that the desired center temperature is 273K. And the reference voltage has to be as low as possible. The operating range is $\pm 40K$. This means that Q will have to be decreased until the minimum temperature for which the circuit still works is equal to 233K. Then R1 has to be increased until $max(V_{ref})$ is located at 273K. The circuit seen in figure 34 is used to demonstrate the effect of the ratio Q and the size of R1 and to validate the equation mentioned above. 4 different scenarios are simulated. Scenarios 1 to 4 want to know what $max(V_{ref})$ will be for T_{break}(the minimum temperature for which the circuit works) is $88K, 148K, 210K$ and $273K$ and $T_{center} = 313K$ with an operating temperature range of $\pm 40K$. It is expected that $max(V_{ref})$ will become lower because Q will have to be decreased to increase T_{break} which means that R1 will have to be increased to set $T_{center} = 313K$. Which means that the offset caused by ΔE_g will become larger which will reduce $max(V_{ref})$. The plots of the different simulations are shown in figures 35 to 38. A close up of V_{ref} for all 4 simulations is shown in figure 39. The final results are also shown in table 15. This does not mean that 0.930 V is indeed the lowest possible reference voltage. This reference voltage is dependent on the temperature dependent leakage current. Because if the voltage over diode 1 decreases faster for higer temperatures it would mean that R_1 would have to be increased which would mean that V_{ref} would decrease. So these simulations really only give an indication of what would happen.

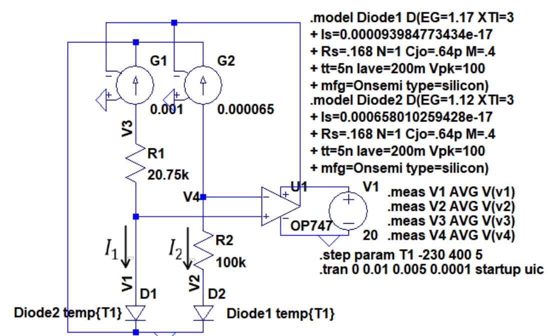

Figure 34. New bandgap reference voltage circuit [6].

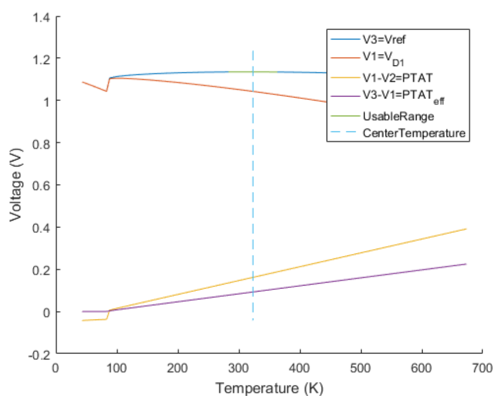

Figure 35. Simulation 1.

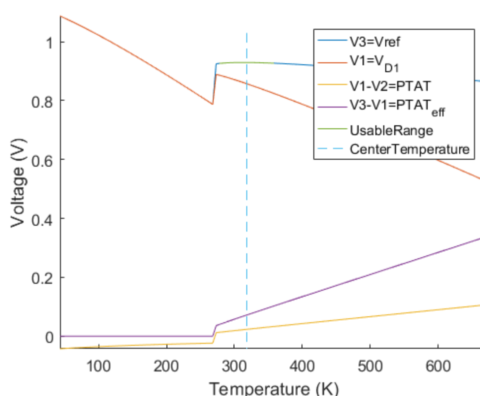

Figure 38. Simulation 1.

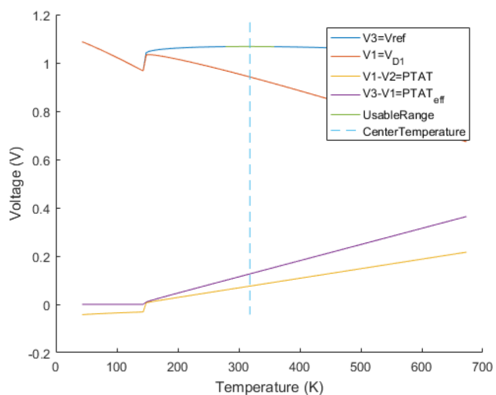

Figure 36. Simulation 1.

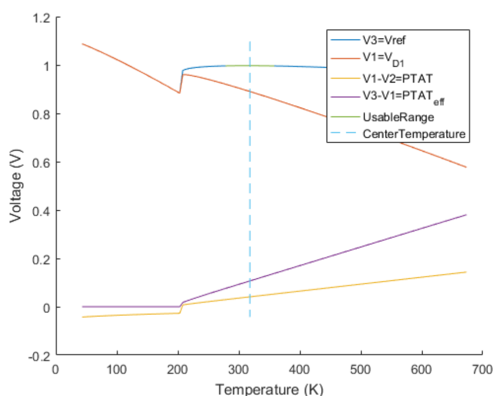

Figure 37. Simulation 1.

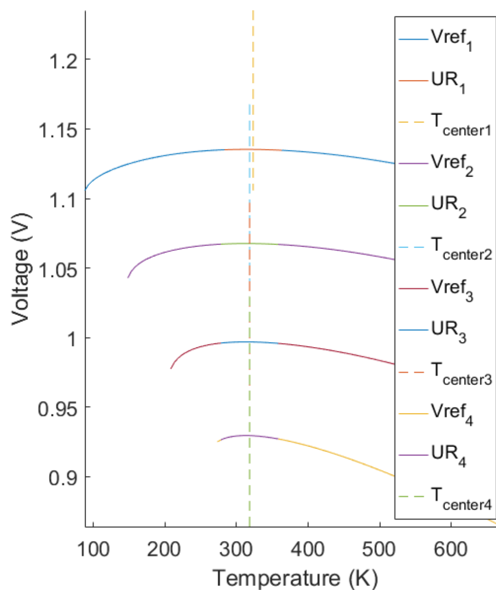

Figure 39. Close up of V_{ref} for simulation 1 to 4.

Table 15
Values of G_2 and R1 and simulations results for all 4 simulations.

Parameters and results of the simulations	Value
$G_2 \cdot 10^{-5}$	
Sim 1	0.5
Sim 2	1
Sim 3	3.5
Sim 4	6.5
$R1(\Omega)$	
Sim 1	28.8
Sim 2	1.69k
Sim 3	9.35k
Sim 4	20.75k
$T_{\text{center}}(K)$	
Sim 1	323
Sim 2	318
Sim 3	318
Sim 4	318
$T_{\text{break}}(K)$	
Sim 1	88
Sim 2	148
Sim 3	210
Sim 4	273
$max(V_{\text{ref}})(V)$	
Sim 1	1.135
Sim 2	1.068
Sim 3	0.997
Sim 4	0.930
$\Delta V_{\text{ref}}(mV)$	
Sim 1	0.660
Sim 2	0.670
Sim 3	1.071
Sim 4	3.076

Appendix F
Method/Materials

Method

Preparation of the diodes

The following steps were performed to bond the diodes to the sample holder.

1) The PCB was cleaned using acetone.
2) The chip with the diodes was connected to the PCB shown in figure 40 using PMMA. The PCB was made by a company. The glued PCB was then put on a hot plate for 30 minutes at 80°.
3) The diodes were bonded to the PCB, the PCB was made so that the gold bond wires are as short as possible. This was done to prevent the connection to the chip from breaking for very high and low temperature. The bonding was done using the tpt HB16 bonding machine. The result of the bonding for diode types 1 to 3 can be seen in figure 42 to 44. The position of the different diode types can be seen in figure 41.

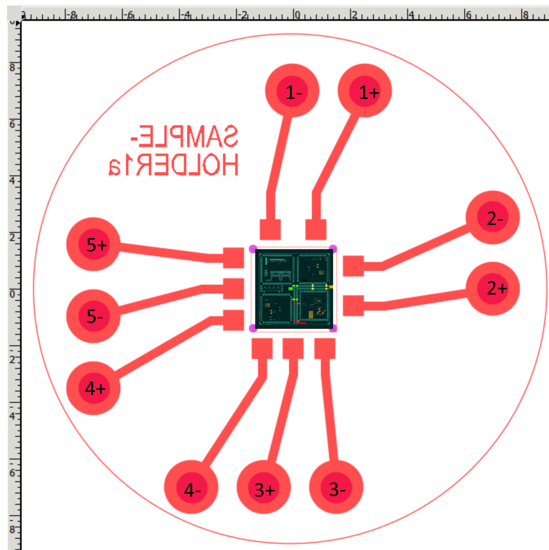

Figure 40. Sample holder PCB, the measurement at the top and to the left are in mm

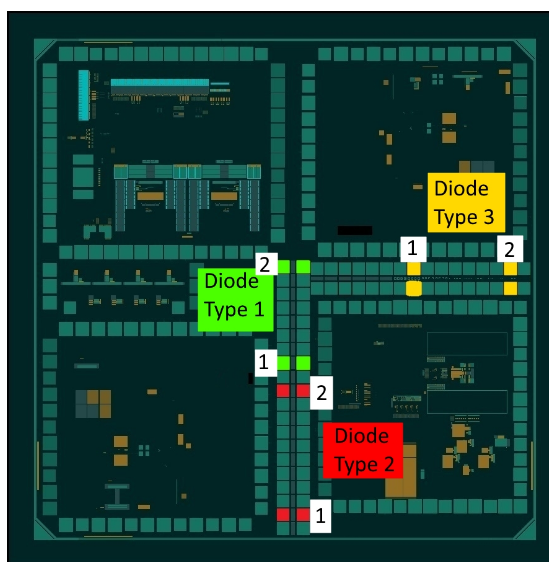

Figure 41. Chip layout

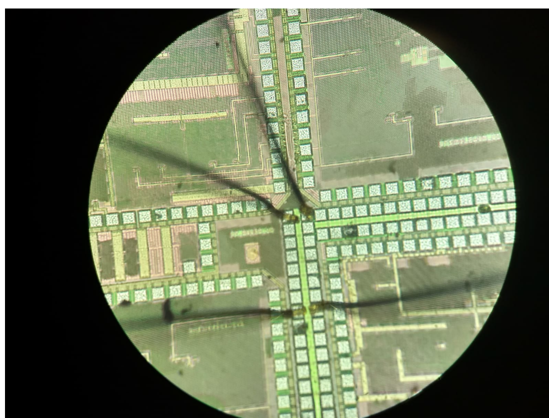

Figure 42. Diodes D_{11} and D_{12}

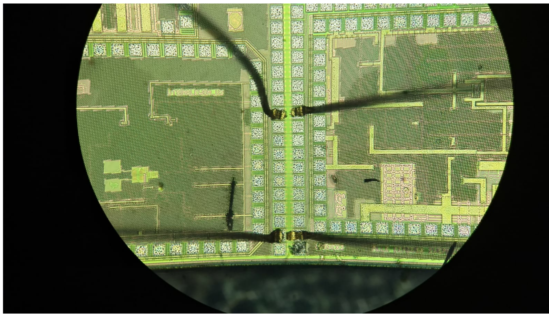

Figure 43. Diodes D_{21} and D_{22}

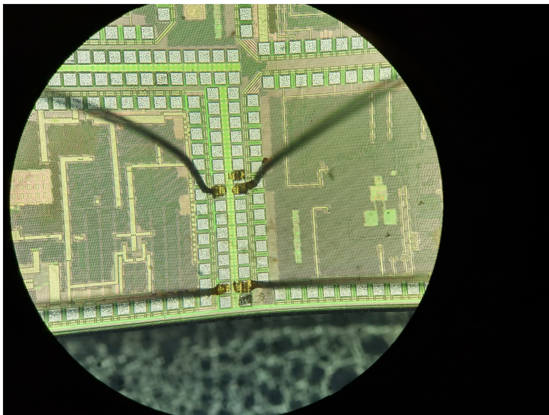

Figure 44. Diodes D_{31} and D_{32}

High Temperature Range

The following preparation steps were taken to set up the measurement setup used to measure the I-V curves and temperatures for the high temperature range:

1) The PCB was placed on a wafer covered with tape. This was done to prevent shorting the diodes.
2) The wafer was placed in the probe shield on the chuck. The wafer was connected to the chuck by pulling vacuum beneath the wafer. The probe shield can be seen in figure 45 and the chuck can be seen in figure 46.
3) The chuck was positioned so that the microscope inside the probe shield was centred on the chip.
4) The probe was connected to the PCB pads that were in turn connected to the diode using bond wires. The probe can be seen in figure 45.
5) The temperature was set using the control unit seen in figure 45.
6) Waiting on settling time was at least 5 minutes from the moment the desired temperature has been reached.
7) The I-V curve was measured using the characterization system shown in figure 45. The settings were as follows. Swept voltage range: -10.5V to 1V, step size: 0.005V. The compliance was 1 µA. Without any light. A second measurement was taken without any light, a voltage range: 0V to 1.2V, a compliance of (0.025A). The two different setting configurations can be seen in figures 47 and 48.
8) The timing settings were as follows. Delay factor was 1.3, this was the same delay factor as the "Quiet" setting. Filter factor was 2, this means that two measurements were averaged. A/D aperture time was 1, this means that the measurement time of each sample was equal to the period of the power line.
9) Read the temperature from the temperature control unit. The temperature that was measured was the temperature at the chuck.
10) Then steps 3 till 6 were repeated until all desired temperatures for all 6 diodes were measured.
11) All measurements were done without light sources.

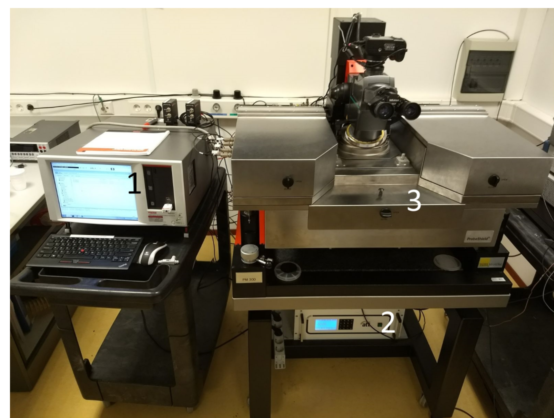

Figure 45. Measurement setup with closed probe shield. 1 is the Semiconductor characterization system, 2 is the advanced temperature test system and 3 is the probe shield

Figure 46. Measurement setup with opened probe shield. 4 are the probes and 5 is the chuck

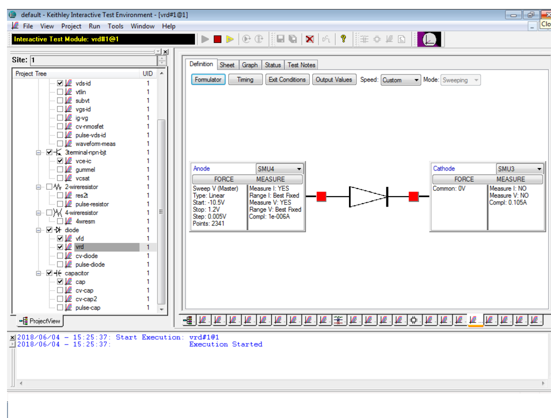

Figure 47. Settings 1

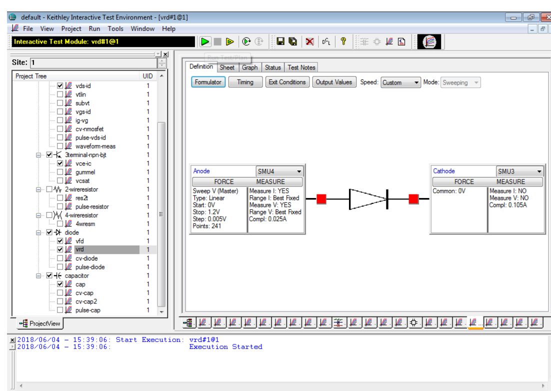

Figure 48. Settings 2

Low Temperature Range

1) The PCB was connected to the probe shown in figure 49. A close up of the sample can be seen in figure 50.
2) The probe was then placed inside the cryostat shown in figure 51.
3) The air around the sample was replaced by helium to remove the normal air which will condense for low temperatures. This was done using the diagram vacuum pump.
4) The probe of the cryostat had one cable coming out. This cable was made up of 12 wires which was in turn connected to a matrix rack from Tudelft. The wires connected to the diodes were found using a multimeter.
5) The helium shown in figure 52 was then pumped into the cryostat using the Gast pump. The temperature of the cyrostat was controlled using the temperature controller shown in figure 53.
6) All measurements were done without light shining on the diodes.
7) the same characterization system that was used for the high temperate range. The only two differences being the settings. Now the current range was set on automatic and the step size for the temperatures 233 K and 203 K was set to 0.05 V instead of the 0.005 V that was used for all other measurements.

Figure 49. Sample holder probe, used in the cryostat.

Figure 50. Close up of the PCB connected to the probe.

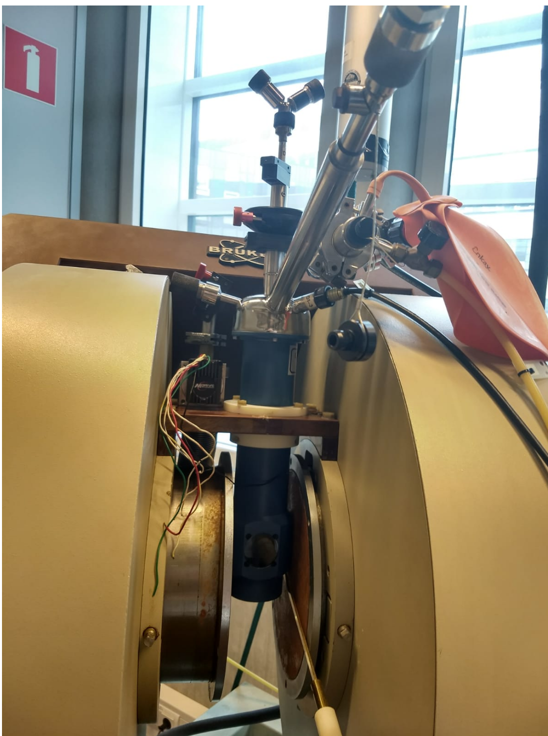

Figure 51. Cryostat.

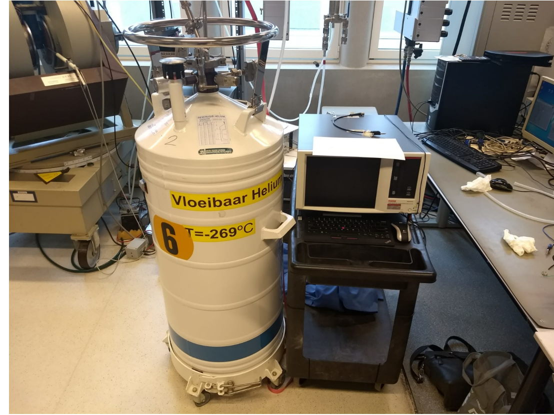

Figure 52. Helium pressure vessel and semiconductor characterization system.

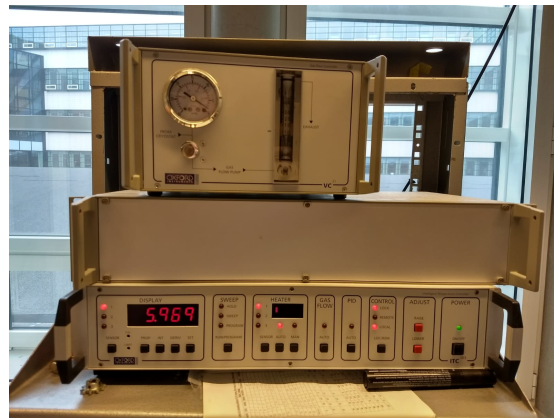

Figure 53. Temperature controller.

Temperature

The temperature was determined by performing the following steps

1) The two separate measurements were combined for each temperature, see figures 54 to 59.
2) The "bad data" was removed and a 5th order polynomial fit was taken over the $ln(I_D/Z)$, see figures 60 to 65. The bad data was there because the compliance was set on 20 mA with a best fixed range. This means that the allowable range was equal to 105 mA to 0.005 mA [23]. This 5 µA was indeed the lower limit for the forward bias measurement seen in the figures 54 to 59. The range was set to automatic for the low temperature measurements so here there was no bad data that had to be removed.
3) The average error between the measured and the fitted curves is calculated for each individual curve. The results can be seen in tables 16 to 18 for the high temperature ranges and table 23 shows the

low temperature range. The fit is taken over the $ln(I_D/Z) - V$ curve. This will increase for higher voltages. That means that when the error is calculated as a current it will also be voltage dependent. Higher voltages will give an higher error then lower voltages. This is shown in table 19 for the high temperature range and table 24 shows this for the low temperature range.

4) The gradient was determined from the fitted data. The gradient of the measured data was also determined to confirm that it was the correct gradient, see figures 72 to 77. Only the graphs of 3 temperatures per diode were shown in order to improve visibility of the graphs.
5) The straightest part was chosen and then the ideality factor for different temperatures and voltages was calculated for the high temperature range (here the temperatures were already known), see figures 84 to 89. The different data points for the ideality factor were interpreted in order to obtain the smooth colour plot.
6) Then the temperatures for both the high and low temperature ranges were determined (assuming that the ideality factor was equal to 1) by looking at the relevant straight parts of the $ln(I_D/Z) - V_D$ curves. The temperature was then calculated using the ranges seen in figures 78 to 83 for the high temperature range and figures 114 and 115 for the low temperature ranges. and the average error for the high temperature range data between the calculated and measured values was calculated for each diode. Using the following equation

$$error = \sqrt{mean((\vec{T}_{calculated} - \vec{T}_{measured})^2)} \tag{87}$$

Here $\vec{T}$ was a vector containing all the temperatures measured for the high temperature range of a diode. This error can be seen in table 4. This was not done for the low temperature range due to the $I - V$ curves of the three lowest temperature measurements of diode D_{11}. These show that the temperature error would become extremely large.
7) The previous step was repeated however this time the ideality factor was estimated by trying to find the minimum average error. The resulting error and estimated ideality factor can be found in table 20.

Difference in bandgap

The difference in bandgap was determined from the data obtained for the high temperature setup, because data from the low temperature setup showed anomalies like shifting the the left for lower temperatures, by using the following steps

1) The measured data points of each diode type were compared, to see if the fitting did not cause some kind of significant error in ΔE_g. See figures 90 to 92.
2) The fitted data points of each diode type were compared, to see whether the bandgap was indeed calculated correctly. See figures 93 to 95.
3) The difference in voltage of the fitted 5th order polynomial $ln(I_D/Z) - V$ curves was calculated for all currents between 3×10^{-7} A to 0.0025 A using the roots function provided by Matlab. The voltage over diode 2 was subtracted from the voltage over diode 1, for each diode type.
4) This was done for each temperature of each diode.
5) The result was plotted against the measured temperature. This was done for a range of currents and can be seen in figures 96 to 98. Figures 99 to 101 show the difference in voltage for one constant current.
6) The difference for one constant current was a descending line which means that ΔE_g can be found by looking the $T = 0$ K if it was assumed that the strain was temperature independent. A linear fit was then taken to find the values at $T = 0$ K. The result can be seen in table 21
7) The difference in bandgap was also calculated using method 2 described in section B. The Constant voltage each temperature was chosen inside the exponential region of the $I - V$ curve that was also used for determining the temperatures. The difference in current vs $1/T$ and the fitted linear line can be seen in figures 102 to 104. The corresponding ΔE_g can be found in table 21.
8) The average ΔE_g was calculated by taking the mean of the ΔE_g obtained using method 1 and 2. The average error was then found by looking at the absolute difference between the average ΔE_g and the ΔE_g obtained using method 1.

Method 1 for obtaining the difference in bandgap has been applied to the combined data of the low and high temperature range of diode type 1. This is done to show that the combined data does indeed give strange result. The resulting plot of current vs temperature vs difference in bandgap can be seen in figure G.

Strain

ΔE_g was found for the high temperature range. Equations 69 and 70 were used to find the corresponding strain. This was done for the assumption that the strain was temperature dependent and that method 1 was used to obtain the bandgap. See figures 105 to 107. The strain was also calculated under the assumption that it was not temperature dependent. In this case the strain was calculated for the obtained ΔE_g of method 1 and 2. The results can be found in table 22. The average was taken of the strain that was calculated by utilising the ΔE_g of method 1 and 2. Then the absolute difference between this average and the strain obtained from the ΔE_g of method 1 equals the error.

PCB sample holder

The PCB sample holder was also measured. This was done in the high temperature range setup. The Needles of the measurement shield were placed directly on the sample holder to see whether it conducts. The result can be seen in appendix G.

Bond wires

The effect of the bond wires was also measured in the high temperature range setup. Here 2 chips with the same diodes were glued to a waver using PMM. This was the same chip as the one that was placed in the sample holder. D_{11} was then select for each chip using needles. This was done for 293 K and 473 K. The results can be seen in appendix G.

Materials

Preparing the diodes

This is a list of all the used materials for preparation of the diodes

- Bonding machine "Accelonix, tpt HB16"
- Gold wire
- PMM glue
- acetone
- Isopropyl alcohol
- PCB sample holder
- Chip with diodes, 65nm CMOS technology, Taiwanese Semiconductor Manufacturing Company, TSMC

High Temperature Range

This is a list of all the used materials for the high temperature measurements

- Sample holder PCB with chip, per sample holder 2 diodes of one type.
- Probe shield SUSS Micro Tec.
- Advanced Temperature Test System, Control Unit M300, Serial No. 030-01886.
- Semiconductor characterization system, 4200-SCS, Keithley Instruments Germany.
- Probes with needles.

Low Temperature Range

This is a list of all the used materials for the low temperature measurements

- Cryostat
- Helium in a gas and liquid state. The liquid helium is kept in a pressure vessel.
- Intelegent temperature controller, ITC503, Oxford instruments.
- Gas flow controller, Oxford instruments.
- Matrix Rack Tu Delft.
- Fluke 179 true RMS multimeter.
- Pump, Model DOA-V122-FD, Gast manufactering inc.
- Diaphragm vacuum pump amd 1, Serial no.: 30407106.

Appendix G
Results

High temperature range

Full I-V plot with error

Figures 54 to 59 show the measured $I-V$ plots of all diodes. Here an error is seen in the forward bias region. This anomaly was caused by the measurement settings of the semiconductor characterization system. It can be seen that the $I-V$ curves move to the right for lower temperatures. The Z seen in the label of the y axis is equal to 1 A.

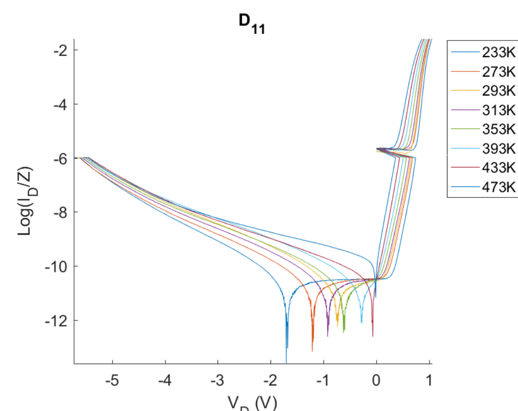

Figure 54. D_{11}, the complete $log(I_D/Z) - V_D$ curve, with error.

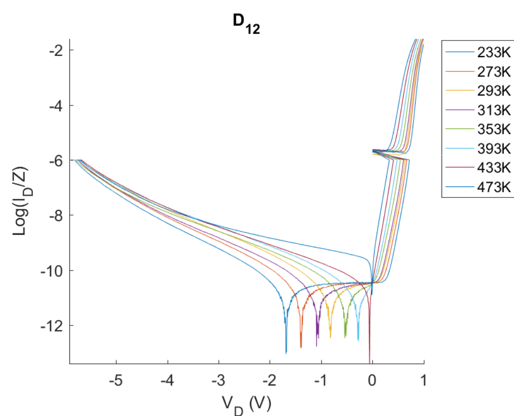

Figure 55. D_{12}, the complete $log(I_D/Z) - V_D$ curve, with error.

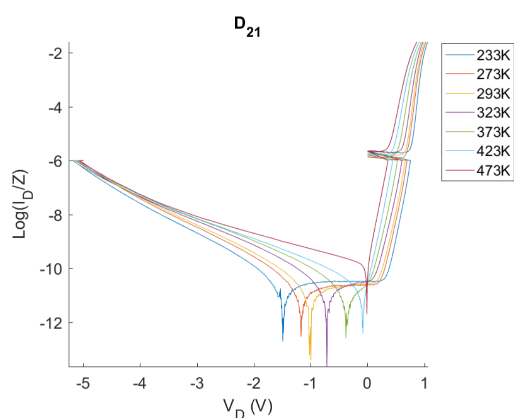

Figure 56. D_{21}, the complete $log(I_D/Z) - V_D$ curve, with error.

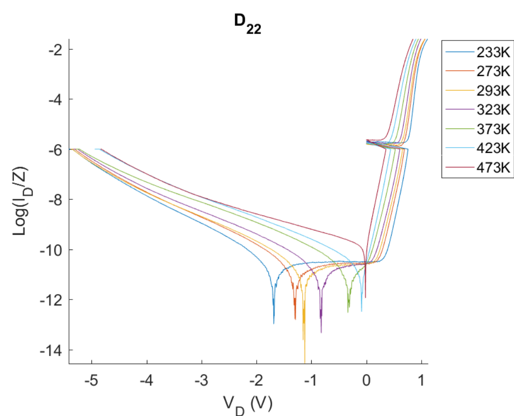

Figure 57. D_{22}, the complete $log(I_D/Z) - V_D$ curve, with error.

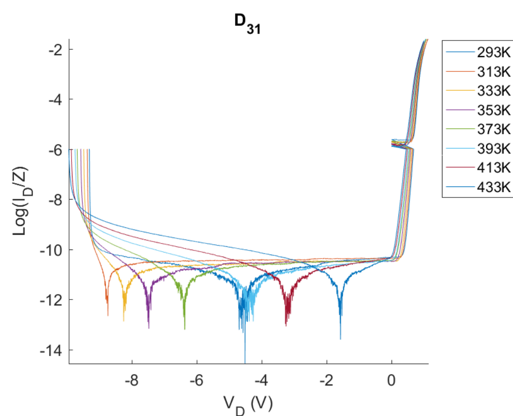

Figure 58. D_{31}, the complete $log(I_D/Z) - V_D$ curve, with error.

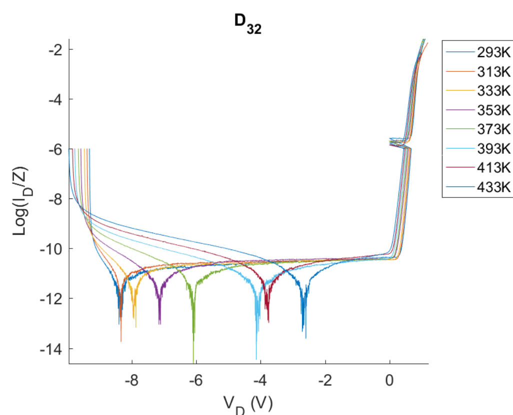

Figure 59. D_{32}, the complete $log(I_D/Z) - V_D$ curve, with error.

Full I-V plot without error

Figures 60 to 65 show the measured $I - V$ plots of all the diodes without the error mentioned in the previous section.

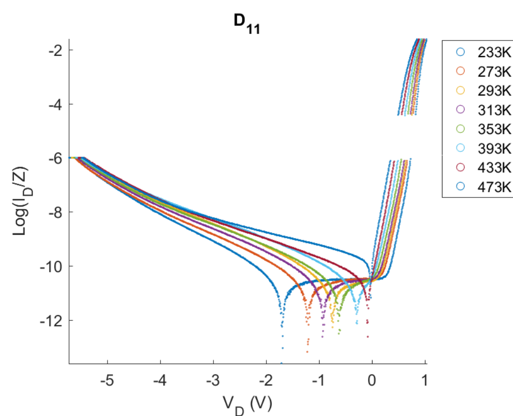

Figure 60. D_{11}, the complete $log(I_D/Z) - V_D$ curve, without error.

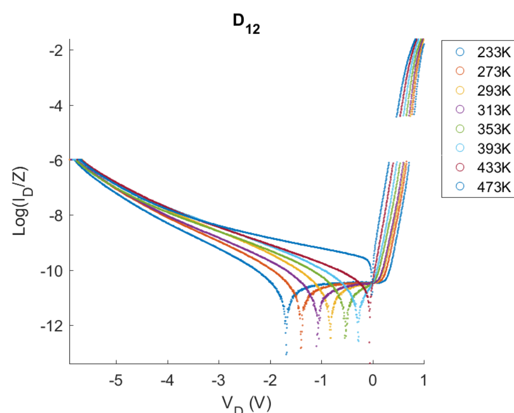

Figure 61. D_{12}, the complete $log(I_D/Z) - V_D$ curve, without error.

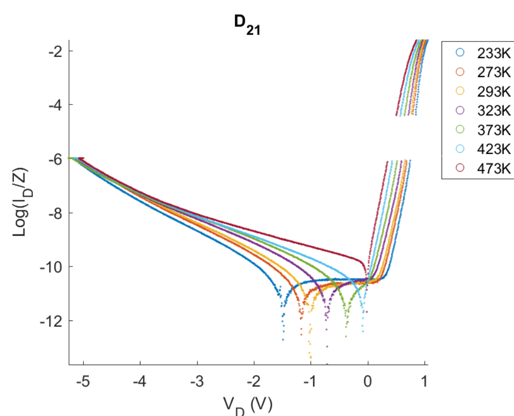

Figure 62. D_{21}, the complete $log(I_D/Z) - V_D$ curve, without error.

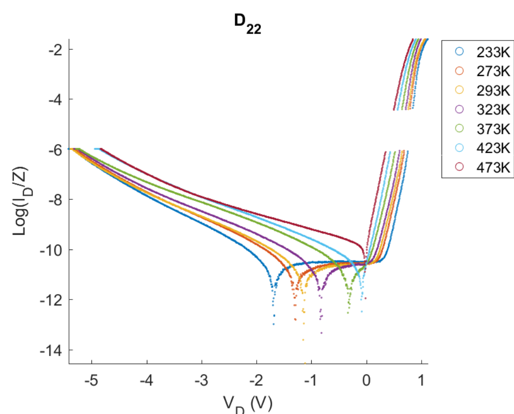

Figure 63. D_{22}, the complete $log(I_D/Z) - V_D$ curve, without error.

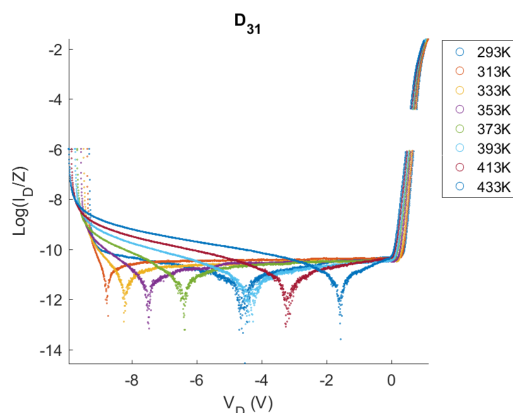

Figure 64. D_{31}, the complete $log(I_D/Z) - V_D$ curve, without error.

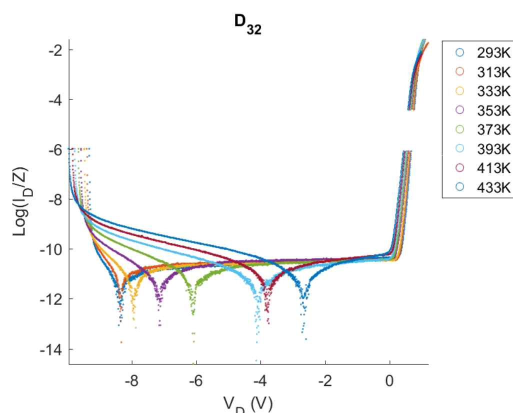

Figure 65. D_{32}, the complete $log(I_D/Z) - V_D$ curve, without error.

Plot with fitted curves

Figures 66 to 71 show the measured $I - V$ plots of all the forward biased region of the diodes along with a fitted curve, M stands for measured data and F stands for fitted data. It can already be seen that for lower temperatures the $I - V$ curve of of diode type 1 and 2 change. For lower temperatures the recombination current becomes higher.

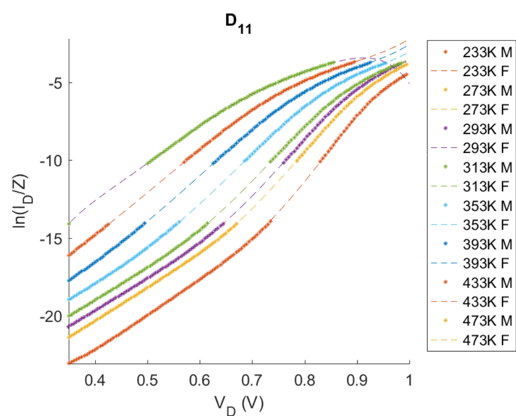

Figure 66. D_{11}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

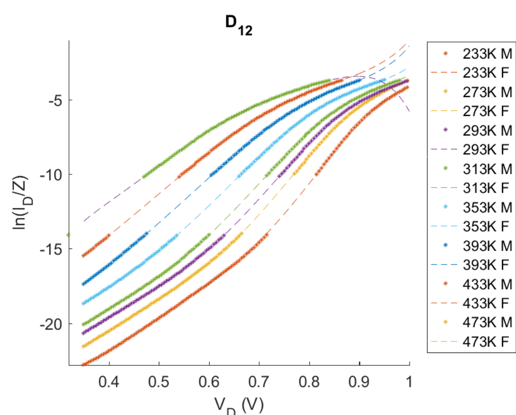

Figure 67. D_{12}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

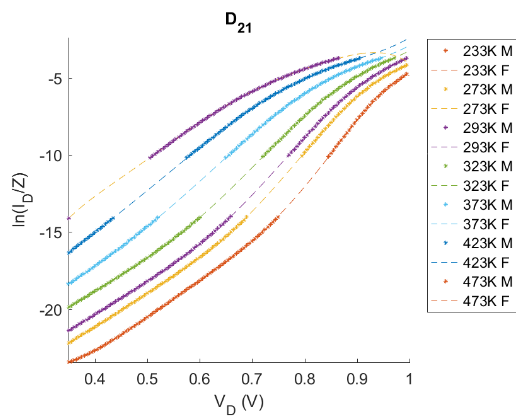

Figure 68. D_{21}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

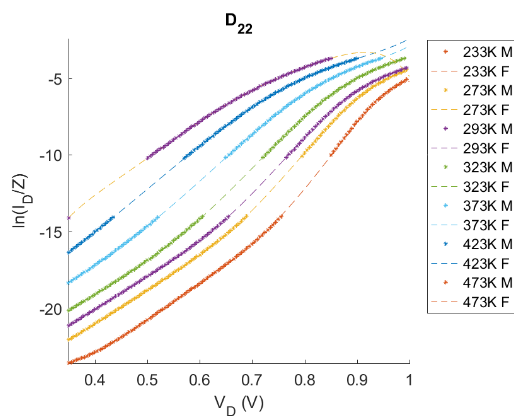

Figure 69. D_{22}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

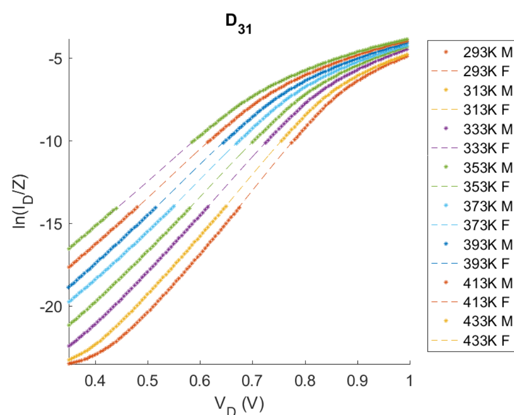

Figure 70. D_{31}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

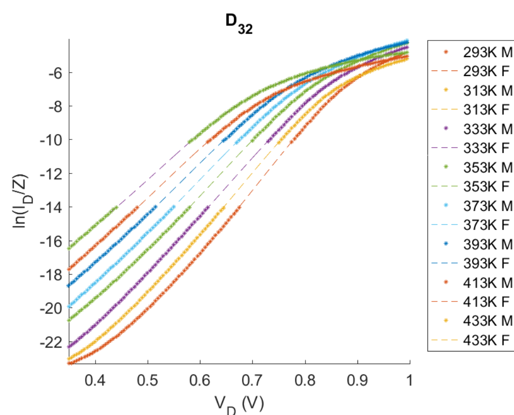

Figure 71. D_{32}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

Tables 16 to 19 show the average error for each temperature and diode. The last one shows the average error for each diode type at a specific voltage. The fit is taken over a log which means that the error expressed in current will increase for higher voltages.

Table 16
RMS of Fitted data for diode type 1

Temperature (K)	$D_{11}(10^{-5}A)$	$D_{12}(10^{-5}A)$
233	0.0262	0.1183
273	0.0597	0.0808
293	0.0641	0.0624
313	0.0129	0.0301
353	0.0089	0.0183
393	0.0024	0.0067
433	0.0006	0.0057
473	0.0015	0.0009
Average	0.0220	0.0404

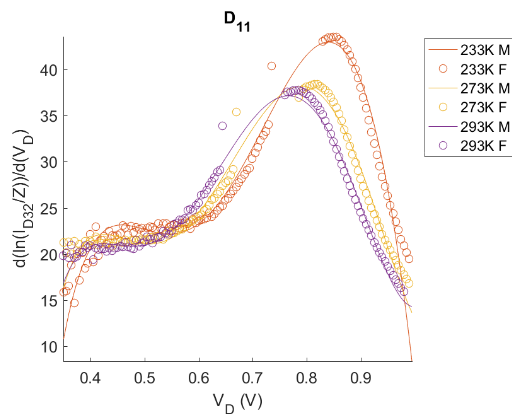

Figure 72. D_{11}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

Table 17
RMS of Fitted data for diode type 2

Temperature (K)	$D_{21}(10^{-5}A)$	$D_{22}(10^{-5}A)$
233	0.0522	0.0667
273	0.0575	0.1334
293	0.0360	0.0836
323	0.0047	0.0242
373	0.0003	0.0027
423	0.0018	0.0018
473	0.0005	0.0014
Average	0.0218	0.0448

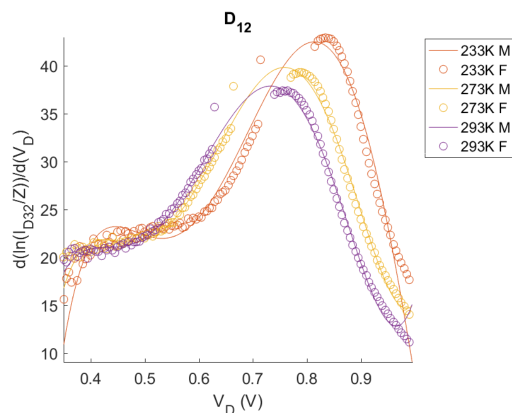

Figure 73. D_{12}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

Table 18
RMS of Fitted data for diode type 3

Temperature (K)	$D_{31}(10^{-5}A)$	$D_{32}(10^{-5}A)$
293	0.0428	0.0411
313	0.0230	0.0250
333	0.0421	0.0415
353	0.0602	0.0388
373	0.0474	0.0508
393	0.0424	0.0543
413	0.0099	0.0148
433	0.0181	0.0062
Average	0.0357	0.0341

Table 19
Error of fitted curves, high temperature.

Diode type	V=0.4V, error (A)	Highest voltage in the measured data set that was used for fitting, error (A)
1	0.071n	0.23m
2	0.030n	0.17m
3	0.216n	0.23m

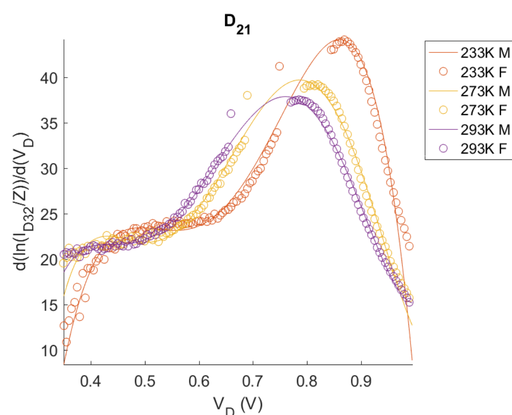

Figure 74. D_{21}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

Differential plot of the current with respect to voltage for measured and fitted data points

Figures 72 to 77 show $(d(ln(I_D/Z))/d(V_D))$, M stands for measured data and F stands for fitted data. Only a three plots per temperature are shown to improve readability. The measured data and fitted data are both shown to prove that the fited data does indeed give correct values.

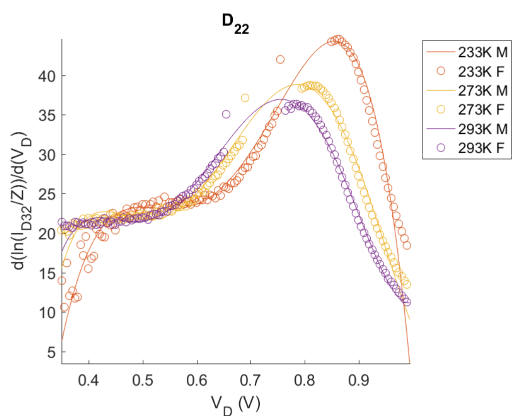

Figure 75. D_{22}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

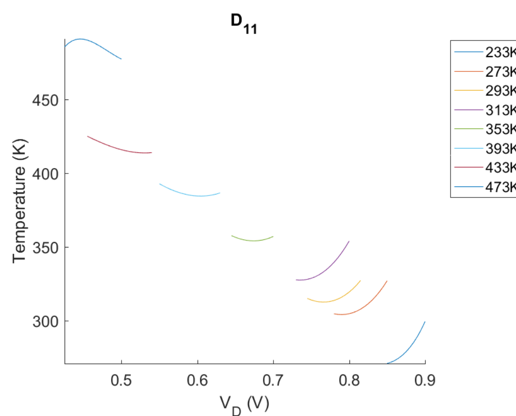

Figure 78. D_{11}, Temperature.

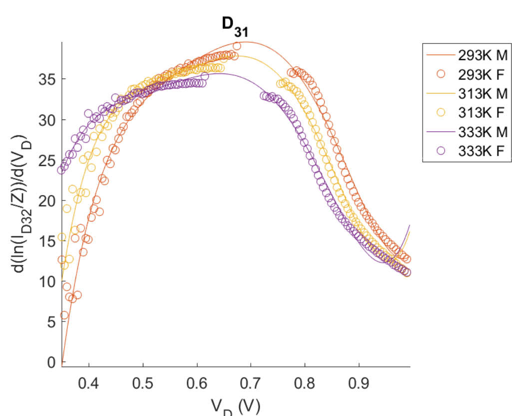

Figure 76. D_{31}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

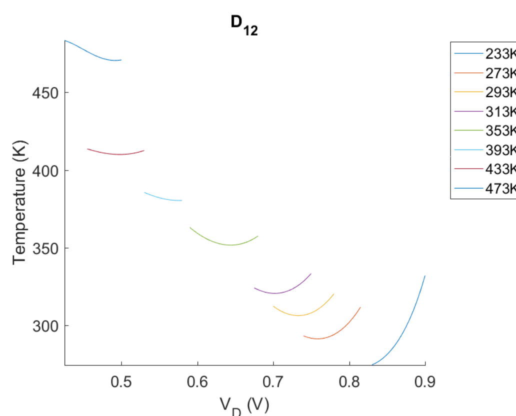

Figure 79. D_{12}, Temperature.

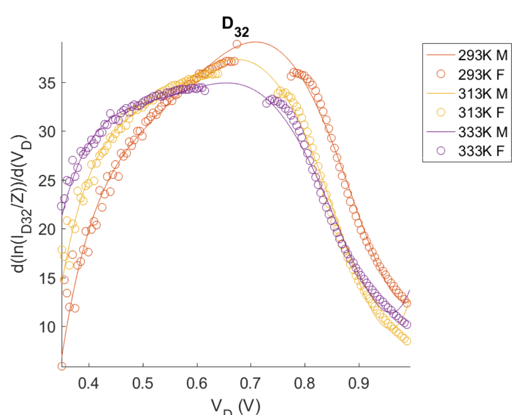

Figure 77. D_{32}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

Curves used to determine temperature

Figures 78 to 83 show the calculated temperature. These values are averaged and compared with the measured temperature.

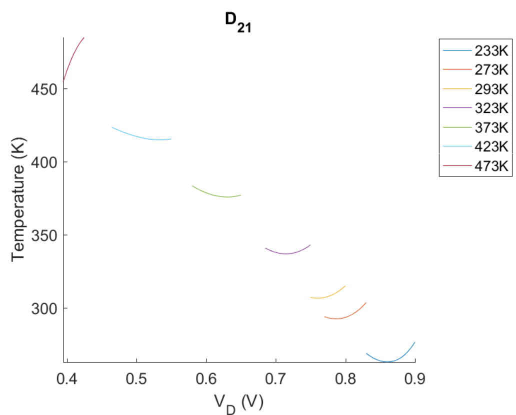

Figure 80. D_{21}, Temperature.

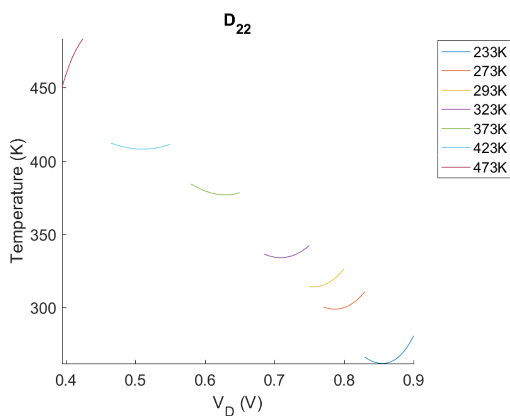

Figure 81. D_{22}, Temperature.

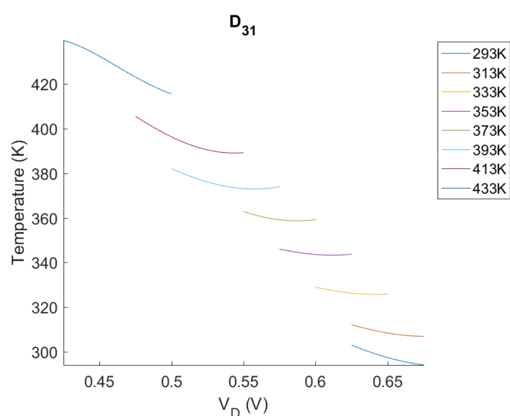

Figure 82. D_{31}, Temperature.

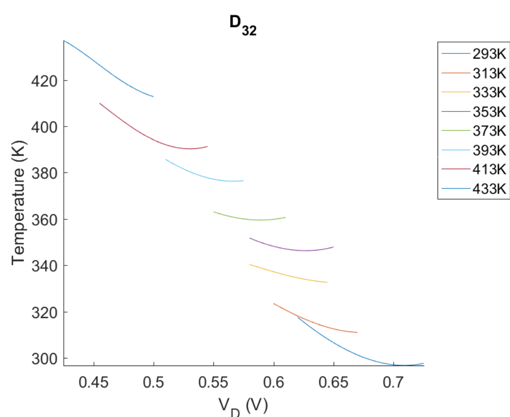

Figure 83. D_{32}, Temperature.

Table 20
Temperature results

Diode	Ideality factor	error (K)	Ideality factor	error (K)
D_{11}	1	30	1.10	9
D_{12}	1	14	1.10	14
D_{21}	1	21	1.10	10
D_{22}	1	25	1.10	5
D_{31}	1	6	0.99	4
D_{32}	1	2	1.00	2

Ideality factor

Figures 84 to 89 show the calculated Ideality factor. The measured temperature was used to calculate this.

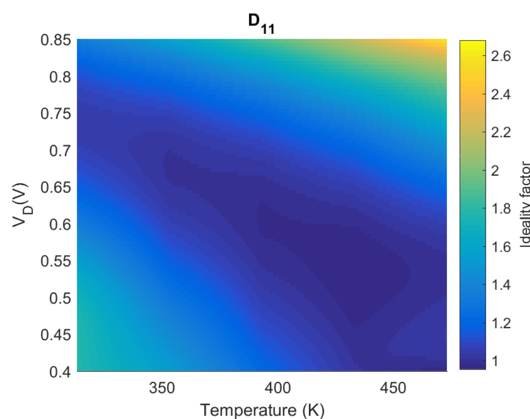

Figure 84. D_{11}, Ideality factor.

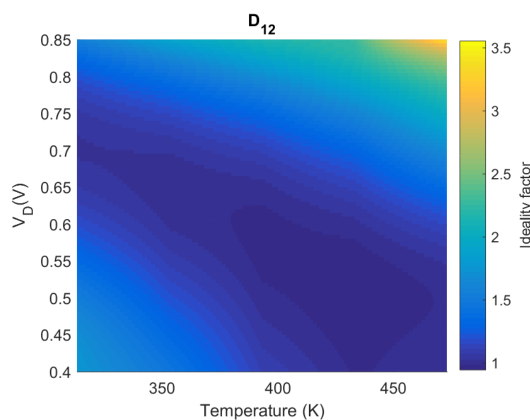

Figure 85. D_{12}, Ideality factor.

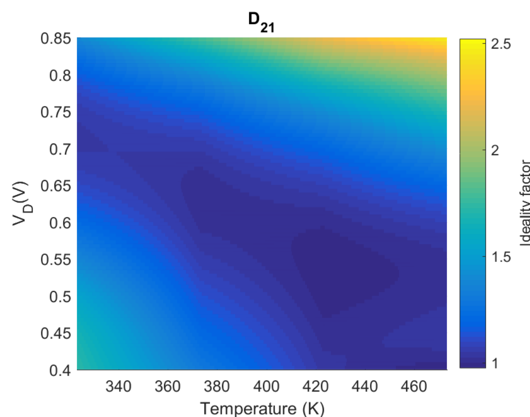

Figure 86. D_{21}, Ideality factor.

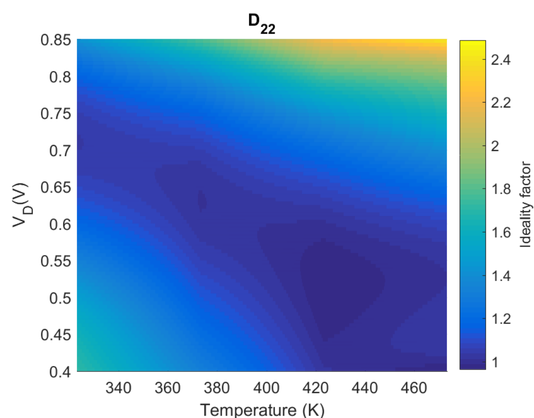

Figure 87. D_{22},Ideality factor.

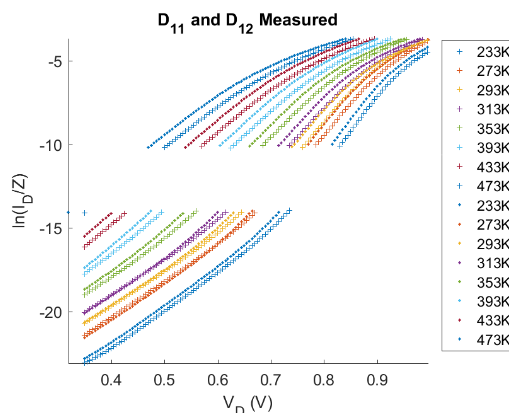

Figure 90. Comparison between the measured values for D_{11} and D_{12}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

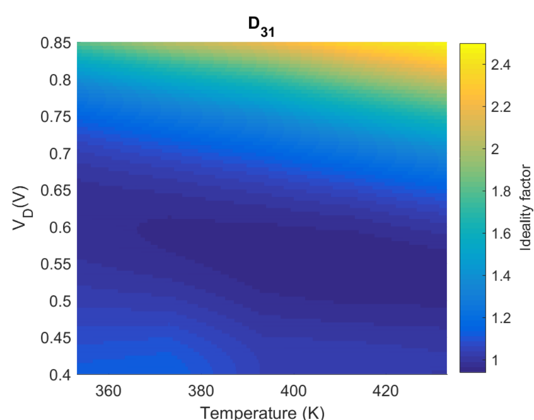

Figure 88. D_{31}, Ideality factor.

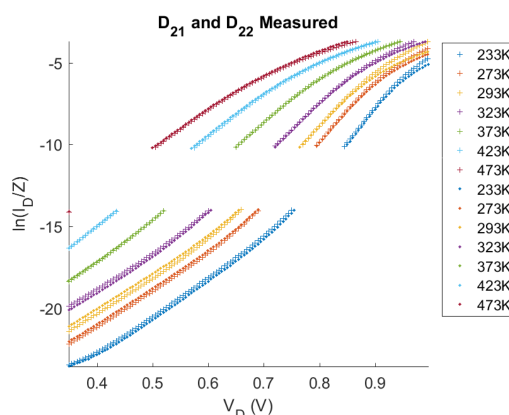

Figure 91. Comparison between the measured values for D_{21} and D_{22}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

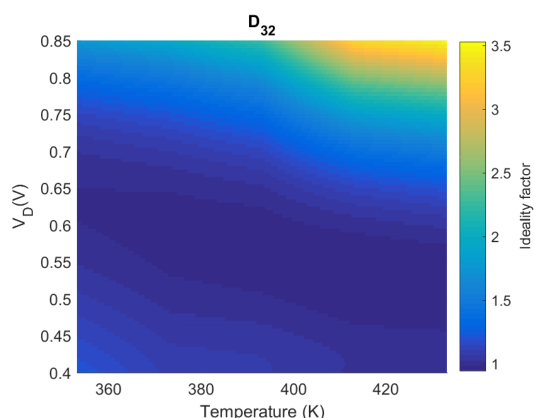

Figure 89. D_{32}, Ideality factor.

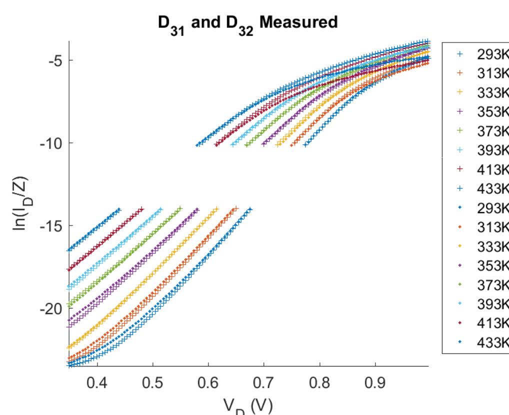

Figure 92. Comparison between the measured values for D_{31} and D_{32}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

Measured values comparison

Figures 90 to 92 show the plots used to compare the measured data of diode 1 and 2 of all diode types.

Fitted values comparison

Figures 93 to 95 show the plots used to compare the fitted data of diode 1 and 2 of all diode

types.

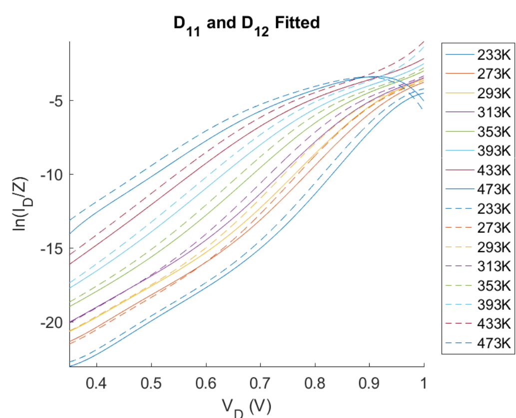

Figure 93. Comparison between the fitted values for D_{11} and D_{11}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

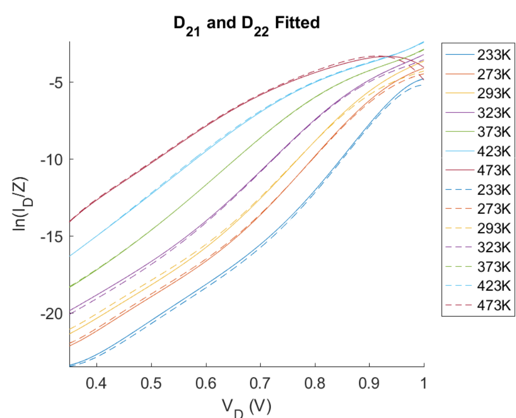

Figure 94. Comparison between the fitted values for D_{21} and D_{22}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

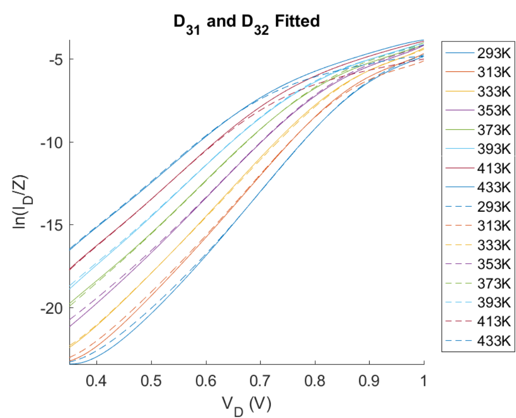

Figure 95. Comparison between the fitted values for D_{31} and D_{32}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

Difference in bandgap

Figures 96 to 98 show the difference in bandgap obtained using method 1. This is done for a range of temperatures and currents. It can be seen that the difference in bandgap is not constant.

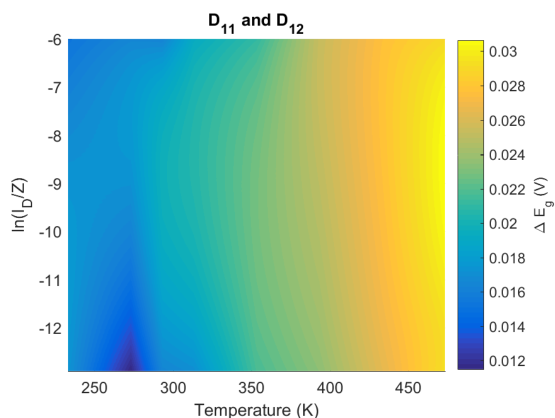

Figure 96. Difference in bandgap for diodes D_{11} and D_{12}

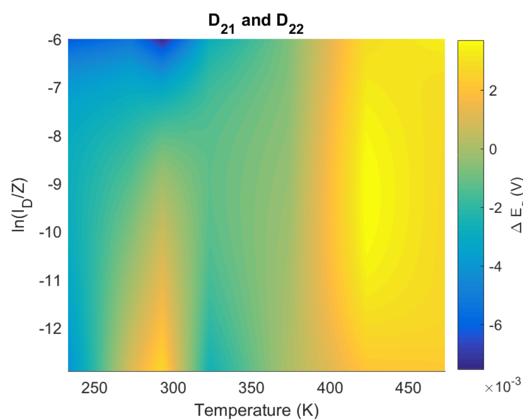

Figure 97. Difference in bandgap for diodes D_{21} and D_{22}

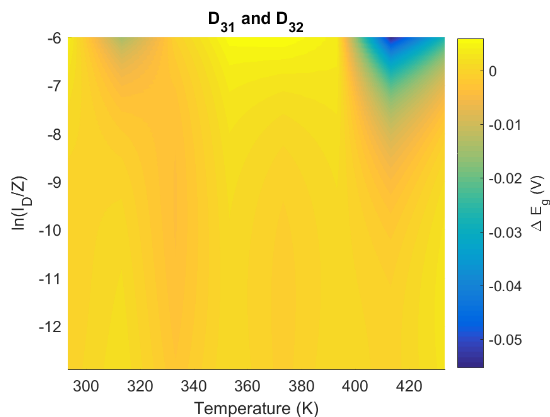

Figure 98. Difference in bandgap for diodes D_{31} and D_{32}

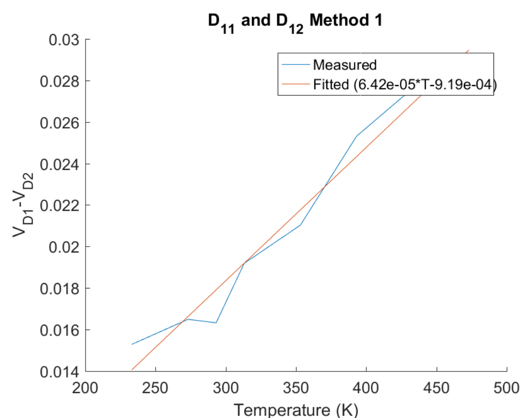

Figure 99. Difference in bandgap for diodes D_{11} and D_{12} for $I_D = 0.0025$

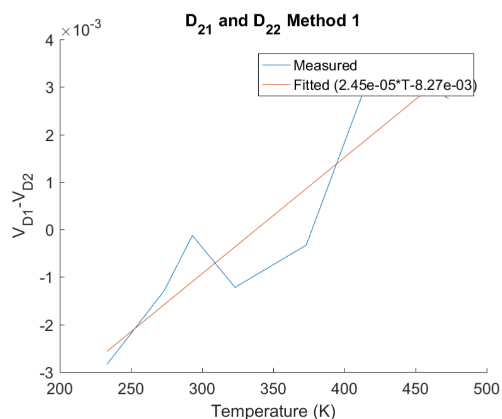

Figure 100. Difference in bandgap for diodes D_{21} and D_{22} for $I_D = 0.00012$

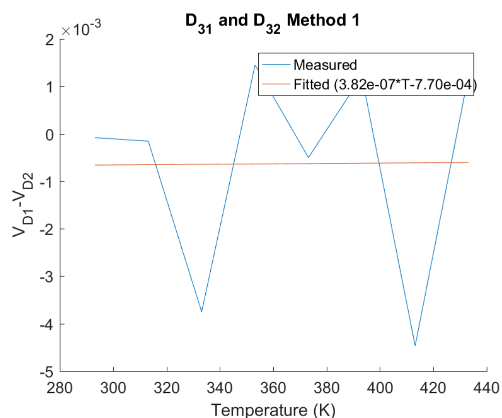

Figure 101. Difference in bandgap for diodes D_{31} and D_{32} for $I_D = 0.00012$

Figures 102 to 104 show the difference in bandgap obtained using method 2. This is only done for one constant voltage in the exponential region of the $I-V$ curve for each temperature. It can be seen that the slope is reasonably constant. The fitted slope is used to find the difference in bandgap.

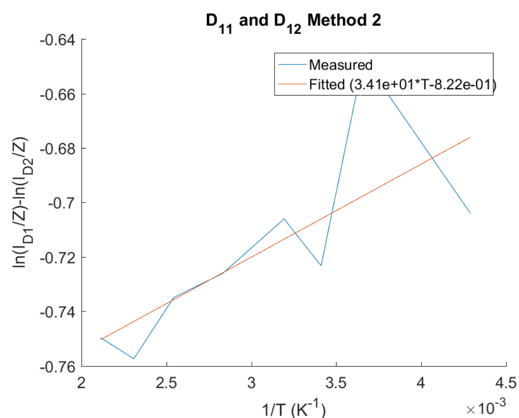

Figure 102. $\ln(D_{11}/Z) - \ln(D_{12}/Z)$ vs $1/T$.

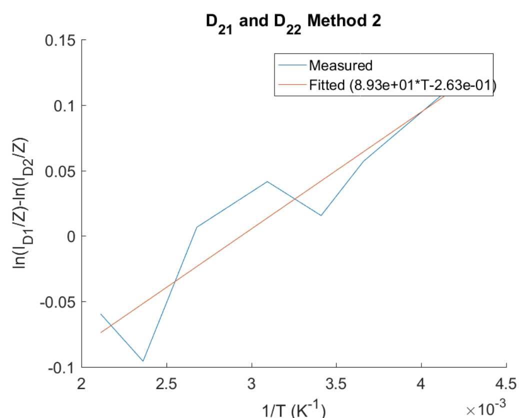

Figure 103. $\ln(D_{21}/Z) - \ln(D_{22}/Z)$ vs $1/T$.

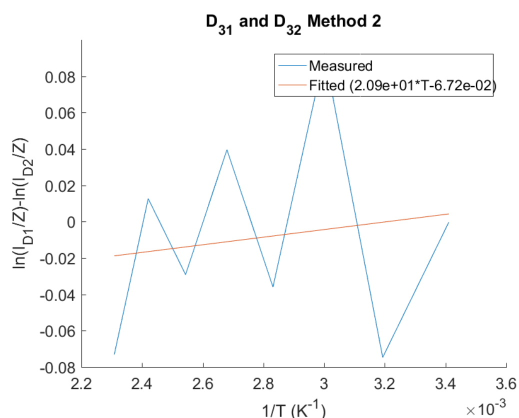

Figure 104. $\ln(D_{31}/Z) - \ln(D_{32}/Z)$ vs $1/T$.

Table 21
ΔE_g, results

Diode	Met 1 $I_D(mA)$	Met 1 ΔE_g (mV)	Met 2 ΔE_g (mV)	Avg ΔE_g (mV)	Error (mV)
D_{11} - D_{12}	2.49	-0.9	-2.9	-1.9	1.0
D_{21} - D_{22}	0.12	-8.3	-7.7	-8.0	0.3
D_{31} - D_{32}	0.12	-0.8	-1.8	-1.3	0.5

Strain

Figures 105 to 107 show the strain responsible for the difference in bandgap obtained using method 1. This is done for a range of temperatures and currents. It can be seen that the strain is not constant while it should be.

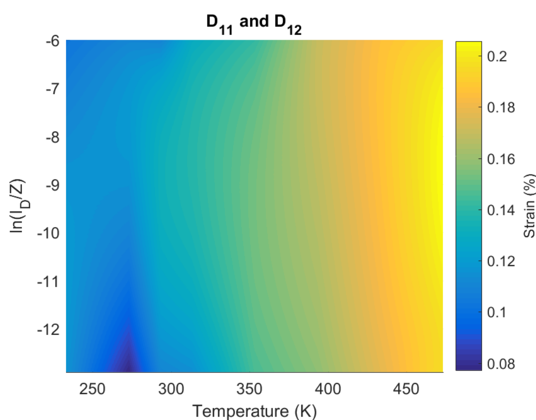

Figure 105. Strain for diodes D_{11} and D_{12}

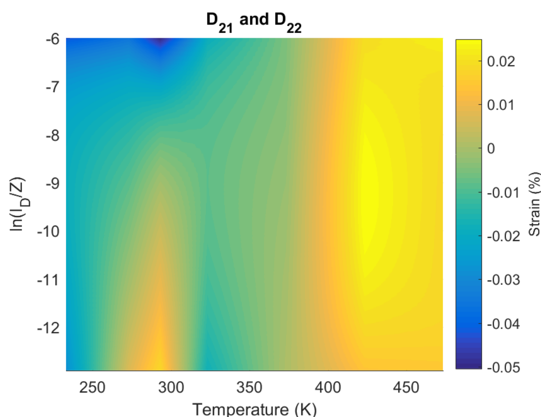

Figure 106. Strain for diodes D_{21} and D_{22}

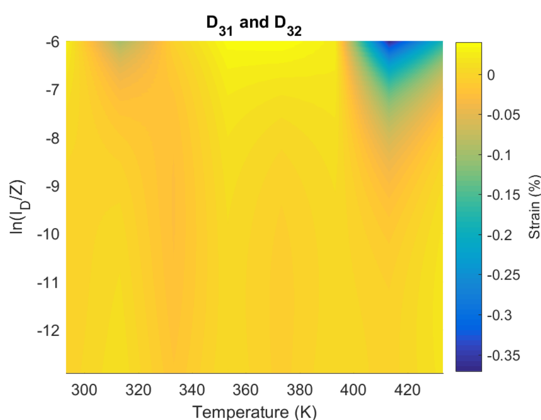

Figure 107. Strain for diodes D_{31} and D_{32}

Table 22 shows the strain obtained under the assumption that the strain is not temperature dependent.

Table 22
Strain results

Diode	Method 1 *Strain* (%)	Method 2 *Strain* (%)	Avg Strain (%)	Error (%)
D_{11} - D_{12}	-0.006	-0.019	-0.013	0.006
D_{21} - D_{22}	-0.056	-0.052	-0.054	0.002
D_{31} - D_{32}	-0.004	-0.009	-0.007	0.002

Low and high temperature ranges

Figures 108 and 109 show the $log(I_D/Z) - V$ curve of diode type 1. The temperatures between 5 K to 233.00 K are the low range temperatures that were measured using the cryostat. Temperatures 233.00 K and 203.00 K had a lower sample rate (0.05 V) compared to all other temperatures (0.005 V). D_{11} moves to the left for the temperatures in the range 5 K to 53 K. At the same tame it can be seen that the measurements done at (233.00 K) and (233.12 K) are not equal even through they should be. The same is true for diode D_{12}.

Full I-V plot

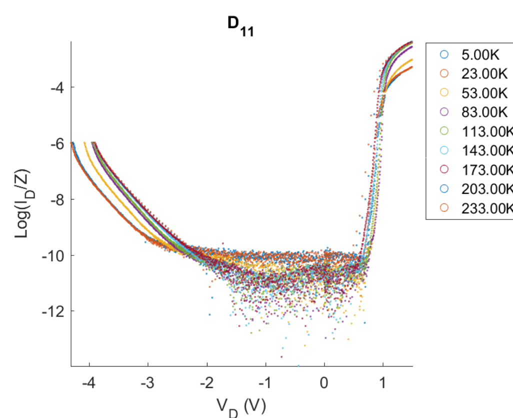

Figure 108. D_{11}, the complete $log(I_D/Z) - V_D$ curve.

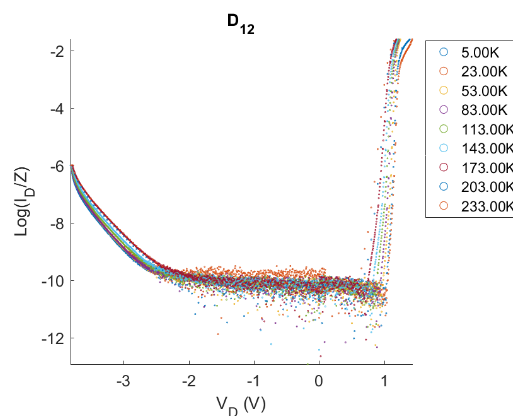

Figure 109. D_{12}, the complete $log(I_D/Z) - V_D$ curve.

Plot with fitted curves

Figures 110 and 111 show the fitted plots of the $ln(I_D/Z) - V$ curves and table 23 shows the error of the fitted curves for each diode.

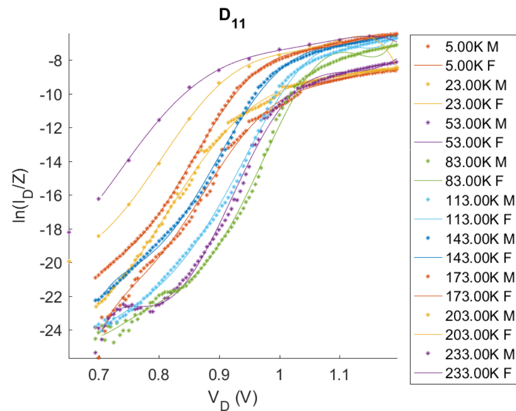

Figure 110. D_{11}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

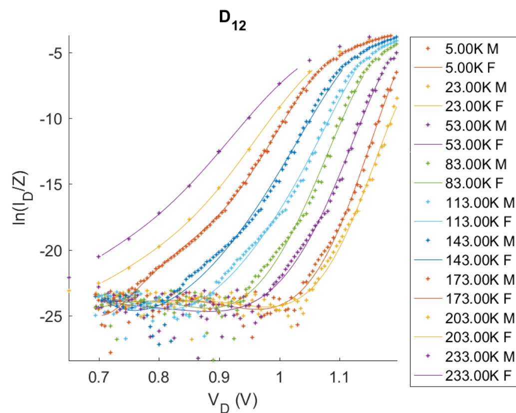

Figure 111. D_{12}, forward biased section of $ln(I_D/Z) - V_D$ curve, with fitted curve.

Table 23
RMS of Fitted data for diode type 3

Temperature (K)	RMS $D_{31} (10^{-5}A)$	$D_{32} (10^{-5}A)$
5	0.0057	0.0741
23	0.0092	0.1308
53	0.1041	0.1467
83	0.1140	0.3429
113	0.1126	1.1785
143	0.2645	1.3955
173	0.2033	1.9220
203	0.0543	0.6506
233	0.0124	0.2705
Average	0.3244	3.7427

Table 24
Error of fitted curves, low temperature.

Diode type	V=0.4V, error (A)	High voltage seen in fig 119 This is different for each curve, error (A)
1	0.0279n	1.2m

Differential plot of the current with respect to voltage for measured and fitted data points

Figures 112 and 113 show the differential for 3 different temperatures. This is done to improve readability.

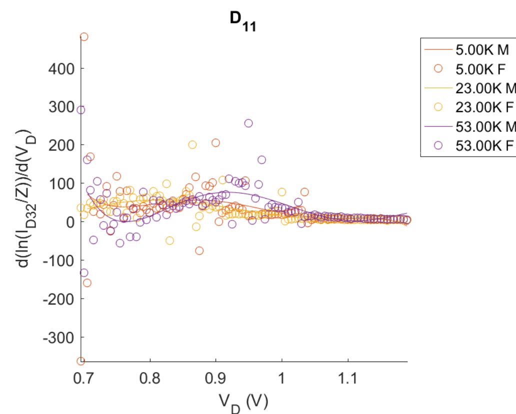

Figure 112. D_{11}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

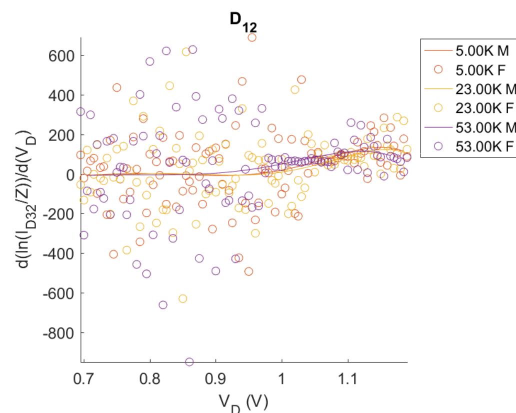

Figure 113. D_{12}, forward biased section of $(d(ln(I_D/Z))/d(V_D))$, with fitted curve.

Curves used to determine temperature

Figures 114 and 115 show the temperatures. Here it is noticeable that the calculated temperatures for the measured temperatures in the range of (5 K to 53 K) are moving to the left.

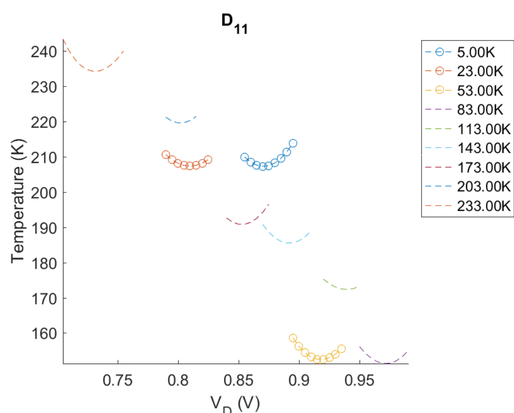

Figure 114. D_{11}, Temperature.

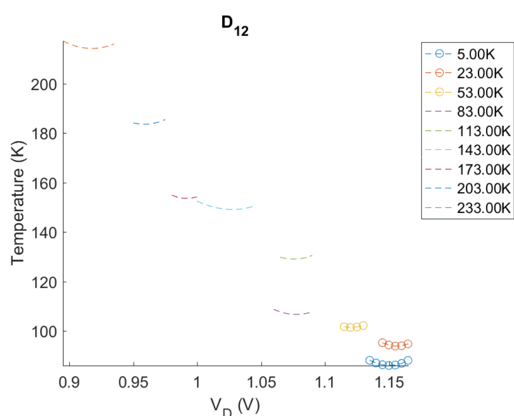

Figure 115. D_{12}, Temperature.

Ideality factor

Figures 116 and 117 show the ideality factor. The results for the $I-V$ curves in the range of (5 K to 53 K) are removed in order to plot the data in a colour plot.

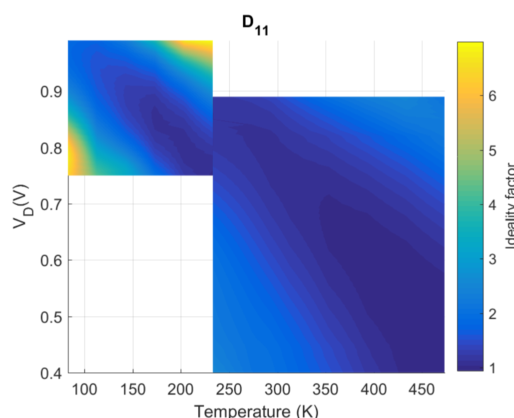

Figure 116. D_{11}, Ideality factor.

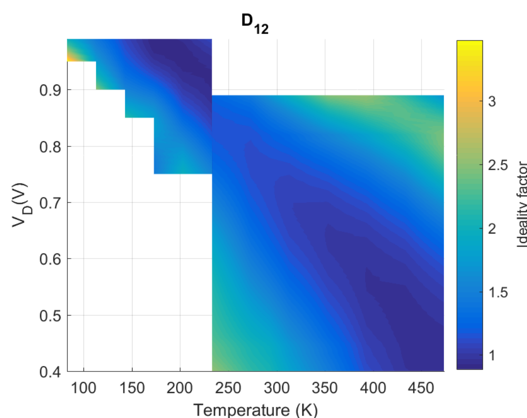

Figure 117. D_{12}, Ideality factor.

Measured values comparison

Figure 118 shows the comparison between the measured data of the two diodes.

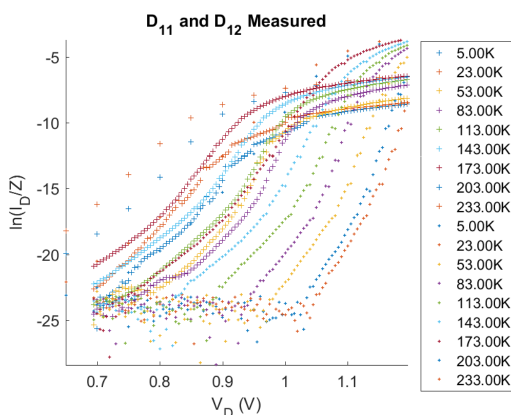

Figure 118. Comparison between the measured values for D_{11} and D_{12}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

Fitted values comparison

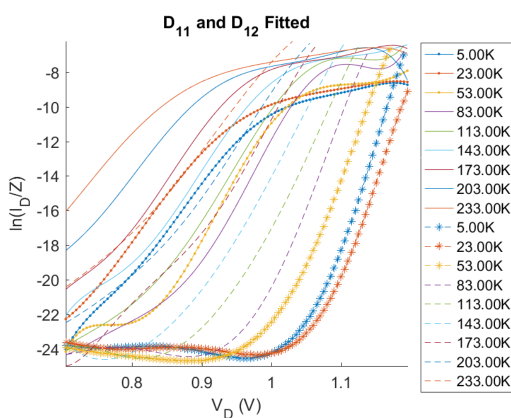

Figure 119. Comparison between the fitted values for D_{11} and D_{11}. The first set of curves in the legend are of diode 1 the second set of curves in the legend are of diode 2.

Difference in bandgap

Figure 120 shows the difference in bandgap and the sudden change between the high and low temperature ranges mention previously.

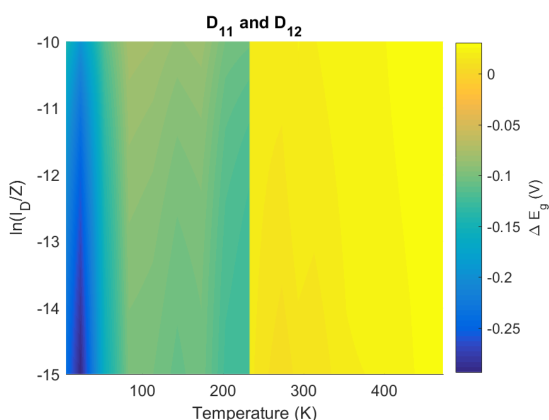

Figure 120. Difference in bandgap for diodes D_{11} and D_{12}

Effect of Bond wires

Figure 121 and 122 show the measurements of three diodes. One was bonded the other two were not. Instead those were measured by placing needles directly on the bond pads. It becomes quite clear that they are not the same.

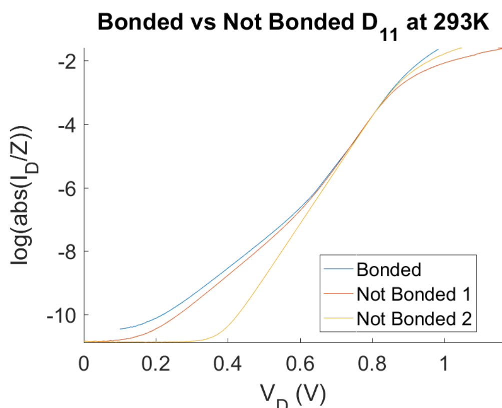

Figure 121. $log(I_D/Z) - V$ curve for a diode that was bonded and two that were not bonded.

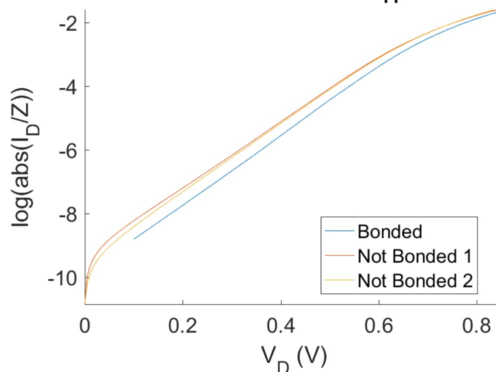

Figure 122. $log(I_D/Z) - V$ curve for a diode that was bonded and two that were not bonded.

Noise

Figure 123 shows the measured current when the needles are floating. Figure 124 shows the measured current over the PCB sample holder. This was measured in the high temperature range measurement setup.

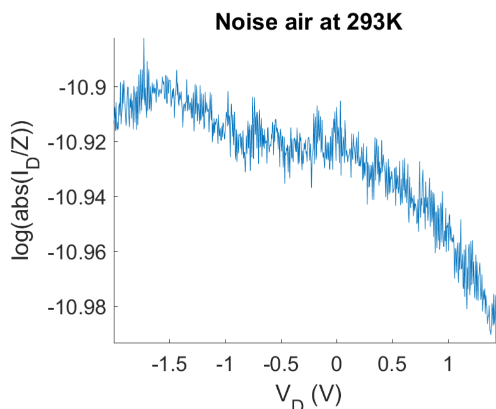

Figure 123. Air noise measured using the high temperature measurement setup

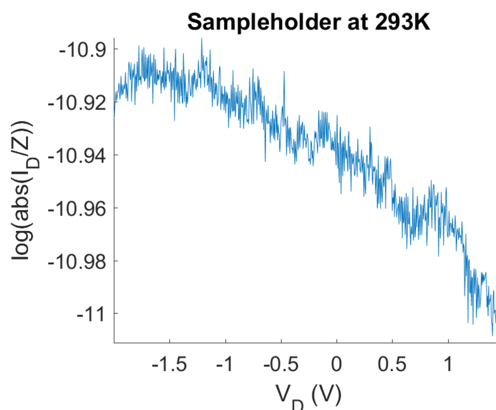

Figure 124. PCB noise measured using the high temperature measurement setup

Appendix H
Parameters

Table 25
List of symbols

Symbol	Description
a	Valence band deformation potential
A	Area
b	valence band shear deformation potential
c	elasticity
$\Delta E_{\mathrm{c,k}}$	Conduction band energy offset
ΔE_{g}	Bandgap energy difference
$\Delta E_{\mathrm{v,k}}$	Valence band energy offset
Δd	change in width of the STI of diode type 2 due to thermal expansion
ΔL	Change in width of diode type 2 due to thermal expansion
D_n	Electron diffusion constant
D_p	Hole diffusion constant
EG	Bandgap
$egnom$	Nominal bandgap
$eg(t)$	Temperature dependent bandgap
$GAP1$	Bandgap constant 1
$GAP2$	Bandgap constant 2
I_{D}	Diode current
I_{D1}	Diode 1 current
I_{D2}	Diode 2 current
I_{rec}	Recombination current
I_{S}	Saturation current
V_{D}	Voltage over diode
V_{D1}	Voltage over diode 1
V_{D2}	Voltage over diode 2
V_{R2}	Voltage over resistor R_2
N	Non-ideality factor
N_{A}	Number of acceptors in units cm^{-3}
N_{c}	Conduction band effective density of states
N_{D}	Number of donors in units cm^{-3}
n_i	Intrinsic carrier density
N_{v}	Valence band effective density of states
L_n	Diffusion length of electrons
L_p	Diffusion length of holes
Q	Current ratio between two diodes
T	Temperature
T_{nom}	Nominal temperature
X	Number of parallel diodes
XTI	Saturation current temperature exponent
Z	Constant used to remove the unit ampere. $Z = 1\,\mathrm{A}$

Table 26
List of the Greek symbols.

Symbol	Description
ε	strain
$\varepsilon_{\mathrm{xx}}$	strain in the x direction
$\varepsilon_{\mathrm{yy}}$	strain in the y direction
$\varepsilon_{\mathrm{zz}}$	strain in the z direction
Ξ_{d}	dilatational deformation potential
Ξ_{u}	uniaxial deformation potential
μ_T	Thermal voltage kT/q

Table 27
List of all the used constants.

Name	Sym	Value
Boltzmann's constant	k	$8.61738 \cdot 10^{-5}$ (eV/K)
elementary charge	q	$1.60218 \cdot 10^{-19}$ (C)
electron Volt	eV	1 (eV)
Planck's constant	h	$6.62617 \cdot 10^{-34}$ (Js)

Table 28
List of the diode parameters. s.i.s. means set in simulation. This parameter is changed depending on the simulation.

Symbol	Description	Value
Cjo	Zero-bias junction capacitance	0.64p (F)
EG	Bandgap	s.i.s. (V)
I_{ave}	The maximum average input current rating	200m (A)
IS	Saturation current	s.i.s. (A)
M	Multiplier factor simulates multiple diodes	0.4
mfg	Manufacturer	Onsemi
N	Non idealty factor	s.i.s.
tt	Transit-time	5n (sec)
$type$	Type of material	Silicon
Rs	Series residence of diode	0.168Ω
Vpk	Peak voltage rating	100 (V)
XTI	Saturation current temperature exponent	3

Acknowledgment

The author would like to thank Dr.Ir. Anne-Johan Annema and Dr.Ir. Ray Hueting for being his daily supervisors and for the feedback they gave on the report. Ing. Henk de Vries for helping with the measurements and the bonding. Ing. Johnny Sanderink for helping with the low temperature measurements. Henk Waayer for helping with the sample holder. Demitri Gestus from Lionix for helping with the bonding of the diodes.

References

[1] R. R. Sanikommu, *Design and Implementation of Bandgap Reference Circuits*. publisher: Linkoping University, Address: 581 83 Linköping, Sweden, Master thesis, (2005). pp, 1, url=https://www.diva-portal.org/smash/get/diva2:20493/FULLTEXT01.pdf, checked:30-05-18.

[2] T. Hemert and R. J. E. Hueting, *Piezoelectric Strain Modulation in FETs*. IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 10, pp, 1-4, (2013), url=https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=6581880, checked: 30-05-18.

[3] B.P.Modi and J.M. Dhimmar *THE TEMPERATURE DEPENDENT IDEALITY FACTOR EFFECT ON I-V CHARACTERISTICS OF SCHOTTKY DIODE*. 2012 1st International Conference on Emerging Technology Trends in Electronics, Communication and Networking, pp, 1-5, url=http://ieeexplore.ieee.org/iel1/16/3465/00121690.pdf, checked: 04-06-18.

[4] M. Pertijs, *Precision Temperature Sensors in CMOS Technology*. publisher: Delft University of Technology, Address: 2, Mekelweg, 2628 CD Delft, Netherlands, Dissertation, (2005). pp, 16.

[5] *Temperature dependence of the saturation current of a junction diode*. publisher: California polytechnic state university, Address: San Luis Obispo, CA 93407, USA, url=http://www.reed.edu/physics/courses/Physics332.s18/pdf/Saturation_Current.pdf, checked: 30-05-18.

[6] V. Gromov, *Development of the bandgap voltage reference circuit, featuring dynamic-threshold mos transistors (DTMOSTs) in 0.13um CMOS technology*. Publisher: NIKHEF, Address, Science Park 105, 1098 XG Amsterdam, the Netherlands, Presentation

slides, (2014), slides, 5-7, url=http://slideplayer.com/slide/259535/, checked: 30-05-18.

[7] *ASM Ready Reference: Thermal Properties of Metals*. Publisher: ASM International, (2002), Chapter 2, url=http://www.owlnet.rice.edu/~msci301/ThermalExpansion.pdf, checked: 21-06-18.

[8] *Silica Silicon Dioxide (SiO2)*. Publisher: AZoM, Company specifications of SiO2 (2001), url=https://www.azom.com/properties.aspx?ArticleID=1114, checked: 20-06-18.

[9] *Silicon Nitride (Si3N4) Properties and Applications*. Publisher: AZoM, Company specifications of Si3N4 (2001), url=https://www.azom.com/article.aspx?ArticleID=53, checked: 20-06-18.

[10] G. Carlotti, P. Colpani, et all*Elastic Properties of Silicate Glass and Silicon Nitride Films for Submicron Eelectronic Devices*. Publisher: Sessions, Proceedings of the 17th International Congress on Acoustics, (2001), url=https://www.icacommission.org/Proceedings/ICA2001Rome/1_05.pdf, checked: 20-06-18.

[11] *Intelegent temperature controller, ITC503*. Publisher: Oxford instuments, Manual, pp 14, url=http://amnol.usv.ro/DOC/itc503.pdf, checked: 15-06-18.

[12] R. J.E. Hueting, A. J. Mouthaan and G. T. Sasse, *Semiconductor Devices Explained More*. publisher: University of Twente, Address: 5, Drienerlolaan, 7522 NB Enschede, Netherlands, chapter 2, Lecture notes, (2013).

[13] *Star-Hspice Manual*. publisher: Corporation and Avant!, Manual, (1998), Chapter 13, url=https://web.engr.oregonstate.edu/~moon/ece323/hspice98/, checked:30-05-18.

[14] T. van Hemert, *Tailoring Strain in Microelectronic Devices*. publisher: University of Twente, Address: 5, Drienerlolaan, 7522 NB Enschede, Netherlands, Dissertation, chapter 4, (2013), Url= http://epdoc.utsp.utwente.nl/88032/1/thesis_T_van_Hemert.pdf, checked:30-05-18.

[15] *MMSD4148*. Publisher: Fairchild Semiconductor, Datasheet url=http://pdf1.alldatasheet.com/datasheet-pdf/view/53822/FAIRCHILD/MMSD4148.html, checked: 30-05-18.

[16] *op747*. Publisher: Analog Devices, Datasheet url=http://www.analog.com/media/en/technical-documentation/data-sheets/OP777_727_747.pdf, checked: 30-05-18.

[17] J. Cai, Y. Ishikawa and K Wada, *Strain induced bandgap and refractive index variation of silicon*. The University of Tokyo, Address: 7-3-1 Hongo, Bunkyo-Ku,Tokyo,113-8656, Japan, Optical Society of America, article, pp, 4-5, (2013), url=https://www.osapublishing.org/viewmedia.cfm?uri=oe-21-6-7162&seq=0, checked: 30-05-18.

[18] T. Skotnicki, C . Fenouillet-Beranger, et all, *Innovative Materials, devices, and CMOS Technologies for LPMM*. IEEE transactions on electron devices, vol.55, no.1, pp, 12, (2008), url=https://ieeexplore.ieee.org/iel5/16/4408767/04408810.pdf, checked: 30-05-18.

[19] M. V. Fischettia and S. E. Laux, *Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys*. publisher: American Institute of Physics, Journal of Applied Physics 80, pp, 5, 14, (1996), url=http://aip.scitation.org/doi/pdf/10.1063/1.363052, checked:30-05-18.

[20] *Semiconductors*. publisher: University of Colifornia, Address: Irvine, CA 92697, pp, 1-3, (2011), url=http://faculty.sites.uci.edu/chem2l/files/2011/04/RDGsemiconductor.pdf, checked:30-05-18.

[21] H. Amin, *Measuring Silicon and Germanium Band Gaps using Diode Thermometers*. publisher: Wabsh College, Address: Crawfordsville, IN 47933, Paper, pp, 1-2, (2007), url=http://www.iontrap.wabash.edu/adlab/papers/S2007_amin_semiconductor_band_gaps.pdf, checked: 30-05-18.

[22] D. R. Franca, *All-optical measurement of in-plane and out-of-plane Young's modulus and Poisson's ratio in silicon wafers by means of vibration modes*. MEASUREMENT SCIENCE AND TECHNOLOGY, vol 15, pp, 867, (2004) url=http://iopscience.iop.org/article/10.1088/0957-0233/15/5/011/pdf, checked: 30-05-18.

[23] *Semiconductor characterization system, 4200-SCS*. Publisher: Keithley Instruments, Manual, pp 21, url=http://www.cedesa.com.mx/pdf/keithley/keithley_4200-SCS_user_manual.pdf, checked: 08-06-18.

[24] *Enhanced Temperature Device Support*. Publisher: Intel, url=https://www.altera.com/products/common/temperature/ind-temp.html, checked: 27-06-18.