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The Belostotski LNA: Combining noise-cancelling and noise matching

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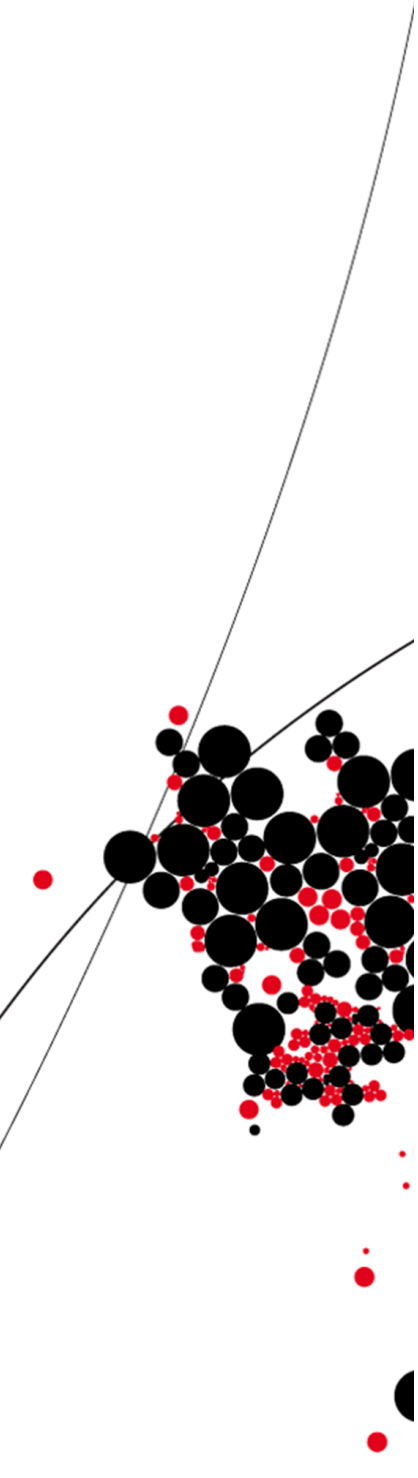

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Abstract

In this report an analysis is performed on the gain and noise behavior of the active negative C LNA proposed by L. Belostotski. This LNA utilizes an active matching element to achieve negative capacitance (negative susceptance proportional to frequency), thereby achieving a noise figure closer to NF_{min} (noise match). The goal of the research was to get a better understanding of the technique used in this LNA and to investigate whether it could also be used in other LNA topologies.

Analysis shows that there are two sources of negative capacitance; 1) feedback of the output to the input through a common-gate transistor and 2) an active inductor formed by the same common-gate transistor which has negative capacitor behavior at frequencies up to a few GHz. Simulation of the negative C LNA in 22nm FDSOI using 1.5u/40n SLVT (super low Vt) transistors shows that the negative capacitance positively affects the noise figure but this improvement is shown to be mainly due to improved bandwidth.

Comparison between the LNA proposed by Belostotski, a BALUN LNA and an active shunt-feedback LNA shows that the Belostotski LNA has better NF when compared to a BALUN LNA with equal power consumption. The regular active shunt-feedback LNA was shown to be on par with regard to noise figure but better linearity is shown in simulation for both the BALUN and shunt-feedback LNA. The conclusion of this research is that the Belostotski LNA (i.e. active negative C LNA) performs quite well compared to other noise-cancelling topologies, but a trade-off exists between linearity and NF. The presence of positive feedback via the cross-coupled transistors helps lower NF, but introduces the risk of high-frequency instability. This cross-coupling is not present in a regular active shunt-feedback LNA.

The final design is aimed at application in the ISM-band at 5.8 GHz. Two desgin where made, one optimized for NF and a second one optimized for linearity: The fist design achieves 1.1 dB NF, 16 dB voltage gain and -16.5 dBm IIP3. The second design was made with more emphasis on linearity, achieving a NF of 2.2 dB, 10 dB voltage gain and -4 dBm of IIP3.

Contents

Chapter 1

Introduction

This research was triggered by a publication by L. Belostotski in which the differences and similarities of noise-cancelling and noise matching in LNAs (low noise amplifiers) were presented [1]. In the same publication an LNA was presented from a prior publication of Belostotski et al., this LNA was designed for improvement on noise-cancelling by also applying noise matching through an active matching element designed to behave like a negative capacitor [2]. A negative capacitor would also allow for lowering input capacitance of the LNA. The research questions for this research are:

- How does Belostotski's LNA generate negative capacitance?
- Does the negative capacitance improve the noise figure of the LNA, and if so to what extend?
- Could the negative capacitor technique be applied in other noise-cancelling LNAs?
- What are the limitations of this technique?

1.1 Low noise amplifiers (LNAs)

Often, receiver systems incorporate a low-noise amplifier (LNA) to amplify the weak signals at the input. This has to be done with as little added noise as possible since all subsequent system blocks will amplify this added noise. In applications where the LNA may be subject to strong blockers, good linearity is needed; gain, IIP3 and noise figure (NF) are generally the specifications to design for in an LNA.

The main figure of merit for noise behavior is noise factor (F) or noise figure (NF):

$$F = \frac{N_{out}}{N_{in} \cdot G}, \qquad NF = 10 \cdot \log_{10}[F], \tag{1.1}$$

where N_{out} and N_{in} are the available noise power at the output and input, respectively and G is the available power gain. The noise factor relates the total noise at the output to the noise due to the input source. The noise figure can also be represented as the ratio between input and output signal-to-noise ratio (SNR):

$$NF = 10 \cdot \log_{10}\left[\frac{SNR_{in}}{SNR_{out}}\right] \tag{1.2}$$

The latter definition is the definition given by Friis [3]. The concept of noise figure and factor can also be extended to systems consisting of multiple block, each having a certain noise figure/factor and gain. The total noise figure of a system is given by the Friis equation [4]:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_N - 1}{\prod_{n=1}^{N-1} G_n} \tag{1.3}$$

and the total gain given by

$$G = \prod_{n=1}^{N} G_n. \tag{1.4}$$

from (1.3) we see that the noise factor of all subsequent blocks get divided by the gain of the first block, while the noise of the first block directly adds to the noise factor. For a low cascade noise factor, the first block (LNA) should have low noise factor and high gain.

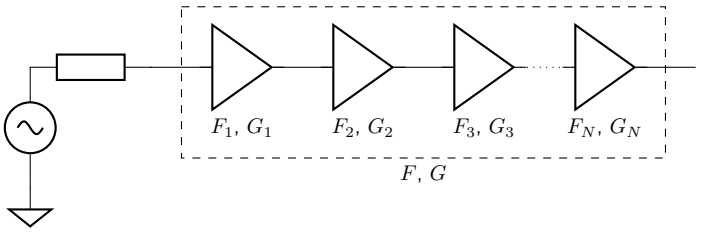


Figure 1.1: A cascade of noisy system blocks.

The NF of an LNA, and two-ports in general, is a function of the connected source impedance. To understand the subject of noise matching and noise-cancelling, two types of matching should be described; noise- and power matching.

1.2 Power matching

Figure 1.2 shows a simple system, a signal source connected to a load impedance. The power transfer from the source (V_S and Z_S) to the load (Z_L) is given by

$$P_{load}\left(Z_S, Z_L\right) = \frac{V_S^2}{Z_S + Z_L} \cdot \frac{Z_L}{Z_S + Z_L}. \tag{1.5}$$

The derivative with regard to load impedance of this function is

$$\frac{\partial}{\partial Z_L}\left[\frac{V_S^2}{Z_S + Z_L} \cdot \frac{Z_L}{Z_S + Z_L}\right] = \frac{V_S^2 \cdot (Z_S - Z_L)}{\left(Z_S + Z_L\right)^3}. \tag{1.6}$$

The maximum delivered power is achieved when equation (1.6) equals zero, i.e.

$$Z_S = Z_L^*, \tag{1.7}$$

where '*' indicates complex conjugation. We call this situation *power matched*.

The reflection coefficient relates the incident and reflected power waves, given in [5] by

$$\Gamma = \frac{Z_L - Z_S^*}{Z_L + Z_S}. \tag{1.8}$$

This result is different from the more well-known version of reflection coefficient, where the source impedance in not conjugated, in case of low loss cables the definition without conjugation can be used. To minimize the reflections, the relation $Z_S = Z_L^*$ should be adhered, hence power match achieves both maximum power transfer and minimum reflections.

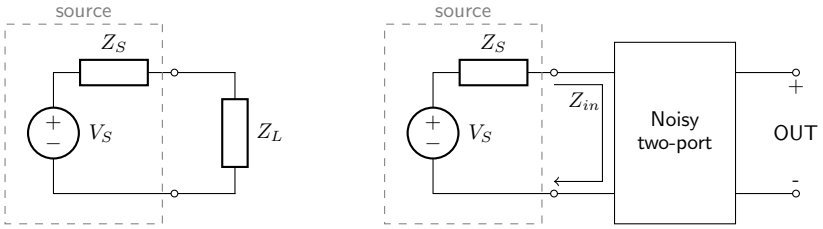


Figure 1.2: A source driving a load impedance (left) and a noisy two-port connected to a signal source (right).

Good power matching is important in situations where reflections are unwanted (e.g. unwanted retransmission of received signals) or where the load impedance affects characteristics of a prior block (e.g. transfer characteristics of a filter).

1.3 Noise matching

In the previous section power match was introduced. The second type of matching used in LNAs is noise matching; where power match is aimed at achieving maximum power transfer and minimizing

power wave reflections, noise matching is aimed at achieving the best possible noise figure (NF_{min}) for a given LNA. Noise matching is explained in [4, 6] for noisy two-ports, figure 1.3 shows different (equivalent) ways of representing the noise of a two-port [6].

An intuitive way of explaining noise matching is: If the noise sources in either of the representations in figure 1.3 are correlated, then appropriate scaling and addition these noise sources at the output can cancel part of that correlated noise [6]. In noise matching this is done by presenting a well-chosen source impedance ($Z_S = Z_{opt}$) to the two-port (see figure 1.2), allowing for partial or full cancellation[1] of the correlated noise components via non-zero Γ (hence $Z_{in} \neq Z_S$, where $Z_{in} = Z_L$ in equation (1.8)). This is given in mathematical form by (see appendix A for derivation)

$$F = F_{min} + \frac{R_n}{\Re(Y_S)} \left| Y_S - Y_{opt} \right|^2, \tag{1.9}$$

where R_n is an equivalent voltage noise resistor ($\overline{v_n^2} = 4kTBR_n$), Y_S and Y_{opt} are the actual and optimum source admittance, and F_{min} is the noise factor for $Y_S = Y_{opt}$, i.e. "noise matched".

Noise matching enables achieving the lowest noise factor ($F = F_{min}$) for a given amplifier, but the optimum source impedance Z_{opt} may not be equal to the complex conjugate of the input impedance of the amplifier[2] leading to reflections. Noise matching introduces two challenges:

1. Choosing a source impedance is not trivial, this impedance is often a given (50Ω), so an impedance-transformation circuit is needed to transform the source impedance to Z_{opt}.

2. RF-filter characteristics are generally dependent on the input impedance of the subsequent block. For instance, if an amplifier is designed such that noise match is achieved when connected to the output of a filter, this amplifier is not necessarily power matched, hence affecting the characteristics of said filter.

1.4 Noise-cancelling LNAs

In the previous sections, power and noise matching have been explained. A clear trade-off between these techniques is shown in figure 1.5, where the NF, S_{11} and the optimum source impedance as function of frequency of the amplifiers of figure 1.4 are compared. The lowest noise figure is achieved by the common-source LNA, while the best power match is achieved by the common-gate LNA.

Noise-canceling LNAs are designed to achieve a good balance between NF and power match. This is done by creating two signal paths; a main (matching) path that achieves wideband power match, this path generally produces a lot of noisy due to the matching constraints and an secondary auxiliary path that senses the noise of the matching path and cancels this noise. Noise-canceling was discovered by E.A.M. Klumperink in 1997 [7]

The first LNAs that utilized noise-canceling were published in 2004 by Bruccoleri et al. [8], this topology already existed but its noise cancelling properties had not been utilized before. The CG-CS LNA is shown in figure 1.4.c, the matching path is formed by the CG amplifier (M1 + R1). The drain noise of the matching stage is in phase at the source of M1, while out of phase at the drain (output $V_{out,+}$). The auxiliary path is formed by the CS stage (M2 + R2), the noise at the source of M1 is amplified and inverted, becoming in phase with the noise voltage at $v_{out,+}$. Taking the output differentially converts the output noise signal to a common mode signal. The signal transmitted by the signal source is transmitted in phase to the positive output, while being transmitted to the negative output out-of-phase, so the noise adds destructively, while the signal adds constructively. It is important to note that only the drain noise of M1 is cancelled, the gate noise of M1, the noise due to the resistors and the noise of the bias circuitry are not cancelled.

Looking at figure 1.5 again, we see that the noise cancelling LNA gives better NF than the CG amplifier and at the same time has superior power match when compared to the CS amplifier (see figure 1.5). This research will focus on wideband LNAs.

[1] Scaling and addition is realized via reflection.

[2] If the F_{min} is achieved through reflections, then by definition $Z_{in} \neq Z_S$.

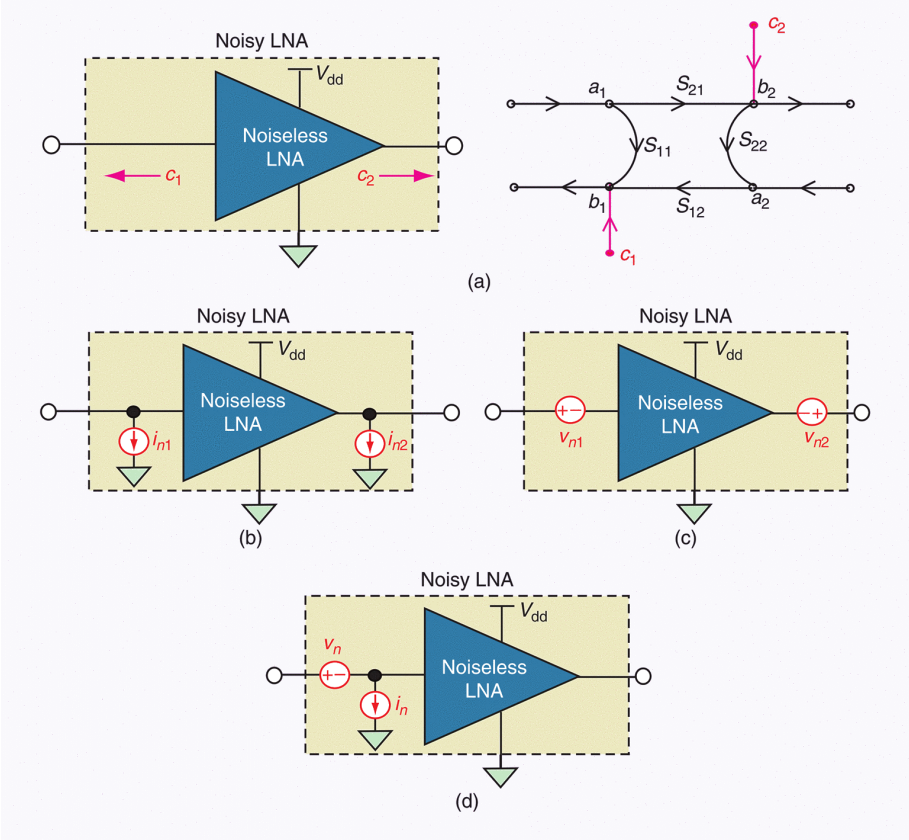


Figure 1.3: Different canonical noise representations, (a) represented as noise waves, (b) as input and output noise current or (c) noise voltage sources, or (d) as an input noise voltage and noise current source. [6]

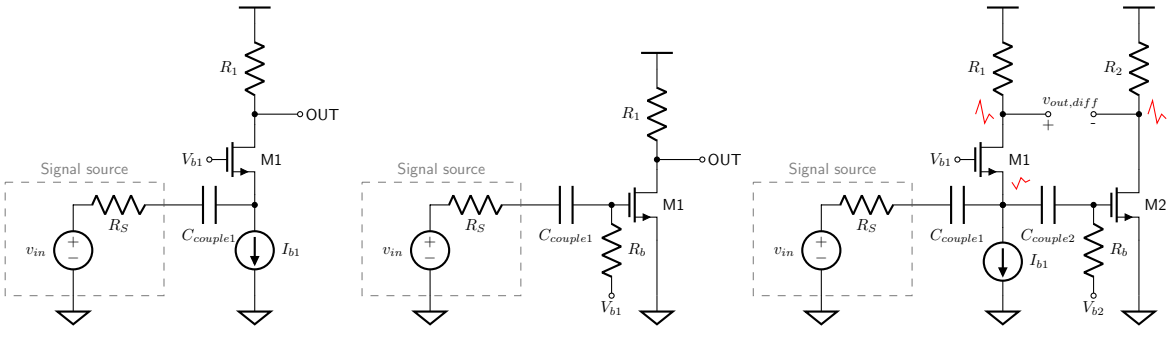


Figure 1.4: Three examples of amplifiers, (a) a common-gate (CG) amplifier, (b) a common-source (CS) amplifier, (c) a combined CS-CG amplifier.

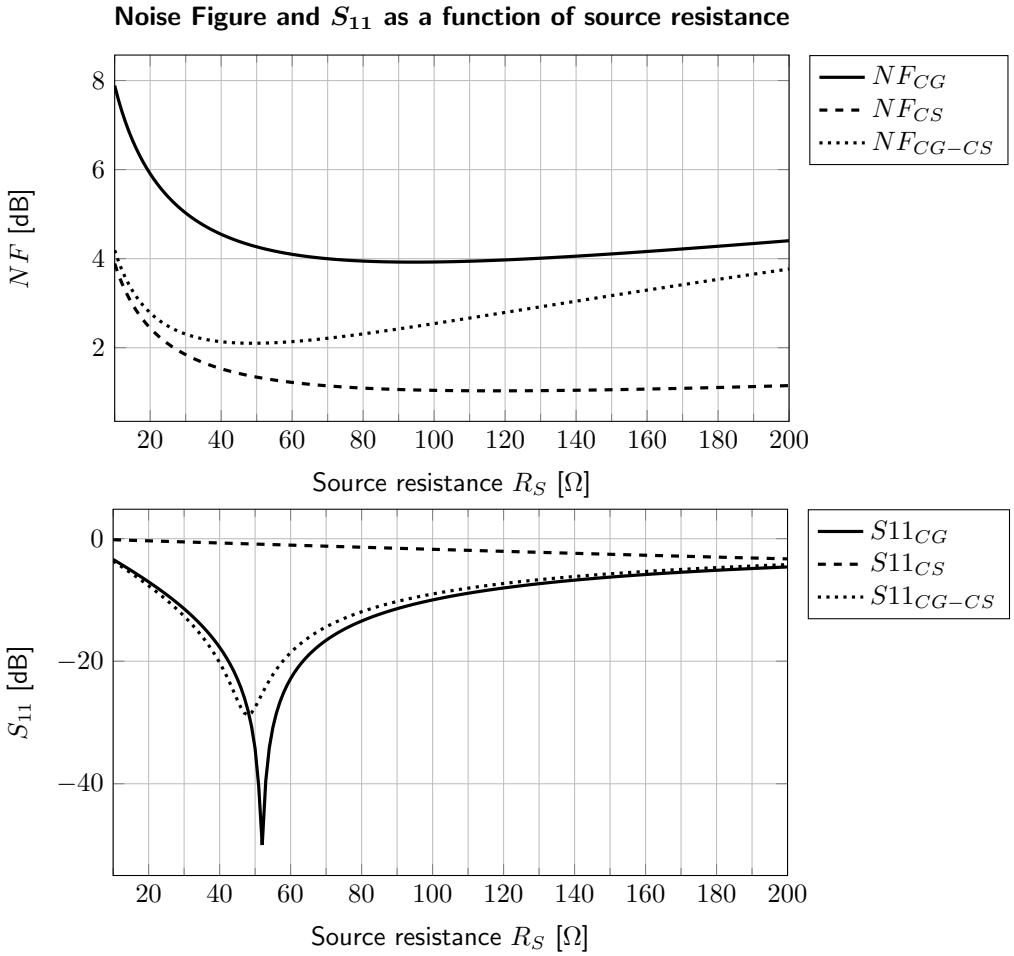


Figure 1.5: Common-source, common-gate and combined (CG-CS) LNAs, designed for 4x voltage gain. The $NF(R_S)$ and $NF_{min}(R_S)$ (top) and the $S_{11}(R_S)$ (bottom) of the three different amplifiers.

1.5 The Belostotski LNA

The LNA proposed by Belostotski is shown in Figure 1.6, the LNA was implemented in 65nm TSMC technology. The main claimed novelty of the LNA is generating -C susceptance at the source of M3, hence realizing noise matching of the CS-transistor M1. The LNA consists of a core LNA (left of the dashed line in Figure 1.6); a common-gate stage and a cascode stage with cross-coupling, and a balun stage (right of the dashed line) to generate a balanced differential output signal.

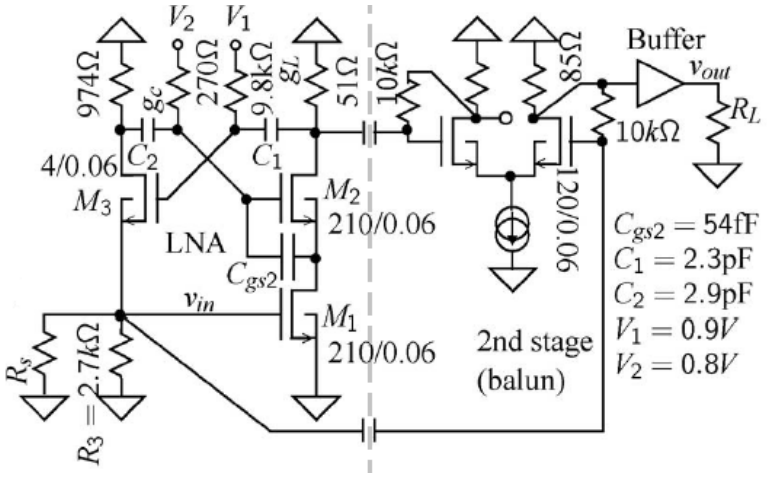


Figure 1.6: The negative C LNA as presented by Belostotski in [2]. The biasing network and the coupling capacitor at the input are not shown.

Negative C

M3 forms a g_m-boosted common-gate stage, where the transconductance is boosted via the gain of the core LNA. The capacitance of M3 is neglected since it is much wider than M1, yielding an input impedance of

$$Z_{in} = \frac{1}{g_{m3} \cdot (1 - A_v) + sC_{gs1}}, \tag{1.10}$$

where A_v represents the transfer from input to the output of the first stage (drain of M2). The transfer can be shown to have positive complex component that is proportional to frequency with the form

$$A_v = \alpha + s\beta, \tag{1.11}$$

where α represents the real part and β represents the imaginary part of the transfer. Via $g_{m3} \cdot (1 - A_v)$ this results in a admittance looking into the source of M3 of:

$$Y_{in,M3} = g_{m3} \cdot (1 - \alpha - s\beta) = (1 - \alpha)g_{m3} - s\beta g_{m3}. \tag{1.12}$$

The last term in Equation 1.12 behaves like a negative capacitor if $\beta > 0$.

The second stage senses the voltage difference between the input of the LNA (v_{in}) and the output of the cascode stage, the main reasons for doing this is better NF and higher gain.

One of the most important design criteria for the second stage is a tail current source with high input impedance, because the output of the core LNA is unbalanced[3]. The noise of the second stage can be neglected as the first stage provides gain.

1.6 Bulk CMOS vs. FDSOI

The LNA in this report was implemented in Fully-Depleted Silicon-On-Insulator (FDSOI) transistors, the difference between the buildup of bulk CMOS and FDSOI transistors is shown in Figure 1.7. An important difference for the implementation in this report is that the substrate of FDSOI transistors is isolated by a thin oxide layer, this allows for body bias voltages that would normally be impossible due to the body diode present in bulk CMOS. 22nm FDSOI was chosen to explore the possibilities of LNA design in technology with high f_T.

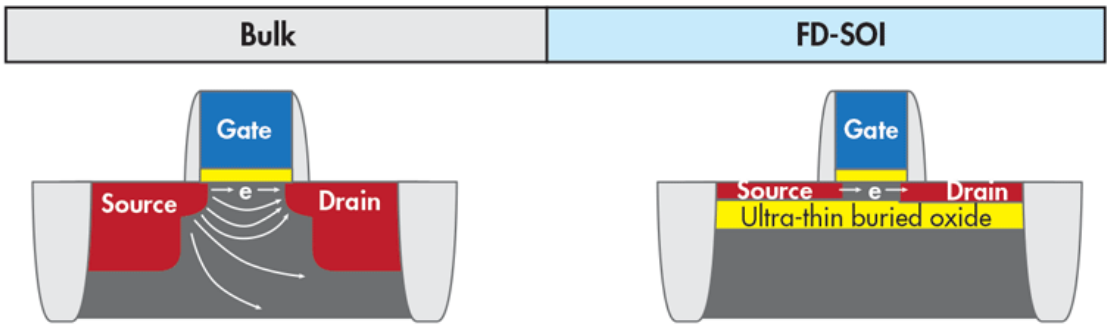


Figure 1.7: Bulk and FDSOI CMOS transistor comparison. Source: http://www.electronicdesign.com/automotive/dual-core-soc-utilizes-fd-soi-low-power-and-high-performance

1.7 Thesis outline

The first part (chapter 2) of the thesis will be used to present the transfer function of the active negative C LNA, this transfer function is then used to explain how negative capacitance is generated. The chapter on the LNA's transfer functions finishes with an exploration of the effect of negative capacitance on the noise figure and gain of the LNA.

The purpose of the second part (chapter 3) is to derive an expression for the noise figure of the negative C LNA, an expression will also be derived for a BALUN LNA and a active shunt-feedback LNA[4] to allow for comparison of noise figure at equal power.

[3] The voltage gain of the cascode could be set to -1, but this would yield unacceptably low gain (6 dB)
[4] The negative C LNA, where the cross-coupling feedback loop is broken.

In the third part (chapter 4) multiple designs will be presented where the back-gate that is present in 22nm FDSOI is utilized to achieve better nonlinearity. This part will conclude with a final design.

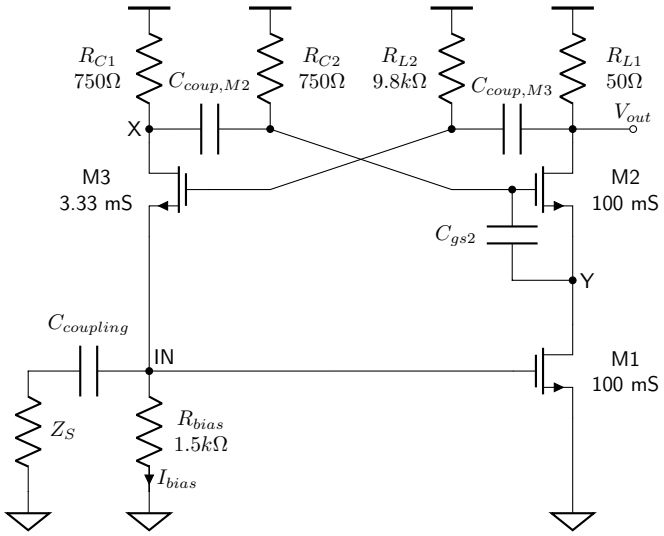
The report ends with conclusions and recommendations for future research.

Chapter 2

LNA transfer characteristics

In this chapter we will analyze the transfer of the LNA proposed by Belostotski. The core of the LNA is shown in Figure 2.1, the gate-source capacitance of M2 is shown because this is the main component that generates a negative capacitor, as will be shown analytically.

The LNA includes two signal paths to the output. The first path is created by M3, leading to output swing through I-V conversion by R_C and subsequent V-I and I-V conversion via M2 and R_L. The second path is formed by a cascode stage (M1, M2 and R_L). The latter path is expected to be dominant for gain, but both paths are taken into account for the analysis.



Bias overview				
Transistor	**Size**	I_d	g_m	V_{ov}
M1	150u/40n	7.7 mA	100 mS	145 mV
M2	150u/40n	7.7 mA	100 mS	145 mV
M3	4.5u/40n	263 uA	3.3 mS	145 mV

Figure 2.1: The core LNA of the active -C LNA (second stage not shown). This is the implementation before linearity optimization.

For the following analysis we take the following assumptions: 1) the channel length modulation of M2 and M3 are ignored, only the gate-source capacitance of M2 is taken into account. 2) The coupling capacitors are assumed to be shorts for AC-analysis. For the path through M1, we have a cascode stage yielding

$$v_{out}|_{\text{transfer via M1}} = -v_{in} g_{m1} \cdot \frac{g_{m2} g_c R_L}{g_c \cdot (g_{ds1} + sC_{gs2} + g_{m2}) + sC_{gs2} g_{ds1} - g_{m2} g_{m3} R_L g_{ds1}}, \qquad (2.1)$$

where $g_c = 1/(R_{C1} + R_{C2})$. M3 forms a g_m-boosted CG stage, as shown in Figure 2.2. The CG-stage is slightly boosting itself via the gain A. Note: *The resistor Z represents the impedance seen when looking out of the drain of M3, $Z \neq R_C$.*

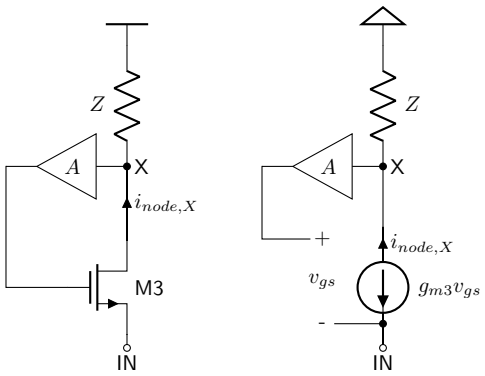


Figure 2.2: Simplified CG with feedback (left) and the small signal equivalent (right).

$$v_{out}|_{\text{transfer via M3}} = -v_{in} \cdot \frac{g_{ds1}g_{m2}R_Lg_{m3}}{g_c \cdot (g_{ds1} + sC_{gs2} + g_{m2}) + g_{ds1}sC_{gs2} - g_{ds1}g_{m2}R_Lg_{m3}} \tag{2.2}$$

The total transfer function is the sum of transfer functions given in (2.1) and (2.2), yielding:

$$\begin{aligned} A_v = \frac{v_{out}}{v_{in}} &= -\frac{g_{ds1}g_{m2}R_Lg_{m3}}{g_c \cdot (g_{ds1} + sC_{gs2} + g_{m2}) + g_{ds1}sC_{gs2} - g_{ds1}g_{m2}g_{m3}R_L} \\ &\quad - \frac{g_{m1}g_{m2}g_cR_L}{g_c \cdot (g_{ds1} + sC_{gs2} + g_{m3}) + g_{ds1}sC_{gs2} - g_{ds1}g_{m2}g_{m3}R_L} \\ &= -\frac{g_{ds1}g_{m2}g_{m3}R_L + g_cg_{m1}g_{m2}R_L}{g_c \cdot (g_{ds1} + sC_{gs2} + g_{m2}) + g_{ds1}sC_{gs2} - g_{ds1}g_{m2}g_{m3}R_L} \\ &= -\frac{g_{ds1}g_{m2}g_{m3}R_CR_L + g_{m1}g_{m2}R_L}{g_{ds1} + sC_{gs2} + g_{m2} + g_{ds1}R_CsC_{gs2} - g_{ds1}g_{m2}g_{m3}R_CR_L} \\ &= -\frac{g_{m2}R_L \cdot (g_{ds1}g_{m3}R_C + g_{m1})}{sC_{gs2} \cdot (1 + g_{ds1}R_C) + g_{ds1} + g_{m2} - g_{ds1}g_{m2}g_{m3}R_CR_L} \end{aligned} \tag{2.3}$$

The total transfer function in (2.3) will be used to show how the negative capacitance is generated. The input admittance of the LNA is given by the parallel combination of a g_m-boosted common gate stage and the parasitic capacitance of M1:

$$Y_{in} = sC_{gs1} + g_{m3} \cdot (1 - A_v)\,, \tag{2.4}$$

where A_v is negative, thus power match is possible using a lower value for g_{m3}.

To understand how negative capacitance is created, we will rewrite the voltage gain, script letters are used to prevent confusion with gain and capacitance:

$$-A_v = \frac{g_{m2}R_L \cdot (g_{ds1}g_{m3}R_C + g_{m1})}{g_{m2} \cdot (1 - g_{ds1}g_{m3}R_CR_L) + g_{ds1} + sC_{gs2} \cdot (1 + g_{ds1}R_C)} = \frac{\mathcal{A}}{\mathcal{C} + s\mathcal{D}} \tag{2.5}$$

Multiplying the denominator with its complex conjugate:

$$\frac{\mathcal{A}}{\mathcal{C} + s\mathcal{D}} = \frac{\mathcal{A}\mathcal{C} - s\mathcal{A}\mathcal{D}}{\mathcal{C}^2 - s^2\mathcal{D}^2} = \frac{\mathcal{A}\mathcal{C} - j\omega\mathcal{A}\mathcal{D}}{\mathcal{C}^2 + \omega^2\mathcal{D}^2} \tag{2.6}$$

where

$$\mathcal{A} = g_{ds1}g_{m2}g_{m3}R_CR_L + g_{m1}g_{m2}R_L$$

$$\mathcal{C} = g_{m2} + g_{ds1} - R_CR_Lg_{ds1}g_{m2}g_{m3}$$

$$\mathcal{D} = C_{gs2} + g_{ds1}R_CC_{gs2}$$

$$\mathcal{A}\mathcal{C} = (g_{ds1}g_{m2}g_{m3}R_CR_L + g_{m1}g_{m2}R_L) \cdot (g_{m2} + g_{ds1} - R_CR_Lg_{ds1}g_{m2}g_{m3})$$

$$\mathcal{A}\mathcal{D} = (g_{ds1}g_{m2}g_{m3}R_CR_L + g_{m1}g_{m2}R_L) \cdot (C_{gs2} + g_{ds1}R_CC_{gs2})$$

Combined with (2.6):

$$\begin{aligned}\frac{G_{source,M3}}{g_{m3}} = \Re\left[-A_v\right] &= \Re\left[\frac{g_{m2}R_L\cdot\left(g_{ds1}g_{m3}R_C+g_{m1}\right)}{g_{m2}\cdot\left(1-g_{ds1}g_{m3}R_CR_L\right)+g_{ds1}+sC_{gs2}\cdot\left(1+g_{ds1}R_C\right)}\right] \\ &= \frac{g_{ds1}g_{m2}^2g_{m3}R_CR_L+g_{ds1}^2g_{m2}g_{m3}R_CR_L+g_{m1}g_{m2}^2R_L+g_{ds1}g_{m1}g_{m2}R_L}{\left(g_{m2}\cdot\left(1-g_{ds1}g_{m3}R_CR_L\right)+g_{ds1}\right)^2+\omega^2\left(C_{gs2}\cdot\left(1+g_{ds1}R_C\right)\right)^2} \\ &\quad -\frac{g_{ds1}^2g_{m2}^2g_{m3}^2R_C^2R_L^2+g_{ds1}g_{m1}g_{m2}^2g_{m3}R_L^2R_C}{\left(g_{m2}\cdot\left(1-g_{ds1}g_{m3}R_CR_L\right)+g_{ds1}\right)^2+\omega^2\left(C_{gs2}\cdot\left(1+g_{ds1}R_C\right)\right)^2}\end{aligned} \tag{2.7}$$

$$\begin{aligned}\frac{B_{source,M3}}{g_{m3}} = \Im\left[-A_v\right] &= \Im\left[\frac{g_{m2}R_L\cdot\left(g_{ds1}g_{m3}R_C+g_{m1}\right)}{g_{m2}\cdot\left(1-g_{ds1}g_{m3}R_CR_L\right)+g_{ds1}+sC_{gs2}\cdot\left(1+g_{ds1}R_C\right)}\right] \\ &= -\omega\cdot\left[\frac{g_{ds1}g_{m2}g_{m3}R_CR_LC_{gs2}+g_{ds1}^2g_{m2}g_{m3}R_C^2R_LC_{gs2}}{\left(g_{m2}\cdot\left(1-g_{ds1}g_{m3}R_CR_L\right)+g_{ds1}\right)^2+\omega^2\left(C_{gs2}\cdot\left(1+g_{ds1}R_C\right)\right)^2}\right. \\ &\quad \left.+\frac{g_{m1}g_{m2}R_LC_{gs2}+g_{ds1}g_{m1}g_{m2}R_LR_CC_{gs2}}{\left(g_{m2}\cdot\left(1-g_{ds1}g_{m3}R_CR_L\right)+g_{ds1}\right)^2+\omega^2\left(C_{gs2}\cdot\left(1+g_{ds1}R_C\right)\right)^2}\right]\end{aligned} \tag{2.8}$$

Interpretation of the last result can be made easier by referring back at (2.6) and noting that (2.8) can be rewritten as

$$\frac{B_{source,M3}}{g_{m3}} = \Im\left[\frac{\mathcal{AC}-j\omega\mathcal{AD}}{\mathcal{C}^2+\omega^2\mathcal{D}^2}\right] = \frac{-\omega\mathcal{AD}}{\mathcal{C}^2+\omega^2\mathcal{D}^2} \tag{2.9}$$

If $\omega^2\mathcal{D}^2 \ll \mathcal{C}^2$, the admittance behaves like a negative capacitor ($B \approx -\omega\mathcal{AD}/\mathcal{C}^2$). For large values of ω the system starts behaving like an inductor ($B \approx -\mathcal{A}/\omega\mathcal{D}$), this behavior is sketched in Figure 2.3, where $\mathcal{A}=\mathcal{C}=\mathcal{D}=1$. Note: *The susceptance in* (2.9) *only accounts for part of the total susceptance, the susceptance looking into the source of M3.* At high frequencies, the susceptance due to M3 will go to zero while the susceptance due to the capacitance of M1 increases, yielding a total susceptance of ωC_{gs1}.

By taking the derivative of $B_{source,M3}/g_{m3}$ and setting it to zero, the frequency ($\omega_{C\to L}$) at which the susceptance switches from capacitive to inductive behavior can be obtained:

$$\frac{d}{d\omega}\left[\frac{B_{source,M3}\left(\omega_{C\to L}\right)}{g_{m3}}\right] = 0 \to \omega_{C\to L} = \sqrt{\frac{\mathcal{C}^2}{\mathcal{D}^2}} \tag{2.10}$$

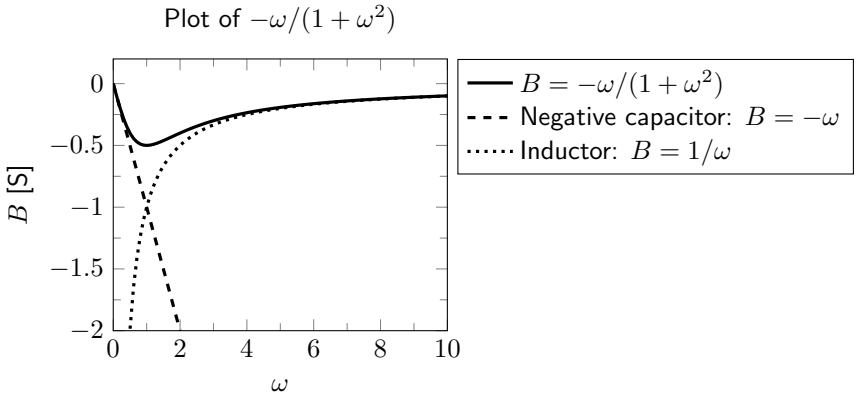


Figure 2.3: Sketch of the function $B=-\omega/\left(1+\omega^2\right)$.

2.1 Active negative C BALUN LNA

The Belostotski LNA is not the only LNA that incorporates an active negative capacitor, which will be shown in this section.

At low frequencies, the input susceptance of a common-gate transistor with a resistor in the gate and a gate-source capacitor (see Figure 2.4) also yields negative capacitance, as seen from equation (2.11) and (2.12). This behavior can possibly be used to cancel the input capacitance of the CS transistor, hence increasing bandwidth and achieving noise match.

$$Y_{in} = \frac{g_{m1} + j\omega \cdot (C_{gs1} - g_{m1} R_G C_{gs1}) + \omega^2 R_G C_{gs1}^2}{1 + \omega^2 \cdot (R_G C_{gs1})^2} \tag{2.11}$$

For low frequency it behaves like a capacitor and a parallel resistor:

$$\begin{aligned} \lim_{\omega \to 0} [Y_{in}] &= \lim_{\omega \to 0} \left[\frac{i_{in}}{v_{in}} \right] \\ &= g_{m1} + j\omega \left(C_{gs1} - g_{m2} R_G C_{gs1} \right) \end{aligned} \tag{2.12}$$

where the equivalent capacitor and resistor are given by:

$$\begin{aligned} C_{eq} &= (1 - g_{m1} R_G) \cdot C_{gs1} \\ R_{eq} &= 1/g_{m1} \end{aligned}$$

At higher frequencies the circuit behaves like a parallel combination of an inductor and a resistor:

$$\begin{aligned} \lim_{\omega \to \infty} [Y_{in}] &= \lim_{\omega \to \infty} \left[\frac{i_{in}}{v_{in}} \right] \\ &= \frac{j\omega \cdot (C_{gs1} - g_{m1} R_G C_{gs1}) + \omega^2 R_G C_{gs1}^2}{(\omega R_G C_{gs1})^2} \\ &= \frac{1}{R_G} + \frac{j\left(1 - g_{m1} R_G\right)}{\omega R_G^2 C_{gs1}} \\ &= \frac{1}{R_G} + \frac{1}{j\omega \frac{R_G^2 C_{gs1}}{g_{m1} R_G - 1}}, \end{aligned} \tag{2.13}$$

where the equivalent inductor and resistor are given by:

$$\begin{aligned} L_{eq} &= \frac{R_G^2 C_{gs1}}{g_{m1} R_G - 1} \approx \frac{R_G C_{gs1}}{g_{m1}} \\ R_{eq} &= R_G \end{aligned}$$

The latter result can also be found intuitively; at high frequencies the gate-source capacitance is effectively a short, so the input source only sees R_G.

Using the same approach as in (2.10), we find:

$$\omega_{C \to L} = \sqrt{\frac{1}{(R_G C_{gs1})^2}} = \frac{1}{R_G C_{gs1}}. \tag{2.14}$$

Equation (2.12) and (2.14) show that there is a clear trade-off between the negative C that can be achieved and the maximum frequency at which the susceptance still behaves like a negative capacitor in the CG-stage; *the negative capacitance is proportional to* R_G (2.12)*, but the maximum frequency is inversely proportional to* R_G (2.13).

Equivalent capacitance at 500 MHz				
R_G	**Equivalent cap.**		R_G	**Equivalent cap.**
0	690 fF		600	59 fF
200	480 fF		800	-136 fF
400	265 fF		1000	-320 fF

Table 2.1: Overview of the equivalent capacitance at 500 MHz ($C_{equi} = B_{in}/2\pi f$) in Figure 2.5a. The values give a good approximation of the equivalent capacitance from DC to 500 MHz.

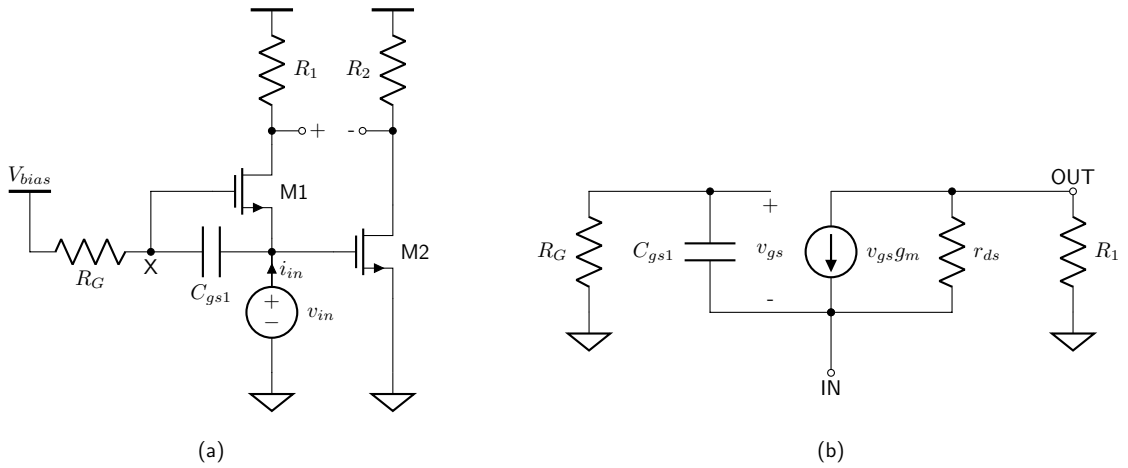


Figure 2.4: (a) CG-stage with resistor in the gate and (b) the small-signal equivalent circuit that yields negative input capacitance.

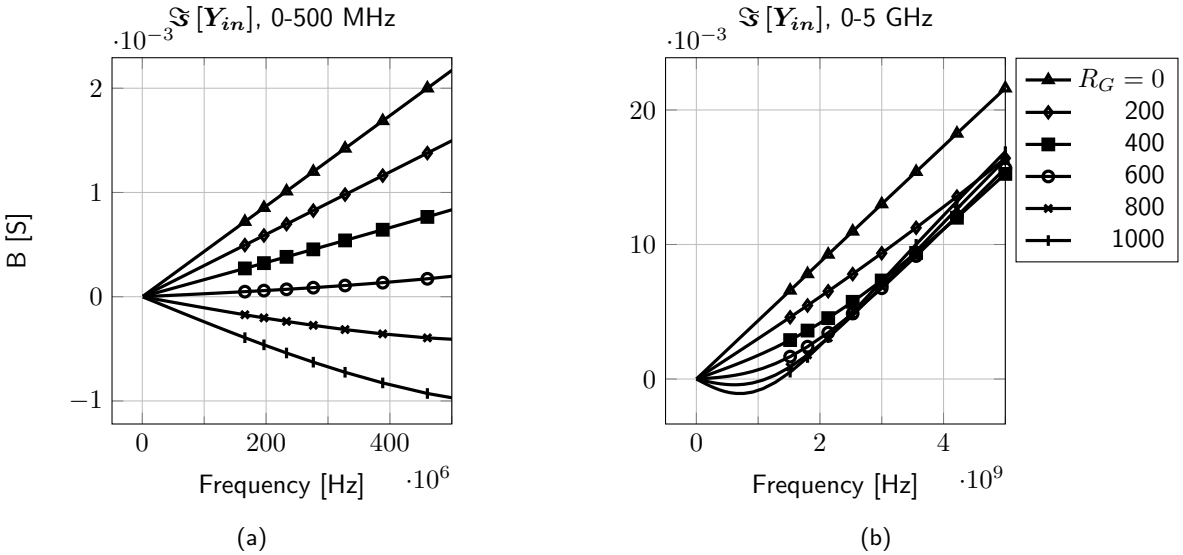


Figure 2.5: Plot of the input susceptance of the LNA in Figure 2.4 versus frequency, with R_G as a sweeping parameter. In the 0 - 500 MHz plot (left) we see the effect of increasing R_G, higher resistance yields stronger negative capacitor behavior. In the plot on the right we see that the frequency range of the negative capacitor is limited, the negative capacitor starts behaving like an inductor (switch from increasing susceptance to decreasing susceptance) around 700 MHz.

2.2 Input susceptance compensation (adding positive capacitance)

Up to this point we assumed that negative capacitance positively affects NF, based on the concept of noise matching. In this section we will try to quantify how strongly and why the negative capacitance affects the NF of the Belostotski LNA.

The design used in the simulations in this section is shown in Figure 2.1

In Figure 2.8 we see the results of the simulation of the circuit in Figure 2.1, where a capacitor is added between signal ground and the source of M3 (see Figure 2.6). This capacitor is used to compensate for the negative capacitance generated by M3, as seen in the simulation results, two things happen when increasing the value of C_{comp}:

- The bandwidth decreases, this is as expected since the input pole shifts to lower frequencies.
- The NF increases, deviating more from NF_{min} (dashed line) as C_{comp} increases.

The NF increased by 0.13 dB at 6 GHz, this could be interpreted as proof that the noise matching

principle is working. But since the voltage gain at 6 GHz has decreased slightly (0.3 dB), the increase of NF could very well be due to decreased gain. The effect of the negative capacitor is positive for the gain and indirectly also benefits the noise figure slightly, but the effect of improving NF via correlation (noise matching) does not seem very significant in this case.

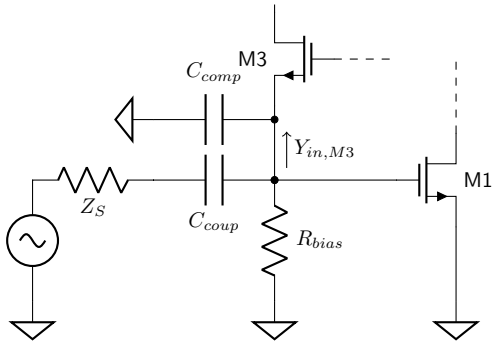


Figure 2.6: Part of the LNA in Figure 2.1, showing the added ideal capacitor and definition of the input susceptance $Y_{in,M3}$.

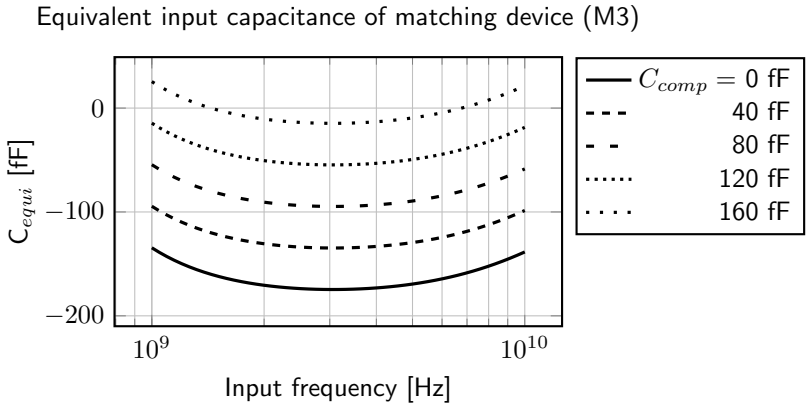
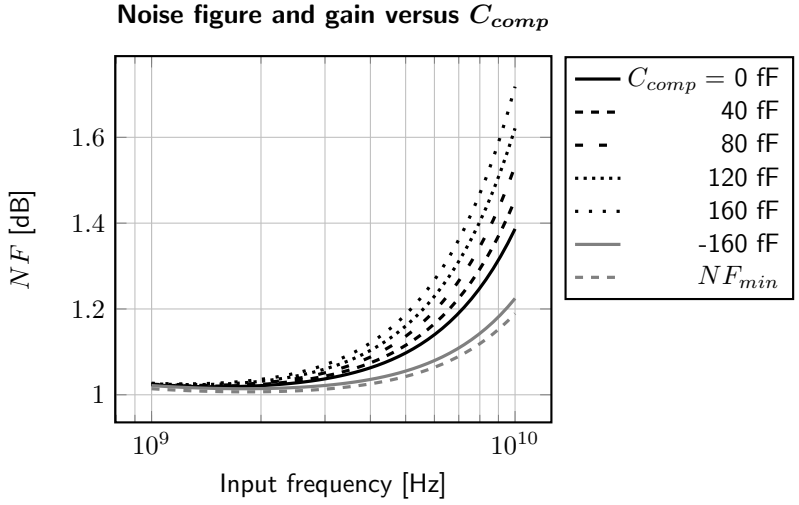
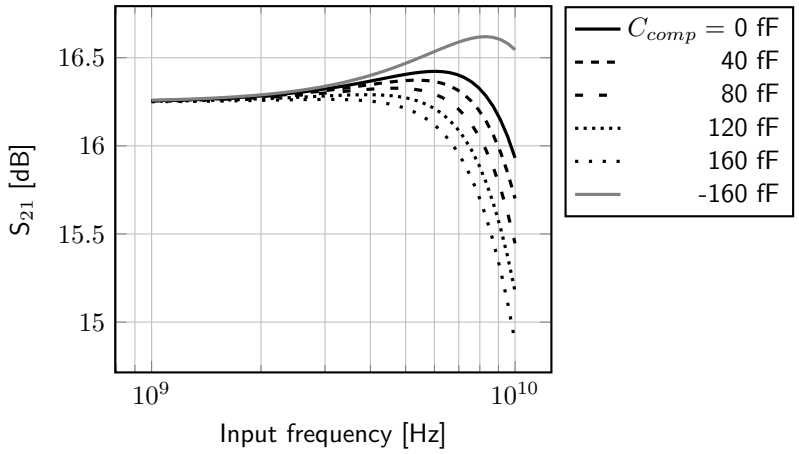


Figure 2.7: The equivalent perceived capacitance at the source of M3 in Figure 2.6. $C_{equi} = \Im\left[B_{in,M3}\right]/\omega_{in}$



(a) Noise figure versus compensation capacitance.



(b) Forward voltage gain versus compensation capacitance.

Figure 2.8: Plot of the NF and gain of the circuit in Figure 2.6, where the value of C_{comp} is increased until the negative capacitance (at 6 GHz) is almost perfectly cancelled. In (a) we see that the noise figure deviates strongly from NF_{min} when the negative capacitance generated by M3 is compensated. In (b) the decrease in bandwidth is shown when the negative capacitance is decreased (by increasing C_{comp}). The equivalent capacitance at 6 GHz is -164 fF when no compensation capacitor is applied. The black line without markers shows the NF and gain when the total input capacitance (including $C_{in,M1}$) is cancelled by adding -160 fF.

Chapter 3

Noise analysis

In this chapter we will analyze the noise transfer of each of the noise sources in the Belostotski LNA, to allow for optimization of the circuit and better understanding of the low NF that is achieved by Belostotski's LNA [2]. The same noise analysis will also be performed on a BALUN and regular shunt feedback LNA, to compare the noise figure/factor to that of other LNA topologies.

The noise analysis is simplified by first solving for the output voltage $v_{out,N}$ as function of a current $i_{inject,N}$ injected into node N, yielding a transresistance:

$$r_{inject,N} \equiv \frac{v_{out,N}}{i_{inject,N}} \tag{3.1}$$

The resulting transresistances can be used to analyze how the noise of the individual components transfers to the output, since each noisy component can be represented by adding a parallel noise current source that sinks or sources current into the different nodes within the LNA.

3.1 Belostotski LNA (active negative C LNA)

Transresistance of the nodes

Node X

The current gets transferred to the output via two paths:

1. The swing at the X node causes a swing at the Y node through the imperfect source follower formed by M1 and M2.

2. The swing at node X also causes an in-phase swing at the input node, which translates to an output swing via g_{m1} and R_L.

Assuming that the impedance looking into the drain of M3 is much larger than R_C, for the first path we have a transfer of:

$$A_1 = \left.\frac{v_{out}}{i_{inject,X}}\right|_{OL} = R_C \frac{-g_{m2}}{1+g_{m2}r_{ds1}} R_L \tag{3.2}$$

$$\beta_1 = \left.\frac{i_{sd,3}}{v_{out}}\right|_{OL} = \frac{-g_{m3}}{1+g_{m3}R_S} \tag{3.3}$$

$$\begin{aligned} r_{inject,X,1} = \left.\frac{v_{out}}{i_{inject,X}}\right|_{CL} &= \frac{A_1}{1-A_1\beta_1} \\ &= \frac{-R_C R_L g_{m2}}{1+g_{m2}r_{ds1} - \frac{g_{m2}g_{m3}}{1+g_{m3}R_S}} \end{aligned} \tag{3.4}$$

For the second path we have a transfer of

$$A_2 = \left.\frac{v_{out}}{i_{inject,X}}\right|_{OL} = -R_C \frac{R_S}{R_S + r_{ds3} + r_{ds3} R_S g_{m3} \cdot (1 - g_{m1} R_L)} g_{m1} R_L \tag{3.5}$$

$$\beta_2 = \left.\frac{i_{sd,3}}{v_{out}}\right|_{OL} = \frac{-g_{m3}}{1 + g_{m3} R_S} \tag{3.6}$$

$$r_{inject,X,2} = \left.\frac{v_{out}}{i_{inject,X}}\right|_{CL} = \frac{A_2}{1 - A_2 \beta_2} \tag{3.7}$$

The combined transresistance is

$$\begin{aligned} r_{inject,X} &= r_{inject,X,1} + r_{inject,X,2} \\ &= -R_C \cdot \left(\frac{g_{ds3} R_S g_{m1} R_L}{1 + g_{ds3} R_S + g_{m3} \cdot (1 - A_v) R_S} + \frac{g_{m2} R_L}{1 + g_{m2} r_{ds1}} \right) \\ &= -R_C \cdot \left(\frac{g_{ds3} R_S g_{m1} R_L}{2 + g_{ds3} R_S} + \frac{g_{m2} R_L}{1 + g_{m2} r_{ds1}} \right) \\ &\qquad \text{Assuming that the intrinsic gain of M1 and M2 is much greater that 1} \\ &\approx -R_C \cdot \left(\frac{g_{ds3} R_S g_{m1} R_L}{2} + \frac{R_L}{r_{ds1}} \right) \end{aligned} \tag{3.8}$$

In the current implementation the first path accounts for a transfer of approximately $1/40 \cdot R_C$ while the second path accounts for $-1/4 \cdot R_C$.

This result might be surprising, since generally the contribution of gate voltage variation of the CS transistor in a cascode (M1 in Figure 2.1) is much larger than the contribution of the gate voltage of the CG transistor (M2 in Figure 2.1). But in the LNA, the gate voltage variation of the CS transistor (M1) is a scaled version of the variation at the gate of the CG transistor (M2). This scaling factor is approximately $(1/2) \cdot R_S / r_{ds3}$, making the variation of M2 200x times larger than that of M1.

Node Y

To solve for the transresistance we assume that simple negative feedback is taking place: the forward gain A is given by the current to voltage conversion at the output node

$$A = \left.\frac{v_{n,OUT}}{i_{n,injected}}\right|_{OL} = R_L. \tag{3.9}$$

the reverse transfer is given by the transfer from the output node to the input node and its consecutive conversion to a current via g_{m1}:

$$\beta = \left.\left(\frac{v_{n,IN}}{v_{n,OUT}} \cdot \frac{i_{ds,1}}{v_{n,IN}} \right)\right|_{OL} = -\frac{g_{m3} R_S}{1 + g_{m3} R_S} g_{m1} \tag{3.10}$$

Combined, the previous equations yield the closed loop transfer

$$\begin{aligned} r_{inject,Y} = \frac{v_{out,Y}}{i_{inject,Y}} &= \frac{A}{1 - A\beta} \\ &= \frac{R_L \cdot (1 + g_{m3} R_S)}{1 + g_{m3} R_S + g_{m1} g_{m3} R_L R_S} \end{aligned} \tag{3.11}$$

Node IN

The transresistance is given by the parallel combination of the source and input impedance, multiplied by the gain of the LNA:

$$r_{inject,IN} = \frac{v_{out,IN}}{i_{inject,IN}} = (Z_S \parallel Z_{in}) \cdot A_v \tag{3.12}$$

In case of input match:

$$r_{inject,IN} = -\frac{1}{2} Z_S g_{m1} R_L \tag{3.13}$$

Node OUT

The transfer is due to negative feedback:

$$A = \left.\frac{v_{out,OUT}}{i_{inject,OUT}}\right|_{OL} = R_L. \tag{3.14}$$

$$\beta = \left.\frac{-i_{ds,2}}{v_{R_C}}\right|_{OL} = -\frac{g_{m3}R_S}{1+g_{m3}R_S}\cdot g_{m1}, \tag{3.15}$$

Here we assume that the transfer via R_C and the gate of M2 is negligible. The closed loop transresistance is given by:

$$\begin{aligned} r_{inject,OUT} = \left.\frac{v_{out,OUT}}{i_{inject,OUT}}\right|_{CL} &= \frac{A}{1-A\beta} \\ &= \frac{R_L}{1+R_L g_{m1}\frac{g_{m3}R_S}{1+g_{m3}R_S}} \\ &= \frac{R_L\cdot(1+g_{m3}R_S)}{1+g_{m3}R_S+g_{m1}g_{m3}R_L R_S} \\ &= \frac{R_L\cdot(1+g_{m3}R_S)}{1+g_{m3}\cdot(1+g_{m1}R_L)\,R_S} \\ &= \frac{R_L\cdot(1+g_{m3}R_S)}{2} \end{aligned} \tag{3.16}$$

The last step can be taken since $g_{m3}\cdot(1+g_{m1}R_L)\,R_S = 1$ if the LNA is power matched. The transfer is equal to the result for node Y, which is not surprising since M2 approximately operates as a current buffer.

Noise contributions per component

In the previous sections we derived the transresistances for each of the nodes, we can use these to describe the output voltage as function of the current injected by component C (C does not represent a capacitance, but is replaced by the component name when filling in the equation e.g. M_1 or R_C):

$$r_{transfer,C} \equiv \frac{v_{out,C}}{i_{injected,C}}, \tag{3.17}$$

where $r_{transfer,C}$ indicated the transresistance of component C, and $v_{out,C}$ and $i_{injected,C}$ represent the output voltage and injected current of component C respectively. Including the sign of each of the noise currents:

$$\begin{aligned} r_{transfer,M1} &= -r_{inject,Y} \\ r_{transfer,M2} &= r_{inject,Y} - r_{inject,OUT} \\ r_{transfer,M3} &= r_{inject,IN} - r_{inject,X} \\ r_{transfer,R_L} &= r_{inject,OUT} \\ r_{transfer,R_C} &= r_{inject,X} \\ r_{transfer,Z_S} &= r_{transfer,R_{bias}} = r_{inject,IN} \end{aligned}$$

We see a trade-off in the noise transresistances associated to $M3$ and R_C: For full cancellation of M3's noise, i.e. $r_{transfer,M3} = 0$, r_{inject} has to equal $r_{inject,IN}$. In that case the transfer of signal current to output voltage is equal to the transfer of the noise current of R_C to the output. The added noise in percent due to R_C is then given by $(Z_S/R_C)\cdot 100\%$. The noise of M2 is fully cancelled, since from analysis follows $r_{inject,Y} = r_{inject,OUT}$

Noise when sensing difference between node IN and OUT

The noise figure can be improved by sensing the difference between the voltages at IN and OUT instead of sensing OUT versus signal ground, as will be shown in this section.

Node X

Node X is in phase with the IN node:

$$\begin{aligned} r_{inject,diff,X} &= r_{inject,X} - r_{inject,X}\frac{g_{m3}R_S}{1+g_{m3}R_S} \\ &= \left(1 - \frac{g_{m3}R_S}{1+g_{m3}R_S}\right) \cdot r_{inject,X} \\ &= \frac{1}{1+g_{m3}R_S} \cdot r_{inject,X} \end{aligned} \tag{3.18}$$

Node Y

The transresistance is proportional to the I-V conversion to the output, minus the transfer from OUT to IN (via M3 as resistive degenerated CS). The feedback that takes place is already accounted for in $r_{inject,Y}$:

$$\begin{aligned} r_{inject,diff,Y} &= r_{inject,Y} \cdot \left(1 - \frac{g_{m3}R_S}{1+g_{m3}R_S}\right) \\ &= \frac{R_L \cdot (1+g_{m3}R_S)}{1+g_{m3}R_S+g_{m1}g_{m3}R_LR_S} \cdot \left(1 - \frac{g_{m3}R_S}{1+g_{m3}R_S}\right) \\ &= \frac{R_L \cdot (1+g_{m3}R_S)}{1+g_{m3}R_S+g_{m1}g_{m3}R_LR_S} \cdot \frac{1}{1+g_{m3}R_S} \\ &= \frac{R_L}{1+g_{m3}R_S+g_{m1}g_{m3}R_LR_S} \\ &= \frac{R_L}{1+g_{m3}R_S \cdot (1+g_{m1}R_L)} \\ &\quad \text{Assuming input match } (g_{m3} \cdot (1+g_{m1}R_L) = R_S^{-1}): \\ &= \frac{R_L}{2} \end{aligned} \tag{3.19}$$

Node IN

$$r_{inject,diff,IN} = \frac{v_{out,IN}}{i_{inject,IN}} = (Z_S \parallel Z_{in}) \cdot (A_v - 1) \tag{3.20}$$

In case of input match:

$$r_{inject,diff,IN} = -\frac{1}{2}Z_S \cdot (g_{m1}R_L + 1) \tag{3.21}$$

Node OUT

The transfer from the OUT node is equal to that of the Y node:

$$\begin{aligned} r_{inject,diff,OUT} &= \frac{R_L}{1+g_{m3}R_S+g_{m1}g_{m3}R_LR_S} \\ &\approx \frac{R_L}{2} \end{aligned} \tag{3.22}$$

The benefit of using the voltage difference between OUT and IN is that the contribution of all sources that insert current into the IN node are amplified, one of which is the input source.

As a sanity check, the transresistances found are used to calculate the expected noise contribution of the individual components, the following equation is used to calculate the noise power (again using C to denote a given component, e.g. $P_{noise,M1}$ is the noise power at the output due to M1):

$$\overline{v_{noise,C}^2} \equiv \overline{i_{noise,C}^2} \cdot r_{transfer,C}^2, \tag{3.23}$$

where resistors are represented by $4kT/R$ and transistors are represented by $4kT\gamma g_m$ with $\gamma = 1$. The results of the comparison are shown in Table 3.1.

Comparison of analytical and simulation results			
Component	$\lvert r_{inject}\rvert$ [Ω]	**Predicted noise power [v²/Hz]**	**Noise summary [v²/Hz]**
$\boldsymbol{Z_S}$	150	7.20 x 10^{-18}	8.27 x 10^{-18}
$\boldsymbol{M1}$	25	1.00 x 10^{-18}	6.83 x 10^{-19}
$\boldsymbol{R_C}$	108	4.97 x 10^{-19}	5.09 x 10^{-19}
$\boldsymbol{R_L}$	25	2.00 x 10^{-19}	3.28 x 10^{-19}
$\boldsymbol{R_{bias}}$	150	2.40 x 10^{-19}	2.78 x 10^{-19}
$\boldsymbol{M3}$	42	9.40 x 10^{-20}	1.25 x 10^{-19}
$\boldsymbol{M2}$	0	negligible	7.79 x 10^{-20}

Table 3.1: Predicted noise power vs. Cadence noise summary results, components order of highest to lowest contribution.

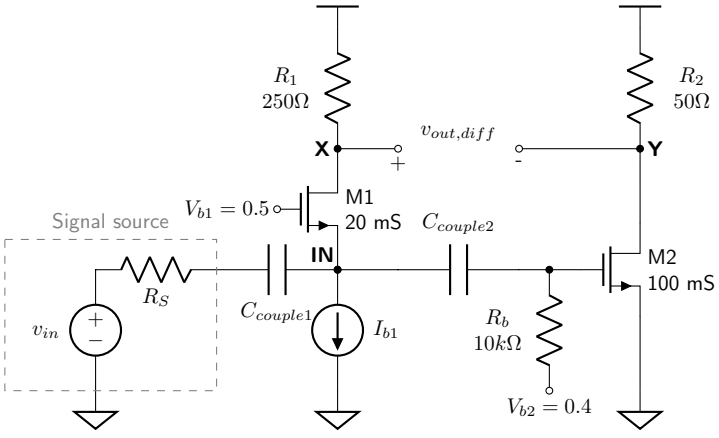
Noise figure based on transresistance

Based on the derived transresistances the noise factor of the Belostotski LNA (as implemented in Figure 2.1) is given by

$$F = 1 + \frac{4R_C R_L^2}{R_S \cdot (g_{m1}R_L + 1)^2 r_{ds1}^2} + \frac{R_S}{R_{bias}} + \frac{R_L}{R_S \cdot (g_{m1}R_L + 1)^2} + \gamma_1 g_{m1} \cdot \frac{R_L^2}{R_S \cdot (g_{m1}R_L + 1)^2} + \gamma_3 g_{m3} \frac{(2R_C R_L - r_{ds1}R_S(g_{m1}R_L + 1))^2}{R_S \cdot (g_{m1}R_L + 1)^2 \cdot r_{ds1}^2}$$

3.2 BALUN LNA

The transresistance approach can also be used to perform noise analysis of the CG-CS BALUN LNA. Figure 3.1 shows the circuit used for analysis. The BALUN LNA was designed with the premise that



Bias overview				
Transistor	**Size**	$\boldsymbol{I_d}$	$\boldsymbol{g_m}$	$\boldsymbol{V_{ov}}$
M1	30u/40n	1.6 mA	20 mS	145 mV
M2	150u/40n	7.7 mA	100 mS	145 mV

Figure 3.1: A CG-CS BALUN LNA. Nodes IN, X and Y shown for noise analysis. The ratio $n = g_{m1}/g_{m2} = R_2/R_1$ is set to 5, this allows the LNA to operate at approximately equal power as the Belostotski LNAs in the previous section (M2 has the same bias current as M1/M2 in Figure 2.1).

power consumption should be approximately equal to that of the Belostotski LNA, to allow for fair comparison. This was achieved by biasing transistor M2 using the same DC current as M1 and M2 in the Belostotski LNA (Figure 2.1).

Transresistance of the nodes

Node X

The current injected into node X gets converted to a voltage by R1 parallel to the small signal resistance seen looking into the drain of M1, r_{drain1}, given by:

$$\begin{aligned} r_{drain,1} = \frac{v_X}{i_{ds,1}} &= \frac{v_{in}}{i_{ds,1}} \cdot \frac{v_X}{v_{in}} \\ &= R_S \cdot \frac{1 + g_{ds1}R_S + g_{m1}R_S}{g_{ds1}R_S} \\ &\approx \frac{1 + g_{m1}R_S}{g_{ds1}} \end{aligned} \tag{3.24}$$

The transfer to the positive output node is given by the parallel combination of R1 and the small-signal resistance looking into the drain of M1:

$$\begin{aligned} r_{inject,X} = R_1 \parallel r_{drain,1} &= \frac{\left(R_1 \cdot \frac{1+g_{m1}R_S}{g_{ds1}}\right)}{\left(R_1 + \frac{1+g_{m1}R_S}{g_{ds1}}\right)} \cdot \left(1 - \frac{v_Y}{v_X}\right) \\ &= \frac{R_1 + g_{m1}R_SR_1}{1 + g_{m1}R_S + R_1g_{ds1}} \cdot \left(1 + \frac{R_Sg_{m2}R_2}{r_{drain,1}}\right) \\ &= R_1\frac{1 + g_{m1}R_S}{1 + g_{m1}R_S + R_1g_{ds1}} \cdot \frac{1 + g_{m1}R_S + R_Sg_{m2}R_2g_{ds1}}{1 + g_{m1}R_S} \\ &= R_1\frac{1 + g_{m1}R_S + R_Sg_{m2}R_2g_{ds1}}{1 + g_{m1}R_S + R_1g_{ds1}} \\ &\quad \text{Replacing } g_{m2}R_2 \text{ by } g_{m1}R_1 \\ &= R_1\frac{1 + g_{m1}R_S + R_Sg_{m1}R_1g_{ds1}}{1 + g_{m1}R_S + R_1g_{ds1}} \\ &= R_1 \end{aligned} \tag{3.25}$$

The last simplification can be applied since $g_{m1}R_S = 1$ if the BALUN LNA is power matched.

Node Y

The current gets converted via R2 parallel to r_{ds2}:

$$\begin{aligned} r_{inject,Y} = R_2 \parallel r_{ds2} &= \frac{R_2r_{ds2}}{R_2 + r_{ds2}} \\ &\quad \text{Ignoring CLM} \\ &\approx R_2 \end{aligned} \tag{3.26}$$

Node IN

The transresistance of node IN is given by the parallel combination of R_S and the resistance looking into the source of M1:

$$\begin{aligned} r_{in,source,M1} = \frac{v_{in}}{-i_{ds1}} &= \frac{v_X}{-i_{ds1}} \cdot \frac{v_{in}}{v_X} \\ &= R_1 \cdot \frac{1 + g_{ds1}R_1}{g_{ds1}R_1 + g_{m1}R_1} \\ &= \frac{1 + g_{ds1}R_1}{g_{ds1} + g_{m1}} \end{aligned} \tag{3.27}$$

This yields the transresistance when combined with the source resistance:

$$\begin{aligned} r_{inject,IN} &= (R_S \parallel r_{in,source,M1}) \cdot (g_{m1}R_1 + g_{m2}R_2) \\ &\quad \text{If the input is matched } (R_S = 1/g_{m1}) \text{ and } R_1g_{m1} = R_2g_{m2} \\ &= \frac{R_S + g_{ds1}R_1R_S}{2 + g_{ds1}R_1 + g_{ds2}R_S} \cdot 2g_{m1}R_1 \\ &= 2 \cdot \frac{R_1 + g_{ds1}R_1^2}{2 + g_{ds1}R_1 + g_{ds2}R_S} \\ &\quad \text{Ignoring CLM} \\ &\approx R_1 \end{aligned} \tag{3.28}$$

Overview

The result of the previous analysis are shown in Table 3.2, a simplified form is also presented where the effect of channel length modulation is ignored. The results in equation (3.29) to (3.35) were verified by comparing the predicted noise contributions to simulation, in Table 3.3.

Summary of BALUN LNA transresistors		
Node	r_{inject} [Ω]	**simplified (no CLM)** [Ω]
X	R_1	R_1
Y	$\frac{R_2 r_{ds2}}{R_2 + r_{ds2}}$	$R_2 = R_1/5$
IN	$2 \cdot \frac{R_1 + g_{ds1} R_1^2}{2 + g_{ds1} R_1 + g_{ds2} R_S}$	R_1

Table 3.2: Overview of transresistances of the BALUN LNA

$$
\begin{aligned}
r_{transfer,Z_S} &= r_{inject,IN} \\
&= 2 \cdot \frac{R_1 + g_{ds1} R_1^2}{2 + g_{ds1} R_1 + g_{ds2} R_S} \qquad (3.29) \\
&\approx R_1 \\
r_{transfer,R_{bias}} &= r_{inject,IN} \\
&= 2 \cdot \frac{R_1 + g_{ds1} R_1^2}{2 + g_{ds1} R_1 + g_{ds2} R_S} \qquad (3.30) \\
&\approx R_1 \\
r_{transfer,M1} &= r_{inject,IN} - r_{inject,X} \\
&= \frac{2R_1 + 2g_{ds1} R_1^2}{2 + g_{ds1} R_1 + g_{ds2} R_S} - R_1 \qquad (3.31) \\
&= \frac{-2 g_{ds2} R_S R_1}{2 + g_{ds1} R_1 + g_{ds2} R_S} \qquad (3.32) \\
&\approx 0 \\
r_{transfer,M2} &= -r_{inject,Y} \\
&= -\frac{R_2 r_{ds2}}{R_2 + r_{ds2}} \qquad (3.33) \\
&\approx -R_2 = -R_1/5 \\
r_{transfer,R_1} &= r_{inject,X} \\
&= R_1 \qquad (3.34) \\
r_{transfer,R_2} &= r_{inject,Y} \\
&= \frac{R_2 r_{ds2}}{R_1 + r_{ds2}} \qquad (3.35) \\
&\approx R_2 = R_1/5
\end{aligned}
$$

Comparison between Belostotski and BALUN LNA

The results of the noise analysis can be used to compare the noise contributions and hence noise figure/factor of both LNAs.

The noise factor for the BALUN LNA (as implemented in Figure 3.1) is given by

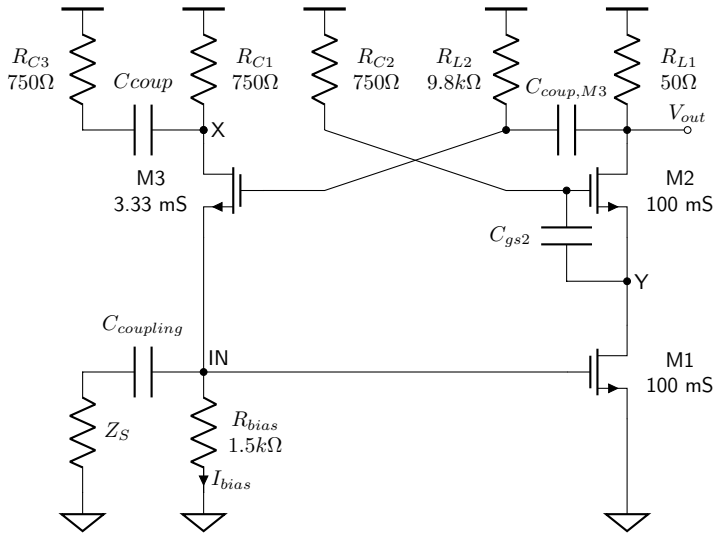
$$
\begin{aligned}
F &= 1 + \frac{R_b^{-1} \cdot R_1^2 + R_1 + \frac{1}{n} R_1 + \gamma_1 g_{m1} \cdot (R_1 - R_1) + \gamma_2 g_{m2} \frac{1}{n^2} R_1^2}{R_S^{-1} R_1^2} \\
&= 1 + \frac{R_S}{R_b} + \frac{(n+1) \cdot R_S}{n R_1} + \frac{\gamma_2 g_{m2} R_S}{n^2}
\end{aligned}
$$

Summary of BALUN LNA implementation results			
Component	$\|r_{inject}\|$ [Ω]	**Predicted noise power [v²/Hz]**	**Noise summary [v²/Hz]**
R_S	291	2.71 x 10^{-17}	1.75 x 10^{-17}
R_1	250	4.00 x 10^{-18}	3.80 x 10^{-18}
$M2$	33	1.15 x 10^{-18}	1.47 x 10^{-18}
$M1$	24	1.21 x 10^{-19}	1.21 x 10^{-18}
R_2	33	5.64 x 10^{-19}	4.36 x 10^{-19}
R_b	291	1.35 x 10^{-19}	9.07 x 10^{-20}

Table 3.3: Predicted noise power (equation (3.23)) vs. Cadence noise summary results, the order of the components is from highest to lowest noise contribution according to the noise summary. Noise summary was generated for spot noise at 5.8 GHz, using a 50 ohm input port and 1 mega-ohm output port connected to the differential output in Figure 3.1. r_{ds1} and r_{ds2} were found in simulation to be 700 uS and 2 mS respectively, corresponding to an intrinsic gain in the order of 30-50.

3.3 Regular active shunt feedback LNA (Belostotski without feedback of CG-output)

Simulation results suggests that the active -C LNA could perform even better when the load of the CG stage gets disconnected from the gate of M2, this would yield a regular shunt feedback circuit (see Figure 3.2).



Bias overview				
Transistor	**Size**	I_d	g_m	V_{ov}
M1	150u/40n	7.7 mA	100 mS	145 mV
M2	150u/40n	7.7 mA	100 mS	145 mV
M3	4.5u/40n	263 uA	3.3 mS	145 mV

Figure 3.2: The core LNA of the active -C LNA, the coupling capacitor between the drain of M3 and the gate of M2 removed. A coupling capacitor is used in combination with R_{C3} to ensure that the load of M3 remains unchanged (when compared to Figure 2.1).

Transresistance of the nodes

We will perform the transresistance analysis again for the LNA in Figure 3.2

Node X

The noise due to this node is ignored, since analysis has already shown that the noise path via M3 is negligible (Equation 3.7), the path via M2 is no longer present.

Node IN

The transresistance of this node is related to the gain of the circuit:

$$r_{transfer,IN} = \frac{v_{out,IN}}{i_{inject,IN}} = (Z_S \parallel Z_{in}) \cdot A_v$$

$$\text{Assuming input match } (g_{m3}(1 - A_v) = 1/Z_S): \tag{3.36}$$

$$= -\frac{1}{2} Z_S g_{m1} R_L$$

Node OUT

The transresistance of this node is related to the gain of the circuit:

$$A = \left.\frac{v_{out,OUT}}{i_{inject,OUT}}\right|_{OL} = R_L \tag{3.37}$$

$$\beta = \left.\frac{i_{ds1}}{v_{out,OUT}}\right|_{OL} = -\frac{g_{m3} Z_S}{1 + g_{m3} Z_S} g_{m1} \tag{3.38}$$

$$r_{inject,OUT} = \frac{A}{1 - A\beta} = \frac{R_L \cdot (1 + g_{m3} Z_S)}{1 + g_{m3} Z_S + g_{m1} g_{m3} Z_S R_L}$$

$$\text{If input is matched } ([1 + g_{m1} R_L] \cdot g_{m3} = 20 \text{ mS}): \tag{3.39}$$

$$= \frac{R_L \cdot (1 + g_{m3} Z_S)}{2}$$

Noise contribution per component

$$\begin{aligned} r_{transfer,Z_S} &= r_{transfer,R_{bias}} \\ &= r_{inject,IN} \\ &= -\frac{1}{2} Z_S g_{m1} R_L \end{aligned} \tag{3.40}$$

$$r_{transfer,R_{C1}} = r_{inject,X}$$

$$\begin{aligned} r_{transfer,R_{C2}} &= R_{C2} \frac{g_{m2} r_{ds1}}{1 + g_{m2} r_{ds1}} \cdot (r_{inject,Y} - r_{inject,OUT}) \\ &= R_{C2} \frac{g_{m2} r_{ds1}}{1 + g_{m2} r_{ds1}} \cdot 0 \end{aligned} \tag{3.41}$$

$$\begin{aligned} r_{transfer,R_L} &= r_{inject,OUT} \\ &= \frac{R_L \cdot (1 + g_{m3} Z_S)}{2} \end{aligned} \tag{3.42}$$

$$\begin{aligned} r_{transfer,M1} &= -r_{inject,Y} \\ &= -r_{inject,OUT} \\ &= -\frac{R_L \cdot (1 + g_{m3} Z_S)}{2} \end{aligned} \tag{3.43}$$

$$\begin{aligned} r_{transfer,M2} &= r_{inject,Y} - r_{inject,OUT} \\ &= r_{inject,OUT} - r_{inject,OUT} \end{aligned} \tag{3.44}$$

$$\begin{aligned} r_{transfer,M3} &= r_{inject,IN} - r_{inject,X} \\ &= -\frac{1}{2} Z_S g_{m1} R_L \end{aligned} \tag{3.45}$$

Noise figure based on transresistance

The transresistances yield a noise factor and figure of

$$\begin{aligned} F &= 1 + \frac{\left(Z_S g_{m1} R_L\right)^2 \cdot \left(1/R_{bias} + \gamma_3 g_{m3}\right) + \left(R_L + g_{m3} Z_S R_L\right)^2 \cdot \left(1/R_L + \gamma_1 g_{m1}\right)}{Z_S g_{m1}^2 R_L^2} \\ &= 1 + \frac{Z_S}{R_{bias}} + \frac{1 + g_{m3} Z_S}{Z_S g_{m1}^2} \left(1/R_L + \gamma_1 g_{m1}\right) + Z_S \gamma_3 g_{m3} \end{aligned} \tag{3.46}$$

If the output is taken as the difference between the voltage at node OUT and IN then the transresistances become (assuming input match in all cases):

$$r_{inject,diff,IN} = -\frac{1}{2} Z_S \left(g_{m1} R_L + 1\right) \tag{3.47}$$

$$r_{inject,diff,X} \approx 0 \tag{3.48}$$

$$\begin{aligned} r_{inject,diff,Y} &= r_{inject,diff,OUT} \\ &= \frac{R_L \cdot (1 + g_{m3} Z_S)}{2} \cdot \left(1 - \frac{g_{m3} Z_S}{1 + g_{m3} Z_S}\right) \\ &= \frac{R_L}{2} \end{aligned} \tag{3.49}$$

The noise transfer due to the source has increased, and the contribution due to currents injected into the OUT and Y nodes have decreased. The noise factor becomes:

$$\begin{aligned} F &= 1 + \frac{Z_S^2 \cdot \left(g_{m1} R_L + 1\right)^2 \cdot \left(1/R_{bias} + \gamma_3 g_{m3}\right) + R_L^2 \cdot \left(1/R_L + \gamma_1 g_{m1}\right)}{Z_S \left(g_{m1} R_L + 1\right)^2} \\ &= 1 + \frac{Z_S}{R_{bias}} + \frac{R_L}{Z_S \cdot \left(g_{m1} R_L + 1\right)} + \frac{R_L^2 \gamma_1 g_{m1}}{Z_S \cdot \left(g_{m1} R_L + 1\right)^2} + Z_S \gamma_3 g_{m3} \end{aligned} \tag{3.50}$$

3.4 Overview of the noise figures found analytically

The noise factor expressions derived in the previous sections are used to compare different topologies, the results of this comparison are shown in Table 3.4.

The LNA by Belostotski has the best noise figure and can achieve sub-1dB noise figure if $\gamma \leq 2/3$. The result for the Belostotski LNA is close to the NF achieved by Belostotski (1 dB) [2].

Summary of noise analysis results					
	Contributor			**NF** [dB]	
Version	**resistors**	**M1**	**M3**	$\gamma_{1,3} = 2/3$	$\gamma_{1,3} = 3/2$
Belostotski (OUT - IN)	1.113	0.139 γ	0.023 γ	0.87	1.32
Shunt FB (OUT)	1.08	0.23 γ	0.17 γ	1.29	2.25
Shunt FB (OUT - IN)	1.06	0.14 γ	0.17 γ	1.03	1.83
	resistors	**M2**			
BALUN	1.25	0.2 γ		1.39	1.89

Table 3.4: Summary of the noise factors and figures found in analysis, based on the designs in Figure 2.1, Figure 3.1 and Figure 3.2. The numbers in the two columns on the right indicate the NF based on the value of γ, the factor that related drain-current noise to that of a resistor with $R = g_m^{-1}$.

Chapter 4

Improving linearity of the Belostotski LNA

The design used up till now has been optimized for low noise, by using weak inversion The big advantages of doing so are; a) the lower theoretical value of the noise excess factor γ (theoretical value in weak inversion: $\gamma = 1/2$, in strong inversion: $\gamma = 2/3$) and b) the higher gain that can be realized due to higher g_m/I_d. Operating in this region also has disadvantages, two of those disadvantages are larger transistors needed for the same g_m, hence more chip size and parasitic capacitance, and worse non-linearity due to exponential instead of quadratic transconductance.

The plot in Figure 4.1 was made to get a better perspective of the maximum gain that can be achieved in the cascode stage (M1, M2 and RL) in the negative C LNA. In this figure we assume that transistors are operating as quadratic devices, hence the ratio between g_m and I_d is inversely proportional to the overdrive and size independent:

$$\begin{aligned} I_d &= \frac{1}{2} K \cdot V_{ov}^2 \\ g_m &= \frac{dI_d}{dV_{gs}} = K \cdot V_{ov} \\ g_m/I_d &= \frac{2}{V_{ov}} \end{aligned} \tag{4.1}$$

The minimal headroom needed for the cascode is equal to 2x the overdrive voltage V_{ov}, which yields the maximum value for load resistor R_{L1}:

$$R_{L1,max} = \frac{V_{dd} - 2V_{ov}}{I_{d1,2}}, \tag{4.2}$$

where $I_{d1,2}$ represents the bias current of M1 and M2. If V_{ov} is increased to yield better linearity and M1 and M2 are scaled to keep $I_{d1,2}$ constant, g_m decreases while R_{L1} has to decrease to account for extra needed headroom. The maximum gain can be expressed in terms of V_{dd} and V_{ov}:

$$R_{L1,max} \cdot g_{m1} = \frac{V_{dd} - 2V_{ov}}{I_{d1,2}} \frac{2}{V_{ov}} \cdot I_{d1,2} = \frac{2V_{dd}}{V_{ov}} - 4 \tag{4.3}$$

This equation yields zero gain if V_{ov} is set to $V_{dd}/2$, which is as expected since all of the supply voltage is needed for M1 and M2's headroom, in that situation. The dashed and dotted lines in Figure 4.1 show the voltage gain that can be achieved when extra voltage headroom is assigned to M1 and M2.

4.1 Design for comparable power consumption

For the designs in this section we will use the following constraints to allow for fair comparison of the specifications after simulation.

- $I_{ds1} = I_{ds2} \approx 8.8$ mA, the value used in the weak-inversion implementation.
- I_{ds3} is allowed to be slightly higher.
- S_{11} should still be lower than -10 dB.
- *NF* is allowed to increase, but should stay well below 3 dB[1].

[1] This is the limit in NF that noise-cancelling LNAs typically try to break.

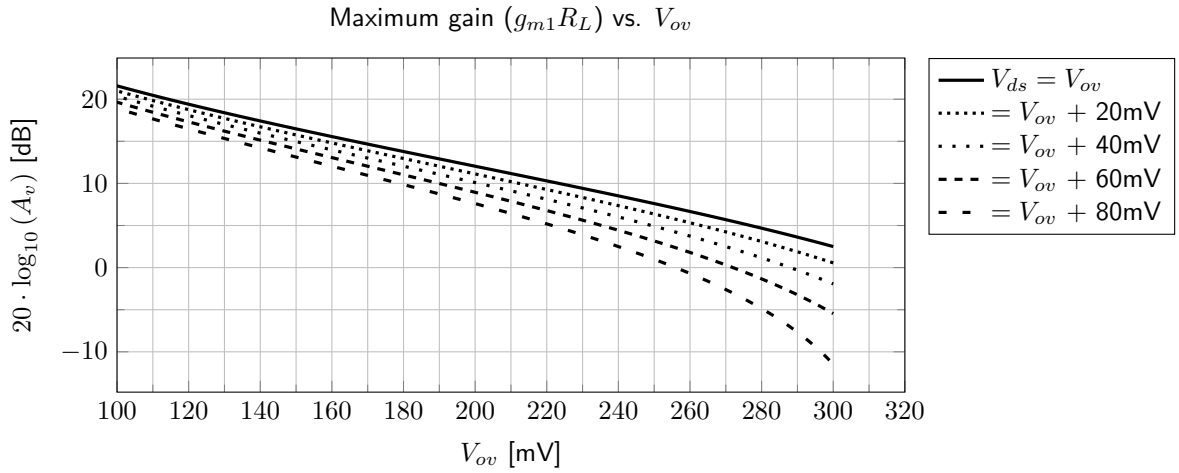


Figure 4.1: The maximum voltage gain from node IN to node OUT that can be achieved as function of overdrive voltage, assuming quadratic devices (saturation) and a resistive load (R_L). The gain limitation comes from the voltage headroom needed for the transistors ($\geq 2V_{ov}$). The headroom for M1 and M2 (V_{ds}) is swept to visualize the trade-off between headroom and gain.

Design with voltage applied to back-gate

The weak inversion implementation does not use the back-gate that is present in 22nm FDSOI. The back-gate terminal can be used to lower the threshold voltage of the MOSFET, simulations of a 1.5u/40n SLVTNFET shows that V_{TH} can be lowered by applying voltage to the back-gate at a rate of -80 mV/V.

The following procedure is followed while designing the LNA with varying amounts of V_b (back-gate voltage):

1. Scale M2/M3 for a bias current of 8.8 mA, yielding $I_{d1,2}$ and $g_{m1,2}$.
2. Allocate voltage headroom $V_{ds,HR}$ for V_{ds}, such that the transistors stay in saturation, we will choose $V_{ds,HR} = V_{ov} + 25$ mV, based on Figure 4.1.
3. Set R_{L1} for a voltage drop of $0.8 - 2 \cdot V_{ds,HR}$.
4. Scale M3 such that $(g_{m1}R_{L1} + 1) \cdot g_{m3} = 20$ mS.
5. Scale R_{bias} for 400mV of voltage drop (bias voltage for M1).
6. Scale R_{C1} for voltage drop of $0.4 - V_{ds}$.
7. Set $V_{bias,M2} = 0.4 + V_{ds,HR}$.
8. Set $V_{bias,M3} = V_{gs1} + V_{gs3} = 0.8$.

1V back-gate voltage

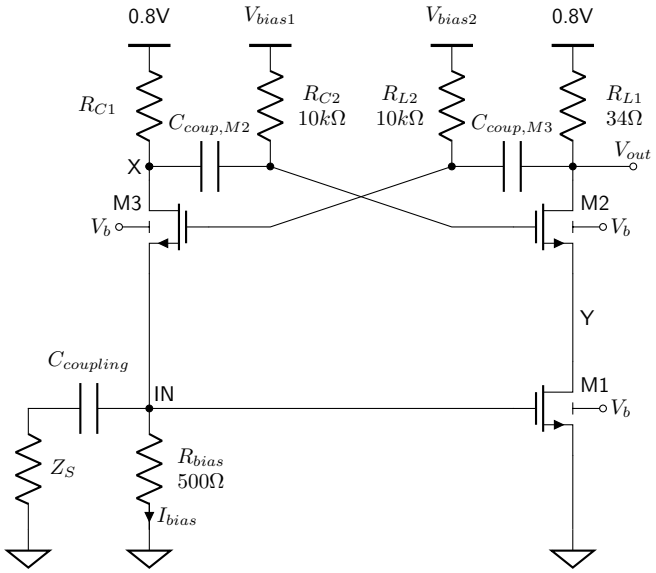
The design procedure in the previous section yields the design for 1V of back-bias in Figure 4.2, the calculations that led to this design are outlined in Appendix C.

There is one remaining degree of freedom, the value chosen for R_{C1}. Choosing low values for this resistor (e.g. 50 Ω) yields slightly lower gain, but better IIP3.

4.2 Designs with other back-gate voltages

For brevity I will only mention the values found, the steps that were taken are the same as in the previous section and Appendix C. The plots of the simulations are shown in Appendix B.

From Table 4.2 it is clear that the design based on hand calculations does not completely fit the supply current constraint. A second iteration of the LNA design was performed where $m_{1,2}$ was increased to come closer to 8.8 mA. The size of M3 and the bias resistor are kept constant.



Bias overview for $V_b = 1$				
Transistor	**Size**	I_d	g_m	V_{ov}
M1	66u/40n	8.8 mA	69 mS	225 mV
M2	66u/40n	8.8 mA	69 mS	225 mV
M3	6u/40n	800 uA	6.3 mS	225 mV

Figure 4.2: Design with $V_b = 1$.

Designs for different V_b				
V_b	**0**	**0.5**	**1.0**	[V]
$m_{1,2}$	106	65	44	[-]
	(140)	(78)	(49)	
$I_{d1,2}$	8.8	8.8	8.8	[mA]
$g_{m1,2}$	102.6	83.2	69.1	[mS]
	(135.5)	(99.8)	(77.0)	
m_3	3	3	4	[-]
I_{d3}	249	405	800	[μA]
g_{m3}	3.1	3.8	6.3	[mS]
R_{L1}	52	43	34	[Ω]
R_{C1}	$\leq$923	$\leq$469	$\leq$188	[Ω]
R_{bias}	1.6 k	988	500	[Ω]

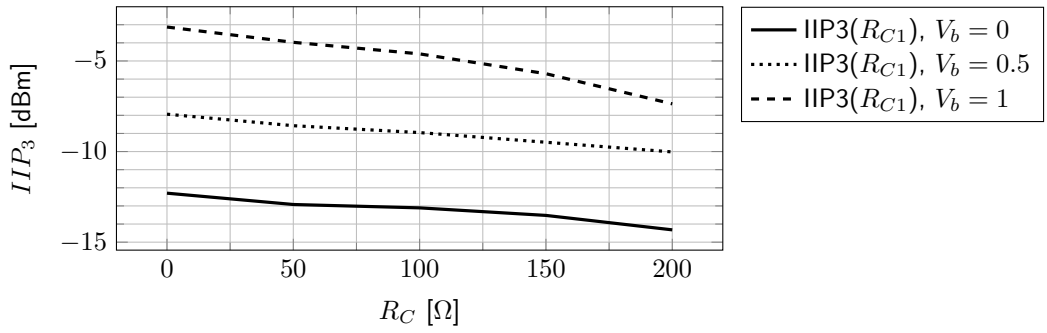
Table 4.1: Values used in the different designs, based on the procedure outlined in section 4.1. Note that a maximum value is given for R_{C1} where M3 stays in saturation, but at this value stability is not guaranteed. Post-optimization results shown in brackets.

4.3 NF-linearity trade-off

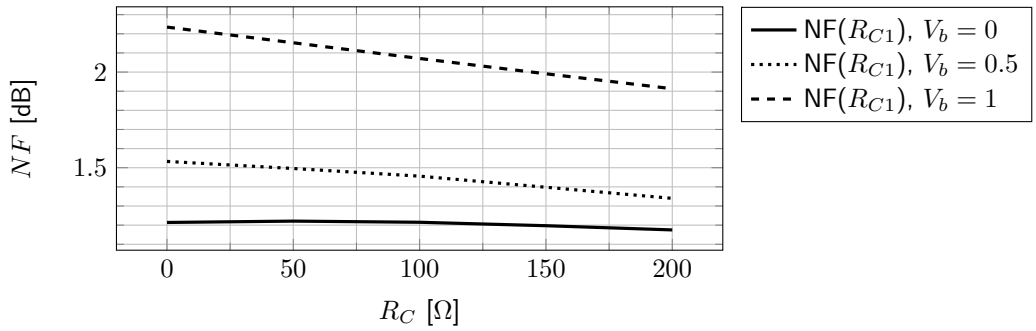
The simulation results of the three designs presented in the previous section are presented in Figure 4.3. The trade-off between linearity (IIP3) and noise figure

Simulation results				
V_b	**0**	**0.5**	**1.0**	[V]
S_{11}	-20.9...-11.9	-20.7...-14.7	-12.7...-11.1	[dB]
	(-18.2...-9.1)	(-33.4...-20.3)	(-20.9...-18.4)	
voltage gain	15.3...16.7	12.5...14.5	10.2...12.0	[dB]
	(15.9...17.7)	(13.2...14.9)	(9.4...11)	
NF	1.21...1.22	1.34...1.54	1.34...1.91	[dB]
	(1.07...1.14)	(1.31...1.48)	(1.85...2.19)	
NF_{min}	1.15...1.21	1.26...1.43	1.24...1.58	[dB]
	(1.00...1.07)	(1.28...1.44)	(1.78...2.06)	
IIP_3	-13.8...-12.6	-12.7...-11.1	-7.0...2.0	[dBm]
	(-16.4...-13.4)	(-11.4...-8.6)	(-8.1...-3.6)	
I_{supply}	6.3 (8.9)	7.3 (8.7)	7.9 (8.8)	[mA]

Table 4.2: Simulation results using the designs in Table 4.1, at 5.8 GHz. Post-optimization results shown in brackets.



(a) Nonlinearity versus R_C



(b) Noise figure versus R_C

Figure 4.3: Simulation results for the design in Figure 4.2 of (a) IIP3 as function of $R_C = R_{C1} \parallel R_{C2}$ and (b) the noise figure at 5.8 GHz. For IIP3 we used two tones (5.8 GHz and 5.9 GHz) and extrapolate between the tone at 5.8 GHz and the intermodulation product at 5.7 GHz. For NF we use the value at 5.8 GHz (in-band), NF is fairly flat ($\pm$0.05 dB) over frequency in 5 GHz - 6 GHz range.

Chapter 5

Conclusions

The noise transfer and the linearity of the active negative C LNA were presented and a sub-1.5dB noise figure LNA was designed in 22nm FDSOI. Simulations at different back-gate biases were performed to explore the trade-off between linearity and noise figure. The noise analysis showed that the low NF found in simulation is mainly due to the transfer functions associated to the nodes within the LNA and the manner in which the output is defined. The negative capacitance generated in by LNA helps in increasing the bandwidth by lowering the input capacitance which benefits near the edge of the bandwidth, but does not significantly lower the NF.

A trade-off between the magnitude of the negative capacitance and the frequency of operation was shown analytically and in simulation, if the magnitude of the negative capacitor is increased, the point where it switches to the behavior of an inductor will move to lower frequency.

In the comparison between a regular shunt-feedback LNA and the design proposed by Belostotski in Table 3.4, a small difference was found in NF when aiming primarily for low noise figure, with good linearity as a secondary goal. The regular shunt-feedback LNA was shown to be more linear than the Belostoski LNA, and removal of the coupling capacitor (yielding regular shunt-feedback) also removed a possible source of instability.

The biggest disadvantages of the topology proposed by Belostotski is the need for a second stage to get a balanced differential output, which is a big advantage of the BALUN LNA and the fact that voltage swing is needed at the output to achieve g_m-boosting, the latter limits the linearity of the LNA.

In this research, the focus was mainly on the core LNA, hence the biasing sources were assumed to be, and implemented as, ideal (noiseless) voltage sources (the noise figures and factors presented are only valid when the bias circuitry adds little extra noise).

The Belostotski LNA appears to be aimed at achieving noise match when it is power matched (connected to a 50-ohm source), which makes it only slightly different from noise-cancelling LNAs like the BALUN LNA, where (to the authors knowledge) compensation of the input capacitance through negative capacitance to boost bandwidth is generally not consciously applied.

One of the research questions was related to applying the concept of negative capacitance in other LNAs. Analysis on a CG-stage with a resistor connected to the gate terminal was shown to generate negative capacitance. However, this resistor produces noise, minimizing this resistor produced the best NF. This shows a design challenge for negative capacitance in LNAs; adding components to generate negative capacitance to achieve noise match is only useful if these components add little noise.

Chapter 6

Recommendations

The following recommendations can be made for further research:

- The amount of negative capacitance can be increased by adding an extra capacitor between the gate and source of M2, in this research there was no focus on finding the ideal value analytically. By optimizing the magnitude of the negative capacitor, the bandwidth of the circuit may be increased a little (the -C shifts the R-C input pole to higher frequencies).
- The analysis and design are based on biasing using ideal voltage sources, in realistic implementations this could be done by implementing current mirrors as current sources (Belostotski indicates using this technique [2]). If the LNA is implemented, proper scaling should be used to prevent significantly increasing the noise figure.
- The second stage should also be implemented to get a real balanced output, the output used in simulation was not truly differential, the voltage swing the IN and OUT node are out of phase, but have unequal amplitude.

Appendix A

Noise figure for correlated sources

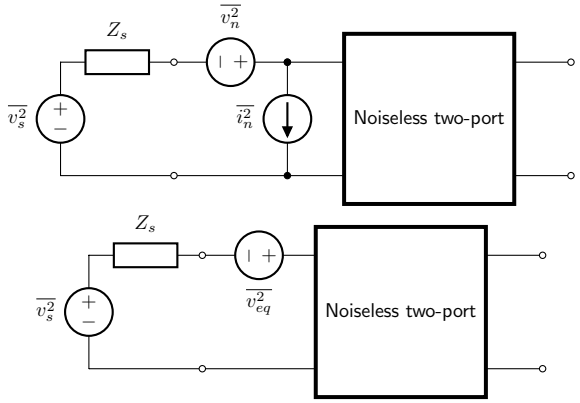


Figure A.1: Noise representations of two-ports.

The following is based on Section 11.6 in [4]: We begin by representing the noise by a current and voltage noise source:

$$v_{eq} = v_n + i_n Z_s \tag{A.1}$$

We then rewrite the noise current as the sum of an uncorrelated (i_u) and a correlated (i_c) noise:

$$v_{eq} = v_n + (i_c + i_u)\, Z_s \tag{A.2}$$

The correlated noise current can be rewritten as the product of the noise voltage and a correlation admittance ($Y_c = G_c + jB_c$):

$$v_{eq} = v_n \cdot (1 + Y_c Z_s) + i_u Z_s. \tag{A.3}$$

Because the first and second term are uncorrelated, the sum of the variances becomes:

$$\overline{v_{eq}^2} = \overline{v_n^2} \cdot |1 + Y_c Z_s|^2 + \overline{i_u^2} \cdot |Z_c|^2 \tag{A.4}$$

The noise factor now becomes:

$$F = \frac{\overline{v_{eq}^2} + \overline{v_s^2}}{\overline{v_s^2}} = 1 + \frac{\overline{v_n^2} \cdot |1 + Y_C Z_S|^2 + \overline{i_u^2} \cdot |Z_S|^2}{\overline{v_s^2}} \tag{A.5}$$

By substituting $\overline{v_n^2} = 4kTBR_n$, $\overline{i_u^2} = 4kTBG_u$ and $\overline{v_s^2} = 4kTBR_s$:

$$F = 1 + \frac{R_n \cdot |1 + Y_C Z_S|^2 + G_u \cdot |Z_S|^2}{R_s} \tag{A.6}$$

Solving to minimize F, we find the following values for $Y_s = Y_{opt} = G_{opt} + jB_{opt}$:

$$B_{opt} = B_s = -B_c,$$
$$G_{opt} = G_s = \sqrt{\frac{G_u}{R_n} + G_c^2},$$

yielding

$$F_{min} = 1 + 2R_n \cdot \left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c \right]^2 , \tag{A.7}$$

with

$$F = F_{min} + \frac{R_n}{G_s} \left| Y_s - Y_{opt} \right|^2 \tag{A.8}$$

Appendix B

Simulation results of the final designs

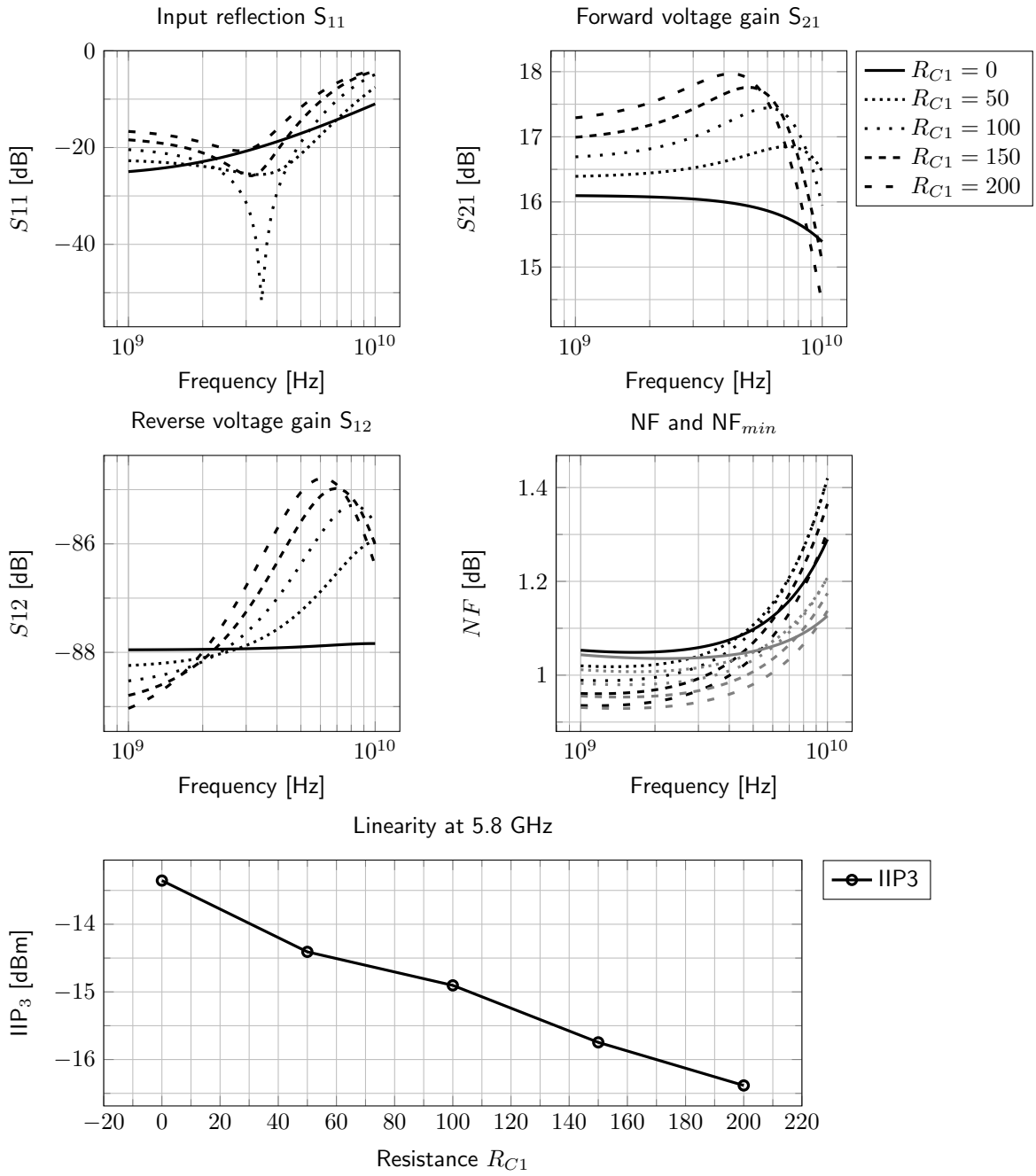


Figure B.1: Simulation results for $V_b = 0$. The simulation are generated in Cadence using a 50 ohm input source and a 1 mega-ohm port between IN and OUT, using the circuit in Figure 4.2 with component values from Table 4.1. The IIP3 is simulated by applying two tones to the input (5.8 GHz and 5.9 GHz) and extrapolating between the output tones at 5.7 GHz (intermodulation product) and 5.8 GHz.

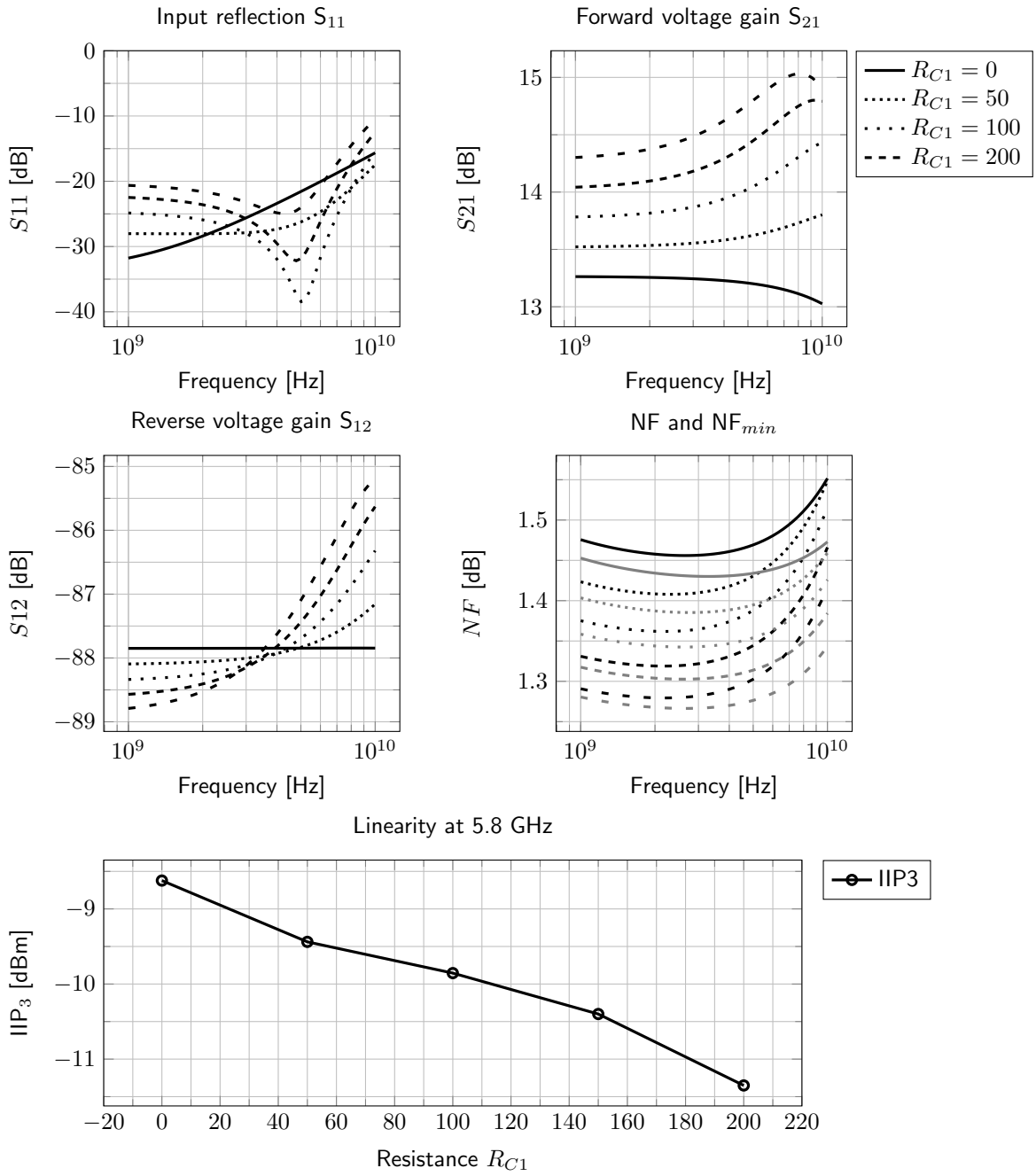


Figure B.2: Simulation results for $V_b = 0.5$. The simulation are generated in Cadence using a 50 ohm input source and a 1 mega-ohm port between IN and OUT, using the circuit in Figure 4.2 with component values from Table 4.1. The IIP3 is simulated by applying two tones to the input (5.8 GHz and 5.9 GHz) and extrapolating between the output tones at 5.7 GHz (intermodulation product) and 5.8 GHz.

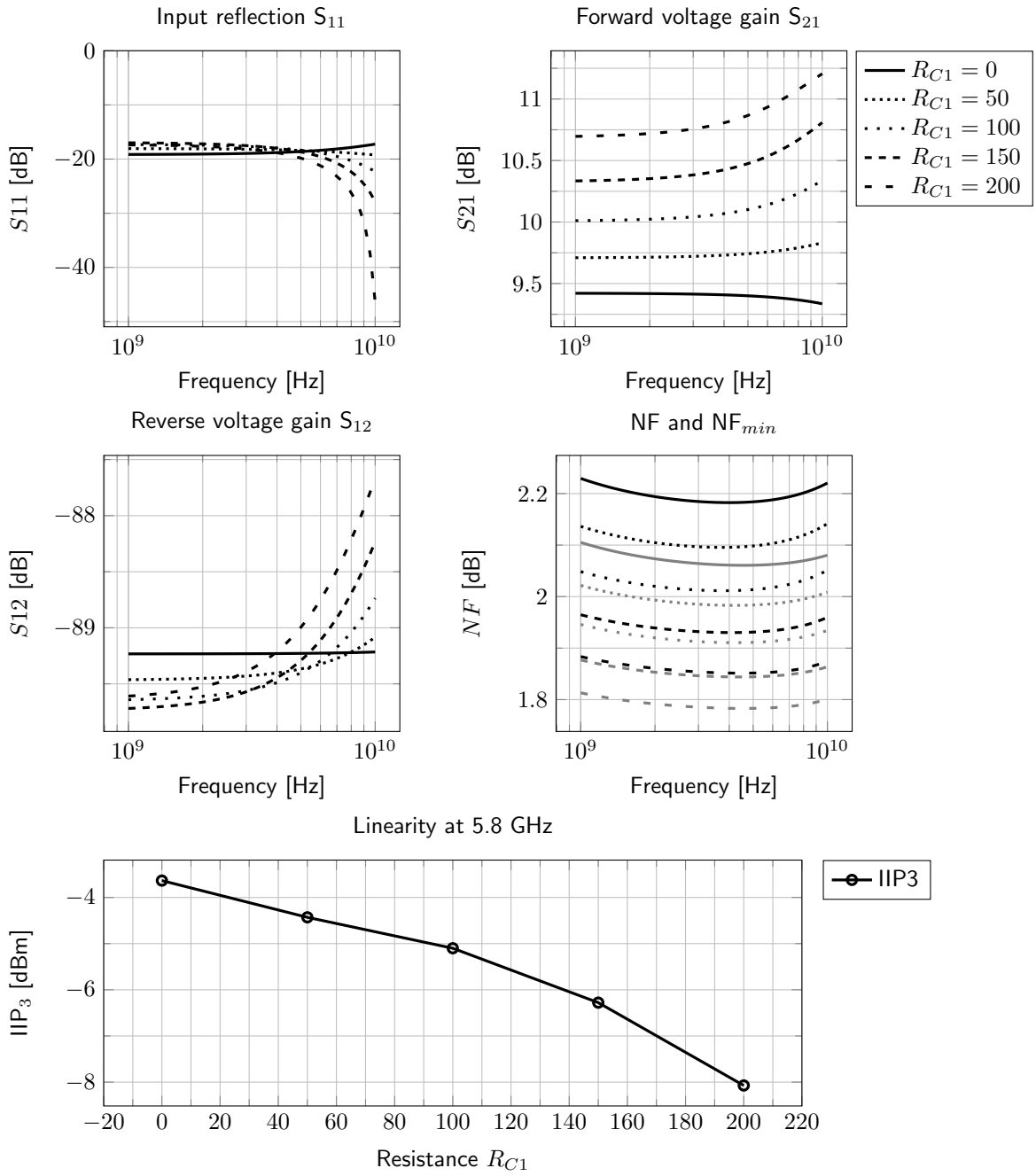


Figure B.3: Simulation results for $V_b = 1$. The simulation are generated in Cadence using a 50 ohm input source and a 1 mega-ohm port between IN and OUT, using the circuit in Figure 4.2 with component values from Table 4.1. The IIP3 is simulated by applying two tones to the input (5.8 GHz and 5.9 GHz) and extrapolating between the output tones at 5.7 GHz (intermodulation product) and 5.8 GHz.

Appendix C

Designing for 1V back-gate bias

The value of V_{TH} at zero V_b is approximately 255 mV. By applying 1V at the backgate, the threshold decreases to a value of 175 mV, yielding:

$$V_{ov} = V_{gs} - (V_{TH}(V_b)) = 0.4 - 0.175 = 225 \times 10^{-3} \text{ [V]}$$

This overdrive yields the following g_m and I_d for a single 1.5u/40n SLVT transistor

$$I_d = 200 \text{ [}\mu\text{A]}$$
$$g_m = 1.57 \text{ [mS]}$$

This yields a multiplier, I_d and g_m:

$$m_{1,2} = \frac{8.8 \times 10^{-3}}{200 \times 10^{-6}} = 44 \text{ [-]}$$
$$I_d = 44 \cdot 200 \times 10^{-6} = 8.8 \times 10^{-3} \text{ [mA]}$$
$$g_{m1,2} = 44 \cdot 1.57 \cdot 1.57 \times 10^{-3} = 69 \text{ [mS]}$$

The minimum V_{ds} is 400 mV - 175 mV = 225 mV, to ensure saturation operation we allocate 250 mV for the drain-source voltage. From here we determine the appropriate value of R_{L1}:

$$V_{R_{L1,bias}} = 0.8 - 2V_{ds,HR} = 0.3 \text{ [V]}$$
$$R_{L1} = \frac{V_{R_{L1,bias}}}{I_d} = 34 \text{ [}\Omega\text{]}$$

The gain from IN to OUT is given by:

$$A_v = -g_{m1}R_{L1} = -2.3$$

This inverting voltage gain means that we need a certain amount of transconductance for M3 and hence get a certain I_d and needed R_{bias}:

$$g_{m3} = \frac{20 \times 10^{-3}}{(1 - A_v)} = 6 \text{ [mS]}$$
$$m_3 = \frac{g_{m3}}{1.57 \times 10^{-3}} = 3.82 \approx 4$$
$$I_{d3} = 4 \cdot 200 \times 10^{-6} = 0.80 \text{ [mA]}$$
$$R_{bias,needed} = \frac{V_{gs}}{I_{d3}} = 500 \text{ [}\Omega\text{]}$$

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