Darwin on a chip: Think Outside of Logic

Master's Thesis Nanotechnology

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Abstract

Current developments in the computing hardware are limited by the operating principles of CMOS technology: fabrication limits of sub-nanometer features and difficulties in the utilisation of the interconnects between chips. This set of obstacles has sparked a search for an alternative computing system. One of them is a computing approach utilising the material system. It was found that by using the physical property of the material itself, the computing method becomes more energy efficient[1]. This has been implemented in a nanoscale system based on a disordered system such as gold nanoparticles[2] or lowly doped silicons[3]. In this thesis, we attempt in evolving the lowly doped silicon chip using the interconnectivity between the chips. We first show the progress on how these experimental setups are developed with the chips, hardware, and the software interface. The experiments are done at the liquid nitrogen temperature using eight lowly doped silicon chips. The rudimental results show that interconnectivity may not be powerful enough to straightforwardly utilize in the genetic algorithm. As such, some suggestions are proposed in the end to further develop and investigate this multi-device system which can, with more optimisation, lead to a scaled-up functionality with the lowly doped silicon chips.

Acknowledgement

As much as my thanks go to every individual who I have been in touch with for the last two years, few groups of people who had helped me with this far into master's thesis deserve special mention and gratitude. The first thanks go to my daily supervisor *Tao* who, from the complex discussion about the solid-state physics to the difference in Japanese and Chinese letters, has offered me a lot of great talks that were sometimes necessary for both academic as well as entertainment. And all the help in fabrication of the nanodevice is worth the thousands of thanks, as they were most vital in my thesis work.

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The theory discussions were also sometimes the solution to the obstacles. For this aspect, I am thankful to the former NE member *Celestine* as well as my previous external member *Hajo*. They have been a great encourager for the switch experiments and many dicussions were very helpful to my progress. And in this regard, I would like to thank my new external member *Bernard* for substituting the external member position. It is not wrong to say I could have not completed my thesis before September if he has not answered my urgent request to be available for my defence.

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And of course my family in Japan.
遠く離れていても見守ってくれていた事、感謝しています。
この2年間の何よりの励みでした。
平成３０年８月　堀　廉太郎　　Ren Hori, Enschede, August 2018

Contents

1 Introduction

The development of the von Neumann architecture, broadly used in the digital systems, are now facing significant challenges for data-intensive tasks. While many companies in the transistor industry are focusing on further reduction in the transistor size[4], alternative approaches based on neuromorphic computing and machine learning have also been extensively studied[5]. Spearheaded by IBM's TrueNorth project, the spiking-neuron integrated circuit with a scalable communication network and interface [6], the neuromorphic computing had become one of the frontline research fields which challenges how closely the humanity can create CMOS devices that "can think", or behave like a human brain. The thesis project will be based on the doped silicon devices [3] that have some promising features to perform such unconventional functionalities that are more close to the human brain than the von Neumann architecture. The dopant device, under low temperature, can show non-linear IV relations that are inherent to the material. This can be exploited to find a solution to the problem such as boolean logic[2] or potentially even more complicated tasks, hence act as a neuromorphic computing chip. However, a few challenges must be addressed before confirming the chip's capability.

The first is the optimisation of the fabrication procedure. The early version of the chip recipe involved many steps that were hindering the production regarding the yield and reproducibility. Without being able to make the chips reliably, the results can not escape the criticism of the luck being involved in the fabrication process. Moreover, doing any type of experiment will come with a risk of destroying the chip, or contribute to the potential degradation of the chip; thus being able to mass produce the individual devices is a crucial goal that must be met before testing its functionalities.

The second challenge is to find a functionality other than the boolean logic gate. Tracing back to the original designless chip idea by Bose et al.[2], finding six boolean logic gate using two-input one-output schematic become very well established and is a finalised functionality. It is now the utmost interest for this chip to be able to do something other than what few sets of transistors can do, to present itself as a neuromorphic computing system.

This report will show its progress in the fabrication aspect of the dopant devices as well as the potential scaled up functionalities that can be achieved via modulating the interconnectivity between the devices. The report will first go over the theoretical aspect behind the application of this dopant devices in the dedicated computing concept called Evolution-in-Materio. After this, the device fabrication procedure, as well as the experimental setup, are described. Following the experimental description, the results obtained from each setups are shown. This results section are divided into two categories, single device and multi-device characterisations. Single device results will discuss the yield and reproducibility of the dopant devices from the new recipe, as well as well established boolean logic results for both dopant system. Multi-device system will cover a result obtained from the new experimental procedure called Darwin Internet. This setup can tune the connection in-between the devices, thus unique input-output behaviour can be recorded by altering the current path between the devices. Since multiple devices can be incorporated in the experiment, the number of allowed input and output scales also, thus further functionality such classification can be attempted. The goal of the thesis is to develop this new experimental system and provide more brain-like behaviour to the dopant chip, thus it can finally "think outside of logic".

2 Theory

2.1 Dopant Conduction

Analyzing the electric conduction in the material is almost inseparable from understanding the band gap of a material. Band gap is an energy range in the solid where no electronic states can exist, thus an electrical property of the material depends heavily on the size or the purity of this band gap. Three principle materials (insulator, semiconductor, and metal) have unique irreplaceable bandgap properties that many electronic systems utilize for their operations. Insulators have significantly large bandgap to prevent electric conduction under the room condition, while the metals have much smaller or non-existent band gap, allowing rapid carrier conduction with ease.

But perhaps the most interesting of all is the semicondutors as their bandgap can be controlled through the material composition. A foreign atom can be artificially introduced into the semiconductor through the means of “doping”. This creates new energy levels within the semiconductor band gap, thus the charge carriers gain a new environment to arrive at their respective (Valence band for holes and Conduction band for electrons) bands. This dopant assisted band conduction is a basis of electrical conduction of semiconductors under a normal condition. In sufficiently low temperature, the transport occur between these dopant sites as a consequence of reduced thermal energy. Within this low temperature regime, transport physics can be further distinguished depending on the density of the impurity sites, as well as the temperature.

This chapter will discuss the electronic property of shallow impurities in the semiconductor at low temperature. Impurity density also determines the conduction mechanism and when it is below the critical concentration, transport is determined by hopping between two impurity sites. Such hopping property also has a slight variance when the temperature is even further reduced. This distinction is broadly covered and then summarized in the end as a temperature dependent conduction mechanism of the lowly doped semiconductor system.

2.1.1 Isolated Impurity States

There are two types of impurity or dopant in the semiconductor system, donor or acceptor, and they have different contribution to the electronic property of the semiconductor. Their energy levels are shown in the figure 1. Donor energy level is in energy vicinity to the conduction band,

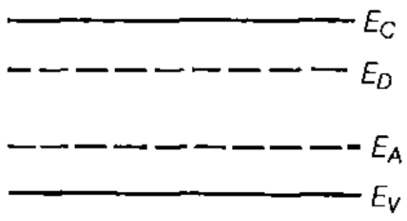


Figure 1: Semiconductor band diagram consisting of conduction band(E_C), valence band(E_V), and the energy levels of the donor and acceptors ($E_{D,A}$)[7]

donors can therefore easily be ionized by "donating" an electron to the conduction band and take part in the electron transport of the semiconductor. In a specific situation where the donor energy level is in close proximity to the conduction band minimum, an excess electron is weakly bound to the donor center. This implies that the atomic structure of the impurity center has a minor effect on the state of the excess electron because its correlation to the center is mostly due to the positive charge at the center. This type of donor is known as a shallow donor due to its "shallow" energy level compared to the conduction band (in contrast to deep energy band) and the impurity center

can be regarded as a point charge and the central potential for the electron motion becomes:

$$U(r) = \frac{e^2}{\kappa r}$$

Where e is an electron charge, r is the distance to the charge center and κ is a dielectric permittivity of a lattice. For the sake of simplifying the theory, the following will treat electrons as a charge carrier and donor level as an impurity band.

The energy required to move electron from the donor level to the conduction band level is called an ionisation energy. Under the room temperature, the thermal energy that the dopants acquire is larger than the ionisation energy, thus the free charge carriers are created in the respective bands, which results in the shifting of the band[8]. At sufficiently low temperature, the electrons are captured by the other donors rather than the conduction bands. This temperature is known as the freeze-out temperature, and the degree of localization of the impurities are critical in theorizing the conduction phenomenon below this temperature. Thus the conductivity of a doped semiconductor in this regime is determined by the impurity states. The wave function of isolated impurity can be approximated as a hydrogen-like wave function with much larger radius, effective Bohr radius a_B, that determines the characteristic dimensions of the wave function.

$$a_B = \frac{\hbar^2 \kappa}{m^* e^2}$$

The interaction between the impurity states can thus be approximated from the overlap between these wave functions, so the electron transfer energy varies exponentially with the distance between two sites. As such, one of the key parameter in the disordered doped semiconductor is the density or concentration of the impurities. Increasing the impurity concentration leads to an exponential increase in the transfer energy between the impurity sites. Thus, there is a critical impurity density above which states are extended and below which states are localized. This impurity density dependent metal-nonmetal behaviour change is known as the Mott transition [9], and the density at which the phase transition occurs is called the Mott concentration. When the states are extended (above Mott concentration), impurity states overlap and the impurity bands are formed, giving the system a metal behaviour (i.e. a finite conduction at T = 0K) In contrast, conduction is defined by hopping from occupied to unoccupied localized impurity state when the concentration is below the Mott concentration. This density and temperature dependent behaviour is intuitively illustrated in figure 2 a) and b).

2.1.2 Hopping Transport

The electron transport in the doped semiconductor is governed by the hopping transition from an occupied impurity states to a free impurity states[10]. In this system, it is assumed that the all the states have a different energy level (i.e. two states with an equal energy have an infinite distance). Hence when the electron hopping occurs, the process is accompanied by a phonon interaction to compensate for the energy difference. The probability of transition between the site i and j can be formulated as:

$$\frac{1}{t_{ij}} \equiv F(\psi_{ij}, f_i, f_j) \left| \int \psi_j^* e^{iqr} \psi_i d^3 r_{ij} \right|^2$$

The exponential factor e^{iqr} in the integral is the phonon wavefunction, r is the distance between site i and j, and ψ is the electronic wavefunction at the site i and j. The density of the disorder sites are assumed low enough that they are localized, but a finite probability of electron transition between two centers are assured due to the exponential tails of the wavefunction which guarantees the certain degree of an overlap. d is the integer number representing the dimensionality of the system. This energy compensation indicates that the electrons at each impurity site will see

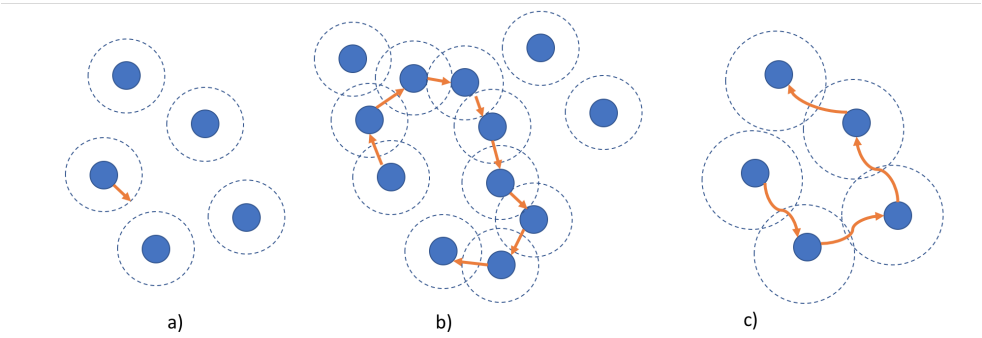


Figure 2: Illustration of electrical conduction dependency on the impurity site (blue dot) density as well as the temperature. a)When the density of the states are below Mott concentration, the system has an insulator property so the charge transfer between the impurity sites(marked by an orange arrow) is hindered. b) If the states are above the Mott concentration, the system has a metallic property, so even at the low temperature(i.e. smaller effective wave function), there's a significant overlap in the wave function(represented by the dashed circle) that there can be a charge transfer. c) However, even in the insulating regime, the system temperature can be increased to effectively create a finite wave function overlap such that they can have a charge transfer. This has pre-requisite that the ionisation energy of the impurity sites to the system should not be overcome.

an energy barrier to hop to an another site. Each pair of impurity centers can be regarded with a fictitious resistance R_{ij}, which is inversely proportional to the transition probability:

$$R_{ij} = R_0 exp^{u_{ij}}$$

$$u_{ij} = \frac{2r_{ij}}{a_B} + \frac{\varepsilon_{ij}}{T}$$

With ε_{ij} representing a characteristic energy difference between site i and j, and T is the temperature. When the impurity density increases, they can be mapped as a scattered charge islands that are interconnected by the resistors. This approximation of the disordered system as the impurity network with a interconnecting resistors was originally proposed by Miller and Abraham[11] and schematically shown in figure 3.

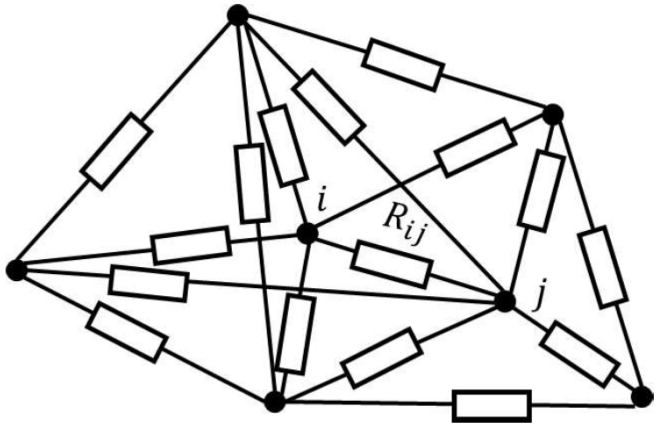


Figure 3: Illustration of resistor network originally suggested by Miller and Abraham[11]. Dots represents the charge island and they are connected by effective resistance R_{ij} from site j to i.

2.1.3 Nearest Neighbour Hopping

The most straightforward hopping activity is one which occurs between the vicinity impurity sites. The maximum of the density of states in the donorband are located at the energy value in the order of the ionisation energy of the isolated dopant which will be referred as E_0. If the hopping distance is so low that the initial and final point, i and j, are the nearest neighbours, energy level of these sites are most likely near the maximum density of states. Hopping event relies on the final point to be free, and the probability that it is free depends on its energy with respect to the fermi level μ as well as the system temperature, and is proportional to:

$$exp\left(\frac{-|\mu - E_0|}{T}\right)$$

Under such scenario, the energy difference between the initial and final site, $\delta_{ij} = |\varepsilon_i - \varepsilon_j|$, is smaller than the distance between the fermi level and the donor level, $|\mu - E_0|$. Thus when the above factor enters all the u_{ij}, its contribution to the scattering vanishes out. This allows such variables to be factored out in the net property analysis:

$$R_{ij} = R_0 exp^{(2r_{ij}/a_B)} r_{ij}$$

The closer the two sites, the lower the resistance between these two sites, thus higher chance of hopping.

2.1.4 Mott Variable Range Hopping

The presumption in realizing the nearest neighbour hopping is the existance of the large number of close neighbour pairs with one of the sites being free. When the system temperature is decreased such that:

$$k_B T << |\mu - E_0|$$

nearest neighbour hopping freezes out because the number of energy sites among the nearest neighbours(which majority is at the E_0) becomes too small. In such case, hopping to the sites located far away but is in energy vicinity can be more favorable than hopping to the nearest neighbour with higher energy gap. Density of states near the μ, in the range of $\mu \pm \varepsilon$, is treated constant ($g = g_\mu$) as an initial assumption. Number of states in within this range and their average distance are thus:

$$N(\varepsilon) = g_\mu \varepsilon$$

$$r_{ij} = N(\varepsilon)^{-1/3}$$

Abraham-Miller network now only connects the sites with the energy range of $g_\mu \pm \varepsilon$. u_{ij} now equals:

$$u_{ij} = \frac{2}{a_B[N(\varepsilon)]^{1/3}} + \frac{\varepsilon}{T} = \frac{2}{g_\mu^{1/3} a_B \varepsilon^{1/3}} + \frac{\varepsilon}{T}$$

The above equation still depends on the unknown ε. To determine from the condition that u_{ij} is minimum:

$$\frac{du_{ij}}{d\varepsilon} = 0, \varepsilon_{min} = \left(\frac{2T}{3g_\mu^{1/3} a_B}\right)^{3/4} = (T^3 T_M)^{1/4}$$

$$T_M \approx (g_\mu a_B^3)^{-1} > T$$

And the average hopping length is:

$$r \approx \left(\frac{a_B}{g_\mu T}\right)^{1/4} \approx a_B \left(\frac{T_M}{T}\right)^{1/4}$$

The power of 1/4 is appropriate for a three dimensional insulator. For a thin insulating film, the parameters change as:

$$r_{ij} \approx [N(\varepsilon)]^{-1/2}$$

$$u_{ij} = \frac{2}{g_\mu^{1/2} a_B \varepsilon^{1/2}} + \frac{\varepsilon}{T}$$

$$\varepsilon_{min} = \left(\frac{T}{g_\mu^{1/2} a_B}\right)^{2/3} = (T^2 T_M)^{1/3}$$

$$T_M \approx (g_\mu a_B^2)^{-1}$$

which means the average hopping length and the resistance are characterized as:

$$r \approx \left(\frac{a_B}{g_\mu T}\right)^{1/3} \approx a_B \left(\frac{T_M}{T}\right)^{1/3}$$

$$R(T) = R_0 exp\left(\frac{T_M}{T}\right)^{1/3}$$

The average hopping length as well as the resistance depends on the temperature, thus this phenomena is named variable range hopping(VRH). This characteristic resistance in particular is known as Mott Variable Range Hopping.

2.1.5 The Efros–Shklovskii Variable Range Hopping

Mott's law of variable range hopping assumed the constant density of state g near μ. When an electron-electron interactions are considered, the situation becomes different in that density of state becomes energy dependent:

$$g(\varepsilon) \propto \left(\frac{\kappa}{e^2}\right)^d |\varepsilon|^{d-1}, g(0) = 0$$

Now the number of states in the vicinity of fermi level depends on the dimension d, thus:

$$N(\varepsilon) \propto \left(\frac{\kappa\varepsilon}{e^2}\right)^d$$

The average distance between two sites are unaffected by the system dimension:

$$r_{ij} \approx [N(\varepsilon)]^{-1/2} \approx \left(\frac{e^2}{\kappa\varepsilon}\right)$$

u_{ij} can now be calculated using similar analogy to Mott Variable Range Hopping theory:

$$u_{ij} = \frac{2}{a_B [N(\varepsilon)]^{1/2}} + \frac{\varepsilon}{T} = \frac{2e^2}{a_B \kappa \varepsilon} + \frac{\varepsilon}{T}$$

$$\varepsilon_{min} = (T T_{ES})^{1/2}$$

$$T_{ES} \approx \frac{e^2}{\kappa a_B}$$

Average hopping length and the resistance are recalculated as:

$$r \approx \left(\frac{e^2 a_B}{\kappa T}\right)^{1/2} \approx a_B \left(\frac{T_{ES}}{T}\right)^{1/2}$$

$$R(T) = R_0 exp\left(\frac{T_{ES}}{T}\right)^{1/2}$$

This new resistance with electron interactions in consideration are called Efros-Shklovskii variable range hopping, owing to the physisists who first theorizezd this phenomena.

2.1.6 Temperature Dependent Conduction

Hopping transport is a characteristic conduction mechanism of lowly doped semiconductor at low temperature. This chapter was dedicated to further categorizing the hopping transport in different range of temperatures. At higher temperature regime, the carrier wavefunctions are delocalized such that the conductivity is of function:

$$\sigma(T) = \sigma_0 exp\left(-\frac{E_0}{k_B T}\right)$$

If the available phonon energy is comparable to the width of the impurity band, transport is characterized by the nearest neighbour hopping:

$$\sigma(T) = \sigma_0 exp\left(-\frac{\varepsilon}{k_B T}\right)$$

When the temperature is further reduced that only the states near the fermi level participate in the conduction, system enters variable range hopping regime:

$$\sigma(T) = \sigma_0 exp\left(-\frac{T_M}{T}\right)^{1/(d+1)}$$

with d representing the system dimension. Temperature sufficiently low enough that elecron-electron interactions are considered:

$$\sigma(T) = \sigma_0 exp\left(-\frac{T_{ES}}{T}\right)^{1/2}$$

Figure 4 shows the sequence of change in the conduction mechanism with a decrease in temperature. It is worth noting that this variant of hopping conductivity depends not only on the temperature, but the material system also[12, 13].

2.1.7 Coulomb Gap

Up until chapter 2.1.6, the energy band formed by the impurities are regarded as one block of a band where the states are populated with occupied or unoccupied sites. The density of states are expected to have a bell-shape with maximum near the E_0 and g_μ lying somewhere within the distribution. The study on the interaction between a localized electron and its nearest neighbours suggested that the density of states must collapse to zero, have a minimum, near the fermi level[14]. As such, impurity band density of states at low temperature does not have a smooth bell-shaped distribution, but rather two peaks separated by the gap located near the fermi level. The argument for this band separation is as follows: defining the energy E_i as the energy of an electron at site i which takes in account of the system disorder and the coulomb interaction with surrounding electrons, energy necessary to move an electrom from an occupied site i to unoccupied site j can be regarded as:

$$\Delta E = E_j - E_i - \frac{e^2}{r_{ij}}$$

With all the sites in the energy above μ are empty and below are full. Assuming the single particle density of state at this level, g_μ is finite and the system is in the ground state, every transfer of electron from occupied to unoccupied sites should involve positive energy (i.e. $\Delta E \geq 0$). Number of sites within the vicinity of fermi level $[\mu-\varepsilon, \mu+\varepsilon]$ is N, and the half of these would be occuped, as well as unccoupied. The distance between the two neighbouring sites in the randomly distributed disorder network is of order: $r \sim (N/V)^{-1/d}$ Substituting for N, the ΔE condition is updated as:

$$E_j - E_i - Ce^2(\varepsilon g_\mu / V)^{1/d} > 0$$

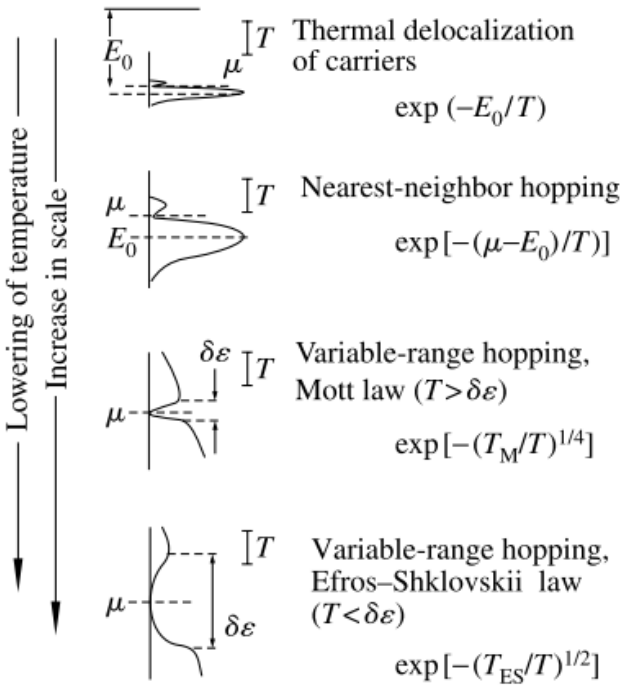


Figure 4: Summary of temperature dependent conduction of doped semiconductor. The density of the states at each regime are located.[8]

where C is a coefficient of order unity. Because of how the energy interval is defined, for small ε, the inequality expression will be violated, indicating that the system is energetically favorable to have zero density of state near the fermi level. This density of state gap is known as Coulomb gap, name owing to the interaction that result in this phenomena. The coulomb gap can also be shown experimentally[15] via tunneling experiment. The linear gap in a two dimensional single particle density of state provides non linear current-voltage behaviour of the system.

2.2 Evolutionary Computation

Evolutionary computation is a class of algorithm for global optimization inspired from a biological evolution. Just as how a set of species change their physical properties to adapt better to the environment over the generations, evolutionary computation utilizes set of solutions, alter them, and make them closer to the global solution. This chapter will begin with the notion of the evolution followed by genetic algorithm in terms of computer science concept. This computation can be realized in the material system rather than in the software platform. Such concept known as Evolution in Materio is later theorized to ensure the reader is aware of the conceptual notion behind this thesis.

2.2.1 Natural Evolution

On explaining the concept of evolution, the giraffe's long neck is a seemingly straightforward example. Its characteristic elongated neck have been observed as an advantageous traits because it allows the giraffs to obtain food beyond the reach of other hoofed animals. This benefit under a certain environmental conditions give higher chance of survival, reproduction, and thus leaving these traits to the offsprings. When intercrossed, these offsprings either inherit the same peculiarities, or have tendency to vary again in the same manner; while the individuals that do not undergo these process are more liable to perish[16]. In the case of the giraffes, evolutionary

pressure gives advantage to the more adapted ones by being able to out-compete others i.e. the unadapted, short-necked individuals gets weeded out and the best-adapted, long-necked ones survive. These variations become dominant in the species as it continues so it evolves. This elementary example is, of course, highly speculative theory, and the idea that longer neck gave benefit in searching for the food has become a target of many criticisms[17, 18]. However, the main concept remains across most of the giraffe argument; the evolution process takes place over the generations and the new individuals are implicitly selected based on their fit to the environment. This natural process forms the basis for the development of evolutionary, or genetic algorithms.

2.2.2 Genetic Algorithm

Genetic algorithm adapt some or all of the principles for solving search and optimization problems. The basic process of genetic algorithm is illustrated in figure 6. A population of coded answers to a problem is randomly generated. The member of this population is ranked by a fitness function, and selections are made depending on their fitness scores. Some members of this population may be mutated, or recombined by shuffling their information content with the other member of the population. Mutation allows a randomly timed sampling of an even better result, and recombination allows implicit testing of combination of the the population members. As process recurs multiple times, the survival of the fittest principle drives the population to better average fitness scores, thus more optimal solution.

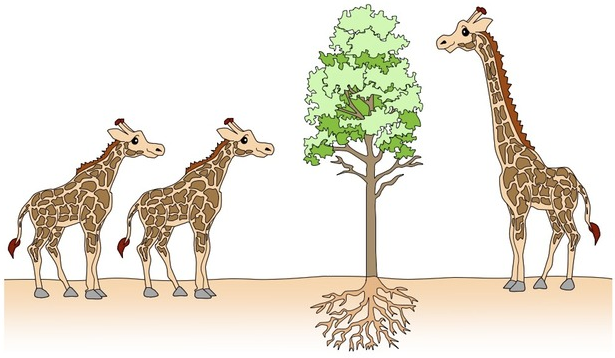


Figure 5: Conceptual image of natural evoltuion. Given species include both short and long necked giraffes, but the long necked one has higher chance providing offsprings due to its food advantage. Image taken from [19]

2.2.3 Evolution in Materio

Evolution in materio(EIM) is a methodology for exploiting the physical material system to perform the computation. It manipulates the physical system by computer controlled evolution process[20]. Through the application of physical signals, various intrinsic property of a material can be configured so that an effective computational function can be obtained. This process is centered by an idea that the application of these signals can alter the way the system responds to the physical input signals, therefore the generated output signal is a convoluted mixture of unique input and control signals. The desired output is always defined for the EIM process. The starting input of the evolutionary process may provide an output that is far from the desired ones. This physical output is converted to an output data, and a numerical fitness value is calculated based on how well the physical response corresponds to the desired response. The process repeats with adding small variation to the control signal to the system, thus the recurring process slowly converges to the global minima of the function.

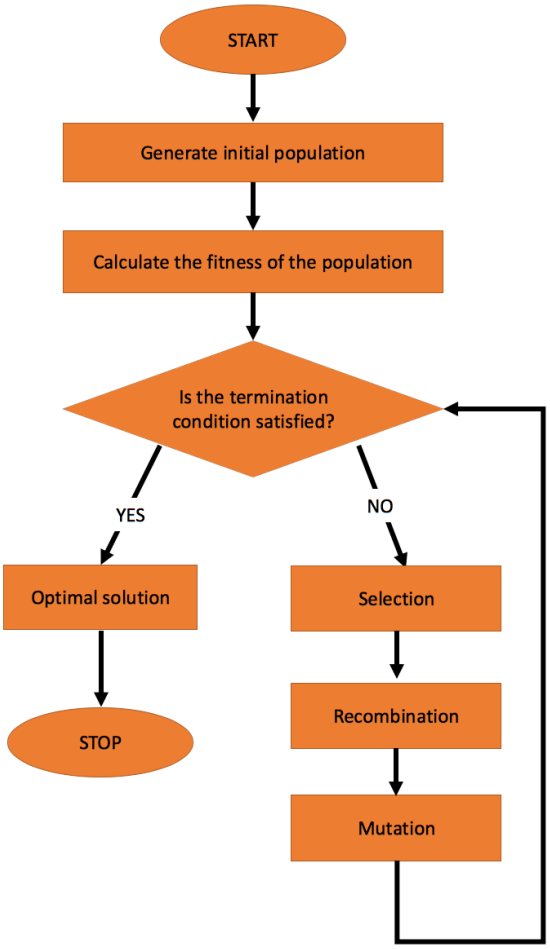


Figure 6: Flowchart of simple genetic algorithm. Genotypes are evaluated to see how fit they are to the desired solution. If enough similarities are achieved, the solution search stops. Until then, the algorithm continues to alter the genes.

In this evolutionary form of function solving, the term genotype is used to the string of numbers that defines a solution to a search problem (i.e control signals). These genotype has individual elements commonly referred as genes. Solving the computational problem is done by assessing how well the genotype represents a solution, or how close the output they provide is to the desired output. Survival of the fittest approach is implemented by sorting out these genotypes by the fitness scores, ranking their performance in the order, and choosing the genes so that the next generation are essentially more fit to the solution than the previous generation. This is conceptually visualized in figure 7.

The process was originally inspired by A.Thompson [21] who used unconstrained evolution to evolve working electronic circuits using a Field Programmable Gate Array(FPGA). In Thompson's experiment, tone discriminator, a digital circuit that distinguishes signals of 1 or 10 kHz, was programmed using evolution procedure. It was concluded that the controlled evolution of the configuring bit strings could relatively easily solve this problem. However, the experiment lead to a discovery that the successful circuits found from the GA worked by utilizing subtle electrical properties of the silicon, which lead to a ongoing research interest of material based computing system, EIM.

Miller and Downing[1] referred to the material with rich and dynamic physics to be a better candidate for the evolution, in contrast to flat and poor material such as silicon chips. This has inspired the computer controlled evolution of many unconventional, particularly disordered

material such as Liquid Crystal Display [22] or a cluster of metalic nanoparticles [2]. These prior research suggests that the physical systems, particularly ones that are high in complexity, are useful in genotype mappings as they can provide many ways of exploitable effects within the material system that can contribute to improved fitness.

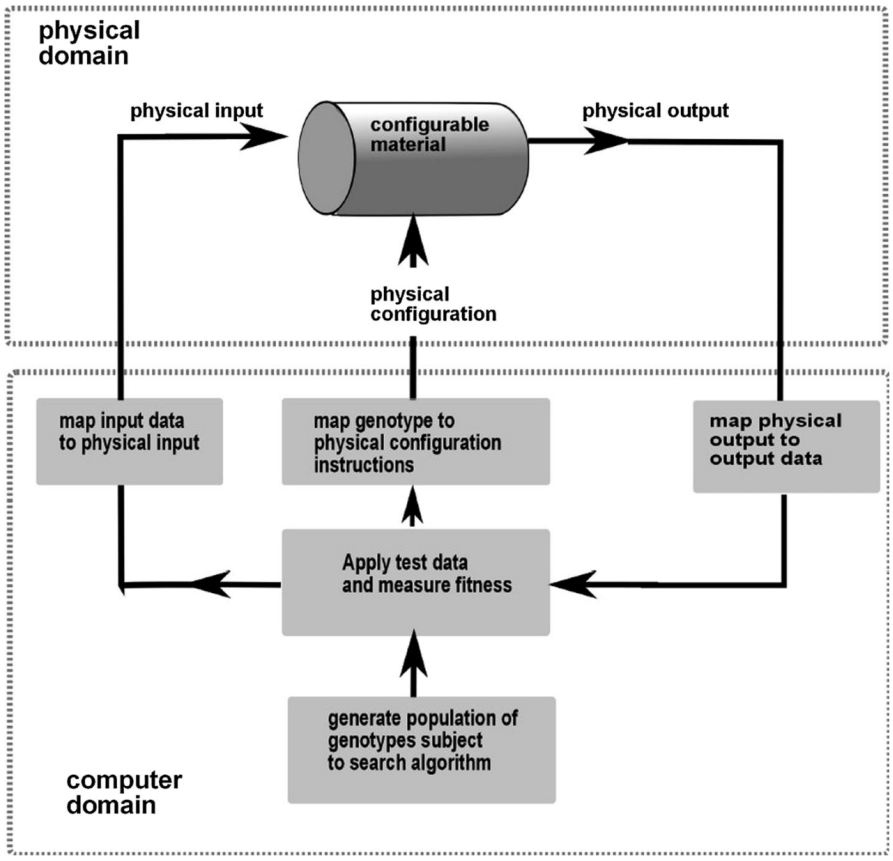


Figure 7: Concept of EIM. There are two domains: physical domain which is a material where signals can be applied or measured, and a computer domain where it controls the input, output, and control signals to be trasmitted. A genotype of numerical data is transferred in computer and is transformed into configuration patterns. The genotypes are subject to an evolutionary algorithm. Physical output signals are read from the material and converted to an appropriate form of data in the computer. A fitness value is obtained from the output data and supplied as a fitness of a genotype to the evolutionary algorithm

3 Device Fabrication

The fabrication scheme is an extension of CMOS device technology and is based on the single charge transport device made by Mueller et al [23]. The large part of the procedure will follow that of the 8 electrode spider design in the previous work by J. van. Gelder [3] and Bose et al [2]. Due to the non uniform nature of some of the procedures, it is not possible to create an indentical device with a same IV characteristics. However, achieving the already-known functionality does not require stringent electrical property, thus the device has rather large room of tolerance in its perfection.

The recipe starts with creating a doped region where the silicon will be bombarded with the dopant. The oxide are grown with a controlled thickness for the dopant window region so the desired dopant concentration is achieved only in that particular area. Pd electrodes are then created by patterning the resist using the photo-lithography technique and depositing Pd through an e-beam based evaporation chamber. The nano-electrodes are made in similar procedure but using electron beam lithography (EBL) to pattern the resist since it is a nanoscale structure, thus unproducable with the conventional photo-lithography system. The materials used for the nanoelectrodes will differ depeding on the dopant used. The steps recorded in this report are in a simplified format. The actual fabrication procedure includes numerous cleaning and baking steps which are necessary as a preparation procedure for the lithography, as well as ensuring the contamination level is low. It is also crucial to inspect the surface structure, particularly the depth, after the individual etching procedures. This improves the reliability of other fabrication processes by ensuring that the etched species are sufficiently removed. The fabrication process flow is depicted at the end of this section in figure 8. This process flow is a refined version of the previous recipe [3]. The changes made as well as the improved characteristics from those changes are discussed under the result section.

3.1 Oxide Growth

The one side polished intrinsic silicon wafer is coated with 200 nm of high quality oxide using the thermal furnace. Annealing was done at 1100^oC with sufficient O_2 gas flow. Ellipsometer was used to accurately determine the thickness of the oxide. This oxidation is followed by hydrogen annealing to passivate the dangling bond of the oxide layer, thus improving the quality of an insulator. $26 * 60$ μm rectangular window is etched by immersing the sample in a BHF(1:7) solution. This wet etching technique is known to result in an isotropic etched profile, a structure that gives an advantage during the processes explained later. It is however, necessary to be cautious of the overetching (i.e. removing too much SiO_2, thus the sample should be placed no more than 4 minutes, sufficient in removing the 200nm thick oxide window vertically.

3.2 Dopant Implantation

Ion implantation is chosen for a method of introducing the dopant into the device. It is a process where accelerated ions hit the wafer, penetrate into the bulk, slow down by collisional and stochastic processes, and come to rest within the material. There are several advantages of this method over the diffusion based doping process. The first and the most significant attribute to our purpose is the lateral confinement of the dopant profile. The sideways spreading of dopant under the mask is considerably less than that of thermal diffusion process in which the depth and the lateral extension are identical in the first approximation. This is especially important in the modern advanced CMOS also, where extremely small dimensions are fabricated. The second reason to choose ion implantation is the higher precision in manipulating the peak dopant concentration. As explained in the theory section, the density of the impurity sites for the electrons

to hop is one of the crucial parameter of the device. The availability of free simulation software such as TRIM, as well as the abundance of previous studies makes it a more matured technique to qualitatively fabricate the device with high control of the dopant concentration. Ion Implantation, however, is not a diffusion-free technique. It is necessary to include high temperature annealing after the implantation as the damages into the silicon crystal from the high energy ion collision must be recovered, and the dopant also has to be activated into the substitutional lattice sites. This can be optimized using the rapid thermal annealing(RTA) procedure where wafer is annealed to high temperature in a very short time (seconds to miliseconds) and is cooled down rapidly without overly exerting the thermal stress to the wafer. This technique is known to minimize the dopant diffusion because of the shorter annealing time, without hugely compromising the amount of dopant activation[24].
For this thesis project, Boron was implanted as BF using 40keV energy and $3 * 10^{14} ions/cm^2$ dosage. Implantation was followed by etching away the 40 nm oxide layer that is grown on the dopant window region in prior for the masking purposes.

3.3 Micro-Lithography

Fabrication of the contact pads and the electrodes should follow the device doping. Using the same photolithography technique as the patterning of the dopant windows, the photoresist was exposed at where the contact pad material will be deposited. The fabrication of this contact pad structure must occur after the ion implantation as the high energy ions from the implantation process could damage the metal structure[3]. Upon development of the resist, few nm of Ti was deposited as a sticking layer, followed by the Pd deposition, both on the entire surface using BAK600. By removing the existing photoresist from the surface, the sputtered material above the photoresist will also be washed away since they are not bounded to the surface of the substrate. The deposition area with no photoresist, where the patterning and development occured, will retain the material. This procedure is known as lift-off, and can result in a structured metallic pattern such as the ones fabricated in this experiment.

3.4 Nano-Lithography

EBL is used to pattern the nano electrode. This technique "writes" on the PMMA negative photoresist by high energy electron bombardment, resulting in very small yet precise feature imprinted on the resist. Upon developing the pattern, nano electrode material can be deposited using Bak600. The electrode structures are present once the PMMA resist has been "lifted-off". At this moment, this electrode has to bridge the dopant window and the Pd contact pad. The wet etching of the oxide had resulted in a sloped oxide structure in contrast to the very sharp vertical wall which is produceable by the other etching technique, dry etching. Thus the nano electrodes can be reliably made without requiring to be deposited on the vertical photoresist side walls. The deposited metals must be chosen based on the dopant element. As later explained in the result section, the surface resistance becomes a hindrance when characterizing the dopant device under the low temperature. As such, the contact resistance arising from the difference between the dopant energy level and the metal's fermi level must be minimal in order to create an efficient device.

3.5 Post-Etching

The dopant concentration underneath the nano electrodes must be above the critical concentration to be in the metallic regime. If this area is in the insulating regime, Schottky barrier will be present at the interface, thus imposing an obstacle in the electronic applications of the device. To achieve the desired dopant concentration at the Si surface without altering the profile near the

nano electrodes, Si surface is etched until the surface concentration is reduced to the insulating regime where the hopping conduction can occur. Previously mentioned wet etching is not suitable because the isotropic etching profile will result in the undercut of the silicon, thus there is a risk of etching away the metallic Si underneath the electrodes, or worse, completely separating the Si from the electrodes by overetching. Therefore the reactive ion etching (RIE),also known as plasma etching, is implemented. RIE is done in a vacuum chanmber filled with a reactive gases. These gases are excited via RF field and produces excited and ionized species that are both important for the etching process. The former can chemically etch away the desired material owing to its high reactivity, and the latter is accelerated by the RF field and impart energy directionally to the surface. The process results in more anisotropic etching profile than the wet etching process due to the sidewall passivation, typically achieved by introducing a carbon-containing fluorine species to the plasma[25]. This makes it a suitable for the highly vertical walls as well as when an accurate reproduction of the photoresist dimensions are needed on to the structure.
For this experiment, the pressure of the TEtske RIE chamber was maintained at 10mTorr and the RF power at 60 W. CHF_3, and O_2, flow were set at 25 and 5 sccm respectively. These flowrates can be varied to achieve different etch rate for SiO_2 and Si[26]. For the purpose of this experiment, this flow rate is sufficient to etch Si at approximately 40 nm/min rate. This can be done for various duration to achieve the desired surface dopant concentration which will ultimately relate to the operational temeprature.
However, RIE process will not give nanoscale precision due to the slight variance in each processes (cleaness of the chamber, sample location on the holder, etc.) Therefore, the technique should be used in combination with the topological analysis such as Atomic Force Microscopy(AFM) in order to qualitatively monitor the etched profile.

3.6 Post fabrication treatment

The masking layer of the ion implantation process is tuned in such way that the peak dopant concentration is located in the vicinity of the oxide interface. By removing this top layer, the silicon surface becomes the layer with the highest dopant concentration. As higher dopant concentration leads to lower resistance, the dopant conduction during our experiment is expected to occur near the surface. As there are no protective oxide layer on top of this active region (not deliberately grown, very thin layer of oxide can exist by an air exposure), the device is often vulnerable to the change in the surface condition. Should the device conductivity degrade, it is possible to restore its functionality by providing post fabrication treatment to “cleanse” the surface state of the device. RIE process described in the previous section leaves the surface with high concentration of fluorine or carbon [27]. This carbon components can be removed with 1 minute of O_2 plasma etch at 10 10mTorr pressure with the induction power of 25 W and the gas flow of 50 sccm. The oxygen terminated surface can then be treated with dipping into HF acid for 30 seconds which will remove the oxygen layer formed from the plasma treatment.

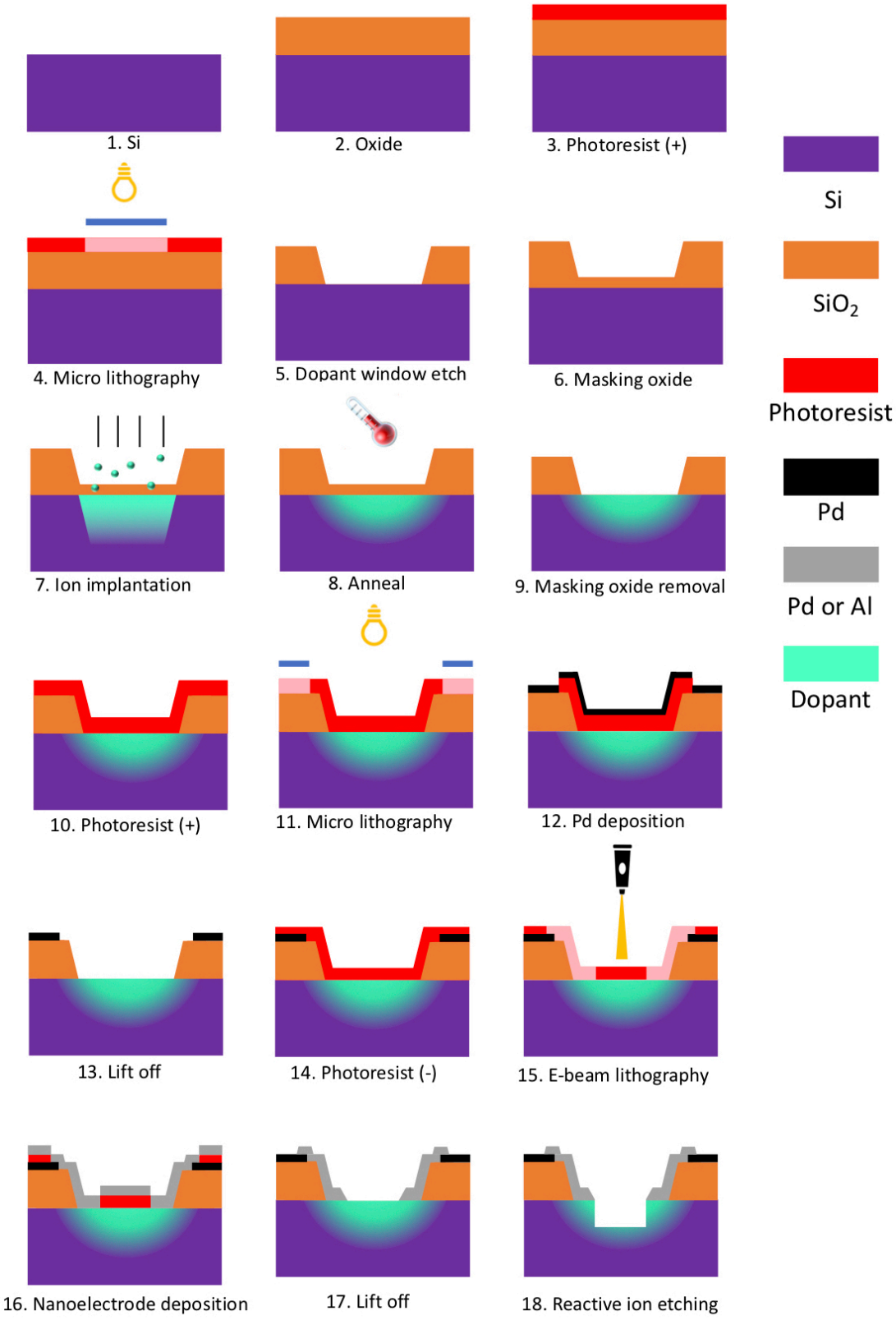


Figure 8: Summary of the fabrication procedure of the dopant device.

4 Experimental Setups

4.1 Boolean Logic

The searching for boolean logic in the disordered system was originally accomplished by Bose et al[2]. The two input and one output requisite of the conventional CMOS is translated in our device as using two electrodes as input where a specific waveform is sent, and one as an output which is used to read an output current varied from the input amplitude and the value of control voltages, which is assigned to the remaining 5 electrodes. These control voltages can locally manipulate the potential landscape of the device and alter the percolation path of the electrons from the input electrode to an output electrode. Thus depending on the control voltage values, unique and rich input-output relations can be obtained, and this relation landscape is explored using the genetic algorithm to find a global minima a.k.a function to be solved.

4.1.1 Fitness score calculation

Referring to the theory section, the control voltages are recorded as genes, and complete set of genes($V_1 \sim V_5$) are referred as genomes. The fitness score (F) will be calculated for each genomes by comparing how closely the output Y satisfies the ideal output X. In contrast to theory, the points of signal transition can lead to unexpected spike or dip in the output, thus these points will be effectively ignored by assigning lower weights W at these areas. For the remainder of the signal that consitututes the output, Y and X are computed as:

$$Y = mX + c$$

by estimating the magnitude m and the offset c. High signal to noise ratio as well as low offset is desired for the good output, thus the fitness score is defined as:

$$F = \frac{m}{\sqrt{r} + \delta|c|}$$

where delta is a mixing parameter and r is the residual error, thus SNR is $(m/\sqrt{r})$. Further parameters can be used to characterize the fitness score, the modified fitness function is defined as:

$$F = A * \frac{m}{\sqrt{r} + \delta|c|} + B * \frac{1}{r} + C * F_Q + D * Novelty$$

where the F_Q is the fitness quality which can be defined as:

$$F_Q = \frac{min_1 - max_0}{max_1 - min_0}$$

where min and max is defined as the minimum and maximum of the signal $I_{out}(t)$ at the time sequence when the signal corresponds to high($f(t) = 1$) or low($f(t) = 0$).

The numerator of the fitness quality is a tolerance parameter which is normalized by the full spectral range($max_1 - min_0$). This method ensures $F_Q < 1$ yet doesn't take in account of the offset of min_0, thus this penalty factor is subtracted from the denominator to redefine the fitness quality as:

$$F_Q = \frac{min_1 - max_0}{max_1 - min_0 + |min_0|}$$

Novelty is a concept that can be potentially introduced in defining the output-input similarities. It is a parameter which gives credibility to a set of genes $V_{6\sim10}$ that are vastly different from the set of genes $V_{1\sim5}$ yet gives very similar output. Finally, the variables A to D define the weight of each parameters. Currently, the structure of novelty has not been fully calculated. Furthermore, improvement in the search efficiency can be expected from modifying the fitness calculation. However, redrawing of the algorithm is outside the scope of this thesis, thus further development is expected to be made in the future.

4.1.2 Breeding mechanism

Each generation G_n consists of set of genomes $g = G_{n,i}$ for $1 < i < m$ that have different fitness scores. Just like the natural selection, it is in the best interest to preserve the genomes that perform well and abolish the underwelming ones for the sake of improving the entire species. For a set of 20 genomes, 5 best performing ones directly proceed to the next generation. The 5 following best ones (6th to 10th best) are slightly modified by ±1% and bred as $G_{(n+1),i} = G_{n,j} * G_{n,k}$ which consists of a uniform crossover with a mixing ratio of 0.5 in which each gene g_l of the offspring $g = G_{(n+1),i}$ is assigned randomly from either parent gene $G_{n,j,l} or G_{n,k,l}$. Similarly, the following 5 genes are crossover of the five best performing genes with its follower $(G_{n,i} * G_{n,i})$. The final set of genes, ones that are not likely to survive, go through chance of mutation in which they are given a random value with a probability of 0.1. Thus G_n is sorted in the descending fitness order and the next generation is created as followed:

$$G_{(n+1),1} \rightarrow G_{(n+1),5} = G_{n,1} \rightarrow G_{n,5}$$

$$G_{(n+1),6} \rightarrow G_{(n+1),10} = G_{n,i}^{+1\%} * G_{n,i}^{-1\%}$$

$$G_{(n+1),11} \rightarrow G_{(n+1),15} = G_{n,i} * G_{n,i}$$

$$G_{(n+1),16} \rightarrow G_{(n+1),20} = G_{n,i} * RANDOM(G_n)$$

Where i ranges from 1 to 5. Illustration for this breeding mechanism is shown in figure 9.

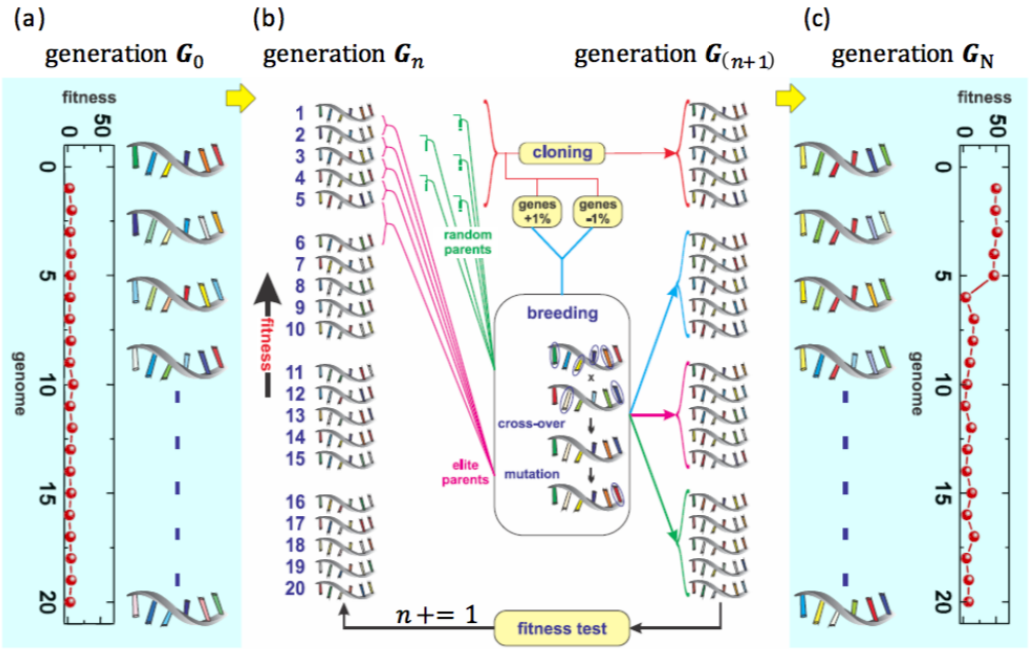


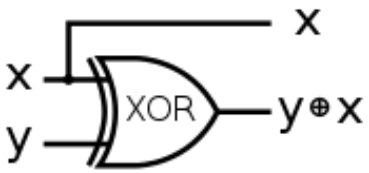
Figure 9: a) The GA starts with a random initial generation. (b) Many cloning and intercrossing processes are done until (c) a final generation is reached. The genome with the highest fitness should have a higher fitness than any genomes from the first generation, G_0.Image taken from [28]

4.1.3 Multiple Boolean Logics

While the performance of the ANN relies heavily on the method of teaching and its learning processes, the hardware realization of such system should also look into the innate intelligence of the material system itself. There are two approaches to measure how "intelligent" the dopant devices

are: IQ test and full-search. IQ test is a quick method where all the input output configuration can be invariantly tried in a speedy manner to get an estimate idea of how "smart". This is done by applying $V_{HIGH} = 1V$ or $V_{LOW} = 0V$ to every electrodes while the one electrode is assigned as an output; forming $2^7 = 128$ voltage configurations. Such method tests the variance in the type of logic obtainable from the set of binary electrode configurations. This can be an efficient method in detecting if a device has a certain boolean logic since it takes less than an hour to try all the voltage configurations for every electrodes as an output. However, it lacks the measure of the abundance as well as the quality of the boolean logic it can find since the applied voltages are fixed to 1V or 0V. Another method is a full-search which generates over thousands of randomly chosen voltage configurations and tests them as one generation. Each output waveform is fit into the 16 solutions, and checks the abundance of each solutions within the devices by creating a plot of the logic abundance with respect to the fitness. This time consuming method can indicate the smartness of the device by showing all boolean logic result which it managed to output with the fitness score taken into account. Previous experiments by Van Gelder [3] have shown that the boolean logic can be found on the arsenic dopant device without utilizing all five control voltages. Therefore, it should be in the next scope to determine how far the 8 electrode device can accomplish in the new goals, rather than determining how well they do in the already established benchmarks of single boolean logics.

Control NOT gate (CNOT) is a standard basis for a two-qubit quantum logic gate. It flips the second bit only when the first bit is HIGH, and leaves it otherwise when the first bit is LOW[29]. The classical representation of CNOT gate is shown in figure 10. It can be treated as two-input-two-output system where two outputs should be a follower of the control input, and an XOR gate. Rather small change is necessary from the conventional boolean logic search in order to aim for



input		output	
x	y	x	y+x
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 10: Classical representation of Control NOT gate. The target signal y is reversed only if the control x is 1

the CNOT gate. Instead of having one output, another electrode that was previously used for one of the control is now assigned as a second output. This method complicates the search dimension since there are now two parameters that need to be optimized, despite reducing the dimensionality by one. Alternative method is using two devices as seen in figure 11 b). Each device will have

one input and one output, with however many control voltages that it is assigned to the remaining electrodes. One electrode from each device wil be used as a bridge for control signal to talk to the input signal. Such method slightly deviates from the goal of challenging the intelligence of the singular device. However, the conceptual goal of achieving higher functionality than the "Standard" boolean logic is still within the scope. Optimizing such logic requires another layer of

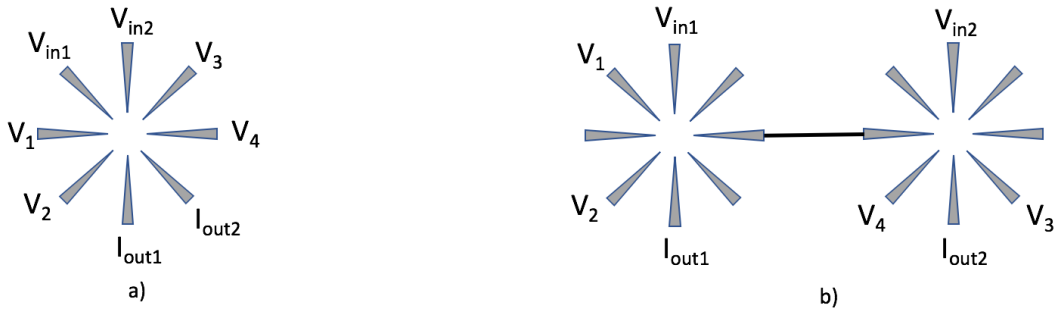


Figure 11: Device setups for the CNOT gate. a) For a single device, it is only a matter of assigning one of the control electrode as an output. The location of control, input, as well as output can be arbitrary. b) Two device setup in which each device has an input and an output. Bridging exists beteen two devices for the control signal to interfere with the input signal

fitness calculation from the previous formula:

$$F_{overall} = E * F_1 + H * F_2$$

where the overall fitness score $F_{overall}$ is calculated as the sum of the fitness scores of the individual output with an assigned weight E and H on it.

4.2 Darwin internet

The logic functionality can be done using few transistors, yet the real computing power of modern laptops and smart electronics are due to the billions of transistors working in parallels. It is thus within the possibility that the dopant network can have higher functionality from incorporating multiple devices. As the dopant network is a designless reconfigurable device, it is unlikely that it has the same scalability as the conventional CMOS devices. However, more complex information/tasks than the boolean logic may be processible by creating an interconnecting network of the dopant devices. This section will be dedicated to the concept of the scaled up system and its experimental setups. The experiment aims to evolve the "interconnectivity" of the dopant internet to achieve functionality. This is within the scope of the overall project to achieve the "scaled-up" functionalities.

4.2.1 Theory: Interconnectivity

The external research estimates that a human brain can have 20 billion neocortical neurons, with an average of 7000 synaptic connections each[30]. The intelligence and the brain capability is tremendous owning to this colossal number of principal units. However, the wiring of synapses play a crucial role in the decision making from the firing activity[31]. The schematic to utilise this interconnectivity in realising functionality is shown in figure 12. 8 electrodes of the first device can be connected to the intermediating layer which from here will be referred as an interconnect layer, and there are $N_I = 8$ layers.

For N_C number of devices in the network, every one of them has N_I electrodes which can be connected to the interconnect layer by means of a switch with a binary state W_{IC} (where 1

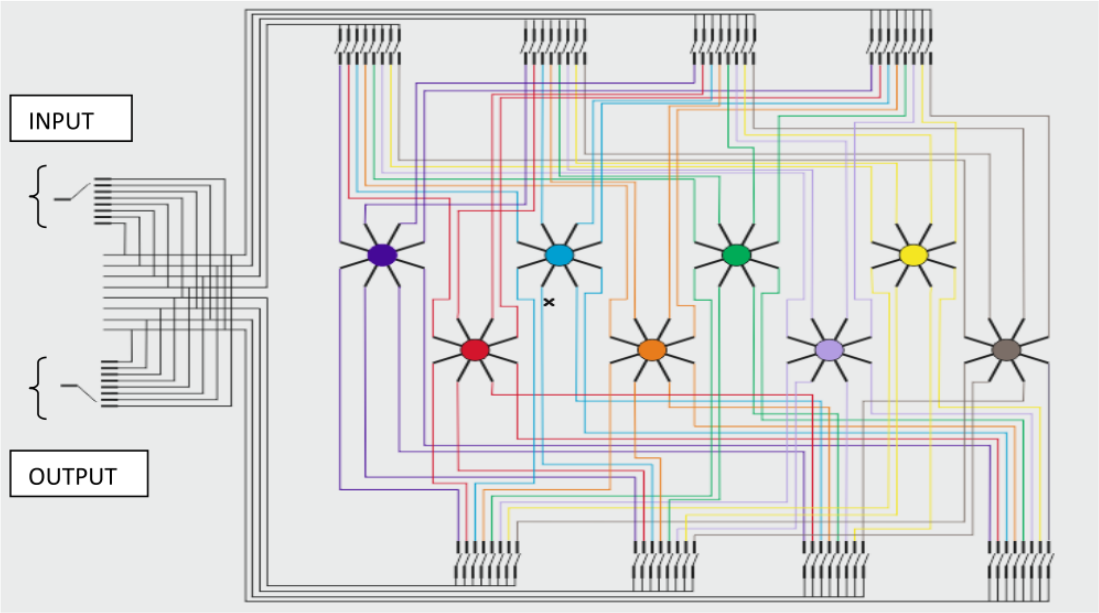


Figure 12: Design schematic of the interconnections between the devices. Image taken from [32]

is closed and 0 is Open). This can be represented by an interconnectivity matrix $W = N_I * N_C$. These interconnect layer can also be connected to the power source as well as the readout sensor, thus another binary matrix W_B and W_O are used to represent the connectivity to those terminals. There are thus 2^{N_I} possibility for the switch states of the power and readout matrix, combined with the interconnectivity matrix W, allows the network to have $2^{N_C N_I + 2N_I}$ connectivity. Referring to figure 12, a current through the network can be wired across any devices, thus each wiring configuration can create a different recurrent neural network(RNN) where the internal states are the electrode voltages. The setup is theoretically possible to deal with time-varying signals if the input is also time-varying. However, it can also be used to obtain a stable current output for certain functionality such as classification. Thus the setup is reduced into a simple feed-forward neural network. This neural network modelling of the dopant internet is illustratively shown in figure 13. With such modelling in mind, any neural network functionality should, in theory, be possible with the dopant internet setup. The applied voltages on each electrode can be tuned by the

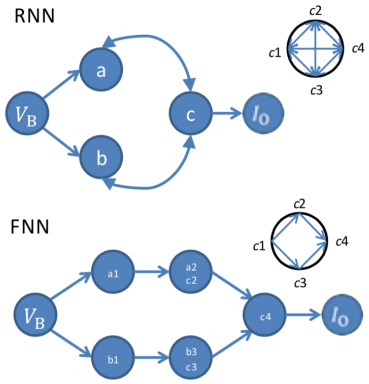


Figure 13: Illustrated model of RNN and FNN. RNN have a recurrent signal path where as FNN have a forwarding signal path with no signals returning to the previous nodes. Image taken from [28]

wiring configuration from the nearest battery source to the said electrode as illustrated in figure

14. Rather than directly applying a desired voltage value to the electrode from the power source as demonstrated in the logic search setup, the connection from the source to the electrode can be manipulated with the switch configuration, thus applying a different value of voltages without requiring multiple sources. In the figure 14 example, it is possible to change I_{out1} and I_{out2} at their electrodes by manipulating the bias at its neighbouring electrode whose connectivity is controlled by switch A and B. By changing the switch configuration such that the switch A is ON, its respective electrode will acquire different bias because the distance from the source, V_{in} has now changed. This wiring configuration can be evolved by controlling the switches using genetic algorithm. For a setup with $N_C = 8$, there are $2^{8*8+2*8} \approx 1.2 * 10^{24} \approx 10^{24}$ wiring configurations. Suppose the source and the sensor electrodes are chosen for all 8 devices, wiring configuration is reduced to $2^{64} \approx 10^{19}$. This number can be further reduced by realizing that there will be some

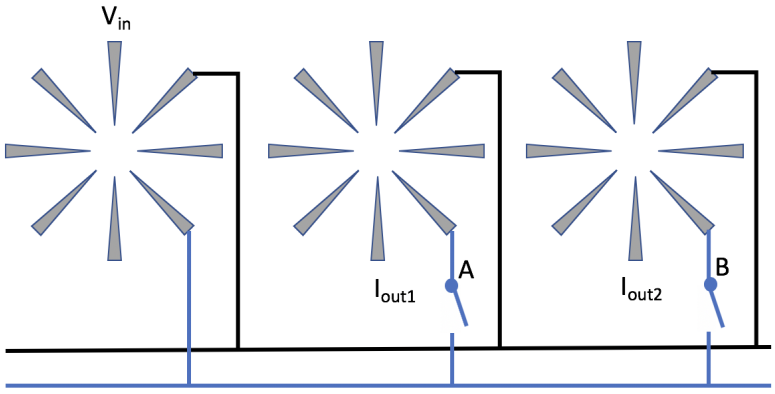


Figure 14: Illustration of difference that the switching can make. The output current recorded from two I_outs are different depending on the state of their respective switches because the current path from the V_{in} will change drastically.

degenerate configurations with respect to the current-voltage relations. However, in practice, it is difficult to assume the exact reduction due to the resistance variance amongst devices as well as the asymmetry of the Coulomb gap between the electrodes under low-temperature condition. Nevertheless, with correctly determining the desired output, the large area of the search dimension is irrelevant as genetic algorithm should slowly yet deterministically "figure its way out".

4.2.2 Theory: Pattern Recognition

The fundamental principle behind the classification task is "If X is satisfied, then Y"[33] where X is the antecedent of the rule and is formed from a set of conditions and Y is the consequent of the rule, i.e. predicted class. This can be applied in various ways to define own classification rules. For a specific input, only one output has to be responsive to be able to classify the information on the input. This will be incorporated in the interconnectivity experiment. For the purpose of our experiment, dopant internet with $N_C = 8$, interconnectivity matrix W will consist of input, output, and interconnect layers as seen in figure 15 b).

In this context, if the digit 1 is implemented, the pixels that constitutes 1 is mapped in the matrix such that $W_{1b} = W_{1e} = W_{1h} = W_{c2} = W_{f2} = 1$ and the rest is 0. W_B is set as {1,1,0,0,0,0,0,0} which connects battery only to the input layer and W_o is set as {0,0,0,0,0,0,0,1} such that the last row of matrix W is the output layer. The remaining row is used for the weights of the hidden layer. For example, the output node h8 can recognize the digit 1 if there is a flow of current after setting $W_{8h} = 1$ only if the input image looks like a 1. In a similar manner, if the nodes $a8$ to $g8$ can recognize the digits 2 to 8, then the dopant internet can fulfil the classification functionality.

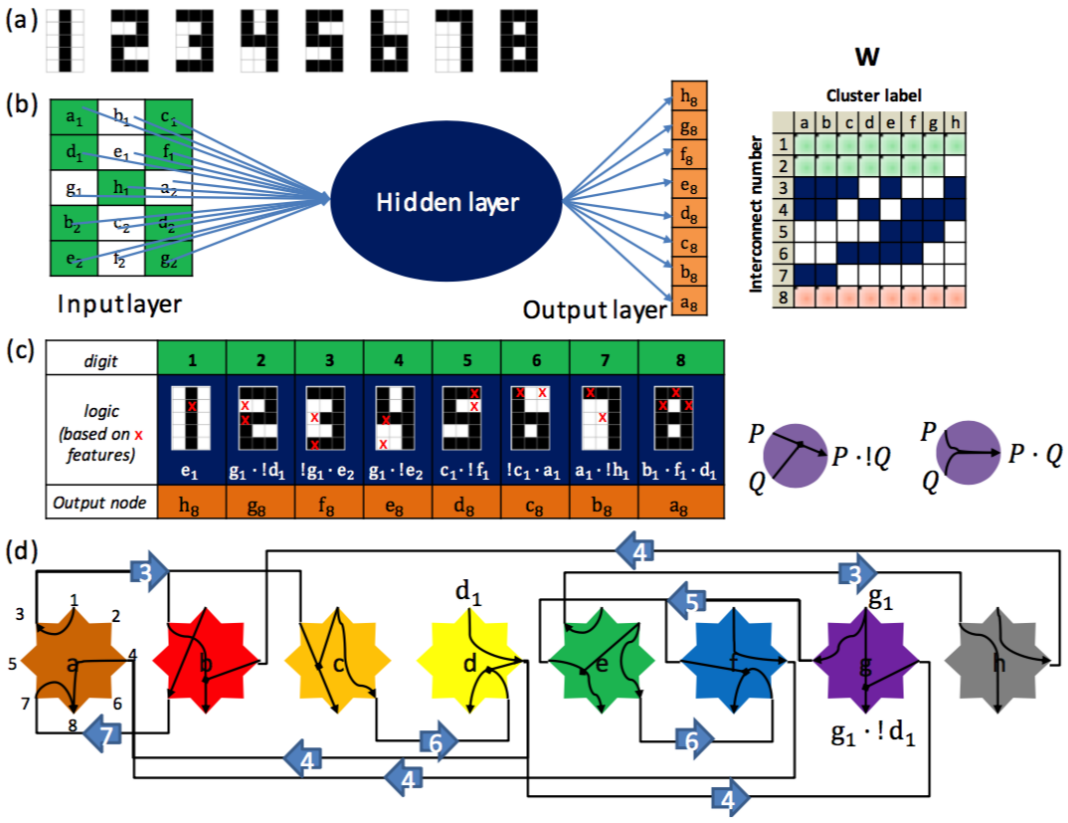


Figure 15: Conceptual image of 3 by 5 digit classification a) digit from 1 to 8 can be represented with 15 pixels b) which can be translated as an input, and be shrinked down to 8 output. c)Only two kinds of logic are necessary to uniquely recognize the output d) Realization of c) with the actual network. Image taken from [28]

4.2.3 Practicals: Switch experiment overview

Overview of the whole switch experiment can be seen in figure 16. The process begins with the 8 by 8 array of booleans. The individual segment of the array corresponds to a particular switch from the ICs. Thus by setting that boolean to true, the switch will connect the corresponding electrode to the interconnect layer. This interconnect layer is a floating metallic island, and the access can be shared by the same electrode of 8 different devices. Furthermore, by connecting to the input of the current source unit, Keithley2400, the voltage can be applied from any of the interconnect layers. Similarly, another interconnect layer(not the same one as the input, for an obvious reason) can be connected to the output of the Keithley2400, thus the current value can be recorded from any of the interconnect layers. This interconnect layers that are connected to the battery and the sensor will be referred to a source layer and a sensor layer. Suppose a particular switching configuration is in effect, the current from any particular output electrode can be detected by ensuring the switching such that only that electrode is connected to the sensor layer. Thus by sweeping switch configuration so every output electrodes are singularly open, multiple I_{out}'s can be obtained.

With $N_C = 8$ and one sensor layer, it is possible to classify 8 different inputs provided that

1. For every input, one output electrode is HIGH
2. The output electrode is HIGH for only one particular input and LOW for the other input combination

The first requirement corresponds to whether the network can detect the solution. If no out-

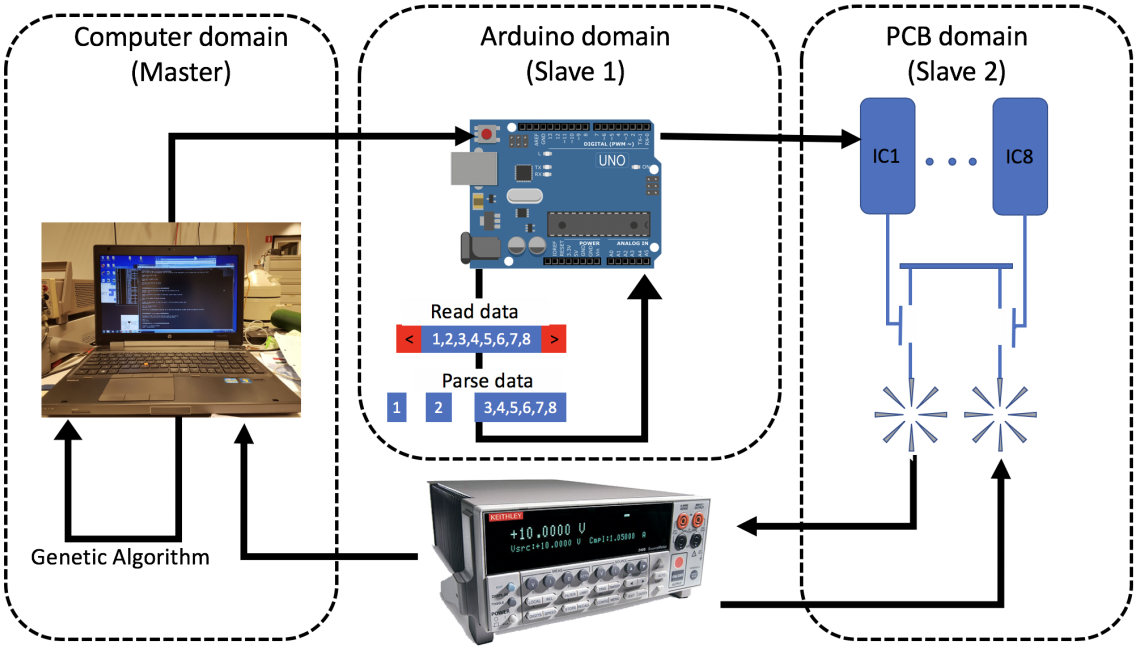


Figure 16: The image overview of the whole protocol. Arduino bridges the Computer and PCB domain to translate the instructions.

put is HIGH, then the system simply did not understand what the input is. While more than one output being HIGH indicates that the system could not differentiate the input from two possible solutions out of the eight. The second requirement corresponds to the network's ability to separate the solution. If an output electrode is HIGH for two different inputs, it means that the system can not differentiate two different inputs (e.g not being able to find the difference between 3 and 8.) As such, the system with N different input and M different outputs (one source layer and sensor layer) will have an output array W_{NM} where the individual item in the array corresponds to the detected current at the electrode of the device M from a particular switch configuration with the Nth input. What is considered HIGH and LOW are ambiguous and can be tuned depending on the experiment. For this experiment, all the current values will be normalized with with the highest value of current from the respective rows and columns. A certain percentage value can be set to determine the threshold value which distinguishes the HIGH and LOW. By setting this threshold value low, the condition to achieve singularity is also harsher because the range of values that can be considered HIGH with respect to the maximum value broadens. The evaluation method using the HIGH and LOW status of the output is explained in the next section.

Above requirements are met if (1)only one value from a row is HIGH and (2)that value is also the lonely HIGH value from its column. This evaluation process is illustrated in figure 17. In the figure, a) shows the effect of the threshold setting on the evaluation result. Yellow boxes are the row-wise highest current value recorded in nA. As the threshold value decreases to 0.8, the first row fails to meet the requirement (1) because 4 nA and 4.1 nA results are also considered HIGH in respect to the 5 nA result. When the threshold is further reduced to 0.5, the red boxes become newly "indistinguishable" output, therefore no rows meet the requirement (1). To meet both requirements, column-wise highest also has to be mapped, this is illustrated with the green box in figure 17 d). The orange box in the output array is where the row and column-wise highest meet. Thus these results meet both requirement (1) and (2), concluding with three items classifiable for threshold = 0.9.

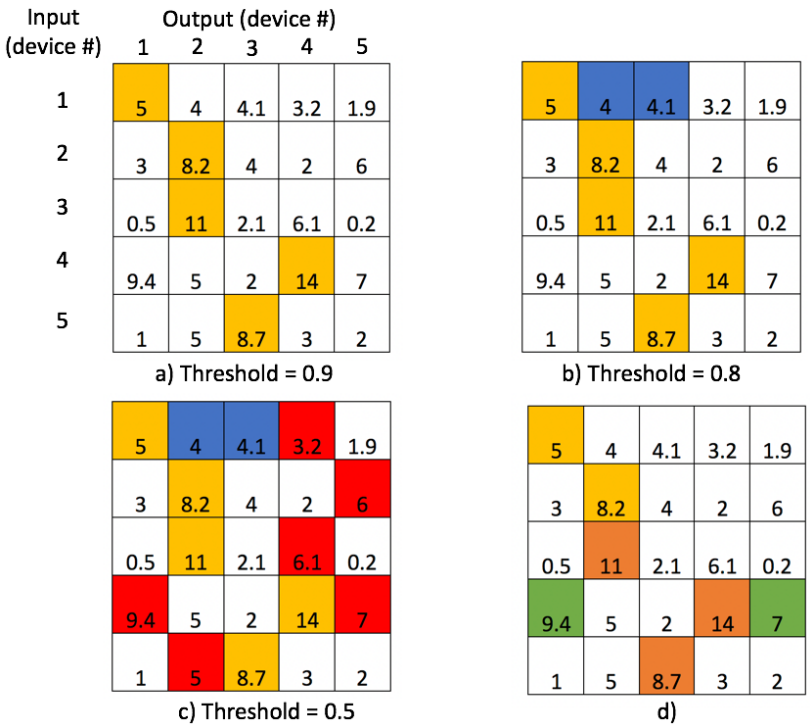


Figure 17: 5 by 5 output array showing the current value in nA where a) box in yellow indicates the row-wise highest value. a)If threshold =0.9 ,b) =0.8, blue is indistinguishable from the highest, first row now unsatisfies the requirement. c) At threshold of 0.5, red is also indistinguishable. No rows from the output array meet requirement (1) d) The array from a), but green is the column-wise highest value. Orange is where both requirement(1) and (2) are satisfied, hence classifiable.

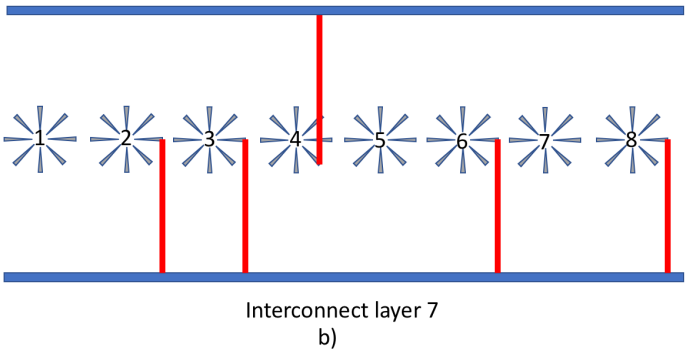
4.2.4 Practicals: Experimental procedure

The 8 by 8 boolean array which from here on will be referred to switch configuration, is an important segment of data which not only represents the state of the switch but are used for representing the hardware connections to the respective switches/interconnect layers. Figure19 a) illustrates the relationship between each boolean in the array and the experimental parameters. As later explained in the PCB development section, controlling of the individual switches are done by Arduino. To turn on particular switches, their boolean state must be converted to the byte. The top segment of a) tells the bytewise identity of each switch. These individual switches have bridges between a particular electrode of the particular device, to the intermediate layer. The right and the bottom segment can be used to guide which switch is being turned ON. b) and c) show the exact hardware location of the where these individual switches are controlling the access of. Lastly, when the switch is turned ON, the electrode make a connection to one of the eight interconnect layers. To identify which electrical port from the dipstick should be connected to the Keithley source to label the source and sensor layers, the left segment of a) can be used. d) shows which port is connected to which row in the switch configuration. As an example, if an electrode 1 of device 7 is used as a source, the boolean that is at the intersection between the device 7 and electrode 1 must be turned ON. This means the Arduino will send byte information of 64 to the PCB to turn ON that switch, and to allow the flow of current from there, simply connect the output of the Keithley to the port 4 of the connection pins seen in d). This way, it is possible to acquire IV curves between any electrode by turning on two switches that correspond to those electrodes, so long as the sensor and source layers are selected carefully. The current experimental setup also allows acquisition of all the IV relation between one electrode to the seven others of the same device. The experimental procedure for the internet experiment follows that of standard GA procedure;

1. Generate initial populations
2. Calculate their fitness
3. Select the fittest of the population
4. Recombine/mutate

	Device / Electrode	1	2	3	4	5	6	7	8
Irrelevant (Input)	5	1	0	0	1	0	1	0	1
Does not contribute (sole ON)	6	0	0	0	1	0	0	0	0
	7	0	1	1	0	0	1	0	1
	8	1	0	1	1	1	1	1	0
Irrelevant (Output)	1	1	0	0	0	1	0	0	1
	2	1	1	1	0	0	0	0	0
	3	1	0	0	0	1	1	0	1
	4	1	0	1	0	1	1	0	0

a)



b)

Figure 18: Illustration to indicate the flaws in generating genomes randomly. a) Some rows are irrelevant in the variety(row1 and row 5), or effectively meaningless(row2). b) The physical meaning of what row 2 and row 3 does. The situation in row 2 is effectively the same as having no switch ON

The initial population here is a set of switch configurations or genomes. While generating multiple 8 by 8 arrays of boolean is extremely simple, ensuring the variation amongst them becomes extremely important. Take the example shown in figure 18. The configuration shown has three rows that are unoptimized. The input and output rows, electrode 5 and 1 respectively for these experiments, will not contribute to the interconnectivity between the devices because they are connected to the source and sensor layers. Thus with the straightforward genome generation, two genomes which have identical row 2,3,4,6,7,8 will be treated as different genomes, yet will effectively result in very same switch configuration. Moreover, any configuration where there is only one ON in the entire row should also be discarded. Referring to the same figure, there are 4 devices with switch ON for their electrode 7, indicating that 4 connections have been made to the interconnect layer 7. The row above has only one switch ON from the device 4. This situation leads to a false interpretation of a variance in the genomes because having no other connection only creates interconnect layer 6 as a floating metal, thus is no different to having that switch OFF.

With the above concerns, the following procedures are taken in the modified code for the full search experiment:

1. Randomly generate arrays
2. Transform the input/output rows to zero
3. Transform all column with no device to zero
4. For the columns unaffeected from 3, check if any rows have only one 1s
5. Go through all the genomes for a duplicate check

If any genomes are flagged from item (4) and (5), they are scratched and another array is randomly generated and goes through the procedures again until all the genomes satisfy above conditions to ensure the variety amongst them. This elimination of invalid switch configurations can reduce the number of possible configuration to:

$$\frac{(2^{N_C} - N_C)}{2^{N_C}} * 2^{N_I * N_C - (N_B * N_S) * N_C}$$

Where N_B and N_S is the number of rows used for the input and output respectively. The factor in the exponent takes care of the reduced switch configuration from neglecting the input/output row state. The fraction represents the reduction from eliminating the only one connection per row situation.

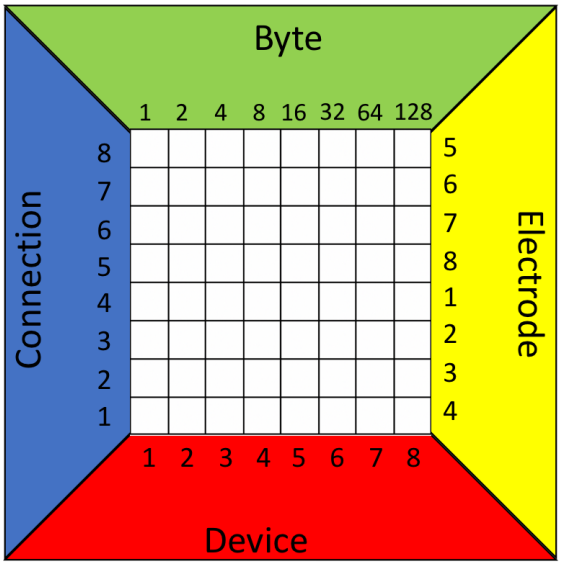
Referring to the switch overview chapter, every genomes will come with a certain W_{NM} output current array. For the purpose of evaluating the genomes, this array must be converted to a certain fitness score to determine how close they are to the ideal solution. This experiment will use two values; fitness score and success number. Fitness score is calculated by normalizing with respect to the highest value from the row. For every element, their absolute value status is determined as:

$$\frac{(I^{AB}_{OUT} / I^{A}_{max})}{Tolerance} = \begin{cases} HIGH, & if \quad \geq \quad 1.0 \\ LOW, & if \quad < \quad 1.0 \end{cases}$$

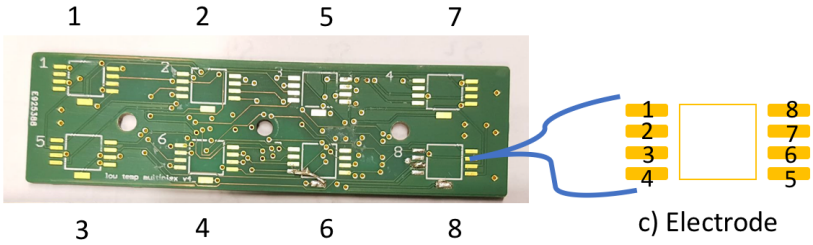
With I^{AB}_{OUT} being the output current at row A and Column B, I^{A}_{max} is the highest output current value from row A, and tolerance is a parameter that determines the threshold value for HIGH and LOW. This checking will be done to every item in row A of the output array. When only one item is labelled HIGH, the output row A has no current that can be considered HIGH in respect to the highest value from that row apart from the highest one itself. Therefore, when this counter is one, fitness score adds 3 points to itself, indicating a successful one-to-one input-output relation; $Fitness = Fitness + 3$. For a scenario where more than two are considered HIGH, fitness score subtracts a point for x number of HIGHs that were counted; $Fitness = Fitness - xFitness$.

This fitness score only focuses on whether for a particular input, more than one output was sufficiently responsive or not. To truly determine the unique input-output relation, the output array must be a permutation matrix, where exactly one entry of 1 in each row and each column and 0s elsewhere. Firstly, the highest value from row A of the output array is pointed. Then the column list of that value is also scanned, and check whether the I^{AB}_{OUT} is the highest from the column B. If I^{AB}_{OUT} represents the singular highest value from both row A and column B, then it can be defined as a successful classification, hence the success number is incremented by one:

$$I^{A}_{max} \stackrel{?}{=} I^{B}_{max} \begin{cases} Success = Success + 1, & if \quad True \\ Success = Success, & if \quad False \end{cases}$$

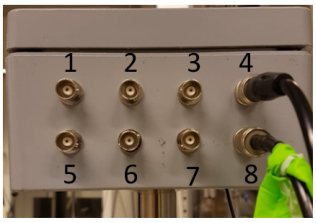


a)Overview



b) Devices

c) Electrode



d) Connection

Figure 19: Hardware schematics of the switch array. a)8 by 8 boolean array to indicate the switch state. Each side describes the corresponding information that are used in hardware or software interfaces. b) The indications of where each information from a) corresponds to. Note the numbering of the device on the PCB itself does not correspond to the device numbering.

Once all the genomes of the generation have been evaluated, they are ranked in the descending order of the fitness score. Currently designed selection procedure selects one genome who had the highest score, and the rest are discarded. The 4/5 of the new population is reborn as a mutation of this sole winner. The copy of this winner array is made, then by every bit, they are given 30% chance to switch their boolean state. The remainder of the new population is an entirely new genome, randomly generated like the initial population.

The python code to implement the entire procedures is available on the skyNEt github repository. Here a pseudo-code is included to give the reader a general idea of the GA process.

Algorithm 1 Interconnectivity Experiment

```
1:  procedure SWITCH EXPERIMENT
2:      i,j ← generation, genome
3:      SwitchConfig ← initial pop
4:      Make Connection to Arduino and Keithley:
5:
6:      for i number of times do
7:          for j number of times do
8:              Record the output current
9:              Evaluate their score
10:         Choose the winner
11:         Mutate the rest
```

4.2.5 Practicals: Dipstick development

To carry on the switch experiment, entirely new model of dipstick had to be developed since the number of electrical connections as well as the mounting PCB is vastly different from the conventional dip sticks used in NE lab. The early model of the dipstick designed for the interconnect experiment can be seen in figure 20 a). The samples will be wired on the PCB which will be mounted on the dipstick with a sealed vacuum can located at the right side of the stick in the figure 20 a). This PCB can communicate with the master unit, Arduino, through the wiring in the hollow metallic pipe. At the end of this wire, a necessary number of connections are made to the Arduino to configure switching configuration.

Upon confirming the switching functionality under the liquid nitrogen temperature, the dipstick was taken to the workshop multiple times to make the necessary changes to support the long evolution experiment in a more electrically isolated environment. The later model of the dipstick can be seen in figure 20 b). From the PCB mounter to the connection to Arduino, changes are applied to (1)prepare multiple connectors such that all the interconnect layers are accessible by a voltage source and (2)create a pressure exhaust such that the vaporized Nitrogen can escape to the outside. Change (1) was easily accomplished by installing a flat ribbon cable between the PCB and the Arduino. The cable contains 25 conductive wires electrically isolated from each other which satisfies the number of connection path needed between the setups. Insulation-displacement connector and the female PCB header can give each male PCB pins an individual access to the unique cables, thus the required connections can be made for PCB, devices, as well as the Arduinos. Change (2) was realized as a consequence of an early stage try-out of an experiment. Initially, the dipstick was designed with a vacuum setup in the scope. The vacuum will seal the can which protects the PCB as well as all the electronics from being in direct contact with the liquid. However, the multiple changes in the hardware as well as the scope of the project worsened the viability of installing a vacuuming system in the setup. Without the vacuum, the sealing can could unexpectedly detach itself from the dipstick, exposing all the electronics in the liquid

a) b)

Figure 20: a)The initial model of the dipstick designed for the switch experiment. b) The final model of the dipstick. The hole has been drilled to the can and headpiece has been attached.

unprotected. The solution to this sealing can was met simply by drilling a hole to keep them connected using a screw. Another hole was drilled at the bottom of the can to allow a flow of liquid Nitrogen to touch the sample such that no atmosphere particles are present when cooling down. This leads to exposing the electronics to a liquid, yet the sealing can still protects the PCB and the samples from unwanted collisions when inserting/extracting the dipstick. This will produce a vaporized Nitrogen inside of the dipstick rather than the outside. Thus an escape path from the PCB to the outside of the vessel was necessary. Apart from the ribbon cable, the dipstick is made with a hollow tube which should be more than enough to ventilate the built-up pressure within the dipstick. However, due to the number of aluminium soldered electrical connection, as well as the presence of Arduino UNO, better option was to not expose the sensitive components of the experimental setup to a blast of pressure ventilation. This problem was solved by first filling the hollow space of the dipstick with a silicon paste to avoid the flow of gas, and then inserting an exhaust tube to directly connect the top of the hollow tube area to the atmosphere. Such measure allowed the airflow from the top of the hollow tube, where the nitrogen gas is expected to accumulate, to the atmosphere without having the electronics in contact with the gas. The simplified schematics of the inner component of the dipstick can be seen under figure 21.

4.2.6 Practicals: PCB development

The PCB used for the boolean logic experiment can support one device and eight electrical connections to the control unit. The interconnect experiment will accommodate a maximum of eight devices and sixty-four electrical connections, individually allocated for every electrode in the devices. Thus a new type of PCB had to be created to support such experiments. The upgraded PCB seen in figure 22 was originally developed by a previous student who performed an internship at NE lab[32].

The top layer can support the dopant chips just like boolean experiment PCB. The electrical connection to the bottom layer is bridged by the four connector units in the centre. The switching is done by the MAX395 IC chips of which its schematics and timing diagrams are shown in figure 23. The chip was chosen for low leakage current, fast switching time, availability of 8 switches,

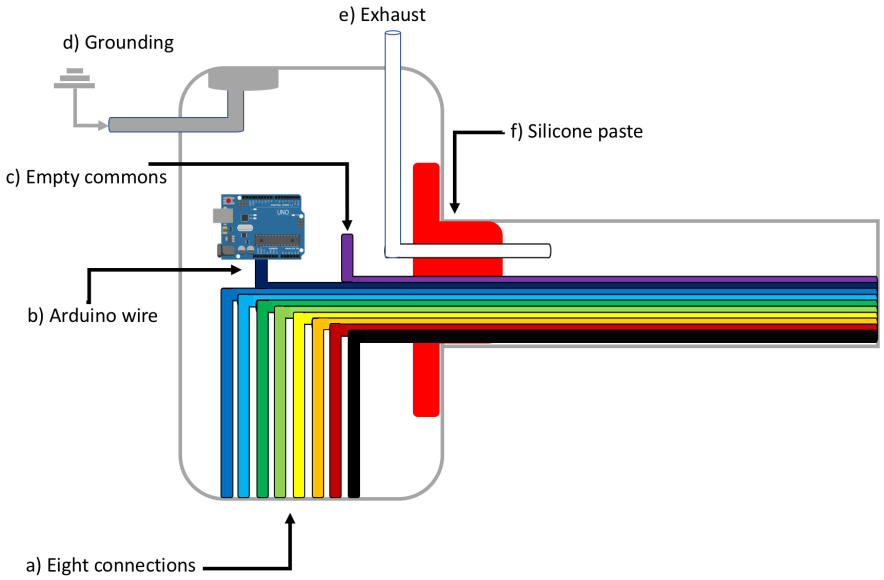
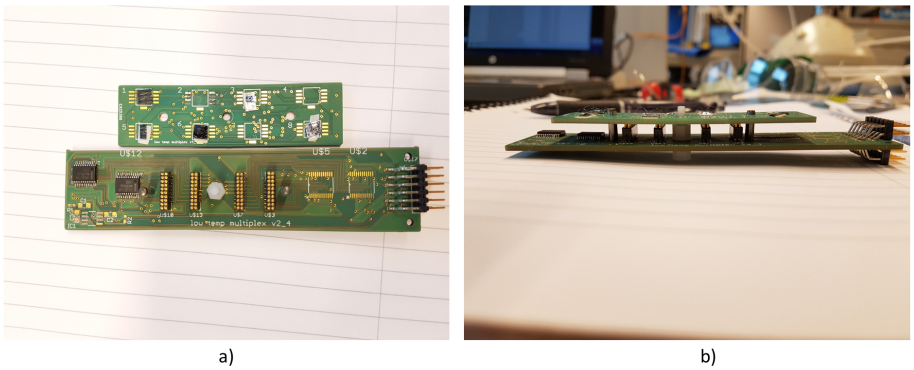


Figure 21: Simplified schematics of the top of the dipstick flat cables consist of a)eight signal line, b)Arduino signals and c)unused common lines. d)External grounding ensures the proper grounding. e)Exhaust line allows gas flow from the top of the hollow tube of which the flow to the electronic box is prevented by the f)red silicone paste. The size of the wires, headpart of the stick, as well as Arduino not up to the scale.



a) b)

Figure 22: The eight device PCB originally developed by Krishna.R and Celestine.L. The physical version has been finalized by Martin.S. a) Top view of the device layer and IC layer. b) sideview when mounted.

as well as their capability to be daisy chained for the purpose of serial data transfer. The working of these chips can be regarded as an 8-bit shift register. Each ICs are responsible for controlling eight switches on the board, thus the 8-bits information that is transferred can be representative of the eight switches. This data first arrives at the first IC. The data output of this IC is connected to the data input of the following IC, thus when the second 8-bit information is sent, the first set of information is transferred to the second IC, while the first IC welcomes the arriving second set of the information. The process is done using Serial to Peripheral Interface(SPI) method which synchronously operates with the clock signal that arrives at the SCK(clock signal) or SCLK pin of ICs. When the last set of 8-bit information is sent, the first set of information arrives at the last IC, thus the new switch configurations are in ready to be reflected. The rising edge of CS(Chip Select) signal will trigger the switch to change to a corresponding new state.

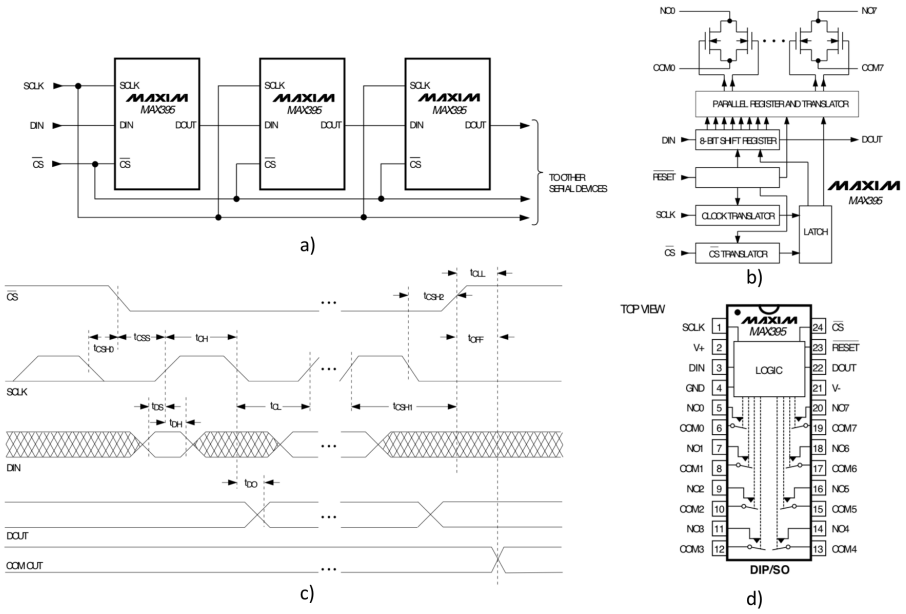


Figure 23: a)MAX395 chip in Daisy chain b)Functional diagram c)Timing diagram d)Pin configuration. Images taken from [34]

As such, every ICs have pins that are connected to the SCK, CS, and Din (and Dout) for the SPI protocol, V+, V-, GND for the power, and NO pins that contain the switches for the every electrodes. These separate signals are treated by independent pins from PCB as seen in figure 24. The pins with S label corresponds to the signal line, and C for the common line. For the requirement of the interconnect experiment, no common signals are necessary, thus all the C pins will not be used.

4.2.7 Practicals: Software development

The EIM requires both physical and computer domain in the cycle to maintain the evolutionary process. As such, the procedure to carry on all the experiment had to be written in Python 3.0 and Arduino. The coding language was chosen based on the preference of the BRAINS group members. Daisy chaining of ICs will allow transfer of 8-byte(64 bits) information, serially per byte. As such, from the software interface, the information must be sent to the data line one at a time. The switch configuration transfer from Arduino to PCB are done using SPI, thus the information is synchronized on both sender and receiver side. However, PC to Arduino communication are done asynchronously, thus both devices must be programmed appropriately to transmit data with no abruption. To put in detailed perspective, Arduino UNO operates at 16MHz which equals one

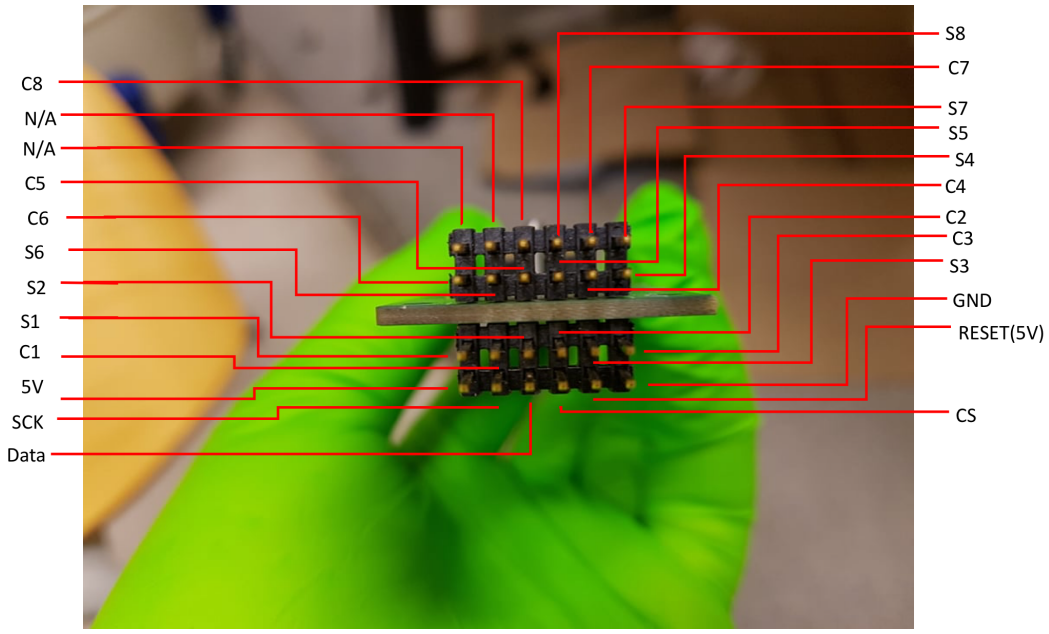


Figure 24: The sideview of the PCB in figure 22, shown with the labeling for each pins.

cycle or instructon every 62.5 nanoseconds. For serial communication with baudrate of 115200 (baud means bit per second), 14400 byte of information can be sent per second, or 1 byte per 70 microseconds. In the time it takes to transmit 1 byte of information over the serial line at 115200 baudrate, Arduino will execute approximately 1120 instructions. This requires some form of synchronization of Arduino and the incoming data to let Arduino know when all the data is there to be processed. The method used in this experiment will utilize the starting and ending marker to control the Arduino's data reading. Before sending the 8-byte information, PC first sends the starting marker character. This will trigger the readout function of the Arduino, thus the information sent after the starting marker will be stored in Arduino's buffer, but not before. When all the data is sent from PC, the end marker character is sent to finish the transmission process. Upon receiving this character, Arduino will go out of the readout state, thus can proceed to process the information. For the purpose of this experiment, < and > are used for starting and ending marker respectively. In theory, any characters that are not number nor comma can be used

Algorithm 2 Arduino algorithm for marker based receiving

```
    procedure RECEIVEDATA
2:      recvInProgress = False ← Boolean
        flag = False ← Boolean2
4:      rc ← received character
        while Data is available and flag is false do Assign the data to rc
6:          if rc is < then
                recvInProgress is True
8:          if recvInProgressis True then
                if rc is not > then
10:                 Store data in the buffer
                else
12:                 Terminate receiving
                    recvInProgress = False
14:                 flag = True
```

for the markers. This functionality is illustrated in a pseudo code 2. While the data is available to be read on the serial line, any detected character is read and stored in *rc* valuable. The reading process starts only when *recvInProgress* flag becomes true which is only possible if the received character is a starting marker, <. The process terminates when the received character is an ending marker, then the *recvInProgress* flag is reversed and *newData* flag becomes true to move out of the while loop.

Arduino receives information by individual characters. Suppose the 8-bit 11111111 is sent to Arduino in a byte as 255, Arduino buffer will not receive 8 1s nor 255 as a three digit number, but the character 2 followed by 5 and then another 5. To correctly reformat this into 255, data parsing has to be done on the Arduino side. strtok() function from C library can be used to parse the strings. Such function will split the set of strings into tokens which are sequences of characters separated by the delimiter parameter. The function will initialize the pointer at the first character within the temporary array which is copied from the Arduino buffer. Then continue down the buffer until the delimiter character is detected, and then tokenizes whatever set of characters are found until then. This is immediately followed by atoi() function which converts the string into an integer, the variables usable by SPI communication protocol, and then stored in the switcharray which will be used to send 8-byte information to the PCB.

Algorithm 3 Arduino algorithm separating data to bytes

```
    procedure PARSEDATA
        Strtok ← Temporary array of chars
3:      if flag is True then
            Collect the char from Strtok
            if char is "comma" then
6:              Tokenize the string
                Convert to integer
                Assign it to switcharray
```

Therefore, PC to Arduino interface requires no clock signal to synchronously treat data, but rather gives Arduino some initializing and ending token to inform the duration in which the informations are sent. Full set of C code used on Arduino for this experiment can be seen under the skyNEt github repository.

5 Result/Discussion

The result section will cover two different set of experiments; single dopant device characterization and darwin internet experiments. The single device characterization results were mostly covered in the mid term report, thus will be touched very minimally in this report. For the single chip containing multiple devices, the chip will be referred with two digit number where the 10^{th} bit refers to the column number and the 1^{st} bit refers to the row number with the bottom left device as 1 for both numbers. Furthermore, the electrodes will be numbered from 1 to 8 to identify them. From the upright point of view, the top electrode will be referred as electrode 1 and is labelled in the ascending order in the counter clock direction. This electrode labelling is also used for the internet experiments. Readers are encouraged to refer to the "practiclas:experimental procedure" section for the device number as well as matrix rows and columns descriptions.

5.1 The refined recipe IV characteristics

Previous dopant recipe by Jeroen et al.[3] left few challenges particularly in the reproduciblity as well as the yield per chip. Few changes were made to tackle these issues.

First change in the recipe is the shift from diffusion based doping to an ion implantation based doping. The thermal diffusion doping technique had lead to a formation of schottkey barrier at the interface between the silicon and the nano-electrode. This is a consequence from the large depth that must be etched in order to go below Mott concentration at the surface of the diffusion based devices. Using RIE as a post-etch process, over 100nm depth of etching was required to reach the Mott concentration at the silicon surface. Presence of the nano-electrodes resulted in uneven as well as unpredictable etching profile. Thus it was necessary to have "pre-etch" to etch away majority of the required etching depth, deposit EBL electrodes, and do minimal post-etch process. This tuning of the recipe, unfortunately, lead to many surfaces containing schottkey barrier as the surface concentration at the end of pre-etch was likely already below the Mott concentration. This schottkey barrier is an unwanted feature because not only it affects the performance of the device by imposing a large amount of surface resistance, but accurate characterization of the charge transport mechanism is hindered due to the measured resistance not being purely from the resistive dopant network. Ion implantation can overcome this by tuning the masking layer thickness and the implanting dosage to ensure the dopant concentration at the silcion surface is above the Mott concentration.

The second change in the fabrication protocol is made at the separation of the EBL electrodes. 200 nm diameter active region, in most case scenario, led to a short circuitting of neighbouring electrode under the room temperature measurement. This issue seem to have disappeared upon fabricating a device with 300 nm diameter, effectively increasing the electrode separation. However, whether this change had direct impact on the shorting of the electrodes is unexperimented.

The third change made was the use of Ti and Pd as the electrode for the Boron doped devices. Previously, Al were deposited as the nano-scale electrode for both Arsenic and Boron devices[3]. As the presence of schottkey barrier was a significant issue, reffering to the first change from the refined recipe, work function of the electrode metal would be more ideal if it's in vicinity to the energy level of the dopant in the silicon. Figure 25 a) shows the dopant energy level in the silicon band. As Si has a work function around 4.85 eV[36], Al, with work function of 4.20 eV[36], was not suitable for the shallow acceptor such as Boron because the charge carrier from the electrode will see a significant energy barrier in moving to the dopant energy level. Pd have much higher work function of 5.22 eV[36]. This is beneficial as its fermi level will be located below the fermi level of the Silicon, thus the majority carrier energy level will be in vicinity to the boron energy level. In practice, Ti have to be deposited first as a sticking layer, thus Pd layer will be deposited on top of thin Ti. This is illustrated in figure 25.

Figure 26 shows the room temperature resistance analysis of of the diffusion-based chip that

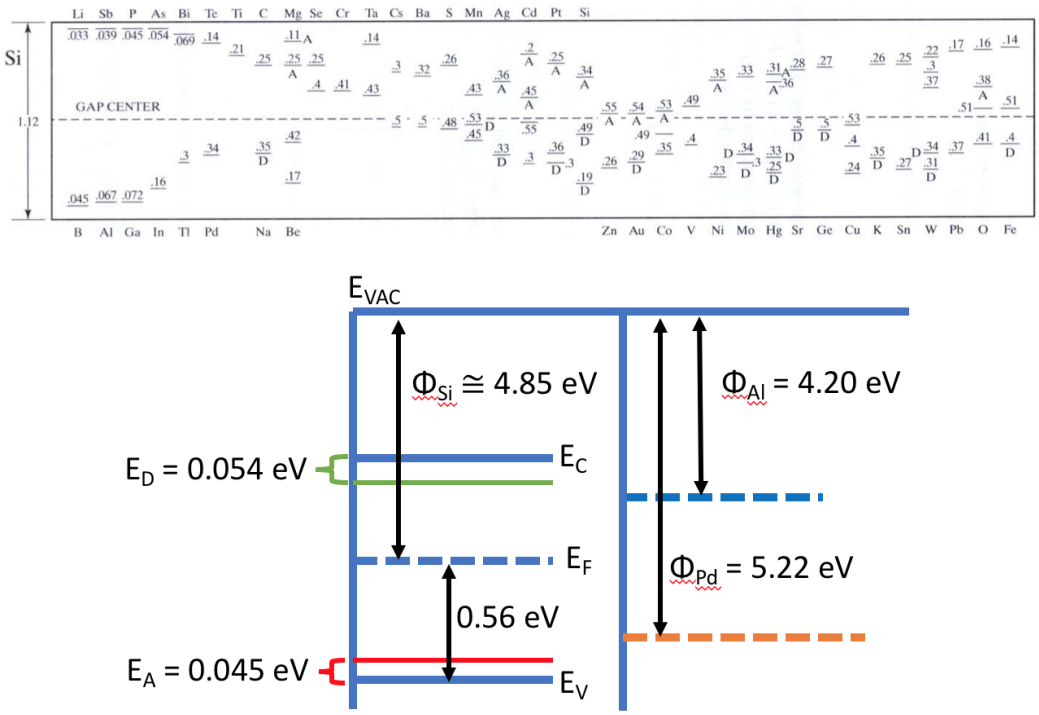


Figure 25: (top) Dopant energy levels within the Si bandgap, data(image) taken from [35]. (bottom) Illustration of the work function difference in relation to the dopant level.

has 300 nm diameter of Pd electrodes. The 5 by 5 box on the right indicates the chip status where the red is unmeasured or broken, while yellow has an inconsistent resistances as to the rest of the chpis. The unshaded box indicate chips with 8 unbroken electrodes. The resistances are also measured between the neighbouring electrodes. The recorded value is rounded down to the first whole number and plotted as a histogram on the left. Most of the resistance value falls into $4 \sim 7M\Omega$ region. As seen, this change alone already gives significant edge to previous recipe of Al electrodes with 200 nm diameter which had very low lower yield. This device unfortunately still suffers from the schottkey barrier which was experimentally measured by annealing the device at 150^oC for 10 minutes. This annealing induces diffusion of aluminium into the silicon and vice versa, thus reducing the contact resistance at the silicon-nanoelectrode interface. Majority of this chip's resistances were reduced into $10k \sim 100k\Omega$ regime, indicating that there was a large surface resistance, as expected from the diffusion based chip.

Figure 27 shows the the room temperature resistance of each neighbouring electrodes from individual devices on the implanted chip that has 300 nm diameter of Pd electrodes. The 4 by 4 box on the right indicates the whole second row have unusuable devices. However these were fabricated with different electrode designs, thus with regards to the total yield of the dopant devices, this design has achieved 100% yield. The large variance in the inter-electrode resistances show rather bad uniformity between the devices, however the resistance variation within the device is not large for most of the devices in the chip. This resistance variance between the chip is likely the result of the nonuniformity from the RIE process. Nevertheless, the ion implantation device show no schottkey barrier as the post annealing process resulted in minor, if not hardly any change in the neighbouring electrode resistances. Thus result here can be considered as a milestone for the reliable dopant chip fabrication.

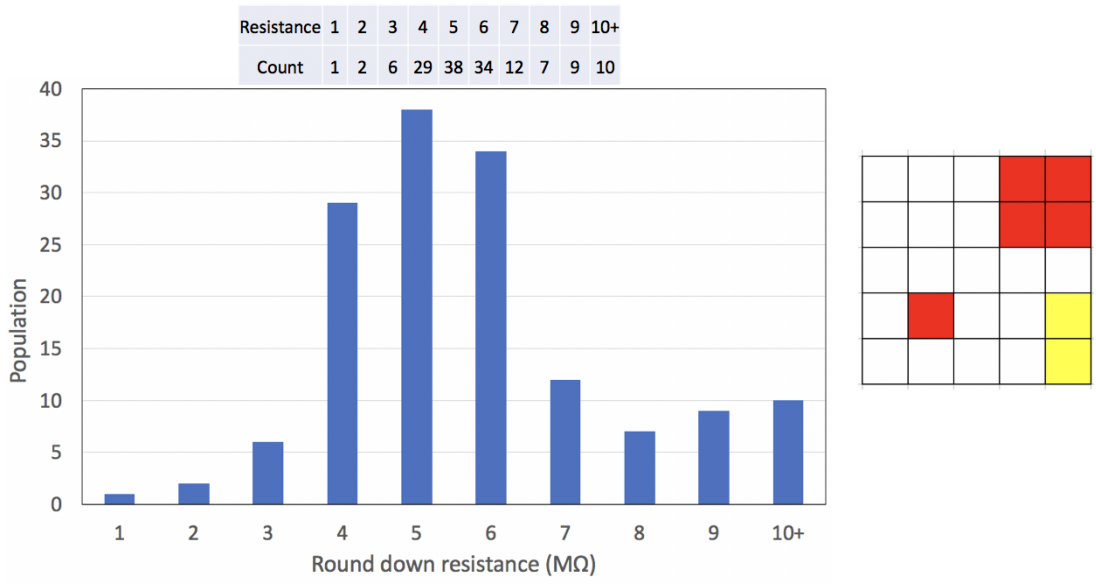


Figure 26: Thermal diffusion based Boron dopant chip with Pd electrodes of 300 nm diameters. (Inset)5 by 5 chip configuration with red as broken/unmeasured sample and yellow as a device with unusually high or low inter-electrode resistance in comparison to the rest of the chip. The histogram of the inter-electrode resistance with the counter at the top. Resistances are round down to the first digit

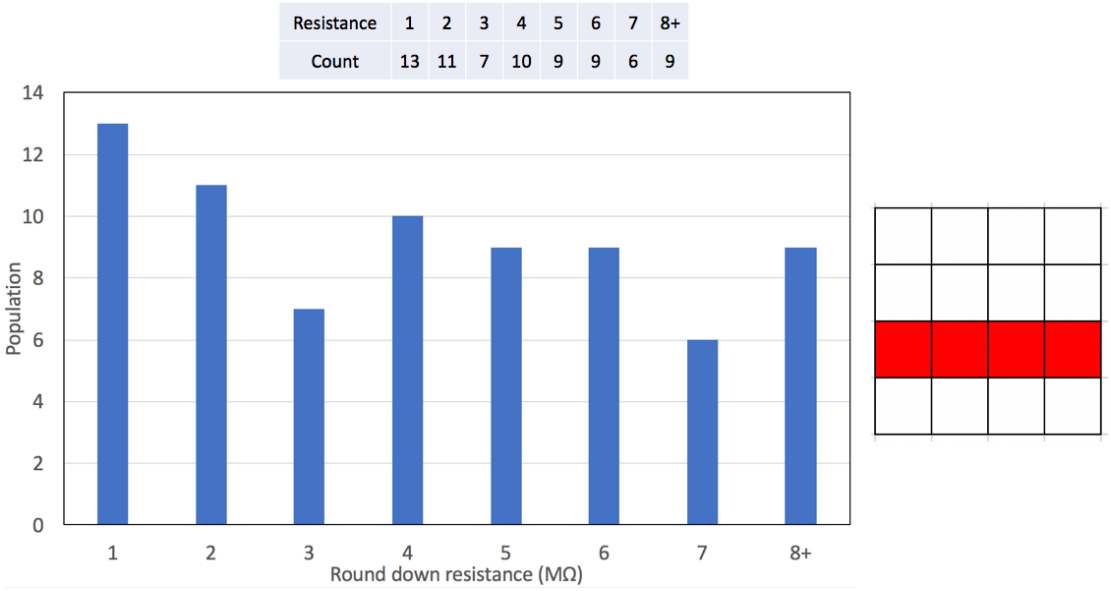


Figure 27: Ion implantation based Boron dopant chip with Pd electrodes of 300 nm diameters. (right)4 by 4 chip configuration with red as unusable chip. (left)The histogram of the inter-electrode resistance with the counter at the top. Resistances are round down to the first digit

5.2 Experimental Coulomb Gap

Referring to the theory section, coulomb gap can be experimentally shown with an IV relation at sufficiently low temperature. This non-linearity is an indicator of the unique input-output behaviour. The following result is obtained at 77K from the implanted chip of which its room temperature resistances were characterized in figure 27. For the discussion of the results, the threshold voltage will refer to the input voltage for $|I_{out}| = 1nA$. The results show clipping of the current at $I_{out} = 3.4nA$. This is the limitation from the Delft rack experimental set up, and does not indicate the vulnebility of the dopant device.

Figure 28 shows measured coulomb gap between each electrodes on device 14. The positive $V_{threshold}$ lies around 500 mV and the negative in the range of -500 to -1000 mV, depending on the electrode pair. The size of the coulomb gap shown here seems to not necessary reflect the resistances measured at the room temperature. This is derived by the fact that their room temperature resistances seem to have no linear relation to the size; the pair that have largest coulomb gap observed does not even have the highest room temperature resistance. It is possible that the room temperature resistance variance within device 14 ($\triangle R$ =700 $k\Omega$) is not large enough to show obvious variance in the coulomb gap at this temperature, or the variance is so minimal that the difference is hidden from the observed hysterisis.

However, figure 29 which shows the coloumb gap between each electrodes on device 33 may corelate the resistance at room temperature. The results here suffer even more from the hysterisis due to the speed of the measurement taken. However the positive $V_{threshold}$ is equal to or higher than 500 mV for all the pairs and negative $V_{threshold}$ is equal to or lower than - 1000 mV for all the pairs. This suggests that the coulomb gap is larger on this device than that of device 14. As this device have almost three times higher room temperature resistance than the device 14, this approximate increase in the coulomb gap can be related to the increased resistance which is likely due to the slightly deeper etching profile of doped silicon.

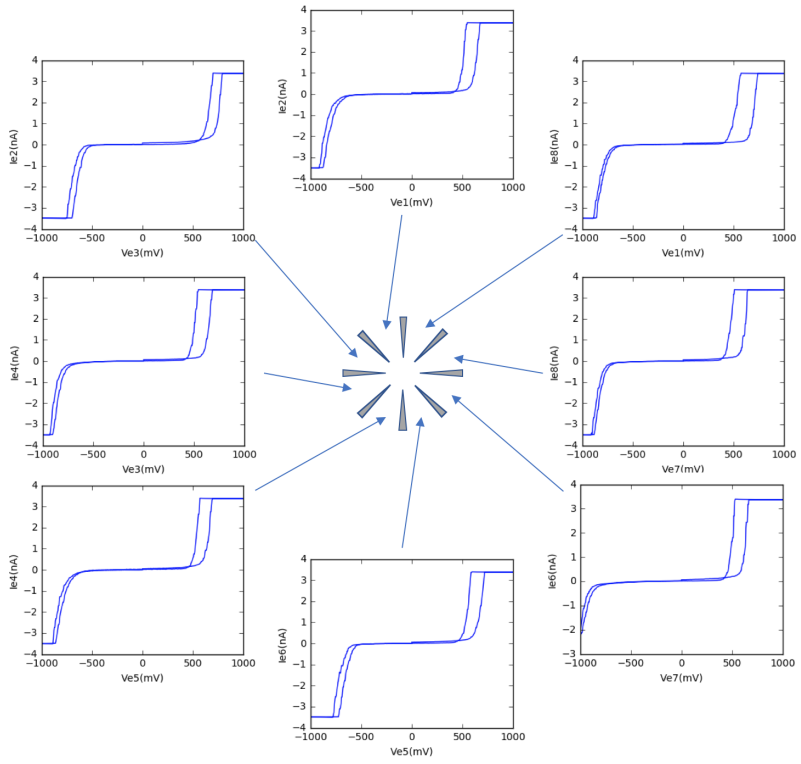


Figure 28: The IV curve in between the neighbouring electrodes of the device 14 at 77K. Coulomb gap of approximately 1200 mV is clearly observed.

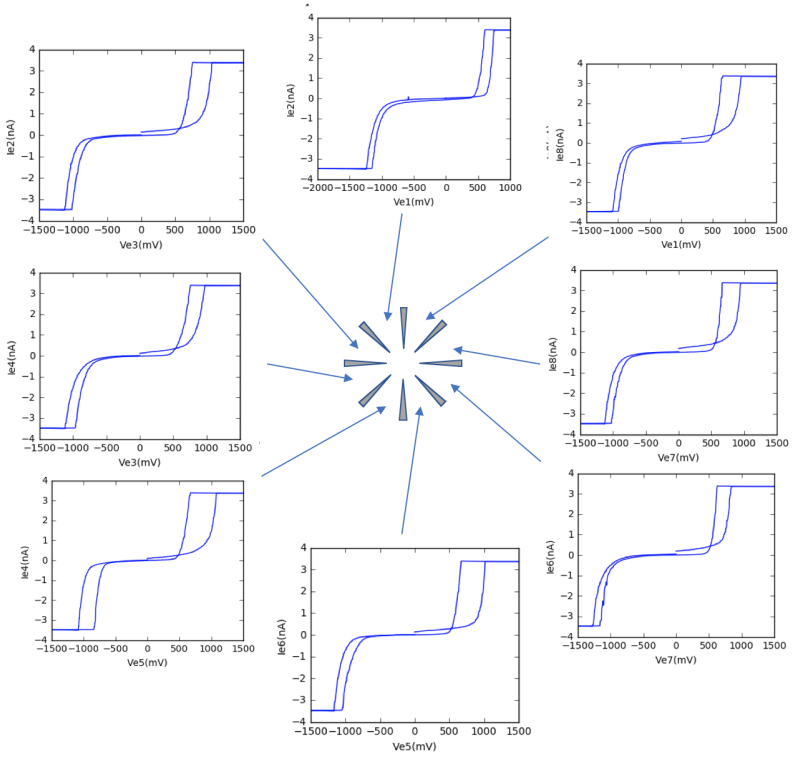


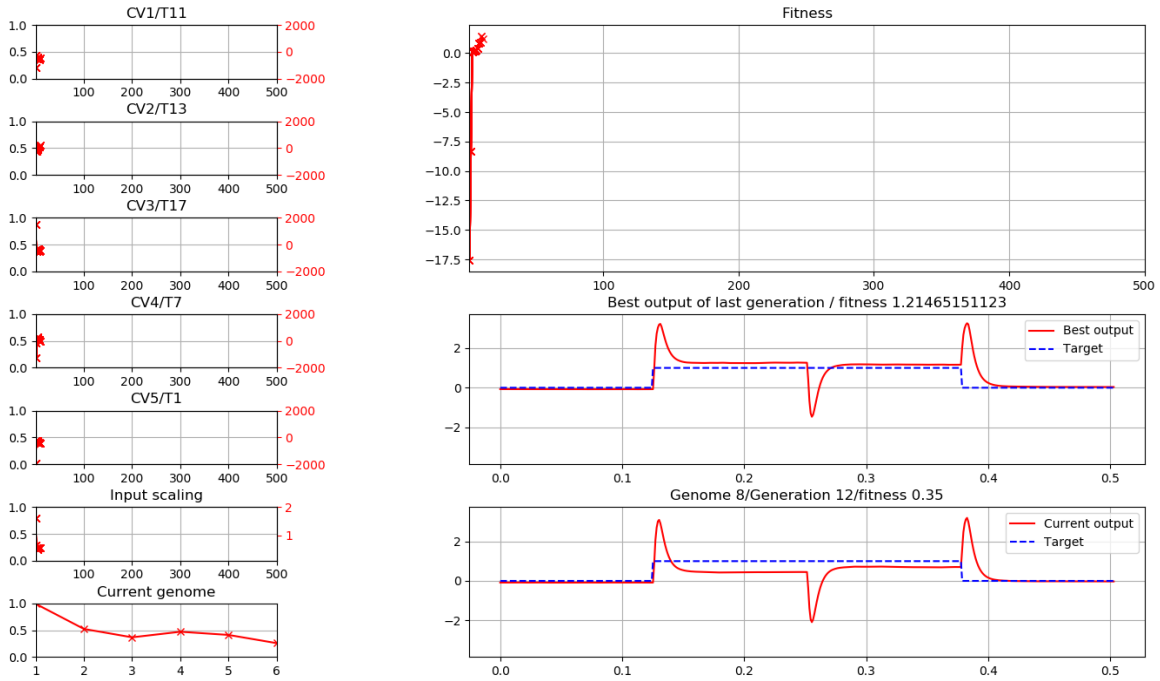
Figure 29: The IV curve in between the neighbouring electrodes of the device 33 at 77K. Coulomb gap of approximately 1500~1600 mV is observed. The result here is affected by hysterisis effect.

From these results, we may corelate the room temperature resistance to the coulomb gap at 77 K. While the relation is not sensitive to the in-device resistance variance of $\triangle R$ =1MΩ, the comparison to the device with significantly higher resistance does increase the coulomb gap. It may be of interest to relate the room temperature resistance or any recordable parameters to the size of the coulomb gap using mathematical means. However, such formulation is out of the scope for this thesis project, thus will be untreated.

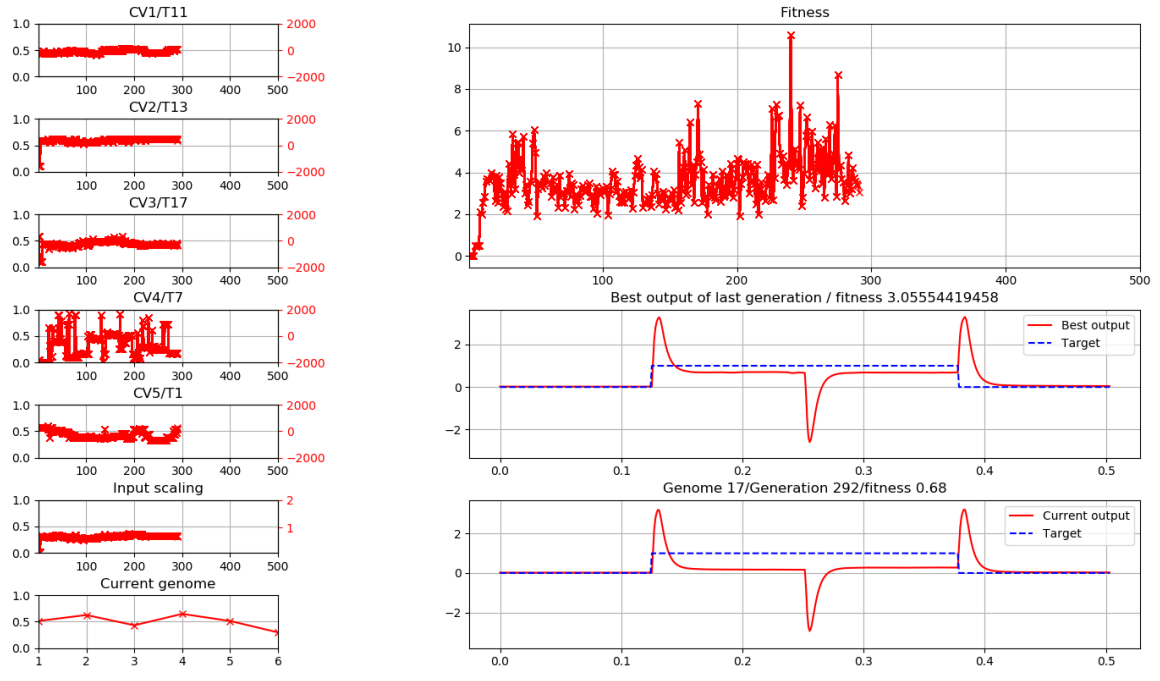
5.3 Boolean Logic: Boron

The following results are the boolean logic found on the boron implanted devices from the new logic search set up using the python script. Figure 30 shows XOR gate with the modified fitness function (which can be referred to the Experimental set up section). The weights of each parameters for the fitness calculation were set as $A = 1, B = 0, D = 0, \delta = 0.01$ and the fitness quality weight, C, was differentiated with 0 on the top result and 1 on the bottom result. The left column of the screen shot contains the evolution of the control voltages, labeled from -2000 to 2000 with the unit of mV, the input scaling which shows the input voltage in the unit of V, and the current genome tab which is used solely to monitor the process speed.

The right column contains the evolution of the calculated fitness with respect to the generations, best output of the last generation where the physical output is the red line and the desired output is the blue dot, and the result at the moment when the experiment was stopped. The graphs that show the output waveforms have x scale in the unit of seconds. The observed spikes at $t = 0.14, 0.26, 0.39$ seconds are due to the voltage transition as explained in the Experimental set up section. This is effectively ignored in the fitness calculation as the weight of the actual output in this spike duration is set to null. Both results show clear XOR behaviour with or without the fitness quality in consideration. In the run with C = 1, three out of five control voltages as well as the input voltage have saturated at the earlier stage. This most likely correlates to the generation around 20 in which the $F = 4$ had been reached, and the large fluctuation of fitness follows the remaining of the search history. The rapid spike of fitness score, only to return to the previous value in the next generation, should not happen as GA should maintain the improvement in the fitness score. This inconsistency was due to the fault at the python code to carry on the selection/recombination process. Currently, the issue is already solved thanks to the work by another members of BRAINS group. However the result shown here does still take into account of this unoptimised procedures. C = 0 result had achieved XOR at much earlier generation than C = 1 result. This may be due to the fact that putting equal weight on the fitness quality to the standard fitness calculation parameter resulted in more strict definition of the fitness. However, conclusion here seems to be that this device had no difficulty in providing XOR result regardless of the fitness restriction we chose. The fitness score parameters were tested only on the XOR gate result. The remaining boolean logic results were obtained using C = 1. Unfortunately XNOR gate was not found with the boron implanted device, however the rest of the boolean logic shows decent fitness score values. Nevertheless, boolean logic on the boron based device had been thoroughly achieved with in the BRAINS group. As such, the discussion shall be omitted. The obtained boolean logic will be included in the Appendix.



a)



b)

Figure 30: XOR search result for a) fitness calculation with C = 0, b fitness calculation with C = 1. The different duration of fitness search likely had no effect in the result as they both found XOR at much early generations.

5.4 Boolean Logic: Arsenic

Boolean logic can also be found with the arsenic dopant device. Though boron and arsenic are two different elements, they should behave similarly under low temperature as they both become a simple dopant island for the charge carriers to reside on. Figure 31 shows the boolean logic result obtained from Arsenic implanted device at 77K with their fitness score F. The fabricated chip had over 50% device yield and has Al electrode deposited with 300 nm gap. The result seen here is obtained using the formally utilized LabView GA program. Thus the unmodified version of the fitness formula is used. The grey dots are the recorded current values, and the blue lines are the fitting done by the software. Here almost all the logic gates are found apart from the OR which is considered as an easier gate than the other boolean logic. The variation in the fitness score suggests device dependent easiness in finding a particular logic, as XNOR is considered difficult logic gate to be found, yet this device managed to achieve XNOR and saturate in the fitness score as early as the approximately 200th generation.

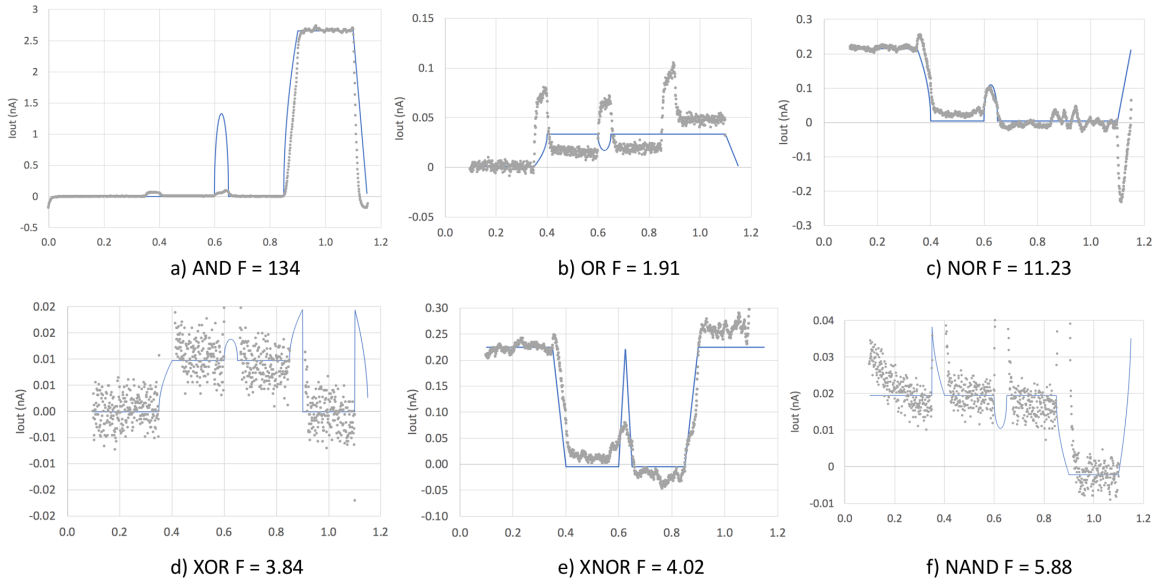


Figure 31: Arsenic boolean logic gates with their respective fitness score: a)AND b)OR c)NOR d)XOR e)XNOR f)NAND

While not all the gates were sufficiently obtained by the arsenic device at 77K, it is very likely that it is only a matter of trial and error until the “champion device” which can find all 6 boolean logic with sufficient fitness score will be found. Unfortunately, the CNOT gate was found in neither boron nor arsenic device. It is possible that the current way of implementing fitness formula is not optimised to find such a goal. The typical GA result from the CNOT experiment had ended with a perfect follower and no XOR gate. So long as a finite non-zero value weight is given to the follower output, which is perhaps one of the easiest functionality to find, the GA will continue to enjoy the high number of score obtained from the follower since it is not difficult to obtain a perfectly matching curve to the input. Future experiment to obtain CNOT gate may need to implement another way to put more weight on acquiring XOR gate.

5.5 Darwin Internet: Processing time analysis

The rudimental version of the GA set up for the interconnectivity experiment was highly unoptimised. The initial attempt in the full search experiment resulted in a gradual slowing of the process, especially during the instructions which involved Arduino. Figure 32 shows the process time analysis that was taken during the six-device full search. Four graphs show the time it took to process each procedure per genome. Conversion refers to the duration in which Computer converted the switch configuration into 8 bytes, followed by conversion 8 strings which are the readable type of value for the Arduino. Array is a time it took for the Arduino to reflect the genome into physical switches. Outputevaluation time is a time it took to measure the output current from every output port, sourcing from every input. Lastly, the fitness calculation time is the time it took the computer to calculate the fitness score using the output array generated during the output evaluation time. From the graph, the instructions that involve updating switch configuration gradually increased the processing time. This had resulted in some faulty switch updating where it will not send all 8 bytes for switching. This is necessary even if the change in the switch configuration involved only 1 byte due to the daisy-chained ICs. Thus leading to incorrect output data for some of the full search result taken.

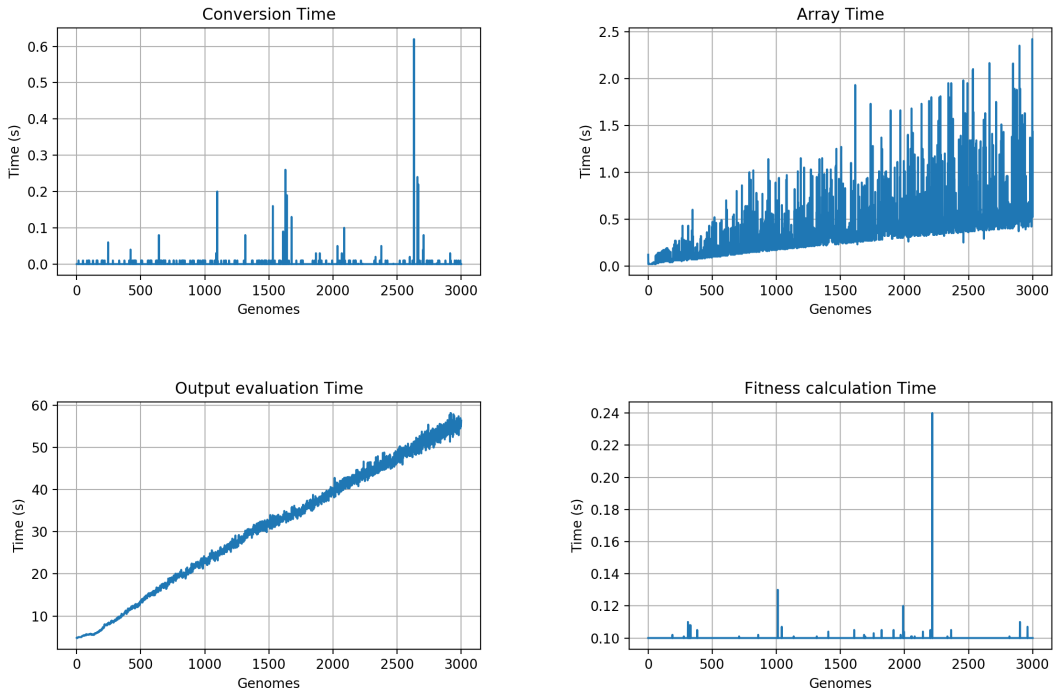


Figure 32: The analysis of the processing time of the six-device full search prior to the code modification.

This slowing down was eliminated simply by adding few print-lines to the full search code written in python. The Arduino code contains a function to print the values that are sent to the PCB. Arduino Code:

```
void showParsedData() {
    Serial.print("Number:");
    Serial.print(String(switcharray[0]));
    Serial.print(" ");
    Serial.print("Number:");
    Serial.print(String(switcharray[1]));
```

```
    Serial.print(" ");
    ...
```

Python Code:

```
receivemessage = ser.readline()
receivemessage = receivemessage.strip()
receivemessage = receivemessage.split()

#Print out the message received from Arduino
print(receivemessage)
```

The printed messages are received by the PC, then processed such that it can be printed in one line, and finally shows all the 8 bytes that are processed by Arduino. As it turns out that these lines on the python code a bigger role than just for a debugging as seen by the processing time analysis of the 8 device full search which incorporated these changes, as seen in figure 33. The inrementing processing time seen in figure32 had disappeared since adding these lines. Although there is still slight variation in the process times, it is very negligible and does not indicate any degraded performance over the long experiment.

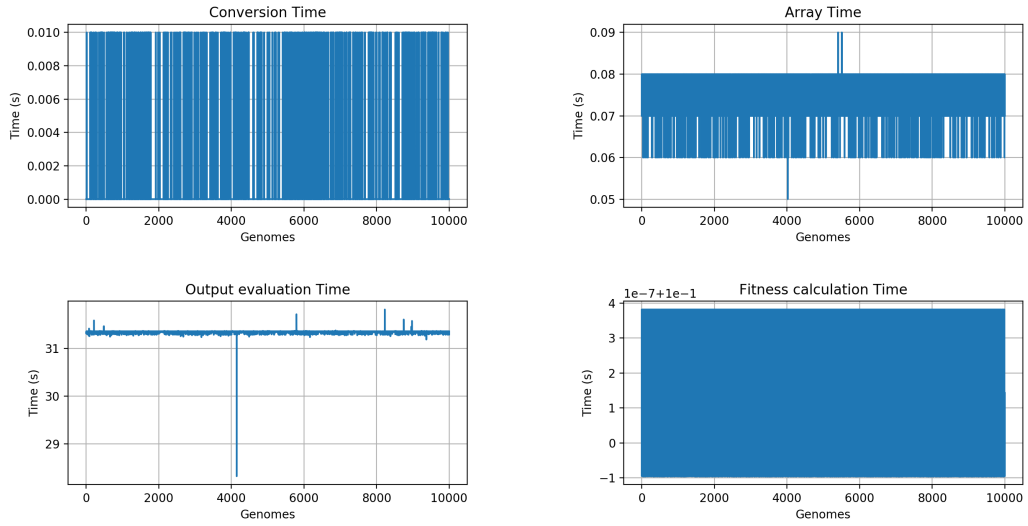


Figure 33: The analysis of the processing time of eight-device full search

The exact mechanism of how this change affected the Arduino is uncertain. The likely scenario is that if a message printed form Arduino is not read by the PC (or any master unit), the Arduino buffer stores this unread messages, filling up the buffer, thus leading to a delay in the operation speed due to a memory issue. While it may be possible to test this by running a long full search without printing, as the finiteness of the buffer storage should lead to a saturation in the processing speed at the slowest operation allowed, such experiment will be disregarded here since it's not of the concern of this thesis. Most important finding from this change and the resulting time analysis is that the processing time of the internet experiment is now sub-optimised, and can be used for a long duration experiment without running into a delayed operation. And this is also true regardless of the scale of the experiment. Figure 34 shows three-device full search. In comparison to figure 33, all four instructions have constant processing time, of which three are similar between the three and seven device results. Output evaluation time is different between these results since one has to process more than forty extra switch configurations to evaluate the current from all the outputs.

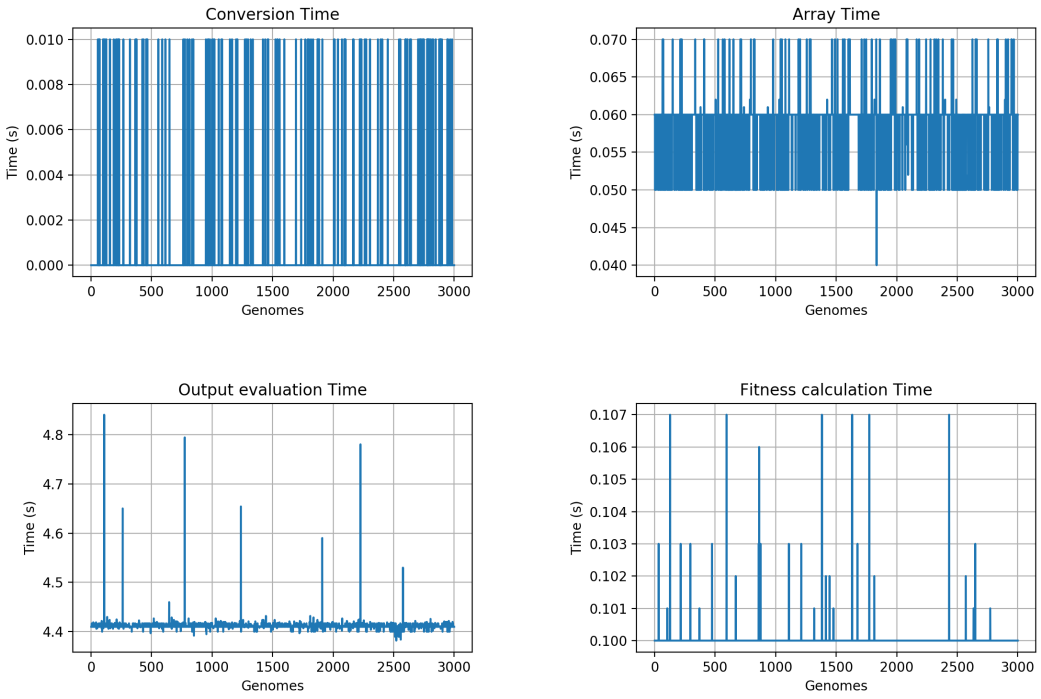


Figure 34: The analysis of the processing time of three-device full search

5.6 Three-Device Full Search

The optimised GA code from the previous section should allow much more diverse switch configuration to be tested. Naturally, the next question should be can it lead to a diverse result, how abundant the goal functionalities are. Interconnectivity experiment with two devices would have $2^{2*8} = 65536 \approx 10^{4.8}$ configurations to experiment with. However, the configuration reduction explained in the experimental set up section reduces the number of configuration to be tested to 2048. While this does not necessary mean the intelligence of the two-device system sis low, the experiment is rather trivial to test the scalability of the dopant device. As such, for a small number full search, the three-device system was experimented. The similar method of the calculation gives 163840($\approx 10^{5.2}$) legitimate configurations to be tested for the three-device system. Figure 35 shows the histogram of fitness score from the 3000 genomes three-device full search result with a tolerance factor of 0.8. The legend provides the actual number of the said scores from the histogram.

Referring to the method of fitnss score calculation, 18 will be the highest fitness score achievable by the three-device system. Thus 1361 genomes having the fitness score of 18 should indicate high number of successful classification. However, the unique input-output relationship, required for the classification, should be read from the success rate score. Figure 36 shows the histogram of the unique input-output relations from the 3000 genomes three-device full search result with a same tolerance factor as 35.

The graph suggests that the majority of the population are one and two classification. A significant argument can be made against the difference between the fitness score and the actual classification success rate. For having the highest population for the highest fitness score, the population of the maximum classification is very low. It is most likely because the current method of the fitness calculation does not take into account of the relation between the row-wise highest and the column-wise highest. To bring a practical example, genome 159 had the highest fitness

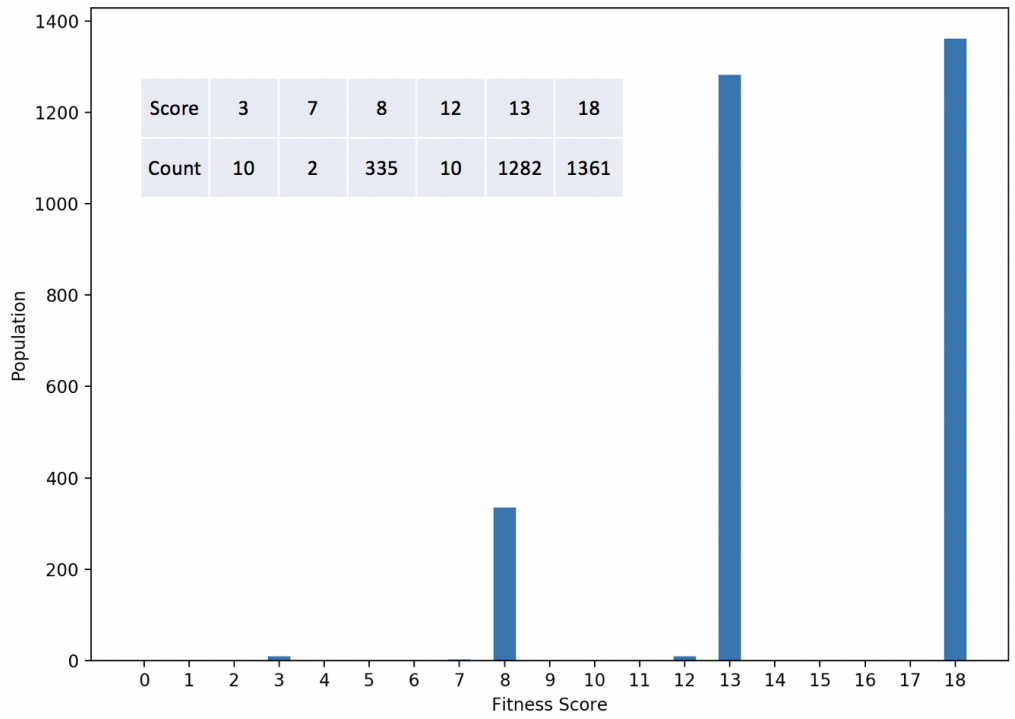


Figure 35: The Fitness score histogram of three-device full search with a counter in the legend

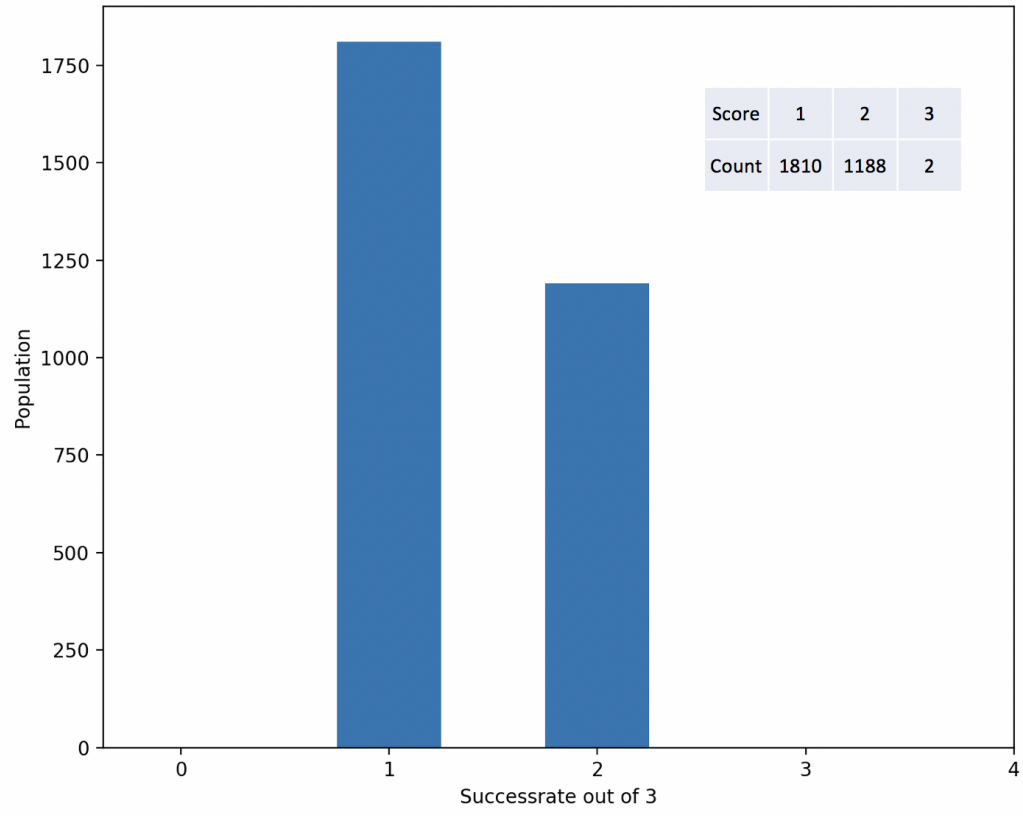


Figure 36: Success rate histogram of three-device full search with a counter in the legend

score of 18 but the success number of 2, with following output current array:

$$I_{159}(nA) = \begin{bmatrix} 4.506456 & 0.1221452 & 0.6901869 \\ 0.2958907 & 0.2416044 & 1.327142 \\ 1.253825 & 0.4055627 & 20.56491 \end{bmatrix}$$

The coulor labels as well as the format of the array follows the one shown in the experimental setups chapter; Yellow is the row-wise highest current, green is the column-wise highest current, and orange satisfies both. With a quick inspection, it can be seen that the highest value from each row and columns are the only HIGHs from their respective units if the tolerance = 0.8. However, the highest value from the row 2, 1.327142 nA, is completely disregarded in the column evaluation because the row 3 of the same column has much higher value. Because of this, permutation matrix could not be obtained, thus resulting in the excellent fitness score, but not a successful classification.

Nevertheless, if the output array had a maximum fitness value with the highest success number, both dependent on N_C, then a system can distinguish unique input-output relation with a clearly defined HIGH and LOW values of the output. With that considered, there are 2 switch configuration from three-device full search that had a success rate of 3 with fitness of 18, genome 360 and 1117. Their output arrays are:

$$I_{360}(nA) = \begin{bmatrix} 3.936 & 0.085 & 0.086 \\ 0.075 & 0.247 & 0.033 \\ 0.066 & 0.078 & 16.844 \end{bmatrix}$$

$$I_{1117}(nA) = \begin{bmatrix} 4.674 & 0.143 & 0.456 \\ 0.119 & 0.263 & 0.129 \\ 1.770 & 0.177 & 18.605 \end{bmatrix}$$

which seem to satisfy the unique input-output relation. The obtained output array is not a permutation matrix, but the identity matrix. The identity matrix is also a trivial result because the $I^{AB}_{out}; A = B$ suggests that the source layer and the sensor layer are connected to the same device. This scenario should be rather easy to obtain because it can be simply found by setting majority of the switches to OFF, thus making no interconnection. For this reason, the identity matrix should not be regarded as a result obtained due to the power of interconnectivity between the devices. With above concern, following 8 by 8 array W_x show their switch configuration for x is their genome number:

$$W_{360} = \begin{bmatrix} 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \end{bmatrix} \quad W_{1117} = \begin{bmatrix} 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 1&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0 \\ 1&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&0&0 \end{bmatrix}$$

For this full search result, devices were located in the slot 1, 3, and 6. Thus the column 2,4,5,7,8 will have no 1's due to the absence of the device, and row 1 and 5 will have no 1's since they're

used for the input and output. The switch configuration for the two genomes, as expected, have most of the relevant switches turned OFF. The most successful results obtained from tolerance = 0.8, are rather weak results due to their uninteresting switch configuration, and most importantly their output being identity matrix and not permutation matrix.

5.7 Eight-device Full Search

One of the advantage of the multiple device systems is that the switch configuration increases very rapidly with the number of the devices. With the maximum number of devices allowed on the PCB, number of possible configuration for the full search is $2^{8*8-2*2} * \frac{2^8-8}{2^8} = 1.17 * 10^{18} \approx 10^{41.6}$. This configuration, even with the potential output degeneracy, is likely to retain astronomical magnitude of the number. With that in consideration, genome number of the eight-device full search is changed to 7000.

However, this increase may have not been enough to compensate for the increase in the search landscape of the full search. Figure 37 shows the fitness score population of the full search. The graph excludes fitness score of less than 0 but it is included in the counter chart on the bottom. This score is due to the failure to achieve the single HIGH output per output row which results in the subtraction of the fitness score scaled with the number of the undistinguishable outputs. So if all eight output port had a very close value of the output current, fitness score will be subtracted by -8. This can result in a rapid decrease of the fitness score and can produce high number of negative score genomes as seen in the table. The result shows two genomes, 3724 and 4768,have achieved the highest obtained fitness score for the eight-device system, 48.

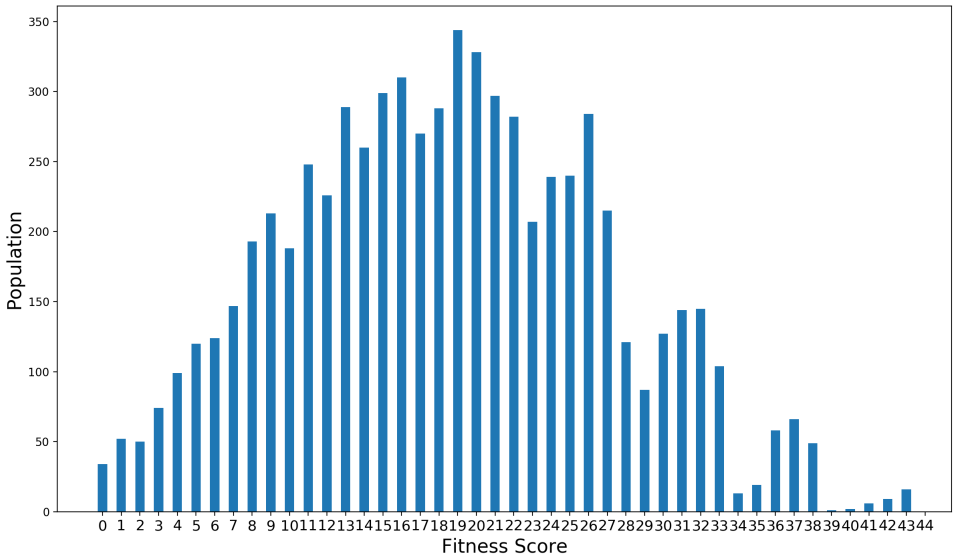
$$I_{3724}(nA) = \begin{bmatrix} 4.528 & 0.515 & 0.301 & 1.131 & 0.498 & 0.299 & 0.919 & 1.105 \\ 0.509 & 1.728 & 0.166 & 0.349 & 0.201 & 0.232 & 0.455 & 0.551 \\ 0.966 & 0.537 & 0.382 & 0.235 & 0.270 & 0.146 & 0.566 & 0.448 \\ 1.533 & 0.246 & 0.608 & 3.073 & 0.596 & 0.563 & 0.496 & 0.556 \\ 0.293 & 0.118 & 0.070 & 0.165 & 3.499 & 0.276 & 0.395 & 0.343 \\ 0.318 & 0.135 & 0.089 & 0.123 & 0.182 & 10.742 & 0.504 & 0.268 \\ 0.934 & 0.491 & 0.341 & 0.322 & 0.356 & 0.364 & 1.358 & 0.501 \\ 0.399 & 0.287 & 0.227 & 0.248 & 0.274 & 0.256 & 0.361 & 0.681 \end{bmatrix}$$

$$I_{4768}(nA) = \begin{bmatrix} 4.754 & 0.399 & 0.312 & 0.208 & 1.695 & 0.607 & 0.414 & 0.327 \\ 1.349 & 2.392 & 0.431 & 0.231 & 1.403 & 0.668 & 0.601 & 0.443 \\ 1.519 & 0.767 & 0.804 & 0.485 & 0.737 & 0.872 & 0.726 & 1.024 \\ 0.760 & 0.295 & 0.373 & 3.373 & 0.379 & 1.332 & 0.400 & 0.381 \\ 1.438 & 0.916 & 0.077 & 0.703 & 4.682 & 2.229 & 0.720 & 0.539 \\ 0.480 & 0.284 & 0.194 & 0.366 & 0.413 & 13.339 & 0.891 & 0.573 \\ 0.416 & 0.242 & 0.172 & 0.253 & 0.239 & 0.471 & 1.350 & 0.456 \\ 0.383 & 0.279 & 0.219 & 0.250 & 0.241 & 0.422 & 0.339 & 0.670 \end{bmatrix}$$

Unfortunately both results do not have much difference from identity matrix as the items that count towards successful classification are all along the diagnola of the matrix. This comes surprising as neither switch configurations are more populated by unconnected switches as seeen below.

$$W_{3724} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \quad W_{4768} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 \end{bmatrix}$$

More crucial information from the two genomes with the highest fitness score is that neither seem to have full classification, success = 8. This can also be seen from figure 38. Approximately



Fitness	<-1	0	1	2	3	4	5	6	7	8	9	10
Count	111	34	52	50	74	99	120	124	147	193	213	188
Fitness	11	12	13	14	15	16	17	18	19	20	21	X
Count	248	226	289	260	299	310	270	288	344	328	297	X
Fitness	22	23	24	25	26	27	28	29	30	31	32	33
Count	282	207	239	240	284	215	121a	87	127	144	145	104
Fitness	34	35	36	37	38	39	40	41	42	43	48	X
Count	13	19	58	66	49	1	2	6	9	16	2	X

Figure 37: (top)Fitness score graph of the eight-device full search. Scores below -1 are disregarded in the graph, but included in the (bottom)counter.

75% of the genomes have managed to classify over half of the maximum input numbers yet none have achieved all 8 classifications. The highest fitness score amongst the 181 genomes that have success = 7 is 43, obtained by genome 887. Below are the output array as well as the switch configuration of the said genome. Unfortunately, the most successful genome with the highest fitness score also seem to have an output that resembles identity matrix.

$$I_{887}(nA) = \begin{bmatrix} 4.941 & 0.319 & 0.077 & 0.309 & 0.072 & 0.222 & 0.156 & 0.429 \\ 0.868 & 2.546 & 0.159 & 0.750 & 0.172 & 0.278 & 0.222 & 0.344 \\ 0.822 & 0.816 & 0.315 & 1.479 & 0.323 & 0.318 & 0.234 & 0.467 \\ 0.280 & 0.521 & 0.215 & 3.029 & 0.138 & 0.197 & 0.164 & 0.298 \\ 0.983 & 0.487 & 0.107 & 0.335 & 2.730 & 0.355 & 0.154 & 0.151 \\ 0.335 & 0.130 & 0.079 & 0.088 & 0.232 & 11.136 & 0.468 & 0.211 \\ 0.644 & 0.269 & 0.175 & 0.166 & 0.211 & 0.216 & 1.321 & 0.294 \\ 0.478 & 0.253 & 0.175 & 0.166 & 0.140 & 0.149 & 0.183 & 0.679 \end{bmatrix} \quad W_{887} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

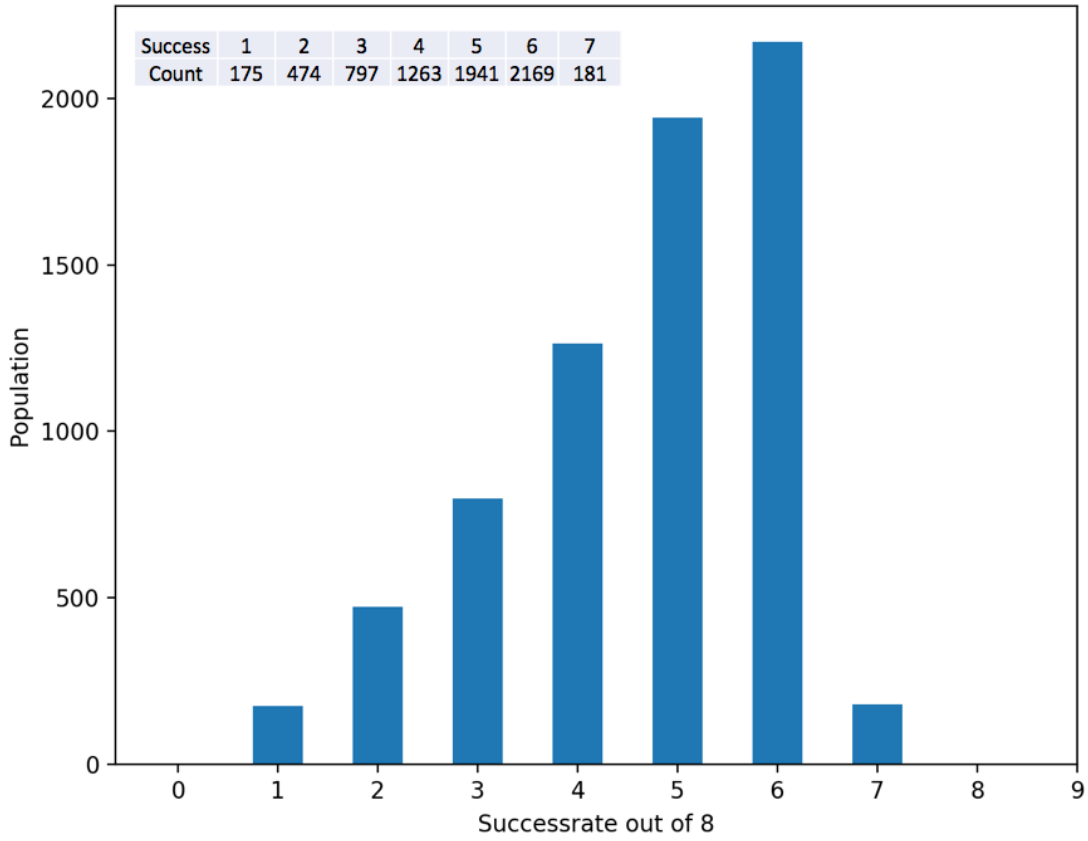


Figure 38: Success rate out of 8. No genomes have managed to classify all 8 inputs

The apparent conclusion that could be drawn from the three and eight device full search result is that high scoring switch configurations tend to result in the identity matrix. This was intuitively expected result as it's plausible that the output from a device would be highest when input is applied to that same device. However, the goal of this one-to-one full search is to find a permutation matrix which can be a strong argument for using interconnectivity as a parameter to utilize in the GA search. Out of 181 genomes which had a success rate of 7, six genomes had not all of their classification lying along the diagonal of the output array. Their switch configuration as well as an output array are as followed:

$$I_{103}(nA) = \begin{bmatrix} 6.898 & 0.287 & 0.146 & 0.270 & 0.522 & 0.424 & 0.559 & 0.606 \\ 0.868 & 2.865 & 0.200 & 0.314 & 0.578 & 0.525 & 0.611 & 0.729 \\ 0.885 & 0.672 & 0.475 & 0.918 & 1.243 & 0.945 & 1.062 & 1.317 \\ 0.383 & 0.134 & 0.254 & 2.243 & 0.375 & 0.177 & 0.418 & 0.263 \\ 1.381 & 0.783 & 0.154 & 0.889 & 4.445 & 0.270 & 0.421 & 0.382 \\ 0.341 & 0.147 & 0.079 & 0.244 & 0.199 & 11.048 & 0.539 & 0.237 \\ 1.218 & 0.578 & 0.490 & 0.573 & 0.594 & 0.542 & 1.414 & 0.588 \\ 0.488 & 0.322 & 0.252 & 0.318 & 0.317 & 0.273 & 0.322 & 0.725 \end{bmatrix} W_{103} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$I_{2633}(nA) = \begin{bmatrix} 6.180 & 0.534 & 0.307 & 0.399 & 1.994 & 0.647 & 0.521 & 0.895 \\ 0.972 & 2.302 & 0.279 & 0.649 & 1.735 & 0.842 & 0.762 & 1.151 \\ 0.976 & 0.657 & 0.505 & 0.797 & 1.070 & 0.806 & 0.771 & 1.187 \\ 0.236 & 0.108 & 0.062 & 2.476 & 0.440 & 0.154 & 0.185 & 0.282 \\ 1.639 & 0.709 & 0.318 & 0.339 & 3.280 & 0.346 & 0.282 & 0.744 \\ 0.385 & 0.147 & 0.082 & 0.134 & 0.187 & 11.227 & 0.443 & 0.255 \\ 0.767 & 0.373 & 0.227 & 0.244 & 0.257 & 0.245 & 1.367 & 0.438 \\ 0.459 & 0.352 & 0.287 & 0.282 & 0.391 & 0.243 & 0.314 & 0.656 \end{bmatrix} W_{2633} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$I_{6055}(nA) = \begin{bmatrix} 5.445 & 0.519 & 0.293 & 0.442 & 0.534 & 2.749 & 0.998 & 1.216 \\ 0.865 & 2.032 & 0.240 & 0.459 & 0.569 & 1.906 & 0.844 & 1.132 \\ 1.214 & 0.695 & 0.502 & 0.572 & 0.667 & 0.819 & 0.701 & 1.254 \\ 0.469 & 0.287 & 0.173 & 2.488 & 0.255 & 0.647 & 0.307 & 0.372 \\ 0.402 & 0.184 & 0.125 & 0.175 & 3.347 & 0.287 & 0.233 & 0.312 \\ 1.298 & 0.591 & 0.369 & 0.430 & 0.436 & 10.119 & 1.043 & 0.726 \\ 0.724 & 0.523 & 0.400 & 0.476 & 0.626 & 0.950 & 1.575 & 0.840 \\ 0.436 & 0.365 & 0.276 & 0.317 & 0.343 & 0.665 & 0.573 & 0.811 \end{bmatrix} W_{6055} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix}$$

$$I_{6136}(nA) = \begin{bmatrix} 3.683 & 0.148 & 0.043 & 0.091 & 0.239 & 0.235 & 0.133 & 0.234 \\ 1.469 & 2.015 & 0.174 & 0.184 & 0.694 & 0.955 & 0.385 & 0.660 \\ 1.338 & 0.835 & 0.573 & 0.806 & 1.618 & 1.497 & 0.893 & 1.663 \\ 0.277 & 0.137 & 0.055 & 1.919 & 0.287 & 0.270 & 0.214 & 0.283 \\ 1.201 & 0.450 & 0.273 & 0.334 & 3.748 & 0.663 & 0.472 & 0.829 \\ 0.356 & 0.250 & 0.191 & 0.236 & 0.347 & 13.226 & 0.772 & 0.420 \\ 0.722 & 0.290 & 0.192 & 0.460 & 0.413 & 0.434 & 1.359 & 0.600 \\ 0.958 & 0.508 & 0.361 & 0.404 & 0.485 & 0.486 & 0.437 & 0.743 \end{bmatrix} W_{6136} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}$$

$$I_{6321}(nA) = \begin{bmatrix} 4.814 & 0.241 & 0.107 & 0.145 & 0.167 & 0.349 & 0.390 & 0.430 \\ 1.250 & 2.478 & 0.248 & 0.358 & 0.513 & 0.686 & 0.576 & 1.137 \\ 1.397 & 0.994 & 0.608 & 0.807 & 0.528 & 0.926 & 0.882 & 1.453 \\ 0.210 & 0.229 & 0.112 & 2.552 & 0.119 & 0.263 & 0.326 & 0.630 \\ 0.312 & 0.121 & 0.074 & 0.113 & 3.010 & 0.157 & 0.098 & 0.137 \\ 0.773 & 0.387 & 0.262 & 0.269 & 0.323 & 11.204 & 0.772 & 0.538 \\ 0.597 & 0.331 & 0.241 & 0.474 & 0.361 & 0.649 & 1.484 & 0.634 \\ 0.595 & 0.362 & 0.263 & 0.333 & 0.232 & 0.639 & 0.548 & 0.838 \end{bmatrix} W_{6321} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix}$$

$$I_{6323}(nA) = \begin{bmatrix} 5.140 & 0.207 & 0.094 & 0.127 & 0.181 & 2.012 & 0.940 & 0.525 \\ 0.869 & 2.495 & 0.176 & 0.480 & 0.503 & 0.975 & 0.670 & 0.728 \\ 1.160 & 0.564 & 0.483 & 1.452 & 0.662 & 1.256 & 1.275 & 1.469 \\ 0.380 & 0.271 & 0.369 & 3.040 & 0.539 & 0.551 & 0.557 & 0.540 \\ 0.131 & 0.084 & 0.045 & 0.093 & 3.173 & 0.322 & 0.191 & 0.201 \\ 1.111 & 0.366 & 0.239 & 0.223 & 0.253 & 14.875 & 1.017 & 0.488 \\ 0.970 & 0.555 & 0.417 & 0.462 & 0.394 & 0.720 & 1.408 & 0.606 \\ 0.649 & 0.372 & 0.276 & 0.366 & 0.321 & 0.533 & 0.418 & 0.738 \end{bmatrix} W_{6323} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

With a fitness score of 26, 31, 20, 31, 32, 22 in the order of display. It is clear from the coloured labelling that they are only marginally away from the identity matrix. Furthermore, their singularity is questionable since all six genomes have I^{38}_{OUT} as part of the classification. However, they are always accompanied by another current from either the same row,3, or column,8, that are only different by few tens of picoamps. Thus resulting in lower fitness score despite the success rate of 7.

The scaled-up eight device full search result have not managed to find a genome that can successfully classify all 8 input. This is a detrimental argument towards the interconnectivity power of the scaled up system, as the three high score achieving genomes, upon analysis, seem to have vastly different switch configurations, yet could not isolate their output from the identity matrix. The results here should not be a discouragement to the digit or image recognition experiments since those inputs require more than two electrodes connected to the source layer. Such situation could vastly change the current pathway because the switch configuration will cause the influence of each input electrode to intertwine with that of every other input electrodes. However, the performed experiments could not satisfy a condition that could be a promoising evidence of the power of interconnectivity.

6 Conclusion/Outlook

Herein, we have shown a reproducible dopant recipe which can result in over 50 % yield for Boron doped device that shows non-linearity at the liquid nitrogen temperature. These boron doped devices have a clear signature of the boolean logics as singular or even as a series setup, which to our definition as of now, should indicate rich dynamic behaviour within the system to support the further functionality. While Arsenic device has only been fabricated once, high yield is also confirmed and thus can be an addition to the future experiments if another dopant system becomes necessary. The boolean logic results seem to suggest that there are more work to be done in the new GA setup as the fitness score calculation is not yet fully optimized, and most importantly, the weighing of these new parameters in the modified fitness score (parameter A, B, C, and D) are yet to be explored. However, a good boolean logic is obtainable even without the fine tuning of the new GA setup, as such, this does not have to be treated as a pressing matter in the future.

Furthermore, we have finalized the darwin internet setup which can be used for a scaled-up operation. The work was done on the dipstick, PCB, and last but not least the software interface to allow interconnectivity experiment in python 3.0 platform. The progress on this setup currently allows (1)multiple IV curves (2)multi-device full search (3)Digit recognition full search and (4)GA Digit recognition. (1) is a useful experiment which can be run before moving on to GA to confirm the Coulomb gap, but due to its lack of novelty, the obtained result will be excluded from the main body of the report. While (3) can easily be initiated and have an analysis tool already written, eight-device full search with a high number of genomes can take more than a day. Thus due to the time constraint of the final version of the thesis, the results will not be included in this report. The software basis for (4) is also already written. However, it is likely that the mutation and recombination process needs revision as they are currently untested, and is highly unoptimized in evolving towards the better result.

Results for (2) are given in this thesis report. With the acquired results, our scaled-up system could not obtain unique input-output relations. There are certain things that could be reviewed to have a different approach to the full search experiments such as the number of genomes. Switch configuration allows a cosmic number of possibility to explore which scales rapidly with the number of the devices. It's possible to conclude that the results shown may not be a good statistical representation of the entire search dimension. Second is the tuning of the initial population. It is yet unclear what magnitude of effect a single switch can have on the input-output relation. If it is preferred to make multiple connections than having none, the initialisation process may need revision to remove all the genomes that contain a row with no connection.

Since the effect of having multiple inputs simultaneously is unclear, it may be of interest to move to multi-input experiments such as a digit or image classification, before fine tuning the single-input-single-output full-search. This is easily done by providing an input that corresponds to a particular information, such as digitalized numbers or images. As an example, digit recognition experiment explained in this thesis requires two rows from the switch configurations to be an input. If we increase the number of information to 24 bits, the third row can also be used as an input thus it may be possible to do 6 by 4 digit recognition. By continuing in this manner, the larger information can be processed with a compromise of some switch configurations. This, in theory, should allow multiple dopant devices to handle MNIST image set which are standardized dataset for the classification. In which case the only limitation that we currently face, apart from the yet investigated true potential of the interconnectivity, is the number of devices and the number of electrodes(and likewise, number of switches on the ICs and the intermediate layers). Since the size of the current PCB allows no more room to fit more device as well as switches, new PCB has to be designed for an even larger system or more electrode dopant devices. It may, however, be easier to fabricate a dopant device that can show non-linear IV curve at the room temperature because the device number limitations is hard-linked to the every hardware kit in the setup.

Room temperature measurement not only allows more samples to be measured but also reduces the risk and delay in the experiment that arises due to the setup requiring liquid nitrogen.

To conclude, no results which can support the interconnectivity GA is obtained. However, there is still a room to investigate the interconnectivity in a more optimised setup as well as procedures. Moreover, The system to support the multi-device experiments are finally available. Thus our goal of scaled up system has been fractionally finalised. It is only a matter of achieving the scaled up functionality with a successful and sufficient result to determine whether the dopant device's performance can also be scaled up using the interconnectivity.

*Any in-progress work related to the potential future experiments can be found on the skyNEt Github repository which contains every script written for the BRAINS project, including all the necessary script for the switch experiments.

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