MASTER THESIS

ATR-IR Microreactor With Ultra Fast Integrated Microvalves For Heterogeneous Catalytic Analysis In The Microsecond Domain

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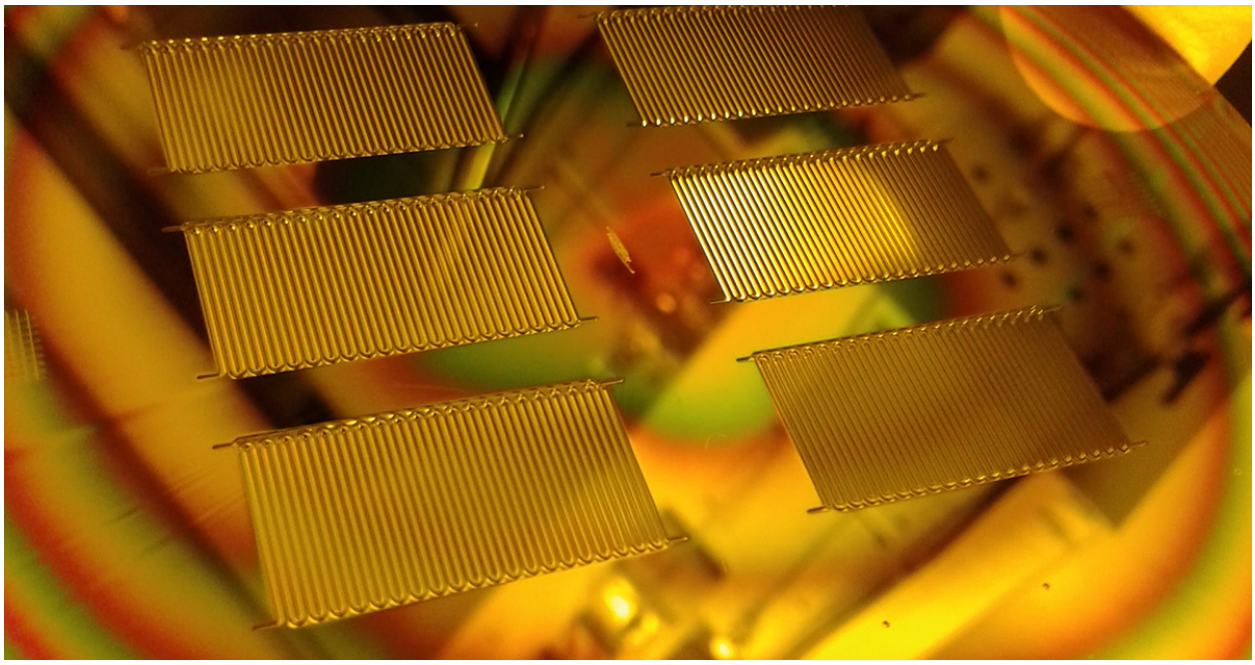

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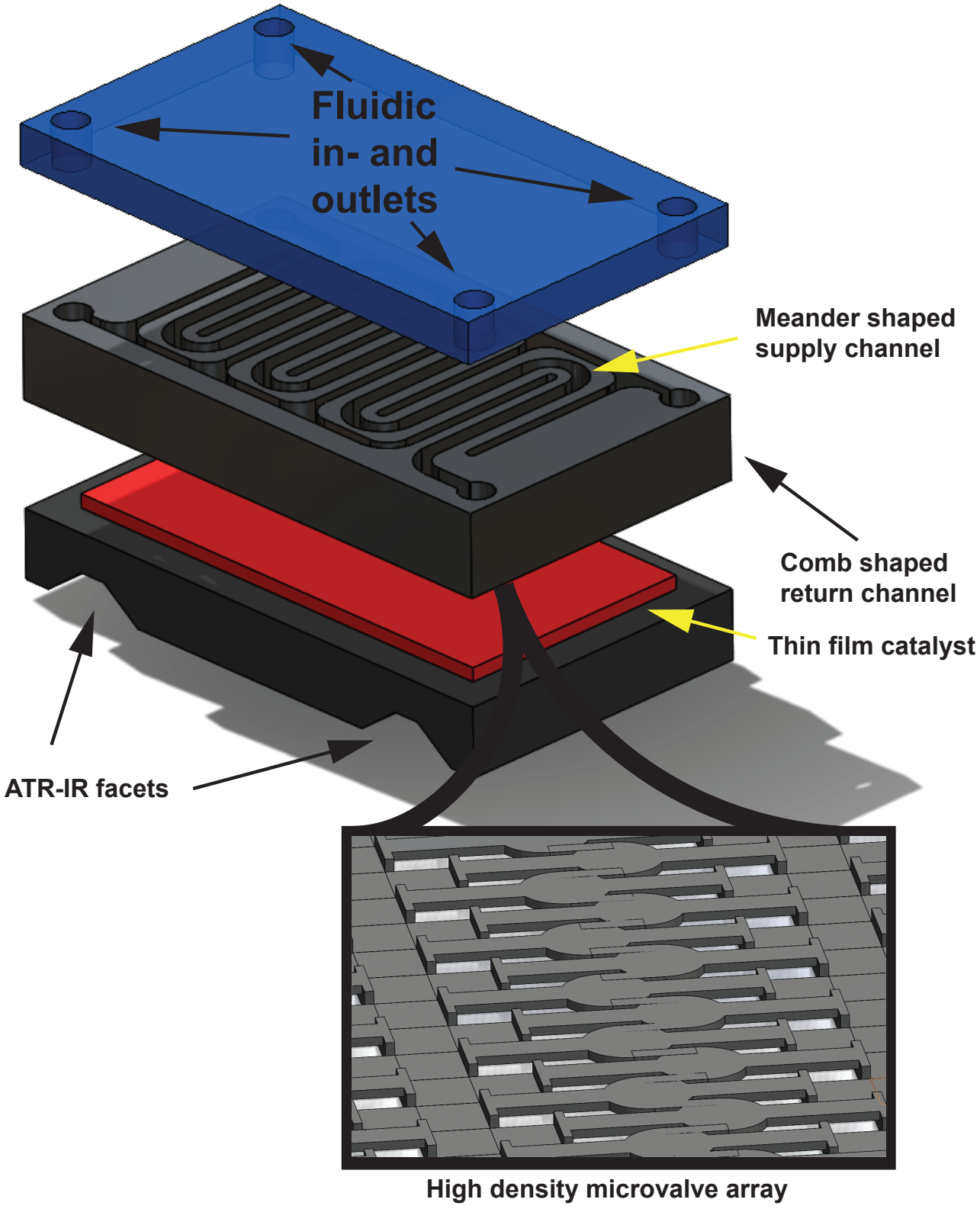


Simplified representation of the microreactor platform for heterogeneous catalytic analysis showing the most important elements of the chip.

ATR-IR Microreactor With Ultra Fast Integrated Microvalves For Heterogeneous Catalytic Analysis In The Microsecond Domain

R. Haverkate, J.J.A. Lozeman, J.G. Bomer, M.J. de Boer, J.W. Berenschot and M. Odijk

***Abstract*—A strongly improved sampling rate for infrared (IR) spectroscopy enables for the first time measurements in the timescale of the reaction kinetics. To enable heterogeneous catalytic analysis a platform is needed that has sufficient speed and control over its mass transport to take advantage of this increased resolution. In this paper we present a reactor chamber platform consisting of a chip with more than 5000 electrostatic actuated microvalves and a chamber volume of less than 1 µL. This platform has a maximum operation temperature of 450 °C and can work under a pressure up to 10 bar to gain control over its mass transport and enhance the detectability of gases. Theoretical analysis showed a total gas transition time of less than 200 µs and therefore measurements to the reaction kinetics in the microsecond domain become possible.**

***keywords:* heterogeneous catalysis, microfluidics, mass transport, attenuated total reflection infrared spectroscopy, electrostatic microvalves, micro fabrication, microelectromechanical systems, sacrificial layer etching, trench filling**

I. Introduction

For the development of novel and efficient heterogeneous catalysts, understanding of the kinetics is of particular interest. Recent improvements in mid-infrared (IR) spectroscopy using quantum cascade lasers (QCLs) have lead to a new type of IR spectrometer. It has a bandwidth of $120\,\mathrm{cm}^{-1}$ and is able to scan the spectrum in less than $1\,\mu\mathrm{s}$.[1–3] The strongly improved sampling speed allows for measurements within the time-frame of reaction kinetics with an accuracy that was never possible before (see in figure 1 the difference in sample rate between QCL-IR spectroscopy and Fourier transform infrared spectroscopy (FTIR) spectroscopy).[3] Setups that make use of a conventional reaction chamber and FTIR do not meet the required speed and control over its mass transport to obtain a sufficient resolution.[4–6] A new IR platform with rapid mass transport is needed that enables catalytic analysis in the unexplored micro second domain (see figure 1 for the step-wise reactant gas concentration necessary to detect the intermediate states).

IR spectroscopy is a frequently used technique to reveal information about molecular compositions and structures.[7, 8] This technique does not require high vacuums during operation and has negligible influence to the characteristics of the molecules, this is an advantage compared to traditional analytical methods like mass spectroscopy or X-ray photo-electron spectroscopy.[9] Since IR spectroscopy is non-destructive, it allows reactions of species to be studied.[9] One specific type of IR spectroscopy makes use of attenuated total reflection (ATR). Multimode internal reflection elements (IREs) for ATR-IR are typically rectangular shaped crystals where light enters one side of a slab and leaves on the other side. The difference between the refractive index of the crystal and the sample makes the light to internally reflect at the surface as the wave propagates through the crystal. During reflection, evanescent fields occur that penetrate the surface (see figure 2). This results in absorption lines at specific wavelengths which depend on the molecules close to the crystal surface. Consequently the absorption spectrum can be studied to identify these molecules.[6, 9–11]

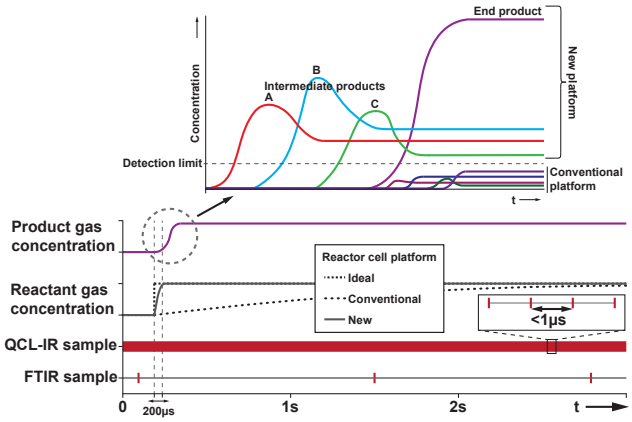


Fig. 1: This schematic representation shows the two critical aspects necessary to perform measurements within the time-frame of the reaction kinetics and to distinguish between short-living intermediates: the sample rate of the spectrometer should be fast enough and the platform to handle the fluids needs a step-wise transitions between gases. The expanded graph of the product gas concentration shows the difference between conventional platforms and the new reactor cell platform proposed in this paper. The new platform is able to distinguish between short living intermediates as the short transition times between gases results in directly sufficient product concentrations available to detect.

Silicon has a high refractive index, but commercial ATR crystals, with a minimal thickness of $2\,\mathrm{mm}$, have a rather limited optical window (approximately 8300 to

$1500\,\mathrm{cm}^{-1}$).[9, 12] Consequently only the group frequency region is available for analysis.[8] A standard $100\,\mathrm{mm}$ silicon wafer with a thickness of only $0.5\,\mathrm{mm}$ has the advantage that also the fingerprint region (approximately $200\,\mathrm{cm}^{-1}$ to $1200\,\mathrm{cm}^{-1}$) can be used, making it very suitable for catalytic analysis.[9]

There is a clear trend of going towards lower reactor-cell volumes to gain control over the mass transport.[4–6, 13] New concepts are proposed that use conventional micro fabrication materials instead of e.g. ZnSe IREs.[9, 13] The group of R. Herzig-Marx has developed a system using a microfabricated silicon crystal. The chip was anodically bonded to an etched pyrex glass wafer to form a channel shaped reactor-cell with a volume of only $4\,\mu\mathrm{L}$.[13] E. Karabudak et al. fabricated silicon IREs out of a standard Si wafer that was cleaved with a sapphire pen tip. Their IRE is rather cheap in comparison to commercial crystals and allows deposition of many different thin film catalysts, enabling fast parallel screening in a cost effective way.[9] Because of the compatibility of these materials with the fabrication of microelectromechanical systems (MEMS) and microelectronics, processes are well established with high control of compositions, material characteristics and dimensions.[9, 13] In addition it offers the possibility for batch fabrication and integration of electronics.[13]

To understand the reaction mechanisms during catalysis and in particular the rate limiting steps, detection of short-living intermediates is of significant importance. Moreover, to find out the mechanism, we need a well defined trigger. Therefore, besides the rapid mass transport, only short transition times between gases are allowed (as shown in figure 1). To obtain transition times in a fraction of a millisecond it becomes necessary to develop a microreactor platform with a high degree of integration by incorporating microvalves. To enhance the signal-to-noise ratio, measurements need to be repeated many times. In order to obtain optimal catalytic reaction and detection conditions the platform should operate both at high temperature and high pressure.

The ideal valve for the microreactor is easy to fabricate and can operate from room temperature up to $450\,^{\circ}\mathrm{C}$. The high temperature limit enables a wide range of chemical reactions to be analyzed. The flow rate should allow the microchamber to be flushed within the microsecond domain and the valve switching speed has a large influence on this transition time. The demanding combination of valve characteristics asks for a parallel array of small valves with low hydraulic resistance that can operate at sufficient differential pressure to allow for high flow rates. To get a step-wise gas transition the leakage flow should also be low.

In general, the environment in which a valve needs to operate puts a demand on the specifications. As a result of this, many different valve designs and concepts are presented in literature.[14–20] K. Oh et al. presented an overview of the different designs and actuation mechanisms reported in the last three decades. Traditional active microvalves are created with surface and bulk micromachining techniques where a beam or membrane is mechanically deflected by coupling

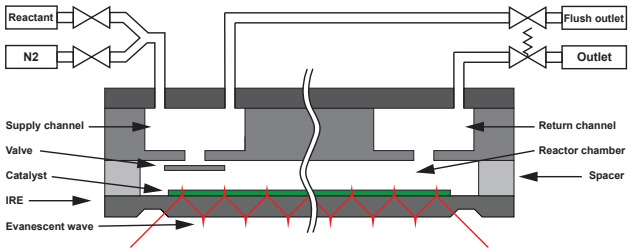


Fig. 2: Schematic representation of the cross view of the reactor cell platform showing the microfluidic chip connected to gas supply and return lines.

it to the e.g. electric, magnetic or thermal domain.[14]

Different types of thermal controlled valves are proposed in literature, like a shape memory alloy or bimetallic or thermopneumatic valve. Although large valve openings can be achieved, they all suffer from slow switching speeds.[14, 16, 17] Magnetic actuated valves also have a low response time, but this originates from the relative large mass for displacement.[14, 15] In the field of microfluidics often soft lithography is used as an alternative to silicon-based microfabrication techniques.[21] However, in this case the switching speed is limited by external valves and hydraulic parasitic effects in tubings. There are many piezoelectric microvalves presented in literature.[4, 14, 15, 17] Piezoelectric materials can produce relative large forces at small displacements. Although valves of this material can generally operate at a lower voltage than electrostatic microvalves they are more complicated to fabricate. Electrostatic valves instead are known to have extreme low power consumption, are relative easy to fabricate and show fast response times, but suffer from high actuation voltage.[17] The valve properties scale favourable with down scaling. Considering the low mass for displacement, also the force per unit area increases exponentially with decreased gap-distance. Therefore, the electrostatic actuation principle is most suitable for the microreactor platform.

P. Dubois et al. presented a normally open electrostatic microvalve for gas applications with ultra-fast switching behaviour at high pressures. The $Ta_{49}Si_{14}N_{37}$ clamped-clamped beam construction switched in less than $100\,\mu\mathrm{s}$ at a differential pressure of $200\,\mathrm{kPa}$. With an orifice of $10\,\mu\mathrm{m}$ a maximal flow rate of $2\,\mathrm{mL/min}$ was measured. When the valve was closed with an actuation potential of $30\,\mathrm{V}$, no leakage was observed. The shape of the valve membrane was optimized to operate at low actuation potential to prevent electric breakdown. Simultaneous actuation of an array of 20 microvalves was demonstrated, showing the potential for parallelization.[19] The fabrication only consist of well established MEMS processes, making the design very suitable for the ATR platform.

In this paper we present a platform for ATR-IR suitable for heterogeneous catalytic analysis in the microsecond domain. A microfluidic chip is designed that can be fabricated using a combination of standard bulk and surface micromachining techniques. An extremely low chamber

volume together with the by P. Dubois et al. inspired electrostatic microvalves enables high speed and control over its mass transport.[19] The platform is designed to be modular, in order to separate the sensing part from the part that holds the microvalve structures, enabling the catalysts to be changed but rest of the chip to be reused. Due to time restrictions the results and discussion section contain intermediate fabrication results and possible solutions to observed problems.

II. Design and simulation

A. System concept

The ATR platform consist of a microfluidic chip that is connected to a nitrogen gas supply, a reactant gas supply[1], a flush outlet and a chamber outlet, as shown in figure 2. The outlet is connected to a pressure relieve valve to maintain a high pressure in the reactor chamber. This valve will automatically open when the chamber operation pressure is exceeded. The two supply lines are connected to electronically controlled pneumatic valves and are set to a higher pressure than the pressure relieve valve. The flush outlet also contains an electronically controlled valve and is connected to the supply channel to facilitate channel flushing in order to achieve short chamber transition times. The supply channel connects all integrated microvalves to the supply line, maintaining a low hydraulic resistance. The parallel connected microvalves are actuated simultaneously to provide a short transition time between the gases. The modular chip can be separated at the topside of the spacer so that different IREs can be used with the same setup. Note that figure 2 is a highly simplified representation where only a single valve is shown and the electronics are omitted.

B. Optical domain

The optimal IRE dimensions are dependent on the optical setup and the dimensions largely influence the signal-to-noise ratio. For example the optimal width of the facet (used to couple the light into and out of the crystal) depends on the laser spot size. And the length of the crystal is a trade-off between sensitivity and signal attenuation. If the crystal is too short the sensitivity is too low due to a low number of internal reflections. With a long crystal you have many internal reflections but attenuation of the signal causes the signal-to-noise-ratio to increase. As a starting point we used a crystal of $30\,\mathrm{mm} \times 15\,\mathrm{mm}$ made from a $100\,\mathrm{mm}$ Si wafer that was optimized for a high signal-to-noise ratio. For the ATR-IR platform, the length and width of the IRE are used as the outer dimensions of the chip.

For the ATR crystal there are three additional design criteria for the platform. First, to limit the signal attenuation it is important that the active sensing area of the crystal does not contain structures with a high refractive index. Second,

[1]The type of gas varies depending on the chemical reaction to be studied

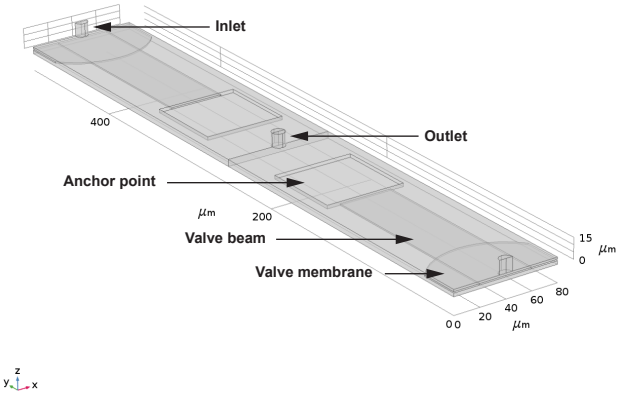


Fig. 3: Reactor chamber simulation geometry used for mass transport analysis containing two half valves at the axial ends and a single outlet located at the center. The valves are located inside the reactor chamber.

the chamber height should be above the penetration depth of the evanescent wave, which is calculated by:

$$d_p = \frac{\lambda}{2\pi\, n_c \sqrt{sin^2(\theta) - (\frac{n_s}{n_c})^2}} \tag{1}$$

Where d_p is the penetration depth, λ the wavelength, θ the angle of incidence ($54.74°$ for $<100>$ KOH etched facets), n_c and n_s respectively the refractive index of the crystal (3.44 for silicon) and the sample (approximately 1 for gases).[8, 9] Also, the thickness of the catalytic film should be only a fraction of the penetration depth to keep sufficient sensitivity.

C. Microfluidic and chemical domain

The influences of pressure, temperature and dimensional parameters to the transition time were investigated using COMSOL (version 5.3). The multiphysics model was reduced to a geometry of a single reactor chamber cell as shown in figure 3. All sides of the reactor cell are symmetry planes. This simplification gives a good estimation of the velocity profile and mass transport everywhere except close to the chamber sidewalls. Since the cells located at these walls are only a small fraction of the total chamber surface the sidewall effect can be ignored. The inlet radius, membrane thickness, valve gap and suspension dimensions were fixed as defined by P. Dubois et al. ([19]). This also sets the cell width ($80\,\mu\mathrm{m}$) which is dependent on the the orifice distance of the valves.[19]

Since we want to know the transition time of the reactor chamber when switching between gases, the reactor cell was pre-filled with N_2 gas and this was subsequently replaced by CO_2 as a reactant gas. The inflow of CO_2 at the inlets was first calculated using the time dependent Navier-

Stokes equation for compressible flow combined with the continuity equation:

$$\rho\frac{\partial \boldsymbol{u}}{\partial t} = -\nabla\cdot\boldsymbol{p} + \mu\nabla\cdot(\nabla\boldsymbol{u} + (\nabla\boldsymbol{u})^T) - \frac{2}{3}\mu\nabla\cdot(\nabla\cdot\boldsymbol{u}) \quad (2)$$

$$\frac{\partial \rho}{\partial t} + \nabla\cdot(\rho\boldsymbol{u}) = 0 \quad (3)$$

Where ρ and μ are the density and viscosity of the CO_2 gas, $\boldsymbol{p}$ and $\boldsymbol{u}$ respectively the pressure and velocity vector and T the temperature of the gas. The inlet and outlet boundary conditions were set to a static pressure. Furthermore, the channel walls were provided with no-flux and slip condition ($\boldsymbol{u} = 0$). Because of the low density of gases and small dimensions of the reactor cell (low Reynolds number) the inertial effects have negligible influence on the transition time and are omitted in this model, giving a creeping flow profile. The pressure and flow velocity fields were used to calculate the mass transport by solving the time-dependent convection-diffusion equation:

$$\frac{\partial c_i}{\partial t} = \nabla\cdot(D_i\nabla c_i) - \boldsymbol{u}\cdot\nabla c_i \quad (4)$$

$$\boldsymbol{N}_i = -D_i\nabla c_i + \boldsymbol{u}c_i \quad (5)$$

Where D_i is the diffusion coefficient of the gas. The concentration, c_i, as a function of pressure and temperature was calculated by using the ideal gas law:

$$c_i = \frac{p}{RT} \quad (6)$$

Where R is the ideal gas constant.

Since the gas concentration decreases with increased temperature, a high pressure is preferred. The chip will operate at elevated temperatures up to $450\,^{\circ}\mathrm{C}$ and the outlet pressure was set to $10\,\mathrm{bar}$. This high pressure increases the gas concentration and the diffusive effect. In figure 4 you can see the effect of different inlet pressures on the transition time.[2] The concentration is averaged over the active sensing-surface area. As can be seen, an increased differential pressure significantly reduces the transition time.

The effect of the reactor chamber height to the concentration profile over time is shown in figure 5a. The transition time improves with a reduced chamber height, this can be explained by the increased velocity flow rate just above the active sensing area ($z \approx 0\,\mu\mathrm{m}$), shown in figure 5b. Since the flow rate close to the sensing area is very low the transition time is largely dependent on diffusion. Despite the fact that the volumetric flow rate decreases using a reduced chamber height, the flow velocity close to this surface increases. As a consequence the diffusive effect is enhanced by convection. For the chip design we used a chamber height of $5\,\mu\mathrm{m}$ since further reduction will interfere with the penetration depth restriction (equation 1) since the valves are constructed inside the reactor chamber.

[2]The transition time is defined as the time it takes to reach $80\,\%$ of the reactant bulk concentration.

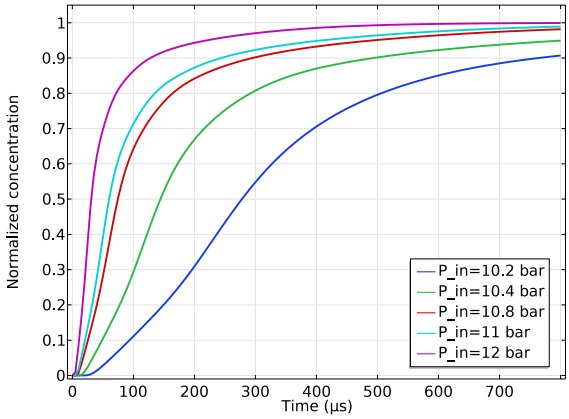
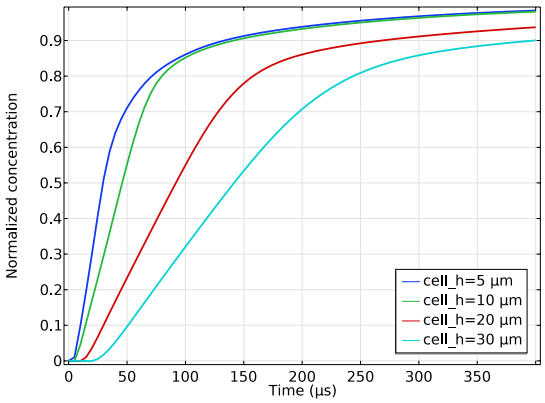
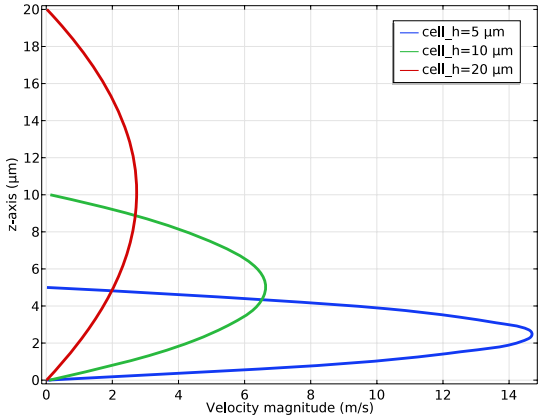


Fig. 4: Gas concentration as a function of time for different pressures. The temperature of the gas is $150\,^{\circ}\mathrm{C}$. *The chamber height and length are respectively* $5\,\mu\mathrm{m}$ *and* $500\,\mu\mathrm{m}$. *With the outlet pressure of* $10\,\mathrm{bar}$ *the differential pressure accross the reactor chamber is evaluated from* 0.2 *to* $2\,\mathrm{bar}$.



(a) Gas concentration as a function of time for difference chamber heights.



(b) Flow velocity profile for different chamber heights at $t = 100\,\mu\mathrm{s}$.

Fig. 5: Concentration and velocity profile for different chamber heights. The chamber length is $500\,\mu\mathrm{m}$, *the temperature of the gas* $150\,^{\circ}\mathrm{C}$ *and the in- and outlet pressure respectively* $12\,\mathrm{bar}$ *and* $10\,\mathrm{bar}$.

The effect of the cell length on the transition time depends on a few factors. First, the space needed for the valves puts a lower limit of $500\,\mu m$ to it. Secondly, the mass transport directly beneath the valve is completely dependent on diffusion. Therefore, an increased cell length means that a larger portion is exposed to the gas flow, making convection of greater influence on the transition time. Another consequence of an increased cell length is that less reactor cells will fit in the reactor chamber, reducing the diffusion dependent volume even further. Thirdly, the hydraulic resistance of the reactor cell is dominated by the valve resistance ($R_{valve} = 0.89 \times R_{cell-total}$ for $L = 500\,\mu m$ and $h = 5\,\mu m$). Hence, for an increased cell length the change in resistance is very small as long as $R_{length} << R_{valve}$. And last, the reactor chamber can be seen as a large parallel array of reactor cells. It turns out that the effect of a larger degree of parallelization is favoured over the other effects and therefore a cell length of $500\,\mu m$ is preferred (see [22] for a short movie of the mass transport of the single reactor cell, pre-filled with N_2 gas that is replaced by CO_2, using the specified optimal parameters).[3]

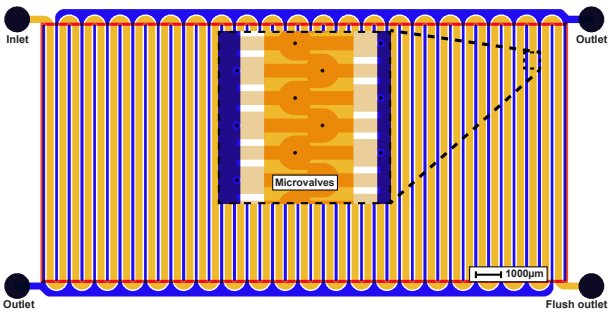


Fig. 6: Top view of channel structures. Black circles: fluidic in- and outlets, red: reactor chamber boundaries, orange: supply channel, blue: return channels. Enlargement shows the high density micro valve structures located inside the reactor chamber underneath the supply and return channels.

Based on the given cell dimensions described above and chamber dimensions specified in section II-B, the chip contains approximatley 5000 microvalves. As we have a creeping flow, we can use the single reactor cell model to extract the hydraulic resistance of one cell using Ohms law for fluidics.[23] Division of this resistance by the amount of valves gives the hydraulic resistance of the reactor chamber. To have a minimal effect on the transition time, the supply and return channels should have a low hydraulic resistance compared to the reactor chamber resistance. Therefore, to enable short switching times between gases, the supply channel is a meander shaped structure with one end connected to the supply line and the other end to the flush outlet.[4] The meander shaped channel is enclosed by comb

[3]See supplementary information S1 for calculations on the hydraulic resistances.

[4]Note: connecting both ends of the meander-shaped channel to the supply line lowers the supply channel resistance by 50%. To keep the first design as simple as possible this is not included in the design.

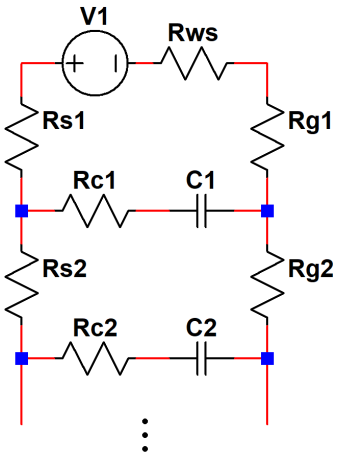


Fig. 7: Simplified RC-model of a microvalve array (125 valves parallel) made in LTSpice. Here, Rs_n is the series resistance of the top electrode, C_n is the single valve capacitance and Rc_n its resistance, Rg_n is the ground plane resistance (bottom electrode) and R_{ws} the total resistance between the voltage supply and the microvalve array.

structures on both sides to connect all chamber outlets to the return channel as shown in figure 6. For the given cell length of $500\,\mu m$ the hydraulic resistance and thus the transition time calculated by COMSOL increases with approximately 25% as a consequence of the rest of the hydraulic network. Increasing the cell length will create space to expand the width of the supply and return channels, lowering this resistance. Nevertheless, the reduced valve density will cause the transition time to increase since the chamber resistance is dominant over the channel resistance. For the design we used a supply and return channel width of respectively $260\,\mu m$ and $100\,\mu m$. The channels have a depth of around $470\,\mu m$ and are separated by walls of $70\,\mu m$.[3]

Using the COMSOL model, the cell outlet radius was set to be equal to the valve inlet ($5\,\mu m$) because doubling the outlet radius is negligible on the transition time and using the same radius simplifies the chip fabrication process.

D. Electrical domain

It is important that only the thin film of the catalyst material reacts with the reactant gas, therefore metals cannot be used for the construction of the microfluidic channels and the reactor chamber, including the integrated microvalves. The microvalves proposed by Dubois et al. ([19]), constructed with $Ta_{49}-Si_{14}-N_{37}$ layers, can therefore not be used, so we need to fabricate these valves from a different material.[5] A LTspice model was used to evaluate the effect of the transition time if heavily doped silicon was used instead. The simplified model with one complete microvalve array (see figure 7) showed that the RC-time of the microvalves is four orders of magnitude larger in

[5]A brief discussion about the material choices can be found in supplementary information S8.1

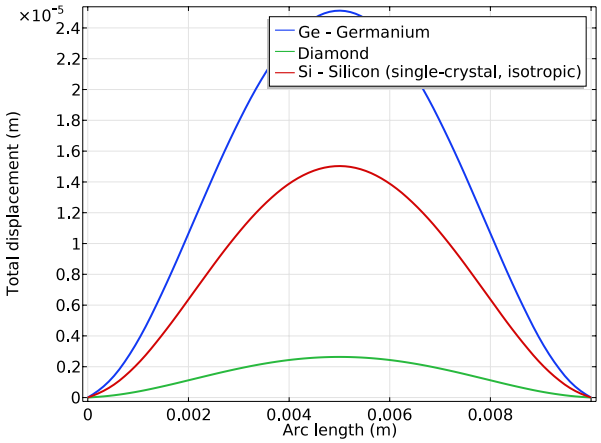


Fig. 8: IRE deflection across the crystal for different materials. The differential pressure across the crystal is $12\,\mathrm{bar}$*. The deflection is at its maximum at the center of the crystal.*

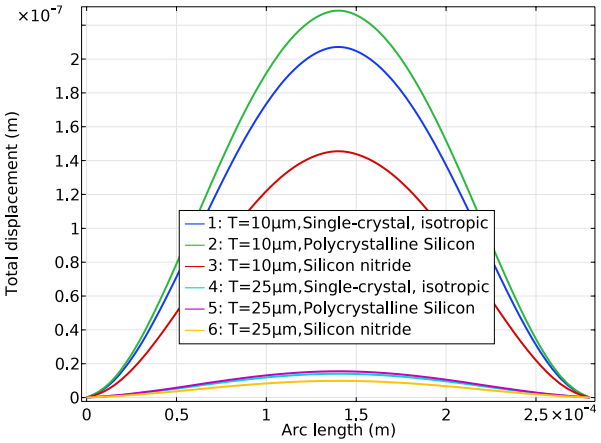


Fig. 9: Deflection of the separating layer between the supply channel and the reactor chamber for different layer thicknesses and materials.

comparison with using metals. However, as the electrostatic force drops quadratic with increased gap space, silicon can still be considered to be a suitable alternative to tantalum as no major effect on the transition time is expected.[6][19] In addition the Youngs modulus is comparable so that the valve design does not require geometric changes.

A large differential pressure requires high electric fields to cause a pull-in force large enough to close the microvalves, since the following force balance applies:

$$F_{total} = F_{pressure} + F_{deflection} + F_{electrical} \tag{7}$$

Where $F_{electrical}$ is in opposite direction to the pressure and deflection forces. If the electric field becomes too dense the dielectric Si_3N_4 layer gets charged, requiring an even higher operation potential and eventually the breakdown voltage will be reached.[18, 24] Once the valve is closed a much smaller potential is needed because the decreased electrode distance increases the field density. To operate the chip at relative low electric potentials without effecting the transition time the platform will switch from a high ($\Delta p = 2\,\mathrm{bar}$) to a low differential pressure ($\Delta p = 200\,\mathrm{mbar}$) when closing the microvalves. Elaboration about the operation principles can be found in the next chapter.

E. Mechanical domain

Large differential pressures across the thin layers and membranes cause design criteria for the chip. For example if the deflection of the IRE becomes too large this will effect the path the IR beam will take through the crystal. If the deflection of the separating layer between the chamber and the supply channel is too big, the valve seat will have limited contact with the membrane, causing high valve leakage.

Deformations were evaluated using a structural mechanics model in COMSOL. The geometry for the IRE consisted of a plate of $20\,\mathrm{mm} \times 10\,\mathrm{mm}$. This is the crystal area excluding the space occupied by the spacer (see figure 2). As boundary condition all the plate edges were fixed and the differential pressure was set to $\Delta P = 12\,\mathrm{bar}$. With a wafer thickness of $510\,\mu\mathrm{m}$ the maximal deflection of silicon was only $15\,\mu\mathrm{m}$, which is small enough to not effect the internal reflections of the IR beam (see figure 8).

The geometry of the separating layer located at a single valve was a beam of $280\,\mu\mathrm{m} \times 80\,\mu\mathrm{m}$, based on respectively the supply channel width and the orifice distance between two microvalves. The inlet orifice of the valve was located at the center of the beam. As boundary condition the beam was fixed at both ends, the other sides were defined as symmetry planes and a differential pressure of $\Delta P = 2\,\mathrm{bar}$ was applied perpendicular to the beam. With respectively a thickness of $T_b = 60\,\mu\mathrm{m}$, $25\,\mu\mathrm{m}$ and $10\,\mu\mathrm{m}$ its deflection was $1.5\,\mathrm{nm}$, $15\,\mathrm{nm}$ and $220\,\mathrm{nm}$ (figure 9 show the deflection for layer thicknesses $10\,\mu\mathrm{m}$ and $25\,\mu\mathrm{m}$). $25\,\mu\mathrm{m}$ is taken as lower limit for the thickness of the separating layer due to fabrication constrains (discussed in section III and section IV). At $T_b \geq 25\,\mu\mathrm{m}$ we expect that the valve leakage caused by deflection is relatively low and therefore it is considered not to be a problem.[7]

To prevent bond breaking due to the high pressure differences between the chip and its surrounding, the chip will be mounted in a rigid stainless steel holder that also facilitates electric and leak tight pneumatic connections to the rest of the setup.[8][25] An overview of the specified design dimensions is given in table I.

III. Methods and Materials

A. Chip fabrication

The micro fabricated ATR chip involves nine lithography steps to form a three wafer sandwich that is at wafer-

[6]In supplementary information S2 more information about the LTspice model and RC-time is given.

[7]Figures and more details about the deflection analysis in COMSOL can be found in supplementary information S3

[8]A short discussion about the clamp design can be found in supplementary information S8.2

TABLE I: Overview predefined design dimensions

Property	Value
Chip length and width	$30\,\mathrm{mm} \times 15\,\mathrm{mm}$
Reactor chamber dimensions	$20\,\mathrm{mm} \times 10\,\mathrm{mm} \times 5\,\mu\mathrm{m}$
Supply channel width	$260\,\mu\mathrm{m}$
Return channel width	$100\,\mu\mathrm{m}$
Channel wall width	$70\,\mu\mathrm{m}$
Separation layer thickness	$\geq 25\,\mu\mathrm{m}$
Valve spacing	$500\,\mu\mathrm{m} \times 80\,\mu\mathrm{m}$
Valve membrane radius	$50\,\mu\mathrm{m}$
Valve suspension length	$340\,\mu\mathrm{m}$
Valve gap	$1.5\,\mu\mathrm{m}$
In-/outlet radius	$5\,\mu\mathrm{m}$

scale bonded together. The IRE facets, microfluidic channels and in- and outlet orifices are made with bulk micro machining, whereas surface micro machining is used for the construction of the spacers, valve seats and membranes (see figure 10)[9]. We use sacrificial layer etching of silicon oxide to create the free suspended membranes of the micro valves and freeze drying to prevent permanent attachment of the membranes to the substrate after etching the oxide layer.[26] The valve seat has a high surface roughness to avoid stiction during operation and the membrane is given a low tensile stress by a proper anneal cycle in order to prevent buckling effects. The valve electrodes can be seen as a plate capacitor where a P++ silicon wafer forms the bottom electrode and a heavily doped poly-silicon membrane the top electrode. These layers are separated by a silicon nitride film that in addition to its dielectric properties also functions as an etch stop and it protects the substrate during wet oxidation. In combination with TEOS, a poly-silicon layer is converted to thermal oxide to fill the $10\,\mu\mathrm{m}$ wide holes of the in- and outlets.[27] The reactor chamber of $<1\,\mu\mathrm{L}$ has 41 columns of 125 mutual connected valves giving a total of 5125 micro valves per chip. Information about the masks that are used during the fabrication process are given in supplementary information S5.

Wafer 1 contains the crystal with on top the metal catalyst and the spacers to define the chamber height, wafer 2 contains the channels, in- and outlet orifices and micro valves and wafer 3 is used to close these channels and to give the mechanical strength necessary for the last bonding step of the device.

For the IRE crystal a P-type $< 100 >$ double sided polished (DSP) silicon wafer is used. At first a $300\,\mathrm{nm}$ low pressure chemical vapour deposition (LPCVD) silicon nitride layer is grown. Then, at the backside of the wafer a lithography step (Olin Oir 907-17) defines the IR facets (mask 1). Subsequently reactive ion etching (RIE) with a CHF_3O_2 plasma is used to pattern the nitride followed by a resist strip (figure 10.a). Next, the wafer is placed in a KOH (25%) bath for $8\,\mathrm{h}$ to etch the IR trenches (figure 10.b). The nitride layers are removed in an undiluted (50%) HF-solution at room temperature for $95\,\mathrm{min}$ and subsequently a $50\,\mathrm{nm}$ thin catalytic film, for example copper oxide, is sputtered at the frontside of the wafer (figure 10.c). This metal is covered and patterned with a $5\,\mu\mathrm{m}$ thick SU-8 layer to define the chamber height (mask 2, figure 10.d). The process flow used for the fabrication of the *IRE wafer* can be found in supplementary information S6.

[9]The complete process outline is given in supplementary information S4

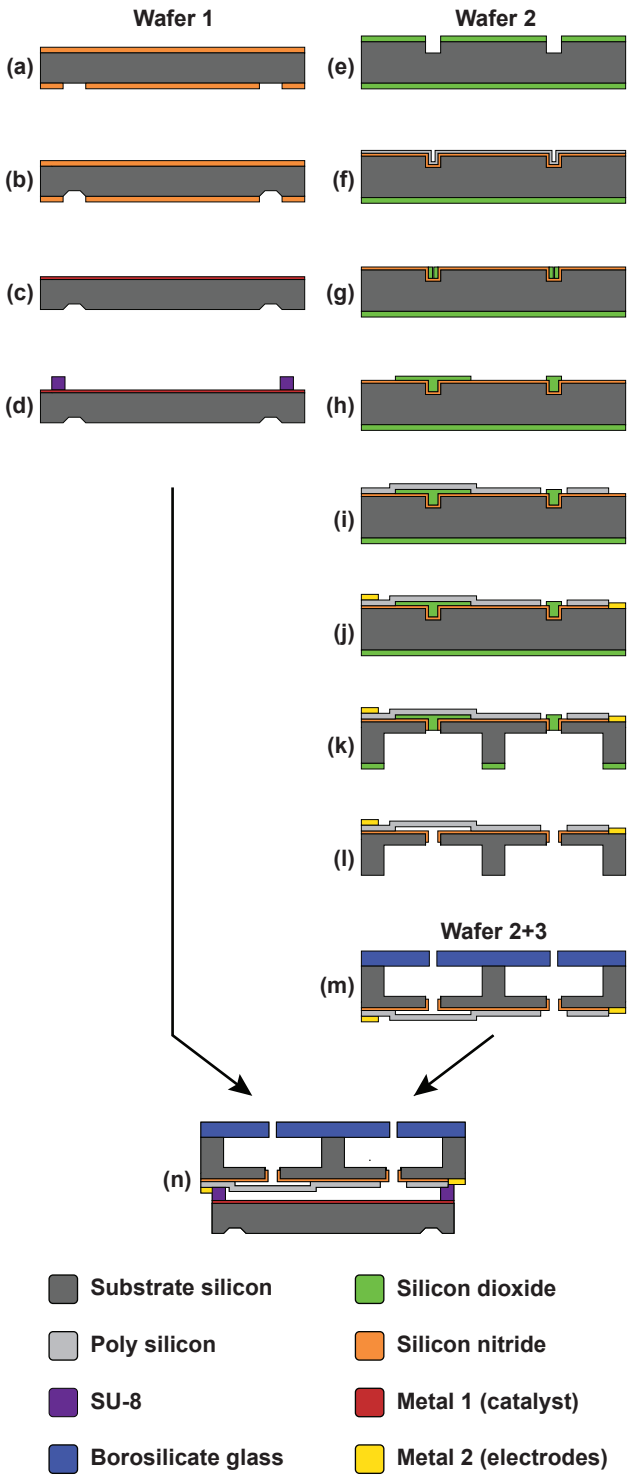


Fig. 10: Chip fabrication process outline. The different steps are explained in the text. Note: structures are not drawn to scale

Wafer 2 uses a heavily doped boron $< 100 >$ DSP substrate as basis. First a silicon oxide layer of about $2\,\mu\mathrm{m}$ is grown by applying wet oxidation at $1150\,^{\circ}\mathrm{C}$ for $23\,\mathrm{h}$. This layer is patterned by RIE (mask 3) with a CHF_3O_2 plasma and subsequently used as an etch mask for the in- and outlet orifices that are created with a deep reactive ion etching (DRIE) high-aspect-ratio silicon etch (HARS) process (SF_6/C_4F_8), see figure 10.e. The cavities have a depth between 80 and $100\,\mu\mathrm{m}$ to make, later in this process, trench etching of the channels at the wafer backside less critical. After removing the oxide layer at the frontside by RIE, a $500\,\mathrm{nm}$ thick nitride layer and subsequently an $1.8\,\mu\mathrm{m}$ poly-silicon layer is grown by LPCVD. This is followed by a two-step RIE process where the silicon and nitride layers are removed from the backside of the wafer (figure 10.f). Next, the poly-silicon at the frontside is directionally etched back till the nitride layer is reached and subsequently the remaining poly-silicon in the holes is fully oxidized by applying wet oxidation at $1150\,^{\circ}\mathrm{C}$ for $48\,\mathrm{h}$. At this stage the in- and outlet cavities are almost completely filled with thermal oxide (TOX) leaving holes between 0.1 to $3\,\mu\mathrm{m}$ in diameter (figure 10.g). These small cavities are filled by growing an $1.63\,\mu\mathrm{m}$ thick tetraethyl orthosilicate (TEOS) layer that also functions as sacrificial layer for the gap spacing. This TEOS layer is patterned with RIE (mask 4) followed by annealing at $1150\,^{\circ}\mathrm{C}$ for $2\,\mathrm{h}$ giving a final layer thickness of $1.5\,\mu\mathrm{m}$ (figure 10.h). At this stage a $1\,\mu\mathrm{m}$ LPCVD poly-silicon layer is grown that functions as valve membrane. Subsequently this layer is doped using a solid source dotation (SSD) boron drive-in process. Annealing at $1050\,^{\circ}\mathrm{C}$ for $2\,\mathrm{h}$ provides the required membrane tensile stress.[28] The poly-silicon layer is patterned with DRIE (mask 5) followed by a RIE step to remove the poly-silicon and TEOS layer at the backside of the wafer (figure 10.i). For the metalization, first the nitride layer is patterned (RIE, mask 6) to gain access to the substrate (bottom electrode). After a lithography step to define the electrode pads (mask 7) the frontside is sputtered first with chromium (adhesive layer) and subsequently with platinum. Lift off is used to remove the residual metallic film (figure 10.j). The backside located TOX layer that is created at the beginning of the processing of wafer 2 is now patterned (RIE, mask 8). Subsequently a HARS DRIE process is used to etch the microfluidic channels in the silicon substrate till a depth of $470\,\mu\mathrm{m}$ is reached (figure 10.k). Next sacrificial layer etching (SLE) is performed in an undiluted (50%) HF-solution at room temperature till the SLE layer and oxide etch mask are completely removed. Subsequently the valve membranes are released by a freeze drying procedure (figure 10.l). [28] The process flow used for the fabrication of the *valve wafer* can be found in supplementary information S7.

Wafer 3 consist of a borosilicate substrate with a thickness of $0.5\,\mathrm{mm}$. Holes are etched using powderblasting (Mask 9). The processed wafer is anodically bonded to wafer 2 closing off the channels (figure 10.m). Subsequently the sandwich construction is bonded to wafer 1 by adhesive bonding and diced in a two-step process. The first dicing step cuts through wafer 1 at specific lines only, to remove the silicon that covers the electrode pads of wafer 2. The second dicing step goes through the complete wafer sandwich to release the chips from the wafer (figure 10.n).

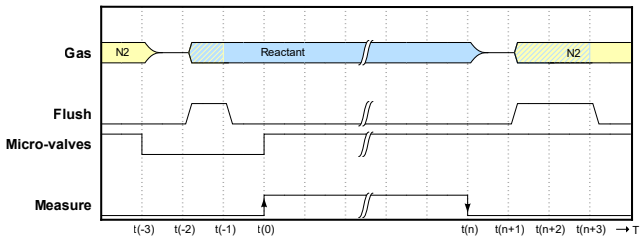


Fig. 11: Operation principle for short transition times without the need for high electric potentials to close the micro valves.

B. Operation principle

To operate at large differential pressures without the need for high electric potentials the following actuation principle was specified (see figure 11): preceding any IR measurement the micro valves are open and the chamber is flushed with N_2 gas at $\Delta p = 200\,\mathrm{mbar}$. At $t_{(-3)}$ the external N_2 valve is closed and simultaneously the micro valves are actuated isolating the reactor chamber. At $t_{(-2)}$ the flush valve is activated and the gas in the supply channel is replaced with reactant gas, denoted by the shaded area in figure 11. Next, the flush valve is closed. At $t_{(0)}$ the micro valves are opened and simultaneously the IR measurement is started, recording the reaction kinetics. At the end of the measurement, at $t_{(n)}$, the reactant gas supply is closed and subsequently N_2 is provided and the flush outlet is opened to fill the supply channel with nitrogen gas (blue shaded area). When the flush valve is closed the pressure in the chamber is increased, opening the pressure relieve valve and therefore flushing the reactor chamber. At this stage the system is ready for the next run.

IV. Results and discussion

In this section fabrication results of the chip are discussed. Because of time restrictions no complete chip was fabricated. To meet the final objective, specific problems that are part of the process flow *"valves and channels"* were solved first (the process flow can be found in supplementary information S7).

The operation of the system is highly dependent on valve function and performance and the construction of the valves also dominates the biggest part of the process flow. At first, this challenge is more important than for example modularity of the system. Since the process flow without system modularity already contains many different process steps that limit the yield, this is excluded from the current process flow.

Other challenges that need special attention are etching the supply and return channels and subsequently bonding

the fragile valve wafer to the MEMpax wafer. Slit dicing and breaking, to access the electric contact pads, is also not straight forward and needs validation.

We started with an $100\,\mathrm{mm}$ wafer box containing 25 P++ DSP wafers and an additional box of P++ single sided polished (SSP) wafers. The wafers in the SSP box were used to verify intermediate process results and are called dummy wafers. We created three different wafer batches to allow evaluation of different fabrication steps in a parallel fashion. During fabrication of certain critical steps these batches were processed gradually in order to prevent wasting all wafers when a single process step failed. Different parts of the process flow were tested independently and are described below.

A. Trench filling for SLE

The 9 to $11\,\mu\mathrm{m}$ valve orifice diameter[10] cannot simply be filled with CVD SiO_2 because of fabrication constrains and this causes high stress levels. We made the decision to reduce the orifice diameter by thermal oxidation of LPCVD poly-silicon. Subsequently a TEOS layer should fill the trench and forms the proper gap spacing for the microvalves. The remaining hole diameter should be less than twice the target valve gap. It turns out that the oxidized poly-silicon layer is 2.19 times the initial layer thickness (an expression for the layer growth by thermal wet oxidation can be found in supplementary information S8.4). With a valve-orifice diameter of 9 to $11\,\mu\mathrm{m}$ and a nitride layer thickness of $500\,\mathrm{nm}$, the poly-silicon layer thickness should be between $1.6\,\mu\mathrm{m}$ and $1.8\,\mu\mathrm{m}$ to ensure the gap can be filled with TEOS but isn't closed in advance.

During the first etch step (etching the SiO_2 layer) damage to the resist layer was observed. The cause of this damage was traced back to stiction of resist to the mask during lithography. Subsequently this resist was stamped to the wafers that followed. All wafers with damaged resist were cleaned with HNO_3 for $5\,\mathrm{min}$, rinsed and dried to allow re-patterning. To limit the amount of wafers with damaged resist, every 5th wafer the mask was cleaned. Either with O_2 plasma or in a bath with *Technistrip D350* and subsequently HNO_3 or rinsed with acetone followed by isopropanol (IPA). The second cleaning method results in the cleanest surface but is most time consuming. Cleaning with acetone and IPA is the fastest method but unfavourable if structures are very small and critical. For mask patterning the in- and outlets, this method is sufficient.

Clean wafers that were more than one day in a box, were cleaned again with either UV-ozone or HNO_3 prior to spin coating resist. This was done in order to remove organic particles, giving a noticeable better result.

Cracks were observed in the positive resist mask (Olin OIR 907-17) when wafers were stored for a longer time in a box prior to plasma etching.[11] This is most likely caused by degradation of resist over time and therefore the loose of elasticity in the layer. To prevent bad results, lithography was always performed less than 2 days before plasma etching.

We used a *PlasmaTherm 790* for SIO_2 etching. It has the advances that four wafers can be processed simultaneously and the wafers aren't fixed by a clamp, enabling the complete wafer surface to be etched. As the plasma is stronger in the center of the reactor chamber, wafers were turned $180°$ half way the etch process. It turned out that despite the symmetric orientation of the wafers inside the chamber, the etch rate was not equal for all wafers (the two in the front were etched faster than the two in the back). Elongation on the total etch time gave rise to the formation of black silicon of the two wafers in the front. Therefore, either the wafers in the back were etched longer after removing the other two wafers or half way the etching process the positions of the wafers were interchanged (and not rotated $180°$). Microscopic inspection was performed on every wafer to verify the result before continuation.

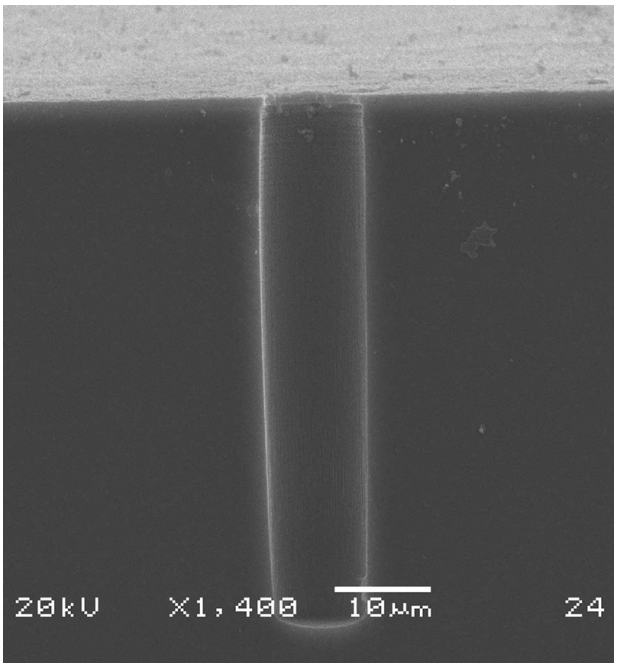


Fig. 12: SEM image of an $11\,\mu\mathrm{m}$ *diameter inlet hole after DRIE.*

The minimal etch depth for the in- and outlet orifices is defined in section II-E. Since the channel diameter is different between the supply and return channel, a RIE lag requires deeper outlet holes (in figure 15 a clear difference can be seen in trench depth between the supply and return channels). The larger the in- and outlet depth the less critical channel etching becomes at the back side of the wafer. The deeper the channel is etched the more fragile the wafer becomes increasing the risk of breaking the wafer during processing. Holes were etched with a depth of 80 to $100\,\mu\mathrm{m}$. This makes trench etching of the supply and return channels on the back side of the wafer considerably less critical

[10]Clarification about different orifice diameters can be found in supplementary information S5

[11]This happened as a consequence of a defect plasma etcher

without putting a restriction to the minimal separation layer thickness that would influence the performance. In figure 12 an inlet hole etched by DRIE is shown. Scallops are visible as a consequence of the used HARS process.

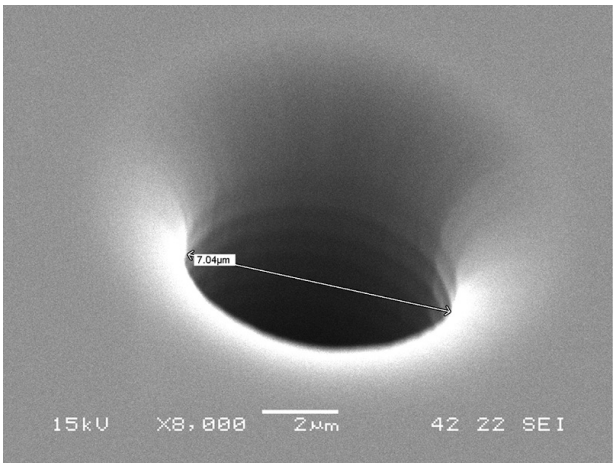


Fig. 13: SEM image of an $11\,\mu\mathrm{m}$ *inlet hole after growing a* Si_3N_4 *and poly-silicon stack.*

The process flow contains numerous different furnace treatments, which are performed one after each other. By proper planning of the furnace sequence a wafer batch can be transported from one furnace to the next without the need for an additional cleaning cycle. To verify the quality of the processed layer, a dummy wafer was always inspected before the next furnace recipe was started. In figure 13 you can see the inlet hole after LPCVD poly-silicon, showing a smooth surface.

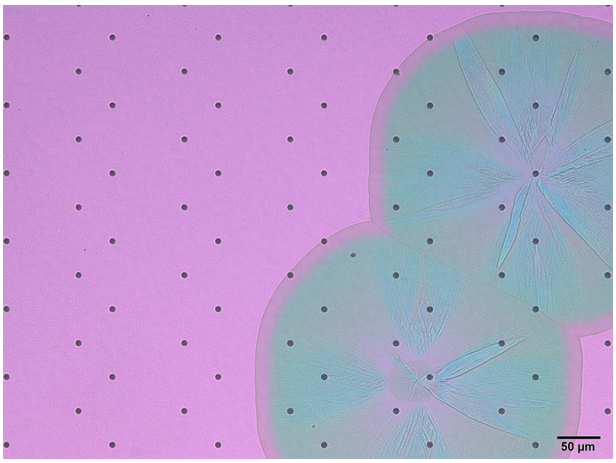
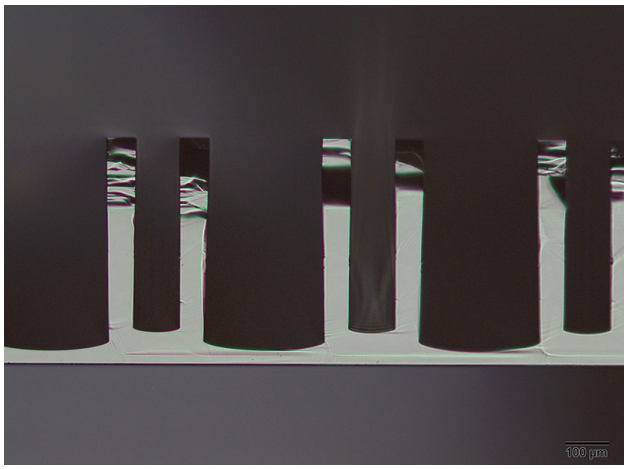
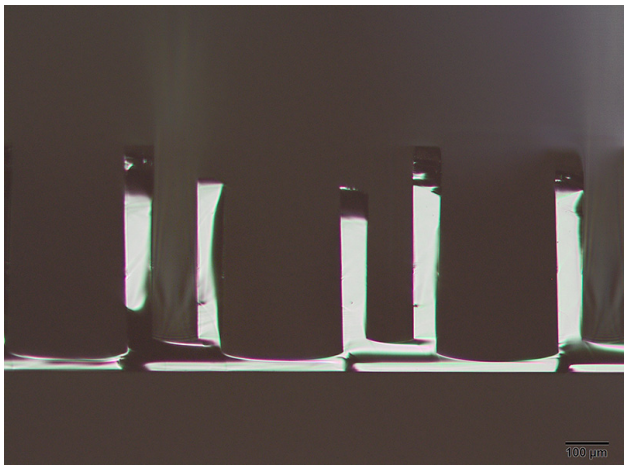


Fig. 14: Optical microscope image showing two delamination spots across multiple in- and outlet holes

Wafer inspection after thermal oxidation of poly-silicon showed delamination of either the oxide or nitride layer, possibly caused by extensive stress. To verify this the wafer bow was measured before and after stripping oxide from the frontside of the wafer using 50%HF.[12] During wet etching the backside was protected with dicing foil, laminated onto it after an UV-ozone treatment (to promote adhesion), because photo resist cannot be used as it dissolves in 50%HF. The measured deflection before and after etching was respectively $7.0\,\mu\mathrm{m}$ and $201.1\,\mu\mathrm{m}$ which indeed confirmed high stress levels in the oxide layer (we used a *Veeco Dektak 8a* surface profiler). To lower the stress, the poly-silicon was etched back till the nitride layer prior to thermal oxidation of poly-silicon of the holes. In addition, the furnace recipe was modified to slow down the transport arm during loading and unloading from $30\,\mathrm{cm/min}$ to $10\,\mathrm{cm/min}$. However, the nitride layer still showed delamination across the wafer, see figure 14. This can possibly be solved by using a smaller ramp up/down time during wet oxidation, lowering the oxidation temperature or use other SLE materials to prevent development of extensive stress in the layers. Additional photos are shown in supplementary information S9 figure 37.



(a) Region of wafer were channel walls are still intact



(b) Region of wafer were mask is partly etched away and channel walls are damaged

Fig. 15: Microscopy image of cross view channels after 1237 cycles DRIE

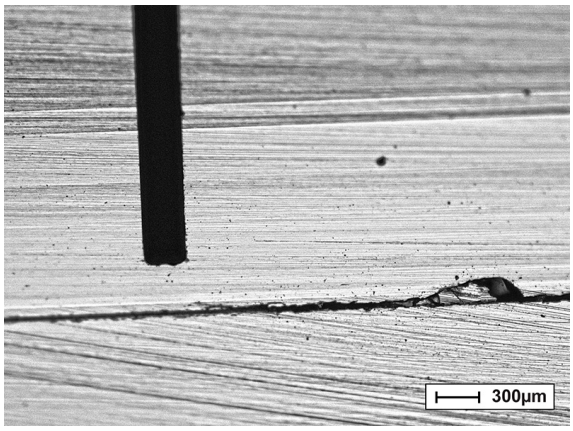
[12] 50%HF was also used to identify the oxide layer as shown in supplementary information S9 figure 36

B. Supply and return channel etching

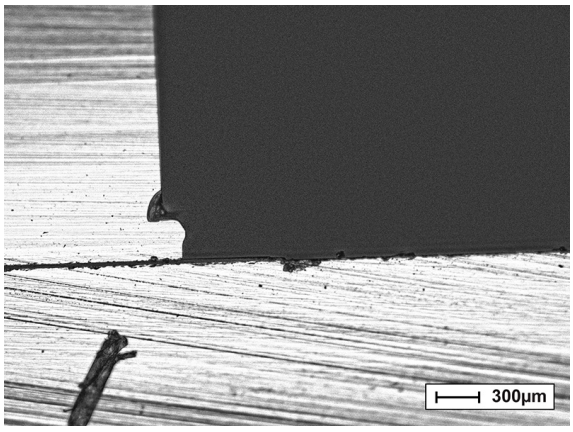
The SiO_2 layer that was grown by wet oxidation early in the fabrication process (1.4 to $2\,\mu m$ thick) was used as etch mask for the in- and outlet orifice etching as well as channel trench etching (see subsection III-A). A HARS DRIE recipe was used for etching the backside of the wafer. Etch results were verified every 200 cycles starting at cycle 600. At approximately 1200 cycles there was no etch mask left in the center region and the etch rate was significantly increased due to the loss of etch selectivity. Additional experiments were performed with an oxide mask of $5.7\,\mu m$ thick (measured with Woollam M-2000UI ellipsometer) and extra thick resist ($5\,\mu m$, measured with Veeco Dektak 8 surface profiler). To solve cracking problems of the thick resist layer, the post-exposure bake was omitted, the performed hard bake had a temperature of $150\,^{\circ}C$ and the ramp up/down time was $10\,^{\circ}C\,min^{-1}$. Even though the etch mask thickness was more than doubled, only a few extra cycles could be etched before damage to the channel walls occurred. Regions without etch masks were perforated quickly as a consequence of locally increased etch rates.[13] In figure 15 an un-damaged and a damaged part of the wafer are shown. Note that the retrograde tapering is very limited resulting in nice straight channel walls. Fast etching of the mask as a consequence of the loss of selectivity between silicon and the etch mask can be explained by a rising temperature of the channel walls. This is possibly a result of bad thermal conduction caused by the trenches becoming deeper. Therefore, the existing recipe needs to be optimized to limit the temperature of the channel walls. A possible solution is to change from a fast to a slow recipe (possibly halfway the target channel depth) or create a recipe that includes a ramp-function, increasing the interval between two etch steps over time. Another option is to include delay functions that enable the walls to cool-down. The chuck temperature can be lowered as well, but this directly effects the ratio between the physical and chemical etch rate (effecting the etch slope). Also modifying the design, by lowering the target channel depth, can be considered as a solution since the problem only arises when the trenches approach the thickness of the wafer. A recipe with a much higher selectivity was also tested but suffered from the formation of black silicon (see supplementary information S9 figure 39).

C. Slit dicing and breaking to access electric contact pads

SU-8 was used as an alternative material to poly-silicon as spacer to fix the *IRE wafer* with adhesive bonding to the rest of the chip. This highly simplifies the process flow[14]. As SU-8 spin coating is not possible if the wafer contains holes, DRIE should be performed after spin coating the resist. However, if the holes are etched and the SU-8 layer gets contaminated during etching, adhesive bonding of the SU-8 layer is not longer possible. Creating holes in the MEMpax wafer by powderblasting is very easy but the need of creating electrodes on the other side of the *valve wafer* makes fabrication of the device much more complicated. Therefore, a two-step dicing process is proposed in order to create access to the electrical contact pads on the *valve wafer*. This process also eliminated the need for an extra etch mask for DRIE.



(a) A part of the top wafer is diced, resulting in a $450\,\mu m$ deep slit



(b) Part of the top wafer is broken and removed

Fig. 16: Microscopy image of wafer cross view of two silicon wafers bonded together with SU-8 to test local slit dicing and breaking.

For the contact pad access, additional slits were defined on mask 8 to locally remove the silicon of the *IRE wafer* (the mask is shown in supplementary information S5 figure 32). This method has been tested using two silicon wafers bonded together with patterned SU-8. A $300\,\mu m$ and $50\,\mu m$ dicing blade were used to create slits that go almost, but not completely, through the top wafer (see figure 16a for $300\,\mu m$ wide slit). Next, tweezers were used to locally create a high force near the slit in order to break the top side that was not bonded with SU-8 (see figure 16b). As can be seen, the break line is not very straight but since the electric contact pads are relatively large (more than $700\,\mu m$ diameter) this

[13]Photos of the wafer backside where the mask is partly removed and the wafer is damaged are shown in supplementary information S9 figure 38

[14]Note: SU-8 limits the maximal operation temperature to about $200\,^{\circ}C$

does not cause any problems.[15]

Some additional results of SLE trench filling and discussions about TEOS deposition, wafer bonding alternatives, experimental setup and valve performance considering surface roughness and particles can be found in supplementary information S8 and S9.

V. Conclusions

In order to gain sufficient control over the mass transport, a chip design is proposed with 5125 integrated microvalves and with a chip volume of less than $1\,\mu L$. Analysis in COMSOL has shown transition times of less than $80\,\mu s$ at the active sensing surface area. Incorporating the microvalve switching speed and the hydraulic network, the total transition takes less than $200\,\mu s$. The designed system can measure the reaction kinetics at a maximum temperature of $450\,^{\circ}C$. An operation scheme is proposed to allow a differential pressure of minimal $2\,bar$ and a gas operation pressure up to $10\,bar$ to enhance the mass transport and detectability of gases in the chamber. A fabrication process flow is proposed, containing a novel dicing method to access electric contact pads located in the center of a three wafer sandwich.

Realization of the platform creates the opportunity to perform measurements to the reaction kinetics in a time scale that was never possible before.

VI. Recommendations for further research

The project is in an early stage of development and much work still needs to be done. The proposed process flow in the paper contains critical fabrication challenges that need to be solved before complete chip fabrication becomes feasible. Trench filling the $11\,\mu m$ wide in- and outlet holes and channel etching described in section IV both need special attention. The use of SU-8 as spacer and bonding material makes valve characterization possible without the need for a chip-clamp. In order to meet the predicted transition time a chip-clamp is needed to limit deflection of the layers. This clamp also facilitate heating up the device. SU-8 need to be replaced in order to operate the chip at high temperatures (up to $450\,^{\circ}C$). The transition time can be validated, without a catalyst, by flushing a nitrogen pre-filled micro chamber with carbon dioxide and measuring the time it takes for the carbon dioxide to replace the nitrogen gas.[16]

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[15] The results using the $50\,\mu m$ dicing blade can be found in supplementary information S9 figure 40

[16] More details can be found in supplementary information S8.

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SUPPLEMENTARY INFORMATION

S1 Channel and cell geometry decisions

Besides the fixed reactor chamber surface and valve dimensions the channels and cell dimensions also needs to be chosen. The maximal supply and return channel dimensions are directly related to the single reactor cell dimensions. Since the transition time is proportional to the hydraulic resistance of the microfluidic network it is important to gain insight in the effect of the different components on the total hydraulic resistance.

Because of both time restrictions and the early design phase, in which proofing the working principle of the highly parallelized micro valves is more important than obtaining the best performance of the proposed design concept, we solved the problem by simple numerical parametric approximation using the matlab script shown in listing 1. At first the hydraulic resistance of a single reactor cell is calculated and separated in two parts: cell length resistance and in- and outlet resistance including valve. We used COMSOL to determine the volumetric flow rate at the outlet with a fixed differential pressure for a single reactor cell of respectively $500\,\mu\mathrm{m}$ (R0) and $1000\,\mu\mathrm{m}$ (R1).[23] The length resistance (R_l) is calculated by subtracting R0 from R1. The in- and output resistance are calculated by subtracting the cell length resistance from the total single cell resistance of R0.

If we take a single cell length of $500\,\mu\mathrm{m}$ we get a chamber density of 5125 microvalves. In that case, the outlet channel resistance isolated from the rest of the hydraulic network can be seen as 21 vertical oriented channels that are connected by short horizontal channels. Because the meander shaped supply channel is enclosed by two return channels, anti parallel oriented, the return channel resistance is divided by two. Every vertical channel contains 125 reactor cell outputs that are evenly spread along the channel, therefore, we take for the vertical channel 50% of the maximal resistance of that channel end.

Listing 1: Matlab script used for hydraulic resistance calculations as a function of chip dimensions

```
function main

clc
clear all;
close all;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Hydraulic resistance
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
mu=2.29e-5;     % Viscosity (Pa*s) for N2 (https://www.lmnoeng.com/Flow/GasViscosity.php)

%Single cell resistance (including valve gap!)
Q0=1.8347e-9;   % Volumetric flow rate [for 500um] (m3/s)
Q1=1.6511e-9;   % Volumetric flow rate [for 1000um] (m3/s)
P=2e5;          % 2bar differential pressure (Pa)
R0=P/Q0;        % Hydraulic resistance of single cell for 500um
R1=P/Q1;        % Hydraulic resistance of single cell for 1000um

disp(['Total single cell resistance resp. 500um, 1000um; ',num2str(R0*1e-12),' : ', ...
    num2str(R1*1e-12),' x 10^12 (N/m2)/(m3/s)']) %

R_t=R0;         % Total single cell resistance for 500um
R_l=R1-R0;      % Single cell length resistance for 500um
R_v=R0-R_l;     % Single valve (incl. in/outlet) resistance

disp(['Resistance for 500um resp. R_t, R_v, R_l; ',num2str(R_t*1e-12),' : ', ...
    num2str(R_v*1e-12),' : ',num2str(R_l*1e-12), ' x 10^12 (N/m2)/(m3/s)'])   %
disp(['Resistance ratio for 500um resp. R_t, R_v, R_l; ',num2str(100),'% : ', ...
    num2str(100*(R_v/R_t)),'% : ',num2str(100*(R_l/R_t)), '% '])   %

%disp('######')
disp(' ')

%Inlet tubing calculation
r1=0.6985e-3;   % 0.6985mm
L1=1e-1;        % Tube length 10cm
R2=(8*mu*L1)/(pi*r1^4);
disp(['Tube inlet resistance: ',num2str(R2*1e-6),' x 10^6 (N/m2)/(m3/s)'])   %

%Outlet channel resistance calculations
%Comb vinger (vertical channel)
H2=470e-6;      % 470um deep channel
W2=100e-6;      % 100um channel width
L2=10e-3;       % 10mm Combfinger length
```

```
%Connection channel (horizontal channel)
H3=H2;          % Identical channel constant
W3=200e-6;      % 200um channel width
L3=1.2e-3;      % 1200um connection channel length

R3=((12*mu*L2)/((1-(0.63*(W2/H2)))*W2^3*H2))/2;  % Comb finger resistance / 2
R4=((12*mu*L3)/((1-(0.63*(W3/H3)))*W3^3*H3));    % Connection channel resistance
R_sum1=R3+R4;
for n=(20):-1:1
 R_sum1=(((R_sum1^-1)+(R3^-1))^-1)+R4;
end
R_sum1=R_sum1/2;    % 21 combdrives on both sides (thus parallel)
disp(['Outlet channel resistance: ',num2str(R_sum1*1e-6),' x 10^6 (N/m2)/(m3/s)'])   %

%Inlet channel resistance calculations
H4=470e-6;      % 470um deep channel
W4=260e-6;      % 260um channel width
L4=10e-3;       % 10mm Combvinger length
%Connection channel (horizontal channel)
H5=H2;          % Identical channel constant
W5=W4;          % 260um channel wdith
L5=785e-6;      % 750um connection channel length (corner)

R4=((12*mu*L4)/((1-(0.63*(W4/H4)))*W4^3*H4));   % Single part (corner to corner) of meander channel
R5=((12*mu*L5)/((1-(0.63*(W5/H5)))*W5^3*H5));   % Connection channel resistance

R_sum3=41*(R4+R5)+2*R5;  % Total hydraulic resistance of supply channel (if no reaction cells ...
    parallel)
%disp(['Total supply channel resistance: ',num2str(R_sum3*1e-9),' x 10^9 (N/m2)/(m3/s)'])   %

%Supply channel resistance between two inlets (separated 80um)
H6=H4;      %
W6=W4;      %
L6=80e-6;   %
R6=((12*mu*L6)/((1-(0.63*(W6/H6)))*W6^3*H6));   % Supply channel resistance between two inlets

disp(['Supply channel resistance between two inlets: ',num2str(R6*1e-6),' x 10^6 ...
    (N/m2)/(m3/s)'])   %

%Resistance of supply channel with reactor chamber (tube and outlet resistance ignored)
R_sum4=R0+R6;   % First valve (end of meander channel)
x=124;
for n=(41):-1:1
 for m=x:-1:1
     R_sum4=((R_sum4)^-1+(R0^-1))^-1+R6;    % Cell+80um channel parallel to another cell
 end
 x=125;
 R_sum4=R_sum4+R5;  % Add corner resistance
end
R_sum4=R_sum4+2*R5;    % Correction factor of return and supply channel to tubing

disp(['Reactor chamber resistance with supply channel (5125 valves): ',num2str(R_sum4*1e-9),' x ...
    10^9 (N/m2)/(m3/s)'])   %

end
```

Listing 2: Matlab output used for hydraulic resistance calculations as a function of chip dimensions

```
Total single cell resistance resp. 500um, 1000um; 109.0096 : 121.1314 x 10^12 (N/m2)/(m3/s)
Resistance for 500um resp. R_t, R_v, R_l; 109.0096 : 96.8879 : 12.1217 x 10^12 (N/m2)/(m3/s)
Resistance ratio for 500um resp. R_t, R_v, R_l; 100% : 88.8801% : 11.1199%

Tube inlet resistance: 24.4968 x 10^6 (N/m2)/(m3/s)
Outlet channel resistance: 349.611 x 10^6 (N/m2)/(m3/s)
Supply channel resistance between two inlets: 4.0849 x 10^6 (N/m2)/(m3/s)
Reactor chamber resistance with supply channel (5125 valves): 28.4149 x 10^9 (N/m2)/(m3/s)
```

As can be seen in listing 2 the hydraulic resistance of a single cell is a few orders of magnitude larger than the tubing and outlet channel resistance. More reactor cells in parallel favour a lower hydraulic resistance as long as the total reactor chamber resistance is larger than the other components in the hydraulic network. The optimal width of the supply and return channels still needs to be found. They are directly related to each other since the width of the channel walls is

fixed by fabrication constraints. Either simulation software can be used or a mathematical model can be derived to relate these parameters to the total hydraulic resistance of the network.

S2 Effect of valve material type to the transition time

Mass transport analysis executed in COMSOL (Section II-C) showed a transition time for the reactor cell of approximately $80\,\mu s$, excluding the time elongation caused by the limited microvalve switching speed. Test results of the microvalves developed by Dubois et al. ([19]) showed a maximal switching speed of about $100\,\mu s$. When the microvalves are actuated but not fully opened, there is already a reduced gas flow through the valves. Therefore, the transition time is not simply the sum of the two contributions but the effect of the microvalve switching speed will be a substantial part of the total transition time.

The switching speed of the microvalves is negatively affected by the RC-time as a result of parasitic effects and this negative effect becomes more prominent when thinner membranes and layers are used. The parasitic resistance of the microvalves described by Dubois et al. ([19]) is rather limited as the resistivity of the used metal is rather low.[29, p. 762] As the chemical application puts a restriction to the use of materials for the construction of the valves a comparison is made for the RC-time between a good conducting metal (platinum) and a heavily doped boron silicon membrane. As the silicon layer has a resistivity that is 5 orders of magnitude bigger than the metal, we expect a noticeable shift in RC-time.[30][29, p. 762]

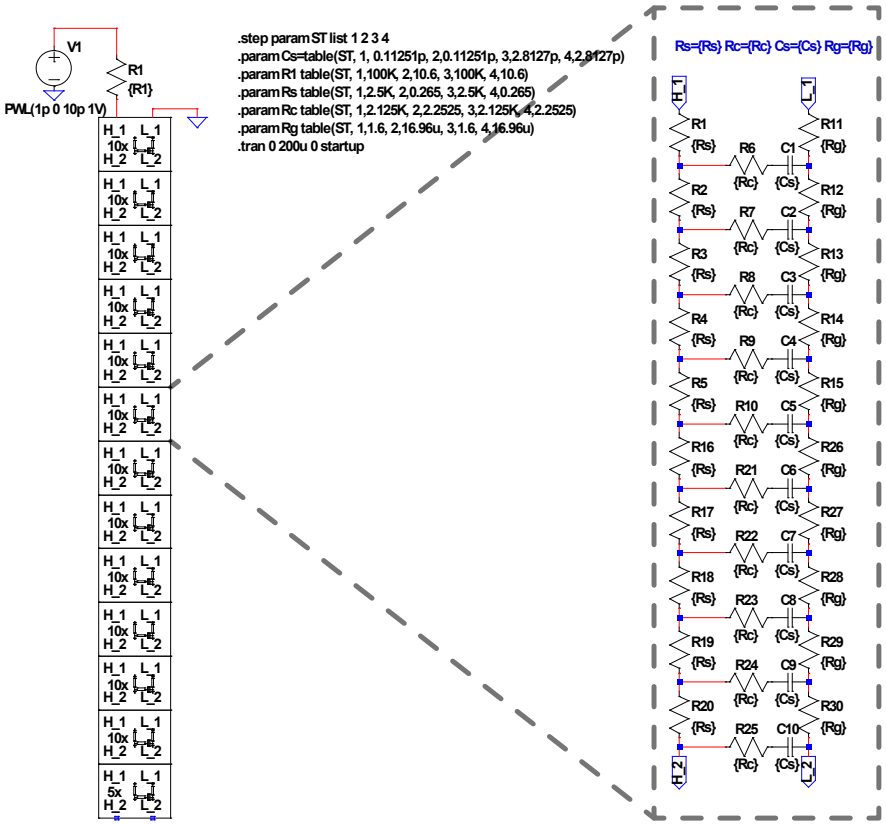


Fig. 17: LTspice simulation model containing one compete valve array of parallel connected microvalves

A simplified RC-model of a single array of 125 microvalves connected in parallel was simulated using LTspice (see figure 17). The rise time of the power supply was set to $10\,ps$ and we used a Matlab script to determine the remaining simulation parameters using the microvalve array dimensions (see listing 3). For both, the open ($Gap = 1.5\,\mu m$) and closed valve state, the capacitance was determined incorporating a $500\,nm$ thick nitride layer (valve seat). The device geometry was used to determine the resistance between two valves (Rs) and the parasitic series resistance of the capacitor (Rc). The resistance between the power supply and a single valve array (R1) was based on the first valve column as this is the longest resistor track between a valve column and the electric contact pads located at the sides of the chip (see supplementary information S5 for electrode positioning). It needs to be said that this is only a rough estimation and verification data is preferred to improve the validity of the model. The same applies for the ground plane resistance (Rg) as it is difficult to determine the actual substrate conductance between two valve nodes. See listing 4 for the parameters used in the LTspice model.

Listing 3: Matlab script used for parameter estimation for the LTSpice RC-time simulation model

```
function main

clc
clear all;
close all;

Rho_pt= 1.06e-7;    % Resistvity: Platium [Ohm*m]
Rho_si= 1e-2;       % 1e19 P++ Boron doped silicon

%Capacitance of one valve:
e0= 8.854187817e-12;     % Vacuum permitivity
e_air = 1;               % Gas permitivity
e_SiN = 8;               % Silicon nitride permitivity ...
    (https://www.ceramicindustry.com/ext/resources/pdfs/2013-CCD-Material-Charts.pdf)
Gap=1.5e-6;              % Air gap 1.5um
D_n=5e-7;                % 500n nitride layer
A=pi*(50e-6)^2+(240e-6*40e-6); % Area of valve

C_air=(e0*e_air*A)/Gap; % Capacitance of air gap (gas) 1.5um
C_SiN=(e0*e_SiN*A)/D_n; % Capacitance of nitride layer 500nm

C_o=(C_air^-1+C_SiN^-1)^-1; % Total capacitance when valve is open
C_c=C_SiN;                  % Capacitance when valve is closed

disp(['Single valve capacitance open/closed: ',num2str(C_o*1e12),' , ',num2str(C_c*1e12),' x ...
    10^-12 F'])   %

%/2 since valve is connected on both sides
R1_si=((Rho_si*(4e-3))/(1e-6*200e-6))/2;  % Resistance between array and supply (rough estimation)
Rs_si=((Rho_si*(80e-6))/(1e-6*160e-6))/2; % Distance between two valves
Rc_si=((Rho_si*(170e-6))/(1e-6*40e-6))/2; % Valve is connected on both sides: length/2
Rg_si=(Rho_si*(80e-6))/(500e-6*1e-3);     % Ground plane resistance (estimation)
disp(['Si: R1, Rs, Rc, Rg: ', num2str(R1_si),' , ',num2str(Rs_si),' , ', num2str(Rc_si),' , ', ...
    num2str(Rg_si),' Ohm'])   %

R1_pt=((Rho_pt*(4e-3))/(1e-7*200e-6))/2;  % Thin layer over silicon (100nm)
Rs_pt=((Rho_pt*(80e-6))/(1e-7*160e-6))/2; %
Rc_pt=((Rho_pt*(170e-6))/(1e-7*40e-6))/2; %
Rg_pt=(Rho_pt*(80e-6))/(500e-6*1e-3);     %
disp(['Pt: R1, Rs, Rc, Rg: ', num2str(R1_pt),' , ',num2str(Rs_pt),' , ', num2str(Rc_pt),' , ', ...
    num2str(Rg_pt),' Ohm'])   %

end
```

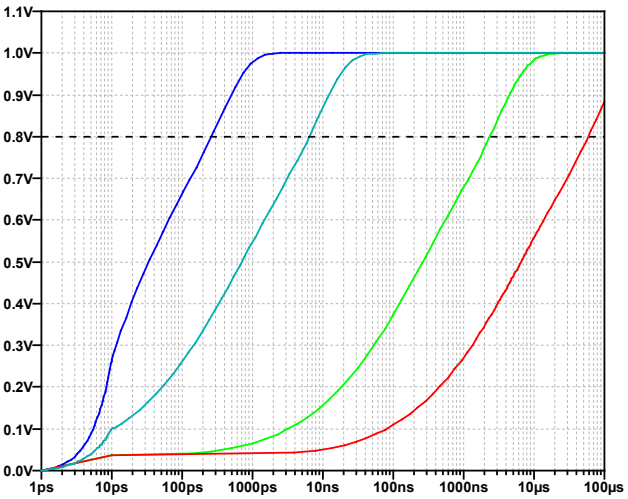
Listing 4: Matlab output for parameter estimation used for LTSpice RC-time simulation model

```
Single valve capacitance open/closed: 0.098906 , 2.4727 x 10^-12 F
Si: R1, Rs, Rc, Rg: 100000 , 2500 , 21250 , 1.6 Ohm
Pt: R1, Rs, Rc, Rg: 10.6 , 0.265 , 2.2525 , 1.696e-05 Ohm
```

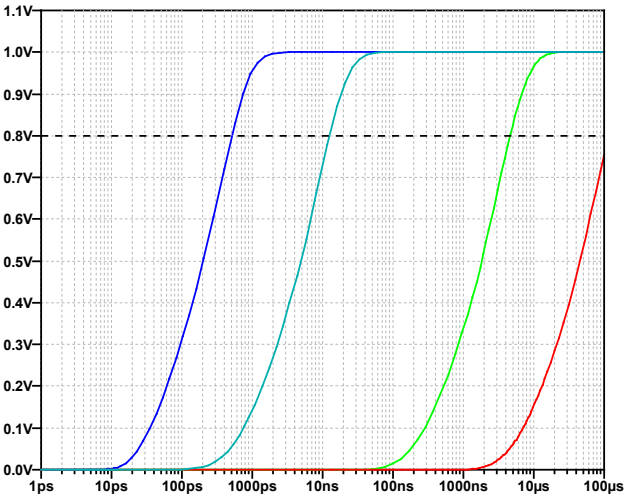
The simulation showed the potential as a function of time for the metal and doped silicon for the open valve state as well as for the closed state. The results for valve 1 and valve 60 are shown in figure 18 in which at $t = 0$ the valves have zero charge. In the figure you can see clearly that the RC-time for the highly doped silicon is 4 orders of magnitude larger than for the metal. The RC-time for metal is only a fraction of the total switching speed of the valve and as a consequence it can be ignored. For the doped silicon instead, the RC-time is in the microsecond domain and therefore the effect on the transition time of the system should be considered.

When a valve is in an actuated state, such that the membrane is in the closed position, the valve capacitance has its maximum value. At the moment that the valve is initiated to open by discharging the parallel plates the charge density should drop below a certain threshold before the membrane will show any displacement. At the moment $Gap > 0$ the F_{el} contribution to the force balance decreases exponentially due to the increased valve gap. In addition, neighboring valves that are already in a more open state will enhance the switching speed as the valves are interconnected. Therefore we expect that the effect of the RC-time when doped silicon is used instead of a metal does not significantly increase the transition time of the system.

Note that parameter estimations and the simulation model are highly simplified and therefore besides parameter validation with experimental data, also model improvements are needed in order to make accurate predictions about the real RC-time.



(a) Valve 1



(b) Valve 60

Fig. 18: LTspice simulation results, darkblue: open valve - metal, lightblue: closed valve - metal, green: open valve - doped silicon, red: closed valve - doped silicon

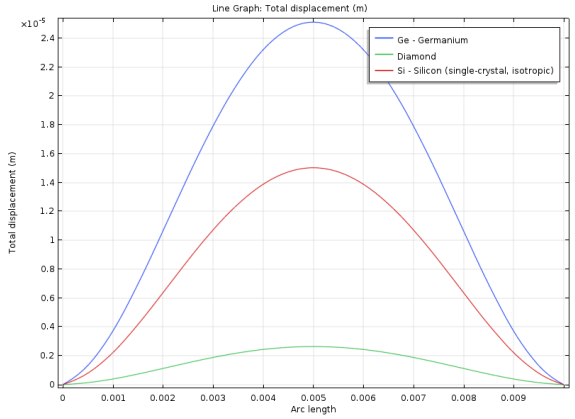
S3 IRE and membrane deflections as a result of high differential pressure

The chip has two areas where relative large deflections can effect the operation of the chip as a result of a high differential pressure across a layer. These were simulated with structural mechanics models in COMSOL. The IRE has a large area where the differential pressure can exceed $10\,\mathrm{bar}$. The deflection of this wafer can influence the path that light will take through the crystal but also affects the reaction chamber volume. Also the separation layer between the supply channel and the reaction chamber is relatively small and therefore it is also sensitive to deflections. If this separation layer experiences large deflections with respect to the valve dimensions this can increase the valve leakage as well as the maximal throughput when the valve is open.

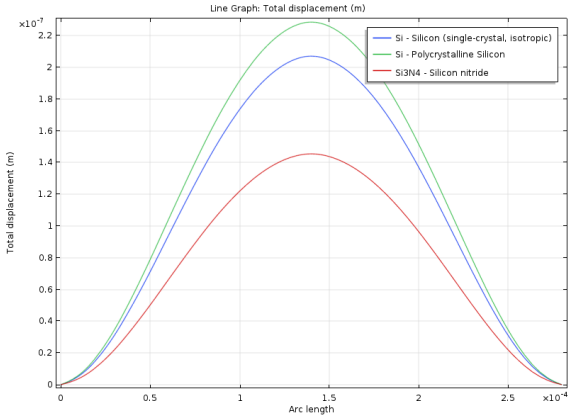
For both simulation models we choose the parameters to mimic a worst case scenario. For example the differential pressure across the IRE was set to $12\,\mathrm{bar}$. And for the channel width a value of $280\,\mu\mathrm{m}$ instead of $260\,\mu\mathrm{m}$ was used to anticipate for possible negative tapering effects (channel widening) as a result of the used fabrication method.

The simulation results are shown in figure 19. For the IRE we compared silicon with diamond and germanium as both materials can be used as IR crystal. The deflection shown in figure 19a is very small compared to the chamber area and therefore we expect that the effect on the internal reflection is negligible. However, the deflection can significantly change the reactor chamber volume since the initial chamber height is only $5\,\mu\mathrm{m}$. As this will change the mass transport across the chamber, the transition time is also directly effected. When operating the chip at high pressures using silicon as IRE it becomes necessary to use a rigid clamp. In this scenario, we can instead use diamond, as this material is much stiffer. However, the clamp should also prevent bond breaking as a result of excessive stress and in addition it is responsible for the electrical and fluidic interconnection to the rest of the setup.[25]

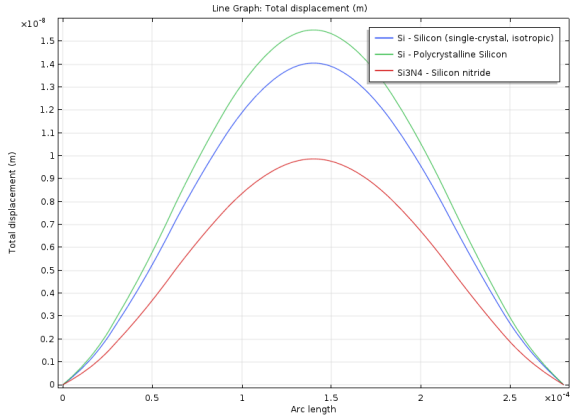
In figures 19b-d the deflections of the separation layer between the chamber and the supply channel is shown. The thinner the separation layer the lower the hydraulic resistance of the channels and in- and outlet orifices, which is favourable for short transition times. Because of fabrication limitations there is a certain degree of non-uniformity across the chip resulting in different thicknesses. Hence, we defined a minimum separation layer thickness of $25\,\mu\mathrm{m}$ which gives a deflection of less than 1% of the initial valve gap.



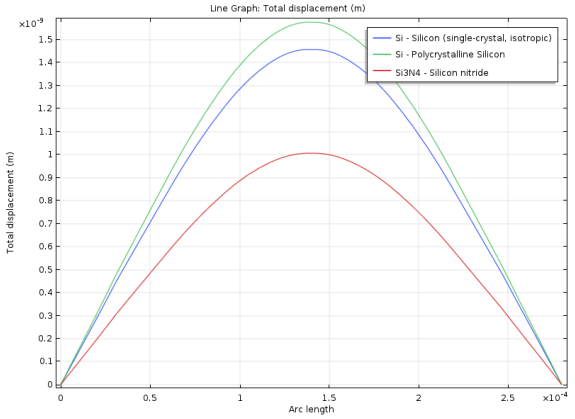
(a) 510 µm thick IRE



(b) 10 µm thick separation layer



(c) 25 µm thick separation layer



(d) 60 µm thick separation layer

Fig. 19: Results COMSOL structural mechanics deflection model

S4 Process outline

The complete process outline is shown in figure 20 and figure 21. Below the figures a list is given that shows the high-level actions to be executed per step.

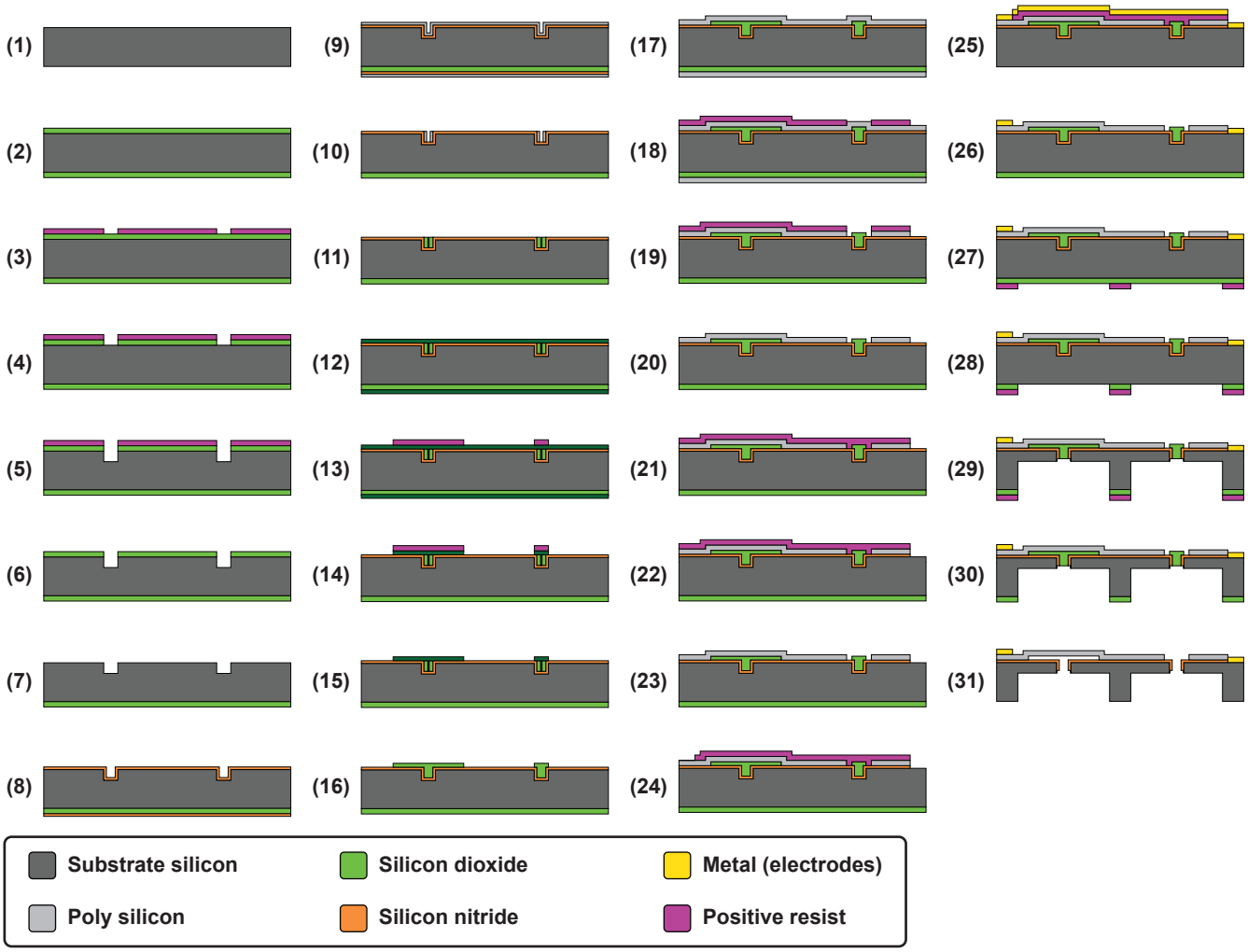


Fig. 20: Process outline of the valve wafer

List of actions per step of figure 20:

(1) 100mm P++ Boron <100> DSP Si *valve wafer*
(2) Wet oxidation Si
(3) Lithography mask 1
(4) RIE SiO_2
(5) DRIE Si
(6) Resist and FC strip
(7) RIE SiO_2
(8) LPCVD Si_3N_4
(9) LPCVD poly-Si
(10) DRIE poly-Si frontside
DRIE poly-Si backside
RIE Si_3N_4 backside
FC strip
(11) Wet oxidation poly-Si
(12) LPCVD TEOS
(13) Lithography mask 2
(14) RIE TEOS frontside
RIE TEOS backside
(15) Stripping resist
(16) Annealing
(17) LPCVD poly-Si
Boron SSD
(18) Lithography mask 3
(19) DRIE poly-Si

(20) Resist strip
Annealing (poly-Si)
(21) Lithography mask 4
(22) RIE Si_3N_4
(23) Resist strip
(24) Lithography mask 5
(25) Sputtering Cr
Sputtering Pt
(26) Lift-off
(27) Lithography mask 6
(28) RIE SiO_2
(29) DRIE Si
(30) Resist and FC strip
(31) 50%HF SiO_2 etching
Freeze drying

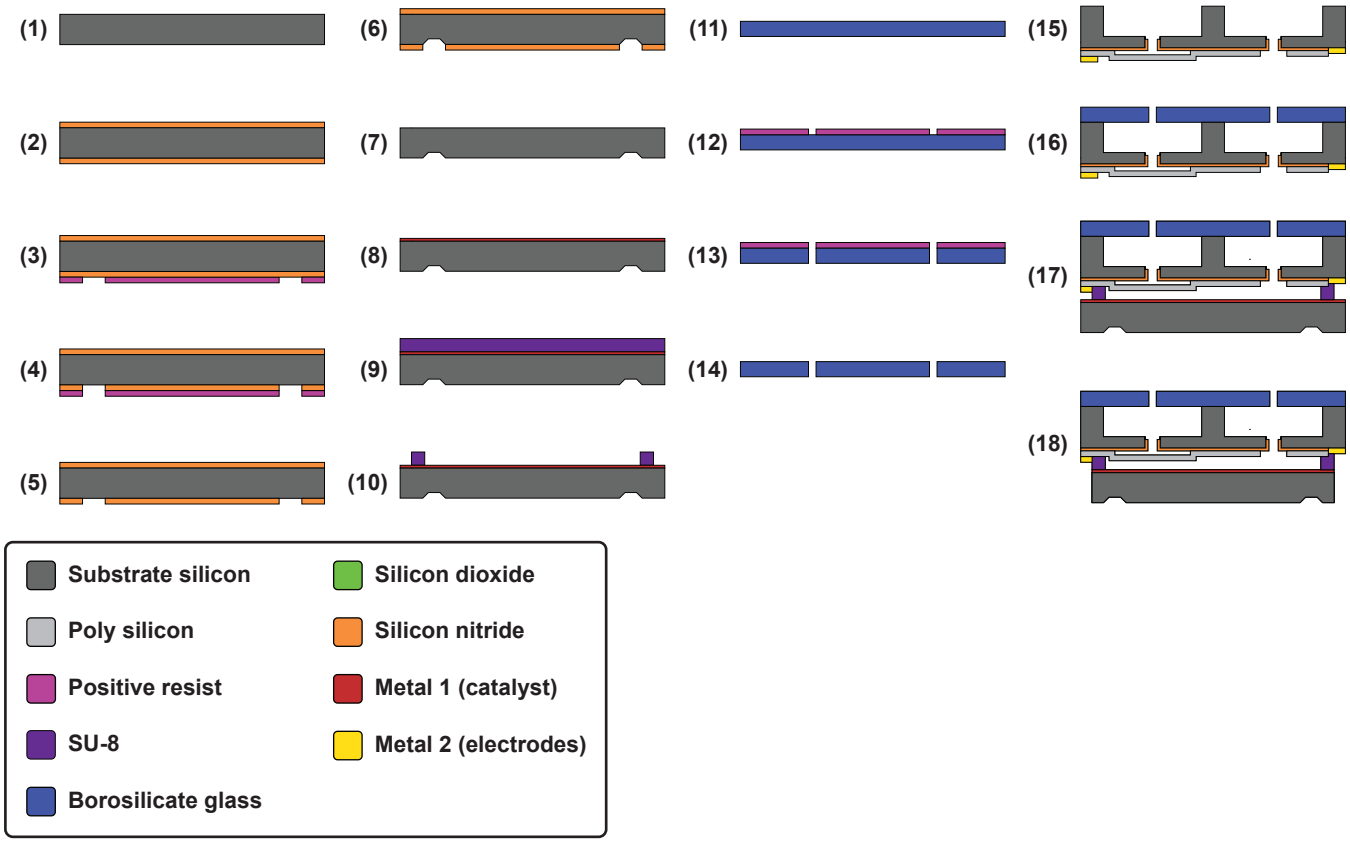


Fig. 21: Process outline of the IRE wafer, powderblasting and total assembly

List of actions per step of figure 21:

(1) 100mm undoped <100> DSP Si *IRE wafer*
(2) LPCVD Si_3N_4
(3) Lithography mask 8
(4) RIE Si_3N_4 backside
(5) Resist strip
(6) KOH Si etch
(7) 50%HF Si_3N_4
(8) Sputtering catalyst
(9) Spin coating SU-8 (negative resist)
(10) Lithography mask 9
(11) 100mm MEMpax glass wafer
(12) Resist foil lithography mask 7
(13) Powderblasting
(14) Remove foil
(15) Valve wafer (M)
(16) Anodic bonding *MEMpax wafer* to *valve wafer*
(17) Adhesive bonding of *valve wafer* to *IRE wafer*
(18) Dicing electric contact slits (marks mask 8)
Dicing chips

S5 Masks

The masks that are used in the process flow are designed in CleWin and shown in figure 25 to 33. A 100 mm wafer mask template provided by the NanoLab (MESA+ - University of Twente) was used as basis, containing alignment marks, supporting text and frames. In order to align 9 different masks the alignment marks table was extended and modified (see figure 22). To limit the need to etch large areas the indication arrows on the template, generally used during lithography, were modified from a large triangle to multiple small triangles in the shape of the original large one (maximal diameter was restricted to 10 µm), see figure 23. Other large structures were removed for the same reason. For producibility and robustness the masks were designed to allow for maximal miss-alignment during fabrication by reducing or extending certain areas on the chip making the alignment process as non-critical as possible.

Figure 24 gives a general overview of the different sections on the wafer. As can be seen, the wafer contains 6 normal chips of 3 different orifice diameters. Since the nitride layer has a thickness of 0.5 µm the default orifice diameter is 11 µm. However, also 10 µm and 9 µm diameter chips are added to the design as trench filling of a smaller diameter is easier. The masks contain also multiple test chips with only a single valve or two valves interconnected. These can be used to test individual valve functionality and performance and are designed for easy handling. For example the electrodes are large and it allows easy fixation of tubing without the need for a chip clamp. The masks also contain some test structures that are used to verify intermediate fabrication results, these are located at the edge of the wafer.

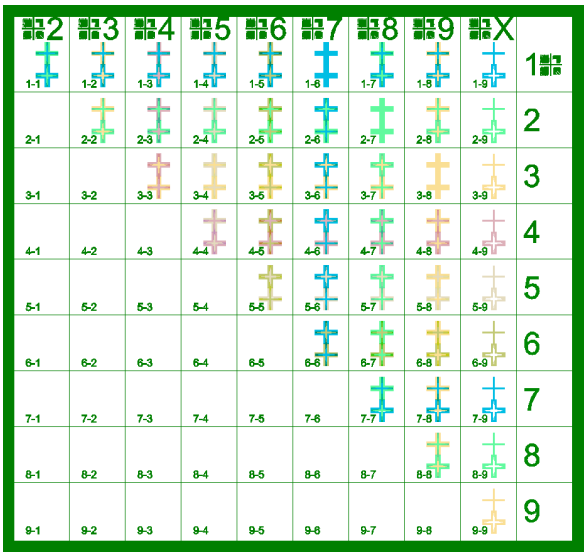


Fig. 22: Alignment marks table for alignment up to 10 different masks

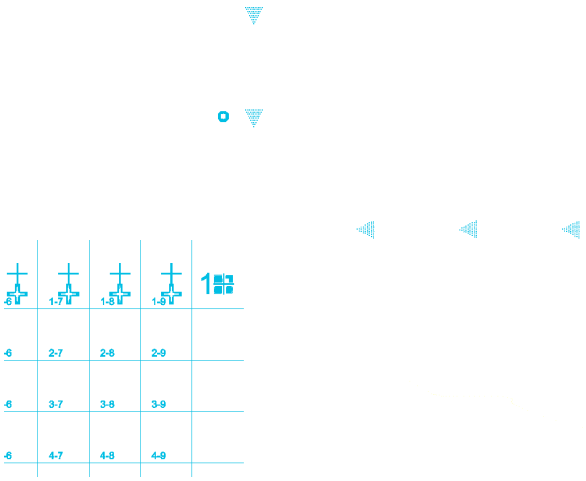


Fig. 23: Alignment mark indicator triangles consisting of multiple small triangles

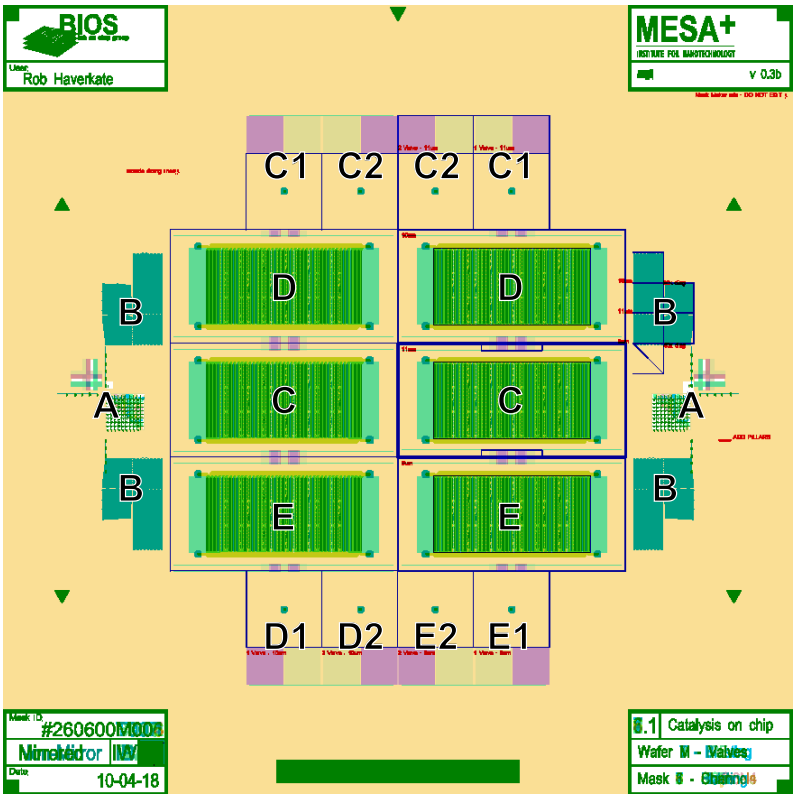


Fig. 24: Mask sectioning: A: alignment marks, B: mask1 high density hole patterns, C,D,E: chips with respectively 11 µm, 10 µm *and* 9 µm *orifice diameter, Cx,Dx,Ex: test chips where x denotes the amount of valves.*

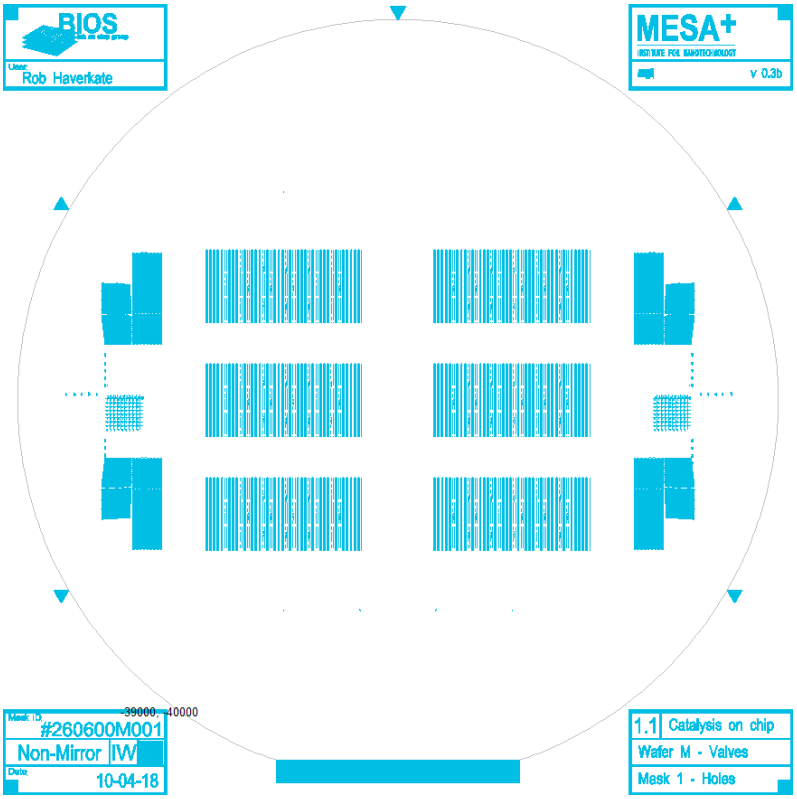


Fig. 25: Mask 1, used for patterning the in- and outlet valve orifices in the silicon substrate.

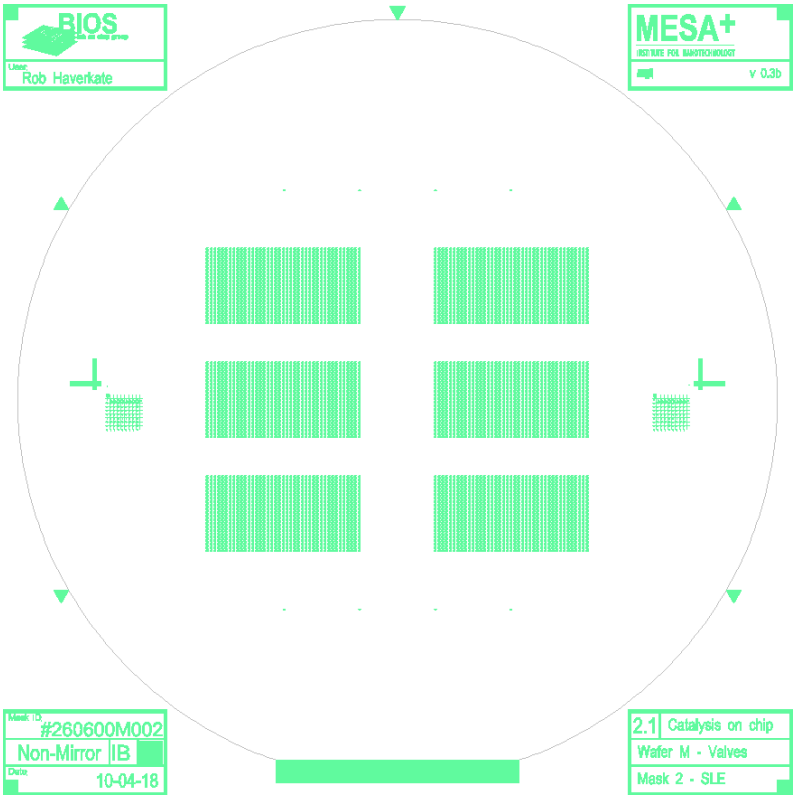


Fig. 26: Mask 2, used for patterning the valve gap SLE TEOS.

Fig. 27: Mask 3, user to pattern the poly-silicon membranes.

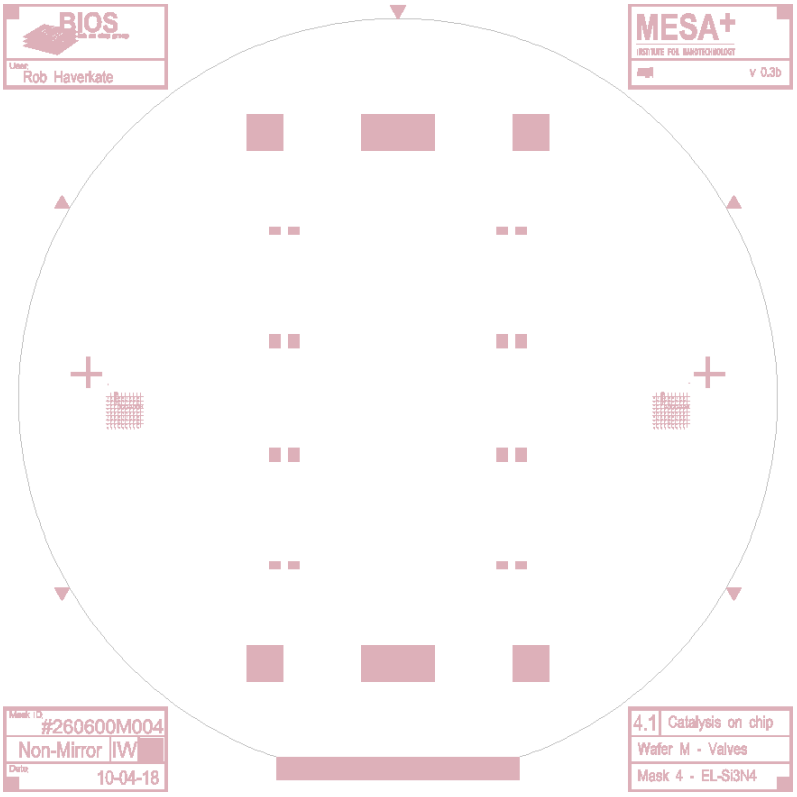


Fig. 28: Mask 4, used to pattern the Si_3N_4 layer for electric contacts.

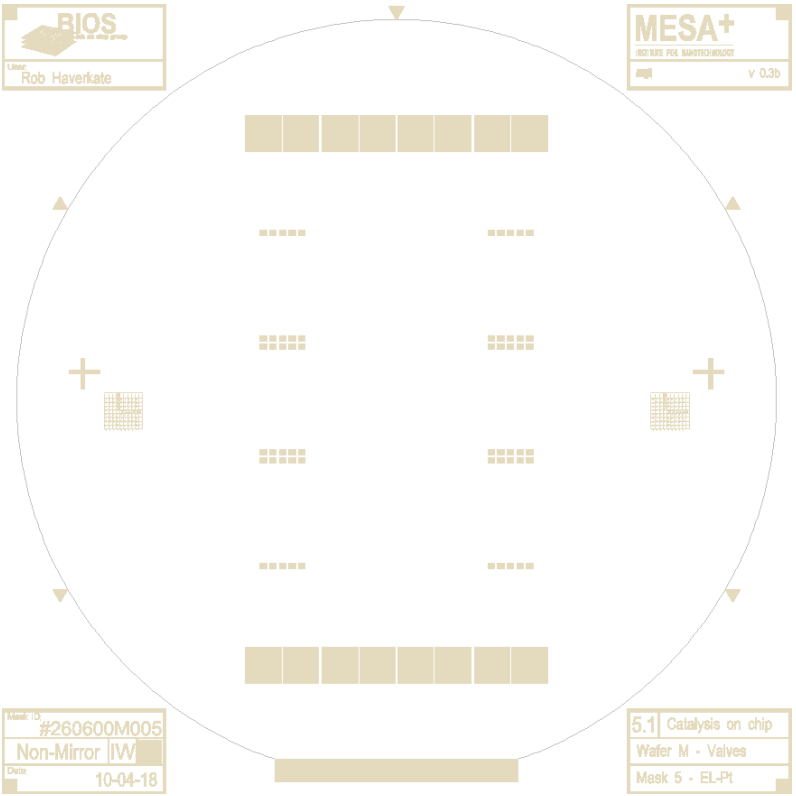


Fig. 29: Mask 5, used for sputtering the electric contact pads utilizing liftoff.

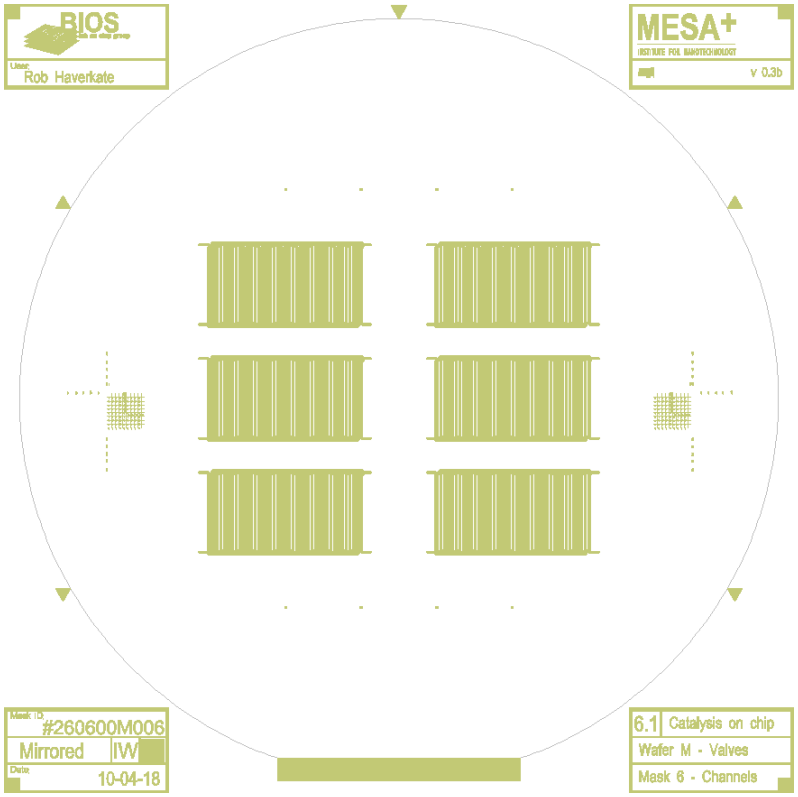


Fig. 30: Mask 6, used to pattern the MF channels in the silicon substrate at the wafer backside.

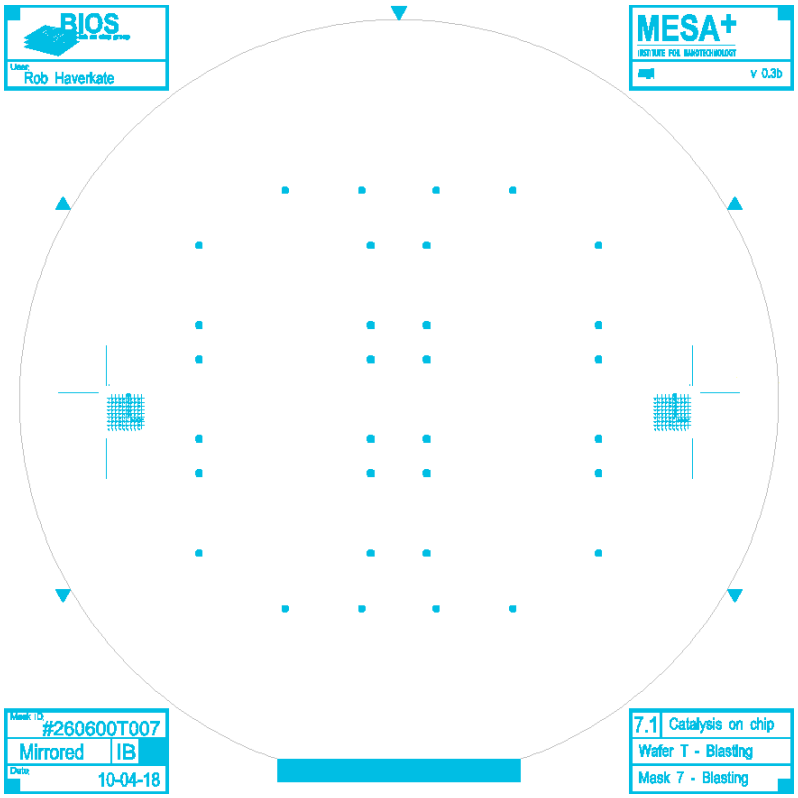


Fig. 31: Mask 7, used for powderblasting the MEMpax wafer.

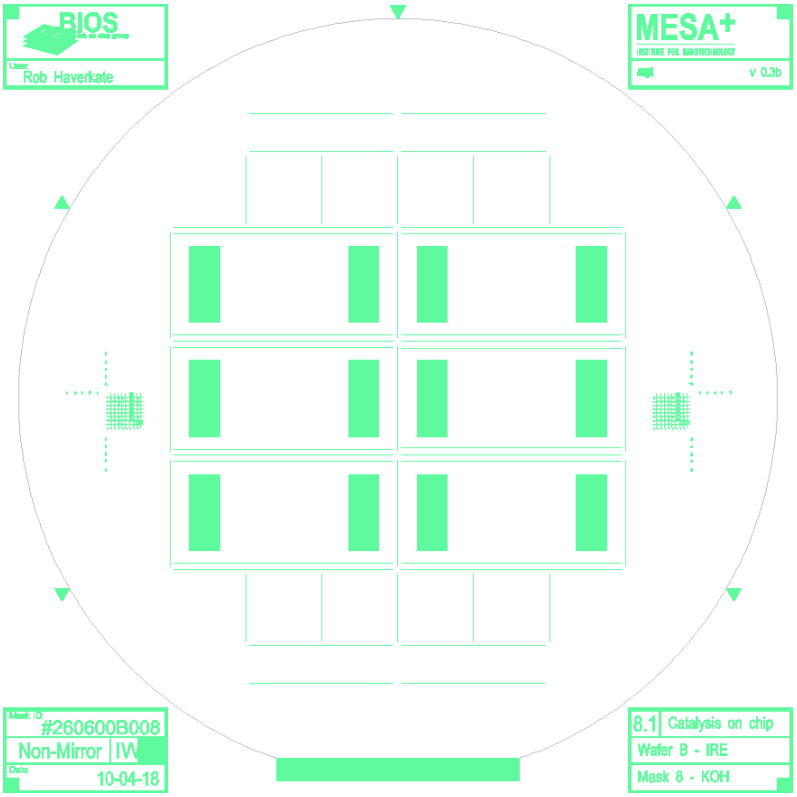


Fig. 32: Mask 8, used for patterning the KOH facets including dicing marks.

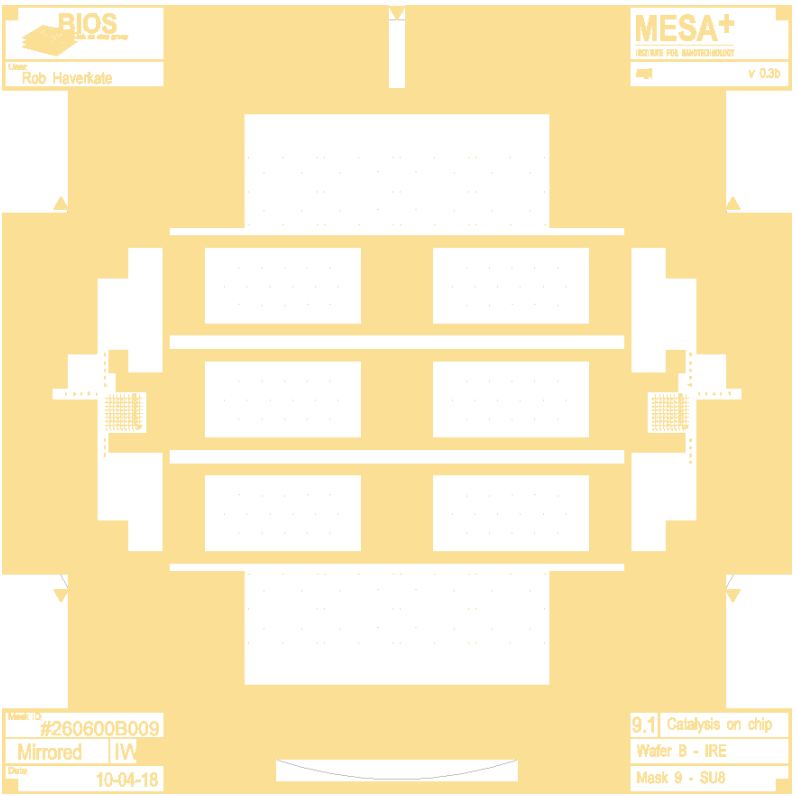


Fig. 33: Mask 9, used for SU-8 resist to pattern the spacers.

S6 Process flow - IRE

Name of process flow:	Catalysis on chip – IRE
Platform:	Fluidics
Creation date:	27-03-2018
Personal information	
User name:	Rob Haverkate
Email address:	r.haverkate@student.utwente.nl
Company/Chair:	BIOS
Function:	Student
Project:	Catalysis on chip
Name of supervisor:	M. Odijk
Status	
Name of advisor:	M.J. de Boer
Last revision:	17-04-2018

ILP: In-line Processing	**MFP: Metal-free Processing**	**UCP: Ultra Clean Processing**	**Removal of Residues**

Step	Level	Process/Basic flow		User comments
1		**Substrate Silicon** (#subs102)	NL-CLR-Wafer Storage Cupboard Orientation: <100> Diameter: 100mm Thickness: 500µm +/- 25µm Polished: Double side (DSP) Resistivity: 5-10Ωcm Type: p/boron	
		film1205: LPCVD of low-stress SiRN (G3-50 MPa)		
				Backside processing
2	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	
3	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
4	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	

5	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min
6	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
7	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!
8	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).
9	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
10	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm)

			• Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
11	MFP	**LPCVD of SiRN (50 MPa)** (#film205)	NL-CLR-LPCVD G3 Program: **N2 SiRN04** **Settings:** • SiH_2Cl_2 flow: 77.5 sccm • NH_3 flow: 20 sccm • N_2 low: 250sccm • Temperature: 820-850-870°C • Pressure: 150mTorr Load your wafers within 4 hours after cleaning!	300 nm = 1h10m (mask for KOH)
12	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scatches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
13	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)				
14	ILP	**Priming HMDS** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 Hotplate** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Settings: • Temperature: 150°C • Pressure: 25 inHg	**IRE Backside processing**

			• Dehydratation bake: 2 min • HMDS priming: 5 min CAUTION: let the substrates cool down before handling with your tweezer!
15	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec)
16	ILP	**Prebake of Olin OiR 907-17** (#litho003)	NL-CLR-WB21 Prebake: Hotplate • Temperature: 95°C • Time: 90s
17	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec
18	ILP	**After exposure bake of Olin OiR resists** (#litho005)	NL-CLR-WB21 After exposure bake: Hotplate • Temperature: 120°C • Time: 60s
19	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21** Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec
20	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
21	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
22	ILP	**Postbake of Olin OiR resists** (#litho008)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min
23	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.
		etch1731: Etching of thin nitrides, oxides and shallow Si by CHF3/O2 Plasma (TEtske)	
24	ILP	**Chamber clean (TEtske)** (#etch198)	**NL-CLR-TEtske** Application: removal of organic and fluorocarbon residues on the chamber wall. Select the correct etch chamber and electrode for your etch process (see next step). • Electrode temperature: 10°C

			• Pressure: 50mTorr • O2 flow: 50sccm • Power: 100Watt • Time: 10 min • DC bias: -600Volt • Load: 65 • Tune: 35 The etch chamber is clean at the moment the plasma color is white.
25	ILP	**RIE with CHF3/O2 Plasma** (#etch193)	**NL-CLR-TEtske** Application: plasma etching of thin layers of various oxides and nitrides, shallow etching (nm) in Silicon and pre-conditioning for XeF2 etching. Use Kapton tape or Kapton foil to protect the edge of the wafer and therefore avoid damage during processing in KOH or TMAH. Select the dirty chamber and the styros electrode. • Electrode temperature: 10°C • Pressure: 10mTorr • CHF3 flow: 25sccm • O2 flow: 5sccm • Power: 60Watt • DC bias: -500 up to - 540Volt Etch rate SiRN (G3-SiRN)**:** 60 nm/min Etch rate SiO2: 30 nm/min Etch rate Si: 15-25 nm/min Etch rate Olin OiR resists: 50 nm/min
26	ILP	**Stripping of Resists** (#strip100)	**NL-CLR-TePla300** Application: stripping of resists by O2 plasma after plasma etching. **PLEASE NOTE** **1. RESTRICTION**: do not strip resists on chromium in the TePla300, but instead use the TePla360 (choose: recipe 041). **2. BACKUP**: TePla300 down? Contact the administrator if you can continue your processing in the TePla360.

Step	O2 (sccm)	N2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	500	1.0	800	0:10:00
Stripping of resist	500	0	1.0	800	*

			* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers. Use the abort option in the last step if you sample requires a shorter stripping time. **Recipe 01**: time = 10 min **Recipe 02**: time = 30 min **Recipe 04**: time = 60 min
27	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP)

			• processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	
28	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
29	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		etch1001: KOH etch - standard (WB17) with RCA-2 post cleaning (WB09)		
30	ILP	**Etching in 1% HF** (#etch192)	NL-CLR-WB16 Beaker: 1% HF • Temperature: 20 °C. • Time: depends on application	
31	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
32	ILP	**Silicon etching in KOH** (#etch138)	**NL-CLR-WB17 Beaker KOH-1 or KOH-2** Chemical: 25wt.% KOH Application: anisotropic etching of crystalline silicon. Settings: • Temperature: 75°C • Use stirrer	7h30m (450m) = 450um deep

			Etch rates: Si <100> = 1µm/min Si <111> = 12.5nm/min SiO2 (thermal) = 180nm/hr SiRN < 0.6nm/hr
33	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
34	ILP	**Substrate transport in demi-water** (#trans003)	**NL-CLR-WB17→WB09** Purpose: transport of wafers for cleaning in RCA-2 after etching in KOH (WB17). Wet transport of substrates in a beaker with demi-water. After transport, return the quartz wafer carrier back to WB17.
35	Rem Res	**Removal of residues in RCA-2** (#residue501)	**NL-CLR-WB09** Purpose: removal of residues after wet-chemical processing (e.g. KOH and metal stripping) in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) . Chemicals: $HCl:H_2O_2:H_2O$ (1:1:5 vol%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.
36	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

37	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		etch1205: Etching in 50% HF (WB02/09/10-private use)		
38	ILP	**Etching in HF 50%** (#etch130)	NL-CLR-WB9/10 Use private beaker HF 50% standard Temp.: room temperature • Si3N4-H2 = 0.64 nm/min • SiRN-G3[#] (nanolab) = 3.1 - 3.5 nm/min • SiO_2 = 1 µm/min	Stripping nitride: 1h35m
39	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
40	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
41				**Front side processing**
		film1500: Sputtering of Titanium (Sputterke)		
42	ILP	**Sputtering of Ti** (#film627)	**NL-CLR-Sputterke** • Target: Ti (gun #: see MIS logbook) • Use Ar flow to adjust sputter pressure • Base pressure: < 1.0 e-6mbar • Sputter pressure: 6.6 e-3mbar • Power: 200W • Deposition rate = 13 nm/min	
		film1507: Sputtering of Palladium (Sputterke)		
43	ILP	**Sputtering of Pd** (#film629)	**NL-CLR-Sputterke** • Target: Pd (gun #: see MIS logbook) • Use Argon flow to adjust sputter pressure • Base pressure: 1.0 -6 mbar • Sputter pressure: 6.6 e-3 mbar • Power: 200 W • Deposition rate = 35 nm/min.	
		film1500: Sputtering of Titanium (Sputterke)		
44	ILP	**Sputtering of Ti** (#film627)	**NL-CLR-Sputterke** • Target: Ti (gun #: see MIS logbook) • Use Ar flow to adjust sputter pressure • Base pressure: < 1.0 e-6mbar • Sputter pressure: 6.6 e-3mbar	

			• Power: 200W • Deposition rate = 13 nm/min	
		litho1833: Lithography SU-8 2005 (negative resist - ILP)		
45	ILP	**Dehydration bake for SU-8** (#lith050)	NL-CLR-WB24 Dehydration bake on hotplate • Temperature: 120°C • Time: 10min	
46	ILP	**Coating SU-8 2005** (#lith176)	NL-CLR-WB24 SüssMicroTec Spinner Delta 20 • Microchem NANO SU-8 2005 TST Bottle Experimental Results: Spin program | rpm | Thickness (µm) 1 | 1000 | 13.6 2 | 1500 | 8.4 3 | 2000 | 7.4 4 | 2500 | 6.0 5 | 3000 | 5.2 6 | 3500 | 4.6 7 | 4000 | 4.1	Program 5, SU-8 type 5, rmp1 = 500, time = 10s, rpm2 = 3000, time = 30s, thickness = 5um
47	ILP	**Softbake SU-8 2005** (#lith177)	**NL-CLR-WB24 Hotplate** Settings: • 1 min @ 65 °C • ramp up to 95°C • 2 min @ 95 °C • cooldown on hotplate to 25°C	
48	ILP	**Alignment & Exposure SU-8 2005** (#lith178)	NL-CLR-EVG 620 Electronic Vision Group 620 Mask Aligner • Exposure time 10sec • Hardcontact	
49	ILP	**Post Exposure Bake SU-8 2005** (#lith179)	NL-CLR-WB24 • Hotplate • apply immedialy after exposure! • Start @ 65 °C • Ramp to 95 °C • Cooldown to 25°C and leave the wafer on the hotplate • Total process time ca. 90 min	
50	ILP	**Development SU-8 2005** (#lith175)	NL-CLR-WB24 TCO Spray Developer Developer: PGMEA (RER600, ARCH Chemicals) • Spray develop 5 cycles x 30sec • Rinse with RER600 • Rinse with IPA • Spin dry • Check result and perform extra cycles if not complete	

			• Check Micro-Chem site for more process information • http://www.microchem.com/products/su_eight.htm	
51	ILP	**Hard bake SU-8** (#lith168)	NL-CLR-WB24 • Hotplate • 2hr @ 120 °C	Skip
52		**Adhesive bonding with wafer 1+2**		Anodic bonder EVG510, 2h, 120 °C, 6000N

S7 Process flow - Valve and channels

Name of process flow:	Catalysis on chip – Valves and channels
Platform:	Fluidics
Creation date:	27-03-2018
Personal information	
User name:	Rob Haverkate
Email address:	r.haverkate@student.utwente.nl
Company/Chair:	BIOS
Function:	Student
Project:	Catalysis on chip
Name of supervisor:	M. Odijk
Status	
Name of advisor:	M.J. de Boer
Last revision:	17-04-2018

ILP: In-line Processing	MFP: Metal-free Processing	UCP: Ultra Clean Processing	Removal of Residues

Step	Level	Process/Basic flow		User comments
1				**Part-1: Fabrication of valve orifice**
2		**Substrate Silicon** (subs104)	**NL-CLR-Wafer storage Cleanroom** Orientation: <100> Diameter: 100 mm Thickness: 525µm +/- 15µm Polished: double side (DSP) Resistivity: 0.01-0.025Ωcm Type: p++/ boron	25 DSP + 10 OSP (dummy batch)
		film1941: Wet Oxidation of Silicon (A3)		
3	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	
4	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
5	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR)	

			Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
6	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min	
7	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
8	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
9	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	Skip
10	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
11	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Skip

			Batch drying of substrates: The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
12	MFP	**Wet Oxidation of Silicon** (#film930)	**NL-CLR-A3 Furnace** Recipe: WETxxx (xxx= temperature setting) Settings: • Standby temperature: 700°C • Temperature range: 700-1150°C • Ramp: 10°C/min • O_2 flow: 4l/min Please mention the following settings in the User Comments: • Target thickness: .**2000nm** • Temperature: **1150 °C** • Time:**1380m**	Target thickness: 2000 nm,
13	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)				
14	ILP	**Priming HMDS** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 Hotplate** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Settings: • Temperature: 150°C • Pressure: 25 inHg • Dehydratation bake: 2 min • HMDS priming: 5 min	Note: pre-cleaning in WB6 for better resist result (less particles): HNO3 5+2m, QDR, drying

			CAUTION: let the substrates cool down before handling with your tweezer!	
15	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec)	
16	ILP	**Prebake of Olin OiR 907-17** (#litho003)	NL-CLR-WB21 Prebake: Hotplate • Temperature: 95°C • Time: 90s	
17	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec • **Hard contact**	**Mask 1 – Holes** Note: clean mask every 5th wafer (mask becomes dirty)
18	ILP	**After exposure bake of Olin OiR resists** (#litho005)	NL-CLR-WB21 After exposure bake: Hotplate • Temperature: 120°C • Time: 60s	
19	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21** Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
20	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
21	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
22	ILP	**Postbake of Olin OiR resists** (#litho008)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
23	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
etch1774: Directional RIE of SiO2 and Si3N4 by CHF3/O2 Plasma (PT790)				
24	UCP	**Etching of SiO2 and Si3N4** (#etch221)	**NL-CLR-PT790** Application: etching of thin layers of oxides and nitrides. Settings: CHF_3 flow: 100sccm O_2 flow: 5sccm Pressure: 40 mTorr Power 250W	Note: check if DC bias = 310V Note: for 2.67um perform 2x42m, rotate 180 °C

Etch rate SiO2: 32 nm/min
Etch rate Si3N4: 30nm/min

Adixen settings (alternative)	C4F8=20sccm (etching), He=150sccm (support), CH4=15sccm (passivation), P=8.5*10-3mbar, power: 2800ICP, 350CCP, substrate holder = 120mm

Note: two wafers on the back need approximatel y 2m extra.

Note: Adixen alternative: 6m for 2.67um, 5m for 2.4um

25 UCP **Chamber clean (PT790)** (#etch199)

NL-CLR-PT790
Application: removal of organic and fluorocarbon residues from the chamber wall.

- Graphite electrode
- O_2 flow: 100sccm
- Pressure: 100mTorr
- Power: 400Watt

Note: always clean the chamber after etching!

26 ILP **Stripping of Resists** (#strip101)

NL-CLR-TePla360
Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!

Skip

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
- continue with UCP processing
- continue with high-temperature processing (MFP)

27 Rem Res **Removal of metal traces in RCA-2** (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

skip

- cleaning in the Pre-Furnace Clean (WB14-MFP)
- processing in the Ultra-Clean Line - Front End (WB12-UCP)
- processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

28	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
29	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Skip

etch1652: DRIE of silicon: Bosch HARS (SPTS Pegasus)

30a	ILP	**Resist stripping using Tepla**		Note: gives better etch result
30b	ILP	**DRIE of silicon HARS** (#etch218)	NL-CLR-SPTS Pegasus Bosch HARS standaard recipe for micro structures 3 upto 100 µm Scallop size: 350 nm Use oxide as mask (no/less retraction) Platen temp: 20°C - He pres: 20 Torr	V1-HARS, 480cycles, 18m, 80um deep Alternative: Estrelas, Fine Scallop HW, 1000 cycles, 100um deep Note: Estrelas has a good FC strip program, 5m

Parameters	Etch	Deposition
Gas	SF6	C4F8
Flow [sccm]	275	150
Boost Flow [sccm - sec]	-	-
Priority	2	1
Time [sec]	1,75	0.50
Pressure [mTorr]	26	20
ICP [Watt]	2200	2000
CCP [Watt]	20 --> 30	0
Boost CCP [Watt - sec]	nvt	-
LF pulse [% duty C.]	20	

			Etch rate Si: 10 µm/min, Olin907: 80 nm/min **Time: 12m**	
31	ILP	**Chamber - Chuck Clean** (#etch219)	**NL-CLR-SPTS Pegasus** Application: removal of organic and fluorocarbon residues from the chuck and chamber wall. Recipe: Clean after use Parameters: O2 flow: 200sccm Pressure: 5mTorr ICP: 2500W CCP: 20W (RF) Time: 15min Note: after cleaning the substrate holder temp will be set to 20°C. Perform this recipe at the moment you are done etching.	
32	ILP	**Stripping of Resists and Fluorocarbon** (#strip104)	**WARNING - PLEASE READ** This recipe is efficient for stripping of fluorocarbon in microstructures with aspect ratios < 5. Contact the administrator in case you want to strip fluorocarbon in microstructures with aspect ratios > 5 or fluorocarbon in nanostructures. This recipe attacks silicon and nitride coatings on the nanometer scale! **NL-CLR-TePla360** Application: stripping of resists and fluorocarbon after DRIE BOSCH processing by O2/CF4 plasma.	Skip: already done at step 30a (resist stripping)
33	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:	Skip

Step	**O2 (sccm)**	**Ar (sccm)**	**CF4 (sccm)**	**H2 (sccm)**	**P (mbar)**	**Power (W)**	**Time (h:mm:ss)**
Preheating	0	600	0	0	0.6	1000	0:10:00
Resist stripping	250	0	0	0	0.5	800	*
Fluorocarbon stripping	237	0	13	0	0.5	800	0:01:00
Residual Fluorocarbon stripping	250	0	0	0	0.8	800	0:01:00

* Select one of the following recipes depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 035: time = 10min
Recipe 037: time = 20min
Recipe 036: time = 60min

BACKUP: The TePla300 is not a backup for this processing! If the TePla360 is down, contact the administrator.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

			• cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	
34	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
35	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Skip
		metro1102: SEM inspection		
36	ILP	**SEM inspection** (#metro103)	**NL-CLR-SEM** • JEOL JSM 5610 SEM • FEI Sirion HR-SEM • High resolution SEM LEO (Mark Smithers)	Use dummy wafer and check profile/depth of trench and measure width of the trench/hole (top. middle, bottem), width of the hole determines layer thickness of SiRN and Poly-layer and oxidation of poly-silicon.
		etch1774: Directional RIE of SiO2 and Si3N4 by CHF3/O2 Plasma (PT790)		

37	UCP	**Etching of SiO2 and Si3N4** (#etch221)	**NL-CLR-PT790** Application: etching of thin layers of oxides and nitrides. Settings: CHF_3 flow: 100sccm O_2 flow: 5sccm Pressure: 40 mTorr Power 250W Etch rate SiO2: 32 nm/min Etch rate Si3N4: 30nm/min	Stripping oxide on front side.
38	UCP	**Chamber clean (PT790)** (#etch199)	**NL-CLR-PT790** Application: removal of organic and fluorocarbon residues from the chamber wall. • Graphite electrode • O_2 flow: 100sccm • Pressure: 100mTorr • Power: 400Watt Note: always clean the chamber after etching!	
39	ILP	**Stripping of Resists** (#strip101)	**NL-CLR-TePla360** Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!	Note: no resist to strip but FC, recipe 35 (or 37) instead
40	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP)	

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

~~**Recipe 011**: time = 10min~~
~~**Recipe 012**: time = 20min~~
~~**Recipe 013**: time = 30min~~
~~**Recipe 014**: time = 40min~~
~~**Recipe 016**: time = 60min~~

Recipe 35 or 37 to remove FC! (short (35) version is OK)

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

			• processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) **(36%)** • Heat up the solution to 70°C (setpoint heater = 80°C) **(set shortly to 95°C till 70°C is reached (to speed up), don't walk away!)** • Slowly add 300ml* of Hydrogen Peroxide (H2O2) **(31%)** • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	
41	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
42	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Note: skip, but place wafers in beaker with DI-water to transport to WB14. Move wafers to WB14 rack before going in the HNO3
		metro1101: Inspection by Optical Microscopy (Olympus)		
43	ILP	**Inspection by Optical Microscopy** (#metro102)	**NL-CLR-Optical Microscopes** Use one of the Olympus microscopes for inspection.	Measure diameter/width of structures and calculate thickness of SIRN, Poly-Si and Thermal oxidation
		film1205: LPCVD of low-stress SiRN (G3-50 MPa)		
44	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	Nitride protection layer

45	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
46	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
47	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min	
48	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
49	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	Skip
50	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	
51	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers	

			Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
52	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
53	MFP	**LPCVD of SiRN (50 MPa)** (#film205)	NL-CLR-LPCVD G3 Program: **N2 SiRN04** **Settings:** • SiH_2Cl_2 flow: 77.5 sccm • NH_3 flow: 20 sccm • N_2 low: 250sccm • Temperature: 820-850-870°C • Pressure: 150mTorr • **Time: 109min (4.6nm/min)** Load your wafers within 4 hours after cleaning!	500 nm, SiRN is used as stop layer for etching TEOS!
54	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scatches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
55	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		film1203: LPCVD of poly-Silicon (F2-590 °C)		
56	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	SLE poly, Note: these steps can be skipped if the wafers are directly transported from G3 to F2 (within 4h)
57	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces.	Skip

			• Beaker 2: 99% HNO_3 • Time = 5 min	
58	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
59	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min	Skip
60	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
61	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	Skip
62	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	Skip
63	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip

64	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	Skip
65	MFP	**LPCVD of poly-Silicon (590 °C)** (#film203)	**NL-CLR-F2 Furnace** Program: Senspoly Settings: • SiH_4 flow: 50 sccm • N_2 low: 250sccm • Temperature: 590°C • Pressure: 250mTorr • **Time: 480min** Maximum thickness: 2.5 um. Load your wafers within 4 hours after cleaning!	Dep time = 3.96nm/m. 1.8um = 7h30m
66	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scatches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
67	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		etch1733: Directional RIE of poly-Si using SF6/CHF3/O2 plasma (TEtske)		
68	ILP	**Chamber clean (TEtske)** (#etch198)	**NL-CLR-TEtske** Application: removal of organic and fluorocarbon residues on the chamber wall. Select the correct etch chamber and electrode for your etch process (see next step). • Electrode temperature: 10°C • Pressure: 50mTorr • O2 flow: 50sccm • Power: 100Watt • Time: 10 min • DC bias: -600Volt	Note: TEtske is not uniform enough, use SPTS: HARS-V1, 30s

• Load: 65
• Tune: 35

The etch chamber is clean at the moment the plasma color is white.

69 ILP

RIE of Poly-Silicon or Silicon
(#etch107)

NL-CLR-TEtske
Application: directional etching of polySi or Silicon.
Use clean chamber/Styros electrode

• Electrode temperature: 10°C
• Pressure: 100mTorr
• SF6 flow: 30sccm
• CHF3 flow: 7sccm
• O2 flow: 11sccm
• Power: 60W

Etch rate of Poly-Si: 360nm/min at 95% load (100 mm wafer scale)

Back etching pol-Si frontside and stripping backside

Note: critical stop at SiRN

70 ILP

Stripping of Resists
(#strip100)

NL-CLR-TePla300
Application: stripping of resists by O2 plasma after plasma etching.

PLEASE NOTE

1. RESTRICTION: do not strip resists on chromium in the TePla300, but instead use the TePla360 (choose: recipe 041).
2. BACKUP: TePla300 down? Contact the administrator if you can continue your processing in the TePla360.

Step	O2 (sccm)	N2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	500	1.0	800	0:10:00
Stripping of resist	500	0	1.0	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers. Use the abort option in the last step if you sample requires a shorter stripping time.

Recipe 01: time = 10 min
Recipe 02: time = 30 min
Recipe 04: time = 60 min

Skip

71 Rem Res

Removal of metal traces in RCA-2
(#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Skip

			Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	
72	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
73	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Skip
		etch1731: Etching of thin nitrides, oxides and shallow Si by CHF3/O2 Plasma (TEtske)		
74	ILP	**Chamber clean (TEtske)** (#etch198)	**NL-CLR-TEtske** Application: removal of organic and fluorocarbon residues on the chamber wall. Select the correct etch chamber and electrode for your etch process (see next step). • Electrode temperature: 10°C • Pressure: 50mTorr • O2 flow: 50sccm • Power: 100Watt • Time: 10 min • DC bias: -600Volt • Load: 65 • Tune: 35 The etch chamber is clean at the moment the plasma color is white.	Note: TEtske is not uniform enough, use PT790 instead.
75	ILP	**RIE with CHF3/O2 Plasma** (#etch193)	**NL-CLR-TEtske** Application: plasma etching of thin layers of various oxides and nitrides, shallow etching (nm) in Silicon and pre-conditioning for XeF2 etching. Use Kapton tape or Kapton foil to protect the edge of the wafer and therefore avoid damage during processing in KOH or TMAH. Select the dirty chamber and the styros electrode. • Electrode temperature: 10°C • Pressure: 10mTorr • CHF3 flow: 25sccm • O2 flow: 5sccm • Power: 60Watt • DC bias: -500 up to - 540Volt Etch rate SiRN (G3-SiRN)**:** 60 nm/min	Etching 500 nm SiRN @ the backside.

Etch rate SiO2: 30 nm/min
Etch rate Si: 15-25 nm/min
Etch rate Olin OiR resists: 50 nm/min

76 ILP **Stripping of Resists** (#strip100)

NL-CLR-TePla300
Application: stripping of resists by O2 plasma after plasma etching.

FC strip, use recipe 35 or 37

PLEASE NOTE

1. RESTRICTION: do not strip resists on chromium in the TePla300, but instead use the TePla360 (choose: recipe 041).
2. BACKUP: TePla300 down? Contact the administrator if you can continue your processing in the TePla360.

Step	O2 (sccm)	N2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	500	1.0	800	0:10:00
Stripping of resist	500	0	1.0	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers. Use the abort option in the last step if you sample requires a shorter stripping time.

Recipe 01: time = 10 min
Recipe 02: time = 30 min
Recipe 04: time = 60 min

77 Rem Res **Removal of metal traces in RCA-2** (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

78 ILP **Quick Dump Rinse (QDR)** (#rinse001)

NL-CLR-Wetbenches
Purpose: removal of traces of chemical agents.

Recipe 1 Quick dump rinsing (QDR)

			Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
79	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
		film1942: Wet Oxidation of polySi (A3)	
80	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min
81	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min
82	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
83	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min
84	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
85	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm)

			Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
86	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	
87	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
88	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
89	MFP	**Wet Oxidation of polySi** (#film931)	**NL-CLR-A3 Furnace (Or B2)** Recipe: WETxxx (xxx= temperature setting) Settings: • Standby temperature: 700°C • Temperature range: 700-1150°C • Ramp: 10°C/min • O_2 flow: 4l/min Please mention the following settings in the User Comments: • Target thickness: **3900 nm** • Temperature: **1150 °C** • Time: ~~**1500 min,**~~ **2880min**	Target thickness: 3.9um, 1150 °C, time: 48h
90	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		etch1774: Directional RIE of SiO2 and Si3N4 by CHF3/O2 Plasma (PT790)		
91	UCP	**Etching of SiO2 and Si3N4** (#etch221)	**NL-CLR-PT790** Application: etching of thin layers of oxides and nitrides.	Skip whole part! (layer is

			Settings: CHF_3 flow: 100sccm O_2 flow: 5sccm Pressure: 40 mTorr Power 250W Etch rate SiO2: 32 nm/min Etch rate Si3N4: 30nm/min **(bad selectivity)** **3600um oxide?= 113min etching**	etched before A3)
92	UCP	**Chamber clean (PT790)** (#etch199)	**NL-CLR-PT790** Application: removal of organic and fluorocarbon residues from the chamber wall. • Graphite electrode • O_2 flow: 100sccm • Pressure: 100mTorr • Power: 400Watt Note: always clean the chamber after etching!	Skip
93	ILP	**Stripping of Resists** (#strip101)	**NL-CLR-TePla360** Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!	Skip

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

94	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP)	Skip

			Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	
95	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
96	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Skip
		film1208: LPCVD of SiO2 (H3)		
97	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	Filling trenches (first do surface inspection (use dummy)) Note: clean can be skipped if transported directly from A3 to H3
98	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	Skip
99	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip

100	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min	Skip
101	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
102	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	Skip
103	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	Skip
104	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
105	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm)	Skip

			• Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
106	MFP	**LPCVD of SiO2 (TEOS)** (#film208)	NL-CLR-H3 Furnace Program: N2 Settings: • TEOS flow: 40sccm • N_2 flow: 30sccm • Temperature: 710°C (zone 1), 725°C (zone 2), 740°C (zone 3) • Pressure: 400mTorr Load your wafers within 4 hours after cleaning!	2 step process, first 1200nm (with Bronkhorst or Lionix) and then remaining 600nm).
107	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scatches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
108	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
109				**Part 2: define SLE of SiO2 and Poly-silicon capping**
		litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)		
110	ILP	**Priming HMDS** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 Hotplate** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven**	

			Settings: • Temperature: 150°C • Pressure: 25 inHg • Dehydratation bake: 2 min • HMDS priming: 5 min CAUTION: let the substrates cool down before handling with your tweezer!	
111	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec)	
112	ILP	**Prebake of Olin OiR 907-17** (#litho003)	NL-CLR-WB21 Prebake: Hotplate • Temperature: 95°C • Time: 90s	
113	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec	**Mask 2 – SLE**
114	ILP	**After exposure bake of Olin OiR resists** (#litho005)	NL-CLR-WB21 After exposure bake: Hotplate • Temperature: 120°C • Time: 60s	
115	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21** Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
116	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
117	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
118	ILP	**Postbake of Olin OiR resists** (#litho008)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
119	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
etch1774: Directional RIE of SiO2 and Si3N4 by CHF3/O2 Plasma (PT790)				
120	UCP	**Etching of SiO2 and Si3N4** (#etch221)	**NL-CLR-PT790** Application: etching of thin layers of oxides and nitrides. Settings: CHF_3 flow: 100sccm O_2 flow: 5sccm	Check uniformity of wafer etch process (dummy). Be careful that SiRN wil also

			Pressure: 40 mTorr Power 250W Etch rate SiO2: 32 nm/min Etch rate Si3N4: 30nm/min **1.5um oxide?= 47 min**	be etched. Strip also TEOS layer at the backside. use the etch time of the frontside. thermal oxide layer should be not etched.
121	UCP	**Chamber clean (PT790)** (#etch199)	**NL-CLR-PT790** Application: removal of organic and fluorocarbon residues from the chamber wall. • Graphite electrode • O_2 flow: 100sccm • Pressure: 100mTorr • Power: 400Watt Note: always clean the chamber after etching!	
122	ILP	**Stripping of Resists** (#strip101)	**NL-CLR-TePla360** Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!	
123	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE**	

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

			1. CAUTION: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.
124	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
125	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
		therm1154: Annealing at 1150°C (H1)	
126	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min
127	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min
128	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
129	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min
130	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR)

			Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
131	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
132	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	
133	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
134	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
135		**Annealing at 1150°C** (#therm001)	NL-CLR- Furnace H1 • Standby temp.: 700°C • Program: ANN1150C • Temp.: 1150°C	Annealing of TEOS is needed to avoid cracking, Temp.

			• N_2 flow: 5slm • Ramp:10°C/min
		film1203: LPCVD of poly-Silicon (F2-590 °C)	
136	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min
137	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min
138	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
139	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min
140	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
141	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!
142	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF

			Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	
143	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
144	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
145	MFP	**LPCVD of poly-Silicon (590 °C)** (#film203)	**NL-CLR-F2 Furnace** Program: Senspoly Settings: • SiH_4 flow: 50 sccm • N_2 low: 250sccm • Temperature: 590°C • Pressure: 250mTorr Maximum thickness: 2.5 um. Load your wafers within 4 hours after cleaning!	Thickness 1000nm = 4h12m (dep rate 4.96nm/m)
146	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scatches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
147	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		dopi1302: Solid source dotation (SSD) of boron 1050°C		
148	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces.	Please INCLUDE THE FILLER

			• Beaker 1: 99% HNO_3 • Time = 5 min	WAFERS from the wafer box of the B1 furnace in the wafer cleaning! The maximum number of wafers is 12 wafers, including the filler wafers.
149	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
150	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
151	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min	
152	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
153	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).	
154	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
155	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner	Please put the cleaned filler wafers back in the wafer

			Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	box of the B1 furnace!
156	MFP	**Solid Source Diffusion (SSD) of Boron at 1050°C** (#dopi104)	NL-CLR-SSD furnace Tempress B1 Standby temperature: 700°C Program: SSD-1050 B2O5 deposition • temp 900°C • gas O_2 , 2 SLM • gas N_2 , 2 SLM • time 15 min Anneal (soak) • temp.: 1050°C • ramp up: 5°C/min • cooldown: 7.5 °C/min • Gas N_2: 4 SLM • Time: variable	Time: 120 min. Please REPLACE ALL FILLER WAFERS in the wafer boat with the previously cleaned filler wafers and PROCESS THE FILLER WAFERS with your process wafers till the end of this basic flow.
157	MFP	**Etching in BHF (1:7)** (#etch119)	NL-CLR-WB02 Private use BHF, please use the dedicated beaker of WB02! Temperature: room temperature Etch rate: 60-80nm/min (for thermal SiO_2).	Strip the wafers for 10 min
158	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
159	MFP	**Substrate drying (WB06-WB08)** (#dry020)	**NL-CLR-WB06 to WB08** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
160	MFP	**Dry Oxidation of SiB** (#film961)	**NL-CLR-B3 Furnace** Purpose: removal of SiB from the surface by oxidation into B2O5 (and wet-chemical etching in BHF).	

			Settings: • Standby temperature: 800°C • Program: Ox800 • Temperature: 800°C • O_2 flow: ....slm • Time: 15 min	
161	MFP	**Etching in BHF (1:7)** (#etch119)	NL-CLR-WB02 Private use BHF, please use the dedicated beaker of WB02! Temperature: room temperature Etch rate: 60-80nm/min (for thermal SiO_2).	Strip the wafers for 10 min
162	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
163	MFP	**Substrate drying (WB06-WB08)** (#dry020)	**NL-CLR-WB06 to WB08** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	Please put the FILLER WAFERS back in the wafer box of the B1 furnace!
164	ILP	**Sheet Resistance measurement** (#metro109)	NL-CLR- Resistance Measurement Equipment	
		film1408: Deposition of PECVD SiO2 (Oxford133)		
165	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	Necessary for the drive in? (to be discussed)
166	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
167	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	

168	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces. • Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min
169	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
170	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!
171	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).
172	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
173	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm)

			• Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
174	MFP	**Deposition of PECVD SiO2** (#film512)	**NL-CLR-OXFORD133** Program: Settings: Temperature: 300°C Pressure: 900mTorr Power LF: 90Watt 2%SiH4/N2: 200sccm N2O: 780sccm Please mention the following settings in the User Comments: • Target thickness: ..... nm • Time: .....min Load your wafers within 4 hours after cleaning!	1 um capping
175	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-Woollam M-2000UI ellipsometer** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
176	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scatches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
		therm1155: Annealing of polySi (B3)		
177	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14** Purpose: removal of organic traces. • Beaker 1: 99% HNO_3 • Time = 5 min	Drive in of boron doping and create slightly tensile stress in valves.
178	MFP	**Cleaning in 99% HNO_3** (#clean002)	NL-CLR-WB14 Purpose: removal of organic traces. • Beaker 2: 99% HNO_3 • Time = 5 min	
179	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
180	MFP	**Cleaning in 69% HNO_3 (95 °C)** (#clean003)	NL-CR-WB14 Purpose: removal of metallic traces.	

			• Beaker 3A or 3B: 69% HNO_3 • Temperature= 95 °C • Time = 10 min
181	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
182	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** Optional drying step. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm) Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!
183	MFP	**Etching in 1% HF** (#etch127)	NL-CLR-WB15 Purpose: remove native SiO2 from silicon. Beaker: 1% HF Temperature: room temperature Time = 1 min This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).
184	MFP	**Quick Dump Rinse (QDR)** (#rinse002)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
185	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) **Batch drying of substrates:** The Semitool uses the following standard procedure: • Rinse: 30 sec (600 rpm) • Q-rinse: 10.0 MΩ (600 rpm) • Purge: 10 sec (600 rpm) • Drying: 280 sec (1600 rpm)

			Note: it is obligatory to apply a single rinsing step in the QDR before using the Semitool!	
186a	MFP	**Annealing of polySi** (#therm155)	**NL-CLR-B3 Furnace** Recipe: ANNxxxC (xxx= temperature setting) Settings: • Standby temperature: 800°C • Temperature range: 800-1100°C • Ramp: 10°C/min • N_2 flow: 2slm Please mention the following settings in the User Comments: • Temperature: .....°C • Time: .....min	Temperature and time has te be defined to create a low tensile stress in the poly-si layer. Meint: 1050 degrees for 60 min (see thesis Rob Legtenberg)
186b		**Stripping capping layer**		
		litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)		
187	ILP	**Priming HMDS** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 Hotplate** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Settings: • Temperature: 150°C • Pressure: 25 inHg • Dehydratation bake: 2 min • HMDS priming: 5 min CAUTION: let the substrates cool down before handling with your tweezer!	
188	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec)	
189	ILP	**Prebake of Olin OiR 907-17** (#litho003)	NL-CLR-WB21 Prebake: Hotplate • Temperature: 95°C • Time: 90s	
190	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner	**Mask 3 - Poly**

			• Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec	
191	ILP	**After exposure bake of Olin OiR resists** (#litho005)	NL-CLR-WB21 After exposure bake: Hotplate • Temperature: 120°C • Time: 60s	
192	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21** Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
193	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
194	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
195	ILP	**Postbake of Olin OiR resists** (#litho008)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
196	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
etch1733: Directional RIE of poly-Si using SF6/CHF3/O2 plasma (TEtske)				
197	ILP	**Chamber clean (TEtske)** (#etch198)	**NL-CLR-TEtske** Application: removal of organic and fluorocarbon residues on the chamber wall. Select the correct etch chamber and electrode for your etch process (see next step). • Electrode temperature: 10°C • Pressure: 50mTorr • O2 flow: 50sccm • Power: 100Watt • Time: 10 min • DC bias: -600Volt • Load: 65 • Tune: 35 The etch chamber is clean at the moment the plasma color is white.	
198	ILP	**RIE of Poly-Silicon or Silicon** (#etch107)	**NL-CLR-TEtske** Application: directional etching of polySi or Silicon. Use clean chamber/Styros electrode • Electrode temperature: 10°C • Pressure: 100mTorr • SF6 flow: 30sccm • CHF3 flow: 7sccm	Check etch process by using window of chamber at the top! Be carefull SiRN will be also etched. strip also poly-

			• O2 flow: 11sccm • Power: 60W Etch rate of Poly-Si: 360nm/min at 95% load (100 mm wafer scale)	silicon on the backside
199	ILP	**Stripping of Resists** (#strip100)	**NL-CLR-TePla300** Application: stripping of resists by O2 plasma after plasma etching. **PLEASE NOTE** **1. RESTRICTION**: do not strip resists on chromium in the TePla300, but instead use the TePla360 (choose: recipe 041). **2. BACKUP**: TePla300 down? Contact the administrator if you can continue your processing in the TePla360. **Step** | **O2 (sccm)** | **N2 (sccm)** | **P (mbar)** | **Power (W)** | **Time (h:mm:ss)** Preheating | 0 | 500 | 1.0 | 800 | 0:10:00 Stripping of resist | 500 | 0 | 1.0 | 800 | * * Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers. Use the abort option in the last step if you sample requires a shorter stripping time. **Recipe 01**: time = 10 min **Recipe 02**: time = 30 min **Recipe 04**: time = 60 min	
200	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	Skip
201	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents.	Skip

Recipe 1 Quick dump rinsing (QDR)
Recipe 2 Cascade rinsing for fragile wafers
Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

202	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Skip

etch1774: Directional RIE of SiO2 and Si3N4 by CHF3/O2 Plasma (PT790)

203	UCP	**Etching of SiO2 and Si3N4** (#etch221)	**NL-CLR-PT790** Application: etching of thin layers of oxides and nitrides. Settings: CHF_3 flow: 100sccm O_2 flow: 5sccm Pressure: 40 mTorr Power 250W Etch rate SiO2: 32 nm/min Etch rate Si3N4: 30nm/min	This is step: 186b
204	UCP	**Chamber clean (PT790)** (#etch199)	**NL-CLR-PT790** Application: removal of organic and fluorocarbon residues from the chamber wall. • Graphite electrode • O_2 flow: 100sccm • Pressure: 100mTorr • Power: 400Watt Note: always clean the chamber after etching!	
205	ILP	**Stripping of Resists** (#strip101)	**NL-CLR-TePla360** Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!	

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

			PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you: • continue with UCP processing • continue with high-temperature processing (MFP)
206	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.
207	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
208	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
209			**Part 3: Metallization**

litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)

210	ILP	**Priming HMDS** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 Hotplate** Purpose: dehydration bake Settings: • Temperature: 120°C

			• Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Settings: • Temperature: 150°C • Pressure: 25 inHg • Dehydratation bake: 2 min • HMDS priming: 5 min CAUTION: let the substrates cool down before handling with your tweezer!	
211	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec)	
212	ILP	**Prebake of Olin OiR 907-17** (#litho003)	NL-CLR-WB21 Prebake: Hotplate • Temperature: 95°C • Time: 90s	
213	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec	**Mask 4 – EL-Si3N4** (to make access to silicon substrate)
214	ILP	**After exposure bake of Olin OiR resists** (#litho005)	NL-CLR-WB21 After exposure bake: Hotplate • Temperature: 120°C • Time: 60s	
215	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21** Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
216	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
217	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	

218	ILP	**Postbake of Olin OiR resists** (#litho008)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
219	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	

etch1731: Etching of thin nitrides, oxides and shallow Si by CHF3/O2 Plasma (TEtske)

220	ILP	**Chamber clean (TEtske)** (#etch198)	**NL-CLR-TEtske** Application: removal of organic and fluorocarbon residues on the chamber wall. Select the correct etch chamber and electrode for your etch process (see next step). • Electrode temperature: 10°C • Pressure: 50mTorr • O2 flow: 50sccm • Power: 100Watt • Time: 10 min • DC bias: -600Volt • Load: 65 • Tune: 35 The etch chamber is clean at the moment the plasma color is white.	
221	ILP	**RIE with CHF3/O2 Plasma** (#etch193)	**NL-CLR-TEtske** Application: plasma etching of thin layers of various oxides and nitrides, shallow etching (nm) in Silicon and pre-conditioning for XeF2 etching. Use Kapton tape or Kapton foil to protect the edge of the wafer and therefore avoid damage during processing in KOH or TMAH. Select the dirty chamber and the styros electrode. • Electrode temperature: 10°C • Pressure: 10mTorr • CHF3 flow: 25sccm • O2 flow: 5sccm • Power: 60Watt • DC bias: -500 up to - 540Volt Etch rate SiRN (G3-SiRN)**:** 60 nm/min Etch rate SiO2: 30 nm/min Etch rate Si: 15-25 nm/min Etch rate Olin OiR resists: 50 nm/min	Etching 500 nm SiN to make electrical contact for metallization.
222	ILP	**Stripping of Resists** (#strip100)	**NL-CLR-TePla300** Application: stripping of resists by O2 plasma after plasma etching. **PLEASE NOTE** **1. RESTRICTION**: do not strip resists on chromium in the TePla300, but instead use the TePla360 (choose: recipe 041). **2. BACKUP**: TePla300 down? Contact the administrator if you can continue your processing in the TePla360.	

Step	O2 (sccm)	N2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	500	1.0	800	0:10:00

			Stripping of resist	500	0	1.0	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers. Use the abort option in the last step if you sample requires a shorter stripping time.

Recipe 01: time = 10 min
Recipe 02: time = 30 min
Recipe 04: time = 60 min

223 | Rem Res | **Removal of metal traces in RCA-2** (#residue504) | Skip

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

224 | ILP | **Quick Dump Rinse (QDR)** (#rinse001) | Skip

NL-CLR-Wetbenches
Purpose: removal of traces of chemical agents.

Recipe 1 Quick dump rinsing (QDR)
Recipe 2 Cascade rinsing for fragile wafers
Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

225 | ILP | **Substrate drying** (#dry001) | Skip

NL-CLR-WBs (ILP)

Single substrate drying:
1. Use the single-wafer spinner
   Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)

226 | ILP | **Priming HMDS** (#litho600)

OPTION 1 Liquid HMDS priming

NL-CLR-WB21/22 Hotplate
Purpose: dehydration bake

			Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Settings: • Temperature: 150°C • Pressure: 25 inHg • Dehydratation bake: 2 min • HMDS priming: 5 min CAUTION: let the substrates cool down before handling with your tweezer!
227	ILP	**Coating of Olin OiR 907-17** (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Olin OiR 907-17 • Spin program: 4000 (4000rpm, 30sec)
228	ILP	**Prebake of Olin OiR 907-17** (#litho003)	NL-CLR-WB21 Prebake: Hotplate • Temperature: 95°C • Time: 90s
229	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ^{2} • Exposure time: 4sec
230	ILP	**After exposure bake of Olin OiR resists** (#litho005)	NL-CLR-WB21 After exposure bake: Hotplate • Temperature: 120°C • Time: 60s
231	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21** Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec
232	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
233	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner

			Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
234	ILP	**Postbake of Olin OiR resists** (#litho008)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	Skip, not needed for lift-off
235	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
		film1501: Sputtering of Chromium (Sputterke)		
236	ILP	**Sputtering of Cr** (#film625)	**NL-CLR-Sputterke** • Target: Cr (gun #: see MIS logbook) • Use Ar flow to adjust process pressure. • Base pressure: < 1.0 e-6mbar • Sputter pressure: 6.6 e-3mbar • Power: 200W • Deposition rate = 15 nm/min	
		film1502: Sputtering of Platinum (Sputterke)		
237	ILP	**Sputtering of Pt** (#film118)	NL-CLR-nr. 37 / Sputterke Pt Target (gun #: see mis logbook) • use Ar flow to adjust sputter pressure • base pressure: < 1.0 e-6mbar • sputter pressure: 6.6 e-3mbar • power: 200W depositionrate = 22-27 nm/min	Or other metal!
		litho1500: Lift-Off with postive resists (WB11)		
238	ILP	**Lift-Off** **(#**litho500)	NL-CLR-WB11 Purpose: removal of resist and excess metal from the surface of the substrate by ultrasonication in Acetone. Use the ultrasonic bath in WB11. • Beaker 1: Acetone • Time = 10 min **Single wafer processing:** Spray the wafer with Acetone for 30 sec and immediately spray with isopropanol (IPA) for 30 sec. **Batch wafer processing:** • Beaker 2: Acetone • Time = 10 min • Beaker 3: Isopropanol • Time = 10 min	
239	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
240				Backside processing
241				Layers present on the back-side:

				thermal oxide of 2.0 um
242				
		litho1802: Lithography of Olin Oir 908-35 (positive resist - ILP)		
243	ILP	**Priming HMDS** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 Hotplate** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Settings: • Temperature: 150°C • Pressure: 25 inHg • Dehydratation bake: 2 min • HMDS priming: 5 min CAUTION: let the substrates cool down before handling with your tweezer!	
244	ILP	**Coating of Olin OiR 908-35** (#litho102)	NL-CLR- WB21 Coating: Primus coater • Olin OiR 908-35 • Spin program: 4000 (4000rpm, 30sec)	
245	ILP	**Prebake of Olin OiR 908-35** (#litho004)	NL-CLR-WB21 Prebake: Hotplate • Temperature: 95°C • Time: 120s	
246	ILP	**Alignment & exposure of Olin OiR 908-35** (#litho302)	NL-CLR- EV620 • Electronic Vision Group EV620 Mask Aligner • Hg lamp: 12 mW/cm ^{2} • Exposure time: 9sec	**Mask 5 - Channels**
247	ILP	**After exposure bake of Olin OiR resists** (#litho005)	NL-CLR-WB21 After exposure bake: Hotplate • Temperature: 120°C • Time: 60s	
248	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21** Development: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
249	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents.	

			Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
250	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
251	ILP	**Postbake of Olin OiR resists** (#litho008)	NL-CLR-WB21 Postbake: Hotplate • Temperature: 120°C • Time: 10min	
252	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
		etch1800: High Rate BOSCH - STD (Oxford Estrelas)		
253	ILP	**High Rate BOSCH** (#etch800)	**NL-CLR-Oxford Estrelas** Application: etching of large squares/holes (in the range of 400-1000 µm) in Silicon Process name: ..... Performance: • Etch rate: 20-25µm/min (at <5% loading) • Selectivity: ~300 (with respect to Olin OiR resists) • Aspect ratio: 0.5 • Scallop: ~350nm • Profile control: 90±10° Ref. document: PT6683.04/PV6683.02	Apply first test run (SEM etc), etch till trench is visible, apply in-situ FC strip.
254	ILP	**Stripping of Resists and Fluorocarbon** (#strip104)	**WARNING - PLEASE READ** This recipe is efficient for stripping of fluorocarbon in microstructures with aspect ratios < 5. Contact the administrator in case you want to strip fluorocarbon in microstructures with aspect ratios > 5 or fluorocarbon in nanostructures. This recipe attacks silicon and nitride coatings on the nanometer scale!	

NL-CLR-TePla360
Application: stripping of resists and fluorocarbon after DRIE BOSCH processing by O2/CF4 plasma.

Step	O2 (sccm)	Ar (sccm)	CF4 (sccm)	H2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0	0	0.6	1000	0:10:00
Resist stripping	250	0	0	0	0.5	800	*
Fluorocarbon stripping	237	0	13	0	0.5	800	0:01:00
Residual Fluorocarbon stripping	250	0	0	0	0.8	800	0:01:00

* Select one of the following recipes depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 035: time = 10min
Recipe 037: time = 20min

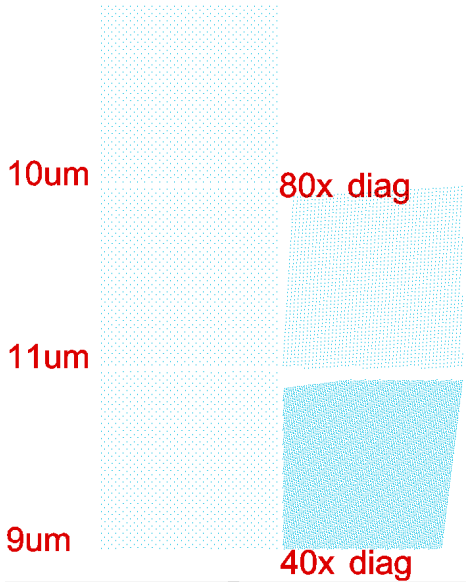
			Recipe 036: time = 60min **BACKUP**: The TePla300 is not a backup for this processing! If the TePla360 is down, contact the administrator. **PLEASE NOTE** It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you: • continue with UCP processing • continue with high-temperature processing (MFP)	
255	Rem Res	**Removal of metal traces in RCA-2** (#residue504)	**NL-CLR-WB09** Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	Skip
256	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	Skip
257	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	Skip
		etch1205: Etching in 50% HF (WB02/09/10-private use)		
258	ILP	**Etching in HF 50%** (#etch130)	NL-CLR-WB9/10 Use private beaker HF 50% standard Temp.: room temperature • Si3N4-H2 = 0.64 nm/min	**SLE etching**

			• SiRN-G3# (nanolab) = 3.1 - 3.5 nm/min • SiO_2 = 1 µm/min
259	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
260	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
261		**Freeze drying during SLE etch (and also thermal oxide on backside will be stripped (functioned was etch mask)).**	
262		**Anodic bonding with MEMpax (powderblasted) wafer**	
263		**Adhesive bonding with RIE wafer**	
264		**Dicing 500um deep slits at electrode locations**	
265		**Dicing chips**	

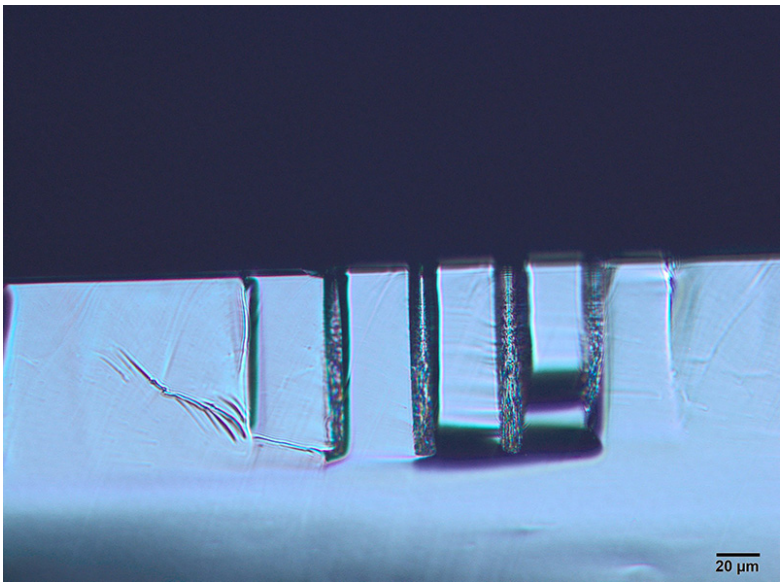
S8 Extended discussion and recommendations

S8.1 Material choices for the micro valves: As mentioned in the paper the micro valve geometries are based on the proposed design by Dubois et al. ([19]). Together with the application and the decision to use a combination of bulk and surface micro machining this characterizes the process outline (and thus process flow). We need at least three different materials that can be etched independently. As the membrane needs to be strong (can handle high differential pressures), an insulating and conductive material are needed and no metals can be used, the material choices become rather limited. For example, polymers (like polyamide) generally suffer from wear and tear, have a very low young's modulus and are not conductive. As the valve membrane should be suspended we need to create a layer between the substrate and the membrane that can easily be removed without damaging the other materials. Therefore, it was decided to choose heavily doped silicon as conductive material and silicon nitride as the insulating layer and valve seat. Silicon oxide was selected as SLE material as this has a high selectivity with respect to the former two materials if wet etching is used. Frequent use of these materials for MEMS devices is a major advantage compared to other materials.

S8.2 Chip clamp design: As the chip operation pressure can exceed $10\,\mathrm{bar}$ the chip clamp should be fabricated from a stiff rigid material like stainless steel. The clamp should have two slits to allow the IR beam to enter and leave the chip. Initially polyether ether ketone (PEEK) tubing will be used for the MF supply and return lines and can be replaced by (more expensive) stainless steel tubing when temperatures above $140\,^{\circ}\mathrm{C}$ are needed. When the chip is modular and it will needs to be compressed to get leak tight sealing of the reactor chamber it is very likely that the force on the chip, applied by the clamp, must be uniform to prevent breaking. The bolts that are responsible for the compression of the chip can be loaded with stiff strings to gain more control over the uniformity of the force applied across the chip. The chip will be joule heated by restive elements where the dissipated power is an indication of the chip temperature (for temperatures much higher than room temperature). Electric connections will be made with spring loaded pins (also called pogo-pins) that will be mounted in the clamp.



(a) CleWin image of three normal rasters and two staggered rasters.



(b) Microscopy images of cross-cut holes. Multiple holes of raster visible of which the third approximately broken through the center of the orifice.

Fig. 34: Staggered holes on mask 1 for easy wafer cleaving through an orifice.

S8.3 Mask test raster modification: Mask 1 contains multiple rasters with a high density of holes located at the edges of the wafer to verify the profile and depth after DRIE. The wafers were cleaved using a diamond pen tip. Despite the high orifice density, often multiple attempts were needed before a break line exactly went through a hole. Therefore, the rasters were modified in such a way that holes were staggered $5\,\mu\mathrm{m}$ in horizontal and vertical direction (see figure 34a). As a result, after cleaving the wafer, always at least one hole was exposed and in general multiple orifices could be analyzed under the microscope (see figure 34b).

S8.4 Layer thickness after thermal wet oxidation of poly-silicon: The resulting oxide layer volume after thermal oxidation of poly-silicon is calculated using the molecular weight and density of the two layers by the following equation:

$$V_{SiO_2} = V_{Si} \times \frac{\left(\frac{M_{SiO_2}}{\rho_{SiO_2}}\right)}{\left(\frac{M_{Si}}{\rho_{Si}}\right)} \tag{8}$$

Where V_{Si} is the initial layer volume of the poly-silicon layer, V_{SiO_2} the volume after thermal wet oxidation, M_{Si} and M_{SiO_2} the molecular weight of respectively the poly-silicon in the initial and oxidized state and ρ_{si}, ρ_{SiO_2} the densities of these layers. As the area of the layer is constant when Si is oxidized to SiO_2, the volumetric growth is equal to the expansion of the layer thickness. When substituting the relevant parameters it turns out that the oxidized state of poly-silicon is 2.19 times the initial layer thickness.

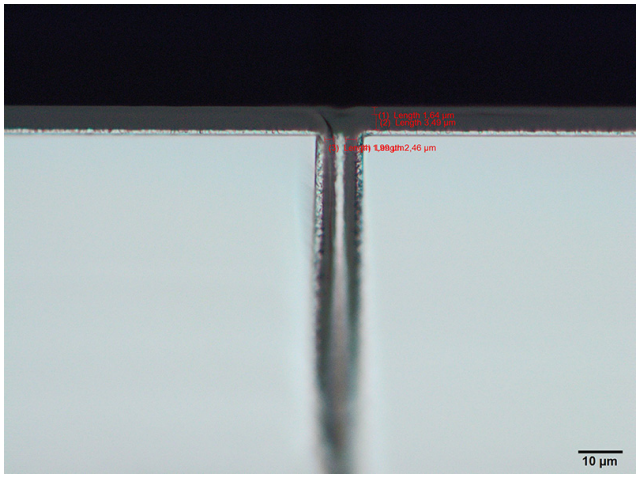


Fig. 35: $1.6\,\mu\mathrm{m}$ *thick TEOS layer grown on thermal oxide. Note that the orifice was already closed after wet oxidation giving a keyhole and therefore the hole is free of TEOS.*

S8.5 TEOS deposition: With the available equipment it was not allowed to grow a TEOS layer thicker than $1.2\,\mu\mathrm{m}$. As we need a final layer of 1.5um we considered a two step process with an anneal in between. As the anneal will introduce stress in the layers it is preferred to first pattern the layer before annealing which is not practical when performed twice because of additional process steps and the involved misalignment during lithography. Therefore plasma enhanced chemical vapour deposition (PECVD) was also considered as an alternative to LPCVD having the advantage that the oxide layer is grown only on one side of the wafer. However, as many wafers need to be processed this method is not preferred since it is very labor-intensive. As it turned out that the main reason for layer thickness restriction of the furnace is contamination, we decided to execute a two step deposition without anneal in between (e.g. $1000\,\mu\mathrm{m}$ and $600\,\mu\mathrm{m}$).[17] During the two TEOS depositions the wafer-carrier is also filled by wafers of other projects/companies to limit the furnace usage. In figure 35 you see a TEOS layer on top of an oxide layer after $2.5\,\mathrm{h}$ LPCVD.

S8.6 Wafer bonding alternatives: There exist many different bonding techniques to join multiple wafers together, which can be separated in temporary and permanent bonding methods. Closing the channels in the *valve wafer* by the MEMpax wafer is allowed to be a permanent bond and therefore anodic bonding was used. When sealing the reactor chamber and in order to allow easy exchange of the IRE there should be a temporary bond between the *IRE wafer* and the *valve wafer*. As mentioned in the paper, for testing purposes, we used SU-8 as a spacer and as bonding material, eliminating the need for a chip clamp and complex bonding. SU-8 can for example be replaced by poly-silicon when modularity and temperatures above $200\,^{\circ}\mathrm{C}$ are needed. Direct bonding is often used for bonding silicon but it is permanent and requires high temperatures and since the *valve wafer* contains metal contact pads this is not a solution. A high temperature compatible glue, adhesive bonding, eutectic and anodic bonding (e.g. via a pyrex layer) should be investigated to replace the SU-8 spacer in the future. If a chip clamp is used and the silicon surfaces are very smooth this will possibly eliminate the need for bonding.

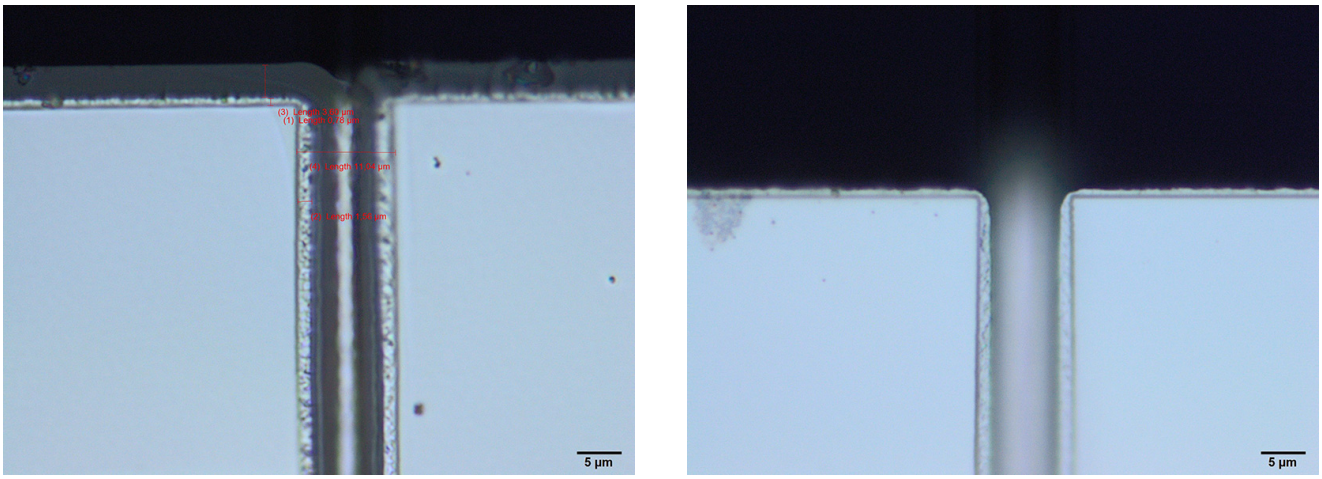
S8.7 Valve performance considering surface roughness and particles: There are many factors that can lead to bad performance of the micro valves like the stress and conductance of the membrane, morphology and surface roughness. The membrane stress can be controlled by annealing, and the conductance depends on the doping concentration. When the total poly-silicon layer is heavily doped this has the advantage that the resistance is lower than for doped membranes and

[17]The shrinkage of TEOS after annealing is approximately 8% giving a final layer thickness of $1.5\,\mu\mathrm{m}$

if only direct tracks to the contact pads exist. However, if an additional mask is used to pattern the doping concentration, the capacitance that arises between the substrate and poly-silicon layer can significantly be reduced, limiting the RC-time (and thus the valve response time). A known problem is the existence of 1 to $300\,\mathrm{nm}$ sized particles after LPCVD Si_3N_4 causing valve leakage. The chip contains over 5000 microvalves and performance is not much effected if a few valves are leaky. It depends on the density of particles whether this should be considered to be a problem or not. The morphology and surface roughness of the valve seats instead effect all micro valves and therefore directly influence the performance of the system.

S8.8 Experimental setup: First experiments will focus on valve function and performance. When the tensile stress in the membrane is not large enough stiction can occur. When the stress in the membrane is too high the valve doesn't close (completely). The same holds if there are large particles, as mentioned in subsection S8.7. The wafer contains multiple test chips that enables testing of individual valves (single or two interconnected) without the need for bonding the sandwitch construction (described in supplementary information S5). The masks are designed in such a way that even when the channel etching is problematic, the test chips can still be fabricated. For one and two valves the following properties will be measured: required actuation potential without differential pressure, the relation between potential and differential pressure to close the valve, effect of the temperature to the performance of the valve, the leakage flow and the switching speed. For the valve arrays the valve yield can be quantified by measuring the reactant gas flow when all valves are closed. Also the maximal flow rate for a given pressure is a relevant parameter to characterize the chips. The transition time of the chip can be measured by using ATR-FTIR in step-scan mode switching between N_2 and CO_2 gas as carbon dioxide is easy to identify with ATR-IR and nitrogen gas gives an empty spectrum. To test the platform with a catalyst at first a simple well predictable model reaction is preferred like the one described in [31].

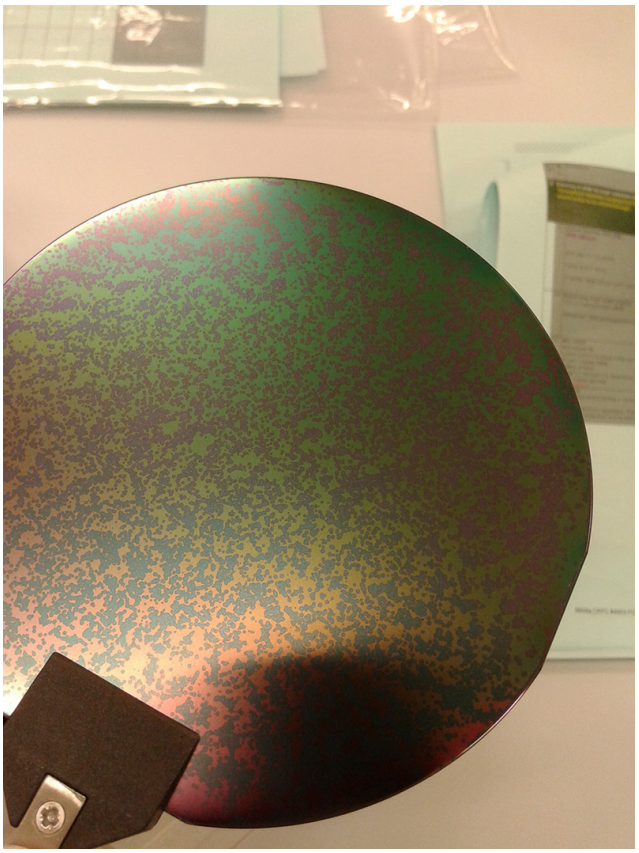
S9 Additional figures to results and discussion



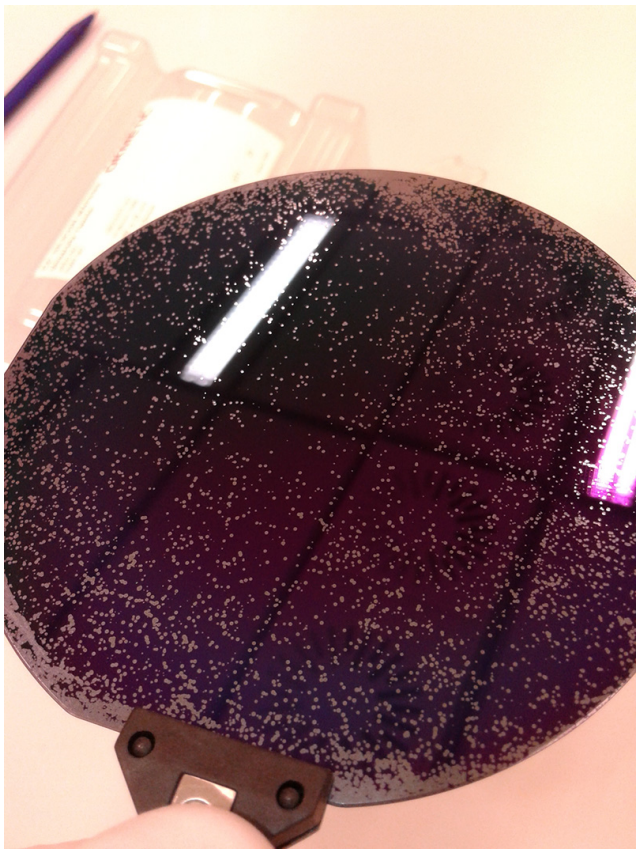
(a) View before 50%HF etch

(b) View after 50%HF etch

Fig. 36: Microscopy images used for oxide layer identification

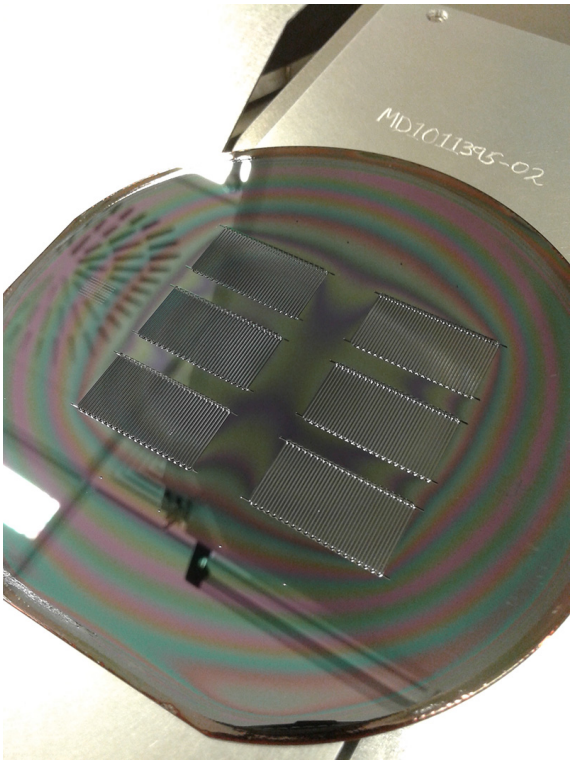


(a) Backside silicon wafer when poly-silicon layer was not removed prior to oxidation.

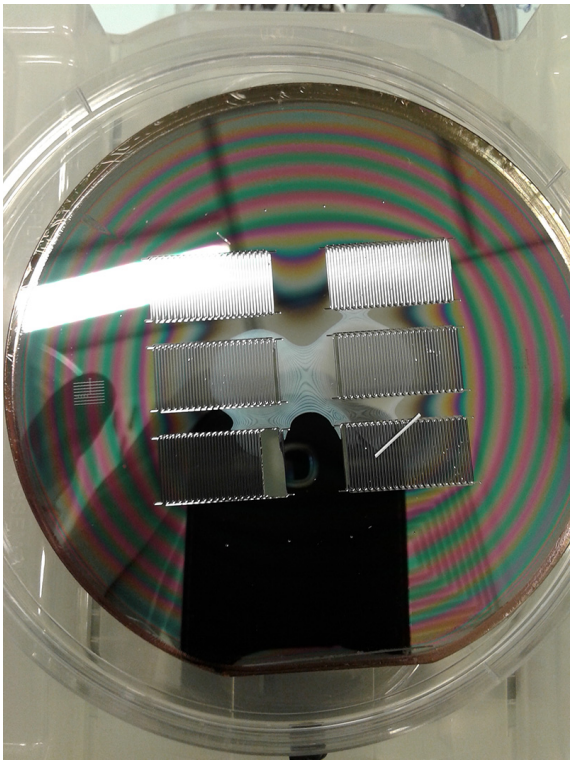


(b) Frontside silicon wafer when poly-silicon layer was removed prior to oxidation.

Fig. 37: Wafer appearances after full thermal wet oxidation of poly-silicon as a result of delamination caused by excessive stress in the layers.

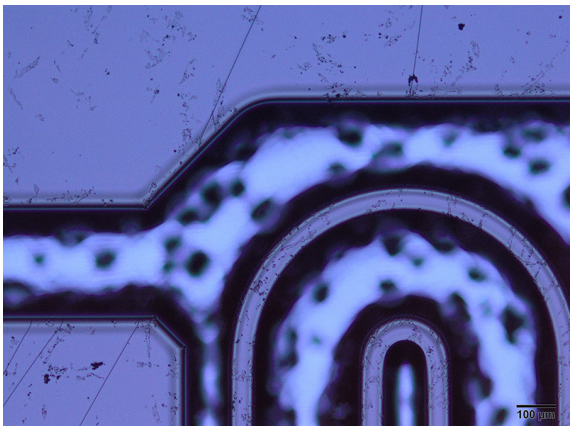


(a) Practically no mask on channel wall structures anymore. Channel walls are etched.

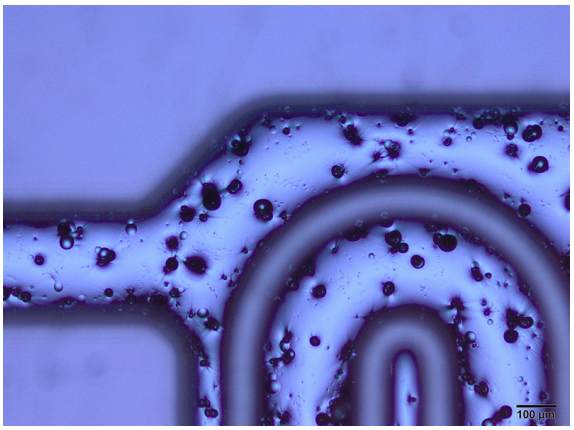


(b) Mask completely removed at the center of the wafer. Part of wafer perforated as a consequence of locally increased etch rate. Note part of broken channel wall on bottom right chip.

Fig. 38: Intermediate results during channel etching. At a certain point the mask selectivity decreases significantly and the mask is etched fast.

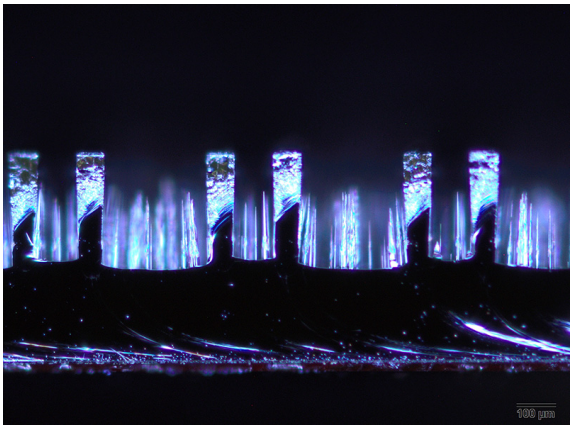


(a) Top view wafer, fine scallop HARS 1500 cycles, focus point on (cracked) resist .



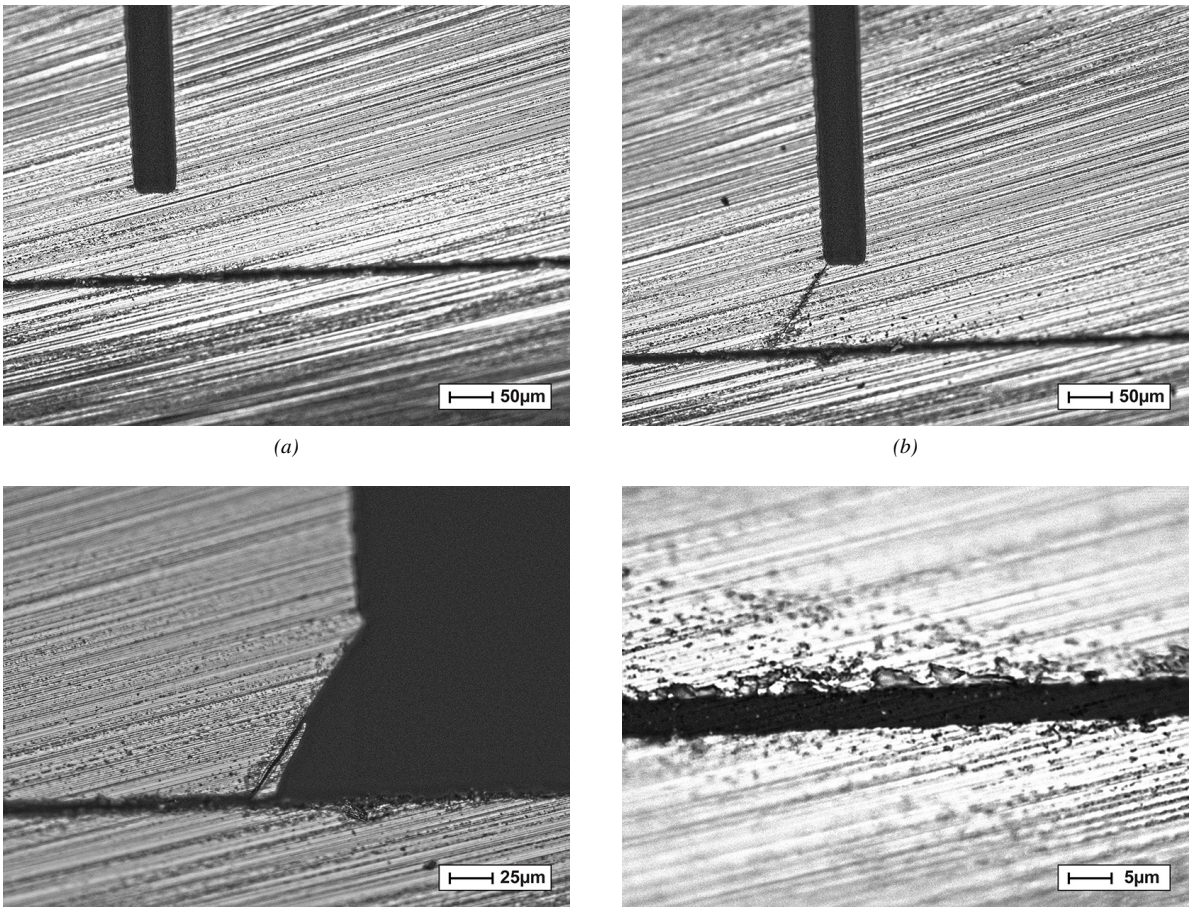
(b) Top view wafer, fine scallop HARS 1500 cycles, focus point on channel bottom, showing black silicon.

(c) Top view wafer, high rate HARS 1200 cycles, focus point on resist layer. Channels don't contain black silicon (for comparison).



(d) Cross section view of wafer, fine scallop HARS 1500 cycles, showing black silicon spikes.

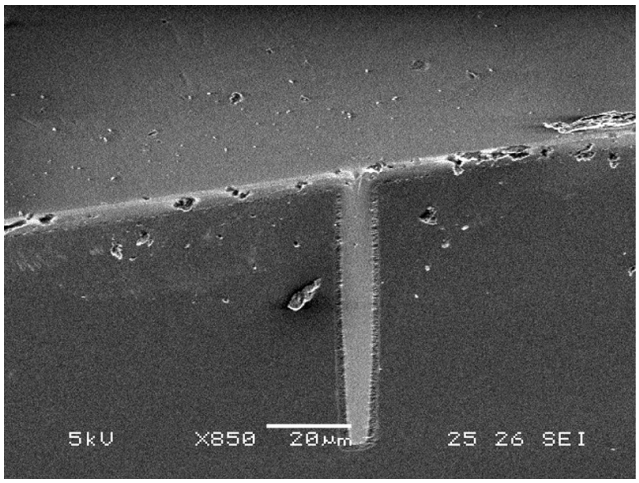
Fig. 39: Additional microscopic images of channels etching



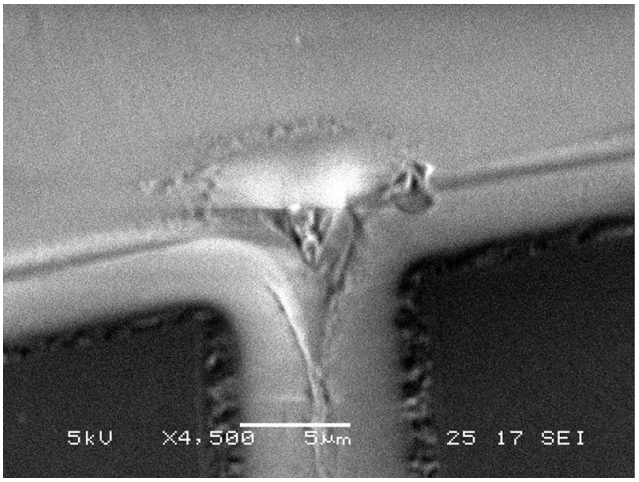
(a) *(b)*

(c) *(d)*

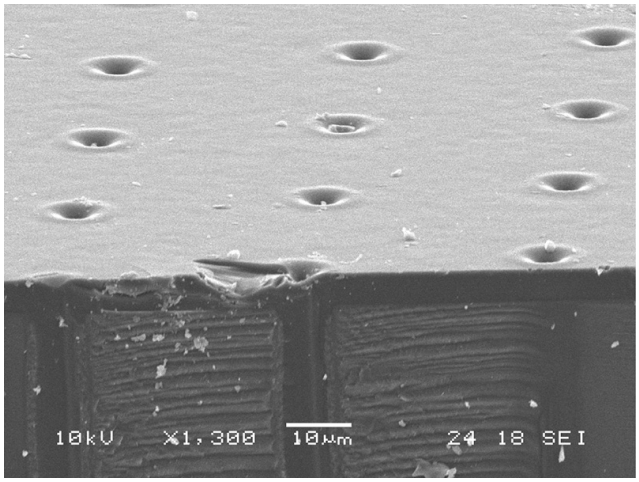
Fig. 40: Microscopic images of wafer dicing and breaking to access electric contact pads located beneath. a: slit is created in the top wafer using a $50\,\mu\mathrm{m}$ *dicing blade, b: pressure is applied locally using tweezers to break the wafer at the slit location, c: zoomed in picture (factor 2) of situation after removal of the released silicon part, d: optical bonding quality inspection of SU-8 adhesive bonding.*



(a) The trench is closed before all poly-silicon is converted to oxide as a consequence of a too thick poly-silicon layer.



(b) Detailed image of a single orifice filled with oxide. Note the grainboundaries of the poly-silicon layer that is not consumed during oxidation.



(c) Image of test rater showing multiple 10 µm orifices

Fig. 41: SEM images of trench filling after thermal wet oxidation