B.Sc. Thesis

Low-cost silicon-based resistive load cell suitable for asymmetric loads

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Summary

In this thesis, the viability of fabricating a silicon load cell out of a single p-type silicon-on-insulator (SOI) wafer using a single photomask and etching step is investigated. For this purpose, three silicon load cell designs have been designed and realized consisting of at least two gauges, one gauge on which a load is applied and one suspended gauge.

The work begins with a comparison of the three realized designs with earlier work produced by Wensink and Zwijze. After that the theoretical background of a silicon load cell is discussed. Starting with some general information about load cells followed by more in depth calculations about the piezoresistive effect in silicon load cells. Finalising the theory with some rough estimations of the load cell its capacity, sensitivity and resistance.

The theoretical part of the thesis is followed with the fabrication method of the proposed designs. After which the experimentals start where all three fabricated designs are measured using three test setups. One of these three test setups is intended for resistance measurement of each of the gauges of a fabricated load cell and the other two are intended to characterise the other parameters of the load cell e.g. sensitivity, creep, and temperature dependence. Five experiments are performed; a zero load measurement to get the resistance of the gauges, a temperature dependency measurement to test if the load cells are temperature dependent, a step response measurement both to test the load cell its sensitivity and creep, a linear load measurement to check the load cell its linear performance, and finally an experiment where the position of a load is determined using multiple load cells. The experiments are finalized with a comparison of the measurements between the three designs and those of Zwijze and Wensink.

The results of the experiment show a linear relation between the output voltage of the load cell and the applied load with a sensitivity in the order of 10 μV/N, corresponding to relative resistance changes in the order of $10^{-5}N^{-1}$. This linear relation was positive for design A and negative for design B due to reasons unknown. Moreover the load cells showed a relative large temperature dependence in the order of 10 μV/K, indicating that better matching between force sensitive and reference resistors is needed. Furthermore, a significant creep of 8% in 10 minutes was observed in all of the tested designs. This is most likely caused by the assembly process utilising epoxy glue. Lastly the position of a load was accurately determined using data from a test setup that could measure three load cells simultaneously.

Finally it is concluded that producing SOI load cells, using a fabrication process consisting of a single mask and etching step, can indeed be a viable way to fabricate these types of load cells. Possible applications lie in the medical field. However more research needs to be done in order to make these load cell designs a better alternative for currently available methods.

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1. Abstract

Many different types of force sensors, also known as load cells, exist. Usually consisting of a steel or aluminum structure with resistive strain gauges attached to it to measure the deformation due to a load. These sensors cannot be easily miniaturized. For applications requiring limited thickness force sensors, e.g. in the order of a few millimeters, an alternative is needed. Existing solutions, like force sensitive resistors, suffer from large creep, hysteresis, and temperature dependence. Silicon force sensors can be a good alternative because they do not suffer from creep or hysteresis.

In this thesis, a low-cost approach of realizing silicon force sensors is investigated. More specifically, it is investigated whether the boron doped silicon device layer in silicon-on-insulator (SOI) wafers can be used for piezoresistive force sensing. Fabrication requiring only a single photomask and etching step and therefore can be relatively cheap. Three sensor designs have been designed and realized, each with a different focus point in mind. Exploiting the buried oxide layer of a SOI wafer as sacrificial layer to realize freely suspended reference resistors that are used for temperature and stress compensation. The resistance of other resistors will change due to the piezoresistive character of p-type silicon.

Measurements show a linear relation between the output voltage and the applied load with a sensitivity of 10 μV/N, corresponding to relative resistance changes in the order of $10^{-5}N^{-1}$. A problem is that the sensors also show a relatively large temperature dependence, resulting in a change of output voltage in the order of 10 μV/K, indicating that better matching between force sensitive and reference resistors is needed. Furthermore, a significant creep of 8% in 10 minutes was observed due to assembly with epoxy.

It can be concluded that fabrication of silicon load cells with resistive readout from a single SOI wafer is indeed possible. However, some changes in the proposed designs are necessary in order to make them less sensitive to temperature and prevent creep.

2. Introduction

Resistive load cells, or force sensors, have been around for many years and are used in various applications for accurately sensing loads in many applications such as laboratory balances and larger industrial scales. Most resistive load cells used in the industry are strain gauges attached to a steel beam or rod. For small loads a relative large area needs to be reserved on the sensor in order to have room for the strain gauges. Moreover the performance of these gauges is limited by the creep and hysteresis of the steel used. However silicon does not suffer from these limitations, since it does not suffer from creep and hysteresis. Furthermore a silicon strain gauge can be easily placed in between two blocks, instead of being placed on the side of it by necessity. Making the whole assembly slimmer than conventional load cells and therefore useful in environments where space is limited.

Previous work in the field [Henk Wensink et al, 1998][1] (see figure 1) have fabricated resistive silicon load cells successfully using the bulk silicon as a stiff spring utilising the deformation of a membrane, and therefore also the strain gauges, to measure the load. However this load cell requires to be made with multiple wafers and masks that need careful alignment for the load cell to work. This thesis will investigate the viability of three different load cell designs made from a p-type silicon-on-insulator (SOI) wafer that uses the device layer of the wafer to carry the load instead, earlier also done by [Zwijze, 2000][2] (see figure 2). However this time using the SOI wafer its buried oxide layer as a sacrificial layer to suspend some of the load cell its structures and therefore eliminating the necessity of using more than one mask and a second wafer, making the production of the load cells cheaper (see figure 3). It must be said however that a second mask was used due to the SOI wafer also being used for different micro electro mechanical system (MEMS) designs that needed a treatment with a second mask.

Possible applications for this technology could be force measurement in the medical field. For example; a knee aligning sensor that does not suffer from hysteresis.

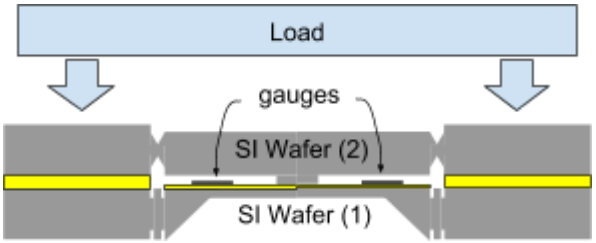


Figure 1, Wensink his device using two stacked SI wafers (1,2) using a membrane to create stress in the gauges (not to scale)

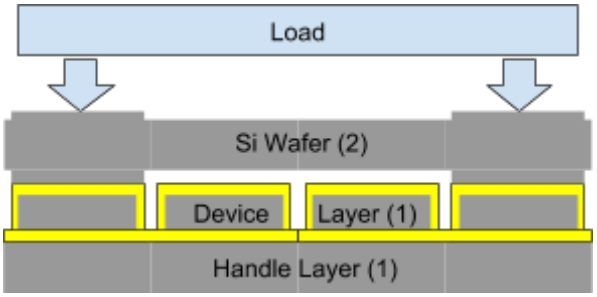


Figure 2, Zwijze his device using one SOI wafer (1) and a second Si wafer (2) to prevent strain in the reference gauges (not to scale)

[1] First Micromachined Silicon Load Cell for Loads up to 1000 kg - Henk Wensink
[2] Micro-Machined High Capacity Silicon Load Cells - Robert Zwijze

3. Theory

3.1. Principle

In conducting and semiconducting materials, changes in geometry, changes in length, width, and thickness of the material, due to mechanical stress causes a change in resistance of the material [3]. Furthermore due to changes in interatomic spacing, as a result from mechanical strain, affect the bandgaps in the materials themselves [5] making it either easier or harder for electrons to be raised into the conduction band and therefore changing the resistivity of the material. These two effects can be used in order to make a sensor that can accurately sense what force is applied to it by measuring the change in resistance of the sensor.

3.2. Theory behind a load cell

The resistance of a certain material can be calculated by following the same approach as in [3]. Using the following equation derived from Ohm's law for a rectangular conductor.

$$R_0 = \rho_0 \frac{l}{wt} \tag{1}$$

Where ρ_0 is the resistivity and l, w, and t the length, width, and thickness of the conductor with the current flowing in the l direction.

When the conductor is either stretched or compressed, by a mechanical force for example, the relative dimensional change is given by

$$\frac{\Delta R}{R_0} = \frac{\Delta l}{l} - \frac{\Delta w}{w} - \frac{\Delta t}{t} + \frac{\Delta \rho}{\rho_0} \tag{2}$$

This equation can be compressed by using Poisson's ratio ν and using $\varepsilon = \frac{\Delta l}{l}$ for strain

$$\frac{\Delta w}{w} = \frac{\Delta t}{t} = -\nu\varepsilon \tag{3}$$

Adding the previous two equations together gives

$$\frac{\Delta R}{R_0} = \varepsilon + 2\nu\varepsilon + \frac{\Delta \rho}{\rho_0} = (1 + 2\nu)\varepsilon + \frac{\Delta \rho}{\rho_0} \tag{4}$$

Finally the gauge factor GF (ratio of relative change in resistance to the mechanical strain) of the material can then be found by dividing everything by the strain

$$GF = \frac{\Delta R/R_0}{\varepsilon} = (1 + 2\nu) + \frac{\Delta \rho/\rho_0}{\varepsilon} \tag{5}$$

Where the terms between parentheses represent dimensional changes and the final term the change in resistivity of the material itself. This equation is mostly used in order to represent the sensitivity of a certain load cell.

In most metals the dimensional component of the equation is dominant [4]. However for semiconductor gauges the resistivity change of the material itself is significantly larger than that of the dimensional component, depending of the doping used [2], due to the piezoresistive effect. Therefore the latter will be neglected and all changes in resistivity will be assumed to be caused solely by the piezoresistive effect.

3.2.1. Piezoresistive effect

To approximate the scale of the change in resistance of a silicon load cell due to the piezoresistive effect, the same approach as in [7] is followed to generate a formula that describes the change in resistance of two resistive gauges as a function of force. The structure that will be examined can be seen in figure 3.

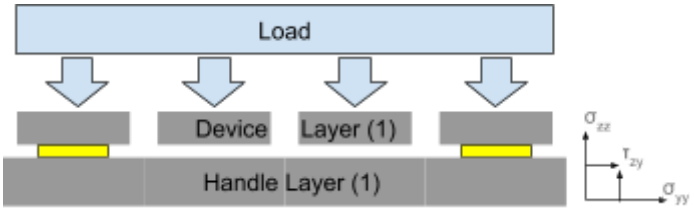


Figure 3, Tested device with one SOI wafer (1) with suspended reference gauges to prevent strain and a reference axis (not to scale)

It is assumed that the load cell has two strain gauges with length L (most left two gauges in figure 3 with L in the xx direction normal to the figure), one sensitive strain gauge where all the weight is distributed on via an insulating layer and one suspended strain gauge, for temperature compensation and resistance reference. Both the sensitive and the compensating strain gauges are mainly subjected to three normal stresses and their corresponding strains. Where $\sigma_{zz},\ \varepsilon_{zz}$ are the stress/strain in the direction of the applied force and $\sigma_{xx},\ \varepsilon_{xx},\ \sigma_{yy},\ \varepsilon_{yy}$ the in-plane stresses/strains. Any resistance changes in the direction of the current of the strain gauge, the xx direction, can be described in the terms of strain.

$$\frac{\Delta R}{R} = G_l\varepsilon_{xx} + G_t(\varepsilon_{yy} + \varepsilon_{zz}) + bT \tag{6}$$

Where G_l and G_t are the longitudinal and transverse piezoresistive strain coefficients that depend on the crystal orientation of the silicon and doping and b the temperature coefficient of resistivity.

In order to translate the strains into stresses, it is assumed that silicon behaves isotropic even though silicon is intrinsically an anisotropic material as can be seen in [6]. Using this assumption one can use the following equation for stress-strain relations [1].

$$\varepsilon_{xx} = \frac{\sigma_{xx}}{E} - \frac{v}{E}(\sigma_{yy} + \sigma_{zz}),\ \varepsilon_{yy} = \frac{\sigma_{yy}}{E} - \frac{v}{E}(\sigma_{xx} + \sigma_{zz}),\ \varepsilon_{zz} = \frac{\sigma_{zz}}{E} - \frac{v}{E}(\sigma_{xx} + \sigma_{yy}) \tag{7}$$

Where E is the Young's modulus and v Poisson's ratio. Combining (5) and (6) gives a formula of the relative change in resistance described in terms of stresses.

$$\frac{\Delta R}{R} = p_l\sigma_{xx} + p_t(\sigma_{yy} + \sigma_{zz}) + bT \tag{8}$$

Where

$$p_l = \frac{G_l - 2G_t v}{E} \text{ and } p_t = \frac{G_t(1-v) - G_t v}{E} \tag{9}$$

Here are p_l and p_t the longitudinal and transverse piezoresistive stress coefficients.

The stresses themselves, σ_{xx}, σ_{yy}, *and* σ_{zz} all consist of different contributions. First of all there are stresses consisting in both the sensitive gauge and the compensating gauge due to bending and stretching of the chip, let us call these σ_{xx}^{bend} and σ_{yy}^{bend}. Furthermore there are also stresses caused by a force being applied on the sensitive gauge and are not equal in both strain gauges. $\sigma_{xx}^{sens}(\sigma_{zz})$ will be defined as the stress in the sensitive gauge caused by a stress σ_{zz} in the same gauge. $\sigma_{xx}^{comp}(\sigma_{zz})$ will be defined as the stress in the reference gauge, caused by a stress σ_{zz} in the sensitive gauge. Moreover there are also shear stresses that are not by definition equal in both gauges. $\sigma_{xx}^{sens}(\tau_{xz},\tau_{yz})$ is the stress σ_{xx} in the sensitive gauge caused by the shear stresses τ_{xz}, *and* τ_{yz} on top of the sensitive gauge. $\sigma_{xx}^{comp}(\tau_{xz},\ \tau_{yz})$ are the stresses in te compensating gauge caused by the same shear stresses. The same explanation holds for the other in-plane stresses $\sigma_{yy}^{sens}(\tau_{xz},\tau_{yz})$ and $\sigma_{yy}^{comp}(\tau_{xz},\ \tau_{yz})$. Now the relative change between the two resistances can be written as

$$\begin{aligned}\frac{\Delta R_{sens}}{R_{sens}} &= p_l(\ \sigma_{xx}^{bend}+\sigma_{xx}^{sens}(\sigma_{zz})+\sigma_{xx}^{sens}(\tau_{xz},\ \tau_{yz})\ )\\ &\quad + p_t(\ \sigma_{yy}^{bend}+\sigma_{yy}^{sens}(\sigma_{zz})+\sigma_{yy}^{sens}(\tau_{xz},\ \tau_{yz})+\sigma_{zz})+bT\\ \frac{\Delta R_{comp}}{R_{comp}} &= p_l(\ \sigma_{xx}^{bend}+\sigma_{xx}^{comp}(\sigma_{zz})+\sigma_{xx}^{comp}(\tau_{xz},\ \tau_{yz})\ )\\ &\quad + p_t(\ \sigma_{yy}^{bend}+\sigma_{yy}^{comp}(\sigma_{zz})+\sigma_{yy}^{comp}(\tau_{xz},\ \tau_{yz})+\sigma_{zz})+bT\end{aligned} \qquad (10)$$

It was assumed that the silicon behaves linearly so $\sigma_{xx}^{sens}(\sigma_{zz})$, $\sigma_{yy}^{sens}(\sigma_{zz})$, $\sigma_{xx}^{comp}(\sigma_{zz})$, and $\sigma_{yy}^{comp}(\sigma_{zz})$ can therefore be written as linear functions of s_{zz} such that (10) can be written as

$$\begin{aligned}\frac{\Delta R_{sens}}{R_{sens}} &= p_l(\ \sigma_{xx}^{bend}+c_1\cdot\sigma_{zz}+\sigma_{xx}^{sens}(\tau_{xz},\ \tau_{yz})\ )\\ &\quad + p_t(\ \sigma_{yy}^{bend}+c_2\cdot\sigma_{zz}+\sigma_{yy}^{sens}(\tau_{xz},\ \tau_{yz})+\sigma_{zz})+bT\\ \frac{\Delta R_{comp}}{R_{comp}} &= p_l(\ \sigma_{xx}^{bend}+c_3\cdot\sigma_{zz}+\sigma_{xx}^{comp}(\tau_{xz},\ \tau_{yz})\ )\\ &\quad + p_t(\ \sigma_{yy}^{bend}+c_4\cdot\sigma_{zz}+\sigma_{yy}^{comp}(\tau_{xz},\ \tau_{yz})+\sigma_{zz})+bT\end{aligned} \qquad (11)$$

Where c_1, c_2, c_3, and c_4 are constants. Now by subtracting the compensating gauge its relative change in resistance from the sensitive gauge relative change gives the total change in relative resistance between the two gauges

$$\begin{aligned}\frac{\Delta R_{sens}}{R_{sens}}-\frac{\Delta R_{comp}}{R_{sens}} &= p_l(\ (c_1-c_3)\cdot\sigma_{zz}+\sigma_{xx}^{sens}(\tau_{xz},\ \tau_{yz})\ -\sigma_{xx}^{comp}(\tau_{xz},\ \tau_{yz})\ )\\ &\quad + p_t(\ (1+c_2-c_4)\cdot\sigma_{zz}+\sigma_{yy}^{sens}(\tau_{xz},\ \tau_{yz})-\sigma_{yy}^{comp}(\tau_{xz},\ \tau_{yz}))\end{aligned} \qquad (12)$$

From (12) can be concluded that a difference in temperature does not cause a difference in resistance. Furthermore the resistance will also not be dependent on any bending or stretching of the chip itself. Finally since the load cells will be loaded with a force applied via a flat surface, the shear stresses will be zero and therefore the equation becomes.

$$\frac{\Delta R_{sens}}{R_{sens}}-\frac{\Delta R_{comp}}{R_{sens}} = p_l(\ (c_1-c_3)\cdot\sigma_{zz}\ )+p_t(\ (1+c_2-c_4)\cdot\sigma_{zz}) \qquad (13)$$

Integrating equation (13) gives a formula where resistance is dependent on force

$$\frac{R_{sens}-R_{comp}}{R_0} = \frac{p_l(c_1-c_3)+p_t(c_2-c_4)}{wl} \cdot F \tag{14}$$

Where

$$F = -\int_0^l \sigma_{zz} \cdot a \, dl \tag{15}$$

With l as the total length of the gauge, w the width of a gauge, R_0 the resistance of a gauge at zero load, and F is the total force on the surface area of the sensitive gauge, which equals the integral of σ_{zz} in the sensitive gauge. Experiments done in [7] show that

$$p_t \approx p_l(c_1 - c_3) + p_t(c_2 - c_4) \tag{16}$$

Reducing (14) to a more pleasant formula

$$\frac{R_{sens}-R_{comp}}{R_0} = \frac{p_t}{wl} \cdot F \tag{17}$$

It can be concluded that, when there are no shear stresses in the load cell and when the compensating element is close and of the same resistance as the sensitive element under the assumption that the silicon behaves isotropically, the difference in resistance is only dependent on the total force on the load cell and independent on force distribution or temperature.

In order to confirm the assumption made in equation (13), where it was assumed that there are no significant shear stresses present in the chip, a simulation of the structure of figure 3 was done using Solidworks. In the simulation multiple of the structures were placed on the right side next to the original figure to generate the same behaviour as a whole chip. The results of the simulation are in figure 4 and 5.

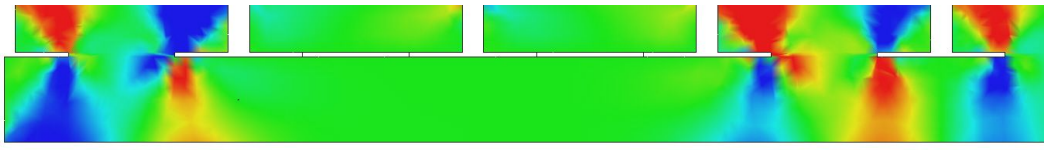


Figure 4, FEM simulation of the shear stresses of figure 3, where the green color is zero shear and the red and blue colors are 4E1 N/mm² [MPa] of shear in the positive and negative z direction in the xz plane

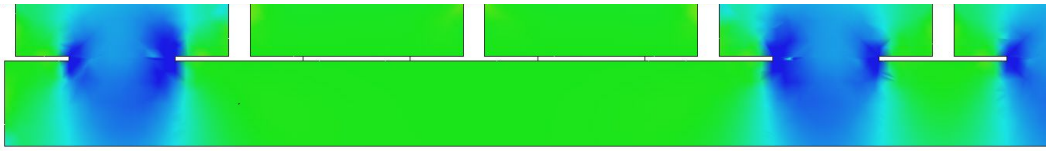


Figure 5, FEM simulation of the normal stresses of figure 3, where green is zero stress and the blue color is 2E2 N/mm² [MPa] of stress in the negative z direction

As can be seen in figure 4, there is certainly shear stress present in the chip. However this value is more than a factor 5 lower than the contribution of the normal stress everywhere in the chip as can be seen in figure 5. Furthermore the shear piezoresistive coefficient is more

than a factor 10 lower than the normal piezoresistive coefficient of p type silicon [2]. This generates a factor 50 or more difference in the resistance change due to normal stresses and shear stresses in the chip. Therefore it is concluded that the resistance change due to shear stresses can indeed be ignored.

3.2.2. Maximum capacity

The applications of a load cell may vary and therefore the maximum capacity of a load cell may be different for each application. In order to calculate the maximum capacity, one needs to know what the weakest point of the material, or in this case chip, is. The strength of the chip is limited by the material where the stresses in the material reaches the material its yield strength[3] first, at which point a material is effectively destroyed since it can no longer go back to its original shape. In this case, due to the process of creating a SOI wafer structure, the insulating layer between the handle and device layer of the chips. The following equation can be found using the equation for stress

$$\sigma = \frac{F}{A} \tag{18}$$

Replacing stress σ for the yield strength of a material gives the maximal force that can be applied on a material until it yields. As can be seen increasing the surface area of the sensitive element of te chip, and thus increasing the surface area of the insulating layer, will make for a load cell that can withstand more force until it breaks.

[3] The maximum force that can be applied until a material permanently deforms or yields

3.3. Load Cell Designs

Using the knowledge that an increase in mechanical strain creates a change in resistance of silicon, a load cell can be constructed. Three designs have been made with different design aspects in mind with the following constraints with a short explanation where the constraint is based on:

- The chip needs to be constructed out of a single SOI wafer using a single mask
  The basis of the research done done in this thesis
- The chip needs to have both a sensitive and reference gauge on chip
  Necessary in order to create a Wheatstone bridge that uses the reference gauge to balance the bridge
- The chip needs to support a cylindrical insulating pushing block of 5mm in diameter
  The test setups used utilise a circular pushing block of this dimension for force application
- The chip needs to have a dimension of 8200µm by 8200µm
  Necessary due to batch fabrication of these chips
- The gauges on the chip need to have a no-load resistance between 100Ω and 100kΩ
  Lower values will cause the material to behave like a heat element and a higher values will cause a lot of noise in the system
- The sensitive gauge needs to have a width of 100nm
  To be able to compare the performance of multiple chip designs

Moreover each of the three designs has a different focus point and this is discussed below.

3.3.1. Design A

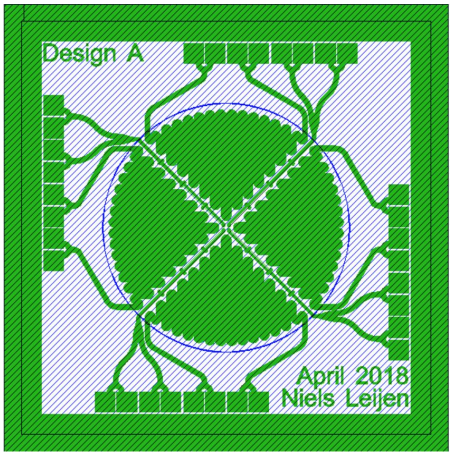


Figure 6, Load cell design A

	Design A
L sens	(4x) 36.5 mm
W sens	100 um
H sens	25 um
L comp	(4x) 5.0 mm
W comp	13.8 um
H comp	25 um

Table 1, Design A parameters

The main focus of the design in figure 6 is maximizing the sensitive surface area of the load cell while also being capable of distinguishing both a normal force and two moments by using the measurements of multiple sections of the load cell. The main disadvantage of this design is that the compensating element is of a different shape and dimensionally much smaller than the sensitive element and thus has a chance to not be perfectly in balance with the sensitive element. Moreover the compensating element is also in a different orientation than the sensitive element and, due to the material used, the resistance may depend on orientation. Furthermore the compensating element is not directly next to a sensitive element and therefore shear stresses will not be perfectly cancelled out.

3.3.2. Design B

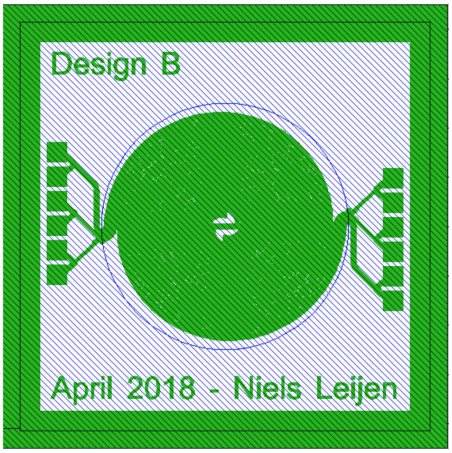


Figure 7, Load cell design B

	Design B
L sens	(1x) 67.0mm
W sens	100um
H sens	25um
L comp	(2x) 67.0mm
W comp	50um
H comp	25um

Table 2, Design B parameters

The design in figure 7 is focussed on a circulair single sensitive element with a compensating element that is both next to the sensitive element and has the same total surface area as the sensitive element. This ensures that differences in temperature will be correctly compensated and that the resistance of the sensitive element is the same as the compensating element ensuring the load cell is in balance. The disadvantages of this design are that it can only sense the normal force and the compensating element uses a relatively large area underneath the pressing block.

3.3.3. Design C

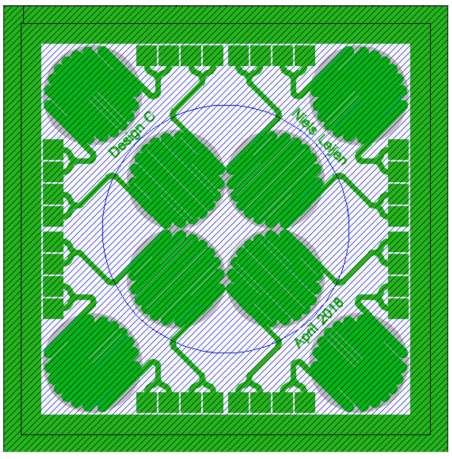


Figure 8, Load cell design C

	Design C
L sens	(4x) 24.3mm
W sens	100um
H sens	25um
L comp	(4x) 24.3mm
W comp	100um
H comp	25um

The final design, that can be seen in figure 8, is focussed on having the same compensating and sensitive elements all in the same shape while still being able to sense both the normal force and two moments. Having exactly the same shaped element ensures that the load cell will have perfectly balanced sensitive and compensating elements at zero load. However, due to the fact that the compensating elements are not next to the sensitive elements, in plane stresses and strains likely will not be correctly compensated for and sudden temperature changes will also not be correctly compensated by the compensating elements due to the relative big distance between the sensitive and compensating elements.

3.4. Theoretical output

3.4.1. Capacity

All chip designs have different shapes for the sensitive gauge in the area where load is applied, the 5mm circular area in the middle of the chip. Therefore their maximum capacity will be different as well. Filling in equation (18), using the lengths as can be seen in tables 1 to 3, a width of 50 μm[4] and for the yield strength 45 MPa. For simplicity it is assumed that the load has an uniform force distribution over the whole contact area. This generates the following formula

$$Capacity \Rightarrow F_{max} = \sigma_{yield} wl = 45 \cdot 10^{6} \times 50 \cdot 10^{-6} \times l\,[N] \quad (18)$$

Filling in equation (18) and, dividing the answer by 9.81 to transform the values from Newton to kg, gives the following table

	Design A	Design B	Design C
Capacity	34 kg	15 kg	22 kg

Table 4, theoretical maximum load cell capacity of each of the three chip designs

As can be seen in table 4 design B theoretically has the lowest theoretical capacity, mainly due to fact that the compensating element in this design uses a significant part of the chip underneath the sensitive area. During further experiments a safety factor of 2 will be used in order to make sure that there is no damage to the chips. Although the actual capacity of the load cells will likely be higher, assuming no point load is applied, due to the conservative yield strength value chosen in formula (18).

3.4.2. Sensitivity

Using the values in table 1 to 3, a rewritten form of formula (17) can be used in order to get an estimation what sensitivity of the load cells will be. It is assumed that the chip is used as one half of a wheatstone bridge with the sensitive element at the top and a compensating element at the bottom of the half bridge. The other half of the bridge consist of a resistor divider that has exactly the same resistances at zero load as the half where the chip is attached to. This gives the following equation for the sensitivity of the bridge.

$$Sensitivity \Rightarrow \frac{1}{F} = \frac{p_t}{wl}\ \left[\frac{1}{N}\right] \quad (19)$$

Where $p_t = 6.48 \cdot 10^{-11}\left[\frac{1}{Pa}\right]$ and the values for w and l are in tables 1 to 3. This gives

	Design A	Design B	Design C
Sensitivity	4.3E-3 N^{-1}	9.3E-4 N^{-1}	6.4E-4 N^{-1}

Table 5, Theoretical sensitivity of chip designs A, B, and C

If one compares the values of table 4 with the ones of table 5, one can see that the more load the chip can handle, the less sensitive it becomes.

[4] Value determined using a rejected chip of design A that had the silica layer exposed

3.4.3. Zero load resistance

The theoretical resistance of each element can be found by filling in formula (1) using the information given by the producer of the SOI wafers (see attachment SOI wafer data). This gives the following formula with only the dimensions of the elements as the unknowns

$$R_{theory} = 50 \cdot 10^{-6} \frac{l}{wh} \tag{20}$$

Using the values in tables 1 to 3, the theoretical resistance values of designs A,B, and C can be found

	Design A	Design B	Design C
R_{sens}	730 Ω	1340 Ω	486 Ω
R_{comp}	725 Ω	2680 // 2680 Ω	486 Ω

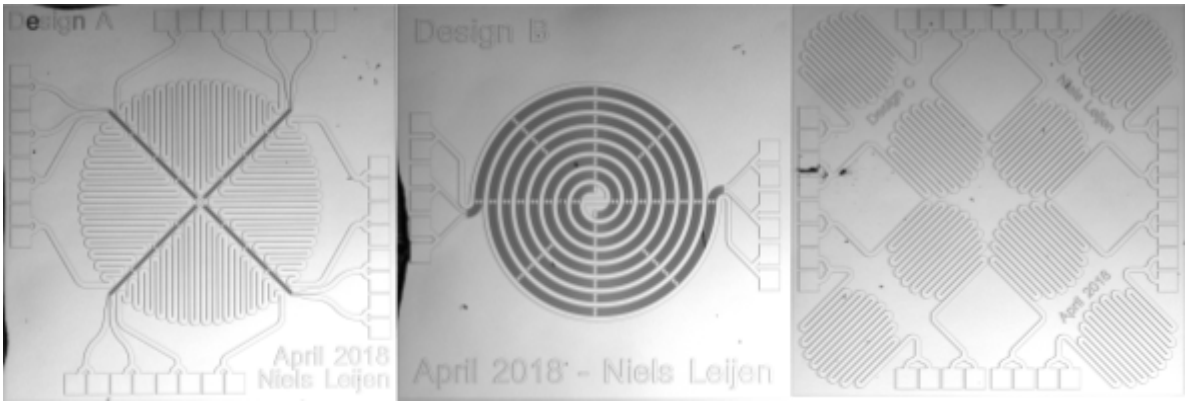
Table 6, Theoretical resistance of the gauges in the load cell designs

As can be seen in table 6, the resistances of the load cells stay well within the design constraints stated earlier.

4. Experimental procedure and results

4.1. Fabrication

Three chip designs were fabricated using the process described in attachment SOI wafer process. After fabrication the chips were visually inspected and glued in the middle a glass plate with epoxy glue (see attachment preparation load cell for more detailed steps and figures 9 to 11 for the fabricated chips). Finally the chips were bond wired to gold plated contacts and ready to be wired to the measurement circuit.



Figures 9, 10, and 11, fabricated chip designs A, B, and C (not yet bond wired)

4.2. Experiments

Multiple experiments were performed using multiple test setups. Firstly a zero load resistance measurement, to confirm that the resistance is within the set constraints. Secondly a temperature dependence measurement was done. Mainly to compare the performance of these chips with those of Zwijze. Moreover a step response test was performed to see if any creep is present. Furthermore a linear response test was done to test the chip its linear performance. Finally a load position determination test was performed to see if it is possible to determine where a load was placed on a test setup. See table 7 for an overview of which experiments was done with which test setup. The specifics of each of the test setups will be discussed later.

	Zero load resistance	Temperature dependence	Step response	Linear response	Load position Determination
Design A	Setup 0	Setup 1	Setup 1	Setup 1[5]	-
Design B	Setup 0	Setup 2	Setup 2	-	Setup 2
Design C	Setup 0	-	-	-	-

Table 7, Overview of the tests performed on the chip designs A,B, and C with which test setup

[5] This Experiment was performed twice; once using a chip that had a loose pushing block and a second time using a chip that had a pushing block epoxy glued on top

4.2.1. Test setups

Three different test setups were used to characterise the three chip designs. Two of which were designed to test the chip its load performance and one specifically to test a chip its resistance.

4.2.1.1. Setup 0

The first test setup, setup 0, its sole purpose is to measure the resistance of each of the chip its gauges. The schematic of the setup can be seen in figure 12.

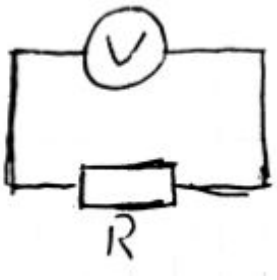


Figure 12, Schematic of setup 0

The setup consists of a HP 34401A multimeter that uses the two wire resistance measurement method to be able to measure the resistance of each of the gauges (this method was chosen over the four wire method due to the designs having up to 32 bond pads and it was more time efficient needing to only bond half of those pads). The multimeter had a BNC cable connected to it that could be connected to a gauge of a chip via a BNC connector.

4.2.1.2. Setup 1 and 2

The other two test setups are made to be able to characterise the load performance of each of the chips and support one or more completed chip assemblies. The test setups can be seen in figures 13 and 14 and in the attachments test setup 1 and test setup 2.

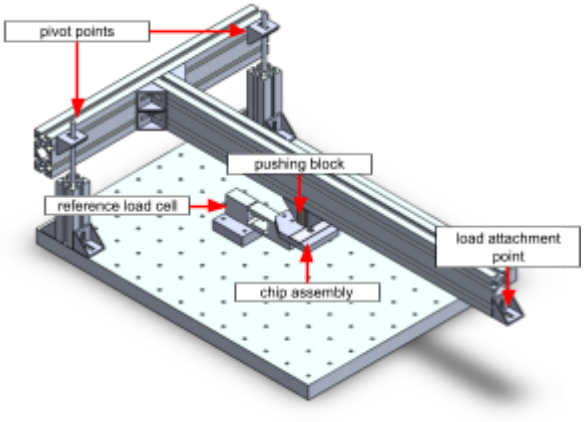


Figure 13, Render of test setup 1

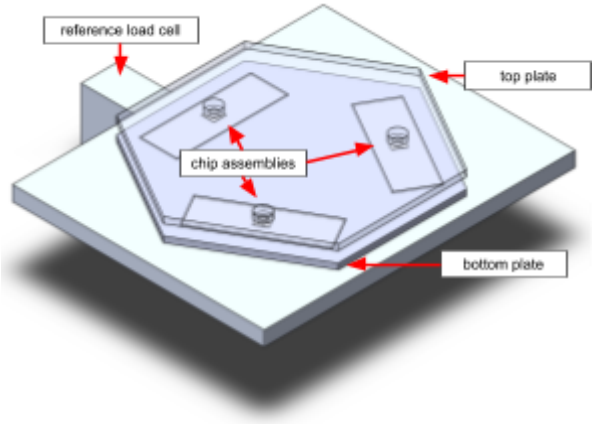


Figure 14, Render of test setup 2

As can be seen in figures 13 and 14, the test setups are quite different. Although both test setups use the same reference load cell. Setup 1 consists of a triangular beam that has two adjustable pivot points, allowing a different angle of the pressure block on top of the chip assembly. The end of the triangular beam has an attachment point mounted for a water container that acts as the load. The load attached multiplied by a factor 2 due to the chip

assembly being in the middle between the load and pivot points, generating up to 1000 Newton of force on the chip.

Setup 2 is constructed out of two hexagon aluminium plates. The top plate having three pushing blocks, one for each of the chips. Whereas the bottom plate has indicators on where to place each of the three chip assemblies. Moreover, the bottom plate provides a place to attach a pt1000 temperature sensor for accurate temperature sensing. The 2mm aluminium plates allow for a maximum total capacity of 200 Newton. To make comparison easier, all the main differences of the test setups are summed up in table 8.

	Test capacity	Pressure block angle	Temperature measurement	Supported chips
Setup 1	0-1000 N	Adjustable	External K-type	1
Setup 2	0-200 N	Fixed	pt1000	3

Table 8, Comparison between test setup 1 and 2

Both test setup 1 and 2 use the same equipment to measure the chips in the chip assemblies. The equipment consists of a HP 34401A multimeter that is connected to a matrix card in a HP 34970A to allow switching between each of the separate gauge pairs in the chips or setup. The reference load cell (see attachment load cell) is powered by a Agilent E3631A power supply. Another output of this same power supply is used to power the gauges in each of the tested chips. Labview NXG was used to automate the measurements (see attachments Labview panel and Labview diagram).

4.2.2. Measurements

4.2.2.1. Zero load resistance

To test if the gauges meet the resistance constraint, each of the gauges of the chips were connected to the multimeter of test setup 0. This was done with bond wires connected to gold plated contacts. These contacts had wires soldered on them that could be connected to a BNC connector and then use this connector to attach the gauge to the multimeter. After that the multimeter was nulled and the resistance of the gauges on each of the chips was measured accordingly. The results of the measurements are in table 9.

	Design A	Design B	Design C
R_{sens}	W1C1: 388, 369, 400, 384 W2C1: 432, 432, 442, 439	W1C1: 698 W2C2: 915 W2C3: 918 W2C4: 887	W2C1: 300, 289, 287, 290
R_{comp}	W1C1: 397, 401, 431, 369 W2C2: 447, 457, 451, 443	W1C1: 1235, 1236 W2C2: 1615, 1619 W2C3: 1629, 1626 W2C4: 1581, 1582	W2C1: 269, 283, 291, 280

Table 9, Measured resistance values. The Wx stand for chips of the same wafer and Cx stands for an unique chip and comma separated values are multiple gauges on that are present on a single chip measured anti-clockwise starting at design x text

As can be seen from the measurement in tables 6 and 39 the resistance of the resistive elements are about a factor 2 higher than calculated in formula (20). Furthermore the chips of wafer 1 had significantly lower resistance values than the chips of wafer 2. So if consistency of the resistance of the load cells is required, one needs to use chips of the same wafer.

4.2.2.2. Temperature dependence

In order to compare the chips to those of Zwijze, and to confirm or disprove that the actual temperature dependence is indeed zero, the temperature dependence of design A and B was measured. This was done by attaching the gauges on the chips to a channel of the measurement setup of test setup 1 and 2, using the same BNC connectors used in the zero load resistance measurement. Figures 15 to 18 describe how the two chip designs were connected to each of the channels of the test setup 1 and 2. Furthermore design B uses an external half bridge composed of three resistances $R_{b1},\ R_{b2},\ and\ R_{b3}$ with $R_{b1} = R_s - 50$, $R_{b2} = 100$, and $R_{b3} = R_c - 50$ to complete the Wheatstone bridge.

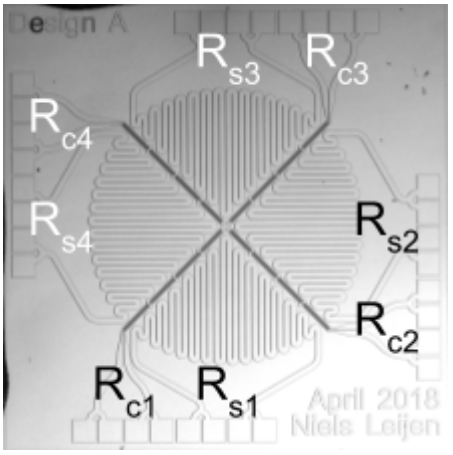


Figure 15, Gauge definitions design A

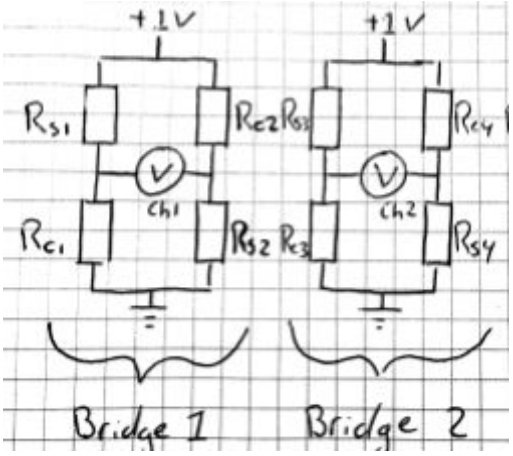


Figure 16, Connection schematic design A in Wheatstone bridge configuration

Figure 17, Gauge definitions design B

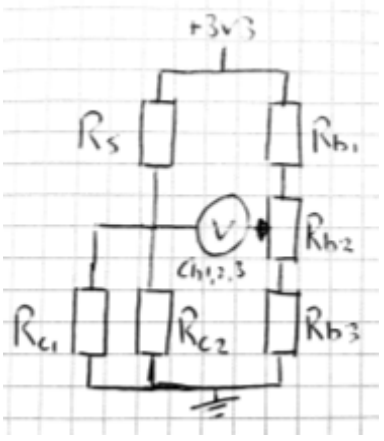


Figure 18, Connection schematic design B with external half bridge

4.2.2.2.1. Design A

A K-type thermocouple was placed next to the chip that was placed on setup 1 and connected according to figure 16. Next the output of the Wheatstone bridge and surrounding lab temperature were measured every 30 seconds for about 2 hours while no load was applied on the chip. The results of this experiment are in figure 19.

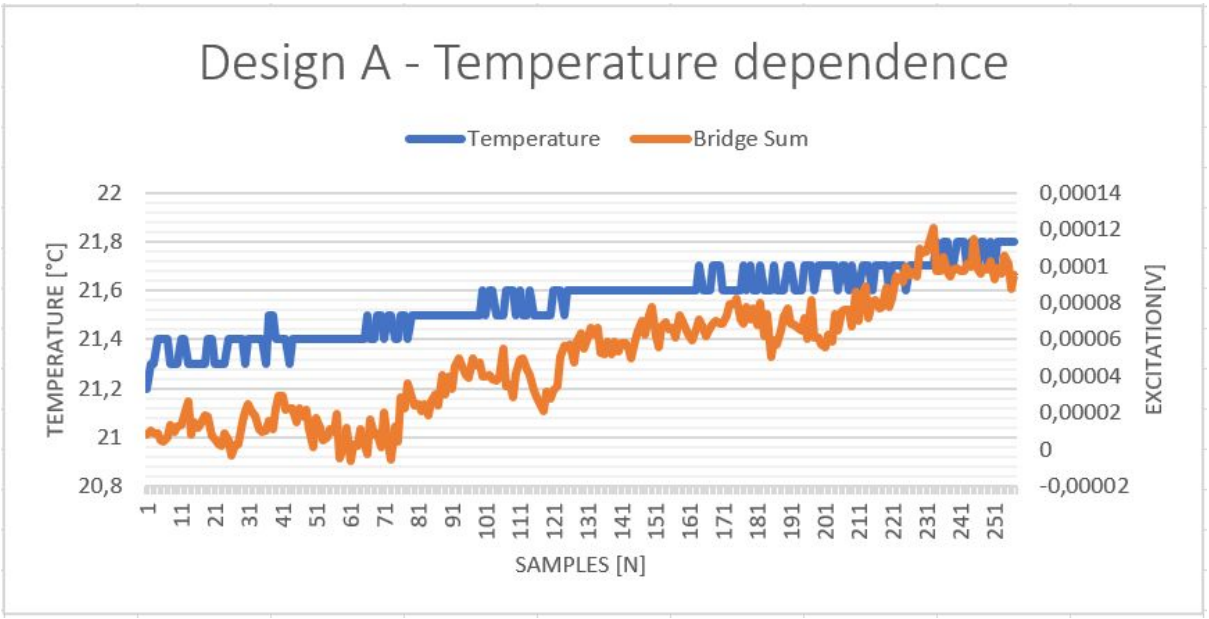


Figure 19, Temperature measurement result design A in test setup 1 with a sample time of 1/30Hz

As can be seen in figure 19 there seems to be a slight linear increase in both the temperature and the and the total excitation of the bridge. In order to confirm this the excitation, the output of the chip, was plotted against temperature (see figure 20).

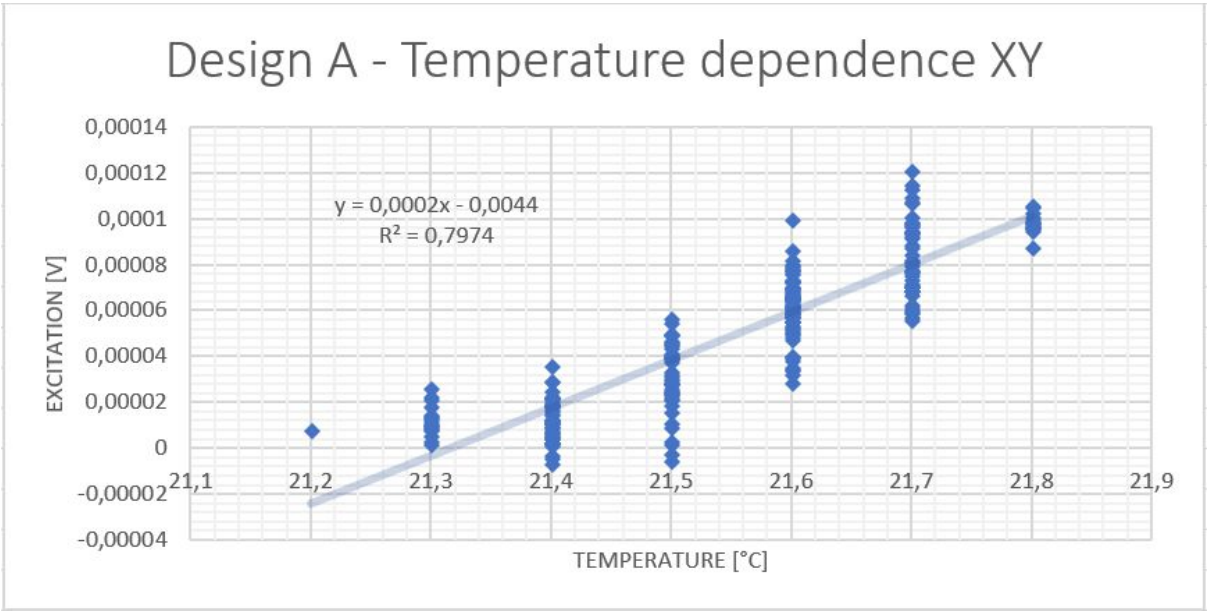


Figure 20, Temperature vs excitation design A with linear trend line

Using a linear fit the temperature dependence can be determined and seemed to be

$$2 \cdot 10^{-4} \left[\frac{V}{°C}\right]$$

It must be said that the coefficient of determination is quite low, only 0.80 , so there could be other factors also of influence. However this low value is most likely caused by the low resolution of the temperature sensor.

4.2.2.2.2. Design B

Just as done before with design A, the surrounding temperature was measured by leaving the chip unloaded on a test setup. This was done for one hour using test setup 2, due to test setup 1 being utilised by design A, with a sample rate of 2/9Hz. The schematic can be found in figure 18, the results are in figure 21. The values of figure 21 are normalized to be able to compare them with figure 19.

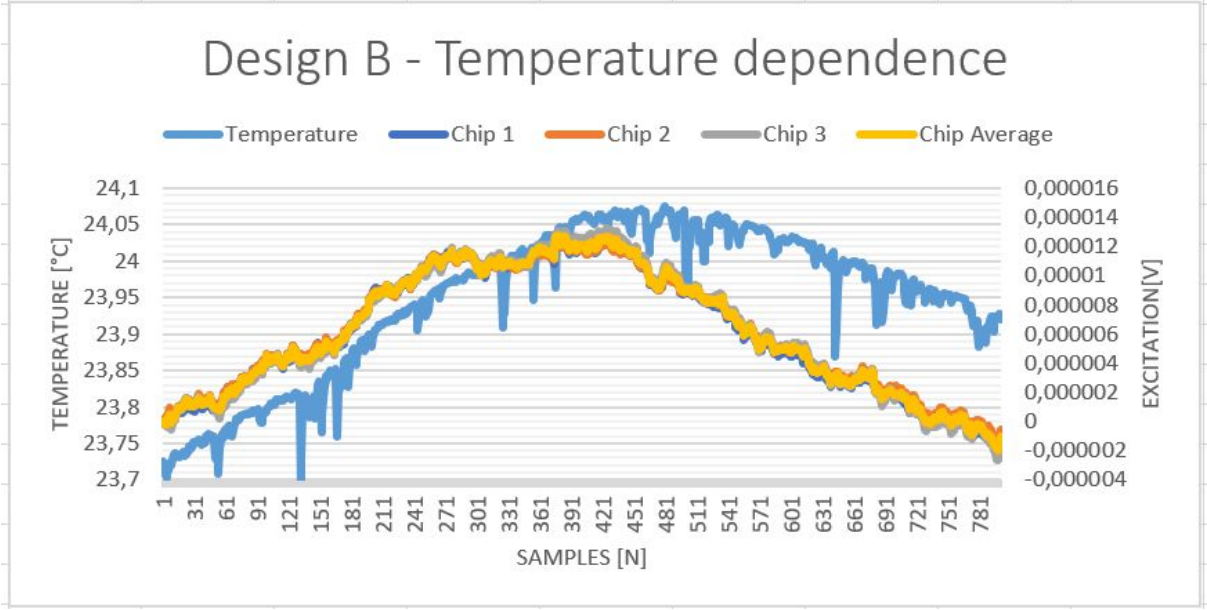


Figure 21, Temperature measurement result design A in test setup 2 with a sample time of 2/9Hz

As can be seen in figure 21, again a linear correlation seems to be present between the excitation voltage of the load cells and the room temperature. Moreover it can be seen that the temperature sensor seems to be lagging with the excitation change of the load cells. In order to get more insight, the temperature is plotted against the average excitation voltage of the three chips (see figure 22).

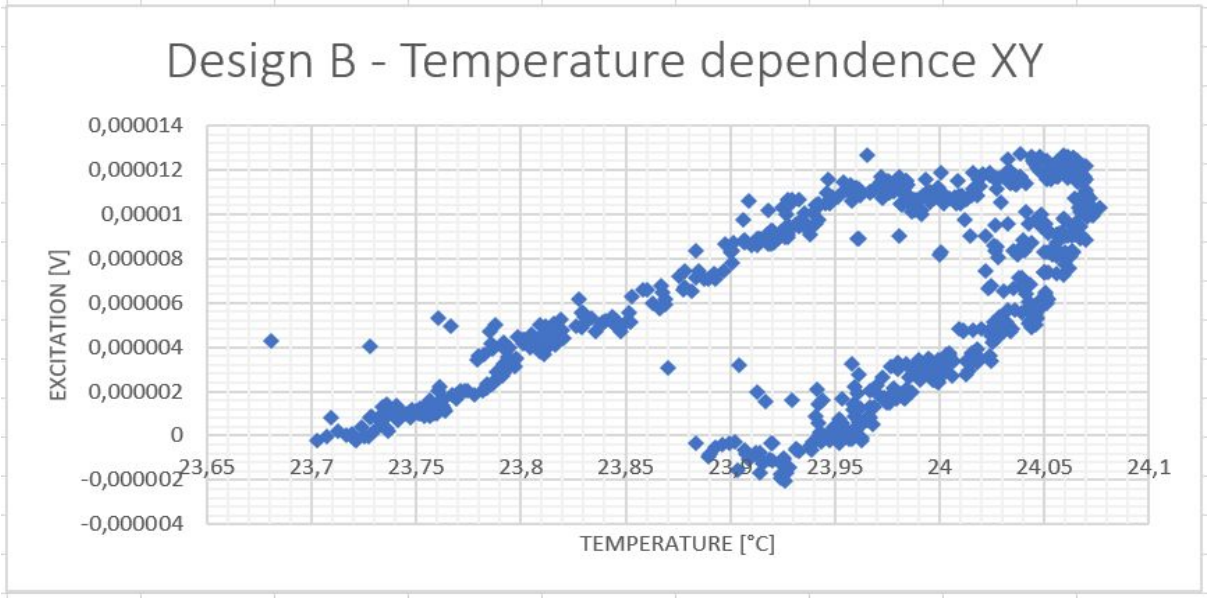


Figure 22, Temperature vs average excitation design B

The suspected lag of the system is confirmed in figure 22. However for a steady linear increase or decrease of temperature, this added time coefficient due to lag does not influence the temperature dependency. Therefore the value of the temperature dependence can still be found using a linear fit for the first 400 samples in figure 21, this gives figure 23.

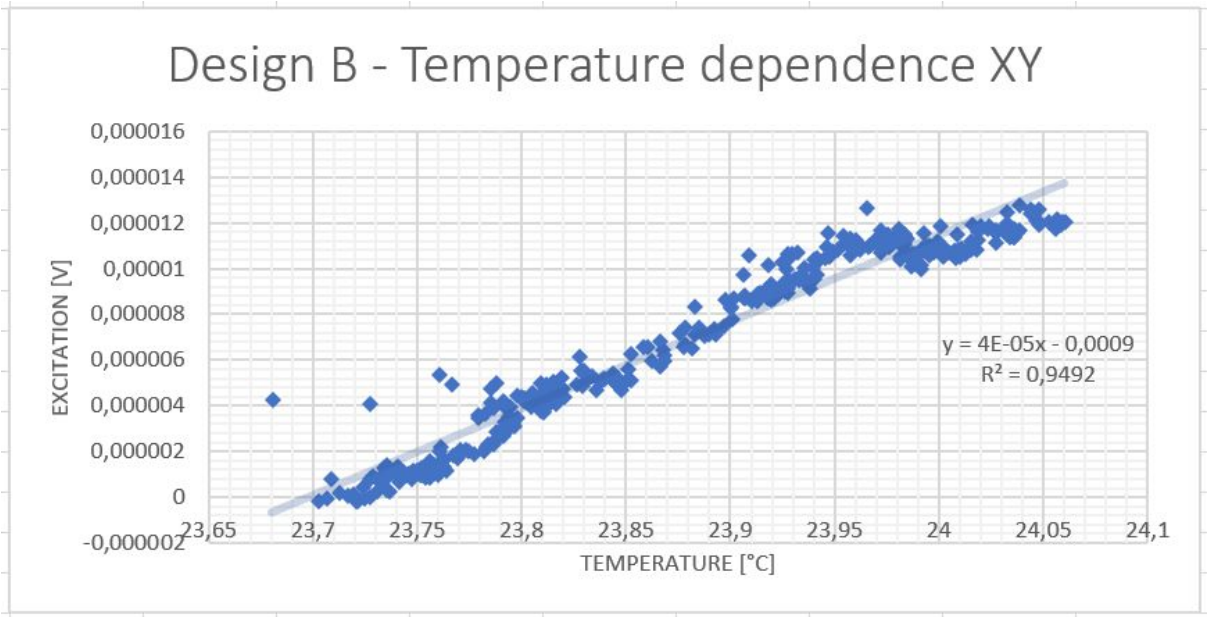


Figure 23, Temperature vs average excitation design B with linear trend line using the first 400 samples

As can be seen in figure 23 a convincing R square value of 0.95 was found using the linear fit. Furthermore it can be concluded that the excitation voltage increased with about $4 \cdot 10^{-5} \frac{[V]}{[°C]}$.
This is five times lower than that of design A. This could be either due to the external half bridge partly compensating part of the temperature coefficient or the different shape of the gauges of the chip or a combination of both.

4.2.2.3. Step response

To determine the sensitivity of the chips and to see the effect of creep, an experiment was performed where the test setups were loaded for 30 minutes and thereafter unloaded and left for 30 minutes.

4.2.2.3.1. Design A

Test setup 1 was once more used to measure design A and wired up the same way as in the temperature measurement. The test setup was loaded using an empty water container that was attached to the load attachment point that can be seen in figure 13. This was done multiple times. The result of this measurement can be seen in figure 24.

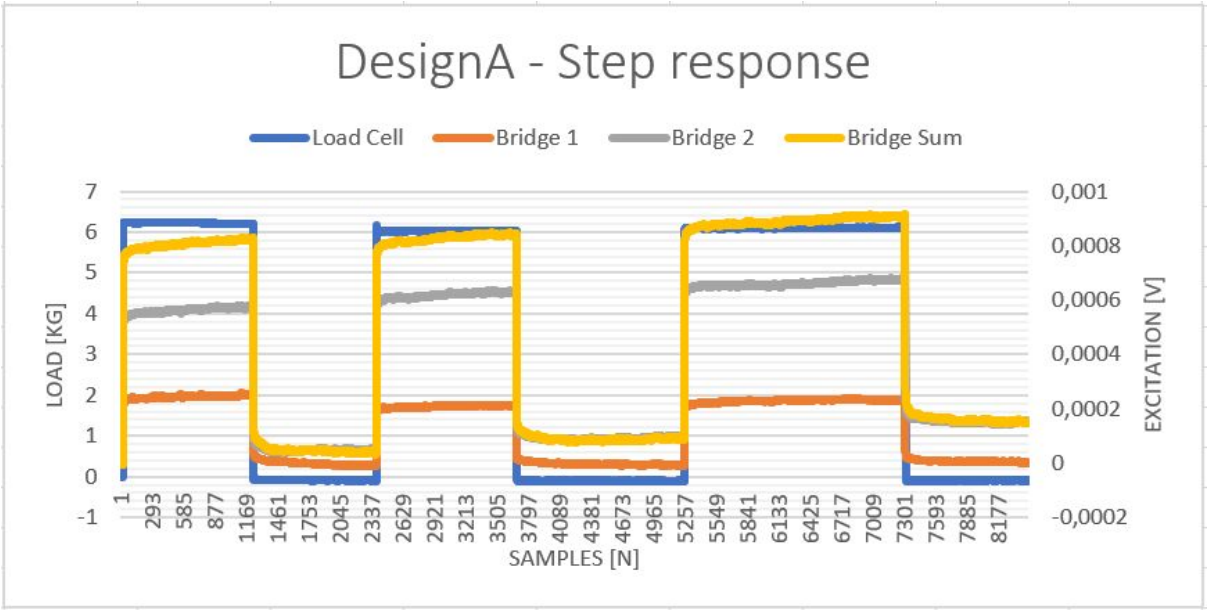


Figure 24, Step response measurement design A with a sample time of 1/3Hz

As can be seen in figure 24, there seems to be a slight linear increase of the excitation of the load cells during the experiment. A possible explanation for this is that the temperature has an influence on the offset of the load cell. Therefore the lab temperature was compensated for using the value found in the temperature dependence test. The compensated results can be found in figure 25.

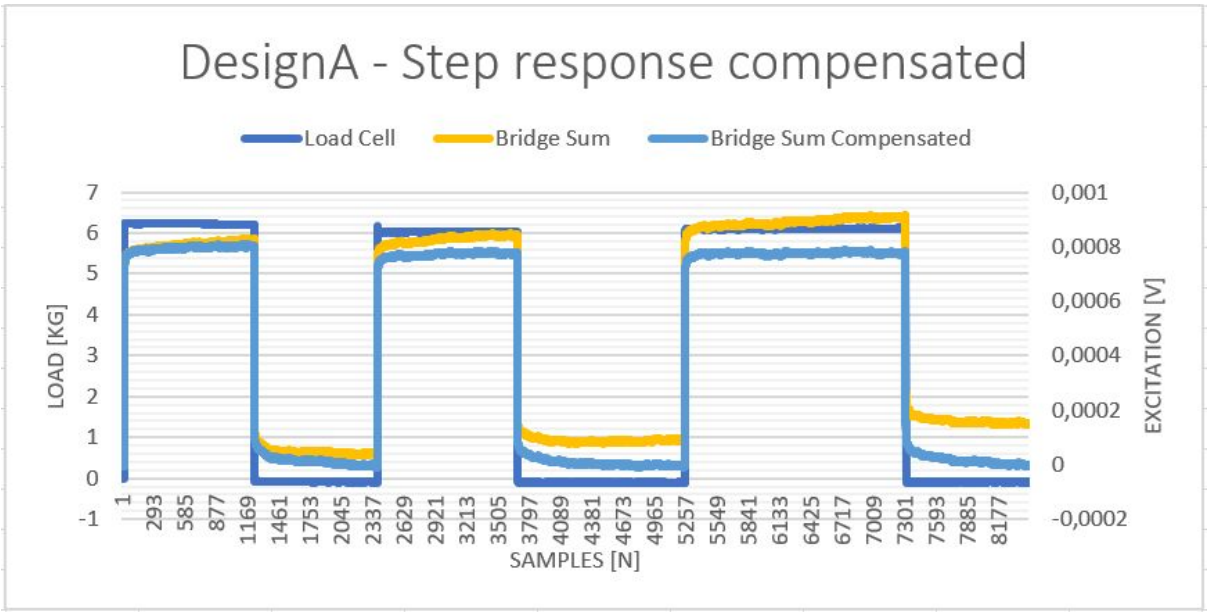


Figure 25, Compensated step response measurement design A with a sample time of 1/3Hz

As can be seen in figure 25, the response of the chip now goes back to the same value at the third loading as the first loading of the chip. Now that the temperature is no longer of much influence in the measurements, the sensitivity can be determined. This was done by plotting the excitation voltage vs the load applied. The results can be found in figure 26.

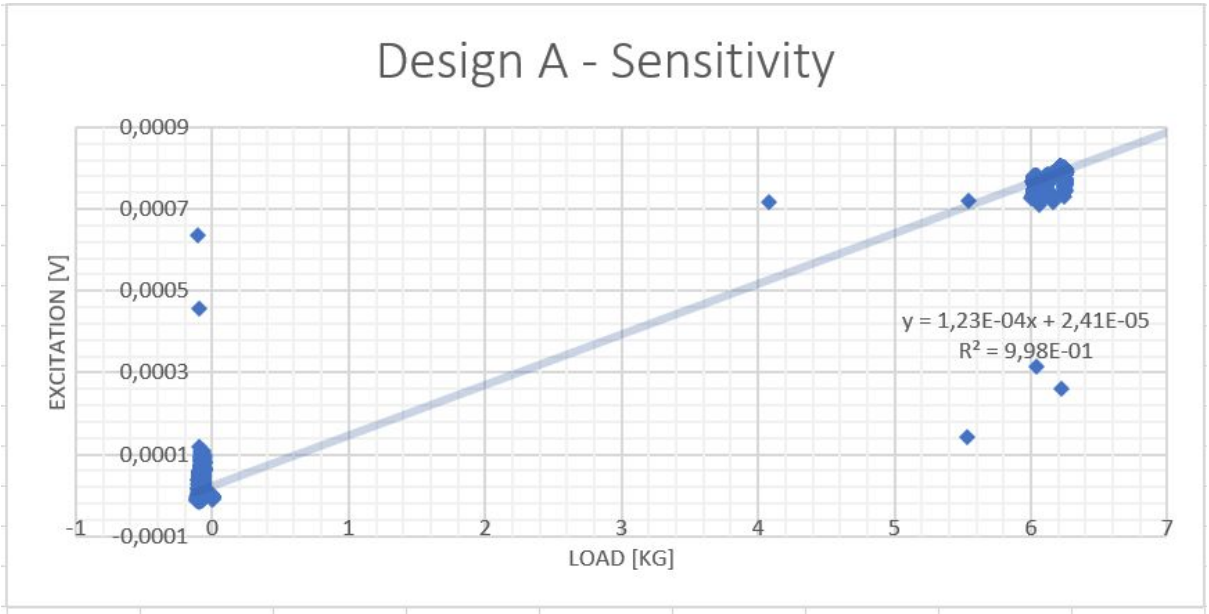


Figure 26, Sensitivity of design A

Using figure 26, and assuming that the output of the chip is linear, a linear fit with a R square value of .99 was used to determine the sensitivity of the chip and gave a value of about

$$\frac{Bridge\,[V]}{Load\,Cell\,[kg]} \approx 1.2 \cdot 10^{-4}\,\frac{[V]}{[kg]}$$

Some seemingly random points can also be seen in figure 26. These are most likely caused due to the asynchronous measurement of test setup 1.

Furthermore the creep of the chip can be determined. For this the results of the third loading, samples 5263 up to 5863, of figure 25 have been used to generate figure 27.

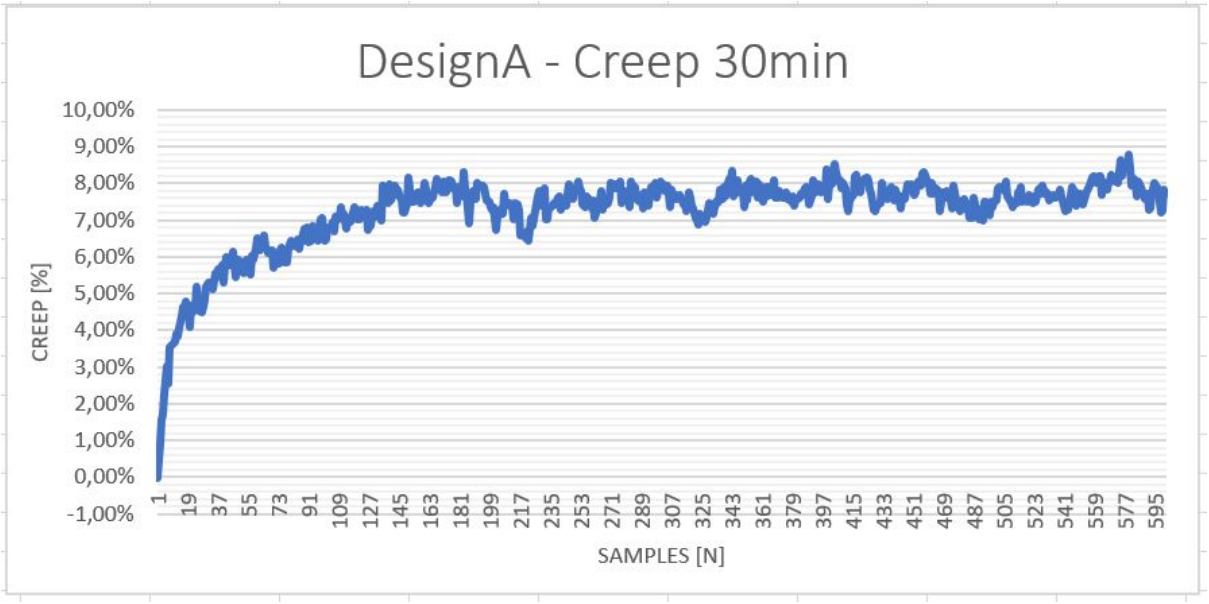


Figure 27, Creep results of design A with a sample time of 1/3Hz

As can be seen in figure 27, the chip creeps about eight percent of its original value in a time span of around ten minutes.

The capability of sensing a moment, or any difference in load between the four sectors, was not tested. This was due to the test setup not allowing for a precise way to adjust, and more importantly measure, the angle of the pushing block in the test setup.

4.2.2.3.2. Design B

Test setup 2 was used once more to measure design B. The chip was connected the same way as in the temperature measurement. This time only one loading and unloading cycle, using a weights as load, was performed due to time constraints. The results can be found in figure 28.

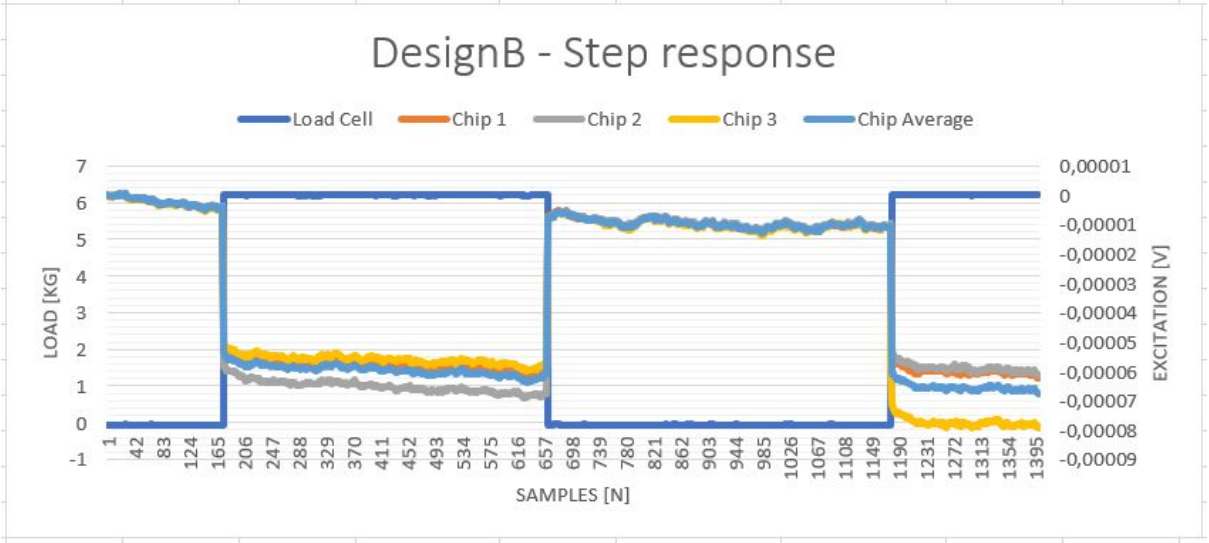


Figure 28, Step response measurement design B with a sample time of 2/9Hz

In figure 28 the outputs of the chips are plotted for about one hour. During which a load was applied and removed. The average output of the chips is also plotted such that design A and B can be compared. Furthermore the second time the load was applied it was placed on a different place on the setup, explaining the difference in excitation voltages during second loading. As expected the output of the chips is changing when a load is applied. What is interesting to see however is that the output of the chips in now seems to have negative dependence with increasing load compared to a positive dependence as with design A. Moreover there seems to be a slight slope during the measurements. Most likely again caused by the temperature dependence of the chip and the changing lab temperature. Therefore temperature compensated results also have been plotted and can be seen in figure 29.

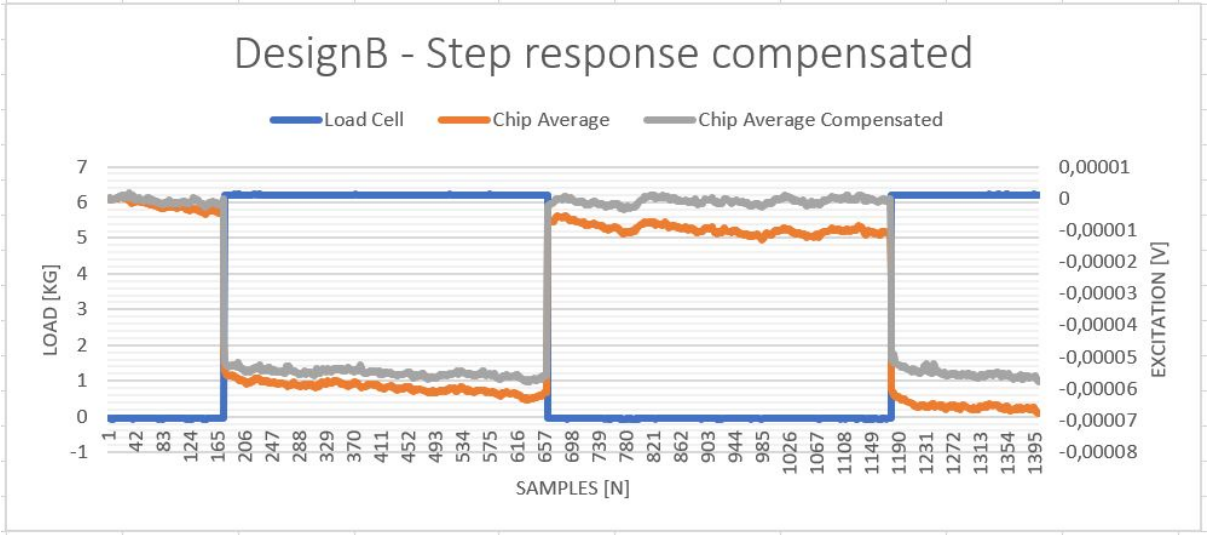


Figure 29, Compensated step response measurement design B with a sample time of 2/9Hz

In figure 29,it can be seen that the temperature dependent effect can be easily compensated for in order to get consistent results. Now that the temperature is of little influence on the excitation output, the creep and sensitivity of design A can be calculated. For the sensitivity an XY plot was made of the average chip excitation, see figure 30 for the results.

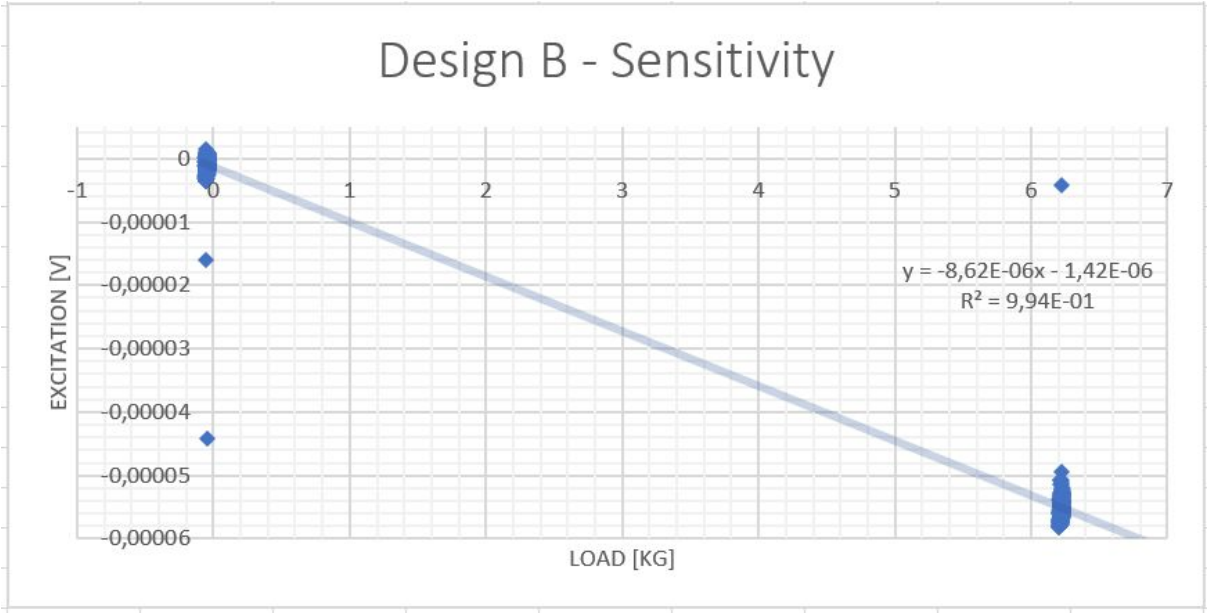


Figure 30, Sensitivity of design B

As can be seen in figure 33, again under the assumption that this design also behaves linear, a linear fit was used in order to determine the chip its sensitivity. Multiplying this value by three gives a single chip its sensitivity which was

$$\frac{Bridge\,[V]}{Load\,Cell\,[kg]} \approx -2.6 \cdot 10^{-5}\,\frac{[V]}{[kg]}$$

This is about a factor 20 lower than that of design A and also flipped direction. A possible explanation for this could be that the resistance of the compensating element decreases more than that of the sensitive element with increasing load. This could be due to the compensating element its relative large size in comparison with the sensitive element and

the compensating element not being entirely floating and and thus also being sensitive to load. If this effect is great enough, it could explain the flip in direction of the excitation voltage.

Finally the creep between points 1179 and 1379 of figure 32 was plotted in figure 34.

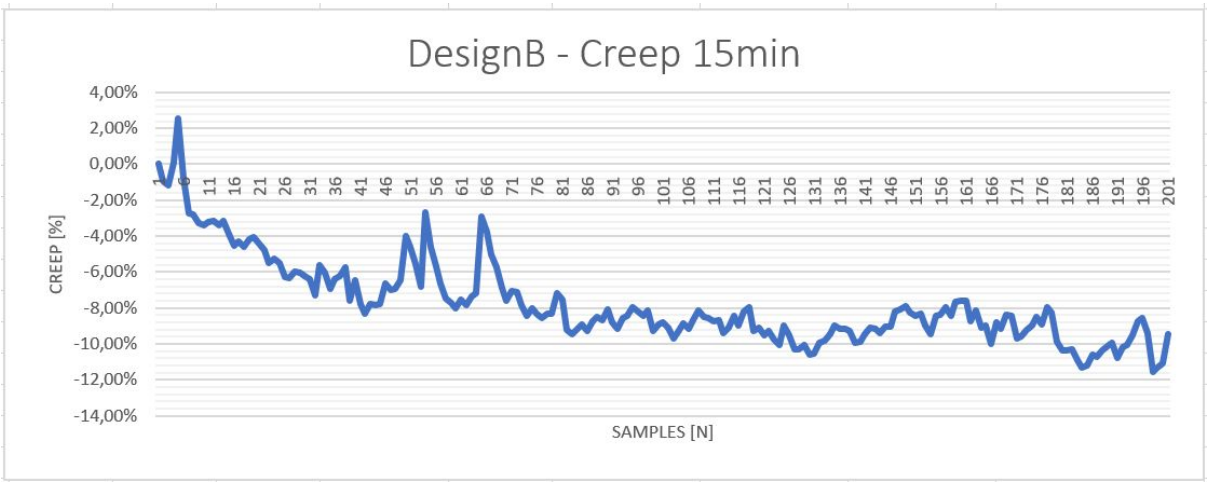


Figure 31, Creep results of design B with a sample time of 2/9Hz

As can be seen in figure 31, this design also suffers from about the same amount of creep as design A and also seems to have the same time coefficient. The creep of both design A and B is likely caused by the mounting method of the pushing block using epoxy glue. Since epoxy glue is a material with relatively high creep compared to silicon.

4.2.2.4. Linear Response

Setup 1 was used in order to confirm that the response of the chip is indeed linear. The linear response of design A was measured. A container was attached to setup 1 via the load attachment point of the setup and slowly filled with water. Firstly using the same chip as was used in the step response and secondly a chip where the pushing block was not attached to the chip using epoxy glue.

4.2.2.4.1. Design A - Glued pushing block

For the first experiment the fully assembled load cell of design A was placed underneath the arm and, using a spring, the arm was adjusted such that no load was applied on the chip. After which a water container was attached to the setup. During the experiment the container was filled with water until a load around 100 Newton was reached. After which the container was emptied and reattached to the load attachment point of setup 1. The setup measured using the same circuit as was used in the temperature dependency measurement. The results of this experiment are in figure 32.

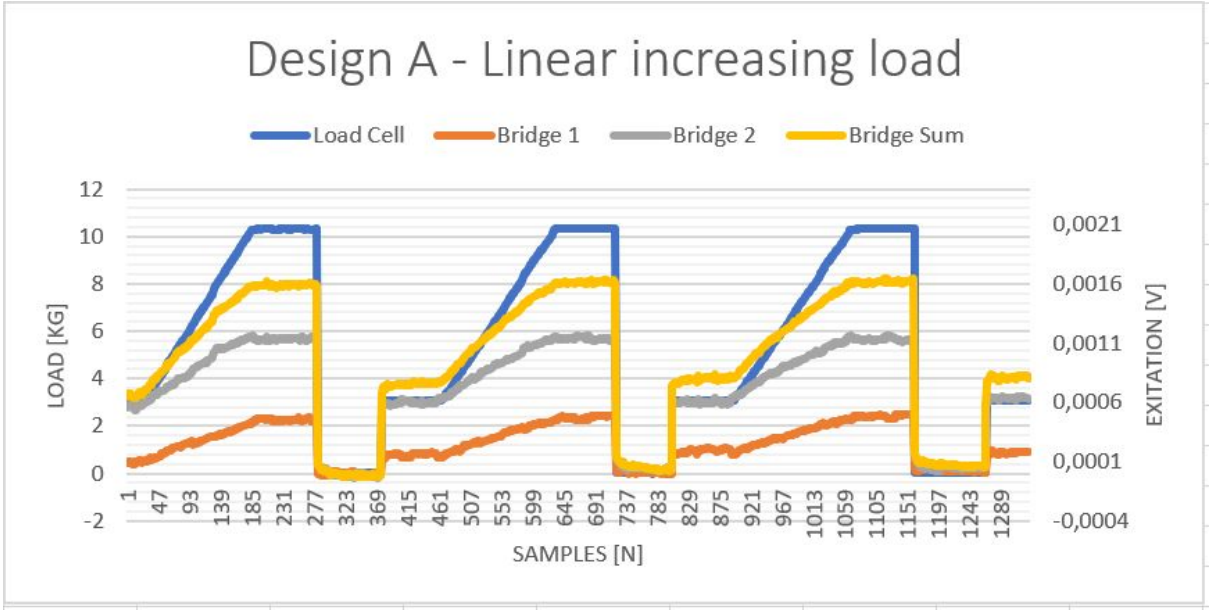


Figure 32, Linear response measurement of design A with a sample rate of 1/3Hz

As can be seen in figure 32, the load cell indeed seems to linearly increase with load. To confirm this the sum of both bridges was plotted against the load in figure 33

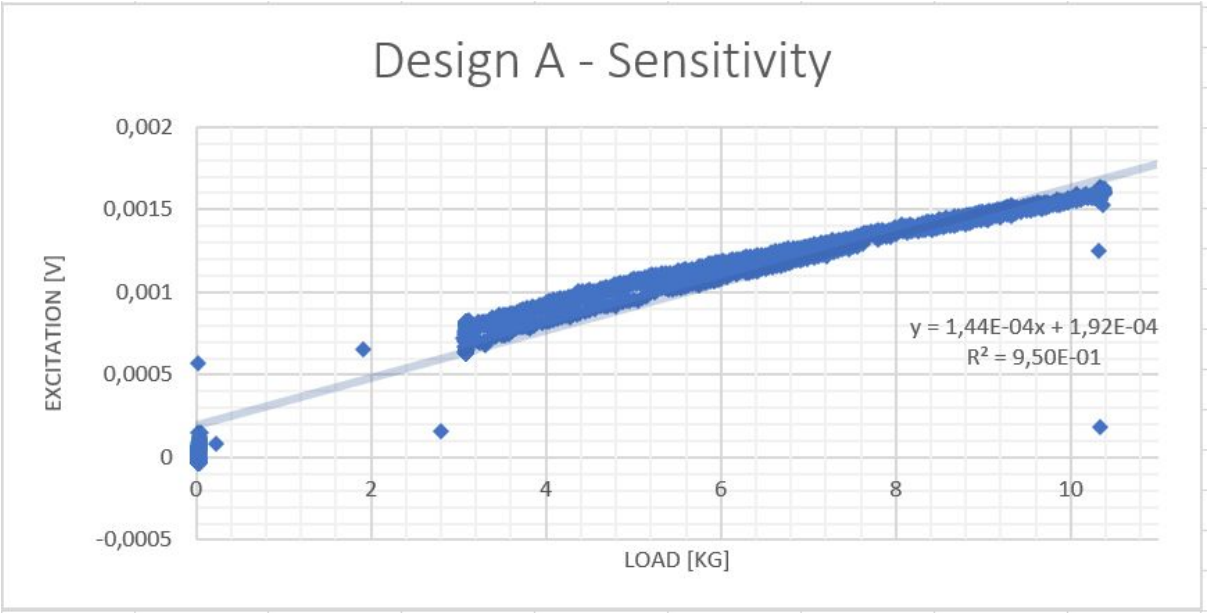


Figure 33, Sensitivity plot of design A of a linear loading

As can be seen in figure 33, seems to be a convincing linear response with a R square value of 0.95 and a load cell sensitivity of

$$\frac{Bridge\,[V]}{Load\ Cell\,[kg]} \approx 1.4 \cdot 10^{-4}\,\frac{[V]}{[kg]}$$

This is a slightly higher value than that was measured during the step response. This could be caused by spring that was used to compensate for the weight of the arm at the beginning of the experiment, which was not done during the step response measurements. However it could also be due to changing temperatures in the lab, but this cannot be confirmed due to missing temperature data. Moreover there are again some random points in the figure likely due to the asynchronous measurement of the chip.

4.2.2.4.2. Design A - Loose pushing block

In order to properly characterise design A, load cell where the pushing block was not attached to the chip itself was used (skipping step 6 of preparation load cell in the attachment). The glass pushing block, normally attached to the chip, was attached to the pushing block of test setup 1 instead and the same experiment was performed. The results are in figure 34.

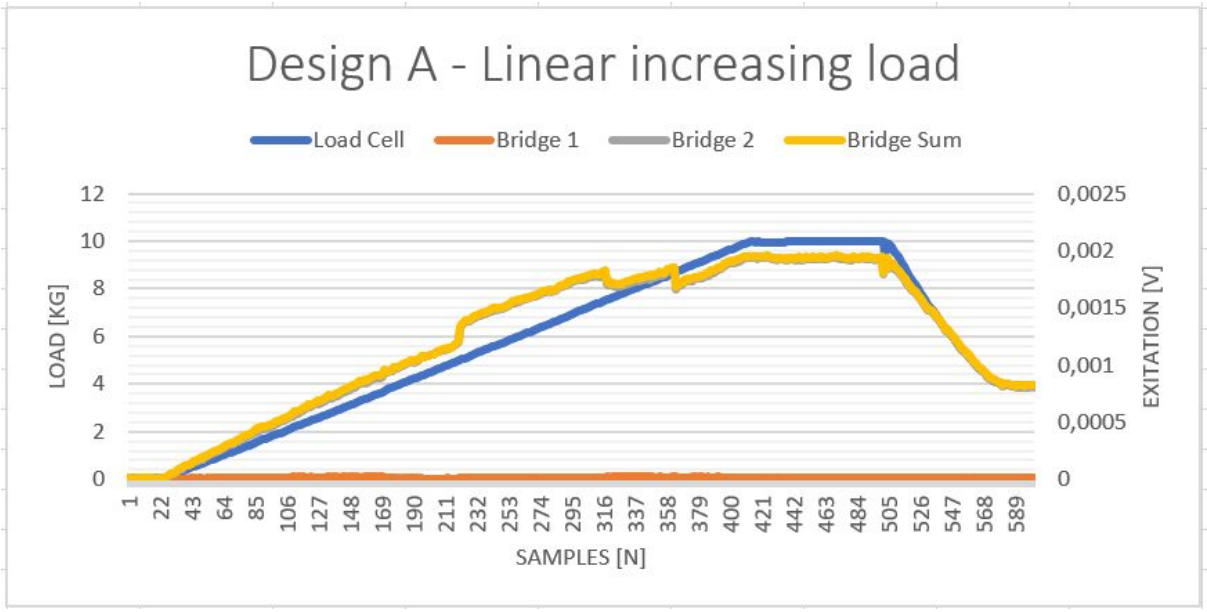


Figure 34, Linear response measurement of design A with a loose pushing block the sample rate is 1/3Hz

As can be seen from figure 34, one of the bridges gives a linear response with an increase in load. However the second bridge does not seem to give a response outside of the noise that was present during the measurements. Furthermore there are some jumps in the measurement. Inspection of the chip underneath the microscope and inspection of the pushing block explain these jumps and gives an explanation for the unresponsiveness of bridge 2 due to the fact that all the load was applied on bridge 1, fracturing the load cell and pushing block due to this asymmetric load (see figure 15 and 16).

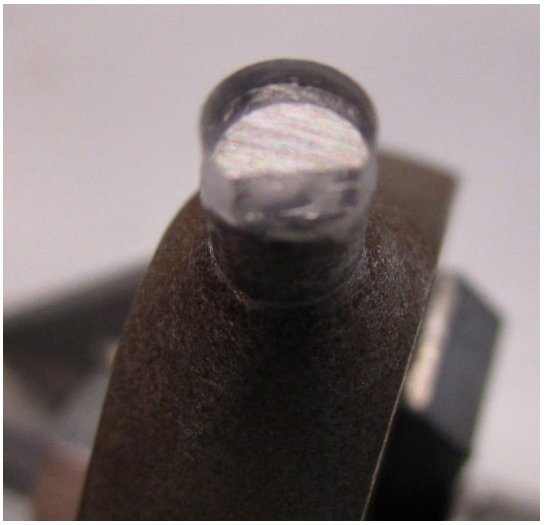


Figure 36, The glass pushing block after asymmetric loading

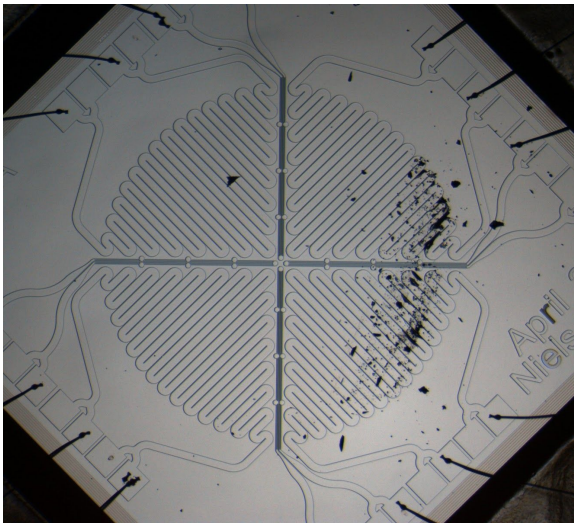


Figure 37, Design A after an asymmetric loading

It seems that both the chip and the pushing block were irreversibly damaged due to the asymmetric load on the chip. In order to still be able to use the results, seen in figure 34, it is assumed that the chip was undamaged when a load of less than five kg was applied due to the lack of sudden jumps in this region. A plot was made from samples 0 to 210 of figure 34 with the excitation voltage of the sum of both bridges against the load on the x axis (see figure 17)

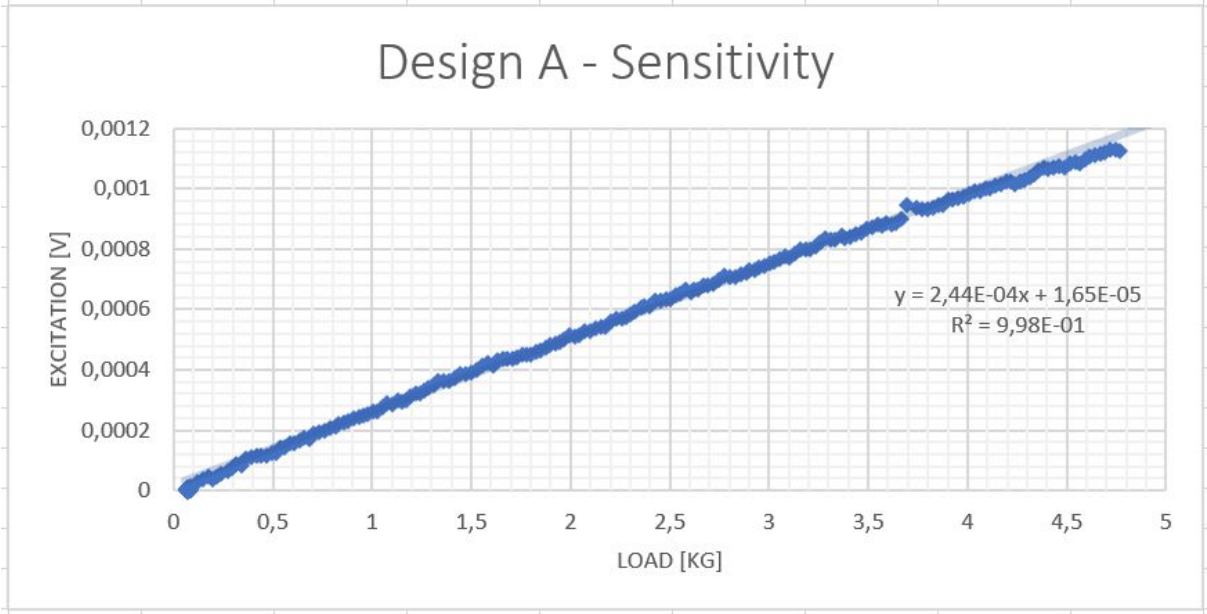


Figure 38, Sensitivity plot of design A with a loose pushing block during linear loading

In figure 38 it can be seen that the part of the load cell gave a convincing linear response, with a R squared value of .99 confirming a close fit, of

$$\frac{Bridge\,[V]}{Load\,Cell\,[kg]} \approx 2.4 \cdot 10^{-4}\,\frac{[V]}{[kg]}$$

The sensitivity of the chip with a loose pushing block on top of it is about a factor 2 higher than that of a chip with a epoxy glued pushing block on top. This is most likely due to the epoxy glue being in between of the elements of the fully assembled chip, the chip with an epoxy glued pushing block on top of it, and therefore absorbing some of the load. This also means that the fully assembled chip likely can handle more load than earlier calculated value in table 4.

It was not possible to compare the difference in creep between chips not having a glued pushing block versus chips that have loose pushing blocks due to the data in figure 34 being the only usable data and the chip being destroyed during the measurement.

4.2.2.5. Load position determination

Test setup 2 allows for multiple chips to be attached to the setup at once. This means that it should be possible to determine where a load is placed on the setup, by using trigonometry on the data that is collected during the measurements. Design B was again connected to the same way as in the temperature dependence measurement and a load of about 60N was applied on different locations on test setup 2 (red circles in figure 39) and the output was measured accordingly.

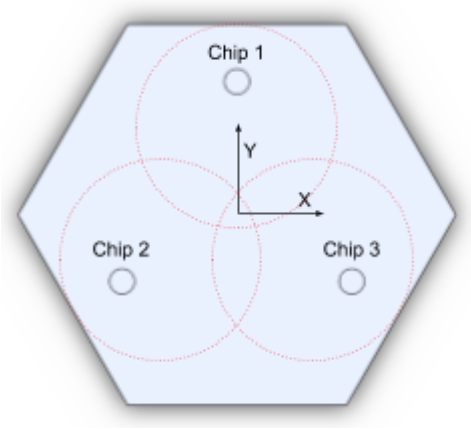


Figure 39, Load placement on test setup 2

At the beginning of the experiment, the test setup was measured without load after which the load was put in the center of the circle above chip 1, then above chip 2, then above chip 3, and finally the load was removed from the test setup. See figure 40 for the temperature compensated results of the experiment. Furthermore attachment extra experiment data has a more extensive version of this experiment.

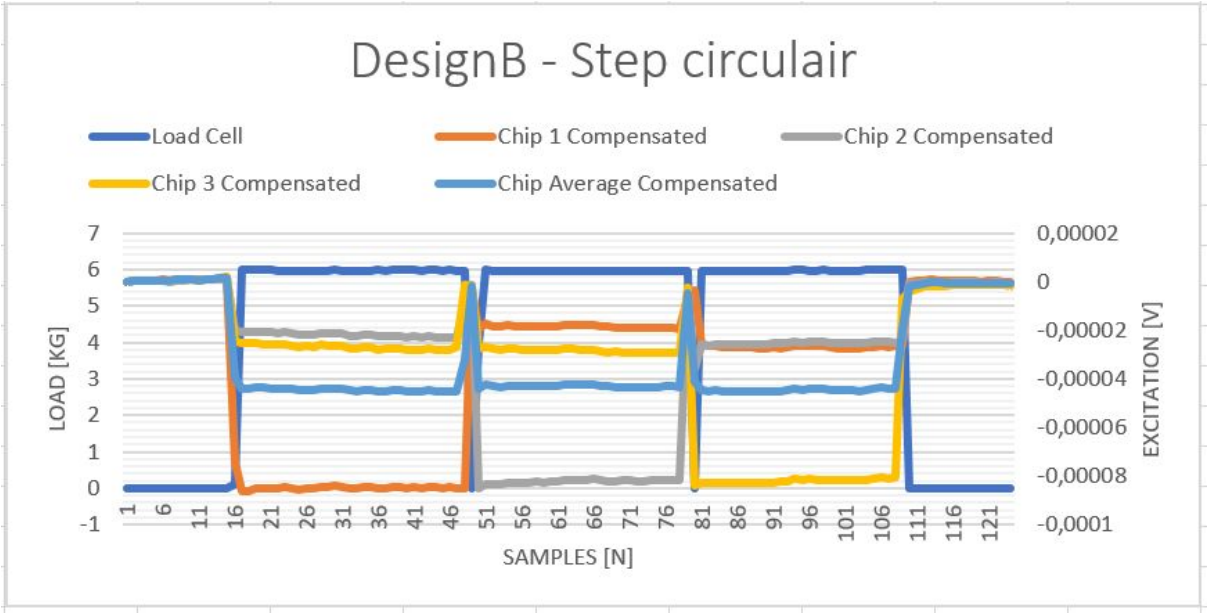


Figure 40, Output of each of the three chips during the position determination experiment

Using the data in figure 40, the x and y components of the load can be determined by using the following formulas

$$position\ load\ [kg] = chip\ position\ data\ [V]\ /\ chip\ sensitivity\ [\tfrac{V}{kg}] \times number\ of\ chips\ [-]$$

$$x_{pos} = \frac{\sqrt{3}}{2} \cdot (V_{chip3} - V_{chip2}) / -2.6 \cdot 10^{-5} \times 3$$

$$y_{pos} = V_{chip1} - \frac{V_{chip2} + V_{chip3}}{2} / -2.6 \cdot 10^{-5} \times 3$$

Applying these formulas on the data in figure 40 gave the position results that can be seen in figure 41.

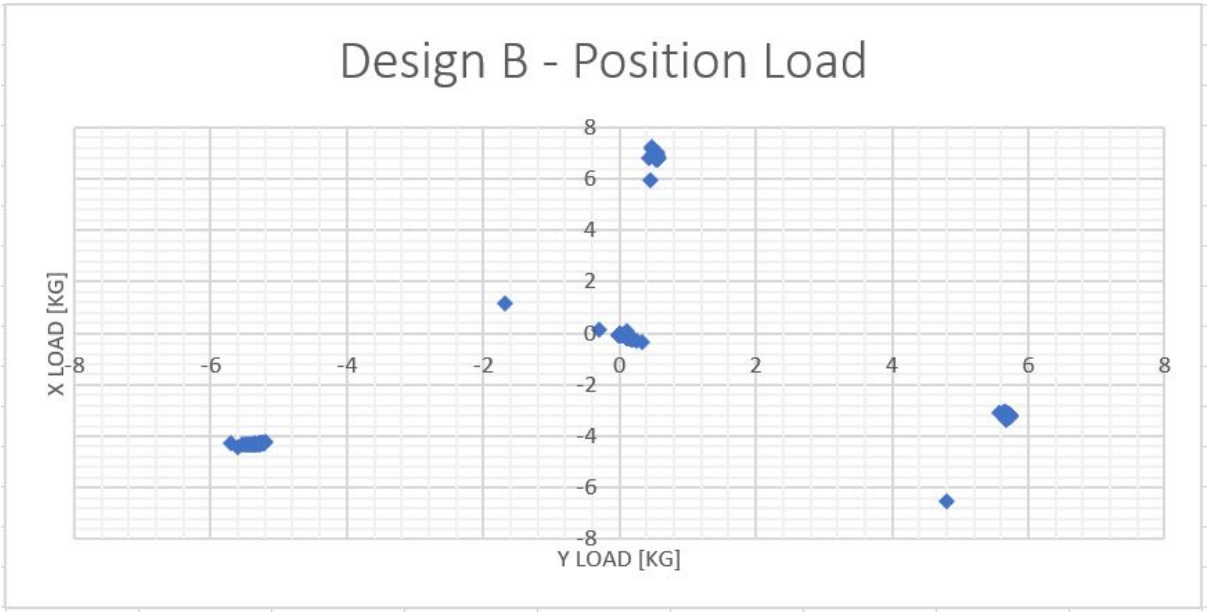


Figure 41, xy components of the load placed on the test setup

As can be seen in figure 41, the position of the center of gravity of the load can be determined using all three chips in the test setup. If one would also like to know what the total value of the load is, a third axis could be added that has the total value of the load. This could be done using the following formula for that axis

$$load\ [kg]\ = \sum chip\ excitation\ [V]\ /\ chip\ sensitivity\ [\tfrac{V}{kg}] \times number\ of\ chips\ [-]$$

Except for four distinct points, three where the load was placed and one zero load point, some random points appear to be present in the plot. Most likely due to the asynchronous measurement of all three chips. Furthermore the of figure 41 shows that the load seems to be not exactly placed in the center of the three red circles of figure 39. This can be due to the load physically not being exactly placed in the middle of the circles due to human error or there could be some slight differences between the sensitivity of each of the load cells, causing an offset.

4.2.3. Comparison chip designs

To conclude the experiments table 10 was constructed. Here the most important experimental results (the capacity, sensitivity, temperature dependence, and creep) of the three designs are put next to each other together with the results of Zwijze en Wensink.

	Design A	Design B	Design C	Zwijze[6]	Wensink
Capacity	34 kg	15 kg	22 kg	1000 kg	1000 kg
Sensitivity	1.2E-5 1/N (2.4E-5 1/N)[7]	-2.7E-6 1/N	(6.4E-4 1/N)[8]	3.3E-6 1/N	5.7E-6 1/N
Temperature dependence	2E-4 V/°C	4E-5 V/°C	N/A	-2380 ppm/°C	N/A
Creep	8 %	8 %	N/A	0.16%	N/A

Table 10, comparison between chip designs N/A means that there is no (quantitative) data available

Table 10 shows the results of all the experiments with some units converted in order to be able to compare them to the results of Zwijze and Wensink. Note that the sample size is very low mostly only consisting out of one chip due to time constraints, so experimental results should be interpreted with caution. What can be seen that the measured sensitivity of each of the designs close to those of Zwijze and Wensink. Which is interesting since the capacity of the designs is much lower than that of Zwijze and Wensink so one would expect a higher sensitivity for the same load instead of roughly the same value.
The temperature dependence could not be converted to the standard unit of ppm/°C due to the experiments not measuring the resistance of each of the chip its gauges. This makes comparing the experimental data found in this thesis with the data of Zwijze difficult. What can be said however is that the temperature dependence found in the experiments is quite substantial, being an order higher than the sensitivity of the chip, whereas the data of Zwijze show relatively low temperature dependence in comparison.
The creep found is was noticeably higher than that of Zwijze. Most likely due to the different attachment method used in to attach the pressure block on top of both load cells.
Finally the hysteresis of the chips was not examined, although an interesting parameter, due to both a lack of experimental data and the relatively high temperature dependence of the chips, making it hard to differentiate hyseteres from temperature deviations.

[6] Using the SOI monocrystalline load cell of Zwijze as comparison material
[7] Using a chip that had the pushing block not epoxy glued on top
[8] Theoretical sensitivity

5. Evaluation

5.1. Conclusion

Fabrication of silicon load cells with resistive readout from a single SOI wafer can indeed be a viable way to produce linear behaving load cells. However, some changes in the proposed designs are necessary in order to make them less sensitive to temperature and prevent creep. A different test setup with resistance measurement capabilities could improve results acquired. The acquired data currently leaves lot of unknowns e.g. it is impossible to explain what the reason for the flipping of signs in the sensitivity of design A and B is.
Finally it can be concluded that using a silicon load cell in the medical field, for instance in a knee aligning sensor, can indeed be a practical application of this type of load cell, due to its small form factor while still having a relative high load capacity and capabilities of sensing the position of a load, but needs further research in order to make it a better alternative than the load cells currently being used.

5.2. Recommendations

In the field of resistive silicon load sensors, still more research can be done in order to produce silicon load cells with a consistent zero load resistance and (almost) no temperature dependence. In order to improve the load cells a list of suggestions has been made.

The test setups used in this thesis seemed to be lacking some capabilities. In order to create more consistent results, a test setup with the capabilities of changing the applied load on the chip, changing the force distribution on the chip, and can accurately control the temperature needs to be designed. Furthermore it needs to be able to measure the resistance of each gauge, in order to get more insight each of the gauges its behaviour under different loads.

In order to consistently place different chips under a test setup. A specially designed printed circuit board needs to be designed that facilitates both easy placement in a test setup and connecting pads close to the chip to make bond wiring relatively simple.

To tackle the problems with the scale of the temperature dependency of the chips any of the following things could be done. A design could be made where a temperature sensor, for example a pt100, is attached to. Then, using a microcontroller for example, the temperature could be compensated for. Another idea is to make a design with a better balanced sensitive and compensating element pair. However it must be said that this would provide a challenge, since neither of the chips of this thesis and Zwijze could achieve this. Finally a design with two identical elements, using a second wafer to relieve one of the elements of the load, could also be made. An advantage of this final method is that the capacity of the load cells could be doubled when a less aggressive etching method is used.

In order to get a consistent resistance in the chip itself between elements, a spiral like design would be a good choice. This design gave the most consistent resistance values between gauges on a single chip on both wafers. However this causes less sensitive chips due to the crystal not being always in the correct orientation for maximal piezoresistive effect.

A better attachment method than using epoxy glue must be found in order to solve the problem of creep. Some substance without a lot of creep of its own that can seep in between the gauges of the chip or something that cannot seep in between of the elements of the chip at all. Another possible solution could be using Pyrex glass and then bonding this to the chip using anodic bonding. However this will induce stress in the chip and change its performance.

Finally boron doped monocrystalline silicon seems like an appropriate material for fabricating these kind of load cells. Theoretically providing the highest piezoresistive coefficient of all possible types of silicon and dopings (mono/poly silicon n/p doping). The only negative point being the relatively high temperature dependence of the material. Furthermore a boron doping is easily achieved using a boron diffusion process, making the base material also relatively cheap.

6. Acknowledgements

I wish to tank various people for their contribution to this project. Special thanks to Professor Wiegerink for giving me the opportunity to do this and his constructive suggestions during this project. Ing. Sanders for his assistance in choosing the instruments needed for the test setups. Finally, I also would like to thank the PHDers of the IDS group for their much needed help in bond wiring the chips.

7. References

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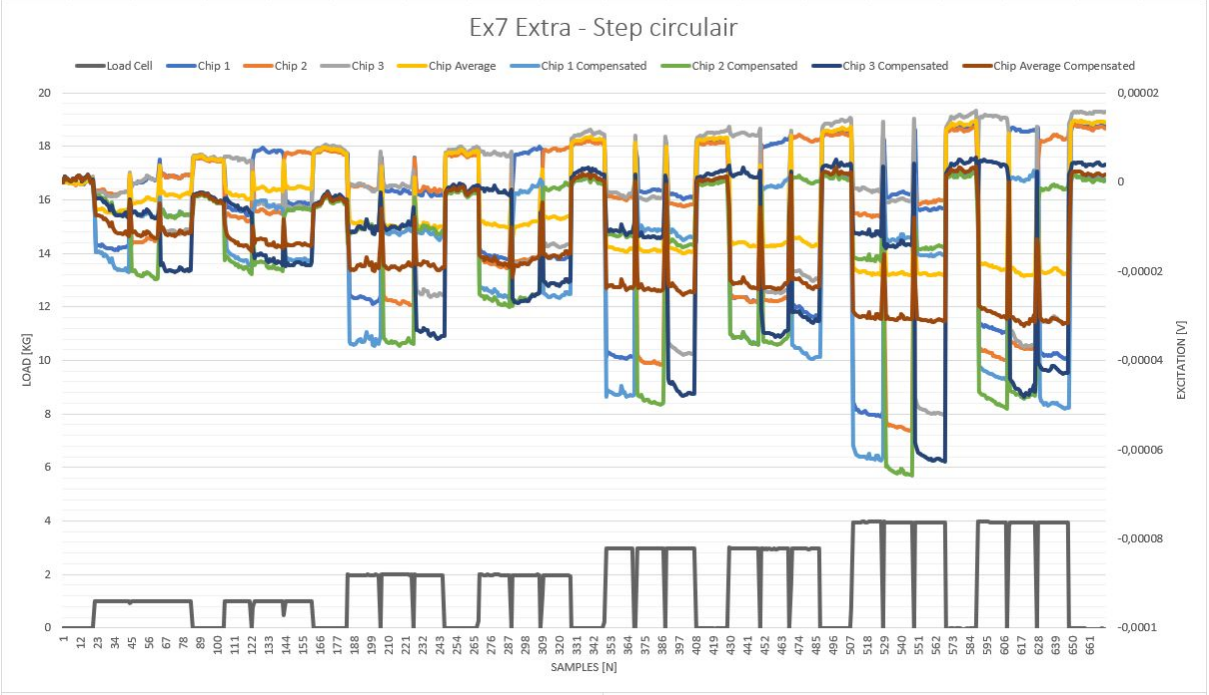
8. Appendices

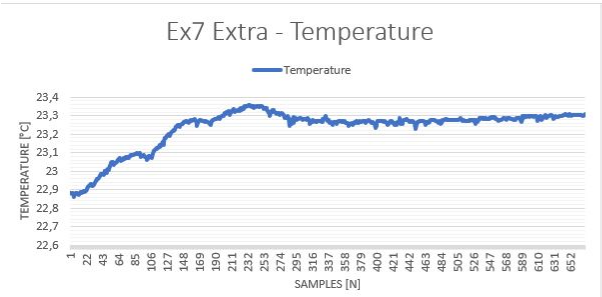
8.1. Abbreviations

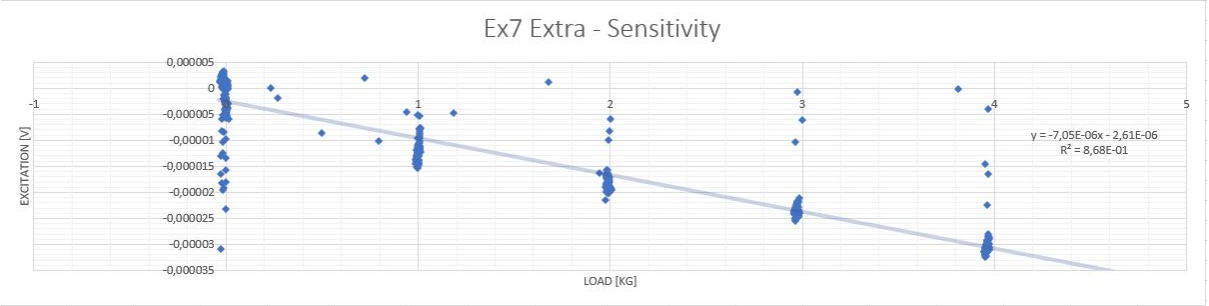
R_0	Zero load resistance of a single element / gauge
ρ_0	Zero load resistivity of a material
l	Gauge length
w	Gauge width
t	Gauge thickness/height
$\Delta \sim$	Difference in $\sim$ its value
v	Poisson's ratio
ε	Strain ($= \frac{\Delta l}{l}$)
GF	Gauge Factor ($= \frac{\Delta R/R_0}{\varepsilon}$) sensitivity of a gauge to a certain strain
σ_{xx}, σ_{yy}	In plane stresses
σ_{zz}	Normal stress
$\varepsilon_{xx}, \varepsilon_{yy}$	In plane strains
ε_{zz}	Normal strain
τ_{xy}, τ_{xz}	Shear stresses in the x plane
τ_{yx}, τ_{yz}	Shear stresses in the y plane
τ_{zx}, τ_{zy}	Shear stresses in the z plane
G_l	Longitudinal piezoresistive strain coefficient
G_t	Transverse piezoresistive strain coefficient
p_l	Longitudinal piezoresistive stress coefficient
p_t	Transverse piezoresistive stress coefficient
V_{in}	Input voltage of a Wheatstone bridge
V_{out}	Output voltage of a Wheatstone bridge

8.2. Attachment - Extra Experiment Data

The same experiment was run as in the position determination experiment, but now the load is also placed between circles 1-2, 2-3, and 3-1. First with 1 then 2 then 3 and finally 4kg. This data not further referred to in the report due to not being able to remove the temperature dependency from the measurement data due to the lag in the temperature measurement of the test setup.







Output data of the load cell and the chips | Temperature data | position data | Excitation voltage vs load cell output with a linear trendline through the points

8.3. Attachment - SOI wafer data

Device Layer:

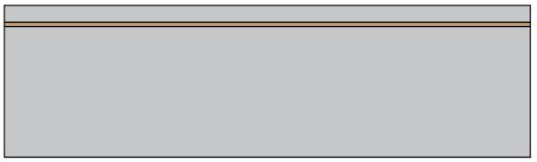
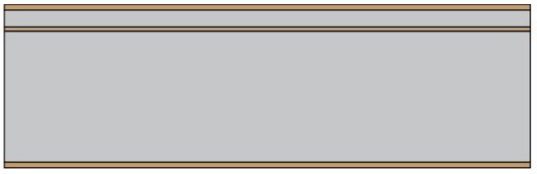
Diameter:	100+/-.2mm
Type/Dopant:	(Mono)P/Boron
Orientation:	<100>+/-.5 deg
Thickness:	25+/-1um
Resistivity:	<.005 Ohmcm
Particles:	<20@.3um
Flats:	Semi Std
Edge exclusion:	5mm
Finish:	Polished

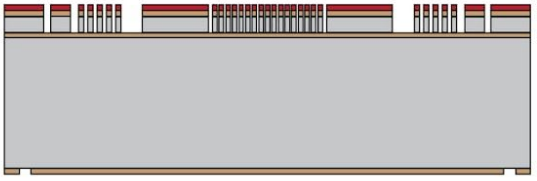
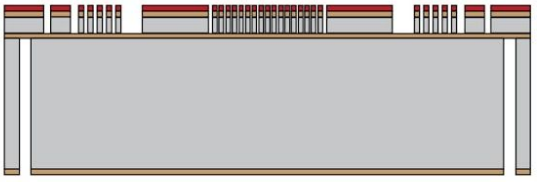
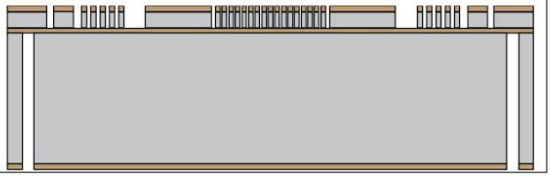
Buried Thermal Oxide:	
Thickness:	2um+/-5%

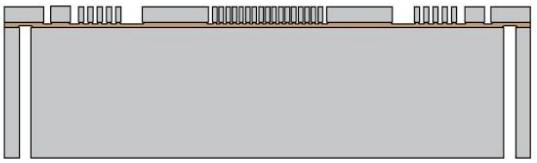
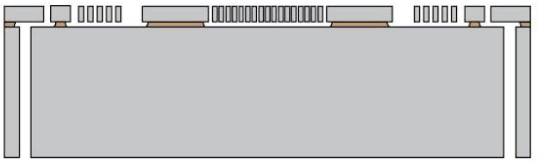
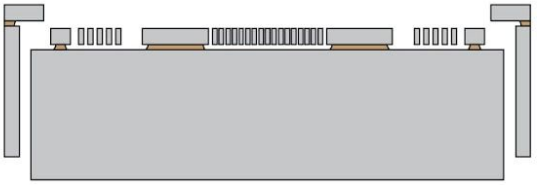
Handle Wafers:

Type/Dopant	(Mono)P/Boron
Orientation	<100>+/-.5 deg
Resistivity:	<.005 Ohmcm
Thickness:	400+/-15um
Finish:	Polished

8.4. Attachment - SOI Wafer Process

• Substrate selection • SOI 25-2-400 • Orientation: h100i • Device layer: 25 um, P++ • Handle layer: 400 um, P+	
• Wafer cleaning • Wet Thermal Oxidation, 2 um • Temperature, 1150 ◦ C • Time: 12:00 h • Measurement of oxide layer thickness	
• Coating handle layer with photoresist, Olin 907-17 • Exposure, mask: HANDLE	
• Etching of silicon dioxide in Adixen DE • depth: 2µm • time: ≈ 5 min	
• Stripping resist, cleaning wafer	

• Coating device layer with photoresist, Olin 907-17 • Exposure, mask: DEVICE	
• Etching of silicon dioxide in Adixen DE • depth: 2µm • time: ≈ 5 min	
• DRIE Etching of silicon in • Adixen SE, top side • Recipe: RB.HARS. • depth: 25 µm • time: ≈ 9 min.	
• DRIE Etching of silicon in Adixen SE, bottom side • Recipe: see section 6.2 • depth: 400µm • time: ≈ 36 min.	
• Stripping resist, cleaning wafer • Fluor carbon removal • O2 plasma cleaning, 800 Watt, 1 hour • Piranha cleaning, 30 min	

• Etching of oxide in 50% HF • Time: ca. 2 min. until oxide at top and bottom side is removed	
• Vapor-HF to release structures and devices • Time: 45 min	
• Release samples by removing surrounding frame • Measurement/Inspection of samples	

8.5. Attachment - Datasheet load cell

Model 1042

Single Point Load Cells

ENHANCED

Features

- Capacities: 1 - 100 kg (2.20 - 220.46 lbs)
- Anodized aluminum construction
- 6 wire (sense) circuit
- Single point 400 x 400 mm platform
- IP66 protection
- NTEP approved 5000 divisions
- OIML approved **6000** divisions

Model 1042 is a low profile, two -beam single point load cell designed for direct mounting of low cost weighing platforms, ideally suited for retail, bench and counting scales.

Available in anodized aluminum, this high-accuracy load cell is approved to NTEP 5000 divisions and other stringent approval standards, including OIML R60 C4 and OIML R60 C3, 30% utilization.

A special humidity - resistant, IP66, protective coating assures long term stability over the entire compensated temperature range. Interchangeable, replacement to industry standard models 1040, 1041, 1140 (stainless).

Tedea-Huntleigh, with models ranging from 1 to 50,000 kg capacities, is the world's largest manufacturer of precision load cells.

The two additional sense wires feed back the excitation voltage reaching the load cell. Complete compensation of changes in lead resistance due to temperature changes and/or cable length changes, is achieved by feeding this voltage into the appropriate electronics.

Also Available from Tedea-Huntleigh
Also in this range, a stainless steel, bolt hole compatible version designated model 1140 and 1142 are available for applications unsuitable for load cells of aluminum construction.

For further details please contact the factory or your local distributor.

TEDEA th. HUNTLEIGH
EXCELLENCE IN LOAD CELLS

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Model 1042

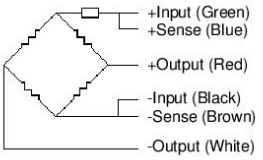
Single Point Load Cells

Parameters	Z	M	E	F	G	G5	G3	I*	I5**	Units
OIML ACCURACY CLASS			**C1**	**C2**	**C3**	**C3 / 50**	**C3 / 30**			
NTEP ACCURACY CLASS/NMAX			**III / 1500**	**III / 2000**	**III / 3000**			**III / 5000**		
Rated Capacity (R.C.)	1, 3, 5, 7, 10, 15, 20, 30, 50, 75, 100									kg
Rated Output (R.O.)	2									mV/V
Rated Output Tolerance	0.2									±mV/V
Zero Balance	0.2									±mV/V
Total Error Per OIML R60	0.075	0.05	0.03	0.02	0.02	0.02	0.02			± % of R.O.
Total Error Per NIST Handbook 44			0.03	0.02	0.02			0.02		± % of R.O.
Creep and Zero Return (30 min.)	0.07	0.07	0.05	0.025	0.017	0.017	0.017	0.033		± % of load
Temperature Effect: On Output	0.07	0.005	0.003	0.0014	0.001	0.001	0.001	0.001		± % of load / °C
Temperature Effect: On Zero	0.025	0.025	0.01	0.006	0.004	0.0023	0.0014	0.0023	0.0014	± % of R.O. / °C
Temperature Range: Safe	-30 to +70									°C
Temperature Range: Compensated	-10 to +40									°C
NTEP V min.					RC/3500			RC/6000	RC/10000	kg
Eccentric Loading Error	0.015	0.015	0.0074	0.0074	0.0049	0.0049	0.0049		0.0049	± % of load / cm
Maximum Recommended Platform Size	40 x 40									cm
Maximum Safe Static Overload (central loading)	150									% of R.C.
Ultimate Static Overload (central loading)	300									% of R.C.
Deflection	< 0.4									mm
Excitation: Recommended	10									Volts AC or DC
Excitation: Maximum	15									Volts AC or DC
Input Impedance	415 ± 15									Ohms
Output Impedance	350 ± 3									Ohms
Insulation Resistance	> 2000									MegaOhms
Weight (nominal)	0.30									kg
Cable Type	6 conductors, 26 AWG, shielded, PVC jacket, 1 meter									
Cable Code	+exc - green, +sig - red, +sen - blue -exc - black, -sig - white, -sen - brown									
Construction	anodized aluminum, except 1 and 3 kg capacities									
Circuit Type	Unbalanced									
Environmental Protection	IP 66									
Approvals	NTEP (5000 divisions) and OIML (4000 divisions)									

NOTES : Balanced span temperature compensation optional. * 85% Utilization standard, other utilization available on request . ** 50% Utilization standard, other utilization available on request

Wiring Schematic Diagram

Unbalanced Bridge Configuration
(Balanced option available)

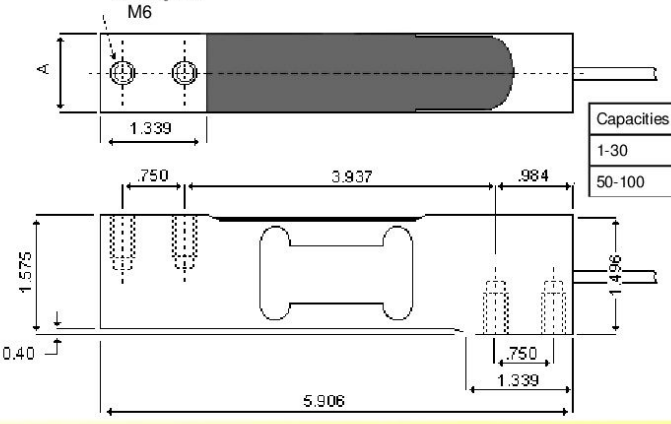


The two "sense" wires sample the bridge supply voltage at the load cell. Complete compensation of charge in the lead wire resistance, due to temperature change and/or cable extension, is achieved by feeding this voltage into appropriate electronics.

Mounting

4 Mounting holes
M6

Outline Dimensions All Capacities (in inches)



Capacities kg	A
1-30	.787
50-100	.992

8.6. Attachment - Datasheet Epoxy

Technical Data Sheet

LOCTITE® M-31CL™

August 2005

PRODUCT DESCRIPTION

LOCTITE® M-31CL™ provides the following product characteristics:

Technology	Epoxy
Chemical Type	Epoxy
Appearance (Resin)	Clear colorless to slightly yellow liquid[LMS]
Appearance (Hardener)	Clear colorless to slightly yellow liquid[LMS]
Appearance (Mixed)	Ultra clear
Components	Two part - Resin & Hardener
Viscosity	Low
Mix Ratio (by weight) Resin : Hardener	100 : 46
Mix Ratio (by volume) Resin : Hardener	2 : 1
Cure	Room temperature cure after mixing
Application	Bonding

LOCTITE® M-31CL™ cures at room temperature once mixed, to form an ultra-clear adhesive bondline with excellent impact resistance and minimal shrinkage. The fully cured epoxy is resistant to a wide range of chemicals and solvents and has excellent dimensional stability over a wide temperature range. Typical applications include bonding, small potting, staking and laminating applications where optical clarity and excellent structural, mechanical and electrical insulating properties are required. LOCTITE® M-31CL™ bonds most materials including glass, optical fibers, ceramics, metals, and many rigid plastics. Suitable for use in the assembly of **disposable medical devices**.

ISO-10993

An ISO 10993 Test Protocol is an integral part of the Quality Program for LOCTITE® M-31CL™. LOCTITE® M-31CL™ has been qualified to Loctite's ISO 10993 Protocol as a means to assist in the selection of products for use in the medical device industry. Certificates of Compliance are available at www.loctite.com or through the Henkel Loctite Quality Department.

TYPICAL PROPERTIES OF UNCURED MATERIAL

Resin:
- Specific Gravity @ 25 °C: 1.1
- Flash Point - See MSDS
- Viscosity, Brookfield - RVT, 25 °C, mPa·s (cP):
  - Spindle 6, speed 20 rpm: 9,000 to 12,000[LMS]

Hardener:
- Specific Gravity @ 25 °C: 1.0
- Flash Point - See MSDS
- Viscosity, Brookfield - RVT, 25 °C, mPa·s (cP):
  - Spindle 5, speed 20 rpm: 1,500 to 9,000[LMS]

Mixed:
- Specific Gravity @ 25 °C: 1.07

TYPICAL CURING PERFORMANCE

Gel Time

Gel time, 100 °C, seconds: 90 to 150[LMS]

Working Life

Working life, minutes: 30

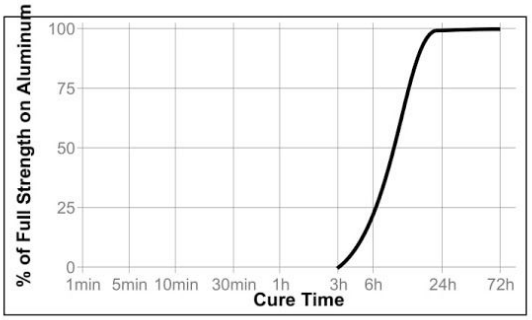
Tack Free Time

Tack Free Time is the time required to achieve a tack free surface.

Tack Free Time, (low humidity), minutes: 160

Cure Speed vs. Time

The graph below shows shear strength developed with time on Aluminum (etched & abraded) lapshears @ 25 °C with an average bondline gap of 0.1 to 0.2 mm and tested according to ISO 4587.



TYPICAL PROPERTIES OF CURED MATERIAL

Cured @ 25 °C except where noted

Physical Properties:

Glass Transition Temperature, ASTM E 228, °C		70
Elongation, ASTM D 638, %		8
Tensile Strength, ASTM D 638	N/mm² (psi)	55.2 (8,000)
Shore Hardness, ISO 868, Durometer D:		
Cured @ 22 °C for 16 to 18 hours followed by 2 hours @ 65 °C		80 to 90[LMS]

Electrical Properties:

Dielectric Breakdown Strength, IEC 60243-1, kV/mm: 19.7

TYPICAL PERFORMANCE OF CURED MATERIAL

Adhesive Properties

Cured @ 65 °C for 2 hours

Lap Shear Strength, ISO 4587:

Aluminum (etched & abraded), 0.13 mm gap	N/mm² (psi)	≥6.9[LMS] (≥1,000)

Cured @ 22 °C for 5 days

Lap Shear Strength, ISO 4587:

Steel (grit blasted)	N/mm² (psi)	21.4 (3,100)

Henkel Technologies

Aluminum (etched & abraded), 0.1 to 0.2 mm gap	N/mm² (psi)	29.4 (4,270)
Aluminum (anodised)	N/mm² (psi)	21.2 (3,070)
Stainless steel	N/mm² (psi)	13.6 (1,970)
Polycarbonate	N/mm² (psi)	13.4 (1,950)
Nylon	N/mm² (psi)	2.4 (350)
Wood (Fir)	N/mm² (psi)	12.1 (1,750)

Block Shear Strength, ISO 13445:

PVC	N/mm² (psi)	7.0 (1,010)
ABS	N/mm² (psi)	8.4 (1,220)
Epoxyglass	N/mm² (psi)	20.6 (2,980)
Acrylic	N/mm² (psi)	1.2 (180)
Glass	N/mm² (psi)	24.4 (3,540)

TYPICAL ENVIRONMENTAL RESISTANCE

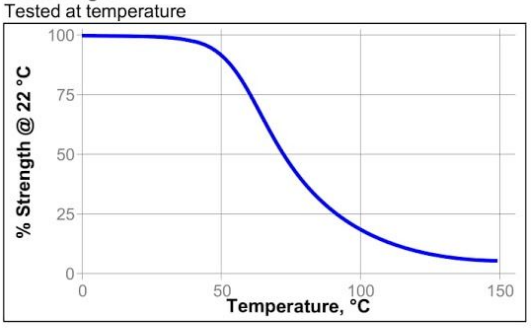
Cured for 12 hours @ 65 °C followed by 4 hours @ 22 °C

Lap Shear Strength, ISO 4587:

Aluminum (etched & abraded), 0.1 to 0.2 mm gap

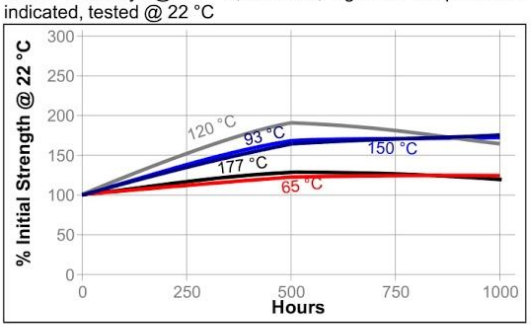
Hot Strength

Tested at temperature



Heat Aging

Cured for 5 days @ 22 °C, on steel, aged at temperatures indicated, tested @ 22 °C



Chemical/Solvent Resistance

Cured for 5 days @ 22 °C, on steel, aged under conditions indicated and tested @ 22°C

		% of initial strength	
Environment	**°C**	**500 h**	**1000 h**
Air	87	155	150
Motor oil (10W-30)	87	160	145
Unleaded gasoline	87	120	110
Water/glycol 50/50	87	145	140
Salt fog	22	70	85
95% RH	38	105	115
Condensing Humidity	49	90	90
Water	22	100	90
Acetone	22	100	105
IPA	22	120	120

Effects of Sterilization

In general, products similiar in composition to LOCTITE® M-31CL™ subjected to standard sterilization methods, such as EtO and Gamma Radiation (25 to 50 kiloGrays cumulative) show excellent bond strength retention. LOCTITE® M-31CL™ maintains bond strength after 1 cycle of steam autoclave. It is recommended that customers test specific parts after subjecting them to the perferred sterilization method. Consult with Loctite® for a product recommendation if your device will see more than 3 sterilization cycles.

GENERAL INFORMATION

This product is not recommended for use in pure oxygen and/or oxygen rich systems and should not be selected as a sealant for chlorine or other strong oxidizing materials.

For safe handling information on this product, consult the Material Safety Data Sheet (MSDS).

Directions for use

1. For high strength structural bonds, remove surface contaminates such as paint, oxide films, oils, dust, mold release agents and all other surface contaminates.
2. Use gloves to minimize skin contact. DO NOT use solvents for cleaning hands.
3. **Dual Cartridges:** To use simply insert the cartridge into the application gun and start the plunger into the cylinders using light pressure on the trigger. Next, remove the cartridge cap and expel a small amount of adhesive to be sure both sides are flowing evenly and freely. If automatic mixing of resin and hardener is desired, attach the mixing nozzle to the end of the cartridge and begin dispensing the adhesive. For hand mixing, expel the desired amount of the adhesive and mix thoroughly. Mix for approximately 15 seconds after uniform color is obtained.
4. For maximum bond strength apply adhesive evenly to both surfaces to be joined.
5. Application to the substrates should be made within 30 minutes. Larger quantities and/or higher temperatures will reduce this working time.
6. Join the adhesive coated surfaces and allow to cure at 25 °C for 24 hours for high strength. Heat up to 93 °C, will speed curing.
7. Keep parts from moving during cure. Contact pressure is neccesary. Maximum shear strength is obtained with a 0.1 to 0.2 mm bond line.

8. Excessive uncured adhesive can be cleaned up with ketone type solvents.

Loctite Material Specification[LMS]
LMS dated February 23, 2000. Test reports for each batch are available for the indicated properties. LMS test reports include selected QC test parameters considered appropriate to specifications for customer use. Additionally, comprehensive controls are in place to assure product quality and consistency. Special customer specification requirements may be coordinated through Henkel Quality.

Storage
Store product in the unopened container in a dry location. Storage information may be indicated on the product container labeling.
Optimal Storage: 8 °C to 21 °C. Storage below 8 °C or greater than 28 °C can adversely affect product properties. Material removed from containers may be contaminated during use. Do not return product to the original container. Henkel Corporation cannot assume responsibility for product which has been contaminated or stored under conditions other than those previously indicated. If additional information is required, please contact your local Technical Service Center or Customer Service Representative.

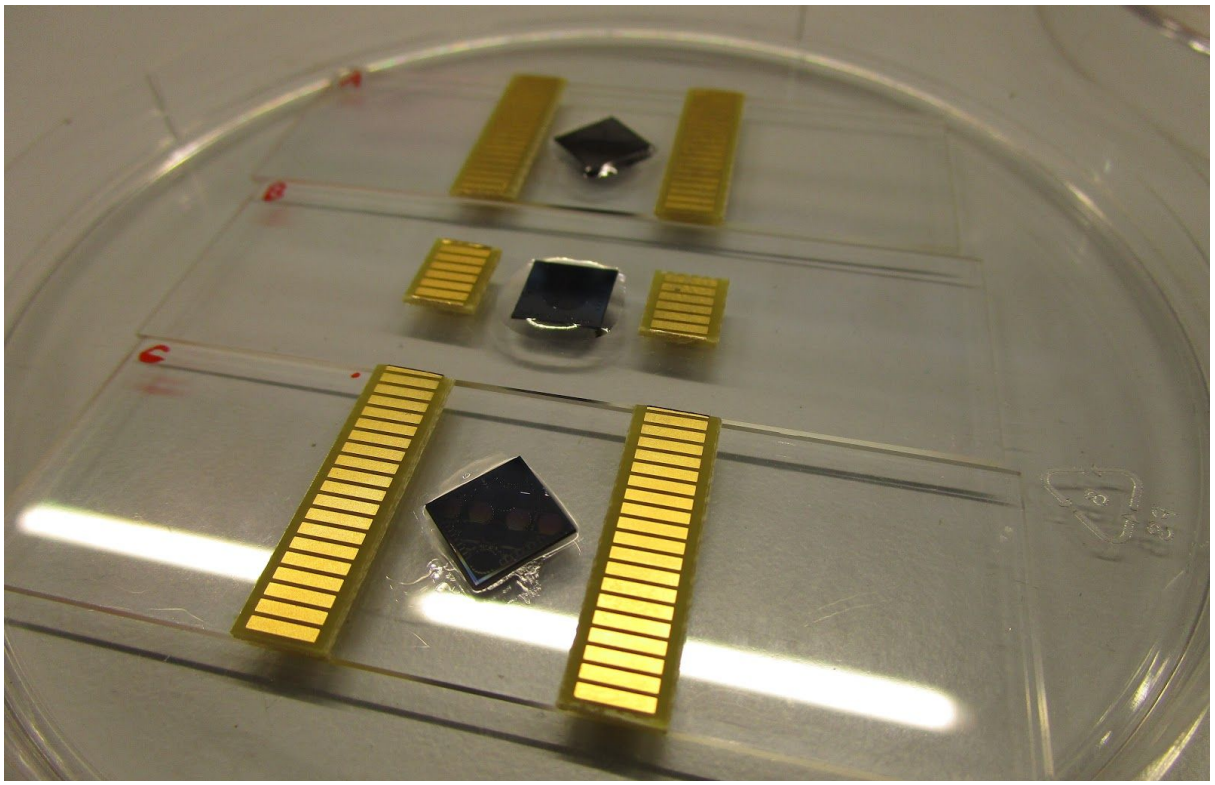
Conversions
(°C x 1.8) + 32 = °F
kV/mm x 25.4 = V/mil
mm / 25.4 = inches
µm / 25.4 = mil
N x 0.225 = lb
N/mm x 5.71 = lb/in
N/mm² x 145 = psi
MPa x 145 = psi
N·m x 8.851 = lb·in
N·m x 0.738 = lb·ft
N·mm x 0.142 = oz·in
mPa·s = cP

Note
The data contained herein are furnished for information only and are believed to be reliable. We cannot assume responsibility for the results obtained by others over whose methods we have no control. It is the user's responsibility to determine suitability for the user's purpose of any production methods mentioned herein and to adopt such precautions as may be advisable for the protection of property and of persons against any hazards that may be involved in the handling and use thereof. In light of the foregoing, **Henkel Corporation specifically disclaims all warranties expressed or implied, including warranties of merchantability or fitness for a particular purpose, arising from sale or use of Henkel Corporation's products. Henkel Corporation specifically disclaims any liability for consequential or incidental damages of any kind, including lost profits.** The discussion herein of various processes or compositions is not to be interpreted as representation that they are free from domination of patents owned by others or as a license under any Henkel Corporation patents that may cover such processes or compositions. We recommend that each prospective user test his proposed application before repetitive use, using this data as a guide. This product may be covered by one or more United States or foreign patents or patent applications.

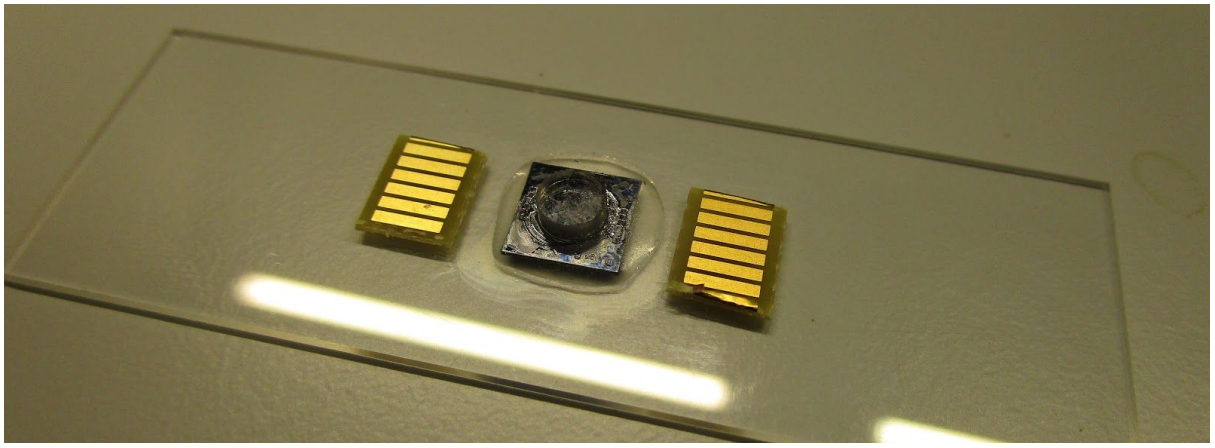
Reference 1.0

8.7. Attachment - Preparation Load Cell

1. Attach 2 gold plated terminals with connection wires 1cm off the middle of a 25x75x1mm glass plate.
2. Attach a load cell in the middle of the glass plate with Loctite Hysol Epoxy with a 45 degree offset in case of design A and C or parallel to the sides of the glass plate in case of design B. (see image below)
3. Leave to cure for at least 24 hours.
4. Wire bond the load cell to the gold plated terminals.
5. Connect the load cell to the setup via the wires.
6. Glue a 2mm glass pillar with the same epoxy in the middle of the chip and leave to cure again for at least 24 hours.

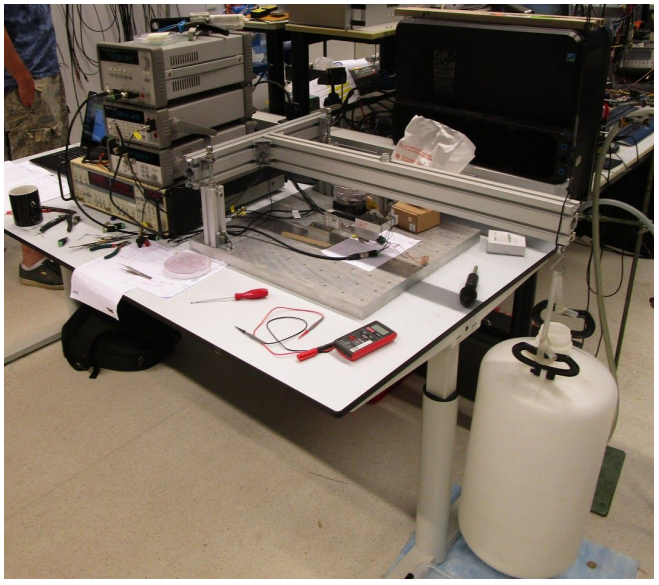


Finished chips without glass pillar

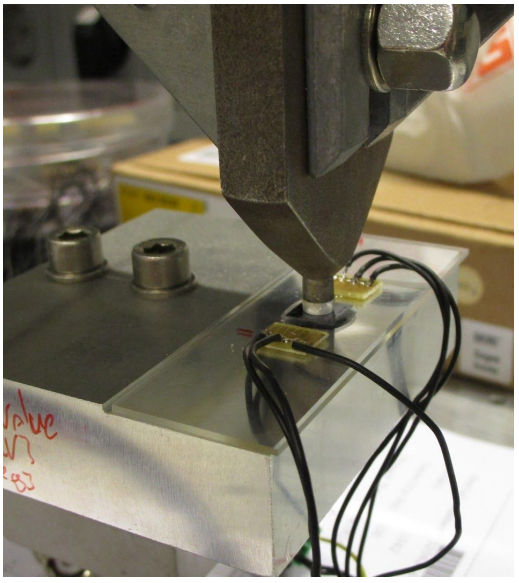


Finished chip with glass pillar

8.8. Attachment - Test setup 1

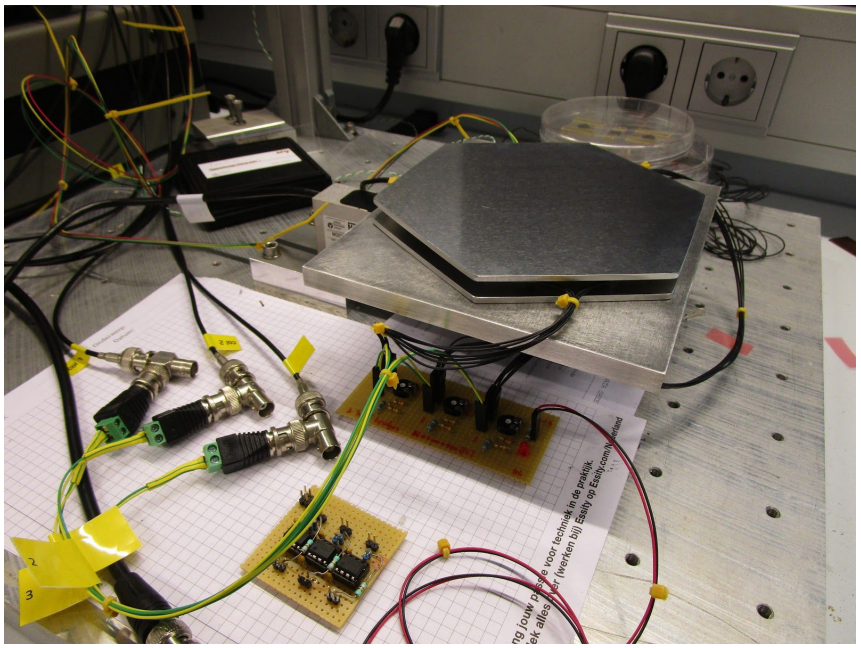


Test setup

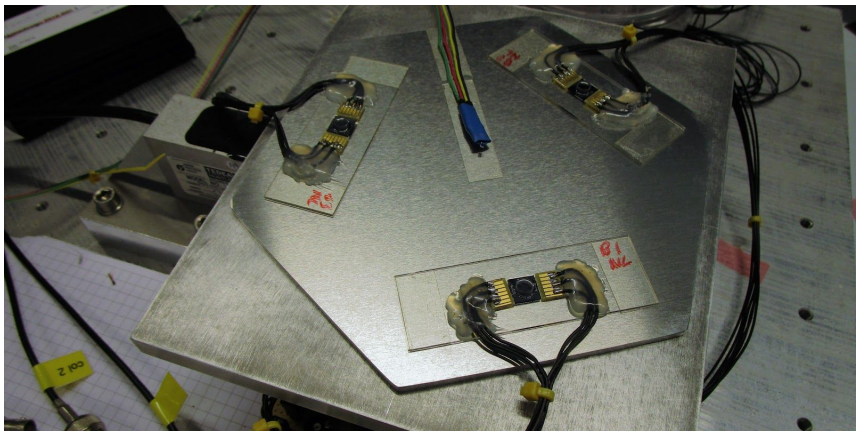


Close-up of chip assembly

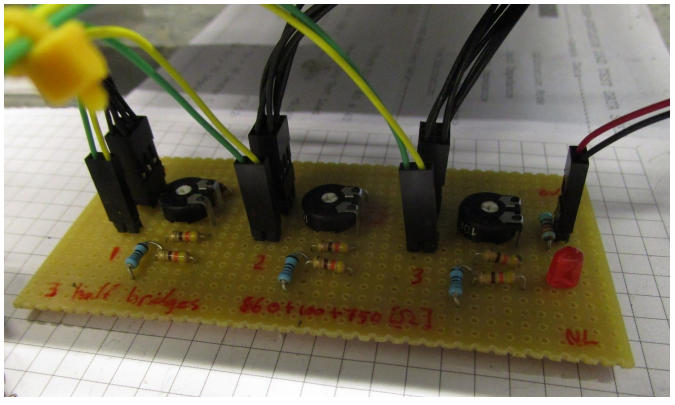
8.9. Attachment - Test setup 2



Test setup

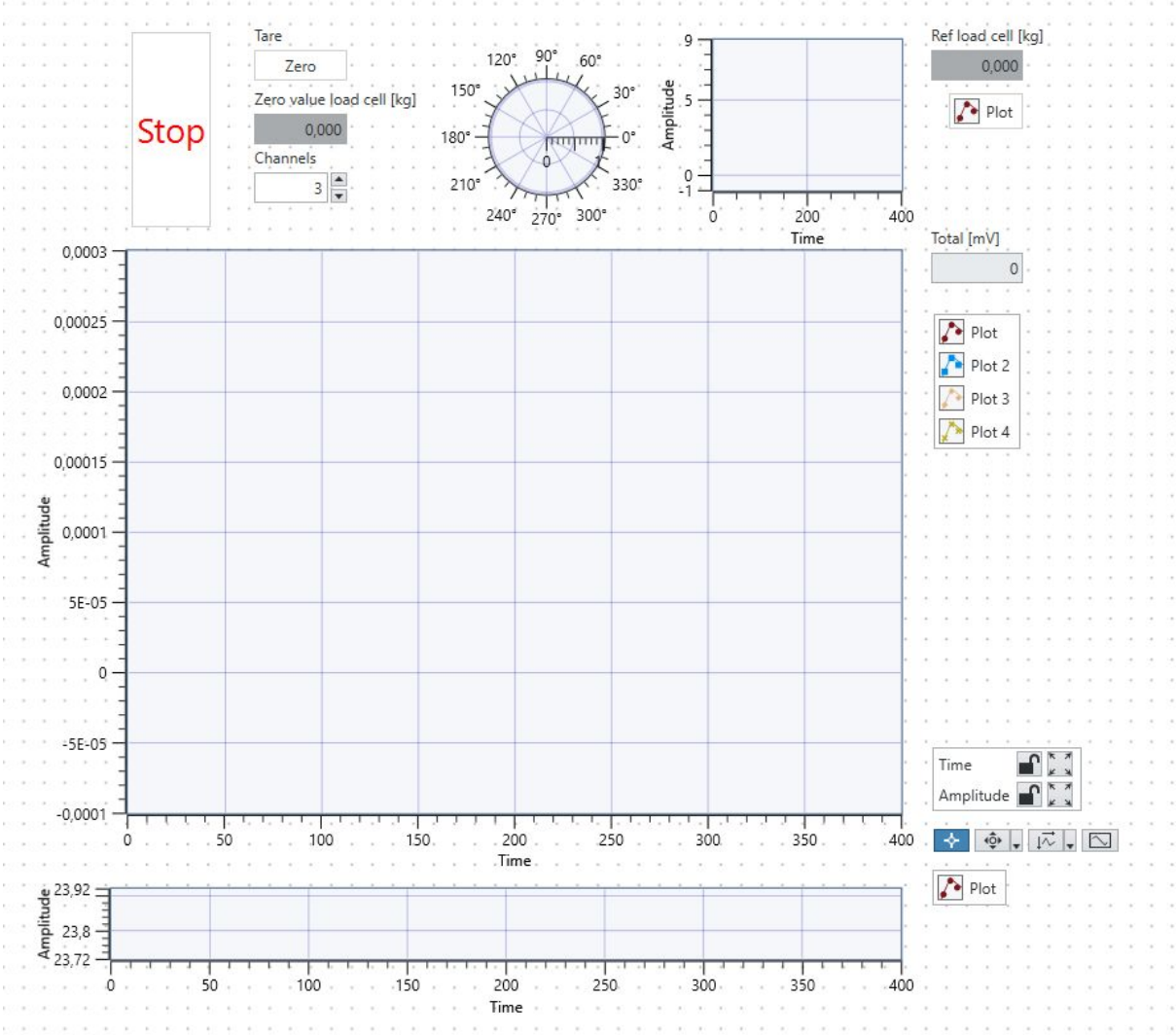


Scale insides

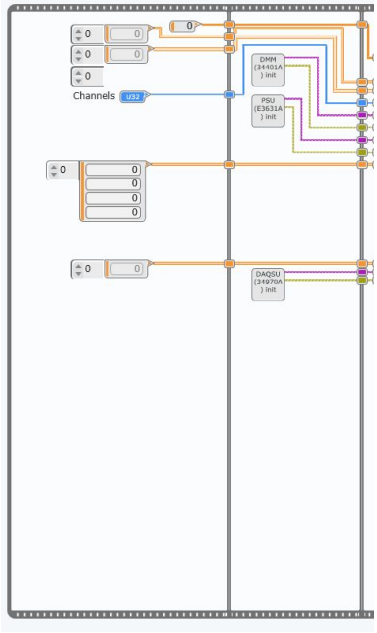


Half bridges x3

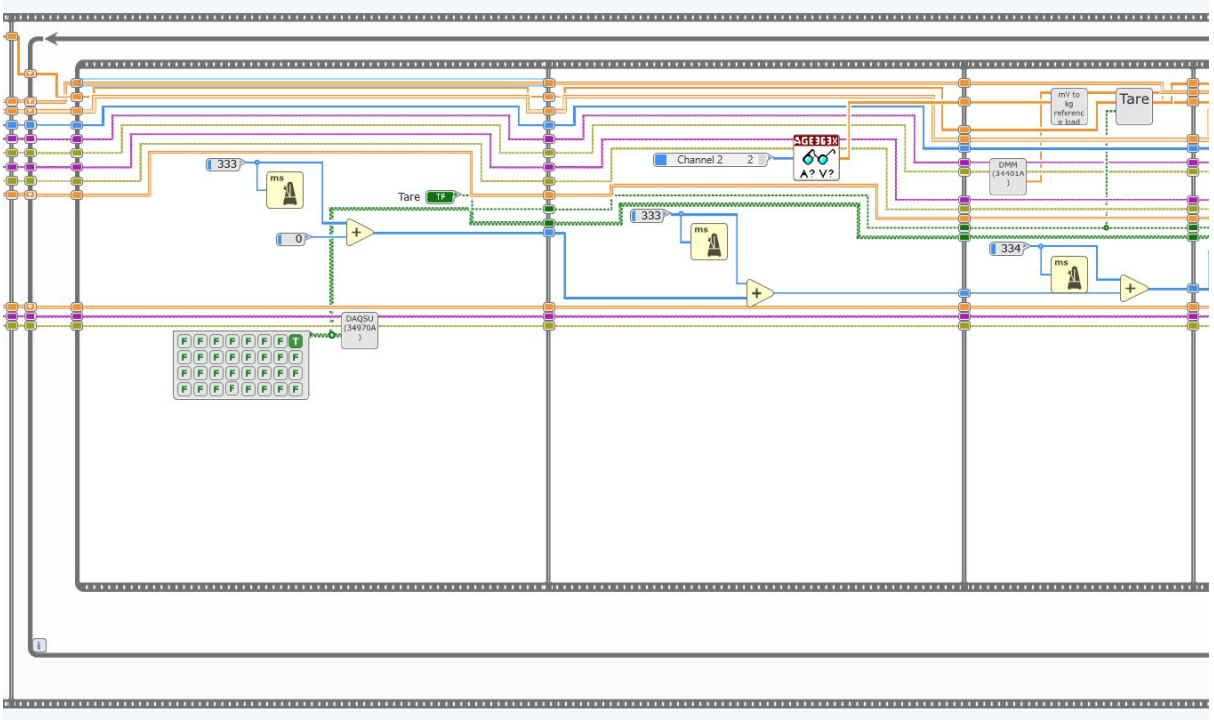
8.10. Attachment - Labview panel



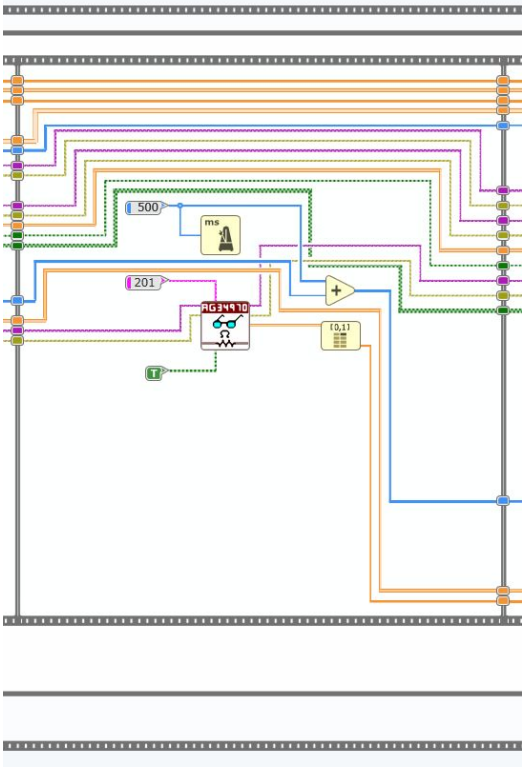
8.11. Attachment - Labview Diagram



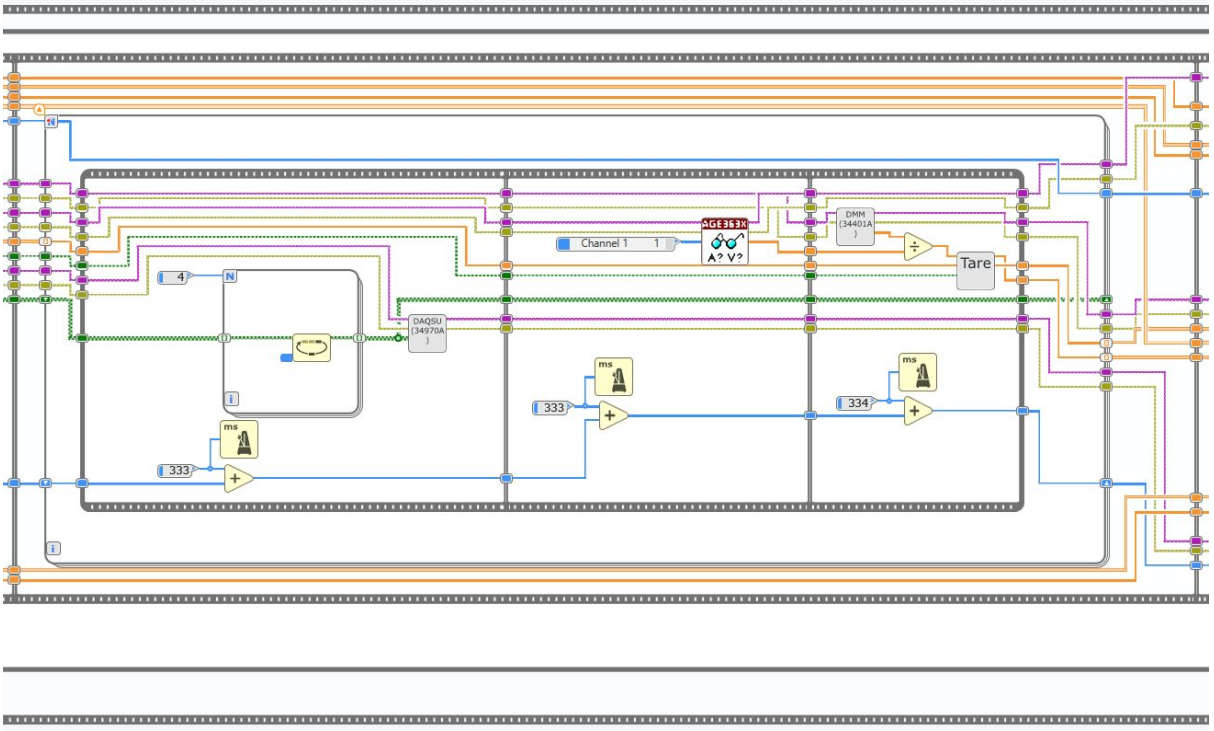
Initialisation step (init variables - init measurement equipment)



Reference load cell measurement (switch to load cell channel - read exact load cell excitation voltage - read load cell with DMM and convert readout to kilograms)

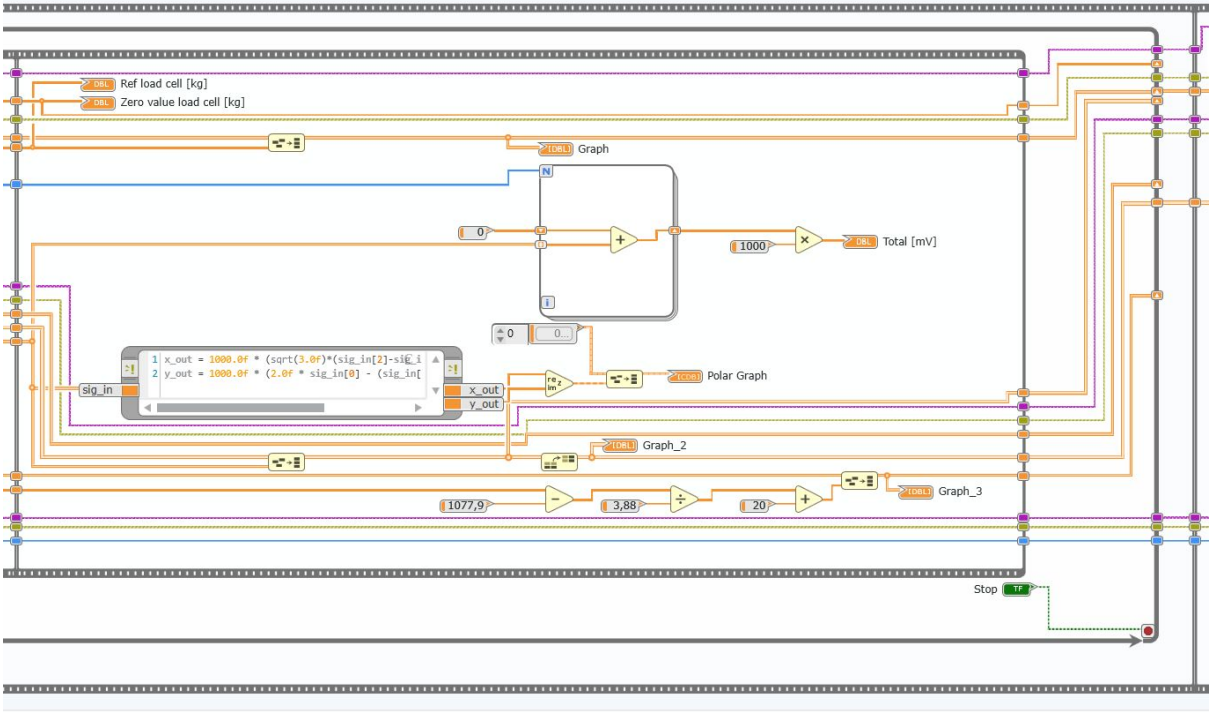


Temperature measurement[9] (read out the data acquisition unit)

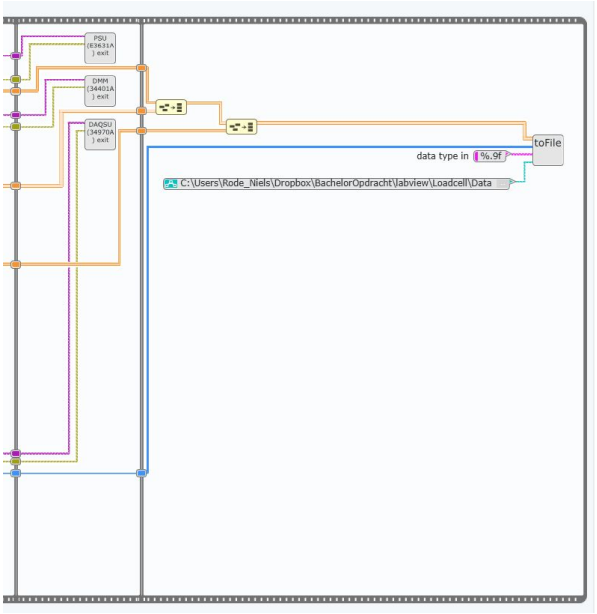


Chip measurement (switch to correct channel - read out the excitation voltage - read out chip with DMM)

[9] This part was not used for design A; an external measurement unit was used instead



Data visualization step (puts all previously collected data in an array and/or do some calculations with previously collected data in order to visualize it)



Exit step (when the stop function is called; terminate connections with measurement equipment - save collected data to file)