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Investigation of Ferroelectricity in Barium Titanate (BTO) thin-films and fabrication of BTO based Ferroelectric Tunnel Junctions (FTJs) using UV & E-Beam lithography

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Mohammadreza Mokhtari: *Investigation of Ferroelectricity in Barium Titanate thin-films and fabrication of BTO based Ferroelectric Tunnel Junctions using UV & E-Beam lithography,*  
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# ABSTRACT

Heterostructures of perovskite oxides have attracted much attention due to enormous different electrical, magnetic and optical properties [Baek & Eom]. Meanwhile, stabilized integration of these structures on silicon, makes it possible to incorporate unique electronic properties with Silicon-device technology which is highly desirable. However perovskites are incompatible with silicon processing line as the latter is an oxygen sensitive technology while the former is usually fabricated in presence of high oxygen pressure.

Within a consortium project named ULPEC, it is aimed to integrate “Ferroelectric Tunnel Junctions” (FTJ) on silicon to realize an ultra-fast and ultra-low-power electronic device used in neuromorphic computation. This work focuses on fabrication and characterization of bottom electrode and ferroelectric layers of aforementioned FTJ as well as fabrication and characterization of top electrode in cleanroom.

FTJ on non-silicon substrate, like single crystal Strontium Titanate ( $SrTiO_3$ ), is a canonical system with proven functionality (functional FTJ), therefore here in parallel to the integration on silicon, a canonical system was fabricated and characterized in order to enable the research team for detection of probable roots of non-functionality of Si-based samples by looking into differences. Ferroelectric layers of Barium Titanate ( $BaTiO_3$ ) as well as bottom electrodes of Strontium Ruthenate ( $SrRuO_3$ ) and Lanthanum Nickelate ( $LaNiO_3$ ) are grown by PLD and characterized structurally by RHEED (in-situ), XRD and AFM. Samples are functionally characterized by PFM.

PFM measurements represent ferroelectricity only in canonical system before fabrication of top electrode. XRD-RSM results indicate that out-of-plane strain in BTO layer in canonical samples results in tetragonality factor with 245% increase compared to bulk BTO. This increase is only 150% for Si-based samples. This larger induced strain in ferroelectric layers has been proved to stabilize ferroelectricity in FTJs. Coefficient of thermal expansion (CTE) of silicon and its difference with the value of typical perovskites, has been taken into account for justifying the difference of strain in two sets of samples. CTE-based Calculations show conformity to the results of XRD-RSM experiments. Origin of non-ferroelectricity in silicon-based samples should be investigated more according to the suggestions in chapter 6.

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# ABBREVIATIONS & SYMBOLS

AFM	Atomic force microscopy
ANN	Artificial neural network
BTO	BaTiO <sub>3</sub> or barium Titanate
EBL	Electron Beam Lithography
IPA	Isopropanol
LNO	LaNiO <sub>3</sub> or lanthanum nickelate
LSMO	La <sub>1-x</sub> Sr <sub>x</sub> MnO <sub>3</sub> or lanthanum strontium manganite
MBE	Molecular beam epitaxy
PDF	Powder Diffraction File
PFM	Piezo-response force microscopy
PLD	Pulsed laser deposition
PZT	Lead zirconate Titanate
SEM	Scanning electron microscope
Si	Silicon
SRO	Strontium oxide
STO	SrTiO <sub>3</sub> or strontium titanate
Nb:STO	Niobium-doped STO
STDP	Spike-timing-dependent plasticity
SRO	SrRuO <sub>3</sub> or strontium ruthenate
TER	Tunneling electro-resistance
UV	Ultra-Violet
XRD	X-ray diffraction
XRR	X-ray reflectivity

# 1

## INTRODUCTION & STATE OF THE ART

Nowadays, due to energy concerns, engineers of different fields try to go for the maximum efficiency possible while designing new devices. This applies as well for electronic devices as the building blocks for computational machines where energy efficiency and low latency are two vital factors. Cognitive computation like pattern recognition and classification are usually relied on complex algorithms (neural network) inspired from human brain. However energy consumed in our brain for the similar tasks is much lower compared to what computational machines consume. **Neuromorphic computation** is the new trend to address these issues and mimic the human brain by hardware realization of the neural networks.

This chapter explains how neuromorphic computation motivates current research. After a short introduction to neuromorphic computation and respective hardware realization methods, memristors are introduced which are known as the most popular device-level components for realization of neuromorphic computation systems. At the end, Ferroelectric Tunnel Junctions (FTJs) are introduced and the goal and approach of current thesis are discussed.

### 1.1 MOTIVATION - BRAIN-INSPIRED COMPUTATION

In Von Neumann architecture, the dominant architecture of current computational machines, digital information is stored in memory unites and is fetched by central unit processor (CPU) whenever needed [Burks et al]. For real-time processing with huge amount of data and complex algorithms like image processing, there is a need for machines working in ultra-low power and ultra-high speed regime. Current machines however fail to work in that regime due to excess heat generated inside CPU as well as limited speed of data transferring between memory and CPU which is known as “Von Neumann Bottleneck” [Wulf & McKee].

Human brain inspires scientists and engineers in efficient processing of huge amount of non-pre-processed and noisy data like pattern recognition, classification in general and face recognition in particular. In fact, brain is more power efficient than our best supercomputers by orders of magnitude therefore, neuromorphic computation is an effort to gain all these advantages by mimicking the behavior of human brain.

The new building blocks of neuromorphic computation systems is nowadays known to be memristors. The word “Memristor” is a portmanteau of “memory resistor”. A memristor is a two terminal, non-linear, passive electrical component which regulates flow of electrical current and remembers the amount of charge that previously flowed through. From definition, one can imagine the first application of memristor as a non-volatile memory cell. The concept of memristor was first proposed by [L. Chua](#) as a result of symmetry consideration in theoretical electronics in 1971. However recently memristor is a term applied for any electronic element which its resistance can be fixed at multiple different values. Recently by employing a network of memristors, [Sheridan et al](#) reported a promising approach for the problem of pattern recognition by using a  $32 \times 32$  crossbar array of analog memristors, an approach which can tolerate the burden of highly massive computations and energy consuming for real time, event based detection systems

Memristive FTJs, are the kind of memristors which is the focus of this thesis. Ferroelectrics are materials with spontaneous electric polarization that can be switched by applying external electric fields. A memristive FTJ is fabricated by sandwiching a thin ferroelectric layer between two electrodes with different materials. The ferroelectric layer should be thin enough to enable quantum tunneling to happen. FTJs are discussed more in detail in chapter 2.

## 1.2 GOALS & APPROACH

This thesis focuses on the fabrication of FTJs on silicon. All the layers of FTJ are Perovskites, a specific type of materials which will be discussed in chapter 2. Due to great lattice mismatch between silicon and perovskites, silicon is buffered with  $SrTiO_3$ (STO) layer as an adaptive layer (figure 1-1, bottom). These received buffered silicon substrates are fabricated using MBE process by ULPEC collaborators in Zurich. Bottom electrode and ferroelectric layers, shown in figure 1-1, are grown then with PLD method. Samples are characterized structurally and functionally to investigate expected structural and functional (Ferroelectricity) properties. Cleanroom processes are applied afterward to fabricate FTJ top electrodes which are not shown in the below image and are usually from Cobalt and Gold.





Figure 1-1 - (Above) Realizing bottom electrode and ferroelectric layer of an FTJ on single crystal  $SrTiO_3$  as main substrate and (Below) Realization of layers on STO-buffered Silicon. Above is a canonical system with reported ferroelectric property in literature.

After functional characterization of silicon-substrate samples with PFM, Ferroelectricity was not observed, therefore fabrication of FTJs on single crystal of STO was started in order to make a benchmark system. As benchmark system uses perovskites in all layers, including substrate, and is a known canonical system with proven ferroelectricity property in BTO layer, it helped the research for exploring the origin of non-ferroelectricity of silicon samples through comparing the results of structural characterization. Therefore the main challenges in this thesis are

- First, Fabrication and structural/functional characterization of silicon based FTJs as well as benchmark FTJs. Exploring the origin of non-functionality in silicon based FTJs is then become possible by comparing the results of the two sets of samples.
- Second, Fabrication of top electrode in both sets in cleanroom using UV/E-Beam lithography & sputtering, as well as characterizing the ferroelectricity of the FTJs to compare results with what was measured in pre-cleanroom phase in order to discover how cleanroom processes affect the quality of FTJ functionality.

To achieve the goals, hetrostructures were fabricated with PLD with the capability of in-situ characterization of films with a RHEED device. RHEED patterns give an immediate idea about the quality of the samples, regarding surface morphology. Next to that, AFM, PFM and XRD measurements are done to characterize the ferroelectricity of FTJ as well as surface morphology investigation, thickness measurement and determination of the crystalline quality and strain studies of the layers.

In the next step, samples are introduced to MESA+ cleanroom for fabrication of top electrodes in dimensions ranging from few hundred nanometers to few micrometers to make the early prototype of the FTJ device. UV & E-Beam lithography used to pattern ferroelectric layer. Sputtering was used to grow cobalt and gold as top electrodes. In order to discover the effects of these processes on functionality of the prototype, PFM measurements were done afterward.

After this introductory chapter, chapter 2 is dedicated to the background physics of ferroelectric tunnel junctions (FTJs) and reviewing literature in the field of material science with a focus on key publications on FTJs with application in neuromorphic computation. Chapter 3 explains the methods and techniques used for the experimental work within both phases 1 & 2. Chapter 4 describes thesis-specific details of fabrication processes. Results are presented in chapter 5 and discussed in chapter 6, where also recommendations for further research are given. The conclusions are presented in chapter 7.

# 2

## LITERATURE REVIEW, BACKGROUND PHYSICS

Outlook of the recent researches on FTJs is useful to justify and elaborate clearly the motivations behind this thesis. Meanwhile a model of FTJ, related mechanism of polarized domains and background physics of ferroelectricity has been presented concisely which enables us to analyze more effectively the experimental results. In general, this chapter consists of more detailed background physics of memristors especially those realized with FTJs and summarizes state of the art and recent advances in fabrication of FTJs.

State of the arts of memristor-based neuromorphic computation is first presented in this chapter. Then, a review of FTJ as the specific ferroelectric-based memristors is given with focus on  $BaTiO_3$  (BTO), the material which was used as ferroelectric layer in fabricated FTJs within this thesis. Remembering the main challenges from chapter 1, a review for integration of perovskites on Silicon is given as well. Finally, basic background physics of FTJs and associated phenomenon are discussed, especially those who made some serious challenges during experimental work like pinned ferroelectric domains, screening charges, depolarization fields and domain switching.

### 2.1 LITERATURE REVIEW

Recently a concise review of the researches performed on the memristors and device challenges regarding their compatibility with CMOS processes, electrical performances and integration is published by [Li et al]. For a comprehensive review on associated hardware of neural network and neuromorphic computation, refer to [Manan Suri] & [Schuman et al]. Soren Boyn has extensively covered experimental and theoretical aspects of fabrication and characterization of FTJs with focus on BFO as the ferroelectric layer in his thesis named: “Ferroelectric Tunnel Junctions: Memristors for Neuromorphic Computation”. I have been inspired by it and found many references for this thesis.

#### 2.1.1 MEMRISTOR-BASED NEURAL NETWORKS

It was first proposed by [G. S. Snider](#) to imitate the function of synapses by use of memristors. There is also agreement that memristors should be arranged in crossbar array in order to have the best inter-neuron connectivity. This is why in most literatures, you see the crossbar array for implementation of neuromorphic devices. A multilevel data storage in crossbar array was demonstrated in 2012 by [Kim et al](#), however, the fabrication process for connecting the array to CMOS technology has not been technically matured yet. Below graphs demonstrate the evolution of researches that “memristor” and “Ferroelectric Tunnel Junction” keywords are in their title. As it can be seen, nearly from 2005 onward, topics has attracted more attention and in 2016/2017 has shown a maximum.

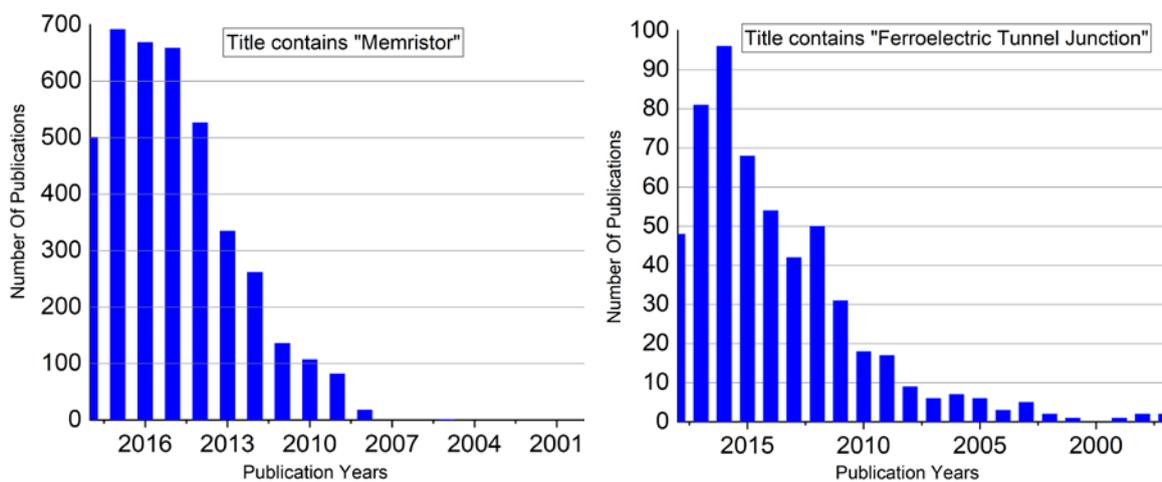


Figure 2-1 - Evolution of research with "Memristor" and "Ferroelectric Tunnel Junction" in their title [source: Web of knowledge research 2018]

A memrsitor should possess the capability of “resistive switching” or in brief “RS”, to be enabled to mimic the behavior of synopsis. In next section, there is a review on different materials showing RS property including memristors.

### 2.1.2 RESISTIVE SWITCHING IN MEMRISTORS & FTJ

“Resistive Switching” or in brief RS, is the fundamental basis for neuromorphic computation realization. A nice survey of different mechanism of RS has been published by [Jeong et al](#). Based on that, number of materials which show such a property, are huge. Binary “Transition Metal Oxides” (TMOs), Perovskite type TMOs and large band gap high-k dielectrics and graphene oxides are among them. They can be considered as competitive technologies for realization of novel generation RAMs as well as building blocks of neuromorphic computation.

Memristors are one of the most studied types of RSDs. Theoretically, Chua predicted the existence of memristors in 1971 as the fourth fundamental electronic device. It means that this device cannot be realized by the 3 other devices, to wit, Resistor, Capacitor and Inductor. Chiolerio et al Believe that memristors are perhaps the best candidate for realization of neuromorphic computation systems which can operate in beyond-Moore era of Nano electronics.

Resistive switching can be divided into two unipolar and bipolar categories. This classification is based on degrees of freedom of the material when it responds to the stimuli of a functional input (like voltage or current). Jeong, D. S. et al clarifies difference between the two classes. Resistive switching in binary TMOs, were reported for  $TiO_2$  [Argall, F.], NiO [Gibbons and Beadle] and  $Nb_2O_5$  [Hiatt and Hickmott] already in 1960s. Resistive switching mechanism of FTJs are only discussed here due to the scope of this thesis. For further and a complete review of different RSDs and respective mechanisms, you can refer to Jeong, D. S. et al.

In short, FTJs are RS Ferroelectrics. The fundamental mechanism of RS phenomena is the quantum mechanical tunneling [Kohlstedt et al], [Tsymbal E Y and Kohlstedt ]. In section 2.2.4 mechanism of RS in FTJs is described concisely regarding the scope of the project. The mechanism is reviewed in Garcia, V. and M. Bibes 2014 as well as in Chanthbouala et al and Tsymbal & Kohlstedt .

### 2.1.3 FTJ AS A MEMRISTOR

FTJs are categorized as Perovskite type TMOs. In FTJs, tunneling probability varies with the ferroelectric switching which in consequence, ferroelectric-resistive switching emerges. Chiolerio et al recently reviewed state of the arts and perspectives of the coupling RS devices (RSD) with neurons. Based on that, crossbar RSD network can potentially offer connectivity similar to neurons with RSD working as synapses.

A very stylish and useful review for the FTJs and their application in Neuromorphic computation as well as storage applications, has been written by Garcia, V. and M. Bibes 2014. How polarization in ferroelectrics can lead to the control of resistive switching has been reviewed nicely there. There is also a nice table demonstrating the reported TER effect within different FTJ realizations.

Biological learning rule by which, neuromorphic computation works, is named Spike-Timing-Dependent Plasticity (STDP). In Soren Boyn's thesis, the accordance of STDP with the resistance switching in FTJs has been investigated. Synapsis in brain connect neurons which

based on STDP rule, strength of the synapsis is changed while brain is performing a certain task. Resistive switching in FTJs play the role of the changing strength and emulates the behavior of synapsis. A selective collection of recent works from some of the leading research groups across the world, working on hardware realization of neuromorphic computation is written by [Manan Suri](#). You can find theoretical analysis of memristive kind STDP, Non-volatile memory with crossbar arrays for Non-von Neumann computing and many different approaches to realize hardware for neuromorphic computation.

Recently a very decent article by [Velev et al.](#) is published to review the development of the ferroelectric tunnel junction concept and the role of theoretical modelling in guiding experimental work. A wide range of physical phenomena that control the functional properties of ferroelectric tunnel junctions are summarized as well as the state-of-the-art achievements in the field. Mechanism of TER is wholly covered as well as effects of phase transition at the interface.

A very nice review on “Surface screening in ferroelectric thin films and its effect on the polarization dynamics and domain structures” has been presented by [Kalinin et al.](#) Surface screening and depolarization effect in thin film ferroelectrics are two major concerns which highly affect the functionalities of FTJs. [Ahluwalia and Srolovitz](#) have shown the correlation between 180° domains and the thickness of the FTJ. They “show that the 180° domain size decreases as the film thickness is reduced and the film abruptly becomes para-electric below a critical size”.

Non-switchable domains are studied by [Myung-Geun et al.](#) . They “show that electronic band bending across film/substrate interfaces locks local polarization direction and further produces unidirectional biasing fields, inducing non-switchable domains near the interface”. I will address this problem in the samples grown on silicon as the main substrate.

#### **2.1.4 GROWING COMPLEX OXIDES (FTJ) ON SILICON**

Integration of functional oxides on silicon has been a hot challenge since two recent decades. Main motivation is to enabling Silicon based device technology to be empowered by novel and rich features of perovskite oxide hetero-structures. Features like Ferroelectricity, Superconductivity, Ferromagnetic, Multiferroic and so on.

[Reiner et al](#) presents a nice review of “Crystalline oxides on silicon”. Meanwhile, [Baek, S. H. and C. B.](#) report “Epitaxial integration of perovskite-based multifunctional oxides on silicon”. The main challenge in integration remains in tendency of silicon to react with oxygen and

creation of silicon oxide on top, which makes deposition of perovskites difficult. This challenge has led the scientists to grow first a buffer layer on top of silicon in order to prevent aforementioned phenomena. However the buffer layer should have on one hand, compatibility with silicon and on the other hand with perovskites. Therefore investigation on different materials as a buffer layer is still going on.

In IMS group, Yttria-Stabilized Zirconia (YSZ), Cerium Dioxide ( $\text{CeO}_2$ ) and lead zirconate titanate (PZT) have been investigated for deposition of LSMO and SRO respectively by [Groenen et al](#), [Dubbink et al](#) and [Dekkers et al](#).

Integrate perovskites with silicon via crystalline, inorganic Nano-sheet templates is the other strategy pursued within IMS group. This strategy as is beyond our target.

If the buffer layer has to admit growing perovskites on top, one option is to choose a perovskite as a buffer layer and find a method to integrate it with silicon avoiding creation of amorphous silicon-oxide on top. Molecular beam Epitaxy (MBE) is the method which meets this requirements by working in ultra-high vacuum (UHV) regime. By providing fine control on various MBE parameters, integration of epitaxial  $\text{SrTiO}_3$ (STO) thin films on bare, defect-free silicon (Si) has been achieved. MBE mechanism can be briefly explained as: first, by depositing half a monolayer of Strontium (Sr) on Silicon (Si), Sr protects Si layer from oxidization. Then by growing thin amorphous STO layer on top of it at near room-temperature, and letting it to be crystalize in vacuum, an epitaxial layer of STO can be formed directly on Si. [[Choi et al](#)]. Early epitaxial growth of STO on (001) Si with MBE method was reported by [McKee et al](#). This was the first attempts and since then many investigations have been done on growing STO on Si.

Meanwhile chemical solution deposition approach (CSD) is another successful technique. [Vila-Fungueiriño et al](#) has reported complex oxide nanostructures epitaxial growth on silicon using the combination of CSD and MBE. Meanwhile, [Diaz-Fernandez et al](#) has reported growth of a 1/2 monolayer (ML) of SRO buffer layer on the reconstructed Si (001) surface by PLD. Deposition of STO was in inert Argon atmosphere with latter oxidation and crystallization phases. MBE growth of BTO layers directly on silicon has been reported by [Dubourdieu et al](#) and [Warusawithana et al](#).

Nowadays STO buffered silicon is a commonly used single crystal substrate for the epitaxial growth of perovskites. STO has a cubic structure with lattice parameter of  $3.905 \text{ \AA}$  which is close to most of the perovskites. When STO is rotated  $45^\circ$  in-plane, respect to silicon, the lattice-mismatch is only 1.7% which makes it suitable for epitaxial growth.

In the result chapter, we will see that when LNO and BTO were grown on top of STO-buffered silicon, BTO layer fails to show switchable polarization domains. This is the issue which is under investigation by IMS group within ULPEC project. Within this thesis, in order to investigate the cause, single crystal STO substrates were chosen to deposit SRO and BTO on top. Results from this approach were used to make a benchmark system with proven ferroelectric properties.

## 2.2 BACKGROUND PHYSICS

### 2.2.1 FERROELECTRICITY

Hysteresis loop is a characteristic of ferroelectrics in macroscopic scale. Applying an external electric field increasing from zero, orients the polarization domains parallel to the field. When external field is sufficiently increased, all the domains are paralleled, resulting to the saturation polarization  $P_s$ , shown in image below. However when field intensity is being decreased, not all the domains switch direction even if the field becomes zero, resulting to the permanent polarization  $P_r$ . By increasing the external field in the opposite direction, more domains will start to switch according to external field in a way that for a certain intensity of external field named coercive field ( $-E_c$ ), domains are directed in different directions and cancel the effect of each other, resulting to zero net polarization. Increasing more the external field results in the negative saturation polarization,  $-P_s$ . As mentioned in introductory chapter 1, this is due to the non-centrosymmetric structure of the crystal.

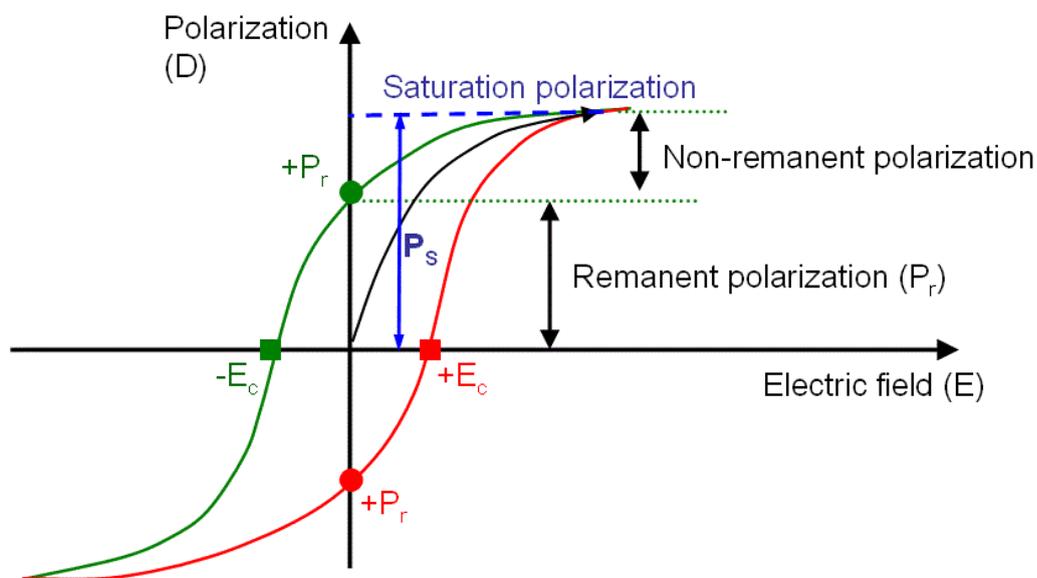


Figure 2-2-2 – Hysteresis loop of a typical ferroelectric material. (Source: [81])

## 2.2.2 FERROELECTRICITY IN PEROVSKITES (BTO)

Ferroelectrics studied and used in this thesis are all Perovskites. Perovskites are materials with the same structure of Calcium Titanium Oxide ( $CaTiO_3$ ), known as the Perovskites structure. The general formula is  $ABX_3$ , where A & B are cations of very different sizes and X is anion which bonds to both cations A and B [Luo et al].

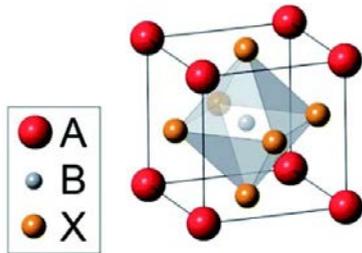


Figure 2-3 – Typical perovskite structure (source: Luo et al)

In symmetric cubic form, “A” cations are in the corners and “B” cations in the center. X anions are in face-centered and make an octahedron around “B” cations. Then each “A” cation has 12 nearest neighbors and the structure is centrosymmetric without displaying any ferroelectricity. If the interaction with cations and anions were purely ionic, there would be no ferroelectricity, however orbital hybridization between X anions and A/B cations, might induce a shift in the atomic positions.

Perovskite used as the ferroelectric layer in this thesis is BTO. Phase transformation occurs in three different temperatures in BTO which in consequence, affects the ferroelectric property of BTO as depicted in figure 2-1. Above  $120^\circ C$ , BTO is in cubic form (a). At  $120^\circ$ , a transformation from cubic to tetragonal occurs which induces ferroelectricity in  $[001]$  direction (b). At approximately  $0^\circ C$ , crystal structure changes from tetragonal to orthorhombic which induces ferroelectricity in  $[011]$  direction (c). Below  $-80^\circ C$ , another phase transition from orthorhombic to rhombohedral takes place which changes the ferroelectricity to  $[111]$  direction (d).

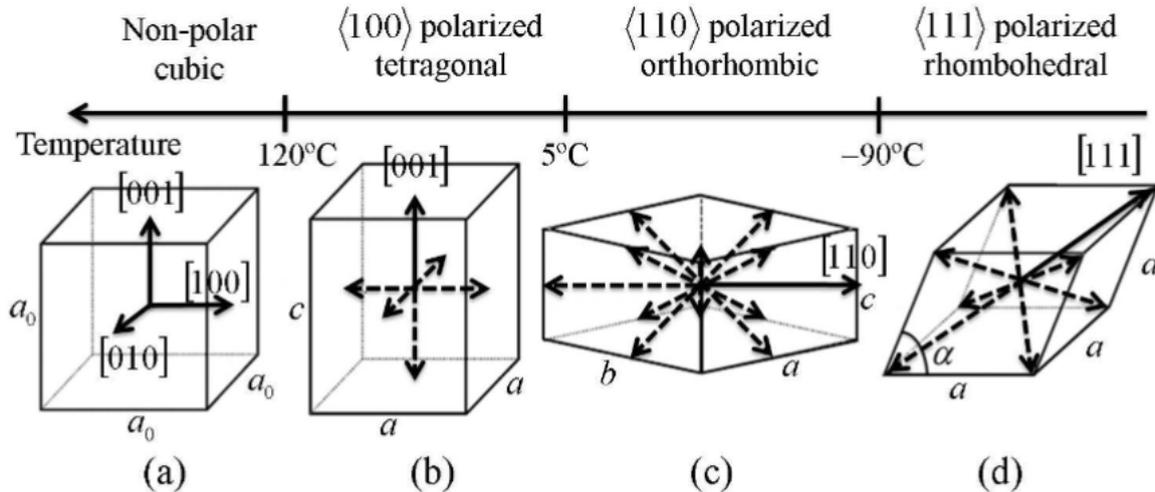


Figure 2-4 - Schematic representation of the crystal structure of BTO at different temperatures (source: Potnis et al).

### 2.2.3 SURFACE SCREENING AND DEPOLARIZATION FIELD

In thin film ferroelectrics, effect of interface charges is crucial. When a ferroelectric material is bound with two metallic electrodes like a capacitor, surface electrostatic charges from ferroelectric material attract screening charges in the electrodes. In a perfect metal, screening charges are distributed ideally at surface of metal, as represented in figure 2-4 (a). Therefore the potential profile would be zero for every x value in x-axis which is perpendicular to the interfaces (c). In a non-perfect (realistic) metal, screening charges are spread over a screening length and not all at the interface (b). This yields a potential profile like as one shown in (d). As can be seen, the induced electric field ( $E_d = -d\phi/dx$ ) due to this charge distribution is in opposite direction to the Polarization P, which decreases polarization and called “Depolarization Field”. In very thin ferroelectric layers, depolarization field effectively destabilizes the polarization and drives formation of domains with opposite polarization direction [Soren Boyn].

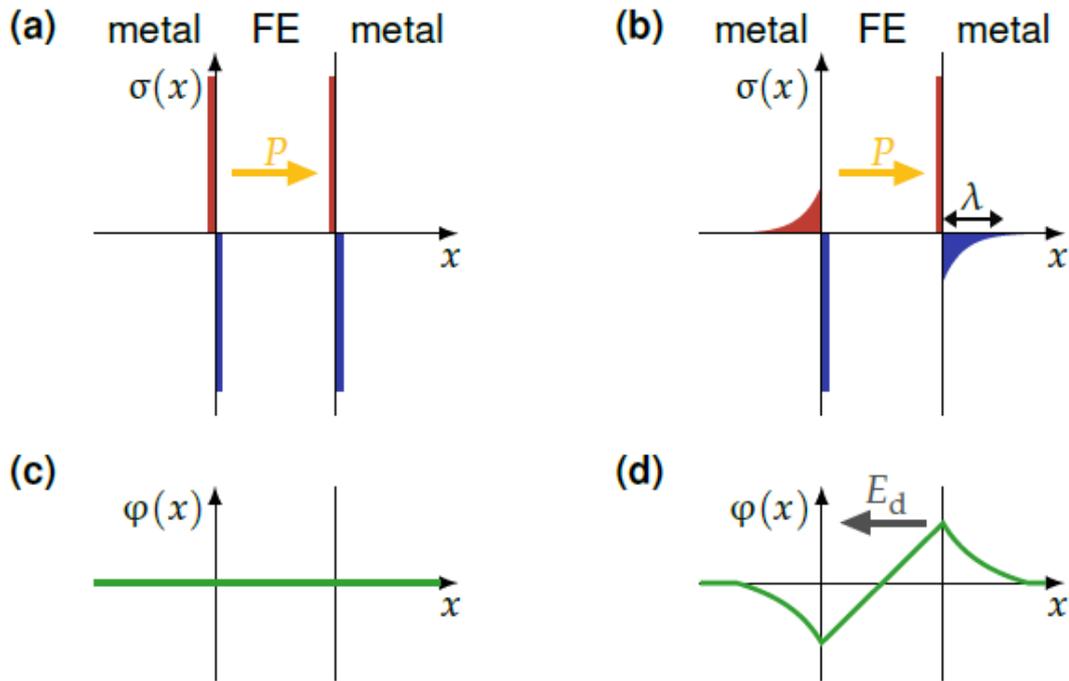


Figure 2-5 Surface charge and potential distribution in an FTJ (source: Soren Boyn)

If there is a lattice mismatch between substrate and ferroelectric layers, strain is induced in ferroelectric layer which in consequence decreases the depolarization field and stabilizes ferroelectricity [Choi et al], [Ederer & Spaldin] and [Ramesh & Spaldin]. In this way, tetragonality of the BTO can increase which strengthens the spontaneous polarization.

## 2.2.4 RESISTANCE SWITCHING MECHANISMS IN FTJ

As discussed before in chapter 1, resistance switching is the fundamental mechanism for every resistive switching material including FTJs. Ferroelectric layer of FTJs are very thin which allows quantum tunneling happen. Therefore, change in resistance in FTJs is summarized as “Tunneling Electro Resistance” or TER in brief. TER is defined as  $TER = \frac{R^{\rightarrow} - R^{\leftarrow}}{R^{\leftarrow}} \times 100$  in which  $R^{\rightarrow}$  &  $R^{\leftarrow}$  are resistance values in two opposite (by 180°) polarization directions, perpendicular to the surface. I will explain here the electrostatic effects which lead to TER. The other effects incorporated to TER, are “Interface Effects” and “Strain Effects”. Below we will see how resistance in different polarization varies and how much?

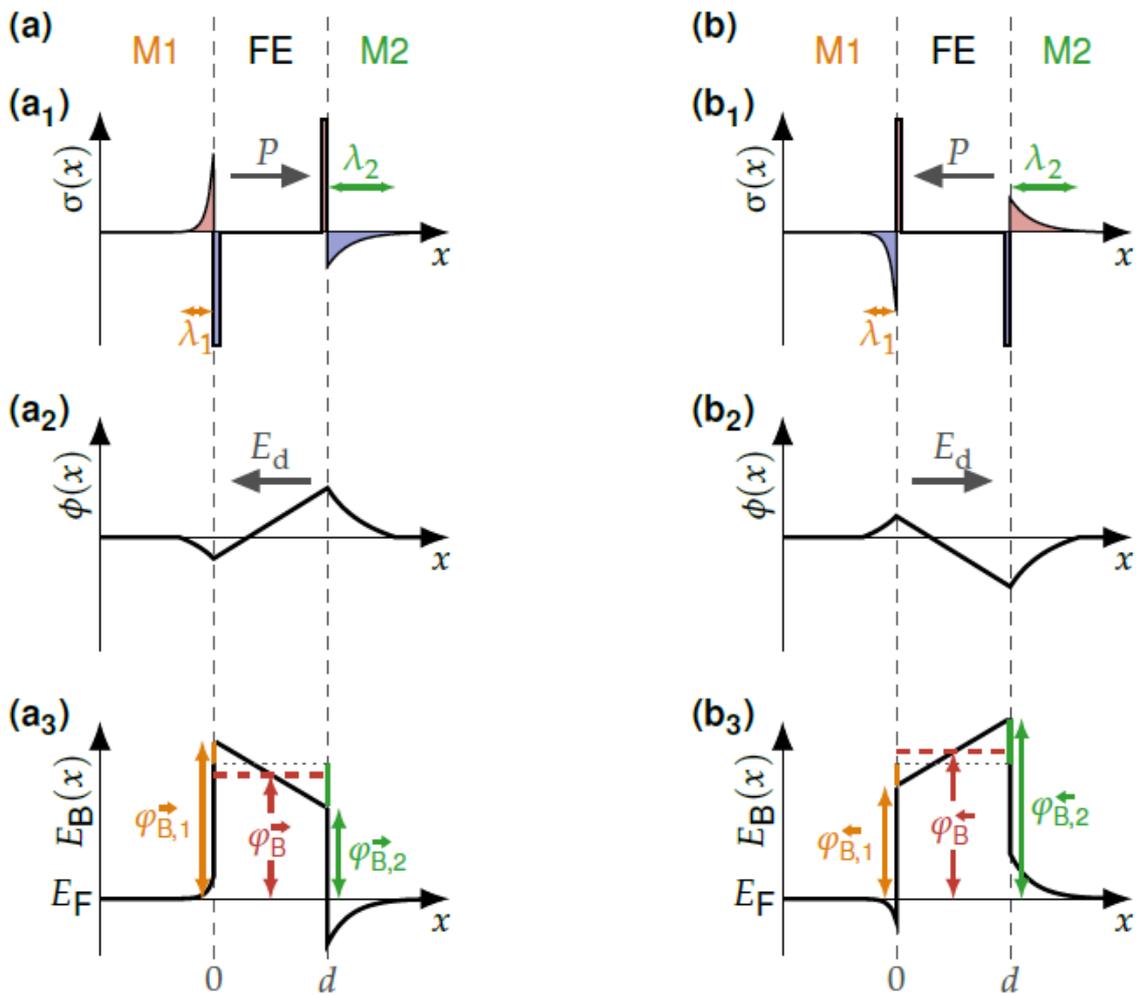


Figure 2-6 TER change based on electrostatic effects in an asymmetric FTJ (source: *Soren Boyn*).

As depicted in figure 2-6, when the two electrodes of the ferroelectric layers are from different materials, screening charge profiles are shaped with different profiles in two sides of FE ( $a_1$ ). In configuration “a”, the polarization points toward right and consequently the electrostatic potential ( $\phi$ ) and energy barrier profiles ( $E_B$ ) are formed as can be seen in  $a_2$  and  $a_3$ . On the other hand, when the voltage is applied to the FTJ with opposite polarity, profiles of “screening charges”, “electrostatic potential” and “energy barrier” in 3 different regions of FTJ is shown in figure 2-6  $b_1$ ,  $b_2$  &  $b_3$ . In brief, asymmetry in screening charges at interfaces induces interfacial energy barrier profiles which are different for two aforementioned configurations. Therefore, the barrier energy inside the FE layer will have profiles with different average value for two configurations which in consequence lead a change to tunneling resistance.

The energy barrier at interface ( $\phi_B$ ) is defined by the difference between metal “work function” and “electron affinity” of the layer (Here BTO). And when the electron transport through the ferroelectric layer is dominated by the “direct tunneling mechanism”, the barrier height has a crucial role and for low bias voltages, current density is proportional to [Soren Boyn]:

$$j \propto V \frac{\sqrt{\phi_B}}{d} \exp(-d \sqrt{\phi_B})$$

This exponential dependency of  $j$  to  $\sqrt{\phi_B}$ , clearly shows why even low changes of  $\phi_B$  leads to huge TER effect.

Two other tunneling effects, to wit “Fowler-Nordheim tunneling (FNT)” and “Thermionic Injection (TI)”, have contribution to the current densities. Contribution of these three different tunneling to the current density has been theoretically calculated and shown below.

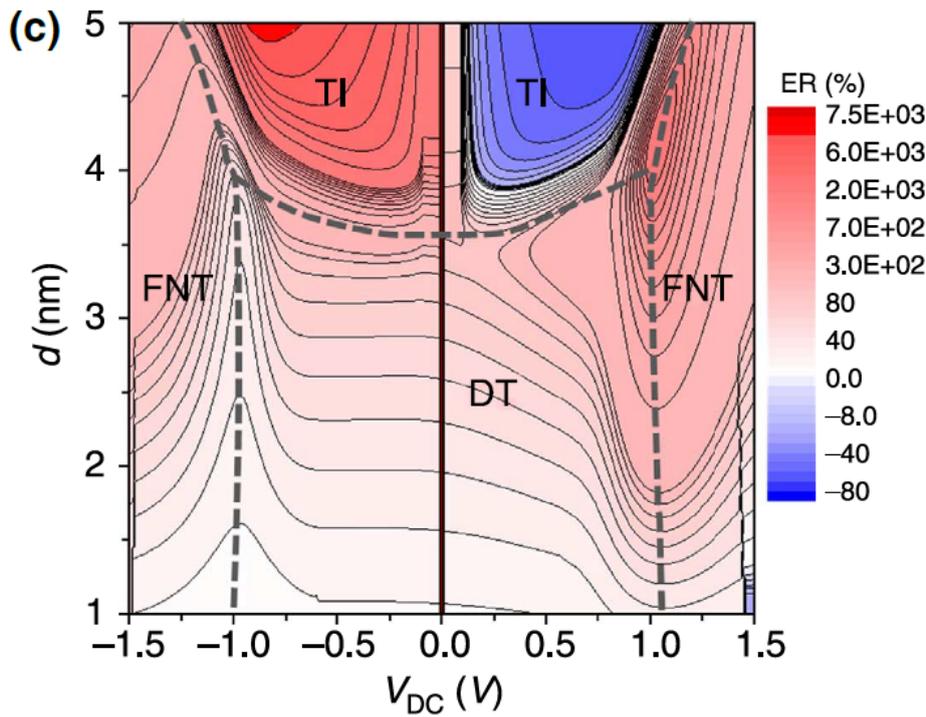


Figure 2-7 Thickness and voltage dependency map of tunneling electro resistance (TER) [source: Garcia and Bibes]

Our ferroelectric layers are fabricated with thickness of around 5 nm and voltages applied for PFM measurements are in the range of ~5 volts. Therefore the two other tunneling currents should be taken into account TI for negative voltages and FNT for voltages above 1 volt.

## 2.2.5 DOMAIN WALLS / SWITCHING MECHANISM

Creation of polarization domains inside a FTJ and mechanism governing the switching of domains are presented here. As depicted in figure 2-8, when an external electric field is applied to a homogeneously polarized ferroelectric layer in opposite direction of polarization vector, leads to creation of small reversed regions named nuclei (figure 2-8 b). Creation of nucleus start from one of the interfaces and gradually grows toward the opposite interfaces forming needle-like shape as shown in figure 2-8 c. Growth of domains continue toward interfaces as well as sideways however, speed of sideway growth is slower than toward interfaces (Figure 2-8 d). Boundary between two opposite polarization domains are called domain walls. Growth continues until domain reversal completes (2-8 e).

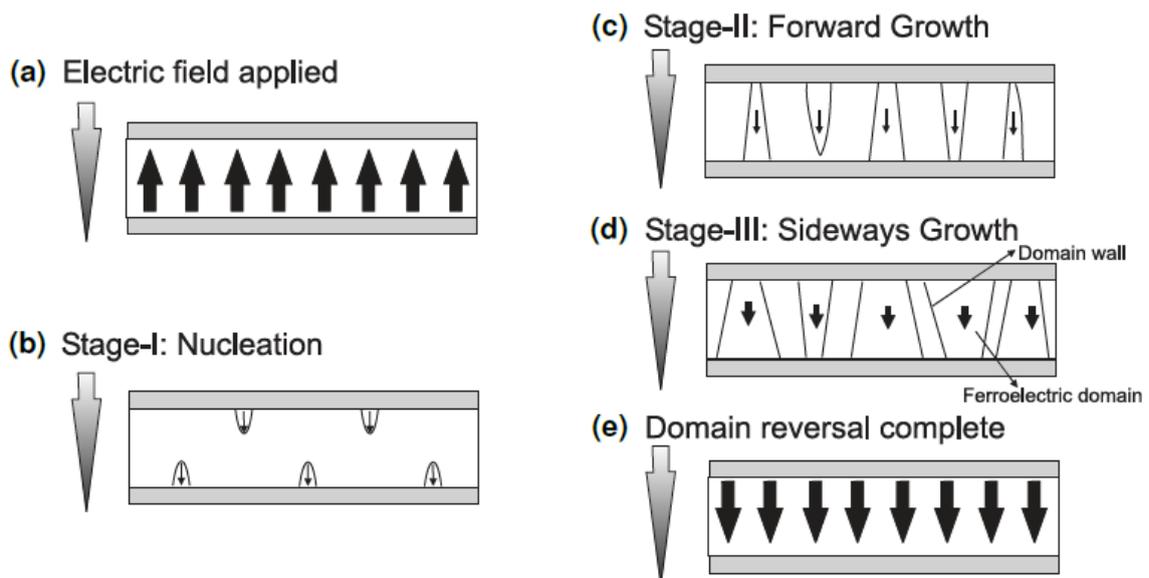


Figure 2-8 Domain creation mechanism [source: *Dawber et al*]

# 3

## METHODOLOGY

Methods, techniques and processes used for fabrication and characterization of samples/devices would be discussed here. This chapter is divided into two sections, in-cleanroom methods and out-of-cleanroom methods.

To fabricate thin-films of Barium Titanate and associated electrodes, “Pulsed Laser Deposition” (PLD) technique is used. “X-Ray Diffraction” (XRD) method is used to investigate the crystalline structure, strain in films and thickness of the layers. Members of “Scanning Probe Microscopy” (SPM) family technique, like “Atomic Force Microscopy” (AFM) and “Piezo-Response Force Microscopy” (PFM) are used to characterize the surface morphology as well as ferroelectric properties of the layers.

E-Beam lithography, UV lithography and Sputtering are used afterward to shape the existing stack of layers and fabricate the “Ferroelectric Tunnel Junction” device. Here, the techniques are introduced and discussed in detail.

### 3.1 PULSED LASER DEPOSITION - PLD

Pulsed laser deposition (PLD) is a physical vapor deposition (PVD) technique in which a high-power, focused laser beam in vacuum ablates target material to be deposited to the substrate surface and make a thin-film. Actual physics behind the interaction of light and matter is quite complex, though, one can model the ejection of material as an evaporation of surface of the target due to superheating. The main advantage of PLD is the creation of stoichiometric plume, similar to the target material whereas in evaporation-based depositions like CVD, composition of materials is dependent to the pressure of the vapor. Apart from this, PLD is fast, conceptually simple, versatile regarding target materials, cost effective and scalable. PLD, known also as “Laser MBE”, can be applied for thin layer deposition of materials like: Hetero-structure metal oxides, high temperature superconducting materials, silicon oxides, high k oxides, metal nitrides, ferroelectric materials, etc. (source: <http://www.adnano-tek.com/pld.html>)

PLD is fast, however, plasma plume is thermodynamically out of the equilibrium. Therefore fine tuning of the parameters is needed to achieve epitaxial, flat and fully crystalline films [Ismail-Beigi et al].

Depositions were done with a research-type PLD, manufactured by “Twente Solid State Technology” (TSST). This PLD has capabilities of rotating target and RHEED in-situ measurement. Schematic diagram of a typical PLD is shown below in figure 3-1.

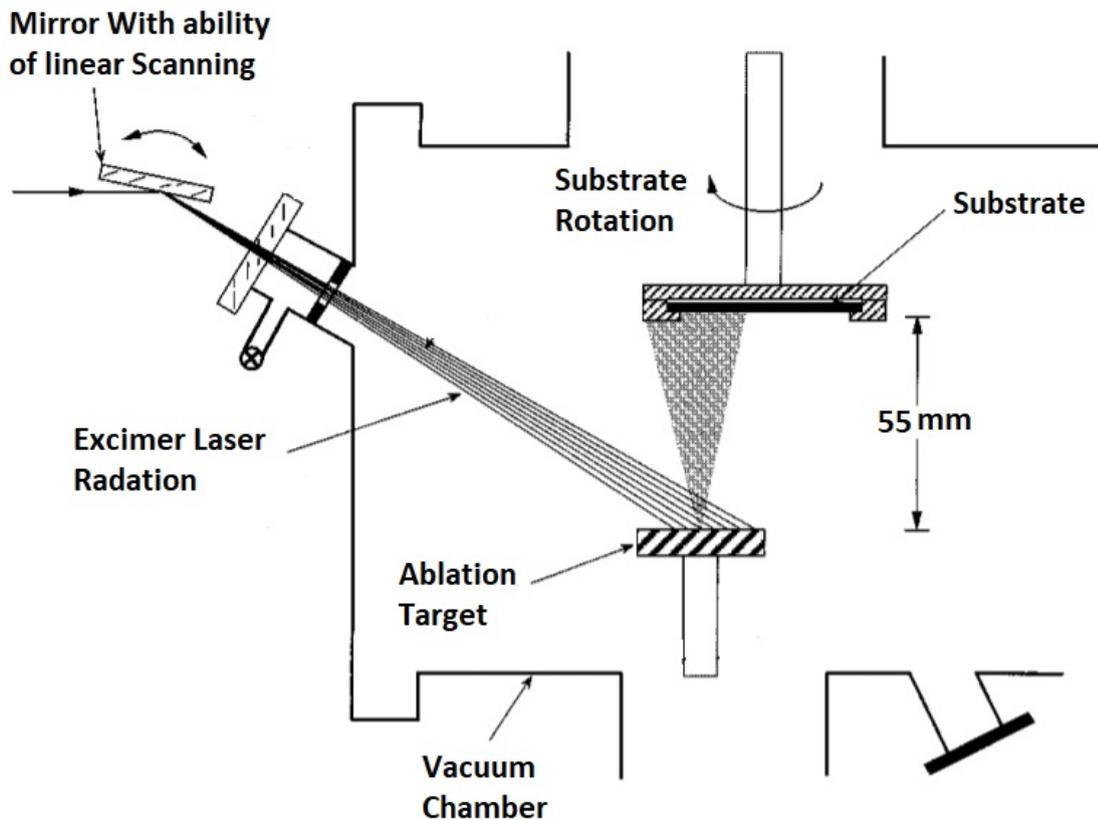


Figure 3-1 - Schematic diagram of large area PLD (source: Greer, J. A., and M. D. Tabat)

When I was involved in the investigation of the deposition, deposition recipes were going to be finalized. Challenges for tuning the parameters of deposition such as temperature, process pressure, and laser fluence and laser spot size on the target were in final step, therefore I did some more deposition as a proof of concept. In our PLD, the mirror is fixed and substrate is not capable of rotation, however target can rotate. In chapter 4, it is shown that explored recipes yielded expected outcomes regarding crystalline structure, and surface morphology.

## 3.2 ATOMIC FORCE MICROSCOPY – AFM

Sources of this section are: [68], [69] and [70]

Atomic Force Microscopy (AFM) is a member of method families known as Scanning Probe Microscopy (SPM). It demonstrates a resolution in the range of fraction of Nanometer (up to 0.1 nm) in vertical direction. Lateral resolution is in the range of ~30 nm. Information of the surface is gathered by means of a mechanical probe named tip. A typical AFM, has three major abilities: Force measurement, Imaging and Manipulation. AFM operational modes are: Contact mode, Non-contact mode and tapping mode. I applied standard tapping mode in air for imaging the surfaces of the samples fabricated with PLD with driving the cantilever at resonance frequency and close to the surface such that the repulsive forces dominate over the attractive interactions.

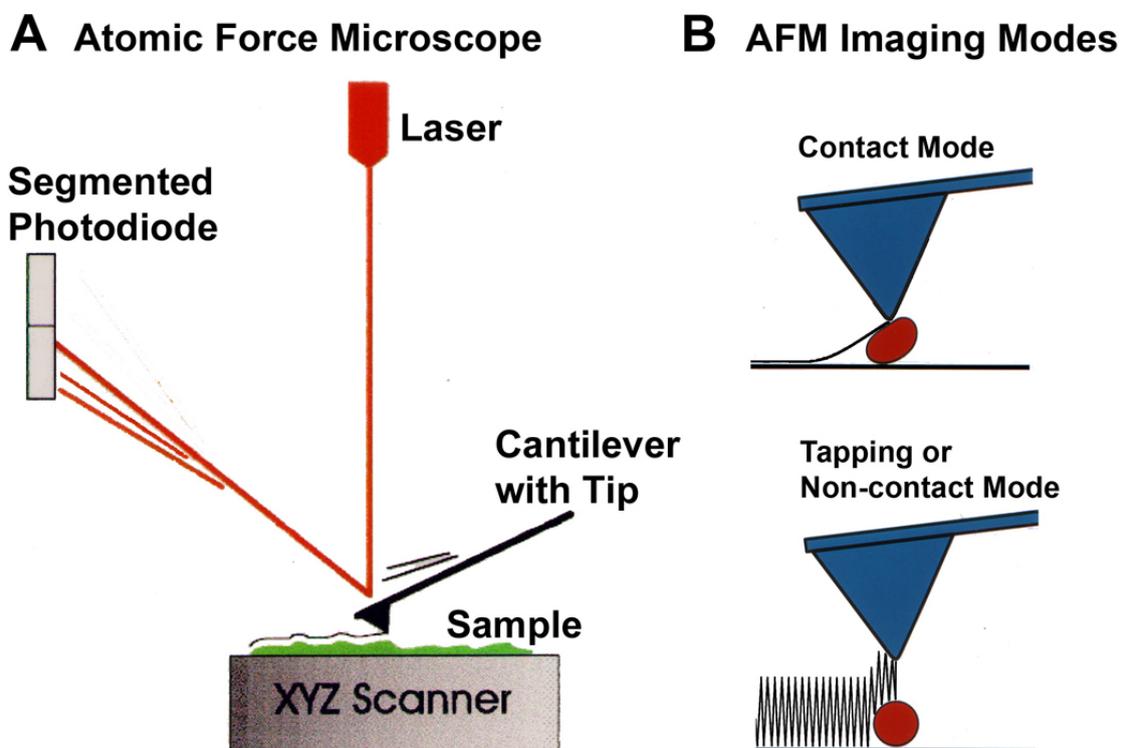


Figure 3-2 – (A) typical configuration of an AFM. Cantilever, Tip (Fixed to open end of a cantilever, acts as the probe), Detector of deflection and motion of the cantilever (Segmented Photodiode), Sample to be measured by AFM, xyz scanner (moves sample and stage in x, y, and z directions with respect to a tip apex), and (B) Two imaging modes (Contact & Non-contact) are shown.

As Ferroelectrics are a subclass of Piezo-electrics, in order to image and manipulate ferroelectric domains in PLD-fabricated samples, Piezo-response Force Microscopy (PFM) has been used. This method is described in consequent section.

### 3.2.1 PIEZO-RESPONSE FORCE MICROSCOPY - PFM

Piezo-response force microscopy (PFM) is a variant of AFM by which, one can manipulate and image the domains of piezo-electric/ferroelectric materials. By bringing a sharp conductive tip into contact with the surface, and applying alternative voltage (current) to the tip, deformation of the surface due to converse piezo-electric effect, will result to the measurement of piezo-electric response.

The bottom electrode beneath the Ferroelectric layer, needed to be electrically connected to the sample stage of AFM to allow the PFM measurement, therefore, silver glue was used on the back and edges of the sample to stick it to a conductive plate which makes the desired electrical connection to the stage.

By applying simultaneously a bias voltage (DC) and a probing bias (AC), Ferroelectric domains are aligned due to DC voltage and are manipulated at specific frequency by AC voltage. This approach results to observation of behavior of domains and measure the piezoelectric resonance via tip deflection. By means of a locked-in amplifier irrelevant frequencies are filtered. Tip reflection is transferred to photodiode via the deflection of the laser and can be used to calculate piezoelectric properties of the sample. Meanwhile, by swapping DC voltage between  $\pm v$ , phase measurement of domains reveals the hysteresis loop.

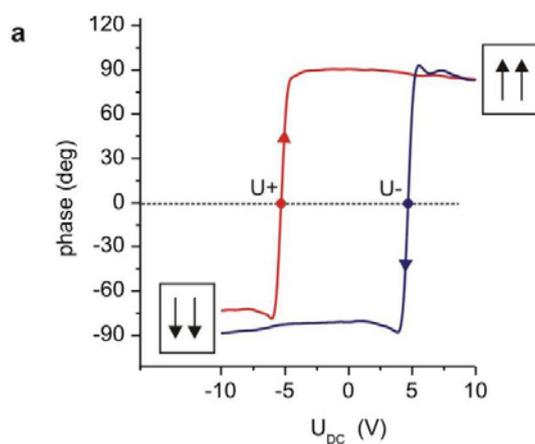


Figure 3-3 - Typical hysteresis loop (source: mentioned at the beginning of this section)

#### 3.2.1.1 Sweep resonance frequency

Source of this section is:[71]

Sweep is a feature of PFM measurement which allows user to find the contact resonance frequency and set the scanning frequency in the neighborhood to boost the piezo-response signals.

The ferroelectric layer must be very thin to maintain the fundamental phenomenon of tunneling effect. Due to this, if high electric fields are applied to tip, it might change the morphology of the surface which in consequence, distorts the imaging data measured by the device. To have better indication of Ferroelectric properties, AFM imaging in contact mode, beforehand the PFM imaging can help to compare the results and eliminate the effects of high voltage application to the surface.

### 3.3 X-RAY DIFFRACTION - XRD

*This section is based on the materials from "MIT Center for Materials Science and Engineering". [72]*

X-ray diffraction (XRD) is a technique to analyzing the structure of a material from the scattering pattern produced when a beam of X-rays interacts with it. High Resolution X-Ray Diffraction (HRXRD) and X-Ray Refraction (XRR) methods are different sub techniques used to study and characterize thin films. While former is used to measure structural information and defects, the latter usually used to measure thickness, surface roughness and density of topmost layer. HRXRD measures scattered X-Ray intensity as a function of  $\omega$  and  $2\theta$ . Below picture shows a typical set up of a diffractometer:

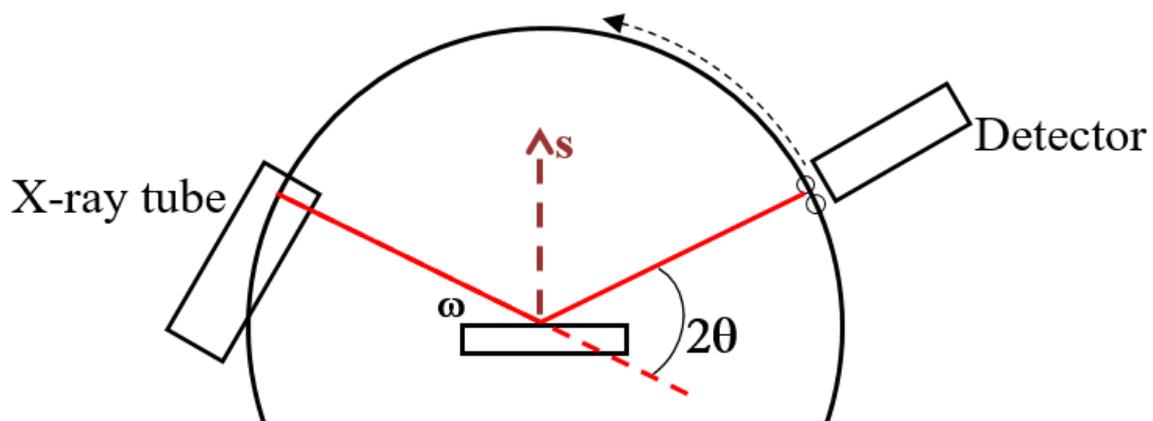


Figure 3-4 General setup of an X-Ray diffractometer (source: link mentioned in the beginning of this section)

$2\theta$  (Diffracted angle): angle between incident beam and detector,

$\omega$  (Incident angle): angle between sample surface and X-Ray Source

Incident X-Ray beam is scattered in different directions, however in a crystalline form, coherent scattering of X-Ray in different angles, produce peaks in a typical diffraction pattern

like the one below. Each material has its own unique pattern named Powder Diffraction File (PDF). In simplistic model, Bragg's law determines the condition for maximum constructive diffraction.

$$\lambda = 2d_{hkl} \sin \Theta_B$$

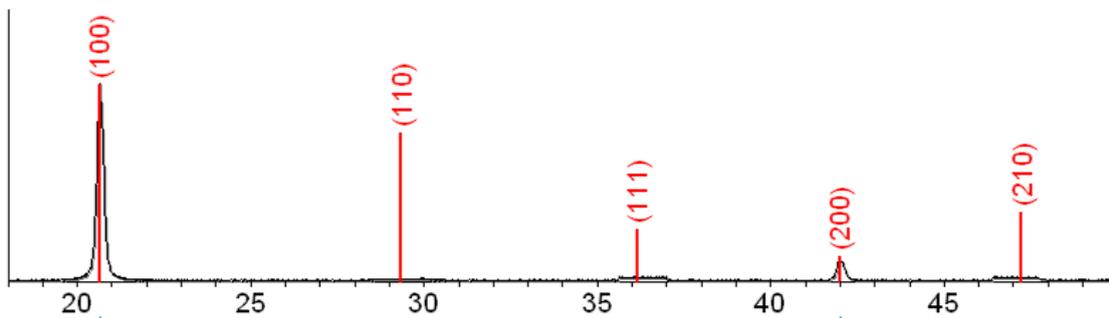
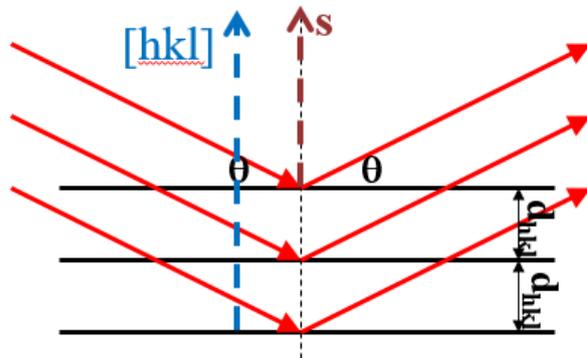


Figure 3-5 Diffraction pattern (counts vs 2Theta angle) for a typical material – Coupled scan mode (source mentioned at the beginning of this section)

Three types of scans which is done within this project, by means of X-Ray Diffractometer are:

- A **Coupled Scan** is a plot of scattered X-ray intensity vs  $2\theta$ , but  $\omega$  also changes in a way that is linked to  $2\theta$  so that  $\omega = \frac{1}{2} * 2\theta + \text{offset}$ . In this way, scattering vector is always perpendicular to the sample surface.

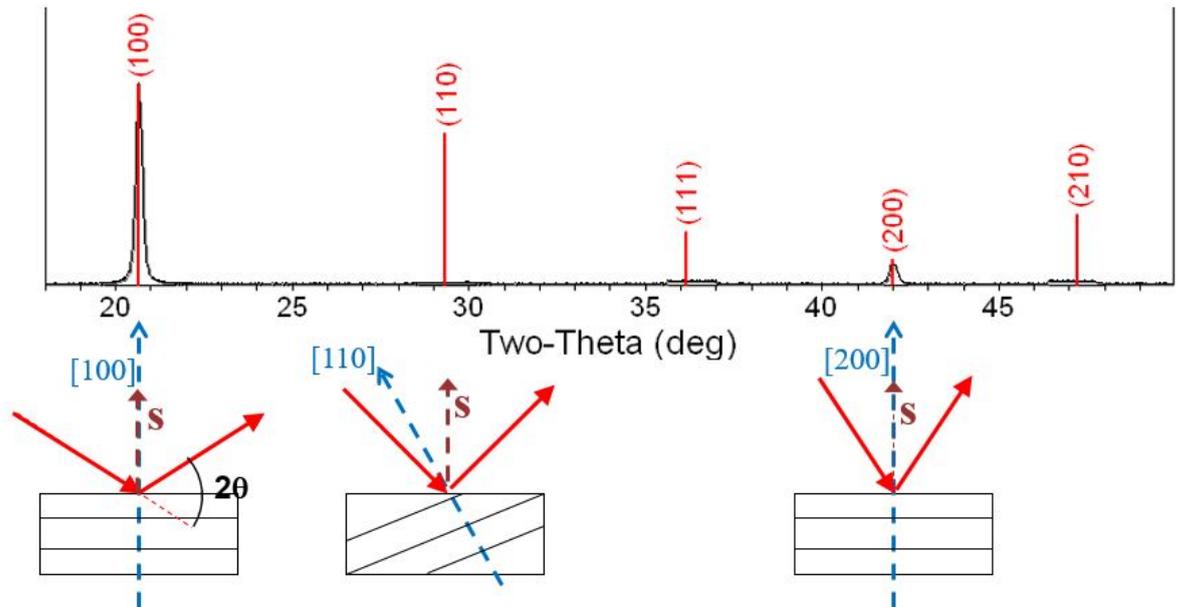


Figure 3-6 (Left) “At  $20.6^\circ 2\theta$ , Bragg’s law fulfilled for the (100) planes, producing a diffraction peak”. (Middle) “The (110) planes would diffract at  $29.3^\circ 2\theta$ ; however, they are not properly aligned to produce a diffraction peak (the perpendicular to those planes does not bisect the incident and diffracted beams). Only background is observed.” And (right) the (200) “planes are parallel to the (100) planes. Therefore, they also diffract for this crystal. Since  $d_{200}$  is  $\frac{1}{2} d_{100}$ , they appear at  $42^\circ 2\theta$ ” (source is mentioned at the beginning of this section)

Usually a coupled scan is used to measure lattice mismatch, ternary composition, relaxation, thickness and super-lattice period. Our main goal was to determine the ternary composition of our stack.

- A **Rocking Curve** or  $\omega$  scan, is a plot of X-ray intensity vs  $\omega$ . It is usually used to study defects like dislocation, density, mosaic spread, curvature, disorientation and inhomogeneity. In this method, detector is set to a specific Bragg’s angle and sample is tilted. By this way, intensities from plans which are not perfectly parallel are observed and widen the peak. Full Width at Half Maximum (FWHM), is the standard indication for quality of thin-films. Smaller FWHM indicates better thin films. I used it to measure the quality of the layers in our samples.
- **Reciprocal Space Map** provide the most complete amount of information and are necessary for the analysis of strained films however, it usually takes longer time. It consists of a set of continuous coupled scans for a range of tilts. In this way, for each tilt, a coupled scan is done and the peaks are revealed, then by collecting all the peaks from epi-layers, one can analyze strain in multi-layer thin-films. This is because strain

shifts the reciprocal lattice points, preventing the collection of data with a single coupled scan (image below).

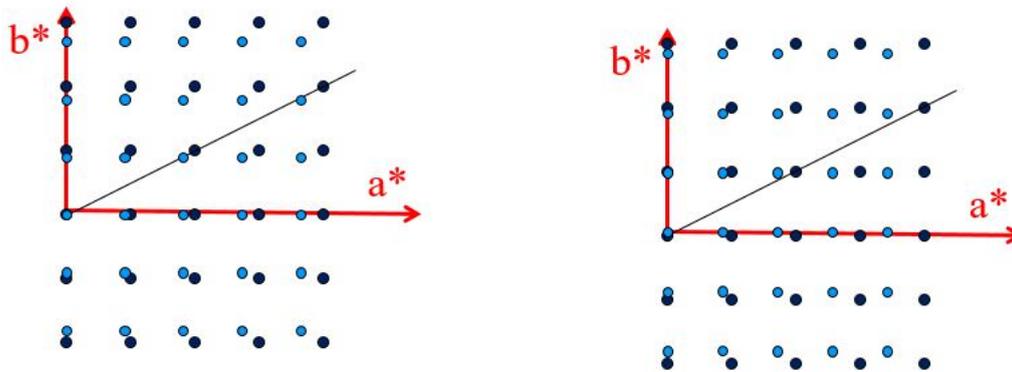


Figure 3-7 - Effects such as strain will shift reciprocal lattice points, preventing the collection of data with a single scan (source is mentioned at the beginning of this section)

- **X-Ray Reflectivity** can give information on Thickness, interface roughness, and composition or density. XRR works with non-epitaxial and even non-crystalline thin films.

## 3.4 UV LITHOGRAPHY

*This section is based on the materials from “Semiconductor Lithography from [lithoguru.com](http://lithoguru.com) site”*

UV lithography, also termed as photolithography or optical lithography is a microfabrication process to pattern part of the thin-film or a bulk of substrate. A light sensitive polymer called photoresist is exposed to UV light and then developed to pattern a 3D relief image on the substrate. In principal, UV lithography consists of following steps. Please note that mostly the general mechanisms of UV lithography are mentioned here, for the specific information in our experiments like resists type, exposure machine and development process, please refer to chapter 4 section 4.2.1.2.

### 3.4.1 SUBSTRATE PREPARATION

This step is intended to improve the adhesion of photoresist to the substrate by substrate cleaning, dehydration bake and addition of adhesion promoter. Heating to certain temperatures (150°) prevents aqueous layer between sample and photoresist and adding adhesion promoter results to better adhesion between sample and photoresist.

In our experiments, samples had to be cleaned before introduction to cleanroom processes and after the PLD deposition process. Main contaminations were silver glue on the back of the sample which was used to adhere the sample to the heater stage of the PLD. Specific Investigation and experimental efforts to find an effective and non-invasive method yielded that grinding back of the sample with care and putting it in acetone and afterward in ethanol, could remove silver contaminations as well as other unwanted contaminations. Samples were already heated in PLD chambers during annealing procedure and cleaning was already done in cleaning phase.

### **3.4.2 PHOTORESIST COATING & PREBAKE**

Simple process of spin coating can establish a thin, uniform coating of photoresist with a desired thickness. A viscous, liquid solution photoresist material is dispensed onto the sample and to produce a uniform thick layer, sample is spun with a controlled velocity. Stringent requirements for speed, uniformity of coating and thickness should be met. Therefore a set of parameters should be controlled during the process as well as before the process start. Volume and properties of the resist like viscosity and solvent composition are among them. Typically speed is around 1200 to 1400 rpm for a duration of 30 to 60. Fluid mechanics and the phenomenological models can be used to describe the physics behind the spin coating process, however variation of uniformity and thickness of the resist with process parameters should be obtained experimentally. To drive off the photoresist solvent, the covered sample is pre-baked at specific temperatures (90° to 100°) for certain time (30 to 60 seconds). This is mainly done to stabilize the resist film.

### **3.4.3 EXPOSURE, DEVELOPING & POST-BAKE**

Desired pattern is printed (exposed) to the photoresist layer via exposure of intense UV light through a master pattern named mask, by means of a device named Lithography exposure (KARL SUSS MA56 Mask Aligner in our case). Exposure can be done in contact or proximity mode. Solubility of the resist in the developer is changed upon exposure to light in a way that parts exposed to light, become removable by developer (Positive resist). Those parts of the sample whose photoresist on-top is removed and are not anymore protected by photoresist, are etched by a wet chemical solution or by dry plasma etching technique. As wet etching is an isotropic type, usually used in cases when the area to be etched is bigger in width compared to

the etch depth. The post-bake is used to harden the resist in a way that it will withstand the harsh environments of further processing.

### 3.4.4 PHOTORESIST STRIP (LIFT-OFF)

To remove the unwanted photoresist as well as the material on-top of it, after etching, a process named lift-off is applied. By using resist stripper resist is chemically changed in a way that no longer adhere to the substrate. Acetone is the most common stripper however as it tends to leave residues on the samples, it is used with combination of IPA.

## 3.5 SPUTTER DEPOSITION

*This section is based on the materials from [73] and [74]*

Sputtering is a physical vapor deposition (PVD) and a member of thin-film deposition family techniques. Deposition thickness varies from angstroms to microns and can be a single or multiple material coating. Solar cells, optical components and semiconductor wafers are just a few possible substrates that can be used in sputtering. Targets can be pure atomic materials like metals as well as molecules such as oxides and Nitrides.

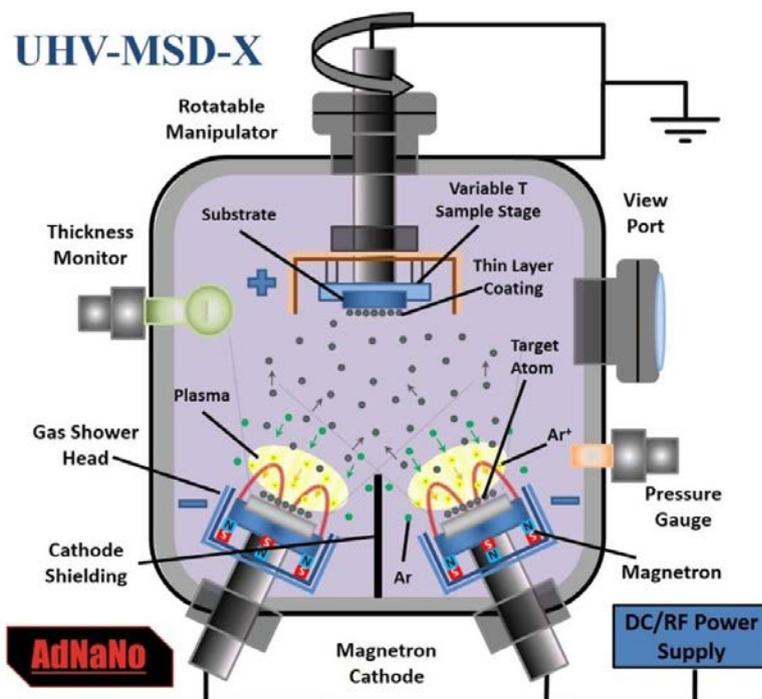


Figure 3-8 - Magnetron Sputtering (co-deposition) in action (source mentioned at the beginning of this section)

A chemically inert gas, which is called process gas and is usually Argon, is introduced into evacuated chamber while cathode is electrically energized to establish a Plasma. Process gas is chosen based on the material which is being to be deposited. Outermost surface of cathode is covered with a slab of target material whereas substrate is connected to anode. Inside plasma, gas atoms lose electron and become positive ions. Ions are accelerated to cathode and strike the target with sufficient energy to dislodge atoms and molecules of target material and sputter them, a kind of atomic level bead blasting process. In consequence, sputtered material traverse the chamber to hit the substrate surface and stick to it as a coating or a thin-film layer. To avoid overheating of substrate due to bombardment by free electrons and to speed up the sputter rate, magnetic fields can be used in cathode to control the speed and direction of electrons as well as Ions. This kind of sputter machine is called Magnetron sputtering.

Sputter system used in this thesis is a Magnetron Sputtering Deposition (MSD) with specific features described in chapter 4. Desired thickness in nanometer scale is achievable by first monitoring and then controlling the time of deposition. Tables for thickness is available in MESA+ cleanroom. In section [4.2.2](#), I have described how sputter machine in MESA+ cleanroom is used to deposit electrodes on top of our samples.

## 3.6 E-BEAM LITHOGRAPHY

*This section is based on the materials from [75] and [76].*

**Electron beam lithography** (e-beam lithography) is a lithography technique in which a beam of electrons is accelerated to hit and write a specific pattern, down to sub-10 nm, on the resist coated substrate. Solubility of the resist is changed by the electron beam and enables selective removal of either the exposed or non-exposed regions of the resist by developing it in a developer. There are two types of e-beam lithography systems, scanning system and projection system. In scanning system electron beam is controlled by a computer in accordance to a pattern so, there is no need for a mask or template. Projection system is not mentioned here as in this thesis, a scanning e-beam is used.

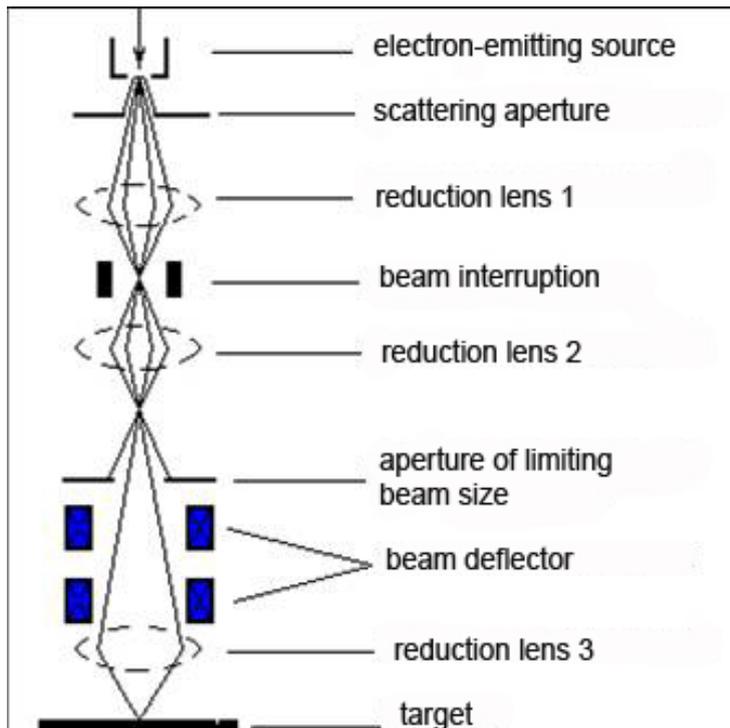


Figure 3-9 - Scanning electron-beam lithography system (source is mentioned at the beginning of this section)

Main advantage of e-beam lithography is the high resolution of sub-10 nm. However the throughput of the technique is quite low due to direct writing which limits the applications for photomask fabrication and research and development.

“Write field” is the area than can be written by e-beam without changing the position of the stage, ranging from  $\sim 10 \mu\text{m}$  to 1-2 mm. If the pattern is bigger than write field, stage should move one field size ahead which might causes some overlaps or discontinuities which is known as stitching error problem. This effect can be reduced to nanometer scale precision, by using laser interferometry stage position system.

Electron scattering in the resist cause issue of difference between width of digital line in the pattern and the actual developed feature size. This difference is usually a fixed value called bios and can be considered while pattern is designed to eliminate the issue.

“Proximity effect” is the issue associated with scattering and back-scattering of electrons in resist. This can result in undesired exposure of the resist in regions adjacent to the primary incident beam and becomes vital especially in layouts with high features density. Proximity effect results to rounding of the corners in the pattern, modification of gap spacing and linewidth, and merging or elimination of specific feature.

I have fully described how E-Beam lithography machine in MESA+ cleanroom has been used to transfer the required pattern to the surface of our samples, in chapter 4, section [4.2.1](#).

# 4

## FABRICATION

In this chapter, I will discuss specific details for the fabrication processes done with PLD as well as cleanroom processes. Here the way that the experiments were done is contextualized. In avoid to make chapter 5 very thick, here very general aspects of what has been done during deposition and cleanroom fabrication, is presented. Whenever needed in chapter 5, there is a reference to this chapter.

Deposition of perovskites on perovskites substrates are well studied in IMS group however as mentioned before, new challenge was to grow perovskites on top of a silicon based substrates. Meanwhile, cleanroom processes for shaping the deposited stack and fabricate an early-stage device was another challenge. The main challenge was to first explore the suitable method for lithography and sputtering and then process the samples and investigate the ferroelectric properties afterward.

### 4.1 DEPOSITION

Here I will discuss preparation process for different layers of samples, respective fabrication details and challenges.

#### 4.1.1 SUBSTRATE

ULPEC member at IBM Research Zurich achieved to grow strontium Titanate ( $SrTiO_3$ ) on silicon by molecular beam epitaxy. These are the silicon-substrate samples which we investigated first. Front side of the samples were covered with resist to protect the BTO layer during transport. Based on an exploratory work already done by Yorick A. Birkholzer in his master thesis, in order to remove resist and prepare samples for deposition, different solvents, acids and bases as well as ozone and oxygen plasma treatment were tried. Finally acetone and isopropanol achieved to remove residue traces of resist. Annealing the substrate in reported temperature can yield a very smooth surface.

#### 4.1.2 BOTTOM ELECTRODE

LNO is a pseudo-cubic perovskite structure with a lattice parameter of 3.84 Å. The resistivity is isotropic and low, and the temperature dependence ( $\frac{dr}{dt}$ ) reveals a good metallic behavior [Guo et al]. Recent investigation on growth of ferroelectric thin films such as BaTiO<sub>3</sub>, PZT and PLZT on LNO substrates have been reported by Guo et al. He has measured the resistivity versus temperature of a LNO thin film deposited at 700 °C in 35 Pa oxygen for the interval of 50 K to 300 K, by dipping in liquid nitrogen. The result curve is quite similar to normal metals. Meanwhile *SrRuO<sub>3</sub>* is the first perovskite superconductor that did not contain copper. It is metallic and often used as the electrode for the Lead zirconate Titanate (PZT) devices. It has been studied vastly in IMS group. Due to these properties, it was selected as the first candidate for bottom electrode for *SrTiO<sub>3</sub>*-substrate approach. On the other hand, *LaNiO<sub>3</sub>* was chosen as the bottom electrode for the silicon-based substrates.

Following deposition parameters emerged to be the de facto standard for growing *SrRuO<sub>3</sub>* and *LaNiO<sub>3</sub>*.

*LaNiO<sub>3</sub>*: 600° C, 1.9 J/cm<sup>2</sup> Laser energy density, 0.04 mbar oxygen gas pressure, 2 Hz laser repetition frequency.

*SrRuO<sub>3</sub>*: 600° C, 2.5 J/cm<sup>2</sup> Laser energy density, 0.13 mbar oxygen gas pressure, 4 Hz laser repetition frequency.

Applying these parameters, samples were fabricated with expected results regarding surface morphology and crystalline quality. Meanwhile following considerations were taken into account in order to achieve better results.

- Prior to every two or three deposition or if the target for deposition is changed, the targets are pre-ablated in a true background pressure (like 0.01 mbar) in oxygen. It is recommended for having a smooth homogenous target surface which leads to near ideal deposition conditions.
- As it was necessary to attach the small samples on heater stage, silver glue was used to prevent evaporation in vacuum during deposition.
- Laser energy was measured before and after the deposition to be recorded to see if the laser was stable during deposition.

Above considerations also apply for growth of Ferroelectric layer which will be discussed next.

### 4.1.3 FERROELECTRIC LAYER

$BaTiO_3$  is already introduced in chapter [2.2.2](#).  $BaTiO_3$  is the first ferroelectric oxide with a perovskite structure to be discovered [48]. Liang et al has reported  $BaTiO_3$  biaxial compressive stress grown on top of  $LaNiO_3$  and tensile stress for  $LaNiO_3$ . By setting the following parameters for  $BaTiO_3$  growth on  $LaNiO_3$  and  $SrRuO_3$  respectively, promising results emerged regarding crystalline structure and surface morphology. Quality of results are discussed in chapter 5.

$BaTiO_3$  on  $LaNiO_3$ :  $700^\circ C$ ,  $1.9 J/cm^2$  Laser energy density, 0.02 mbar oxygen gas pressure, 2 Hz laser repetition frequency.

$BaTiO_3$  on  $SrRuO_3$  :  $700^\circ C$ ,  $1.9 J/cm^2$  Laser energy density, 0.02 mbar oxygen gas pressure, 2 Hz laser repetition frequency.

In literature, there was no reference for the growth parameters of PLD for  $BaTiO_3$  on  $LaNiO_3$  and  $BaTiO_3$  on  $SrRuO_3$ .

## 4.2 CLEANROOM SHAPING

### 4.2.1 LITHOGRAPHY

#### 4.2.1.1 E-Beam

E-Beam lithography is one of the most precise lithography methods. Therefore it is used in microelectronic industry to create fine patterns ranging from  $>10$  nm. As I have shown in sections [5-2-1](#) and [5-2-2](#), e-beam made features ranging from  $>25$  nm to 1.4 microns to have different pattern-sized circles and squares as prospective top electrode forms.

After experiencing UV lithography with some samples, E-Beam lithography was chosen as the main method to shape our samples due to two main reasons. First, it is needed to create patterns in  $>10$  nm range which is not feasible with UV lithography and second, developing and stripping substances used in this method are the chemicals which had been tested already for the substrate preparation and cleaning samples, to wit, Acetone, ethanol and isopropanol. As aforementioned chemical substances proved to be harmless to our stack of grown materials, e-beam lithography process could be done without making damage to our samples. This is why we did not use other patterning processes like FIB or dry etching techniques which had the risk to attack our samples. Meanwhile using dry etching techniques need new exploratory works to find out the side effects and compatibility and consistency of the process to our materials which

was beyond the time scope of this thesis. However it can be taken as an alternative method into account.

I used positive resist PMMA (poly-methyl methacrylate) with trade name of *NANO<sup>TM</sup>* 950PMMA Series Resists in Chlorobenzene Positive Radiation Sensitive Resists from MicroChem corp. Two spin coating curves are shown in figure 4-1. Details about the curves can be find [here](#).

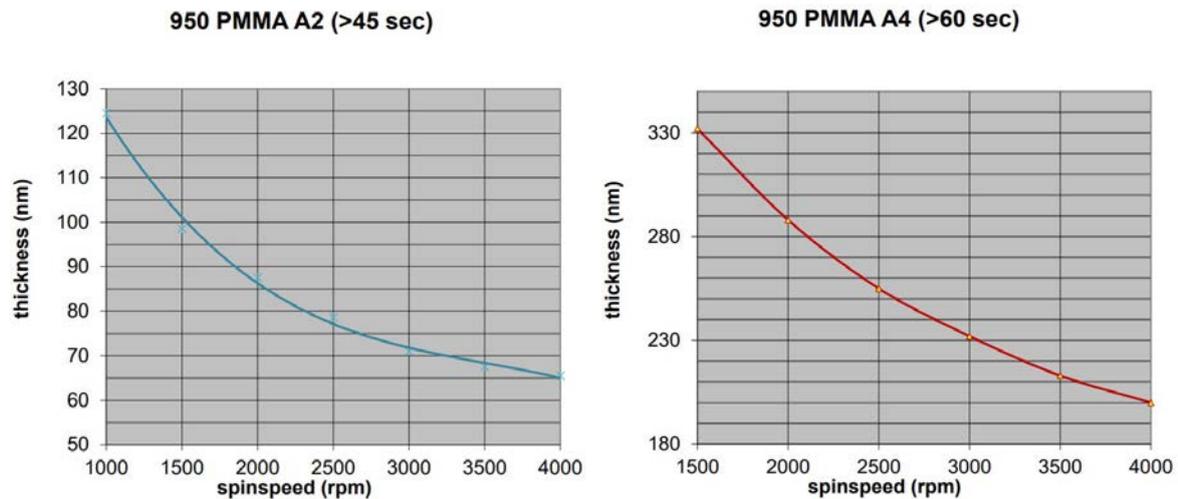


Figure 4-1 Spin Speed Curves, picture taken from MIS site:

[https://mesaplusnanolab.ewi.utwente.nl/mis/generalinfo/downloads/usermanuals/96/PMMA\\_spin-curve\\_A2.pdf](https://mesaplusnanolab.ewi.utwente.nl/mis/generalinfo/downloads/usermanuals/96/PMMA_spin-curve_A2.pdf)

Layer processed in this thesis is shown in a simple form in figure 4-2. In our case, spin coating was done with either of following parameters:

- Spinning 950 PMMA A2 (2% PMMA in anisole) at 1500rpm for 45 seconds resulted thickness of 100nm.
- Spinning 950 PMMA A4 (4% PMMA in anisole) at 4000rpm for 60 seconds resulting thickness of 200nm.

MicroChem PMMA resists produce low defect coatings over a broad range of film thicknesses. We used MIBK:IPA 1:3 in 40 seconds for developing and Nitrogen gas for drying. MIBK is the solvent and active ingredient, which controls the solubility and swelling of the resist. Afterward we avoided post-baking due to the fact that resist would reflow above 120°C and destroy our pattern. Meanwhile I was assured that internal temperature of the sputtering machine would not exceed above 120°C which later on revealed to be less than 50°C. The only bake done was the bake after spinning in order to remove the solvent, this is done at 160 degrees for 2 minutes.

E-Beam exposure was done by “RAITH150TWO System” which is a high resolution Electron Beam Lithography system manufactured by “RAITH Nanofabrication” company. It is capable of handling samples from few mm to 8 inches wafers to pattern sub 8 nm features. It also works in low KV and has imaging capability like SEM. Meanwhile it is armed with thermo-stabilization system. The pattern wrote on the samples are presented in chapter 5 and discussed in chapter 6.

In develop process, PMMA resists are compatible with immersion (21° C), spray puddle, and spray process modes. Process variables such as soft bake, exposure conditions, choice of resist and developer should be optimized to achieve desired results. Development was done by Acetone in ultrasonic bath, rinsing with IPA and drying with Nitrogen gas.

Samples now were ready for deposition of metals to build electrodes and liftoff to strip resist and complete the process. I will explain the details in next section.

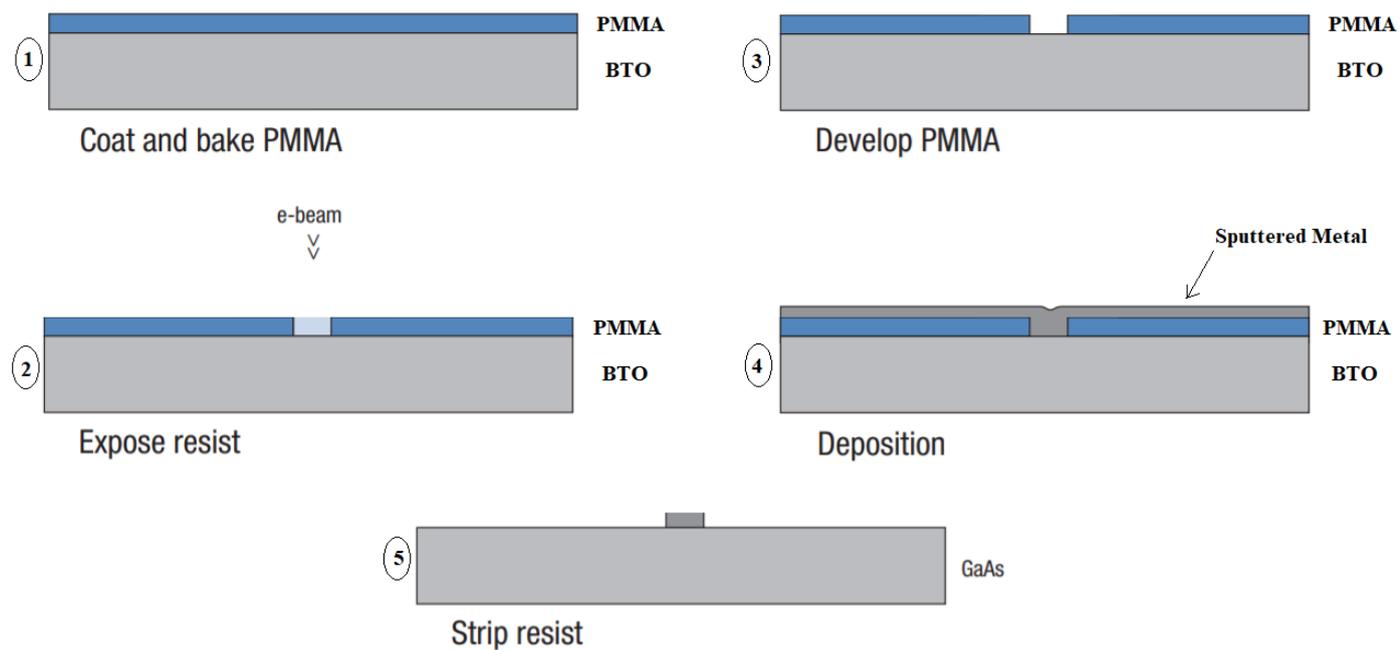


Figure 4-2 layer process including (1) spin coating, (2) exposure, (3) develop resist, (4) sputtering and (5) liftoff. Picture adapted from MIS site:

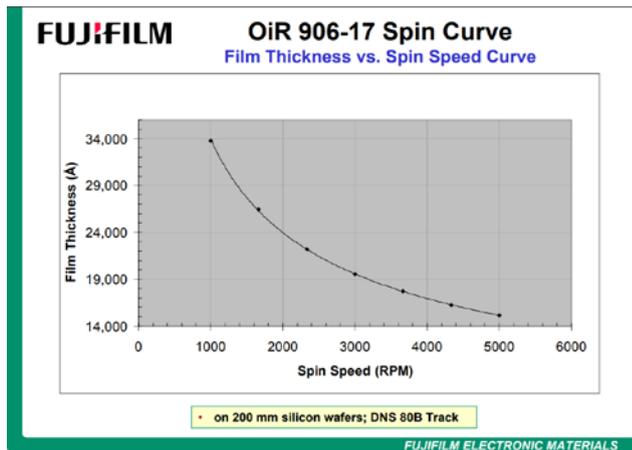
[https://mesaplusnanolab.ewi.utwente.nl/mis/generalinfo/downloads/usermanuals/96/PMMA\\_Data\\_Sheet.pdf](https://mesaplusnanolab.ewi.utwente.nl/mis/generalinfo/downloads/usermanuals/96/PMMA_Data_Sheet.pdf)

#### 4.2.1.2 UV

UV lithography principals have been given in chapter 3. Here ultra-violet beam is exposed to the resist instead of beam of electrons. Therefore resist is also different due to chemical reactions needed when exposed to the UV light. We used Olin resist with available properties

and spin speed curves like PMMA. Exposure is done with the exposure machine named “KARL SUSS MA56 Mask Aligner” [51]. Capabilities of the machine as well as details about supported wafer sizes and embedded microscope can be found in the MESA+ web site.

Applied resist is Olin 907-12 which coats sample with a layer of 1.2  $\mu\text{m}$  thick when spins at the speed of 4000 rpm for 45 sec. Bake time after spin coating was 1 minute at 90°C. Exposure time was 7 sec at 10mW/cm<sup>2</sup>. There was no post bake and development process was done within 1 minute in OPD 4262.



## 4.2.2 SPUTTERING

“Sputterke” machine in MESA+ cleanroom was used for deposition of cobalt and gold on samples with already processed with e-beam and UV lithography systems. It is a UT manufactured sputter machine with 3 guns to enabling 3 different metals to be sputtered in a single run. It is equipped with Argon mass flow controller and two Pirani and Penning vacuum gauges. Gauges enable the machine to measure fore-line rotary pump pressure as well as base vacuum pressure associated with turbo-molecular pump. Operation of the machine is straightforward and by controlling the shutter, one can deposit up to 3 different metals. Power of the guns and Argon flow are usually set to 200 Watt and 140~145 sccm (Standard Cubic Centimeters per Minute). It is equipped with a load-lock which can introduce sample to the reactor without breaking the reactor vacuum.

For the stabilization of the sputtering process, usually first 1 minute of the sputter time is done with closed shutter. Therefore, one needs to add 1 min extra for what has been calculated for desired thickness. Thickness vs deposition time has been calculated for different metals and is available as a table. In my case, I deposited first 10 nm of cobalt straight to the BTO layer and

then 50 nm of Gold on top of it. Based on ULPEC collaborator experience, cobalt has better adhesion to BTO and therefore was chosen as the bottom layer of electrode. Calculated times for these two metals are shown below inside the log system of the machine.

Layer	Gun(H:M:S)		Argon Pressure DC				Time		Argon Pressure DC				Time	Aim	Measured	
							[W]	[m:s]					[W]	[m:s]	[nm]	[nm]
1	Co*	Pre	142.5	0.0066	200.0	1:00		Sputtering	142.5	0.0066	200.0	1:20	10.0	0.0		
2	Au+	Pre	142.5	0.0066	200.0	1:00		Sputtering	142.5	0.0066	200.0	2:09	50.0	0.0		

*Calculated sputter time to achieve desired thickness*

*Thickness*

Thickness of the whole electrode was measured with AFM and presented in chapter 5. It conforms to the expected value (60 nm).

# 5

## RESULTS

This chapter summarizes fabrication and characterization results and presents associated key-findings. To enable the comparison of our ferroelectric devices on silicon, parallel to the silicon-substrate samples, growing of samples based on STO-substrates started to build a benchmark system. In fact,  $LaNiO_3$  and  $BaTiO_3$  layers were grown on top of STO buffered Silicon substrates in parallel to growing of  $SrRuO_3/LaNiO_3$  and  $BaTiO_3$  on single crystal of STO (STO/LNO/BTO and STO/SRO/BTO layers). Results of the aforementioned “benchmark system” are presented and discussed first. Then, results from the Silicon substrates are shown. Based on benchmark results, one can get insights into origin of non-ferroelectricity in silicon samples by comparing two sets and looking into differences.

Results from structural characterization (RHEED, AFM & XRD) and functional characterization (PFM) are presented here. Results of single crystal growth as well as Si-based samples are shown in section 5-1. RHEED patterns and AFM images check required quality for the surface of thin films. XRD measurements help us for the crystalline quality and strain calculation in films. The latter is the key factor for stabilization of ferroelectricity in BTO layer and therefore play a vital role. In section 5.2 results of cleanroom processes for both categories are summarized. In section 5.3 a comparative discussion for the results of sections 5.1 and 5.2 are presented respectively.

### 5.1 DEPOSITION

#### 5.1.1 GROWTH ON SINGLE CRYSTAL STO (001) SUBSTRATE

Monolithically growth of all-perovskites LNO/BTO and SRO/BTO hetero-structures on single crystal STO (001) layer are presented and highlighted. BTO film in both hetero-structures are epitaxial with low surface roughness and ferroelectric property. Results of this section build a benchmark for growth of BTO on silicon.

Figure 5-1 shows the stack of layers which were grown on top of the single crystal STO (001). Substrates have a thickness of  $500\mu\text{m}$ .

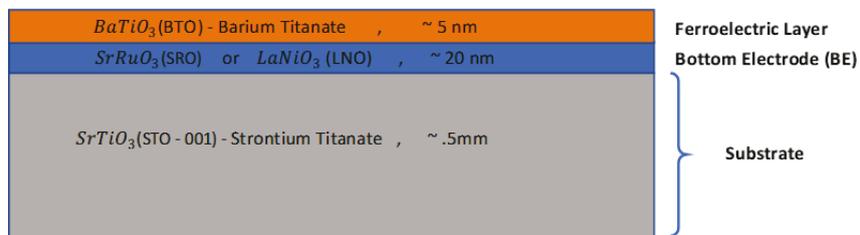
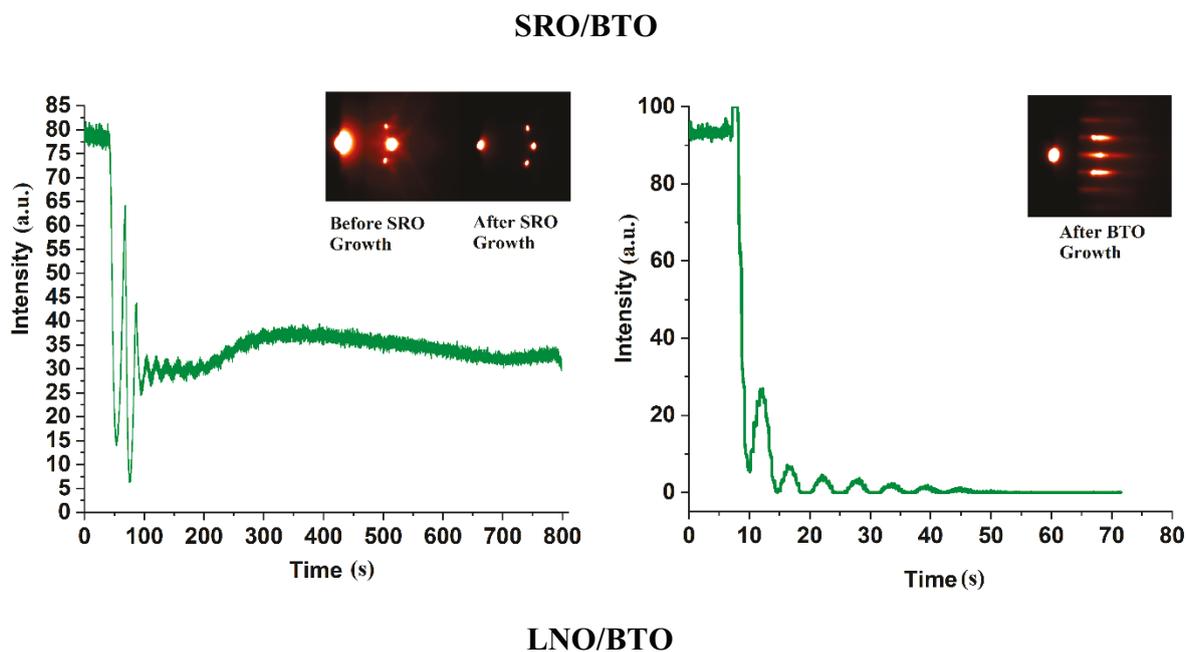


Figure 5-1 Schema of the layers in STO-substrate samples with respective thickness.  $\text{BaTiO}_3$  has thickness of  $5\text{ nm}$  which is above the reported critical thickness in literature ( $t_c \sim 2.4\text{ nm}$ , source [Lee et al]).

Figure 5-2 shows RHEED pattern recorded *in situ* during the growth of SRO and LNO on BTO. In SRO/BTO stack, SRO was grown in pressure of  $0.13\text{ mbar}$  at  $650^\circ\text{C}$  and BTO in pressure of  $0.02\text{ mbar}$  at  $700^\circ\text{C}$  but both with the same laser spot size of  $1.768\text{ mm}^2$ . LNO was grown in  $0.04\text{ mbar}$  and BTO in  $0.02\text{ mbar}$  both at  $700^\circ\text{C}$ . Deposition parameters were varied in individual PLD tries and grown samples were characterized afterward. Eventually a set of optimized parameters were established in which expected surface morphology and crystalline quality were observed. Here the results for optimized deposition parameters are presented.



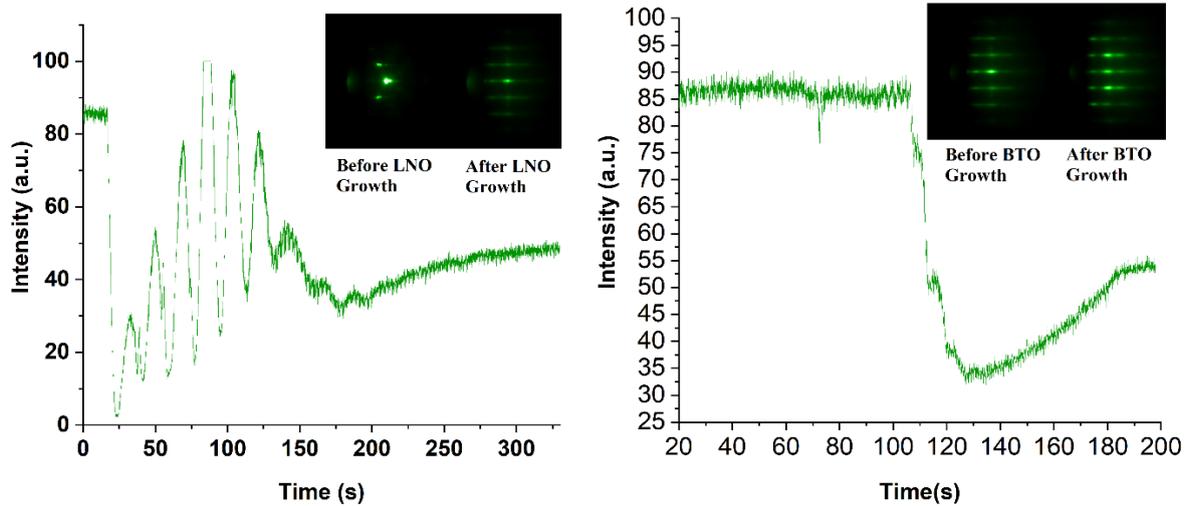


Figure 5-2 RHEED pattern of (top) SRO/ BTO and (bottom) LNO/BTO growth as well as evolution of intensity for specular RHEED spot during deposition of hetero-structure. Number of oscillations indicate number of grown unit cells.

In SRO growth, intensity shift is from the specular spot towards the two first order side spots upon termination inversion (see [Koster et al](#)). SRO pattern indicates flat single crystalline surface as all diffraction spots have the same intensity and are on the Laue zones.

The BTO RHEED patterns in both stacks are streaky, signaling an atomically flat surface. The RHEED pattern of BTO on SRO show flat surface with small domains. Reciprocal rods are broader due to effect of the Laue function for finite sample sizes. Finite sample sizes originate from small domains with sizes smaller than coherent length of electron beam. Intersections between the Ewald sphere and the reciprocal rods become larger ellipses, resulting in elongated and broader diffraction spots (streaks) in the RHEED pattern [[S. Hasegawa](#)].

BTO on LNO pattern shows multilevel stepped surface. This pattern is characterized by elongated streaks which are modulated in perpendicular direction. In fact they are superposition of two-stepped surface pattern with various spacing. Constructive interference from same-level surfaces as well as destructive interference from different-level surfaces modulate intensity of streaks [[S. Hasegawa](#)].

The surface morphology of BTO layer in LNO/BTO and SRO/BTO stacks (figure 5-3), measured with topographic measurements (AFM), are confirmed to be atomically flat on which terraces are observed with rms roughness below 0.2 nm and the line profile indicating variation in range of  $\mp 0.6$  nm.

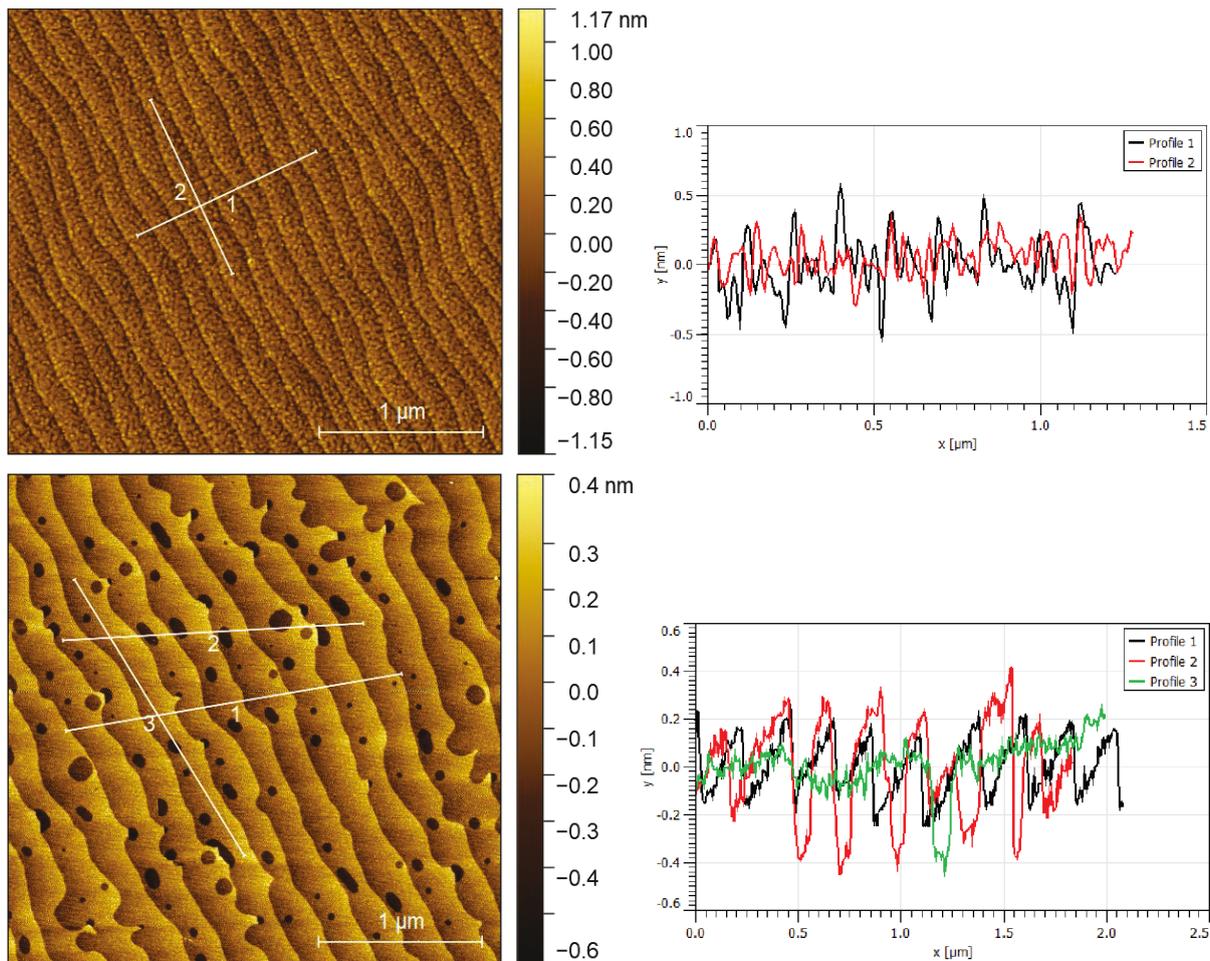


Figure 5-3 AFM topography & respective line profile for (Top) LNO/BTO and (Bottom) for SRO/BTO.  $Rms(sq)$  values are 176.3 and 158.9 pm respectively.

LNO/BTO layer shows more roughness compared to SRO/BTO, however mean average in both cases is less than 0.2 nm. Islands smaller than 0.1 micron are observed on LNO/BTO surface. They are classified as “clusters” which are formed due to experimental conditions and type of deposited materials [Bäuerle]. As reported, formation of particulates can be minimized by outgassing of the target material, employing smooth target materials and optimization of the laser parameters like fluence, frequency and spot size. Holes observed on BTO layer in the SRO/BTO AFM image, can be originated by different growth rate on A-site and B-site terminated SRO layer. However they are not deep ( $\sim 0.4$  nm), therefore the closer guess could be the difference in diffusivity of the SRO layer which may be originated from gradient of SRO surface energy [Zucker et al].

Crystal quality of the grown layers are studied by X-Ray diffraction measurements.  $2\theta - \omega$  Scan of SRO/BTO is highlighted below.

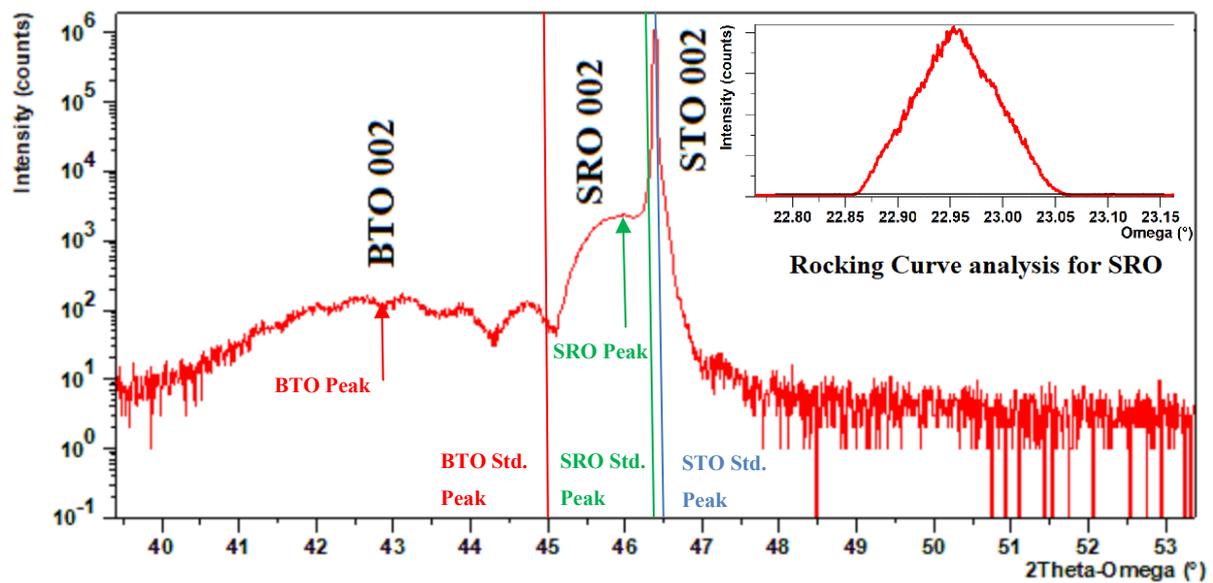


Figure 5-4 XRD  $2\theta - \omega$  scan for STO/SRO/BTO highlighting the (002) film peaks of BTO and SRO as well as the (002) STO sharp peak (single crystal). Rocking Curve analysis for SRO is included with FWHM value of around  $0.1^\circ$  likely caused by Mosaicity.

In agreement with the RHEED patterns, high resolution XRD scans along symmetrical reflections show reflections from the STO, SRO and BTO layers. Standard peaks of bulk materials are shown as  $46.535^\circ$  for STO,  $45^\circ$  for BTO and  $46.409^\circ$  for SRO, taken from HighScore plus database (Using Bragg's law and bulk lattice parameters, gives the same results). As can be seen, STO peak is not shifted whereas SRO peak is shifted for about  $0.3^\circ$  and BTO peak for  $2^\circ$ . The corresponding rocking curve around the SRO (002) reflection (embedded image on top-right) presents a full width at half maximum of  $0.15^\circ$  indicating crystalline orientation for SRO with low mosaicity.

For LNO on BTO, XRD measurements are highlighted in figure 5-5.

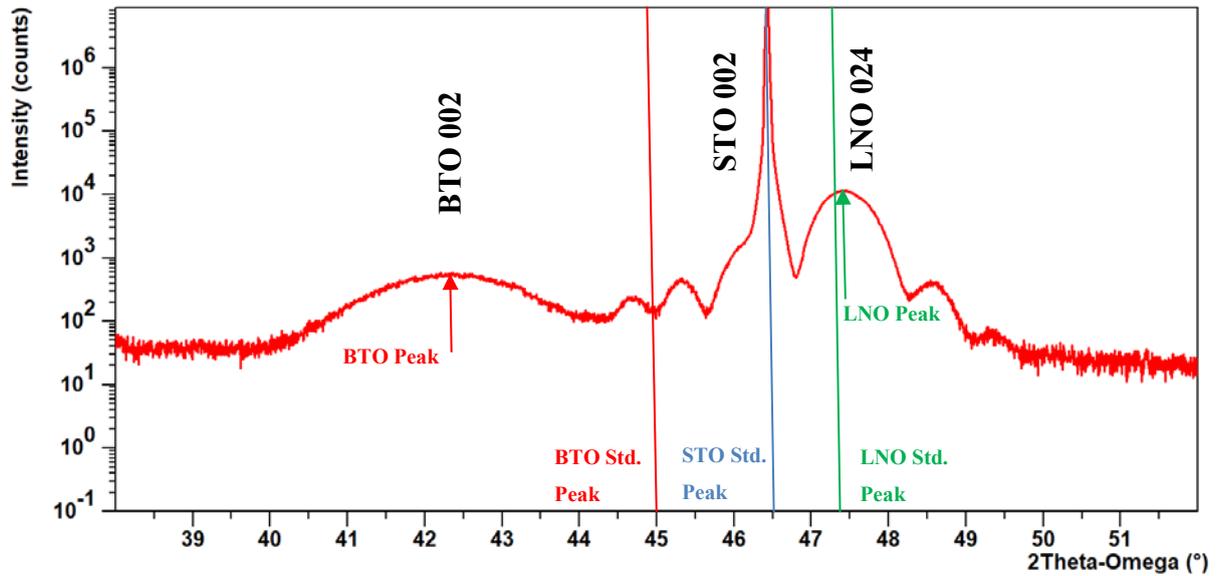


Figure 5-5 XRD  $2\theta - \omega$  scan for STO/LNO/BTO highlighting the (002) film peak of BTO (024) peak for LNO as well as the (002) STO sharp peak (single crystal).

Out-of-plane strain has a direct influence in stabilization of ferroelectricity of thin films. Therefore in order to investigate in-plane and out-of-plane strain in hetero-structure layers, in first step, values for strains are calculated from bulk material lattice values by assuming the epitaxial growth and fully strained layers. Then, RSM structure characterization results are shown and new values are extracted from them. Then two sets of values are compared as well as comparison with similar-approach extracted-values for silicon samples in section 5.1.2.

Lattice parameters for perovskites are summarized in below table:

Property Material	Crystal Structure	Lattice Parameters a, b, c (Å)	Lattice Volume	Poisson Ratio
BTO	Tetragonal	3.966, 3.966, 4.035 [83]	63.467 Å <sup>3</sup>	0.23[Sakhya]
SRO	Pseudo-cubic	3.923, 3.923, 3.923	60.375 Å <sup>3</sup>	0.31 [84]
	Orthorhombic	5.567, 5.530, 7.8446	241.500 Å <sup>3</sup>	
LNO	Pseudo-cubic	3.837, 3.837, 3.837	56.490 Å <sup>3</sup>	0.27[Masys et al] 0.34
	Rhombohedral	5.456, 5.456, 13.1430	391.24 Å <sup>3</sup>	
STO	Cubic	3.905, 3.905, 3.905	59.547 Å <sup>3</sup>	0.24[Sakhya]
Silicon (When STO grown Epitaxial )	Cubic (with 45° rotation)	5.431, 5.431, 5.431 (3.840, 3.840, 3.840)	160.190 Å <sup>3</sup> 56.623 Å <sup>3</sup>	0.27[85], [82]

Table 5-1 Crystal structure, Lattice parameter and Poisson ratio for selected materials. Lattice volume is calculated based on the crystal structure and lattice parameters. Values for lattice parameters are taken from PANalytical HighScore Plus software version 3.0.5 and Poisson ratios from [Masys et al],[Sakhya],[84], [85] & [Masys et al].

To calculate in-plane and out-of-plane strain in each layer (SRO, LNO and BTO), below formulas are used (Com.: = Compressive strain, Ten.: = Tensile strain, INP: = In-Plane, OOP: = Out-Of-plane):

$$S_{INP} = \frac{a_b - a_l}{a_l} \times 100 \quad , \quad S_{OOP} = \frac{\left(\frac{V_l}{(a_b)^2}\right) - a_l}{a_l} \times 100 \quad (5-1)$$

In which  $a_l$  denotes lattice parameter of the layer,  $V_l$  is the lattice volume of the layer, and  $a_b$  is the lattice parameter of the layer beneath (substrate). Formula for out-of-plane strain ( $S_{OOP}$ ) is a simple calculation with assumption of conservation of lattice volume, however for uniformity of calculations with the RSM measurement calculations which will be presented later on in this section, I will use the Poisson Ration formula (Formula 5-4) to calculate out-of-plane lattice parameter:

$$S_{OOP} = \frac{a_{\perp} - a_l}{a_l} \times 100 \quad \text{Where} \quad a_{\perp} = \frac{2\nu}{\nu-1} a_{\parallel} - \frac{\nu+1}{\nu-1} a_0 \quad (5-2)$$

Where  $a_0$  is the bulk lattice parameter,  $a_{\parallel}$  is the in-plane lattice parameter and  $a_{\perp}$  the out-of-plane lattice parameter. Substituting Poisson ratio for materials in table 5-1, results specific formula for them:

$$\begin{aligned} a_{\perp STO} &= 1.63 \times a_{\parallel STO} - 0.63 \times a_{0STO} \\ a_{\perp SRO} &= 1.90 \times a_{\parallel SRO} - 0.90 \times a_{0SRO} \\ a_{\perp LNO} &= 1.74 \times a_{\parallel LNO} - 0.74 \times a_{0LNO} \\ a_{\perp BTO} &= 1.60 \times a_{\parallel BTO} - 0.60 \times a_{0BTO} \end{aligned} \quad (5-2)^*$$

As SRO, STO and LNO are either considered cubic or pseudo-cubic, I have written the formulas only for a lattice parameter, however for BTO which is tetragonal, calculation for out-of-plane (c) parameter will consider necessary correction. Therefore, orthorhombic SRO [110] and rhombohedral LNO [001] are considered as pseudo-cubic growth on cubic STO [001] [Vailionis et al].

In-plane strain for SRO on STO can be calculated using  $a_l = 3.923 \text{ \AA}$  and  $a_b = 3.905 \text{ \AA}$  which results in  $S_{INP} = -0.46\%$  Com. and  $S_{OOP} = 0.41\%$  Ten. The sign determines if it is

Compressive (-) or Tensile (+). Strain in middle layer (LNO or SRO) then is propagated to the top layer (BTO), therefore calculations are based on the fully strained middle layer. Similar calculations yield values which are summarized in table 5-2.

Stack	Middle layer		Top layer	
	In Plane	Out Of Plane	In Plane	Out Of Plane
SRO/BTO	SRO	BTO	-0.46 % Comp. = - 0.018 Å	-1.54% Comp. = -0.061 Å
			+0.41 % Ten. = + 0.0162 Å	+0.92 % Ten. = 0.037 Å
LNO/BTO	LNO	BTO	1.77 % Tens. = +0.068 Å	-1.54% Comp. = -0.061 Å
			-1.24% Comp. = -0.476 Å	+0.92 % Ten. = 0.037 Å

Table 5-2 Calculated out-of-plane strain in layers of two stacks SRO/BTO & LNO/BTO with assumption of fully strained layers.

From table 5-2, it can be seen that if layers are fully strained, BTO layer will have the same in-plane compressive strain and out-of-plane tensile strain in both stacks. This is however not the case in our measurement. By comparing figures 5-4 and 5-5, BTO peak on LNO shows more shift to the left, equivalently more strain.

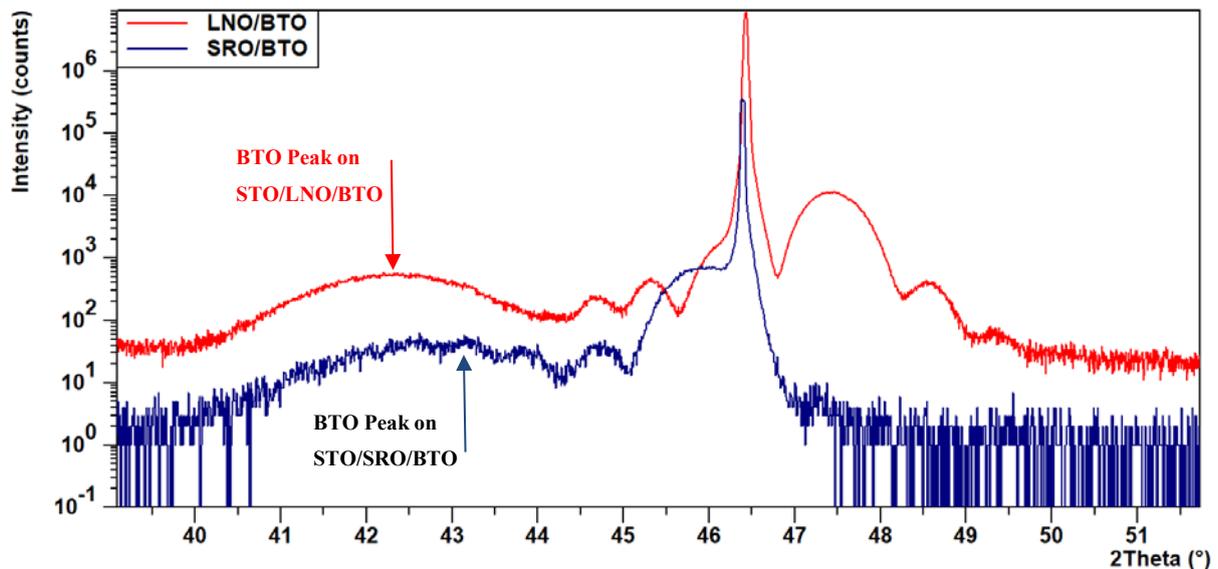


Figure 5-6 BTO shift compared in two stacks of STO-substrate. BTO shows more out-of-plane strain in LNO/BTO rather than SRO/BTO likely due to defects or dislocations. (Figures 5-4 & 5-5 combined here for the ease of comparison)

From calculations based on Bragg's law, strain for BTO in SRO/BTO is 3.7% and is 5.1% in LNO/BTO. Here from new calculations the out-of-plane strain is 4.15% for both cases, assuming full strain in the layers.

RSM measurements presented here can lead to better indication of the strain and more accurate values.

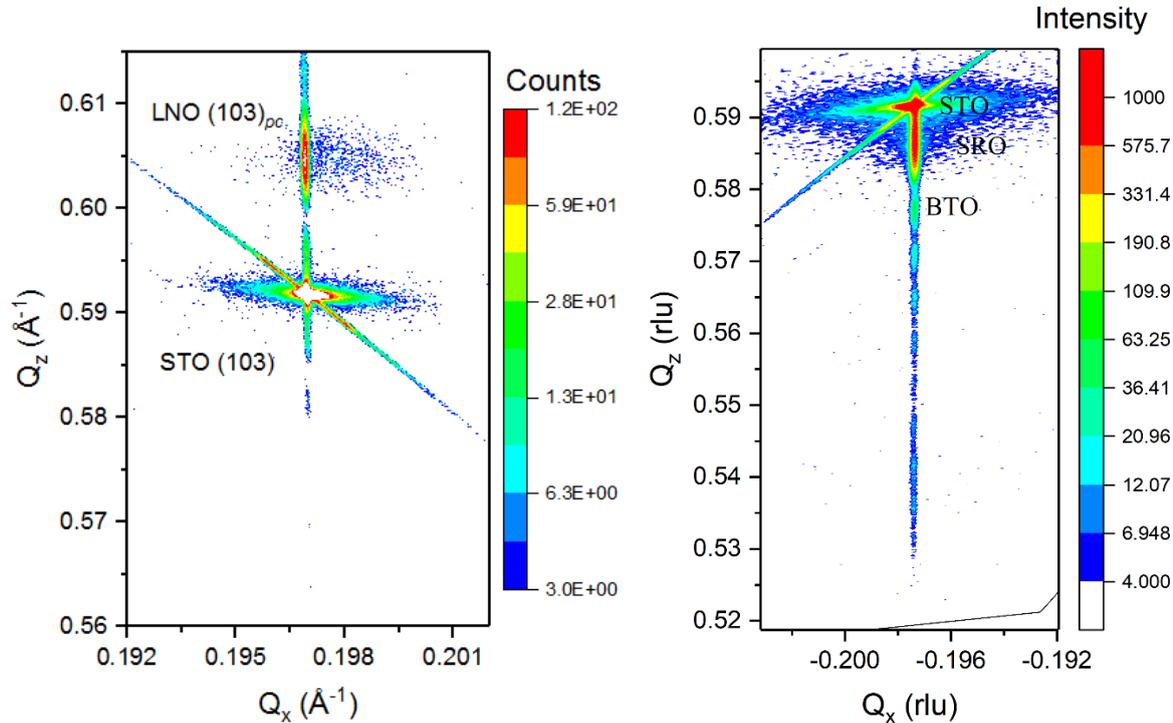


Figure 5-7 Reciprocal Space Map (RSM) for (left) STO/LNO and for (right) STO/SRO/BTO. Both SRO and LNO show out-of-plane tensile strain.

All peaks in three RSM maps in figure 5-7 are almost aligned in  $Q_z$  with a single  $Q_x$  value which indicates epitaxial (Fully strained) growth. By using following formula, lattice parameters of the layers can be calculated.

$$a = \frac{\lambda \sqrt{h^2 + k^2}}{(Q_x \cdot 2)} \quad , \quad c = \frac{\lambda \cdot l}{(Q_z \cdot 2)} \quad (5-3)$$

Where  $\lambda$  is the XRD wavelength and [h, k, l] crystal direction. By substituting  $Q_x = 0.1970$ ,  $Q_z = 0.605$ ,  $h = 1$ ,  $k = 0$ ,  $l = 3$  and  $\lambda = 1.54 \text{ \AA}$  yields  $a = 3.909 \text{ \AA}$  &  $c = 3.82 \text{ \AA}$  for LNO, and with  $Q_z = 0.592$  yields  $a = 3.90 \text{ \AA}$ ,  $c = 3.91 \text{ \AA}$  for STO. Respectively with  $Q_x = 0.1970$ ,  $Q_z = 0.586$ ,  $a = 3.909 \text{ \AA}$ ,  $c = 3.94 \text{ \AA}$  for SRO. And with  $Q_z = 0.577$ , yields  $a = 3.909 \text{ \AA}$ ,  $c = 4.0 \text{ \AA}$  for BTO. However, the values need to be adjusted by Poisson ratio (as before) which indicates how a material deforms when it is stretched or compressed.

$$a_{\perp} = \frac{2\nu}{\nu-1} a_{\parallel} - \frac{\nu+1}{\nu-1} a_0 \quad (5-4)$$

Where  $a_0$  is the bulk lattice parameter,  $a_{\parallel}$ , the measured in-plane lattice parameter and  $a_{\perp}$ , the out-of-plane lattice parameter. Bulk values, calculated values with the assumption of fully strained layers as well as extracted values from measurements are summarized in below table.

Lattice Parameter a, b, c (Å) Material	Bulk	Fully strained	RSM extracted	RSM Poisson Adjusted
BTO In SRO/BTO	3.966,	3.905	3.909	3.909
	3.966,	3.905	3.909	3.909
	4.035	4.072	4.000	4.076
SRO In SRO/BTO	3.923,	3.905	3.909	3.909
	3.923,	3.905	3.909	3.909
	3.923	3.939	3.940	3.930
LNO In LNO/BTO	3.837,	3.905	3.909	3.909
	3.837,	3.905	3.909	3.909
	3.837	3.714	3.820	3.760

Table 5-3 comparative table for lattice parameters obtained from calculations and measurements. Fully strained column shows calculated lattice parameters assuming fully strained layers. RSM values with Poisson adjustments present measured values from RSM measurements.

Comparing “Fully Strained” and “RSM Poisson Adjusted” columns, it can be seen that strain in SRO layer is less than calculated whereas in BTO and LNO is higher. This higher strain may be originated by oxygen vacancies or defects in the crystal.

After XRD and AFM characterization of the samples, in order to investigate ferroelectric properties of the samples, Piezoelectric Force Microscopy (PFM) is used. SRO/BTO and LNO/BTO samples showed ferroelectric properties. Figure 5-8 shows the phase and amplitude of the PFM measurement.

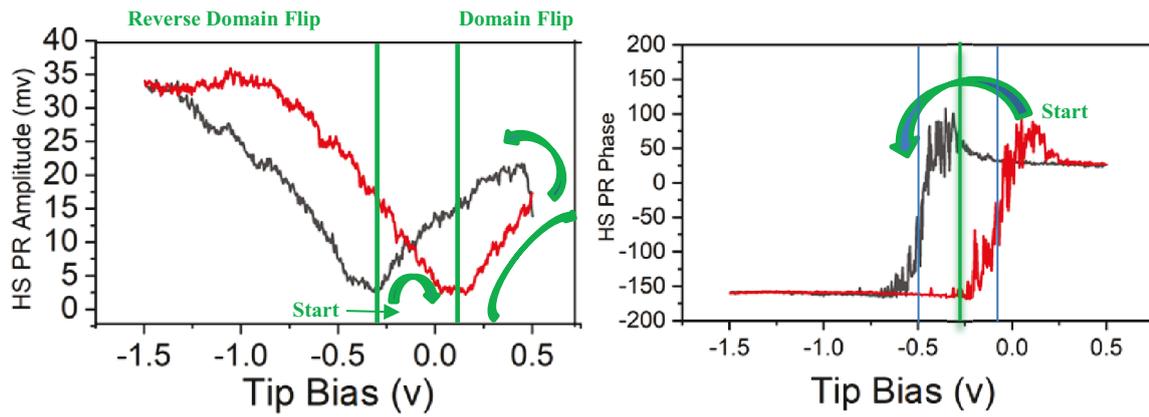


Figure 5-8 Characteristic ferroelectric hysteresis loop measured by PFM on a STO/SRO/BTO sample.

Above curves are produced by a feature in PFM measurement in which, amplitude and phase are measured while voltage is ramped up and down in a definite range (in our case, from -1.5 to 0.5). Remembering again that all ferroelectrics are piezo-electric, one can justify the amplitude curve above with the referring to section 2.2.1. Domain Flip and Reverse domain flips are highlighted. Symmetry of the loop is not around zero which can be explained by internal electric field inside BTO layer due to screening charges in interfaces [Glinchuk et al] or inhomogeneity of polarization along vertical axis perpendicular to layer surface [Zubko et al].

Poling of BTO surface (writing strips of upward and downward polarization areas on the surface) is done by applying voltage with different polarity to the tip while scanning the surface. Then afterward, another scan without applying voltage to the tip (0 v), produced following image in figure 5-9.

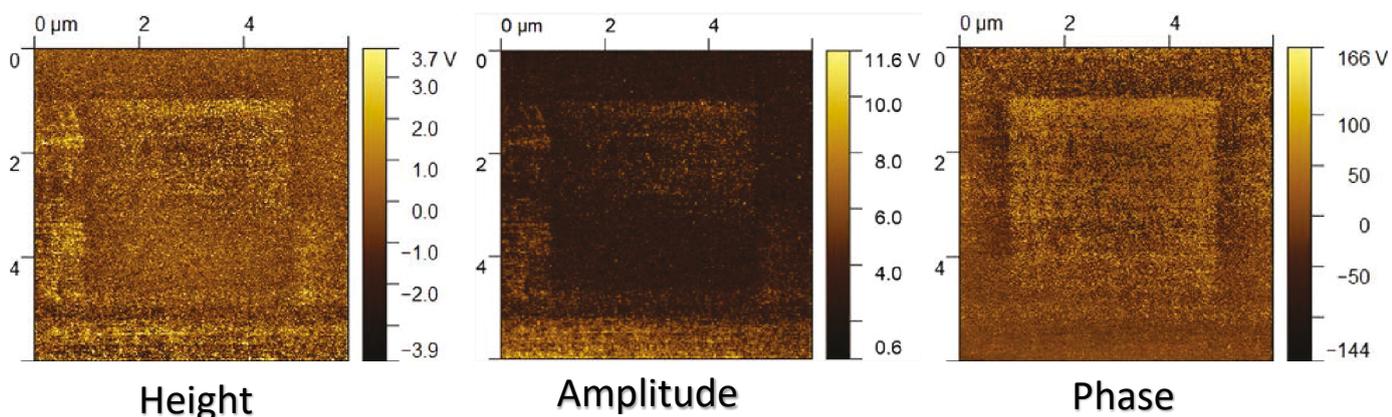


Figure 5-9 PFM topography, Z sensor, amplitude, and phase images. First, the outer  $6 \times 6 \mu\text{m}^2$  square was written with +2V tip bias and then the inner  $4 \times 4 \mu\text{m}^2$  square at -2 V. Then the whole  $6 \times 6 \mu\text{m}^2$  area was read at 0 V. The voltages correspond to values above, below, and within the hysteresis loop shown in fig. 5-11.

Ferroelectric property implies that domains oriented in opposite directions should yield the same amplitude. This implication is not reflected perfectly in the images because poling voltages were chosen wrong during writing. In the phase image of figure 5-8, margins of the hysteresis loop as well as symmetry axis of the hysteresis loop is shown (symmetry is around -0.25 volt). That poling voltages have to be  $>+0.5$  v and  $<-0.75$  v with reading voltage of -0.25 v, then all the domains are switched and aligned fully with external field (voltage) which leads to sharp contrast in the boundaries of the poling image. Otherwise poling of the surface is done with wrong values which can not necessarily fully align the domains and lead to a clear high-contrast poling image. Therefore voltages of -2v, +2v and 0v led to the low quality of the image due to asymmetry around zero. Despite that, hysteresis feature, reveals clear loop shown in figure 5-8. As mentioned in the beginning of this chapter, PFM measurements are subject to the fact that cannot be considered as an unambiguous method for discovery of ferroelectricity. Here we got confirmation for ferroelectricity of BTO layer from our collaborators in ULPEC project.

As a summary, RHEED patterns indicate flat 2D growth which was confirmed by AFM topographic measurements. Both set of samples demonstrated smoothness (RMS value below 200 pm) regarding surface morphology with rms value smaller than 1 nm. Fully characterized XRD and RSM measurements revealed strain in layers of aforementioned stack with good consistency with calculated values. BTO layer showed increase of about 1% out-of-plane lattice parameter on SRO/BTO stack. Functional characterization also revealed existence of ferroelectricity in BTO layer which was confirmed by ULPEC collaborators (Unambiguously).

## 5.1.2 SILICON SUBSTRATES

Results for deposition of LNO/BTO layers on silicon substrate are highlighted in this section:



Figure 5-10 Schema of the layers deposited on top of substrate with respective thickness.

Figure 5-11 shows RHEED pattern for LNO and BTO growth on STO buffered Silicon substrate.

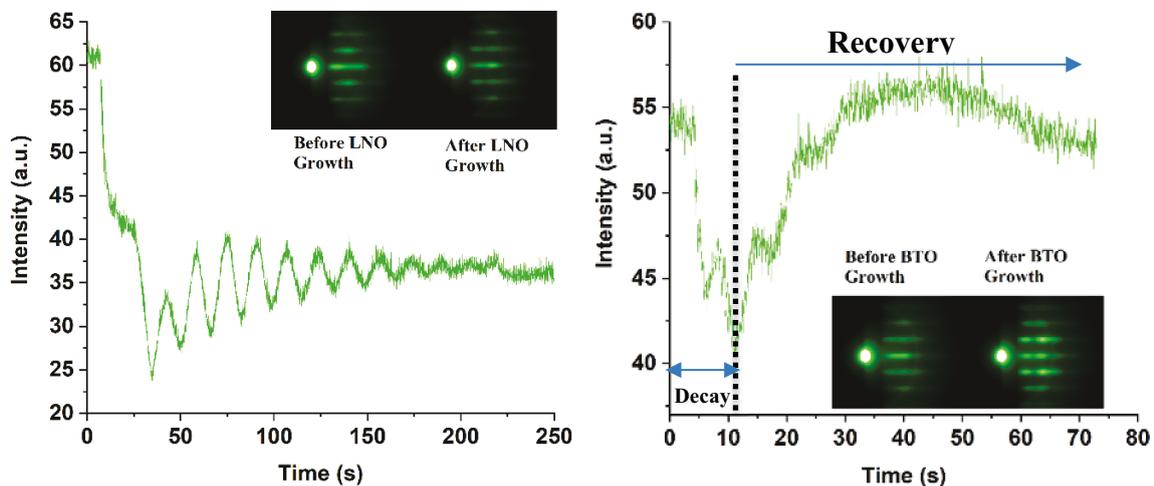


Figure 5-11 (Top) RHEED pattern and intensity for the LNO and (Bottom) for BTO growth. Diffraction spots are clearly visible in both, especially after growth in both LNO and BTO. RHEED intensity shows decay and recovery during growth for central spot. The Intensity shows number of oscillations indicating number of grown unit cells which is 13 for LNO and 7 for BTO.

Both are grown in pressure of 0.04 mbar with the same laser spot size of  $1.753 \text{ mm}^2$ . BTO pattern shows multilevel stepped surface combined with 3D island growth. Streaks are modulated in intensity in perpendicular while modulated parts are tending to separate and shaping dots which is the characteristic of 3D island growth [S. Hasegawa]. This conforms to AFM measurement in Figure 5-12 with islands distributed all over the surface. RHEED Intensity is high at the beginning which indicates the crystallinity of substrate. When deposition

starts, surface morphology changes periodically due to nucleation and coalescence of islands in the growing layer. This is why we see a decay in intensity just after deposition start and gradually when new layers grow, intensity increases. This periodically change continues and each peak corresponds to a new layer grown.

Annealing can give more energy to ad-atoms to decrease the number of dislocations. Meanwhile, it allows oxygen to diffuse to the grown layer to fill the probable oxygen vacancies and improve the crystalline quality. Stripes in the RHEED pattern of BTO indicate that growth is not in a three dimensional island growth mode. This agrees with the AFM image (Figure 5-12), in which no islands are formed. The same description for particulates mentioned in previous section, applies here.

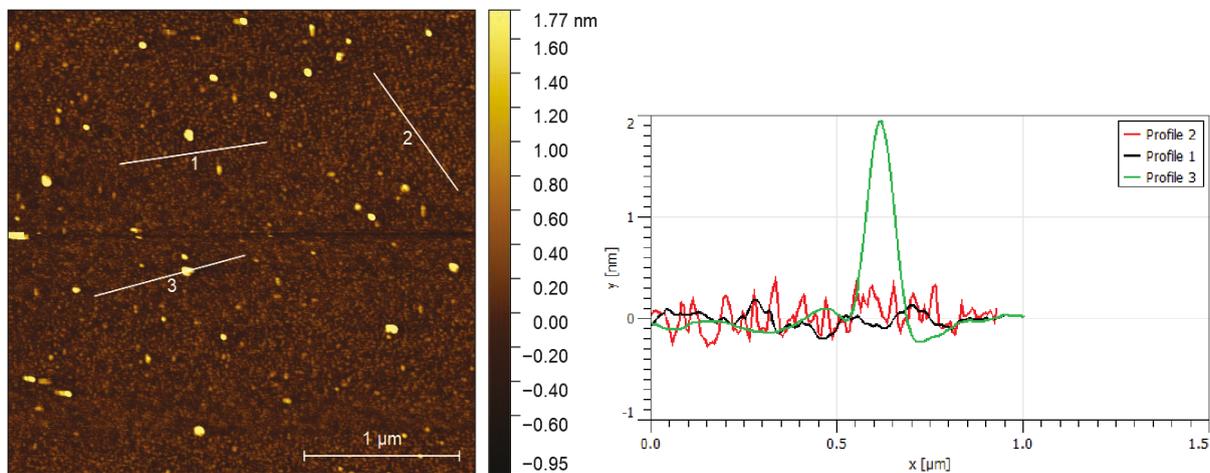


Figure 5-12 AFM topography (left) & respective line profile (right) bounded between  $\sim -0.3$  to  $\sim +0.4$  nm for profiles 1 & 2 (non-crossing the droplets) with respective  $Rms(sq)$  value of 268 pm.

AFM measurement with respective line profile depicted in figure 5-12, indicates a smooth surface. Height difference is limited to  $\pm 0.7$  nm for line profiles not crossing the droplets (profiles 1 & 2).

Figure 5-13 is a  $2\theta - \omega$  scan with peaks associated with layers in figure 5-10. Standard peaks of STO, BTO and LNO are shown for comparing with what we got in single crystal growth. BTO has broader peak due to small thickness. Fringes of the LNO are convoluted with the STO peak, therefore STO peak cannot be seen clearly. BTO peak is broadened and shifted to the left by approximately  $1.3^\circ$  comparing to standard peaks which indicates strain in BTO layer. This is true only if the film is fully strained and no defect contribute to this effect.

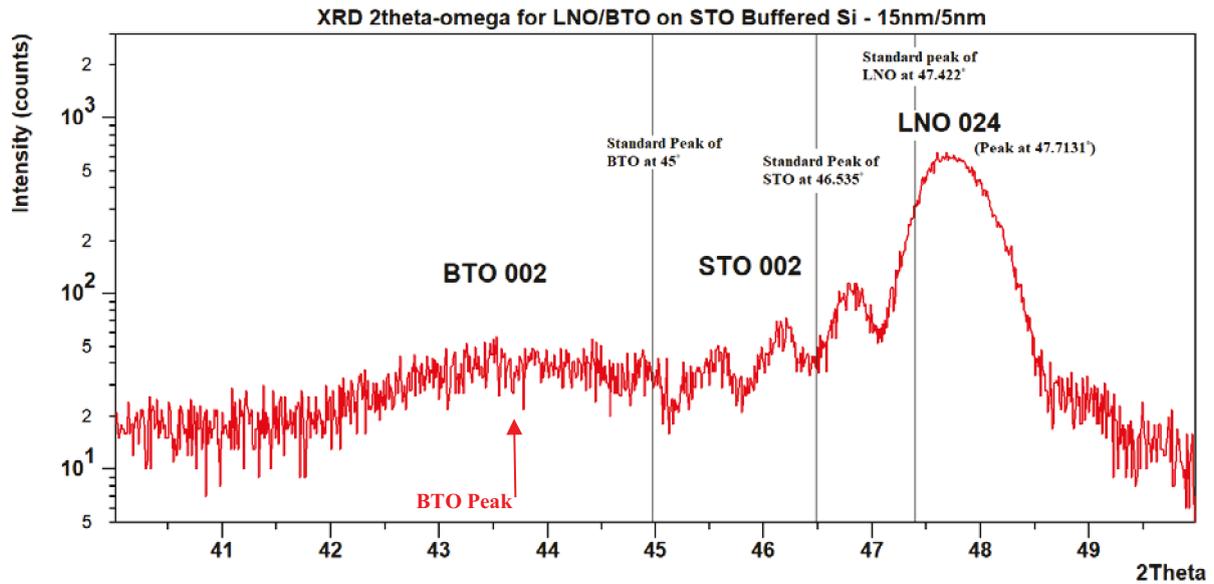


Figure 5-13-1 XRD  $2\theta - \omega$  scan highlighting the (002) film peaks of BTO and STO as well as the (024) rhombohedral LNO peak. Standard values taken from respective PDF files from “HighScore plus software”. (Silicon [001] peak is not in the range).

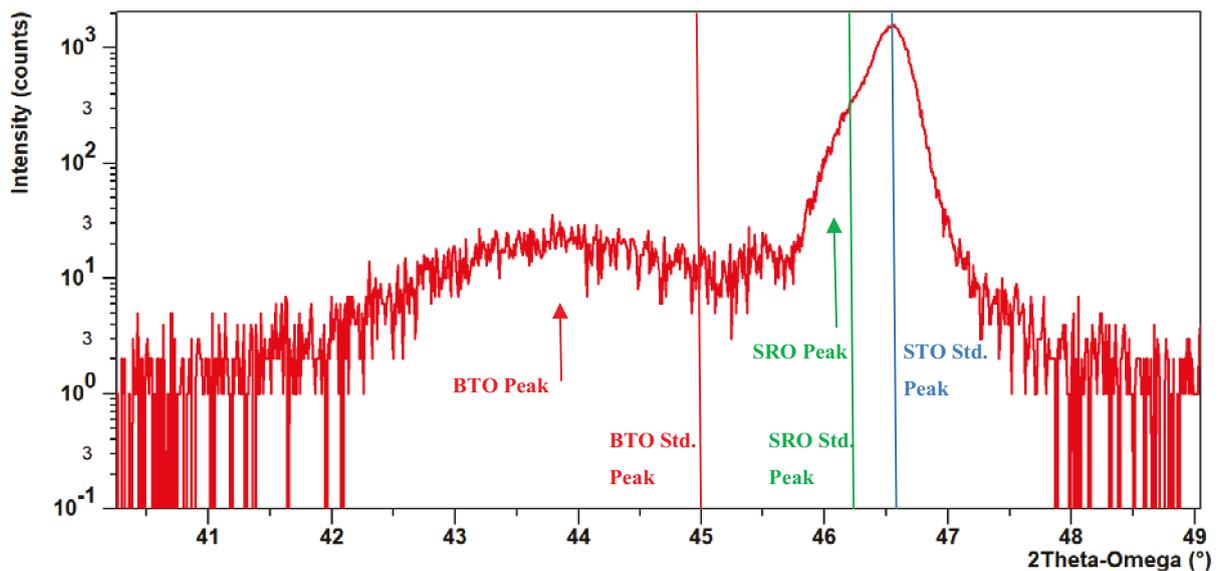
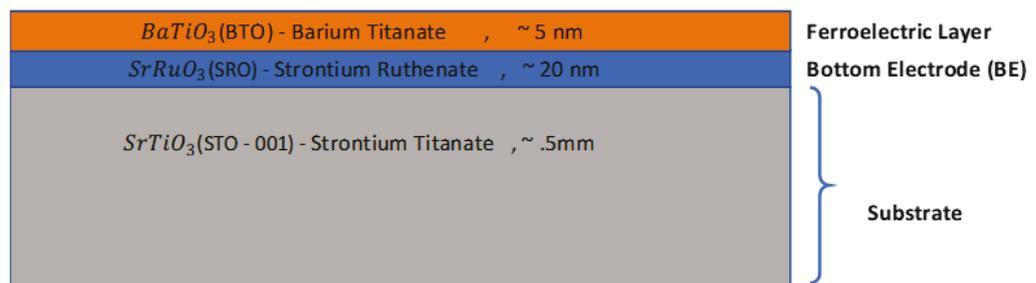


Figure 5-13-2 XRD  $2\theta - \omega$  scan highlighting the (002) film peaks of BTO and STO as well as the (002) orthorhombic SRO peak.

The stack of layers corresponding to figure 5-13-2 is depicted below:



RSM map of the SRO/BTO sample is shown below:

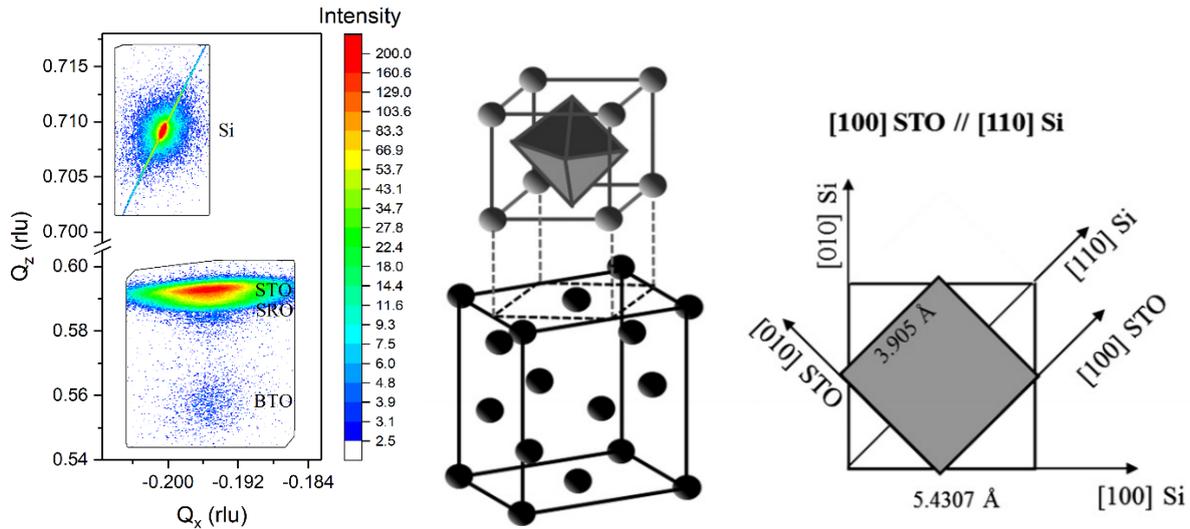


Figure 5-14 (left) RSM map for  $[103]$  STO/SRO/BTO as well as  $[115]$  Si layers. (Right) demonstration of growth of STO on top of Si due to lattice mismatch (source: Baek et al). XRD measurement of STO/Si substrates in IMS group has confirmed growth of  $45^\circ$  in-plane rotated STO lattice on Si.

Lattice mismatch between Si and STO is large ( $5.4307\text{\AA}$  &  $3.905\text{\AA}$ ), therefore STO needs to be grown epitaxial by  $45^\circ$  in-plane rotation respect to Si unit cell which makes a better lattice match between STO lattice parameter and half of the diagonal distance of the Si unit cell ( $3.84\text{\AA}$ ) [Baek et al]. Similar calculation for fully strained layers as well as calculation based on the RSM measurements, yield the following values, summarized in below table.

Lattice Parameter a, b, c (Å)	Bulk	Fully strained	RSM extracted	RSM Adjusted	Poisson
Material BTO	3.966,	3.843	3.949	3.949	
	3.966,	3.843	3.949	3.949	
	4.035	4.109	4.053	3.976	
SRO	3.923,	3.843	3.949	3.949	
	3.923,	3.843	3.949	3.949	
	3.923	3.995	3.907	3.900	
STO	3.905,	3.843	3.949	3.949	
	3.905,	3.843	3.949	3.949	
	3.905	3.944	3.895	3.870	

Table 5-4 comparative table for lattice parameters obtained from calculations and measurements. Fully trained column shows calculated lattice parameters assuming fully strained layers. RSM values with Poisson adjustments present measured values from RSM measurements.

I will use 4.053 Å as c in BTO layer because is consistent with the RSM and couple scan measurements. To highlight the differences, it is better to use an index defined by the ration of  $c/a$  or equivalently,  $(\frac{c}{a} - 1) \times 100$  as the percentage of tetragonality. Calculations are summarized in table 5-5. As can be seen, silicon has still increased the tetragonality factor by  $(\frac{2.63}{1.74} - 1) \times 100 = 51\%$  whereas single crystal STO has increased it by 146% which is almost 3 times greater.

Properties Material	Lattice dimension (Bulk)	Lattice dimension (from RSM on STO)	Lattice dimension (from RSM on Silicon)	Tetragonal factor (%) on bulk material	Tetragonal factor (%) on STO (RSM)	Tetragonal factor (%) on Silicon (RSM)
BTO	3.966	3.909	3.949	1.74	4.27	2.63
	3.966	3.909	3.949			
	4.035	4.076	4.053			
SRO	3.923	3.909	3.949	0	0.54	-1.24
	3.923	3.909	3.949			
	3.923	3.930	3.900			

Table 5-5 Comparative values of lattice parameter and strain in BTO and SRO layers of samples from single crystal and silicon based substrates.

As can be seen, BTO is strained to the substrate in both single crystal STO and Silicon however Silicon reduces the tetragonality of BTO which in consequence decreases the ferroelectricity. Below discussion can be helpful in order to get more insight to the role that thermal expansion coefficient of silicon plays in epitaxial growth of BTO.

Perovskites like STO, BTO, LNO and SRO have all near the same coefficient of Thermal Expansion (CTE) around  $8.7 \times 10^{-6}$  while this value is around  $2.6 \times 10^{-6}$  for silicon. Zhang et al has reported a strategy to continuously tune epitaxial strains in perovskite films grown on

Si(001) by utilizing the large difference of thermal expansion coefficients between the film and the substrate. Strain in STO layer grown on silicon has been measured and also calculated. Lattice parameter change due to temperature change and the resulting strain is shown in figure 5-15.

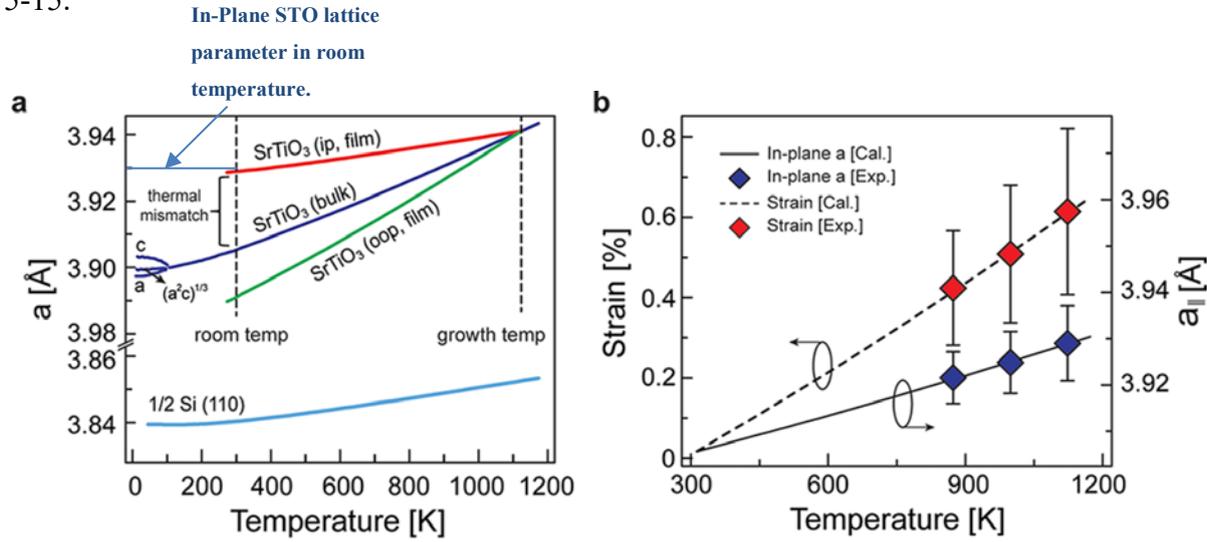


Figure 5-15 (a) Lattice parameters of bulk SrTiO<sub>3</sub> (purple line) and Si (blue line) and calculated out-of-plane (green line) and in-plane (red line) lattice parameters for SrTiO<sub>3</sub> films on Si substrate. (b) Calculated in-plane strain (dashed line) and calculated in-plane lattice parameters (solid line) of SrTiO<sub>3</sub> films and experimental results. (Source: Zhang et al).

As can be seen in Figure 5-15 (left), when STO on top of silicon is grown in 1200°C and then cooled down to room temperature, in-plane lattice parameter is still greater than bulk value of STO. This is due to the tensile in-plane strain induced to STO from silicon with lower CTE value. On the other hand, out-of-plane lattice parameter is smaller than the bulk value. Figure 5-15 (right) demonstrates induced strain percentage and lattice parameter changes vs temperature change. As we calculated in section 5.1.1, strain in bottom layers can be propagated to the top layers, therefore in-plane tensile strain in STO layer, can decrease out-of-plane lattice parameter in LNO and BTO layers which in consequence has negative effect on the stabilization of ferroelectric property of BTO layer.

Using aforementioned CTE values for Silicon and STO, in-plane lattice mismatch between Silicon and STO after deposition in temperature of 600°C can be calculated theoretically. Then result can be compared with the values from fully strained layers calculations to see the effect. Assuming room temperature of 23°C, the temperature difference of 577°C induces  $\Delta l_{Si}$  and  $\Delta l_{STO}$  in in-plane lattice parameter (as well as out-of-plane lattice parameter which is not of our attention now)

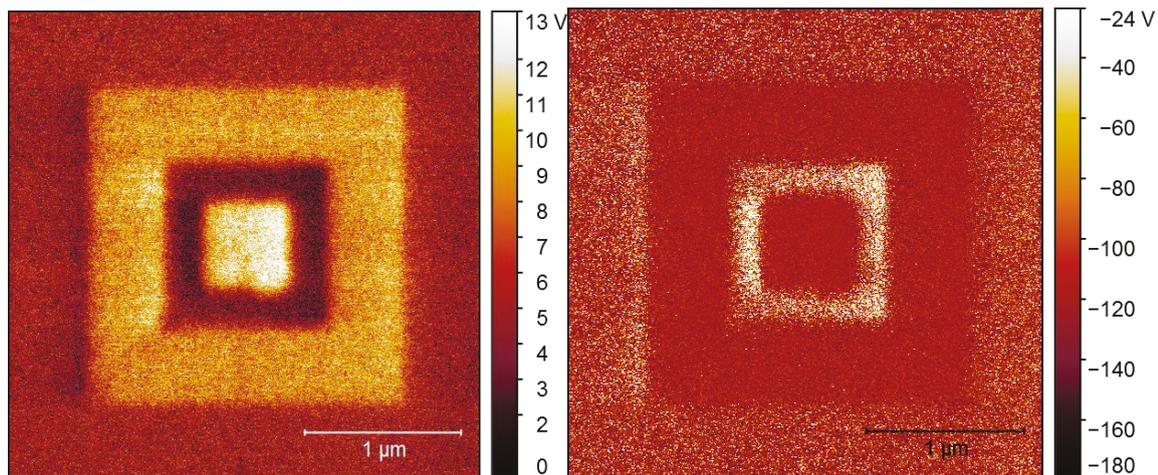
$$\Delta l_{Si} = a_{Si} \times \sqrt{2} \times (23 - 600) \times 2.6 \times 10^{-6} = - 8.153 \times 10^{-3} \text{Å}$$

$$\Delta l_{STO} = a_{STO} \times (23 - 600) \times 8.7 \times 10^{-6} = - 19.602 \times 10^{-3} \text{Å}$$

But as STO is strained to Silicon, the contraction of its lattice parameter is limited to  $(19.602 - 8.153) \times 10^{-3} \text{ \AA}$  or  $0.011 \text{ \AA}$ . It means in-plane lattice parameter of STO will expand to  $3.905 + 0.011 \text{ \AA} = 3.916 \text{ \AA}$ . This new value can now be used to calculate BTO out-of-plane lattice parameter assuming fully strained layers:  $c_{BTO} = 3.996 \text{ \AA}$ . It shows BTO layer is still strained with extension in out-of-plane lattice parameter, however tetragonality factor is now 2.04 which is less than 2.63, which is the value from RSM experiments.

To investigate ferroelectricity in BTO layer on Silicon, samples were functionally characterized with PFM measurements and results are demonstrated in figures 5-16 and 5-17.

*Figure 5-16 Characteristic ferroelectric hysteresis loop measured by PFM on a Si/STO/LNO/BTO sample. Later on, it was revealed that domains are not switchable and what is observed was artefacts.*



*Figure 5-17 PFM topography, amplitude, and phase images. First, the second outer  $2 \times 2 \mu\text{m}^2$  square was written with  $+0.3 \text{ V}$  tip bias and then the next  $1 \times 1 \mu\text{m}^2$  square at  $1.3 \text{ V}$ . Again  $0.5 \times 0.5 \mu\text{m}^2$  with  $+0.3 \text{ V}$ . Then the whole  $3 \times 3 \mu\text{m}^2$  area was read at  $0.8 \text{ V}$ . The voltages correspond to values above, below, and within the hysteresis loop shown in fig. 5-16.*

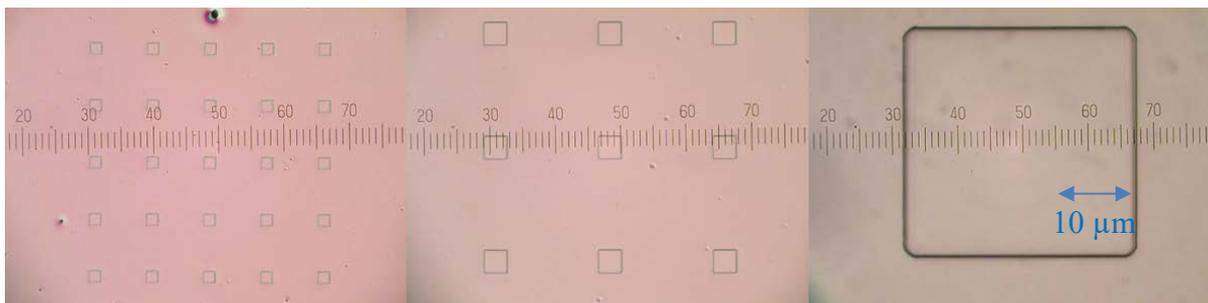
Figure 5-17 demonstrates poling of the BTO surface with the details mentioned in the caption of the figure. Later on it was revealed that the domains were not switchable (an artefact). This artefact can originate from charge induction when poling is done. Limitations and reliability of PFM measurement will be extensively discussed in chapter 6.

## 5.2 CLEANROOM PROCESS

### 5.2.1 SILICON SUBSTRATES

The aforementioned samples were introduced to cleanroom for UV lithography. The main goal as mentioned in chapter 4, was to grow metal top electrodes on top of ferroelectric layer (BTO). This is the first step for the realization of a FTJ. This step is necessary due to using combination of materials for fabrication of FTJ which are different from materials used in a normal silicon based cleanroom process.

It was decided to use two different lithography methods starting from micro-scale patterning by UV lithography and gradually decrease the sizes of the desired pattern to Nano-scale. Pattern used for micro-scale range is depicted below in figure 5-18. As can be seen, rectangular patterns ranging from  $20\ \mu\text{m}$  to  $350\ \mu\text{m}$  each side, have been transferred to the surface of the BTO. This is an image from resist layer on top of BTO after UV exposure and development and before sputtering.



*Figure 5-18 UV lithography pattern is patterned on top of the sample and resist is developed. Sample is ready for sputtering. Square patterns ranging from  $2\ \mu\text{m}$  to  $35\ \mu\text{m}$  are patterned in different location of sample.*

Squares with different sizes are patterned to BTO layer for enabling benchmarking of ferroelectricity in respective patterned areas. Afterward metal electrodes sputtered with profile of 10 nm of Cobalt first and 50 nm of Gold on top. Cobalt was used as it was proven to have better adhesion with BTO layer. Meanwhile [Chanthbouala et al.](#) has reported using 10 nm of Au on top of 10nm of cobalt as an electrode sputtered on BTO layer. The difference in Au layer

thickness between his work and ours is arbitrary. Other set of samples were patterned with E-beam lithography to sputter electrodes in Nano-size range. The pattern is shown below:

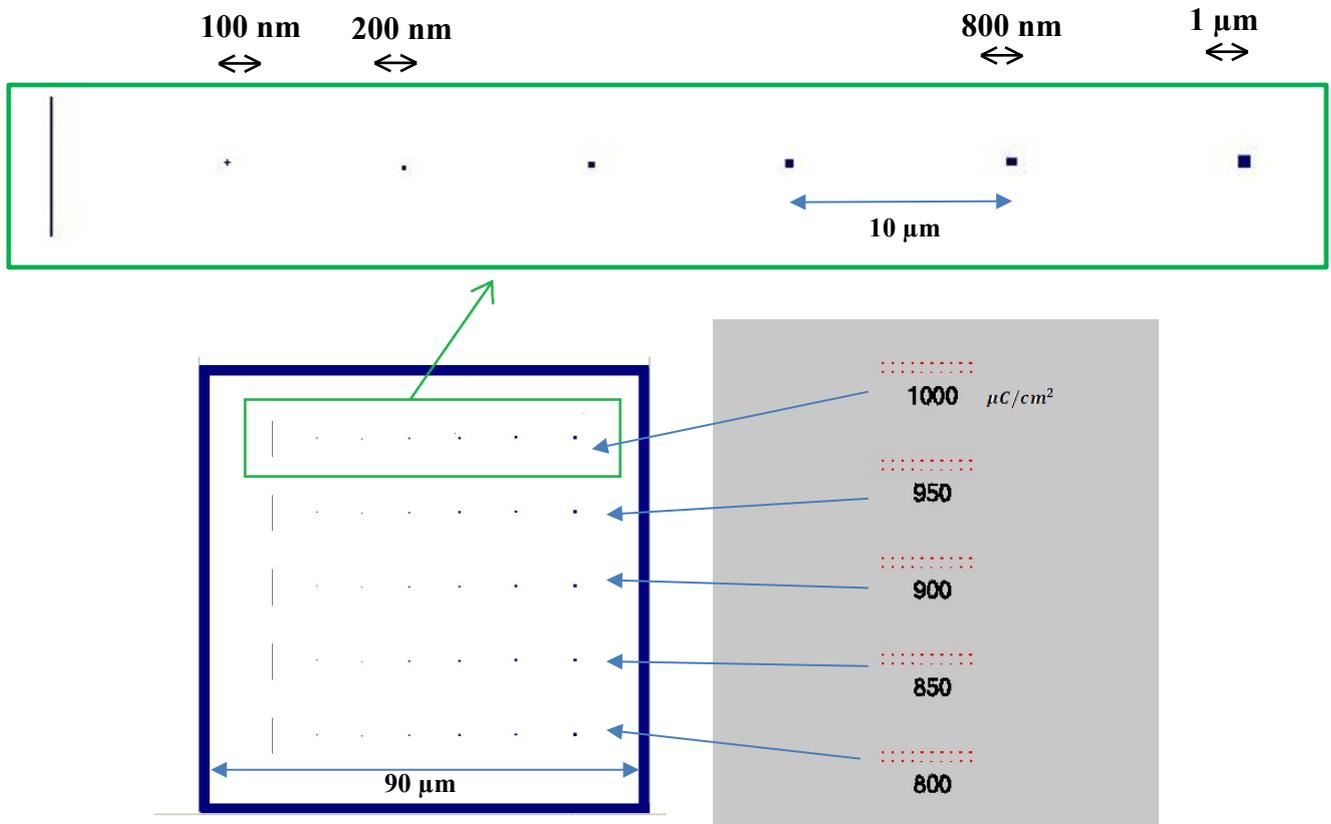


Figure 5-19 (Below-left) Outer square framework consists of 5 row of small squares ranging from 100 nm to 1  $\mu\text{m}$ . (Above) One of the rows have been zoomed out. Dose pattern (below-right) ranging from 800 to 1000  $\mu\text{C}/\text{cm}^2$ .

Squares ranging from 100 nm to 1  $\mu\text{m}$  in each side have been arranged in horizontal line and have been repeated with different doses (coulomb/square cm) in vertical arrangement. Respective dose pattern is shown in right image. Each row is then written with the different dose pattern shown in the below-right of the figure ranging from 800 to 1000  $\mu\text{C}/\text{cm}^2$ . Doses have different proximity effects which can be taken into account during measurements of ferroelectric properties.

The big square containing this pattern has been written by E-beam lithography multiple times in the center of sample to enable multiple choice of measurements in different locations of the sample surface. Written pattern after liftoff on top of BTO layer is shown in figure 5-20. It is taken with an optical microscope or AFM before measuring AFM. Again 10 nm of Cobalt first and 50 nm of Gold is sputtered and then resist layer is done liftoff by using Acetone and Isopropanol for 10 minutes each, applying ultrasound bath while the sample is in solvents.

Time for liftoff seemed not to be enough as can be seen in figure 5-20 that 3 of the big squares have still Gold. By doing the liftoff again for longer time and applying ultrasound bath, these 3 squares also were processed completely.

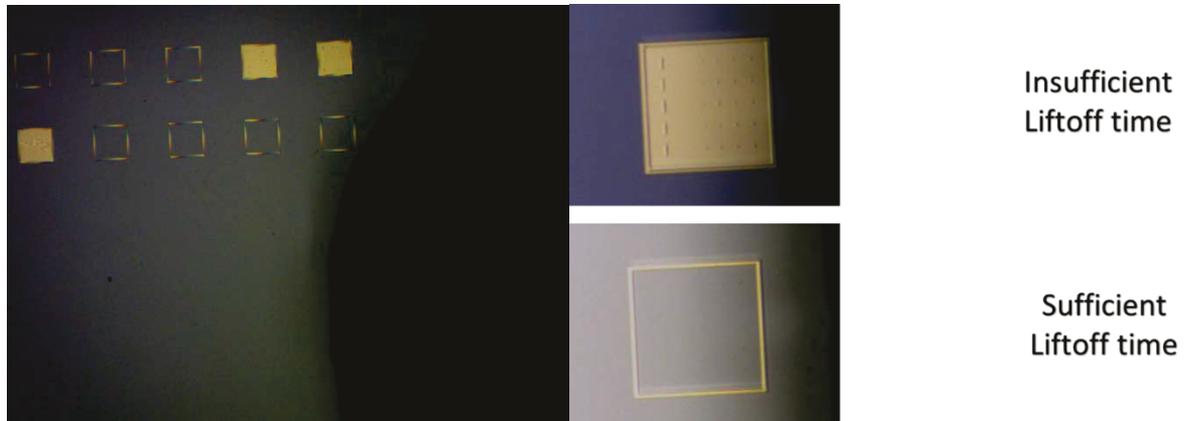


Figure 5-20 (left) Surface of sample after sputtering and liftoff. Outer square framework mentioned in figure 5-19 is patterned in 10 different locations to provide more option for measurement. Squares with gold color, are not perfectly treated with lift-off process (right-above) and some are perfectly done (right-below). This issue is due to insufficient liftoff time and ultrasound bath time.

AFM measurement for a region of  $50 \times 50 \mu\text{m}^2$  containing one of the liftoff aforementioned squares is shown in figure 5-21 on left-side. On right-side, AFM image shows the surface of the Gold metal on top of the electrode.

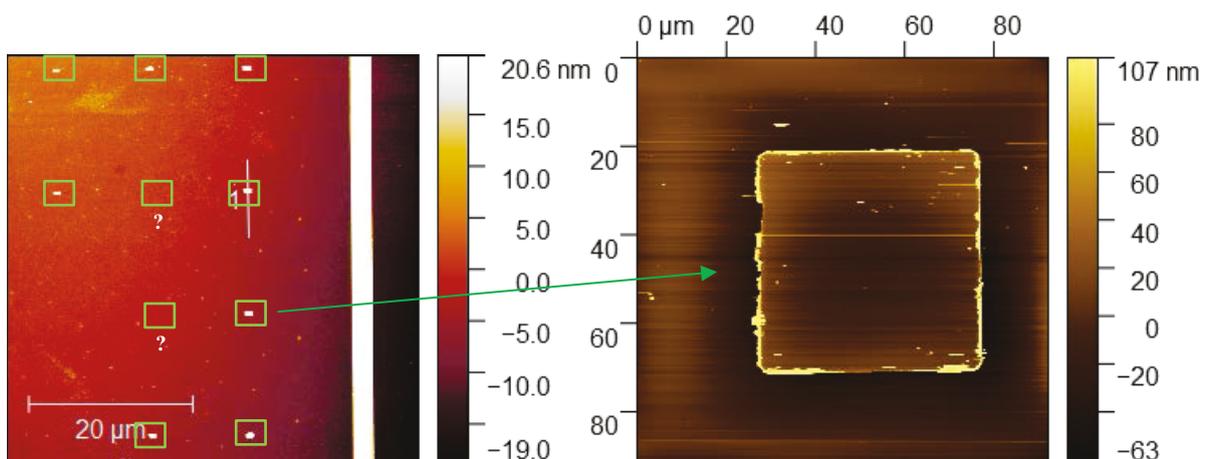
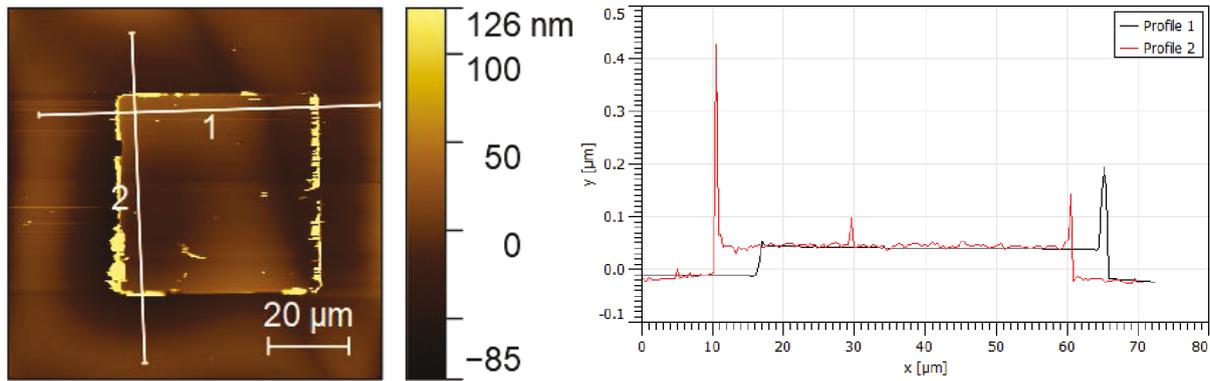


Figure 5-21 (left) AFM image of one of the big square frameworks. Some of the sputtered electrodes are broken probably during liftoff using ultrasound bath. (Right), AFM image from top of the gold electrode.

First attempt to measure the ferroelectricity on top of the electrode and BTO surface on UV patterned sample is shown in image 5-22. AFM image and respective line profile of the electrode shows some edge distortion. Tip movement with relatively fast scan speed may cause abrupt peaks in line profiles however for x in interval [17, 60]  $\mu\text{m}$  the height is around 0.06  $\mu\text{m}$  or simply 60 nm. It is in accordance to the sputtered height of electrode.



*Figure 5-22 (top-left) AFM measurement on samples processed with UV lithography in a region containing electrode with dimension of  $0.5 \times 0.5 \mu\text{m}^2$ . (top-right) line profile shows  $\sim 60 \text{ nm}$  height of the electrode. Peaks at boundaries of electrode might indicate low quality and precession of sputtering.*

Sweep of the frequency in PFM measurement on top of sample surface (BTO) layer for finding suitable resonance frequency of the layer did not succeed. Sweep in lower frequencies also did not reveal a contact resonance frequency. Contact resonance frequency and sweep feature to find it, is explained in section [3.2.1.1](#). In order to find out if the surface is ferroelectric, other attempts were done but they did not succeed either. Please notice that for all PFM measurements on BTO layer in benchmark system, sweep of the resonant frequency was done and succeeded. Then measurements were done using that frequency.

Attempts with a frequency near to observed frequencies in samples before UV process was done to write 45 degree cross bar strip with upward and downward polarizations which is shown in figure 5-23.

Contact resonance frequency could not be observed after several tries. As the tip is stationary while sweeping the frequency range, it is dependent to the location of the surface beneath. Several tries in different locations without finding the contact resonance frequency, indicates to corruption of the tip or absence of piezoelectric layer.

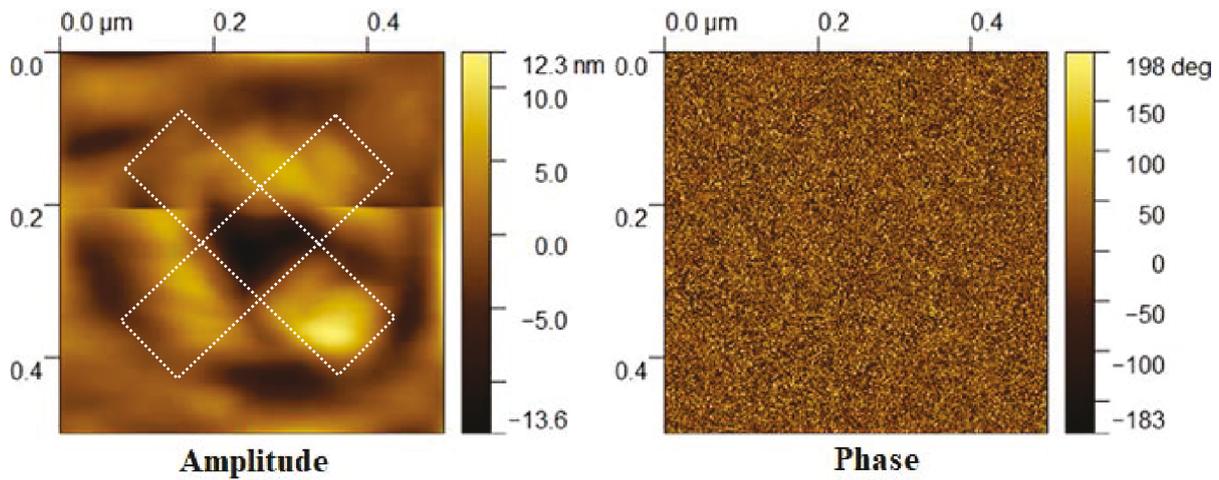


Figure 5-23 Attempt to write a crossbar (dotted area) on top of a UV processed sample with resonance frequency of 278 KHz. Z Sensor and phase does not show any ferroelectric domains. Surface of the sample seems to be damaged due to increasing tip bias voltage to 4 V.

The measured layer is thin (~ 5nm), therefore applying high voltages, induces high currents which can change topography of the layer by moving atoms and deform the surface. In figure 5-23, an attempt was done to write a crossbar (dotted area) by applying +4 and -4 volt to the tip respectively for each strip of crossbar. In PFM images, domains oriented in opposite directions should yield the same amplitude, but the phase should shift by 180° if the layer is ferroelectric. What is expected to be observed is schematically shown in figure 5-24 for amplitude and phase.



Figure 5-24 (Left) Perfect amplitude pattern and (right) phase pattern after writing cross-strips on BTO layer.

This is because polarized domains in opposite directions does not show change in amplitude whereas show 180° contrast in phase.

Results from Silicon-substrate samples were shown above. Despite good crystal quality and smooth surface of the samples, we cannot conclude the presence of the ferroelectricity of the sample after cleanroom processes (UV & E-Beam + Sputtering & liftoff). Lithography

processes above, induce charge and energy to the surface and this can change the property of the very thin layer of BTO.

## 5.2.2 STO-SUBSTRATES

Down to

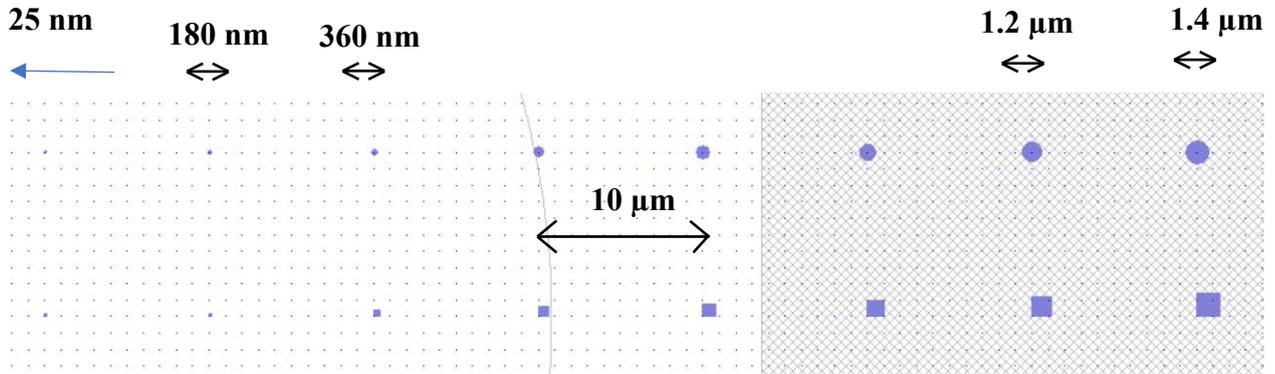


Figure 5-25 - One row of the pattern for e-beam lithography on STO-substrate samples. This is the new internal row pattern inside the outer square framework which was described in figure 5-19. It consists of both squares and circles ranging from 25 nm to 1.4 μm. Again Each row is then written with the different dose pattern shown in figure 5-16 ranging from 800 to 1000  $\mu\text{C}/\text{cm}^2$ .

The pattern used for the e-beam lithography is shown in figure 5-25.

This time electrodes are patterned in both square and circular cross-section area to enabling investigations for different electrode shape and comparing the PFM results regarding this difference. The lateral size of the square and radius of the circles are ranging from 100 nm to 1400 nm which only those ranging from 150 nm upward are shown here. Distance between two adjacent electrodes is 10 μm. Crossbar array which would be fabricated as the final realization of the FTJ device, will have the crosses area in Nano-scale range, therefore in STO-substrate samples, only E-Beam lithography is used.

PFM measurement on off-electrode STO-Based samples demonstrated following results.



Figure 5-26 - E-Beam pattern written with different doses on BTO surface. Pictures taken with optical microscope of AFM machine. Doses are written beside each pattern.

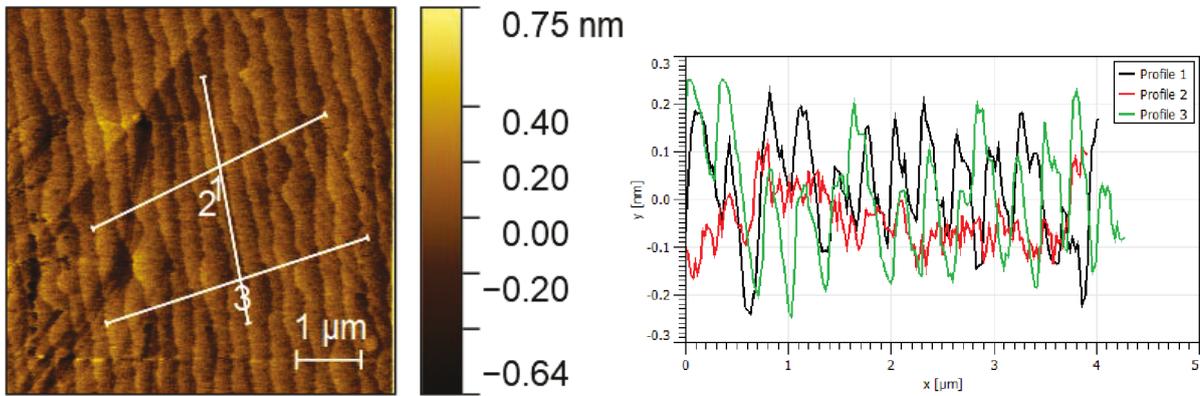


Figure 5-27 - AFM topography (left) & respective line profile (right) bounded between  $\sim -0.3$  to  $\sim 0.3$  nm for cross-terrace and along-terrace. Respective Rms(sq) value is 139 pm.

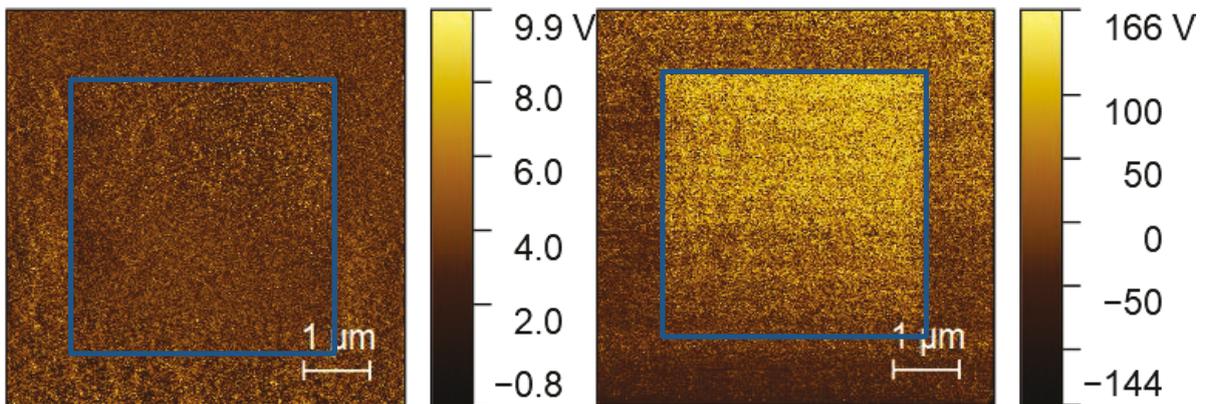
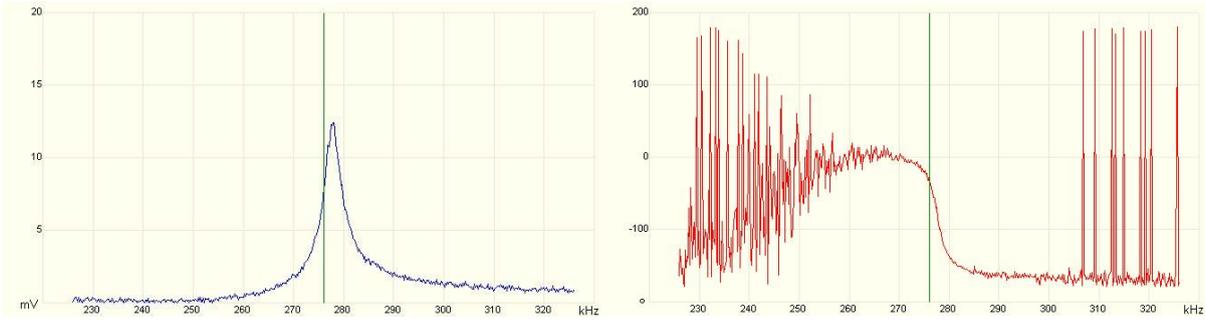


Figure 5-28 PFM topography, amplitude (left), and phase (right). First, the outer  $1 \times 1 \mu\text{m}^2$  square was written with  $+3\text{V}$  tip bias and then the inner  $.5 \times .5 \mu\text{m}^2$  square at  $-3\text{V}$ . Then the whole  $1 \times 1 \mu\text{m}^2$  area was read at  $0\text{V}$ .

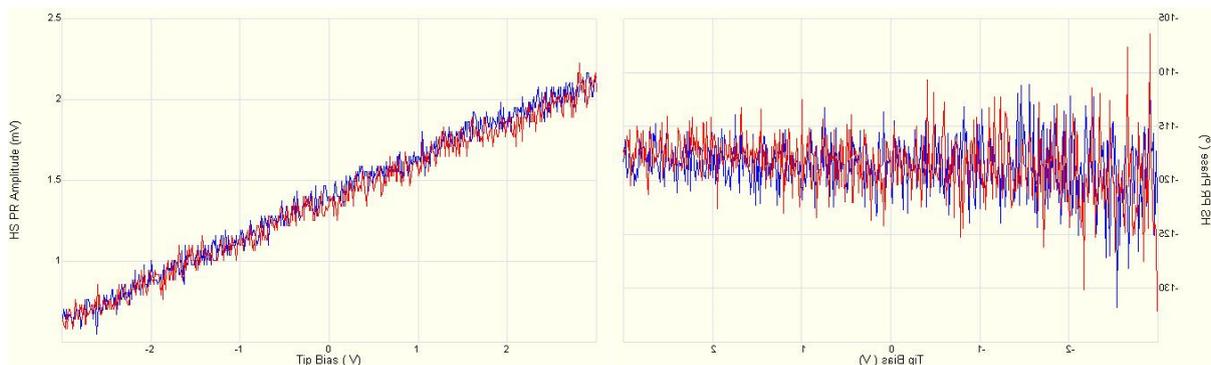
To measure the ferroelectricity, attempt to find the resonance frequency was successful with following results:



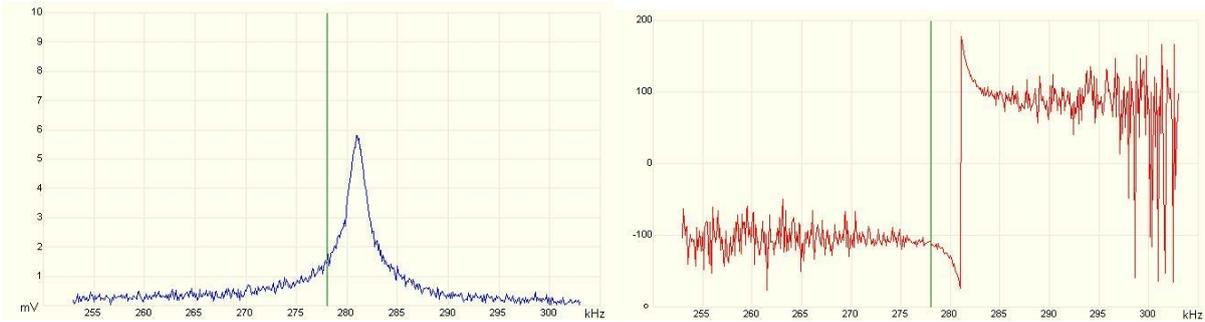
**Figure 5-29 - Resonance frequency found by sweeping contact resonance frequency over the range shown. Left, amplitude and right, phase of the resonant layers. Sweep failed to find resonance frequency for lower frequencies using hard and soft tips. Therefore an attempt with soft tips and in higher frequencies achieved a value of ~ 276 KHz.**

Discussion for figure 5-28 also applies here. In PFM images, domains oriented in opposite directions should yield the same amplitude, but the phase should shift by  $180^\circ$  if the layer is ferroelectric which can be seen here (Note that the principle is the same but poling areas changed from cross shape to nested rectangles).

Second attempt was done later on to investigate more the ferroelectricity on e-beam processed sample. This time ferroelectricity was measured on top of the electrodes and on the surface of BTO. For the locations close to the e-beam patterned area and also on top of the electrodes, no ferroelectric property (Figure 5-30) could be measured despite that the contact resonance frequency was sharply available (Figure 5-31)

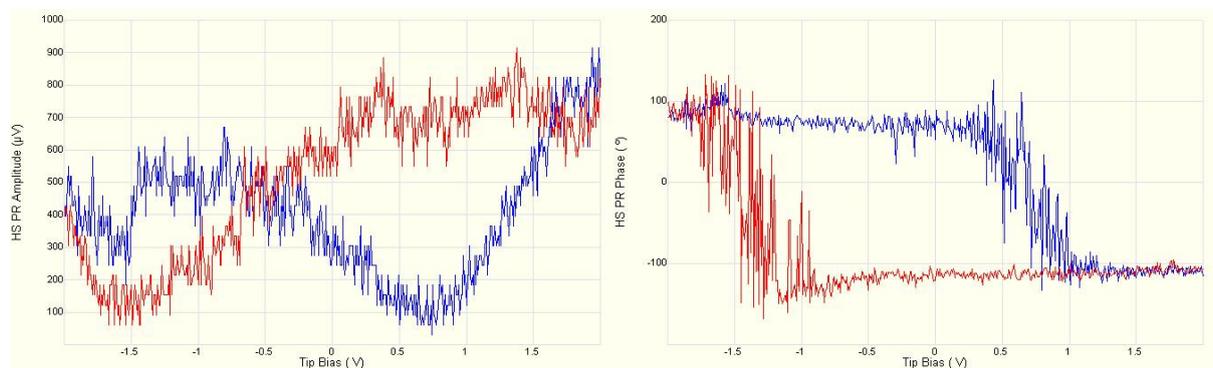


**Figure 5-30 - Amplitude and phase measurement for hysteresis loop on top of electrodes and region near e-beam patterned.**

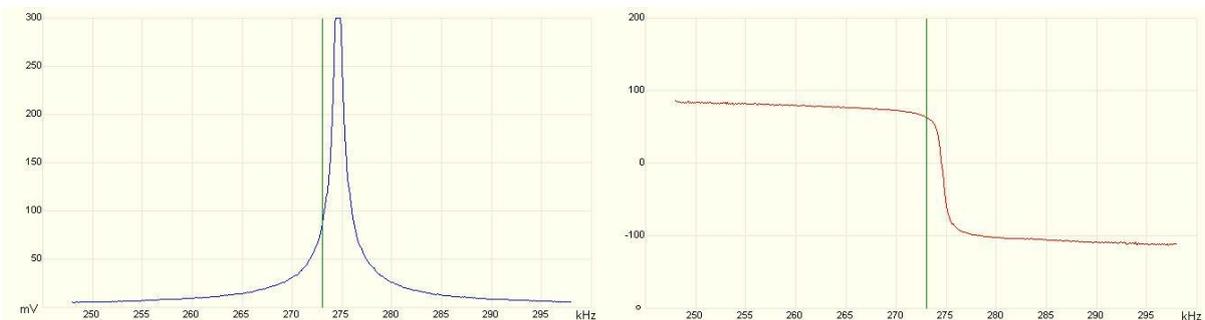


**Figure 5-31 - Contact resonance frequency for the regions near to the e-beam patterned area.**

However measurement for the areas far enough (more than 100  $\mu m$ ) from the e-beam patterns showed ferroelectricity (figure 5-32) with sharp contact resonance frequency (figure 5-33).



**Figure 5-32 - Characteristic ferroelectric hysteresis loop measured by PFM on a BTO/SRO//STO sample.**



**Figure 5-33 - Contact resonance frequency for the regions further than 100 micron from the e-beam patterned area.**

Ferroelectricity is not conclusive from the images. This indicates that E-Beam processed STO-Substrate samples does not show ferroelectricity after cleanroom processes. Some literatures have reported the effect of E-Beam current (and not energy) on the polarization of PZT domains [Li et al]. Meanwhile, an electron beam possess charge and energy which can be absorbed by the layer. This can potentially pole films (change the ferroelectric domain structure). Electron beam poling has been used for purposely poling and modifying ferroelectric thin films [Lu et al]. Fabrication of very small lithographic structures, implies thin photo resist. Likely charge

and electrons will leak through this thin layer. Therefore, likely and accidentally this may pole/erase the poling.

To test the effect of e-beam lithography on the ferroelectricity of the thin film of BTO, it is planned to pattern a new sample with the same pattern mentioned in figure 5-25. This time PMMA resist will be stripped immediately after patterning therefore, no sputtering will be done. PFM measurement on this new sample will reveal the truth or on contrary falsify our hypothesis. I am not sure if the results will be ready until my thesis defense, if yes, I will update this text and include the results here.

## 5.3 SUMMARY

### 5.3.1 DEPOSITION

Samples grown in both sets were characterized regarding structure (surface morphology, crystalline quality and strain calculation) and function (Ferroelectricity).

RHEED patterns indicate 2D surface growth in both sets, a fact that is confirmed later on by AFM measurement with rms value bounded to 0.3 nm. In fact RHEED and AFM images reveal necessary smoothness of thin films.

PFM measurements indicate that Si-based samples are not ferroelectric whereas the STO-based ones demonstrate ferroelectricity. In pursue for the origin of non-ferroelectricity in silicon based samples, XRD-RSM measurements from two sets are compared regarding strain in BTO layer. Strain values extracted from RSM measurements signaling that tetragonality factor in BTO layer for single crystal samples is 1.6 times (table 5-5) the value for Si-based samples.

Comparing thermal expansion coefficient of silicon ( $\sim 2.6 \times 10^{-6}/^{\circ}\text{C}$ ) with complex oxides like STO ( $\sim 8.7 \times 10^{-6}/^{\circ}\text{C}$ ), shows lower value for silicon. Tensile in-plane strain induced from Si to STO layer, can justify the difference in strain propagated in BTO layer. In fact this in-plane strain reduces the out-of-plane strain required for stabilization of ferroelectricity in BTO.

### 5.3.2 CLEANROOM PROCESS

Si-based samples which processed with UV and E-Beam lithography failed to demonstrate ferroelectric properties. However, STO-based samples which were processed with E-Beam lithography, achieved to show preservation of ferroelectric domains in the regions where patterning was not done.

# 6

## DISCUSSION AND RECOMMENDATIONS

In this chapter results from chapter 5 are reflected upon to make a coherent picture of the work and revisit the goals of the thesis. Meanwhile recommendations for further investigations are given.

### 6.1 REFLECT UPON DEPOSITION RESULTS

Samples grown with an optimized set of fabrication parameters were fully characterized regarding structure and function by RHEED, AFM, XRD and PFM.

In-situ RHEED patterns show 2D flat surface of BTO layer in both sets of samples (Despite some islands on silicon-based samples), a fact that was confirmed by AFM measurements indicating average surface roughness below 0.3 nm. Smooth surface in thin films of ferroelectrics is a basic must to provide necessary condition for functionality of the films. Otherwise rough thin film cannot be used for further processes to fabricate crossbar array of FTJs.

PFM measurements revealed that silicon-based samples are not ferroelectric whereas STO-based samples are. Ambiguity of PFM measurements was resolved by confirmation of the results via ULPEC collaborators in Zurich. Ambiguity in PFM measurements is discussed in this chapter in section 6.3.

Couple scans of HRXRD, demonstrated shift of the peaks for all the layers of films in both samples. Shifts in silicon-based samples were lower than respective layers in STO-based samples. More shift, results to more extension in out-of-plane lattice parameter. This more strain can stabilize the ferroelectricity in BTO layer.

To have a deeper look into properties of the layers, strain studies was done with both theoretical and experimental approaches. In theoretical approach, pseudomorphic, epitaxial growth of layers was assumed and strain in layers was calculated. In experimental approach, HRXRD-RSM measurements were done and strain in layers were extracted from measurement results. As we see in Table 5-3, for STO-based samples, values from two approaches are very close to each other and indicating fully strained BTO layer with stabilized ferroelectricity. However for silicon-based samples, it was observed that strain in out-of-plane direction is decreased which has decreased tetragonality of BTO layer (Table 5-4). Values in table 5-5 indicate that

Tetragonality factor for BTO layer in STO-based samples is 1.46 times in bulk BTO. Meanwhile silicon had increased this factor by 51%. If we simply assume that ferroelectricity is proportional to the strain in BTO layer, then functional characterization by PFM measurements also support the results from RSM measurements.

In next step, an effort was done to find the potential origin of difference in strain values in BTO layer of two sets. By a calculation, it was shown that silicon thermal expansion coefficient likely reduces out-of-plane strain.

## 6.2 REFLECT UPON CLEANROOM RESULTS

First samples were fabricated with the pattern shown in figure 5-18. Samples were not ferroelectric therefore naturally no ferroelectricity was observed after UV lithography. It is aimed to grow nanoscale top electrodes on BTO layer, therefore e-beam lithography was applied in rest of the samples including STO-based samples.

As it was shown in section 5.2.2, e-beam processed samples could not reveal ferroelectric property. This can lead us to focus on the resist thickness, e-beam energy and respective development process as the main factors for changing ferroelectricity of samples during UV lithography. Electron beam deposits charge and energy which can potentially pole films (change the ferroelectric domain structure). Fabrication of very small lithographic structures, implies thin photo-resist through which likely charge and electrons will leak. Therefore, likely and accidentally this may pole/erase the poling.

All Samples processed with e-beam lithography. Despite that samples reveals ferroelectric properties, they fail to expose it after e-beam lithography. As E-Beam has not affected those regions which are far from patterned areas, it signals for electron-beam energy and intensity as the main reason for absence of ferroelectric properties. Focus can be made on energy of e-beam and resist thickness.

## 6.3 HINT ABOUT USING PFM

PFM cannot be known as an unambiguous method for ferroelectric measurement in thin films. As Kalinin et al points out, ionic and electrochemical phenomenon can play a major role in PFM measurements. Hysteresis loop as well as poling measurements are successfully reported even for non-ferroelectric materials e.g. LaAlO<sub>3</sub>/SrTiO<sub>3</sub>, amorphous LaAlO<sub>3</sub>, or transition metal oxides [Scigaj]. Guan et al has proposed a method to unambiguously identify the intrinsic

ferroelectricity in thin films. Ferroelectrics with Fast switching dynamic like BTO and slow switching dynamics like PVDF as well as non-ferroelectrics like  $\text{Al}_2\text{O}_3$  thin films have shown hysteresis loop and poling pattern during PFM measurements.  $V_{ac}$  and  $V_{dc}$  play important role for PFM measurement. In fact for fast dynamic ferroelectrics, hysteresis loop vanishes above a  $V_{ac}$  threshold voltage. Therefore by sweeping  $V_{ac}$ , a specific  $V_{ac}$  can be found for ferroelectrics for which hysteresis loop collapses.

From my point of view, one needs to spend time to learn the underline physics of PFM to be able to steer the device correctly in different situations. One can be trapped in artefacts due to some subsidiary phenomenon like presence of charges accumulated on surface. Lack of knowledge about the interaction between surface and the tip can emerge wrong deductions. Although equipment available in the IMS lab (Bruker Icon) is not optimized for performing advanced PFM at ambient conditions, recently new features and optimizations are added to enable the device for this kind of sensitive measurements. The results might be enhanced if using new prospective features.

Meanwhile, by consulting with some of colleagues, devices with contact resonance frequency tracking systems, can achieve better results. These devices can track the contact resonance frequency and while surfing the surface, change the frequency appropriate to the surface beneath.

## 6.4 RECOMMENDATIONS FOR FURTHER RESEARCH

### 6.4.1 SHORT TERM

- It was achieved to make a relation between amount of strain and the existence of ferroelectricity in STO and silicon samples however it is very qualitative. In first step I suggest to make a reliable relation between these two. It can be achieved by growing thicker layers of BTO on silicon substrates. As ferroelectricity is accumulative, increasing the thickness might help to increase accumulative strain and observe ferroelectricity. Then a quantitative relation can be built upon observed values which may lead to better modeling of ferroelectricity on silicon.
- It was observed that silicon samples demonstrate strain in BTO layer more than in bulk BTO, therefor according to the strain calculations, the next step could be considered as the investigation of layer interfaces and atomic arrangement of samples in a cross-section view. By observing the structure of layers in the interfaces using TEM, one can

gather more information about the properties of layers and get more insight to possible hypothesis like, B-site atom movements in perovskite structures and columnar growth of layers which can propagate through the layers. The latter can lead to the increase of energy required for switching the ferroelectric domains like the growth of layers shown by [Mirzadeh et al](#) below. This can help a lot to find out the origin of non-ferroelectricity in silicon samples.

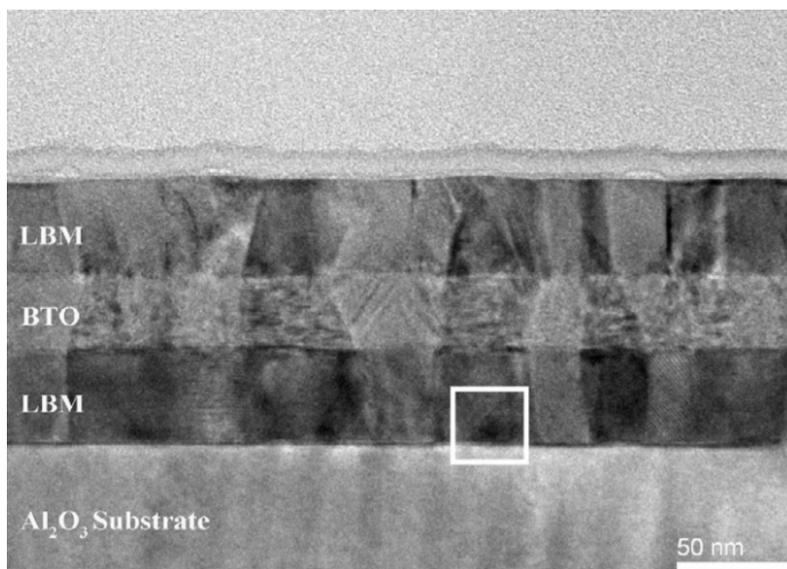


Figure 6-1 TEM micrograph of LBMBT hetero-structure. Columnar growth propagated from LBM layer to BTO layer.

## 6.4.2 MID TERM

- E-Beam lithography affects ferroelectricity in the regions where e-beam is exposed. Domains are affected by the cleanroom process and there is a need for optimization of the parameter set including all the process parameters involving E-Beam Lithography chemicals and developers as well as energy and doses of the electron beams. Thickness of the sputtered electrodes can change the uniformity of the field induced by tip. Therefore, sputtering electrodes with different heights can give more insight to the new investigations. PFM-family measurements (PFM & C-AFM) on e-beam processed samples should be continued to establish a set of reliable de facto methods within IMS. This includes measurements for TER calculation and quality of FTJs.
- TEM images with high-angle annular detector in which the contrast ensues from a high angle scattering strength, gives rise to the so-called Z-contrast imaging (Z being the atomic number). This allows for the easy identification of the BTO, LNO, and STO layers in the low-magnification STEM image which can help to distinguish high quality

and the epitaxial relationship of the hetero-structures and investigations of the quality of interfaces between the layers regarding existence or absence of intermixing or Nano-precipitates [Scigaj].

### 6.4.3 LONG TERM

- Then, after establishing a steady method for patterning with e-beam lithography and achieving samples with ferroelectric properties, electrical properties of the sample can be measured by applying voltage and measuring tunneling currents through the sputtered electrodes and measuring the TER values.
- Designing and Nano-fabrication of early-stage FTJ device, rather than simply electrodes, can be the next necessary step toward the fabrication of cross-array of memristors. This thesis already aimed for fabrication of device however due to time limitation and focus on benchmark system growth, it did not happen. By proper etching of the ferroelectric and bottom electrodes down to substrate and sputtering top and bottom electrodes which can be bond to wires, individual FTJ islands in the range of few 10 nm are fabricated. This way, TER measurements and ferroelectricity investigations can be done within a single device. On the other hand, the road to fabricate crossbar array of memristors which is considered long term or final goal of the ULPEC project, would be opened.

# 7

## CONCLUSIONS

In this work, integration of functional-oxide perovskites on silicon is investigated by means of structural and functional characterization of FTJ layers. A canonical system was built to establish a benchmark for the Si-based samples. By looking into the differences between XRD-RSM results of two sets of samples, it was observed that tetragonality of BTO layer in silicon-based samples is almost 3 times smaller than STO samples. This quantitative result is consistent with functional results of ferroelectricity in STO & silicon samples. Role of the coefficient of thermal expansion (CTE) of silicon was taken into account for justifying the differences. It was shown that CTE can justify the observed difference. Therefore, establishing a quantitative relation between out-of-plane strain in BTO layer and ferroelectricity of BTO is the first key finding of this thesis. Another findings of this thesis was demonstration of ferroelectric property of two sets. In fact the second finding can be summarized as checking existence of ferroelectric property in cleanroom processed samples. It was shown that none of sets demonstrated ferroelectric property after e-beam lithography and sputtering.

The next step for the investigation can be considered as deposition of thicker layers of BTO on silicon substrate. Characterization of cross section of samples with SEM imaging technique and looking into arrangement of atoms in different layers can be done in parallel. This can reveal the role of phenomena affecting the ferroelectricity of samples like columnar growth of layers which was mentioned in recommendation part. Meanwhile, for finding the roots of non-functionality of the samples in both sets after cleanroom process, e-beam lithography should be investigated regarding introducing charge and energy to the ferroelectric layer.

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